RCA REVIEW

a technical journal

RADIO AND ELECTRONICS
RESEARCH • ENGINEERING

Published quarterly by
RCA LABORATORIES
in cooperation with all subsidiaries and divisions of
RADIO CORPORATION OF AMERICA

VOLUME XXIII DECEMBER 1962 NUMBER 4

CONTENTS

RCA REVIEW is regularly abstracted and indexed by *Abstracts of Photographic Science and Engineering Literature, Applied Science and Technology Index, Bulletin Signalétique des Télécommunications, Chemical Abstracts, Electronic and Radio Engineer, Mathematical Reviews, and Science Abstracts* (I.E.E.-Brit.).

RCA REVIEW

AN ANALYSIS OF THE EFFECTS OF REACTANCES ON THE PERFORMANCE OF THE TUNNEL-DIODE BALANCED-PAIR LOGIC CIRCUIT*

BY

JAMES J. GIBSON

RCA Laboratories,
Princeton, N. J.

Summary—The concept of wave scattering is used in an analysis of the balanced-pair circuit. Lead inductances and diode capacitances introduce a delay in the transmission path between the two diodes in the circuit. It is shown that this delay, and not the finite switching speed of the diodes, is the principal factor which limits the speed of the circuit. At the present state of device and circuit technology, the maximum repetition rate at which the circuit can operate reliably with a fan power of four and a sinusoidal clock source is 250 mc. An attempt to optimize the circuit parameters indicates that for a wide range of realistic reactances the optimum peak current is 5 to 15 milliamperes. At this peak current the impedance level is such as to represent a compromise between the speed-limiting effects of lead inductances and diode capacitances.

INTRODUCTION

THE TUNNEL-DIODE BALANCED-PAIR logic circuit is a one-port threshold gate synchronously driven by an a-c source.[1,2] Directionality of the flow of information in a system of these gates can be obtained by driving successive gates with successive phases of a three-phase a-c source. The repetition rate, f, and the stage delay, $1/(3f)$, are consequently determined by the fundamental frequency of the a-c source. Unavoidable reactances determine the highest frequency at which the circuit can operate reliably and with a sufficient logic gain to be useful in a system. The purpose of this paper is to analyze the reactive effects, to estimate the maximum frequency, and to synthesize the circuit for high-frequency operation.

Figure 1 shows the circuit. It is a bridge consisting of two identical tunnel diodes and two identical resistors, r. A balanced d-c and a-c power source, represented by two identical equivalent voltage sources

* Manuscript received April 17, 1962.

[1] First suggested at the RCA Laboratories by Dr. Arthur Lo; French patent No. 1,246,084 January 27, 1960; Belgian patent No. 586,900 January 25, 1960.

[2] E. Goto et al, "Esaki Diode High-Speed Logical Circuits," *I.R.E. Trans. on Electronic Computers*, EC-9, Vol. No. 1, p. 25, March (1960).

$E(t)$ in series with the "source" resistors, r, drives the diodes in the same direction. The logic input signal and the threshold bias, represented by an equivalent current source, I, drive the diodes in opposite directions. The load is represented by an equivalent load resistor, R_L.

At the beginning of the a-c cycle both diodes are in their low-voltage positive-resistance regions and are driven towards their peaks and negative-resistance regions by the a-c power source. The logic input current favors one of the diodes, say diode I, with the consequence that diode I reaches its peak and negative-resistance region before diode II. As diode I goes over its peak, it sends an inhibiting signal to diode II, which, hopefully, reaches diode II in time and with sufficient strength to turn back diode II from its negative-resistance region, over its peak and into its low-voltage positive-resistance region. As diode I enters its negative-resistance region a regenerative process starts, switching diode I to its high-voltage positive-resistance region and

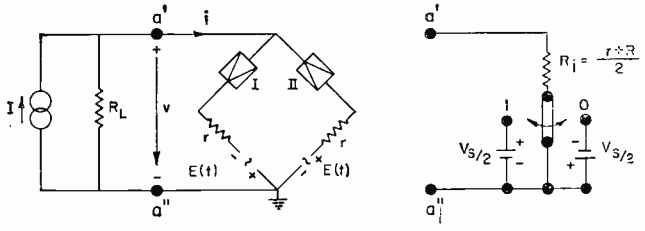


Fig. 1—The balanced-pair circuit and a crude "equivalent" toggle-switch circuit.

driving diode II deeply back into its low-voltage positive-resistance region. As a result, a large output voltage, with the same sign as the small logic input current, is obtained across the load R_L. At a later instant in the a-c cycle, diode I is reset to its low-voltage positive-resistance region, and the process can start over again.

The critical part of the process is the "locking" process which occurs during the small fraction of the a-c cycle when the diodes go over their peaks. The success of the locking process at high source rates, $dE(t)/dt$, depends on the intensity and the speed with which the diodes can communicate with each other over the lossy reactive network made up by the source resistors, the load, and unavoidable reactances. Reactive effects may also cause the circuit to burst into relaxation oscillations, even if the locking process is initially successful. In the subsequent analysis the diodes are considered as "individuals" which communicate with each other by emitting waves which are delayed and scattered by the circuit elements. Before proceeding to this analysis, which is the main topic of the paper, the performance

of the circuit at low frequencies is reviewed. The constraints on the waveform $E(t)$, on the available logic input, and on the required logic output, when the circuit is embedded in a practical system of similar gates, are also discussed. These system constraints are of great importance in a realistic estimate of the speed of the circuit.

Some Design Considerations

Consider a specific example. The tunnel diodes have peak currents $I_p = 10$ milliamperes, the series combination of the resistance of the tunnel-diode bulk material and the external source resistor is $r = 6.5$ ohms, and the load has a resistance $R_L = 50$ ohms. A tunnel diode has

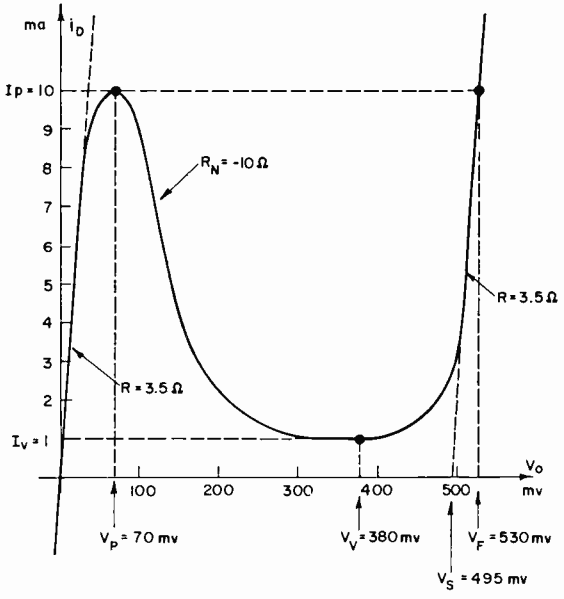


Fig. 2—Current versus voltage characteristic of germanium tunnel-diode with zero bulk resistance.

a current-versus-junction-voltage characteristic as shown in Figure 2. This characteristic is idealized in that the low- and high-voltage positive-resistance regions are linearized to have the same resistance, $R = 3.5$ ohms, over large portions of the characteristic. Some parameters specifying the characteristic are defined in Figure 2.

The current-versus-voltage characteristics seen by the load for various levels of the power source voltage, E, are shown in Figure 3. The load line for a very small logic input current is also shown in Figure 3. The dotted lines in Figure 3 are the nominal end states of

the circuit, i.e., one nominal inactive state when both diodes are low, and two nominal active states when one diode is high and the other low. The nominal end states are defined in the crude equivalent "toggle-switch" circuit shown in Figure 1.

At the beginning of the process E is small and the operating point is close to the origin in Figure 3a. Seen from the load, the circuit in this state is equivalent to a resistance $R_i = (r + R)/2 = 5$ ohms. As E increases, the diodes are driven towards their peaks, and the resist-

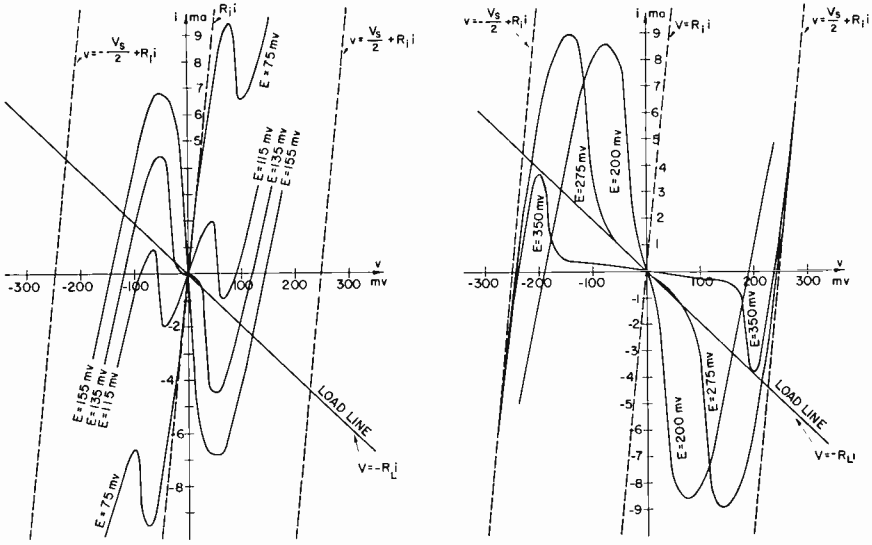


Fig. 3—Current versus voltage characteristics of a 10-ma circuit ($r = 6.5$ ohms) seen by the load for various states of the power source.

ance of the circuit seen by the load increases and becomes infinite at a source voltage

$$E_{\text{lock}} = rI_p + V_p = 135 \text{ mv}. \tag{1}$$

At a slightly larger source voltage, the resistance seen by the load becomes negative and the circuit becomes unstable. At this point a number of events may occur which cannot be predicted from the characteristics in Figure 3. If everything functions as intended, the circuit switches to a stable state, producing a positive or negative output voltage depending on the sign of the logic input current. Once "locked" in one of these states, the circuit is insensitive to variations in the input and the logic input current can be removed. As E continues to increase, the operating point approaches one of the active end states

as shown in Figure 3b. The output voltage and the output current approach the nominal values

$$|V_0| = \frac{R_L}{R_i + R_L}\frac{V_S}{2} = 225 \text{ mv},$$
$$|I_0| = \frac{1}{R_L + R_i}\frac{V_S}{2} = 4.5 \text{ ma}. \qquad (2)$$

If E is increased beyond a certain maximum voltage,

$$E_{\max} = E_{\text{lock}} + \frac{R_L}{R_i + R_L}\left(\frac{V_F - V_p}{2}\right) = 344 \text{ mv}, \qquad (3)$$

both diodes are pulled over their peaks and the operating point switches back to a conditionally stable point at the origin. Under normal operation E must not exceed $E_{\max}$. As E decreases, the operating point moves back towards the origin. At a certain voltage $E_{\min} = 115$ millivolts, which is less than E_{lock}, the operating point becomes unstable and jumps back to the origin. This terminates the process.

The intersections between the load line and the i–v characteristics in Figure 3 give a relation between the output voltage, v, and the source voltage, E. The mushroom-shaped characteristic in Figure 4 shows this relation. Given a waveform $E(t)$ and assuming no reactances in the circuit, the output voltage as a function at time can be determined graphically. This is illustrated with an example in Figure 4.

The success of the locking process depends strongly on the source rate, dE/dt, during locking. If the source rate is too high, both diodes switch before they have time to "notice" each other. Although it is theoretically possible to synthesize a waveform $E(t)$ which varies slowly during the locking process, it is difficult in practice to produce and distribute any waveform other than a combination of d-c and sinusoidal a-c. In a three-phase system of gates with reasonable tolerances on timing and lead lengths of interconnections, it is required[3] that the output pulse be approximately half a cycle wide at the base and have the widest possible flat top. Figure 4 shows that to meet these requirements the d-c bias must be approximately E_{lock}, and the a-c amplitude must be approximately

---

[3] H. S. Miiller and R. A. Powlus, "An Evaluation of Tunnel-Diode Balanced-Pair Logic Systems," *RCA Review*, Vol. XXIII, p. 489, Dec. 1962.

$$\hat{E} \cong E_{\max} - E_{\text{lock}} \cong \frac{R_L}{R_i + R_L}\left(\frac{V_F - V_p}{2}\right). \tag{4}$$

In general R_i is substantially smaller than R_L, with the consequence that the required a-c amplitude is essentially independent of all circuit parameters; it is approximately 200 millivolts for germanium tunnel

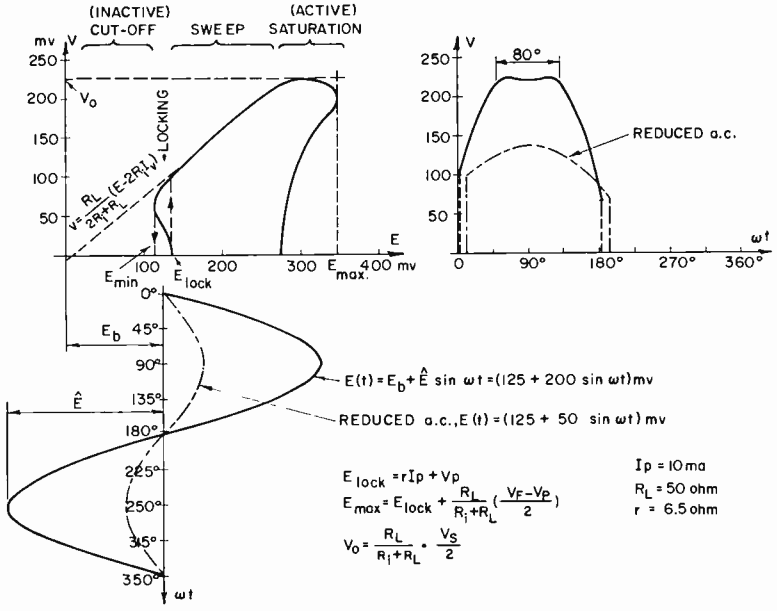


Fig. 4—Cutput voltage as a function of source voltage and as a function of time.

diodes. With these constraints on $E(t)$, the locking process unfortunately occurs when the source rate has a maximum

$$\left.\frac{dE(t)}{dt}\right|_{E_{\text{lock}}} \cong 2\pi f \hat{E}. \tag{5}$$

This relation between the source rate during locking and the frequency is used later for an estimate of the maximum frequency. The source rate can be reduced by reducing the a-c amplitude, but this has the undesirable effect of reducing the amplitude of the output pulse and of rounding the pulse top as shown in Figure 4.

Although it is desirable to draw as much output current as possible from the circuit (theoretically, it is possible to draw a current

$I_p - I_v \cong 0.9\, I_p$), a heavy load reduces E_{max} and consequently also the width of the flat pulse top. To obtain flat-top pulses of nominal amplitude, the largest current that can be drawn from the circuit is between 0.4 I_p and 0.6 I_p. Thus, the load resistance R_L is established within narrow bounds.

The source resistance has a significant influence on the locking process. If r is too large the diodes may not be able to "communicate" with each other with sufficient intensity, with the consequence that both diodes switch. If r is too small the circuit may burst into oscillations. The source resistance also has a significant influence on the pulse shape. If r is increased, the saturation region of the v–E characteristic is increased, which has the desirable effect of widening the flat top of the output pulse. Another important consideration in the choice of r is "systems-noise." In a system, signals are generated by a large number of gates. To prevent these signals from propagating through the system to places where they are not desired, it is important to keep the internal impedance, and consequently r, small.

If all reactances are neglected, the choice of peak current determines only the level of the signals. It is obvious that if all resistances are scaled in inverse proportion to the peak current, the v–E characteristic, and consequently the performance of the circuit, is independent of peak current. Reactive effects, however, have a strong influence on the choice of peak current.

A detailed analysis is required to find an optimum design compromise among fan power, pulse shape, noise, and tolerance requirements on components, sources, and lead lengths of interconnections; such an analysis has been made.[3] The systems constraints are illustrated with only rough figures applicable to the typical circuit used here.

With a source voltage $E(t) = 125 + 200\sin\omega t$ millivolts, output pulses one half cycle wide at the base and with fairly wide flat tops of nominal amplitude are obtained, as shown in Figure 4. The output current is 0.4 I_p. With a fan-in of two and a fan-out of two, the logic input current is 0.1125 I_p. The interconnecting resistors, one in each of the four fan branches, are $R_c = 4R_L - R_i = 195$ ohms, and the voltage attenuation of a signal propagating from a gate to one of its four neighbors is $R_c/R_i = 39$, which is adequate[3] to keep system noise at a tolerable level. With quite tight tolerances on components and sources, it has been estimated[3] that noise, internal imbalances, and input signal fluctuations reduce the effective available logic input current from .1125 I_p to 0.0425 I_p. Keeping in mind the constraints on $E(t)$, on available logic input, and on required output, we can now consider the reactive effects.

The Reactances

Figure 5 shows the circuit with reactances. The diodes in Figure 5 are "ideal" diodes, stripped of bulk resistance and reactances, having current-versus-voltage characteristics as shown in Figure 2. It can be seen from Figure 5 that a signal traveling from one diode to the other

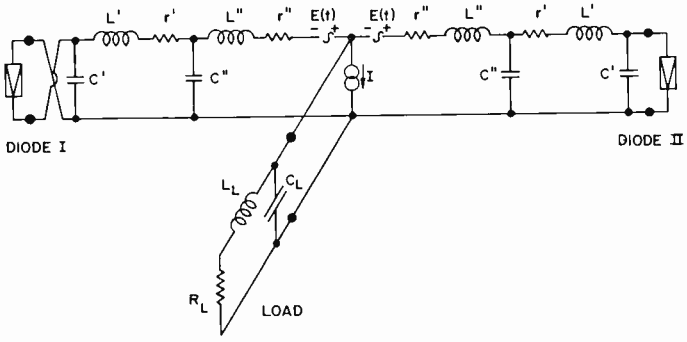


Fig. 5—The balanced-pair circuit with reactances.

encounters many obstacles en route. These are

r' = bulk resistance of the diode,

r'' = external source resistance,

R_L = load resistance,

C' = nonlinear transition and injection capacitance of a tunnel diode. For diodes with peak currents ranging from 5 to 50 milliamperes, C' ranges from 0.5 to 12 pf for voltages below the valley voltage (pf = picofarad = 10^{-12} farad). For higher voltages, C' increases rapidly with voltage. Usually C' is specified at the valley voltage. If C'_v is the capacitance at the valley voltage, V_v millivolts, then it is assumed that the capacitance at the peak voltage, V_p millivolts, is

$$C'_p = C'_v \sqrt{\frac{580\text{-}V_v}{580\text{-}V_p}} \cong \frac{1}{1.6} C'_v$$

C'' = case capacitance of a diode (0.5 to 1.5 pf),

C_L = stray capacitance of the load (0.5 to 1.5 pf),

L' = inductance of a diode (100 to 700 ph),
(ph = picohenry = 10^{-12} henry)

L'' = inductance of a source resistor (100 to 700 ph),

L_L = inductance of the load (> 500 ph).

Mutual inductances between L'_1, L'_2, L''_1, and L''_2 can, for all practical purposes, be represented by equivalent changes in these inductances and in the load inductance, L_L.

Since the circuit in Figure 5 is too complicated for a practical analysis, the following simplifying approximations are made:

(1) The bulk resistance r' is incorporated with the external source resistance r'' to form an effective source resistance $r = r' + r''$. This is justified by the fact that the time constant $r'C''$ is much smaller than other time constants in the circuit.

(2) The stray capacitance of the load, C_L, is uniformly distributed along the load inductance to form a transmission line of characteristic impedance $Z_L = \sqrt{L_L/C_L}$ and delay $\tau_L = \sqrt{L_L C_L}$. This is justified so long as the waveforms entering the load terminal have rise times greater than τ_L.

(3) The junction capacitance C' is assumed to be constant and equal to the junction capacitance at peak voltage C'_p. This is justified for an analysis of the locking process, since both diodes operate in the vicinity of their peaks during locking.

(4) The capacitance $C = C' + C''$ is uniformly distributed along the inductance $L = L' + L''$ to form a transmission line of characteristic impedance $Z = \sqrt{L/C}$ and delay $\tau = \sqrt{LC}$. This is a major approximation which we shall try to justify as we go along with the discussion.

With these approximations the circuit takes the form of the transmission-line model shown in Figure 6. To get a feel for the magnitude of the characteristic impedances and the delays involved in this circuit, it will be assumed that the typical 10-milliampere circuit has the following reactances: $C' = 1$ pf, $C'' = 1$ pf, $C_L = 0.4$ pf, $L' = 200$ ph, $L'' = 200$ ph, $L_L = 1000$ ph, whereby $C = 2$ pf and $L = 400$ ph, and consequently $Z = 14.14$ ohms, $\tau = 28.28$ ps, $Z_L = 50$ ohms, $\tau_L = 20$ ps (ps = picosecond = 10^{-12} second). For all realistic assumptions about the reactances, Z varies between 4 and 40 ohms and τ between 12 and 120 ps.

In the transmission-line model it is convenient to consider all signals as waves. The intensity of a wave at a particular instant and location can be defined as the square root of its instantaneous power. The signal at a diode port can thus be expressed by

$$C = \frac{1}{2}\left(\frac{v_D}{\sqrt{Z}} + i_D\sqrt{Z}\right) = \text{incident wave on the diode in (watts)}^{1/2}, \tag{7}$$

$$D = \frac{1}{2}\left(\frac{v_D}{\sqrt{Z}} - i_D\sqrt{Z}\right) = \text{reflected wave from the diode in (watts)}^{1/2}, \tag{8}$$

where v_D is the voltage across the diode in volts, and i_D the current through the diode in amperes. Given a characteristic impedance Z and the i_D-versus-v_D characteristic of the diode, the reflection properties

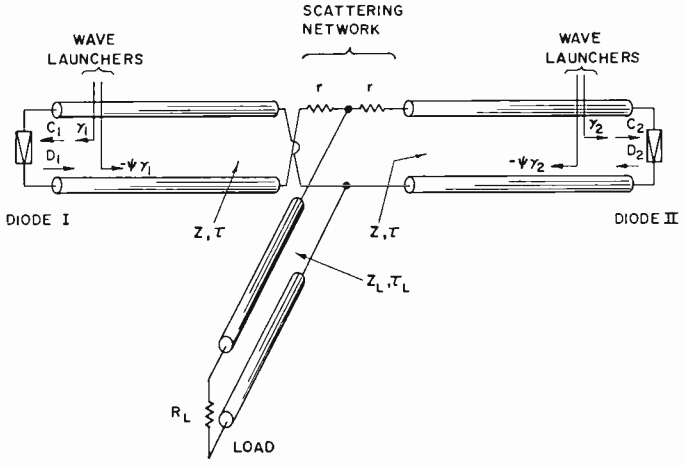


Fig. 6—The transmission line model of the balanced-pair circuit.

of the diode can be represented by a relation.

$$D = \theta(C) = \phi(C) + \psi C, \tag{9}$$

where $\psi = (R - Z)/(R + Z)$ = reflection coefficient of the diode in the linear part of the low-voltage positive-resistance region, and $\phi(C)$ = nonlinear part of the reflection characteristic $\theta(C)$.

The reflection characteristic, $D = \theta(C)$, is the normalized tunnel-diode characteristic $i_D\sqrt{Z}$ versus $v_D/\sqrt{Z}$ inverted and rotated 45° clockwise, as shown for three cases of peak currents and characteristic impedances in Figure 7. The nonlinear part $\phi(C)$ of the reflection characteristic is shown for one of the cases in Figure 8. Figure 7

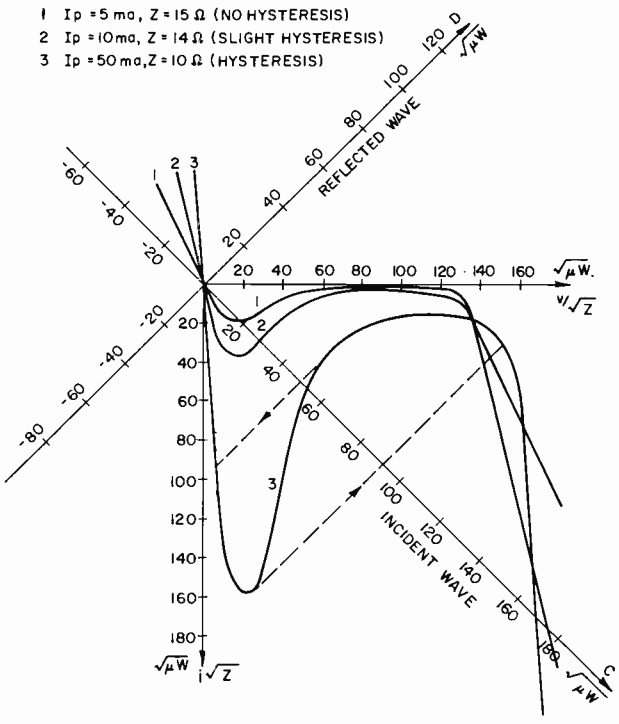


Fig. 7—Reflection characteristics of tunnel diodes.

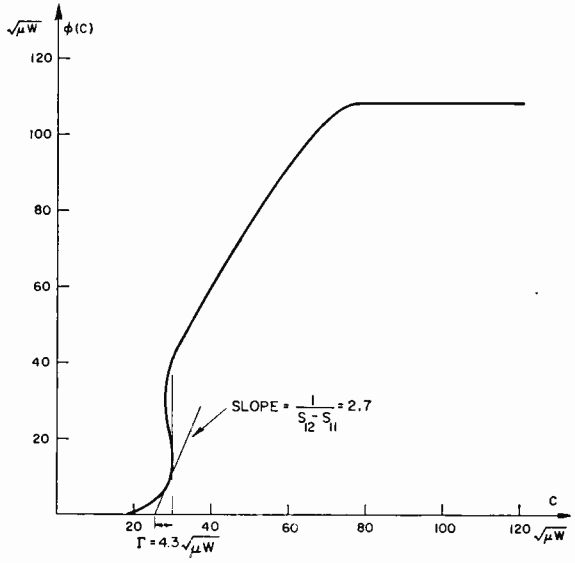


Fig. 8—Nonlinear part of the reflection characteristic of a 10-ma diode with $Z = 14.14$ ohm.

shows that when the peak current and/or the characteristic impedance is large, the reflection characteristic exhibits hysteresis. Hysteresis indicates that whenever the diode is driven to a point in the negative-resistance region where the magnitude of the negative resistance, $|R_n|$, is equal to the characteristic impedance Z of the transmission line connected to the diode, the diode switches infinitely fast along a line $C = \text{constant}$. This means that the region of the characteristic where $|R_n| < Z$ cannot be reached under any circumstances. The property of hysteresis is related in a simple manner to the stability conditions of a voltage-controlled negative-resistance device loaded by a resistor. These stability conditions are indicated in Figure 9. It is seen that whenever $|R_n| < Z$ the system is unconditionally unstable. It is of interest for a justification of the transmission-line model that the stability conditions are the same whether all shunt capacitances are

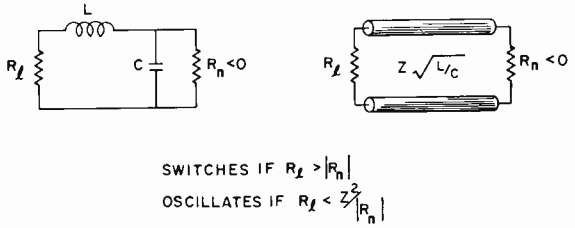


Fig. 9—Stability conditions for a voltage controlled negative resistance.

lumped together at the negative-resistance element or are uniformly distributed along the lead inductance. It should be pointed out that although the stability criteria and the nature of the events which happen in an unstable state are the same for both models, the shapes of the waveforms generated in an unstable state are different. Infinitely fast switching, for example, can obviously not occur in a system with lumped reactances.

In the transmission line model shown in Figure 6, all the sources in the system are represented by equivalent "wave launchers" at the diode ports. This is permissible because of the assumption that the network which interconnects the ideal diodes is linear. To determine the intensity of the wave launchers, let the diodes be replaced by resistances R and let the currents through these resistances be $i(t) + \Delta i$ and $i(t) - \Delta i$, where $2\Delta i$ is the logic input current and $i(t)$ is caused by the power source $E(t)$. If the reactances are small, the current $i(t)$ is approximately

$$i(t) = \frac{E(t)}{R + r}. \tag{10}$$

According to Equation (7) the incident wave on a resistor R caused by its closest launcher is

$$\gamma(t) \pm \Delta\gamma = \frac{1}{2}\,(i(t) \pm \Delta i)\left(\frac{R}{\sqrt{Z}} + \sqrt{Z}\right), \tag{11}$$

which causes a reflected wave $\psi(\gamma(t) \pm \Delta\gamma)$ where

$$\psi = \frac{R - Z}{R + Z}. \tag{12}$$

Consequently all the sources in the system can be replaced by a set of wave launchers $\gamma(t) \pm \Delta\gamma$ directed towards the diodes, and a set of wave launchers $-\psi(\gamma(t) \pm \Delta\gamma)$ directed from the diodes towards the network. The latter cancel the reflected waves from the diode ports when the diodes are replaced by resistances R, thus de-energizing the network which interconnects the resistances R. Consequently, all events which occur in the interconnecting network when the diodes are reinserted, can be attributed to the fact that the diodes depart from being linear resistances.

The events in the system can now be formally expressed. As a simplification, a load resistance R_L is chosen which matches the characteristic impedance, Z_L, of the load port. With this assumption, the incident waves on the diodes at time t are

$$\begin{pmatrix} C_1(t) \\ C_2(t) \end{pmatrix} = \begin{pmatrix} \gamma(t) + \Delta\gamma \\ \gamma(t) - \Delta\gamma \end{pmatrix} + \begin{pmatrix} S_{11} - S_{12} \\ -S_{12} \quad S_{11} \end{pmatrix} \begin{pmatrix} \theta[C_1(t - 2\tau)] - [\gamma(t - 2\tau) + \Delta\gamma]\psi \\ \theta[C_2(t - 2\tau)] - [\gamma(t - 2\tau) - \Delta\gamma]\psi \end{pmatrix}, \tag{13}$$

where S_{11} is the reflection coefficient and S_{12} the transmission coefficient of the resistive pad made up by the source resistors and the load:

$$S_{11} = \frac{r^2 - Z^2 + 2rZ_L}{(r + Z)(r + Z + 2Z_L)},$$

$$S_{12} = \frac{2ZZ_L}{(r+Z)(r+Z+2Z_L)}. \tag{14}$$

The problem is to find the steady-state solution of Equation (13) for periodic sources $\gamma(t)$. However, it is much simpler to find the transient solution assuming that at the beginning of the process the system has recovered from past transients and that the diodes are on the linear parts of their low-voltage positive-resistance regions going towards their peaks under the influence of the wave launchers $\gamma(t) \pm \Delta\gamma$. If the reflection characteristic $\theta(C)$ has no hysteresis, the sequence of events can be completely determined by iteration of Equation (13), given a starting point. If $\theta(C)$ has hysteresis, several starting points must be tested to see where they lead. The iteration process is fairly simple, and some results of such point-by-point calculations are given later. A point-by-point calculation is fine for a final analysis of a given circuit operating under given circumstances. However, to estimate the maximum frequency, f_{max}, and to synthesize the circuit for high-frequency operation, an approximate explicit expression for f_{max} is required.

Locking

The events during locking can be discussed with the help of the simple circuit shown in Figure 6. At the beginning of the cycle, both diodes are low and both are driven towards their peaks by time-varying sources. Let the intensity $\gamma(t) + \Delta\gamma$ of the wave launcher associated with diode I be ahead of the intensity $\gamma(t) - \Delta\gamma$ of the wave launcher associated with diode II by a small amount, $2\Delta\gamma$, determined by the input logic signal. As long as the diodes are on the linear parts of their low-voltage positive-resistance regions, they behave as resistors R, and consequently nothing happens in the network which interconnects them, provided the circuit has recovered from past transients. There is no communication between the diodes and neither one of them knows which is ahead. As diode I enters the nonlinear region around its peak, it sends an inhibiting signal to diode II. This signal is delayed a time 2τ and attenuated by a factor S_{12} before it reaches diode II. In the meantime, diode II enters its nonlinear region. If the source rate $d\gamma(t)/dt = \dot{\gamma}$ is high, diode II may go far into its negative-resistance region before it receives a significant inhibiting signal from diode I. If diode II goes far enough, a regenerative process starts which carries it over the negative-resistance region. After this regenerative process has terminated, it is possible, but not certain, that the inhibiting signal from diode I will reset diode II to a low state.

However, while switching, diode II emits a strong signal, which also may reset diode I to its low state. Thus both diodes may, temporarily, be brought back into their low states, until diode I switches again. This type of relaxation oscillation continues until the source intensity $\gamma(t)$ becomes so large that the diodes can no longer reset each other. These oscillations cause an output consisting of one or many short pulses. Although it is possible for the process to end with diode I high and diode II low, it is more likely to end with both diodes in their valleys. The outcome depends on the shape of the diode characteristics throughout the negative-resistance regions, slight imbalances, slight variations in logic input, and slight variations in the waveform of the power sources. For reliable operation, it is therefore necessary that diode II not go very far into the steep part of its negative-resistance region. Exactly how far it can go is an academic question, since it is exceedingly difficult to manufacture tunnel diodes with tight tolerances on the shape of the negative-resistance region. Furthermore, since the steep part of the negative-resistance region spans a voltage range which is fairly small compared to the total voltage range of the characteristic, the precise limit to which diode II can go is of no practical concern. In terms of the transmission-line model, the incident wave on diode II must not exceed a certain critical value C_{fire}. For diodes with hysteresis, C_{fire} is close to the point where the diode switches unconditionally to a high state. For diodes without hysteresis, C_{fire} corresponds to a state somewhere between the peak and the steepest part of the negative-resistance region.

Given C_{fire}, what is the largest possible source rate $\dot{\gamma}$ during locking? Let t_0 be the instant when diode II is turned back, i.e., when

$$\left.\frac{dC_2(t)}{dt}\right|_{t=t_0} = \dot{C}_2(t_0) = 0.$$

Assume that the source rate $\dot{\gamma}$ is so high, and the curvature of the reflection characteristics in the vicinity of the peaks so sharp, that both diodes are still in the linear parts of their low-voltage positive-resistance regions at an instant $t_0 - 4\tau$. A consequence of this assumption is that the incident waves on the diodes at an instant $t_0 - 2\tau$ are caused only by their own wave launchers.

$$C_1(t_0 - 2\tau) = \gamma_1(t_0 - 2\tau) = \gamma(t_0 - 2\tau) + \Delta\gamma,$$

$$C_2(t_0 - 2\tau) = \gamma_2(t_0 - 2\tau) = \gamma(t_0 - 2\tau) - \Delta\gamma.$$

The incident wave on diode II at the instant t_0 is therefore, according to Equation (13),

$$C_2(t_0) = \gamma_2(t_0) + S_{11}\,\phi[\gamma_2(t_0 - 2\tau)] - S_{12}\,\phi[\gamma_1(t_0 - 2\tau)].$$

Since $\phi(C)$ is a monotonically increasing function of C, as shown in Figure 8, it follows that if $S_{11} > S_{12}$, $C_2(t_0)$ can be negative only if $\gamma_1 > \gamma_2$. Thus, if $S_{11} > S_{12}$, the success of the locking process depends entirely on the magnitude of the logic input signal. Since this signal is small and unreliable, reliable operation requires that S_{12} be substantially larger than S_{11}. When this is the case and when the logic signal is small, the equation for $C_2(t_0)$ can be approximated by replacing γ_2 by γ_1 in the second term on the right, i.e.,

$$C_2(t_0) \cong \gamma_2(t_0) - (S_{12} - S_{11})\,\phi\,[\gamma_1(t_0 - 2\tau)]. \tag{15}$$

Since the source rate is approximately constant for a duration of 2τ, the condition $\dot{C}_2(t_0) = 0$ gives the relation

$$\phi'\,[\gamma_1(t_0 - 2\tau)] = \frac{1}{S_{12} - S_{11}}. \tag{16}$$

The graphical construction in Figure 10 shows that the tangent of the function $\phi(C)$ with a slope $1/(S_{12} - S_{11})$ intersects the C axis at

$$C_0 = \gamma_1(t_0 - 2\tau) - (S_{12} - S_{11})\,\phi\,[\gamma_1(t_0 - 2\tau)]. \tag{17}$$

Consequently, the condition $C_2(t_0) \leq C_{\text{fire}}$ gives the relation

$$\gamma_2(t_0) - \gamma_1(t_0 - 2\tau) \cong \dot{\gamma} 2\tau - 2\Delta\gamma \leq C_{\text{fire}} - C_0 = \Gamma, \tag{18}$$

or

$$\dot{\gamma} \leq \frac{\Gamma + 2\Delta\gamma}{2\tau}, \tag{19}$$

where Γ is defined by the graphical construction in Figure 10.

Equation (19) can be expressed in terms of the circuit parameters. Figure 10 shows that Γ can be expressed as

$$\Gamma = (S_{12} - S_{11})\,\phi\,(\overline{C}), \tag{20}$$

where $\overline{C}$ is close to, but less than, C_{fire}. According to Equations (7), (8), (9), and (14),

$$\Gamma = \frac{Z - r}{Z + r} \cdot \frac{\bar{v}_D - R\bar{i}_D}{\left(1 + \frac{R}{Z}\right)\sqrt{Z}} \tag{21}$$

where $(\bar{v}_D, \bar{i}_D)$ is a point on the tunnel-diode characteristic corresponding to an incident wave $\bar{C}$. Thus $(\bar{v}_D, \bar{i}_D)$ is somewhat closer to the peak than the point on the tunnel-diode characteristic corresponding to an incident wave C_{fire}, i.e., the point to which diode II is allowed to go.

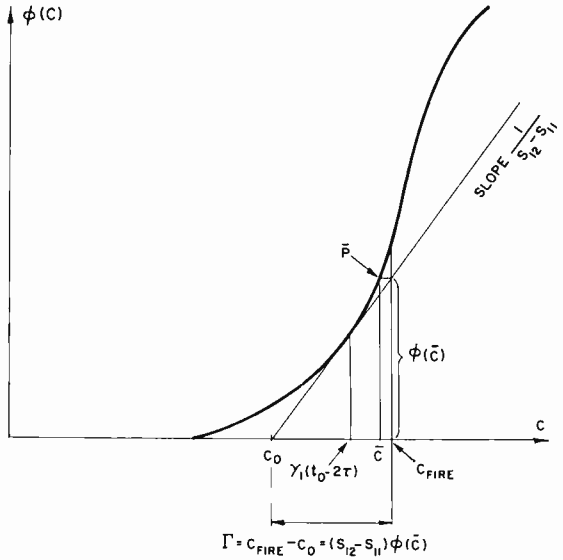


Fig. 10—Graphical determination of the quantity Γ appearing in Equation (19).

If the source voltage E is a periodic function of time with a fundamental frequency f, the source rate during locking is

$$\left.\frac{dE}{dt}\right|_{t=t_0} = 2\pi f \left.\frac{dE(\vartheta)}{d\vartheta}\right|_{t=t_0}, \tag{22}$$

where $\vartheta = 2\pi ft$. According to Equations (10), (11), and (22),

$$\dot{\gamma} = 2\pi f \left.\frac{dE(\vartheta)}{d\vartheta}\right|_{t=t_0} \frac{\left(1 + \frac{R}{Z}\right)\sqrt{Z}}{2(R + r)}, \tag{23}$$

$$2\Delta\gamma = \Delta i\left(1+\frac{R}{Z}\right)\sqrt{Z}. \tag{24}$$

Insertion of Equations (21), (23), and (24) in Equation (19) gives an approximate expression for the maximum fundamental frequency of the a-c source;

$$f_{max} \cong \frac{1}{2\pi \left.\dfrac{dE(\vartheta)}{d\vartheta}\right|_{t=t_0}} \cdot \frac{1}{\tau}\left[\frac{(\bar{v}_D - R\bar{i}_D)(R+r)(Z-r)}{\left(1+\dfrac{R}{Z}\right)^2 Z(Z+r)} + \Delta i(r+R)\right] \tag{25}$$

To illustrate this formula, consider the 10-milliampere circuit discussed earlier, for which $r = 6.5$ ohms, $R = 3.5$ ohms, $Z = 14.14$ ohms, and $\tau = 28.28$ ps. The circuit operates with a sinusoidal a-c, as shown in Figure 4, for which

$$\left.\frac{dE(\vartheta)}{d\vartheta}\right|_{t=t_0} = \hat{E} = 200 \text{ millivolts}.$$

A graphical determination of Γ, carried out in Figure 8, reveals that the factor $\bar{v}_D - R\bar{i}_D$ is 56 millivolts. At the maximum frequency, diode II reaches the critical point of unconditional switching, which is where the negative resistance is equal to $Z = 14.14$ ohms. This is a little further than the point $\bar{v}_D = 89$ millivolts, $\bar{i}_D = 9.5$ milliamperes. Figure 2 indicates the location of this point. The effective logic input current, after all fluctuations are accounted for, is $2\Delta i = .425$ milliampere, as estimated earlier. Insertion of these data in Equation (25) gives

$$f_{max} = f_{crit} + \Delta f = (255 + 60) = 315 \text{ megacycles}. \tag{26}$$

The first factor within the bracket of Equation (25) is independent of the input signal and contributes to f_{crit}, while the second factor is proportioned to the input signal and contributes to Δf. To operate the circuit at a frequency larger than f_{crit}, an input signal is required, while at frequencies below f_{crit}, the circuit can operate with random positive and negative locking without input signal. Equation (26) indicates that even if the input signal is doubled, the maximum frequency increases only from 315 to 375 mc, i.e., 20 per cent. Thus, to

operate the circuit at frequencies substantially larger than f_{crit}, a very large input signal is required, with the consequence that the logic gain becomes so small as to make the circuit useless.

To check Equation (25), the sequence of events in the 10 milliampere circuit has been determined point by point by iteration of Equation (13). Figure 11 shows the incident waves on the diodes as a function of time when the circuit operates at 300 mc. It is seen that diode II is barely turned back before the incident wave reaches C_{fire}. It is also seen that the success of the locking process is established before any fast regenerative process has started. The fact that the signals involved during locking are essentially made up of frequency components at substantially lower frequencies than the cutoff frequency

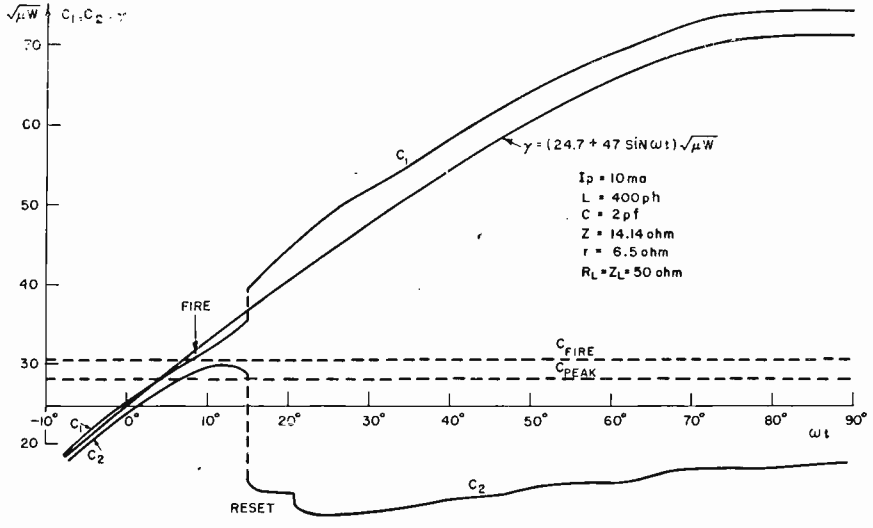


Fig. 11—Incident waves of the diodes in the 10-ma circuit operating with a 300-mc sinusoidal source.

of the actual reactive network, justifies the transmission-line model. Figure 12 shows the output pulse. It begins with a very slow rise during the locking process. The fact that the output during locking is very small justifies the approximation involved in neglecting reflections from the load due to a possible mismatch between R_L and Z_L. Since the diodes in this circuit have hysteresis, diode I switches infinitely fast, causing a sudden jump in the output. With some lumping of the distribution of the reactances, the rise-time of this "jump" will be of the order of magnitude of τ. After the jump, the output hesitates

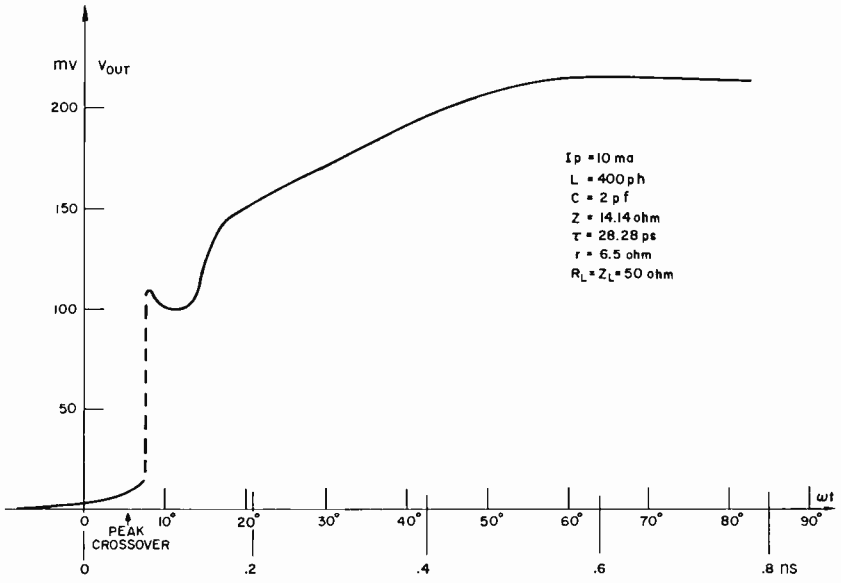


Fig. 12—Output pulse of the 10-ma circuit operating with a 300-mc sinusoidal source.

a little before it approaches a course which can be predicted by the static v–E characteristic in Figure 4.

Figure 13 shows the output when the circuit runs at 400 mc. Both

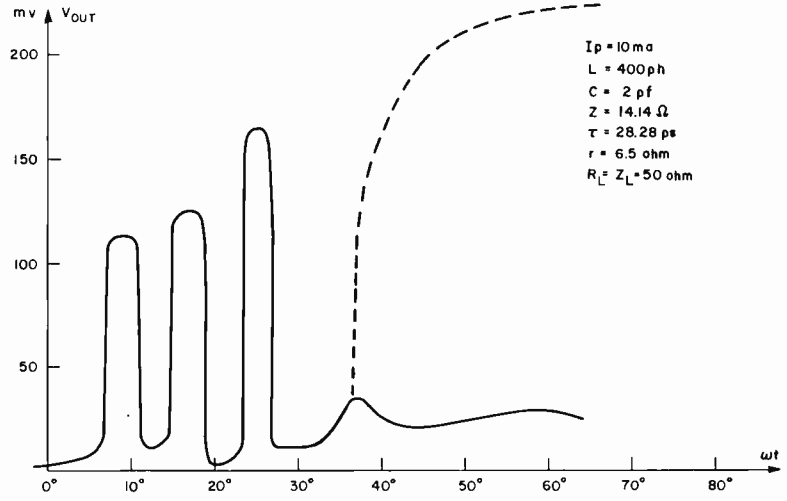


Fig. 13—Output waveform of the 10-ma circuit operating with a 400-mc sinusoidal source.

diodes switch, reset each other, switch again and then, depending on some very touchy conditions, either both diodes remain in their high states with no output (solid line), or diode II is reset with full output (dotted line). The short pulses in the output are typical for this mode of operation. To make the circuit work reliably at 400 mc, the input current must be increased by a factor of 2.4, i.e., to 1.02 milliamperes. In a system of gates with a fan power of four, this is about the maximum available logic input current, and there would be no margin for tolerances and noise. Point-by-point calculations by iteration of Equation (13) thus show that the circuit barely works at 300 mc, and that it does not work at 400 mc. This confirms the estimate of a maximum frequency of 315 mc indicated in Equation (26).

What can be done to increase the maximum frequency? Since not much can be done about the input signal, consideration is given to f_{crit}, which depends on the first term within the bracket of Equation (25). For a given circuit, the only parameter that can be varied is the waveform of the source $E(t)$. With a sinusoidal a-c, the amplitude of the a-c can be reduced to a point where the circuit barely locks and unlocks at the crests of the a-c, and theoretically there is no limit to the maximum frequency. However, the output pulse will be so poor that the circuit would be useless for operation in a system. Figure 4 shows the degradation of the pulse shape in the 10-milliampere circuit when the a-c is reduced by a factor of 4, i.e., from 200 to 50 millivolts, thereby theoretically boosting the maximum frequency from 315 to 1260 mc. Experimentally, balanced pair circuits have operated[3] with reduced a-c at frequencies above 1000 mc.

Another possible way of reducing the source rate during locking is to include harmonics in the a-c source. Figures 14 and 15 show that the 10-milliampere circuit can operate at 1000 mc when the a-c waveform contains 40 per cent second harmonic. The source rate during locking in this case is, in fact, smaller than with a sinusoidal a-c of 300 mc. Figure 14 shows that diode II is turned back before it reaches its peak. Figure 15 shows that the output pulse has a smaller and delayed flat-top region compared to that of the pulse obtained with a sinusoidal drive. Although harmonics in the a-c source definitely help to make the locking process successful, they introduce the practical problem of distributing the composite a-c waveform with precise shape, balance, and level. The tolerance requirements on this waveform and on the d-c bias are very stringent, since it is required that the slowly varying part of the waveform occur during the very short locking interval.

The factor $\bar{v}_D - R\bar{\imath}_D$ in Equation (25) is the only factor which depends on the shape of the tunnel-diode characteristic. It is the voltage

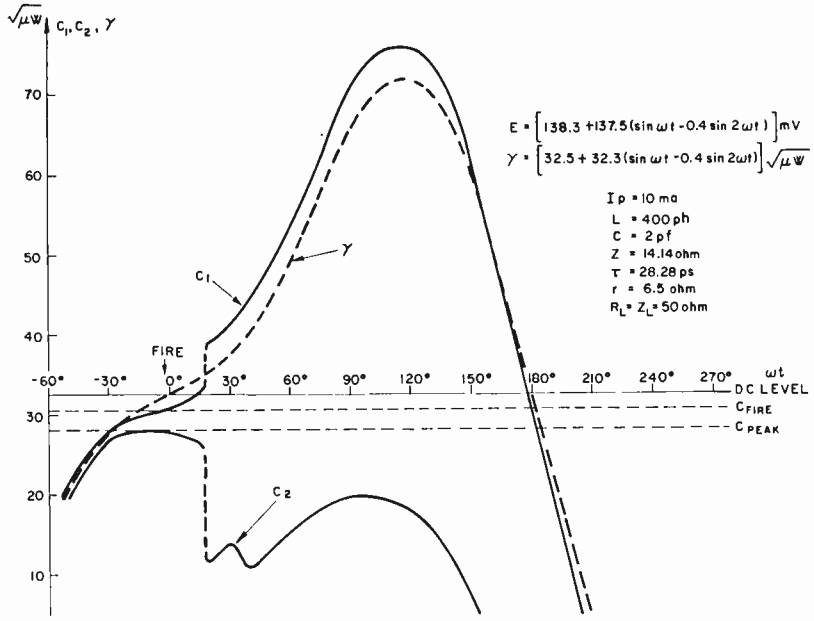


Fig. 14—Incident waves on the diodes in the 10-ma circuit operating with a 1000-mc nonsinusoidal source.

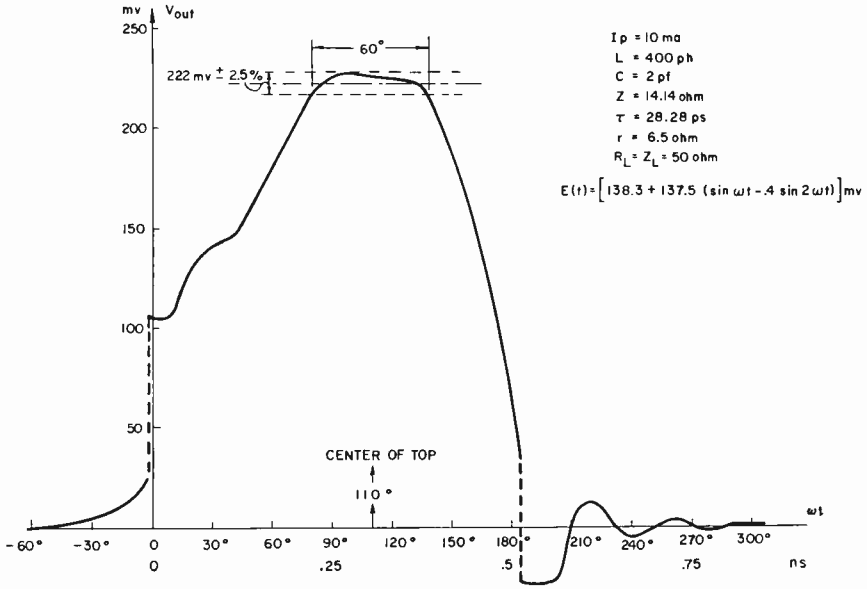


Fig. 15—Output pulse of the 10-ma circuit operating with a 1000 mc nonsinusoidal source.

departure of the point $\bar{v}_D$, $\bar{\imath}_D$ (which is on the negative-resistance region part of the characteristic) from the linear part of the low-voltage positive-resistance region. It is thus a measure of the width of the peak. The point $\bar{v}_D$, $\bar{\imath}_D$, which is close to the point to which diode II may go, is fairly independent of other circuit parameters, and consequently the peak-width factor $\bar{v}_D - R\bar{\imath}_D$ is also fairly independent of the circuit parameters, including the peak current. For the characteristic shown in Figure 2, the peak-width factor varies between 40 and 60 millivolts. The peak width has a significant influence on the locking process. Suppose, for example, that it is zero, which it would be if the characteristic abruptly changed from a positive resistance R to a negative resistance. Then, the maximum frequency would be entirely dependent on the logic input. For the 10-milliampere circuit, the maximum frequency would be only 60 mc! If the peaks are broad, the diodes have more time to "talk" to each other before something drastic happens. One way of obtaining something equivalent to broad peaks, is to drive the circuit "backwards," i.e., to let the process start with both diodes in their high state and let them lock over their broad valley regions. This mode of operation has several disadvantages—it is very difficult to manufacture tunnel diodes with tight tolerances on their properties in the valley- and high-voltage regions; these regions are temperature and pressure sensitive; the capacitance in these regions can be much larger than at the peaks; and the power consumption of the circuit is very high.

For a circuit operating in the ordinary mode with a sinusoidal drive of sufficient amplitude to produce flat-top output pulses

$$\bar{v}_D - R\bar{\imath}_D \cong 50 \text{ mv}, \quad \left.\frac{dE(\vartheta)}{d\vartheta}\right|_{t=t_0} \cong 200 \text{ mv},$$

and consequently, the critical frequency is

$$f_{\text{crit}} \cong \frac{1}{8\pi}\,\frac{1}{\tau}\,\frac{(R+r)(Z-r)}{\left(1+\dfrac{R}{Z}\right)^2 Z(Z+r)}. \tag{27}$$

The parameters R, $Z = \sqrt{L/C}$ and $\tau = \sqrt{LC}$ are functions of the peak current. For diodes made of the same material, the resistance R varies with peak current as $R = k_R/I_p$. To conform with the characteristic shown in Figure 2, we shall assume that $k_R = 35$ millivolts. The diode capacitance at peak voltage varies with peak current according to the

relationship $C = K_c I_p + C''$. Usually the diode capacitance is specified at valley voltage. According to Equation (4), the valley capacitance is approximately $C_v = 1.6\, K_c I_p + C''$.

With this dependence of R and C on peak current, the critical frequency can be determined as a function of peak current for an optimum source resistance r. This relation is shown in Figure 16 for two cases of inductances, $L = 600$ ph and $L = 200$ ph, and for two cases of diode capacitances, $C_v = .16 I_p + 1$ pf and $C_v = .08 I_p + .5$ pf, where I_p is in milliamperes. Figure 17 shows the optimum source resistance as a function of peak current. Figure 16 shows that the critical frequency

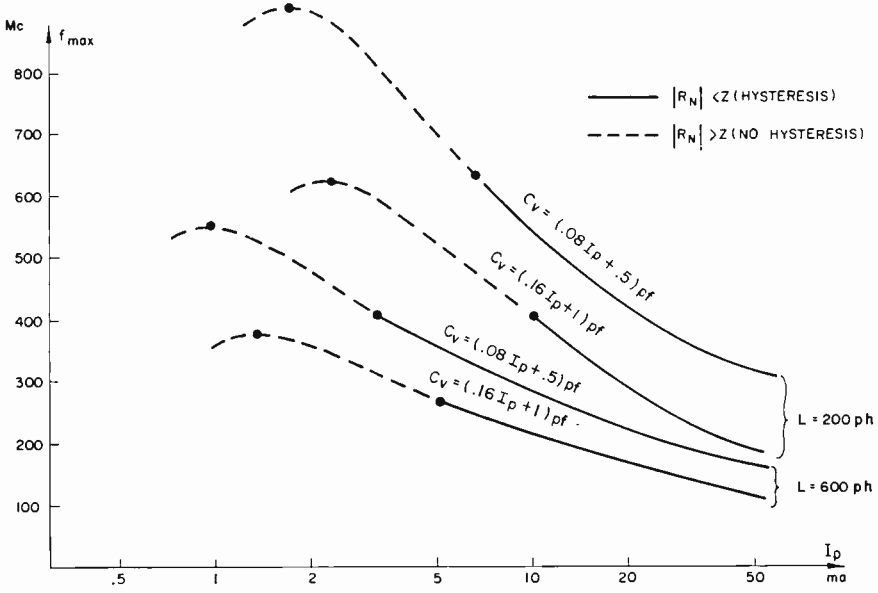


Fig. 16—Maximum frequency versus peak current for optimum source resistance and small input signals.

has a maximum for a rather small peak current. The optimum peak current is roughly $k_R/\sqrt{L/C''}$. The optimum peak current is below 10 milliamperes even for extremely small inductances ($L = 100$ ph), extremely large case capacitances ($C'' = 5$ pf), and extremely large peak voltages ($V_p = 100$ mv, $k_R = 50$ mv). The optimum source resistance for an optimum peak current is always zero, and for a wide range of peak currents and reactances it is below 10 ohms.

Diodes with peak currents in the vicinity of this optimum peak current have case capacitances which are substantially larger than their junction capacitances. Consequently $Z = \sqrt{L/C''}$ and $R = Z$. Since

the magnitude of the negative resistance in the steepest part of the negative-resistance region is approximately $R_n \cong 3R \cong 3Z$, the maximum reflection gain of an optimum peak current diode is approximately

$$\left(\frac{d\theta(C)}{dC}\right)_{\max} = \frac{R_n + Z}{R_n - Z} \cong 2.$$

With such a small gain, the locking process must, in general, span a duration much longer than 4τ, which violates the assumptions on which Equation (25) is based. The validity of Equation (25) and of the curves in Figure 15 are therefore doubtful in the vicinity of the optimum peak current. The performance of circuits with low-gain

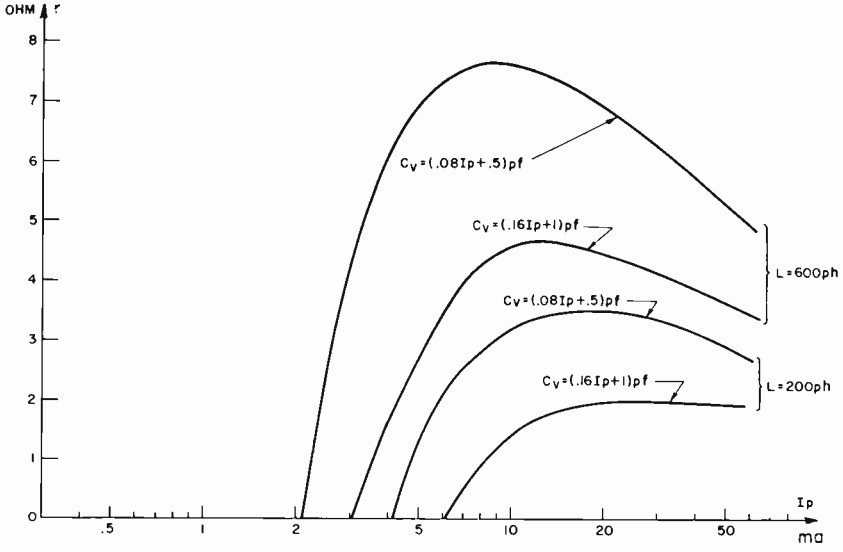


Fig. 17—Optimum source resistance for high locking frequency versus peak current.

diodes must therefore be analyzed with a point-by-point determination of the sequence of events. Consider, for example, a circuit with optimum peak current diodes, zero source resistance, and no load. Let the peak current be $I_p = 1.91$ milliamperes, the capacitance $C = .1I_p + 1 = 1.19$ pf, the inductance $L = 400$ ph, and the logic input current $2\Delta i = .1I_p$. The delay is $\tau = 21.8$ ps and the characteristic impedance is $Z = R = 18.35$ ohms. Figure 18 shows the incident waves on the diodes as a function of time when the circuit operates at 380 mc. It is seen that the locking process, although successful, spans a long duration of

time during which diode II makes several excursions deep into the negative-resistance region (C_{fire} in Figure 18 corresponds to the steepest part of the negative-resistance region). This oscillatory behavio is typical for circuits with small source resistors. Besides being unreliable, this circuit is unrealizable ($r = 0$) and useless ($R_L = \infty$). When the circuit operates with a realistic source resistance $r = 18.35$ ohms and a load $R_L = 200$ ohms, the output pulse is as shown in Figure 19. The circuit can operate at 320 mc with an input current $2\Delta i = 0.076\ I_p$, but does not work if either the frequency is increased to 480 mc or the logic input is reduced to $0.038 I_p$. The rise time is long, the pulse top rounded, and the success of the locking process is sensitively de-

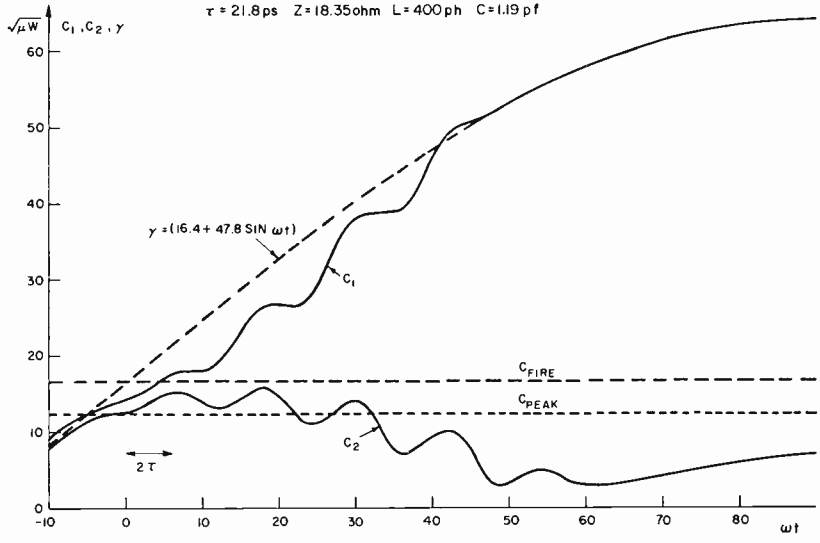


Fig. 18—Incident waves on diodes in a circuit with 1.9-ma diodes, no source resistance, and no load operating with a 380-mc sinusoidal source.

pendent of the logic input. According to Equation (25), the critical frequency for this circuit is zero and the maximum frequency with an input current $2\Delta i = 0.076 I_p$ is only 100 mc, which is much lower than the 320 mc at which the circuit actually can work. Equation (25) is clearly not valid for low-gain diodes. Low-gain diodes are, however, of little interest for high-speed circuits, not only because of poor rise time, strong dependence on logic input, rounded pulses, and sensitivity to the exact shape of the negative resistance region, but also because, for all realistic reactances, the peak current is extremely low with the consequence that the impedance level is impractically high.

For these reasons, a peak current must be chosen which is much larger than the peak current that theoretically gives the highest frequency. Some hysteresis in the reflection characteristic is desirable to secure a fast and reliable locking process and a short rise time. Judging from Figure 15, it appears that for a wide range of realistic reactances, the best compromise is a peak current between 5 and 15 milliamperes. At larger peak currents the impedance level becomes so low that lead inductances limit the speed, while at lower peak currents, the impedance level becomes so high that the diode capacitances limit the rise time. The 10-milliampere circuit is an example of a compromise design. The inductance assumed, $L = 400$ ph, is perhaps

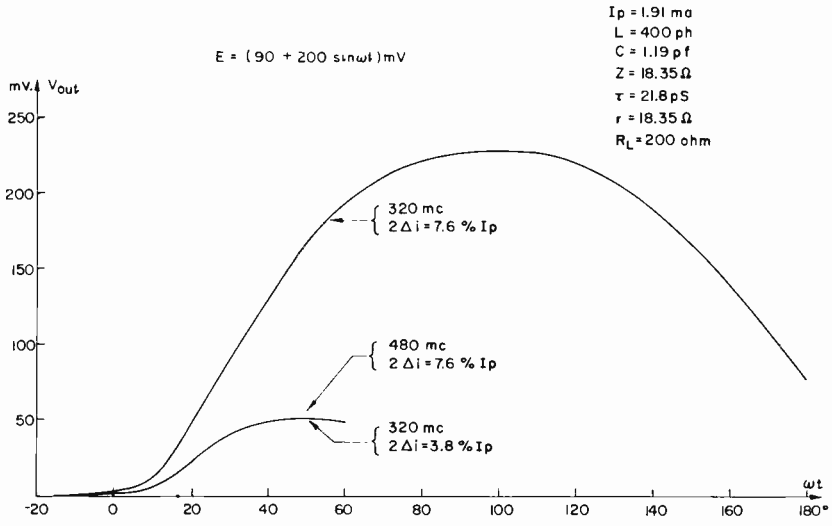


Fig. 19—Output waveforms of a circuit with low-gain diodes.

optimistically small. In reality the inductance is likely to be larger than 500 ph, and the maximum frequency closer to 250 mc than to 300 mc. Although the optimum source resistance for high-frequency operation is, according to Figure 17, about 3 ohms, a larger source resistance ($r = 6.5$ ohms) has been chosen to widen the top of the pulse and to prevent oscillations of a type which are discussed in the next section.

The effect of imbalances can be estimated by perturbation methods. During the locking process, imbalances generate signals which have the same effect as a logic input current, and consequently they "eat up" some of the available input. An estimate of these undesirable

signals is not difficult to carry out, but is a rather lengthy procedure and is not included here. The main conclusion is, as can be guessed, that tolerance requirements are extremely stringent when the circuit operates close to its maximum frequency. The balance of the capacitances and the peak widths of the diodes, which can be expressed in terms of peak-voltage balance, is particularly critical. Peak voltages and diode capacitances must be balanced within less than 10 per cent for a worst-case design. However, it is not realistic to hope that a worst-case-designed circuit can operate at the predicted ultimate speed. Individual adjustments of the threshold bias on the gates appear to be a necessity. Imbalances due to aging are probably small compared to initial imbalances.

Other Reactive Effects

Recovery

The analysis of the locking process in the previous section is a transient analysis based on the assumption that the circuit has completely recovered from past transients at the beginning of the process. When the locking process starts, both diodes have been in the linear part of their low-voltage positive-resistance regions for about half a cycle of the fundamental frequency of the power source. An investigation of the natural complex frequencies of the circuit, with the diodes replaced by resistances R, reveals that for all realistic reactances and all realistic designs of the circuit, the circuit has recovered within half a cycle of the maximum frequency at which the circuit can operate with a sinusoidal a-c. Thus, in a properly designed circuit, recovery is not a problem. If the frequency is boosted by using harmonics in the a-c waveform, recovery may become a problem. Also, if the inductance in the load is exceptionally large, $L_L > 10$ nh (nh = nanohenry = 10^{-9} henry), the circuit may not recover. Whatever is left of the output current in L_L when the process starts anew, acts as a logic input current. This may cause alternate positive and negative locking of the circuit.

When the circuit produces an output of the same sign for a long duration of time, it is possible that a bias can build up, either by thermal imbalance of the diodes or by "d-c buildup" in the power-distribution system. With some care in the choice of diodes and in the design of the power-distribution system,[3] such bias buildup can be limited to a tolerable level.

Self Resetting

Occasionally it is found that the diode which initially switches will

reset itself. This phenomenon may occur even at low source frequencies if the source resistance is small and the lead inductances are large. It can be discussed with the help of the transmission-line model shown in Figure 6. Let diode I be favored by the logic input. Let the locking process be successful, and let diode I switch. A strong wave of intensity A is emitted from diode I at the switching instant t. At an instant $t + 2\tau$ diode I receives a reflected wave $S_{11}A$. If S_{11} is negative, which it is if $r(r + 2Z_L) < Z^2$, this reflected wave can be strong enough to reset diode I. Even if it is not strong enough to reset diode I, it will cause an undesirable oscillatory behavior of the switching process. In a properly designed circuit, the source resistance and the load should be chosen so as to make $S_{11} > 0$, i.e., $r(r + 2Z_L) > Z^2$. The 10-milliampere circuit satisfies this condition. Even when $S_{11} > 0$, self-resetting may occur. The strong wave A, emitted by diode I, is also transferred through the resistive pad, reaches diode II, drives it deeply back into its low-voltage, positive-resistance region, is reflected by diode II, goes back through the pad, and reaches diode I at an instant $t + 4\tau$ with an intensity $\psi S_{12}^2 A$. If ψ is negative, which it generally is, this wave may be strong enough to reset diode I. To avoid this kind of self-resetting, S_{12} and $|\psi|$ must not be too large. This means that the source resistance must not be too small and the peak current must not be too large. An exact criterion for avoiding self-resetting is difficult to derive, because it depends on the shape of the characteristic throughout the negative-resistance region. A sufficient condition is that $S_{11} + \psi S_{12}^2 > 0$. The 10-milliampere circuit satisfies this condition when the source resistance is 6.5 ohms, but not when the source resistance is 3 ohms, which is theoretically the optimum for high-frequency operation. The choice of source resistance is thus a compromise between the desire to have low attenuation in the communication path between the diodes to secure locking and high attenuation to prevent self-resetting. After self-resetting a new and usually unsuccessful locking process starts. Self-resetting may also repeat a few times.

Self-resetting occurs more readily at low frequencies than at high frequencies. At high frequencies the source may drive diode I so far into its high-voltage positive-resistance region before the reflected wave comes back, that the reflected wave cannot reset the diode. Thus, it is possible that a circuit may work at high frequencies but not at low frequencies.

Switching Speed

In the transmission-line model, diodes with hysteresis switch infinitely fast. This is an obvious misrepresentation of reality. If all

the capacitance of a diode is lumped at the junction, the rise time of the voltage transient across the diode when it switches from a low-voltage stable bias V_L to a high-voltage stable bias V_H is

$$\tau_r \cong C_v \frac{(V_H - V_L)}{(I_p - I_v)},$$

where τ_r is in nanoseconds, C_v in picofarads, V_H and V_L in volts, and I_p and I_v in milliamperes. For germanium tunnel diodes with I_p/C_v ratios between 5 and 10, the rise time of the voltage transient across the diode is between 0.1 and 0.05 ns. Thus, as long as the frequency of the a-c source driving the balanced pair circuit is less than 300 mc, which is roughly the maximum frequency at which the circuit can operate reliably with a sinusoidal a-c, this rise time is much less than 1/4 of the cycle time. Consequently, even with a lumped model of the circuit, the finite switching speed of the diodes does not have a significant influence on the pulse shape.

The finite switching speed of the diodes may, however, have a significant influence on the performance of circuits operating at much higher frequencies, which is theoretically possible with a nonsinusoidal a-c source. The pulse shape shown in Figure 14 for a circuit operating at 1000 mc is unrealistic because, in reality, the rise-time takes a good portion of 1/4 of a cycle.

In circuits with diodes which do not have hysteresis, which in practice means diodes with small peak currents, the switching process is slow, with the consequence that the pulse shape should be about the same when computed with the transmission line model as with a lumped model.[4]

It is concluded that, in general, the finite switching speed of the diodes, measured in terms of their I_p/C_v ratios, is not the principal factor that limits the speed of the balanced-pair circuit.

Conclusions

At the present state of device and circuit technology, the maximum repetition rate, f_{max}, at which the balanced pair circuit can operate reliably with useful output pulses, a total fan power of four, and a sinusoidal clock-source, is approximately 250 mc. As the frequency is increased beyond f_{max}, the outcome of the switching process depends

[4] G. B. Herzog, "Tunnel-Diode Balanced-Pair Switching Analysis," *RCA Review*, Vol. XXIII, No. 2, p. 187, June (1962).

on a large number of uncontrollable factors such as the oscillatory behavior of the circuit; the exact shape, level, and frequency of the power source; the balance of the reactances; and the exact shapes of the characteristics of the tunnel diodes throughout their negative-resistance and valley regions. To operate the circuit reliably at a frequency substantially larger than f_{max}, a large logic input signal is required, with the consequence that the logic gain becomes so small as to make the circuit useless.

With a three-phase clock source, the stage delay at a clock-frequency of 250 mc is 1.3 ns, which is an order of magnitude larger than the rise-time (transition time) of the junction voltage of a high-speed tunnel diode switching from a low-voltage state to a high-voltage state. The basic reason why the balanced pair circuit is so slow compared to the speed capability of tunnel diodes is that the success of the switching process depends on the communication between the two diodes during the small fraction of the a-c cycle when the diodes are driven over their peaks. Lead inductances and diode capacitances introduce a delay in the transmission path between the diodes. This delay, and not the finite switching speed of the diodes, is the principal factor which limits the speed of the circuit. At the present state of device and circuit technology, this inter-diode path delay is only a few hundredths of a nanosecond, which is the time it takes light to travel a fraction of an inch in free space. The fact that such a small delay is the main factor that limits the speed of the circuit indicates that microminiaturized integrated circuit techniques are required to increase the speed of the circuit significantly. However, heat dissipation is already a problem with the present "large" packaging of the circuit, and consequently heat will put a limit to the extent the circuit can be miniaturized. Therefore, it does not seem likely that improved technology could significantly improve the speed of the circuit. To generalize a little, it appears that because of unavoidable path delays, a switching circuit intended for kilomegacycle speed must not depend on the interaction between two devices, as the balanced-pair circuit does.

By introducing harmonics in the a-c source in such a manner as to slow down the source rate during the time when the diodes are driven over their peaks, the repetition rate can theoretically be increased to a point where factors such as the finite switching speed of the diodes, ringing, and recovery limit the speed of the circuit. It has been estimated that with a-c containing a second harmonic, the circuit could operate at a repetition rate three times larger than with sinusoidal a-c. However, the method of introducing harmonics in the a-c, besides degrading the pulse shape somewhat, introduces the practical problem

of distributing the composite a-c waveform with precise balance, shape, and level. It appears to be difficult to use such a composite a-c clock-source in a practical system.

The repetition rate can also be significantly increased at the expense of the shape and amplitude of the output pulse by operating the circuit with a sinusoidal a-c of less than "nominal" amplitude. This conclusion is confirmed by the experimental fact that balanced-pair circuits have operated up to 1200 mc.[3] However, tolerance requirements on components and sources are already very stringent in a system operating with "nominal" a-c amplitude.[3] By reducing the a-c amplitude and degrading the pulse shape, the tolerance requirements become impractical. Thus, it does not appear that the method of increasing the repetition rate by reducing the amplitude of the a-c could be used in a practical system.

The reactances have their most significant influence on the performance of the circuit during the locking process, which occurs during the small fraction of the a-c cycle when the diodes are driven over their peaks. Their effects during the remaining part of the a-c cycle have, in general, a minor influence on the performance of the circuit. Reactive effects such as ringing, recovery, oscillations, limited switching speed, thermal unbalance and d-c buildup during repetitious switching can be kept under control with some care in the design of the circuit, the interconnections between circuits, and the power distribution system.

Attempts to optimize the parameters of the balanced-pair circuit indicate that for a wide range of realistic reactances the optimum peak current is between 5 and 15 milliamperes. At higher peak currents, the impedance level of the circuit is so low that lead inductances limit the speed, while at lower peak currents the diode capacitances limit the speed. This result, which indicates that a maximum speed is obtained at an impedance level that represents a compromise between the speed-limiting effects of capacitances and inductances in devices, components, and interconnections, may be of interest for the design of high-speed circuits and systems in general.

AN EVALUATION OF TUNNEL-DIODE BALANCED-PAIR LOGIC SYSTEMS

BY

H. S. MIILLER AND R. A. POWLUS

RCA Laboratories
Princeton, N. J.

Summary—The major problems that thus far have limited applications of tunnel-diode circuits in computers are those of distribution of power supply voltages, packaging, subsystem fabrication techniques, and system tolerances. This paper presents experimental and analytical results obtained in an exploratory program to determine, in relation to the above problems, the applicability of tunnel-diode balanced-pair circuits as building blocks for high-speed computers.

Part I discusses solutions to the first three of the above problems and presents experimental results obtained from operating balanced-pair circuits with sinusoidal power supplies having a frequency (repetition rate) range of 100 mc to 1 kmc. These power supplies have, in addition to the a-c component, a d-c component which is used for biasing purposes. Two basic power distribution techniques are described. These techniques were employed in scale-of-two counters operating at both 150- and 450-mc repetition rates and in two, three-bit end-around shift registers operating at 150-mc repetition rates. The fabrication technique used in one of the shift registers, which is suitable for small systems, is also described.

Part II deals with the problem of system tolerances, which remains as the limiting factor in the application of tunnel-diode balanced-pair circuits for high-speed computers.

PART I—POWER SUPPLY, PACKAGING AND SUBSYSTEM FABRICATION

INTRODUCTION

TUNNEL-DIODES are being considered as prime candidates for high-speed computer applications due to their high cutoff frequency, simplicity, and stability.[1-5] The major problems which have thus far limited applications of tunnel-diode circuits in

[1] L. Esaki, "New Phenomenon in Narrow Germanium p-n Junctions," *Phys. Rev.*, Vol. 109, p. 603, January 15, 1958.

[2] H. S. Sommers, "Tunnel Diodes as High-Frequency Devices," *Proc. I.R.E.*, Vol. 47, p. 1201, July, 1959.

[3] R. Trambarulo and C. A. Burns, "Esaki Diode Oscillators from 3 to 40 kmc," *Proc. I.R.E.*, Vol. 48, p. 1776, October, 1960.

[4] M. H. Lewin, "Negative Resistance Elements as Digital Computer Components," *Proc. E.J.C.C.*, Boston Mass., p. 15, December 1-3, 1959.

[5] J. A. Rajchman. "Solid-State Microwave High-Speed Computers," *Proc. E.J.C.C.*, Boston, Mass., p. 38, December 1-3, 1959.

computers are those of distribution of power supply voltages, packaging, subsystem fabrication techniques, and system tolerances. The purpose of this paper is to report results obtained in an exploratory program to determine, in relation to the above system problems, the applicability of a particular class of tunnel-diode circuits, the balanced-pair circuits, as building blocks for high-speed computers.

A logical building block must provide a functionally complete set as well as meet electrical requirements of signal amplification and standardization. As logical decision rates (the reciprocal of the time required to perform a logical decision) increase, building-block requirements, particularly those of physical size and reliability, vastly increase. Geometrical positioning and logical versatility of high-speed (0.5-nanosecond stage delay) computer building blocks are extremely important since the delay in a wiring path four inches long is equivalent to one stage delay. Due to these constraints, system organization is no longer separable from geometrical problems.

Tunnel-diode balanced-pair circuits amplify and standardize signals each time a logical decision is made, and are, in principle, capable of 11 separate logical functions in addition to amplification. They are of small size (3×10^{-2} cubic inch) and low in power consumption (on the order of 50 milliwatts). These properties qualify balanced-pair circuits for consideration as high-speed computer building blocks.

A balanced-pair circuit is basically a pair of matched tunnel-diodes and matched power supplies arranged in a symmetrical configuration giving a one-port circuit which is capable of both positive and negative output pulses. Logical directivity is obtained by using a multiphase power supply system. A balanced-pair majority circuit[6] uses two opposite nodes of the symmetric circuit, one of which is common to the two power supplies and the other of which is common to the two tunnel diodes, as input–output terminals. A balanced-pair inverter circuit[7] uses as output terminals the same input–output terminals as the majority circuit. One of the inverter input terminals, which is also an output terminal, is the node common to the two power supplies. The other input terminal is the intersection of two resistors connected in series between the two remaining nodes of the symmetric circuit. Each of these two nodes is common to a power supply and a tunnel diode.

Part I of this two-part paper discusses basic concepts of the two types of balanced-pair circuits, namely, operating principles of both

[6] A. W. Lo. French patent No. 1,246,094 issued January 27, 1960; Belgian patent No. 586,900 issued January 25, 1960.

[7] Interm Research Report No. 7A for High-Speed Data Processor System Research, RCA, Camden, N. J., for the period June 1, 1960 to August 30, 1960, p. 2-2 to 2-4, ASTIA document No. AD 253.919 (11 April 1961).

majority and inverter balanced-pair circuits. Each of these concepts is viewed from purely static conditions. That is, all reactances are neglected and switching is considered to be instantaneous. In addition, Part I describes methods of distributing a-c power-supply voltages to large numbers of balanced-pair circuits, several small experimental subsystems which were constructed to evaluate balanced-pair circuits, circuit packaging, and subsystem fabrication techniques useful for large-scale subsystems. Although fabrication techniques discussed were not evaluated above 450 mc, the concepts employed appear to be extendable to 1-kmc systems.

A discussion of the factors which govern the widths of output pulses of majority circuits, the restrictions on lengths of transmission lines used for logic interconnections between balanced-pair circuits, and of the influence of these factors on the problem of circuit tolerances is contained in Part II. The results of a static tolerance analysis of balanced-pair logic systems are also presented.

Majority Circuit

Majority logic is performed with a linear summation network at the input–output terminals of a majority circuit. Majority circuits discriminate between positive and negative current inputs resulting from the summation, then amplify and produce standardized output pulses. Tolerances permitting, weighted majority logic is possible. The logical AND and OR operations are special cases of the majority operation with a constant reference, either "1" or "0", applied to one or more inputs of the summation network. The effect of this constant reference can be achieved by either initially choosing tunnel diodes with unequal peak or valley currents or unbalancing two matched diodes with a d-c current source applied directly to the input–output terminals.

Principles governing operation of majority circuits will now be described in terms of operating points on tunnel-diode voltage–current characteristics. All reactances are neglected and switching is considered instantaneous.

The schematic diagram of a balanced-pair majority circuit is shown in Figure 1. The two matched power supplies, e_g, each having a sinusoidal waveform with a d-c component, can be varied to give two modes of operation which differ with respect to one another due to relative magnitudes of the d-c component of the power supplies. In mode (a), the d-c component is such that both tunnel diodes are initially in the low-voltage state, with one tunnel diode switching to its high-voltage state: in mode (b), both tunnel diodes are initially held in their high-voltage state by the d-c component of the power supplies, with one

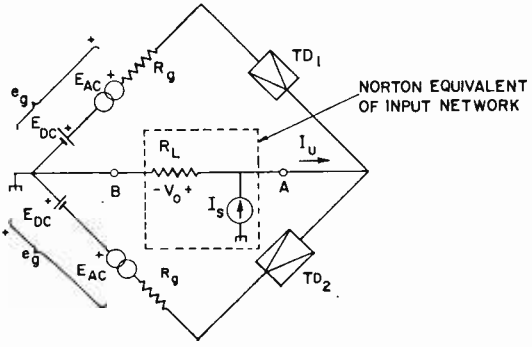


Fig. 1—Tunnel-diode balanced-pair majority circuit. I_s is the Norton equivalent of the input current from other circuits.

tunnel diode switching to its low-voltage state. It will be shown that mode (a) operation is preferable. But first a more complete description of the two modes of operation will be given.

The basic operation of a majority circuit in mode (a) is illustrated in Figure 2. Here, curve D_1, which represents the V–I characteristic

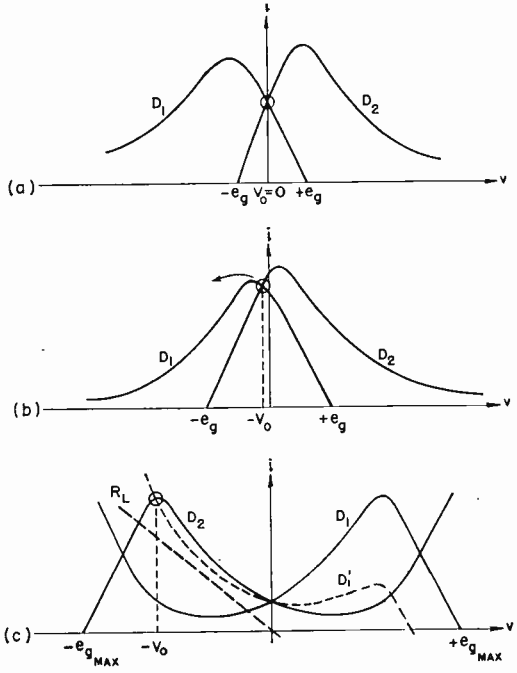


Fig. 2—Characteristic curves of a majority circuit for various values of e_g in mode (a) operation.

of diode TD_1, is a nonlinear load line applied to curve D_2, which represents the V–I characteristic of diode TD_2. (Effects of the source resistance of the power supplies, R_g, is included in the curves D_1 and D_2.) Initially, both tunnel diodes are in their low-voltage regions as shown in Figure 2a and the output voltage, V_0, is zero. As the balanced power supply voltages, e_g, increase, as shown in Figure 2b, V_0 will assume a negative value if the peak current of diode TD_2, I_{P2}, is greater than the peak current of diode TD_1, I_{P1}. Conversely, if I_{P1} is greater than I_{P2}, V_0 will be positive.* When e_g reaches its maximum

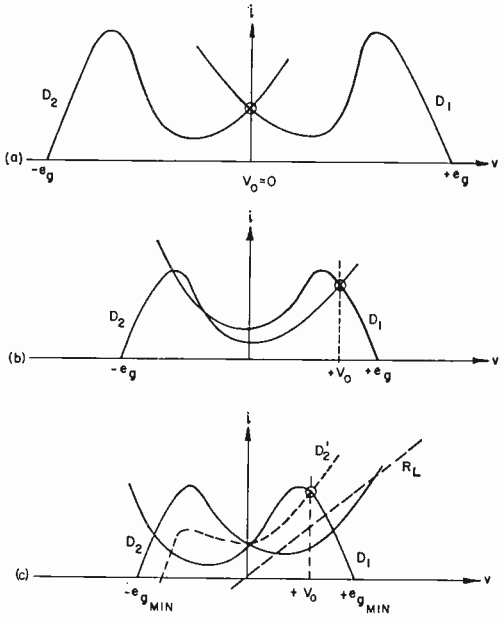


Fig. 3—Characteristic curves of a majority circuit for various values of e_g in mode (b) operation.

value, the characteristic curves are shown in Figure 2c. Effects of a net load, R_L, i.e., the parallel combination of fan-in and fan-out resistors, across input–output terminals AB in Figure 1, may be included as an increase in the loading on diode TD_2. The net load line on curve D_2 is then a composite of D_1 and R_L, D'_1 in Figure 2c.

Operation of a majority circuit in mode (b) is illustrated in Figure 3. Here, curve D_2 is a nonlinear load line applied to curve D_1. Initially,

* In this paper, a positive V_0 represents a "1" and a negative V_0 represents a "0."

both tunnel diodes are in their high-voltage regions and V_0 is zero as shown in Figure 3a. As e_g decreases (Figure 3b), V_0 assumes a positive value if the valley current of diode TD_1, I_{V1}, is greater than the valley current of diode TD_2, I_{V2}. Conversely, if I_{V2} is greater than I_{V1}, V_0 will be negative. When e_g reaches its minimum value, the characteristic curves are as shown in Figure 3c.

Majority circuits exhibit a locking property,[5,6] i.e., circuit *states* which represent a "1" and "0" at the output terminals AB are, once they have been reached, stable and independent of other inputs and reasonable loading. For a unilateral logic system, then, it is sufficient that majority circuits, when bilaterally coupled, be powered with a multiphase power supply of at least three phases.

When a majority circuit is operated in mode (a), neglecting reactances, the instant of locking, or the point where the *state* which the circuit will enter is determined, is when $e_g = V_P$, where V_P is equal to the peak voltage, E_P, associated with the tunnel-diode characteristic plus $I_P R_g$, the voltage drop across R_g. For mode (b), locking takes place when $e_g = V_V$, where V_V is equal to the valley voltage, E_v, associated with the tunnel-diode characteristics plus $I_V R_g$, the voltage drop across R_g. Experience has shown that E_V has a greater variation from circuit to circuit than E_p. This indicates that *a switching threshold as determined by the valley region of a tunnel-diode characteristic is not clearly defined. For this reason, mode (a) operation is preferable.*

Unbalancing the tunnel-diode currents as their peaks or valleys are being passed determines the ultimate circuit *state*. This imbalance can be accomplished by inserting a small current into terminal A if diode TD_2 is to enter its high-voltage region, or by drawing a small current from terminal A if diode TD_1 is to enter its high-voltage region (see Figure 1). Final circuit *states* also can be affected by choosing tunnel diodes with unbalanced peak or valley currents. As such, majority circuits not only discriminate as to the polarity of the input current from the linear summation network but also the magnitude of these current inputs.

The magnitude of the ratio of current entering or leaving terminal A (Figure 1) to nominal peak current of the tunnel diodes for an operating circuit is termed the *sensitivity* of a majority circuit. *Minimum sensitivity* denotes the lowest value of sensitivity for which a circuit will operate properly. Experimentally, minimum sensitivities of the order of 1 per cent were commonly achieved at a 150-mc repetition rate by adjusting only the d-c bias current. This adjustment served to overcome many inherent circuit imbalances. Similar experiments have required a minimum sensitivity of 6 per cent for operation at 1-kmc and 1.2-kmc repetition rates. Empirical information on output-

Table I

Frequency (mc)	Peak Current of Tunnel Diode (ma)	Net Load Ohms	Net Load Current (ma)	Minimum Sensitivity (%)	Output Voltage (mv)
150	5	7.5	2.4	1	±180
150	50	12.5	14	1.5	±180
750	50	25	7.2	6	±180
1200	50	50	3.6	6	±180*

* estimate

voltage amplitude, maximum loading, and sensitivity is sufficient to give a circuit's fan power and yield an appropriate value for coupling resistors. Values of minimum sensitivity, output-voltage amplitude, and net load derived from operation of several majority circuits in the 150-mc to 1.2-kmc frequency range, are tabulated in Table I. Typical *V–I* characteristics of the germanium tunnel diodes used to obtain the results given in Table I are shown in Figure 4. The capacitances of the 50-ma and 5-ma diodes were 10 picofarads (10×10^{-12} farad) and 3 picofarads, respectively.

Figure 5 shows typical "1" and "0" output waveforms of the 5-ma and 50-ma majority circuits operating at a 150-mc repetition rate.

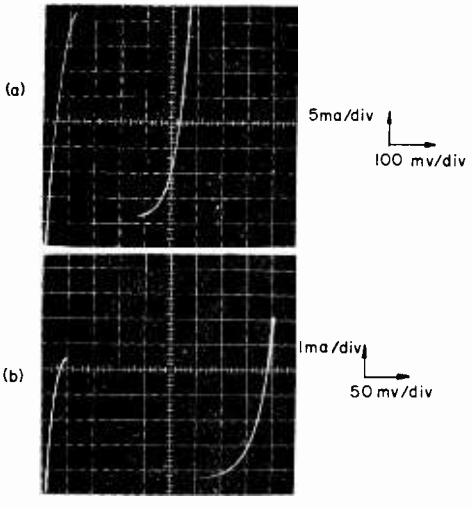


Fig. 4—Typical tunnel-diode volt-ampere characteristics: (a) 50-ma germanium unit; (b) 5-ma germanium unit.

In addition, Figure 5 shows an output voltage waveform for 1.2-kmc operation.* Measured rise and fall times were 0.3 nanosecond (0.3×10^{-9} second) which was equal to the rise time of the sampling oscilloscope. The triangular shape of the output pulses is typical of the performance of these majority circuits above 150 mc.

If the information given in Table I is used to calculate fan-power, the 5- and 50-ma circuits at 150 mc have fan-powers of 48 and 14, respectively, while the 50-ma circuits at 750-mc and 1,200-mc have

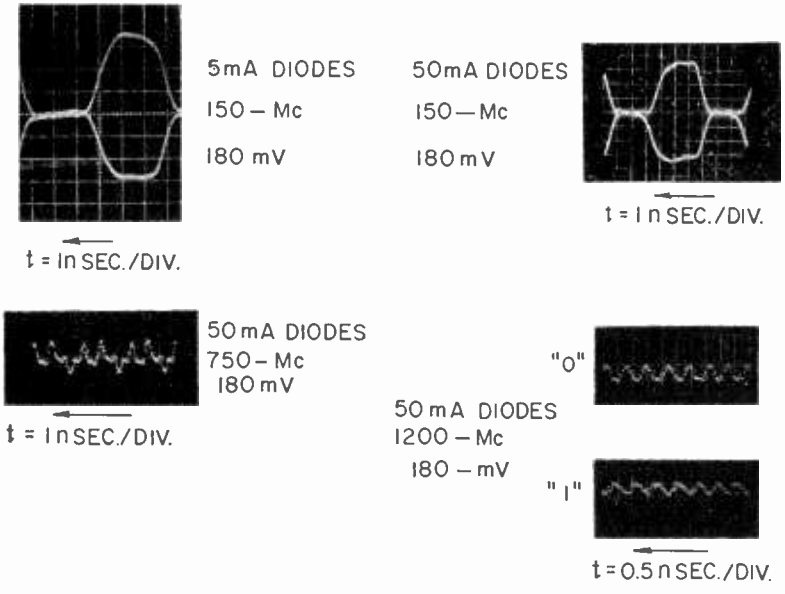


Fig. 5—Output waveforms of balanced-pair majority circuits.

fan-powers of two and one, respectively. The information used to calculate these values of fan power was obtained from circuits operating individually with no concern for system tolerances. When these circuits are incorporated into a system, various tolerances must be considered. In order to obtain reliable operation, much of this fan-power must be sacrificed. Thus, even though majority circuits can operate in excess of 1-kmc repetition rates, the amount of fan-power available at repetition rates above the 150-mc range is insufficient to allow any sacrifice for reasonable system tolerances.

The exact amount of fan-power as a function of system tolerances for the 5- and 50-ma circuits at 150 mc is discussed in Part II.

* Unless otherwise specified, mode (a) operation was used in experimental work described in this paper.

Inverter Circuit

The balanced-pair inverter circuit is shown in Figure 6. An input or signal current, I_{UI}', at inversion terminals CD will produce equal signal currents in resistors labeled R_1 in the figure. If the net output resistance, R_{LI}, across terminals AB is infinite, no signal current flows through the two diodes. If R_{LI} is finite, an additional path to ground is provided for input signal currents. As a consequence, one half of I_{UI}, the current through R_{LI}, flows through each of the tunnel-diodes, TD_1 and TD_2. In combination with power-supply currents, this results in unequal currents in the diodes. The tunnel-diode with a larger net

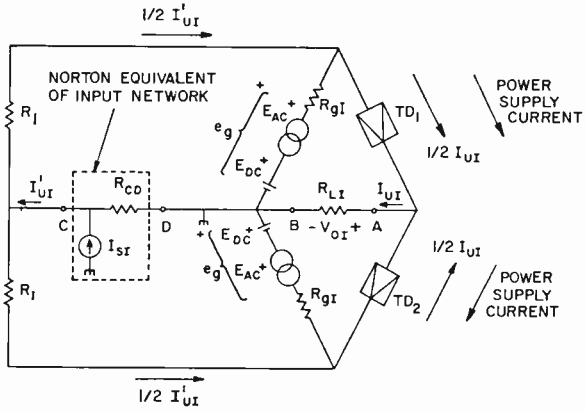


Fig. 6—Balanced-pair inverter circuit. Terminals CD are the inversion input terminals and terminals AB are the output terminals. I_{SI} is the Norton equivalent input current from other circuits.

current (in this case TD_1) will be switched to its high-voltage region. Thus, a current entering terminal C will cause diode TD_1 to be switched to its high-voltage region with a resulting negative output voltage, V_{OI}, across R_{LI}. Conversely, a current leaving terminal C will cause diode TD_2 to be switched to its high-voltage region with a resulting positive output voltage, V_{OI}, across R_{LI}.

It is possible to perform majority logic with some inputs complemented by using the inverter circuit. Input signals are connected to both its input and output terminals (complemented inputs to terminals CD). Thus, balanced-pair majority and inverter circuits are capable of 11 separate logical junctions including amplification.[7] In other respects, balanced-pair inverter circuits are similar in behavior to

majority circuits; thus, further discussions are restricted primarily to majority circuits.

Two balanced-pair building blocks, one which is capable of AND and OR logic and another which is capable of inversion, have been described. Together, these building blocks provide a functionally complete set that amplifies and standardizes logic signals. The problems of distributing the high-frequency a-c supply voltages as well as problems of packaging and subsystem fabrication techniques are determining factors in successful integration of these building blocks into high-speed computers. Solutions to these problems will now be discussed.

Power-Supply Requirements

As seen by the a-c power supply, the input impedance of 5- and 50-ma germanium-diode majority and inverter circuits ranges from one to ten ohms. To obtain a practical distribution system for the a-c component of the power supply, conversion of a current source into a voltage source at the circuit level is desirable. These current sources should be obtained, in part, with reactive components to prevent excessive power dissipation, providing these reactive components do not store sufficient energy to distort normal d-c supply voltage levels. When transmission lines are used to distribute a-c power, precautions must be taken to prevent any undesirable switching of the balanced-pair circuits because of improper terminations. In order to provide ground-return paths for high-frequency logic signals, a ground point should be available at the individual circuit level. Isolation of power-supply ground currents from logic ground currents is necessary to prevent power-supply interaction with logic signals.

Two methods of power distribution which meet the above considerations have been experimentally used. These are: (1) the constant-k filter method, and (2) the stub-matching method. A variation of the stub-matching method is also discussed.

Constant-k Filter Method

This a-c power-distribution technique, which is useful for small numbers of circuits, consists of inserting constant-k filter sections into an a-c power bus (a terminated 50-ohm transmission line).* These

* This a-c power supply distribuiton technique was originally suggested by E. L. Willette, formerly with RCA Laboratories, Princeton, New Jersey, to solve the problem of distributing high-frequency square-waves composed of their first, third. and fifth harmonics.

filter sections are constructed by narrowing a short length of printed 50-ohm transmission line to form a high-impedance section. This high-impedance section appears as a series inductance. A constant-k filter is obtained by placing a capacitor between the middle of the high-impedance section and ground. A small resistor, R_g, in series with this shunting capacitor provides a low-voltage, low-impedance source for the tunnel diodes. By proper design, connections can be made between constant-k sections with arbitrary lengths of 50-ohm coaxial cable or printed transmission line. Thus, multiphase power supplies are easily obtained. This method of supplying a-c power has been used in experiments with single balanced-pair circuits and also in two separate, high-speed, scale-of-two counters. There are several disadvantages associated with the constant-k a-c power-distribution system. First, a large amount of power is wasted in the termination of the a-c power bus in comparison with the power supplied to the circuits. Second, the voltage along the a-c power bus decreases as more filter sections are inserted.

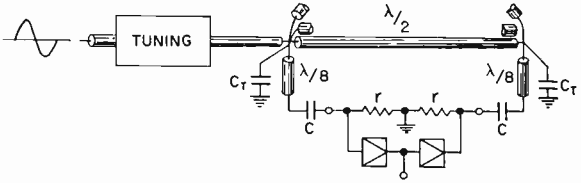


Fig. 7—Stub matching method of distributing a-c power supply voltage.

Finally, it is difficult to achieve a high packing density of balanced-pair circuits. The constant-k method of distributing a-c power is thus restricted to applications involving small subsystems.

Stub-Matching Method

The stub-matching method of distributing a-c power avoids many of the shortcomings of the constant-k method. Figure 7 shows how capacitors again provide a constant current, which, in combination with the shunt resistors R_g, give the necessary low-impedance, low-voltage sources. A number of balanced-pair circuits can be supplied from a single a-c supply line by supplying a-c power to a tie point, which, in turn, is connected to a second tie point by means of a half-wavelength-long transmission line (at the power-supply frequency). These two tie points are the supply points for the two a-c power-supply voltages opposite in phase. Transmission lines, normally one-eighth wavelength long,* are connected from each tie point to the capacitors in series

* The choice of an eighth-wavelength assures maximum attenuation of the fundamental and third harmonic of the interaction voltages discussed in following paragraphs.

with appropriate sides of balanced-pair circuits. In order that the main a-c power source will see a matched load, a single or double-stub tuner is added to the a-c transmission line on the power-supply side of the tie points (hence the name stub-matching method).

Balanced-pair circuits tend to interact with each other via the power-supply distribution system. When a circuit switches, a small pulse is fed back into each a-c power supply line, and consequently a change may occur in the values of power-supply voltages of other circuits. The effect of these pulses on other circuits is reduced by the combination of the capacitors C at the balanced-pair circuits and capacitors C_T placed from each tie point to common ground (see Figure 7). An analysis of this interaction is discussed in the following section.

1. *Interaction Between Balanced-Pair Circuits*

The interaction problem can be conveniently studied by considering a group of ten majority circuits being fed from a common source using the previously described stub-matching method. Maximum undesirable effects on any one circuit occur when all of the other nine circuits are switching in identical directions, e.g., all negative output pulses. Effects of continuous switching in one direction of the nine majority circuits on nominal values of power supply voltages on the tenth circuit are easily determined by employing the following model of majority circuits.

A tunnel diode switching to its high-voltage region is replaced by a linear resistance, r, and a nonlinear current source, $I_n = f_1(V_r)$, in parallel with r,[8,9] where V_r is the voltage across r. This current source I_n, in parallel with r, can be replaced by a nonlinear voltage source $E_n = f_2(V_r)$ in series with r. A tunnel diode which remains in its low-voltage region is replaced by only r. All reactances are neglected.

As seen from one power-supply feed line, a majority circuit is replaced by a Thévenin voltage source and resistance. This Thévenin voltage source is expressed in terms of E_n. There are two possible values for this Thévenin voltage depending upon which tunnel diode switches to its high-voltage region. This Thévenin voltage is easily

[8] J. B. Geller and P. A. Mantek, "Tunnel-Diode Large-Signal Simulation Study," *Proc. I.R.E.*, Vol. 49, p. 803, April, 1961.

[9] J. J. Gibson, "An Analysis of the Effects of Reactances on the Performance of the Tunnel-Diode Balanced-Pair Logic Circuit," *RCA Review*, Vol. XXIII, p. 457, Dec. 1962.

related to the observable output voltage, $V_o = f(E_n)$, across terminals AB. Then, by a suitable transformation of the form $V_o = g(t)$, this Thévenin voltage becomes a known function of time.

The resulting linear transmission line problem of nine Thévenin equivalent circuits feeding interaction voltages through one tie point to a tenth circuit which is represented by only its Thévenin equivalent resistance was solved. For typical 150-mc, 50-ma, germanium-diode majority circuits, the peak value of the interaction voltage appearing across the Thévenin resistance of the tenth circuit amounted to no more than 0.5 per cent of the nominal peak a-c power-supply voltage. One-eighth wavelength long power supply feed lines from tie points to circuits were assumed, since this length resulted in the greatest attenuation of the interaction voltages. (C and C_T were 10 and 200 picofarads, respectively.)

The impedance transformation caused by the one-eighth wavelength transmission lines, together with the necessity of providing a current source at circuit levels, requires than an a-c power-supply voltage much larger than that appearing at a majority circuit itself be impressed on the tie points. For example, when 200 millivolts is required for 50-ma germanium-diode majority circuits, the a-c voltage at the tie points is approximately four volts.

2. *A Variation of the Stub-Matching Method*

A variation of the above a-c power-distribution system which has been experimentally used is described at follows. The capacitors at the circuit ends of the a-c power supply feed lines are removed and low-wattage terminating resistors are added in series with each line at the tie-point ends. The feed lines are increased to a quarter-wavelength to minimize the dissipation in the terminating resistors. The impedance at the tie points is held to a low value by means of large capacitors to ground, C_T. Pulses entering this power-distribution network from balanced-pair circuits are absorbed at the tie point ends by the terminating resistors. As a result, the power-supply interaction problem is essentially eliminated.

Subsystems

The subsystems to be described are two scale-of-two counters and two three-bit end-around shift registers. These subsystems were constructed to gain experience with balanced-pair logic subsystems as well as to determine the feasibility of the power-distribution techniques in the 150- and 450-mc range. 50-ma tunnel diodes were chosen for these subsystems since they were the best diodes available at the time.

Scale-of-Two Counters

Two high-speed binary counters were constructed and operated at 150- and 450-mc repetition rates. These counters used the constant-k power-distribution method. The logic diagram of the counters is shown in Figure 8a. Bistable storage for both counters is provided by three balanced-pair circuits connected in the form of a ring. This ring is capable of storing a "1" or "0" as a circulating positive or negative pulse. Two of the three circuits of the ring perform AND and OR logic

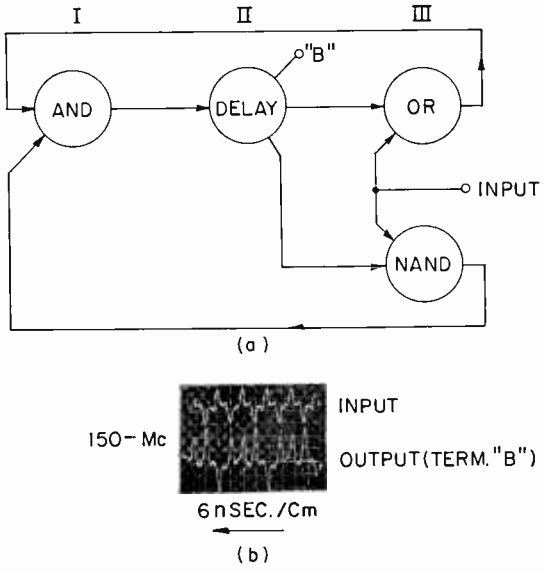


Fig. 8—Binary counter: (a) logic diagram; (b) input and output waveforms.

for setting and resetting the storage ring. These two circuits plus the addition of a NAND gate cause the state stored in the ring to change with the application of a positive pulse at the input. Input and output waveforms of the 150-mc counter are shown in Figure 8b. Similar waveforms were obtained from the second counter which was operated at 450 mc.

Three-Bit Shift Register

Thirteen majority circuits using 50-ma germanium tunnel-diodes and one inverter circuit using 50-ma gallium arsenide diodes were used to construct a three-bit shift register. This shift register employed the stub-matching method of a-c power distribution. Three-phase rings of the type used in the counters were the storage elements in this shift

register as shown in the logic diagram in Figure 9a. Initially, the three storage rings were set with appropriate information by overriding existing information within the rings with a d-c bias of proper polarity. This bias was applied through push buttons connected to the delay gates in the rings. The inverter circuit was used to reset all storage rings to "0". The maximum fan-in plus fan-out of any circuit in the shift register was four. A photograph of this shift register is shown in Figure 10.

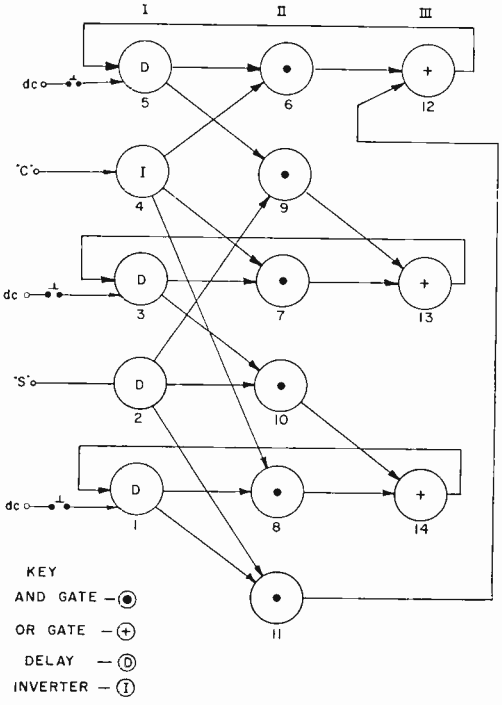


Fig. 9(a)—Logical diagram of three-bit shift registers. The gates are arranged in columns according to their power-supply phase; gate numbers are located beneath the gates.

Forty-ohm carbon resistors were used to make interconnections between balanced-pair circuits. These resistors were connected on a point-to-point, minimum-length basis and located inside the copper cylinder around which the circuit boards were grouped. This cylindrical construction gave two separate ground paths, one for logic current and one for power supply current. Three-phase 150-mc sine-wave voltages were brought directly to the four circuit boards by subminiature coaxial cable. Trimmer capacitors were used to control the a-c voltage

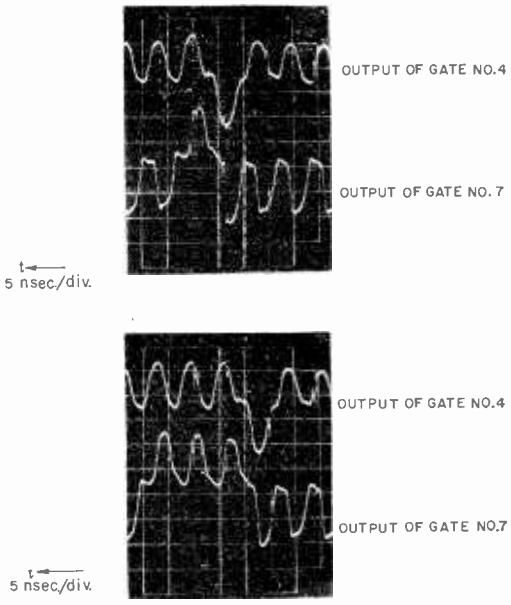


Fig. 9(b)—Waveforms of shift registers of Figure 9(a) operating at 150 mc.

balance on each gate. The adjustment, once made, was never repeated. The large "mushrooms" on each circuit board formed the large capacitors, C_T, between the tie points and ground. D-C bias current was supplied to the circuits from a separate bus via r-f chokes.

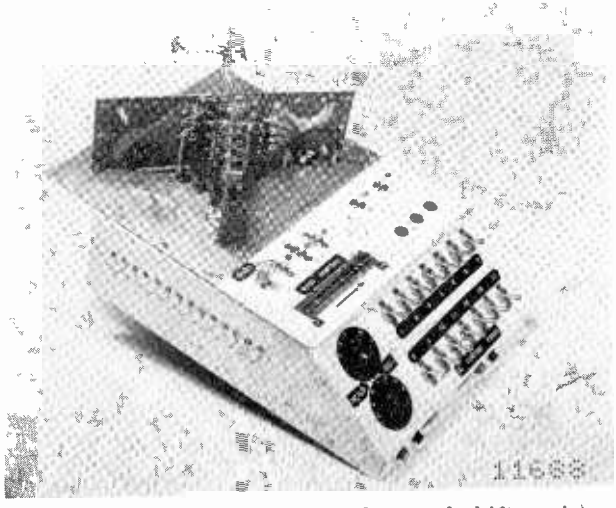


Fig. 10—A 150-mc, three bit, end-around shift register.

Waveforms obtained in shifting a "1" between two of the storage rings are shown in Figure 9b.

Evaluation of Subsystems

In general, performance of these subsystems indicates the importance of the problems of packaging, subsystem fabrication technique, and system tolerances in influencing the operation of balanced-pair circuits. For example, the counter waveforms in Figure 8b and the shift-register waveforms in Figure 9b greatly differ from the waveforms of individual balanced-pair circuits operating at 150 mc illustrated in Figure 5. In particular, the counter and shift-register waveforms indicate, by the small changes in the base line, the significance of the feedthrough of undesirable signals (often referred to as *noise*) in balanced-pair logic systems. Feedthrough is but one part of the system tolerance problem and is treated in detail in Part II of this paper.

The necessity of careful package and subsystem fabrication procedures was also emphasized by the performance of these three subsystems. For example, one experiment with the shift register indicated that particular care must be taken to eliminate stray reactances associated with circuit loads. The shift-register circuits exhibited an alternate "1"–"0" output when operating with a 25-ohm load having a series inductance of 20 nanohenries (20×10^{-9} henry) or approximately one inch of number 22 wire. This output pattern, which occurred in the absence of other inputs, was due to energy stored in this inductance, i.e., if the previous output of the circuit is a positive pulse, a current will persist in the inductor creating negative logic input current for the next cycle and, thus, the "1"–"0" output pattern. For reliable operation, this effect must be overcome by desired input currents.

The necessity for careful packaging and subsystem fabrication procedure led to the development of better packaging and fabrication techniques for balanced-pair circuits. To obtain practical experience with these improved techniques, a second three-bit shift register was constructed.

Packaging Requirements

As shown in Part II, lengths of logic interconnections between circuits must be exceedingly short. As a consequence, the shape of balanced-pair packages and their geometrical arrangement must be such that the circuits which comprise a given subsystem can be interconnected within the range of the longest permissible logic interconnec-

tion lead length, according to the logic diagram. In many cases, these considerations naturally lead to spherical or cylindrical subsystem configurations. For example, an end-around shift register lends itself to cylindrical configurations while some portions of control logic lend themselves to spherical configurations. However, due to difficulties caused by the cylindrical nature of the first shift register, a planar configuration was chosen for all subsequent subsystems.

In the planar system, package areas are minimized in the logic plane. Further, under the principles set forth below, two planar arrays can be assembled so as to achieve many of the advantages of cylindrical and spherical configurations. Additionally, planar arrays allow power-supply distribution systems to be complicated since the third dimension can be arbitrarily large (subject to some practical restrictions, of course). Ground-current paths for logic currents and power supply currents are also separated. The principles set forth in fabricating balanced-pair subsystems are:

1. All logical interconnections are made in the X-Y or logic plane.
2. All power supply distribution is made in the Z, or third, dimension.

Compact balanced-pair packages were developed which measured $\frac{1}{4} \times \frac{1}{4} \times \frac{1}{2}$ inch (62.5×10^{-3} square inch in the logic plane). Figures 11 and 12 show photographs of this package in various stages of construction. Two tunnel-diodes are first welded to an input–output tab as shown in the highly magnified photograph at the top in Figure 11. Two carbon disk-shaped resistors, a ground tab, and two power-supply tabs are then soldered to this unit as shown at the bottom in Figure 11. This unit is made as small as possible to reduce the inductance which tends to limit the upper operating frequency of these balanced-pair circuits.[9,10] The entire assembly is placed in an electroformed copper shield can as shown in Figure 12. There still remains sufficient space in this package to include the logic resistors for terminating interconnecting transmission lines. Alternatively, these logic resistors can be included in the interconnecting transmission lines.

This package is designed to be adaptable to either coaxial cable or printed-circuit power-supply feed systems. A printed-circuit feed system allows individual packages to be plugged into it. Cable connections allow individual balanced-pair circuits in the logic plane to be connected to any one of three phases of the a-c power supply as required by the logic diagram.

[10] G. B. Herzog, "Tunnel-Diode Balanced-Pair Switching Analysis," *RCA Review*, Vol. XXIII, p. 187, June 1962.

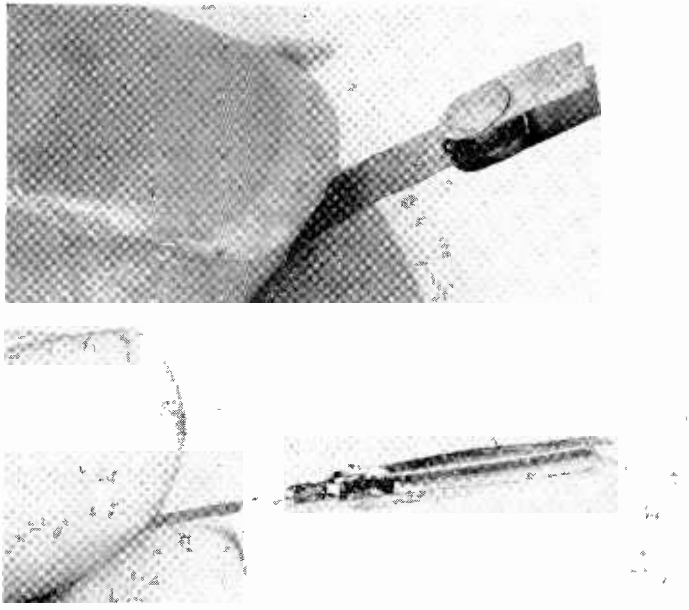


Fig. 11—The tunnel-diode assembly.

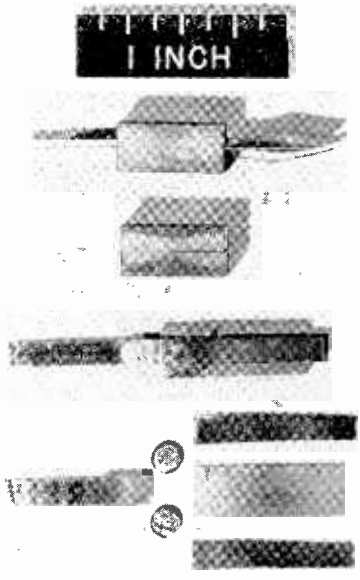


Fig. 12—Steps in the assembly of the balanced-pair package.

D-C bias to the center of the tunnel-diode pair is distributed in the same plane as in the a-c power-distribution system. Sufficient space is left in the shield can to include a resistor and by-pass capacitor for d-c bias purposes.

Fifteen packages of this type were built using 50-ma germanium tunnel diodes. Uniform operating characteristics of these packages were obtained at 150 mc. These packages were incorporated in the second three-bit shift register which was constructed according to the principles set forth above. Miniature coaxial cables were used for logical interconnections and were terminated in their characteristic impedence at each end. In general, the construction and packaging techniques were found to be satisfactory.

To achieve repetition rates approaching 1 kmc in subsystems using balanced-pair circuits, micro-fabrication techniques must be employed. Towards this end, a proposed geometrical arrangement for majority circuits which should operate near 1 kmc is illustrated in Figure 13. This package consists of two ceramic cylinders placed end-to-end and separated with a ceramic seal and the logic tab, as shown in Figure 13. This seal permits individual etching of the two tunnel-diodes. The diodes themselves have a cylindrical junction to minimize internal inductance.[11] Both n-on-p and p-on-n types of tunnel diodes are used. Small cylindrical "slugs" of germanium are positioned on top of the tunnel-diodes to form the R_g's. A-C power is brought into this package via coaxial or printed-circuit transmission lines which are connected directly to the top and bottom of the cylindrical package as indicated in Figure 13. These cylinders are metalized with several mils of silver except in close proximity to the logic-tab and power-supply connections. This forms a cylindrical conductor which minimizes inductance in the transmission path between the tunnel diodes. The exterior metalized surface completes the coaxial structure in which the majority circuit resides.

Conclusions

Two balanced-pair building blocks have been described. Together these building blocks provide a functionally complete set that amplifies and standardizes logic signals. An individual balanced-pair circuit was operated in excess of a 1-kmc repetition rate. However, only the 5- and 50-ma circuits, which were operated at a 150-mc repetition rate, have sufficient gross fan power or logic gain to indicate a potential usefulness in high-speed computers.

[11] D. E. Nelson, private communications.

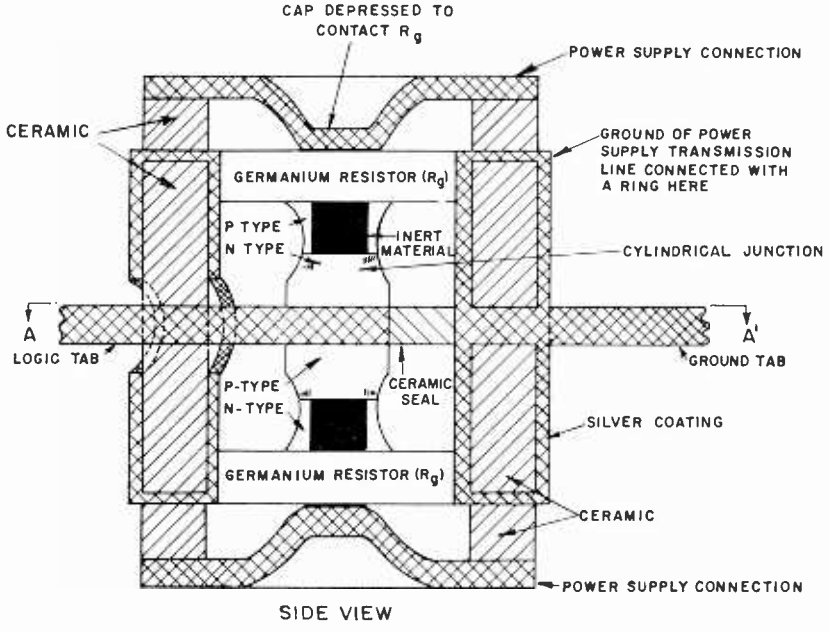


Fig. 13—Proposed majority circuit package.

The major problems of distribution of high-frequency a-c supply voltages and packaging and subsystem fabrication techniques were successfully solved. However, two other major problems — feedthrough of undesirable signals in balanced-pair logic systems and circuit tolerances — remain to be discussed in Part II.

PART II — SYSTEM TOLERANCES

Introduction

In Part I, two balanced-pair building blocks were described. Together, these building blocks provide a functionally complete set which amplifies and standardizes logic signals. An individual balanced-pair circuit was operated at a repetition rate greater than 1 kmc. It was noted, however, that only the 5- and 50-ma majority circuits operating at a 150-mc repetition rate have sufficient gross fan power or logic gain to be useful in high-speed computers. Solutions to the major problems of distribution of high-frequency a-c supply voltages and packaging and subsystem fabrication techniques were also discussed.

Part II of this paper discusses the two other major problems — feedthrough of undesirable signals in balanced-pair majority circuit systems and circuit tolerances. The discussions of these problems are based upon a linearized majority circuit transfer characteristic which depicts the relationship between the output voltage and the power-supply voltage of a majority circuit. This transfer characteristic is first derived and then used to select the optimum ratio between the a-c and d-c components of the power supply. The limits on the lengths of transmission lines used to interconnect balanced-pair circuits are then determined. Finally, these fundamentals are used in an analysis of a generalized balanced-pair majority circuit network.

Linearization of Tunnel-Diode *V–I* Characteristic

All discussions in this part of the paper are based on a linearized tunnel-diode volt–ampere characteristic. This linearization of the tunnel-diode characteristic facilitates the derivation of simple closed-form expressions approximating the low-frequency (repetition rate) behavior of balanced-pair circuits. The particular linearization chosen for the tunnel-diode *V–I* characteristic is illustrated in Figure 14. In this figure, the point (E_p, I_p) is chosen to coincide with the peak of the actual tunnel-diode characteristic (dotted line). E_F is that voltage which corresponds to the tunnel-diode conducting a current of I_p when it is in its high-voltage region. The point (E_V, I_V) is chosen to correspond to the intersection of an extension of the linear region of the high-voltage portion of the tunnel-diode characteristic with an extension of the relatively flat portion of the valley region. E_V' denotes the actual valley voltage of the tunnel diode.

When a balanced-pair circuit is operated in mode (b) at a low repe-

tition rate, pronounced oscillations occur immediately prior to switching when the voltage across one of the tunnel diodes is less than E_V' but greater than E_V. To avoid this problem, the point (E_V, I_V) rather than the tangential point (E_V', I_V) was chosen as the break point in the linearized tunnel-diode characteristic. Point (E_V, I_V) corresponds to a point on the actual tunnel-diode characteristic where the negative resistance is small enough to permit fast switching without any oscillation.

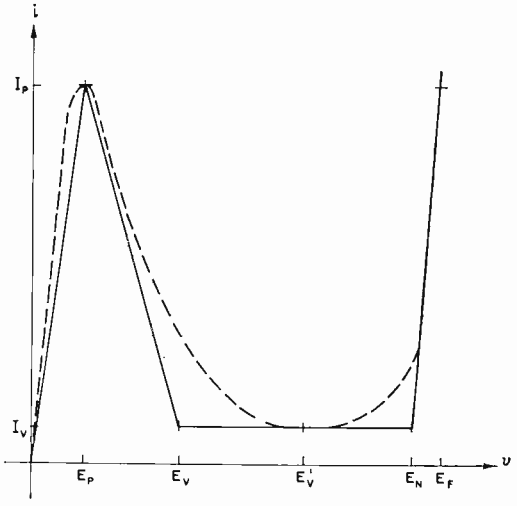


Fig. 14—Piecewise-linear approximation of tunnel-diode characteristic.

Transfer Characteristic

The linearized balanced-pair transfer characteristic, which depicts the relationship between the magnitude of the output voltage, $|V_o|$, and the power supply voltage, $2e_g$, of a majority circuit, is obtained by using the piecewise linear tunnel-diode V–I characteristic discussed above in a manner similar to that illustrated in Figures 2 and 3. For this linearized case, the procedure for construction of the transfer characteristic for mode-(a) operation is shown in Figure 15. In this figure, the linearized characteristic of tunnel diode TD_2 in series with the internal resistance, R_g, of the power supply $-e_g$ is shown by the heavy lines, D_2. The parallel combination of the load resistance, R_L, and the remaining tunnel diode TD_1 in series with the internal resistance, R_g, of the power supply $+e_g$ form the *load line* for the heavy characteristic and is represented by the light lines, D_1'.

In Figure 15a, $|e_g|$ has been increased to the point where the existing operating point (circle), at which both tunnel diodes are in their low-voltage regions, is about to jump to the next stable operating point (solid dot), where TD_1 is in its valley-voltage region and TD_2 is in its low-voltage region. Prior to the condition shown in Figure 15a, the output voltage, V_o, is zero as shown by the transfer characteristic. The construction of the transfer characteristic for continued increases in $|e_g|$ is illustrated in Figures 15b, c, and d. The complete mode-(a) transfer characteristic is shown in Figure 16a. Equations for the

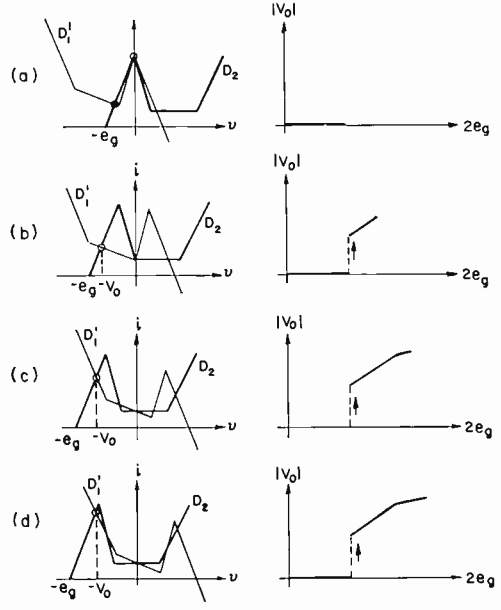


Fig. 15—Construction of balanced-pair transfer characteristic.

various break points in the transfer characteristic in terms of the tunnel-diode and circuit parameters are given in Appendix A.

There are several important concepts which can be easily shown in terms of the transfer characteristic and will be emphasized. These concepts are concerned with the states of the circuit and the shape of the transfer characteristic and output waveform.

1. *States*

The transfer characteristics for mode-(a) operation (Figure 16a) and mode-(b) operation (Figure 16b) indicate the seven stable *circuit states* (e.g., both tunnel-diodes in their low-voltage regions; one tunnel

diode in its valley-voltage region and one tunnel diode in its low-voltage region, etc.) in which a balanced-pair circuit can exist. The two *circuit states* in which one tunnel diode is in its valley-voltage region and the other is in its high-voltage region do not exist. Of the seven discernible *circuit states* shown by the two transfer characteristics, only three distinguishable *output states* exist at terminals AB. Two of these three *output states* are customarily assigned the logical values "0" and "1" as discussed in Part I. These states occur during the on-half

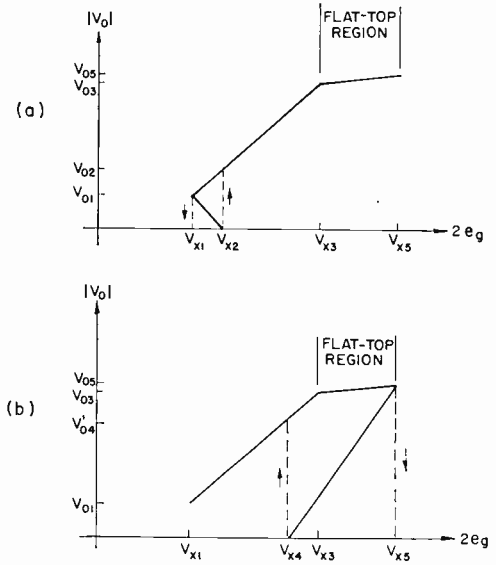


Fig. 16—Balanced-pair transfer characteristic: (a) in mode-(a) operation, and (b) in mode-(b) operation.

of the balanced-pair circuit power supply cycle. The third *output state* (often called a null or dead state) is defined as that state reserved for the off-half of the power-supply cycle, during which the output voltage is zero.

2. *Flat-Top*

The transfer characteristic has essentially a flat-top bounded by V_{x3} and V_{x5}. Consequently, the waveshape of the output voltage will have essentially a flat-top during the time when $|e_g|$ is between $V_{x3}/2$ and $V_{x5}/2$. This occurs during part of the on-half of the power-supply cycle. It should be pointed out that the flat-top is absolutely flat if the low-voltage and high-voltage regions of the tunnel diodes have the same slope.

The principal parameter which governs the width of the flat-top region of the transfer characteristic for a given tunnel-diode characteristic is R_g. The effect of increasing R_g on the curves used in constructing the transfer characteristic is shown in Figure 17. As R_g increases, the curves take on an increasing tilt. As a result, the next stable operating point (solid dot) moves from the circuit state in which TD_1 is in its valley-voltage region and TD_2 is in its low-voltage region to the circuit state in which TD_1 is in its high-voltage region, and TD_2 remains in its low-voltage region. When TD_1 is in its valley-

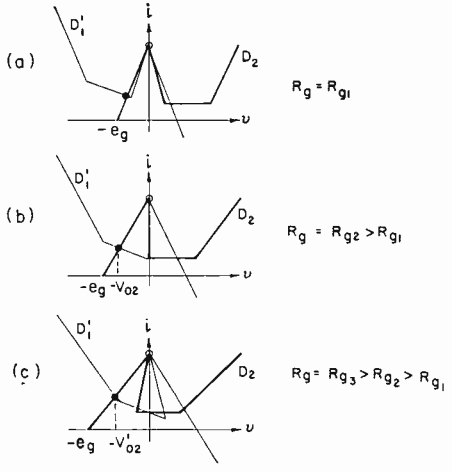


Fig. 17—Effect of increasing R_g on the characteristic curves of a balanced-pair circuit.

voltage region, the output voltage is denoted as V_{O2}; when TD_1 is in its high-voltage region, the output voltage is denoted as V_{O2}'.

For a small R_g, as illustrated in Figure 17a, the output voltage will be V_{O4}' for mode-(b) operation. If R_g is increased sufficiently, the output voltage will correspond to the circuit state in which one tunnel diode is in its valley-voltage region and the other is in its low-voltage region. In this case, the output voltage is denoted by V_{O4}.

Design Considerations

It was just pointed out that a flat-top region, the size of which is essentially controlled by R_g, exists in the transfer characteristic of a balanced-pair circuit. It is desirable to spend as much time as possible during the on-half of the power supply cycle in the flat-top region for several reasons. First, the amplitude of the output waveform will be

insensitive to tolerances in e_g during a large part of the on-half of the power supply cycle. The second reason concerns the length of logical interconnections between balanced-pair circuits.

Balanced-pair circuits are interconnected via lengths of transmission line (e.g., coaxial cable or printed-circuit transmission lines). These transmission lines, which have a characteristic impedance of Z_o, are terminated at both ends in their characteristic impedance. The value of Z_o is equal to one-half the value of the coupling resistor R_c. To obtain the greatest degree of freedom in the physical placement of balanced-pair circuits, the maximum permissible length of interconnecting transmission lines should be as long as possible.

The maximum and minimum lengths of the interconnecting transmission lines are determined from the shape of the output waveform. The necessary and sufficient information for determining the restrictions on lengths of interconnecting transmission lines is the following: the angle of the power-supply voltage, e_g, at which locking occurs (when $2e_g = V_{x2}$ in mode-(a) operation); the angle at which the circuit unlocks or returns to the null state (when $2e_g = V_{x1}$ in mode-(a) operation); and the width of the flat-top region of the output waveform. Assuming mode-(a) operation, the above three characteristics of the output waveform are determined in terms of the ratio of the d-c component to the a-c component of the power-supply voltage. These three characteristics are then combined into a set of equations which yield the maximum and minimum lengths of the interconnecting transmission lines.

Power-Supply Voltage Selection

Power-supply voltages are selected so as to obtain a maximum width of the flat-top region of the output waveform. As seen from the transfer characteristics, Figure 16a, maximum and minimum bounds can immediately be placed on the power-supply voltages;

$$V_{x1} < (2e_g)_{\max} < V_{x5},$$

and

$$(2e_g)_{\min} < V_{x1},$$

where

$$e_g = E_{DC} + E_{AC} \sin \omega t,$$

and E_{AC} is the peak value of the a-c component. In terms of the individual components of e_g, the bounds become

$$\frac{V_{x1}}{2} < E_{DC} + E_{AC} < \frac{V_{x5}}{2},$$

and

$$E_{DC} - E_{AC} < \frac{V_{x1}}{2}.$$

These bounds are the only restrictions that must be imposed on the power-supply components. However, the output pulse of a balanced-pair circuit has a flat-top only during the time that $2e_g$ is greater than V_{x3}. To maximize the width of the flat top in the output pulse, additional restrictions are placed upon E_{AC} and E_{DC}.

A necessary condition to insure the maximum width of the flat-top given either E_{DC} or E_{AC} is

$$2(E_{DC} + E_{AC}) = V_{x5}. \tag{1}$$

Another necessary condition that must be satisfied in order to return the circuit to the null state is

$$2(E_{DC} - E_{AC}) < V_{x1}. \tag{2}$$

Together, conditions (1) and (2) are sufficient to insure a maximum width to the flat-top of the output waveform and proper circuit operation, given an arbitrary E_{AC} or E_{DC}.

Interconnecting Transmission Line Lead Length

Since it is convenient to use the ratio of E_{DC}/E_{AC} (defined as x) as the independent variable in determining restrictions on interconnecting leads, conditions (1) and (2) are solved to yield

$$E_{AC} = \frac{V_{x5}}{2(x+1)} \tag{3a}$$

and

$$x < \frac{V_{x5} + V_{x1}}{V_{x5} - V_{x1}}. \tag{3b}$$

E_{AC} as given above will be used in the equations for lengths of interconnecting leads. These equations are developed as follows.

The length of interconnecting leads is chosen such that when the power supply, $2e_g$, is between V_{x3} and V_{x5}, the gates powered by the subsequent phase of the power supply will lock. This choice gives a minimum variation in output voltage during the time these gates are locking. Letting t_3 be the time when

$$V_{x3} = 2E_{AC}(x + \sin \omega t_3);$$

then

$$\omega t_3 = \sin^{-1}\left(\frac{V_{x3}}{2E_{AC}} - x\right).$$

The width of the flat-top of the output pulse expressed in degrees of the power-supply cycle is

$$\phi = 2\left(90° - \frac{180}{\pi}\omega t_3\right), \tag{4}$$

Note that the flat-top is centered about the 90° point in the operating cycle (i.e., when $e_g = E_{AC} + E_{DC}$). This point is also used as the reference for all other angles.

Locking of a majority circuit occurs when

$$V_{x2} = 2E_{AC}\,(x + \sin\psi);$$

then

$$\psi = \sin^{-1}\left(\frac{V_{x2}}{2E_{AC}} - x\right), \tag{5}$$

where ψ is the locking angle in degrees. Unlocking occurs when

$$V_{x1} = 2E_{AC}\,(x - \sin\beta);$$

then

$$\beta = \sin^{-1}\left(x - \frac{V_{x1}}{2E_{AC}}\right), \tag{6}$$

where β is the unlocking angle in degrees.

It can be seen from Figure 18 that the maximum interconnection lead length, L, in degrees for a three-phase power supply system is given by

$$L = (L_1, L_2)_{min}$$

where

$$\begin{aligned} L_1 &= (\psi + 240°) - \beta, & 180° - \psi \geqq 0 \\ L_1 &= (\psi - 120°) - \beta, & 180° - \psi < 0 \end{aligned} \tag{7a}$$

$$L_2 = (\psi + 120°) - \left(90° - \frac{\phi}{2}\right), \qquad 180° - \psi \geqq 0$$

$$L_2 = (\psi - 240°) - \left(90° - \frac{\phi}{2}\right), \qquad 180° - \psi < 0 \tag{7b}$$

where $0° < \psi \leqq 360°$. Conditions (7a) will apply over (7b) if

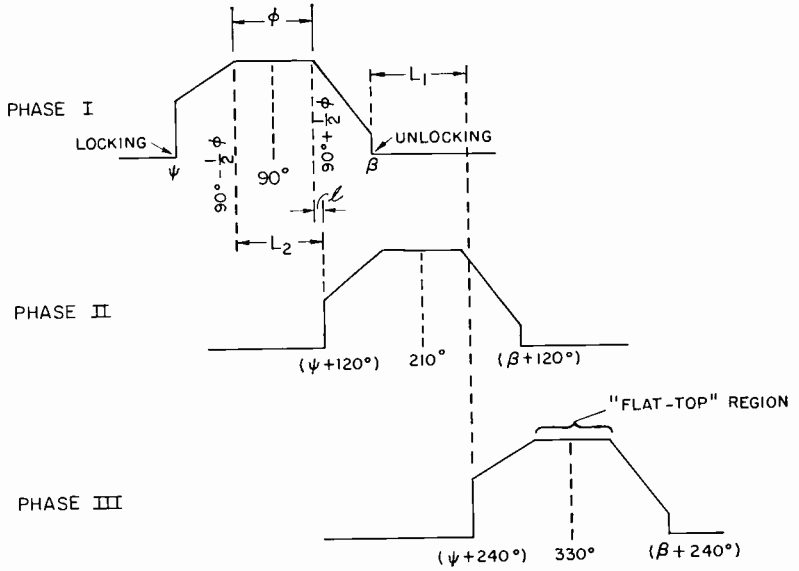


Fig. 18—Illustration of output waveform showing how limits on lengths of interconnecting transmission lines are determined. The centers of the flat-top regions of the output waveforms are the reference points.

$$\beta + \frac{\phi}{2} \geqq 210°.$$

Also, from Figure 18, the minimum interconnection lead length in degrees, l, is

$$l = (\psi + 120°) - \left(90° + \frac{\phi}{2}\right), \qquad 180° - \psi \geqq 0$$

$$l = (\psi - 240°) - \left(90° + \frac{\phi}{2}\right), \qquad 180° - \psi < 0$$

where $0° < \psi \leq 360°$ and where $l \geq 0°$. It is possible, for certain choices of peak current and ratio of E_{DC} to E_{AC}, that the minimum lead length for the interconnecting transmission lines will be longer

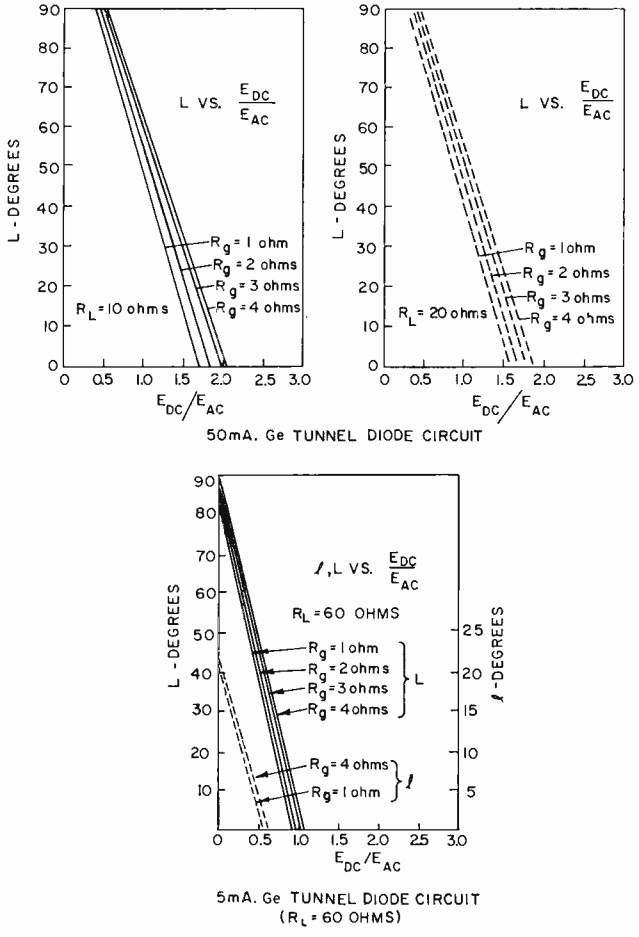


Fig. 19—Lengths of interconnecting transmission lines as a function of E_{DC}/E_{AC}.

than the distance between two circuits to be interconnected. This may cause difficulty in the physical layout of a subsystem.

The restrictions on interconnecting lead lengths (L is the maximum and l is the minimum) are plotted for typical 5-ma and 50-ma germanium-diode majority circuits as functions of x in Figure 19. Two important points in relation to these curves are:

(1) Increasing E_{DC}/E_{AC} increases the width of the output waveform and also the width of the flat-top region of the output waveform.

(2) Choice of E_{DC}/E_{AC} such that the width of the flat-top region of the output waveform is a minimum maximizes permissible lengths of interconnections but, unfortunately, minimizes the variation in these lengths.

It is important to note that (2) does not contradict the original assumption that the relationship between E_{AC} and E_{DC} is adjusted to yield a maximum width to a flat-top region given an arbitrary E_{AC} or E_{DC}.

System Tolerance Analysis

The balanced-pair transfer characteristic previously described can be used as the foundation for determining the worst-case output waveform of a balanced-pair circuit. Similarly, the procedure outlined above for determining restrictions on interconnecting transmission lines can be followed to obtain the corresponding worst-case restrictions on these lines. Provided amplitude variations in the output waveform are within some easily determined limits, this information, at first glance, appears complete enough to design a workable balanced-pair logic network. But, *system noise* is a very important problem inherent in tunnel-diode networks, in general, and must be considered in the design of a workable balanced-pair logic network. System noise (in part, feed through of unwanted signals) arises because tunnel-diodes are two-terminal active devices and consequently have no isolation between input and output terminals. In addition to the general problem of system noise, the design of a workable balanced-pair logic network must include consideration of imbalances in the two power supplies of the circuits. These imbalances have a major effect on the locking process of balanced-pair circuits.

In this section, a worst-case tolerance analysis of a majority circuit within a generalized balanced-pair logic network composed only of majority circuits is described by the development of a complete tolerance criterion. Due to the similarity between the two types of balanced-pair circuits, conclusions reached for the general majority-circuit logic network considered are equally valid for logic networks containing inverter circuits. This tolerance analysis does not determine an upper limit on the operating frequency of balanced-pair networks, but it does determine tolerance requirements that circuit parameters must meet to design a workable system at any frequency. Before actual develop-

ment of the tolerance criterion, the two major problems inherent in balanced-pair circuits mentioned above are discussed.

System Noise

Currents present at the input terminals of a majority circuit other than the desired logic current are termed *system noise*. There are two components of system noise: (1) feedthrough current, which is defined as the aggregate of currents from all circuits other than the one chosen for study except those circuits providing desired logic-input currents; (2) imbalance current, which is defined as the aggregate of currents caused by imbalances in the circuit chosen for study.

1. *Feedthrough Current*

The sources of feedthrough current, I_x, are

(1) Active circuits or "on" circuits in other portions of the logic network that are producing useful logical information that is not being sent directly to the circuit chosen for study.

(2) Circuits in their null state that are not completely "dead" due to tolerances in circuit parameters or other factors.

Currents from the more-remote circuits are attenuated at nearby circuits by the voltage-divider action of the coupling resistors, R_c, and the internal impedance of the majority circuit, R_0. For this reason, it is important to have the ratio R_c/R_0 as large as is practical.

The nature of feedthrough current is analyzed by studying a general network of linear equivalent circuits of majority circuits. This network is chosen to represent a logic network of majority circuits at the locking instant of the circuit chosen for study. An important property of this network is that none of the N outputs ($N =$ fan-out) and M inputs ($M =$ fan-in) of the majority circuits are left unconnected. It is primarily because of this property that the selection of the circuit for study is arbitrary. This linear network will extend to infinity in all directions. However, the feedthrough current behaves asymptotically such that, for the cases analyzed, only circuits up to four levels removed from the circuit chosen for study need be accounted for. The rules for setting up this general network are

(1) Active circuits are replaced by an equivalent circuit of a battery of V volts with an internal resistance R_0.

(2) Circuits in their null state are replaced by an equivalent circuit of a battery of E_i volts with an internal resistance R_0. (Subscript i denotes the phase of the power supply for the particular circuit.)

(3) All of the N outputs and M inputs of the circuits within the network are connected to other appropriate circuits within the network.

The voltage V is the maximum open-circuit voltage of an active circuit. The value of V may be determined by letting R_L approach infinity in Equations (17) and (22) of Appendix A. The voltages E_i represent the open-circuit imbalance voltage across the input–output terminals AB of circuits within the network that are in the null state. The value of E_i is the magnitude of the maximum imbalance voltage during the locking interval of the circuit chosen for study. The procedure for determining E_i is contained in Appendix B. This imbalance voltage

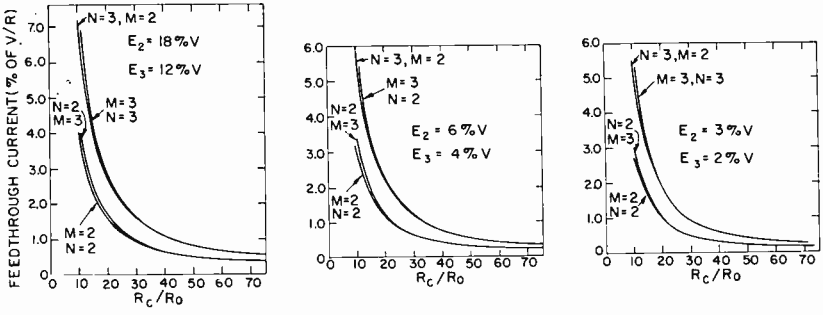


Fig. 20—Feedthrough current as a function of R_c/R_0.

results from power-supply, tunnel-diode, and circuit-parameter imbalances including those steady-state effects caused by reactive imbalances.

The feedthrough current is obtained by looking back into the linear equivalent network from the input–output terminals of the circuit chosen for study and computing the Norton equivalent circuit. To a close approximation, the resistance in parallel with this Norton current source I_x is equal to the coupling resistance divided by the number of inputs plus outputs of the circuits, or R_L. Thus, R_L is used as the value of the shunt resistance in all subsequent calculations.

I_x versus R_c/R_0 for several combinations of E_i's is given in Figure 7. In this figure, I_x is expressed as a percentage of the current V/R_0. The data contained in Figure 20 as applied to the 5-ma and 50-ma circuits discussed in Part I of this paper for two-input, two-output majority circuits are also tabulated in Table II. The appropriate values of E_2 and E_3 to choose for the selection of an I_x for use in the tolerance analysis are discussed in Appendix B.

The effect of feedthrough current can be readily appreciated when expressed as a percentage of the Norton equivalent of the logic current. The value of the Norton logic current is given by

$$I_{LN} = \frac{V_{05}}{R_c},$$

where V_{05} is given by Equation (22) in Appendix A. Using the values given in Table III, I_{LN} and V/R_0 are obtained for both the 50-ma and 5-ma circuits. This information is then used in conjunction with the information tabulated in Figure 20 to yield Table IV.

Table II

E_2 (% of V)	E_3 (% of V)	Feedthrough Current (I_x) (% of V/R) 50-ma Diodes ($R_c/R_0 = 14.4$)	5-ma Diodes ($R_c/R_0 = 38.4$)
12%	8%	2.5%	0.70%
6%	4%	1.9%	0.40%
3%	2%	1.7%	0.30%

2. *Imbalance Currents*

Undesirable effects on a circuit which originate in the surrounding network were transformed into an equivalent Norton input current as described above. Undesirable effects originating within the circuit chosen for study will now be considered.

These imbalance effects are accounted for by a Norton equivalent current source, I_{UB}, given by

$$I_{UB} = \frac{E_j}{R_L},$$

where j indicates the phase of the circuit chosen for study. E_j is determined in Appendix B. Typical values of I_{UB} are 0.614 ma for 50-ma circuits and 0.30 ma for 5-ma circuits.

Relative Power-Supply Imbalances

The major effects of relative power-supply imbalance are accounted for in the calculations for I_x and I_{UB} (see Appendix B). Two other

Table III

	50-ma Circuits	5-ma Circuits
I_P	47 ma	5.3 ma
I_V	7 ma	0.6 ma
E_P	120 mv	45 mv
E_V	240 mv	200 mv
E_V'	360 mv	300 mv
E_N	480 mv	400 mv
E_F	560 mv	440 mv
R_g	3 ohms	4 ohms
R_L	10 ohms	60 ohms
R_0	40 ohms	240 ohms
L	600 picohenries	600 picohenries
C	10 picofarads	4 picofarads

effects of relative power-supply imbalance are (1) an increase in the tolerance band of the amplitude of the output waveform; and (2) a decrease in the nominal values of E_{AC} and E_{DC}. However, these effects are secondary in relation to the major effect accounted for in system noise.

Tolerance Criterion

A tolerance criterion, in the form of a statement of a single requirement on the peak current imbalance of the tunnel diodes, TD_1 and TD_2,

Table IV

		Feedthrough Current Expressed as a Percentage of Norton Equivalent of Logic Current			
		50-ma Circuits		5-ma Circuits	
E_2	E_3	$I_{LN} = 4.4$ ma	$V/R_0 = 79.2$ ma	$I_{LN} = 0.70$ ma	$V/R_0 = 31.7$ ma
12%	8%	1.90 ma	43.2% I_{LN}	0.222 ma	31.4% I_{LN}
6%	4%	1.51 ma	34.4% I_{LN}	0.127 ma	18.2% I_{LN}
3%	2%	1.35 ma	30.7% I_{LN}	0.095 ma	13.6% I_{LN}

will be developed for any majority circuit within the generalized balanced-pair logic network. Proper operation of the generalized logic network is contingent upon the fulfillment of this criterion.

In addition to desirable logic currents and variations thereof, system noise current as discussed above also exists at the input of a majority circuit. Therefore, each circuit in the generalized network must be designed so that the noise currents will not interfere with the correct response of the circuit to its logic inputs. To better express the criterion, assume that the circuit arbitrarily chosen for study is a two-input, two-output logical gate whose characteristics are defined by

Table V

Input		Output
A	B	0
+	+	+
+	−	−
−	+	−
−	−	−

Table V. To insure proper operation when tolerances are applied to circuit components, the following two conditions must be satisfied:

1. When both inputs are in the same direction, the minimum sum of the logic currents must be sufficient to overcome the maximum noise current in the opposite direction, and cause the circuit to respond properly.
2. When the inputs are in opposite directions, their maximum difference plus the maximum noise currents must be insufficient to cause the circuit to respond improperly.

To express these conditions in a more-quantitative fashion, certain currents will be defined.

1. *Diode Currents*

The nominal peak current of the tunnel diodes is I_P. To perform a logical function, peak currents of the two tunnel diodes within a majority circuit are chosen to be unbalanced an amount defined to be ΔI_P. Accuracy to which ΔI_P is specified is defined as δI_P. (In a large network, it is preferable to perform a logical function by initially choosing peak currents of tunnel diodes unequal rather than by using

a bias current applied to terminal A; this is because any bias current at terminal A will contribute to noise current at other circuits.)

2. *Logic Currents*

The total logic current into the majority circuit chosen for study is obtained from a Norton equivalent of the input network. The magnitude of the current source in this equivalent circuit is defined as I_S (see Figure 1). The shunt resistance is R_L. For a two-input logical gate, $I_S = 2I_{LN}$.

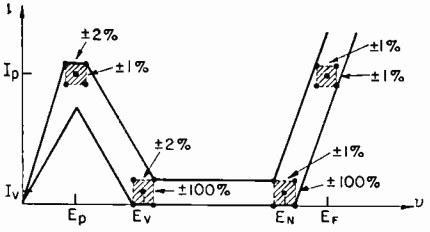
The tolerance on this Norton equivalent current is defined as ΔI_S, which can easily be derived as a percentage of I_S. It will, however, be converted to a current for use in the criterion. ΔI_S is comprised of three components, g_1, g_2, and γ.

The quantity g_1 is defined as the largest per cent amplitude tolerance in the output waveform of a majority circuit caused by diode, resistor, and power-supply tolerances over the region of interest. The region of interest in the output waveform is that region present at the inputs of the circuit chosen for study during its locking interval. (Because of circuit tolerances, the locking time is an interval rather than an instant.) The quantity g_2 is defined as the per cent amplitude tolerance on the output waveform over this same region of interest caused by the logic current itself. Finally, the quantity γ is defined as the per cent tolerance on coupling resistors. An approximate value of ΔI_S expressed as a current rather than as a percentage of I_S is given by

$$\Delta I_S = \frac{1}{100} (g_1 + g_2 + \gamma) I_S. \tag{8}$$

It is assumed in calculations for g_1 that the two diodes, TD_1 and TD_2, for each majority circuit of the network are selected at random from a distribution of tunnel diodes whose linearized characteristics fall within the tolerance range of the piecewise-linear approximation to the tunnel-diode V–I characteristic as shown in Figure 21. Further, it is assumed that the e_g's are identical; i.e., only equal-amplitude variations, within tolerance limits, are allowed in the a-c and d-c components. The equal-amplitude variations in the a-c component arise from two sources. The first source is the variation in the power sources and the associated distribution system to the circuits. The second source is the variation in the voltages reaching the circuits caused by parameter variations in majority circuits which terminate the transmission lines.

g_2 is the result of the following. Since a net logic current entering or leaving a majority circuit must flow through the parallel combination



CIRCUIT		POWER SUPPLY	RELATIVE	ABSOLUTE
R_g	±1%	E_{DC}	±1%	±2.3%
R_c	±2%	E_{AC}	±1%	±2.3%
L	±30% } 150 — Mc	θ	±1.5°	±1.5°
C	±25% }			

Fig. 21—Tunnel-diode, circuit, and power-supply tolerances used in the calculations.

of the load resistance and the internal impedance of the circuit, a voltage across the input–output terminals is produced. This voltage is in addition to any voltage produced by the switching of TD_1 or TD_2. As a result of this voltage, the magnitude of the output voltage of the circuits supplying logic current to the circuit chosen for study is increased by g_2 as long as the net input current to these driving circuits persists. g_2 is conveniently expressed as a function of R_c/R_0. Figure 22 is a graph of g_2 versus R_c/R_0 for $M = 2$ and $M = 3$ and values of

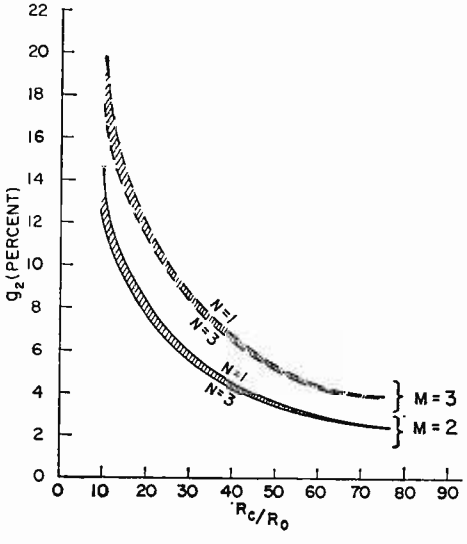


Fig. 22—g_2 as a function of R_c/R_0.

N from 1 to 3 (M is fan-in, N is fan-out). For two-input, two-output circuits of the type discussed in Part I, Figure 22 indicates that g_2 is 10 per cent for 50-ma circuits and 4 per cent for 5-ma circuits.

3. *The Criterion*

The currents I_S, I_x, and I_{UB} are all Norton equivalent current sources, and as such are shunted by the load resistance in addition to the internal impedance, R_0, of the circuit being studied. Therefore, they must be appropriately reduced by the current division factor $R_L/(R_0 + R_L)$ before they can be compared to the diode peak imbalance, ΔI_P.

The two conditions stated previously as necessary for proper circuit operation are now expressed as equations in terms of the currents just defined. The first condition states that

$$\Delta I_P + \delta I_P < [I_S - \Delta I_S - I_x - I_{UB}] \frac{R_L}{R_0 + R_L}. \tag{9}$$

The second condition states that

$$\Delta I_P - \delta I_P > [\Delta I_S + I_x + I_{UB}] \frac{R_L}{R_0 + R_L}. \tag{10}$$

Combining Conditions (9) and (10) gives the criterion on ΔI_P.

$$[I_S - \Delta I_S - I_x - I_{UB}] \frac{R_L}{R_0 + R_L} - \delta I_P > \Delta I_P > [\Delta I_S + I_x + I_{UB}] \frac{R_L}{R_0 + R_L} + \delta I_P. \tag{11}$$

If Condition (11) indicates that a range of allowable values for ΔI_P exists, majority circuits with the tolerances specified should, on the basis of this static analysis, operate properly in a large logic network. If such a range of values does not exist, a workable network cannot be built from elements having the given tolerances.

Since it is only required that a range of ΔI_P exist, ΔI_P can be eliminated and the criterion established on I_S. Thus Condition (11) becomes

$$[I_S - \Delta I_S - I_x - I_{UB}] \frac{R_L}{R_0 + R_L} - \delta I_P > [\Delta I_S + I_x + I_{UB}] \frac{R_L}{R_0 + R_L} + \delta I_P$$

which, when simplified, gives

$$I_S > 2\left[\Delta I_S + I_x + I_{UB} + \frac{\delta I_P(R_0 + R_L)}{R_L}\right]. \tag{12}$$

Condition (12) is a single requirement that must be satisfied by a given majority circuit design if the large logic network is to function properly. One half the amount by which I_S exceeds the right-hand side of Condition (12) is termed the excess input current. It is this current, modified by the factor $R_L/(R_0 + R_L)$, which serves to overcome dynamic problems of balanced-pair circuits.[12]

This criterion on I_S will now be applied to balanced-pair logic networks comprised of typical 50-ma and 5-ma germanium-diode majority circuits similar to those used in the experimental work reported in the first part of this paper.

4. *Application of Criterion*

The results of applying Condition (12) to the 5-ma and 50-ma circuits (see Figure 21 and Table III) are tabulated in Table VI. For purposes of comparison, the currents involved in the criterion have been expressed as percentages of the peak current, I_P, of the respective tunnel diodes.

In Table V the component of I_{UB} from reactive causes reflects the effect of imbalances in the series inductance, L, and shunt capacitance, C, of the tunnel diodes on the steady-state behavior of the circuits at 150 mc. For the 50-ma circuits, this was 1 per cent of I_P while for the 5-ma circuits it was negligible. If the 50-ma circuits were operated at a repetition rate substantially less than 150 mc, this component of I_{UB} could be neglected. However, the excess input current would still be $-0.01\ I_P$.

One other point is worth noting in conjunction with Table VI. Recall that for the 50-ma circuits $R_c/R_0 = 14.4$, while for the 5-ma circuits $R_c/R_0 = 38.4$, a factor of 2.68 difference. This difference in R_c/R_0 between the two circuits reflects itself in the values of I_x where the value for the 50-ma circuit is approximately twice that for the 5-ma circuits. Primarily, this difference in the R_c/R_0 ratio is due to the fact that R_g was not increased in approximately the same proportion that I_P was decreased. That is, if R_g and R_c had been scaled with

[12] J. J. Gibson, G. B. Herzog, H. S. Miiller, and R. A. Powlus, "Tunnel-Diode Balanced-Pair Switching Characteristics," presented at the 1962 International Solid-State Circuits Conference, Philadelphia, Penna.; February 14-16, 1962.

approximately the same ratio as I_P, the characteristics of the 5-ma circuits would have been identical with those of the 50-ma circuits, provided, of course, that the voltage characteristics of the tunnel diodes are invariant with changes in I_P.

The other effect of decreasing I_P without increasing R_g on the waveshape of the output voltage is shown in Figure 23. As previously discussed, the way to increase the width of the flat-top region in the output-voltage waveshape is to increase R_g, all other parameters remaining constant. With these particular circuit examples, R_g was not increased in proportion to the decrease in I_P. Consequently, the width

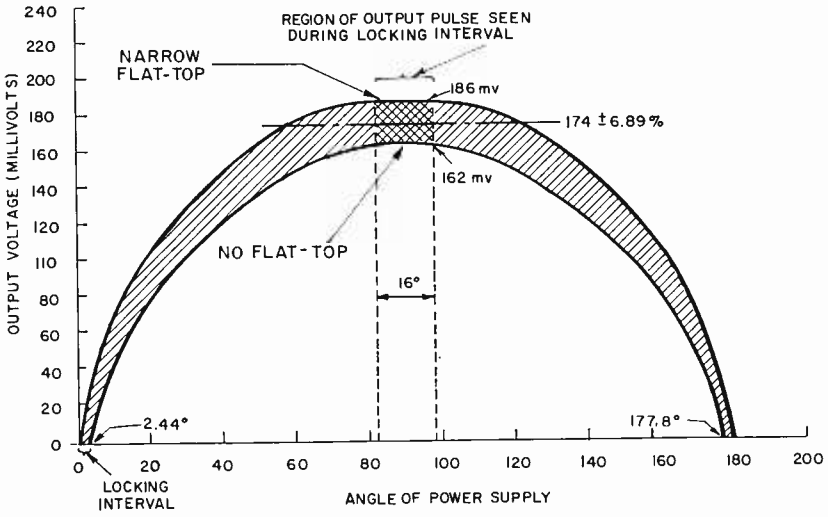


Fig. 23—Calculated output waveform for the 5-ma circuit.

of the flat-top region in the transfer characteristic was reduced and the flat-top region in the output waveshape was all but eliminated, as Figure 23 indicates. For the waveshape shown in Figure 23, the permissible lengths of the interconnecting transmission lines are restricted to 31.2° ± 3.8° in length. (The value 3.8° is an assumed quantity.) Assuming a relative phase error between phases of the three-phase power supply system of ±3.0°, the region of the output waveform seen by circuits in the subsequent phase is 16° wide. Consequently, the nominal value of V_0 is 174 millivolts and its tolerance is ±7 per cent, a value reflected in the ΔI_S entry in Table VI.

These results certainly indicate that a workable balanced-pair logic system can be made with low-peak-current tunnel diodes and the given tolerances. A choice of 5 ma is, perhaps, a little too low due to the

reduction in the flat-top of the output waveshape. An increase in R_g or a doubling of the peak current would probably yield a design where an appropriate compromise is made between noise current and output pulse flap-top. Of course, tolerances on tunnel diodes and circuit components are still rather restrictive. However, this is a worst-case tolerance approach and a procedure for individual trimming of the balanced-pair circuit components would certainly increase the permissible initial variations in parameters.

Table VI

Characteristic	50-ma Circuit	5-ma Circuit
Fan In	2	2
Fan Out	2	2
Nominal Logic Current (I_S)	18% I_P	28% I_P
Total Load Current ($2I_S$)	36% I_P	56% I_P
Feedthrough Current (I_X)	3.1% I_P	1.5% I_P
Imbalance Current (I_{UB})		
Reactive Causes	1.0% I_P	—
Static Causes	2.0% I_P	1.5% I_P
Variation in Nominal Logic Current (ΔI_S)	3.6% I_P	4.2% I_P
Inaccuracy in Peak Current Imbalance (δI_P)	1.0% I_P	1.0% I_P
$2\left[\Delta I_S + I_X + I_{UB} + \left(\frac{R_0 + R_L}{R_L}\right) I_P\right]$	22.0% I_P	16.6% I_P
Excess Input Current	−2.0% I_P	+5.7% I_P

CONCLUSIONS

In Part I, two balanced-pair building blocks were described. Together, these building blocks provide a functionally complete set which amplifies and standardizes logic signals. An individual balanced-pair circuit was operated in excess of a 1-kmc repetition rate. However, only the 5- and 50-ma circuits operating at a 150-mc repetition rate have sufficient gross fan power or logic gain to indicate potential usefulness in high-speed computers.

The major problems of distribution of high-frequency a-c supply voltages and packaging and subsystem fabrication techniques were successfully solved. However, system tolerance requirements remain as the limiting factor in the application of balanced-pair circuits as

building blocks for high-speed computers. A worst-case study of the system tolerance requirements indicates that component and circuit tolerances must be in the one to two per cent region. However, a procedure for individual trimming of the balanced-pair circuits would certainly increase the permissible initial variations in component and circuit parameters and broaden the application of balanced-pair circuits to computers.

Acknowledgment

The authors wish to acknowledge that many of the results reported in the first part of this paper were obtained by the collective efforts of W. E. Barnette, G. A. Brown, and S. Fiarman in addition to those of the authors. The authors also wish to express thanks to their colleagues for many helpful suggestions during the course of this work. In particular, the guidance of J. A. Rajchman and M. H. Lewin and the contributions of J. J. Gibson, W. F. Kosonocky, and C. M. Wine are gratefully acknowledged.

Appendix A—Transfer Characteristic Equations

The important voltages in Figure 16 are listed in terms of circuit and tunnel-diode parameters as follows:

$$V_{x1} = \frac{R_L + r_1}{2R_L + r_1} 2V_V + \frac{R_L r_1}{2R_L + r_1} 2I_V , \tag{13}$$

$$V_{x2} = 2V_P , \tag{14}$$

$$V_{x3} = \frac{R_L + r_1}{2R_L + r_1} 2V_N + \frac{R_L r_1}{2R_L + r_1} 2I_V , \tag{15}$$

$$V_{x4} = 2V_V , \tag{16}$$

$$V_{x5} = \frac{R_L + r_2}{2R_L + r_2} 2V_P + \frac{R_L}{2R_L + r_2} 2V_N + \frac{r_2 R_L}{2R_L + r_2} 2(I_P - I_V), \tag{17}$$

$$V_{01} = V_V - \frac{V_{x1}}{2}, \tag{18}$$

$$V_{02} = \frac{R_L r_1}{R_L + r_1} (I_P - I_V) \quad \text{if} \quad V_{02} \leqq (V_N - V_P), \tag{19a}$$

$$V_{02}' = \frac{R_L(r_1 + r_2)}{R_L(r_1 + r_2) + r_1 r_2} b \quad \text{if} \quad V_{02}' > (V_N - V_P), \tag{19b}$$

$$V_{03} = V_N - \frac{V_{x3}}{2}, \tag{20}$$

$$V_{04}' = \frac{V_V - r_1 I_V}{1 + \dfrac{r_1}{R_L}} \quad \text{if} \quad V_{04}' < (V_N - V_V), \tag{21a}$$

$$V_{04} = \frac{R_L r_1}{R_L(r_1 + r_2) + r_1 r_2} d \quad \text{if} \quad V_{04} \geqq (V_N - V_V), \tag{21b}$$

$$V_{05} = \frac{V_{x5}}{2} - V_P, \tag{22}$$

where

$$V_P = E_P + I_P R_g,$$

$$V_V = E_V + I_V R_g,$$

$$V_N = E_N + I_V R_g,$$

$$V_F = E_F + I_P R_g,$$

$$r_1 = \frac{V_P}{I_P},$$

$$r_2 = \frac{V_F - V_N}{I_P - I_V},$$

$$b = V_P\left(\frac{r_2 - r_1}{r_1 + r_2}\right) + V_N\left(\frac{r_1}{r_1 + r_2}\right) - I_V\left(\frac{r_1 r_2}{r_1 + r_2}\right),$$

$$d = V_V\left(\frac{r_2}{r_1} - 1\right) + (V_N - r_2 I_V).$$

Tunnel-diode parameters E_P, E_V, E_N, E_F, I_P, and I_V are defined in Figure 14. The foregoing equations were derived from purely geometrical considerations of volt–ampere characteristics denoting operation of majority circuits.

As a typical example of the method of deriving the above equations, the derivation of Equation (17) is given.

The limiting case for $2e_g$ such that $|V_o| > 0$ is shown in Figure 24. The procedure of equating currents is employed to derive V_{x5}, the power-supply voltage associated with the limiting condition. In this case, the current through the tunnel diode in the high-voltage region is

$$i = \frac{V_{x5} - (V_N + V_P)}{r_2} + I_V .$$

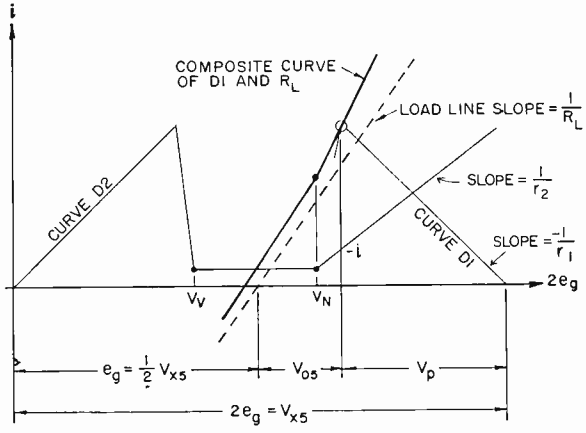


Fig. 24—Characteristic curves used in the derivation of V_{x5}. The effect of R_g is included in curves D1 and D2.

The sum of this current and the current through the load, $i = V_{o5}/R_L$ must be I_P. That is,

$$I_P = \frac{V_{o5}}{R_L} + \frac{V_{x5} - (V_N + V_P)}{r_2} + I_V .$$

The equation for V_{o5}, obtained directly from Figure 24, is

$$V_{o5} = \frac{V_{x5}}{2} - V_P .$$

Solving these two equations for V_{x5} by eliminating V_{o5} gives Equation (17),

$$V_{x5} = \frac{R_L + r_2}{2R_L + r_2} 2V_P + \frac{R_L}{2R_L + r_2} 2V_N + \frac{r_2 R_L}{2R_L + r_2} 2(I_P - I_V).$$

APPENDIX B

Imbalance Voltages

The values of the open-circuit imbalance voltages E_2 and E_3 given in Table IV are obtained in the following manner. E_i is made up of three components. One is due to the imbalances in tunnel-diode volt–ampere characteristics, the second is due to power-supply tolerances,

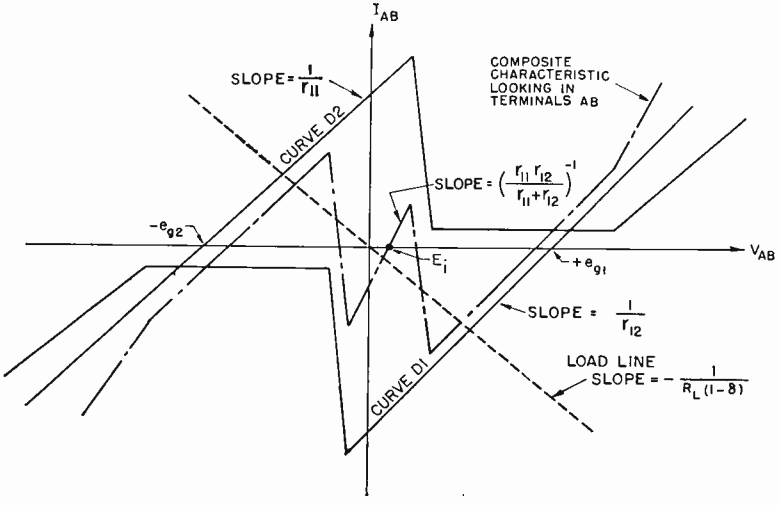


Fig. 25—Characteristic curves used in the derivation of the unbalanced voltage E_i. The effect of R_{g1} and R_{g2}, the internal resistance of power supplies e_{g1} and e_{g2}, is taken into account in curves D1 and D2, respectively.

and the third is due to steady-state reactive imbalances (discussed below). The contributions of the first two components are accounted for in the following equation (see Figure 25):

$$E_i = \left| \frac{\frac{r_{11}}{r_{12}} e_{g1}(t) - e_{g2}(t)}{1 + \frac{r_{11}}{r_{12}}} \right|_{\max} \tag{23}$$

where $e_{g1}(t)$ and $e_{g2}(t)$ are the appropriate values of the two power-

supply voltages for the subscript i. In this equation, r_{11} and r_{12} result from imbalances in the tunnel-diode parameters. They are given by

$$r_{11} = \frac{E_P(1+\beta) + I_P R_g(1+\alpha)(1-\gamma)}{I_P(1+\alpha)},$$

$$r_{12} = \frac{E_P(1+\beta) + I_P R_g(1-\alpha)(1+\gamma)}{I_P(1-\alpha)},$$

where α, β, and γ are tolerances on I_P, E_P, and R_g, respectively. In Equation (23), the maximum value of the right-hand side is obtained while t varies during the time of the locking interval of the circuit chosen for study. A rearrangement of Equation (23) puts it into better form for determining this maximum. It will then be shown that for certain assumptions about the locking interval, the effect of the variation in time can be neglected.

To allow for both relative and absolute tolerances in the two power supplies, let

$$e_{g1}(t) = (1 \pm d_o)E_{DC} + (1 \pm a_o)E_{AC}\sin\omega t$$

$$e_{g2}(t) = (1 \pm d_o)(1 \pm d_1)E_{DC} + (1 \pm a_o)(1 \pm a_1)E_{AC}\sin(\omega t \pm \theta)$$

where d_o and a_o are absolute tolerances and d_1, a_1, and θ are relative tolerances. In this case, $e_{g1}(t)$ has been used as the reference power supply. It is convenient and practical to assume that $d_o = a_o$ and that $d_1 = a_1$. Thus, since $r_{11}/r_{12} < 1$, Equation (23) becomes

$$E_i = E_{AC}\left|\frac{\dfrac{r_{11}}{r_{12}} - (1+d_1)\left[1 + \dfrac{\theta}{\tan\omega t + x\sec\omega t}\right]}{1 + \dfrac{r_{11}}{r_{12}}}(1+d_o)(x+\sin\omega t)\right|_{max} \quad (24)$$

where θ is assumed to be a small angle and is expressed in radians. If a few more assumptions are made, Equation (24) can be even further simplified.

To eliminate the need for determining the maximum value of the right-hand side of Equation (24) during the locking interval of the circuit chosen for study, $x(= E_{DC}/E_{AC})$ is selected such that $\psi = 0°$. Consequently $(d/dt)e_g(t)$ is at its largest possible value, and the elapsed time for $2e_g(t)$ to pass through the locking interval is mini-

mum. Therefore, the variation of $|e_i|_{max}$ with time during the locking interval is assumed to be negligible. Further, assuming that the circuit chosen for study is on phase-two of a three-phase power supply system, E_2 is given by

$$E_2 = \frac{-\frac{r_{11}}{r_{12}} + (1+d_1)\left(1+\frac{\theta}{x}\right)}{1+\frac{r_{11}}{r_{12}}}(1+d_o)\,xE_{AC}, \qquad (25)$$

and E_3 is given by

$$E_3 = \left|\frac{\frac{r_{11}}{r_{12}} - (1+d_1)\left(1-\frac{2\theta}{3.46+x}\right)}{1+\frac{r_{11}}{r_{12}}}\right|(1+d_o)\,xE_{AC}. \qquad (26)$$

The value of E_{AC} to use in Equations (25) and (26) is determined as follows. From Equation (17), Appendix A, V_{x5} is obtained. Its value plus the value of x as obtained from Equation (5) is used with Equation (15) to obtain E_{AC}. This value of E_{AC} has not been reduced to allow for tolerances and thus tends to offset the approximations used in arriving at Equations (15) and (26).

For the parameters of the 5- and 50-ma circuits described in Table III and Figure 21, this procedure yields a value of I_x of 1.45 ma for the 50-ma circuits and 0.075 ma for the 5-ma circuits by interpolation from Table IV.

Reactive Imbalances

To a good approximation, the effect of imbalances in the series inductance, L, and shunt capacitance, C, of the tunnel diodes on the steady-state behavior of the circuits can be accounted for in I_{UB}. Essentially, the process is simply to replace the tunnel diodes with a linear resistor equal to E_P/I_P, to unbalance only the reactive components of the circuit, and to solve for the resulting sinusoidal voltage across R_L. For the 50-ma circuits of Table III and Figure 21, this voltage was only 4.59 mv at 150 mc for $\omega t = 0$. For the corresponding 5-ma circuits, this voltage was negligible. Therefore,

$$E_j = \frac{1}{1 + \dfrac{r_{11}r_{12}}{R_L(1+\delta)(r_{11}+r_{12})}} E_i + V_r ,$$

where V_r is the voltage due to the above-mentioned reactive imbalances. For these 5- and 50-ma circuits

$$1 > \frac{r_{11}r_{12}}{R_L(1+\delta)(r_{11}+r_{12})} .$$

MICROAPERTURE HIGH-SPEED FERRITE MEMORY

By

R. Shahbender, T. Nelson, R. Lochinger, and J. Walentine

RCA Laboratories
Princeton, N. J.

Summary—A novel approach to the fabrication and operation of ferrite elements for random-access memories with a read–write cycle time of 100 nanoseconds is described. The fabrication technology involves the use of electron-beam drilling to form microapertures, and printed wiring for ease of assembling. Experimental data for both the element fabrication and operation are presented.

Introduction

PRESENT-DAY DIGITAL COMPUTERS employ ferrite cores for random-access storage. Available memories, operating in a current-coincident mode, have capacities up to approximately 2×10^6 bits and cycle times in the neighborhood of 10 microseconds.[1] Shorter cycle times, around 1 microsecond, have been achieved in commercial systems by resorting to a word-organized mode of operation.[2] Because of the increased cost of the required electronic circuitry, bit capacities in the latter type are in general less than those of a coincident-current storage.

Impulse switching techniques[3] together with advanced fabrication technologies are being used to reduce cycle times to the vicinity of 100 nanoseconds. This paper presents results which establish the feasibility of medium-size, random-access ferrite memories with cycle times of 100 nanoseconds. This goal, which has also been sought through an approach based on magnetic thin films,[4,5,6] is achieved by the well-established technology of ferrites.

---

[1] J. A. Rajchman, "Computer Memories: A Survey of the State-of-the-Art," *Proc. I.R.E.*, Vol. 49, p. 104, Jan. 1961.

[2] J. A. Rajchman, "Ferrite Apertured Plate for Random Access Memory," *Proc. I.R.E.*, Vol. 45, p. 325, March 1957.

[3] R. E. McMahon, "Impulse Switching of Ferrites," *Digest of Technical Papers, Solid State Circuits Conference*, Philadelphia, Pa., p. 16, Feb. 1959.

[4] A. V. Pohm and E. N. Mitchell, "Magnetic Film Memories—A Survey," *Trans. I.R.E. PGEC*, Vol. EC-9, p. 308, Sept. 1960.

[5] Raffel, et al., "Magnetic Film Memory Design," *Proc. I.R.E.*, Vol. 49, p. 155, Jan. 1961.

[6] W. E. Proebster, "The Design of a High-Speed Thin Magnetic Film Memory," *1962 International Solid State Circuits Conference*, Philadelphia, Pa., Feb. 1962.

The general philosophy adopted for the program is

(1) miniaturization of the size of the storage element to attain high speed;

(2) use of printed-circuit techniques to facilitate fabrication and assembly.

The miniaturization of the element results in power requirements for high-speed switching that are compatible with semiconductor devices. The use of printed-circuit techniques permits the use of automatic fabrication processes with potential cost reduction.

Electron-beam milling, a recently developed fabrication process, opens up new vistas in microminiaturization. The use of this technique to form micromagnetic elements, as described in this paper, is timely, since the minimal size limits attainable lie between those achieved by present techniques and those to be expected from research in the area of miniaturization by controlled crystal growth. Further, the automatic programming of milling operations is easily accomplished by controlling the position, energy, and size of the milling tool, i.e., the electron beam. The process is particularly suited to automation since the variables are naturally suited to electronic control.

Ferrite Switching Characteristics

The switching characteristics of a toroidal core are described by the well-known relationship[7]

$$T_s\,(H - H_c) = S_w\,,$$

where T_s = switching time,

H = applied magnetic reversing field,

H_c = coercive field of the core,

S_w = switching constant characteristic of the core composition.

This relationship has been experimentally verified over a large range of applied fields and for a variety of material compositions (both ferrites and magnetic metals). The experiments indicate a decreasing value of S_w for high fields.[8]

---

[7] N. Menyuk and J. B. Goodenough, "Magnetic Materials for Digital Computer Components," *Jour. Appl. Phys.*, Vol. 26, No. 1, p. 8, 1955.

[8] W. Lee Shevel, Jr., "Millimicrosecond Switching Properties of Ferrite Computer Elements," *Jour. Appl. Phys.*, Supplement to Vol. 30, No. 2, p. 475, 1959.

Irrespective of the mechanism involved (rotational or domain-motion switching), experiments have shown that a core may be switched in a few nanoseconds by the application of a sufficiently high drive field. For the case where $H \gg H_c$ the switching relation reduces to

$$T_s I \simeq 2\pi r_0 S_w$$

where I = applied reversing current (assuming single-turn windings) and r_0 = average core radius.

Since a core is a closed magnetic path, there are no demagnetizing fields present. This implies that the average core radius is not limited by fundamental considerations due to demagnetizing effects. Thus, for a given switching speed, the current required to reverse the flux around an aperture is reduced by reducing the average radius of the aperture, r_0, and/or the switching constant of the material.

For a toroidal geometry, the switching current decreases linearly with decreasing radius. The current-carrying capacity of a conductor linking the core decreases as the square of the radius. This places a lower limit on aperture radius given by

$$r \geqslant \frac{2 S_w}{K T_s} = 0.55 \times 10^{-6} \text{ meter } (= 0.02 \text{ mil}),$$

where

$K = 10^9$ amperes per square meter = permissible conductor current density,

$T_s = 30$ nanoseconds = switching speed required for 100-nanosecond memory,

$S_w = 8.3 \times 10^{-6}$ ampere-second/meter (0.1 oersted-microsecond) = lowest switching coefficient measured for ferrites.

For a core of average radius r_0, radial extent Δr, and axial length L, the energy E required to switch it, and the output voltage V derived from it are

$$E \propto \frac{S_w L}{T_s} r_0 \Delta r, \quad V \propto \frac{L \Delta r}{T_s}.$$

The ratio of output voltage to energy, which may be considered as a figure of merit for magnetic elements, is

$$\frac{V}{E} \propto \frac{1}{S_w r_0}.$$

This ratio may be increased at constant output voltage by reducing the effective core size. The output voltage is determined by the product of L and Δr. For obvious reasons Δr must be kept small (a fraction of r_0). The axial length, L, may not be made arbitrarily large to obtain arbitrarily large output voltages since this introduces delay and slows

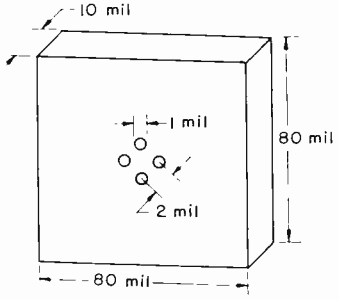


Fig. 1—Geometry of a microaperture ferrite element.

the memory cycle. Thus, depending on the actual memory-element configuration, a specified value of L must be used representing a compromise between output voltage and delay.

The expressions given above may be used to estimate the element size required for a given drive current. Drive-current limitations exist since the memory is to be operated with associated electronic circuits capable of delivering the required pulses at a 10 mc repetition rate. If a drive current of 200 ma (a reasonable value for solid-state devices) and a switching time of 30 nanoseconds are assumed, the average core radius is

$$r_0 \leqslant \frac{T_s I}{2\pi S_w} = 120 \times 10^{-6} \text{ meter } (\simeq 5 \text{ mils} = 0.005 \text{ inch}).$$

Memory Element and System Organization

The memory element selected consists of a ferrite wafer 80 × 80 × 10 mils. Four apertures with a diameter of 1 mil each and a center-to-

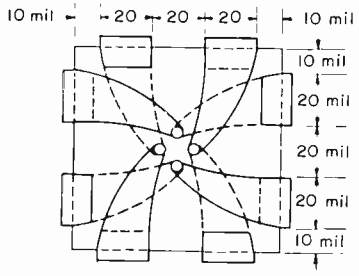


Fig. 2—Winding pattern for microaperture element.

center spacing of 2 mils are electron-beam drilled in the center of the wafer as shown in Figure 1. Four separate windings, each linking an aperture in the pattern shown in Figure 2, are fabricated by photo-etching techniques to give a wired element. The elements are assembled in a mosaic and the individual windings are interconnected by mass fabrication techniques to give a wired memory plane as shown schematically in Figure 3.

The memory is operated in a word-organized, two core per bit mode[2] under impulse switching conditions. The two X-directed windings are for the word currents; the read and write currents are applied to different windings. The two Y-directed windings are for digit and sense. The effective internal diameter of an equivalent core is approximately 4 mils (this is the diameter of the circle circumscribing the four apertures). The effective external diameter is determined by the magnitude of the switching currents.

A two-wire system is also possible (and in fact may be preferable) in which bipolar pulses for read–write are applied to the X-directed winding, and the Y-directed winding is used for digit-sense. The ferrite element and winding patterns are suitably modified by having two apertures per wafer (each with a diameter of 1 mil and a center-

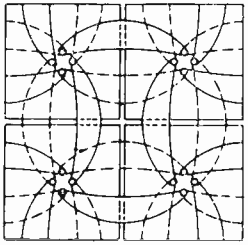


Fig. 3—Mosaic of interconnected wafers (four wire system).

to-center spacing of 2 mils) instead of four: the winding pattern is shown in Figure 4.

The four-wire system reduces the burden on the electronic drive circuitry since unipolar pulses may be used on the word lines. The advantage in having separate digit and sense windings is only marginal because of the inherent tight coupling between these windings. The two-wire system requires bipolar pulses on the word lines. However, it offers an advantage in halving the number of apertures and interconnections. The reduction in the number of windings per wafer

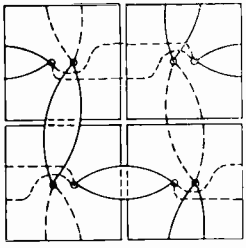


Fig. 4—Mosaic of interconnected wafers (two wire system).

permits the use of rectangular wafers with a reduced dimension in the digit direction. This decreases propagation delays along the digit-sense windings which is of importance for high-speed operation.[9]

Memory Fabrication Technology

*Ferrite Wafer Fabrication**

Dry-pressing techniques are utilized to fabricate the ferrite wafer blanks for the memory system. Investigations were conducted to determine optimum conditions (composition, particle size, binder content, compacting pressure, firing schedule, etc.) for fabricating blanks with the required magnetic characteristics and a high degree of dimensional tolerance to permit mosaic assembly. As a result of these investigations, blanks were fabricated with nominal dimensions of 80 × 80 × 10 mils, with tolerances of ±0.5 mil in lateral dimensions, and ±0.1 mil in thickness; an 80 per cent yield was obtained. The compositions

---

[9] J. A. Rajchman, "Computer Memories—Possible Future Developments," *RCA Review*, Vol. 23, p. 137, June 1962.

* This phase of the work was conducted at the RCA Semiconductor and Materials Division—Ferrite Operation, Needham Heights, Mass., under the direction of J. J. Sacco.

used are of the conventional variety, with the metal ion content and final firing temperature adjusted to give the required magnetic characteristics. For the composition selected, the coercive force is approximately 1.0 oersted and the switching coefficient is 0.3 oersted-microsecond. A variation in firing temperature of more than ±20°C is sufficient to cause serious deterioration in the high-speed switching characteristics.

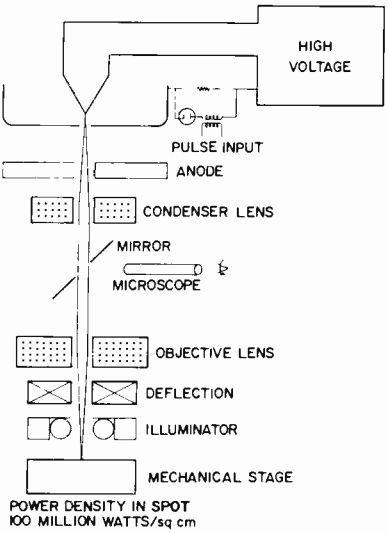


Fig. 5—Schematic of the electron-beam drilling machine.

Microaperture Drilling†

The microapertures are formed in the blank wafers by electron-beam drilling. In this technique, a beam of high-energy electrons is focused onto the work piece in the manner indicated schematically in Figure 5. The energy of the incident electrons is absorbed at the point of impact by the work piece and converted to heat. Exceedingly high power densities (10^8 watts per square centimeter) are attained resulting in the local generation of very high temperatures and high temperature gradients. To protect the work piece thermally and con-

† This phase of the work was performed using the electron-beam milling facility of L. R. Industries, Mt. Vernon, N. Y., available on a jobbing basis. A description of this facility is included in the "Proceedings of Annual Symposium on Electron Beam Processes," held by the Alloyd Corporation on March 24-25, 1960.

fine the elevated temperature zone to the impact region, a pulsed beam is used. For ferrites, the locally generated heat is sufficient to sublimate the material without causing excessive recrystallization in neighboring regions.

In drilling the microapertures in the ferrite wafers, beam voltages in the range of 80 to 100 kilovolts, peak beam currents in the range of 150 to 200 microamperes, pulse widths of 10 microseconds and a pulse repetition rate of 100 per second were found optimum. The beam is focused under these conditions to produce an aperture having a diameter of 1 mil. The experimental work performed indicates that the optimum drilling conditions depend on the ferrite composition and the thickness of the work piece. An increase in wafer thickness requires a higher drilling voltage. Samples as thick as 30 mils were successfully drilled by increasing the beam voltage to 135 kilovolts.

Under optimum focusing conditions, the electron-beam drilling machine used for the experimental work produced apertures with a diameter of 0.3 mil. To drill larger-diameter apertures the beam is de-focused. This results in a nonoptimum power-density distribution across the beam, a reduction in the temperature gradient in the work piece, and an increase in the size of the recrystallized zone surrounding the drilled apertures. Overcoming this difficulty would require a redesign of the electron optics.

To drill the four-aperture pattern of Figure 1, the beam is sequentially deflected to the four positions by energizing the deflection coils shown in Figure 5 from a relay control unit.

To facilitate the drilling operations, the semiautomatic jig shown in Figure 6 was designed and built. The function of the jig is to precisely position wafers, supplied from a storage magazine, under the drilling beam and to remove the wafers after they are drilled. The precision in positioning the wafers under the beam is necessary to facilitate fabrication of the windings. The jig is made of nonmagnetic stainless steel and is actuated via a flexible shaft and rotary vacuum seal by an electric motor mounted outside the vacuum chamber. The jig must be operated without lubricants because of the deleterious effects of the high x-ray levels generated during drilling. The supply magazine has a capacity of 120 wafers which are manually loaded prior to insertion in the machine. The drilling rate of 6 wafers per minute achieved is mainly limited by operation of the jig rather than the time required for the actual drilling.

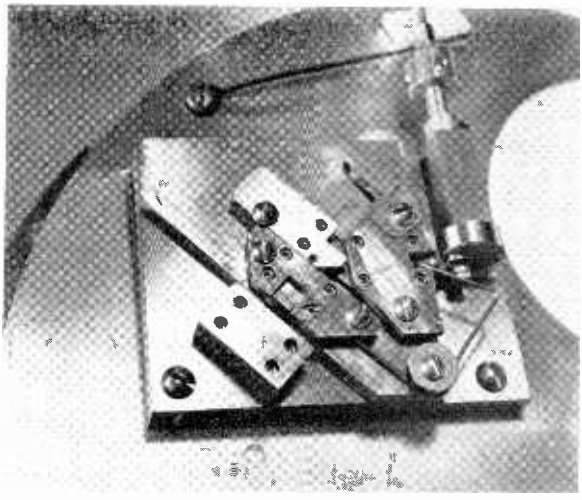


Fig. 6—Drilling jig.

Figure 7 is a micrograph of a polished section through two apertures in an 8.8-mil-thick wafer. The recrystallized zone is clearly

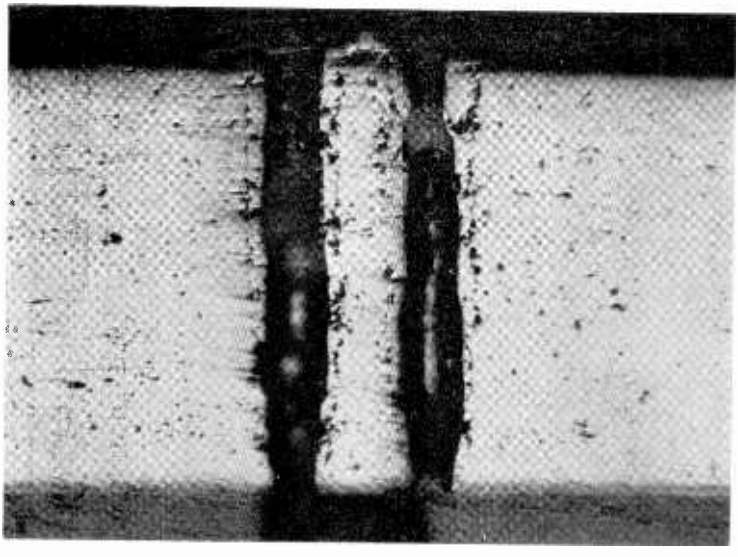


Fig. 7—Micrograph of section through two electron-beam-drilled apertures.

visible. In addition, a small crater and mound can be seen at the top of the sample corresponding to the entry side of the beam. The crater and mound formation seems to be inherent in electron-beam drilling, and necessitates lapping the entry surface prior to fabricating the windings. Figure 8 is a micrograph of the surface of a sample after lapping. Again, the recrystallized zone can be clearly seen.

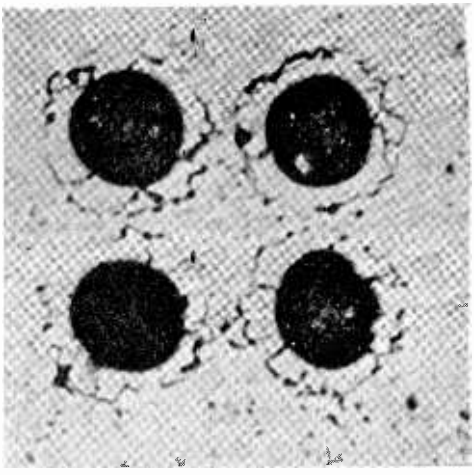


Fig. 8—Micrograph of the surface of a lapped wafer.

*Winding Fabrication**

The following three-stage process is used to fabricate the windings on the individual wafers:

(1) The apertures are filled with a conducting paste consisting of a mixture of finely powdered silver and silicone oil. The paste is placed on a glass substrate and the wafers are pressed into it. This forces the paste into the apertures. The paste is sintered at a low temperature and the surfaces of the wafers are lapped to remove the excess paste and the crater and mound formed during the electron beam drilling. Figure 9 shows a photomicrograph of the cross section of an aperture with the sintered silver paste in it.

(2) The two surfaces of the wafer are metalized by vacuum evaporation with an 0.5-mil-thick layer of copper. The deposited

* This phase of the work was conducted at the RCA Electron Tube Division, Harrison, N. J., in the Chemistry and Physics Laboratories under the direction of N. Freedman.

copper surface is a replica of the ferrite surface and under proper illumination shows the location of the apertures as depressions.

(3) The metalized wafers are coated with photoresist, optically aligned in a high magnification system with a photomaster and exposed to ultraviolet radiation. The copper is then etched to give the required winding pattern after which the photoresist is removed.

Because of the high precision attained in drilling the apertures with respect to a reference corner, coarse alignment (within a few tenths of a mil) is achieved by the jigging fixtures; thus the final alignment requires only small motions of the wafer with respect to the photomaster.

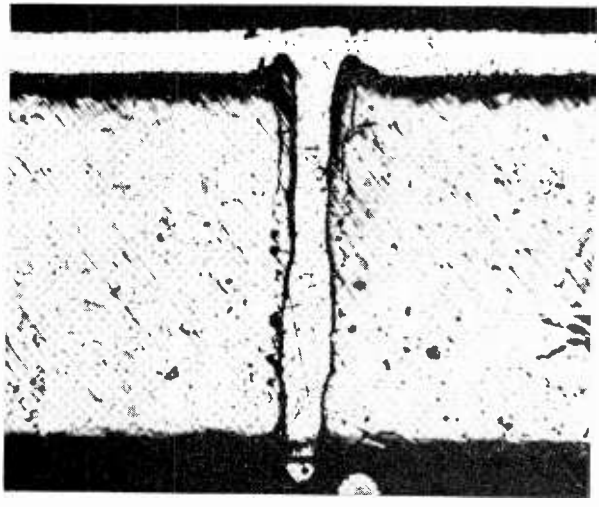


Fig. 9—Micrograph of section through drilled aperture showing injected silver conductor.

The electrical resistance of the silver plugs, as measured by two fine probes, had a minimum value of 0.04 ohm. A total winding resistance of 0.1 ohm was acceptable, and those showing a higher value were rejected.

Mosaic Assembly

The winding pattern shown in Figure 2 is designed to permit all interconnections to be performed from one surface. This is accomplished by having the windings overlap the edges of the wafer. To interconnect the wafers a printed circuit board with a pattern of holes

and interconnecting tabs is fabricated. The holes are 55 mils in diameter and the interconnecting tabs are photoetched in the copper. A low-temperature solder is electroplated onto the board prior to etching. The wafers are assembled into a mosaic on the board and are held in position by the application of a vacuum to the back surface of the board. The entire assembly is heated to effect the soldering of the wafers to the interconnecting tabs.

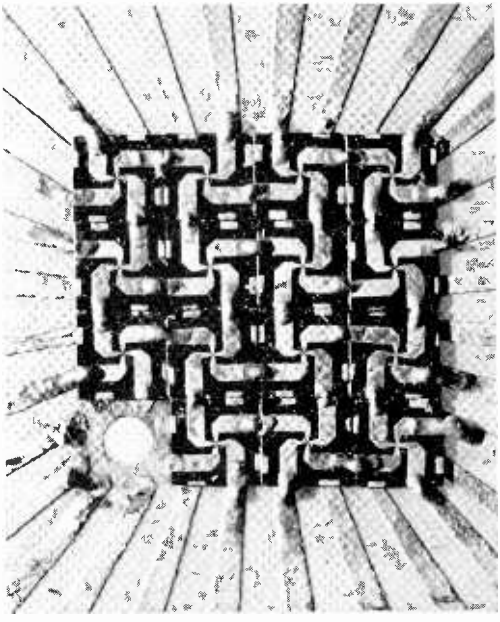


Fig. 10—4 × 4 mosaic of microaperture wafers.

Figure 10 is a photograph of a 4 × 4 mosaic assembled in this fashion. The corner wafer is removed to show the hole and interconnecting tabs. Because of difficulties encountered in having the windings overlap the edges of the wafers, the interconnections on the top surface of the mosaic were manually soldered. An improved assembly technique is under development to permit the interconnections to be made on both surfaces. This eliminates the need for having the windings overlap the edges of the wafers.

In addition to the 4 × 4 mosaic shown in Figure 10, a 4 × 8 mosaic was assembled. Total winding resistance of the 4 × 8 mosaic ranged from a low value of 0.2 ohm to a high value of 10 ohms. A 12 × 16 mosaic is presently being assembled.

Operating Mode

The mode of operation selected for the memory is word-organized with two wafers per bit. In this mode all bits of a selected word are subjected to the same read–write current pulses. The optimum digit drive technique,† selected on the basis of experimentation, applies a digit pulse to either one or the other of the two wafers of a bit in time coincidence with the write pulse and of such a polarity to always add to it. In other words, if the two wafers of a bit are labeled A and B, wafer A is digited to write a binary "1" and wafer B is digited to write a binary "0," the polarity of the digit pulses in both cases being chosen to add to the write current pulse.

Sensing is differential in that the output sense voltage obtained during read is the difference between the two voltages induced along the digit-sense windings linking the two wafers of a bit. The sense voltage corresponding to the two binary states is bipolar since the difference in the irreversible flux switched in the two wafers of a bit is positive or negative depending on which of the two wafers received the digit pulse.

The digit-sense windings link corresponding wafers in all words of the memory. Thus the digit pulses, unless controlled in magnitude, will disturb the information stored in the memory. The effect of the digit pulses acting to disturb the stored information is minimized by the digiting technique described above. Alternative digiting techniques (e.g., a binary "1" is entered by adding magnetomotive force to wafer A and subtracting it from wafer B by digit pulses, and the reverse for binary "0") may in principle result in larger sense voltages for the same magnitude currents; however, experimentally it was found that the sense voltages were reduced to zero or even reversed in polarity under appropriate disturb conditions. The alternative digiting techniques investigated always resulted in sense outputs considerably smaller than those obtained with the technique described above, when fully disturbed, and with the current amplitudes adjusted to optimum.

The observed disturb effects indicate that a partially switched ferrite element has a considerably higher disturb threshold for current pulses tending to switch additional flux in the element than for current pulses of the opposite polarity. For the digiting technique selected, the disturb pulses are unipolar and of the same polarity as the write current, resulting in minimal changes in the sense output

† This technique was suggested and verified by H. Amemiya of RCA Electronic Data Processing, Advanced Development, Pennsauken, N. J.

voltages as a result of the application of disturb pulses following writing and prior to reading.

In a random-access memory operating with a cycle time of 100 nanoseconds, digit disturb pulses may occur at a minimum time separation of 100 nanoseconds and a maximum repetition rate of 10 mc after the initiation of writing at a given location and prior to reading at that location. The total number of applied disturbs is essentially unlimited. As is to be expected, the repetition rate at which the disturb pulses occur influences the degree to which they disturb the magnetic states of the two wafers constituting a bit. To a first order this may be explained on the basis of the change in average value of a long sequence of unipolar pulses of fixed width and amplitude and variable repetition rate. The higher the repetition rate, the higher the average value of the pulse train and the greater is the disturb effect. Further, since the digit pulses are time limited, each disturb pulse can produce partial effects only. Thus the full disturb effects can only be assessed by applying a large number (of the order of a hundred) of disturb pulses.

The minimum elapsed time between writing and the application of disturb pulses is of great importance in determining the effect of the disturb pulses. In general, for the compositions tested, the disturb effects decreased with increasing minimum elapsed time up to 0.5 microsecond. Beyond 0.5 microsecond, no further decrease was evident. Similar effects have been reported by others[10] and are explained in terms of relaxation mechanisms. The experimental work performed indicates that this effect is material dependent; in the composition selected for the memory, the effect is minimized.

Experimental Data

Ferrite Compositions

Ferrite compositions investigated are of the conventional square-loop type with variable metal-ion concentrations. Both hand-wired electron-beam-drilled wafers and toroids were pulse tested to determine high-speed switching characteristics. The toroids were also used to obtain low-frequency hysteresis loops. The results indicate a dependence of switching coefficient, coercive force, squareness ratio (defined as the ratio of remanent flux to saturation flux), and Curie temperature on the concentration of the metal ions. The minimum

[10] W. Lee Shevel, Jr., personal communication to J. A. Rajchman.

switching coefficient measured is approximately 0.15 oersted-microsecond, with a corresponding coercive force of 0.1 oersted, Curie temperature of 70°C, and a squareness ratio of 0.5. The material selected for the memory has a switching coefficient of 0.3, a coercive force of 1.0, a Curie temperature of 100°C and a squareness ratio of 0.7.

Bit Operation

A number of wafers of different compositions are electron-beam drilled with the two-aperture geometry of Figure 4 (1-mil diameter

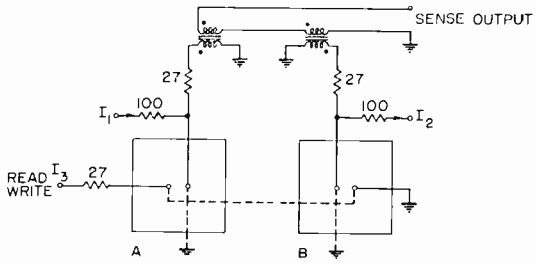


Fig. 11—Circuit used to test memory bit.

on 2-mil centers). Two wafers of a kind are hand wired (using 0.7-mil-diameter wire) and mounted on strip-line board for operation as a memory bit. A schematic of the circuit configuration is shown in Figure 11. Read, write, and digit pulses are provided by transistor drivers (fixed pulse width of 30 nanoseconds at the base and adjustable amplitude) triggered by commercially available 10-mc logic building blocks. The sense output transformers have a 1:1 turns ratio (10 turns on each side) wound on ferrite beads.

Three basic pulse programs are used to evaluate the performance of a bit. These are

(1) alternate "One–Zero" read–write,

(2) alternate "One–Zero" read–write with disturbs,

(3) mixed "One's" and 'Zero's" read–write with disturbs.

1. *Alternate "One–Zero" Read–Write*

In this program an alternating pattern of "1" and "0" is cyclically written into, and read out of the memory bit at a cycle time of 100 nanoseconds and a repetition rate of up to 10 mc. Figure 12 shows the pulse program used and Figure 13 shows oscillograms of the volt-

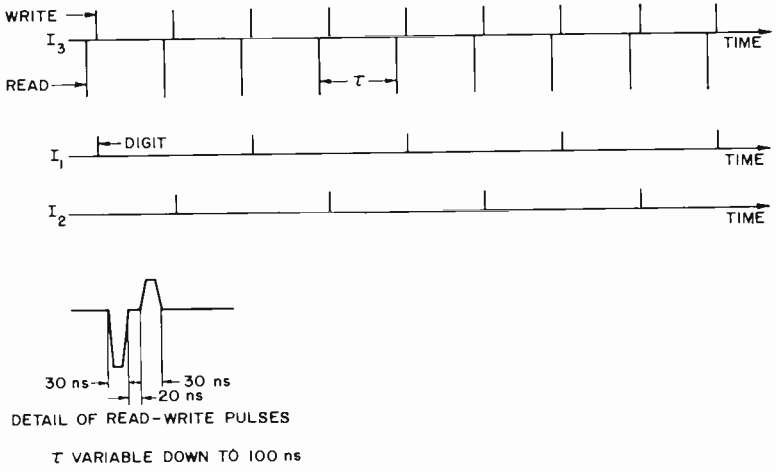


Fig. 12—Alternate "one" and "zero" pulse program.

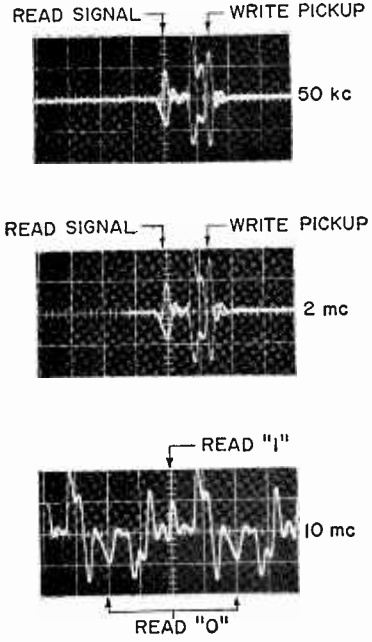


Fig. 13—Sense output voltages at 0.05, 2, and 10 mc (pulse program of Figure 12).

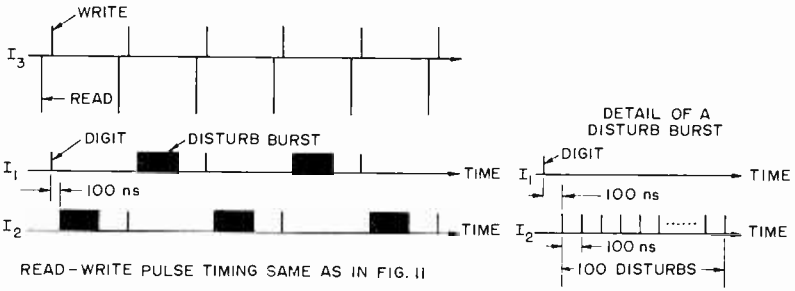


Fig. 14—Alternate "one" and "zero" with disturbs pulse program.

age developed at the sense output terminals under constant drive conditions and at three different repetition rates: 0.05, 2.0, and 10 mc. The "1" and "0" outputs are shown superimposed at the lower repetition rates and separated by 100 nanoseconds at the 10 mc repetition rate. Inspection of Figure 13 shows that the sense voltage is independent of repetition rate. The operating current levels and sense outputs are:

read current: 600 ma
write current: 250 ma
digit current: 45 ma
undisturbed sense output: ±85 mv

2. *Alternate "One–Zero" Read–Write with Disturbs*

In this program an alternating pattern of "1" and "0" is cyclically written into the memory bit. Each write operation prior to reading is followed by the application of disturb pulses aimed at destroying the stored information. Figure 14 shows the pulse program and Figure 15 shows oscillograms of the voltage developed at the sense output terminals for the same current-drive levels as above.

The disturbed sense voltages are ±65 mv; a decrease of 20 mv due

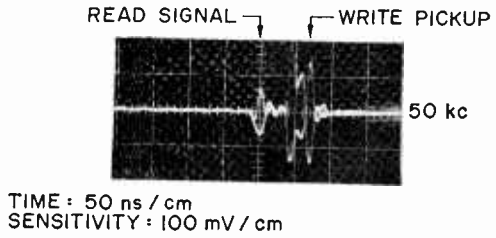


Fig. 15—Sense output voltages with 10 mc disturbs (pulse program of Figure 14).

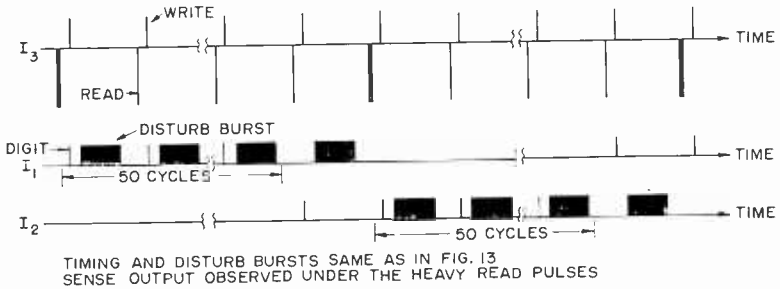


Fig. 16—Mixed "one" and "zero" with disturbs pulse program.

to the digit disturbs. Experimentally it was determined that 3×10^5 disturb pulses produced no additional disturb effects as compared to only 100 pulses.

3. *Mixed "One's" and "Zero's" Read–Write with Disturbs*

The preceding pulse program is not the most pessimistic. A further deterioration of the sense signal occurs if the following pulse program is applied: a large number of "1"'s, each followed by disturbs in the "1" direction is written and read from the bit; this is followed by a single "0", which is then disturbed in the "1" direction. This "0" is then read out and the output voltage recorded. The mirror image of this program is then applied, and a "1" read out and recorded. The program is shown in Figure 16; Figure 17 shows oscillograms of the voltage developed at the sense output terminals for the same current levels as above. The sense voltages obtained are ±55 mv. Comparing Figures 13, 15, and 17, a progressive decrease in output voltage is noted. It is felt that the pulse program of Figure 16 represents a sufficiently stringent test so that a memory bit that yields the acceptable output of Figure 17 under the conditions of the test will perform satisfactorily in a computer under random conditions.

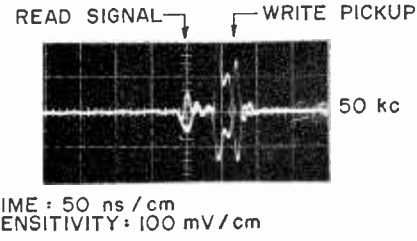


Fig. 17—Sense output voltages with 10-mc disturbs (pulse program of Figure 16).

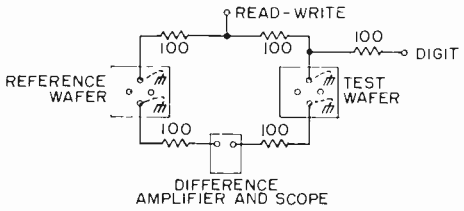


Fig. 18—Circuit for testing uniformity of drilled wafers.

Uniformity of Electron-Beam-Drilled Wafers

The uniformity of the magnetic characteristics of electron-beam-drilled wafers is obviously of importance in determining the feasibility of this fabrication process. A measure of this uniformity is obtained by measuring the difference in output voltages between a reference wafer and a test wafer for the same read current pulse and the following write conditions:

(1) Both wafers subjected to equal write pulses ("0" state),

(2) The reference wafer is subjected to the write pulse and the test wafer is subjected to a write plus digit pulse ("1" state).

The circuit configuration used is shown in Figure 18. The data obtained for four groups with a total of 34 unselected, hand-wired wafers is plotted in Figure 19. The four groups were drilled in succession under the same operating conditions with the vacuum released and the machine pumped down after each group drilling. The test current pulses are 50 nanoseconds wide at the base and have the

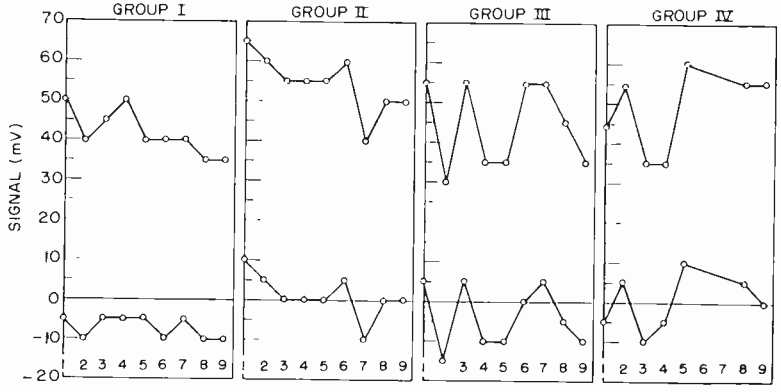


Fig. 19—Uniformity of "1" and "0" outputs of drilled wafers.

following amplitudes:

read current: 400 ma
write current: 200 ma
digit current: 50 ma

The data of Figure 19 shows a spread of approximately 25 mv in the "1" output and a somewhat smaller spread in the "0" output. This spread in outputs is tolerable for operation with the sense voltages shown previously. However, since each wafer is fabricated with its individual windings, automatic pretesting with segregation into batches prior to assembly is feasible.

Temperature-Rise Measurement

The average power required to switch a wafer at a 10 mc repetition rate is approximately 200 milliwatts. The temperature rise above ambient, experimentally measured with a miniature thermocouple having a 3-mil-diameter junction bead in contact with a hand-wired wafer switched by a 10 mc sine wave, is 35°C for a low coercive force material (0.1 oersted) and 24°C for a high coercive force material (0.8 oersted) for a drive current peak amplitude of 200 ma.

The temperature-rise data given above indicates undesirable heating effects. The situation is alleviated by the presence of the large radiating surfaces of the printed conductors in intimate contact with the ferrite in the region of the microapertures. These surfaces are effective in providing the necessary cooling. In addition, the output sense voltages shown in Figure 13 show no deterioration with increased repetition rate up to 10 mc. Thus heating is not a serious problem for a high-speed ferrite memory.

Circuitry

Three basic circuits are required for a word-organized random-access storage. These are

(1) word drivers,
(2) digit drivers,
(3) sense amplifiers.

Word Drivers

The word drivers are to deliver the read–write currents to individual words. A diode matrix is normally used to reduce the number of drivers. For a two-wire system, a bidirectional diode matrix is needed. For a read–write cycle time of 100 nanoseconds, the word

drivers must be capable of delivering externally triggered pulses with a base width no greater than 30 nanoseconds at a maximum repetition rate of 10 mc. The maximum word length is determined by the breakdown voltage of the output transistor in the drivers. The back voltage developed along a word line is in the range of 300 to 500 millivolts per wafer depending on the magnitude of the switching current. High-speed, high-current transistors with collector breakdown of 50 volts are commercially available. This implies that word lengths of 25 to 40 bits (50 to 80 wafers per word) are feasible.

The load impedance presented by a selected word may be considered as lumped, and is highly resistive. This is valid since the number of

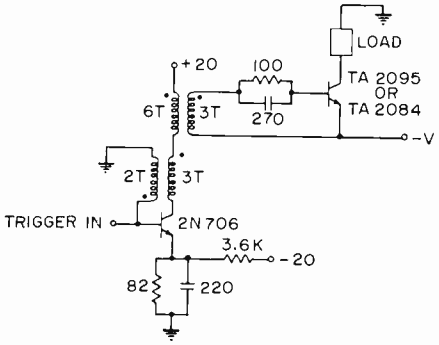


Fig. 20—Two-stage transistor driver (negative polarity output).

bits per word is normally small, so that propagation effects in the word direction are negligible. Further, the switching characteristics of a square-loop element from an energy point of view are such that it is to a first order approximation equivalent to a resistor. For a two-wafer-per-bit system with bipolar sense output, the load impedance presented by the word line is constant independent of the stored information.

Driver Circuits

The two-stage transistor driver shown in Figure 20 was designed, built, and tested. With the RCA developmental type TA2084 transistor (140 volts collector breakdown) for the output stage, current pulses of 300 ma into 300 ohms and repetition rates up to 10 mc were achieved, as shown by the oscillograms in Figure 21.

Positive current pulses with the same characteristics as the negative ones are obtained by modifying the output stage of the circuit of

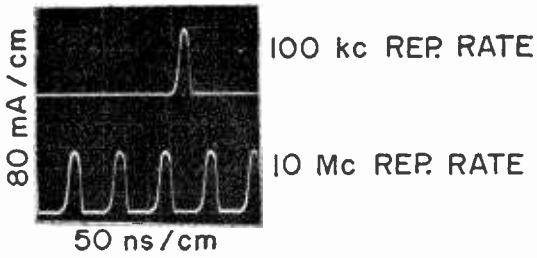


Fig. 21—Oscillogram of the current output into a 300-ohm load of a positive polarity driver.

Figure 20 to that of Figure 22. Positive and negative drivers are interconnected in the manner shown in Figure 23 to deliver bipolar pulses into a common load. The two drivers are interconnected via back-biased diodes to permit operation close to the collector breakdown, i.e., the voltage transient induced in the load due to the positive pulse is absorbed by the diode in the negative driver circuit and vice versa.

Bidirectional Diode Matrix

A square diode matrix with $\sqrt{N}$ rows and $\sqrt{N}$ columns will drive a memory with a capacity of N words. For a bidirectional matrix the number of unipolar drivers is $4\sqrt{N}$. Half of the drivers may be transistor switches, e.g., in Figure 24, A_i and B_i may be drivers and C_i and D_i may be switches.

The diodes must have fast reverse recovery, high forward conductance, high reverse voltage breakdown, and low junction capacitance. The fast recovery is necessary for high-speed random access. High forward conductance decreases diode dissipation and allows more of the voltage developed by the driver to overcome the back voltage due to flux switching, i.e., longer words. The reverse breakdown must be approximately the same as the back voltage developed across the load.

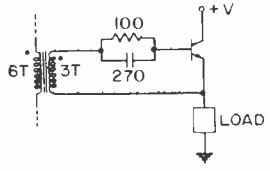


Fig. 22—Second stage of transistor driver connected for positive polarity output.

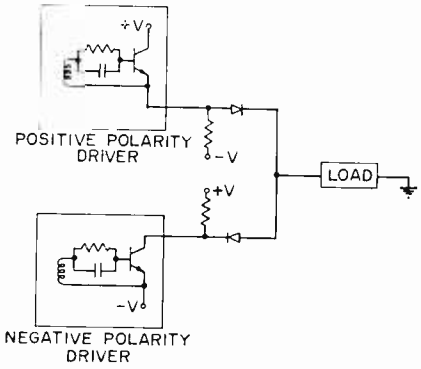


Fig. 23—Bi-directional driver.

Low junction capacitance reduces the current drain on the drivers since each A_i or B_i driver (Figure 24) operates into a load consisting of the selected word line in parallel with the capacitance of $(\sqrt{N}-1)$ back-biased diodes. Each C_i or D_i driver operates into a load consisting of the selected word line in parallel with $(2\sqrt{N}-1)$ back-biased diodes.

The RCA developmental type TA1126 diodes, as well as other commercially available diodes have characteristics compatible with the above requirements. The 2×2 bidirectional matrix shown in Figure 25 was built and operated at a 10-mc repetition rate. Three of the loads shown are 51-ohm resistors, and the fourth is effectively a 48-bit (96-wafer) word. This load consisted of four ferrite plates each

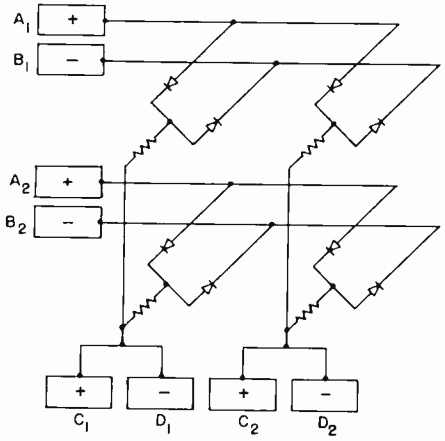


Fig. 24—2×2 bi-directional diode matrix (simplified schematic).

having dimensions of 300 × 300 × 10 mils with a 4 × 6 array of electron-beam-milled aperture clusters. One aperture in each cluster was hand wired to give a total of 96 apertures connected in series. In addition, capacitors were added to the circuit ($C = 120$ picofarads) at the points shown in Figure 25 to simulate the effects of unselected lines. Biasing voltages are supplied to all rows and columns through series *R-L* networks to maintain all unselected diodes in reverse bias.

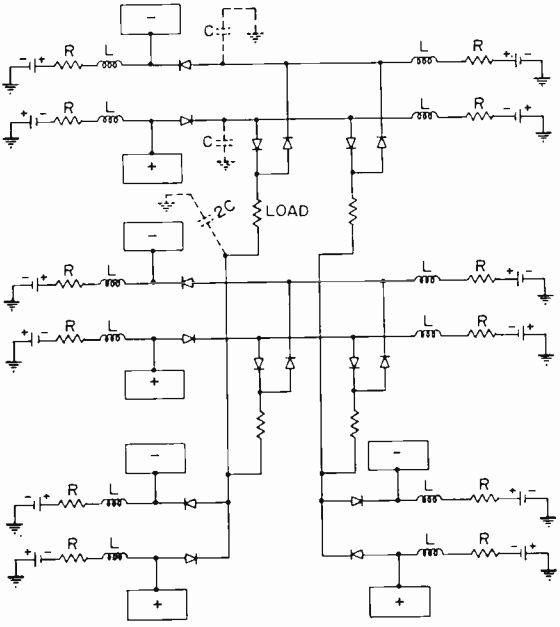


Fig. 25—Schematic of tested 2 × 2 bi-directional diode matrix.

For 300 milliamperes through the selected load, the total voltage developed across the load (*IR* drop as well as back voltage due to flux switching) is 30 volts. The capacitive current in an unselected diode is 3 ma, and the current shunted to ground by each *R-L* bias network is 10 ma.

Digit Driver

The digit drivers deliver the digit pulses to the digit-sense windings. The lengths of these windings are of the order of ten feet (80 inches for a 1000-word memory) and propagation effects are no longer negligible. The characteristic impedance of a digit-sense line is a

function of the geometry of the element winding pattern and the magnetic and dielectric characteristics of the ferrite. Experimental measurements and theoretical calculations indicate a characteristic impedance in the range of 250 to 500 ohms. Thus the digit drivers must deliver current to a relatively high-impedance load. The magnitude of this current is 15 to 25 per cent of the write-current amplitude, leading to voltage requirements in the range of 10 to 25 volts.

The digit pulse normally overlaps the write-current pulse. Additional pulse width must be provided to compensate for the delay in the digit pulse due to propagation along the digit-sense winding to insure coincidence for all words. In the experimental work undertaken, the digit and write-current pulses are of the same duration and are provided by identical drivers.

*Sense Amplifiers**

A two-stage transistor amplifier followed by a tunnel-diode strobing stage and an additional transistor stage was developed for operation as a differential sense amplifier at high speed. A current-limiting diode network is used to interconnect the sense-digit lines and digit drivers to the sense amplifiers. The diode network limits the signal appearing at the input of the sense amplifier to about 1.5 volts during the digit transient.

The amplifier is designed to sense a signal of 30 millivolts, has an output of 5 volts, a delay of less than 10 nanoseconds, and a recovery from the digit transient of less than 40 nanoseconds.

Future Developments

The memory system as described is based on the fabrication of individual wafers assembled into a mosaic. The merits of this approach are

(1) a high yield of wafers is obtained as compared with the fabrication of plates, where a single faulty bit necessitates scrapping the entire plate,

(2) automatic pretesting of wafers is easily accomplished,

(3) replacement of faulty wafers in a mosaic is possible.

Wafer dimensions of 80 × 80 × 10 mils were selected at the beginning of the program to ease fabrication difficulties. The results of the work performed indicate that smaller lateral wafer dimensions are

* This phase of the work was conducted at RCA Electronic Data Processing in the Advanced Development Activity, Pennsauken, N. J., under the direction of A. I. Pressman.

more desirable so as to reduce the propagation delays along the sense-digit windings and the back voltages induced along the read–write windings without decreasing the sense outputs. Reduction in wafer thickness will reduce the back voltage along the read–write windings and the sense output. Measurements on wafers with dimensions of 80 × 30 × 10 mils show a decrease of approximately 30 per cent in back voltage. A new design is being completed based on wafers of 50 × 30 × 10-mil dimensions with the wafers assembled on 50-mil centers in the word direction and 30-mil centers in the digit direction. This will lead to a 30 per cent increase in bits per word and a reduction in the propagation delay by a factor of approximately 2.

Further extensions involving the fabrication of multiple bits per wafer are possible. A modest start is to combine the apertures on two wafers into a single wafer, i.e., use a single wafer with two clusters, each cluster having two apertures in it to store one bit. Experimentally, a separation of 20 mils between clusters leads to sense outputs identical to those shown previously. Figure 26 is a photograph of a "microapertured plate" containing 16 clusters of apertures. The clusters are positioned by mechanical motion of the plate under the beam. The apertures within a cluster are positioned by deflection of the beam. The feasibility of fabricating such "microapertured plates" depends on the mechanical tolerances that can be maintained in locating the clusters to facilitate the photoetching of the winding patterns.

Cycle-Time Considerations

Rajchman[9] has shown that the cycle time, T, of a memory can be expressed as

$$T = 2t_s + t_t + t_g + t_a + t_n,$$

where t_s is the switching time, t_t the transmission time, t_g the amplification time, t_a the addressing time, and t_n the preread delay time. For the microaperture memory the switching time is 30 nanoseconds. The transmission time along the sense digit winding for the 80 × 80 × 10-mil wafers is 28.3 nanoseconds per 1000 words (assuming a propagation velocity of 1/3 and 1/10 that of light for the paths between clusters and through the clusters, respectively). For the 50 × 30 × 10-mil wafers the transmission time is 15.8 nanoseconds. The amplification time is the sum of the time delays through the sense amplifier and the digit driver. The sense amplifier time delay is 5 nanoseconds and the same value is assumed for the digit driver giving $t_g = 10$ nanoseconds. For 1000 words the addressing time is the delay through 10 logic levels, which is assumed to be 30 nanoseconds. The preread delay

in the sense amplifier is 30 nanoseconds. Thus the cycle time for the memory is approximately 150 nanoseconds for a 1000-word capacity.

Conclusions

The data obtained from the operation of a 4 × 8 mosaic establishes the feasibility of high-speed ferrite memories with cycle times of 150

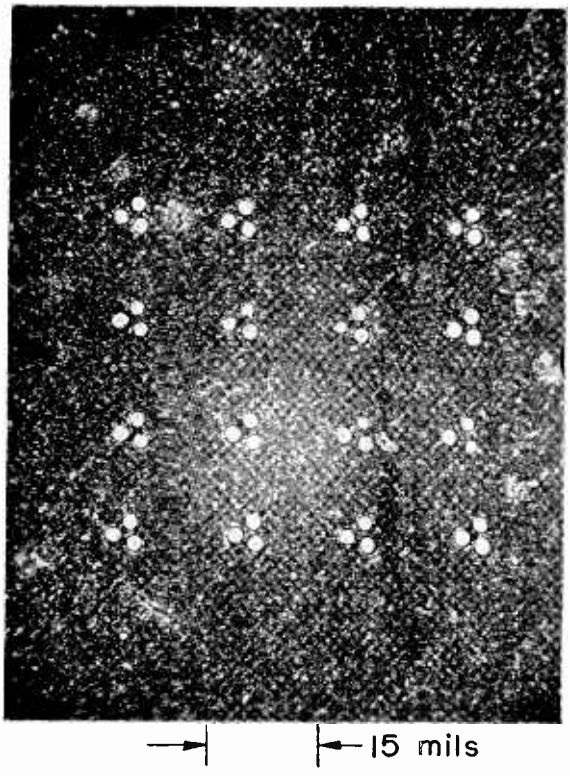


Fig. 26—Integrated microaperture ferrite plate.

nanoseconds for a 1000-word capacity. A 12 × 16 mosaic is to be tested in the near future. Word lengths of 40 bits are feasible with presently available transistors. Write and digit current requirements are modest and sense output voltages are exceptionally high. Read current levels are relatively high. Nominally, the read current required should be no greater than the sum of the write and digit currents. The not too well understood effects in the high-speed switching characteristics of fer-

rite required the use of the high read currents. Research in the synthesis of ferrite compositions for high-speed application indicates that this is not a fundamental limitation.

The conclusions to be inferred are that microapertured ferrite elements are eminently suited for high-speed applications and have advantages that place them in a more favorable position than thin magnetic films.

ACKNOWLEDGMENTS

The authors wish to express their gratitude to J. A. Rajchman, Director, Computer Research Laboratory, RCA Laboratories, under whose direction this work was performed, for the many ideas he contributed and for his understanding help and guidance.

To their many colleagues at RCA Laboratories and the operating divisions of the Corporation who were involved in this program, the authors wish to express their thanks for the help they received. Thanks are also due A. Monsen of RCA Laboratories who hand wired most of the samples tested.

VAPOR PRESSURE DATA FOR THE SOLID AND LIQUID ELEMENTS

By

Richard E. Honig

RCA Laboratories
Princeton, N. J.

Summary—Vapor pressures, melting and boiling points, and their associated energies have been selected, evaluated, tabulated, and plotted for 79 elements that are solid or liquid at room temperature. Vapor pressures have been plotted as log p (Torr) versus log T (°K). This collection contains data available before September 1, 1962.

Introduction

In 1957, a collection of vapor pressure data was published (**40**) which included 57 elements solid or liquid at room temperature. The considerable volume of information that has become available in the intervening years makes it desirable to bring this collection up to date. The present paper presents information, both published and unpublished, for 79 solid or liquid elements. For gaseous elements, the reader is referred to a separate collection (**41**) published in 1960.

Data and Computations

The vapor pressure data presented in this paper come from the following major sources: "Selected Values for the Thermodynamic Properties of Metals and Alloys," by Hultgren and collaborators (**43**); "JANAF Interim Thermochemical Tables," by Stull and collaborators (**46**); "Thermodynamic Properties of the Elements," by Stull and Sinke (**75**); a thorough literature search covering articles and abstracts available before September 1, 1962; and a number of private communications concerning unpublished results.

To keep the list of references to a reasonable number, the three collections mentioned above, rather than original articles, have been quoted whenever possible. In addition to these, a total of about 125 articles and abstracts were consulted, out of which some 75 references have been selected and quoted. References presenting results that appear seriously out of line with other work have been omitted. Since this compilation is based on the data of many workers who measured vapor pressures by different techniques under widely differing experimental conditions, it is often very difficult to choose between two apparently equivalent sets of results, and at times the preference expressed may be subjective and arbitrary.

To compare vapor pressure data from various sources, they were plotted on log p versus log T graphs, where p is in Torr (mm Hg) or atm and T in °K. Hultgren's data (**43**) for many metals, tabulated as temperatures at given pressures, could be plotted directly. Stull's data (**46, 75**), tabulated as log p (atm) at given temperatures, could be put directly on the log p versus log T plots with the help of a special scale. Most of the individual references present experimental results in terms of the general equation

$$\log_{10} p = AT^{-1} + B\log_{10} T + CT + DT^2 + E, \qquad (1)$$

where

p = pressure, expressed in this paper in Torr (mm Hg)

T = absolute temperature, in °K

A,B,C,D,E = coefficients characteristic of the element (in most cases, only A and E are used).

A computer was employed to determine from Equation (1) the temperatures corresponding to fixed pressures, starting at 10^3 and going in decade steps down to 10^{-13} Torr. Newton's method of successive approximations was used until the final value matched the equation to five significant figures. The data were checked for accuracy and correctness of transcription by comparing the computed boiling point for each element with the known value, and by checking to see if the pressures obtained from the solid and liquid equations matched at the melting point. The tabulated results were then plotted over the range 10^3 to 10^{-11} Torr.

For the elements whose gas phase is made up of two or more species of known concentrations, total vapor pressures were obtained by adding the individual curves graphically. These cases are identified by a Σ preceding the chemical symbol. For those elements that are made up predominantly of atomic species, contributions from molecular species have been neglected, and the symbol is given without a subscript. For the few elements that consist largely of one molecular species, the appropriate subscript has been added.

In a number of cases, the vapor pressure equation is known for the solid, but not for the liquid phase, and in a few instances the reverse is true. To obtain data for the missing temperature range, the following approximation was employed. Assuming coefficients B, C, and D of Equation (1) to be zero, the vapor pressure at the melting point can be expressed by

$$\log p_{MP} = -\frac{A_s}{T_{MP}} + E_s = -\frac{A_l}{T_{MP}} + E_l \qquad (2)$$

where subscripts "s" and "l" refer to the solid and liquid states, respectively. From the well-known Clausius–Clapeyron equation it follows that

$$A_s = \frac{1000\,\Delta H_{S,T}}{4.576}, \qquad A_l = \frac{1000\,\Delta H_{V,T}}{4.576}, \qquad (3)$$

where

$\Delta H_{S,T}$ = heat of sublimation at temperature T, in kcal/mole

$\Delta H_{V,T}$ = heat of evaporation at temperature T, in kcal/mole.

Finally,

$$\Delta H_{S,T} = \Delta H_{V,T} + \Delta H_M \qquad (4)$$

where

ΔH_M = heat of melting, in kcal/mole.

Thus, Equations (2), (3), and (4) permit computation of approximate vapor pressures for the liquid from solid-phase data and the heat of melting, and vice-versa.

As seen below, the gas phase of a substantial number of elements contains two or more species, each having its individual heat of sublimation, ΔH_S. Where feasible, these energies have been determined by mass spectrometric means, but in some cases the value for the dimer, $\Delta H_S(X_2)$, is obtained from the cycle (**25**)

$$\Delta H_S(X_2) = 2\Delta H_S(X_1) - D_0(X_2) \qquad (5)$$

where

$\Delta H_S(X_1)$ = heat of sublimation of monomer, in kcal/mole

$D_0(X_2)$ = dissociation energy of dimer, in kcal/mole, determined from spectral band data.

RESULTS

Table I presents the desired vapor pressure data over the range 10^{-11} to 10^3 Torr, together with literature references and the tem-

perature range of the original data. To simplify the tabulation, temperatures have been quoted to ± 1° between 200 and 1000°K; to ± 5° between 1000 and 2000°K; and to ± 10° above 2000°K. These values reflect the accuracy with which the curves in Figures 1A through 1C can be read. However, it is rare for pressure measurements to be made to better than ± 20%, which corresponds to a temperature uncertainty of between one and two percent. Thus, the last figure quoted in Table I may not be significant. The symbol ⊙, inserted between the appropriate columns, indicates the melting point, thus defining at a glance the solid and liquid ranges.

Figure 1 presents the vapor pressure data in graphical form on three separate sheets.* To locate a given element, the column marked "Curve Sheet" in Table I should be consulted. Sheet A contains mostly elements from the first half of the alphabet, Sheet B those from the second half, and Sheet C the rare earth elements and estimated curves (shown dashed). However, placement of some of the elements was determined by the need to minimize excessive overlapping of curves. The circled point ⊙ shown on most curves is again the melting point. The letters "s" (solid) or "l" (liquid) have been appended to the chemical symbol if the melting point falls outside the range of the graph. Where two elements fall on the same curve and one of them is based on estimated values, the symbol of the latter is placed in a dashed circle. For some elements, there exist several different, but apparently equivalent, sets of vapor pressure data as determined by different workers. Where these measurements appear equally reliable, the set nearest the mean has been selected.

Table II summarizes temperatures (°K) and energies (kcal/mole) for the melting and vaporization processes of the elements, as well as the references selected. The significant figures shown and errors quoted are those of the original articles and may, in many instances, give an over-optimistic impression of the accuracy of the data. Three different vaporization energies are quoted whenever available: ΔH_V, the heat of vaporization at the boiling point; $\Delta H_{S,0}$, the heat of sublimation at 0°K; and $\Delta H_{S,298}$, the heat of sublimation at 298°K. If the gas phase contains several species, they are arranged in the order of relative abundance, and energies are quoted for each. Estimated values are shown in parentheses. Different, but equivalent, values obtained by different workers have been listed with their corresponding references.

---

* Reproductions are available in two sizes, 20 x 25 and 8½ x 11 inches; requests for copies should be addressed to RCA Laboratories, Princeton, N.J.

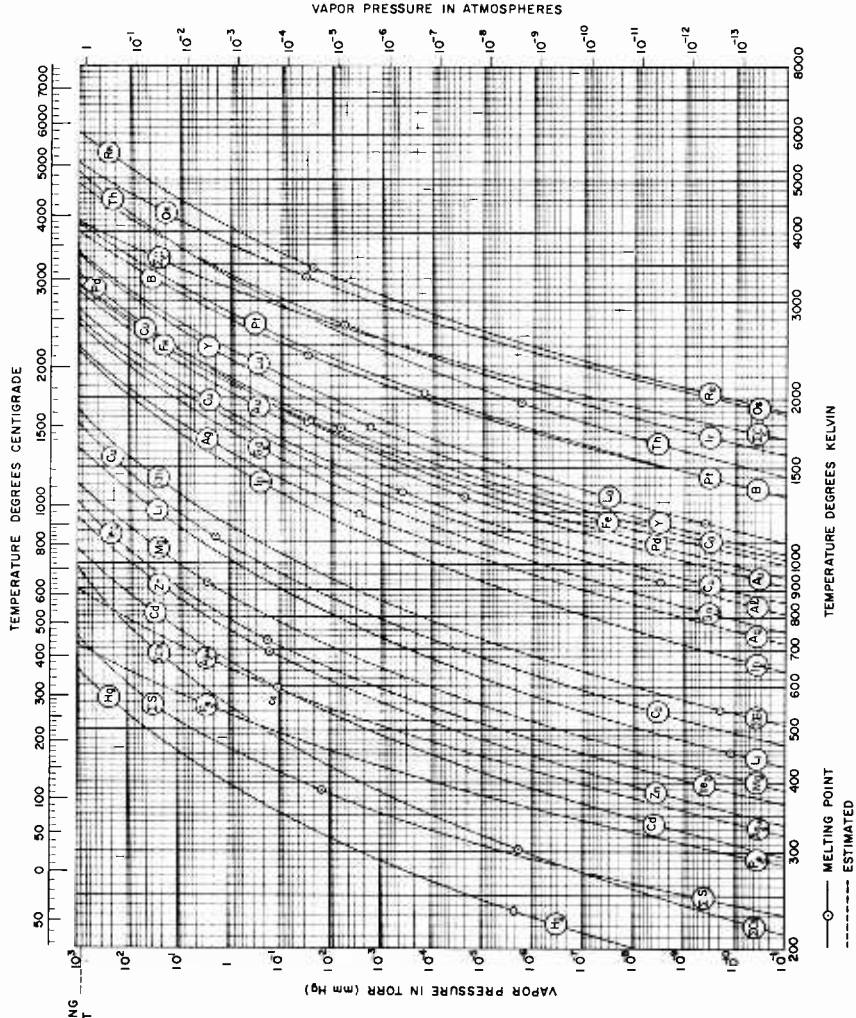


Fig. 1A—Vapor pressure data for the solid and liquid elements.

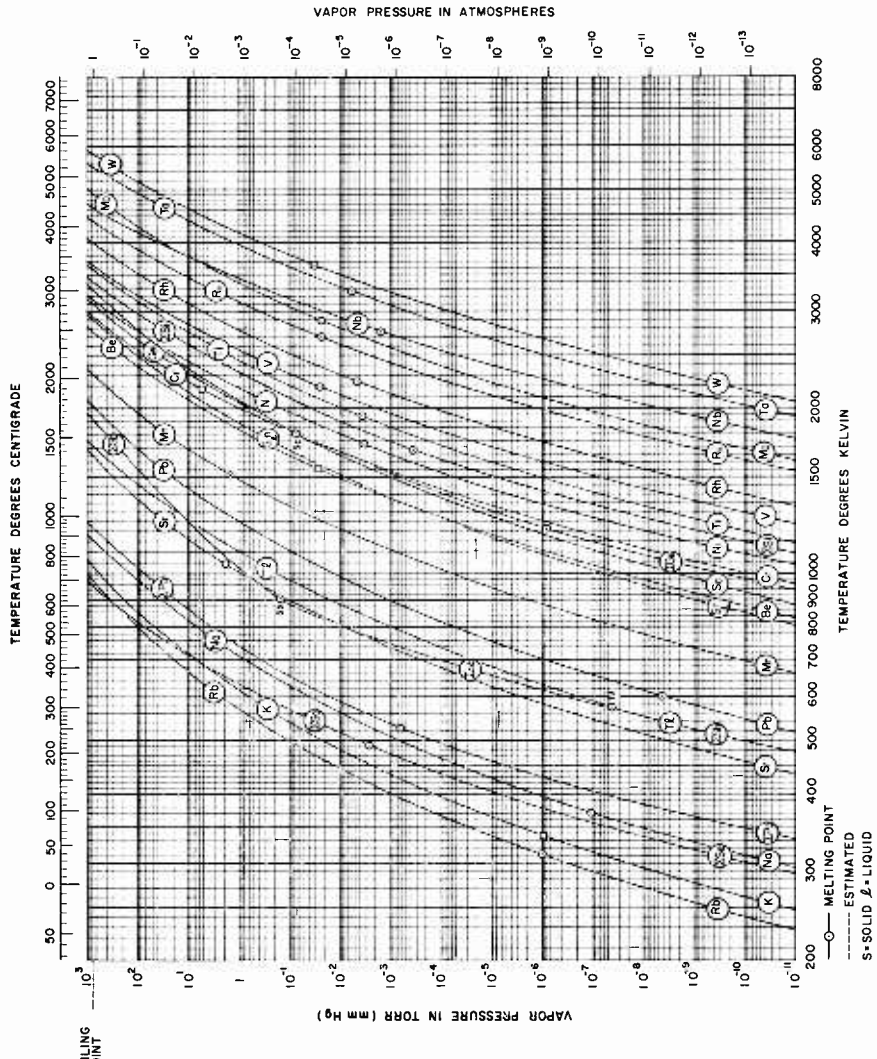


Fig. 1B—Vapor pressure data for the solid and liquid elements.

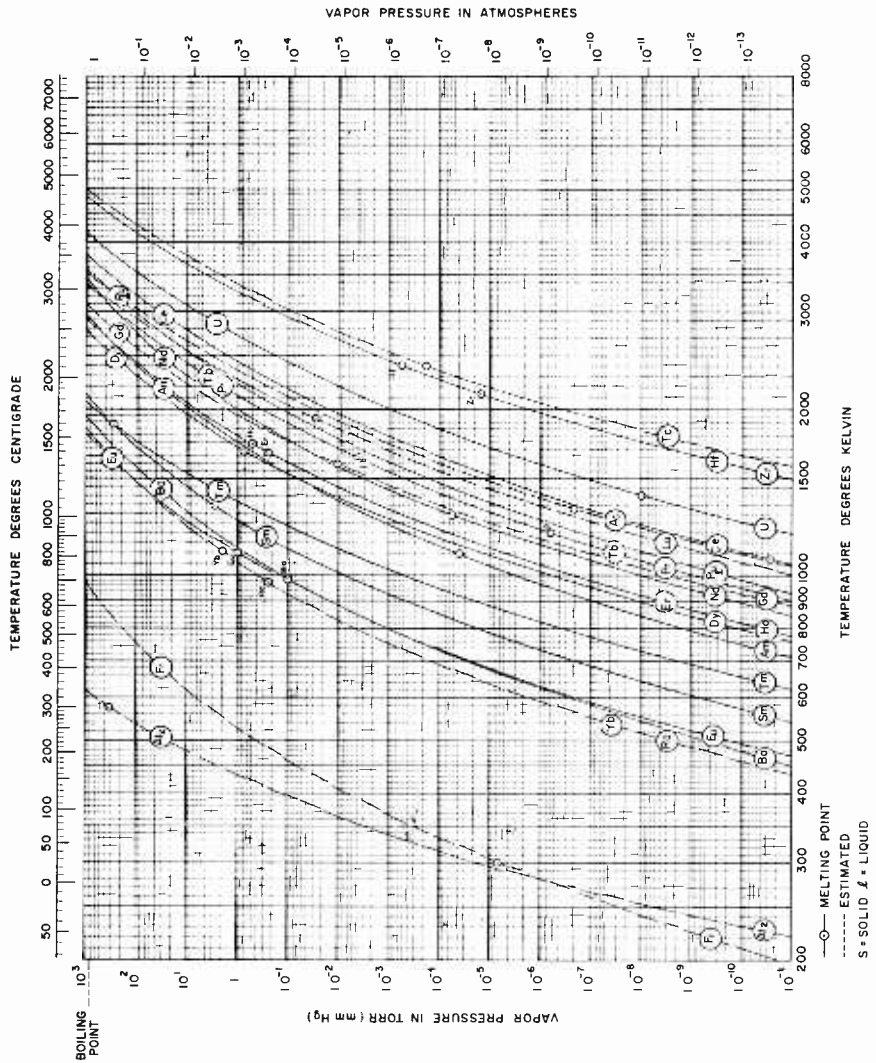


Fig. 1C—Vapor pressure data for the solid and liquid elements.

Table I—Vapor Pressure Data for the Solid and Liquid Elements.

SYMBOL	ELEMENT	CURVE SHEET	REFERENCE	DATA TEMP. RANGE, °K	TEMPERATURES (°K) FOR VAPOR PRESSURES (TORR)														
					10^{-11}	10^{-10}	10^{-9}	10^{-8}	10^{-7}	10^{-6}	10^{-5}	10^{-4}	10^{-3}	10^{-2}	10^{-1}	1	10^{1}	10^{2}	10^{3}
Ac	ACTINIUM	C	28	1873, EST.	1045	1100	1160	1230	1305	1390	1490	1605	1740	1905	2100	2350	2660	3030	3510
Ag	SILVER	A	34,58,81	958–2200	721	759	800	847	899	958	1025	1105	1195	1300	1435	1605	1815	2100	2490
Al	ALUMINUM	A	46	1220–1468	815	860	906	958	1015	1085	1160	1245	1355	1490	1640	1830	2050	2370	2800
Am	AMERICIUM	C	11	1103–1453	712	752	797	848	905	971	1050	1140	1245	1375	1540	1745	2020	2400	2970
As_4	ARSENIC (s)	A	75		323	340	358	377	400	423	447	477	510	550	590	645	712	795	900
At_2	ASTATINE	C	75	EST.	221	231	241	252	265	280	296	316	338	364	398	434	480	540	620
Au	GOLD	A	43	1073–1847	915	964	1020	1080	1150	1220	1305	1405	1525	1670	1840	2040	2320	2680	3130
B	BORON	A	46	1781–2413	1335	1405	1480	1555	1640	1740	1855	1980	2140	2300	2520	2780	3100	3500	4000
Ba	BARIUM	C	43	1333–1419	450	480	510	545	583	627	675	735	800	883	984	1125	1310	1570	1930
Be	BERYLLIUM	B	46	1103–1552	832	878	925	980	1035	1105	1180	1270	1370	1500	1650	1830	2080	2390	2810
Σ Bi	BISMUTH	A	43		510	540	568	602	640	682	732	790	860	945	1050	1170	1350	1570	1900
Σ C	CARBON (s)	A	24,46	1820–2700	1695	1765	1845	1930	2030	2140	2260	2410	2560	2730	2930	3170	3450	3780	4190
Ca	CALCIUM	A	43	730–1546	470	495	524	555	590	630	678	732	795	870	962	1075	1250	1475	1800
Cd	CADMIUM	A	43	411–1040	293	310	328	347	368	392	419	450	490	538	593	665	762	885	1060
Ce	CERIUM	C	43	1611–2038	1050	1110	1175	1245	1325	1420	1525	1650	1795	1970	2180	2440	2780	3220	3830
Co	COBALT	A	43,79	1363–1522	1020	1070	1130	1195	1265	1340	1430	1530	1655	1790	1960	2180	2440	2790	3220
Cr	CHROMIUM	B	43	1273–1557	960	1010	1055	1110	1175	1250	1335	1430	1540	1670	1825	2010	2240	2550	3000
Σ Cs	CESIUM	A	43	300– 955	213	226	241	257	274	297	322	351	387	428	482	553	643	775	980
Cu	COPPER	A	43	1143–1897	855	895	945	995	1060	1125	1210	1300	1405	1530	1690	1890	2140	2460	2920
Dy	DYSPROSIUM	C	42,43	1258–1773	760	801	847	898	955	1020	1090	1170	1270	1390	1535	1710	1965	2300	2780
Er	ERBIUM	C	43	1773, EST.	779	822	869	922	981	1050	1125	1220	1325	1450	1605	1800	2060	2420	2920
Eu	EUROPIUM	C	43	696– 900	469	495	523	556	592	634	682	739	805	884	981	1100	1260	1500	1800
Fr	FRANCIUM	C	75	EST.	198	210	225	242	260	280	306	334	368	410	462	528	620	760	980
Fe	IRON	A	36,43	1356–1889	1000	1050	1105	1165	1230	1305	1400	1500	1615	1750	1920	2130	2390	2740	3200
Ga	GALLIUM (ℓ)	A	14	1179–1383	755	796	841	892	950	1015	1090	1180	1280	1405	1555	1745	1980	2300	2730
Gd	GADOLINIUM	C	75	EST.	880	930	980	1035	1100	1170	1250	1350	1465	1600	1760	1955	2220	2580	3100
Σ Ge	GERMANIUM	B	75	1510–1885	940	980	1030	1085	1150	1220	1310	1410	1530	1670	1830	2050	2320	2680	3180

Table I—Vapor Pressure Data for the Solid and Liquid Elements *(Continued)*.

SYMBOL	ELEMENT	CURVE SHEET	REFERENCE	DATA TEMP. RANGE, °K	TEMPERATURES (°K) FOR VAPOR PRESSURES (TORR)														
					10^{-11}	10^{-10}	10^{-9}	10^{-8}	10^{-7}	10^{-6}	10^{-5}	10^{-4}	10^{-3}	10^{-2}	10^{-1}	1	10^{1}	10^{2}	10^{3}
Hf	HAFNIUM	C	55,59	2035–2277	1505	1580	1665	1760	1865	1980	2120	2270 ⊙	2450	2670	2930	3240	3630	4130	4780
Hg	MERCURY	A	43,46	193– 575	170	180	190	201	214	229 ⊙	246	266	289	319	353	398	458	535	642
Ho	HOLMIUM	C	16	923–2023	779	822	869	922	981	1050	1125	1220	1325	1450	1605 ⊙	1800	2060	2410	2910
In	INDIUM (ℓ)	A	43,54	646–1348	641	677	716	761	812	870	937	1015	1110	1220	1355	1520	1740	2030	2430
Ir	IRIDIUM	A	37,60,62	1986–2600	1585	1665	1755	1850	1960	2080	2220	2380	2560 ⊙	2770	3040	3360	3750	4250	4900
K	POTASSIUM	B	43,76	373–1031	247	260	276	294	315 ⊙	338	364	396	434	481	540	618	720	858	1070
La	LANTHANUM	A	1	1655–2167	1100	1155 ⊙	1220	1295	1375	1465	1570	1695	1835	2000	2200	2450	2760	3150	3680
Li	LITHIUM	A	43	735–1353	430	452 ⊙	480	508	541	579	623	677	740	810	900	1020	1170	1370	1620
Lu	LUTETIUM	C	80	EST.	1000	1060	1120	1185	1260	1345	1440	1550	1685	1845 ⊙	2030	2270	2550	2910	3370
Mg	MAGNESIUM	A	43	626–1376	388	410	432	458	487	519	555	600	650	712	782	878 ⊙	1000	1170	1400
Mn	MANGANESE	B	81	1523–1823	660	695	734	778	827	884	948	1020	1110	1210	1335	1490 ⊙	1695	1970	2370
Mo	MOLYBDENUM	B	43	2070–2504	1610	1690	1770	1865	1975	2095	2230	2390	2580	2800 ⊙	3060	3390	3790	4300	5020
Na	SODIUM	B	43	496–1156	294	310	328	347	370 ⊙	396	428	466	508	562	630	714	825	978	1175
Nb	NIOBIUM	B	73	2304–2596	1765	1845	1935	2035	2140	2260	2400	2550	2720	⊙2930	3170	3450	3790	4200	4710
Nd	NEODYMIUM	C	43	1240–1600	846	895	945	1000	1070	1135	1220 ⊙	1320	1440	1575	1770	2000	2300	2740	3430
Ni	NICKEL	B	43	1307–1895	1040	1090	1145	1200	1270	1345	1430	1535	1655	⊙1800	1970	2180	2430	2770	3230
Os	OSMIUM	A	61	2300–2800	1875	1965	2060	2170	2290	2430	2580	2760	2960	3190	3460	3800	4200	4710	5340
P_4	PHOSPHORUS (s)	A	75		283	297	312	327	342	361	381	402	430	458	493	534	582	642	715
Pb	LEAD	B	43	1200–2028	516	546	580 ⊙	615	656	702	758	820	898	988	1105	1250	1435	1700	2070
Pd	PALLADIUM	A	21,38	1294–1640	945	995	1050	1115	1185	1265	1355	1465	1590	1735 ⊙	1920	2150	2450	2840	3380
ΣPo	POLONIUM	B	31,75	711–1286	332	348	365	384	408	432	460	494 ⊙	537	588	655	743	862	1040	1250
Pr	PRASEODYMIUM	C	43	1423–1693	900	950	1005	1070	1140	⊙1220	1315	1420	1550	1700	1890	2120	2420	2820	3370
Pt	PLATINUM	A	21,37,43	1697–2042	1335	1405	1480	1565	1655	1765	1885	2020 ⊙	2180	2370	2590	2860	3190	3610	4170
Pu	PLUTONIUM (ℓ)	C	63	1392–1793	931	983	1040	1105	1180	1265	1365	1480	1615	1780	1975	2230	2550	2980	3590
Ra	RADIUM	C	75	EST.	436	460	488	520	552	590	638	690	755	830	920	⊙1060	1225	1490	1840
Rb	RUBIDIUM	B	75		227	240	254	271	289	312 ⊙	336	367	402	446	500	568	665	802	1000
Re	RHENIUM	A	43	2494–2999	1900	1995	2100	2220	2350	2490	2660	2860	3080	3340 ⊙	3680	4080	4600	5220	6050

Table I—Vapor Pressure Data for the Solid and Liquid Elements *(Continued)*.

SYMBOL	ELEMENT	CURVE SHEET	REFERENCE	DATA TEMP. RANGE, °K	TEMPERATURES (°K) FOR VAPOR PRESSURES (TORR)														
					10^{-11}	10^{-10}	10^{-9}	10^{-8}	10^{-7}	10^{-6}	10^{-5}	10^{-4}	10^{-3}	10^{-2}	10^{-1}	1	10^{1}	10^{2}	10^{3}
Rh	RHODIUM	B	22,37,43,60	1709–2205	1330	1395	1470	1550	1640	1745	1855	1980	2130	Θ 2310	2520	2780	3110	3520	4070
Ru	RUTHENIUM	B	43,61	2000–2500	1540	1610	1695	1780	1880	1990	2120	2260	2420	2620	Θ 2860	3130	3480	3900	4450
ΣS	SULFUR	A	10,46,52		230	240	252	263	276	290	310	328	353	382	Θ 420	462	519	606	739
ΣSb	ANTIMONY	B	5,44,67	693–1110	477	498	526	552	582	618	656	698	748	806	885	Θ 1030	1250	1560	1960
Sc	SCANDIUM	B	1,48	1301–1780	881	929	983	1045	1110	1190	1280	1380	1505	1650	Θ 1835	2070	2370	2780	3360
ΣSe	SELENIUM	B	29,45,53	550– 950	286	301	317	336	356	380	406	437	472	Θ 516	570	636	719	826	972
ΣSi	SILICON	B	6,18,33	1640–2054	1090	1145	1200	1265	1340	1420	1510	1610	Θ 1745	1905	2090	2330	2620	2990	3490
Sm	SAMARIUM	C	43	789– 833	542	573	608	644	688	738	790	853	926	1015	1120	1260	Θ 1450	1715	2120
Sn	TIN (ℓ)	B	43	1424–1753	805	852	900	955	1020	1080	1170	1270	1380	1520	1685	1885	2140	2500	2960
Sr	STRONTIUM	B	75		433	458	483	514	546	582	626	677	738	810	900	1005	Θ 1160	1370	1680
Ta	TANTALUM	B	43	2624–2948	1930	2020	2120	2230	2370	2510	2680	2860	3080	Θ 3330	3630	3980	4400	4930	5580
Tb	TERBIUM	C	80	EST.	900	950	1005	1070	1140	1220	1315	1420	1550	Θ 1700	1890	2120	2420	2820	3370
Tc	TECHNETIUM	C	75	EST.	1580	1665	1750	1840	1950	2060	2200	2350	2530	Θ 2760	3030	3370	3790	4300	5000
Te_2	TELLURIUM	A	51,56	481–1128	366	385	405	428	454	482	515	553	596	647	706	Θ 791	905	1065	1300
Th	THORIUM	A	17	1757–1956	1450	1525	1610	1705	1815	1935	Θ 2080	2250	2440	2680	2960	3310	3750	4340	5130
Ti	TITANIUM	B	43,46	1510–1822	1140	1200	1265	1335	1410	1500	1600	1715	1850	Θ 2010	2210	2450	2760	3130	3640
Tl	THALLIUM	B	5,30	519– 924	473	499	527	556	Θ 592	632	680	736	803	882	979	1100	1255	1460	1750
Tm	THULIUM	C	43	809–1219	624	655	691	731	776	825	882	953	1030	1120	1235	1370	1540	1760	Θ 2060
U	URANIUM	C	2, 4,65	1630–2071	1190	1255	1325	Θ 1405	1495	1600	1720	1855	2010	2200	2430	2720	3080	3540	4180
V	VANADIUM	B	43	1666–1882	1235	1295	1365	1435	1510	1605	1705	1820	1960	2120	Θ 2320	2560	2850	3220	3720
W	TUNGSTEN	B	43,46	2518–3300	2050	2150	2270	2390	2520	2680	2840	3030	3250	3500	Θ 3810	4180	4630	5200	5900
Y	YTTRIUM	A	1	1774–2103	1045	1100	1160	1230	1305	1390	1490	1605	1740	Θ 1905	2105	2355	2670	3085	3650
Yb	YTTERBIUM	C	77	EST.	436	460	488	520	552	590	638	690	755	830	920	1060	Θ 1225	1490	1840
Zn	ZINC	A	5,43,67	422–1089	336	354	374	396	421	450	482	520	565	617	681	Θ 760	870	1010	1210
Zr	ZIRCONIUM	C	46	1949–2054	1500	1580	1665	1755	1855	1975	2110	Θ 2260	2450	2670	2930	3250	3650	4170	4830

Table II—Melting and Vaporization Data for the Solid and Liquid Elements.

	MELTING			VAPORIZATION				
SPECIES	MP °K	ΔH_M kcal/mole	REF.	BP °K	ΔH_V @BP kcal/mole	$\Delta H_{S,0}$ @0°K kcal/mole	$\Delta H_{S,298}$ @298°K kcal/mole	REF.
Ac	1320 ± 50	(3.4)	50,74	3470 ±300	(95)			28
Ag	1234	2.885	43,50	2435		67.99 ±.3	68.10 ±.3	43,58,81
Ag_2						98		25
Al	932 ±1	2.55 ±.05	46	2736	70.7 ±.4	77.4 ±.4	78.0 ±.4	46
Al_2						109		13
Am	<1103 1269		11 9	2880 2700	57.		66	11 9
As_4 As_2 As	1090	6.62	75	886	30.5		34.5 >48 >69	75
At_2	(575)	(5.7)	75	(610)	(21.6)			75
Au	1336	2.955	43	3081		88.0 ±1.0	88.0 ±1.0	26,34,39,43,57,64
Au_2						126		25
B	2300 >2420	5.3	46 70	3950		128.0 – 136.7	129.2 – 137.9	3,12,27,32,46, 62,66,69,70,78
B_2						190 – 199	191 – 200	
Ba	983	1.83	50	1895	36.7		41.74	43
Be	1556	2.8 ±.5 3.52 ±.08	46 47	2757	71.14	77.25 ±.5	78.25 ±.5	46
Bi_2 Bi	544.5	2.6 ±.1	43	1852		53.12 49.56	52.50 49.50	43 43
C_3				4130		188.1 ±2.3	189.7 ±2.3	24,46
C						169.58 ±.45	170.89 ±.45	
C_2						195.8 ±1.7	199 ±1.7	
C_4						230 ±6	242 ±6	
C_5						233 ±6	242 ±6	
Ca	1123	1.97	43	1756		42.26 ±.4	42.37 ±.4	43
Ca_2							79	8
Cd	594	1.46 ±.03	43	1040	22.96	26.78 ±.15	26.77 ±.15	5,43
Cd_2							50.8	8
Ce	1077	1.238 ±.004	72	(3740)	92.9 (@1800)		97 ±3	43

Table II—Melting and Vaporization Data for the Solid and Liquid Elements *(Continued)*.

SPECIES	MELTING			VAPORIZATION				
	MP °K	ΔH_M kcal/mole	REF.	BP °K	ΔH_V @BP kcal/mole	$\Delta H_{S,0}$ @0°K kcal/mole	$\Delta H_{S,298}$ @298°K kcal/mole	REF.
Co	1768 ±1	4.1	43	3174		101.1 ±1.0	101.5 ±1.0	43
Cr	2176	(5.0)	43	2938		94.3 ±.5	94.9 ±.5	43
Cs	301.8	0.52 ±.02	43	955		19.05 ±.07	18.67 ±.07	43
Cs_2						27.70	26.62	43
Cu	1357	3.12 ±.15	43	2846		80.25	80.53	43
Cu_2						114		25
Dy	1680 ±5	(4.1)	15	2710	62.5			42,43
							71.4	68
							61.6	80
Er	1770 ±15	(4.1)	15	(2850)		75.67 ±.34	75.39 ±.34	43,77
							66.4	80
Eu	1099 ±10	(2.5)	43	1764		43.4 ±.4	43.11 ±.25	43,77
Fr	(300)	(0.5)	75	(950)	(15.2)			75
Fe	1809	3.63 ±.6	43	3148		98.99 ±.20	99.55 ±.20	43
						100.5 ±.4		36
Ga	302.9	1.335	43	2676			68.96 ±.19	14
Ga_2							106	13
Gd	1585 ±15	(3.7)	71,75	(3000)		81.91 ±.32	81.22 ±.32	75,77
							83.6	80
Ge	1210	7.6	75	3100	79.9		90.	75
Ge_2							115	25
Hf	>2400	(5.2)	59,75	4690			145.5 ±1.0	42,59
				4800			146.59 ±.24	42,55
Hg	234.29	0.5486	43,46	629.73	14.171	15.441 ±.013	14.691 ±.013	43,46
Hg_2							27.4	8
Ho	1734 ±5	4.6 ±.6	16	2842			70.6 ±.7	16,80
						75.47 ±.44	75.04 ±.44	77
In	429.3	0.78	43	2364			58 ±2	43,54
In_2							94	20

Table II—Melting and Vaporization Data for the Solid and Liquid Elements *(Continued)*.

	MELTING			VAPORIZATION				
SPECIES	MP °K	ΔH_M kcal/mole	REF.	BP °K	ΔH_V @BP kcal/mole	$\Delta H_{S,0}$ @0°K kcal/mole	$\Delta H_{S,298}$ @298°K kcal/mole	REF.
Ir	2727	(6.3)	50	4810 ±100			159.9 ±2.0	37,60,62
K	336.4 ±.1	0.562 ±.006	43	1031	19.176 ±.053	21.629 ±.050	21.415 ±.050	43,76
K_2							30.37 ±.50	43
La	1193	(1.29)	43	3610		104.1 ±.7	104.0 ±.7	1
						100.24 ±.9	100.18 ±.9	43
Li	453.69 ±.03	0.717 ±.005	43	1597	35.403 ±.400	38.164 ±.400	38.584 ±.400	43
Li_2							50.41 ±.90	43
Lu	1925 ±5	(4.6)	15,43	(3300)			102.8	35,77
							94.7	80
Mg	923	2.14 ±.05	43,46	1376		35.01 ±.25	35.3 ±.25	43
Mn	1517	3.5	75	2309		66.45 ±.05	66.74 ±.05	81
Mo	2890	(6.65)	43	4924		158.3 ±.8	158.7 ±.8	43
Na	370.98 ±.02	0.6217 ±.0010	43	1156.2	23.426 ±.150	25.901 ±.150	25.852 ±.150	43
Na_2							33.4	8
Nb	2770	(6.4)	73	4640		171.80 ±.49	172.53 ±.49	73
Nd	1297	1.705 ±.019	43	3335		77.5 ±2.0	77.3 ±2.0	43
							76.3	80
Ni	1725 ±4	(4.21)	43	3159		102.18 ±1.4	102.67 ±1.4	43
Os	3318	(7.0)	61,75	5260			187.4 ±.9	61
P_4	870	4.5 ±.2	46	704			30.77 ±.40	46
P_2							42.7	75
P							79.8	75
Pb	600.6	1.14	43	2016		46.76 ±.30	46.60 ±.30	43
Pb_2							70	25
Pd	1823 ±3	4.2	43	3310		89.0 ±.8	89.2 ±.8	21
							91.0 ±.8	38

Table II—Melting and Vaporization Data for the Solid and Liquid Elements *(Continued)*.

	MELTING			VAPORIZATION				
SPECIES	MP °K	ΔH_M kcal/mole	REF.	BP °K	ΔH_V @BP kcal/mole	$\Delta H_{S,0}$ @0°K kcal/mole	$\Delta H_{S,298}$ @298°K kcal/mole	REF.
Po_2	527	(3.0)	50	1220			32.9	31,75
Po							34.5	75
Pr	1208	1.65	35	3295			85.1	68
							77.9	80
Pt	2043	(4.7)	43	4097		134.8 ±1.0	135.0 ±1.0	43,21,37
Pu	913		19	3508 ±19	80.46 ±.32 (@1592)			63
Ra	973	(2.0)	75	(1800)	(32.7)			75
Rb	312	0.56	75	974	16.54		19.60	75
Rb_2							27.55	75
Re	3453 ±20	(7.9)	43	5960	169.	185.9 ±2.0	186.1 ±2.0	43
Rh	2239	(5.15)	43	4000 ±100		132.8 ±.5	133.1 ±.5	43
Ru	(2700)	(6.1)	43	4392 ±100			154.9 ±1.3	43,61
S_8	388.36	0.41052	46	717.75	2.3		24.35	10,75
S_2							30.84	75
S							66	8
Sb_4	903	4.69 ±.10	43	1908		50.2	49.0	43
Sb_2						56.8	56.3	43
Sb						62.6	62.7	43
Sc	1811 ±2	4.2	35	3280		79.7 ±0.4		1
							82.28	48
Se_6	490	1.3	75	952	6.29 kcal/g-at		35.38	75
Se_2							34.12	75
Se							55	23
Si	1685 ±2	12.095 ±.1	46	3418			107.4 ±3.0	6,18,33
							140	25
Si_2							146	46
Si_3								
Sm	1345	2.061 ±.015	43	2076		49.42 ±.60	49.56 ±.60	43
Sn	505	1.75	43	2891		72.1 ±.5	72.1 ±.5	43
Sn_2							98	25
Sr	1043	(2.2)	75	1640	33.2		39.1	75
Ta	3270	(7.5)	75	5510		186.8 ±.6	186.9 ±.6	43
Tb	1638	3.9	43,50	(3295)			87.1	80
							91.9	77

Table II—Melting and Vaporization Data for the Solid and Liquid Elements *(Continued)*.

SPECIES	MELTING			VAPORIZATION				
	MP °K	ΔH_M kcal/mole	REF.	BP °K	ΔH_V @BP kcal/mole	$\Delta H_{S,0}$ @0°K kcal/mole	$\Delta H_{S,298}$ @298°K kcal/mole	REF.
Tc	(2400)	(5.5)	75	(4900)	(138)		(155)	75
Te_2	723	4.18	75	1267			35.6	75
Te							46.5	75
Th	1968	(3.74)	75	5020			136.6 ±.5	17
Ti	1940	4.46	43	3575		112.08 ±.50	112.74 ±.50	43
Tl	577	0.975 ±.050	43	1710		42.85 ±.20	42.70 ±.20	5,30
Tm	1873 ±50	4.4	43	2005			58.8 ±.2	43
U	1405.5 ±.8	4.7 ±.2	7,65	4090	106.8	116.6 ±.1	117.2 ±.1	2,65
V	2190 ±10	(5.05)	43	3652		122.37 ±.30	123.17 ±.30	43
W	3650 ±5	8.42	43,46	5800		201.5 ±2.0	201.8 ±2.0	43,46
Y	(1773)	(4.1)	75	3570		97.6 ±.4	85.71	1 49
Yb	1097 ±5	2.2	50	(1800)			40.0	68
Zn	692.7 ±.1	1.765 ±.080	43	1184		31.11 ±.05	31.25 ±.05	43
Zr	2128 ±25	(4.9)	43,46	4747	136.4	145.1 ±.4	145.4 ±.4	46

Discussion

Since the publication in 1957 of the first collection, enough new data have become available so that the present edition contains information on all naturally occurring elements solid or liquid at room temperature. In some instances, however, the data are only rough estimates, or there is not yet satisfactory agreement between different sets. These cases are discussed briefly below.

Astatine: Stull's data (**75**) are only an estimate, obtained by extrapolation from the other halogens.

Boron: The wide range in $\Delta H_{s,298}$ (129.2 to 137.9 kcal/mole) proposed in ten recent publications (see Table II) is indicative of the difficulties encountered in handling this element. Since Stull's recent values (**46**) are near the mean of the different sets of data, they were used for the vapor pressures in Table I and the curve in Figure 1A.

Dysprosium: Hultgren's tabulation (**43**), based on data by Savage,

Hudson, and Spedding (**68**), has been accepted for the solid phase, but liquid vapor-pressure data were recalculated by the method discussed above. Reference (**68**) quotes a value for $\Delta H_{S,298}$ which differs considerably from that proposed by White et al (**80**).

Erbium: Vapor pressures relative to those of Nd have been presented by White et al (**80**), who quote a $\Delta H_{S,298} = 66.4$ kcal/mole. On the other hand, Trulson et al (**77**) have measured $\Delta H_{S,298} = 75.39 \pm 0.34$ kcal/mole, which is very close to the value for the neighboring element Ho, whose vapor pressure is known (**16**). In the absence of more accurate information, the Er vapor pressure is assumed to fall on the Ho curve.

Lutetium: Vapor pressures relative to those of Pr are given by White et al (**80**) who also quote $\Delta H_{S,298} = 94.7$ kcal/mole. While the value obtained by Trulson et al (**77**) differs significantly ($\Delta H_{S,298} = 102.8$ kcal/mole), their rough vapor-pressure estimate is in fair agreement. White's relative values have been used for the vapor-pressure curve in Figure 1C.

Polonium: Stull and Sinke's vapor pressure values (**75**) have been plotted in preference to Giorgi's (**31**) whose constants are apparently in error.

Sulfur: In the low-pressure region, the data by Briske et al (**10**) are in good agreement with Stull's (**75**) values for S_8. Above the melting point, Kubaschewski's equation (**52**) has been selected.

Terbium: Vapor pressures relative to Nd have been presented by White et al (**80**) and are used here as a basis for an estimated curve.

Yttrium: There exists a considerable discrepancy in the values for ΔH_S measured by Ackermann and Rauh (**1**) and by Karelin et al (**49**), and their respective vapor pressures differ by more than one order of magnitude. Since many more details are known about the experimental work of Reference (**1**), it has been selected.

Ytterbium: No absolute vapor pressures are available, but values relative to Sm have been obtained by Savage et al (**68**), and these were used for an estimated curve.

ACKNOWLEDGMENTS

It is a pleasure to acknowledge the helpful assistance of the following people who made information available to the author in advance of publication: A. T. Aldred, Argonne National Laboratory; L. C.

Beavis, Sandia Corp.; L. Brewer, University of California; P. Grieveson, Carnegie Inst. Tech.; R. R. Hultgren, University of California; T. F. Lyon, General Electric Co., Evandale, Ohio; J. L. Margrave, University of Wisconsin; J. P. McCullough, Bureau of Mines, Bartlesville; D. W. Osborne, Argonne National Laboratory; M. B. Panish, Avco Corp.; E. G. Rauh, Argonne National Laboratory; A. W. Searcy, University of California; F. H. Spedding, Ames Laboratory; D. R. Stull, Dow Chemical Co.; O. C. Trulson, Union Carbide; R. F. Walker, National Bureau of Standards; B. J. Zwolinski, A and M College. Special thanks are due to J. Drowart, University of Brussels, for several fruitful discussions and advance information, and to H. O. Hock, RCA Laboratories, for setting up and streamlining the computer program. The help of A. L. Eichenbaum and J. I. Pankove, who helped the author to evaluate some of the articles available only in Russian, is gratefully acknowledged.

REFERENCES

[1] R. J. Ackermann and E. G. Rauh, "Vapor Pressures of Scandium, Yttrium, and Lanthanum," *Jour. Chem. Phys.*, Vol. 36, p. 448, Jan. 15 (1962).

[2] R. J. Ackermann, E. G. Rauh, and R. J. Thorn, "Effect of Oxygen on the Vapor Pressure of Uranium," *Symposium on the Thermodynamics of Nuclear Materials*, Vienna, May (1962).

[3] P. A. Akishin, O. T. Nikitin, and L. N. Gorokhov, "Determination of the Heat of Sublimation of Boron by the Mass-Spectroscopic Method," *Doklady Akad. Nauk S.S.S.R.*, Vol. 129, p. 1075 (1959).

[4] C. B. Alcock and P. Grieveson, "A Thermodynamic Study of the Compounds of Uranium with Silicon, Germanium, Tin, and Lead," *Jour. Inst. Met.*, Vol. 90, p. 304, April 1962 (1961-2).

[5] A. T. Aldred and J. N. Pratt, private communication (1962).

[6] R. L. Batdorf and F. M. Smits, "Diffusion of Impurities into Evaporating Silicon," *Jour. Appl. Phys.*, Vol. 30, p. 259, Feb. (1959).

[7] B. Blumenthal, "The Transformation Temperatures of High-Purity Uranium," *Jour. Nuclear Materials*, Vol. 2, p. 23, March (1960).

[8] L. Brewer, "Heats of Sublimation of the Elements," UCRL Report 2854 (revised) (1955).

[9] L. Brewer, UCRL Report 10012 (1961).

[10] C. Briske, N. H. Hartshorne, and D. R. Stranks, "The Vapor Pressures and Latent Heats of Sublimation of α-, β-, and γ-Sulphur," *Jour. Chem. Soc.* [London 1960], p. 1200 (1960).

[11] S. C. Carniglia and B. B. Cunningham, "The Vapor Pressure of Americium Metal," *Jour. Am. Chem. Soc.*, Vol. 77, p. 1502, March 20 (1955).

[12] W. A. Chupka, private communication quoted in Reference (27).

[13] W. A. Chupka, J. Berkowitz, C. F. Giese, and M. G. Inghram, "Thermodynamic Studies of Gaseous Metallic Carbides," *Jour. Phys. Chem.*, Vol. 62, p. 611, May (1958).

[14] C. N. Cochran and L. M. Foster, "Vapor Pressure of Gallium, Stability of Gallium Suboxide Vapor, and Equilibria of Some Reactions Producing Gallium Suboxide Vapor," *Jour. Electrochem. Soc.*, Vol. 109, p. 144, Feb., Part I (1962).

[15] A. H. Daane, "Physical Properties of the Rare Earth Metals," *Rare Earth Symposium, Annual Meeting Am. Soc. Metals*, Chicago (1959).

[16] A. H. Daane, G. F. Wakefield, and F. H. Spedding, "The Vapor Pressure of Holmium Metal," to be published (1962).

[17] A. J. Darnell, W. A. McCollum, and T. A. Milne, "Vapor Pressure of Thorium," *Jour. Phys Chem.*, Vol. 64, p. 341, March (1960).

[18] S. G. Davis, D. F. Anthrop, and A. W. Searcy, "Vapor Pressure of Silicon and the Dissociation Pressure of Silicon Carbide," *Jour. Chem. Phys.*, Vol. 34, p. 659, Feb. (1961).

[19] R. H. V. M. Dawton and K. L. Wilkinson, "Plutonium: Evaporation Tests, Ionization Potential, and Electron Emission," AERE Report No. GP/R 1906 (1956).

[20] G. DeMaria, J. Drowart, and M. G. Inghram, "Thermodynamic Study of InSb with a Mass Spectrometer," *Jour. Chem. Phys.*, Vol. 31, p. 1076, Oct. (1959).

[21] L. H. Dreger and J. L. Margrave, "Vapor Pressures of Platinum Metals. I. Palladium and Platinum," *Jour. Phys. Chem.*, Vol. 64, p. 1323, Sept. (1960).

[22] L. H. Dreger and J. L. Margrave, "Vapor Pressures of Platinum Metals. II. Rhodium," *Jour. Phys. Chem.*, Vol. 65, p. 2106, Nov. (1961).

[23] J. Drowart, private communication (1962).

[24] J. Drowart, R. P. Burns, G. DeMaria, and M. G. Inghram, "Mass Spectrometric Study of Carbon Vapor," *Jour. Chem. Phys.*, Vol. 31, p. 1131, Oct. (1959).

[25] J. Drowart and R. E. Honig, "A Mass Spectrometric Method for the Determination of Dissociation Energies of Diatomic Molecules," *Jour. Phys. Chem.*, Vol. 61, p. 980, July (1957).

[26] R. K. Edwards, private communication, quoted by R. Hultgren in Reference (43).

[27] W. H. Evans, D. D. Wagman, and E. J. Prosen, "Thermochemistry and Thermodynamic Functions of Some Boron Compounds," NBS Report No. 6252 (1958).

[28] K. W. Foster and L. G. Fauble, "The Volatility of Actinium," *Jour. Phys. Chem.*, Vol. 64, p. 958, July (1960).

[29] G. Gattow and A. Schneider, "Vapor Pressures of Zinc, Selenium, and Tellurium," *Angew. Chem.*, Vol. 71, p. 189, March (1959).

[30] L. K. Genov, A. N. Nesmeyanov, and Y. A. Priselkov, "Measuring the Vapor Pressure of Thallium by a Radioactive Tracer Method," *Doklady Akad. Nauk S.S.S.R.*, Vol. 140, p. 159 (1961).

[31] A. Giorgi, *A Study of the Density and Molecular Species of Polonium and Tellurium Vapor*, Ph.D. Thesis, Univ. N. M., June (1957).

[32] P. Grieveson, private communication (1962).

[33] P. Grieveson and C. B. Alcock, "The Thermodynamics of Metal Silicides and Silicon Carbide," pp. 183-208, in *Special Ceramics*, P. Popper, Ed., Heywood and Co., London (1961).

[34] P. Grieveson, G. W. Hooper, and C. B. Alcock, "The Vapor Pressure of the Liquid Metals Copper, Silver, and Gold," Part I, pp. 341-52 in *Physical Chemistry of Process Metallurgy*, G. R. St. Pierre, Ed., Interscience Publishers, New York, N. Y. (1961).

[35] K. A. Gschneidner, Jr., *Rare Earth Alloys*, D. Van Nostrand Co., Inc., Princeton (1961).

[36] E. A. Gulbransen and K. F. Andrew, "Vapor Pressure Studies on Iron and Chromium and Several Alloys of Iron, Chromium, and Aluminum," *Trans. Met. Soc. AIME*, Vol. 221, p. 1247, Dec. (1961).

[37] R. F. Hampson, Jr., and R. F. Walker, "Vapor Pressures of Platinum, Iridium, and Rhodium," *Jour. Res. NBS*, Vol. 65A, p. 289, July-Aug. (1961).

[38] R. F. Hampson, Jr., and R. F. Walker, "The Vapor Pressure of Palladium," *Jour. Res. NBS*, Vol. 66A, p. 177, March-April (1962).

[39] D. L. Hildenbrand and W. F. Hall, "Vapor Pressure and Heat of Sublimation of Gold," *Jour. Phys. Chem.*, Vol. 66, p. 754, April (1962).

[40] R. E. Honig, "Vapor Pressure Data for the More Common Elements," *RCA Review*, Vol. 18, p. 195, June (1957).

[41] R. E. Honig and H. O. Hook, "Vapor Pressure Data for Some Common Gases," *RCA Review*, Vol. 21, p. 359, Sept. (1960).

[42] Estimate for temperatures above melting point based on ΔH_S and ΔH_M.

[43] R. R. Hultgren, "Selected Values for the Thermodynamic Properties of Metals and Alloys," Report of the Minerals Research Laboratory, Univ. of California, Berkeley, Calif. (1962).

[44] V. V. Illarionov and A. S. Cherepanova, "The Pressure of Saturated Vapors of Liquid Antimony and their Associative State," *Doklady Akad. Nauk S.S.S.R.*, Vol. 133, p. 1086 (1960).

[45] V. V. Illarionov and L. M. Lapina, "Association States of Selenium in the Gas Phase," *Doklady Akad. Nauk S.S.S.R.*, Vol. 114, p. 1021 (1957).

[46] *JANAF Interim Thermochemical Tables*, Dow Chemical Company, Midland, Mich. (1962).

[47] P. B. Kantor, R. M. Krasovitskaya and A. N. Kisel, "Determination of Enthalpy and Specific Heat of Beryllium at 600-2200°K," *Phys. Met. and Metallogr.*, Vol. 10, No. 6, p. 42 (1960).

[48] V. V. Karelin, A. N. Nesmeyanov, and Y. A. Priselkov, "Vapor Pressure of Metallic Scandium," *Doklady Akad. Nauk S.S.S.R.*, Vol. 144, p. 352 (1962).

[49] V. V. Karelin, A. N. Nesmeyanov, and Y. A. Priselkov, "Measurement of Vapor Pressure of Metallic Yttrium," *Vestn. Mosk. Univ. Ser. II Khim.*, Vol. 17, No. 2, p. 40 (1962).

[50] K. K. Kelley, "High-Temperature Heat-Content, Heat-Capacity, and Entropy Data for the Elements and Inorganic Compounds," *Bur. Mines Bull.* 584 (1960).

[51] I. V. Korneeva, A. S. Pashinkin, A. V. Novoselova, and Y. A. Priselkov, "Determination of the Vapor Pressure of Solid Tellurium," *Zhur. Neorg. Khim.*, Vol. 2, p. 1720 (1957).

[52] O. Kubaschewski and E. L. Evans, *Metallurgical Thermochemistry*, Third Ed., Pergamon Press, New York (1950).

[53] A. A. Kudryavtsev and G. P. Ustyugov, "Determination of the Saturated Vapor Pressure of Tellurium," *Zhur. Neorg. Khim.*, Vol. 6, p. 2421 (1961).

[54] A. P. Lyubimov and Y. N. Lyubitov, "The Measurement of the Vapor Pressure of Liquid Indium with the Mass-Spectrograph," *Obrabotka Stali i Splavov*, Moskov, Inst. Stali im. I. V. Stalina, Sbornik, No. 36, p. 191 (1957).

[55] T. F. Lyon, private communication (1962).

[56] R. E. Machol and E. F. Westrum, Jr., "Vapor Pressure of Liquid Tellurium," *Jour. Am. Chem. Soc.*, Vol. 80, p. 2950, June 20 (1958).

[57] A. N. Nesmeyanov, L. A. Smakhtin, and V. I. Lebedev, "The Measurement of the Vapor Pressures of the Solid Solutions Au-Ag and Au-Cu," *Doklady Akad. Nauk S.S.S.R.*, Vol. 112, p. 700 (1957).

[58] M. B. Panish, "Vapor Pressure of Silver," *Jour. Chem. Eng. Data*, Vol. 6, p. 592 (1961).

[59] M. B. Panish, private communication (1962).

[60] M. B. Panish and L. Reif, "Vaporization of Iridium and Rhodium," *Jour. Chem. Phys.*, Vol. 34, p. 1915, June (1961).

[61] M. B. Panish and L. Reif, "Vaporization of Ruthenium and Osmium," *Jour. Chem. Phys.*, Vol. 37, p. 128, July 1 (1962).

[62] C. Paule, *Vapor Pressures of Iridium, Ruthenium and Boron*, Ph.D. Thesis, Univ. of Wis. (1962).

[63] T. E. Phipps, G. W. Sears, R. L. Seifert, and O. C. Simpson, "Vapor Pressure of Liquid Plutonium," *Proc. Intern. Conf. Peaceful Uses Atomic Energy*, Geneva, 1955, Vol. 7, p. 382 (1956).

[64] E. G. Rauh, private communication (1962).

[65] E. G. Rauh and R. J. Thorn, "Vapor Pressure of Uranium," *Jour. Chem. Phys.*, Vol. 22, p. 1414, Aug. (1954).

[66] H. E. Robson, quoted by J. M. Leitmaker, M. G. Bowman, and P. W. Gilles, *Jour. Chem. Phys.*, Vol. 36, p. 350, Jan. 15 (1962).

[67] G. M. Rosenblatt and C. E. Birchenall, "Vapor Pressure of Antimony by the Torsion-Effusion Method," *Jour. Chem. Phys.*, Vol. 35, p. 788, Sept. (1961).

[68] W. R. Savage, D. E. Hudson, and F. H. Spedding, "Mass Spectrometric Study of Heats of Sublimation of Dysprosium, Samarium, Thulium, and Ytterbium," *Jour. Chem. Phys.*, Vol. 30, p. 221, Jan. (1959).

[69] P. O. Schissel and W. S. Williams, "Mass Spectrometer Study of the Vaporization of Certain Refractory Compounds," *Bull. Am. Phys. Soc.*, Series II, Vol. 4, p. 139, March 30 (1959).

[70] A. W. Searcy and C. E. Myers, "The Heat of Sublimation of Boron and the Gaseous Species of the Boron-Boric Oxide System," *Jour. Phys. Chem.*, Vol. 61, p. 957, July (1957).

[71] F. H. Spedding, A. H. Daane, and L. D. Jennings, ISC-1049 (1958).

[72] F. H. Spedding, J. J. McKeown, and A. H. Daane, "The High Temperature Thermodynamic Functions of Cerium, Neodymium, and Samarium," *Jour. Phys. Chem.*, Vol. 64, p. 289, March (1960).

[73] R. Speiser, P. Blackburn, and H. L. Johnson, "Vapor Pressure of Niobium," *Jour. Electrochem. Soc.*, Vol. 106, p. 52, Jan. (1959).

[74] J. G. Stites, M. L. Salutsky and B. D. Stone, "Preparation of Actinium Metal," *Jour. Am. Chem. Soc.*, Vol. 77, p. 237, Jan. 5 (1955).

[75] D. R. Stull and G. C. Sinke, "Thermodynamic Properties of the Elements," *Advances in Chemistry*, Series 18, Am. Chem. Soc., Washington, D. C. (1956).

[76] R. J. Thorn and G. H. Winslow, "Correction of the Potassium Vapor Pressure Equation by the Use of the Second Virial Coefficient," *Jour. Chem. Phys.*, Vol. 65, p. 1297 (1961).

[77] O. C. Trulson, D. E. Hudson, and F. H. Spedding, *Cohesive Energies of Europium, Gadolinium, Holmium, and Erbium*, Ames Laboratory Report No. 929 (1962).

[78] G. Verhaegen and J. Drowart, "Mass Spectrometric Determination of the Heat of Sublimation of Boron and of the Dissociation Energy of B_2," *Jour. Chem. Phys.* (to be published in Oct. 1962).

[79] E. Z. Vintaikin and Y. Tomash, "Vapor Pressure of Pure Cobalt," *Zhur. Fiz. Khim.*, Vol. 35, p. 2121 (1961).

[80] D. White, P. N. Walsh, H. W. Goldstein, and D. F. Dever, "Rare Earths. II. A Mass Spectrometric Determination of the Heats of Sublimation (or Vaporization) of Neodymium, Praseodymium, Gadolinium, Terbium, Dysprosium, Holmium, Erbium, and Lutetium," *Jour. Phys. Chem.*, Vol. 65, p. 1404, Aug. (1961).

[81] P. L. Woolf, G. R. Zellars, E. Foerster, and J. P. Morris, "Vapor Pressures of Liquid Manganese and Liquid Silver," U. S. Bureau Mines Rept. Invest. #5634 (1960).

DESIGN CONSIDERATIONS FOR DOUBLE-DIFFUSED SILICON SWITCHING TRANSISTORS

By

H. Kressel, H. S. Veloric, and A. Blicher

RCA Semiconductor and Materials Division,
Somerville, N. J.

Summary—This paper reviews some of the basic concepts of transistor design and discusses their application to present processing and materials technology. Typical design information is presented, including sample design calculations for a representative epitaxial silicon transistor.

Device Description

Figure 1 shows the circular geometry used in a typical epitaxial planar silicon transistor, the 2N1708. In this type of structure, which can be readily fabricated by existing techniques, boron and phosphorous diffusions are used to form the base and emitter regions, and a photoresist process is used to define the surface geometry. The lightly doped collector region is grown on the heavily doped substrate wafer by epitaxial techniques.

Figure 2 shows a representative impurity distribution for the 2N1708 transistor, and Table I lists some of the structure parameters of the device.

Basic Junction Parameters

Junction Capacitance and Avalanche Breakdown

Junction capacitance has been evaluated for various cases such as linear-graded transition,[1] abrupt transition,[2] p+in+ structure,[3] and erfc and Gaussian impurity distributions.[4] In the linear-graded transition, the space-charge layer is divided equally between the two sides of the junction. The abrupt junction has its depletion layer entirely in the lightly doped region. For the p+in+ type, the barrier width is

[1] H. S. Veloric and K. D. Smith, "Silicon Diffused Junction Avalanche Diodes," *Jour. Electrochem. Soc.*, Vol. 104, p. 222, April 1957.
[2] K. G. McKay, "Avalanche Breakdown in Silicon," *Phys. Rev.*, Vol. 94, p. 877, May, 1954.
[3] H. S. Veloric and M. B. Prince, "High Voltage Conductivity Modulated Silicon Rectifier," *Bell Sys. Tech. Jour.*, Vol. 36, p. 975, July 1957.
[4] H. Lawrence and R. M. Warner, Jr., "Diffused Junction Depletion Layer Calculations," *Bell Sys. Tech. Jour.*, Vol. 39, p. 389, Oct. 1959,

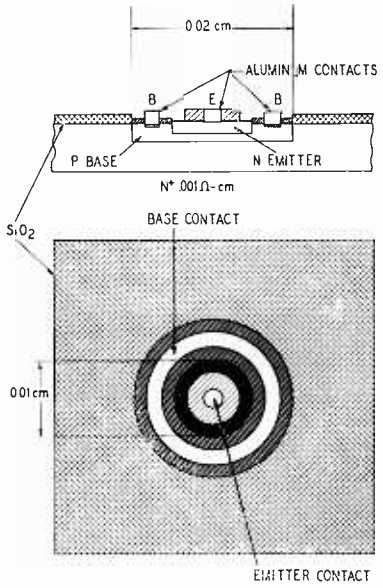


Fig. 1--The geometry used for the 2N1708 double-diffused epitaxial planar transistor.

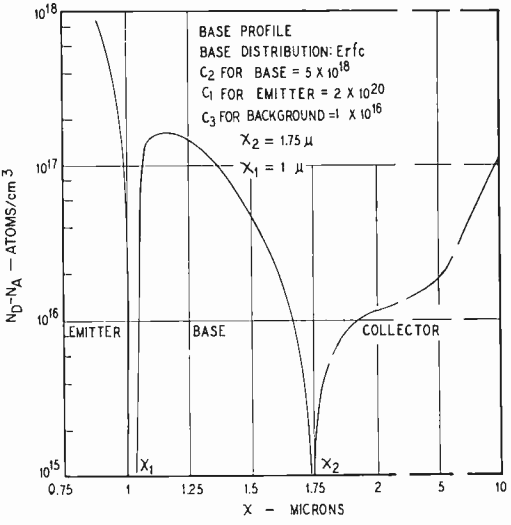


Fig. 2—One of the possible impurity distributions for the 2N1708 transistor.

determined by the width of the intrinsic region, *i*. Gaussian types have the space-charge layer divided unequally.

The general expression for barrier capacitance, C, is

$$\frac{C}{A} = \frac{K\epsilon_0}{X_m}, \tag{1}$$

where A is the junction area, ϵ_0 is the permittivity, K is the dielectric

Table I

R_p, Pellet radius	2.5×10^{-2} cm
A_c, Collector area	3.2×10^{-4} cm^2
R_e, Emitter radius	5×10^{-3} cm
A_e, Emitter area	7.8×10^{-5} cm^2
w, Base width	0.75×10^{-4} cm
x_s, Depth of collector–base junction	1.75×10^{-4} cm
R_s, Base sheet resistance	400 ohms per square
W_c, Thickness of high-resistivity collector region (approximate)	5×10^{-4} cm
ρ_c, Collector-region resistivity (after all diffusion steps)	1 ohm-cm
a_c, Gradient at collector-base junction	4×10^{20} cm^{-4}
a_e, Gradient at emitter-base junction	10^{23} cm^{-4}

constant, and X_m is the thickness of of the space-charge region. For a step junction,

$$\frac{C}{A} = K\epsilon_0 \left[\frac{q(N_D - N_A)}{2K\epsilon_0 V} \right]^{1/2}, \tag{2}$$

where q is the charge of an electron, V is the total potential, and N_D and N_A are the donor and acceptor densities, respectively. For graded junctions,

$$\frac{C}{A} = \frac{K\epsilon_0}{2} \left[\frac{2qa}{3K\epsilon_0 V} \right]^{1/3}, \tag{3}$$

where a is the impurity gradient. For exponential-type distributions,[1] the capacitance expressions exist only as tabular functions.

For diffused-junction transistors, the linear-graded case is a rea-

sonable approximation. For epitaxial structures, in which the space-charge region extends into the heavily doped substrate, the p+in+ calculation approximates the expression for the capacitance. Capacitance decreases as the reverse voltage increases until the avalanche[5] or reach-through voltage is attained.

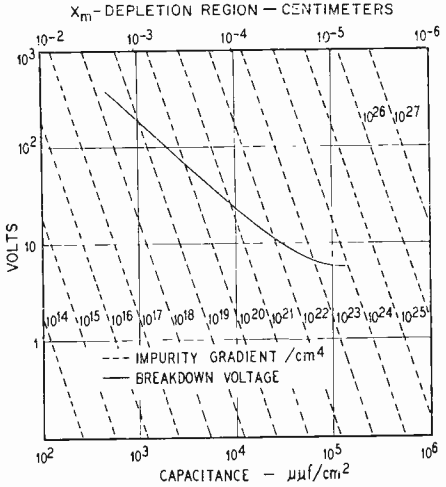


Fig. 3—Relationship between space-charge width, capacitance, potential and breakdown voltage for linear graded silicon p-n junction. (After Veloric and Smith.[1])

Figure 3 shows the relationship between space-charge width, capacitance, potential, and breakdown voltage for various values of impurity gradient. The breakdown voltage is estimated from experimental data.[6] The curve shows that for a given impurity gradient, the variation of capacitance with potential and the avalanche breakdown voltage are fixed.

Figure 4 is a curve which relates breakdown voltage to barrier width and junction capacitance for p+in+ structures. At low voltages, the barrier extends through the intrinsic region and remains fixed up to the breakdown voltage indicated in Figure 4. The 2N1708, which has a collector body 5 microns thick, has a *maximum* collector

[5] S. L. Miller, "Avalanche Breakdown in Ge," *Phys. Rev.*, Vol. 99, p. 1234, Aug., 1955.

[6] H. S. Veloric, M. B. Prince and M. Eder, "Avalanche Breakdown Voltage in Silicon Diffused p-n Junctions as a Function of Impurity Gradient," *Jour. Appl. Phys.*, Vol. 27, p. 895, Aug., 1956.

breakdown voltage of 80 volts. Because the collector body is not intrinsic, the breakdown voltage is less than 80 volts.

Minority Carrier Lifetime

Minority-carrier lifetime affects device parameters such as current gain, saturation current, and storage time.

Shockley and Read[7] have discussed the dependence of bulk lifetime

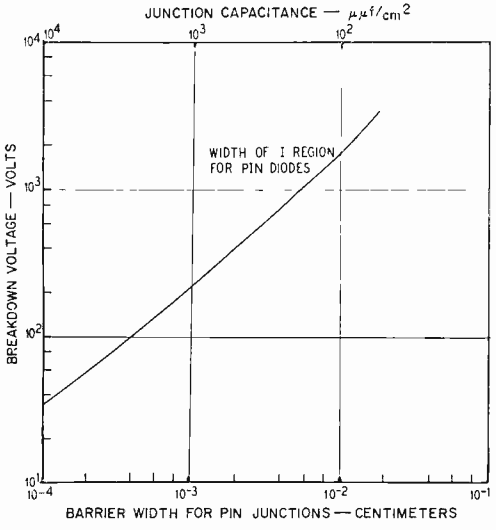


Fig. 4—Breakdown voltage, barrier width, and junction capacitance for p+in+ silicon structures. (After Velonic and Prince.[3])

on the density of recombination centers in great detail. When the density of recombination centers is N, with a capture cross section σ_{p0} for holes and σ_{n0} for electrons, the minority-carrier lifetime τ for a low level of minority-carrier injection is

$$\tau = \frac{n_0 + n_1}{n_0 + p_0}\tau_{p0} + \frac{p_0 + p_1}{n_0 + p_0}\tau_{n0}. \tag{4}$$

The terms n_0 and p_0 represent the equilibrium electron and hole densities; n_1 and p_1 are given by

$$n_1 = n_i \exp \frac{(E_{t1} - E_i)}{kT} \tag{5a}$$

[7] W. Shockley and W. J. Reed, Jr., "Statistics of the Recombination of Holes and Electrons," *Phys. Rev.*, Vol. 87, p. 835, Sept. 1952.

$$p_1 = n_i \exp \frac{(E_i - E_{t2})}{kT}. \tag{5b}$$

The term n_i is the intrinsic carrier density, E_{t1} and E_{t2} are recombination center energy levels, and E_i is the intrinsic Fermi level.

The lifetime of holes injected into highly n-type material is

$$\tau_{p0} = \frac{1}{\sigma_{p0} v_p N}. \tag{6a}$$

The lifetime of electrons injected into highly p-type material is

$$\tau_{n0} = \frac{1}{\sigma_{n0} v_n N}, \tag{6b}$$

where v_p and v_n are the thermal velocities for holes and electrons, respectively.

The most commonly used technique for controlling minority-carrier lifetime in silicon is the introduction of gold. The diffusion of gold introduces two trapping levels: an acceptor level at 0.54 electron-volt below the conduction band and a donor level at 0.35 electron-volt above the valence band.[8,9] In n-type silicon, only the acceptor level is assumed to be effective; in p-type silicon, only the donor level is assumed effective.

For an n-type sample in which n_0 is much greater than p_0, Equation (4) can be reduced as follows:

$$\tau = \tau_{p0}\left(1 + \frac{n_1}{n_0}\right)$$
$$\tau = \tau_{p0}\left[1 + \exp \frac{(E_{t1} - E_f)}{kT}\right], \tag{7}$$

where E_f is the Fermi level of the sample.

When n_1 is much greater than n_0, the material is lightly doped. The Fermi level is lower than the level of the trap. The traps are mostly empty, and recombination is limited because electrons are not

[8] G. Bemski, "Recombination Properties of Gold in Silicon," *Phys. Rev.*, Vol. 111, p. 1515, Sept. 1958.

[9] C. B. Collins, R. O. Carson and C. J. Gallagher, "Properties of Gold Doped Silicon," *Phys. Rev.*, Vol. 105, p. 1168, Feb. 1957.

readily available for recombination with holes. For high-resistivity n-type silicon, Equation 4 may be reduced as follows:

$$\tau \cong \tau_{p0} \frac{n_1}{n_0}. \tag{8}$$

For a given number of recombination centers, the lifetime in a high-resistivity crystal increases as the resistivity is increased because the efficiency of recombination decreases.

In strongly n-type material in which E_f is greater than E_{t1} and n_0 is much greater than n_1, the lifetime is independent of doping and may be expressed as follows:

$$\tau \cong \tau_{p0} \cong \frac{1}{\sigma_{p0} v_p N}. \tag{9}$$

In this case, which is the approximation of practical interest,[10] all the traps are full, and sufficient electrons are available to permit ready recombination with holes.

Figure 5 shows a curve of τ_{n0} and τ_{p0} and gold concentration for silicon as a function of the temperature of gold introduction. For this curve, it is assumed that the gold concentration is determined by the temperature at which the gold is introduced. The solubility is based on results published by Collins *et al.*[9]

Figure 6 shows τ/τ_{n0} or τ/τ_{p0} as a function of the net impurity concentration with gold as the recombination center. The curve, which is a plot of Equations (7) and (8), illustrates the effect of the Fermi level approaching the trapping level. Because of the different effective trapping levels, lifetime is more difficult to reduce in moderately doped p-type material than in similarly doped n-type silicon. Figures 5 and 6 present all the data required to estimate lifetime from the temperature at which gold is introduced and the net impurity concentration. For n-type and p-type materials, there is an increase in lifetime when the gold concentration is comparable to the background doping.

Space-Charge-Generated Reverse Current

It has been determined that reverse current[11] in silicon p-n junc-

[10] A. E. Bakanowski and J. H. Foster, "Electrical Properties of Gold Doped Diffused Silicon Computer Diodes," *Bell Sys. Tech. Jour.*, Vol. 39, p. 87, Aug. 1959.

[11] C. T. Sah, R. N. Noyce and W. Shockley, "Carrier Generation and Recombination in p-n Junctions and p-n Junction Characteristics," *Proc. I.R.E.*, Vol. 45, p. 1228, Sept. 1955.

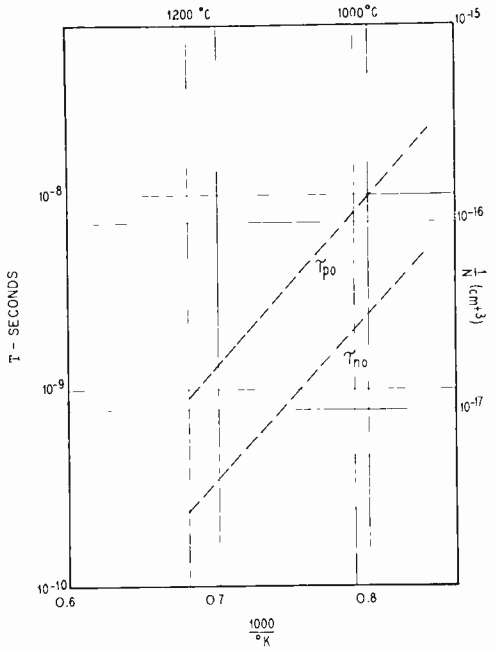


Fig. 5—τ_{p_0}, τ_{n_0} and gold concentration as a function of the temperature of gold introduction (gold solubility data from Collins *et al*[9]).

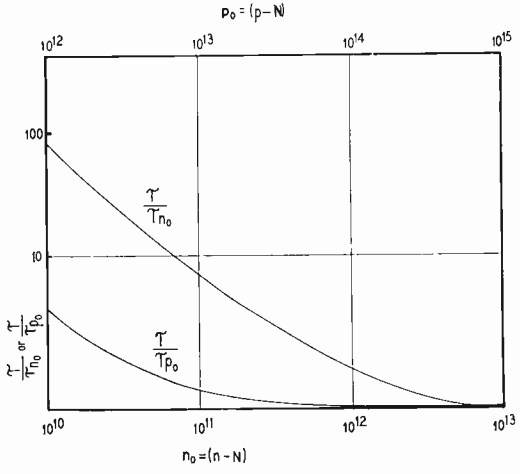


Fig. 6—τ/τ_{n_0}, τ/τ_{p_0} as a function of n_0 or p_0 with gold as the recombination center.

tions arises from carrier generation in the space-charge region. For moderate reverse bias, the reverse current I_{CO} is[10]

$$I_{CO} = qUX_mA$$
$$U = \frac{n_i}{\tau_{n0} + \tau_{p0}}. \tag{10}$$

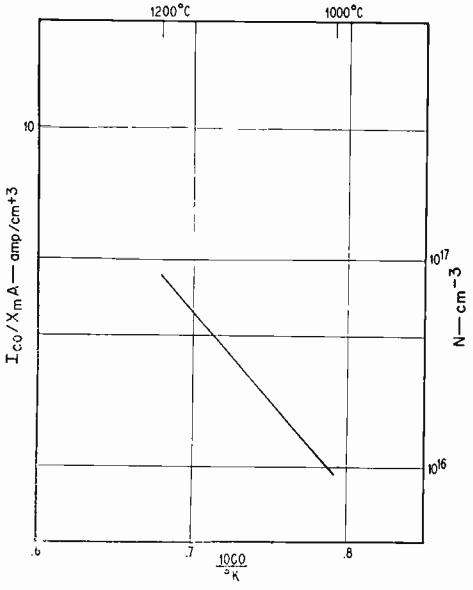


Fig. 7—Gold concentration, N, and space-charge-generated current as a function of the temperature at which the gold is introduced.

Figure 7 shows gold concentration and space-charge-generated current as a function of the temperature at which the gold is introduced.

TRANSISTOR PARAMETERS

Collector-to-Emitter Voltage, V_{CE}(sat)

This section reviews the Ebers and Moll derivations[12] covering the voltages and currents required to operate a transistor in the three operating regions. In saturation, the potentials of the p-type material relative to the n-type material are expressed

[12] J. J. Ebers and J. L. Moll, "Large Signal Behavior of Junction Transistors," *Proc. I.R.E.*, Vol. 42, p. 1761, Dec. 1954.

$$\phi_e = \frac{ykT}{q} \ln \left(- \frac{I_E + \alpha_i I_C}{I_{EO}} + 1 \right) \tag{11}$$

$$\phi_c = \frac{ykT}{q} \ln \left[- \frac{I_C + \alpha_i I_E}{I_{CO}} + 1 \right] \tag{12}$$

where y varies between 1 and 2. ϕ_e and ϕ_c are the voltages across the emitter–base and base–collector junctions, respectively. I_E and I_C are the emitter and collector currents respectively, α_i is α with the collector as emitter, and I_{EO} and I_{CO} are the emitter and collector saturation currents, respectively, at zero bias.

Subtracting Equation (11) from Equation (12) and rearranging terms results in the following expression for $V_{CE}(\text{sat})$, which neglects ohmic drops in the emitter and collector region:

$$V_{CE}(\text{sat}) = \pm y \frac{kT}{q} \ln \frac{1 + \dfrac{I_C}{I_B}(1 - \alpha_i)}{\alpha_i \left[1 - \left(\dfrac{1 - \alpha}{\alpha} \right) \dfrac{I_C}{I_B} \right]}. \tag{13}$$

If $y = 1$,

$$V_{CE}(\text{sat}) \cong \pm .026 \ln \frac{1 + h_{FEI} + \dfrac{I_C}{I_B}}{h_{FEI} \left(1 - \dfrac{I_C}{I_B h_{FE}} \right)}.$$

where I_B is the base current, h_{FE} is the common-emitter current-transfer ratio, and h_{FEI} is the common-emitter current-transfer ratio with the collector as the emitter.

Figure 8 shows V_{CE} as a function of h_{FE} for various values of h_{FEI} when the circuit gain I_C/I_B is 10. If the h_{FE} is greater than four times I_C/I_B, there is no appreciable decrease in V_{CE}. The V_{CE} is shown to be a strong function of h_{FEI} and, therefore, increases with decreasing symmetry. The magnitude of the saturation voltage shown in Figure 8 suggests that the Ebers–Moll expression does not predict the major voltage drop in a diffused junction transistor. In these devices, the voltage drop resulting from the collector spreading resistance, R_{SC}, is significant.

The collector-to-emitter voltage in saturation, including the collector spreading resistance and neglecting the emitter resistance, is

$$V_{CE}(\text{sat}) \cong \phi_c - \phi_e + I_C R_{SC}. \tag{14}$$

Spreading resistance calculated from solutions of the Laplace equation by Kennedy[13] is shown in Figure 9 in a form applicable to a range of geometrical parameters. The curve shows normalized spreading resistance as a function of the height and radius of the cylinder for values of the ratio of emitter radius to cylinder radius.

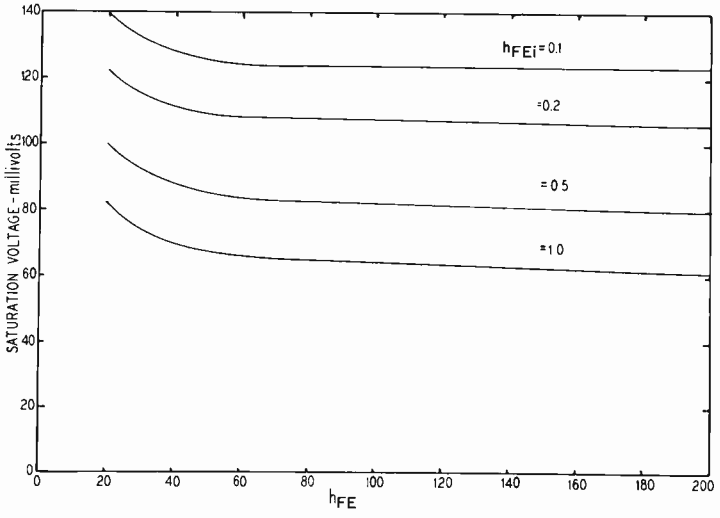


Fig. 8—Low current V_{CE} as a function of h_{FE} for various values of h_{FEI} for $I_C/I_B = 10$.

Base-to-Emitter Voltage, V_{BE}

The base-to-emitter voltage V_{BE} essentially consists of two terms, one term resulting from the base resistance and the other term derived from the emitter-diode equation in which injection from the collector is included. Ebers and Moll[12] have shown that the latter voltage is given by Equation (11).

The saturation current of the emitter junction at zero collector current, I_{EO}, is proportional to the emitter area. At low current densities, the saturation current in silicon junctions is generated in the space-charge layers, and the value of y in Equation (11) is 2. At higher current densities, the saturation current originates mainly in

[13] D. P. Kennedy, "Spreading Resistance in Cylindrical Semiconductor Devices," *Jour. Appl. Phys.*, Vol. 31, p. 1490, Aug. 1960.

the bulk and y reduces to unity. At still higher current densities y again has a value of 2.

In an emitter–base circuit,

$$V_{BE} \cong \phi_e + I_B r_{b'} \tag{15}$$

where $r_{b'} = (R_S/2\pi)$ ln (R_1/R_e), and R_S is the base sheet resistance

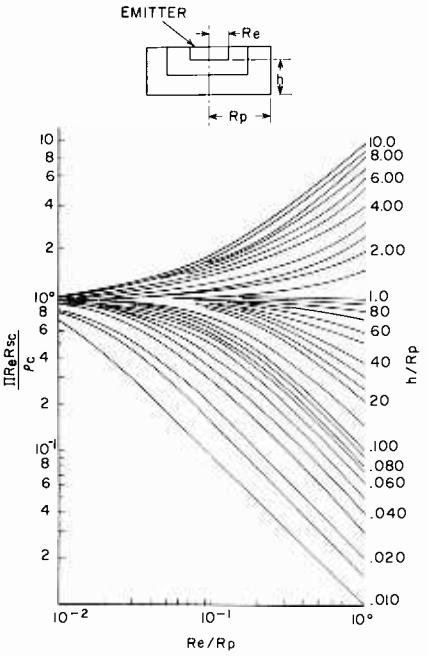


Fig. 9—Normalized collector spreading resistance R_{sc} as a function of the height and radius of the cylinder for various values of the ratio of emitter radius to the cylinder radius. (After Kennedy.[13])

in ohms per square, R_1 is the base contact radius and R_e is the emitter radius. The resistance under the emitter can be neglected because of conductivity modulation effects. Figure 10 shows $r_{b'}$ as a function of R_1/R_e, with R_S as the plotted parameter.

Figure 11 shows ϕ_e as a function of I_E, measured for a transistor having an emitter area of 7.8×10^{-5} square centimeter. There is reasonable agreement at low current; the deviation at high current levels may be attributed to underestimating the value of the $I_B r_{b'}$ term and the $\alpha_i I_C$ term at high current density.

Emitter-to-Collector Breakdown Voltage, V_{CEO}

In a transistor structure, multiplicative processes are important in the analysis of the minority-carrier base current collected at the collector junction. The common-base current gain of a transistor,[14] with the base open, as a function of the applied voltage V_{CE} and the

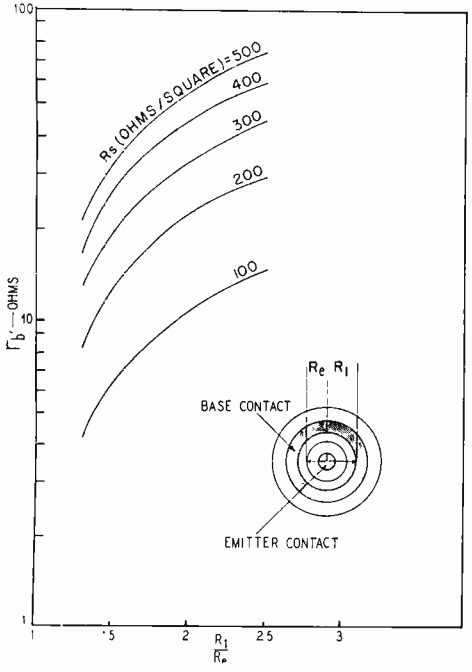


Fig. 10—$r_{b'}$ as a function of the ratio of the distance from the edge of the base contact to the emitter edge with the base sheet resistance as the plotted parameter.

bulk breakdown voltage V_{CBO} of the collector-base junction is expressed as follows:

$$\alpha(V) = \frac{\alpha}{1 - \left(\frac{V_{CE}}{V_{CBO}}\right)^n}. \tag{16}$$

From Equation (16), the collector-to-emitter voltage V_{CEO} at which

[14] J. J. Ebers and S. L. Miller, "Design of Alloyed Junction Germanium Transistors for High Speed Switching," *Bell Sys. Tech. Jour.*, Vol. 34, p. 893, July 1955.

$\alpha(V)$ becomes unity is given approximately by

$$V_{CEO} \cong \frac{V_{CBO}}{(h_{FE})^{1/n}}. \tag{17}$$

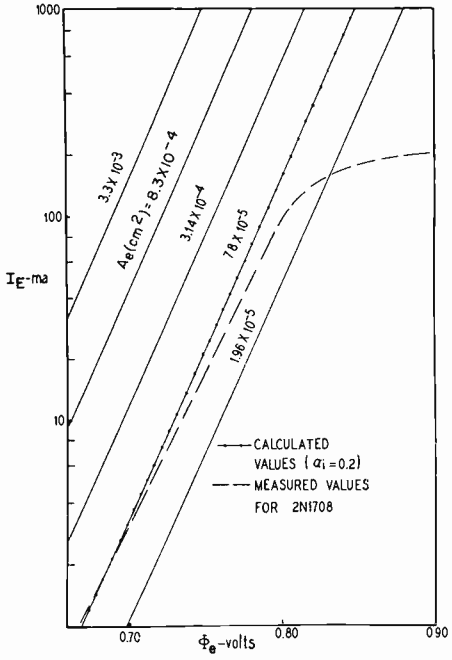


Fig. 11—ϕ_e as a function of emitter current with the emitter area as the plotted parameter.

The sustained collector-to-emitter voltage is determined by the collector breakdown voltage, the current gain, and the value of n for the particular junction. For n-p-n silicon transistors, the value of n is[15] between 3 and 4. Figure 12 shows the collector-to-emitter voltage as a function of the common-emitter current gain and the avalanche-breakdown voltage for a 2N1708 transistor. The value of n is in reasonable agreement with Miller's data.[15] The data show that, for typical values of current gain, the V_{CEO} will be about 40 per cent of the collector-to-base breakdown voltage.

[15] S. L. Miller, "Ionization Rate for Holes and Electrons in Silicon," *Phys. Rev.*, Vol. 105, p. 1246, Feb. 1957.

Common-Emitter Current Gain, h_{FE}

It has been shown[14,16] that gain is a function of four parameters:

(1) The emitter efficiency γ, which is the ratio between the emitter current carried by minority carriers from the emitter to the base region and the minority-carrier current flowing from the base into the emitter.

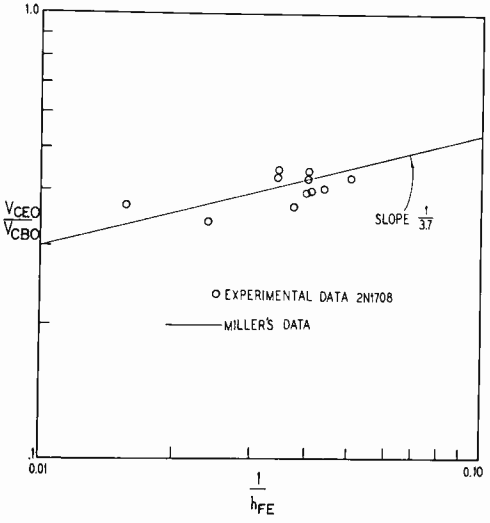


Fig. 12—The collector to emitter voltage V_{CEO} of a silicon n-p-n transistor as a function of the common emitter current gain and the avalanche breakdown voltage.

(2) The base transport factor β, which is the fraction of minority carriers which diffuse across the base and reach the collector.

(3) The collector efficiency α^*, which is assumed to be unity in this analysis.

(4) M, which is the voltage-dependent current-multiplication factor.

The total common-base current gain α is the product of all four parameters. The common-emitter current gain, h_{FE}, is $\alpha/(1-\alpha)$.†

The emitter efficiency is determined by the ratio of the doping in

---

[16] W. Shockley, M. Sparks and G. K. Teal, "P-N Junction Transistors," *Phys. Rev.*, Vol. 83, p. 151, July 1951.

† The full expression of the common-emitter current gain was derived by W. M. Webster, "On the Variation of Junction-Transistor Current Amplification Factor with Emitter Current," *Proc. I.R.E.*, p. 914, June 1954. The effect of surface recombination and base modulation which occurs at high current injection levels was neglected in the present simplified analysis.

the emitter (within a diffusion length L_e of the emitter junction) to the net doping in the base. For a double-diffused n-p-n silicon transistor having an emitter surface concentration C_1, base-surface concentration, C_2, and a background doping C_3, the emitter efficiency can be calculated[17] as follows.

If $M = 1$ and $\beta = 1$, then

$$h_{FE}(\max) = \frac{\gamma}{1-\gamma} =$$

$$\left[\int_{L_e}^{x_1}\left(C_1 \operatorname{erfc}\frac{x}{2\sqrt{D_1 t_1}} - C_2 \operatorname{erfc}\frac{x}{2\sqrt{D_2 t_2}} + C_3\right) dx\right]\frac{D_n}{D_p B}. \qquad (18)$$

The total net number of acceptors under the emitter, B, is assumed to be 2×10^{12} atoms per cm^2, the number required to prevent electrical reach-through at 25 volts; D_n and D_p are the diffusion coefficients for electrons and holes, respectively; x_1 and x_2 are the emitter and collector junction penetrations, respectively; L_e is the diffusion length of holes in the emitter; and $\sqrt{D_1 t_1}$ is the diffusion length of emitter diffusants and $\sqrt{D_2 t_2}$ is the diffusion length of base diffusants.

Figure 13 shows $\gamma/(1-\gamma)$ as a function of the diffusion length in the emitter, L_e; three values of collector penetration are plotted as parameters. As the collector penetration is increased, the diffusion length in the emitter must be increased to maintain high emitter efficiency. At very high frequencies, the emitter efficiency is limited by the reduction of the effective diffusion length of the minority carriers.[18]

In many cases, the current gain of a transistor is limited by the transport factor. If the effect of the transport factor alone is considered, the following expression may be written for h_{FE} (max):

$$h_{FE}\ (\max) = \frac{\beta}{1-\beta} \cong \frac{2 D_n \tau}{w^2} \qquad (19)$$

where w is the base width. According to Fletcher,[19] a radial voltage

---

[17] H. S. Veloric, C. Fuselier and D. Rauscher, "Base-Layer Design for High-Frequency Transistors," *RCA Review*, p. 112, March 1962.

[18] H. L. Armstrong, "On Calculating the Current Gain of Junction Transistors with Arbitrary Doping Distributions," *IRE Trans. Electronic Devices*, Vol. ED-6, p. 1, Jan. 1959.

[19] N. H. Fletcher, "Self-bias Cut-off Effect in Power Transistors," *Proc. I.R.E.*, Vol. 43, p. 1669, Nov. 1955.

drop resulting from the flow of the base current causes current emission at the edge of the emitter rather than at its center. High current density at the emitter edge causes conductivity modulation, even at low emitter currents. This fringing effect swamps out any built-in field originally present in the base region. Therefore, the effect of the built-in field has been neglected here. Double-diffused structures

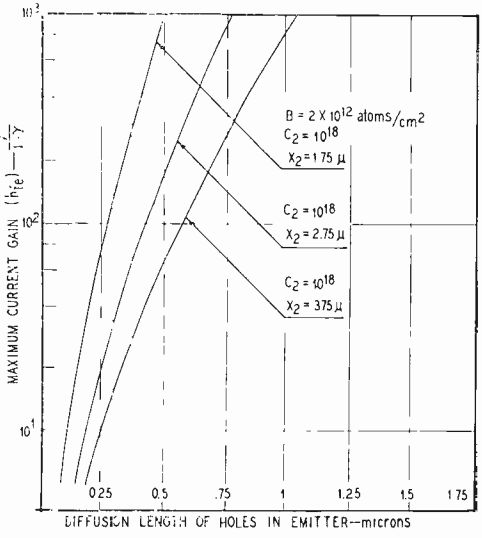


Fig. 13—$\gamma/(1-\gamma)$ for a double-diffused n-p-n transistor as a function of the diffusion length in the emitter with three values of collector penetration as the plotted parameter.

have both a retarding and an accelerating field which tend to cancel each other.

Figure 14 shows the transport-limited current gain $\beta/(1-\beta)$ as a function of base width, with the lifetime in the base as the plotted parameter. If the base width is of the order of 1 micron, the lifetime must be in the order of 10^{-8} second for reasonable values of h_{FE}.

The current multiplication term M is an empirical expression[15] defined as follows:

$$M = \frac{1}{1-\left(\frac{V_{CE}}{V_{CBO}}\right)^n}.$$

Electrical Reach-Through Voltage

If the impurity distributions in the base and collector regions are known, solutions of Poisson's equation determine the space-charge penetration as a function of the applied voltage. Solutions were obtained for several impurity[17] distributions. The error-function complement distribution is described by

$$|N_{\prime\prime} - N_A| = C_1 \operatorname{erfc} \frac{x}{2\sqrt{D_1 t_1}} - C_2 \operatorname{erfc} \frac{x}{2\sqrt{D_2 t_2}} + C_3. \quad (20)$$

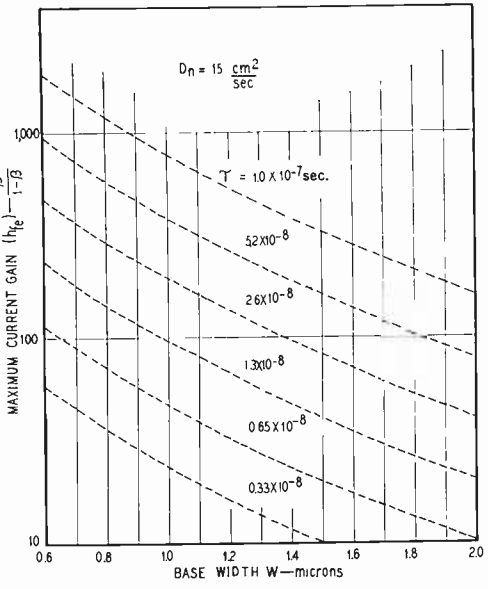


Fig. 14—$\beta/(1-\beta)$ as a function of base width with the lifetime in the base as the plotted parameter.

Equation (20) can be simplified to the case of a single-diffused junction in material of constant impurity doping if the contribution of the emitter diffusion is neglected.[4] With several approximations, and by selecting specific values for the impurity distribution parameters C_1, C_2, C_3, and x_2, it is possible to integrate Equation (20) and relate the impurity parameters to the reach-through voltage. If C_1 is fixed at 2×10^{20}, C_3 at 2×10^{16}, and $x_2 - x_1 = w = 7.5 \times 10^{-5}$ centimeter, the reach-through voltage can be plotted as a function of x_2 for two values of base surface concentration $C_2 = 5 \times 10^{18}$ and $C_2 = 5 \times 10^{19}$.

The total number of uncompensated impurities between x_1 and x_2 is evaluated by integrating Equation (20). The space-charge layer sweeps out an equal number of impurities in the collector region, and the reach-through voltage can be computed from the spread of the space-charge layer into the collector region.

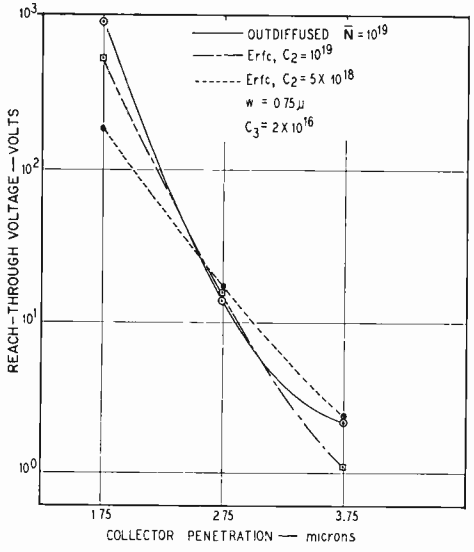


Fig. 15—Reach-through voltage as a function of collector penetration for a silicon transistor having a base width of 7.5×10^{-5} cm, with two values of surface concentration as the plotted parameter.

Figure 15 shows the reach-through voltage as a function of collector penetration for a silicon device having a fixed base width of 7.5×10^{-5} centimeter; two values of surface concentration are plotted as the parameters. Because the reach-through voltage depends upon the doping under the emitter, it is insensitive to the surface concentration, but sensitive to collector penetration. For a reach-through voltage in excess of 25 volts, the total number of net impurities under the emitter must be in excess of 2×10^{12} atoms per square centimeter.

Switching Parameters

The frequency response of a transistor is determined by calculating the signal delay between injection of electrons at the emitter and the signal response at the output circuit. f_t, the frequency at which h_{FE}

is 1, is

$$f_t \cong \frac{1}{2\pi \sum \tau_d}$$

where $\sum \tau_d$ is the summation of the four time constants associated with the various delays in moving the charge from the emitter to the collector circuits. The four delay times are the emitter phase delay τ_e, the base transit-time delay τ_b, the transit time across the collector space-charge region τ_m, and the time required to charge the collector capacitance τ_c.

$$\tau_e = \left(\frac{kT}{qI_E}\right) C_{TE} \tag{21}$$

where I_E is the emitter current, and C_{TE} is the emitter transition capacitance.

$$\tau_b \cong \frac{w^2}{2D_n},$$

$$\tau_m = \frac{X_m}{2V_{\max}} \cong \frac{X_m}{10^7}, \tag{23}$$

where $V_{\max}$ is the maximum drift velocity for electrons.[20] X_m can be obtained from the collector spreading resistance, R_{SC}, and junction capacitance C_C (see Figure 4).

$$\tau_c = R_{SC}\, C_C, \tag{24}$$

assuming no load resistance.

Turn-On Delay and Rise Time

The charge required to turn a transistor on consists of three parts: Q_E, which goes into the emitter transition region; Q_C, which goes into the collector transition region; and Q_B, which goes into the base proper. Hence, the total time t_{on} required to bring the collector current to its final value is given by

---

[20] E. J. Ryder, "Mobility of Holes and Electrons in High Electric Fields," *Phys. Rev.*, Vol. 90, p. 766, June 1953.

$$t_{on} = \frac{Q_E + Q_C + Q_B}{I_{BI}} \tag{25}$$

where I_{BI} is the turn-on base current.

For the double-diffused transistor, it can be shown by integrating the junction capacitances between the on and off voltages that Q_E and Q_C may be approximated by

$$Q_E = 3.68 \times 10^{-15}\, \alpha_e A_e \left([V_{BE}\,(\text{off}) + V_i]^{2/3} - (V_i)^{2/3}\right), \tag{26}$$

$$Q_C = 3.68 \times 10^{-15}\, \alpha_c A_c \left([V_{CC} + V_{BE}\,(\text{off}) + V_i]^{2/3} - [V_{CC} + V_i]^{2/3}\right), \tag{27}$$

where V_i is the built-in junction potential; α_e and α_c are the doping density gradients at the emitter and collector junctions, respectively; A_e and A_c are the emitter and collector junction areas; V_{CC} is the collector bias voltage; and $V_{BE}(\text{off})$ is the applied base-to-emitter voltage.

The delay time t_d is defined as the time required for the collector current to reach 10 per cent of its final value. This time is approximately

$$t_d \cong \frac{Q_E + Q_C}{I_{BI}}. \tag{28}$$

This expression neglects the fraction of the delay time determined by the transit time of minority carriers through the base. This additional time, approximately equal to one tenth of the rise time, is generally small compared to the time required to charge the junction capacitances.

The additional time required to introduce Q_B, which increases the collector current to 90% of its final value, is defined as the rise time. P. E. Kolk[21] has derived an expression for the rise time which takes into consideration the effect of the impurity distribution in the base layer. Moll and Thomas[22] have shown that α, f_a, and f_t are related as follows:

$$K^* = \frac{f_t}{\alpha f_a}. \tag{29}$$

---

[21] P. E. Kolk, Private Communication.

[22] D. E. Thomas and J. L. Moll, "Junction Transistor Short Circuit Gain and Phase Determination," *Proc. I.R.E.*, Vol. 46, p. 1177, June 1958.

Theoretically K^* should be 0.82 when no fields are present in the base, less than 0.82 for built-in aiding fields, and greater than 0.82 for retarding fields. Equation (29) was derived on the assumption that no appreciable cutoffs result from collector, base, or emitter resistances combining with the collector-junction capacitance. This assumption is not valid for the 2N1708.

However, it has been found experimentally that the measured values of α, f_α, and f_t are related by a constant, K' having a value of about 0.8 (Table II).

Table II—Calculated and Observed Rise Time for Typical 2N1708 and 2N697 Transistors*

f_α (3 db) (5v, 10ma) (measured)	α (5v, 10 ma) (1 kc) (measured)	f_t (5v, 10 ma) (measured)	K' (calculated)	h_{FE} (1 kc) (5v, 10 ma) (measured)	Measured t_r (nsec) I_C = 10 ma I_{B1} = 3 ma R_L = 220 ohms	C_O pf (1v) (measured)	Calculated t_r (nsec)
			2N1708				
485	0.9766	330	0.700	39.0	7.6	3.45	6.05
495	0.9768	355	0.735	38.9	6.0	3.50	5.80
445	0.9710	320	0.746	34.1	7.0	3.20	4.85
420	0.9756	380	0.928	37.8	8.0	3.35	4.50
460	0.9741	380	0.740	35.0	8.0	3.10	4.04
460	0.9778	350	0.782	40.8	8.0	3.45	5.10
			2N697				
V_{CC} = 10v I_C = 5 ma							
108	0.9785	90.5	0.860	44.1	28	28.4	29.05
102	0.9794	95.0	0.950	46.1	22	25.8	24.85
105	0.9807	83.0	0.810	49.0	24	27.9	27.70
101.5	0.9821	84.5	0.840	52.8	28	30.2	31.50
106	0.9839	96.5	0.930	59.1	28	28.9	30.50
117	0.9912	101.0	0.870	120.0	22	26.6	25.60
106	0.9864	90.0	0.860	68.7	24	28.7	27.80
98.9	0.9836	88.5	0.910	58.1	28	29.1	30.80
103.5	0.9871	86.5	0.850	73.8	24	28.4	28.10
105	0.9842	84.5	0.820	61.1	28	29.8	29.75

* Data supplied by P. E. Kolk.

The complete equation relating the rise time t_r to pertinent device and circuit parameters is

$$t_r = \frac{h_{FE} K'}{\omega_t} \left[\frac{\omega_t (R_L + R_{SC}) C_C}{\alpha K'} + 1 \right] \ln \left[\frac{1 + \dfrac{(K' - 1)(1 - \alpha)}{K' \left(\dfrac{f_t}{\alpha K' f_c} + 1 \right)}}{1 - \dfrac{0.9 I_C}{h_{FE} I_{BI}}} \right], \quad (30)$$

where

$$\omega_t = 2\pi f_t,$$

$$f_c = \frac{1}{2\pi C_C (R_L + R_{SC})},$$

$$f_t = f_a K' \alpha,$$

R_L = Load resistance.

Table II compares the measured rise times and the values calculated from Equation (30). The agreement is very good for the slower devices, and quite good for the very fast ones, considering the difficulties in making measurements at these speeds because stray circuit capacitances and resistances are appreciable in relation to those of the device itself.

Minority-Carrier Storage Time

Ebers and Moll[12] have derived an expression for the storage time of minority carriers in the base, t_s, assuming no storage in the collector:

$$t_s = \frac{\omega_N + \omega_I}{\omega_N \omega_I (1 - \alpha \alpha_i)} \ln \frac{I_{B1} - I_{B2}}{I_C \dfrac{(1 - \alpha)}{\alpha} - I_{B2}} \quad (31)$$

where ω_N and ω_I are the forward and inverse alpha cutoff frequencies multiplied by 2π. This equation is generally valid for alloyed devices. For diffused-base transistors, however, the assumption of no collector storage is no longer valid. In fact, storage times calculated from Equation (31) yield values considerably smaller than those observed, because minority-carrier storage occurs mainly in the collector region.

Grinich and Noyce[23] have calculated the storage time for this type

[23] J. Grinich and R. N. Noyce, "Switching Time Calculations for Diffused Base Transistors," *IRE-Wescon Convention Record*, 1958.

of transistor by using the diode-recovery equation of Lax and Neustader[24] for the collector-base diode;

$$\text{erf}\sqrt{\frac{t_s}{\tau}} = \frac{I_f}{I_f + I_r}, \tag{32}$$

where τ is the collector minority-carrier lifetime, I_r is the minority-carrier current flow in the collector body during the recovery phase, and I_f is the minority-carrier current flow in the collector body during the period of forward conduction.

The various diode currents can be translated into equivalent transistor currents as follows:

$$I_f = \frac{h_{FE} I_{B1} - I_C}{1 + h_{FE}}, \tag{33a}$$

$$I_r = \frac{h_{FE} I_{B2} - I_C}{1 + h_{FE}}, \tag{33b}$$

where I_{B1} is the base current during the forward bias, and $-I_{B2}$ is the current during the recovery period. Hence, Equation (32) may be rewritten

$$\text{erf}\sqrt{\frac{t_s}{\tau}} = \frac{h_{FE} I_{B1} - I_C}{h_{FE}\,(I_{B1} + I_{B2})}. \tag{34}$$

Equation (34) yields fair agreement with measured values of transistor storage time if the value of τ calculated from the diode recovery time for the collector–base diode is used (Figure 16); the calculated values are generally optimistic.

For nonepitaxial transistors, the storage time is found to increase with collector current up to a peak value, and then to decrease again. This effect has not been noticed in epitaxial transistors. An attempt has been made to explain this behavior[25,26] as follows: The voltage drop due to the base resistance $r_{bb'}$ is the only significant voltage drop in an epitaxial transistor because R_{SC} is small. As a result, the bulk of the minority carriers which are injected into the collector region

---

[24] B. Lax and S. F. Neustadter, "Transient Response of p-n Junction," *Jour. Appl. Phys.*, Vol. 25, p. 1148, Sept. 1954.

[25] J. E. Iwerson, "Storage Time in Diffused Base Transistors," *Solid State Device Research Conference*, June 1961.

[26] J. Stewart, Private Communication.

during saturation are injected under the base contact rather than under the emitter. The storage time of the device is the storage time of the base–collector diode because the transistor part of the device (i.e., the part under the emitter) receives only a negligible portion of the minority carriers injected into the collector region.

The same model predicts the behavior of nonepitaxial transistors in saturation. R_{sc} is of the order of $r_{b'}$. At high values of I_C and low

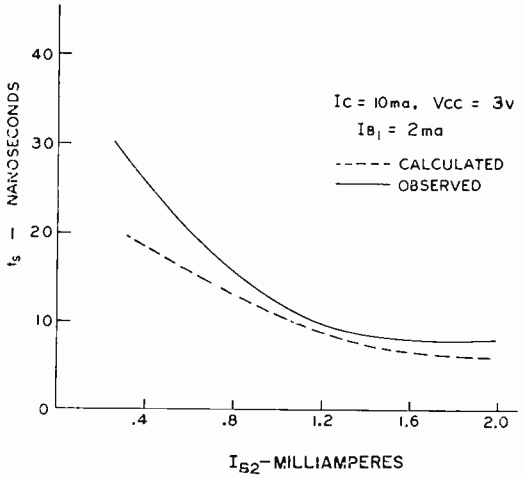


Fig. 16—Observed and calculated values of storage time using the lifetime calculated from collector–base diode recovery time.

values of I_{B1}, the "transistor part" is in saturation because the voltage drop resulting from R_{sc} is appreciable. For low values of I_C and high values of I_{B1}, the diode is the important storage factor because the voltage drop due to $r_{b'}$ is much greater than the drop resulting from R_{sc}. When gold is not used to reduce the lifetime in the collector region, the diffusion length of the minority carriers can be greater than the width of the epitaxial layer. The time required for the charge injected at the collector–base junction to diffuse through the width of the epitaxial layer is important in determining storage time. This is the "narrow diode" case previously considered by Kingston.[27] Figure 17 shows the storage time parameter $T = Dt_s/W_c^2$ as a function of circuit conditions and h_{FE}, where W_c is the width of the collector region. From T, the storage time can be determined if the effective

[27] R. H. Kingston, "Switching Time for Junction Diodes and Junction Transistors," *Proc. I.R.E.*, Vol. 42, p. 829, May 1954.

width of the epitaxial layer is known and it is assumed that the epitaxial boundary is a high recombination interface.

Comparison of Calculated and Observed Parameters

The following comparison of observed and calculated device parameters, based on the 2N1708, indicates areas of agreement and deviation; these data are summarized in Table III.

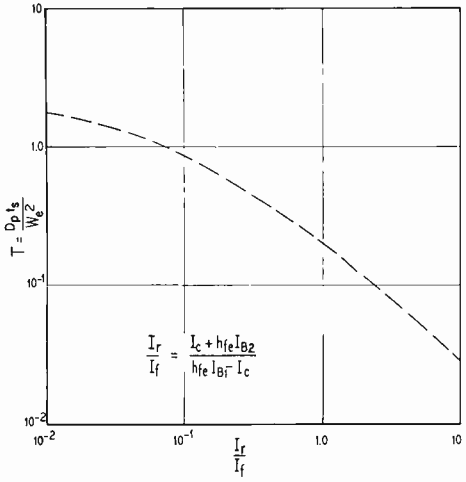


Fig. 17—$T = Dt_s/W_e^2$ as a function of circuit conditions and h_{FE} for the case where the diffusion length is much greater than the width of the epitaxial region, W_e. (After Kingston.[27])

Diffused-Junction Breakdown Voltage, V_{CBO}, and Junction Capacitance, C_C

For the calculated gradient, 4×10^{20} cm^{-4}, V_{CBO} from Figure 4 should be 60 volts. The lower observed median value of 55 volts can be attributed to the inadequacy of the linear-graded approximation for this shallow diffused junction and to nonuniformity in the crystal. From Figure 3, at 5 volts and with a gradient of 4×10^{20} cm^{-4}, C/A_C is 9×10^3 picofarads per square centimeter, and C_C is 2.9 picofarads. The median observed value (excluding case capacitance) is 3 picofarads.

Lifetime and Collector-Junction Saturation Current, I_{CBO}

If gold is diffused into the junction at 1000°C, Figure 5 indicates that $\tau = 9 \times 10^{-9}$ second and $I_{CBO}/(X_m A_C) = 0.2$ ampere per cubic

centimeter. If the collector junction reverse bias is 20 volts the value of X_m from Figure 3 is 2×10^{-4} cm and I_{CBO} is approximately 13×10^{-9} ampere. However, this value is too high; the median measured value of I_{CBO} for the 2N1708 is 5×10^{-9} ampere, which agrees with the measured lifetime estimated from the collector–base diode recovery time of 28×10^{-9} second. This higher lifetime, three times that calculated, may be attributed to annealing of the gold in processing operations subsequent to the gold diffusion.

Table III—Summary of Calculated and Observed Parameters for the 2N1708

Parameter	Calculated Values	Median Observed Values	Test Conditions*
V_{CBO}	60 volts	55 volts	$I_{CBO} = 10^{-6}$ amp
C_C	2.9 pf	3 pf	$V_{CB} = 5$ volts
$r_{b'}$	20 ohms	30 ohms	
I_{CBO}	5×10^{-9} amp	13×10^{-9} amp	$V_{CB} = 20$ volts
V_{BE}	0.75 volt	0.77 volt	$I_C = 10$ ma, $I_B = 1$ ma
V_{CE}(sat)	0.17 volt	0.17 volt	$I_C = 10$ ma, $I_B = 1$ ma
h_{FE}	20	30	$V_{CE} = 1$v, $I_C = 10$ ma
t_d	5.5×10^{-9} sec	7×10^{-9} sec	$V_{CC} = 3$v, $I_C = 10$ ma, $I_{B1} = 2$ ma
t_r	5×10^{-9} sec	8×10^{-9} sec	$I_C = 10$ ma, $I_{B1} = 3$ ma, $R_L = 220$ ohms
f_t	690 mc	330 mc	$V_{CC} = 5$v, $I_C = 10$ ma, measured at 100 mc
t_s	7×10^{-9} sec	15×10^{-9} sec	$I_C = I_{B1} = I_{B2} = 10$ ma, $V_{CC} = 10$v

* Conditions at which the transistor is normally specified.

Collector-to-Emitter Voltage, V_{CE}(sat)

$$V_{CE} \cong \phi_c - \phi_e + I_C R_{SC}.$$

From Figure 8, when $h_{FE} = 30$, $h_{FEI} = 0.2$, and $I_C/I_B = 10$, then $\phi_c - \phi_e \cong 0.11$ volt. From Figure 9, since $R_e/R_p = 0.2$ and $h/R_p = 0.02$, $R_{SC} = 6$ ohms. If $I_C = 10$ milliamperes, $V_{CE} \cong 0.11 + 0.06 = 0.17$ volt, which is the same as the observed value.

Conductivity modulation of the collector region becomes important in epitaxial and triple-diffused devices if the intrinsic region is smaller

than the diffusion length of minority carriers in the collector; the value of R_{SC} has to be changed accordingly. Because the lifetime in this device is very low, the diffusion length is generally smaller than the intrinsic region. At high current densities, however, the effective diffusion length is increased by the strong field, and conductivity modulation is significant.

Base-to-Emitter Voltage, V_{BE}

$$V_{BE} \cong \phi_e + I_B r_{b'}.$$

If $I_E = 10$ milliamperes, and $h_{FEI} = 0.2$, Figure 11 shows that $\phi_e = 0.71$ volt. From Figure 10, for the same geometry, $r_{b'} \cong 25$ ohms, which is lower than the measured value of 35 ohms. The higher value may be attributed to contact resistance and nonuniform emission. When $I_C/I_B = 10$, $I_C = 10$ milliamperes; the calculated V_{BE} is 0.74 volt which is lower than the observed median of 0.77 volt.

Common-Emitter Current Gain, h_{FE}

For the impurity concentrations used, the calculated electron lifetime in the base is 5×10^{-9} second. If it is assumed that emitter efficiency is unity, Figure 14 shows that h_{FE} should be approximately 20. The median observed value is 30. This value is consistent with a higher lifetime than the one estimated from the gold diffusion temperature.

Frequency at which h_{fe} ***is unity,*** f_t

f_t can be estimated from the sum of the delay times in the various regions of the transistor. The emitter delay time τ_e when I_E is 10 milliamperes and C_{TE} is approximately 12 picofarads, is

$$\tau_e = \frac{kT}{q}\frac{C_{TE}}{I_E} = 2.6 \times 10^{-11} \text{ second.}$$

The base transit time when the base width is 0.75×10^{-4} cm and D_n is 15 centimeters square per second (neglecting built-in fields) is

$$\tau_b = \frac{w^2}{2D_n} = 18.6 \times 10^{-11} \text{ second.}$$

The delay in the collector depletion region for a space-charge width of 10^{-4} cm and a limiting high-field electron velocity of 5×10^6 centimeters per second is

$$\tau_m = \frac{X_m}{10^7} = 1 \times 10^{-11} \text{ second.}$$

The collector delay time for a collector spreading resistance R_{sc} of 6 ohms and a collector junction capacitance C_c of 3 picofarads is

$$\tau_c = R_{sc} C_c \cong 1.8 \times 10^{-11} \text{ second.}$$

Therefore,

$$\tau_e + \tau_b + \tau_m + \tau_c = 24 \times 10^{-11} \text{ second}$$

and

$$f_t \cong 690 \text{ megacycles.}$$

This value is higher than the observed value of 330 megacycles.

Turn-On Delay Time, t_d

The transistor turn-on delay time is essentially the time required to charge the emitter and collector capacitances. If V_{CC} is 3 volts,

$$V_i = 0.7 \text{ volt}, V_{BE}(\text{off}) = 1 \text{ volt, and } I_{B1} = 2 \text{ milliamperes,}$$

$$Q_E = 3.68 \times 10^{-15} A_e a_e [(1.7)^{2/3} - (0.7)^{2/3}]$$

$$= 7.4 \times 10^{-12} \text{ coulomb}$$

$$Q_C = 3.68 \times 10^{-15} A_e a_e [(4.7)^{2/3} - (3.7)^{2/3}]$$

$$= 3.6 \times 10^{-12} \text{ coulomb.}$$

The delay time t_d is given approximately by

$$t_d \cong \frac{Q_E + Q_C}{I_{b1}} = 5.5 \times 10^{-9} \text{ second.}$$

This value is in reasonably good agreement with the observed value of 7×10^{-9} second.

Rise Time, t_r

See Equation (30) and Table II.

Collector Storage Time, t_s

The storage time is assumed to depend on the collector lifetime and circuit parameters. When I_C, I_{B1}, and I_{B2} are 10 milliamperes,

and h_{FE} is 30,

$$\operatorname{erf}\sqrt{\frac{t_s}{\tau}} = \frac{h_{FE}I_{B1} - I_C}{h_{FE}(I_{B1} + I_{B2})}$$

and, therefore,

$$t_s \cong 0.23\tau.$$

The calculated lifetime gives an extremely low value, about 2×10^{-9} second.

When the lifetime estimated from diode recovery time is used (28×10^{-9} second),

$$t_s = 7 \times 10^{-9} \text{ second.}$$

This value is lower than the median measured value of 15×10^{-9} second.

Conclusion

The parameters not dependent on lifetime can be predicted with reasonable accuracy. Lifetime is dependent upon methods of quenching the devices after the introduction of gold; as a result, it is more difficult to predict. If the lifetime estimated from gold solubility data is reduced by a factor of 3, the observed saturation current and storage time are in fair agreement with the estimated values.

Acknowledgments

The authors are grateful to A. Bosso and P. Kolk for making many of the measurements, and to J. Hilibrand for a number of helpful suggestions.

RCA TECHNICAL PAPERS†

Third Quarter, 1962

Any request for copies of papers listed herein should be addressed to the publication to which credited.

"Apparatus for Measuring the Temperature Dependence of Photo-Hall Effects in High-Resistivity Photoconductors," H. E. MacDonald and R. H. Bube, *Rev. Sci. Instr.* (July) 1962

"An Application of Inverse Probability to Fault Isolation," F. D. Brown, N. F. McAllister, and R. P. Perry, *Trans. I.R.E. PGME* (July) 1962

"Compact Nuvistor Product Detector," R. M. Mendelson, *Electronics World* (July) 1962

"Composite Characteristics of Negative Resistance Devices and Their Application in Digital Circuits," C. A. Renton and B. Rabinovici, *Proc. I.R.E.* (July) 1962

"Computations of Spherical Aberrations," H. Weinstein, (Letters to the Editor), *Jour. Opt. Soc. Amer.* (July) 1962

"Correlation Function at the Output of a Nonlinear Device," G. E. Roberts and H. Kaufman (Correspondence), *Trans. I.R.E. PGIT* (July) 1962

"Cross Modulation and Modulation Distortion of RF Transistors," G. E. Theriault, *Trans. I.R.E. PGBTR* (July) 1962

"Design Considerations for Using the RCA 2N828 in High Speed Logic Circuits," B. Zuk, *Solid-State Design* (July) 1962

"Effects of Elevated Temperatures on the Fluorescence and Optical Maser Action of Ruby," J. P. Wittke, *Jour. Appl. Phys.* (July) 1962

"Experimental Tunnel-Diode Electromechanical Transducer Elements and Their Use in Tunnel-Diode Microphones," E. S. Rogers, *Jour. Acous. Soc. Amer.* (July) 1962

"A Light Source Modulated at Microwave Frequencies," J. I. Pankove and J. E. Berkeyheiser, *Semiconductor Device Conf.*, Durham, N. H. (July) 1962

"A Nuvistorized Converter for 220 Mc," J. Filipczak, *QST* (July).. 1962

"Rectification and Space-Charge-Limited Currents in CdS Films," J. Dresner and F. V. Shallcross, *Solid State Electronics* (July-August) 1962

"Reliability Considerations in the Application of Power Transistors to Consumer Products," C. F. Wheatley and J. W. Englund, *Trans. I.R.E. PGBTR* (July) 1962

"Reflectivity Measurements on InSb-In_2Te_3 and InAs-In_2Te_3 Alloys and on Pure InSb, InAs and In_2Te_3," D. L. Greenaway, *Proc. Semiconductor Conf. International*, Exeter, England, July 11-12 1962

"The Conduction Cooling of Power Tubes in Vehicular Communication Equipment," J. W. Gaylord, *Electronic Equipment Engineering* (August) 1962

"Design Aspects of the Hot Stage for EMU-3 Series Electron Microscopes," A. J. Cardile and J. W. Coleman, *Scientific Instruments* (August) 1962

† Report all corrections to *RCA Review*, RCA Laboratories, Princeton, N. J.

"Design Considerations for Automobile AM/FM Receivers," R. A. Santilli and H. Thanos, *Semiconductor Products* (August) .. 1962

"Direct Observation of Longitudinal Modes in the Output of Optical Masers," R. C. Duncan, Jr., Z. J. Kiss, and J. P. Wittke, *Jour. Appl. Phys.* (August) 1962

"5-KW and 10-KW Transmitters for High-Fidelity AM Programming," N. E. Katz, *Broadcast News* (August) 1962

"High-Efficiency Gallium Arsenide Solar Cells," M. F. Lamorte, *Proc. Power-Sources Conf.* (August) 1962

"Increase in Dielectric Constant during Switching in Barium Titanate and Triglycine Sulfate," E. Fatuzzo, *Jour. Appl. Phys.* (August) 1962

"Injection Currents in Insulators," M. A. Lampert, *Proc. I.R.E.* (August) 1962

"Magnesium Primary Cells," G. Lozier and R. Ryan, *Proc. Power-Sources Conf.* (August) 1962

"Magneto-Ionic Duct Propagation Time (Whistler-Mode) vs. Geomagnetic Latitude at 4 KC," C. V. Greenman (Correspondence), *Proc. I.R.E.* (August) 1962

"Neutron Activation Analysis of Gallium Arsenide Contamination by Quartz," W. Kern, *Jour. Electrochem. Soc.* (August) 1962

"New Rechargeable Systems," E. F. Uhler and G. S. Lozier, *Proc. Power-Sources Conf.* (August) 1962

"Nonlinear Distortion in Tunnel-Diode Amplifiers," R. M. Kurzrok and A. Newton (Correspondence), *Proc. I.R.E.* (August).... 1962

"100 KW Shortwave Transmitter for International Broadcasting," W. S. Day and J. Q. Lawson, *Broadcast News* (August)..... 1962

"Preparing Carbon Film Nets," J. J. Byrd, *Scientific Instruments* (August) 1962

"RCA Introduces the New EMU-3G," F. J. Hermann, *Scientific Instruments* (August) 1962

"RCA Video Alignment Tape," *Broadcast News* (August) 1962

"Spectrographic Analysis of Gold Alloys Used in Semiconductor Devices," H. M. Hyman, *Applied Spectroscopy* (August) 1962

"A Technique for Equalizing Parabolic Group Delay," R. M. Kurzrok, (Correspondence), *Proc. I.R.E.* (August) 1962

"A Varidirectional Condenser Microphone," M. Rettinger, *Jour. S.M.P.T.E.* (August) 1962

"X-Ray Methods for Determination of Plate Thickness," E. P. Bertin and R. J. Longobucco, *Metal Finishing* (August) 1962

"Current Saturation in Piezoelectric Semiconductors," R. W. Smith, *Phys. Rev. Letters* (August 1) 1962

"Energy Levels of Divalent Thulium in CaF_2," Z. J. Kiss, *Phys. Rev.* (August 1) 1962

"Fundamental Reflectivity of GaAs at Low Temperature," D. L. Greenaway, *Phys. Rev. Letters* (August 1) 1962

"Alpha-Cutoff Test Set Checks VHF Transistors," J. Lempner, *Electronic Design* (August 2) 1962

"Precise Converter Takes Current Analog of Digital Voltage Pulses," N. Aron, *Electronics* (August 10) 1962

"Magnetic-Field Dependence of the Velocity of Sound in Metals," J. J. Quinn and S. Rodriguez, *Phys. Rev. Letters* (August 15) 1962

"Versatile Zener Diode Array Forms High-Speed Quantizer," J. J. Kolarcik, *Electronics* (August 17) 1962

"The Analysis of Major and Minor Constituents in Ceramic Materials by X-Ray Spectrometry," R. J. Longobucco, *Analytical Chemistry* (September) 1962

"Couplings in Direct-Coupled Waveguide Band-Pass Filters," R. M. Kurzrok (Correspondence), *Trans. I.R.E. PGMTT* (September) 1962

"Effects of Fading on Quadrature Reception of Orthogonal Signals," G. Lieberman, *RCA Review* (September) 1962

"Electronic Techniques in a System of Highway Vehicle Control," L. E. Flory, G. W. Gray, R. E. Morey, W. S. Pike, and C. O. Caulton, *RCA Review* (September) 1962

"Emission Spectrographic Method for the Determination of Microgram Quantities of Ba, Sr, Mg, Mn, Si, and Ni in Sublimed Deposits on Micas, Grids, Plates, and Glass Bulbs of Electron Tubes," A. M. Liebman, *Analytical Chemistry* (September).. 1962

"Heating of Waveguide Windows as a Limit to the Output Power of Microwave Tubes," F. Paschke, *RCA Review* (September).. 1962

"Heterodyne Receivers for RF-Modulated Light Beams," D. J. Blattner and F. Sterzer, *RCA Review* (September) 1962

"A Light Source Modulated at Microwave Frequencies," J. I. Pankove and J. E. Berkeyheiser (Correspondence), *Proc. I.R.E.* (September) 1962

"Limiting-Current Effects in Low-Noise Traveling-Wave-Tube Guns," A. L. Eichenbaum and J. M. Hammer, *RCA Review* (September) 1962

"Nonlinear Electrodynamics of Superconductors with a Very Small Coherence Distance," R. H. Parmenter, *RCA Review* (September) 1962

"An Organic Photoconductive System," H. G. Greig, *RCA Review* (September) 1962

"The Razor's Edge of Support System Management," J. W. V. Roy, *Trans. I.R.E. PGEM* (September) 1962

"Some Physical Aspects of Electron-Receiving-Tube Operation," M. Natapoff, *Amer. Jour. Phys.* (September) 1962

"Spectral-Line Interference in X-Ray Fluorescence Spectrometry," E. P. Bertin and R. J. Longobucco, *Norelco Reporter* (September) 1962

"Stability of Tunnel-Diode Oscillators," F. Sterzer, *RCA Review* (September) 1962

"Studies of the Ion Emitter Beta-Eucryptite," F. M. Johnson, *RCA Review* (September) 1962

"Accuracy Is Improved in Vidicon Bandwidth Tests," J. Pirkle, *Electronics* (September 14) 1962

"How to Design Micromodules," R. DiStefano, Jr., *Electronics* (September 14) 1962

"Dispersion Relations for Electron Scattering from Atomic Helium," E. Gerjuoy and Coauthor, *Phys. Rev.* (September 15) 1962

"Evidence for the Existence of High Concentrations of Lattice Defects in GaAs," J. Blanc, R. H. Bube, and L. R. Weisberg, *Phys. Rev. Letters* (September 15) 1962

"Ferroelectricity in SbSI," E. Fatuzzo, G. Harbeke, W. J. Merz, R. Nitsche, H. Roetschi, and W. Ruppel, *Phys. Rev.* (September 15) 1962

"Theoretical Considerations on the Switching Transient in Ferroelectrics," E. Fatuzzo, *Phys. Rev.* (September 15) 1962

"Chirp Signals for Communications," M. R. Winkler, *I.R.E. Wescon Convention Record, Part 7, Communications* 1962

"A Comparative Evaluation of Sequential Decoding Algorithms," D. M. Jones, W. R. Wadden, and J. J. Bussgang, *I.R.E. Wescon Convention Record, Part 4, Automatic Control; Electronic Computers; Information Theory* 1962

"Considerations on Communication with Intelligent Life in Outer Space," M. Handelsman, *I.R.E. Wescon Convention Record, Part 5, Aeronautical and Navigational Electronics; Military Electronics; Space Electronics and Telemetry* 1962

"The Cost of Radio Frequency Interference," F. L. Ankenbrandt, *I.R.E. International Convention Record, Part 5, Aerospace and Navigational Electronics; Military Electronics; Radio Frequency Interference; Space Electronics and Telemetry* 1962

"A Design Plan for an Integrated Satellite Tracking and Communications System," L. Farkas, *I.R.E. Wescon Convention Record, Part 5, Aeronautical and Navigational Electronics; Military Electronics; Space Electronics and Telemetry* 1962

"General Principles of Operations in Neuron Nets with Application to Acoustical Pattern Recognition," T. Martin, F. Putzrath, and Coauthor, *Proc. Second Annual Bionics Symposium, Biological Prototypes and Synthetic Systems*, Vol. 1 1962

"Interleaved Sound Transmission Within the Television Picture," J. L. Hathaway, *I.R.E. International Convention Record, Part 7, Audio; Broadcasting; Broadcast and Television Receivers* 1962

"Microwave Phase Measurement of Dispersed Pulse Transmitter Systems," R. F. Koontz, *I.R.E. Wescon Convention Record, Part 1, Antennas; Microwave Theory and Techniques* 1962

"A 120-Watt 50-Megacycle Transmitter," G. D. Hanchett, *Ham Tips* (Summer) 1962

"Performance of Digital Communications Systems in an Arbitrary Fading Rate and Jamming Environments," A. B. Glenn and G. Lieberman, *I.R.E. Wescon Convention Record, Part 5, Aeronautical and Navigational Electronics; Military Electronics; Space Electronics and Telemetry* 1962

"Placement of Technical Papers for Maximum Effectiveness," C. A. Meyer, *I.R.E. International Convention Record, Part 10, Education; Engineering Management; Engineering Writing and Speech* 1962

"Potential Application of Recent Advances in Communication Technology," E. W. Keller and Coauthor, *5th National Symposium on Global Communications* 1962

"The RCA Multi-Font Reading Machine," W. J. Hannan, *Proc. Symposium on Optical Character Recognition* (January 15-17) 1962

"A Simplified Work-Load Evaluation and Cost Control Method for Report Production," P. Alelyunas, *I.R.E. Wescon Convention Record, Part 8, Instrumentation; Engineering Management* 1962

"Some Special Sample-Mounting Devices for the X-Ray Fluorescence Spectrometer," E. P. Bertin and R. J. Longobucco, *Advances in X-Ray Analysis*, Vol. 5, p. 447, Plenum Press, New York, N. Y. 1962

"Transmission Programming for Energy Conservation in Space Communications," N. S. Potter, *I.R.E. International Convention Record, Part 8, Communications Systems; Vehicular Communications* 1962

AUTHORS

ADOLPH BLICHER studied Electrical Engineering at the University of Toulouse, France, where he received the B.S. degree in Electrical Engineering. He received the M.S. degree in Electrical Communications from the École Supérieure d'Electricité in Paris, France. In 1938, he received the Sc.D. degree in Physics from the Technical University of Warsaw, Poland. Dr. Blicher has been active in the semiconductor field in this country since 1954 and has been associated with the RCA Semiconductor and Materials Division since 1955. Prior to organizing the Special Products Development Department, he was the Manager of Computer Device Development working on a wide variety of silicon and germanium transistors and diodes. Dr. Blicher is a Senior Member of the Institute of Radio Engineers, a member of the Electrochemical Society, and a member of the New York Academy of Sciences.

JAMES J. GIBSON received the degree of Civilingenjor in electrical engineering from the Royal Institute of Technology, Stockholm, Sweden, in 1947, where he also did graduate work in 1950 to 1951. In 1946 he served with the Swedish Air Force working on UHF antennas and circuits. From 1947 to 1952 he was engaged in research on antennas, microwave circuits and pulse circuitry at the Research Institute of National Defence, Stockholm, Sweden. From 1952 to 1954, as an Honorary Fellow of the American Scandinavian Foundation, he was engaged in research on UHF antennas and transistor circuits at RCA Laboratories, Princeton, N. J. From 1954 to 1956 he was in charge of a group working on transistor circuits at the Royal Institute of Technology, Stockholm, Sweden. In 1956 he joined RCA Laboratories, Princeton, N. J., where he has been engaged in research in television, communication theory, and most recently, high-speed switching circuits. He is a member of the Institute of Radio Engineers.

RICHARD E. HONIG received the B.S. degree in Electrical Engineering from Robert College, Istanbul, Turkey, in 1938; the M.S. degree in 1939, and the Ph.D. degree in Physics in 1944, both from the Massachusetts Institute of Technology. In 1940-1941, he was instructor of Physics at Bluffton College, Ohio. He taught and did research work at M.I.T. as Research Assistant from 1941 to 1944, and as Research Associate from 1944 to 1946. He was at the Socony Vacuum Research Laboratories, Paulsboro, N. J., from 1946 to 1950, working mainly in the field of mass spectrometry. Since 1950, he has been at RCA Laboratories, Princeton, N. J., engaged in fundamental research in solid-state physics. In 1955/6, on a year's leave of absence from RCA Laboratories, he studied vaporization phenomena at the University of Brussels, Belgium. Dr. Honig is a member of Sigma Xi and the American Physical Society.

HENRY KRESSEL received the B.A. degree from Yeshiva College in 1955. He received the S.M. degree in Applied Physics from Harvard University in 1956, and the M.B.A. degree from the University of Pennsylvania, Wharton School in 1959. Mr. Kressel joined the RCA Semiconductor and Materials Division in 1959. He has been instrumental in the research and development of high-frequency mesa, planar, and planar epitaxial silicon transistors. Special contributions were in the area of diffusion techniques, metal contacting and material lifetime control. Mr. Kressel joined the Gallium Arsenide Product Development Department as Engineering Leader of the Microwave Diode group. He is responsible for research, development and pilot line engineering of GaAs and silicon microwave diodes. Mr. Kressel is the author of several papers on semiconductor devices. He is a member of the Institute of Radio Engineers and the Electrochemical Society.

ROLF B. LOCHINGER received the M.S. and Ph.D. degrees in Electrical Engineering from the Swiss Institute of Technology in 1956 and 1959, respectively. From 1956 to the early part of 1960, Dr. Lochinger was at the Swiss Federal Institute of Technology, Department of Advanced Electrical Engineering. During the academic year 1956-57, he was an assistant in the department and later was a co-worker of Professor Strutt. Dr. Lochinger conducted research in the fields of illumination and electroluminescent cell applications. He joined RCA Laboratories in 1960 and is presently engaged in research in high-speed switching circuits for digital computers. He is a member of the Institute of Radio Engineers.

HENRY S. MIILLER received the B.S. and M.S. degrees in Electrical Engineering from the University of Illinois and the University of Pennsylvania. In 1958, he joined RCA Laboratories, where he has been involved in work on ultra-high-speed computer circuits utilizing microwave phase-locked oscillators and tunnel diodes. His current interests relate to tunnel-diode–transistor hybrid digital circuits and systems. Mr. Miiller is a member of the Institute of Radio Engineers and Eta Kappa Nu.

THOMAS J. NELSON received the S.B. and S.M. degrees from MIT in the field of Electrical Engineering in 1957. He conducted his studies under the Electrical Engineering cooperative program. In 1957, Mr. Nelson joined RCA Laboratories. He has been engaged in research in the areas of high-speed memory systems, high-speed switching circuits, and wide-band amplifiers. He is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Xi.

ROBERT A. POWLUS received the B.S. degree in Electrical Engineering from the Pennsylvania State University in 1959. In June of 1959, he joined the technical staff at RCA Laboratories. He received the M.S. Degree in Electrical Engineering from Princeton University in 1961. Since joining RCA Laboratories, he has been engaged in research in semiconductor plasmas and digital computer circuitry. He is a member of the Institute of Radio Engineers, Eta Kappa Nu, and Tau Beta Pi.

R. SHAHBENDER received the B.E.E. degree from Cairo University, Cairo, Egypt, in 1946, the M.S. degree in Electrical Engineering from Washington University, St. Louis, Mo., in 1949, and the Ph.D. degree in Electrical Engineering from the University of Illinois in 1951. After completing his undergraduate studies, Dr. Shahbender joined the Anglo-Egyptian Oilfields, Ltd. for a period of two years and did work in geophysical oil exploration. In 1951 he joined the staff of the Minneapolis-Honeywell Regulator Co., Brown Instruments Division, and conducted research in the behavior of nonlinear control systems. In 1955, Dr. Shahbender joined RCA in Camden, N. J., and worked in the areas of adaptive systems, nonlinear filters, electron-beam devices, ultrasonic devices and airborne fire control systems. Dr. Shahbender transferred to RCA Laboratories, Princeton, N. J., in 1959 and has been active in the area of high-speed digital memory systems. He is presently head of the magnetic memory and devices research group in the Computer Research Laboratory. Dr. Shahbender is a member of the Institute of Radio Engineers, the American Institute of Electrical Engineers, the Franklin Institute, and the Societies of Sigma Xi, and Eta Kappa Nu.

HAROLD S. VELORIC (see *RCA REVIEW*, Vol. XXIII, No. 1, March 1962, p. 133.)

JOSEPH L. WALENTINE completed a four year evening course in machine design in 1939 at the School of Industrial Arts in Trenton, N. J., while serving his apprenticeship as a tool and die maker in the ceramic industry. During the war, Mr. Walentine worked at the experimental department of the Brewster Aircraft Co., Hatboro, Pa. He joined the RCA Research Center, Princeton, N. J., in 1945. In 1956, he joined International Telemeter Corp., Los Angeles, California. In 1959, he returned to RCA Laboratories as a Technical Staff Associate. Mr. Walentine has been active in developing ferrite fabrication and testing techniques. He is also partially responsible for the hermetically sealed enclosure used for RCA parametric and tunnel diodes. Mr. Walentine holds two U. S. patents.

RCA REVIEW

a technical journal

RADIO AND ELECTRONICS
RESEARCH • ENGINEERING

INDEX

VOLUME XXIII

TABLE OF CONTENTS