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INFO/CARD 2

Summer 1980



- Summer Cover "Tools of the trade". Some common and not so common RF components utilized by the RF designer in his daily work.
- System Intermod Performance Don't guess, risk or estimate the intermod performance of your system. Calculate it in five minutes.
- A 1-200 MHz Distributed Amplifier Using Power MOSFETs The use of medium power DMOSFETs (SD205) in a broadband configuration are described.
- Noise Bandwidth of Chebyshev Filters Theory, BASIC 19 language program and example of filter noise bandwidth determination are given.
- Simple Transmission Line Matching Circuits Seven methods of providing approximate and exact circuit matching solutions using transmission line(s).
- **Class E Switching-Mode RF Power Amplifiers** Low power dissipation, low sensitivity to component tolerances (including transistors), and well-defined operation.

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ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 Min.	11 Typ.	+38 Typ.	+24V	0.6A	199.00	(1-9)
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A Riddle

want to share a thought with you, you the engineer. When one introduces himself as an engineer, and this is your first meeting with the person, what thoughts do you immediately have? Do you say to yourself "I wonder where he's working?" "What's he doing?" "How much is he making?" "Where did he get his degrees and which ones does he have?" Those are some of the possibilities.

However, I'm almost willing to bet that your impression of him

and specifically his trade is more concrete. You know that he's probably worked his butt off acquiring his degree by means of a combination of four or more years of day and/or night school; he's entered a profession that most of his friends and probably family have frowned upon from a monetary point of view; and he's seen one, two or three roller-coaster "recessions" that appear to better describe the classical definition of a depression. You see this individual as a logical person capable of working from a whisper of an idea to a bodacious airborne rack of equipment circling the globe defining friend or foe. The RFQ(s), RFP(s), proposals, monthlies, interims, final reports these are all taken for granted. Of course your friend knows how

to clearly and succinctly document his work.

Take a closer look. This person is YOU. You've worked on projects that were for the public good and some not so good (but these we won't talk about). You've pushed back the frontiers in component technology and in some cases actually created them. You've designed instrumentation that should not perform at that high a frequency, but it does, and it does it faster, and more accurately, and you can fit it in a briefcase.

But you've been guilty of a crime. You've kept it to yourself. You haven't disseminated the information to others. Oh, I don't mean just your company documentation and advertisements. I mean articles in the leading well read journals (like *r.f. design*).

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System Intermod Performance

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W henever getting ready to set up the building blocks of a system, a block diagram is drawn, and the specification of each block is detailed. From the assigned specifications, the Noise Figure and Gain of the system can be precisely found. But even if the Third Order Intermodulation Performance of the building blocks are specified, estimating the overall Intermodulation Performance is risky. Several equations can be used, and these become lengthy, even with calculators. Here is a simple and accurate way of finding out exactly what the performance will be. Using the block diagram as a working model, the only two specifications necessary to work with is Output Intercept Point (OIP) and Gain.

Knowing the OIP of a Module, the *Input Intercept Point* can be found by subtracting the gain. Whenever the OIP of a module is determined by interfacing with another module, the IIP of that module is degradated by the same value. The Interface performance can never exceed the lowest performance value of either module, but is actually less than the lowest. The actual value can be determined from the chart.

Several steps are involved, but once the steps are recognized, it is a repetition of two steps, and a block diagram of the same type as Figure 1. It should not take the engineer more than a couple of minutes to evaluate the correct performance.

By taking the trouble of following the assigned steps, the greatest performance degrading module can be noted at a glance and steps taken to remedy it.

The Intermod Performance of two interfaced modules is always determined by the lower performance module. Therefore, starting at the last module locate + 40 dBm on the scale and draw a line to simulate its specified IIP, i.e. + 20 dBm.

With an IIP of A3 of +20 dBm, a lossy module preceding it, and intermod performance of the lossy circuit considered as not applicable, the Interface Performance is not degraded. Hence +20 dBm does not change and the IIP of BPF2 is +24 dBm.

i.e. + 20 dBm - (-4 dB) = + 24 dBm.

X2 OIP is given as +20 dBm, and it is operating into another block whose IIP is +24 dBm. Using the $\triangle P$ equation of P2-P1 = $\triangle P$, we find +24 - 20 = +4 dB, where P2

	Table 1. Specifications	
Module	Gain (dB)	OIP (dBm)
Pre-Selector	- 2	NA
A1	20	+ 20
X1	- 8	+ 20
BPF1	- 1	NA
A2	10	+ 30
X2	- 8	+ 20
BPF2	- 4	NA
A3	20	+ 40
-		

is the IIP of A2, and P1 is the OIP of A1, (where A1 and A2 are two simple building blocks, see Figure 3). Using + 4 dB as $\triangle P$, find α from the graph. $\alpha = 1.45$ dB. This therefore is the degradation imparted to the OIP of X2. Go to Figure 2 and at the interface junction, locate OIP ACTUAL, of X2, i.e. $20 - \alpha = 18.55$ dBm.

Since X2 is a lossy module (-8 dB), X2 IIP is +26.55 dBm.

A2 OIP is + 30 dBm and operating into a + 26.55 dBm



Don't guess, risk, or estimate the intermod performance of your system. Calculate it in five minutes.



IIP block. Therefore $\triangle P = 26.55 - 30 = -3.45$ dB, and a = 5 dB. The OIP of A2 is degraded by 5 dB, i.e. it now has an actual value of 30 - 5 = +25 dBm. A2 IIP is now 25 - 10 = +15 dBm. Again the BPF1 loss actually enhances the IIP of A2 by 1 dB, and IIP of BPF1 is now + 16 dBm.

X1 OIP is + 20 dBm and operates into a + 16 dBm IIP block. Therefore $\triangle P = 16 - 20 = -4$ dB, and $\alpha = 5.5$ dB. The OIP of X1 is degraded by 5.5 dB, i.e. it now has an actual value of 20 - 5.5 = 14.5 dBm. Its IIP is 14.5 - (-8) = 22.5 dBm.

A1 OIP is +20 dBm and operates into a +22.5 dBm block. Therefore $\triangle P = 22.5 - 20 = 2.5$ dB and $\alpha = 1.9$ dB. The OIP of A1 is degraded by 1.9 dB, i.e. it now has an actual value of +20 - 1.9 = 18.1 dBm. Its IIP is 18.1 - 20 = -1.9 dBm. With the Pre-Selector preceding it, the IIP at the antenna is -1.9 + 2 = 0.1 dBm.

The final value of + 0.1 dBm, at the antenna J1 represents an IIP of 0.1 dBm and an OIP of + 27.1 dBm at J2.

Several ways of improving the Intermod Performance of this circuit can be considered:

a. Reduce A1 gain.

b. Raise IIP of X1 by preceding it with a pad. Both of the above will affect NF. Best choice would be to raise the OIP of A1, but not easily accomplished without affecting A1 NF.

c. BPF1 can have more loss, thus raising its IIP while degradation of X1 OIP would not reduce it to 14.5 dBm. If BPF1 had 6 dB loss, then its IIP would be + 21 dBm, and interfaced with X1, $\Delta P = 1$ dB and $\alpha = 2.5$ dB, would degrade the OIP of X1 to 20 - 2.5 = 17.5 dBm. Its IIP would then be + 25.5 dBm. The reduction factor α , for A1 would be only 1.05 dB and the OIP of A1 would then be 18.95 dBm, and the IIP of A1 would be - 1.05 dBm. J1 IIP would be + 0.95 dBm.

Advantage of this analysis is accuracy with speed, without any great mathematical computation to go through. Once the scaled graph is plotted a quick glance can determine the most critical point of the system.

A note of caution concerning filters. Some form of distortion takes place in filters at higher levels than designed levels, and the not applicable note should be construed as final. The purpose of this graph is to reduce the hours it takes to analyze a system down to a maximum of five minutes, once the steps are understood.

A 1-200 MHz Distributed Amplifier Using Power MOSFETs

The use of medium power DMOSFETs (SD205) in a broadband configuration are described. A brief discussion of the desirable features of DMOSFETs is given in the appendix.

Ed Fong Consultant

Introduction

The requirements of broad bandwidth, high gains, higher powers, low distortion and low cost in amplifiers can be approached in several ways. One of these is the distributed amplifier. Traditional configurations usually suffer from the following disadvantages:

1. The broader the bandwidth, the lower the gain and vice versa.

2. The maximum usable frequency (f_T) is given by $f_T = gm/2\pi C_{in}$. Where C_{in} is the input capacitance and gm is the transconductance.

3. Achieving high power at high frequencies is always a problem since the device must be physically large. This causes the input capacitance to increase and thus lowers f_T . A highly desirable device is one with large gm and small C_{in} . Exotic devices such as GASFETS and MESFETS achieve this at considerable expense. In addition, commercially available GASFET devices offer only several watts at 1 GHz. The cost of these components at the time of this writing is in the hundreds of dollars.

The amplifier described in this paper uses inexpensive DMOSFETS^{1,2} and overall, no exotic components. At low signal levels (10mW), it offers + 13.5 dB \pm 0.5 dB gain with a bandwidth of 200 MHz. It has a saturated output of 4.5 watts. The noise figure at 150 MHz is 5 dB and thus one can conceive of using this in a broadband front-end. As a power amplifier driver its second order harmonic distortion is – 26 dB at a 1 watt output level and wasn't measurable when the *input* level was 0 dBm. This is due to the fact that MOSFETS are square-law devices. The amplifier is in a distributed configuration used extensively by Ginzton³. This scheme was first conceptualized by Percival⁴ in 1935. With the aid of modern devices, higher gains and powers are achieved.

Design Considerations In A Distributed Amplifier

It is well known that the f_T of a device is given by $gm/2\pi C_{in}$. If more power is desired, the area of the die must be increased. This also increases the input capacitance, Cin. Thus the gain-bandwidth is kept constant. For example, if the size is doubled so will the input capacitance. If gm remains the same, the cutoff frequency at the input is halved. Even though the transconductance may increase due to a large device it will not increase proportionally at high frequencies with Cin. If one desires high gains with high power, it does not seem feasible with traditional approaches. By paralleling, the power dissipation can improve, but the gain is still constant since gm and Cin are increasing approximately at the same rate. The technique of the distributed amplifier circumvents this problem. Gain and power is additive and yet capacitance is not. Cascading in the traditional approach will improve gain, but not power since the power is limited by the output device. The first commercially available distributed amplifiers used tubes. It was manufactured by Hewlett-Packard⁵. Several companies have since produced similar amplifiers6-7.

The distributed amplifier uses the principles of an ideal transmission line. For example, the coaxial transmission line shown in Figure 1a can be modeled as a combination of L's and C's as shown in Figure 1b.

The characteristic impedance of such a line is given by (1)

$$Z_o = \sqrt{L/C} \tag{1}$$

where L and C are the equivalent distributed inductance and capacitance in the line. The transmission line has a limited frequency response as demonstrated by a single unit length of coax. (See Figure 2.) The transfer function is given by

$$V_o = \frac{V_{in}}{1 + S^2 LC} \tag{2}$$





The pole is thus given by

$$\omega_{3dB(rad/sec)} = \frac{1}{\sqrt{L/C}}$$
(3)

If we divide the above by radians and take the reciprocal, we obtain the time delay of the transmission line per unit length.

or
$$t_{delay} = \sqrt{LC}$$
 (seconds per unit length) (4)

or
$$V = 1/t = 1/\sqrt{LC}$$
 (5)

It is well known that

$$t = \frac{d\Phi}{d\omega} \tag{6}$$

where Φ is the phase shift per unit length. By performing the above integral it is not difficult to see that

$$\Phi = \omega \sqrt{LC} (radians per unit length)$$
(7)

From (3), the cutoff frequency was given by $1/\sqrt{L C}$. This is the point where the magnitude is -3 dB and excess phase shift occurs in the line. (1) is no longer valid at this frequency. For a detailed understanding, the model in Figure 1b is not entirely correct. This is because the first capacitor would be in parallel with a second capacitor of the same size if a coax cable were connected to it. The capacitor will add and upset the characteristic line impedance. This is because the shunt C's must be evenly distributed throughout the line. An improved model is given below in Figure 3.



In Figure 3 the first inductor is not L but L/2 since it is discontinuous. The remaining L/2 comes from the transmission line. This lump element model can thus interface with other transmission lines directly without affecting the match. An ideal resistor can be modeled as an ideal transmission line. Figure 3 can be redrawn as shown in Figure 4.

Figure 4 is suitable for an amplifier configuration. It was mentioned previously that input capacitance of a semiconductor device limits the maximum frequency of the device. If the device size is doubled, so is the input capacitance. Thus the gain does not increase for a given frequency. Figure 4 shows a distributed capacitance of value C. This can be the input capacitance of an MOS

r.f. design



device. The drain line can be designed in a similar fashion with the output capacitance as the distributed capacitance. Notice that a bipolar transistor is not ideal for a distributed amplifier configuration because of the base spreading resistance r_b . This will equivalently shunt the distributed C's and introduce losses. A simplified schematic for a MOS distributed amplifier is shown in Figure 5.



The distributed capacitance at the input is the gate to source capacitance of the MOSFET and the distributed capacitance at the output is the drain to source capacitance. The gain from gate to drain per device is given by $gm \cdot Z_o$. However, only half the gain appears at the output because a terminating resistor must be inserted to keep the impedance constant looking from both directions. The terminating transmission line can be replaced by a 50 ohm resistor thus acts as an infinite 50 ohm transmission line.

The operation of the transmission line amplifier can be explained as follows: as the input signal is applied, it travels down the transmission line with the distributed capacitance formed by the input capacitance of each device. The drain voltage gives an amplified version of this signal. From the drain it travels in both directions (left and right). Consequently half the signal is lost in the pseudo load. However, the other half travels down the line to the desired load. After the first inductor, the signal will suffer a phase shift. The amplified signal at the drain of M1 will combine with the signal at the drain of M2. However, to assure that the signal does sum at the drain of M2, the signals must be in phase. This puts another constraint on the system. The phase delay (or equivalently, time delay) from the gate of M1 to M2 must have the same delay as from the drain of M1 to M2. Otherwise the signals will be slightly out of phase preventing an ideal summation. According to (7) we must have:

$$\sqrt{L_1 C_1} = \sqrt{L_2 C_2} \tag{8}$$

The following conditions must also hold if the system is 50 ohms and no matching transformers are used.

$$Z_o = \sqrt{L_1/C_2} = \sqrt{L_2/C_2} = 50 \text{ ohms}$$
 (9)

For optimum summation this says that $L_1 = L_2$ and $C_1 = C_2$. Thus the *drain* capacitance must equal the *gate capacitance*. This can be done by adding capacitance to either the gate or drain depending upon which is smaller. The gain of the system can be summarized as follows:

$$V_{out}/V_{in} = \sum_{k=1}^{n} \frac{Z_o}{2} gm_k$$
 (10)

or simplifying,

$$A_{v} = n \frac{Z_{o}}{2} gm \tag{11}$$

where n is the number of sections.

In a first-order analysis the power gain is strictly an additive function. However due to non-ideal conditions this will not occur. Also, as the input frequency is increased, the gate of the MOS devices is no longer a pure capacitance. It begins to see an inductor and a shunt resistance. For accurate modeling this must be concluded in the calculations. The series inductance may be incorporated as part of L but the shunt R, which may be as low as 100 ohms at high frequencies must be modeled as a lossy element. This will change the characteristic impedance of the line.

Response Characteristic of the Line

The transmission line described in the previous section is called a constant-K artificial line. It has certain characteristics which are not obvious. It is seen by Figure 3 that the transmission line is actually a lowpass filter. The characteristic impedance was given by VUC. This is valid for low frequencies. The exact characteristic impedance is given by³

$$Z_{o} = \frac{\sqrt{Z_{1}Z_{2}}}{\sqrt{1 + \frac{Z_{1}}{4Z_{2}}}}$$
(12)

where
$$Z_1 = j\omega L_1$$
 (13a)

$$Z_2 = \frac{1}{i\omega C_1}$$

where fois given by

$$f_o = \frac{1}{2\pi \sqrt{LC}} \tag{15}$$

(14)

(14) shows that the impedance approaches infinity when the input frequency approaches the cutoff frequency. Thus the transmission line is no longer ideal. This causes a peaking at the terminating end of the line. This is because the transmission line's impedance is a function of frequency while the load impedance is constant with frequency. By substituting in (11) the gain should peak at the upper end. This becomes

$$Av(f) = \left(\frac{ngmR_o}{2}\right) \sqrt{\frac{1}{1 - \left(\frac{f}{f_{max}}\right)^2}}$$
(16)





because

14

Substituting (13a) and (13b) into (12), gives

It is evident that oscillations will occur at the upper end, but with careful loading, it can be minimized. Network synthesis program SPICE[®] was used to optimize this design. To improve the gain flatness, M-derived filter sections could be used. But a gain fluctuation of ± 0.5 dB, obtained with this amplifier, is more than adequate for most applications.

A Distributed Amplifier Using Power MOSFETS

An amplifier using the above principles was constructed using DMOSFETS (Signetics SD205). The input capacitance on these devices is 11.0 pFd and the output capacitance 6.0 pFd. Thus in order to have the proper phase velocity, 5.0 pFd must be added to the drain. The inductance was calculated to be 3.75 nH. A 50 ohm pseudo load was found to be inadequate in that peaking and at times oscillations occurred. This is shown by (16).

Program SPICE was again used to determine the optimum resistor. A 30 ohm resistor resulted in a gain of $\pm 13.0 \pm 0.5$ dB and with a - 3 dB point at 200 MHz. Yet the VSWR never exceeded 1.4:1. With a 50 ohm resistor, gain and frequency response improved (16.0 ± 2.0 dB up to 280 MHz) but gain linearity was poor. The inductors chosen were found to be optimized when compared to computer results.

The saturated output with TO-5 fin heat sinks was 4.5 watts. This value can be increased if more elaborate heat sink techniques are utilized. However, this is physically difficult with the TO-5 package. Because of the broad bandwidth, the amplifier performs well as a power pulse amplifier. With a + 13.0 dB gain and a 1.0 V P-P output, it has a 1.73 nanosecond rise time.

The amplifier has an advantage that it can be overdriven without suffering a charge storage time as associated with the base in bipolar transistors. This is ideal for applications where the recovery time is of primary concern. This occurs MOSFETS are majority carrier devices. The time delay is calculated by the following relationship

$$\tau_{Delay} = \sqrt{(\tau_{Total})^2 - (\tau_{Input})^2}$$
(17)

The data for the risetime was taken from Figure 8.





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A schematic diagram and parts layout is shown in Figure 6 and 9 respectively. Notice that the DMOSFETs are mounted on the bottom side of the printed circuit board to provide ease of heat sinking as shown in Figure 9.

Conclusion

A guide for the design of distributed amplifiers has been presented. Although this technique is not new, its principles can be applied to state-of-the-art devices where broad bandwidths can be achieved. A design example was **Figure 10.** Photo of the amplifier showing the transistor mounted on the side opposite the components.

given for a medium power amplifier using inexpensive DMOSFETs. With the aid of Computer Aided Design (CAD), the amplifier has a -3 dB bandwidth of 200 MHz with 13.0 \pm 0.5 dB of gain. It has a saturated output of 4.5 watts.

Acknowledgements

I would like to thank Vickie Saunders for her art work and Richard Zeman for his encouragement.



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Noise Bandwidth of Chebyshev Filters

Theory, basic language program and example of filter noise bandwidth determination.

Jack Porter, Cubic Corp., San Diego, Calif.

R eceiver sensitivity calculations often require values for the noise bandwidths of the filters used in the receiver. Although noise bandwidth is often approximated by the half-power (-3 dB) bandwidth, for some types of filters the noise bandwidth is significantly greater or less.

The one-sided noise bandwidth of a low-pass filter with transfer function $H(j\omega)$ is usually defined as

$$B_n = \frac{\int_0^\infty |H(j\omega)|^2 df}{|H(j\omega_r)|^2}$$

where $|H(j\omega_r)|$ is the magnitude of the transmission at DC.' If white noise is applied to such a filter the noise power at the output is the same as that which would appear at the output of a rectangular (brick-wall) filter with transmission $|H(j\omega_r)|$ and bandwidth B_n.

Although the noise bandwidth is defined for a low-pass filter, it has been shown that the ratio of noise bandwidth to filter bandwidth is invariant when the low-pass to bandpass transformation is made². Thus results obtained for low-pass filters also apply to bandpass filters of the same type.

Various methods of integration have been used to evaluate noise bandwidth. The simplest is the method used by Ku³. He showed that the noise bandwidth of any all-pole filter is simply $\pi c/2$, where c is the shunt capacitance adjacent to the open-circuited end of a singleterminated low-pass prototype filter of that type.

These capacitance values can be obtained from tables, such as those in Zverev's handbook⁴, but this isn't necessary for Chebyshev and Butterworth filters. A paper by Orchard⁵ gives explicit formulas for the capacitor values for these filters. When they are substituted for c in the above relation by Ku, the formulas in Figure 1 result. Since the Chebyshev prototype element values calculated from Orchard's formulas are for a ripple bandwidth of 1 radian/sec, the value of B_n calculated from

Noise Bandwidth "Calcs" Program Steps
Figure 2.
100 PRINT "CHEBYSHEV FILTER NOISE BANDWIDTH"
110 $C1 = LOG (10)/20$
120 PRINT
130 PRINT "N, AM (DB)";
140 INPUT NT, AU
150 IF NICTIMEN 390
100 IF AU20 THEN 210
200 GO TO 120
210 A1 = EXP(C1*A0)
$220 \text{ A2} = \text{A1}^{*}\text{A1}$
230 B0 = LOG $(1 + 2/(A1 - 1))$
240 $X1 = EXP(B0/(2 \cdot N1))$
250 B1 = B1 $(X_1 + 1/X_1)/2$
260 A3 = 2
270 IF N1>2*INT (N1/2) THEN 310
280 B1 = B1*A1
290 A3 = A3*A2
300 GO TO 320
310 B1 = B1/A1
320 X1 = SQR ((A3 - 1)/(A2 - 1))
$330 X2 = LOG (X1 + SQR (X1^*X1 - 1))$
340 X1 = EXP(X2/N1)
350 W1 = (X1 + 1/X1)/2
360 B2 = B1/W1
370 PHINT BN = ", B1, "BNH = ", B2
300 GUTUTZU
390 END

$$A_{V} = 10^{(A_{m}/20)}$$

$$\beta = 2 \tan h^{-1} \left(\frac{1}{A_{V}}\right) = \ln \left(1 + \frac{2}{A_{V} - 1}\right)$$

$$A_{H} = 2 \text{ For N Odd}$$

$$A_{H} =$$

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The same formula is often used in the literature for calculating the half-power bandwidth of both odd and even order Chebyshev filters. The value of $\omega_{\rm H}$ calculated from this is the frequency at which the response is 3 dB down from that at the ripple peaks. It seems more correct to define the half-power bandwidth as the frequency at which the response is down 3 dB from that at DC for low-pass filters or center frequency for bandpass filters. This definition results in a different formula for even-order filters.

Figure 3.	
Chebyshev Filter Noise E	Bandwidth
N, AM (DB)? 3, .1 BN = 1.44178	BNH = 1.038
N, AM (DB)? 4, .1 BN = 1.26134	BNH = 1.03637
N, AM(DB)? 11, .1 BN = 1.0193	BNH = .992162
N, AM(DB)? 12, .1 BN = 1.03799	BNH = 1.01427
N, AM(DB)? 3, .5 BN = 1,16659	BNH = .999231
N, AM(DB)? 45 BN = 1,19565	BNH = 1.08074
N, AM(DB)? 4, 1 BN = 1,22553	BNH = 1,14086
N, AM(DB)? 5. 1 BN = .943285	BNH = .912431
N. AM(DB)? 5, 2 BN = .826565	BNH = .816972
N, AM(DB)? 6, 2 BN = 1.29422	BNH = 1.26562
N, AM(DB)? 11. 2 BN = .8009	BNH = .798965
N, AM(DB)? 12, 2 BN = 1.26767	BNH = 1.26057
N. AM(DB)? 5, 0 BNH = 1.01664	
N, AM(DB)?0.0	

Figure 3 shows the values of B_n and B_{nH} calculated by the program for several values of N and A_m .

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10DB

20DB

30DB

40DB

50DB

60DB

70DB

80DB

RF Power Field-Effect Transistors **Short Form**

July 1980

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B

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150 200 250 300 350

50 100

B Siliconix

12.5 Volt DC-300 MHz Series

Part Number	Test* Freq (MHz)	Typical Power Out (Watts) @ 12.5 VDC	Typicai Gain (dB) 12.5 V, 175 MHz	Suggested Max Supply Voltage (VDC)	Min BV _{D\$\$}	θ]c (°C/W)	Comments
DV1202S	175	2.5	10	24	50	17.6	
DV1202W	175	2.5	10	24	50	14.1	
DV1205S	175	5	10	24	50	8.8	
DV1205W	175	5	10	24	50	7.0	
DV1210S	175	10	10	24	50	4.4	
DV1210W	175	10	10	24	50	3.5	
DV1220S	175	20	10	24	50	2.2	
DV1220W	175	20	10	24	50	1.8	
DV1230T	175	30	10	24	50	1.5	
DV1230W	175	30	10	24	50	1.2	
DV1240T	175	40	10	24	50	1.1	
DV1240W	175	40	10	24	50	.9	
DV1210Y	175	10	20	24	50	TBD	Two stage hybrid
DV1220Y	175	20	20	24	50	TBD	Two stage hybrid
DV1230Y	175	30	20	24	50	TBD	Two stage hybrid

* All parts tested at 20:1 VSWR

Note: See application notes AN80-4, AN80-6

Power Out vs Frequency



Ordering Information



- T= 500J0FX= C-220 Push-PullU= 500SOEFY= C-220 Hybrid
- V = Push-Pull Z = 280SOE

Package Types



Package Type S 380SOEF



Package Type T 500JOF

28 Volt Push-Pull DC-300 MHz Series

Part Number	Test* Freq (MHz)	Typical Power Out (Watts) @ 28 VDC	Typical Gain (dB) 28 V, 175 MHz	Suggested Max Supply Voltage (VDC)	Min BV _{DSS}	θ]c (°C/W)	Comments
DV2810V	175	10	10	35	80	8.8	
DV2810X	175	10	10	35	80	7.0	
DV2820V	175	20	10	35	80	4.4	
DV2820X	175	20	10	35	80	3.5	
DV2840V	175	40	10	35	80	2.2	Was DV1110
DV2840X	175	40	10	35	80	1.8	
DV2880V	175	80	10	35	80	1.1	Was DV1111
DV2880X	175	80	10	35	80	.9	
DV28120V	175	120	10	35	80	.73	Was DV1112
DV28120X	175	120	10	35	80	.6	

*All parts tested at 20:1 VSWR

Note: See application notes AN80-4, AN80-6

Power Out vs Frequency









Package Type X Push-Pull

Package Type Y Hybrid



Package Type Z 280<mark>SOE</mark>

Linear Performance Review of Selected RF Power FETs

Two-tone, 3rd-order intermodulation tests have been conducted on 4 typical Siliconix RF Power FETs, the DV2820S, DV2840S, DV2880T and DV28120T. The following graphs provide the Two-Tone Intercept Point (tones separated by 30 KHz).



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28 Volt DC-300 MHz Series

Part Number	Test* Freq (MHz)	Typical Power Out (Watts) @ 28 VDC	Typicai Gain (dB) 28 V, 175 MHz	Suggested Max Supply Voltage (VDC)	Min BV _{DSS}	θ]c (°C/W)	Comments		
DV2805S	175	5	10	35	80	17.6			
DV2805W	175	5	10	35	80	14.1			
DV2810S	175	10	10	35	80	8.8			
DV2810W	175	10	10	35	80	7.0			
DV2820S	175	20	10	35	80	4.4			
DV2820W	175	5 20 10 35		35	80	3.5	1000		
DV2840S	175	40	10	35	80	2.2			
DV2840W	175	40	10	35	80	1.8	was DV1007		
DV2880T	175	80	10	35	80	1.1			
DV2880U	175	80	10	35	80	1.1	Was DV1008 (Note)		
DV2880W	175	80	10	35	80	0.9			
DV28120T	175	120	10	35	80	.73	Was DV1009		
DV28120U	175	120	10	35	80	.73	Was DV1010		
VMP4	200	10	10	30	60	5.0	· · · · ·		

*All parts tested at 20:1 VSWR

Note: See application notes AN80-4, AN80-6

Power Out vs Frequency



Ordering Information







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Simple Transmission Line Matching Circuits

Seven methods of providing approximate and exact circuit matching solutions using transmission lines.

Andrzej Przedpelski A.R.F. Products, Inc. Boulder, Colorado

For some reason there seems to be an aura or mystery about transmission line matching circuits. With the exception of the widely used quarter-wave transformer to match real impedances', the usual approach is to design the circuit on paper using lumped elements and then transform it to an equivalent distributed configuration. Probably, this is a result of most of us being weaned on lumped circuits and regarding transmission lines as a necessary evil. Converting lumped capacitors and inductors to distributed equivalents, however, is not an accurate method in most cases. It is just as easy to obtain the exact desired results by attacking the problem in the distributed form from the beginning.

The following discussion will show both approaches and methods for obtaining exact results, as well as the more common approximate solutions.

To facilitate the discussion, a simple matching problem will be analyzed. Figure 1 shows the requirement for matching a complex impedance 5-j28 to a real impedance of 50 ohms. Only the simplest circuits will be considered.

Method 1: Substitution Of Equivalent Distributed Circuit

The lumped element matching circuits have first to be



determined. Figure 2 shows the four possible twopole matching configurations². These then have to be converted to the distributed equivalents. Litty³ describes the most common method of using a high impedance line as a series inductance and a low impedance as a shunt capacitance. Figure 3 shows the design formulas. It can be seen that only circuit a of Figure 2 can be thus con-





verted. The others have parallel inductances and/or series capacitors, which cannot be converted by this method. Since the impedance to be matched is 50 ohms, a higher line impedance was chosen for the inductance and a lower one for the capacitance. The actual choice is left up to the designer. The two cases shown are for a narrow and wide spread of line impedances, respectively. Using the chosen values of Z_1 and Z_2 , and the calculated values of Θ_1 and Θ_2 we can transform the original impedance of 5-j28 to a new impedance by using:

$$\frac{Z_{in}}{Z_T} = \frac{\frac{Z_{out}}{Z_T} + j \tan \Theta_T}{1 + j \frac{Z_{out}}{Z_T} \tan \Theta_T}$$
(1)

twice 4, 5.

To determine how good a match is obtained, the reflection coefficient $|\Gamma|$ can be calculated using:

$$|\Gamma| = \frac{Z_{in} - Z_o}{Z_{in} + Z_o} \tag{2}$$

and, if desired, the VSWR can also be obtained:

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|}$$
(3)

The calculations of Figure 3 show that, for reasonable values of Z_1 and Z_2 (100 and 10 ohms respectively), a reflection coefficient of 0.204 and a VSWR of 1.51:1 can be obtained. To improve these figures unreasonable impedance values have to be used. In this example, Z_1 and Z_2 of 1000 and 1 ohm, respectively, will result in a reflection coefficient of 0.007 and a VSWR of 1.014:1.

Method 2: Another Distributed Circuit Substitution

Matthaei⁶ shows another substitution method, shown in Figure 4. Again, using equations 1, 2 and 3 the resultant reflection coefficient and VSWR can be calculated. The respective values are very similar and are shown in Figure 4 for the same line impedance values used in the Method 1 example. To obtain a low reflection coefficient and VSWR, unreasonable line impedance values have to be used.





Method 3: Quarter-wave Transformer Plus a Reactance

In this approach the reactance is first "tuned out" and then the resulting resistance is transformed by means of a quarter-wave transformer, as shown in Figure 5.

In the example shown, an inductance is needed to cancel the capacitive reactance. The method 1 approach can be used to determine the length of the required line for a given line impedance and the length of the quarter-wave transformer can be calculated by using the well known relationship:

$$Z_2 = \sqrt{Z_1 \times 50} \tag{4}$$

The results (reflection coefficient of 0.038 and VSWR of 1.08:1) are considerably better than those obtained using Methods 1 or 2. This solution is suitable when X_a is capacitive.



2

Method 4: Single Transmission Line — Exact Solution

This is the simplest method, shown in Figure 6⁵. Unfortunately it does not give a solution in all cases. When it does, however, the match is exact.

Method 5: Exact Two Line Solution

This is an extension of Method 4. It is obvious that if a solution cannot be obtained with a single transformation, two lines can be used, the first one transforming to some intermediate impedance and the second, using Method 4, to the final desired impedance. (See Figure 9.) Many versions of this approach are possible. The simplest, using a programmable calculator, is the trial-and-error method, where convenient values of Z_1 and Θ_1 are selected and then Z_2 and Θ_2 are calculated (using Method 4). If no solution exists or if the values are not convenient, another set of Z_1 and Θ_1 are chosen and the process is repeated until desired results are obtained. The entire procedure, using a programmable calculator is quite simple and fast. The obtained match is exact, since no approximations are made and the exact transformation equation (1) is used.

A suitable program for an HP-19C (29C) calculator is given in Table I. Using this program some typical matching solutions to the problems of Figure 1 are shown in Figure 9. Z_1 and Θ_1 are chosen to be the same as in Method 1 and 3 examples to show the magnitude of the error introduced by these approximations,

Method 6: Quarterwave Transformer Plus Line — Exact Solution

Two transmission lines are used: one in parallel with the complex impedance and the other, 90° long, in series, as shown in Figure 7. The shunt line tunes out the reactance of the complex impedance and the series line, being a quarter-wave transformer, matches the remaining resistance to 50 ohms. Two possible configurations exist: shunt line shorted or open.' The reactance of the shorted line is:



Figure 7. Exact Solutions Using Quarter Transformer Plus Line. (5)

And of the open line:

$$Z_{(Open Stub)} = \frac{Z_1}{j \tan \Theta_1}$$
(6)

The calculator program of Table II performs all the necessary calculations:

• The series complex impedance is converted to parallel form,

 \bullet Θ_1 is determined using (5) or (6) necessary to tune out the reactance,

Z₂ is determined using (4).

The program is suitable for both the shorted and open configuration, depending upon whether a 1 or a 2 is stored in register 0.



	Tat	ole IA			
Step	Instructions	Input Data/Units	Ke	ys	Output Data/Units
1	Enter Program				F. 73
2	Store Source and Load Impedances	50 Ra Xa	STO STO STO	1 6 7	
3	Select and Store First Transmission Line Impedance and Electrical Length	Ζ ₁ Θ ₁	STO STO	8 9	
4	Calculate Second Transmission Line Impedance and Electrical Length	on	(g) 0	LBL	Ζ ₂ Θ ₂
5	Repeat Steps 3 and 4 For Other Z_1 , and Θ_1 values, If Desired				N. C. S.
	Note: Use Θ_1 , Electrical Lengt In Degrees or Radians (Which Your Calculator is Set to); Θ_2 Will Be in the Same Units	h, ever			



Method 7: Another Exact Solution Using A Quarter-wave Transformer Plus Line

This is Method 6 with the two lines reversed, as shown in Figure 8. The procedure is somewhat more complicated. The quarter-wave transformer impedance is chosen so that the $R_a + jX_a$ is transformed into 50 + jX. The shunt line then "tunes out" the jx leaving 50 ohms, therefore providing a "perfect" match. Again, the shunt reactance is calculated using (5) or (6) and the transformation using (4).

The calculator program of Table III performs all the necessary calculations and obtains Θ_1 and Z_2 for any chosen value of Z_1 .

		Table IIA			
Step	Instructions	Input Data/Units	Ke	ys	Output Data/Units
1	Enter Program				
2	Store Source And Load Impedances	50 Ra Xa	STO STO STO	1 2 3	
3	Select Z1 and Store	Z1	STO	4	
4	Select Open or Shorted Z ₁ Line Configuration 1 For Shorted 2 For Open	1 or 2	STO	0	
5	Calculate Θ_1 And Z ₂		GSB	0	$\Theta_1 Z_2$
6	Repeat Steps 3, 4 and 5 For Other Z ₁ Values And Configuration, If Desir	ed			

			Table	e IB			
Sten	Key Entry	Key Code	Comments		070.0	15.00	
004		05 44 00			5103	45 03	
001	(g) LBL U	25 14 00			X < Y	45.04	
	HUL 9	35 09			BCI 3	55.03	
	(I) tan	10 44				25.53	
	BCL 6	45.00			BCL 4	55.04	
	HUL O	51		040	(0) x2	25 53	
	BCI 8	55.08		040	(9/ ~	41	
	BCL 0	55.00			BCL 1	55 01	
	BCL 7	55.07			x	51	
010	x	51			RCL 1	55 01	
010	_	31			(q) x^2	25 53	
	(q)→P	25 34			RCL 3	55 03	
	STO 2	45 02			х	51	
	R∔	12			_	31	
	STO 5	45 05			RCL 3	55 03	
	RCL 0	55 00		050	RCL 1	55 01	· · · · · · · · · · · · · · · · · · ·
	RCL 8	55 08			-	31	
	×	51			+	61	-
	RCL7	55 07			(f) \sqrt{x}	16 53	Z2
020	+	41			PRx	65	
	RCL 6	55 06			HCL 1	55 01	
	(g) → P	25 34			HCL 3	55 03	
	RCL 2	55 02			-	51	
	÷	61				55.04	
	HCL 8	55 08		060	RCL 4	55.01	
	X	51		060	ROLI	51	
	X < Y	55.05			<u>~</u>	61	
	HULD	55.05			(α) tan -1	25 44	Θο
020	V >V	11			PRx	65	- 2
030	^ ≪ y (f) → R	16 34			(g) RTN	25 13	

				Reg	isters				
0	1 50	2	3	4	5	6 Ra	7 Xa	8 Z1	9 O
S0	S1	S2	S3	S4	S5	S6	S7	S8	S9
A		В	С		D	E		1	

Conclusions

The above analysis indicates that several methods exist to provide an exact match (at one frequency) using simple transmission line circuits. Therefore it seems unnecessary to use the common approximations. It is true, that in most cases the calculations may be more complicated for the exact methods. However, the programmable pocket calculator performs all these calculations with a

	Tat	ole IIIA			
Step	Instructions	Input Data/Units	Key	/5	Output Data/Units
1	Enter Program				
2	Store Source And Load Impedances	50 Ra Xa	STO STO STO	1 2 3	
3	Select Z1 and Store	Ζ1	STO	4	
4	Select Open or Shorted Z ₁ Line Configuration 1 For Shorted 2 For Open	1 or 2	STO	0	
5	Calculate Z_2 and Θ_1		GSB	0	Ζ ₂ Θ ₁
6	Repeat Steps 3. 4 and 5 For Other Z_1 Values and Configuration. If Desired				

minimum of effort. In addition, the programs permit quick changes in line characteristics to obtain the optimum physical configuration (short to ground, high impedance to ground, suitable line lengths and widths, etc.).

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Table IIB							
Step	Key Entry	Key Code	Comments	Step	Key Entry	Key Code	Comments
001	(g) LBL 0	25 14 00			STO 5	45 05	
	RCL 3	55 03		020	R↓	12	
	RCL 2	55 02			RCL 1	55 01	
	(q) → P	25 34			x	51	
	(g) 1/x	25 64			(f) $\sqrt{\mathbf{x}}$	16 53	
	(f) → R	16 34			PBx	65	Z ₂
	(a) 1/x	25 64			STO 6	45 06	2
	x ≥v	11			(a) RTN	25 13	
	GŠBí	13 12			(a) LBL 1	25 14 01	
010	(g) tan - 1	25 44			(g) 1/x	25.64	
	$(a) \times >0$	25 41			RCL 4	55.04	
	GTO 3	14 03		030	÷	61	
	1	01		000	CHS	22	
	8	08			(a) RTN	25 13	
	õ	00			(a) B 2	25 14 02	
	+	41			RCL 4	55 04	
	(a) I BL 3	25 14 03				51	
	PRx	65	Θ		(a) RTN	25.13	
	1110	00			(9)	2010	

				Reg	isters				
0 1 or 2	1 50	2 Ra	з Ха	4 Z ₁	5	6	7	8	9
S0	S1	S2	S3	S4	S 5	S6	S7	S8	S9
A	В		С		D		E	1	

			Tab	ole IIIB			
Step	Key Entry	Key Code	Comments	Step	Key Entry	Key Code	Comments
001	(g) LBL 0 RCL 2 (g) x ² RCL 3 (g) x ² + RCL 2 ÷	25 14 00 55 02 25 53 55 03 25 53 41 55 02 61		030	RCL 1 x RCL 4 ÷ (g) tan - 1 (g) x>0	61 55 01 51 55 04 61 13 12 25 44 25 41	
010	RCL 3 RCL 2 \div (g) x ² 1 + \div (f) \sqrt{x}	55 03 55 02 61 25 53 01 41 61 16 53			GTO 3 1 8 0 + (g) LBL 3 PRx STO 5	14 03 01 08 00 41 25 14 03 65 45 05	Θ1
020	RCL 1 (f) √x x PRx STO 6 RCL 2 RCL 3	55 01 16 53 51 65 45 06 55 02 55 03	Z ₂	040	(g) RTN (g) LBL 1 (g) RTN (g) LBL 2 (g) 1/x CHS (g) RTN	25 13 25 14 01 25 13 25 14 02 25 64 22 25 13	

				Regi	isters				
0 1 or 2	1 50	2 Ra	з Ха	4 Z ₁	5	6	7	8	9
S0	S1	S2	S3	S4	S5	S6	S7	S8	S9
A	В		С		D	E		1	

Class E Switching-Mode RF Power Amplifiers

Typical characteristics include low power dissipation, low sensitivity to component tolerances (including transistor), and well-defined operation.

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Class E switching-mode RF power amplifiers offer high efficiency (consequently low power dissipation, low junction temperature and high reliability) and low sensitivity to component tolerances, including transistor characteristics (consequently manufacturing reproducibility). Circuit operation is well-defined and predictable; measured performance agrees with design calculations to within measurement error.

Shortcomings of Conventional Class B And C Amplifiers, and Advantages Of Class E

The Class E amplifier' can now replace Class B and C transistor RF power amplifiers in most applications, yielding improved performance, reliability and manufacturing, and moving the design procedure from the realm of "art" to that of "science." The theory and operating characteristics of Class E circuits have now been verified independently by a number of organizations; some have published their results ²⁻³⁻⁴. All confirm the information given in the original publication'. To understand the advantages of Class E circuits, let us first review the present status of conventional Class B and C circuits.

Conventional Amplifier Design

Class B and C transistor power amplifiers are usually designed empirically; the published design equations only provide a starting point for the empirical work. The resulting amplifiers are generally considered to be quite sensitive to variations of transistor characteristics and loadnetwork component values, although a *priori* predictions of these sensitivities are never given. It is common (even necessary in some cases) for an equipment manufacturer to require that transistors be purchased from the one vendor around whose transistor the circuit was designed. If transistors of the same type-number from another vendor are used, it is often necessary to change the circuit design substantially to accommodate the substitute transistor, even though the two transistors are marked with the same type-number and meet the same set of specifications. Unfortunately, it is not possible to make a priori predictions of the variation of amplifier performance with frequency or with deviations in component values; hence a priori evaluation of design trade-offs (commonly done in other electronic designs) is not feasible for these conventional amplifiers. That places a severe limitation on the possible degree of design optimization. It also increases the cost of design, because the designer must try out experimentally every candidate design being compared against other alternatives, instead of trying out only the few candidate designs which are known a priori to be the most attractive.

The reason for the poor predictability and reproducibility is straight-forward: the commonly used design procedures are based on invalid assumptions.⁵ Nevertheless, a skilled engineer can ultimately produce an acceptable design by the "trial-and-error" process. The resulting circuit will dissipate as heat about 20-40 percent of the DC input power (25-67 percent as much as the RF output power). Careful thermal design is needed to keep the transistor junction temperature low enough to obtain satisfactory reliability.

Class E Amplifier Advantages

In contrast to the situation described above, Class E amplifiers are *a priori* predictable, have low (and predictable) sensitivities to variations in component values, exhibit considerable indifference to variations in transistor parameters, and dissipate as heat only about 10-20 percent of the DC input power (11-25 percent as much as the RF output power). The reduced power dissipation (by a factor of about 3 for a given RF output) results in about an order of magnitude reduction of transistor failure rate, and about 20 percent reduction of DC power input for a given RF output. The reduction of power input extends battery life in portable applications and reduces the cost of electric power for high-power equipment. Well-defined circuit operation means that design decisions can be made with full knowledge of the trade-offs among any alternative sets of design parameters being considered. A straight-forward design procedure, which results in a circuit which works the way it was designed to work, gives confidence in the integrity and reproducibility of the design. This is in contrast to the trial-and-error method of design commonly used for conventional amplifiers.

Class E circuits can use bipolar transistors, fieldeffect transistors, or vacuum tubes.

Principles of Class E Operation

Switching-mode power converters are now widely accepted for use in DC power supplies. They achieve high efficiency by operating the transistor as a switch. When the transistor current is high (the "on" state of the switch), the voltage across it is low (V_{CE} (sat)); when there is high voltage across the transistor (the "off" state of the switch), the current is virtually zero because the transistor is fully "off." Power dissipation is low because high voltage and high current are not imposed simultaneously on the transistor. These switching-mode principles can be applied to RF power amplifiers, too, and indeed have been. An extensive bibliography of previous work in high-efficiency amplifiers can be found in Reference 1.

Performance of the usual switching-mode amplifier is severely limited if the transistor switching times are longer than only a small fraction of the RF period. However, the Class E amplifier extends high-efficiency switching-mode operation to higher frequencies, *even if the transistor switching time is an appreciable fraction of the RF period.* Before observing how this can be done, we shall first review the operation of a relatively primitive switching-mode circuit.

Switching Transistor's Voltage And Current Relationships

In general, a switching transistor's voltage and current waveforms will both be approximately trapezoidal, as shown in idealized form in Figure 1. The voltage will be near zero during the transistor's "on" interval and will be high (e.g. at about $2V_{CC}$) during the "off" interval. Similarly, the transistor current will be virtually zero while the transistor is off, and a relatively high value while the transistor is on. If the load is resistive, the voltage rise occurs at the same time as the current fall, and vice versa, as illustrated in Figure 1.

During the voltage and current transitions (while the transistor is switching on and off), appreciable voltage and current are applied to the transistor simultaneously (e.g., halfway through the switching transition, 50 percent of the maximum voltage and 50 percent of the maximum current are applied to the transistor). At every instant of time, the power dissipation is the product of the transistor voltage and current; therefore there will be large power dissipation during the switching transitions. If those transitions occupy an appreciable fraction of the RF period, the average power dissipation (averaged over the RF period) will be large. In



addition, the application of appreciable voltage and current simultaneously may cause continual deterioration of a power transistor, eventually resulting in transistor failure.⁶ (The same condition occurs in many conventional Class B and C amplifiers, but is usually not considered explicitly.) Despite the designer's best efforts to make the transistor switch as fast as possible, the switching power dissipation remains an ultimate limitation on the circuit performance at high frequencies. Attempts to reduce the switching times may actually *increase* the secondbreakdown stress!

What About Power Dissipation?

Can anything be done about the power dissipation during switching? The key to high-efficiency and lowstress operation is in the transistor voltage and current waveforms: the current has to rise and fall, and so does the voltage, but they don't have to do it at the same time! We need a current in which the voltage and current transitions are displaced in time relative to one another. If we can achieve this, we will have created an amplifier the Class E amplifier — which can have high power efficiency even if the switching times are considerable fractions of the RF period. Figure 2 shows the desired waveforms, in idealized trapezoidal form to present the concept.

In addition to the displacement of the voltage and current transitions, another characteristic of Class E waveforms is illustrated in Figure 2. This feature removes a second source of appreciable power dissipation and second-breakdown stress which exists in conventional RF power amplifiers and in some switching-mode amplifiers. In every RF power amplifier, there is a capacitor in parallel with the transistor — either intentionally wired into the circuit as part of the load network, or just the unavoidable capacitances of the transistor and the wiring. If the transistor is turned on when the voltage (V) across this capacitance is any value other than V_{CE} (sati

the transistor will discharge the capacitor to $V_{CE (sat)}$. In that event, the stored energy of 1/2C $(V-V_{CE (sat)})^2$ will be dissipated as heat, *independent of the transistor switching time and the resistance in the discharge path.* To avoid this condition, the passive network components must cause the capacitor voltage to be *already* at $V_{CE (sat)}$ at the time the transistor will be turned on.

Frequency Response and Rate of Current Change

A third feature of the Class E waveforms, also shown in Figure 2, caters to a limitation of bipolar junction transistors at high frequencies: the transistor will unsaturate if the rate of change of transistor collector current is required to exceed a certain defined value. In that event, the resulting high collector voltage



causes high-power dissipation and second-breakdown stress during the turn-on transition. In the Class E amplifier, this limitation is avoided by requiring of the transistor only a moderate (and well-defined) rate of current increase, known to be within the capability of the type of transistor being used, at the input drive being provided. The current which the transistor must conduct immediately at turn-on is equal to C(dV_{CE}/dt) at that time, where C is the capacitance across the transistor. By making dV_{CE}/dt zero at turn-on time, the Class E amplifier requires the transistor to begin conducting at only zero current. Some conventional designs, which turn on the transistor when dV_{CE}/dt is positive, require the transistor to abruptly conduct a large value of current. The transistor then unsaturates because it cannot turn on abruptly, resulting in undesirable power dissipation and second-breakdown stress.

High Efficiency Design Requirements

Now we can see that the waveforms of Figure 2 r.f. design

meet the three conditions for high efficiency discussed above:

(a) the voltage and current transitions occur at different times,

(b) the voltage across the transistor at turn-on time is $V_{\text{CE}\,(\text{sat})}$ and

(c) the slope of the transistor voltage at turn-on time is zero.

Figure 3 shows the approximation to the waveforms of Figure 2 generated by the low-order implementation of Class E principles discussed in this paper. The



waveforms of Figure 3 are like those of Figure 2, except (a) the waveform tops are rounded instead of flat, and (b) for each waveform, the rise time is not equal to the fall time. We shall now discuss the synthesis of a circuit to generate the desired Class E waveforms.

Design Procedure

In a circuit containing a periodically operated switch plus passive components (L, R, C, and transmission lines), the current through the switch in the "on" state, and the voltage across the switch in the "off" state, are both determined by the transient response of the passive network connected to the switch, excited by the periodic operation of the switch. Figure 4 shows a circuit which will give a low-order approximation to the desired waveforms if the component values are chosen properly. L1 is a high-reactance shunt-ted choke which only feeds DC into the circuit, and takes no further part in the RF action. R is the load to which the RF power is to be delivered. C1 is a first approximation to a delay element to delay the rise of the voltage while the transistor current is falling during the turn-off transition (C1 gives a parabolic-shaped approximation to a true delay). This satisfies the first requirement for high-efficiency operation, discussed above: the voltage rise is delayed until after the current fall. C1, C2, L2 and R comprise a damped-resonant network which rings after the transistor turns off. The resonant frequency (not the same as the amplifier operating frequency) and the damping factor are chosen to meet the remaining requirements for high-efficiency operation: the voltage fall occurs before the current rise, the capacitor voltage just before transistor turn-on is VCE (sat), and the slope of the voltage waveform at turn-on is zero.



Design Equations for Low-Order Class E Circuit

The following design equations define the component values for the circuit of Figure 4 when the transistor duty cycle is 50 percent (conduction angle is 180°). Modified equations apply for other values of duty cycle.

The peak collector-emitter voltage should be less than the transistor breakdown voltage to avoid damaging the transistor:

$$V_{CE(pk)} < BV_{CEV} \tag{1}$$

 BV_{CEV} is the collector-emitter breakdown voltage with the base-emitter junction reverse-biased (e.g., by one volt). (BV_{CEV} is the applicable voltage rating because, in a Class E circuit, the base is solidly reverse-biased by the time that V_{CE} approaches its peak value.)

Having defined the maximum allowable peak voltage, the working peak voltage can be chosen, using whatever safety factor the user wishes. Then the powersupply voltage is:

$$V_{CC} = \frac{V_{CE(pk)} + 2.562 V_{CE(sal)}}{3.562}$$
(2)

With the power-supply voltage chosen, the required value of R is:

$$R = 0.5768 \frac{(V_{CC} - V_{CE[sat]})^2}{P}$$
(3)

where $V_{CE \text{ (sat)}}$ is the collector-emitter saturation voltage in RF operation (usually one to three volts larger than the value measured in a DC test), and P is the RF power delivered to R.

The network loaded Q (Q_1) can be chosen by the designer, considering the trade-offs among operating frequency range, power losses in the reactors, and harmonic output (to be discussed in the next section). It is required, however, that:

$$Q_L \ge 1.7879 \tag{4}$$

Choosing Q_L defines the value of L2:

$$L2 = Q_L R/2\pi f$$

where f is the operating frequency. The required value of C2 is then:

$$C2 = \frac{1}{2\pi f Q_L R} \left[1 + \frac{1.110}{Q_L - 1.7879} \right]$$
(6)

Inductor L1 is chosen to be large enough such that the current in L1 is almost pure DC, and L1 then has little effect on the RF operation:

$$L1 \ge 10/(2\pi f)^2 C1$$
 (7)

Now the required value of C1 is:

$$C1 = \frac{0.1836}{2\pi t R} \left[1 + \frac{0.81Q_L}{Q_L^2 + 4} + \frac{0.7}{(2\pi f)^2 L 1} \right]$$
(8)

The last term is small, and can be neglected for a first approximation.

The collector efficiency is:

$$\eta C = \frac{1 - (2\pi A)^2/6 - \frac{V_{CE}(sat)}{V_{CC}}(1 + A - [2\pi A]^2/6)}{1 - (2\pi A)^2/12}$$
(9)

Here, t_f is the collector-current fall time, 100 percent to 0 percent of an assumed ramp waveform, and A= $(1 + 0.82/Q_L)$ ft_f.



(5)



Effects of Deviations in Circuit Parameter Values

The Class E amplifier is guite tolerant of deviations from nominal frequency and component values. The reason can be deduced from physical considerations: deviations from nominal cause the voltage waveform to deviate from the low-voltage/zero-slope condition at turn-on time. But the waveform has a broad, flat bottom in the vicinity of the intended turn-on time. Thus, if Q1 is turned on somewhat earlier or later than at the exact bottom point of the waveform, the voltage on C1 will be little different from the value at the intended turn-on time, and the slope will be nearly equal to the intended zero slope. Similarly, certain changes in component values will cause the bottom of the waveform to move up or down from the intended value of V_{CE (sat)}. This will cause the voltage at turn-on time to be not quite equal to V_{CE (sat)}, but not nearly as large as in some conventional amplifiers which have approximately 2V_{CC} on the capacitor at turn-on time. The Class E amplifier operates nominally at a very favorable operating point, and the changes of operating conditions with variations of frequency or component values are fairly small. Mathematical analysis' gives exact value for these variations. The results are shown in Figures 5 (vs frequency and 6 (vs component values).* Independent verifica-

*Figures 5 and 6 are for a circuit which does not clamp negative $V_{CE}.$ Some RF power amplifier circuits clamp negative V_{CE} (intentionally or unintentionally) by any one or more of several mechanisms. Parts of Figures 5 and 6 are changed if negative V_{CE} is clamped.

References

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tion was published by Raab³, who obtained an analytical solution using a high-Q approximation.

Harmonic Output

Sokal and Raab[®] give the harmonic output of the Class E amplifier as a function of the harmonic number and the value chosen for QL. Their results are shown in Table 1. They also give the resulting harmonic suppression requirement for the filter (if any) which is placed between the output of the L2-C2 branch and the load R (usually a radio-transmitting antenna), in order to reduce the amplitudes of all harmonics at R to any specified number of dB below the amplitude of the fundamental-frequency component.

As in all other types of RF power amplifiers, there is a trade-off in the choice of QL:

1. A higher value of Q_L reduces the harmonic output (see Table 1).

2. A lower value of Q₁ reduces the fraction of the transistor output power which is dissipated in the RF resistances of L2 and C2.

3. A lower value of Q_L allows operation of high efficiency over a wider frequency range. Figure 5 shows a graph of efficiency vs. frequency for values of QL from 1.7879 (the minimum value for which Class E operation is possible) to 20.

With the information in Table 1 and Figure 5, and a knowledge of filter design methods, the designer can choose the combination of Class E load-network QL and filter design which best meets the requirements of a particular design project.

Table 1. Harmonic Components of Current Flowing to Load Through C2 and L2.

n is the harmonic number; \mathbf{I}_{n} is the nth-harmonic current.

n	i_n/l_1 with $Q_L =$					
·	2			3 or more		
N	1	1.000		1.000		
	2	2.70E-1		$\sim 0.51/Q_L$		
	3	4.76E-2		~0.080/QL		
	4	2.31E-2		~0.037/QL		
	5	1.03E-2		~0.016/QL		
	6	6.35E-3		~0.010/QL		
	7	3.76E-3		\sim 0.0059/QL		
	8	2.61E-3		\sim 0.0041/QL		
	9	1.77E-3		\sim 0.0028/QL		
	10	1.32E-3		\sim 0.0021/Q _L		

Experimental Results

During the past few years a moderate number of HF and VHF Class E amplifiers have been built at Design Automation, Inc., the first author's firm. Here we shall summarize the measured results obtained with a few of those amplifiers and compare them, where possible, with published data for conventional Class C amplifiers using the same transistor types.

Table 2 compares the performance of Class E and Class C 27 MHz designs using the Motorola MRF472 transistor. Data are given for the Class E amplifier at two DC supply voltages. The Class C amplifier was built by Motorola Semiconductor Products⁹. To make a fair comparison, one should really add a harmonic-suppression filter to the Motorola amplifier and subtract a few percentage points of efficiency from the tabulated value to account for the unavoidable filter power losses.

Table 3 compares results for Class E and Class C VHF amplifiers using the Communications Transistor Corporation A25-28 transistor.

The Class C amplifier data are given on the CTC transistor data sheet. Again, a few percentage points of efficiency should be subtracted for parasitic losses in a subsequent harmonic-suppression filter.

Table 2. Compari	son of 27 MHz Amp	olifiers Using Motorola I	MRF472 Transistor.
	CI	ass E	Class C
V _{CC} (V)	13.5	27	12.5
Power output (W)	5.0	20	4.0
Collector efficiency (%)	85	86	65*
$P_{diss}/P_{out} = 1/\eta - 1$	0.18	0.16	0.54
Second harmonic (dBc)	N	67	Not given
Third harmonic (dBc)	-	67	Not given
Number of stages		3	1
RF power input (mw)	1	0	200 typ
Harmonic-suppression filter included?	Y	es	No.

*Class C amplifier efficiency would be reduced by a few percentage points if a harmonic-reduction filter were added, and P_{diss}/P_{out} would be increased.

Table 3. C	omparison of VHF Am	plifiers Using CTC A25	5-28 Transistor.
	Clas	ss E	Class C
	Sample 1	Sample 2	
Power output (W)	27	28	25
Frequency (MHz)	54	54	80*
Collector efficiency (%)	87	92	65**
$P_{diss}/P_{out} = 1/\eta - 1$	0.15	0.09	0.54
Power gain (dB)	Not Available	12	9.9 typ. @ 80 MHz 13.1 typ. @ 54 MHz
Harmonic-suppression filter included?	Yes	Yes	No**

*According to the manufacturer, efficiency at 54 MHz is approximately the same as at 80 MHz. **Class C amplifier efficiency would be reduced by a few percentage points if a harmonic-suppression filter were

added, and P_{diss}/P_{out} would be increased.

The last example of a Class E amplifier has no Class-C counterpart. Figure 7 is a photograph of a demonstratormodel Class E amplifier being manufactured by Design Automation, Inc. This unit is designed as a demonstrator for test and evaluation by others who may wish to evaluate Class-E technology in their own laboratories. Output is up to 7 W at 10.5 MHz, depending on the DC collector supply voltage (the RF output voltage is linearly proportional to the DC supply voltage). The amplifier will accommodate any TO-5 output transistor the user wishes to plug into the socket. We have interchanged many different transistor types, from numerous manufacturers, with hardly any change in circuit operation. That is virtually unthinkable in a conventional Class B or C circuit. Table 4 lists examples of transistors which have been so interchanged.



Table 4. Examples of Transistor Interchangeability in 10.5-MHz Demonstrator.

2N3553	RCA, Motorola, Raytheon
2N3725	Motorola, T.I., Fairchild
2SC2329	Nippon Electric
BRS23A	Philips (Amperex)
2N5262	RCA
2N3735	Motorola, UPI Semiconductor
2N3734	Raytheon
2N6376	National Semiconductor
2N5108	Solitron
2N5913	TRW Semiconductor

Acknowledgement

This material was first presented at the 1979 ELECTRO conference in New York in April. Kind permission for utilization of this information was provided by Electronic Conventions, Inc.



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Transmitter Type Ceramic Capacitors 1pf to .068mfd • 2.5 to 30KVDC





RF Component Catalog

Texscan Corporation announces the availability of its new 68-page component catalog. Detailed information is provided on the full line of attenuators, including fixed pads to 18 GHz, rotary attenuators to 12.4 GHz and a complete line of programmable attenuators for computer controlled test applications.

The filter section offers graphs and instructive information on tunable, cavity, tubular and miniature lumped component filters. A third section on oscillators provides theory and applications for oscillators available over the frequency range of 5 MHz to 18 GHz.



This three section catalog is a must for all RF system designers, says Texscan.

Contact Texscan Corporation, 2446 North Shadeland Avenue, Indianapolis, IN 46219. Circle INFO/CARD #122.

Composite Elastomer EMI/RFI Shield

Combo[®] Seal, vulcanized strip gasketing combining silicone rubber with knitted metal mesh to provide an effective EMI/RFI shield as well as a seal against severely hostile environments, has been announced by Metex Corporation, Edison, New Jersey.

The new shielding gaskets can be extruded in a wide variety of forms and shapes that not only lend themselves to wide adaptability in original designs, but also permit retro-fit into existing product configurations.

The Combo[®] Seal strip gasketing retains its inseparable structural integrity as well as its flexibility in extremes of temperatures, in corona and ozone atmospheres, moisture and steam,



and after prolonged weathering and aging. While the compression-deflection characteristics of the gasketing material is one of its prime features, the nature of the silicone rubber/knitted metal mesh extruded composite construction assures excellent resistance to compression set.

Total shielding effectiveness of up to 90 dB, 10.0 kHz to 1.0 GHz, 20 psi, is claimed for the material. The silicone rubber component of the Combo[®] Seal composite meets and exceeds the specification for Rubber, Silicone: Low- and High-Temperature Tear Resistant, ZZ-R-765, Class 11a, Grade 50. It is colored gray, has a specific gravity of 1.13 ± 0.03 ; brittle point, 100°F. ASTM D-746. The composite gasketing offers a peel strength of 3 lbs. (min) per linear inch.

Contact Metex Corporation, 970 New Durham Road, Edison, N.J. 08817. INFO/CARD #127.

Thick-Film Filters

Telonic Berkeley, is now offering thick-film filters in volume production runs. By combining thick-film technology, developed and proven in the company's attenuator products, with new computer-aided filter designs, Telonic Berkeley now has nine different thick-film filters in volume production.

Two major advantages to thick-film filters are lower cost and excellent repeatability. Photolithography is the key in both instances, as it provides a greatly reduced labor requirement and ensures exact repeatability of the design from one production order to another.

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44



Contact the Marketing Department, Telonic Berkeley, 2825 Laguna Canyon Road, Laguna Beach, Calif. 92652. INFO/CARD #126.

Automated Counter

Built-in calculating capability and automatic measurement routes are featured in this new HP 5335A electronic counter.

The HP 5335A combines reciprocaltaking measurement techniques with automatic interpolators to provide 9 digits per second display for all frequency measurements up to 200 MHz (standard) or to 1.3 GHz (optional). Single-shot time interval resolution is 2 nanoseconds, while time interval averaging yields a resolution down to 100 picoseconds when measuring repetitive events. The high single-shot resolution allows measurements where time information must be extracted precisely without averaging. For example, statistics are meaningful only with high single-shot resolution.

Other measurements included are: frequency ratio, period, period average, and totalizing. The counter's full sensitivity, bandwidth and input signal conditioning capabilities can be applied to both numerator and denominator in frequency ratio measurements.



The following measurements requiring pressing one or several keys on the HP 5335A front panel keyboard are phase, duty cycle, rise and fall times and slew rate. In addition, statistical data such as standard deviation and mean value are automatically computed and displayed for any of the measurements.

For those RFI/EMC sensitivity test situations, the 5335A has been designed to meet most MIL STD 461/2/3

and VDE 0871/0875, FTZ 526/1979 and 527/1979 limits for electromagnetic compatibility (radiated and conducted emissions and susceptibility). This suits the 5335A for applications such as sensitive receiver testing and maintenance.

Contact Inquiries Manager, Hewlett-Packard Company, 1507 Page Mill Road, Palo Alto, Calif. 94304.

Termination Insensitive Mixer

ANZAC Division of Adams-Russell has developed a Termination Insensitive Mixer covering the 1 to 7 GHz region. Now the microwave system can have the benefits of TIM; flat conversion loss regardless of sum frequency match, and flat, predictable 3rd order intermodulation performance even into high IF mismatch. The MD-162 provides 6 dB typical, 7.5 dB Max conversion loss with IF port response to 2.0 GHz. The mixer also features +8 dBm 1 dB compression point and 3rd order intercept of +18 dBm.



Contact ANZAC division, Adams-Russell, Inc., 80 Cambridge Street, Burlington, Mass. 01803. INFO/CARD #132.

New 2·kW Broadband RF Amplifier

The constant search for smaller, lighter-weight high-power amplifiers for broadband RF applications has been rewarded with the introduction of the Model 2000L by Amplifier Research Corporation, Souderton, Pa.

In an attractively-styled 5-foot-high stand-alone cabinet occupying less than four square feet of floor space, the new AR Model 2000L delivers 2000 watts minimum cw power across its entire bandwidth of 10 kHz to 220 MHz, and 4000 watts minimum in pulse mode at 25 percent duty cycle to 150 MHz. As with all AR amplifiers, a 1-milliwatt signal from a frequency synthesizer or sweep generator is more than ample to drive this Class AB linear amplifier at its rated output power.

The 2000L is totally impervious to load mismatch, withstanding even the infinite VSWR of shorted or open output connections without damage to itself or shutdown of the system. Its entire

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hybrid circuits can provide. And Fluke's commitment to quality insures maximum uptime at a price that's right for the line – only \$699 U.S."

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bandwidth is instantly available, requiring no tuning or gain adjustment during sweep operations. Pulse and blanking capability make this an attractive amplifier for high-power pulsed NMR or physics experiments. Cooling is either self-contained forced air or tap water. An optional IEEE-bus-compatible computer interface module is available for automatic control of amplifier switching.

Contact Amplifier Research Corporation, 160 School House Rd., Souderton, Pa. 18964. INFO/CARD #136.

Miniature Filter Line

A line of miniature RF and microwave filters, the UltraminTM Series. has been introduced by Wavetek Indiana, According to Wavetek, a breakthrough in the filter miniaturization process allows them to produce filters in the 10 to 1000 MHz range that give high performance in a small, lightweight package.

A52U UHF

UltraminTM filters are designed to save circuit board space and reduce weight in critical applications such as airborne systems. The smallest Wavetek filter, the T5, is only 0.36 inches in diameter and weighs less than 0.046 ounces

The new Wavetek filter line includes the: T5, a 3 to 4 section filter that mounts in a T0 5 case; T8, a 3 to 6 section filter in a TO 8 case; T8S, a T8 filter with a threaded mounting stud for improved grounding: R Series, a 3 to 10 section filter in a 0.31 by 0.44 inch rectangular metal case; and the S Series, a 3 to 12 section filter in a 0.31 by 0.31 inch square metal case.

Computer designed Ultramin[™] Filters are available in Bandpass, Lowpass, Highpass, and Bandstop designs. A typical 0.01 dB Tchebychev or Butterworth response is standard and Gaussian. Bessel or Linear Phase responses are available on special order. Bandpass filters are available with 3 dB Bandwidths from 2 percent to 70 percent of center frequency.

Contact Wavetek Indiana, Inc., P.O. Box 190, Beach Grove, Ind. 46107. **INFO/CARD #137.**





Similar in appearance to the A62 RF Sweep Amplifier pictured, the A52U RF Sweep Amplifier has a frequency range of 1–900 MHz. Flatness is ±.5 dB. Gain is 30 dB nominal. Input VSWR is 1.5:1 max with typical VSWR of 1.2:1. Available in 50 or 75 ohm impedance, the unit is an excellent general purpose lab amplifier amplifying signals for receivers, frequency counters, spectrum analysers, oscilloscopes, markers and detectors. It is rugged enough for mobile applications. Line filtering and double shielding prevent ambient and power line interference.

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2. RESOLUTION: 0.1 Hz to 12 MHz, 1 Hz to 50 MHz, 10 Hz over 50 MHz.

3. ALL METAL CASES: Not only are the heavy gauge aluminum cases rugged and attractive, they provide the RF shielding and minimize RFI so necessary in many user environments. 4. EXTERNAL CLOCK INPUT/OUTPUT: Standard on the 8010/ 8013 series and optional on the 7010 series is a buffered 10 MHz clock time base input/output port on the rear panel. Numerous uses include phase comparison of counter time base with WWVB (U.S. National Bureau of Standards). Standardize calibration of all counters at a facility with a common 10 MHz external clock signal, calibrate scopes and other test equipment with the output from precision time base in counter, etc., etc.

5. ACCURACY: A choice of precision to ultra precision time base oscillators. Our \pm 1 PPM TCXO (temperature compensated xtal oscillator) and \pm 0.1 PPM TCXO are sealed units tested over 20-40°C. They contain voltage regulation circuitry for immunity to power variations in main instrument power supply, a 10 turn (50 PPM) calibration adjustment for easy, accurate setability and a heavily buffered output prevents circuit loads from affecting oscillator. Available in the 8010 and 8013 series is our new ultra precision micro power proportional oven oscillator. With \pm .05 PPM typical stability over 10-45°C, this new time base incorporates all of the advantages of our TCXO's and virtually none of the disadvantages of the traditional ovenized oscillator: Requires less than 4 minutes warm-up time, small physical size and has a peak current drain of less than 100 ma.

6. RAPID DISPLAY UPDATE: Internal housekeeping functions require only .2 seconds between any gate or sample time

period. At a 1 second gate time the counter will display a new count every 1.2 seconds, on a 10 second gate time a new count is displayed every 10.2 seconds. (10.2 seconds is the maximum time required between display updates for any resolution on any model listed).

7. **PORTABILITY:** All models are delivered with a 115 VAC adapter, a 12 VDC cord with plug and may be equipped with an optional ni-cad rechargeable battery pack installed within its case. The optional Ni-Cad pack may be recharged with 12 VDC or the AC adapter provided.

8. COMPACT SIZES: State-of-the-Art circuitry and external AC adapters allowed design of compact easy to use and transport instruments.

Series 8010/8013: 3" H x 7-1/2" W x 6-1/2" D Series 7010: 1-3/4" H x 4-1/4" W x 5-1/4" D

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10. CERTIFIED CALIBRATION: All models meet FCC specs for frequency measurement and provided with each model is a certificate of NBS traceable calibration.

11. LIFE TIME GUARANTEE: Using the latest State-of-the-Art LSI circuitry, parts count is kept to a minimum and internal case temperature is only a few degrees above ambient resulting in long component life and reliable operation. (No custom IC's are used.) To demonstrate our confidence in these designs, all parts (excluding batteries) and service labor are 100% guaranteed for life to the original purchaser. (Transportation expense not covered).

12. PRICE: Whether you choose a series 7010 600 MHz counter or a series 8013 1.3 GHz instrument it will compete at twice its price for comparable quality and performance.

MODEL 8010A/8013 1.1 GHz/1.3 GHz



MODEL	RANGE (From 10 Hz	10 MHz TIME BASE			AVG SENSITIVITY		GATE	RESOLUTION		EXT. CLOCK	SENSITIVITY	NI-CAD	
		STABILITY	AGING	DESIGN	IU Hz to 500 MHz	500 MHz to 1.1 GHz	TIMES	12 MHz	60 MH2	Max. Freq	INPUT/OUTPUT	CONTROL	BATTERY PACK
7010A	600 MHz	±1PPM	<1 PPM/YR	тсхо	15 mV	NIA	(3) 1. 1. 10 sec.	.1 Hz	1.82	10 Hz (600 MHz)	YES OPTIONAL	NO	YES OPTIONAL
7010 1A		± 0.1 PPM											
8010A	1 1 GHz	± 1 PPM	<1 PPM/YR	тсхо.	15 mV	30 mV	(4) 01 1. 1. 10 sec	1 Hz	1.Hz	10 Hz 1 GHz)	YES STANDARD	YÉ5	YES OPTIONAL
8010 1A		±01PPM											
8010 05A		± 05 PPM		осхо									
8013	1 3 GHz	± 0.1 PPM	1.0014.04	TCXO.	15	30 mV	(4) 01. 1, 1, 10 se c .	1942	1 Hz	10 Hz (1 3 GHz)	YES STANDARD	YES	YES OPTIONAL
8013 05		± 05 PPM	I PPM TF		vmci								

SERIES 7010A

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	Circuitry Installed Inside Unit	\$19 9
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#8010A	1.1 GHz Counter - 1 PPM TCXO
#8010 1A	1 1 GHz Counter - 0 1 PPM TCXO
#8010.05A	1 3 GHz Counter - 05 PPM Oven
#8013 1	1 3 GHz Counter - 0 1 PPM TCX0
#8013.05	1.3 GHz Counter - 05 PPM Over

OPTIONS

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Are its RF characteristics as good as Teledyne's other TO-5 relays?

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