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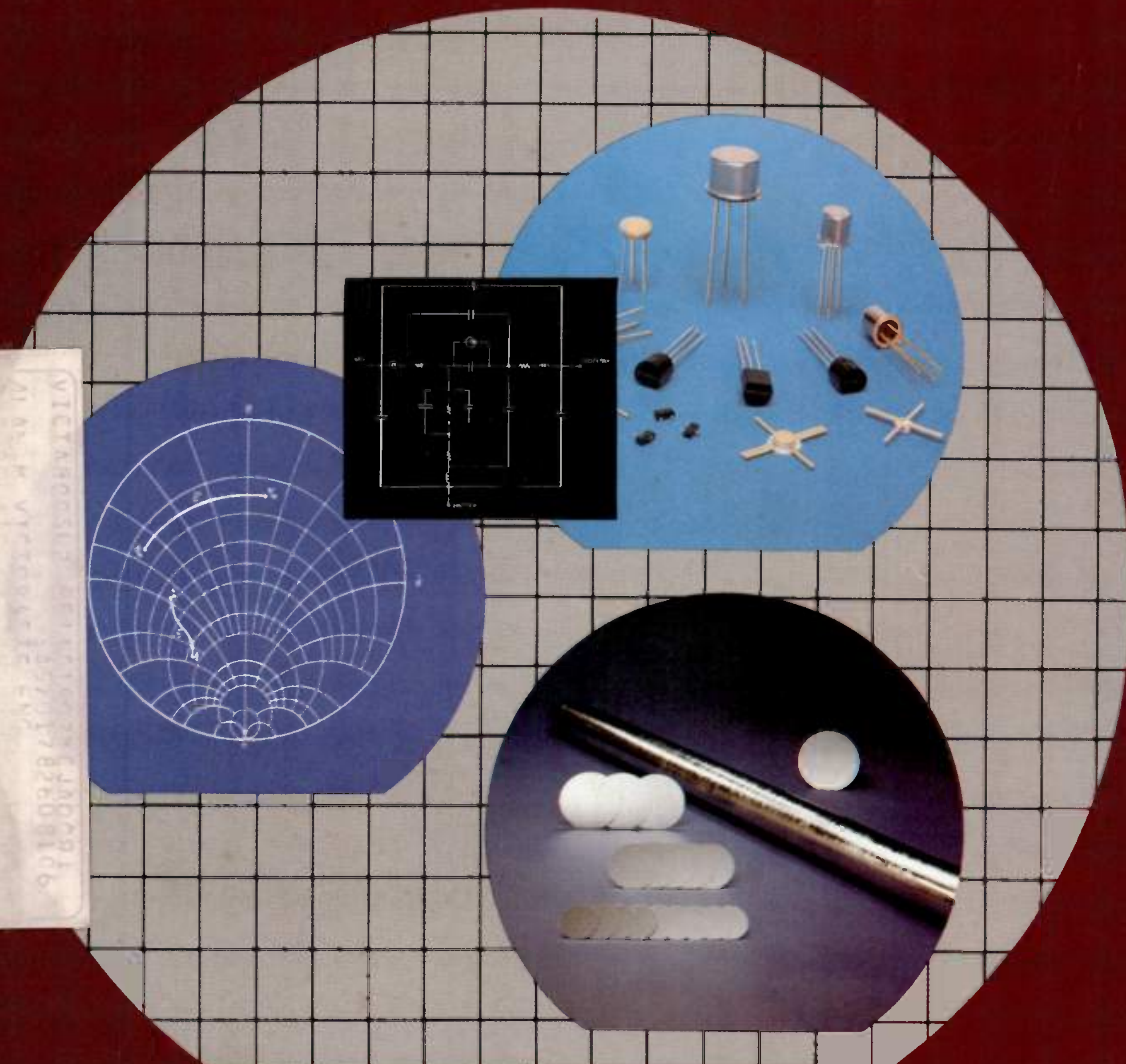

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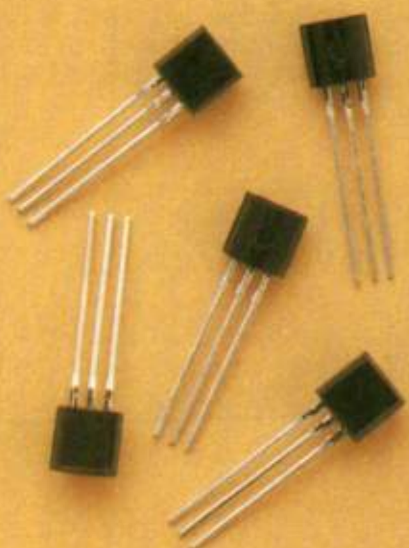

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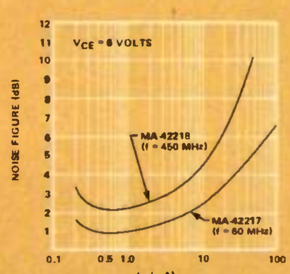
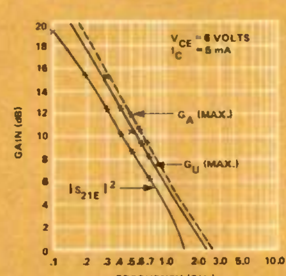
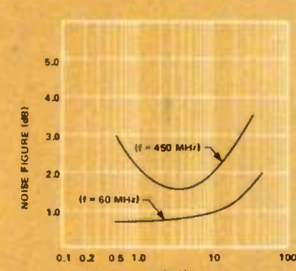


Optimum Noise Figure vs. Collector Current @ 60 and 450 MHz



Gain Parameters vs. Frequency

MA-42217,8 Series



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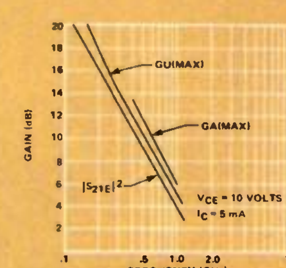

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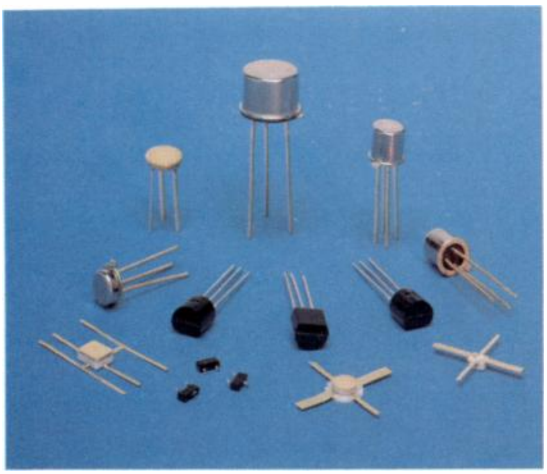

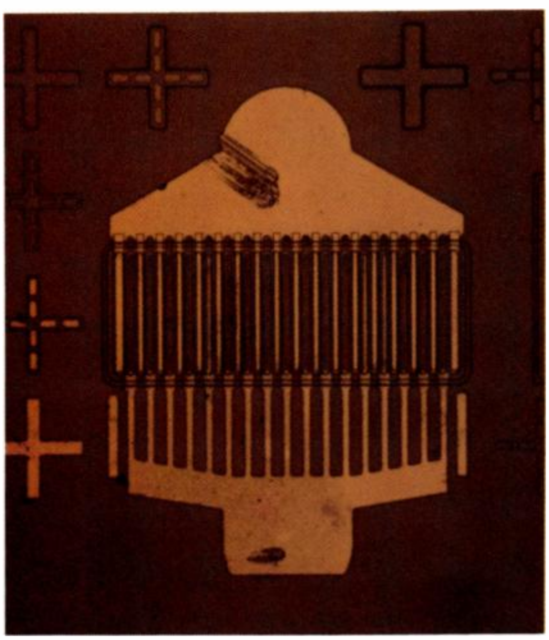

Next Month's Issue—The theme for November/December issue will be "antennas". Look for an issue featuring new antennas and new antenna applications. Also next issue will be part II of our active devices theme.

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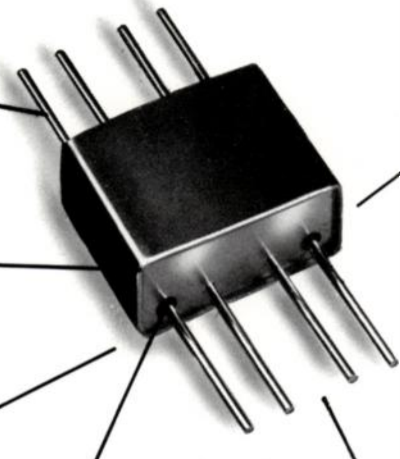

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	LO-IF	35	25
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Alternate Procedure

Editor:

In reading "A Binary Stepped Transmission Line" in the July/August 1982 issue of "R.F. Design" magazine, I came across an HP-25 program to calculate VSWR from load and characteristic impedances. Although the program appears to calculate the VSWR, it does so with a great deal more program steps than are necessary. RPN, stack oriented calculators like those made by HP, can carry both the real and imaginary parts of a complex number in the stack. The built-in rectangular-to-polar, and polar-to-rectangular functions make it easy to convert the complex number components to forms for complex multiplication and division (polar form) or complex addition or subtraction (rectangular form). By operating in the complex domain, the 44 step program shown in the article, can be reduced to a 24 step program that not only calculates the VSWR, but also provides the complex reflection coefficient. This new, 24 step program is shown below. The input sequence is nearly like the original article:

For ZL in rectangular form: key in RL followed by ENTER
key in XL followed by R/S, VSWR returned.

For ZL in polar form: key in <ZL followed by ENTER
key in |ZL|
execute P→R
execute X<>Y followed by R/S, VSWR returned.

STEP	KEYSTROKES
1	STO 2
2	X<>Y
3	STO 1
4	RCL 0
5	—
6	→P
7	STO 3
8	X<>Y
9	STO 4
10	RCL 2
11	RCL 1
12	RCL 0
13	+
14	→P
15	STO/3; |Γ|
16	X<>Y
17	STO-4; <Γ
18	RCL 3
19	1
20	+
21	RCL 3
22	1
23	—
24	/ ; VSWR

The register assignments are the same as in the referenced program:

RO Zo (actually Re(Zo))
R1 Re(ZL)
R2 Im (ZL)
R3 |Γ|
R4 <Γ

This same technique of treating both parts of a complex number in the stack has application beyond the calculation of VSWR. It makes network analysis and Smith Chart type calculations very easy to do on a handheld calculator.

Bruce K. Murdock
Staff Consultant
Delco Electronics

9th Grade Algebra

Dear Editor:

I like your magazine. More than half your articles are of interest to me and relate to work I do, but———

I distinctly feel that as printed, your articles contain more than a reasonable number of errors. I suspect many of these are due to typesetting. As one example, in the May/June 1982 issue, p. 25 equations (14) and (15) read:

$$X_2 = (X_6 + X_2) - X_6$$
$$X_4 = (X_7 + X_4) - X_7$$

Since by 9th grade algebra, these reduce to $X_2 = X_2$ and $X_4 = X_4$, which may be absolutely correct but of little use, I suspect some subscripts are mixed up.

Keeping equations, subscripts and symbols consistent and correct requires care by the author and as well as care in typesetting. Does your pro-

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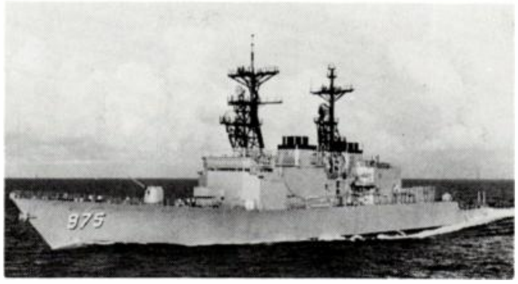

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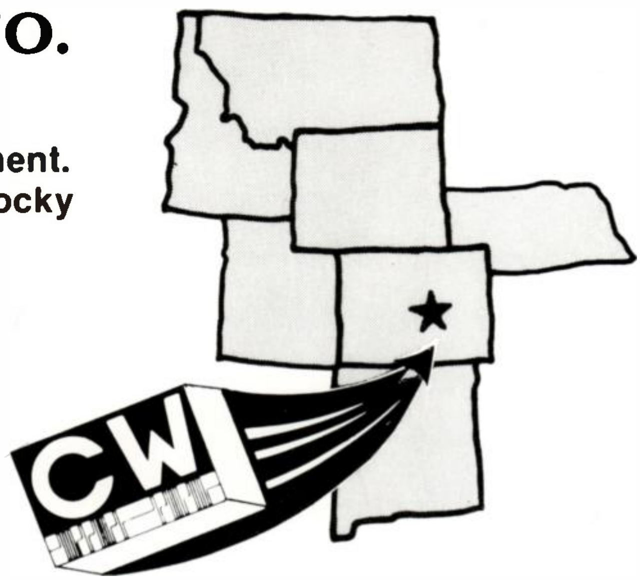

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INFO/CARD 6

cess include a chance for the authors to have a "galley print" review—or at least a review by a technical editor?

J.W. Streater
Manager, Engineering
Mentor Radio Co.

Dear Mr. Streater:

I am glad to see that some people actually read all the equations. Yes, 9th grade algebra still applies! You are correct in stating that equations (14) and (15) are actually identities, and they were meant to be. Since this was a short article, I did not want to use additional equations and subscripts. You will notice that the quantity (X_6 + X_2) is defined by equation (10) and X_6 by equation (3). Thus subtracting (3) from (10) gives X_2, as stated in equation (14) and paragraph c.

I am sorry that the short cut caused some confusion. The program (and the circuit) has been used successfully mainly in IF amplifiers.

Thanks again for the comments.

Andrzej B. Przedpelski
Vice President, Development
A.R.F. Products, Inc.

TRS-80 Tuned Circuit Program

Dear Editor:

Referring to Andrzej Przedpelski's article on designing low impedance doubled-tuned circuits with the aid of an HP-41C/CV program, here is a listing for the TRS-80 that will calculate the values of the five capacitors. The program is not elegant or refined—strictly utilitarian. Nor does it plot the frequency response. The program may be rerun with a changed value by entering a variable assignment statement, then GOTO 85. For example, after solving for a set of conditions that included a coil Q of 100, type in:

QL = 150 (Enter)
GOTO = 85 (Enter)

and new values will be presented for a coil Q of 150.

Capacitor reactances are printed as positive rather than negative.

Readers that have access to a TRS-80, but not an HP-41C or CV, may be interested.

J.W. Streater
Manager, Engineering
Mentor Radio Co.

```
10  CLS: PRINT TAB(12) "DOUBLE TUNED COUPLING CIRCUIT DE-
    SIGN": PRINT
20  PRINT "ENTER SOURCE RESISTANCE (RS) AND LOAD RESIST-
    ANCE (RO)."
30  INPUT "RS = "; RS: INPUT "RO = "; RO
40  PRINT "ENTER LOWER AND UPPER 3 DB FREQUENCIES (F1
    AND F2)."
50  INPUT "F1 = "; F1: INPUT "F2 = "; F2
70  PRINT "ENTER INDUCTOR (L) VALUE IN HENRYS. BOTH IN-
    DUCTORS HAVE"
75  PRINT "SAME VALUES."
80  INPUT "L = "; L
82  INPUT "QL = "; QL
85  F0 = SQR(F1*F2): PRINT "GEOMETRIC MEAN CENTER FRE-
    QUENCY F0 = "; F0
90  XL = 6.28319*F0*L: PRINT "XL = "; "OHMS"
100 Q0 = F0/(.7*(F2-F1)): PRINT "Q0 IS"; Q0
110 X3 = XL*Q0
120 XT = X3/(Q0 - 1)
150 RL = QL*XL: PRINT "EQUIVALENT INDUCTOR SHUNT RESIST-
    TOR RL = "; RL
160 RT = (Q0*XL*RL)/RL - Q0*XL)
180 R1 = RT/(1 + RT*RT/XT/XT)
200 X1 = SQR(R1*RS*RS/(RS - R1))
220 X5 = SQR(R1*RO*RO/(RO - R1))
240 X6 = RS*RS/X1/(1 + RS*RS/X1/X1)
260 QT = RT/XT:X2 = - X6 + XT*QT*QT/(1 + QT*QT)
280 X7 = RO*RO/X5/(1 + RO*RO/X5/X5)
290 X4 = X6 + X2 - X7
310 PRINT
320 PRINT "X3 = "; X3; TAB(20); 1/(6.28319* F0*X3); "FARADS"
330 PRINT "X1 = "; X1; TAB(20); 1/(6.28319* F0*X1); "FARADS"
340 PRINT "X5 = "; X5; TAB(20); 1/(6.28319* F0*X5); "FARADS"
350 PRINT "X2 = "; X2; TAB(20); 1/(6.28319* F0*X2); "FARADS"
360 PRINT "X4 = "; X4; TAB(20); 1/(6.28319* F0*X4); "FARADS"
400 END
```

TRS-80 Program.

SLICING S-PARAMETERS

By R. Brand and P. Ledger
M/A-COM Silicon Products, Inc.
Burlington, MA 01803

How meaningful are your discussions with the transistor supplier when tight S-parameter tolerances are needed? Can you relate physical elements of the semiconductor to model elements or S-parameter behavior?

Circuit designers using S-parameters in low-noise bipolar transistor amplifier design often impose tight S-parameter tolerances on the transistor supplier so as to minimize circuit tuning during amplifier assembly. Wide-spread use of computer-aided circuit design (CAD) and automatic S-parameter measurements, coupled with prior work on modeling bipolar transistors, enable rapid determination of the critical elements required of a transistor such that it would work in a given application. Could you, given only the transistor, obtain such a model and use it both to design the amplifier and communicate your needs to the transistor supplier?

This article deals with a simple lumped element model of a state-of-the-art UHF/VHF silicon (MA42141-511) low-noise bipolar transistor chip within a package. Independent of any knowledge of the transistor chip design, we obtain close matching of modeled versus measured S-parameters and tben proceed to show that the critical element values obtained are consistent with values obtained by other methods. The calculations are presented in the form of an example such that an entrant electrical engineer not familiar with transistor design methods could quickly become comfortable in using these devices in his first low-noise amplifier project, as well as effectively communicating his requirements to the transistor supplier.

We have chosen a model which has almost a one-to-one correspondence with the physical properties of the chip, given the program and final element values used in the modeling exercise. We have also included a simple description of the transistor chip structure which concentrates on its electrical properties rather than its semiconductor processing schedule.

Transistor Chip and Circuit Model

The common emitter T-equivalent model[1] is shown in Figure 1. The part corresponding to the transistor chip is embraced by dotted lines. The exterior elements are associ-

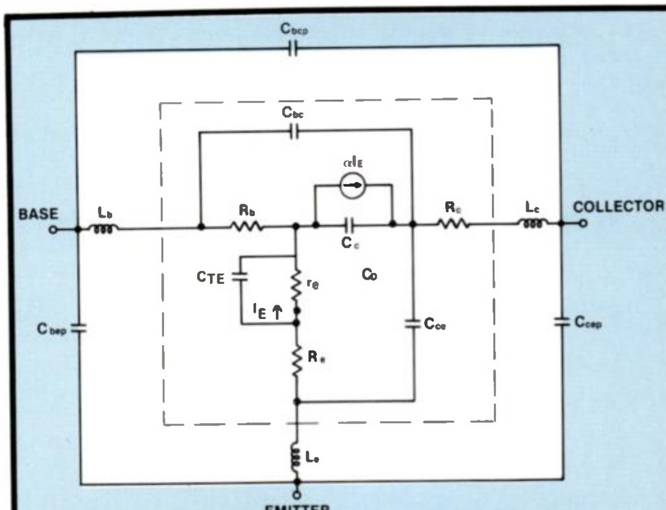

Figure 1. Equivalent Circuit used to Model S-Parameters.

ated with the package which is a stripline ceramic hermetically sealed package (see Figure 2). Figure 3 shows the simplest physical chip structure in which a block of silicon has been suitably doped to create emitter, base and collector regions with wires attached to provide connection. To help the modeling process, it is useful to relate the model elements (Figure 1) to their physical location within the silicon chip (Figure 3). The base resistance, R_b, includes the contact resistance of the wire to the base (shaded dot) as well as the resistance of the P-type base region itself. The emitter transition capacitance, C_{TE}, is determined by the product of the emitter area, ABCD, and the capacitance per unit area of the emitter-base junction. The emitter resistance, r_e, depends only on the emitter-base forward bias current and is given by:

$$r_e = \frac{25.4}{I_E} \text{ ohms} \qquad (1)$$

where I_E is the emitter current in milliamperes. R_e is the emitter—metal contact resistance (ABCD shaded). R_c is the collector series resistance determined by the addition of the resistance of the N+ collector region and the collector-metal contact (EFGH). The capacitance, C_c, does not have any physical relation to the structure depicted in Figure 3, and was adjusted in value only to obtain the correct S-parameters. It can be calculated[1] from a detailed knowledge of the base structure, but this information is not generally available to the circuit designer. Finally the common base current gain, α, used in the generator αI_E, is approximated by the single-pole expression[1]:

$$\alpha = \frac{\alpha_o}{1 + j\frac{f}{f_b}} \exp\left[-\, j\, 2\pi f \tau\right] \qquad (2)$$

where τ is the collector depletion delay time (time for electrons to travel across the N-collector region), f_b is the base cut-off frequency which is determined by the time, τ_b, for electrons to diffuse across the P-type base region and α_o is the common base d.c. current gain.

τ can be calculated for a saturation drift velocity, V_{SL}, of 8.5×10^{-6} centimeters per second, from:

$$\tau = \frac{W}{2 V_{SL}} = \frac{2 \times 10^{-4}\text{cm}}{2 \times 8.5 \times 10^{-6}} = 11.7 \text{ picoseconds} \qquad (3)$$

where W is the width of the N-collector region.

Such a transistor structure would be ideal, but it is physically too small to make the electrical connections as shown. In order to achieve the performance of the transistor under discussion, the unit cell in Figure 3 measures 0.078 mils (AB) × 0.8 mil (BC) × 4.0 mils (DE). This represents a volume barely visible to the naked eye for which 17,000 would pass simultaneously through the eye of a typical household needle. To circumvent the physical size limitation of the unit cell in Figure 3, the base contacts are brought to the same surface as the emitter by the addition of additional silicon [see Figure 4(a)]. Such a move, however, penalizes performance. The C_{TE} increases because of the increase in emitter area DI and DC [Figure 4(b)]. This reduces the achievable low current gain. The base resistance, R_b, increases because of the additional resistance paths R_b' [Figure

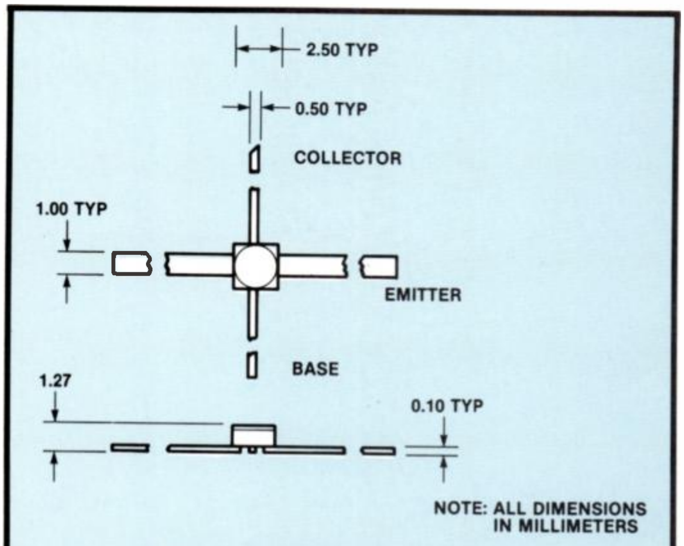

Figure 2. ODS-511 Package.

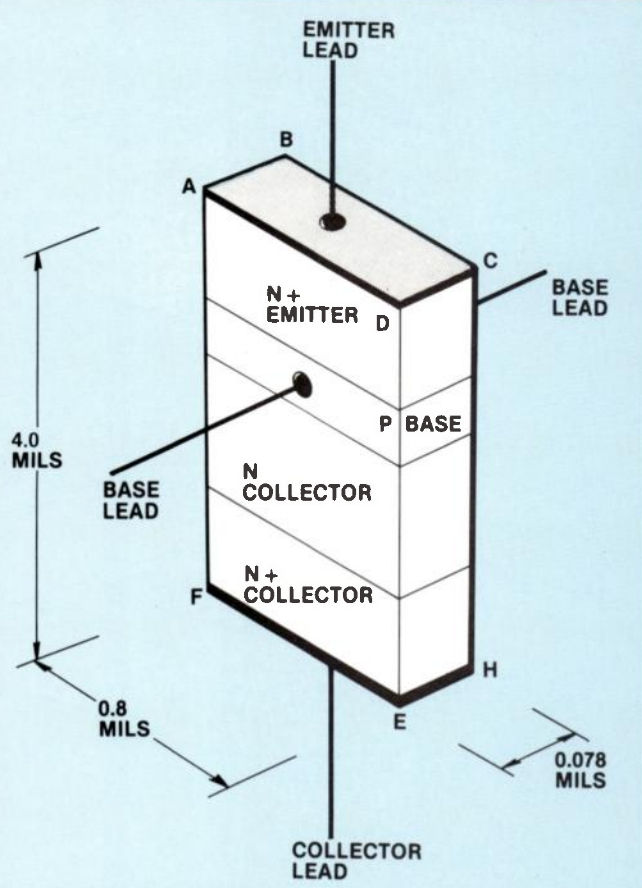

Figure 3. Basic Transistor Structure.

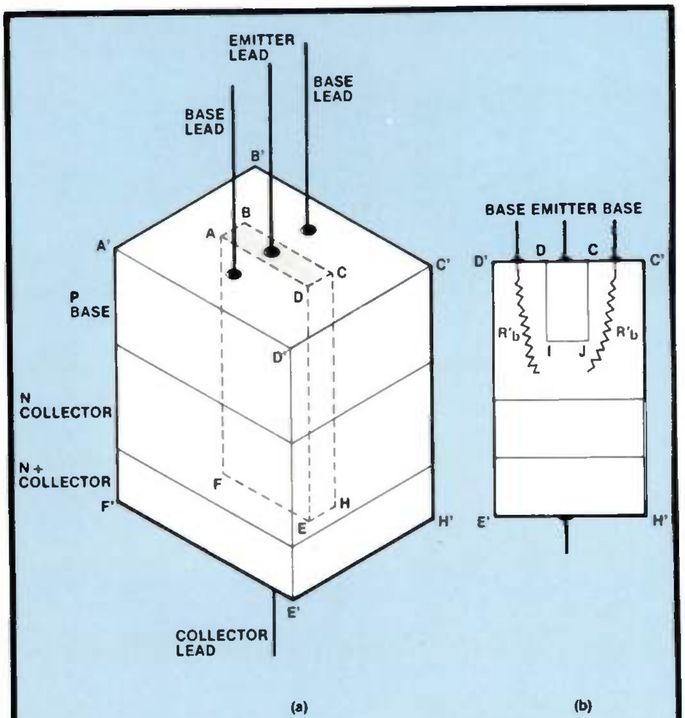

Figure 4. Base Connections Brought to same Surface as Emitter to give "Planar" Construction.

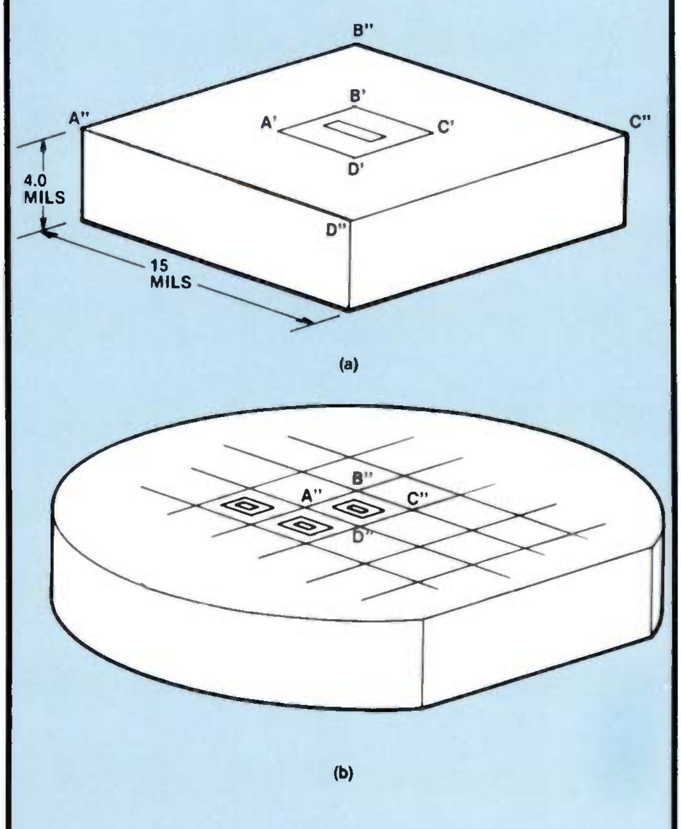

Figure 5. Final Silicon Chip Size and its Placement in the Wafer.

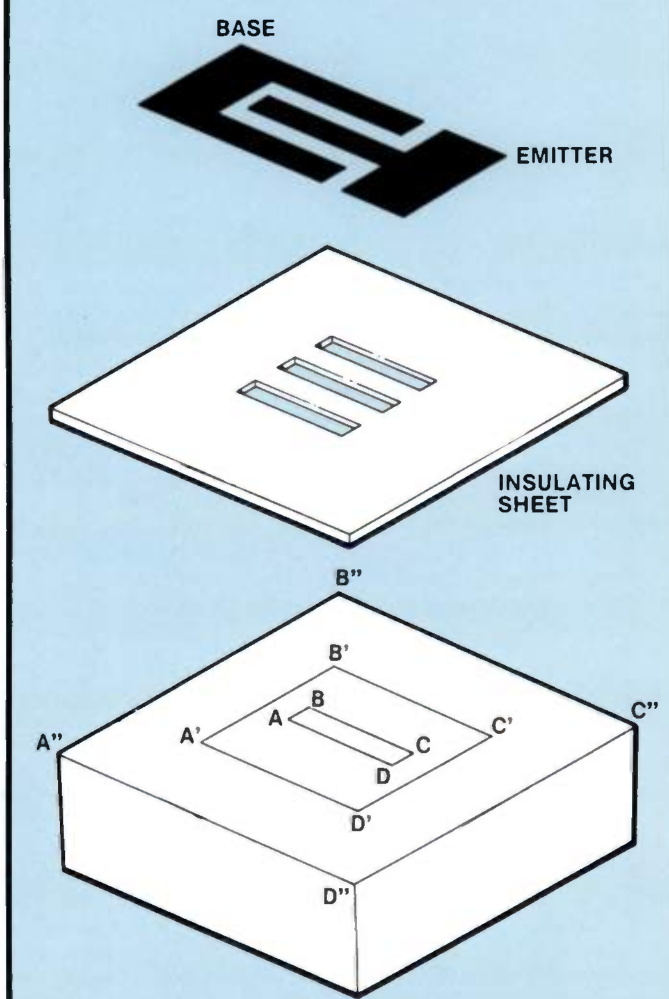

Figure 6. Addition of Metal Contact pads for Bonding Wire to Emitter and Base.

4(b)] degrading noise figure. Finally collector area has increased (to E′F′G′H′), which increases C_C further reducing gain. The "planar" construction of Figure 4 still lacks adequate physical size (it measures 0.23 mil × 0.8 mil × 4.0 mils) and lacks a practical method for attaching wires to the base and emitter regions. Additional silicon to cure the size problem can be made without further degradation of performance as shown in Figure 5(a). The silicon chip size shown in Figure 5(a) is 4.0 × 15 × 15 mils, more than adequate to hold while attaching wires to the chip or bonding wires or chips to packages. These chips can be positioned in a silicon wafer as shown in Figure 5(b). Since the transistor geometry is confined to one plane, they can be replicated by the thousands using standard semiconductor processing techniques.

To solve the problem of attaching wires to the emitter and base regions, metal patterns are fabricated consisting of thin fingers designed to connect to the critical regions, which in turn are attached to expanded metal areas large enough that 0.7 mil diameter gold wire can be thermocompression bonded to them. However, as illustrated in Figure 6, a thin insulating sheet, into which has been cut suitable contact holes aligning themselves over the emitter and base regions, must be placed between the expanded metal contacts and the silicon chip in order to prevent shorting of the emitter-base and collector-base junctions by the metal stripes. This insulating sheet, which in practice

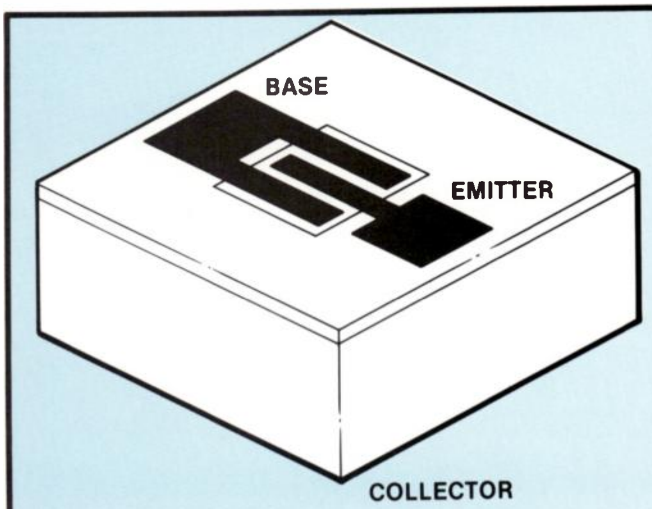

Figure 7. Finished Metalized Bipolar Transistor Chip.

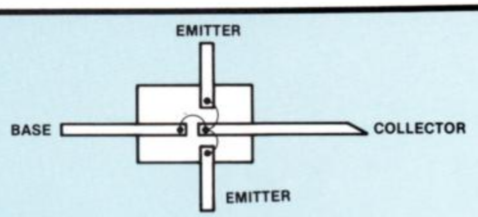

Figure 8. ODS-511 Package Wire Bonded without Chip.

is only 0.2 mils thick, appears naturally as the silicon dioxide layers grown during the semiconductor processing schedule. A consequency of this insulation system however is the creation of additional capacitance between the metal pads and semiconductor body; and these are included in the circuit model as C_{bc} (base to collector pad capacitance) and C_{CE} (emitter to collector pad capacitance). The final transistor chip is shown in Figure 7. Since wires are used to connect the metal pads to the package, they give rise to base inductance, L_b, emitter inductance, L_e, and collector inductance, L_c, which have to be taken into account for accurate prediction of S-parameter variation with frequency. Actually, for the transistor under discussion, 15 unit cells as shown in Figure 3 are connected in parallel in order to reduce the base resistance, R_b, which improves noise figure. However, connecting unit cells in parallel reduces low current gain and the trade-off between these two parameters gives rise to the proliferation of transistor geometries available today, each having its own unique combination of gain, noise figure, and S-parameter characteristics.

S-Parameter Modeling

A commercially available CAD program, COMPACT[2], was used to calculate the S-parameters of Figure 1 over the frequency range 0.4 to 2 GHz. The COMPACT program used is given in Table 3. The purpose of this article is to develop a useful model given only the packaged transistor, access to a network analyzer and a computer, when α_o, the package elements, L_b, L_c, L_e, C_{bep}, C_{cep}, and C_{bcp} were known at the outset. The DC gain, α_o, can be measured using a standard curve tracer. The package element values can usually be obtained from the manufacturer. The most common technique for obtaining them is to measure S-parameters of an

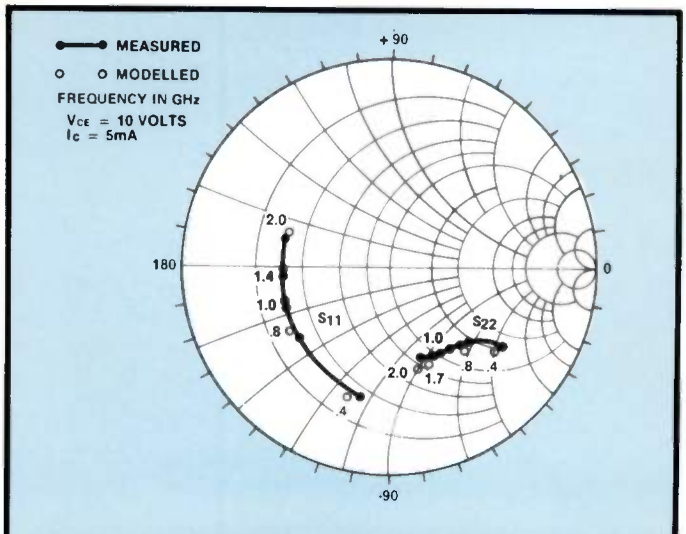

Figure 9. Measured and Modeled S_{11} and S_{22} versus Frequency of Packaged Device.

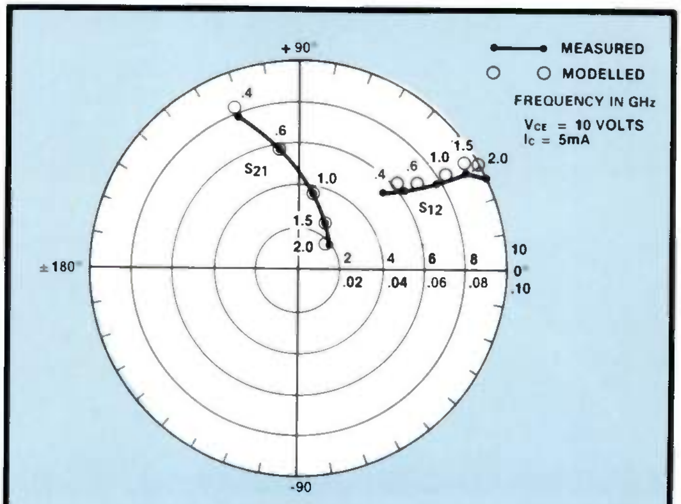

Figure 10. Measured and Modeled S_{21} and S_{12} for Packaged Device.

open package (without wires or chips) and a shorted package where wires are connected from each package lead to the collector lead (Figure 8). By matching modeled versus measured S-parameters over the frequency range of interest, values for the package elements are established. If package elements are not available from the manufacturer they can be established during the modeling exercise of the transistor itself.

S-parameters for a transistor were measured and element values in the chip model were varied until a cost match on all S-parameters over the frequency range of interest was achieved. Measurements were made on a Hewlett-Packard Model 8542A network analyzer using a standard transistor test fixture, Hewlett-Packard Model 11608A. The results are shown in Figures 9 and 10. The final package and chip element values are given in Table 1. In addition, three of the critical circuit elements, C_{TE}, R_b and f_b were obtained independent of the modeling exercise and were found to agree with the model values. C_{TE} can be obtained by plotting the reciprocal of the common emitter cut-off frequency, f_T, against the reciprocal of emitter current, I_E. Theory predicts that:

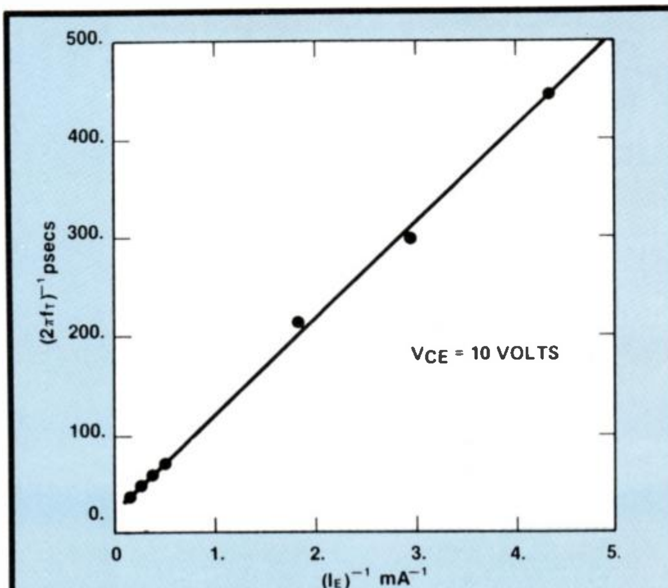

Figure 11. $1/2\pi f_T$ versus $1/I_E$.

$$\frac{1}{2\pi f_T} = \frac{25.4}{I_E} C_{TE} + \tau_b + \tau \quad (4)$$

where I_E is in milliamperes. S-parameters at 1 GHz were measured over a current range of 0.25 to 8 mA and transformed to h-parameters. f_T at each current is given by $h_{21} \times f(f = 1\text{ GHz})$. A plot of $(2\pi f_T)^{-1}$ versus $(I_E)^{-1}$ is shown in Figure 11. The linear relation, as predicted by Equation (4), enables C_{TE} to be derived from the slope and $(\tau_b + \tau)$ from the intercept on the ordinate. The slope, obtained from a best straight-line fit to the measured values was 97.1 mA/psec. The intercept was 23.4 picoseconds, which implies a value for τ_b of 11.7 pico-seconds. f_b can be calculated from $1/2\pi f_b = \tau_b$. A comparison of model values to these measured values is shown in Table 2 and close agreement is found. Finally, optimum noise figure (at a single bias condition of $I_c = 5$ mA and $V_{CE} = 10$ volts) was measured at four fre-

PACKAGE ELEMENT VALUES		CHIP ELEMENT VALUES	
L_b	1.0 nH	r_e	5 ohms
L_c	0.65 nH	C_{TE}	4.0 pF
L_e	0.225 nH	C_{ce}	0.25 pF
C_{bep}	0.2 pF	R_c	5 ohms
C_{bcp}	0.03 pF	R_e	1 ohms
C_{cep}	0.38 pF	R_b	15 ohms
		C_c	0.016 pF
		C_{bc}	0.417 pF
		α_o	0.99
		f_b	10 GHz
		τ	10 psecs

Table 1.

ELEMENT	MODEL	MEASURED
C_{TE}	4.0 pF	3.8 pF
f_b	10 GHz	13.6 GHz

Table 2.

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RES CC SE 5.0	RESISTANCE r_e. SERIES CONNECTED 5 ohms
RES DD SE 1.0	RESISTANCE R_e. SERIES CONNECTED 1 ohm
CAP EE SE 0.250	CAPACITANCE C_{ce}. SERIES CONNECTED 0.25 pF
CAP FF SE 0.016	CAPACITANCE C_c. SERIES CONNECTED 0.016 pF
CAP GG SE 0.417	CAPACITANCE c_{bd}. SERIES CONNECTED 0.417 pF
GEN HH CC .01 1E5 .990 10000 .00001E-6	DEFINES THE GENERATOR
CAP II SE 0.380	CAPACITANCE C_{cap}. SERIES CONNECTED 0.38 pF
SRL JJ SE 5.0 0.65	SERIES CONNECTED R_c, 5.0 ohms. L_c, 0.65 nH
CAP KK SE 0.20	CAPACITANCE C_{bep}. SERIES CONNECTED 0.2 pF
IND LL SE 1.0	INDUCTANCE L_b. SERIES CONNECTED 1.0 nH
IND MM SE 0.225	INDUCTANCE L_e. SERIES CONNECTED 0.225 nH
CAP NN SE 0.03	CAPACITANCE C_{bcp}. SERIES CONNECTED 0.03 pF
CON AA T2 2 3	CONNECTS AA BETWEEN NODES 2, 3
CON BB T2 3 4	CONNECTS BB BETWEEN NODES 3, 4
CON DD T2 5 6	CONNECTS DD BETWEEN NODES 5, 6
CON EE T2 6 7	CONNECTS EE BETWEEN NODES 6, 7
CON FF T2 3 7	CONNECTS FF BETWEEN NODES 3, 7
CON GG T2 2 7	CONNECTS GG BETWEEN NODES 2, 7
CON HH T4 4 5 3 7	CONNECTS HH BETWEEN NODES 4, 5 and 3, 7
CON II T2 8 0	CONNECTS II BETWEEN NODES 8, 0
CON JJ T2 7 8	CONNECTS JJ BETWEEN NODES 7, 8
CON KK T2 1 0	CONNECTS KK BETWEEN NODES 1, 0
CON LL T2 1 2	CONNECTS LL BETWEEN NODES 1, 2
CON MM T2 6 0	CONNECTS MM BETWEEN NODES 6, 0
CON NN T2 1 8	CONNECTS NN BETWEEN NODES 1, 8
DEF AA T2 1 8	DEFINES AA AS NODE 1 TO NODE 8
PRI AA S1 50	PRINTS S-PARAMETERS FOR NODES 1,8
END	
400 2000 100	FREQUENCY RANGE 0.4 GHz to 2 GHz in 100 mHz STEPS
END	

Table 3.

quencies and compared to calculated values (Figure 12). Optimum noise figure, F_{min}, is given by[4]:

$$F_{min} = a\frac{R_B + R_{opt}}{r_e} + \left(1 + \frac{f^2}{f_b^2}\right)\frac{1}{\alpha_o} \quad (5)$$

where the optimum source resistance, R_{opt}, is given by:

$$R_{opt} = \left\{R_B^2 - X^2_{opt} + \left(1 + \frac{f^2}{f_b^2}\right) \times \frac{r_e(2R_B + r_e)}{\alpha_o a}\right\}^{1/2} \quad (6)$$

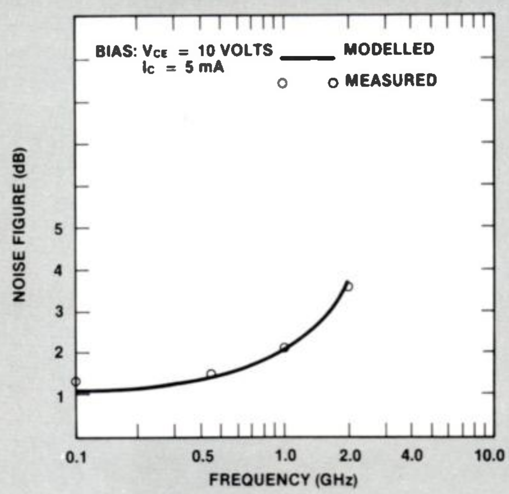

Figure 12. Measured and Modeled Minimum Noise Figure versus Frequency.

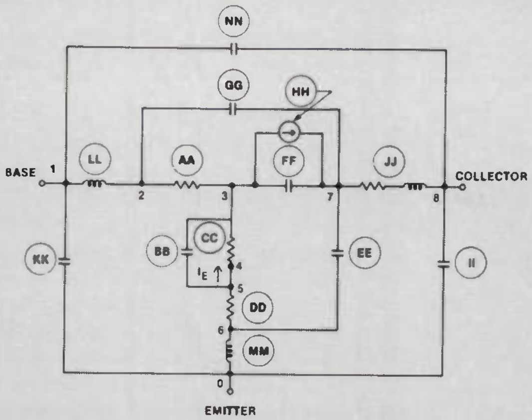

Figure 13. Circuit Model used in Computer Program.

both X_{opt} and a are given by:

$$X_{opt} = \left(1 + \frac{f^2}{f_b^2}\right) \frac{2\pi f\, C_{TE}\, r_e^2}{\alpha_o a} \qquad (7)$$

and

$$a = \left\{ \left(1 + \frac{f^2}{f_b^2}\right)\left(1 + \frac{f^2}{f_e^2}\right) - \alpha_o \right\} \frac{1}{\alpha_o} \qquad (8)$$

where $f_e = 1/2\pi r_e C_{TE}$. Good agreement was obtained between measured and calculated minimum noise figure, as shown in Figure 12, using the values for R_B, f_b and C_{TE} obtained from the modeling exercise.

Conclusion

With the aid of CAD programs and a simple lumped element model, low-noise bipolar transistor S-parameter behavior with frequency can be obtained which closely matches measured values. Models so derived can be used to refine the amplifier design. Furthermore, the model elements correspond to physically relatable elements of the semiconductor so that meaningful discussions with the transistor supplier can prevail when discussing applications requiring tight S-parameter tolerances. The method is flexible enough to accommodate many different package styles.

Acknowledgements

We wish to thank Dr. J.F. White, Technical Director, and Mr. W.R. Rushforth, of the M/A-COM Components Corporate Technology Center, for helpful discussions and guidance in the transistor modeling. Finally, we would like to thank D. Blanchard for preparation of the manuscript.

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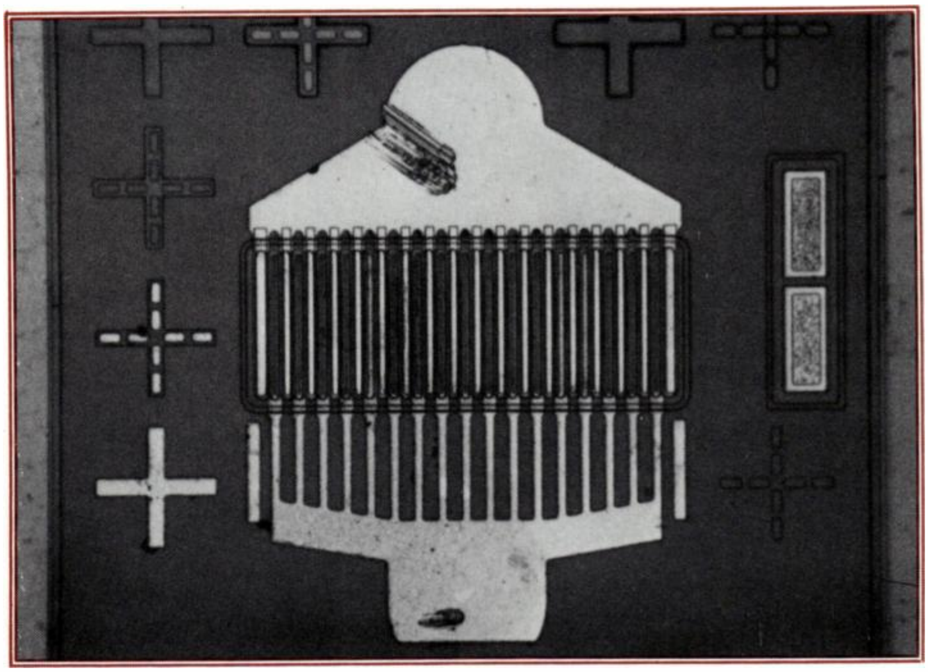
4. R.J. Hawkins, "Limitations of Nielsons and Related Noise Equations Applied to Microwave Bipolar Transistors and a new Expression for the Frequency and Current-Dependent Noise Figure", Solid-State Electronics, 1977, Vol 20, pp 191-196.

A High-Voltage RF Bipolar Transistor

A design account of an RF bipolar transistor developed to fill the need for driver devices in the CRT display section of modern test and measurement equipment.



By Michael D. McCombs
Device Engineering Supervisor and
Chris Nixon,
Device Engineer
TRW Semiconductors
Lawndale, CA 90260

Modern test and measurement equipment often requires cathode ray tube display sections for the presentation of data or test results. Examples are oscilloscopes, spectrum analyzers, network analyzers, and digital logic analyzers. There is an evolving requirement for higher writing speeds in the CRT displays. Driving circuitry for the display must be fast, requiring semiconductor devices capable of higher switching speeds. Higher breakdown voltages in the new electrostatic CRTs are also required. Here we describe a bipolar device which meets these criteria.

In an RF transistor, the requirements for high f_t as well as high break-

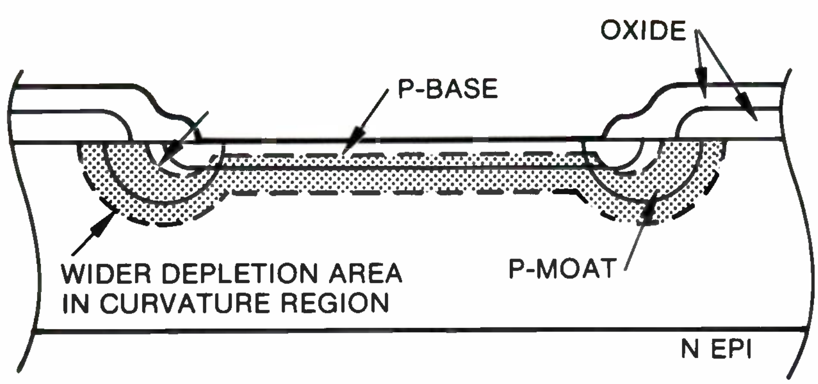


Figure 1. P-Moat Structure.

for CRT Driver Applications

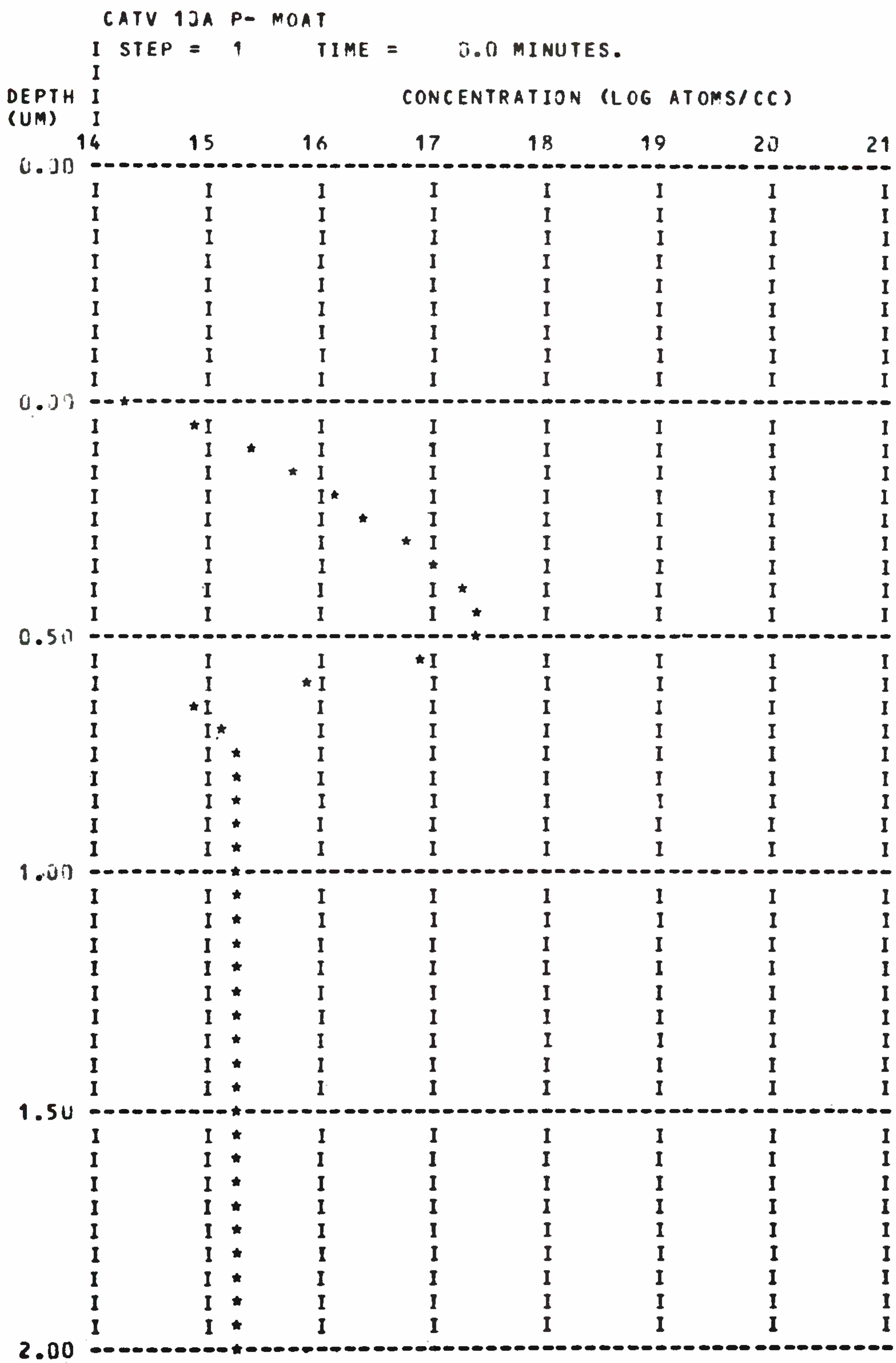


Figure 2. SUPREM Profile of the P-Moat Structure.

down voltages are normally thought of as mutually exclusive. That is, things that improve the voltage capability of the transistor result in a loss of gain-bandwidth or switching speed performance. The device described provides both high f_t and high breakdown voltage. It combines shallow RF bipolar processing with a breakdown-enhancement technique. While production worthy, this processing doesn't add capacitance or use inordinate amounts of epi.

Performance Goals

H_{fe} = 20-50
BV_{CEO} = 60V min
BV_{CBO} = 120V min
$f_t \geq 1.5$Ghz
$C_{OB} \leq 2.5$ pf @ 10V

Fabrication Procedure

One requirement for this transistor was that it be manufacturable and, if possible, use existing mask sets and processes. Because of the requirement for high-breakdown voltages, it was necessary to obtain an epitaxial starting material with higher resistivity and thickness than typical materials used in RF power or linear applications. To allow for the predictable epitaxial depletion at target voltages, an epi material 9-10μm thick with a resistivity of 3 Ω cm was selected. The substrate was heavily doped with antimony to a level of .01 Ω cm. This type of silicon epitaxy is easily grown and is readily available from several vendors.

The mask set selected had been designed at TRW several years ago to build discrete RF transistors for the CATV marketplace and military communications applications. The mask is a basic interdigitated design. Selection was based on its relative ease of use in production. The mask uses no emitter ballasting and takes advantage of relatively "loose" 5μm contact geometry. This makes it an extremely production-worthy mask set.

Fabrication proceeds in a straightforward manner. There are no processing "tricks." The most difficult part of the target specifications to achieve is the BV_{CBO} goal of 120V. A typical RF base process would require epi of such a high value of resistivity that the gain-bandwidth target could never be achieved. Some type of breakdown enhancement is required. We selected the P-moat process, perfected for microwave power devices requiring relatively high breakdown voltages. Low resistivity epi was previously used for higher saturated power output capability. In this case, high resistivity epi was selected because of the high BV_{CEO} requirement of the part. The moat provides a correspondingly high BV_{CBO}.

Figure 1 illustrates the principle of operation of the P-moat. Essentially, the higher breakdown is achieved by defeating curvature breakdown of the junction. This is accomplished by providing a very lightly doped p region around the edge of the base. This allows more depletion. Therefore, higher voltages are supported. Our experience shows that this process provides breakdowns of over 90% of bulk, if done correctly. In contrast, the more conventional P+ moats or depletion rings do well to give 50% of bulk.

To develop the P-moat process for this application, it was decided to model the process first. The Stanford modeling program, SUPREM, was used. This one-dimensional process modeling program accepts inputs in the form of oxidation and diffusion and ion implantation schedules. Figure 2 shows the output of a SUPREM profile for the P-moat structure used on the device. It can be seen that SUPREM predicts a junction depth of 0.86μm and a peak doping concentration of a little over 1×10^{17}cm/cm^3. The predicted sheet is 3700Ω/□. This compares very well with the experimental results described below.

Figure 3 is a schematic representation of the fabrication process. Figure 3(a) shows the formation of the P-moat by ion implantation. The moat must be deep enough to allow depletion toward the surface. This is accomplished with a 150 kev, 5×10^{12}a/cm^2 boron implant followed by an anneal cycle of 90 min @ 1100°C. Sheet resistance readings of 4000 Ω/□ and a junction depth of 1.0μm are obtained.

In Figure 3(b), the base structure is shown. We selected a base and emitter structure developed for TRW microwave power devices. It results in nearly 2GHz f_t performance on this chip. The base is a standard diffused process.

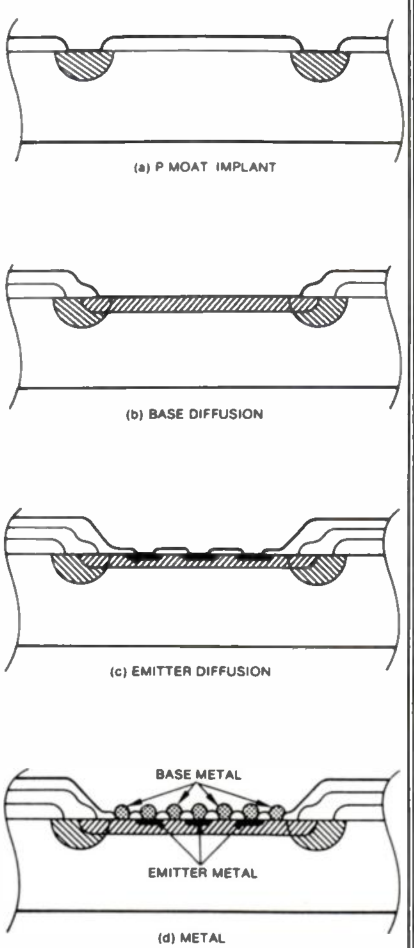


Figure 3. Wafer Fabrication Process.

BN source wafers and a 900°C deposition cycle are followed by a 1025°C diffusion cycle. The result is a base with a junction depth of .25μm and a sheet resistance before emitter of 650 Ω/□.

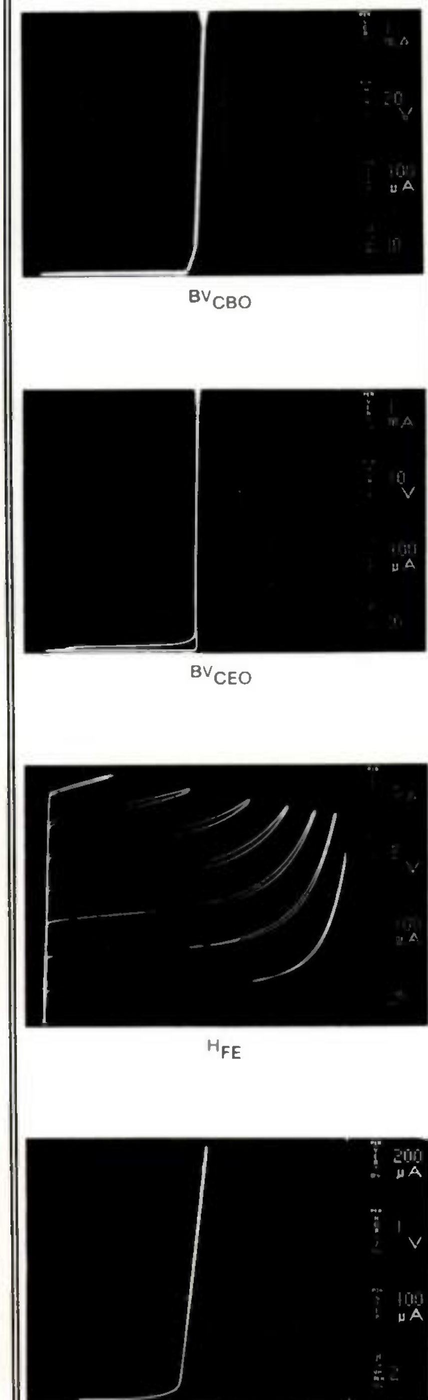
Figure 3(c) shows formation of the self-aligned contact scheme using LPCVD silicon nitride as a mask. Before nitride deposition, a thin layer of thermal oxide is grown. This relieves the stress created between the nitride and the silicon. The contact scheme is interdigitated with an emitter width of 1.8μm, a base contact width of 6.3μm, and a contact spacing of 2.3μm.

Figure 3(d) illustrates the emitter diffusion—a standard phosphorous diffusion using $POC1_3$ as a source. Emitter sheet resistance is approximately 30 Ω/□, with a final base and emitter junction depth of .5μm and .25μm, respectively.

The metalization scheme uses a PtSi ohmic contact. This is followed by a Ti/W barrier with a sputtered gold final metal, which is then defined by PR and etched back. All PR uses contact technology with iron oxide working plates. The devices are passivated with Silox as a scratch protection.

Characterization

The DC characteristics of the transistors are shown in Figure 4. The breakdown goals were met, even though more margin would be desirable. The beta characteristic shows a typical value of 30, which is well within the original objective. Of course,



BV_{CBO} BV_{CEO} H_{FE} BV_{EBO}

Figure 4. DC Characteristics.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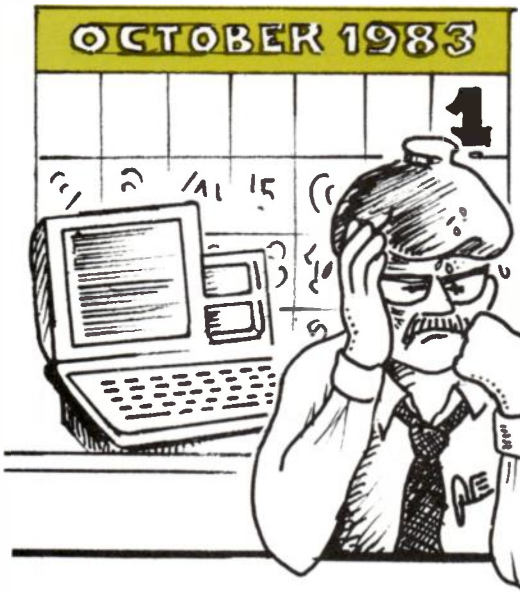

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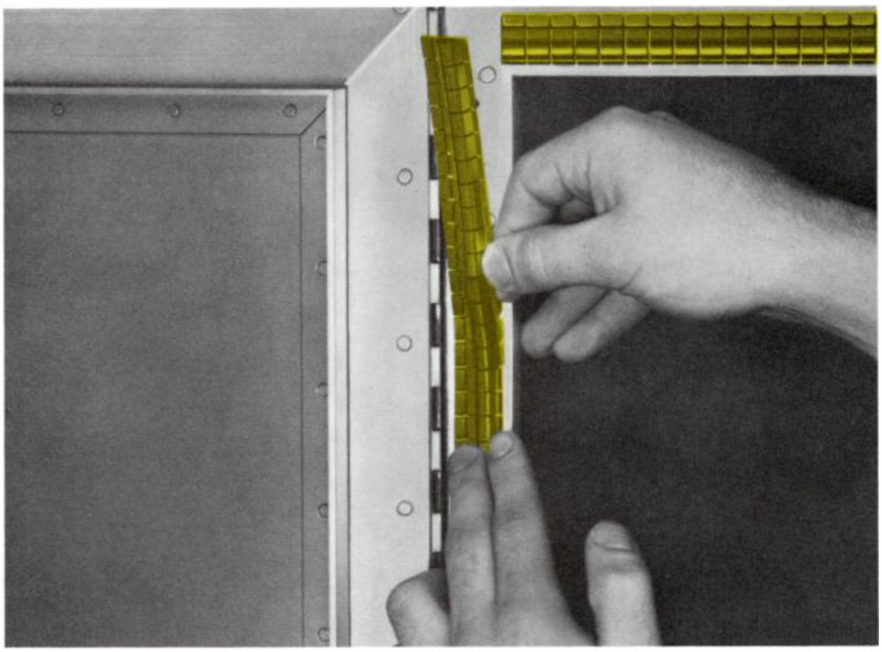

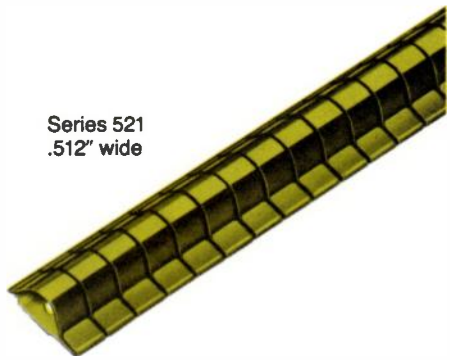

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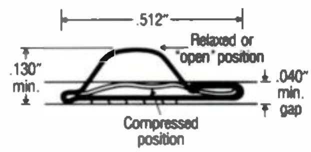

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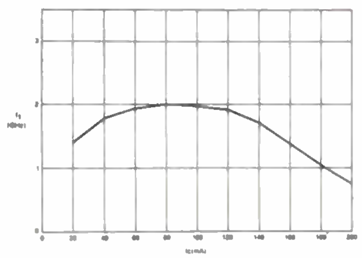

Figure 5. Gain Bandwidth.

targeting the devices for higher beta would require a sacrifice in BV_{CEO} without modifying the starting material.

The f_t vs I_c data (Figure 5) shows that the microwave process is yielding a f_t of nearly 2GHz. This is excellent for high-resistivity epitaxial material. The plot peaks out at 90 ma. The device should be operated at this level for maximum gain.

The inherent f_t performance of the vertical geometry is about 3GHz. Normally, base transit time can be a significant delay contributor in a bipolar device. In this case, a base width of 0.25 m contributes only about 15% of the total. The primary contributors are the emitter delay and the collector-base depletion transit time. To achieve the high BV_{CEO} breakdown voltage, we increase the collector-base transit time by 90%. The f_t value of 2GHz is lower than the theoretical level of 3GHz for this reason.

Summary

We have described a device that fills a void in present RF device technology. The design was undertaken with an emphasis on manufacturability. The horizontal geometry is 'loose' by present high frequency standards, and doesn't require any photolithographical tricks to achieve the performance goals. The vertical geometry is certainly shallow—.5μm—but takes advantage of a proven TRW RF technology. The metalization scheme is all gold. This offers high reliability and the option for compatibility with thin or thick film hybrid technology. Work is continuing on more devices of this type that will attain even higher performance capability.

Acknowledgements

We are grateful to Gene Brannock, Product Engineering Manager/Linear Low Noise, for device characterization and Bill Imhauser, Engineering Supervisor, for discussions on P-moat processing. □

Part I

Power FETs for RF Amplifiers

New power FETs with impressive electrical ratings finally rival not only bipolar power semiconductors but also the time-honored power vacuum tube— especially in military communications equipment where reliability and performance cannot be compromised.

By Gary Appel, Applications Engineer, and
Jim Gong, Product Manager
Siliconix, Inc.
Santa Clara, California

Motivated by the inherent and distinctly superior thermal and noise characteristics of field-effect transistors (FETs) over bipolar junction transistors (BJTs), FET suppliers have steadily optimized device performance specifically for application in high-power communications equipment. This trend is evident in the evolution of RF power FET technology summarized in Table 1, which is marked by periodic improvements in power-handling capability at high frequencies.

Recently reported developments are a laboratory demonstration of an RF power FET delivering 100W at an operating frequency of 1GHz (Semiconductor Research Institute of Japan) and a commercially available device introduced this year that has a 150W rating at 100MHz. This latter device, the Siliconix DVD150T, also has the highest supply voltage (80 to 120V) and drain-to-source breakdown voltage (260V, typical) ratings yet available.

Many RF power FETs are already used in high-power, broadband VHF military communications amplifiers, such as the ECCM frequency-hopping SINCGARS (Single Channel Ground/Airborne Radio Subsystems). With performance on a par with that of power vacuum tubes, FETs bring the potential benefits of reduced system size, weight and cost plus the physical ruggedness necessary for service in hostile military environments.

This article, the first of a two-part series, compares MOSFET and BJT performance characteristics in RF power applications. The second article details procedures for designing a broadband amplifier using RF power FETs.

Advantages of MOSPOWER FETs

RF MOS power FETs, now commercially available from at least six major semiconductor manufacturers, are used increasingly in the design of RF power amplifiers. Growing preference for MOSFETs over traditional bipolar transistors is based on the many advantages offered by the RF power MOSFET.

Inherent Thermal Stability: The current gain (beta) of a typical bipolar power transistor increases with temperature. This positive temperature coefficient is responsible for the occurence of "thermal runaway" in a bipolar amplifier. In contrast, the transconductance of a power FET has a negative temperature coefficient: An increase in device temperature decreases transconductance. As a result, a power FET tends to shut down as device temperature increases.

This characteristic is most easily observed on the device level, however, it also occurs across the transistor die; hotter portions of the die tend to shut themselves down. The overall result is the prevention of destructive phenomena characteristic of bipolar devices: current hogging, hot-spotting and second breakdown. Also, no source ballasting resistors are required with their inherent gain reduction, increased parasitic capacitance, and increased fabrication costs. Moreover, several power FETs can be connected in parallel without the added expense of meticulous selection to match device parameters.

Low Noise: One of the most serious challenges in designing an RF power amplifier is the avoidance of spurious signal generation, which can result either from inadvertant generation of undesired mixing products or simply from the presence of broadband noise.

The transfer characteristic for a typical power FET displays no abrupt changes in shape, but instead varies slowly and smoothly with gate-to-source voltage (see Characteristics of the DVD150T). A power series expansion of this transfer characteristic would yield small values for the higher-order coefficients. This property, which is attributed to the square-law variation of drain current at low gate voltage, results in less generation of high-order intermodulation products than that of a similar bipolar transistor biased under Class AB conditions. Similarly, drain characteristics coupled with the high value of reverse isolation (−35dB) result in excellent back-intermodulation characteristics which is ideal for co-site and combat environments.

A power FET also generates far less broadband noise, typically 10 to 15dB better than a comparable bipolar transistor. Reduced noise generation is due partially to the absence of a forward-biased junction and its associated shot noise. The low noise generation of RF power FETs together with the benefits of reduced levels of high-order intermodulation and back-intermodulation distortion products lead to an increased dynamic range. Finally, ultralinear amplification is possible by employing Class A operation in combination with feed-forward techniques.

Reduced Feedback: Yet another advantage of power FETs is a reduction in the internal feedback paths. High gate impedance results in a gate waveform with amplitudes as high as 20V peak-to-peak. In contrast, the base of a typical bipolar transistor is unlikely to reach 5V peak-to-peak.

The higher gate voltage has two benefits. First, the voltage induced across the common lead (source) inductance affects the FET input voltage about one-fourth as much as it does the input voltage of the bipolar transistor, substantially reducing the unwanted feedback. Second, the effect of reverse transfer capacitance, already low in the power FET, is further reduced by the lower voltage gain. The end result is reduced Miller effect of the FET amplifier. Gain degeneration and slope are reduced due to the reduced common-lead feedback, while stability and input VSWR are less affected by load VSWR.

Circuit Design Simplicity: The unique properties of a power FET can contribute to simplified amplifier circuit design. The negative temperature coefficient allows the use of a fixed bias voltage in Class A and AB operation. No complex temperature compensation is required. Small leakage current, which is in the nanoampere or even picoampere range, results in virtually no power consumption in the gate bias supply. Consequently, a low-power bias supply can be used. Moreover, low gate current allows the power FET to have narrower gate metalization and thus reduced input capacitance.

Another circuit simplification results in the input matching network of a broadband amplifier design. The power FET gate, essentially a MOS capacitor, must be externally shunted by a resistor to properly terminate the input matching network. This combination results in the well-behaved input VSWR and flat gain response of the matching network used. No feedback or frequency compensation is required to control the input impedance or flatten the gain response. The higher input impedance of the power FET simplifies the design of matching networks.

The capacitive input of the device is an attractive feature for distributed amplifier applications. These circuits traditionally are designed around vacuum tubes whose capacitances are integrated with other circuit components. Power FET input capacitance can be exploited in the same manner.

Finally, the absence of minority-carrier storage time in power FETs is ideal for high efficiency amplification or applications with critical phase-tracking requirements.

Reliability: Many of the previously discussed power FET properties increase device reliability. For example, the negative MOSFET temperature coefficient prevents thermal runaway, and minimal internal feedback paths lessen the chance of destructive oscillation. Device reliability is further enhanced by the reduced gate current, which results in less metal migration. Then because input impedance is high, internal impedance-matching components are not required, thus further preserving reliability. Power FET reliability is further enhanced by the lack of a reverse diode breakdown possibility (base-emitter) and its associated degradation in gain (McDonald effect).

High Operating Voltage: Additional advantages become apparent in the design of a high-power amplifier when operating voltage is increased. As the supply voltage is doubled, the current demand is halved and impedance levels increase fourfold. Increased impedance results in several significant benefits.

One improvement is the reduced effect of parasitic inductance elements, especially the common-lead inductance. The inductive elements in the matching network now be-

	FET	BIPOLAR
1968	-DMOS by Bell Laboratory -Planar, 5W @ 10MHz by ECOM (Signal Corps Electronic Command at Ft. Monmouth)	-80W @ 30MHz, 28V -20W @ 400MHz, 28V - 2W @ 3.0GHz, 28V
1969	-VMOS concept reported in *Electronics* by Japan	-30W @ 400MHz, 28V
1972	-VMOS, 10W @ 1.5GHz by Office of Naval Research with Westinghouse R & D center	-50W @ 400MHz, 28V -Internal matched.
1973	-MOSFET, 10W @ 200MHz (KP901A) by Russian	-80W @ 175MHz, 28V -70W @ 30MHz, 12V
1975	-VMOS, 10W @ 200MHz (VMP1) by Siliconix, U.S.A.	-100W @ 30MHz, 12V -100W @ 400MHz, 28V
1976	-VMOS, 10W @ 200MHz (VMP4), first commercial RF VMOST	-100W @175MHz, 28V -Balance Transistors.
1978	-VMOS, 100W @ 175MHz, 35V (BF100-35) by CTC, U.S.A.	-20W @ 2.0GHz, 22V
1980	-VMOS, 80W @ 175MHz, 28V (DV2880T) by Siliconix, U.S.A.	-16W @ 2.3GHz, 22V
1981	-DMOS, 22W @ 1.1GHz, 28V (lab results) by Hitachi, Japan -VMOS, 120W @ 175MHz, 28V (DV28120T) and 60W @ 175MHz, 12V by Siliconix, U.S.A. -DMOS, 120W @ 100MHz, 80V (2SK317) Hitachi, Japan	-6.0W @ 4.0GHz, 22V
1982	-VMOS, 150W @ 100MHz, 100V (DVD150T) Siliconix, U.S.A.	

Table 1.

	Min.	Typ.	Max.
Breakdown voltage, BV_{DSS}	220V	260V	
Supply voltage, V_{DD}	80V		120V
Output power (100MHz, 17dB gain)	150W		
Transconductance (I_D = 5A)		1.5 mho	
Transconductance (I_D = 0.5A)		0.6 mho	
Input capacitance, C_{iss} (1MHz, 30V)		340pF	400pF
Output capacitance, C_{oss} (1MHz, 30V)		75pF	100pF
Reverse transfer capacitance, C_{rss} (1MHz, 30V)		10pF	15pF

Table 2. Device Characteristics.

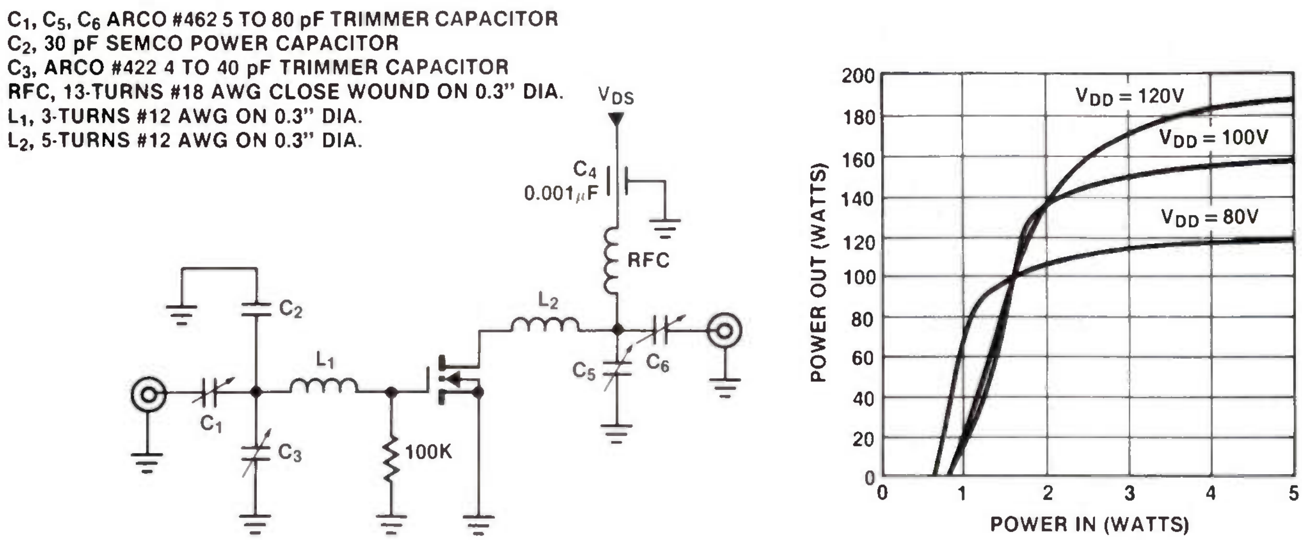

Figure 1. Test fixture and power measurements for 100MHz operation.

come lengths of wire, instead of the length of a bond leads inside the device package.

Capacitor reactance values also become more realistic. At higher operating voltages the reactance of a capacitor used as a matching element is more easily measured, and a half ohm of internal capacitor resistance will not generate destructive heat levels. Using RF bypass capacitors at the appropriate points now becomes a textbook design procedure instead of an art.

Finally, the increased impedance values allow easy construction of broadband transformers resembling ideal components with minimal parasitic effects.

Device Characterization

The RF power FET discussed in the remainder of this article is the Siliconix DVD150T, which has the highest ratings available for supply voltage, drain-to-source breakdown voltage and VHF output power, Table 2. The input and output capacitances shown in the table are determining

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- L-band digital transmitters (JTIDS)
- Data link transmitters
- Up/down converters
- Airborne pulse amplifiers

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- Command/destruct transmitters
- Guided weapon data link amplifiers
- Military drone transmitters

Radar Amplifiers
- L-band transmitters
- S-band pulse drivers for 3-D radar
- Shipboard drivers for AN/SPS-48 radars

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- Class A linear power amplifiers
- Linear AB wideband jammers
- Jamming simulators

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- Communication command links
- UHF transceiver amplifiers/modulators
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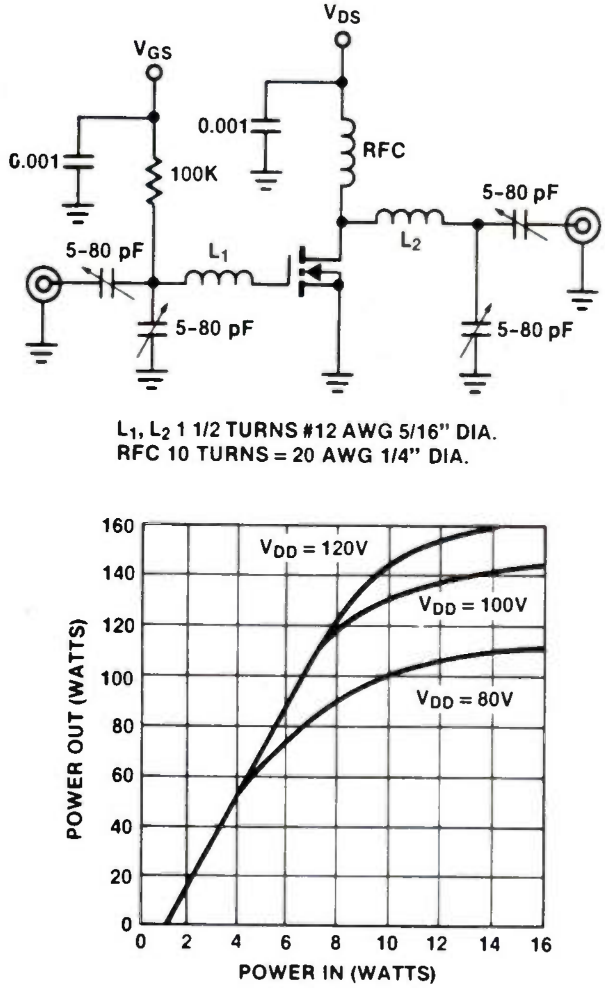

Figure 2. Test fixture and power measurements for 175MHz operation.

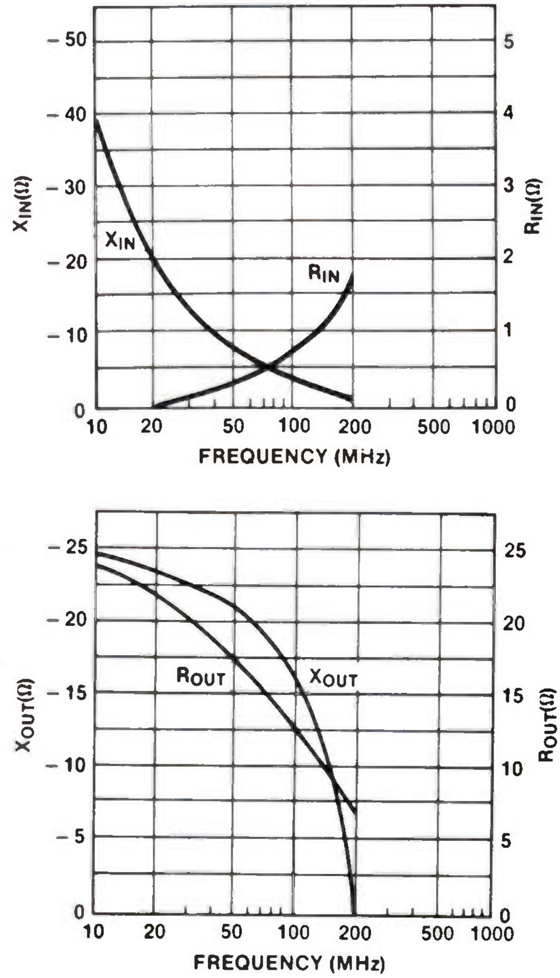

Figure 3. Plots of series equivalent input and output impedance vs. frequency used for constructing a device model.

factors in the design of broadband input and output matching networks.

The DVD150T has been characterized for Class C ($V_{GS} = 0$) operation at both 100 MHz and 175 MHz. The 100 MHz test fixture and results are shown in Figure 1. A supply voltage of 100V yielded a 150W output at a gain of 17dB. Drain efficiency measured at this point was 65%.

In the 175 MHz test fixture, Figure 2, the device was operated at zero gate voltage and with a 100V drain supply. This circuit produced an output power level of 140W at a gain of 10dB and a 64% drain efficiency.

Input and Output Models

In designing an amplifier around the DVD150T, it is important to have an adequate device model. For this purpose, the input and output impedances* are shown in Figure 3 for frequencies between 10 and 200 MHz. The capacitive nature of the input impedance as well as the small frequency-dependent resistive component are evident in this plot. The output impedance of the FET is basically identical to that of a similar bipolar transistor.

For simplified input and output matching network design, the device must be modeled in terms of electrical components. This task is relatively simple for an RF power FET. The input model is merely a series resonant circuit with capacitive, resistive and inductive elements, Figure 4a. The most significant component is the input capacitance C_{in}, which is the combined gate-to-source capacitance and Miller capacitance. Input inductance L_{in} is the combined bond-wire and lead inductances in the gate and source paths. Input resistance R_{in} is a parasitic element due to losses and power feedthrough to the output circuit. For many HF and VHF applications the input can be modeled simply by the input capacitance.

Figure 4b is a broadband matching network for an RF power FET incorporating the input model. A simplified high-frequency equivalent circuit is shown in Figure 4c. Neglecting the affect of R_{in} and L_{in}, this network is a combination of a low-pass filter and an ideal transformer. Ob-

*The term "output impedance" here refers to the conjugate of the load impedance.

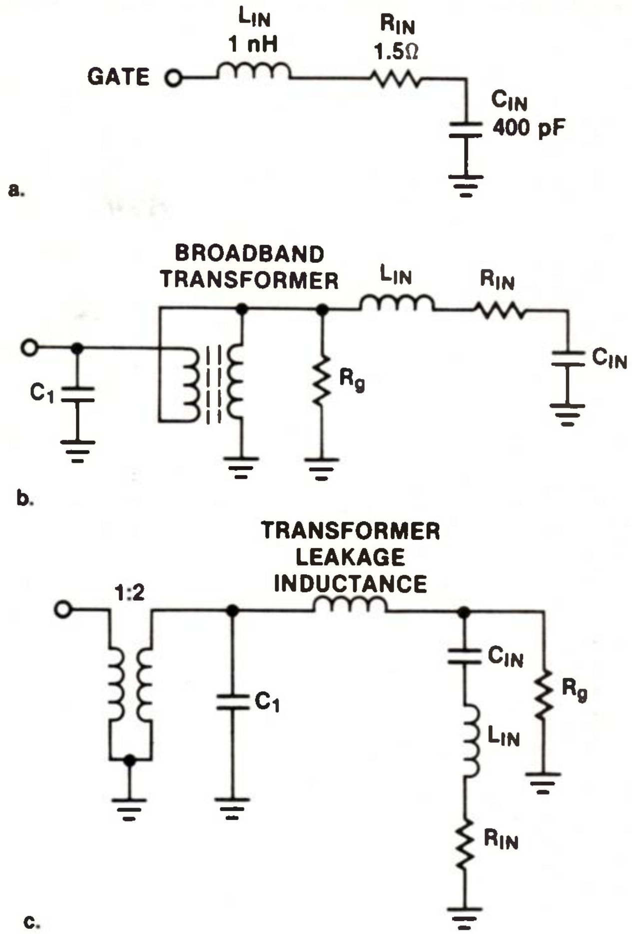

Figure 4. Applying the device input model to broadband matching network design: approximate input model, a; input model with the broadband matching network, b; and the simplified network illustrating the low-pass structure, c.

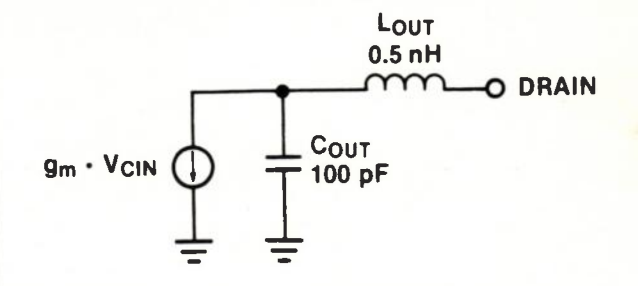

Figure 5. Approximate device output model.

taining the desired VSWR response is simply a matter of choosing the correct element values and absorbing device elements into the filter structure.

The input network is primarily responsible for the gain-bandwidth tradeoff in an RF power FET amplifier. In order to extend the cutoff frequency of the low-pass filter, the termination resistance must be lowered since C_{in} is fixed. At the same time, however, the RF voltage swing on the gate decreases, as does amplifier gain.

Two precautionary measures must be exercised when developing an input matching network. First, the amount of inductance in series with the gate lead must be minimized. The input network is basically a series resonant circuit whose resonant frequency, in most cases, lies well above the desired operating frequency. However, external series inductances can lower this resonant frequency into the operating band with a resultant gain peak followed by a declining gain response. This problem is avoided by making sure that the input termination resistor is placed as close to the device as possible.

Second, it is poor practice to operate a power FET without the input termination resistor—except near the maximum rated operating frequency. The potential problems include poor input VSWR, excessive ripple in the gain response, gate oxide puncture from excessive gate voltage and oscillation due to high-gain existing at low frequencies.

The output requirements for an RF power FET are identical to those for a bipolar transistor. The classical equation for determining the required load resistance,

$$R_L = \frac{(V_{DS} - V_{sat})^2}{2P_{out}}$$

applies equally well to a FET amplifier.

In the output model for an RF power FET, Figure 5, the capacitor and inductor can again be absorbed into a low-pass filter circuit to optimize the output bandwidth. Assuming a load resistance of 25 ohms and an output capacitance of 100pF, an output bandwidth of approximately 60 MHz should be obtainable by properly choosing the output filter network components.

This filter network must be a singly terminated design since the device output does not provide any resistive loading at the filter input. An attempt to increase the output bandwidth by lowering the load resistance will result in reduced gain and efficiency plus possible reduction of the saturated output power.

The transconductance of the circuit in Figure 5 is relatively flat with frequency, but varies with bias conditions and drive level. These characteristics produce the flat gain response of the FET amplifier and account for the low levels of intermodulation products under Class AB bias conditions.

The second article of this two-part series shows how to apply the characteristics of the DVD150T power FET in the design of a broadband push-all RF amplifier.

Characteristics of the DVD150T

Development of the DVD150T was based on work done during 1981 for NADC regarding RF power MOSFET design and application in linear broadband high-frequency circuits. The product of this development is industry's highest power and voltage ratings for RF power FETs. Device electrical characteristics shown here, combined with favorable thermal and noise properties, are particularly beneficial for designing RF amplifiers used in communications equipment.

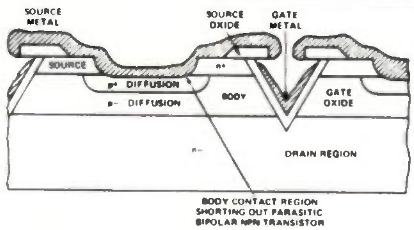

Figure 6. Shadowmask VMOS Metallization.

The DVD150T is fabricated with state-of-the-art processes, including shadow-mask structures that minimize gate capacitance and ion implantation that provides uniform electrical characteristics across the entire chip.

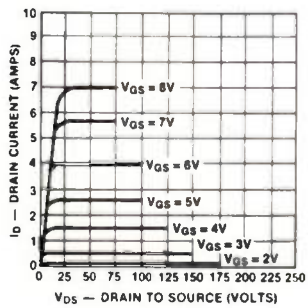

Figure 7. Typical Output Characterization.

DC output characteristics exhibit the high output impedance and square-law behavior at low gate voltages typical of power FETs.

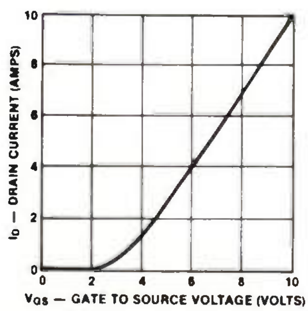

Figure 8. Static Transfer Characteristics.

Static transfer characteristics follow the square law at low gate voltages and become linear at increased current levels—an ideal response for Class AB amplification.

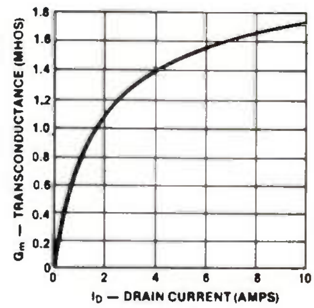

Figure 9. Typical Transconductance vs. drain current.

The variation of transconductance with drain current is typical of RF power FETs.

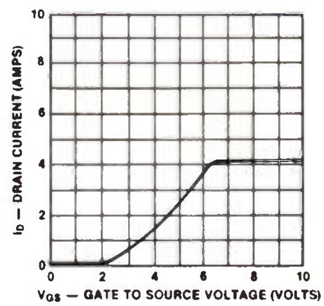

Figure 10. Dynamic Transfer Characteristics.

This plot of the dynamic transfer characteristics is developed from the dc output characteristic by assuming a quiescent current of 500mA and a 100V supply, and by superimposing a 25-ohm load line.

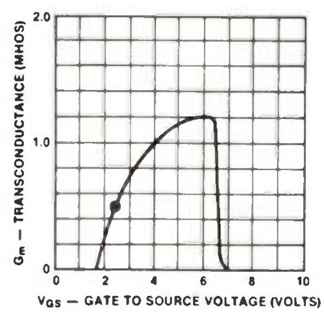

Figure 11. Transconductance vs. Gate Voltage.

In the transconductance vs. gate-voltage plot for a 25-ohm load line, the drop in transconductance just past 6V is due to device saturation. The dot on the curve indicates the recommended bias point for Class AB amplification. □

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IMD 1416-3	1.4-1.6	0.5	3.0	50	24	15.0	C	MF-4
IMD 1416-6	1.4-1.6	1.0	6.0	50	24	9.0	C	MF-4
IMD 1416-12	1.4-1.6	2.0	12.0	45	24	5.5	C	MF-3
IMD 1416-20	1.4-1.6	4.5	20.0	45	24	3.5	C	MF-3
IMD 1618-1	1.6-1.8	0.2	1.0	50	24	22.0	C	MF-4
IMD 1618-3	1.6-1.8	0.5	3.0	50	24	15.0	C	MF-4
IMD 1618-6	1.6-1.8	1.0	6.0	45	24	9.0	C	MF-4
IMD 1618-12	1.6-1.8	2.2	12.0	45	24	5.5	C	MF-3
IMD 1618-20	1.6-1.8	4.5	20.0	45	24	3.5	C	MF-3
IMD 1720-1	1.7-2.0	0.2	1.0	50	24	22.0	C	MF-4
IMD 1720-3	1.7-2.0	0.5	3.0	50	24	15.0	C	MF-4
IMD 1720-6	1.7-2.0	1.0	6.0	45	24	9.0	C	MF-4
IMD 1720-12	1.7-2.0	2.2	12.0	40	24	5.5	C	MF-3
IMD 1720-20	1.7-2.0	4.5	20.0	42	24	3.5	C	MF-3
IMD 1821-1	1.8-2.1	0.2	1.5	45	24	22.0	C	MF-4
IMD 1821-3	1.8-2.1	0.5	3.0	50	24	15.0	C	MF-4
IMD 1821-6	1.8-2.1	1.0	6.0	45	24	9.0	C	MF-4
IMD 1821-10	1.8-2.1	2.2	10.0	40	24	5.5	C	MF-3
IMD 1821-18	1.8-2.1	4.5	18.0	40	24	3.5	C	MF-3
IMD 1922-1	1.9-2.2	0.2	1.0	45	24	22.0	C	MF-4
IMD 1922-3	1.9-2.2	0.5	3.0	50	24	15.0	C	MF-4
IMD 1922-6	1.9-2.2	1.0	6.0	45	24	9.0	C	MF-4
IMD 1922-10	1.9-2.2	2.2	10.0	40	24	5.5	C	MF-3
IMD 1922-18	1.9-2.2	4.5	18.0	40	24	3.5	C	MF-3
IMD 2023-1	2.0-2.3	0.2	1.0	45	24	22.0	C	MF-4
IMD 2023-3	2.0-2.3	0.5	3.0	50	24	15.0	C	MF-4
IMD 2023-6	2.0-2.3	1.0	6.0	45	24	9.0	C	MF-4
IMD 2023-10	2.0-2.3	2.2	10.0	40	24	5.5	C	MF-3
IMD 2023-16	2.0-2.3	4.0	16.0	40	24	3.5	C	MF-3
IMD 2223-18	2.2-2.3	4.5	18.0	40	24	3.5	C	MF-3
IMD 2327-1	2.3-2.7	0.25	1.0	40	24	22.0	C	MF-4
IMD 2327-3	2.3-2.7	0.5	2.5	40	24	15.0	C	MF-4
IMD 2327-5	2.3-2.7	1.0	5.0	40	24	9.0	C	MF-4
IMD 2327-10	2.3-2.7	3.0	9.0	30	24	5.5	C	MF-3
IMD 2327-15	2.3-2.7	5.0	15.0	30	24	3.5	C	MF-3

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A Primer on

Electronic Tuning Address Systems

Higher and higher degrees of integration keep changing communications tuning systems. This article gives the basics of electronic tuning address systems with particular emphasis on PLL systems.

By Leonard I. Suckle
Market Development Manager
World Strategic Marketing
Motorola Semiconductor Products Sector

Introduction

For many years the selection of a desired frequency by a tuning system had been performed by mechanically varying the LC ratio of a tuned circuit. Correct tuning was determined by means of a "feedback loop" which included the human operator in a procedure of adjustment and decision based on visual readout or, as in the case of tuning a radio, non-distorted audio-output.

The advent of voltage variable capacitors (VVC) permitted the replacement of the sometimes cumbersome mechanical variable capacitor with a potentiometer to control a voltage, but this system still required the same human interface feedback system.

Further developments in characterization of the VVC voltage-to-capacitance relationships permitted the design of tuning systems which stored reference voltages that corresponded to the required capacitance for the desired frequency(s). The storage and selection medium generally consisted of a bank of switches and presettable variable resistors. Each desired frequency was preset with a potentiometer and an automatic frequency control (AFC) circuit was used to maintain correct tuning over temperature and component variations. This system was the forerunner of Electronic Tuning Address Systems (ETAS) and represented an electronic variation of the mechanical pushbutton selector commonly used in automobile radios.

A more sophisticated version of this system in use today utilizes a digital memory and D/A converter to provide voltages that correspond to the desired frequencies. These voltages are initially programmed to approximate the correct corresponding frequency. An AFC circuit may be used to update the digital information to the exact frequency, correcting for temperature and other variations. Unfortunately this system and the previously described system are dependent upon the reproducibility of the voltage-to-capacitance characteristics of the VVC, thereby creating a problem in a production environment. Furthermore, digital entry of the desired frequency may only be approximated due to the unpredictability of the characteristics of the components in the system.

Frequency Synthesis

Frequency synthesis refers to a technique that can generate many different frequencies with the use of a few reference frequencies. By appropriately defining the system, a multitude of specific frequencies may be generated by supplying corresponding digital information. This concept may be applied in a receiver where the digitally defined frequency is used as the local oscillator to heterodyne the desired incoming signal to the intermediate frequency (IF) circuits. The capabilities of frequency synthesis provide a means of tuning by switch closure or by the use of a microprocessor. Features such as digital frequency selection via keypad and frequency display are easily implemented.

How Does Frequency Synthesis Work?

The two most popular methods for frequency synthesis use either a phased locked loop (PLL) or a frequency locked loop (FLL); however, operation of both PLL and FLL systems is similar. A basic frequency synthesis system is shown in Figure 1. A reference frequency, f_R, equal to the desired output frequency, f_o, is applied to the detector X. This detector typically represents a phase comparator in a PLL system or a frequency comparator in a FLL system. When the two input signals to the detector are equal in either phase or frequency (dependent upon the type of system), the error voltage V_E will be at reference zero. If the output frequency deviates from the reference frequency, an appropriate error voltage will be generated and fed back to the VCO which generates the output frequency. By means of this feedback loop, the output frequency is continually and automatically adjusted to be identical to the reference frequency.

PLL Vs. FLL

The difference between a phase locked loop and a frequency locked loop system lies primarily in the type of detector used to generate the error feedback voltage (X in Figure 1). In the PLL system, a phase comparator is used which compares the phase of the two incoming signals. This is most often performed "digitally", where the incoming signals are squared and the leading edges are compared. The comparison is made on a cycle by cycle basis, which results in a fast response time to changes.

The FLL detector most often consists of some form of counter which determines the number of cycles of signal occurring in a fixed period and generates the error voltage based on the deviation of this count to the desired count. For example, the incoming comparator signal, f_V, would be applied to the clock input of a counter. The counter would be enabled for some fixed period of time, Tp, at which time the count would be compared to a value equal to the number of cycles of reference frequency, f_R, which would occur in Tp. If, after the reference period was completed, the count differed from that associated with fr, then an appropriate error voltage would be generated.

Both of these methods have their advantages and disadvantages. The PLL has a fast response time where the error voltage is updated on a cycle by cycle basis at the reference frequency. This fast response results in a disadvantage that the error voltage will contain varying amplitudes of frequency at multiples of the reference frequency which must be filtered before it is applied to the VCO. As will be shown later, the reference frequency must be chosen as a compromise, to provide the tuning resolution required as well as to be at a frequency that may be adequately filtered.

The FLL system may be implemented by using a counter or even an MPU instead of the phase comparator required in a PLL system. Furthermore, the residual frequency components in the error voltage are very easily filtered, independent of tuning resolution. The main disadvantage of FLL is slower response time, since the error voltage may only be updated at the rate of the sample period, Tp. This sample period, as with the case of reference frequency in PLL, is chosen as a compromise to provide sufficient tuning resolution while also providing adequate response time.

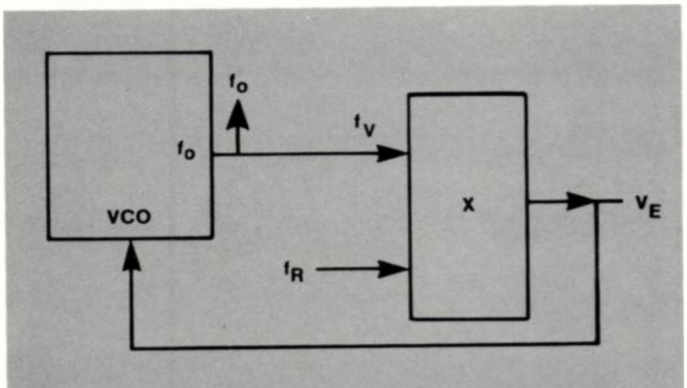

Figure 1. Basic Frequency Synthesis System.

PLL Frequency Synthesis

PLL is the most commonly used frequency synthesis method in use today. The remainder of this article will be devoted to this particular method.

The addition of programmable counters, C_N, C_P and C_R as shown in Figure 2, provides a means of programming for a variety of desired output frequencies. These counters may be programmed to divide their input frequency by a count of N, P or R, respectively. In this system, the reference frequency f_R is equal to the clock frequency f_{CLK} divided by R. Also, the detector input frequency, f_V, is now equal to the output frequency, fo, divided by the product of P and N. The feedback operation described for Figure 1 is identical is this system, and the error voltage adjusts the VCO until f_V equals f_R. In terms of the clock frequency and the output frequency,

$$f_o = (N)(P)(f_{CLK})/R$$

It should follow that a wide selection of frequencies may be generated by correctly programming the three counters.

System Components

Each system component shown in Figure 2 must be chosen to create a system which meets the design specification and capabilities of existing available products.

Counter C_P is called a prescaler. It is generally a non-programmable counter and has the function of reducing the desired output frequency, f_o, to a value which can be handled by the programmable counter C_N, since programmable counters typically have lower clock speeds, generally in the range of 20 to 30 MHz. If an f_o of 500 MHz is required, a prescaler with this frequency capability and a count value of greater than 25 would be required. High frequency prescalers are presently available for operation at 1 GHz and above.

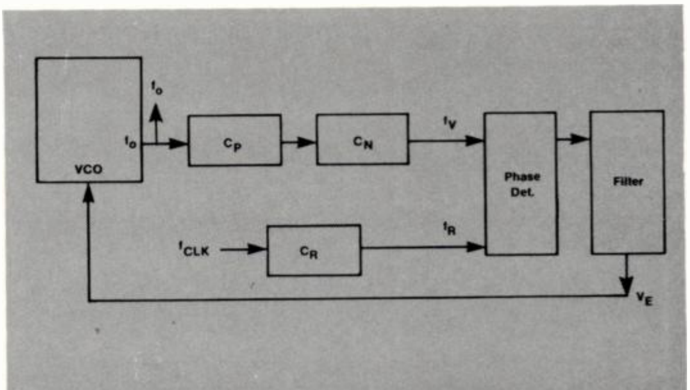

Figure 2. PLL Frequency Synthesis System.

Counter C_N is a programmable counter that provides the capability of selecting the output frequency. To determine the value of this counter, we must first determine the reference frequency to be applied to the PLL. The reference frequency selected is dependent upon the required tuning resolution. Referring once again to Figure 2, it may be seen that the phase comparator frequency, f_V, will be equal to the output frequency, f_o, divided by the prescaler count P, and also divided by whatever count, N, that has been programmed into C_N. If we let N = 1, then $f_V = f_o/P$. As we increase the value of N in unit increments, f_o will increase in increments of f_o/P. The finest resolution to which we can adjust f_o is equal to $(f_V)(P)$. But the feedback system will always adjust f_V to equal f_R. Thus, the actual resolution of our system is

$$\text{Resolution} = (f_R)(P)$$

Since the required resolution is specified by the application, and the prescaler value is determined by the maximum frequency of operation and the electrical limitations of programmable counters, the reference frequency may be determined using the above equation. Once this frequency is derived, C_N may be determined by

$$N(max) = f_o(max)/((P)(f_R)).$$

Counter C_R is used to derive the required reference frequency. Generally clock oscillators are available in a system, or oscillators of certain frequencies are easier or more cost effective to produce than the actual reference frequency required. The divide value R of C_R is appropriately chosen.

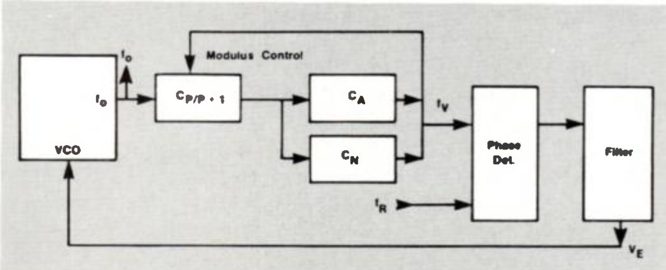

Figure 3. Dual Modulus Frequency Synthesis System.

Single Vs. Dual Modulus

The system shown in Figure 2 has been shown to develop an output frequency equal to the reference frequency times the product of the prescaler and programmable counters. This type of system is called "single modulus" because for any specific frequency, N and P are fixed and always reset to the same designated value. The tuning resolution of the system has been shown to equal $(f_R)(P)$, and to increase the resolution either the value of P or the reference frequency must be reduced. Reducing the value of P may exceed the input frequency capabilities of Cn. Reducing the value of the reference frequency lowers the residual frequency at the output of the phase comparator, which increases the difficulty of adequately filtering the error voltage.

An alternate system is shown in Figure 3. This is called a "dual modulus" system because the moduli of the frequency counters C_P and C_N change on alternating resets. A special dual modulus prescaler is required for this system. The precaler will count either to P or P + 1, depending on a modulus control input. Furthermore, the programmable counter C_N in Figure 2 is replaced by two programmable counters, C_A and C_N.

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Model	Attenuation, dB	Attenuation Tolerance	Frequency MHz	Attention Change over Frequency Range, MHz		VSWR Max. (50 ohms)	
				DC-1000	1000-1500	DC-1000	1000-1500
—AT—3	3	±0.2dB	DC-1500	0.6dB	1.0dB	1.3:1	1.5:1
—AT—6	6	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1
—AT—10	10	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1
—AT—20	20	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1

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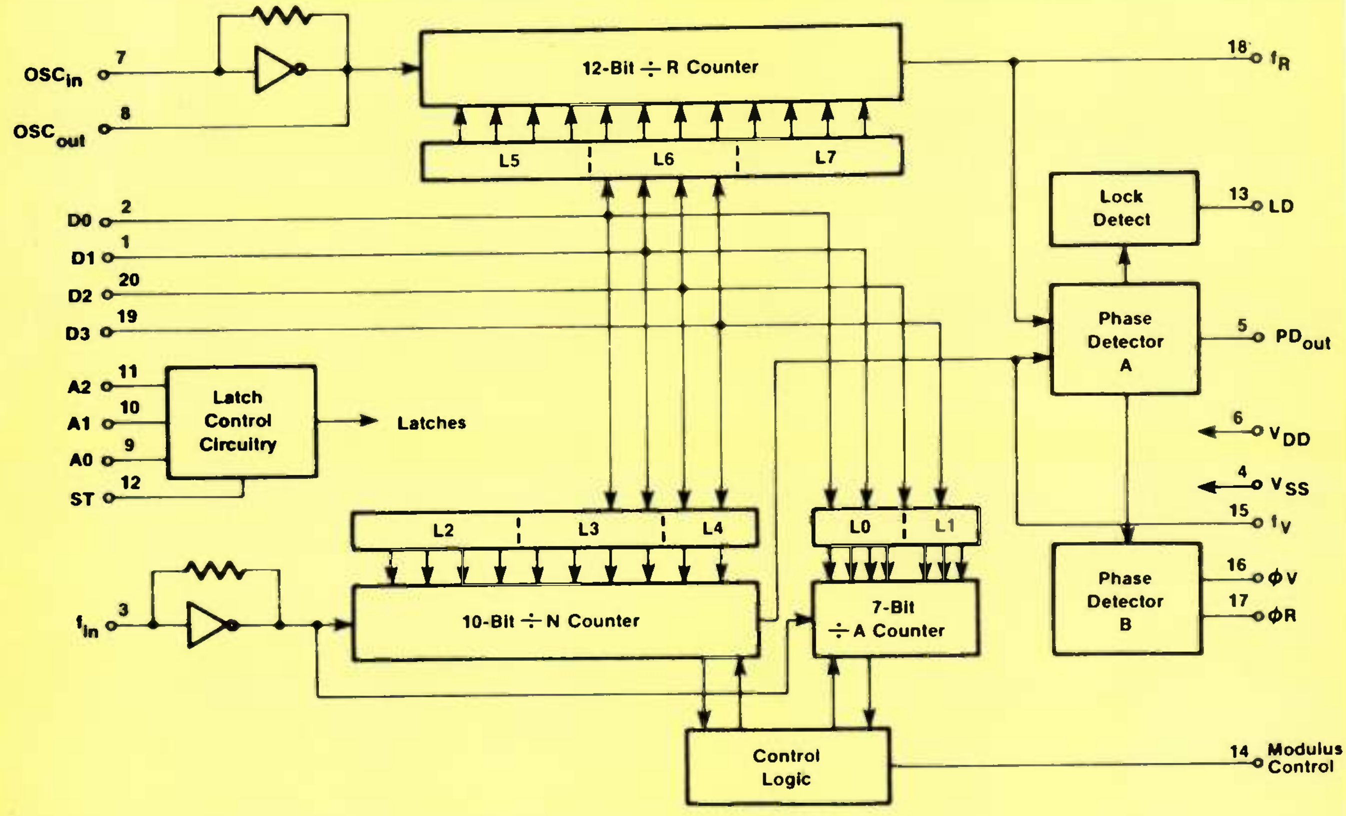

Figure 4. Motorola MC 145146 Dual Modulus Frequency Synthesizer.

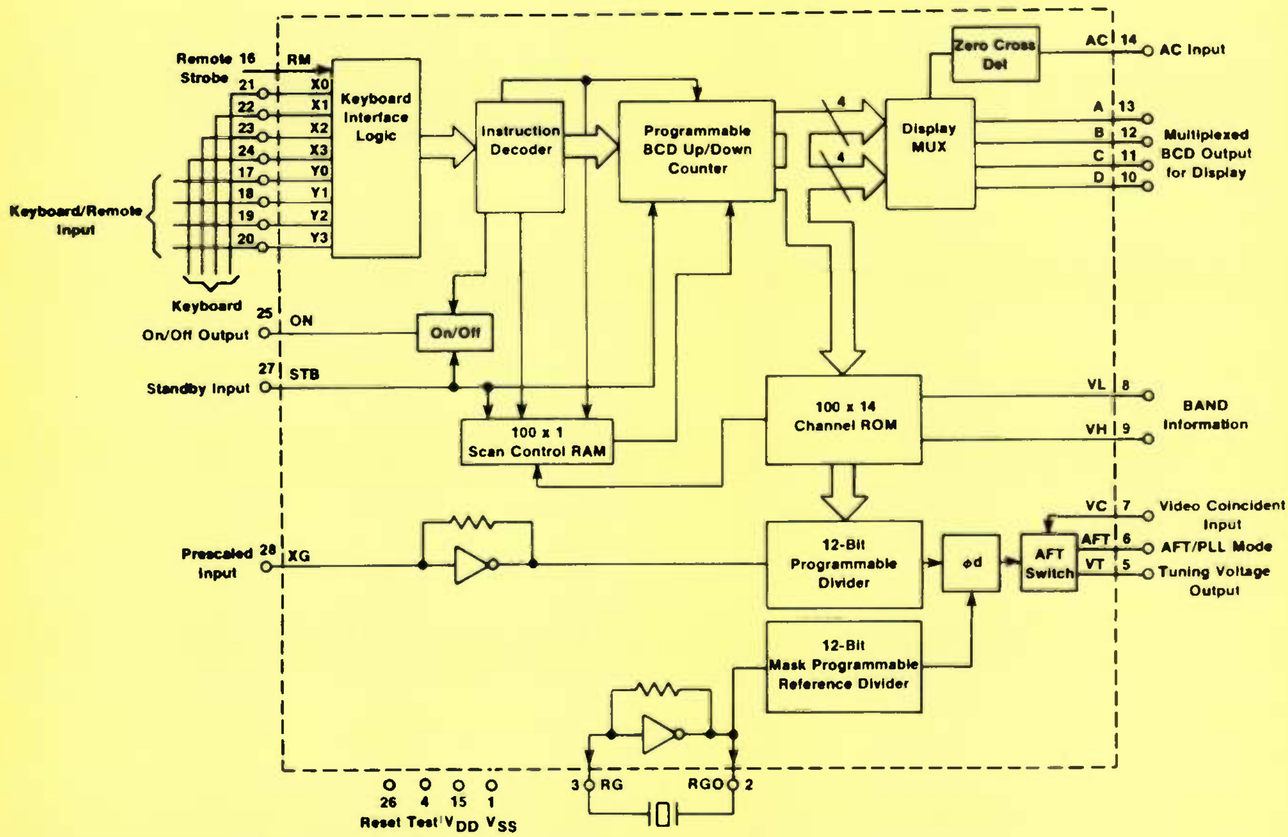

Figure 5. Motorola MC 6191 Frequency Synthesizer Block Diagram.

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Literature: INFO/CARD 2

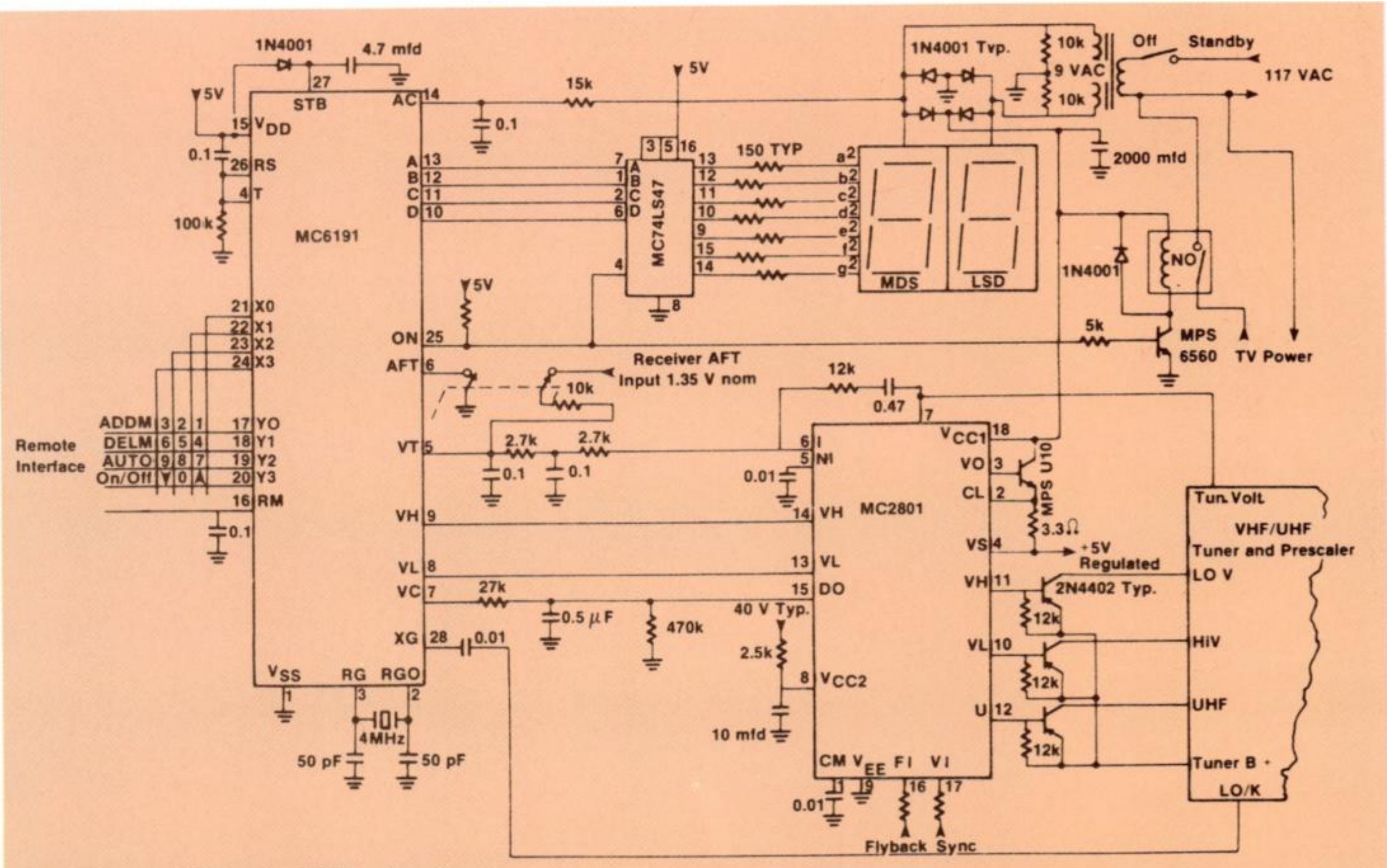

Figure 6. Full Feature TV Tuning System.

In an analysis of operation, the preset value A is less than B. Both counters are reset and begin to count simultaneously, and the modulus control output is reset to cause the prescaler to count by P + 1. When a count of A is reached in both programmable counters, the modulus control switches so the prescaler now counts by P. This condition remains until a count of N is reached, whereupon C_A, C_N and the modulus control are reset and the count begins again. Since the feedback system adjusts so that fv equals fr,

$$f_o/f_R = A(P + 1) + (N - A)P = A + (N \times P)$$

Unlike the single modulus system where unity change in N was always multiplied by the prescaler value, P, the value of C_A may be incrementally changed (by one) to provide a tuning resolution equal to the reference frequency. The system thus provides higher tuning resolution than single modulus with comparable prescaler values and a comparable or higher reference frequency.

System Definition

A wide variety of semiconductor products are available today to facilitate frequency synthesis systems. Basic building block devices exist, such as oscillators, fixed and programmable dividers, and phase detectors and comparators.

Further integration has also resulted in complete systems and subsystems being implemented on a single integrated circuit. Two examples are shown in Figures 4 and 5.

Figure 4 represents a general purpose dual modulus IC fabricated in CMOS technology to provide low power operation. This device contains an oscillator with a 12-bit divider to derive the reference frequency from a cost effective and commonly available crystal. The IC also contains a 10-bit C_N and a 7-bit C_A, with the associated control circuitry to generate the modulus control to interface with a dual modulus prescaler. In addition to the counters, the device contains two individual phase detectors that can be used to derive either a single ended or differential error voltage, as well as determine when phase lock has occurred.

An even higher level of integration is presented in Figure 5. This integrated circuit provides a complete tuning control system for a television. It not only includes the C_N and C_R programmable counters and clock oscillator, but it also contains ROM storage with the values of N for all of the TV channels available in the US. (Other standards are also available). Furthermore, keyboard scan, channel display drive, and tuner switching signals are also provided. All that remains to provide the complete TV tuning system is to add the display, a VVC tuner and prescaler, and some minimal drive and decoding circuitry. A diagram for a complete system is shown in Figure 6.

Conclusion

The basics of electronic tuning address systems (ETAS) using frequency synthesis have been presented, with particular emphasis on PLL systems. Examples of the level of semiconductor integration have been shown, where nearly every component required in the system is provided on a single piece of silicon. It is expected that with the advances being made in industry, higher degrees of integration will continue to be implemented. □

Reference

"Electronic Tuning Address Systems", Motorola Publication SG-72, Motorola Semiconductor Products Sector, Phoenix, Arizona, 1981.

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INFO/CARD 34

SPECIAL LOW

A return to "Old-fashioned" image parameter design methods for those special applications.

By Andrzej B. Przedpelski
A.R.F. Products, Inc.
Boulder, Colorado

An ideal filter (let's discuss only the amplitude characteristics) is one which passes the frequencies of interest and attenuates the unwanted frequencies the minimum required amount—and no more. Unneeded attenuation (or passband) only complicates the design and its execution.

When a lowpass filter is required, an engineer will usually look for a Chebyshev, Butterworth, or, maybe, an eliptic design. These, in a large number of applications, are very inefficient and costly. These applications include any basically fixed frequency signal which contains harmonics, which are undesirable. Typical examples are fixed frequency transmitter output and converting a square wave signal to a sine (such as after frequency division).

While the above mentioned filter types may be "Modern Network Theory", the "old-fashioned" image-parameter design may be more suitable in this case. In an m-derived filter,[1] the value of m can be chosen so that the maximum pass frequency is the desired frequency and the second harmonic (for instance) frequency is the frequency of maximum attenuation. The third and higher harmonics will be attenuated less, but that is what is usually required in these applications. Unfortunately, the values for m become unreasonable (0.87 for second harmonic attenuation and 0.94 for third, where about 0.6 is preferred).

A much better approach is to start from the beginning and analyze the problem systematically. Let's start with a simple pi type lowpass filter section, as shown in Figure 1(a). In addition, it has been shown that this configuration is also suitable for matching two unequal characteristic impedances ($R_i \neq R_o$). The component reactances, at the pass frequency, (F_o), are[2]:

$$X_a = -\frac{R_i}{Q} \tag{1}$$

$$X_b = \frac{R_i\left[Q + \sqrt{\frac{R_o}{R_i}(1 + Q^2) - 1}\right]}{1 + Q^2} \tag{2}$$

$$X_c = -\frac{R_o}{\sqrt{\frac{R_o}{R_i}(1 + Q)^2 - 1}} \tag{3}$$

where Q is any value equal to or higher than Q_{min}:

$$Q_{min} = \sqrt{\frac{R_i}{R_o} - 1} \tag{4}$$

At the stop frequency, (F_∞), we would like to make the circuit look like Figure 1(b), which would give infinte attenu-

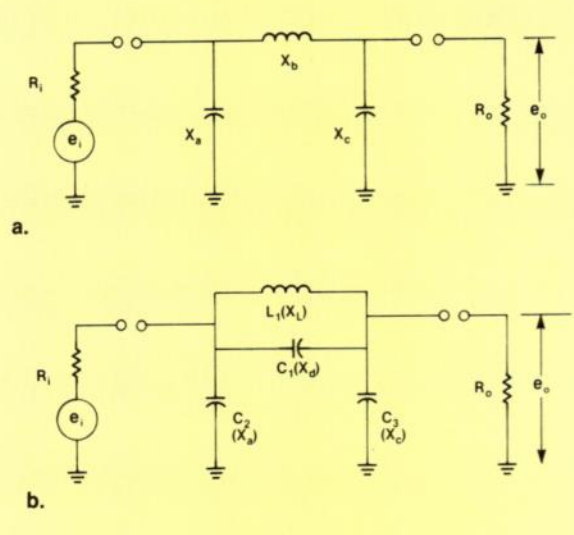

Figure 1. Lowpass Matching Circuit.

PASS FILTERS

ation at that frequency, using lossless components. Since $F\infty$ is larger than F_o, this is a feasible requirement. Starting with:

$$X_L = -X_d \text{ at } F\infty \qquad (5)$$

we obtain:

$$L_1 = \frac{1}{(2\pi F_\infty)^2 C_1} \qquad (6)$$

Since the two circuits of Figure 1 have to be equivalent

$$\frac{1}{\frac{1}{2\pi F_o L_1} - 2\pi F_o C_1} = X_b \qquad (7)$$

Substituting (6) into (7) and equating to (2), the value of C_1 can be calculated:

$$C_1 = \frac{F_o(1 + Q^2)}{2\pi R_i(F\infty^2 - F_o^2)\left[Q + \sqrt{\frac{R_o}{R_i}(1 + Q^2) - 1}\right]} \qquad (8)$$

C_2 can be calculated from (1):

$$C_2 = \frac{Q}{2\pi F_o R_i} \qquad (9)$$

and C_3 from (3):

$$C_3 = \frac{\sqrt{\frac{R_o}{R_i}(1 + Q^2) - 1}}{2\pi F_o R_o} \qquad (10)$$

Equations (8), (6), (9) and (10) thus give component values for a filter which passes F_o, attenuates $F\infty$ and provides maximum power transfer from the source (R_i) to the load (R_o) at the pass frequency.

An HP-41 C/V program which calculates all the circuit values is shown in Table I. The program calculates Q_{min} and asks for a value for Q (given R_i, R_o, F_o and $F\infty$). Any value equal to Q_{min} or higher can be used. The significance of the chosen Q will be discussed later. R_i has to be larger than R_o for the component calculation. However, the filter is bilateral and can be used in either direction.

Once the filter is designed its performance should be checked to see if it satisfies the performance requirements. This can be done using the program of Table II. If only non-lossy components were used, the task of calculating the insertion loss would be easy. The reflection coefficient could be calculated and, from it, the insertion loss[3]. However, to make the program more versatile a lossy inductor was included, which is more representative of the actual circuit. This necessitates a different method of insertion loss calculation[4]. This method is shown in Figure 2. In this case either R_i or R_o can be larger. The program will calculate the correct step-down or step-up insertion loss.

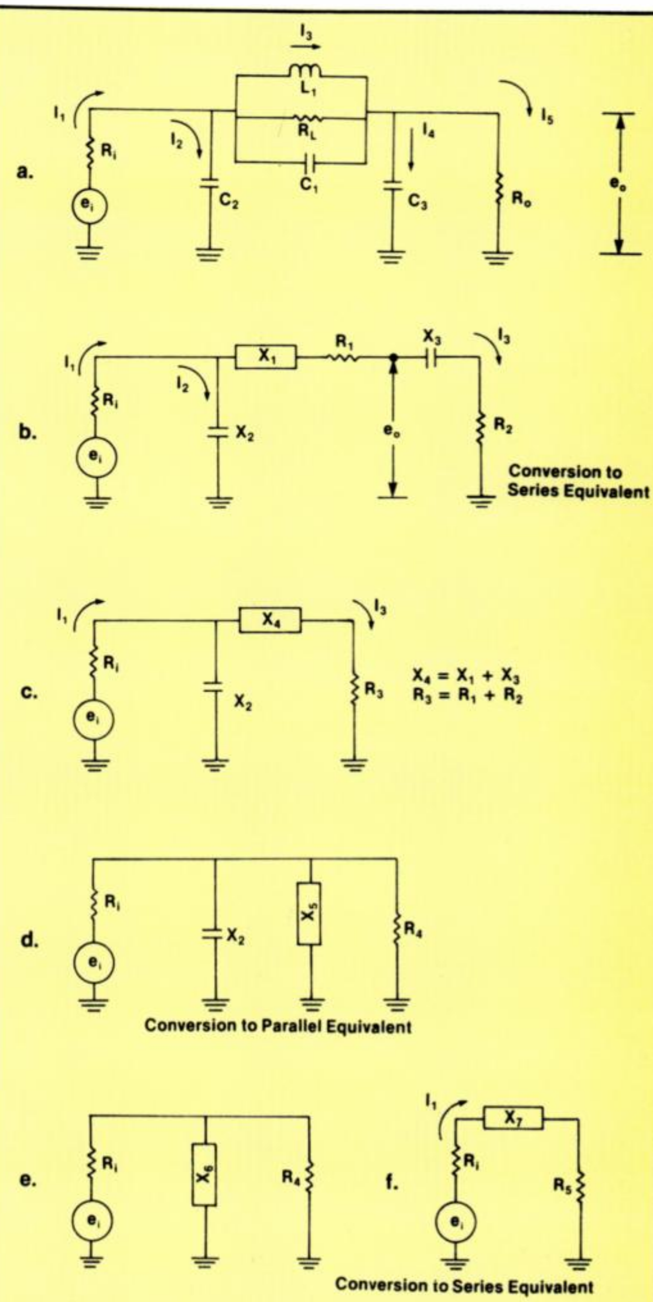

Figure 2. Equivalent Circuits.

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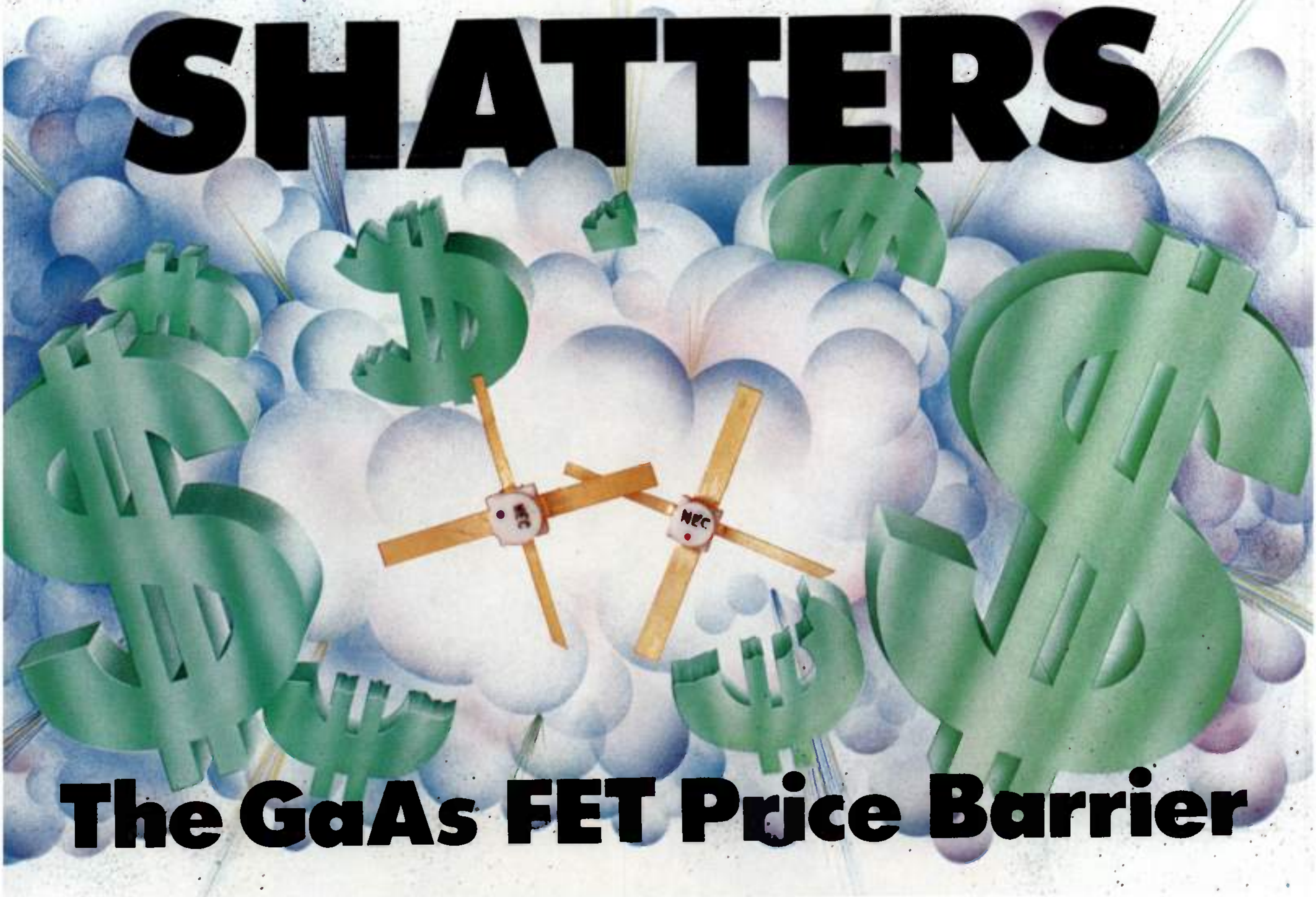

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	8	1.2	11.0
	12	1.9	9.0

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V_{DS} = 3V, I_{DS} = 10mA	4	1.0	13.0
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Using

$$I_1 = \frac{e_i}{R_i + R_5 + jX_7} \quad (11)$$

and

$$e_o = I_3(R_2 + jX_3) \quad (12)$$

and

$$\frac{I_3}{I_1} = \frac{R_5 + jX_7}{R_3 + jX_4} \quad (13)$$

the circuit gain can be calculated:

$$\frac{e_o}{e_i} = \frac{I_3(R_2 + jX_3)}{I_1(R_i + R_5 + jX_7)} = \frac{(R_5 + jX_7)(R_2 + jX_3)}{(R_3 + jX_4)(R_i + R_5 + jX_7)} \quad (14)$$

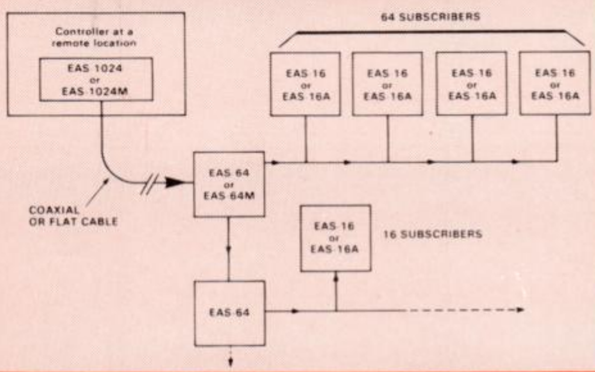
which can be expressed in dB:

$$\frac{e_o}{e_i} = 20 \log \left| \frac{R_5 + jX_7)(R_2 + jX_3)}{(R_3 + jX_4)(R_i + R_5 + jX_7)} \right| \text{dB} \quad (15)$$

This gain includes the transformation gain, circuit losses and the effect of source impedance (i.e., a lossless circuit with $R_i = R_o$ will give a gain of -6 dB).

An example will show the advantages of this circuit compared to the usual lowpass filter. Let's assume that a signal, at a 500 ohm impedance level, has a second harmonic content of -20 dBC and a third harmonic of -30 dBC. An output, at 50 ohms, with a harmonic content of less than -60 dBC is required. Dissipative insertion loss cannot exceed 1 dB and the circuit should be matched for maximum power transfer.

Using a lossless standard Butterworth lowpass filter, an 8-pole design is needed. In addition, an impedance transformation network is required. With a lossless 1 DB ripple Chebyshev design only 5 poles are required in addition to



```
01+LBL "TRAF"
02 SF 21
03 RCL 12
04 RCL 13
05 /
06 1
07 -
08 SQRT
09 "MIN Q = "
10 ARCL X
11 AVIEW
12 "Q = ?"
13 PROMPT
14 "Q = "
15 ARCL X
16 AVIEW
17 ENG 2
18 STO 14
19 2
20 /
21 PI
22 /
23 RCL 15
24 /
25 RCL 12
26 /
27 RND
28 STO 19
29 "C2 = "
30 ARCL X
31 AVIEW
32 RCL 13
33 RCL 12
34 /
35 RCL 14
36 X↑2
37 1
38 +
39 *
40 1
41 -
42 SQRT
43 STO 18
44 2
45 /
46 PI
47 /
48 RCL 15
49 /
50 RCL 13
51 /
52 RND
53 STO 20
54 "C3 = "
55 ARCL X
56 AVIEW
57 RCL 14
58 X↑2
59 1
60 +
61 RCL 15
62 *
63 2
64 /
65 PI
66 /
67 RCL 12
68 /
69 RCL 16
70 X↑2
71 RCL 15
72 X↑2
73 -
74 /
75 RCL 18
76 RCL 14
77 +
78 /
79 RND
80 STO 18
81 "C1 = "
82 ARCL X
83 AVIEW
84 PI
85 ST+ X
86 RCL 16
87 *
88 X↑2
89 *
90 1/X
91 RND
92 STO 17
93 "L1 = "
94 ARCL Y
95 AVIEW
96 ADV
97 END
```

STORE:
$R_{12} - R_i$
$R_{13} - R_o$
$R_{15} - R_o$
$R_{16} - F_\infty$

Table I.


```
01+LBL "LPTR"
02 FS? 00
03 GTO 00
04 "F=? "
05 PROMPT
06 VIEW X
07+LBL 00
08 ST+ X
09 PI
10 *
11 STO 21
12 FIX 2
13 RCL 17
14 *
15 STO 25
16 1/X
17 RCL 18
18 RCL 21
19 *
20 -
21 1/X
22 RCL 25
23 RCL 26
24 *
25 X<>Y
26 1/X
27 X<>Y
28 1/X
29 R-P
30 1/X
31 P-R
32 STO 24
33 X<>Y
34 STO 25
35 RCL 13
36 RCL 20
37 RCL 21
38 *
39 CHS
40 X<>Y
41 1/X
42 R-P
43 1/X
44 STO 22
45 X<>Y
46 STO 23
47 X<>Y
48 P-R
49 ST+ 24
50 X<>Y
51 ST+ 25
52 RCL 25
53 RCL 24
54 R-P
55 ST/ 22
56 X<>Y
57 ST- 23
58 X<>Y
59 1/X
60 P-R
61 1/X
62 X<>Y
63 RCL 19
64 RCL 21
65 *
66 -
67 X<>Y
68 1/X
69 R-P
70 1/X
71 ST* 22
72 X<>Y
73 ST+ 23
74 X<>Y
75 P-R
76 RCL 12
77 +
78 R-P
79 ST/ 22
80 X<>Y
81 ST- 23
82 RCL 22
83 LOG
84 20
85 *
86 FS? 00
87 RTN
88 "RESP= "
89 ARCL X
90 "├ DB"
91 AVIEW
92 ADV
93 END
```

STORE:
$R_{12} - R_i$
$R_{13} - R_o$
$R_{17} - L_1$
$R_{18} - C_1$
$R_{19} - C_2$
$R_{20} - C_3$
$R_{26} - Q_L$

SET FLAG 00 FOR PRPLOT

Table II.

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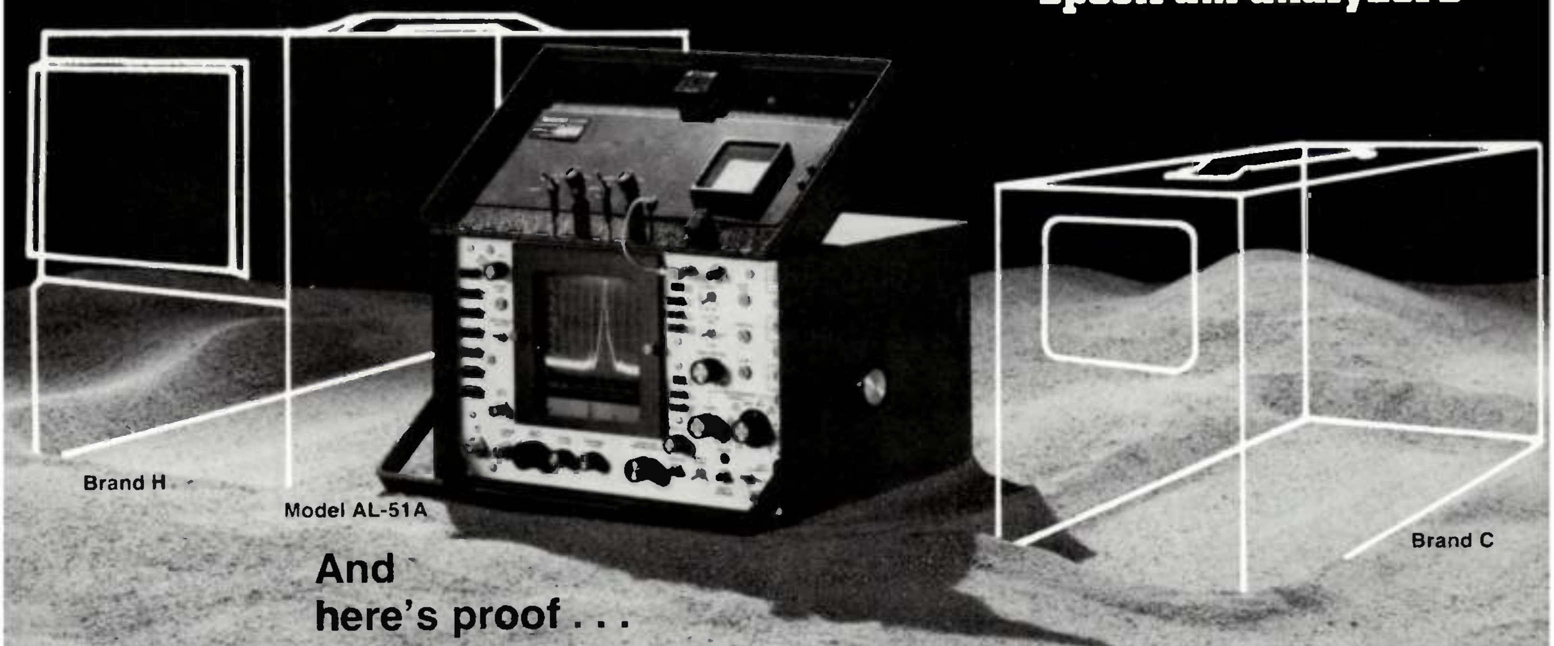

And here's proof . . .

SPECIFICATION	BRAND H*	TEXSCAN'S AL51A	BRAND C*
FREQUENCY RANGE DISPERSION FREQUENCY ACCURACY	0.1—1500 MHz 50KHz—1000MHz 2% of dispersion ±5MHz	0.4—1000MHz 20KHz—1000MHz ±0.01%	1—1000MHz 100KHz—100MHz ±5MHz
AMPLITUDE DYNAMIC RANGE AVERAGE NOISE LEVEL ACCURACY (total worst case)	70dB −107dBm (10KHz resolution) ±3.5dB	60dB −118dBm (10KHz resolution) ±4dB	70dB NOT SPECIFIED ±3dB
RESOLUTION (min)	1KHz	500Hz	2KHz
STABILITY SHORT TERM P/P LONG TERM	1KHz NOT SPECIFIED	500Hz 25KHz/10 min	NOT SPECIFIED 50KHz/5 min
NOISE SIDEBANDS	−65dB 50KHz away	−70dB 50KHz away	−70dB 50 KHz away
OPERATING POWER	115/230vac	115/230vac 12 vdc	115/230 vac
SIZE CUBIC INCHES	2059	1092	1503
WEIGHT LBS	40lbs	27lbs (incl battery)	30lbs
FEATURES	**BRAND H***	**TEXSCAN'S AL51A**	**BRAND C***
INTERNAL BATTERY	NOT OFFERED	STANDARD	NOT OFFERED
EXTERNAL 12v ac oper	NOT OFFERED	STANDARD	OPTIONAL
PHASELOCK	NOT OFFERED	STANDARD	NOT OFFERED
AUDIO	NOT OFFERED	OPTIONAL	STANDARD
FREQUENCY MARKERS	NOT OFFERED	STANDARD	NOT OFFERED
DIGITAL STORAGE	OPTIONAL	OPTIONAL	NOT OFFERED
PRESET FREQUENCY BANDS	NOT OFFERED	STANDARD	NOT OFFERED
TWO LOG RANGES	STANDARD	STANDARD	NOT OFFERED
RUGGED CARRYING CASE WITH FRONT PANEL COVER	OPTIONAL	STANDARD	OPTIONAL

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Q = 4.00	Q = 4.00	Q = 5.00
C2 = 1.27E-9	C2 = 1.27E-9	C2 = 1.59E-9
C3 = 2.66E-9	C3 = 2.66E-9	C3 = 4.03E-9
C1 = 373.E-12	C1 = 373.E-12	C1 = 440.E-12
L1 = 17.0E-6	L1 = 17.0E-6	L1 = 14.4E-6
1,000,000.00	1,000,000.00	1,000,000.00
RESP= -16.30 DB	RESP= -16.02 DB	RESP= -16.38 DB
2,000,000.00	2,000,000.00	2,000,000.00
RESP= -76.45 DB	RESP= -94.04 DB	RESP= -79.90 DB
3,000,000.00	3,000,000.00	3,000,000.00
RESP= -46.19 DB	RESP= -46.19 DB	RESP= -49.82 DB
$Q_L = \infty$	$Q_L = 100$	$Q_L = 100$

Table III. Results Using Different Values of Circuit Q and Inductor Q_L.

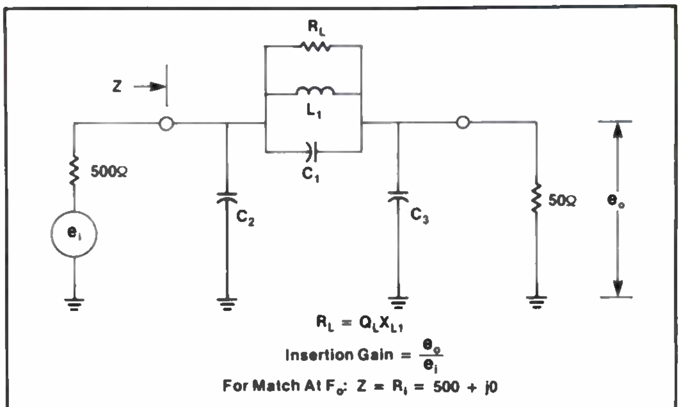

Figure 3. Typical Lowpass Matching Example.

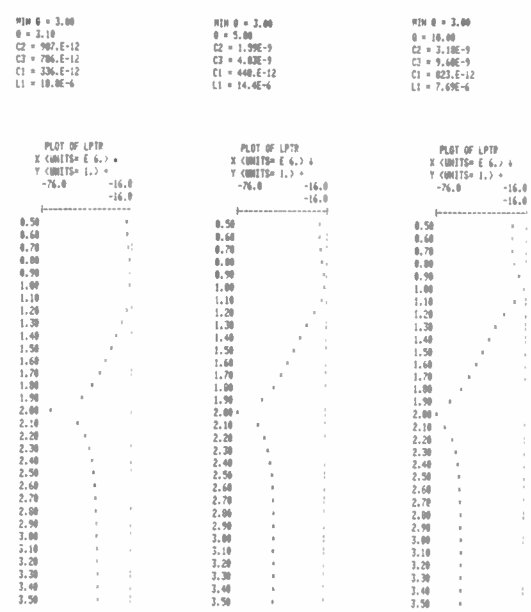

Figure 4. Frequency Response for Different Values of Circuit.

the impedance transformation. The impedance transformation can be incorporated in the basic filter design, but these impedance matching filters are not "off-the-shelf" designs. Using the filter shown in Figure 3 the required filtering and matching can be easily accomplished using 4 components in a non-critical configuration. Program I (of Table I) calculates the component values and Program II (Table II) calculates the frequency response. The finite value of the Q of the inductor, Q_L, can be used to calculate the response including circuit losses (capacitors usually have much higher Q values.) Using the example of Figure 3, the circuit values and the response at the second and third harmonics were calculated (Table III). The first column shows that using a lossless inductor, a circuit Q of 4 will provide barely adequate attenuation at the third harmonic. When a reasonable inductor loss is used ($Q_L = 100$), the difference in response at third harmonic and fundamental is not enough, by a fraction of a dB, as shown in the second column. Column three shows that using a circuit Q of 5 provides adequate attenuation for the harmonics even using $Q_L = 100$. The insertion loss due to the 10:1 step-down is 16.02 dB and the loss in the inductor is 0.36 dB, or less than the maximum desired of 1 dB.

Figure 4 shows the frequency response of the circuit of Figure 3 for different values of circuit Q. In all cases a Q_L of 100 was used. While higher values of circuit Q give higher attenuation at frequencies above cut-off, the passband at F_o becomes smaller and the circuit may become more critical. The plots were obtained using the HP-41C/V PRPLOT routine and FS 00.

In general, the circuit is quite useful (and easy to use) where a narrow range of desired frequencies is present and both power matching and harmonic attenuation are needed.

References

1. F.E. Terman, "Radio Engineer's Handbook", McGraw-Hill Book Co., N.Y., 1943, p. 228.
2. A. Przedpelski, "Simplify conjugate bilateral matching of complex impedances", Electronic Design, March 1, 1978.
3. A. Przedpelski, "Eliminate bandwidth calculation drudgery with a universal calculator program", Electronic Design, Oct. 11, 1979.
4. A. Przedpelski, "Low Impedance Double Tuned Circuit", r.f. design, May/June 1982.

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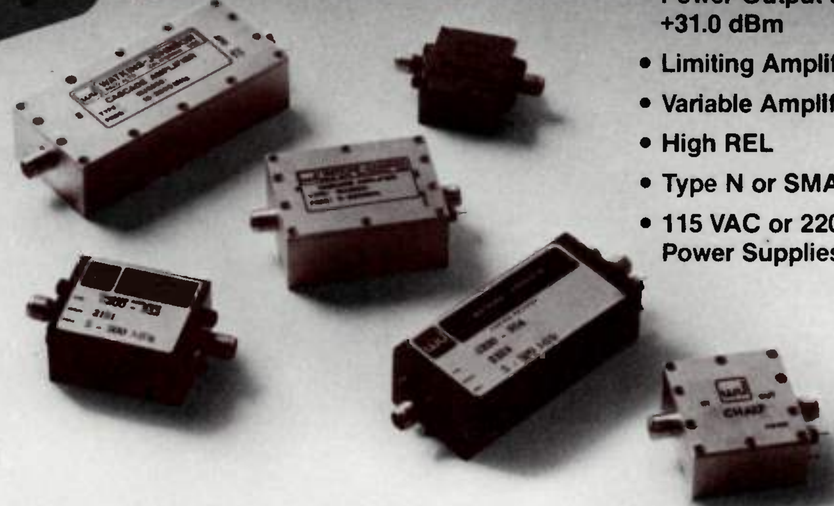

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INFO/CARD 39

Programmable Semiconductor Parameter Analyzer

A new development in semiconductor analysis called a semiconductor parameter analyzer has been introduced by Hewlett-Packard.

The HP Model 4145A stimulates voltage and current-sensitive semiconductor devices and measures their resulting current and voltage responses. This new type of curve tracer is designed especially for electrical engineers and scientists who design, study, use or process semiconductor devices.

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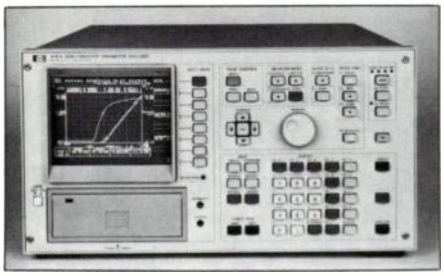

This innovative new HP instrument saves measurement setup time and reduces setup errors by storing complex dc test sequences on floppy discs.

In addition, the HP 4145A can manipulate measurement data and display such parameters as h_{FE} vs I_C and g_m vs V_{GS}, adding up to a fast and complete analysis of semiconductor dc characteristics.

The U.S. price is $19,220. Call local **Hewlett Packard sales office or circle INFO/CARD #140.**

Monolithic Filters

What are believed to be the world's first monolithic filters for RF applications were unveiled by Thinco Division of Hull Corp. Three devices were introduced: A high pass Butterworth filter, a low pass Butterworth filter, and a simple bypass filter. Full characteristics of the units are still being evaluated. Size of the high pass and low pass filters is 0.140" × 0.180" × 0.025". The high pass and low pass filters can be furnished with cut-off frequencies between 60 and 400 MHz. The bypass filter is available in two sizes. The smaller, the LC-55, measuring 0.077" × 0.116" × 0.025", has inductances from 30 to 240 nH, and

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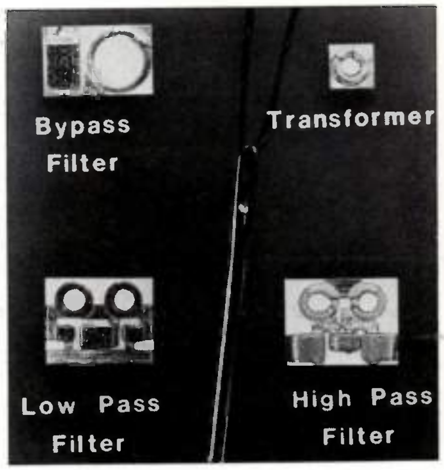
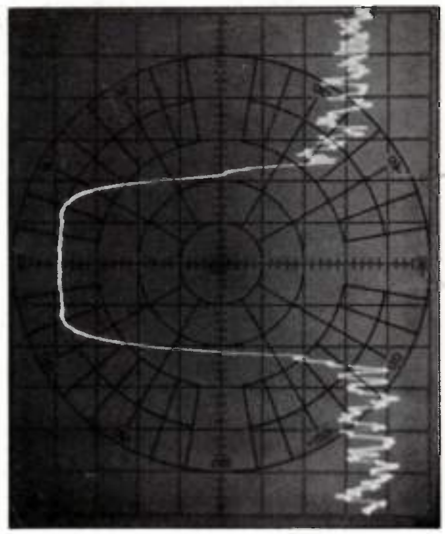


capacitances from 12 to 110 pF. The larger, model LC-100, measuring 0.114" × 0.177" × .025", has inductances from 215 to 540 nH, and capacitances from 50 to 500 pF. **Thinco Div., Hull Corp., Hatboro, PA 19040, (215) 675-5000 or INFO/CARD #139.**

Wideband Saw Filters

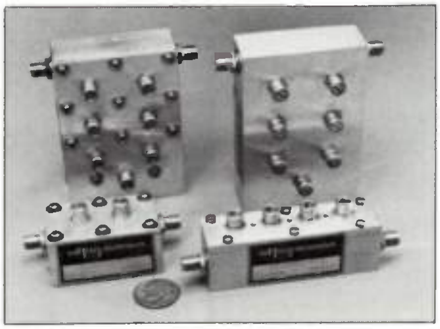
Sawtek Inc. has announced a new family of 70 MHz surface acoustic wave (SAW) wideband filters. Designed primarily for use in home satellite receiver systems, these new filters



are available with bandwidths in the 18 to 36 MHz range. This new SAW design has a shape factor (40 dB to 3 dB) as low as 1.4 to 1 with 60 dB ultimate rejection. An insertion loss of 20 to 25 dB is achieved with no matching or with a single inductor. **Sawtek, Inc., 2541 Shader Rd., P.O. Box 7756, Orlando, FL 32854, (305) 299-4441 or INFO/CARD #138.**

Dielectric Resonator Bandpass Filters from 3.3 to 12.4 GHZ

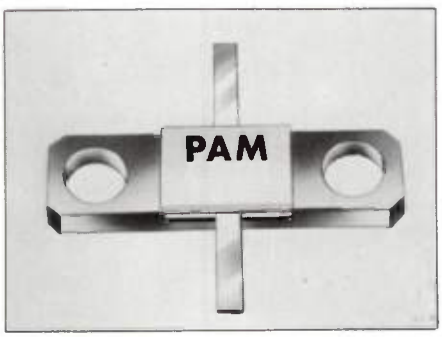
The AT-BPF100 series of bandpass filters use high dielectric constant, temperature stabilized, dielectric resonators to obtain fixed performance comparable to waveguide bandpass filters at the same frequency. Two to eleven pole designs are available having 3 dB bandwidths up to 6%. The filters are capable of handling up to 12 watts of CW power. Insertion loss, in most cases, is negligibly higher than their waveguide counterparts. These dielectric resonator filters offer superior frequency vs. temperature stability (2 PPM/°C) than traditional filters while being physically smaller and less expensive. Among many available options are a wide operating temperature range of −54°C to +85°C, constant group delay and different package form factors. Typically deli-



very is 30-60 days ARO in small quantities. Contact R.C. Havens, **AD-TECH MICROWAVE, INC. 7755 E. Redfield Rd., S-500, Scottsdale, AZ 85260, (602) 998-1584 or INFO/CARD #137.**

Compact Attenuator

KDI Pyrofilm announces a new compact attenuator module PAM—(db) for use in stripline and microstrip circuits. This low VSWR attenuator module is available in db values from 1 thru 10 db and is useable thru X-Band with a VSWR of 1.30:1 at 4 GHz, and 1.50:1 at 12.4 GHZ in .025 thickness microstrip line with a dielectric



constant of 10. **KDI Pyrofilm Corp., 60 S. Jefferson Road, Whippany, N.J. 07981, (201) 887-8100 or circle INFO/CARD #136.**

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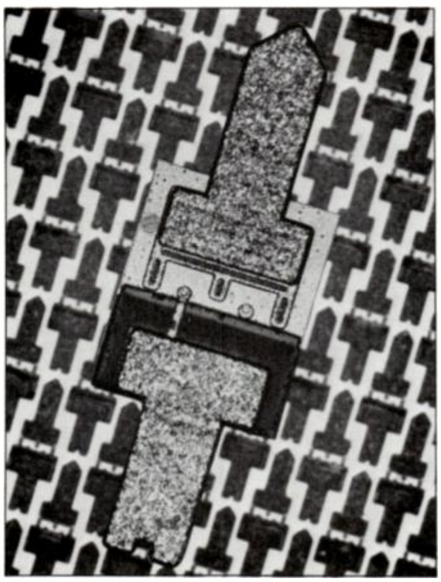
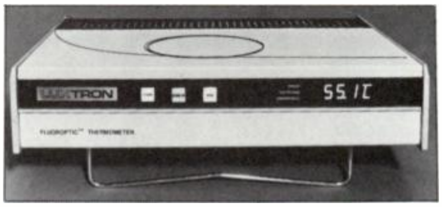
Microwave Schottky Diodes

With a choice of 20 different part numbers, an array of new beam lead Schottky diodes well suited for test automation is offered the microwave designer by Hewlett-Packard. The HSCH-5300 series beam lead diodes



are RF and DC tested and available in low or medium barrier. Three capacitance selections also are available for single or batch-matched versions. With repeatable RF characteristics through K_u band, the HSCH-5300 series diodes may be used in stripline or microstrip circuits. Pricing and delivery information is available through authorized **Hewlett-Packard components distributors or circle INFO/CARD #133.**

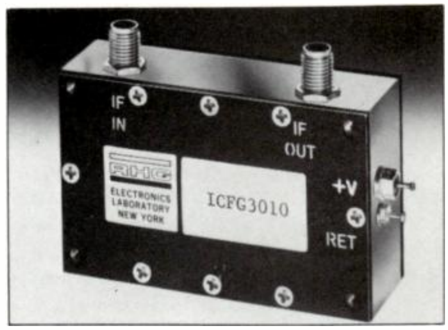
Optical Fiber Probe Thermometer



Luxtron Corporation introduces a patented new technology for temperature measurement with the Model 1000A Fluoroptic Thermometer. The Model 1000A employs a single optical fiber probe which allows measuring temperature accurately in an RF environment. A new optical technique for measurement of temperature using the ratio of intensities of fluorescent emission lines of certain rare earth phosphors. Makes possible the measurement of temperatures from – 50°C to 200°C (392°F) to 0.1°C precision with total electrical isolation and minimum thermal perturbation. Uses a small, inert optical fiber probe which is non-metallic, non-conducting and non-contaminating. **Luxtron, 1060 Terra Bella Ave., Mountain View, CA 94043, (415) 962-8110 or INFO/CARD #132.**

Variable Bandwidth IF Preamplifiers

A new series of variable bandwidth IF preamplifiers which enable receiver designers to electronically vary system IF bandwidth is available from RHG Electronics Laboratory, Inc. The new RHG preamplifiers are designated as the ICFG series for fixed gain models



and the ICFK series for variable gain models. Four models, covering operating frequencies of 21, 30, 45, and 60 MHz, are listed for each series. ICFG units maintain gain at 20 dB as the bandwidth is varied. On ICFK units, the gain varies inversely with the bandwidth providing a constant gain bandwidth product and the resulting constant "grass" level seen on an "A" type display. Model ICFG3010 is priced at $795 each; and Model ICFK6020C at $750 each. Delivery of either is 90 days ARO. **RHG Electronics Laboratory, Inc., 161 East Industry Court, Deer Park, N.Y. 11729, (516) 242-1100 or INFO/CARD #131.**

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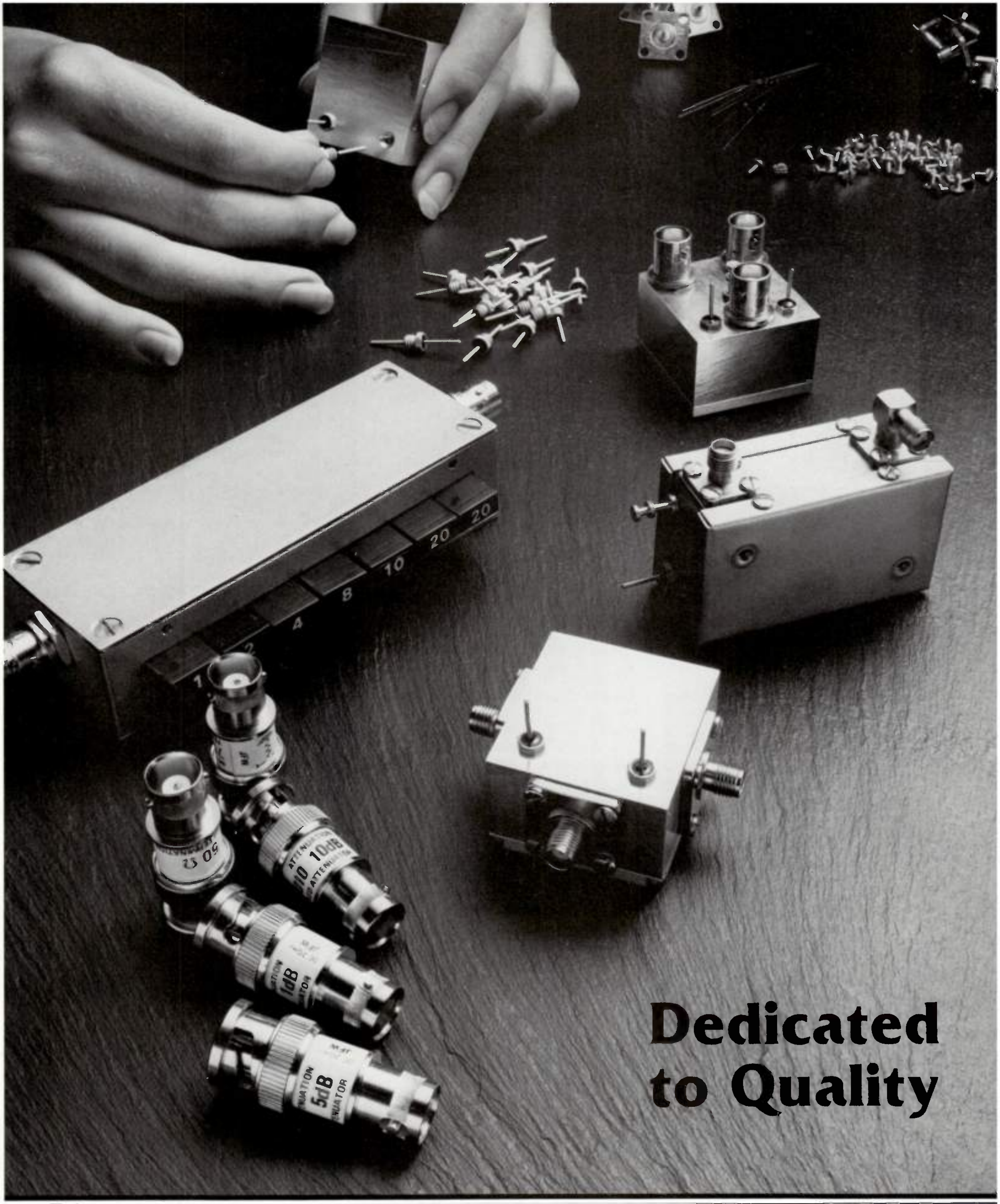
The Comer Communications R30K is an extremely small general coverage communications receiver, measuring only 2 inches by 4 inches by 6 inches. Despite this small size the R30K is able to perform equally if not better than most receivers occupying 18 times the volume. Frequency coverage is from 50 KHz to 30 MHz, and selection is by means of a five digit push wheel switch giving 1 KHz resolution, a VFO is provided to interpolate between the 1KHz steps. Reception modes are AM, LSB, USB and CW. **Comer Communications, 609 Washingtonia Drive, San Marcos, California 92069, (714) 744-3215 or INFO/CARD #130.**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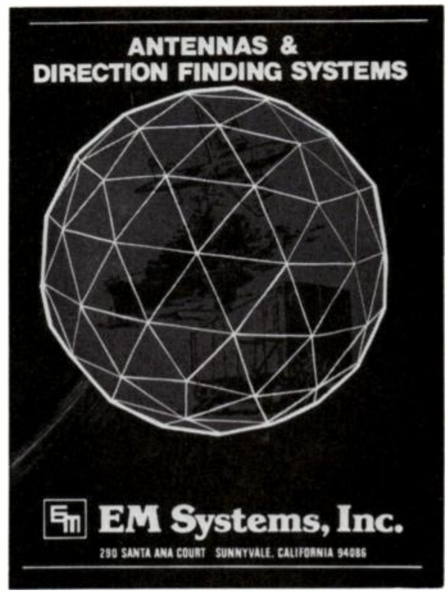
LogiMetrics has announced the availability of a new 60 page publication presents details on the company's product lines including: Traveling Wave Tube Amplifiers, Signal Generators, Electromagnetic Field Generating Systems, EW Systems and High Voltage Power Systems. Contact **J. Deutsch, LogiMetrics, Inc., 121-03 Dupont Street, Plainview, N.Y. 11803, or INFO/CARD #104.**

Variable Capacitor Design Manual

New 20-page catalog includes a wide selection of variable capacitors, microwave tuning elements, microwave diode holders, and prototyping kits. Easy-to-use format tabulates by part number, photo, and characteristics the types and styles available. **Johanson Manufacturing Corporation, 400 Rockaway Valley Road, Boonton, N.J. 07005, (201) 334-2676 or INFO/CARD #114.**

Antenna Catalog

EM Systems' new antenna catalog



presents the company's EW antennas and direction finding systems. It's fifty pages describe high technology antenna products ranging from the classic dual polarized horn through wide-band directional and omnidirectional log periodics, spirals and biconical antennas to sophisticated rotary direction finding systems as well as multi element arrays for monopulse direction finding systems. **EM Systems, Inc., 290 Santa Ana Court, Sunnyvale, CA 94086, (408) 733-0611 or INFO/CARD #113.**

Transformers For Telecommunications

The Midcom Unit of Midland-Ross Corporation announces the publication of a totally new transformer catalog. This 24-page catalog, *Transformers for Telecommunications,* features vital information on products, test procedures, and terminology. **Midland-Ross Corporation, Midcom Unit, P.O. Box 3328, North Mankato, MN 56001, (507) 625-6521 or INFO/CARD #112.**

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A new booklet is available from Magnecraft with methods for solving coil design problems. New formulae compare wire gage to coil resistance, coil turns, power dissipation and ampere turns. Applications meet many

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RF and Microwave Components Brochure

A 53-page brochure of RF and microwave components made by the Swiss corporation Huber + Suhner AG is available from Uniform Tubes, Inc., Collegeville, PA. The catalog illustrates

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(Continued on page 70.)

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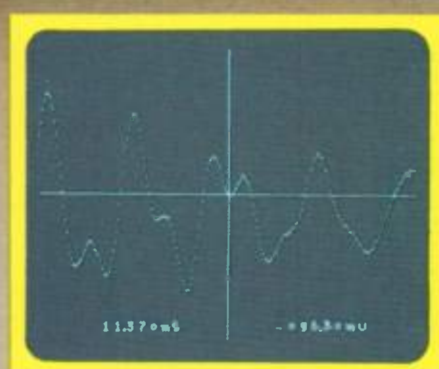

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Newark Electronics Catalog

Catalog 106 is now in production and scheduled for release this fall. The Newark catalog features products from 190 major manufacturers. It is a custom produced catalog and all items listed are stocked. Catalog 106 is free and you may now order in advance of publication. **Newark Electronics, Catalog Dept. NR, 500 N. Pulaski Road, Chicago, Ill. 60624 or INFO/CARD #106.**

Filter Catalog

This 16-page catalog (BTV/82) features filters, traps and channel combiners designed to eliminate interference in broadcast TV systems and to combine several transmitters to one antenna. **Microwave Filter Company, Inc., 6743 Kinne St., East Syracuse, NY 13057, 1-800-448-1666 (toll-free) or INFO/CARD #105.**

New Books

Microwave Semiconductor Engineering

By Joseph F. White

This book analyzes the complex field of semiconductor microwave engineering. Explained are the essentials of the physics of semiconductors, reliability estimates, driver circuits, matrix theory, computer-aided design and how to use filter theory with microwave semiconductor networks, complete with examples. Included is information that saves time on the job: the basis of the Smith Chart, tables and charts on microstrip, stripline, coax and waveguide and the properties of materials needed in semiconductor microwave design.

Partial Contents: The PN junction, PIN diodes and the theory of microwave operation, practical PIN diodes, binary state transistor drivers, fundamental limits of control networks, mathematical techniques and computer-aided design (CAD), limiters and duplexers, switches and attenuators,

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phase shifters and time delay networks, and appendices.

Available from Van Nostrand Reinhold Co., 135 West 50th St., New York, N.Y. 10020 576 pages, $28.50, Hardcover, Nov. 1981.

GaAs FET Principles And Technology

Edited by James DiLorenzo and Deen Khandelwal.

Drawing on contributed material from experts throughout the international community, this work is intended to provide the reader with a complete look at the science and art of design, fabrication, and application of GaAs FETs. Included are chapters on material technology, device technology, microwave circuit technology, digital integrated circuit technology and new physics concepts.

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Available from Artech House, Inc., 610 Washington St., Dedham, MA 02026. $45.00, Hard cover, 1982.

Introduction to Radio Frequency Design

By W.H. Hayward

This comprehensive yet basic treatment of the fundamental methods used in radio frequency design is intended for engineers, technicians and advanced radio amateurs. It prepares the reader to design HF, VHF and UHF equipment and to read and understand much of the current literature in this field. An emphasis is placed on simplicity of presentation. Frequent examples are used and comprehensive lists of references and suggested readings are provided at the ends of individual chapters. Mathematics is used as required to develop reader intuition for r.f. circuits and systems. Structured equation sets aid the reader in writing programs for small computers or hand-held programmable calculators. The book reviews traditional material from the perspective of the r.f. designer.

Contents: Low frequency transistor models, filter basics, coupled resonator filters, transmission lines, two-port networks, practical amplifiers and mixers, oscillators and frequency synthesizers, the receiver: an RF system.

Available from Prentice-Hall, Inc., Englewood Cliffs, NJ 07632, 400 pages, $27.95, Hard cover, 1982.

Practical RF Design Manual

By Doug Demaw

A plain language solid-state design text that emphasizes circuit explanation, anomalies and performance traits. Explains solid state design of RF communications circuits for transmitters and receivers from low frequency through UHF. Design approaches given along with practical examples of proven circuits with assigned component values. The text is built on practical experiences in design and laboratory testing as opposed to the singular theoretical treatment found in similar books. There is minimal emphasis on mathematics and strong emphasis on circuit explanation and performance traits.

Contents: Preface. Transmitter and Receiver Fundamentals. Frequency-Control Systems. Small-Signal RF Amplifiers. Large-Signal Amplifiers. Frequency Multipliers. Mixers, Balanced Modulators, and Detectors. IF Amplifiers, Filters and AGC Systems.

Available from Prentice-Hall, Inc., Englewood Cliffs, NJ 07632. 272 pages, $24.95, Hardcover, 1982.

Power FETs And Their Applications

By Edwin S. Oxner

This book covers the technology and applications of power Field-Effect Transistors. The book begins by comparing FETs with several power semiconductors and gives a brief history of power FET development. Numerous types of power FETs with their features, performance and characteristics are compared. A chapter on characterization and modeling should give the designer a better understanding of the performance of power FETs. The remainder of the book is dedicated to applications ranging across a wide range of interests.

Partial Contents: Types of power FETs. Fabrication of power FETs. Characterization and modeling of power FETs. Using the power FET in switching power supplies . . . audio power amplifiers . . . motor control . . . logic control . . . as a switch . . . in high frequency applications. Selecting the right FET for the right job.

Available from Prentice-Hall Inc., Englewood Cliffs, NJ 07632, 315 pages, $24.95, Hardcover, 1982. □

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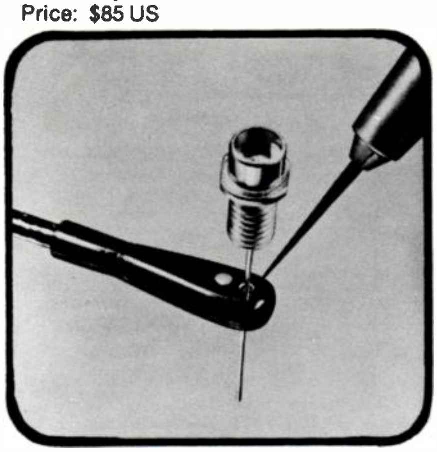

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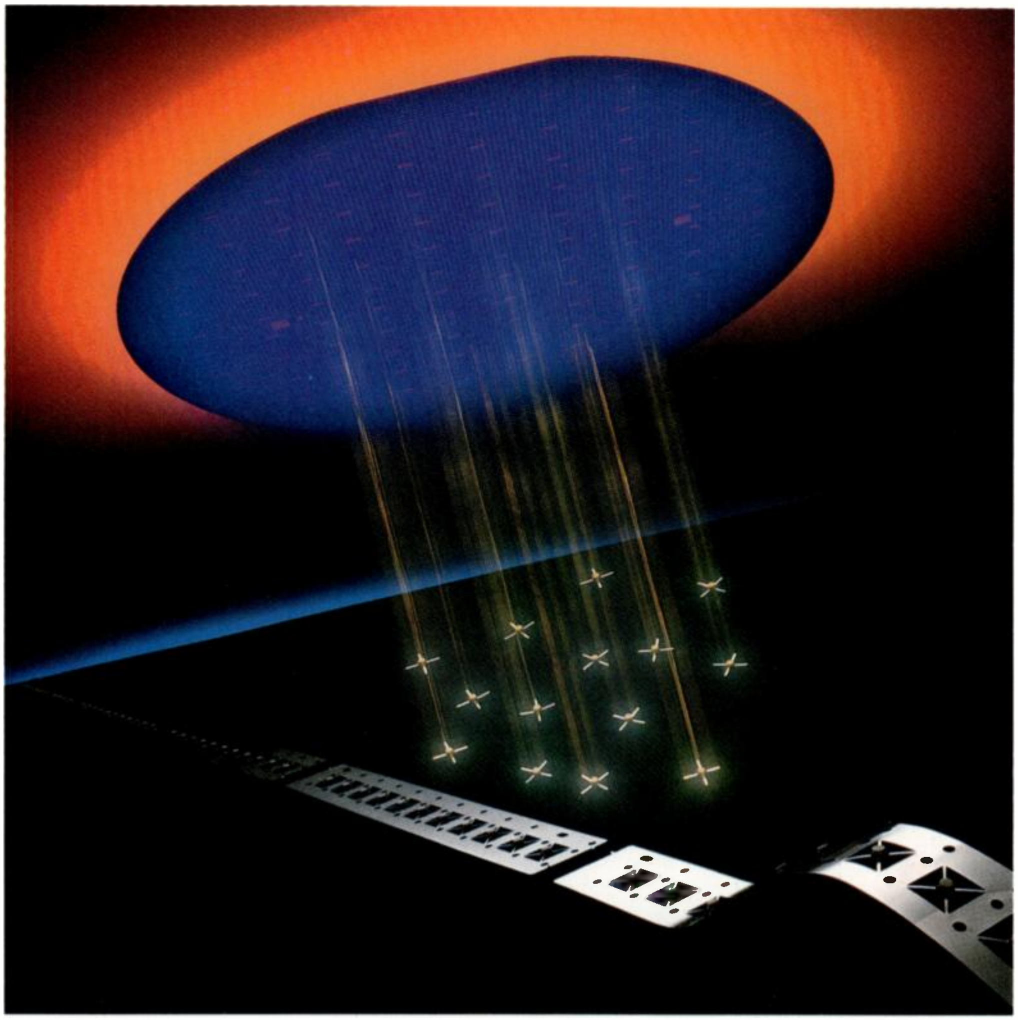

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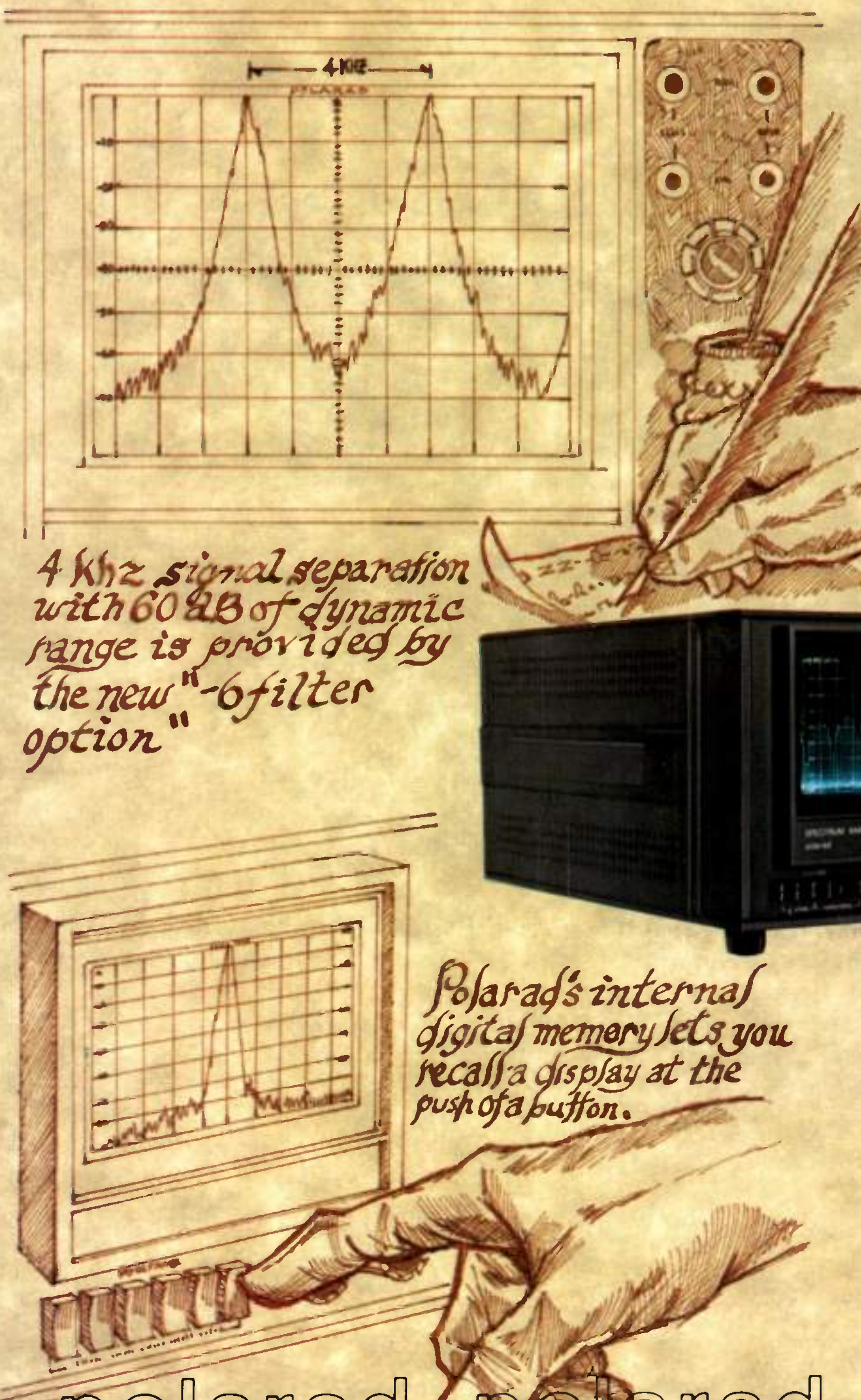

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