rf design

high frequency and analog engineering

January 1988

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Featured Technology — High Speed ADCs and DACs

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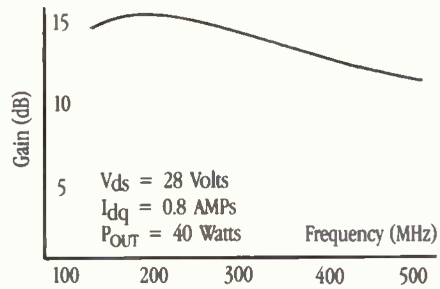

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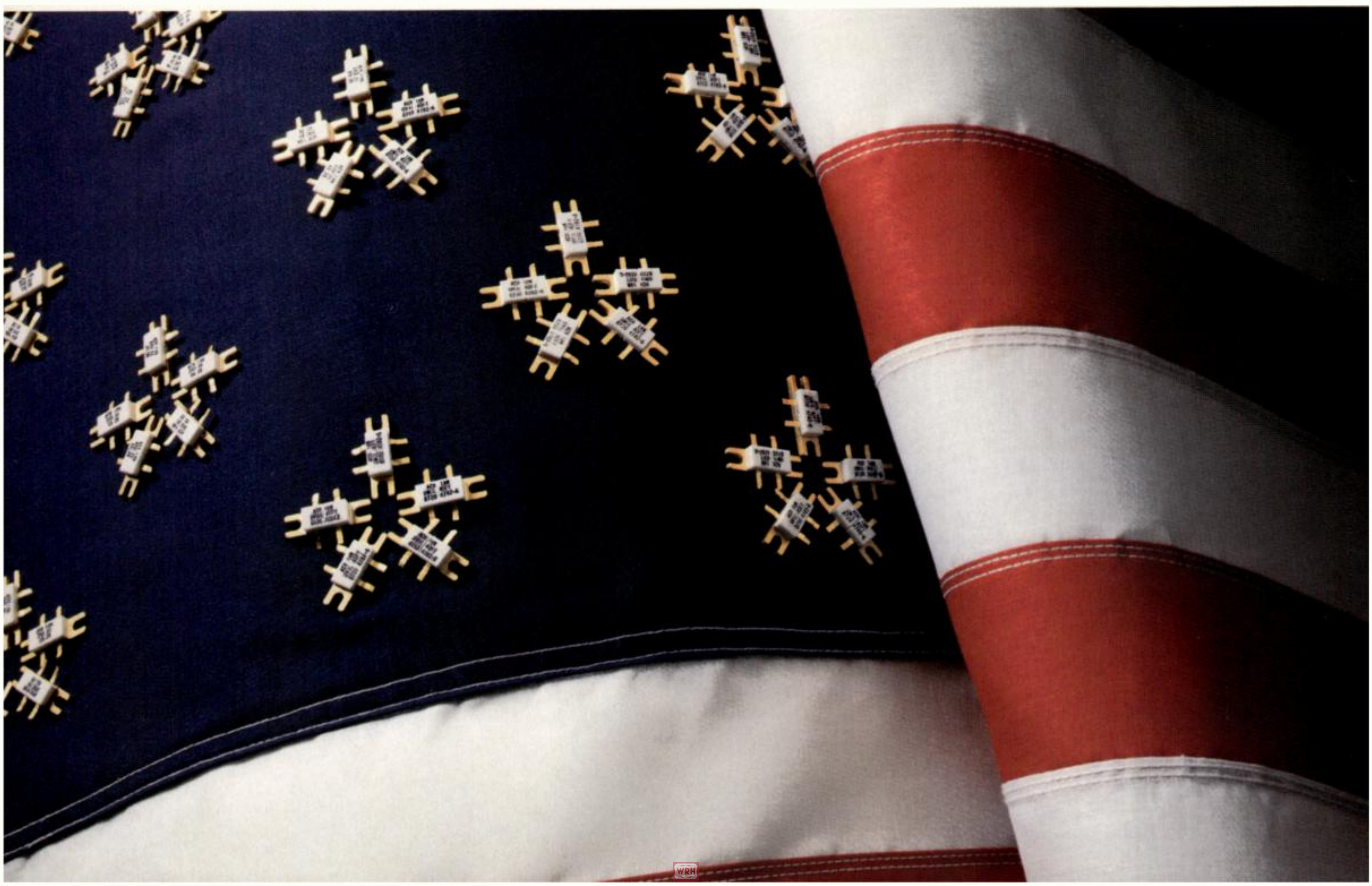

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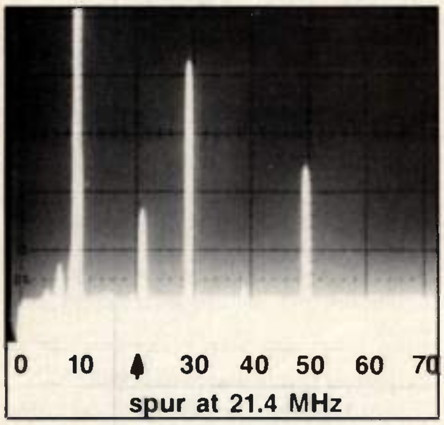

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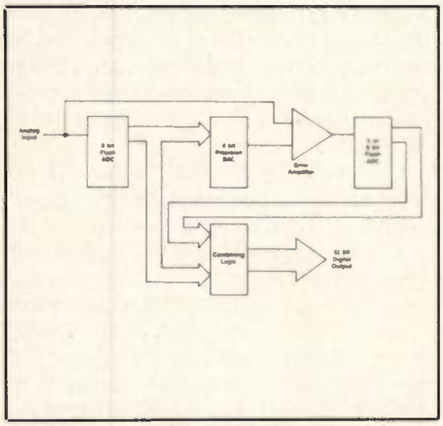

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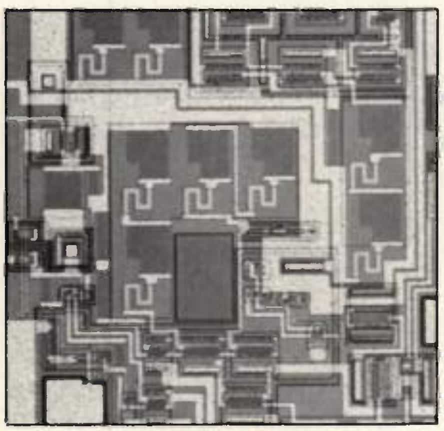

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Cover Story

Featured Technology Section

Departments

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rf editorial

A *High Speed* Beginning for 1988

By Gary A. Breed
Editor

To let everyone know we are serious about keeping pace with technology, we are starting the new year with an issue loaded with information on high speed techniques, a rapidly growing part of RF technology. Those of you involved in data communications or digital signal processing will find plenty of pertinent information, while the "radio" engineers among you might find some surprises in the articles on high speed A/D and D/A conversion and operational amplifiers.

Those surprises might include the 40 MHz R-C active filter described in the Cover Story. There is also plenty of basic information on the use of high speed ADCs and DACs. How about a receiver that is basically an antenna feeding an analog-to-digital converter? With new high speed circuits, this application is a reality, along with many more that were "dreams of the future" just a few years ago.

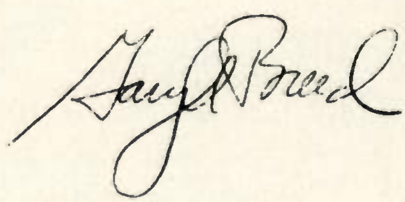
More high speed coverage is coming, too. Through the year, we will cover instrumentation, fast PLLs, position sensing, and data communications, in addition to the more traditional RF topics of RF power, audio circuits, microstrip design, electromagnetics modeling, and modulation techniques. These areas of emphasis will be complemented by a wide range of RF and analog topics, both fundamental and advanced. We want to make sure that engineers get *all* the information they need!

Where's the Action in 1988?

In July, we announced that *high speed* as well as high frequency circuit design is now considered part of *RF Design's* natural realm of coverage. Since then, our decision has been applauded by both engineers working in these areas, and by companies who make high speed products. Our ideas have even been copied, further evidence that we made the right decision.

My prediction for 1988 is that RF-like high speed circuits will be the growth leader in electronics, driven by the demand for data communications, precision instrumentation, and complex signal processing — all seeking higher operating speeds. Combined with solid performance in the more traditional RF applications, this year should be a good one for most *RF Design* readers and advertisers.

However, I suppose I should temper my enthusiasm for RF, no matter how strong the technology. There are a lot of factors involved in business beyond "mere" technology, such as international economics and politics. But as long as these factors are stable, 1988 looks very good from my vantage point. rf



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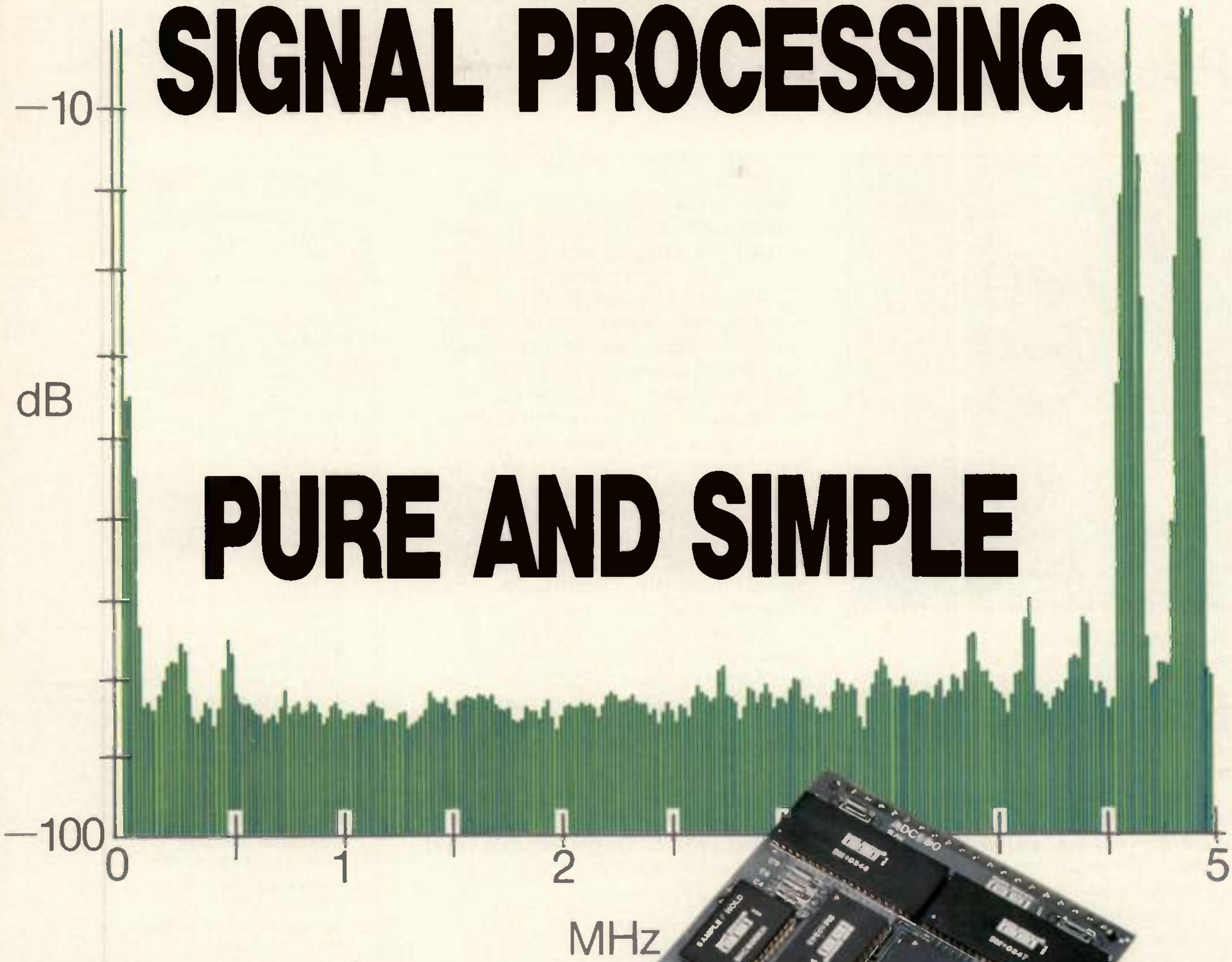

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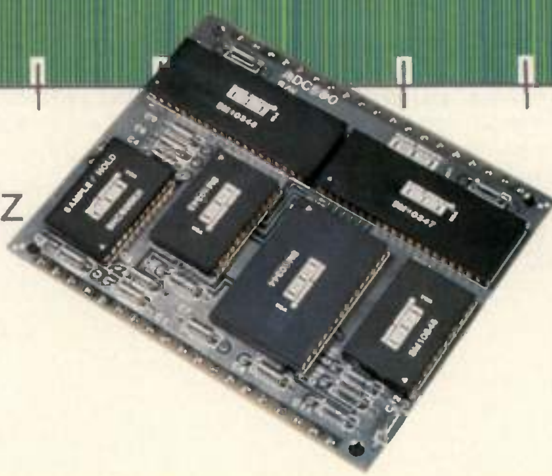

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Improving Data Conversion Productivity

Pockets of Prosperity

By Keith Aldrich
Publisher

Economists are saying that when the record of '87 is completely known,the electronics industry will be seen to have been in a recession.

That may be true as a generalization, but like all pictures painted with a broad brush, this one tends to cover some substantial differences between various specific electronics markets. If you're selling microprocessor chips to car makers, for instance, your sales are no doubt dropping with declining auto sales. But if you're selling fiberoptic drivers to makers of telecommunications equipment, chances are your sales curve is on a steep uphill climb.

Many of the "pockets of prosperity" on the electronics scene, like this one, are examples of a sweeping new technological trend which might be described as *high-speed electronics.* That is not exactly the same as "RF," which traditionally suggests some variation of radio communications (radar, paging, *et. al.*) — but it does imply the use of high frequencies in applications which have nothing to do with radios. Computers, data transmission, medical instrumentation, are just a few of the areas that are beginning to use RF and even higher frequencies for the sole purpose of making things work faster. And because there is a growing need for speed, these areas tend to be among those enviable pockets of prosperity.

Your own prosperity, of course, is defined by your own employment and productivity. The trend to high-speed electronics bodes well for the continued and increasing employment of RF engineers, or at least electronics engineers who can handle RF technology.

All of which adds up to a reassurance for readers of this magazine. You are in demand. Fear not. Go get 'em. Stay tuned to this magazine and you'll be in tune with the times.

Keith Aldrich

rf design

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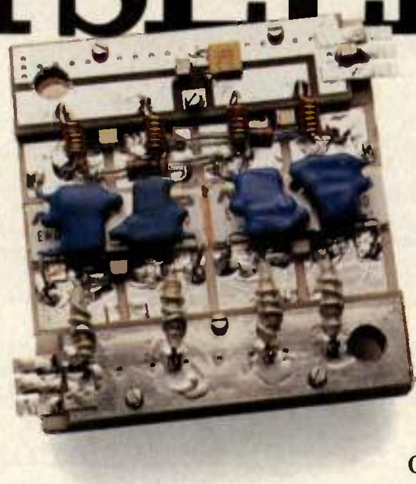

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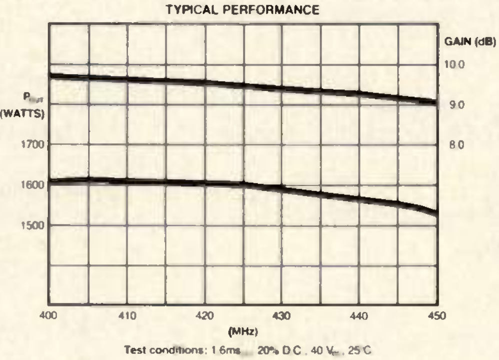

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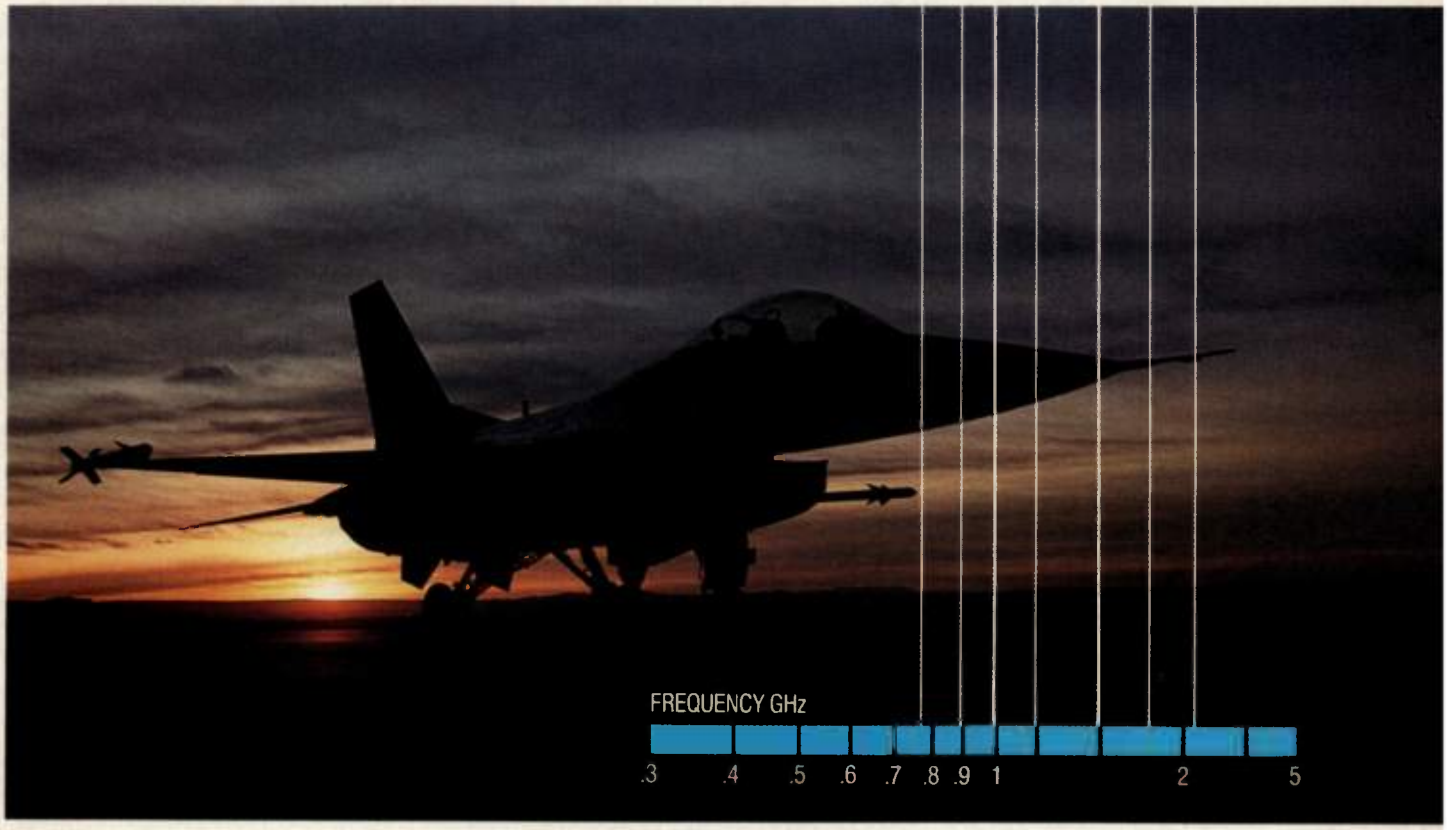

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INFO/CARD 11

rf letters

Letters should be addressed to: Editor, *RF Design*, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111.

Smaller Power Dividers: The Author's Response

Editor:

I would like to respond to a letter by Mr. Garner in the November issue where he correctly states that a power divider of similar size built on an alumina substrate outperforms my proposed device. This exactly illustrates the advantage of my design, since it is built on a G-10 circuit board which has a much lower dielectric constant than alumina; if it were implemented on alumina, its size would be considerably smaller.

Furthermore, Cohn's four-section power divider which Mr. Garner uses as an example of a better design can be improved by following the approach suggested by my article: replace the transmission line sections between isolation resistors by nonsynchronous transformers.

The purpose of my article was not to construct a power divider to replace all power dividers, but to illustrate a design technique where an impedance-matching circuit consisting of two or more cascaded transmission lines can often replace a single-section transmission line of longer overall length.

Peter Vizmuller
Motorola Canada

A Complimentary Commentary

Editor:

I recently had a very pleasant encounter with one of your advertisers. As a result of a hard disk crash, which is a very distressing event for an analog engineer, I lost all of the programs purchased from Etron RF Enterprises. I am most pleased to relate that one phone call to John Simmons resulted in the replacement of all lost programs. In this day and time it is rather exciting to receive this type of service coupled with the exceptional value that this series of programs represents.

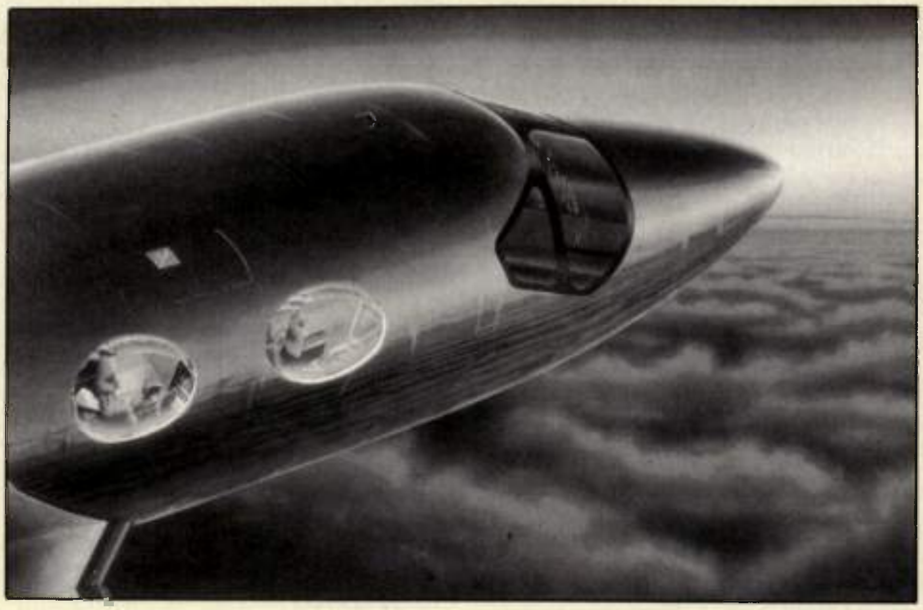
I thought I would let your know that you have some very good clients and I feel that your magazine serves a valuable purpose.

Keep up the good work.

Lothar A. Krause Jr.
Lintech Inc.

Help celebrate the 10th Anniversary of *RF Design* during 1988 — send us your observations, recollections, or philosophical musings about the past ten years of RF technology. We will print as many letters as we can.

Aviation Industry Uses Satellite Communications



The aviation industry will soon be getting real time communications, leading to a point where satellite transmission is being used for air traffic control communications, engine monitoring, dispatch of information, weather reports, crew change orders, and the selection of flight paths that will save the maximum amount of fuel. In addition, this system will enable the cabin crew to provide passengers with up-to-date information on connecting flights, departure times and gate locations.

One of the first applications of this type of communication will be achieved in part by a blade type antenna system for low speed data transmission via communications satellites. The antenna system, from Ball's Outreach family, is being built by Ball Aerospace in Boulder, CO, for Northwest Airlines. Northwest will install these systems in ten of its Boeing 747-400 aircraft. The first antenna is expected to be delivered by December 1988.

A second aeronautical Outreach antenna called Airlink™ is being developed by Ball as well. Airlink will provide telephone services and other voice communications as well as data transmission. By 1989, airlines that opt to enter satellite communications with data only systems for crews will have the option of upgrading their systems with an Airlink antenna. This antenna will help usher in a host of new passenger services, including both telephone and data services via satellite. Business flyers and others will be able to communicate with people all over the world via portable computers, facsimile machines or telephones. "These new services will be invaluable to executives who travel a lot and need to stay in touch with various corporate offices," said Richard Herring, President of Ball Aerospace Systems Division.

The external portion of the Airlink antenna system consists of two conformal antenna arrays mounted on opposite sides of the aircraft fuselage, a configuration that yields a minimum amount of drag and correspondingly small losses of inflight performance. This results into potential fuel savings compared with other designs requiring radomes. The antenna requires two 5 cm holes in the aircraft skin to accommodate the cable bundles connecting the antennas with phase shifters and other electronic components inside the aircraft.

Each antenna array consists of 16 radiating elements. On airplanes, each antenna is mounted at an angle of approximately 45 degrees on either side of the fuselage. From these locations, each antenna can steer its beam electronically through at least 60 degrees in any direction. The two antennas provide a gain of 12 dB over approximately 85 percent of the upper hemisphere. This results in good pattern coverage with reduced gain in the direction of the nose and tail.

Airlink incorporates a beam steering computer to activate the appropriate array and send commands to phase shifters to point beams in specified directions. The computer calculates satellite position from the aircraft's inertial navigation system data or automatically tracks satellites by analyzing received signal strength. The receive frequency range for the 16-element phased array antenna is from 1530 MHz to 1559 MHz while the transmit band is from 1631.5 MHz to 1660.5 MHz. A complete Ball Airlink system uses Collins satellite avionics.

The Airlink antenna is being developed by Ball under a $1 million contract from the International Maritime Satellite Organization. The first airlink is planned to be flown on a Federal Express DC-10 by mid 1988.

GAMI Launches Three Study Programs

Gorham Advanced Materials Institute (GAMI) of Gorham, ME, is planning to conduct three studies related to superconducting ceramics. The studies are designed to provide subscribers with marketing and technology advantages in the race to develop and commercialize superconducting ceramics. GAMI has been engaged in a program for the past six months and has developed high transition temperature superconducting ceramics in the $Y_1Ba_2Cu_3O_x$ perovskite phase utilizing several process variations. Additional information on these programs can be obtained by contacting Mr. Gregory L. Perron at (207) 892-5445.

IEEE Society to Meet at NBS

The initial meeting of the IEEE Instrumentation and Measurement Society, Precision Coaxial Connectors Subcommittee will be held at the National Bureau of Standards in Boulder, CO, on February 24, 1988. The subcommittee will extend IEEE Standard 287-1968 to cover coaxial connectors for precision electrical measurements above 18 GHz and update the standard for 14 mm and 7 mm connectors. Further information can be obtained from Harmon Banning of W.L. Gore at (302) 368-3700.

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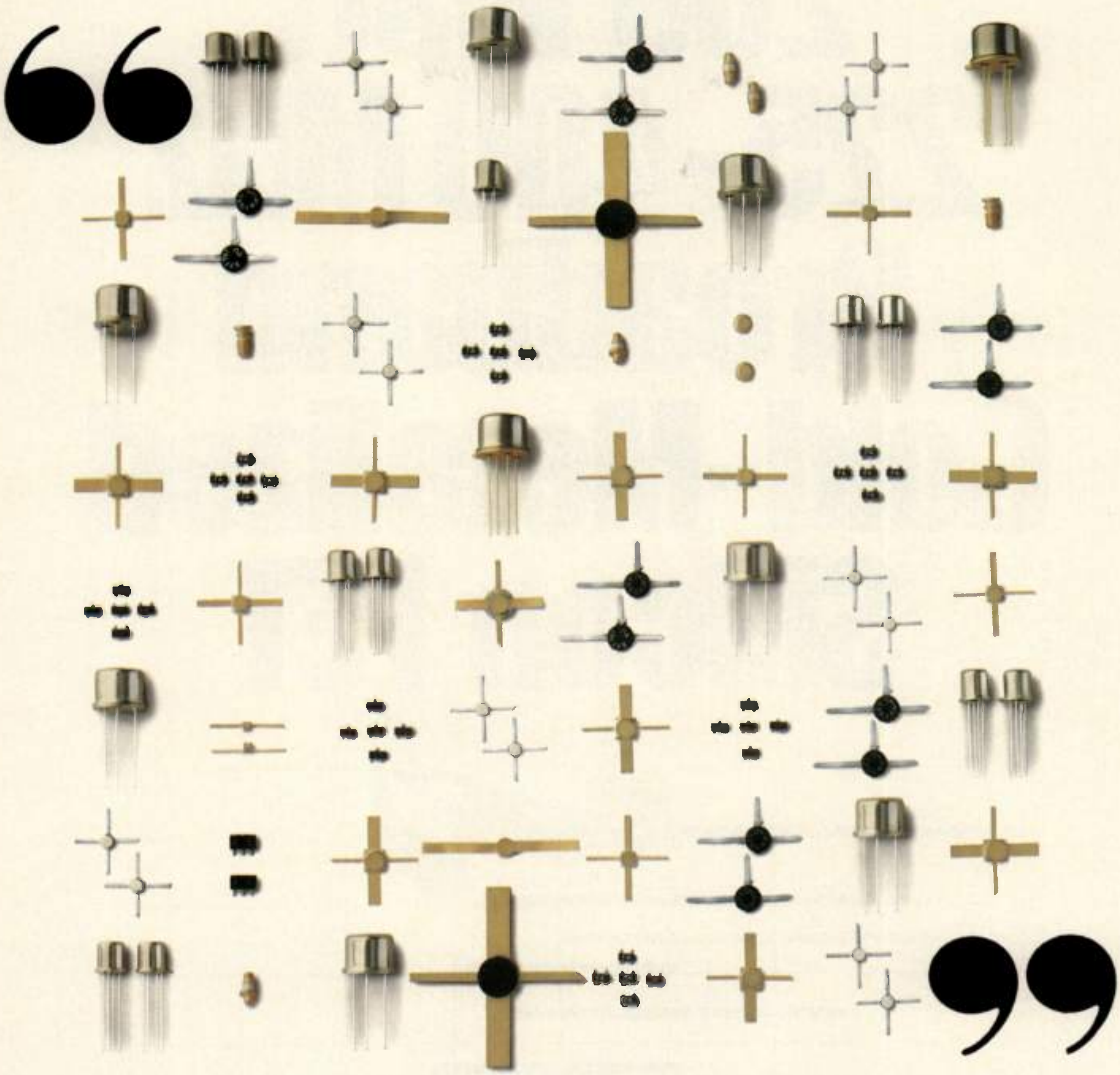

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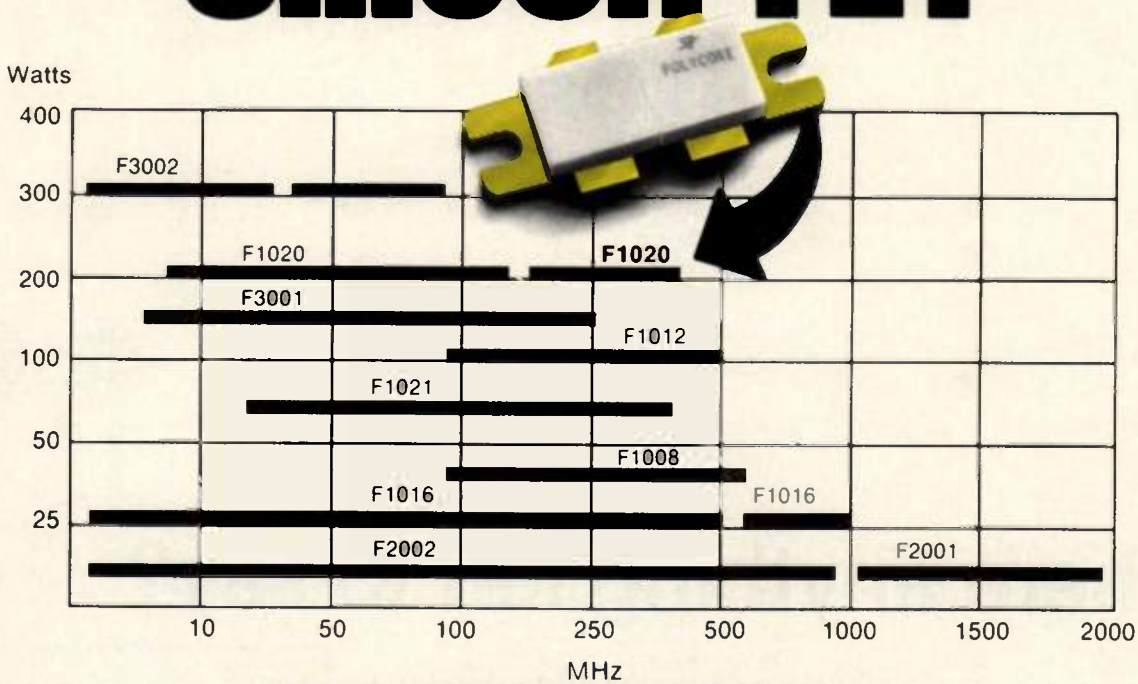

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Report Predicts Rise in Demand For EMC Products and Services

U.S. end-users demand for electromagnetic compatibility (EMC) products and services topped $1 billion in 1985 and will advance at a real, annual growth of 8.5 percent and reach over $1.5 billion in 1990. At least six individual EMC product/service types will outstrip this aggregate growth rate however, and will advance at rates anywhere between 10 percent up to 23.5 percent annually. A 194-page analysis of the electromagnetic compatibility products and services market in the U.S. is available for $1775 by contacting Frost & Sullivan, Inc., at (212) 233-1080.

FPS and Clemson University Announce Agreement

Floating Point Systems, Inc. announced a research and development agreement with Clemson University, Clemson, South Carolina, to create software development tools which can be used on the FPS T Series supercomputer. Clemson will provide support from its Mathematical Sciences and Computer Science departments, and from the Division of Computing and Information Technology; FPS will provide the necessary hardware and technical support. Clemson recently received a university research grant from the Office of Navy Research. The grant provided funding in support of the purchase of the FPS T 20 supercomputer and was designed to promote excellence in the areas of discrete math and computational analysis.

Quartz Conference Proceeding Now Available

Volume 2 of the Proceedings of the Electronic Industries Association's 9th Quartz Devices Conference and Exhibition held August 25-27, 1987 in Kansas City is now available. Volume 1 was available at the conference and contained eleven of the seventeen papers presented. This publication contains the remaining six technical papers in a variety of topics including: A Digital Compensation Technique of Crystal Oscillators, and Crystal Fiber Design. Volume 2 may be ordered prepaid ($45) from the Electronic Industries Association's Component Group at 2001 Eye St. N.W., Washington, DC 20006.

Epsco Receives $1.1 M

Epsco, Inc. of Westwood, MA, announced the receipt of a $1,133,987 contract from the U.S. Naval Air Systems Command for the production of CV2461A/A signal data converters used on the U.S. Navy's P-3C anti-submarine warfare aircraft program. The data converter provides the interface between the P-3C aircraft digital computer and its synchro-transmitters and receivers. The converter has 32 synchro input channels and 16 synchro output channels.

Rohde and Schwarz Move to DC Area

Rohde and Schwarz have moved their corporate headquarters from Lake Success, NY to Lanham, MD, east of Washington, DC. Their new address is Rohde and Schwarz, 4425 Nicole Drive, Lanham, MD 20706. Their telephone number is (301) 459-8800.

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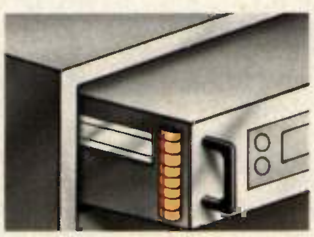

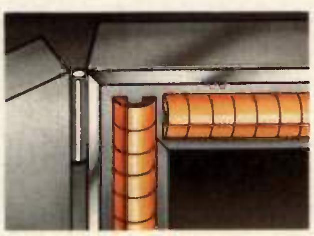

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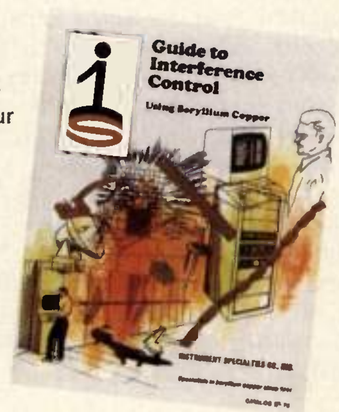

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Ball Awarded $14 M

Ball Corporation's aerospace systems division will build all-light level TV subsystems for the Air Force's AC-130U gunship program under a contract awarded by the North American Aircraft Operations of Rockwell International Corp., the program's main contractor. Rockwell will install a single turreted subsystem underneath the left wheel faring of each of a dozen AC-130U aircraft. The subsystem will be used for surveillance, navigation and battlefield applications such as target detection, target acquisition, target recognition, weapons fire control and laser designation.

Ball's design incorporates active laser illumination, which enables the system to "see" as well on a moonless night as it does during the day. The advanced sensor subsystem also includes a 13" reflecting telescope, a low light level television camera, a cryocooled gallium arsenide laser illuminator, a laser rangefinder designator, a video target tracker, a control panel and a stabilization mechanism. This mechanism isolates the sensors from the vibrations of the aircraft's four turboprop engines and from the effects of air turbulence in flight. Ball will deliver the first subsystem in January 1989 and will build the others over a three year period.

CE Awarded McDonnell Douglas Contract

Cincinnati Electronics (CE) has been awarded contracts by McDonnell Douglas Corp. to manufacture and test range safety receivers for two U.S. space launch vehicle programs, the USAF Medium Launch Vehicle (MLV/Delta II) and the McDonnell Douglas Commercial Delta. The agreements call for CE to provide 70 range safety receivers. The total combined value of these contracts is $2 million and authorization for the first phase, worth approximately $600,000 has been given. The range safety receiver is a device used to terminate the flight of a space launch vehicle should it veer off course and threaten range personnel or buildings.

DTL Expands EMI/EMC Testing Department

Detroit Testing Laboratory, Inc. (DTL), Oak Park, MI, announced the expansion of its EMI/EMC testing department to include approximately 12,000 square feet of laboratory facilities and an open test site near Willow Run airport, Belleville, MI.

European Electronics Market to Peak in 1988

1988 is forecast by Benn Electronics to be a year of high growth for the West European Electronics market. In the 15th edition of their *Yearbook of West European Electronics Data*, Benn Electronics estimates that the market for electronic equipment and components will reach $144 billion (U.S.) at constant 1986 values and exchange rates, a real growth of 7.5 percent over 1987. However, 1988 is seen as a peak, with growth tailing off again from 1989 to 1991 at an average of 4 percent per annum over the three period. More information on this publication can be obtained from Benn Electronics Publications Ltd., P.O. Box 28, Luton, LU2 OED, England. Tel: (0582) 421981. It is priced at $625 (U.S.).

rf calendar

January 20-21, 1988
San Diego Electronics Show
Del Mar Fairgrounds, San Diego, CA
Information: Epic Enterprises, Show Management, 3838 Camino Del Rio North-Suite 164, San Diego, CA 92108; Tel: (619) 284-9268

February 7-9, 1988
ADEE 88
Rivergate Exhibition Center, New Orleans, LA
Information: Show Manager, ADEE West, Cahners Exposition Group, 1350 East Touhy Ave., P.O. Box 5060, Des Plaines, IL 60017-5060. Tel: (312) 299-9311

February 10-12, 1988
RF Technology Expo '88
Disneyland Hotel, Anaheim, CA
Information: Linda Fortunato, Cardiff Publishing Company, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111; Tel: (303) 220-0600; (800) 525-9154

February 23-25, 1988
NEPCON West '88
Anaheim Convention Center, Anaheim, CA
Information: Jerry Carter, Cahners Exposition Group, 1350 East Touhy Ave., P.O. Box 5060, Des Plaines, IL 60017-5060; Tel: (312) 299-9311

March 3-4, 1988
33rd International SAMPE Symposium & Exhibition
Anaheim Convention Center, Anaheim, CA
Information: Marge Smith, P.O. Box 2459, Covina, CA 91722; Tel: (818) 331-0616

March 7-10, 1988
33rd International SAMPE Symposium & Exhibition
Anaheim Convention Center, Anaheim, CA
Information: Marge Smith, P.O. Box 2459, Covina, CA 91722; Tel: (818) 331-0616

May 9-11, 1988
38th Electronic Components Conference
Biltmore Hotel, Los Angeles, CA
Information: EIA, 2001 Eye St. N.W., Washington, DC 20006

May 10-12, 1988
Electro '88
Bayside Exposition Center, Boston World Trade Center, Boston, MA
Information: Electronic Conventions Management, 8110 Airport Boulevard, Los Angeles, CA; Tel: (213) 772-2965

May 25-27, 1988
1988 IEEE MTT-S International Microwave Symposium
Javits Auditorium, New York City, NY
Information: Charles Buntschuh, Narda Microwave Corp., 435 Moreland Road, Hauppauge, NY 11788; Tel: (516) 231-1700

June 1-3, 1988
42nd Annual Frequency Control Symposium
Stouffer Harborplace Hotel, Baltimore, MD
Information: Raymond L. Filler, Frequency Control and Timing Branch, Department of the Army, Electronics Technology and Devices Laboratory, Fort Monmouth, NJ 07703-5000

rf courses

The George Washington University

SAW Devices and their Signal Processing Applications
February 22-25, 1988, Washington, DC
Electromagnetic Interference and Control
February 22-26, 1988, Washington, DC
Fiber-Optics System Design
February 29-March 2, 1988, Washington, DC
Electronic Countermeasures
February 29-March 4, 1988, Washington, DC
Microwave Radio Systems
March 7-8, 1988, Washington, DC
Hazardous RF Electromagnetic Radiation
March 16-18, 1988, Washington, DC
Frequency-Hopping Signals and Systems
March 21-23, 1988, Washington, DC
Elements of Optical Warfare
March 30-April 1, 1988, Washington, DC
Spread-Spectrum Communications Systems
April 4-8, 1988, Washington, DC
Grounding, Bonding, and Shielding
April 7-8, 1988, Washington, DC
Modern Communications and Signal Processing
April 18-22, 1988, Washington, DC
Introduction to Receivers
April 18-19, 1988, Washington, DC
Modern Receiver Design
April 20-22, 1988, Washington, DC
Information: Shirley Forlenzo, Continuing Education Program, George Washington University, Washington, DC 20052; Tel:(800) 424-9773, (202) 994-8530

Besser Associates

Microwave Circuit Design I: Linear Circuits
June 20-24, 1988, Los Angeles, CA
August 15-19, 1988, Baltimore, MD
Microwave Circuit Design II: Non-linear Circuits
August 22-26, 1988, Baltimore, MD
Information: Les Besser, Besser Associates, Inc., 3975 East Bayshore Road, Palo Alto, CA 94303; Tel: (415) 969-3400

UCLA Extension

Modern Microwave Techniques
April 25-28, 1988, Los Angeles, CA
Information: UCLA Extension, P.O. Box 24901, Los Angeles, CA 90024; Tel:(213) 825-1901; (213) 825-1047; (213) 825-3344

Test Systems, Inc.

MIL-STD-1553
May 10-11, 1988, Phoenix, AZ
Information: Leroy Earhart, Test Systems, Inc., 217 W. Palmaire, Phoenix, AZ 85021; Tel: (602) 861-1010

Interference Control Technologies, Inc.

Grounding and Shielding
February 22-26, 1988, Atlanta, GA
March 7-11, 1988, Palo Alto, CA
March 21-25, 1988, Hilton Head, SC
April 11-15, 1988, San Diego, CA
April 25-29, 1988, Chicago, IL
Tempest Facilities
April 12-15, 1988, Washington, DC
Intro to EMI/RFI/EMC
March 15-17, 1988, Orlando, FL
Information: Penny Caran, Registrar, Interference Control Technologies, Inc., State Route 625, P.O. Box D, Gainsville, VA 22056; Tel:(703) 347-0030

Integrated Computer Systems

Digital Signal Processing
March 1-4, 1988, Ottawa, Canada
March 8-11, 1988, San Diego, CA
March 22-25, 1988, Washington, DC
April 26-29, 1988, Toronto, Canada
May 10-13, 1988, Washington, DC
Image Processing and Machine Vision
February 23-26, 1988, Ottawa, Canada
February 23-26, 1988, San Diego, CA
April 12-15, 1988, Washington, DC
April 26-29, 1988, Palo Alto, CA
Hands-On Programming in C
February 16-19, 1988, Montreal, Canada
Hands-On Advanced Programming in C
February 23-26, 1988, San Diego, CA
March 8-11, 1988, Ottawa, Canada
April 5-8, 1988, Washington, DC
April 19-22, 1988, Los Angeles, CA
May 10-13, 1988, Toronto, Canada
May 24-27, 1988, Palo Alto, CA
Fiber Optic Communication
February 23-26, 1988, Washington, DC
March 15-18, 1988, Palo Alto, CA
Information: Barbara Fischer, Integrated Computer Systems, 5800 Hannum Avenue, P.O. Box 3614, Culver City, CA 90321-3614; Tel:(800) 421-8166, (213) 417-8888

Compliance Engineering

Compliance Seminars: EMI, Safety, ESD, Telecom
April 19-22, 1988, Chicago, IL
June 7-10, 1988, Boston, MA
Information: Compliance Engineering, 593 Massachusetts Avenue, Boxborough, MA 01719. Tel: (617) 264-4208

EMC Services, Inc.

EMI Control in Switched Mode Power Supplies
February 17-19, 1988, San Diego, CA
June 27-30, 1988, Boston, MA
Filter Design for Switching Supplies
February 22-23, 1988, San Diego, CA
Information: Mark Nave, EMC Services, 11833 93rd Avenue North, Seminole, FL 33542. Tel: (813) 397-5854

Georgia Institute of Technology

Principles of Pulse Doppler Radar:
High, Medium and Low PRF
February 23-25, 1988, Atlanta, GA
Infrared Technology and Systems Applications
February 24-26, 1988, Atlanta, GA
Information: Deidre Mercer, Education Extension Services, Georgia Institute of Technology, Atlanta, GA 30332-0385. Tel: (404) 894-2547.

Southeastern Center for Electrical Engineering Education

Antennas: Principles, Design, and Measurements
March 2-5, 1988, St. Cloud, FL
August 2-5, 1988, San Diego, CA
Information: Ann Beekman, SCEEE, 1101 Massachusetts Ave., St. Cloud, FL 32796. Tel: (305) 892-6146

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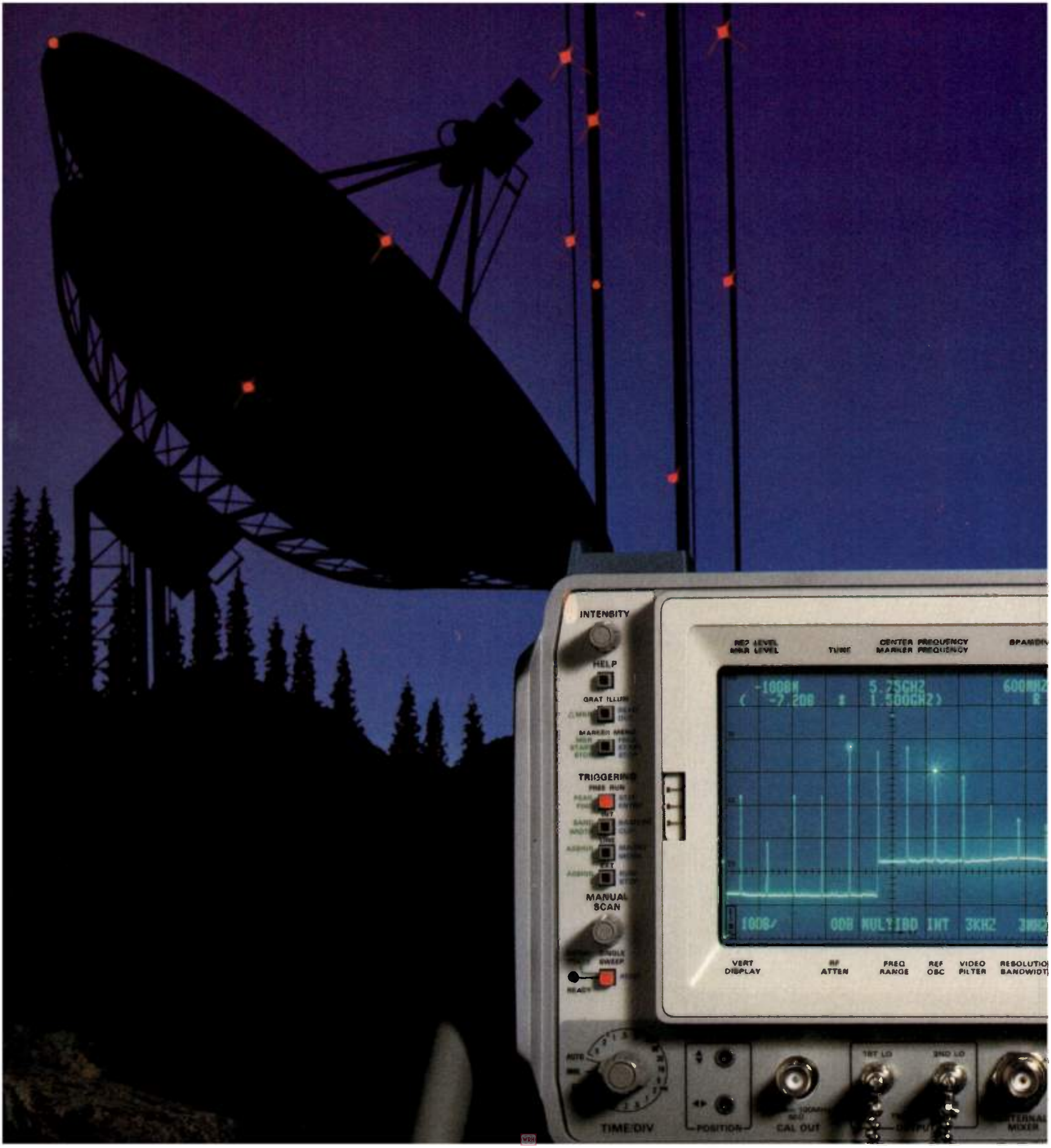

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High Speed Monolithic Op Amps: New RF Building Blocks

By Scott Evans and David Potson
Comlinear Corporation

One of the characteristics of RF technology is the continual increase in functionality demanded of new designs; not only must your RF systems do more, but they must do it in smaller packages with less power. This evolution in functionality is occurring in components and building blocks such as MMICs, filters, and most recently, the monolithic op amp — a device previously reserved only for video speed and slower systems. The design and process technologies have now matured to the point where monolithic op amps provide performance that often surpasses alternative designs.

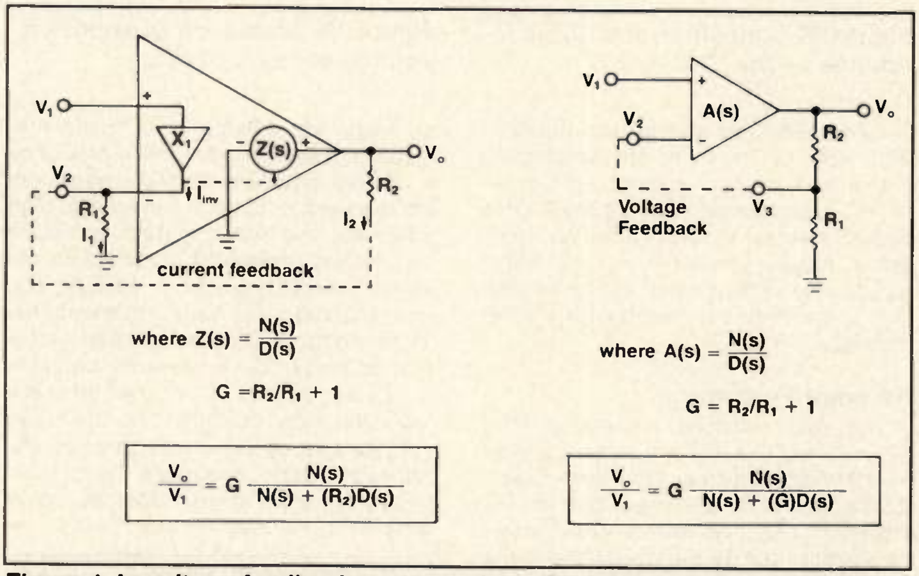

Figure 1. In voltage feedback op amps the poles of the response are scaled by the gain setting whereas in the current feedback op amp, the poles are scaled only by R_2 which is constant.

Remarkably, the op amp itself is older than the transistor. Original implementations constructed using tubes had bandwidths of only a few kHz and were used primarily in analog computers. Improvements in the speed of the parts has traditionally been through improved semiconductor process technology. As transistor f_Ts improved, the op amps improved. Unfortunately, process improvements could not keep pace with engineering needs for speed. Hybrids were a partial solution in that high speed PNP and NPN transistors could be put together on a substrate, thereby improving performance. Design modifications such as AC feedforward were also tried, but resulted in tradeoffs in functionality (optimum performance in inverting mode only) and in reproducibility (products which were very sensitive to transistor and environmental changes). However, even this was not enough. Basic topology improvements were needed.

Current Feedback

In 1982, the CLC103 was introduced by Comlinear. This op amp architecture eliminated the key performance deficiencies of the older architectures while bringing many new benefits(1). The basic design utilizes current feedback instead of voltage feedback (see Figure 1).

As can be seen from the transfer function, the current feedback architecture has a dynamic response which, unlike the traditional design, is relatively independent of closed loop gain setting. The result is a virtual elimination of the "gain bandwidth product" and a true DC-coupled bandwidth which exceeded 150 MHz over a wide gain range. In addition, many other performance measures were dramatically improved; for example, settling times broke the 100 ns barrier and fell to 10 ns, slew rates reached 6000 V/us, plus the need for external compensation was eliminated yielding consistent results in a production environment.

Due to the limitations in monolithic processes for high-speed op amps, the CLC103 was of hybrid construction. Other current feedback hybrids followed offering better DC performance, tighter settling, higher bandwidths, and lower cost. But even with such design solutions, the usage in RF designs was often limited to typical DC-coupled designs such as data conversion, where alternative designs were impractical.

In the monolithic arena, process technology continued to evolve and yielded a few basic technologies appropriate for high-speed op amps, including GaAs and complementary bipolar using either dielectric or junction isolation. Unfortunately, each process has limitations which degrade performance. For example, gallium arsenide op amps have been introduced which have gain bandwidths of up to 350 MHz (17.5 MHz bandwidth at gain of 20), but they have excessive noise at low frequencies (0.9 mV rms referenced to the input).

Dielectric isolation, which uses a dielectric well to isolate the transistors to improve the bandwidth of the PNP transistors has yielded amplifiers having gain bandwidth products on the order of 600 MHz (30 MHz bandwidth at a gain of 20). Unfortunately, charge storage effects limit settling performance to not much under 100 ns for most conditions.

CLC400 and CLC401 Op Amps

Through the combination of the current feedback topology and a new superior monolithic process technology, two new monolithic RF op amps have been developed, the CLC400 and the CLC401. The CLC400, with its −3 dB bandwidth of 200 MHz, is designed for low-gain ($A_v = \pm 1$ to ± 8) applications and the CLC401, featuring a −3 dB bandwidth at a gain of +20 of 150 MHz (see Figure 2), is designed for high-gain applications ($A_v > 7$). Both pro-

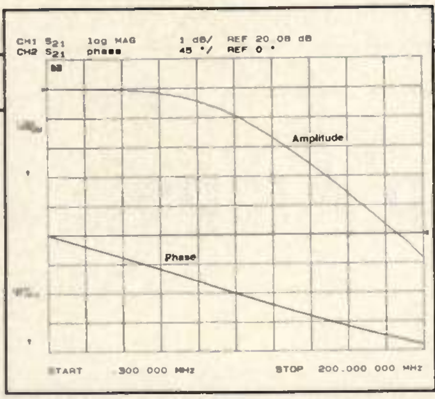

Figure 2A. Amplitude and phase response of the CLC400.

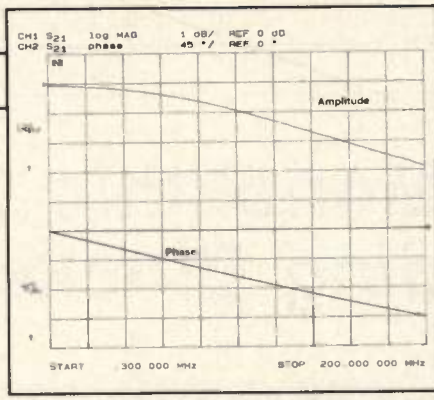

Figure 2B. Amplitude and phase response of the CLC401.

ducts feature 10 ns settling to 0.1 percent. (See table 1.) The monolithic process is one of the fastest complementary bipolar processes available. The f_Ts are 4 GHz and 2.5 GHz for the NPN and PNP transistors, respectively. Vertical construction isolates the various junctions and is the key to the wide bandwidth of the PNP transistor.

Relevant Features

The most obvious features of the CLC400 and CLC401 are their very wide −3 dB bandwidths (see Figure 2) and fast 2.5 ns rise and fall times. But for RF engineers, nearly as interesting as the raw bandwidth may be the ability to set the amplifier's voltage gain by changing only one resistor. The benefit is that system-level changes affecting required amplifier gain are easily accommodated without having to change or add amplifiers or attenuators.

True DC coupling is another salient feature. Here, DC means DC — not a few kHz as is often the case with other RF amplifiers. More and more RF designs are requiring DC coupling; one need only look at the growing use of data conversion components to see this. For these applications, an RF op amp is the obvious choice. Of course, a DC blocking capacitor may be used in applications needing AC coupling.

Though not always scrutinized by the RF world, settling time is one of the most revealing op amp parameters. Many consider it the "acid test" of an op amp design since good settling performance requires good performance in many other areas, such as phase linearity, harmonic distortion, and gain flatness. Both the CLC400 and CLC401 settle in 10 ns to 0.1 percent. The CLC400 is guaranteed to settle to 0.05 percent in 15 ns or less. In addition, the closed loop characteristics of the RF op amp provide very low intermodulation distortion over a wide bandwidth.

Comparison To Hybrids

Monolithic and hybrid current feedback op amps are different in a number of respects. The key performance difference is in drive capability. Hybrid devices are still required for large signal swings, high slew rates, and high output currents since the fastest monolithic processes are limited in these respects. (In addition, current feedback's elimination of gain bandwidth product is more pronounced in hybrid op amps than in currently available monolithic devices.) Of course, price is a key difference; monolithic op amps are half the cost of the lowest cost hybrids. Although many engineers have used hybrid op amps in their designs, many were willing to sacrifice performance for cost and forego the op amp solution. Now, with a greatly reduced price, many more designers can enjoy the benefits of RF op amp technology.

Applications

The number of RF design applications seems to grow daily(2). As more and more engineers recognize the benefits of the RF op amp, the applications will continue to grow. Sometimes the op amp design will provide a solution that is difficult to otherwise achieve. In other instances, board space savings or the reduction in component count is the motivation.

A good example of a quick op amp design solution having outstanding performance is the op amp-based peak detector, a circuit function required in applications ranging from ultrasound to radar cross sectioning. Shown in Figure 3 is an implementation of this circuit using the CLC401. Peak signal levels can be captured in as little as 50 ns. Since the CLC400 and CLC401 are immune to input overdrive, they will not be damaged by input signals causing the output to saturate. When overloads do occur, the op amp recovers in less than 10 ns. For very

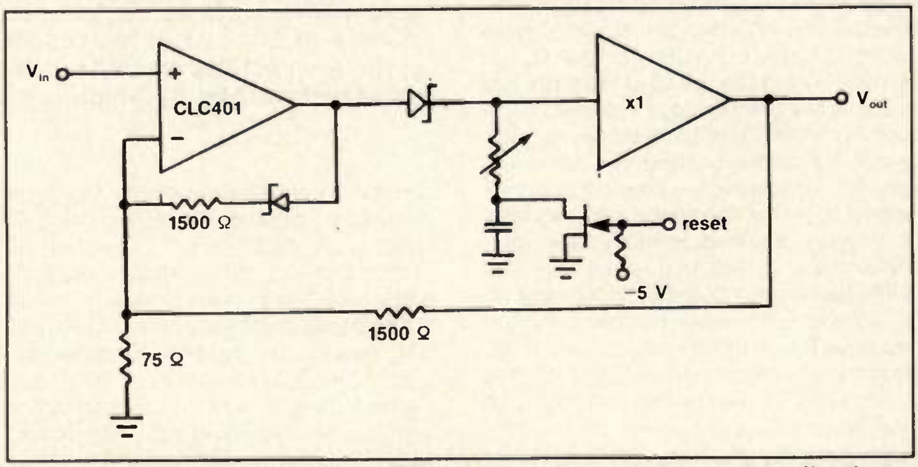

Figure 3. RF op amps provide quick solutions in peak detector applications.

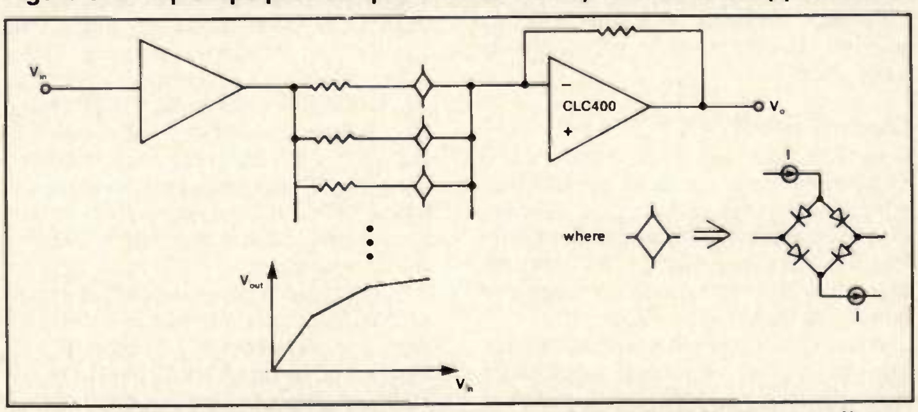

Figure 4. Nonlinear elements can be used to provide the nonlinear response needed in log amplifiers and VCO linearization circuits.

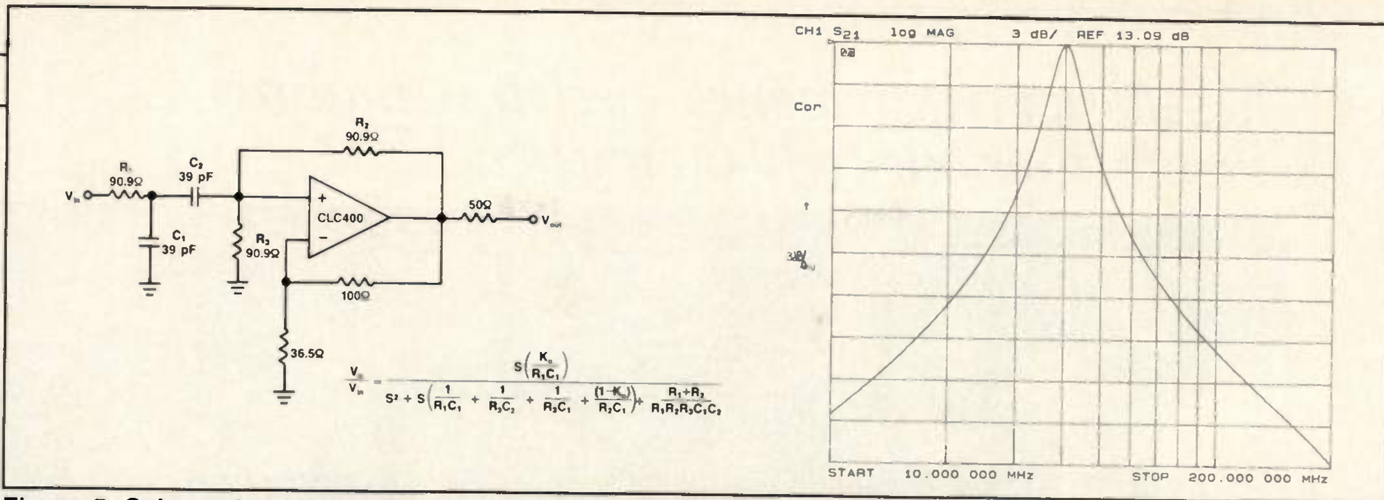

Figure 5. Schematic and amplitude response of the 40 MHz bandpass filter.

Feature	CLC400 (low gain)	CLC401 (high gain)
−3 dB bandwidth (2 Vpp)	200 MHz (Av=2)	150 MHz (Av=20)
linear phase deviation	0.2° (to 50 MHz)	0.2° (to 75 MHz)
harmonic distortion	−80 dBc at 1 MHz	−68 dBc at 1 MHz
	−60 dBc at 20 MHz	−45 dBc at 20 MHz
group delay	1.6 ns	2.5 ns
group delay distortion	150 ps (to 75 MHz)	100 ps (to 50 MHz)
slew rate	700 V/us	1200 V/us
rise/fall time	1.6 ns	2.5 ns
settling time (0.1%)	10 ns	10 ns
input offset voltage	2 mV	3 mV
output voltage/current	3.5 V/70 mA	3.5 V/70 mA
supply power (Vcc=±5 V)	150 mW	150 mW
internal compensation	yes	yes
short-circuit protected	yes	yes
over-voltage protected	yes	yes
immune to latchup	yes	yes
package AJP	8-pin plastic DIP	8-pin plastic DIP
package AID/AMD	8-pin sidebrazed ceramic DIP	8-pin sidebrazed ceramic DIP
gain range	±1 to ±8	±7 to ±50
pricing	$15.50 (100s)	$15.50 (100s)

Table 1. Key specifications

large input signals ($V_{in}>V_{cc}$), the inputs to the op amps may be clamped with fast-acting diodes.

Another useful op amp application involves creating a nonlinear amplitude response by using diodes or other nonlinear elements to provide a nonlinear gain-setting resistance (see Figure 4). Applications include log amplifiers, VCO linearization circuits, and CRT gamma correction circuits(3). RF op amps are also used as IF amplifiers. The wide bandwidth, linear phase, and low intermodulation distortion provide a very wide spurious-free dynamic range. Also, flexibility in adjusting the gain proves very useful.

Finding greater usage are quadrature amplitude modulated (QAM) communication systems. Of course, in this case, RF op amps are used to drive the I and Q channel A/D converters. The bandwidth, phase linearity, and gain flatness needed for low bit error rates are easily provided by the new RF op amps. Active filters are easily constructed using operational amplifiers (4, 5). Many designers have expressed the desire to eliminate inductors from their filter circuits or to have a well-controlled gain response that is not dependent upon transistor parameters. The circuit and amplitude response shown in Figure 5 are of a bandpass filter with a center frequency of 40 MHz.

The filter topology used is the KRC topology which keeps reactive elements out of the feedback path, which simplifies stability criteria with the current feedback op amp topology. The transfer function presented assumes an infinitely fast op amp — an approximation that is valid for center frequencies well below the op amp bandwidth. For filters working outside this assumption, as in the circuit shown, one needs to account for the time delay through the op amp (1.6 ns). Other filter functions may be implemented such as high pass, low pass, and band stop.

References

1. S. Evans, "A New Approach to Op amp Design," *RF Design*, September 1985.
2. "OA-7, Circuit Guide for Current Feedback Op Amp," Comlinear Corporation application note, 1987.
3. D. Potson, R. S. Hughes, "Extremely Fast Log Amp Handles Narrow Pulses," *Microwaves and RF*, April 1985.
4. A. Budak, *Passive and Active Network Analysis and Synthesis*, Houghton Mifflin Company, Boston, 1974.
5. IEEE Transactions on Circuits and Systems, volume CAS-27, number 12, pages 1155-1163, December 1980.

About the Authors

Scott Evans is product marketing engineer and David Potson is manager of applications engineering at Comlinear Corporation, 4800 Wheaton Drive, Fort Collins, CO 80525.Tel: (303) 226-0500.

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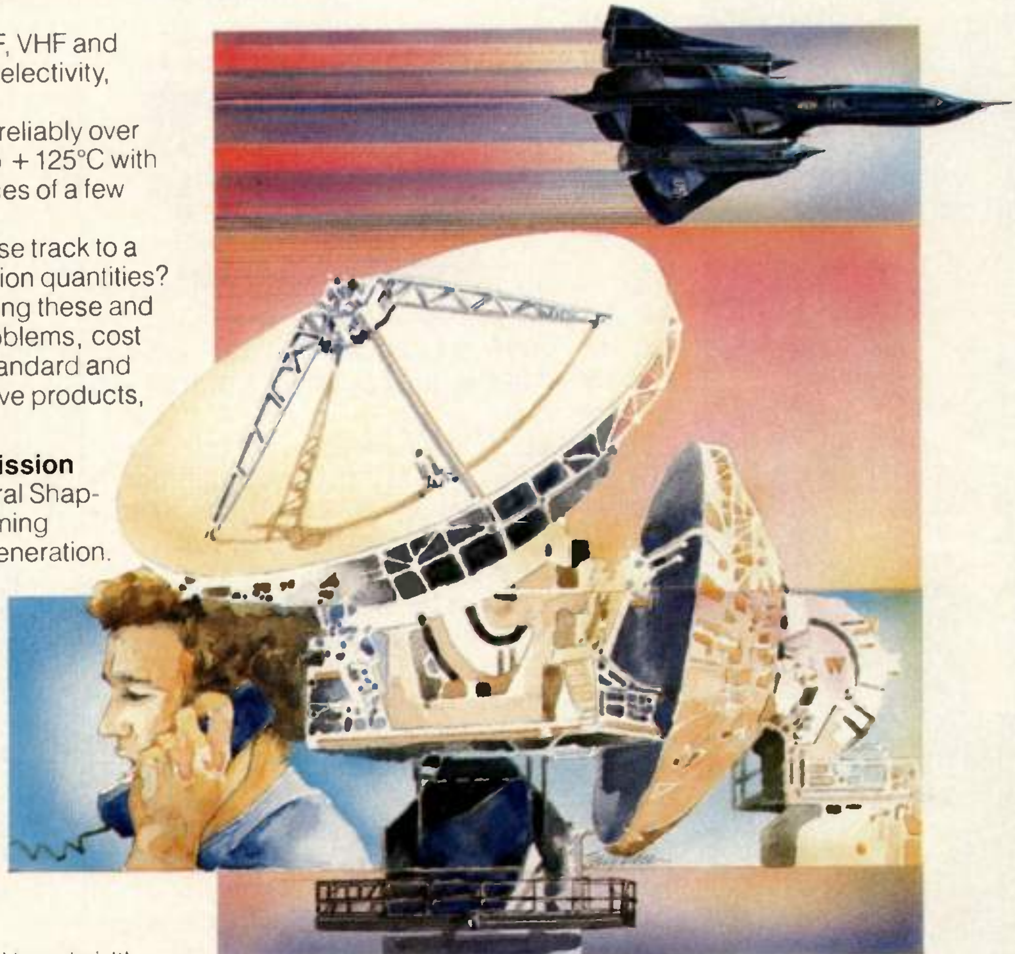

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A Simple Spectrum Analyzer

Pocket-Sized 0 to 100 MHz Unit Uses Only Three ICs

By Albert Helfrick
Doty RFL Industries

Here is one of our RF Design Awards contest entries, an extremly simple spectrum analyzer usable with a general-purpose oscilloscope. It is a valuable tool, allowing detection of RF energy at low levels. In addition to the circuit design and equipment troubleshooting applications noted by the author, this unit should be extremly useful in locating leakage from shielded enclosures, pinpointing sources of radiation in digital circuits, and tracking down sources of interference.

This simple spectrum analyzer is constructed using only three integrated circuits. The unit covers inputs from near zero to 100-plus MHz and has a log display range of more than 60 dB with a minimum detectable signal of −75 dBm. The sweep linearity and log display linearity is excellent.

The analyzer is most often used as a low level signal searching tool for troubleshooting and developing RF circuits. The analyzer is used with one or two turn coils attached to a length of coaxial cable to *sniff out* the presence of RF signals. As an example, the analyzer can be used to tune oscillators and amplifiers by placing the pick-up coil near the circuit to be tuned. The analyzer is invaluable for tuning transmitters since parasitic oscillations often occur when a transmitter is poorly tuned. It is also suitable for tuning low level circuits where levels high enough to be used with a crystal detector or an oscilloscope would saturate the circuit being tuned.

Circuit Description

The spectrum analyzer uses the conventional multiple conversion superheterodyne technique. The input frequency

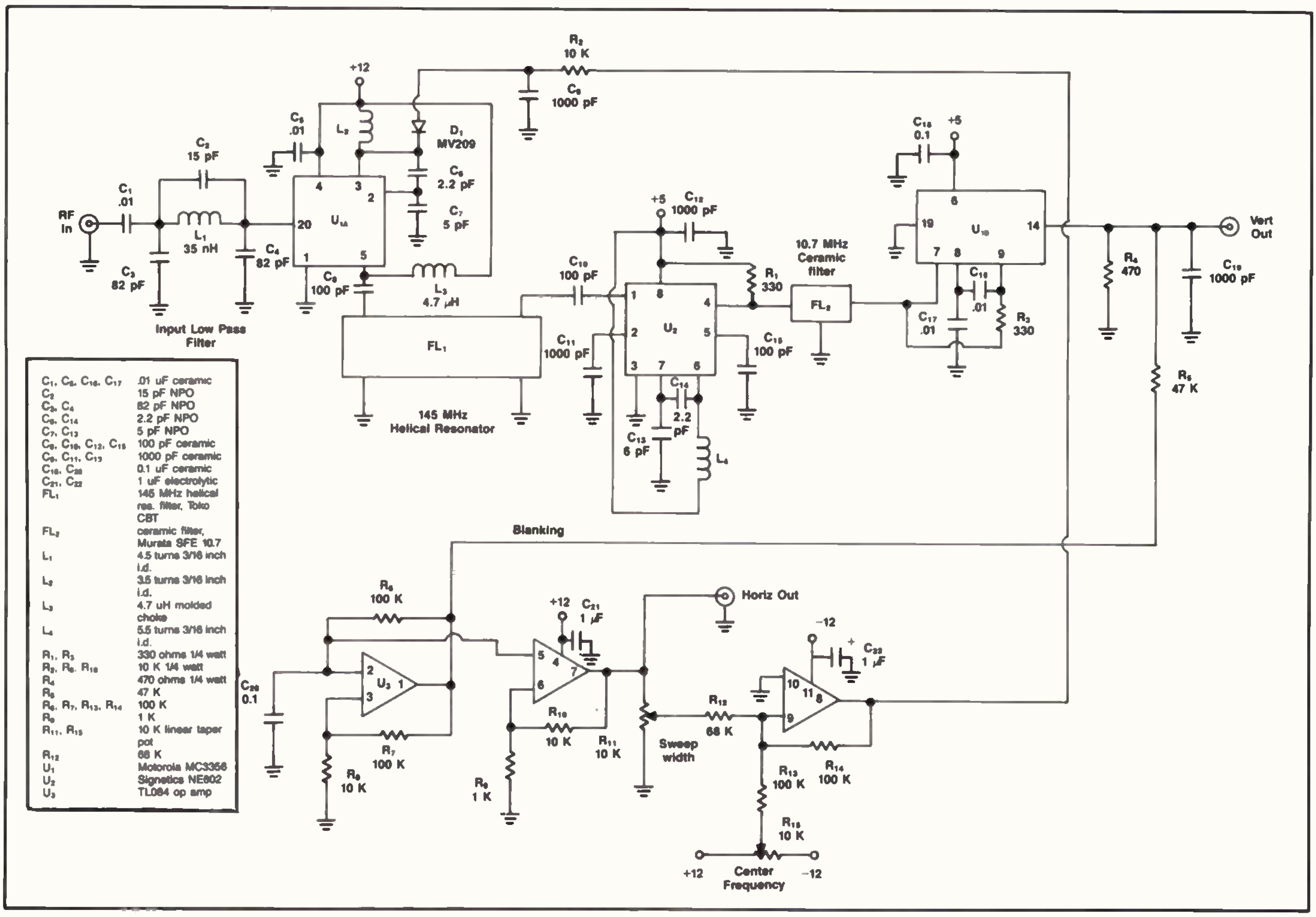

Figure 1. Circuit diagram of the spectrum analyzer.

range of zero to 100 MHz is converted to the first IF of 145 MHz using the converter section of a Motorola MC3356 FSK receiver chip. The local oscillator for the first conversion covers from 145 MHz to 245 MHz and uses the local oscillator of the FSK chip with varactor tuning. The Motorola chip is specified for 200 MHz operation but there is no difficulty operating the oscillator at more than 260 MHz. The frequency capability of the mixer output is not specified but it is used at 145 MHz.

The mixer output is tuned using a helical resonator. This device is normally used in front-ends of VHF FM receivers. The helical resonator is the most expensive device in the design, and the cost of the analyzer could be reduced significantly by substituting a home-made helical resonator made with bus wire and a good-quality trimmer capacitor. Commercial resonators are available in several bandwidths and have good image rejection at the second IF of 10.7 MHz. The resonator is matched, or more accurately mismatched, to the mixer output. The resulting loss of gain does not affect the analyzer since the full 60 dB of dynamic range available from the log amplifier is realizable. The ultimate sensitivity of the

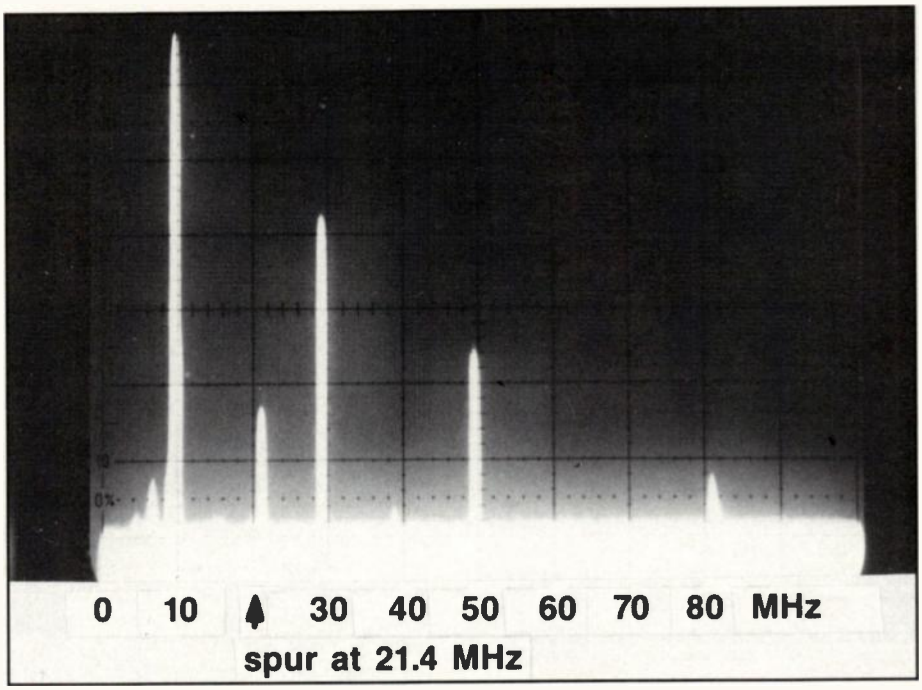

Figure 2. Photo of spectral representation of a distorted 10 MHz signal from a function generator providing a square wave. The 21.4 MHz spur can be eliminated with an improved helical filter.

analyzer is −75 dBm and extends up to −15 dBm. Because the mixer of the 3356 does not have a well defined input impedance such as a diode double balanced mixer, the broadband frequency response of the analyzer is not spectacular, but quite decent at plus or minus 3 or 4 dB over the full frequency range.

The first IF of 150 MHz is mixed down to the second IF of 10.7 MHz using a Signetics NE602 oscillator/mixer chip. The oscillator frequency of the NE602 operates at 155.7 MHz, which is 10.7 MHz above the first IF of 145 MHz. The oscillator frequency is tuned by deforming the coil. The output of the second mixer is filtered with a 10.7 MHz ceramic filter which offers a passband of about 250 kHz and is gaussian shaped for minimum scan loss. This filter sets the ultimate resolution of the analyzer and the FM broadcast bandwidth is in concert with the frequency scan rate and inherent phase noise of the oscillators.

The 10.7 MHz IF is where the majority of gain for the spectrum analyzer is obtained. This is normal for a design of this type. The MC3356 chip is configured as an FSK receiver but it has an output which is proportional to the log of the limiter input. This output is used as the log output of the spectrum analyzer. Note that the discriminator is not used.

Simplicity is the key to the analyzer design. A simple relaxation oscillator consisting of an op-amp is used as the basic time base generator. The linear ramp does not need to be shaped for frequency linearity if a hyperabrupt varactor diode is used such as the MV209 in this circuit. The resulting linearity is about 1 or 2 percent of the total frequency span.

The output ramp is buffered and used as the Y axis drive for the oscilloscope. The same buffered ramp is attenuated with the scan width potentiometer and fed to a summing amplifier which sums the center frequency potentiometer voltage. The output of this amplifier is used to drive the varactor diode. In order to gain the maximum voltage available for the diode, the diode is biased to +12 volts by directly connecting it to the oscillator coil which is a DC path to the +12 volt supply. The approximately ±10 volts peak output from the summing amplifier results in a −2 to −22 volts bias across the diode. The negative going voltage applied to varactor diode is the opposite polarity of the ramp applied to the X axis of the oscilloscope. This results in the proper relationship between the sweep voltage of the oscilloscope and the analyzer frequency.

The output of the ramp generator op-amp, which is a square wave, is used as a blanking voltage. Rather than using the Z axis of the oscilloscope for blanking, the oscilloscope trace is "pushed off the screen" during retrace by applying the square wave to the log output. This eliminates the need to supply three connections to the oscilloscope and to contend with the differing Z axis blanking requirements.

The cost of the analyzer is obviously a function of the individual parts and primarily the cost of the helical filter. It should not be difficult to replicate the analyzer (complete, power supply, case and all) for less than $50 if the helical resonator is home-made. It's probably the best $50 tool an RF designer could own. rf

About the Author

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rf featured technology

High Speed A/D and D/A Conversion

Basic Information About this Fast-Growing Technology

By Gary A. Breed
Editor

With more analog electronic circuits reaching RF operating speeds, two significant results have been created. First, new methods of implementing radio circuits are available to the RF engineer; and second, the traditional analog designer is faced with the need to use RF design methods in his or her work. This month, RF Design *features one major part of this high speed revolution: the interface between analog information and digital computational circuitry.*

How fast are today's A/D and D/A circuits operating? Depending on the number of bits of resolution, it could be 10 MHz or over 1 GHz. There are GaAs comparators, or 1-bit analog-to-digital converters (ADCs), operating at over 1 GHz, and monolithic silicon 8-bit ADCs are available with sampling rates above 150 MHz. Digital-to-analog converters (DACs) are easier to build than ADCs of the same resolution. GaAs technology has reached the point where an 8-bit DAC can be had with 1 GHz update rate. Silicon is faster, too, with 8-bit devices at 400 MHz, and 10-bit parts close to that.

Analog-to-Digital Conversion

In simplest terms, an ADC captures a time-varying function in the "real world" and converts it to binary information for manipulation and processing using digital techniques. Limitations on speed (and accuracy) can be both internal, in the architecture and fabrication of the ADC, and external, in the analog processing of the input signal or in the physical layout of the circuit. First, the internal considerations:

Slower ADCs use either the *successive approximation* or *integrating* method of conversion. The former compares the input to a series of accurately-know binary fractions of full-scale, dividing the signal into smaller and smaller increments until the requisite number of bits is represented. Integrating converters count pulses during a period proportional to the input. Since these types require multiple steps in the conversion process, they are relatively slow.

High speed ADCs use either *flash* or *serial* conversion, along with *pipelining* or *subranging* techniques to further improve speed and accuracy. Flash converters are obvious in concept: a stack of comparators equal to the binary value of the output word. For example, 256 comparators are needed for an 8-bit ADC. The sequential information of the comparators is converted to parallel binary form using internal logic. Because the operation is essentially a one-step process, it can be used at very high conversion rates. The main drawbacks are the requirement for a large number of very accurate comparators, and a complex array of gates in the decoding logic.

Serial ADCs are interesting in concept. The input is presented to a series of amplifiers which determine whether the signal is above or below one-half of full-scale, then applying a gain of −2 if above the reference, or +2 if below. The following stage then applies the same rule to what is now two quarter segments of full-scale, with 1/8, 1/16, etc., increments thereafter. A binary word representing the input is built from the high/low decision made at each stage. Although an *n*-bit conversion takes the time for propagation through *n* stages, the 1 or 0 decision of each stage can be latched and the next conversion begin before the preceding is finished. This process is called pipelining, and greatly increases the rate at which conversions come out of the pipeline, despite the significant delay from beginning to end of each one. The principal limitation of this process is the required accuracy of the amplifier stages, which restricts its practical use to only a few bits.

Subranging (Figure 1) is a process that can increase the accuracy (number of bits resolution) of a high speed ADC. Typically, the signal is first presented to an 8-bit flash ADC, which has its output reconstructed using an 8-bit DAC. This output is then subtracted from the input signal, resulting in an error that is, in theory, equal to the unresolved detail of the original signal. This error is then digitized in a 5- or 6-bit flash ADC and combined with the previously determined 8 most significant bits (MSB) to create an accurate 12-bit output. At the highest speeds currently achieved by high-resolution ADCs, this is the method of choice.

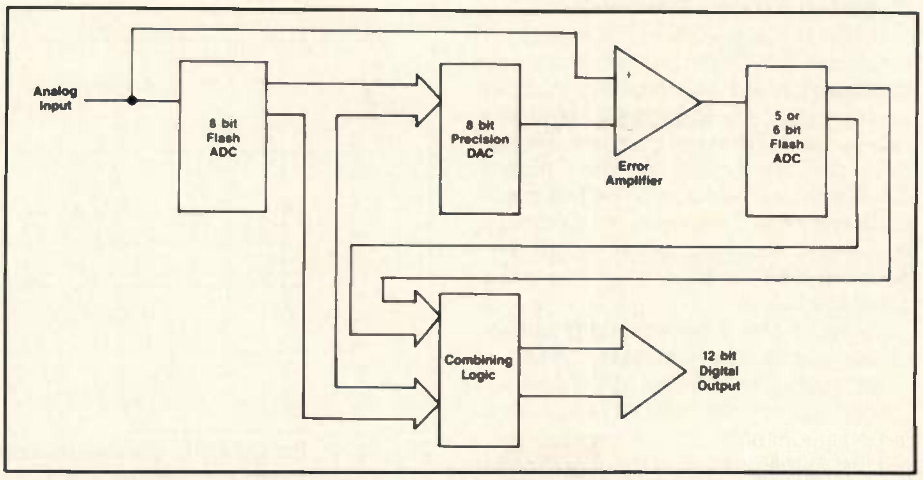

Figure 1. Basic subranging technique to improve resolution of high speed ADCs.

At this point, the basic function of ADCs has been introduced, but there is much more information that is necessary to select and use a particular device or assembly. Coding of the output needs to be selected to match the digital processing requirements. Binary, offset binary, BCD, or two's complement are possible choices. Overrange output may be a necessary function, as well. Of course, compatibility with the logic family in use is a necessity, but even this choice is not always clear. Some devices can be used with 5 volt TTL logic, and with power supply and decoupling changes, also accommodate −5.2 ECL levels. It should be noted that, with ADCs and DACs, the term "bipolar" does not mean the fabrication method. Instead, it means that the input or output includes both positive and negative voltages.

Performance specifications include the following: *Absolute accuracy* is the difference between the theoretical and actual input voltages required to produce a given digital output, usually specified at the midpoint of the input range. *Relative accuracy,* the deviation between the actual analog input and a given output code, relative to full scale, is specified in fractions of a LSB, per cent, or in ppm. *Linearity* is a measure of deviation from an ideal straight line input-to-output response. *Differential linearity* is a measure of linearity from step to step, in fractions of a LSB. *Quantizing uncertainty* is inherently ±1/2 LSB. Any additional quantizing errors should be specified for a device. *Gain, conversion speed, common-mode rejection,* and *temperature coefficient* are self-explanatory.

Digital-to-Analog Conversion

Unlike ADCs, there is but one structure for all common DACs: a network of precision resistors and switches (Figure 2). In addition, each particular device will have appropriate logic level inputs and internal drive circuitry for the switches, output amplifiers, and perhaps an on-board reference voltage. The output of this design is current, requiring either a low impedance load, or an op amp to provide a voltage output.

Many of the functional and performance specifications are either the same, or correspond to those for ADCs. One exception is the *multiplying DAC* which uses a varying reference input to create an output that is the product of the digital code and the reference. Analog output specifications are also specific to a DAC, such as output current ratings and *compliance voltage range,* over which the current rating is valid. Other unique specs are output *noise, capacitance, gain* and *offset.*

Finally, a particularly important performance area is *glitch energy.* Glitches are the switch transitions that occur whenever a change in input occurs, significant when several bits change state, such as at one-half of full scale, when all bits change. These transitions can be propagated to the analog output where they contribute to the total noise. Many DACs employ *deglitchers,* which are fast sample- and-hold circuits that delay updating the output level until the switches have settled.

ADC and DAC High Speed Circuits

Somewhere in the MHz range of frequencies, simple components begin to behave in a more complex fashion. The inductance of component leads becomes significant, stray capacitance becomes a part of all circuits, and every wire and circuit board trace is a transmission line. Although these phenomena are second nature to an experienced RF engineer, not every designer called upon to implement a high speed circuit is well-versed in RF techniques. On the other hand, the RF engineer is not accustomed to dealing with the fast rise times of digital circuitry, or the number of possible crosstalk sources that a multi-bit digital bus presents.

At all speeds, the separation of digital and analog portions of systems involving ADCs and DACs is a problem. The close proximity of input and output within a monolithic device guarantees this. At high speed/frequency operation, several factors compound the analog/digital crosstalk problem. First, capacitive reactance decreases with frequency, so stray capacitance couples greater energy between adjacent components. Also, the increasing inductive reactance of lead and traces increases the magnetic fields generated, and therefore the transformer-type coupling between circuit elements. The problem is further compounded by the sizeable harmonic energy contained in fast rise time digital signals.

Another significant problem is time delay. All bits of a digital bus and all clock timing signals have to propagate through a circuit that, at high speed, can be a significant portion of a waveform's period. This problem is common in all high speed digital work, but might be occasionally overlooked until the circuit doesn't work.

The digitization of high frequency analog signals in an ADC has some special difficulties. One is the "snapshot" time during which the signal is sampled. A fast-slewing waveform won't stay constant long enough to assure that an accurate level has been seen by the ADC. The solution is a fast sample-and-hold circuit which locks the input at fixed levels, grabbing another sample each cycle of the clock to provide a stable input to the ADC during its digitization computation. However, every addition to the complexity of a circuit will further reduce its speed capability.

Another high speed problem is true representation of the maximum bandwidth of the analog signal. Like a digital waveform, the input can be a complex signal containing harmonic energy, modulation sidebands, or multiple signals. Although it may have an easily identifiable fundamental frequency, the additional spectral content must be accommodated in the ADC if the signal is to be accurately represented in digital form. This is especially true in IF processing applications, where microwave or mm-wave wide bandwidth signals are to be digitally analyzed.

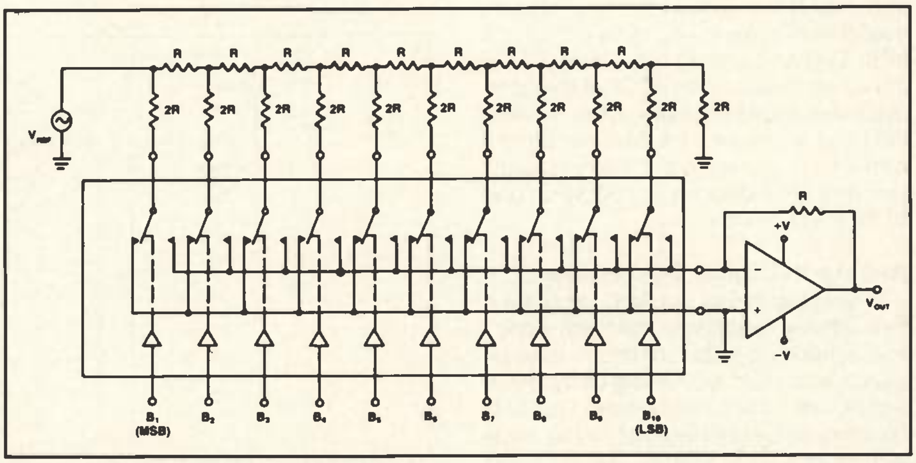

Figure 2. Basic DAC configuration.

Summary

High speed analog and digital circuitry requires *both* RF and digital engineering expertise. Whether these advanced techniques are used for RF, control or other applications, both aspects must be considered. *RF Design* encourages readers to submit examples of the problems they have encountered in these circuits, and the methods used to solve them. rf

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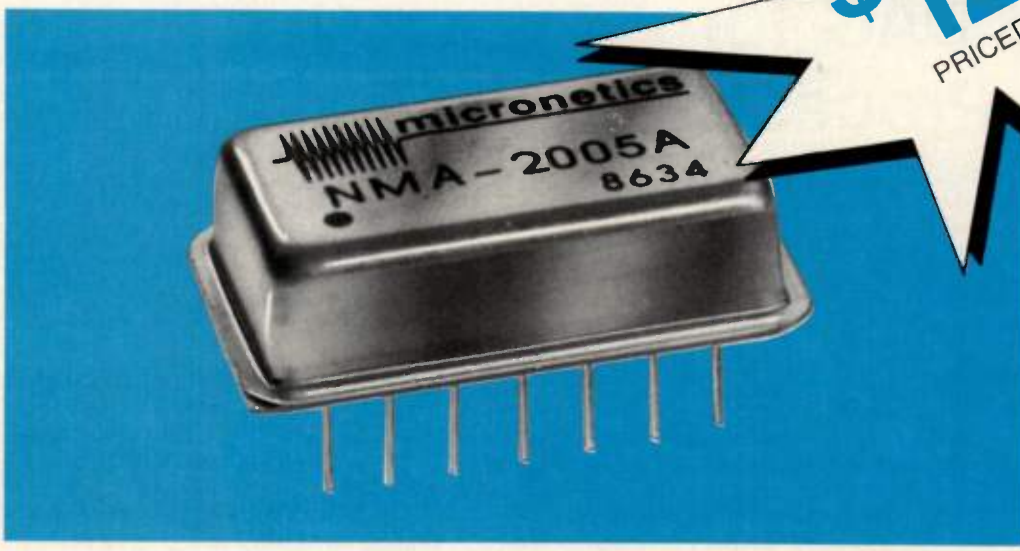

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NMA-2003	100Hz-1MHz	± .5 dB	10	10.0	−27	−87	87.0
NMA-2004	100Hz-3MHz	± .5 dB	10	5.8	−27	−92	82.2
NMA-2005	100Hz-10MHz	± .5 dB	10	3.2	−27	−97	77.0
NMA-2006	100Hz-30MHz	± .5 dB	5	.91	−33	−108	66.2
NMA-2007	500Hz-100MHz	± .75dB	2.5	.25	−39	−119	55.0
NMA-2008	500Hz-300MHz	±1.0 dB	4.4	.25	−34	−119	55.0
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INFO/CARD 31

Monolithic DAC for RF Signal Processing

By John Sylvan
Analog Devices, Inc.

The typical tradeoff in IC technology has always been speed for accuracy. In RF applications such as waveform generation, frequency synthesis and analog-to-digital conversion, monolithic digital-to-analog converters have offered megahertz bandwidths, but at limited accuracy and resolution. Since many RF signal processing applications now demand 12-bit or better performance, designers require D/A converters that promise both high speed and high resolution. Process technology improvements now make this possible.

The dominant high-speed D/A converter architecture uses a segmented ladder approach to produce a programmable analog output. Although segmented DACs typically have low glitch error and good differential nonlinearity, they suffer from poor integral nonlinearity. In addition, the decoding logic for the segmented DAC also adds an output delay, which many DACs do not include in their settling time specifications. A DAC employing an R-2R resistor ladder and scaled current sources, combined with on-chip laser trimming of resistors, can overcome these restrictions.

Bandwidth limitations of the DACs also result from their high impedance levels, producing parasitic circuit capacitances. The solutions to this problem is to either rely on multichip hybrid designs or dielectric isolation fabrication technology. Both approaches add circuit complexity, adding cost to the final design. A complementary bipolar (CB) process technology, which combines fast NPN and PNP transistors on a single IC substrate, can minimize circuit impedances, improving bandwidth. In addition, laser trimming of on-chip resistors can ensure 12-bit linearity.

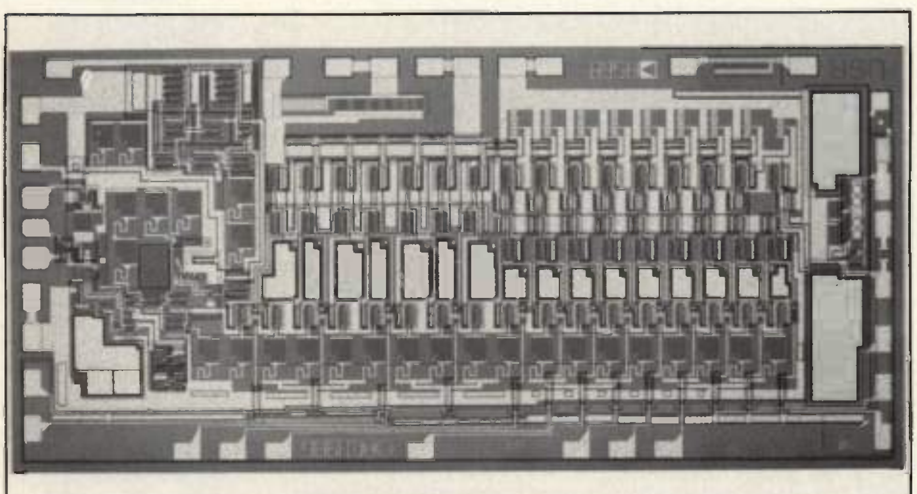
Circuit Design

Obtaining 12-bit performance at RF frequencies is a demanding task. High bandwidths make formerly negligible parasitic capacitances and inductances significant. Poor circuit design techniques can quickly degrade performance, rendering a high-resolution D/A converter worthless. Where tens of millamperes are involved, fractions of an ohm of misplaced impedance can generate errors several least significant bits (LSBs) in magnitude. Careful attention must be paid to all circuit factors. Proper RF techniques must be used in board design, device selection, supply bypassing and ground management.

Separate reference, output and digital power grounds permit careful management of ground currents for low noise and high-speed settling performance. The multiple ground returns minimize changes in current flow in the analog signal paths, and ensure logic return currents are not summed into the analog signals. Still, it is important for designers to understand what signal and supply currents are flowing in which grounds, and design their circuit accordingly.

If used properly, ground planes perform a myriad of functions on high-speed circuit boards: bypassing, shielding, and current transport. In mixed-signal designs, the digital and analog portions of the board should be distinct from one another. The analog ground plane should cover analog signal traces and the digital plane be confined to areas covering digital interconnection. The ground planes should be connected at or near the DAC. Also, designers must ensure that the ground plane is uninterrupted over crucial signal paths. Wide runs or planes on power lines will provide a low series impedance power supply to the DAC as well as offering capacitive decoupling of the appropriate ground plane.

Selection and placement of power supply bypass capacitors can be critical in a design. The dominant criteria is minimization of series resistance and inductance. Many capacitors will start to look inductive at 20 MHz and above. Ceramic and film-type capacitors generally feature lower series inductance than tantalum or electrolytic types. The capacitors should be installed with the



Die photo for the AD568 12-bit D/A converter.

shortest possible leads to minimize lead series inductance. (Chip capacitors are the optimal choice in this respect.) In addition, some series inductance between the DAC supply pins and the power supply plane (ferrite bead) may help to filter out high-frequency power supply noise.

Glitch Performance

In many high-speed DAC circuits, glitch performance is a critical parameter. Glitch arises from two factors: digital feedthrough and data skew.

When switching times exceed 10 MHz and precision surpasses 12-bits or more, interface issues are complex. No amount of design effort can perfectly isolate the analog portions of a DAC from the spectral components of digital input signals with 2 ns risetimes. Inevitably, high-frequency components of the digital signals will find their way into analog nodes, producing digital feedthrough glitch. To reduce feedthrough, the designer should omit on-board latches. This reduces the level of digital switching that occurs on the chip, and eliminates the need for a latch clock pulse. The trailing edge of this pulse typically produces a substantial glitch, even when the DAC is not changing codes. The on-board reference also eliminates the need for a reference input pin, which typically is a culprit for digital noise finding its way to the analog portions of a chip.

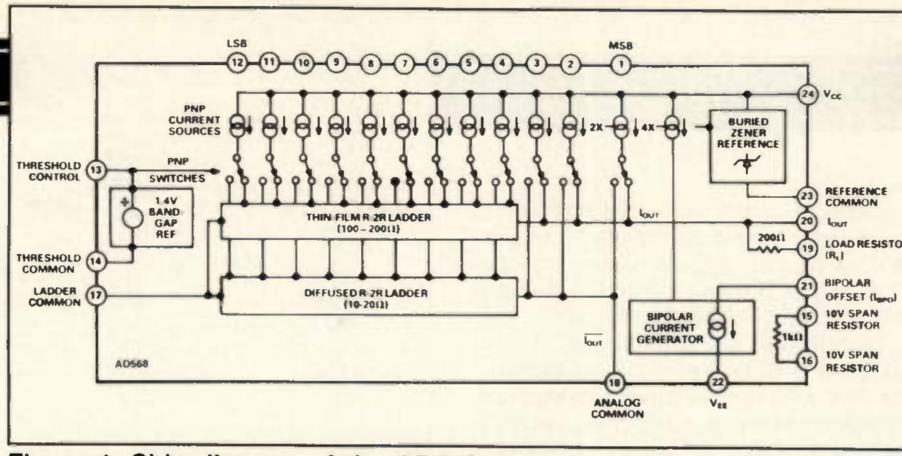


Figure 1. Chip diagram of the AD568.

Data skew arises if the input bits are not changed simultaneously, or if DAC bits switch at different speeds. The DAC may momentarily take on an erroneous value, and will be especially troublesome at major carry points. (A major carry point may be a change in a single LSB, but require the switching on or off of several most significant bit current sources.)

Successive Approximation ADCs

A key application for high-speed DACs is in successive approximation analog-to-digital converters. When combined with high-speed logic and comparators, designers can use Analog Devices' AD568 (Figure 1) to build a 1 MHz, 12-bit ADC.

The circuit in Figure 2 converts a negative input voltage to a current and brings it into a summing juunction with the DAC current. Two Schottky diodes, D1 and D2, clamp the summing junction to limit its voltage excursion from ground. A discrete preamp circuit differentially amplifies the signal and passes it to a high-speed comparator. The circuit latches the comparator output and feeds it back to the successive approximation register. The register is then clocked to generate the next set of codes for the DAC.

To complete a 1 μs conversion in 12 cycles, only 80 ns is available for each cycle. Since the Schottky diodes clamp the voltage of the summing junction, the DAC settling time approaches the current settling time of 35 ns, or half the budgeted time. Newer high-speed SAR chips, such as Zyrel's ZR504, can keep up with this pace quite easily by cutting the logic overhead in half from older classic 2504 SARs.

A simple clock that runs at a constant rate with a 90 percent duty cycle suffices for medium performance designs. If designers require even better performance, they can implement a variable clock frequency. Since the DAC settles to smaller and smaller increments as the conversion progresses, the clock frequency can be increased. (It takes less time for a DAC to settle to ±1 LSB as the test bit size decreases.)

When using the AD568 with a comparator, the comparator must respond to an overdrive of 250 μV (1 LSB) in less than 25 ns. The LT1016 comparator has the necessary quick response, but requires at least 5 mV of overdrive to maintain this speed. The discrete preamplifier in the circuit amplifies the summing-junction voltage to sufficiently overdrive the comparator. Designers should exercise care in laying out the preamp/comparator block to avoid introducing comparator instability with the preamplifier's additional gain.

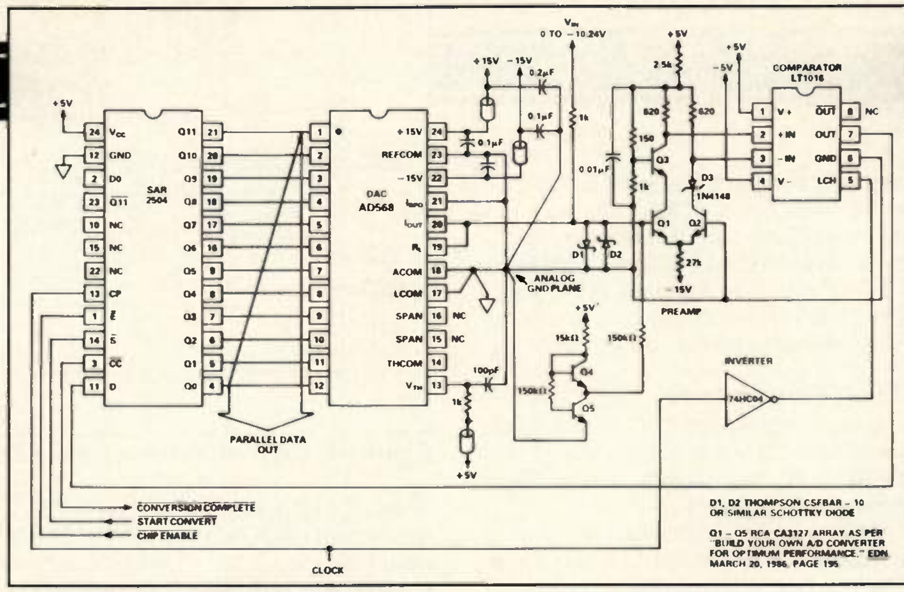


Figure 2. A 1 MHz, 12-bit ADC.

About the Author

John Sylvan is Technical Marketing Specialist at Analog Devices, Two Technology Way, Norwood, MA 02062. He can be reached by telephone at (617) 329-4700.

The RF Technology Expo 88 Technical Program

A Wide Variety of Topics Offers Something For Everyone.

Under the direction of Program Chairman Dr. Ulrich Rohde, the technical program for RF Technology Expo 88 represents a marvelously diverse collection of interesting and timely RF topics. Engineers should make their way to Anaheim next month to take part in this exchange of practical engineering ideas. With tutorials on power amplifiers, oscillators, propagation, and components, plus all the rest of the RF spectrum, every engineer will find information on his or her most important topic.

Fundamentals of RF Circuit Design
Les Besser, Besser Associates

A One-Day Short Course:
Tuesday, February 9, or
Wednesday, February 10

Once again, this popular course in RF design fundamentals is being offered to RF Technology Expo attendees. This course covers component behavior at radio frequencies, reviews the Smith chart, and presents basics of amplifier design using manual and CAD techniques.

An additional fee of $130 is charged for this course, and advance registration is required.

Wednesday — 8:30 to 11:30 a.m.

Session A-1 — RF Power Amplifier Tutorial
Chair: Sam Klein
Microwave Modules and Devices

Causes and Cures to RF Power Amplifier Instability
Peter Kwitkowski, Motorola

Designers often ignore the effects of misterminating an RF power transistor at frequencies outside the band of interest. Included are problems and solutions.

Practical Narrowband MOSFET VHF Power Amplifiers for Communications
Dan Peters, Falcon Communications

This paper will discuss three different power amplifiers. 50 W, 100 W and 250 W units will be highlighted.

Concept and Design of an 800 Watt UHF Power Amplifier
Harald Wickenhaeuser, Rohde and Schwarz

The amplifier mentioned above has a frequency range of 225 to 400 MHz. With 800 W PEP and 300 FM power, this unit has stringent specs to suit its multipurpose use.

Session B-1 — Frequency Synthesis I
Chair: Dr. Ulrich L. Rohde
Compact Software, Inc.

Designing Frequency Synthesizers
Cornell Drentea, Honeywell

The various synthesizer forms are discussed in this paper. Implementations mentioned include "direct brute force" with digital division of reference frequency, mixing of derivatives of the same reference frequency, mixing of two or more reference frequencies or combinations of the above.

GaAs Phase/ Frequency Comparator Use
Dan Gavin, Avantek

RFI from Synthesizers
Douglas J. Hughes, IIT Research Institute

A synthesizer primer is the topic of this paper.

Session C-1 — Data Transmission
Chair: James Eagleson
Alan Bradley RF ID Products

Microwave Radio LANs Utilizing the Multi-point Distribution Radio Service (MDS)
Bruce Ziemienski, City of Fresno

An economical solution to data communications distribution is proposed through the 950 MHz band. FCC rules are discussed as well as the use of multiple addressing — a scheme that incorporates a central location that uses an omnidirectional antenna to reach multiple remote locations. Useful definitions are included.

A Frequency Agile BPSK Demodulator
Richard Roberts, Harris Corp.

This frequency synthesizer is embedded inside a Costa loop.

High PRF GHz RF Pulse Modulator with High On/Off Ratio
Seymour Rubin, SR Associates

This modulator is used in an acousto-optic driver. It has a 1 ns pulse rise time and 25 dB extinction ratio.

Wednesday — 1:30 to 4:30 p.m.

Session D-2 — Filter Design
Chair: Tom Sporkmann
Compact Software, Inc.

Chebyshev and Butterworth Filter Gain and Delay Considerations
Robert Kane, Motorola

This paper is a discussion on delay distortion and equalization networks.

Filter Design Techniques Using Personal Computers
Michael Ferrand, Microlab/FXR

An overview of filter design techniques using personal computers is presented.

High Power Notch Filters
Greg Kinnetz, Microwave Filter Co.

The design, component fabrication techniques and measured results of high power notch filters for transmitter applications is covered.

Session E-2 — Frequency Synthesis II
Chair: Earl W. McCune
Digital RF Solutions Corp.

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February 10, 1988 — Wednesday A.M. (choose one session)
A-1 ☐ B-1 ☐ C-1 ☐

February 10, 1988 — Wednesday P.M. (choose one session)
D-2 ☐ E-2 ☐ F-2 ☐

February 11, 1988 — Thursday A.M. (choose one session)
G-3 ☐ H-3 ☐ I-3 ☐

February 11, 1988 — Thursday P.M. (choose one session)
J-4 ☐ K-4 ☐ L-4 ☐

February 12, 1988 — Friday A.M. (choose one session)
M-5 ☐ N-5 ☐ O-5 ☐ P-5 ☐

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Operation of a Synthesizer Settling Time Test Fixture
Larry Tichauer, Hughes Aircraft
The paper starts with why a frequency synthesizer's settling time value and consistency is important and must be measured. The application discussed is a frequency agile, fast hopped modulated communication system. A block diagram of the test system is shown and explained.

Digital RF Synthesis: Theory and Application of a Booming Technology
Greg Lowitz, Hewlett-Packard
Combination of ECL logic and GaAs DAC technology leads to off-the-shelf digital RF synthesizers suited for applications from radar/EW to communications and magnetic recording. A overview of digital synthesis theory and applications is provided.

An ATE Software System for RF Module Testing
J. C. Lunsford, Hughes Aircraft
The primary intent of the system design discussed is to reduce time overhead associated with RF performance testing of spread spectrum communications system.

Session F-2 — Testing, Instrumentation and Measurements Chair: Malcolm Levy Racal-Dana Instruments, Inc.

High Frequency Text Fixturing for Microwave Hybrid Circuits and Leadless Devices
John Logan, Inter-Logic Systems
Two issues on high frequency test fixturing are addressed: 1. The importance of testing at the earliest possible point in device fabrication and; 2. The increasing use of hybrid circuit technology and leadless devices in microwave module fabrication.

Noise Parameter Measurements
W. C. Mueller, Avantek
F_{min}, both the absolute value and angle of gamma optimum and R_n are the noise parameters determined using the proposed technique. Standard production test equipment is used.

Synchronous Detector and Phase Noise Measurement System
Jon GrosJean, Woodstock Engineering
The design uses a Motorola C-QUAM AM stereo decoder integrated circuit to measure the noise of receiver's local oscillators, other received signals or evaluate signal generators and oscillators for noise.

Thursday — 8:30 to 11:30 a.m.

Session G-3 — Oscillator Tutorial Chair: Carl Erickson McCoy Electronics

Practical Considerations in Specifying Hi-Stability Crystal Oscillators
Glenn Kurzenknabe, Piezo Crystal Co.
This paper is a tradeoff study between design and cost. Frequency stability, aging, SSB phase noise, Allen variance, and environmental conditions are some of the performance criteria discussed.

K Band Dielectric Resonator Oscillator
Ching Ho, Collins Div., Rockwell International
The paper features feedback type DRO's designed with Super Compact. An HP 8510 was used to measure the dielectric resonator characteristics in a fixture that consisted of 50 ohm microstrip line and quartz spacer above an AT/Duroid substrate.

Statistical Analysis of Phase Noise, Allan Variance, G Sensitivity and Aging Data of Crystals
Robert Ziegler, Piezo Crystal Co.
This paper shows the importance of statistics in analyzing data as it relates to manufacturing and specifying oscillators. The author does this by presenting a compilation of measurements involving hundreds of precision quartz crystal oscillators.

Session H-3 — Phase-Locked Loops

Improved Accuracy for PLL Transient Analysis
David Badger, Wavetek RF Products
The limitations of existing PLL transient analysis is studied. Also, a new phase detector model was developed and used to simulate frequency step response for two different PLL designs.

Use of Pole-Zero Cancellation to Improve PLL Noise Performance
David Badger, Wavetek RF Products
A discussion of how a lowpass (pole) followed by a highpass (zero) circuit introduced between phase detector and VCO can reduce coarse steering, fractional division jitter correction and consequently the noise without affecting the overall transfer function is presented.

A Phase Lock Loop That Works — Almost: Part 3
Mike Black, Texas Instruments
The pitfalls of PLL design that should be avoided are featured in this paper. Block diagrams, supporting math and response curves are shown.

Session I-3 — CAD/CAE Techniques Chair: Les Besser Besser Associates

Microwave Harmonica
Rowan Gilmore, Compact Software, Inc.
This paper discusses a mainframe software routine that's based on the harmonic balance simulation technique which accurately analyzes and optimizes HF through microwave non-linear techniques.

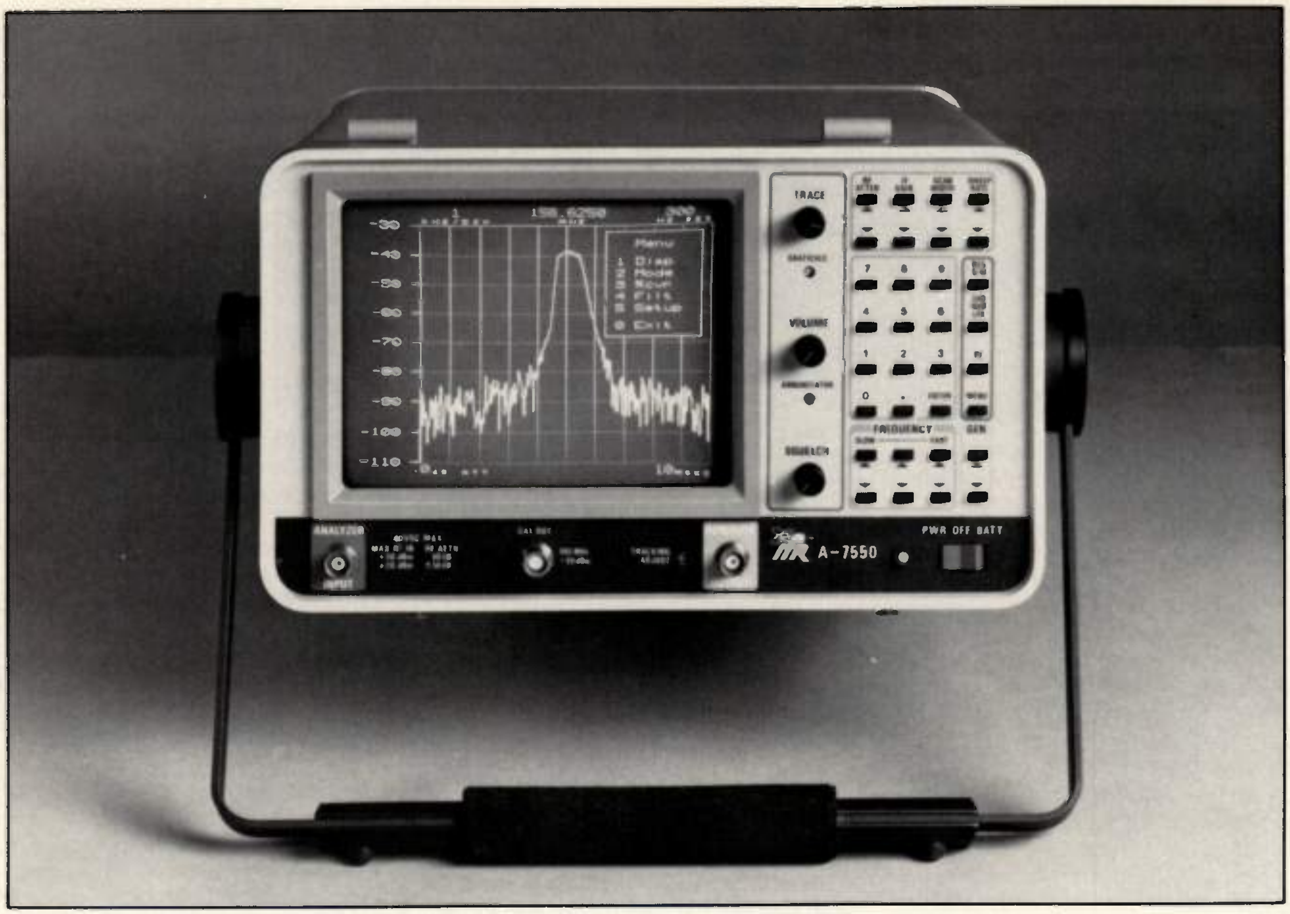
Supercomputer Aided Designs for Viable Near-Future RF Systems
Dr. P.S. Neelakanta, Univ. of South Alabama
Specific areas where SuperCAD is needed in RF system development include large structured conventional transmission lines, antennas and passive/active elements eg. MIMIC, monolithic phased arrays, high speed interconnection networks in high density IC packages, multi-layered microstrip structures, electromagnetically active exotic surfaces and on-chip microwave metrology. Extended analytical techniques such as FFT, spectral domain approach, method of moments, double variation techniques and finite element/finite difference time domain solutions will profit from Super CAD.

A GaAs Pulse Modulator Design for RF Signal Generators
Ted Dudziak, Wavetek RF Products
This modulator was designed for use in the Model 2520 RF signal generator. CAD modelling is discussed together with the effects of the pulse modulator performance due to hybrid implementation.

Thursday — 1:30 to 4:30 p.m.

Session J-4 — Radiowave Propagation Tutorial

Radio Wave Propagation Tutorial
Daniel R. Dorsey, Control Data Corp.
This session consists of a discussion of basic principles and characterizations (Maxwell equations, ionospheric composition, solar effects). This is followed by a discussion of HF propagation as well as various propagation prediction methods. The final section of this session covers



Runnerup Prize: The A-7550 Spectrum Analyzer from IFR, Inc. features 100 kHz to 1 GHz frequency coverage and microprocessor control that automatically selects and optimizes bandwidth, sweep rate, and slew rate of control functions. Single function keyboard entry and a menu driven display make operation easy and straightforward.

The runner-up prize is only slightly less grand than . . .

JUDGING CRITERIA

1. **Originality:** The purpose of the contest is to reward engineers for their unique design contributions. Each design will be evaluated according to its similarity to work by others, unusual application of a device or technique, and other judgments of its contribution to the advancement of the engineering craft.

2. **Engineering:** Engineering is the application of technology to solve a problem or meet a design goal. Entrants should clearly identify how their circuit was created in response to such a need. Judges will evaluate performance, practicality, reproducibility and economy.

3. **Documentation:** Communicating ideas to others is the business of *RF Design* and a necessary part of good engineering. Each entry will be judged on its description, analysis and graphical material. Each circuit should have a complete list of components, explanation of functions, and a summary of performance and test data.

ENTRY RULES

1. Entries shall be RF circuits containing no more than 6 single active devices (tubes or transistors), or 4 integrated circuits, or be passive circuits of comparable complexity.

2. The circuit must have an obvious RF function (as defined on page 6 of November 1987, *RF Design*) and operate in the below-3 GHz frequency range.

3. Circuits must be the original work of the entrant.

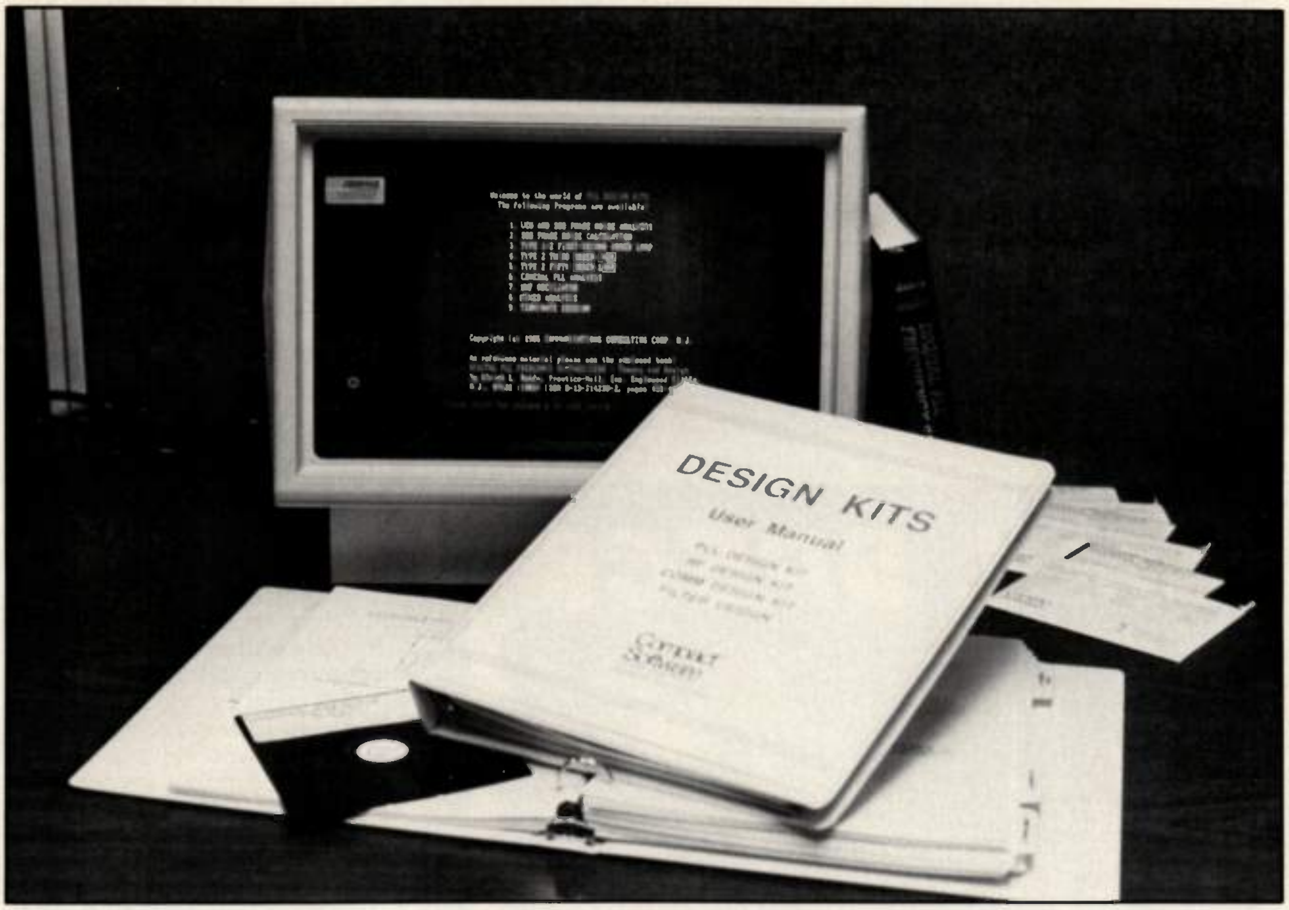
4. If developed as part of the entrant's employment, entries must have the employer's approval for submission.

5. Components used must be generally available, not obsolete or proprietary.

6. Submission of an entry implies permission for *RF Design* to publish the material. All prize winning designs will be published, plus additional entries of merit.

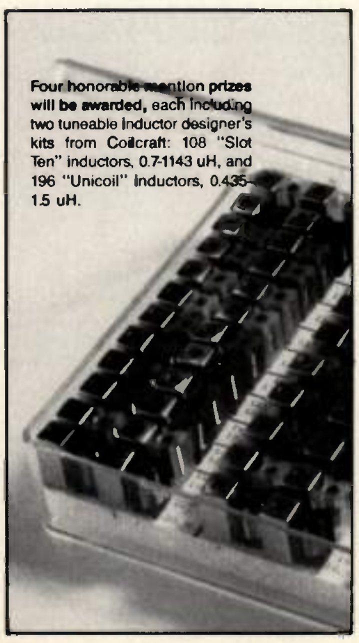
7. Winners shall assume responsibility for any taxes, duties or other assessments which result from the receipt of their prizes.

8. Deadline for entries: **March 31, 1988.**



Grand Prize: Compact Software's Design Kit Series, including the RF Design Kit® for system optimization, plus transformer and oscillator design; the Communications Design Kit® with digital system simulation, antenna evaluation, AGC synthesis and mixer analysis; the PLL Design Kit® for VCO design, plus stability, switching and non-linear analysis; and the Filter Design Kit® for LC, crystal, helical and interdigital filter design.

the grand prize in the 1988 RF Design Awards Contest!



Four honorable mention prizes will be awarded, each including two tuneable inductor designer's kits from Coilcraft: 108 "Slot Ten" inductors, 0.7-1143 uH, and 196 "Unicoil" inductors, 0.435-1.5 uH.

. . . and then there are four "honorable mention" prizes which are also quite grand.

Your chances of winning one of these six awards are better than one in twenty. . . and the grand prize winner will be the subject of our July 1988 cover as well. Those are the kind of odds that make it worth your while to pit your skills and ingenuity against the field. Now's the time to expose that ingenious circuit idea you've always wanted to show off to your engineering peers. Let the world know you're as good as you are!

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from VHF through millimeter wave differences from HF, effects of the atmosphere, special modes and a discussion on satellite communications.

Session K-4 — RF Techniques
Chair: Richard Davis,
Harris Microwave Semiconductor

Accuracy Considerations in RF Measurements
Lorenzo Freschet, Hewlett-Packard
A typical example in this paper considers a reflectometer setup. Discussion of potential measurement errors is included.

Single-Chip 2 GBit/s Clock Recovery Subsystem for Digital Communications
R.M. Hickling, GigaBit Logic
A GaAs IC is used in PLL for microwave and fiber optic digital communication. The IC is characterized with respect to data eye sensitivity, acquisition stability and output jitter and contains both analog and digital components.

Hidden Electronics Detection
Michael Ferrand, Microlab/FXR
A discussion of the history of electronic eavesdropping, "bugs" used, and methods as well as circuits for detection serve as the gist of this paper.

Session L-4 —
Specialized Components
Chair: Joe White
J F White Consulting

A Glass Packaged Varactor as a Hi-Reliability Device
John Howe, Motorola
This paper discusses the physical properties and manufacturing methods used to obtain high performance. A case study using MIL-S-19500 screening requirements to MIL-STD-750 test methods of an actual device lot is presented.

PIN FET Primer
Jack Koscinski, General Optronics
These devices are used as optical receivers for fiber optic links. PIN FETs come in 14-pin DIP packages with the optical connection consisting of a fiber optic pigtail. The primer discusses noise performance, gain, dynamic range, bandwidth and test techniques.

The Convoluted Loop Antenna
Robert Hart, Harris Corp.
The culmination of miniature transmitting and receiving loop research is the topic of this paper. The method discussed uses some interesting techniques to deal with the problem of high currents that exist in an extremely low radiation resistance antenna.

Friday — 8:30 to 11:30 a.m.

Session M-5 —
RF Component Tutorial
Chair: Gene Niemec
Merrimac Industries, Inc.

High Sensitivity Applications of Low Power Integrated Circuits
Donald Anderson, Signetics
Four separate IF strips that utilize a low power VHF mixer and low power IF strip developed around the Signetics NE602 and NE604A are the topic of this paper. The resulting IF strips are reproducible and provide sensitivities less than 2 uV.

Phase Shift Minimized Microstrip PIN Diode Attenuators
Dr. Koryu Ishii, Marquette Univ.
A discussion of available techniques to minimize spurious phase shift in waveguide attenuators down to 0.1 degree per dB at 9 GHz is featured.

Proper Application of Power Dividers — Understanding Power Relationships
Robert S. Larkin, Janel Labs
There are design subtleties that must be considered if divider full performance is to be achieved. Resistive, quadrature isolated, in-phase isolated and in-phase non-isolated dividers are discussed. Using dividers as combiners will also be mentioned.

Session N-5 — Analog Design Principles

System Approach to Automatic Gain Control
John Mohr, Magnavox
The application of linear servo theory to the design of AGC loops is expanded to include the effects of fixed gain within an AGC loop and the effects of group delay in components within the loop. This theory is then applied to an audio compressor, receiver and transmitter ALC circuits.

Design and Test Standardization for Cost Effective Hybrid Integrated Assemblies
Stephan Van Fleteren, FEI Microwave, Inc.
This paper is about an E/J band dual channel microwave integrated receiver that was developed using a modular fixturing test system which simplified and shortened the breadboarding process.

Session O-5 — Power Amplifiers II
Chair: Tawna Wilsey
Varian Associates, Inc.

High Performance Narrow Pulse UHF Power Transmitter
Steven Harrison, System Planning Corp.
Detailed circuit approach to achieve stringent requirements is the feature of this paper. Fundamental and logical modular approach is used.

Envelope Elimination and Restoration System Concepts
Frederick Raab, Green Mountain Radio Research
This technique is used for combining high efficiency non- linear RF amps with high efficiency audio amps to produce a high efficiency linear amplifier system. The effects of non-linearity and AM to PM conversion can be corrected through envelope feedback, polar feedback and cartesian feedback. The paper describes the EER system and provides a description and simplified analysis of the three feedback techniques.

Thermal Considerations In Amplifier Design
Gregg A. Hollingsworth, Acrian, Inc.
Thermal design considerations of die, package, baseplate and system heat exchanger elements of RF power amplifiers are explored.

Session P-5 — RFI/EMC Techniques
Chair: Bruce Gabrielson
Sachs/Freeman Associates

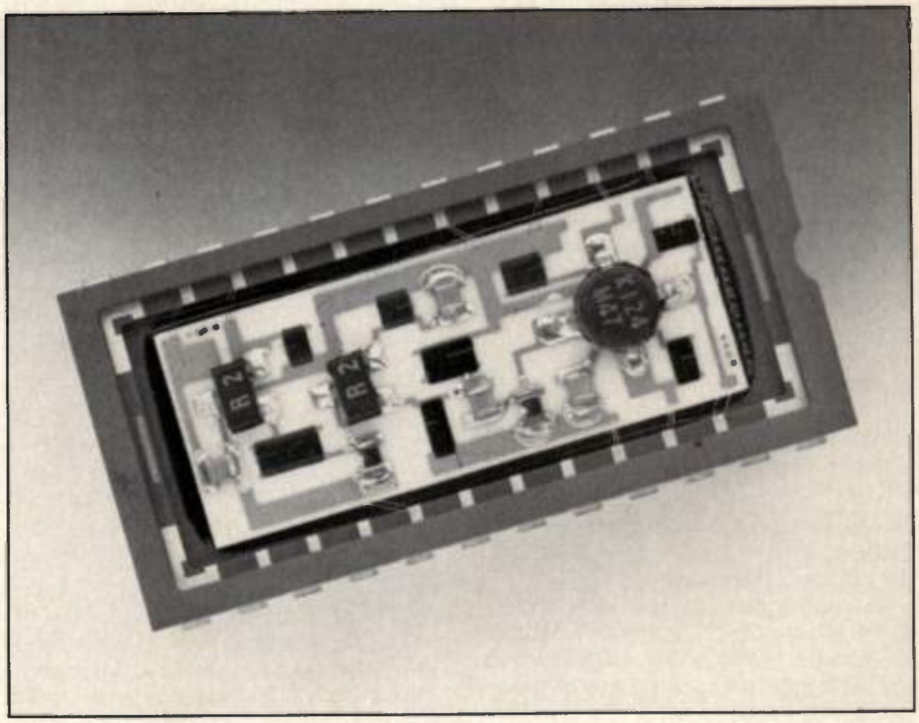
Electronic Equipment Grounding Design
John D.M. Osborne, Interference Control Technologies
This paper addresses the topic of "proper" grounding for electronic equipment. Beginning with a description of the basic aspects of grounding, including a definition of the term, the discussion moves forward through the fundamentals of bonding, earthing, and referencing.

Testing Methods for RF Shielding Effectiveness
Antonio Cardenas, Advanced Measurement Systems, Inc.
The paper deals with MIL-STD-285, NSA65-6 and NSA73-2A. The testing methods described in those documents are highlighted.

Microprocessor Interference to VHF Radios
Daryl Gerke, Kimmel, Gerke & Assoc.
The author highlights two case histories of microprocessor interference to VHF radios and discusses the problems and possible solutions.

Next Generation Low Noise EMC Design
Bruce Gabrielson, Sachs/Freeman Associates
This paper reviews current information and examines new and emerging technologies which may help engineers keep up with the increasing noise related issues.

1 GHz RF Amplifier From National Semiconductor



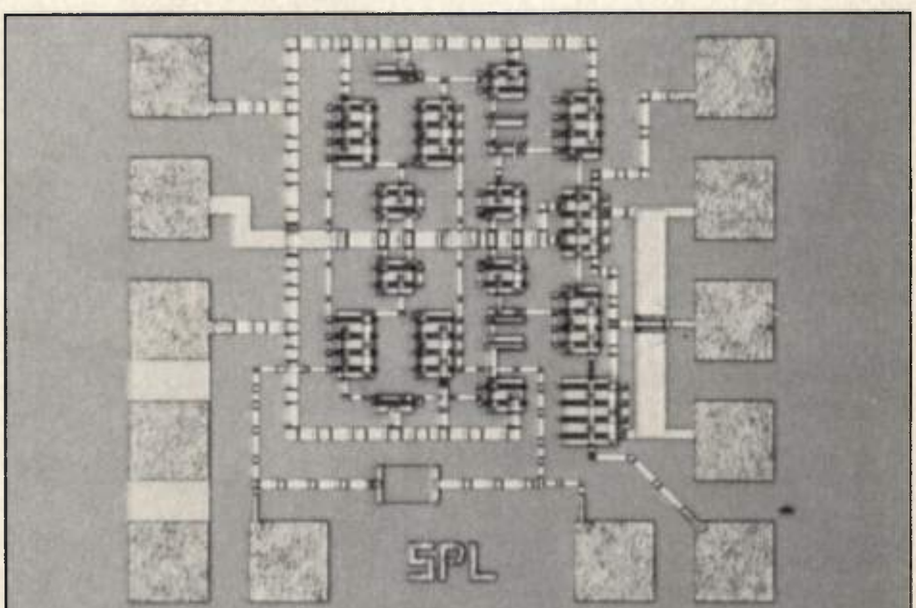
The LH4200 is a general purpose low noise, AC coupled, high frequency amplifier for applications in the 500 kHz to 1 GHz range. It features a gallium arsenide input stage for high frequency performance and bipolar second and third stages for low output impedance. It is useful for a variety of applications including feedback, AGC amplifiers, and signal sources. The amplifier is internally bypassed for good high frequency performance, but should be bypassed externally with a large capacitor to prevent low frequency stability problems.

The amplifier has three inputs: two high impedance gates for signal input, and a low impedance source for series mode feedback. Normally input 1 is used as the signal input while input 2 is used to control the gain of the amplifier for these applications using automatic gain control (AGC). Gain control ranges of over 60 dB are possible to 100 MHz. Input 2 is biased to +1.5 V for maximum gain and −2 V for minimum gain. Input 2 and feedback (Pin 3) can be bypassed with 0.02 uF capacitors for maximum gain.

The second gate, input 2, may be used as a second isolated input for small signal operation. The open loop gain from this input is approximately 6 dB less than from input 1. When the FET is used as a feedback amplifier, the third input is connected to the output with a suitable resistor to set the overall power gain. In this manner, voltage series feedback is used to establish the power gain and increase the input impedance.

The LH4200 has a noise figure of 3 dB in a 50 ohm system, third order intercept point of +25 dBm, and a gain reduction of 60 dBm at 100 MHz. The power at the 1 dB compression point is 14 dBm and nominal quiescent power is 450 mW. In 100 piece quantities, the LH4200CD (commercial) is $54 and the LH4200D (military) is $66. **National Semiconductor Corp., Santa Clara, CA. Please circle INFO/CARD #220.**

Anadigics Introduces a 3 GHz Laser Driver



The ALD30010 is a 10 kHz to 3 GHz laser diode current modulator from Anadigics. It requires a 0.6 $V_{p\text{-}p}$ single-ended input signal and provides 35 mA of adjustable modulation current to the laser diode. It can operate to 4.5 GHz as an analog current driver and up to 5 Gb/s in digital fiber optic systems. Also, it can be used as a wideband buffer amplifier through the use of its voltage-controlled gain and offset feature.

The VSWR for this device is measured to be less than 2:1 and its voltage controlled modulation range is from 0 to 30 mA. The third order intercept point occurs at 8 dBm while large signal rise and fall time ranges from a typical 80 ps to a maximum of 100 ps. The laser driver's input return loss is typically 20 dB. However, this can drop to a minimum of 15 dB. The compression level is 1 dBm and the peak offset current is 70 mA (min). **Anadigics, Inc., Warren, NJ. INFO/CARD #219.**

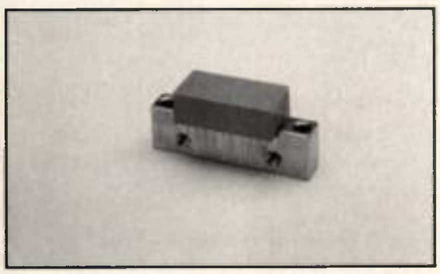
Electrically Adjustable Capacitor

Seiko Instruments introduces the Model S-8511A precision electrically adjustable capacitor (PEAC). The capacity of the PEAC can be adjusted by applying voltage pulses to the I/E terminal. Once set,

the capacitance value of this MOS device is maintained and adjustments can be performed at any time. The capacitance value ranges from 9 pF to 30 pF (max). **Seiko Instrument USA, Torrance, CA. INFO/CARD #218.**

CATV Power Doubler Hybrids

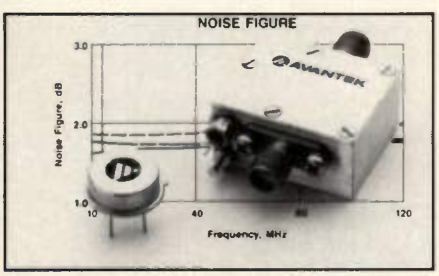
The BGD502 and BGD504 are Philips/Amperex power doubler hybrids with operating bandwidths of 40-550 MHz and power gains at 550 MHz of 19.8 and 21.2 dB respectively. Composite triple beat



with 77 channel loading is typically 67 dB for the BGD502 and 66 dB for the BGD504. Typical noise figure at 550 MHz is 6.5 dB. These hybrids feature thin film chip and wire technology with all gold metallization. **Amperex Electronic Corp., Slatersville, RI. INFO/CARD #217.**

Low Noise/High Gain Amplifiers

Avantek introduces four thin film cascadable amplifiers covering the 10-100 MHz and 20-150 MHz frequency



ranges with minimum gains of 26.5 and 23.5 dB, maximum noise figures of 2.2 and 3.2 dB and minimum 1 dB compressed output powers of 14.5 and 18 dBm respectively. These amplifiers, designated UTO-101, UTC-101, UTO-102, and UTC-102 are intended for applications requiring low noise figure, high gain and wide dynamic range, such as receiver IF stages. **Avantek, Inc., Santa Clara, CA. INFO/CARD #216.**

Multiple Crystal Oscillators

Series CA contains up to 16 independently BCD selectable crystal oscillators at frequencies to 200 MHz. Spurious outputs are better than 100 dBc and typical phase noise for the 100 MHz range output frequency is −115 dBc/Hz at 100 Hz, −136 dBc/Hz at 1 kHz and −152 dBc/Hz at 10 kHz. Options include improved phase noise, and field changeable crystals. **Communication Techniques, Inc., Whippany, NJ. INFO/CARD #215.**

Frequency Synthesizer

The VDS-1700 frequency synthesizer from Sciteq combines direct digital synthesis with phase lock loop circuitry. The instrument has a frequency range of 1200 to 1600 MHz with phase noise less than −80 dBc/Hz at 100 Hz. The switching speed is under 5 msecs. Options such as single or multi-channel chassis, IEEE-488, and internal 10 MHz TCXO are available. The standard VDS-1700 is priced under $2500. **Sciteq Electronics, Inc., San Diego, CA. INFO/CARD #214.**

Amplified Noise Source

The NC1110A amplified noise source has a frequency range of 100 kHz to 1500 MHz with +13 dBm ± 2.5 dB of white Gaussian noise output into a 50 ohm load.

The minimum crest factor is 5:1. The instrument measures 6"× 2"× 1.1" and costs $990. **Noise Com, Inc., Hackensack, NJ. INFO/CARD #213.**

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9 GHz Prescalar

CEL unveils the NEC UPG503B and UPG504B divide by 4 and divide by 2 prescalars that are capable of operating up to 9 GHz. The operating range is from 3 to 9 GHz and they feature a DC blocking capacitor at the input. The devices are hermetically sealed in 8-pin ceramic flat packages. **California Eastern Laboratories, Inc., Santa Clara, CA. Please circle INFO/CARD #212.**

ECL Compatible Oscillator

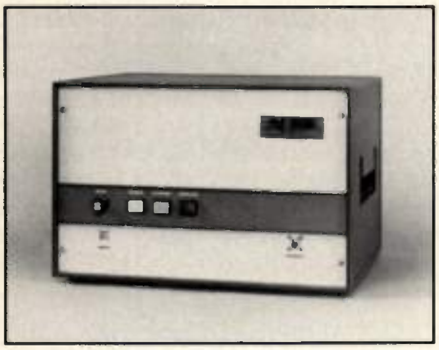
The K1149 Series ECL compatible crystal clock oscillators introduced by Motorola operate from 40 MHz to 150 MHz. They have an open emitter output which allows the user to select the load termination to optimize performance. The oscillators are enclosed in hermetically sealed metal packages and measure .82"× .52"× .245'(.345" for 125 to 150 MHz oscillators). **Motorola, Inc., Components Div., Franklin Park, IL. Please circle INFO/CARD #211.**

Absorptive Linearized Attenuator

The MA2694 from M/A-COM is a miniature voltage variable attenuator that incorporates a hybridized linearizer. The device occupies 0.75 cu-in and is offered with 40 dB or 60 dB dynamic range in standard or sub-octave bands from 2 to 18 GHz. **M/A-COM Components Group, Hudson, NH. INFO/CARD #210.**

150 W Amplifier

Amplifier Research unveils an amplifier that operates from 10 kHz to 220 MHz with output power of 150 W (min). A blanking input is provided to accept blanking pulses from external broadband sources. Full bandwidth is instantly available without need for tuning or bandswitching. The amplifier is immune to load-mismatch



problems, suffering no damage, foldback or oscillation under any magnitude or phase of source and load impedance. It is priced at $10,000. **Amplifier Research, Souderton, PA. INFO/CARD #209.**

Voltage to Frequency Conversion

The AD652 synchronous voltage to frequency converter offers ± 0.005 percent maximum nonlinearity and an on-chip buffered +5 V reference. It operates up to a maximum full scale frequency of 2 MHz and can perform a 16-bit A/D conversion in 32.77 ms. The internal +5 V buffered reference can supply up to 10 mA to an external load such as a bridge transducer to provide direct sensor to digital conversion. In 100's the AD652 is $6.95. **Analog Devices, Norwood, MA. Please circle INFO/CARD #208.**

GaAs Demultiplexer

MSC introduces the TDDX 1500A monolithic integrated serial to parallel data converter that can accept an ECL compatible high speed digital input of up to 1.5 gigabits/sec and demultiplex it into eight synchronous, ECL compatible output data streams. The device has a typical power dissipation of 1.8 W and output rise and fall times of 200 ps. It offers phase controlled divide by 8 clock and frame shift capability and comes in a 44-pin ceramic package measuring .65" square. **Microwave Semiconductor Corp., Somerset, NJ. INFO/CARD #207.**

Two-Phase Lock-In Amplifier

The 5210 is a lock-in amplifier that uses forth-order filters and optimized gain distribution to achieve up to 130 dB S/N

ratio. It can also be used as an independent oscillator, a frequency meter, a 4-channel DC voltmeter, and a programmable DC source. The operating frequency range is from 0.5 Hz to 120 kHz and the typical harmonic rejection is 80 dB. **EG&G Princeton Applied Research, Princeton, NJ. INFO/CARD #206.**

Sweep/Function Generators

The Models 421 and 422 sweep/function generators provide front-panel selection of sine, square and triangle waveform outputs. The 422 features a 6-digit LED display and can function as an internal/

external reading frequency counter to monitor circuit performance. Sweep frequencies have selectable start/stop ranges with 100:1 linear and 1000:1 logarithmic sweep ratios. These sweep ranges may be set at any two points within the 0.5 Hz to 5.0 MHz range. The 421 is priced at $535 while the 422 is $650. **Simpson Electric Company, Elgin, IL. Please circle INFO/CARD #205.**

Airborne/Portable GPS Receiver

An airborne/portable GPS receiver that tracks NAVSTAR GPS satellites to provide precise time transfer and geographic positioning data is available from Datum. The unit can provide time transfer accuracy of better than 1 us at vehicle speeds up to 600 knots. An internal algorithmn automatically determines geographical coordinates regardless of the unit's location. The basic configuration for the Model 9390-5700 includes a corrected 1-pps output, crystal oscillator, dedicated LED time of year display, LCD operation menu and status display, and external antenna/down converter assembly. **Datum, Inc., Anaheim, CA. INFO/CARD #197.**

Test Equipment Reference Guide

Technical specifications and prices for more than 4000 reconditioned test instruments, new instruments, coaxial components, waveguides and waveguide components, and a line of technical books is described in this book. Equipment categories range from amplifiers and analyzers to microwave components and power supplies. **Tucker Electronics Company, Garland, TX. INFO/CARD #184.**

Detector Products Catalog

This catalog from M/A-COM outlines the company's RF and microwave detector product line from 100 MHz to 18.0 GHz. Standard products as well as custom capability designs, and matched parameters packaging are featured. **M/A-COM Components Group, Hudson, NH. INFO/CARD #183.**

Foundry Design Guidelines

Crystal Technology has introduced *Foundry Design Guidelines,* a step by step procedure with which customers can design their own I/O devices on lithium niobate. The guidelines provide a description of the facility and services available in the foundry, a discussion of the generic processes required to fabricate I/O devices, a description of the specific device design procedures necessary to maintain compatibility with the foundry, a detailed discussion of mask design and fabrication, a description of device evaluation and packaging, and a step by step procedure using the guidelines to design an actual device. A refundable licensing fee is charged for the Foundry Design Guidelines. More information can be obtained by circling the reader service number. **Crystal Technology, Inc., Palo Alto, CA. INFO/CARD #182.**

Catalog Describes Signal Conditioning Filters

The active and passive signal conditioning filters described in this catalog have a frequency range of 0.1 Hz to 500 MHz. The catalog is broken down into a passive filter section and an active filter section. The filters described are bandpass, band reject and notch, lowpass, highpass, and programmable. The configurations described include Butterworth, Chebyshev, Twin-T notch, LCR Notch, Anti-aliasing, fixed tuned notch, tunable notch, and Bessel. **TTE, Inc., Los Angeles, CA. INFO/CARD #189.**

Brochure Describes Antenna Positioning Capabilities

A range of capabilities for the design and development of microwave antenna positioning systems is described in a brochure from MDM. It highlights the design, manufacturing, and test capabilities, and features a dual axis gimbal compact two-axis antenna positioner. **MDM, Inc., Chatsworth, CA. INFO/CARD #181.**

Signal Sources to 23 GHz Described in Catalog

CTI has published a catalog providing product data and technical information on its line of RF/microwave sources and multipliers. The devices described include: mechanically tunable phase locked signal sources, low phase noise FM modulatable sources, mechanically and voltage tunable cavity stabilized oscillators, microwave frequency multipliers, single and multiple phase locked crystal oscillators, and 70/140 MHz wideband frequency modulators and demodulators. Also described are products such as the COHO/local oscillator assembly. Technical articles included describe phase locked microwave signal sources and techniques for measuring and interpreting short term frequency stability and tune-up procedures for solid-state phase locked sources. **Communication Techniques, Inc., Whippany, NJ. Please circle INFO/CARD #180.**

Analog Dialogue

Analog Dialogue is a journal on circuits, systems and software for signal processing. Volume 21-1 describes the AD693, a monolithic process control transmitter IC, the 2S81, resolver to digital converter, and the AD9002 150-megasample-per-second analog to digital converter. **Analog Devices, Norwood, MA. INFO/CARD #186.**

BAW Delay Devices Catalog

This catalog describes bulk acoustic wave delay devices in a variety of packages. These devices meet delay requirements from UHF through Ku band with instantaneous broadband processing. They offer non-dispersive insertion delays from 0.2 to 30 us. **Teledyne Microwave, Mountain View, CA. INFO/CARD #185.**

COMMUNICATION DESIGN ENGINEERS

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