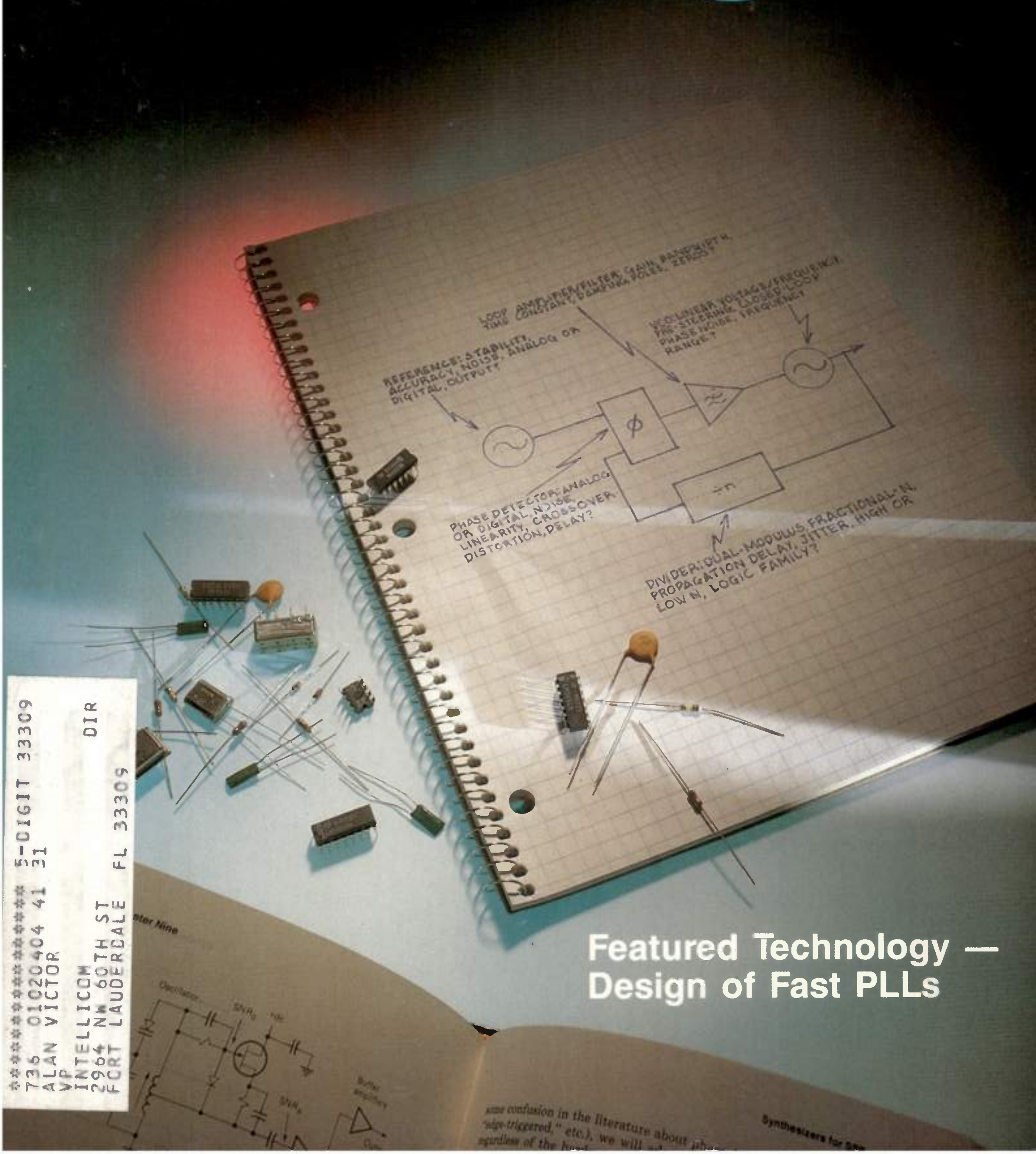
rf design

engineering principles and practices

1978–1988 10th ANNIVERSARY

May 1988



Featured Technology — Design of Fast PLLs

They needed ultra reliability at 650 watts and 120-microsecond bursts to make T/CAS fly.

The best anyone could do at 650 watts was 10-microsecond pulse bursts with 1% duty cycles—nowhere near what it would take to get the Traffic Alert/ Collision Avoidance System (T/CAS II) program off the ground.

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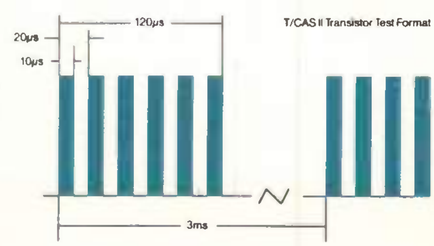

Acrian delivered the 650-watt, 120-microsecond, 50% duty cycle pulse bursts needed in the transistor. And T/CAS II took off.

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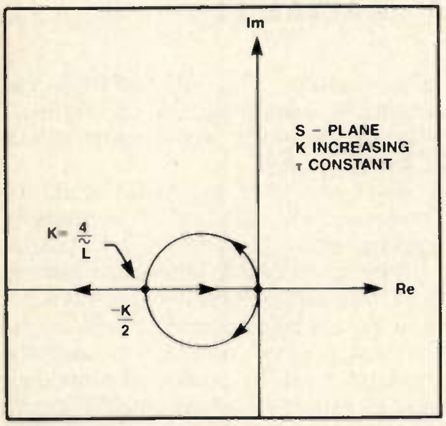
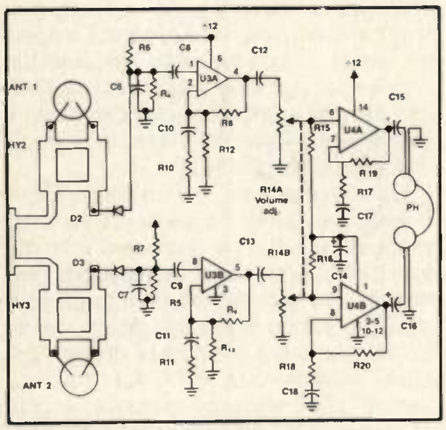
rf design

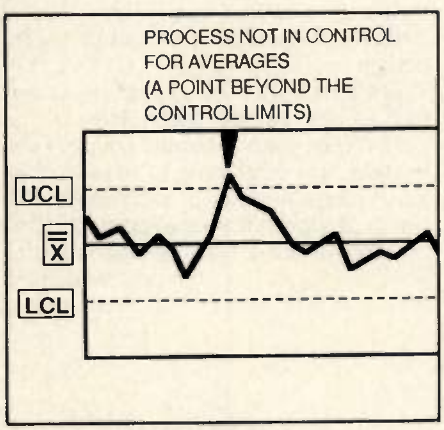
May 1988



Page 26 — PLL Design



Page 43 — Aircraft Warning System



Page 55 — EMC Quality Assurance

Cover Story

Featured Technology Section

Departments

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rf editorial

Technologies to Watch

By Gary A. Breed
Editor

The most fascinating aspect of an editor's job is the opportunity to look at the "big picture" of the RF industry. It is exciting to discover new technologies — components, instruments or design techniques — and watch them develop into useful tools for RF engineers. Here are some of the most interesting ideas that have caught my attention:

Solid State RF Power. The continuing move toward higher power and higher frequencies may be old news, but the search for devices and methods is still going strong. At lower frequencies, power FETs are already around that can deliver 1 kW per device in switching and servo applications. These are now reaching tens of MHz speeds. At the higher frequencies, bipolar and FET devices, plus the techniques to combine them, are upping the limits on an almost daily basis.

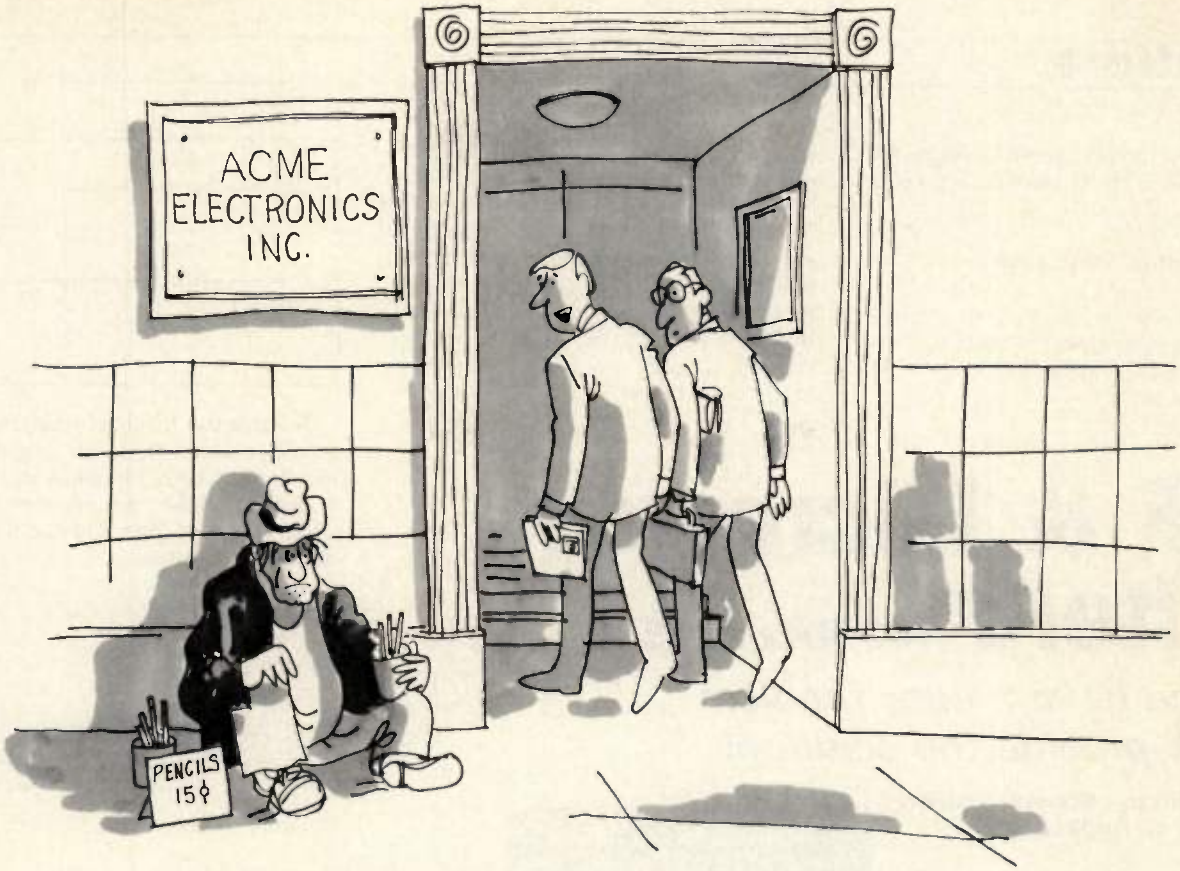
Silicon ICs. Analog integrated circuits are beginning to undergo the same quantum leap in density and complexity that digital ICs have already accomplished. Custom and semi-custom ICs can now be obtained with RF performance to a hundred MHz or more. Lower power consumption, smaller size, and much easier manufacturing of a finished product are advantages of highly integrated RF circuits. No more will RF engineers wonder, "Why doesn't someone make an IC to do what I need?" They will just have one created for them. Standard "catalog item" ICs are becoming more complex and capable, as well.

Test Instruments. Two related trends are worth watching: top of the line instruments getting more powerful for the same money, and "basic" equipment costing less. New components and creative engineering are being combined with microprocessor computing power to make the best use of new technology. The introduction of very low cost synthesized signal generators, spectrum analyzers and other essential RF instruments is especially exciting.

Computer Modeling. RF is finally getting the combination of accurate models for circuit design and analysis, and the right attitude among engineers that CAE can replace a large portion of traditional RF sorcery. (Hopefully, a little black magic will always be needed.)

Combinations of Technologies. Competition and performance demands have made it essential for engineers from different disciplines to get together. Not only does the project benefit from the organized integration of analog, digital, mechanical and other aspects of design, but each engineer learns things that can benefit his particular specialty. Digital engineers are finding that analog implementation of a function is sometimes the best option, and RF guys are discovering the value of digital manipulation, using formerly unthinkable "1s and 0s" technology.

The best part of all this activity is just that — it's *active!* Technology is the natural outgrowth of human curiosity and intellect. It is comforting to know that my job involves an area of technology with plenty of growth and development left to be accomplished. But more than that, it's just plain fun to have the best seat in the house for watching that growth happen.



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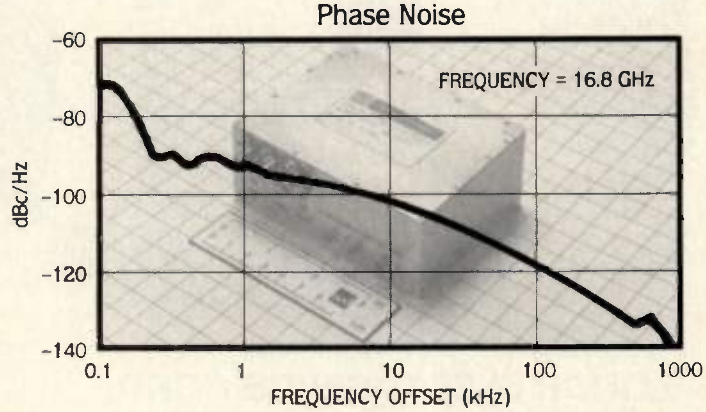
Phase Noise



For more details on Watkins-Johnson phase-locked oscillators, contact VCO Applications Engineering, 440 Kings Village Road, Scotts Valley, California 95066-4081, or telephone (408) 438-2100, ext. 4260.

WATKINS-JOHNSON

INFO/CARD 5

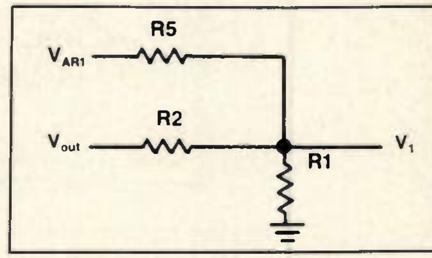
Letters should be addressed to: Editor, *RF Design*, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111.

'Feedforward' Feedback

Editor:

First of all, let me thank you for producing a very fine magazine. It is one I look forward to receiving, and read cover to cover each month.

In the February 1988 issue of *RF Design*, page 85, is an article entitled "Feed-Forward Compensation for Improved DC Performance." I have a problem accepting the mathematics in the feedforward compensation example. In particular, the gain expressions for two of the resistor networks. Referring to Figure 2, the resistor network consisting of R1, R2, and R5 is reproduced below:



The transfer function (gain) from each amplifier output (V_1 and V_{out}) to the resistor common point (negative input of A_{Rh}) is easily derived from nodal analysis.

Let $G_i = 1/R_i$, then, the nodal equation about V_1 becomes:

$$V_1 * (G1 + G2 + G5) = G5*V_{ar1} + G2*V_{out}$$

Solving for V1 yields:

$$V_1 = \frac{G5*V_{ar1} + G2*V_{out}}{G1 + G2 + G5}$$

In terms of resistance, V_1 becomes:

$$V_1 = \frac{R1*R2*V_{ar1} + R1*R5*V_{out}}{R5*(R1 + R2) + R1*R2}$$

The gains, R_T and R_Z are expressed as:

$$R_T = \frac{R1*R2}{R5*(R1 + R2) + R1*R2}$$

and

$$R_Z = \frac{R1*R5}{R5*(R1 + R2) + R1*R2}$$

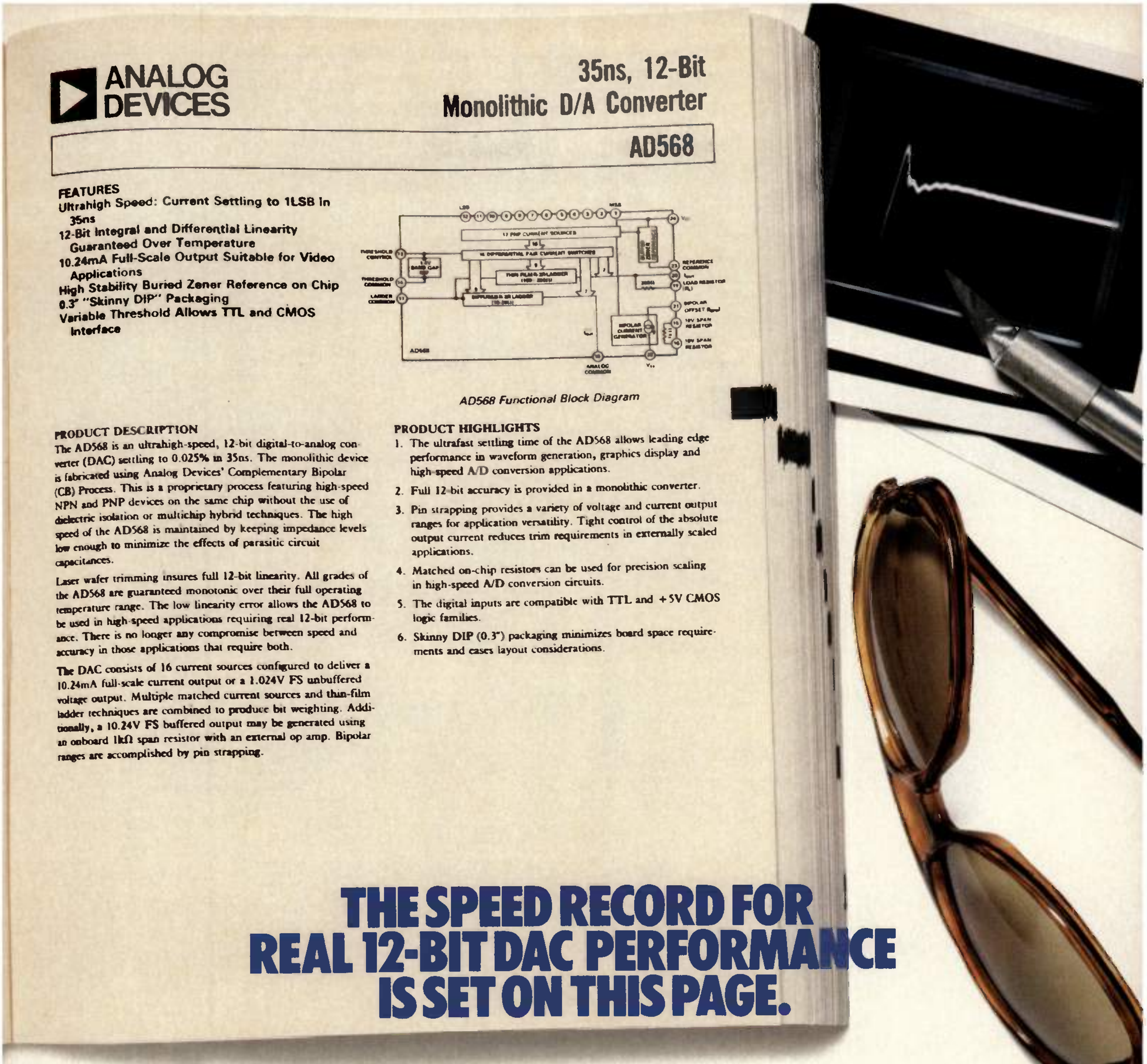
These gain expressions are considerably more complicated than the simple voltage-divider equations presented in the article. The block diagram symbolic manipulation appears correct in Figures 3 through 7.

If the computer responses are based on the gains as implied by the results of the block diagram manipulation, then I must challenge whether the computed responses are correct. Because the gain errors are on an interior loop, the overall effect is reduced by the overall feedback loop. The differences might not show up very much in a coarse (large frequency step) plot as shown in the article.

Thank you for your attention.

Bruce K. Murdock
General Motors Corp.
Delco Systems Operations
Goleta, CA

The author's response is printed on page 17.



ANALOG DEVICES

35ns, 12-Bit
Monolithic D/A Converter

AD568

FEATURES
Ultrahigh Speed: Current Settling to 1LSB In 35ns
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10.24mA Full-Scale Output Suitable for Video Applications
High Stability Buried Zener Reference on Chip
0.3" "Skinny DIP" Packaging
Variable Threshold Allows TTL and CMOS Interface

AD568 Functional Block Diagram

PRODUCT DESCRIPTION
The AD568 is an ultrahigh-speed, 12-bit digital-to-analog converter (DAC) settling to 0.025% in 35ns. The monolithic device is fabricated using Analog Devices' Complementary Bipolar (CB) Process. This is a proprietary process featuring high-speed NPN and PNP devices on the same chip without the use of dielectric isolation or multichip hybrid techniques. The high speed of the AD568 is maintained by keeping impedance levels low enough to minimize the effects of parasitic circuit capacitances.

Laser wafer trimming insures full 12-bit linearity. All grades of the AD568 are guaranteed monotonic over their full operating temperature range. The low linearity error allows the AD568 to be used in high-speed applications requiring real 12-bit performance. There is no longer any compromise between speed and accuracy in those applications that require both.

The DAC consists of 16 current sources configured to deliver a 10.24mA full-scale current output or a 1.024V FS unbuffered voltage output. Multiple matched current sources and thin-film ladder techniques are combined to produce bit weighting. Additionally, a 10.24V FS buffered output may be generated using an onboard 1kΩ span resistor with an external op amp. Bipolar ranges are accomplished by pin strapping.

PRODUCT HIGHLIGHTS
1. The ultrafast settling time of the AD568 allows leading edge performance in waveform generation, graphics display and high-speed A/D conversion applications.
2. Full 12-bit accuracy is provided in a monolithic converter.
3. Pin strapping provides a variety of voltage and current output ranges for application versatility. Tight control of the absolute output current reduces trim requirements in externally scaled applications.
4. Matched on-chip resistors can be used for precision scaling in high-speed A/D conversion circuits.
5. The digital inputs are compatible with TTL and +5V CMOS logic families.
6. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.

THE SPEED RECORD FOR REAL 12-BIT DAC PERFORMANCE IS SET ON THIS PAGE.

If your high-speed DAC applications are often plagued by a loss of accuracy, we'd like to direct you to our AD568. With a settling time of only 35ns to ± 0.025%, no other monolithic DAC is faster. And it combines this speed with unmatched ± 1/4 LSB integral nonlinearity, as well as guaranteed monotonicity over the entire operating temperature range, for real 12-bit performance.

This unique combination of speed and accuracy allows you to delve into new application areas like high-speed/high-resolution A/D converters, vector graphic displays, and direct digital frequency synthesizers.

For design versatility, the AD568 offers a variety of user-programmable voltage and current outputs. And all this comes in a skinny 0.3" CERDIP package, which conserves board space and allows for auto-insertion.

The AD568 delivers an unmatched level of performance with prices starting at only $35 in 100s. Now you could spend almost twice that for other high-speed monolithics, and still not get the same level of accuracy as the AD568. And while some hybrids might come close in performance to the AD568, they also cost twice as much.

To find out how the AD568 can help set speed records for your designs, call Applications Engineering at (617) 935-5565, Ext. 2628 or 2629.

Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

ANALOG DEVICES

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INFO/CARD 7

rf news

1988 IEEE MTT-S Slated for May 24-27

The Microwave Theory and Technique Society (MTT-S) of the Institute of Electrical and Electronic Engineers (IEEE) will be hosting the 1988 IEEE MTT-S at the Marriott Marquis Hotel in New York city from May 24-27 with technical sessions and exhibits from May 25-27 at the Jacob Javits Center, also in New York city. The publicity chairman for the symposium, Bertram D. Aaron, anticipates a registration of 7,500.

The theme this year, "Microwaves, Past, Present, and Future," will celebrate the 100th anniversary of Heinrich Hertz's demonstration on radio waves. Features of the show include an exhibit of replicas of Hertz's work and four papers devoted to Hertz, which will be delivered at the sessions.

The exhibition will have more than 270 microwave companies with a total of 455 booths. The displays will include new microwave products, instruments, accessories and components. Representatives from the companies will be on hand to meet the symposium registrants and discuss technical problems and solutions.

The technical program held jointly with the Microwave and Millimeter-Wave Monolithic Circuits (MMIC) symposium and the ARFTG conference offers a diverse program. The 104 members of the Technical Program committee, divided into 22 subcommittees, selected 100 regular, 65 short and 48 open forum papers. In addition, 12 papers were selected by the MMIC symposium for three joint sessions with MTT-S. Twenty seven invited papers which represent recent technical advances are also scheduled.

The format of the symposium will include regular sessions, focused sessions, European microwave sessions, open forum sessions, panel sessions and workshops. A plenary session will open the symposium on Wednesday morning May 25th. There will be four regular sessions a day which will run for 90 minutes each. The focused sessions cover areas such as high power microwaves, fiber optic links and transmission systems. The European sessions are designed to update the attendees on technology developments throughout Europe. The panel sessions, from noon to 2 p.m. will be held on the 25th, 26th and 27th. Topics to be covered encompass "U.S. Competitiveness in the World Market", "Heterojunction Bipolar Transistor Circuits", "Ferrites at Millimeter Wave Frequencies" and "Noise Measurements".

Eight workshops are planned for Monday and Tuesday. They include "MIC and MMIC FET High Power Amplifier Design Techniques", "Superconductivity and Microwaves", "Packaging Hybrid and Monolithic Microwave and Millimeter Wave Components", "Designing MMICs Through Foundries", "FET Structures and Their Modeling", and "CAD Oriented Modelling of Discontinuities in Microwave/Millimeter Wave Transmission Line Structures". The program committee has also scheduled sessions on solid state devices and their applications, measurements, filters, passive components, MICs, phased array techniques, field theory, guided waves and microwave CAD.

Other scheduled activities for the symposium include a student program, an industry cocktail party, awards banquet, and guest hospitality suite. The student program will consists of students from various metropolitan New York area high schools. They will attend the sessions and exhibits that emphasize Heinrich Hertz's pioneering experiments. They will also tour the exhibit area and will have the opportunity to interact with engineers and scientists at the symposium.

Boeing Selects AIRLINK Antenna

Boeing has selected Ball Corporation as its supplier for satellite communication antennas for its 747-400 aircraft. Ball's AIRLINK antenna will be a standard option available to Boeing airline customers. Airlines can now use satellite communication systems for air traffic control communications, engine monitoring, dispatch information, weather reports, crew change orders and the selection of flight paths that will save fuel.

Also, these systems will enable the cabin crew to provide passengers with up-to-date information on connecting flights, departure times and gate locations. Passenger services such as telephones, portable computers and facsimile machines will also be available. In addition passengers can enjoy computer shopping, teleconferencing, access to news and information services, and the ability to make or change travel arrangements in-flight.

European EMC Market to Grow

In the USA the imposition of regulations by the Federal Communications Commission has boosted growth in demand for EMC products and services. Frost and Sullivan's 1986 report on markets for EMC products and services in the USA identified a strong high technology industry growing at an average annual rate of 8.5 percent. Certain product sectors were, however, forecast to grow well above this average rate.

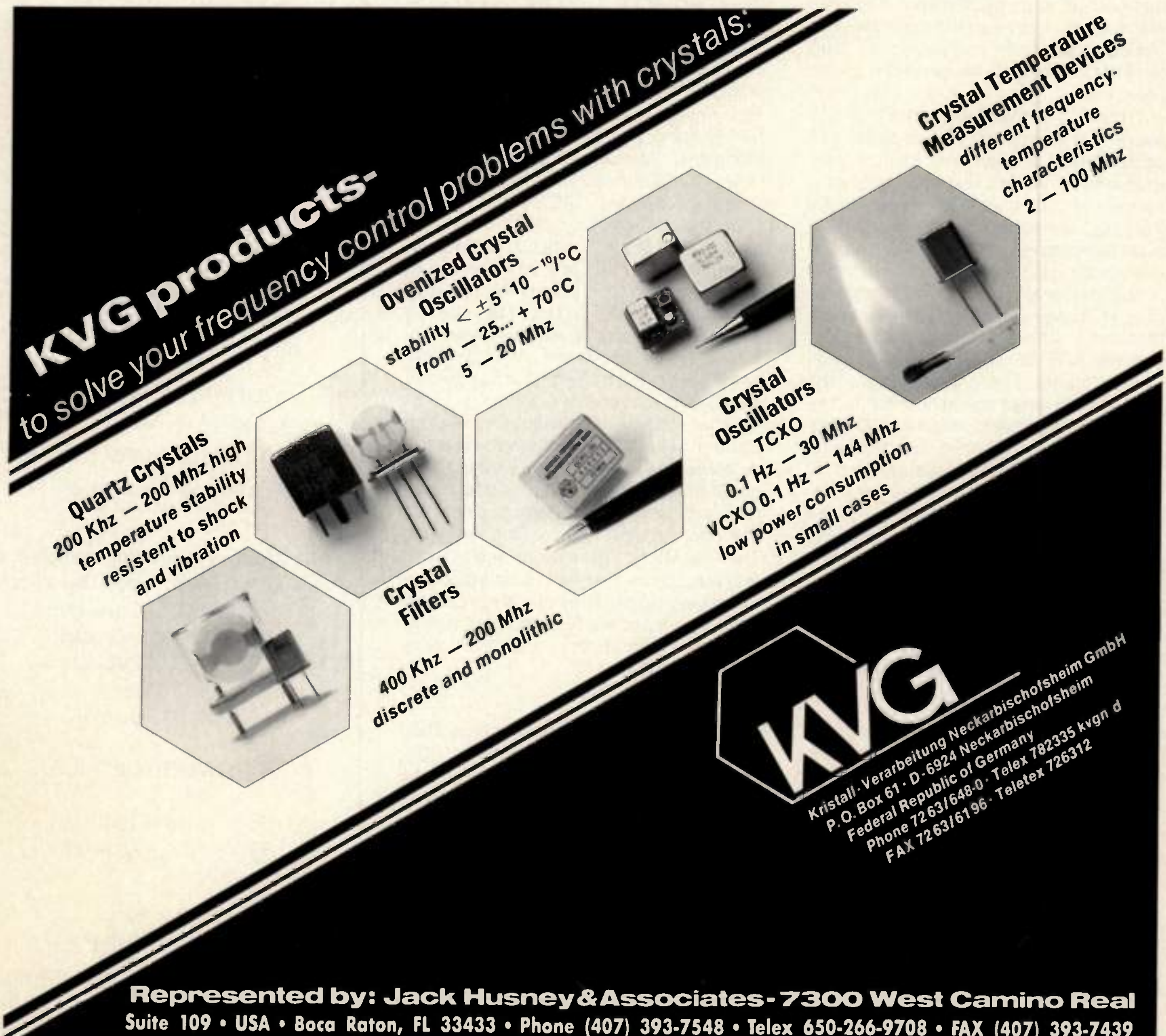
Frost and Sullivan is now publishing its first study on the European market for EMC products and services, which identifies a considerably smaller market than that currently exists in the U.S.A. but one which is forecast to grow much more rapidly through the next decade. The market is estimated to have been worth nearly $200 million in 1986 and is forecast to grow to over $510 million by 1993 in constant dollar terms. This produces an average annual growth of 15 percent. The report analyses and forecasts the West European market for ten EMC product or service categories covering conductive coatings, conductive fillers, conductive polymers, conductive gaskets, filters and suppressors, connectors, shielded cabinets and rooms, test equipment, design consultancy, and test and calibration. The report costs $2,600 and is available from Frost and Sullivan, Inc. at (212) 233-1080.

Radar Monitors Vital Signs

Biomedical researchers at Georgia Tech have developed a radar that can read vital signs at a distance of more than 100 yards. In hospitals, the device would permit non-contact monitoring of burn patients and infants, while in the emergency room, it would speed up the collection of vital signs data.

Microwave Circuit Design Center Established at CU-Boulder

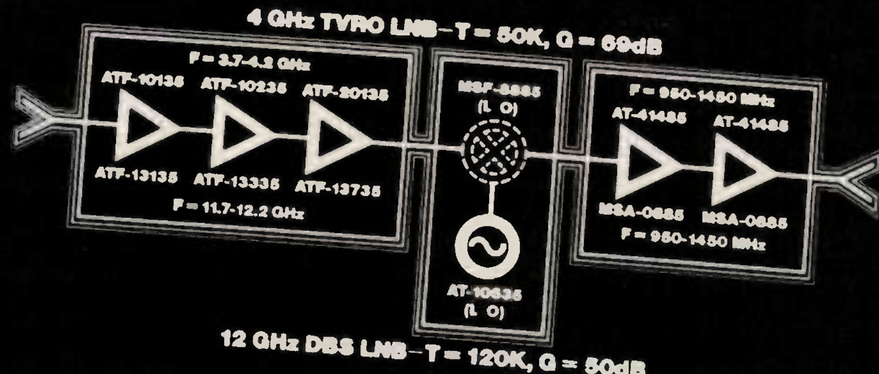
A new multi-million dollar research center has been established at the University of Colorado at Boulder to develop computer-aided techniques for the design of advanced microwave and millimeter-wave integrated circuits. Researchers at the center will focus on the modeling,



Quartz Crystals INFO/CARD 71 Crystal Filters INFO/CARD 72 Ovenized Crystal INFO/CARD 73

Crystal Oscillators INFO/CARD 74 Crystal Temperature INFO/CARD 75

Just What The Doctor Ordered



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Part Number	Frequency (GHz)	Noise Figure (dB)	Gain (dB)
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ATF-13135	12.0	1.2	9.5
AT-41485	1.0	1.4	20.0
MSA-0885	1.0	3.3	22.5

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design methods and non-destructive measuring techniques essential in developing these circuits. A five-year $250,000 grant for the center is being provided by the National Science foundation. The grant will be supplemented with funding from several federal agencies. In addition, a total of $500,000 annually has been pledged to the MIMICAD center by 10 industrial R&D organizations.

Small Enclosure EMI Testing Now Possible

Eaton's 3500 shielded enclosure leak detection system or sniffer, used in testing the EMI shielding effectiveness of large shielded rooms, has been successfully used in testing small EMI filter enclosures for shielding effectiveness. This breakthrough in small enclosure testing will save companies test time by eliminating lengthy calculations. More information on this test method can be obtained from Eaton at (213) 822-3061, ext. 255.

Burle Purchases Former RCA Division From GE

Burle Industries, Inc., formerly RCA new products division, has purchased RCA businesses and the Lancaster, Pennsylvania facility from General Electric. RCA founded the new products division to establish new businesses and to provide advanced products for the corporation's future. However, the 1986 acquisition of RCA by General Electric forced a change in strategy and resulted in the divesture of the Lancaster facility.

Magnetek ALS Signs Naval Contract with Japanese

The Japanese Defenses Agency (JDA) has recently agreed to purchase MagneTek ALS frequency converters for use on its guided- missile destroyers. The contract was negotiated for the ALS Standard Family of PACE (Pulse-Synthesized, Advanced Conversion Equipment) units by the company's Japanese trading company, Nissho Iwai.

David Sarnoff and Compact Software Announce Marketing Agreement

The David Sarnoff Research Center and Compact Software have announced a marketing agreement to sell and support a microwave tuning system called the Programmable Microwave Tuner System (PMTS). The tuning system is computer controlled and simplifies the characterization of microwave devices by providing accurate measurements of noise and impedance parameters.

W-J Shares Profits

Watkins-Johnson Company announced that $4,947,000 of 1987 company profits is being shared with employees. This profit sharing program was instituted in 1967 and is the 21st consecutive year that a significant portion of profits has been shared with employees.

Flam & Russell Wins Contract

Flam & Russell has been awarded a $770,000 contract to provide a customized automated system to Norden Systems, Inc., of Norwalk, CT. The system will be used for high accuracy test and evaluation of the Joint-Stars phased array and for general purpose testing in the 1.0 to 18 GHz band. Positioner equipment is being provided by Orbit Advanced Technologies.

Rantec Opens New Plant

Rantec Anechoic/EMI Systems Group has expanded its anechoic material manufacturing capability and capacity with the opening of a 94,000 square foot plant in Durant, Oklahoma. This plant will triple Rantec's manufacturing capacity of microwave absorber material used in RF shielded and non-shielded anechoic chambers.

EEsof and SDA Sign OEM Agreement

EEsof, Inc. has announced a joint agreement with SDA Systems, Inc. where EEsof will become an OEM/remarketer of selected SDA products, and in turn become a vendor of a complete turnkey CAE/CAD system for the MMIC microwave/RF market. EEsof has agreed to purchase the Design Framework™, schematic capture, mask layout, and physical design verification software applications from SDA, integrate EEsof proprietary microwave circuit simulation tools, develop custom interfaces, and sell the complete turnkey MMIC Design Workstation™ to participate in the U.S. government MMIC program and to the commercial microwave/RF industry.

rf letters *Continued*

The Author's Reply

Editor:

I appreciate Mr. Murdock's interest in my article, "Feed-Forward Compensation for Improved DC Performance." In the article I did not mention that in the actual circuit R5 is much greater than R2 and R1. In addition, R2 is much greater than R1. Using the law of superposition and the above assumptions, the voltage divider relations in the article are correct. However, addressing the more general solution as above, R_T becomes:

$$R_T = \frac{(R1{*}R2)/(R1 + R2)}{(R1{*}R2)/(R1 + R2) + R5}$$

R_z becomes:

$$R_z = \frac{(R1{*}R5)/(R1{*}R5)}{(R1{*}R5)/(R1 + R5) + R2}$$

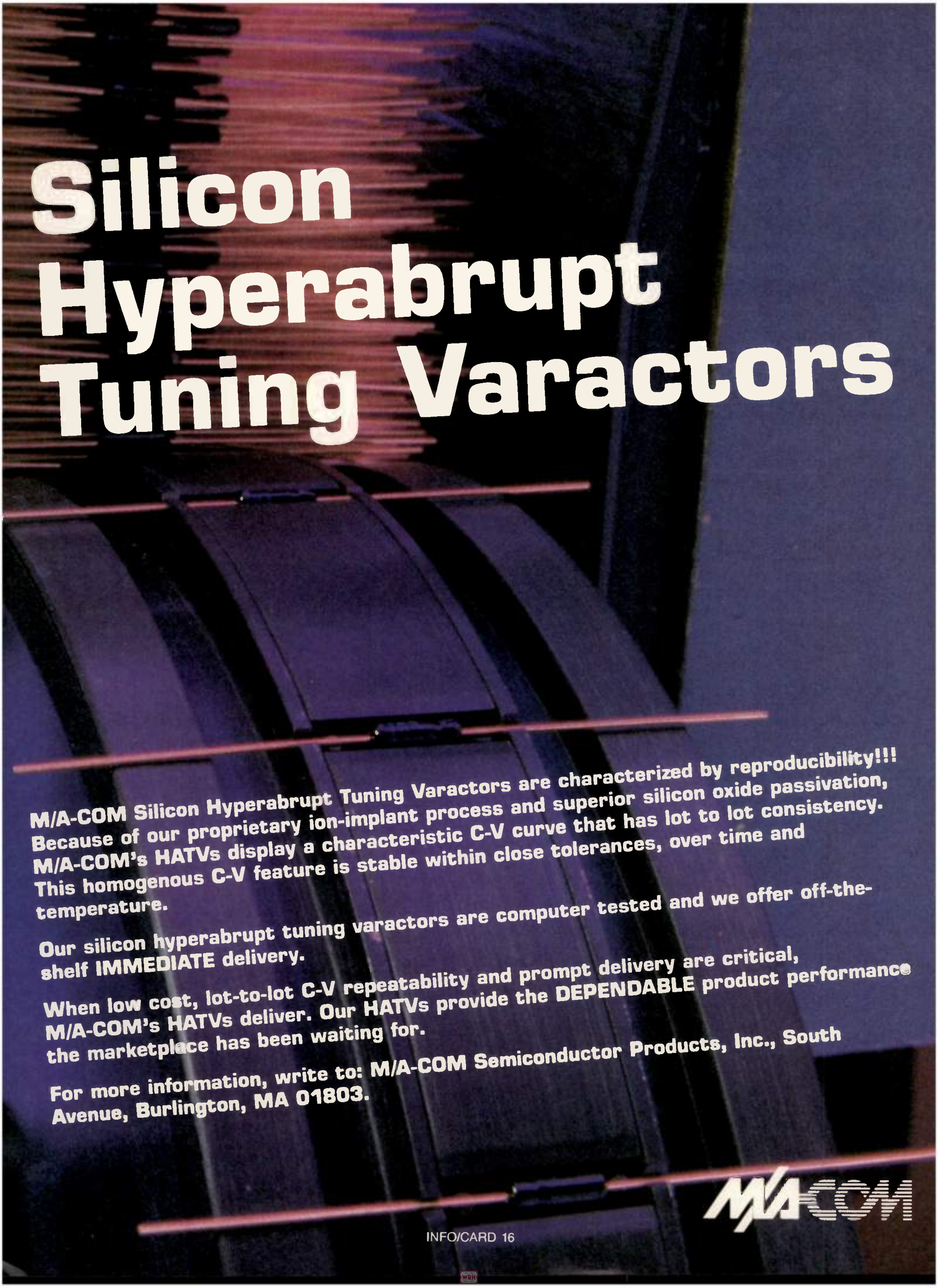
Using the assumptions discussed earlier, these expressions reduce to the voltage divider relations in the article. Again, I appreciate the interest and the comments.

Stan Goldman
Scientific Communications
Garland, TX

Raytheon Wins Sonar Computer Contract

Raytheon Company's Submarine Signal Division has won a contract valued in excess of $10 million by the Applied Physics Laboratory of John Hopkins University of Laurel, Md., to develop and produce a land-based computer system that processes, stores, displays and helps evaluate sonar data recorded from the realtime sea patrol histories of U.S. Navy submarines. Delivery is scheduled in early 1990.

The proposed processor/analyzer will include beamforming and general signal processors to process sonar data at greater than real-time rates. Raytheon will design, fabricate and test the system along with accompanying peripheral equipment and computer software.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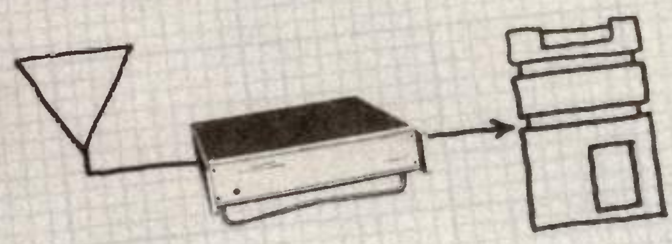

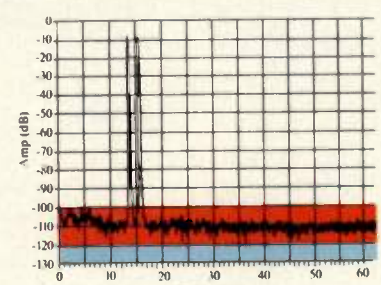

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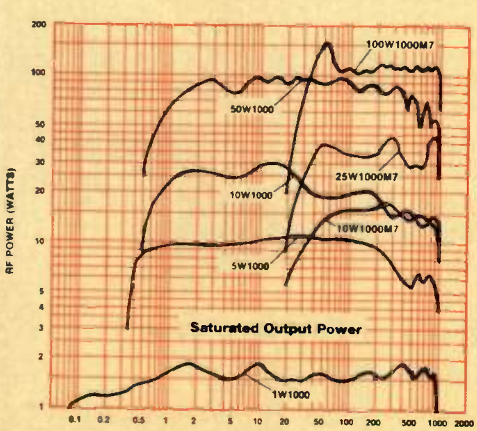

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rf cover story

Phase Locked Loop Design

The Number One Topic in RF Engineering

Synthesizers of all types, and phase locked loops (PLLs) in particular, represent the current design tasks of more RF engineers than any other circuit function.

One big part of this activity is PLLs for general purpose applications; most with modest performance requirements. These design efforts include auto, home and portable radio receivers, television sets, amateur radio equipment, cellular telephone systems, plus land mobile, marine and aviation radios.

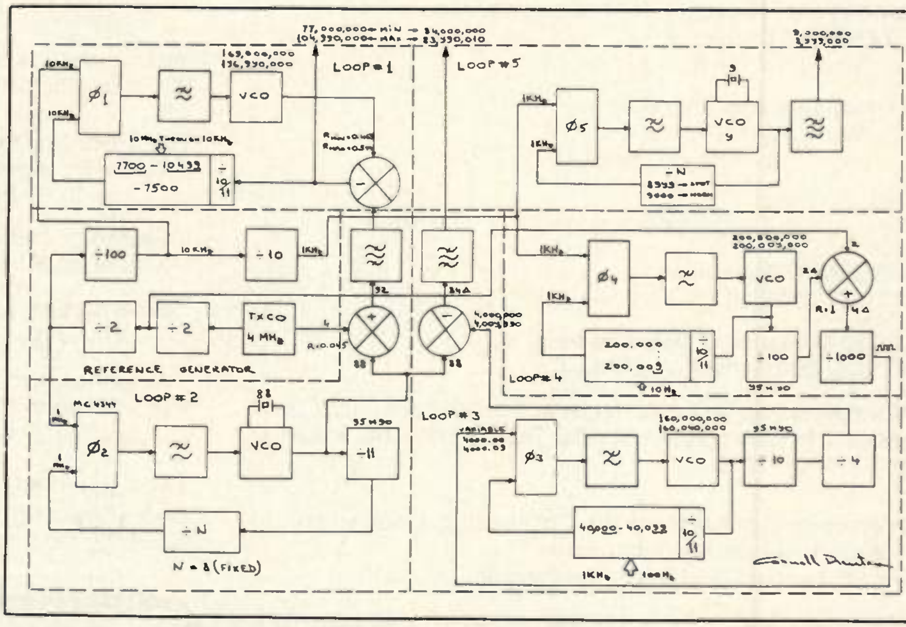
Another significant portion of PLL design activity is in data communications, where system clocks have to be synchronized to an incoming data stream. Instrumentation represents another area of action, in synthesized signal generators, spectrum analyzers that phase lock to an external signal, and internal reference frequencies locked to an external precision standard. Yet another application is FM demodulation in terrestrial and satellite communications systems.

By far, the most technically interesting and demanding applications are in military fast frequency hopping communications and countermeasures systems. Synthesizers for such systems require rapid switching between frequencies, low levels of spurious generation, plus noise specifications adequate for receiver sensitivity and broadband radiation requirements. In addition, most military systems have significant constraints on allowable size and power consumption.

The Primary Design Challenges

Each element of the PLL has a set of particular problems, especially when fast response is required. Being a negative feedback system, a PLL automatically has a significant time delay. This limits the rate at which the frequency can be changed. High speed circuitry in the feedback loop (divider, phase/frequency detector and loop filter/integrator) increases the speed of a step change in frequency, but there are other limitations, as well.

Noise, spurious responses and sidebands are all part of a PLL system. Because the output is voltage tuned, any extraneous voltage impressed upon the control voltage will show up as instantaneous frequency (phase) noise. This can include everything from reference feedthrough to power supply ripple. Assuming these matters are dealt with, the loop elements then become the major contributors to phase noise.



A high resolution synthesizer for an HF communications system; from "Designing Frequency Synthesizers" by Cornell Drentea, Proceedings, *RF Technology Expo 88.*

The divider has jitter in the edge placement of its output waveform. This varies with the logic family type and the logic configuration of the divider. The phase detector, usually digital, has it own jitter plus a degree of uncertainty at a near-zero phase difference, where output pulse widths reach the limits of the device's performance.

The loop filter integrates the phase detector output pulse train. The narrowest bandwidth will filter out high frequency energy and reduce the phase noise sidebands. However, the response time will also be slowest. At the other extreme, a very wide filter will allow fast response, but will not attenuate as much noise. This is the "catch 22" of PLLs — loop bandwidth vs. phase noise.

Finally, the reference and VCO are both subject to the design constraints of all oscillators. The reference is usually a single-frequency, high stability oscillator which is a well- documented item. However, some designs use multiple references, or the reference may be another PLL loop or a different type of synthesizer. The VCO will exhibit a certain sensitivity to its environment, and will have a not-necessarily-linear frequency vs. voltage characteristic. High performance PLLs often require multiple VCOs, each covering a limited frequency range.

Modeling PLL Behavior (S/H)

The development of accurate models and realistic predictions is an essential part of PLL engineering. Any effort to approach the theoretical limits of performance cannot be solely empirical. Few engineers designing high performance PLLs do so without the assistance of computers. The software may be purchased or written in-house, but both require good mathematical models for accurate results. The two articles included in the following Featured Technology section address the modeling issue.

Jeff Blake's analysis of the most common phase locked loop configuration was developed as part of his work with fast-hopping synthesizer design. The second article, by Corinn Fahrenkrug is intended to assist the RF engineer who is designing PLLs with commercial software. She defines the specifications that the programs typically require, so the user can create realistic input data.

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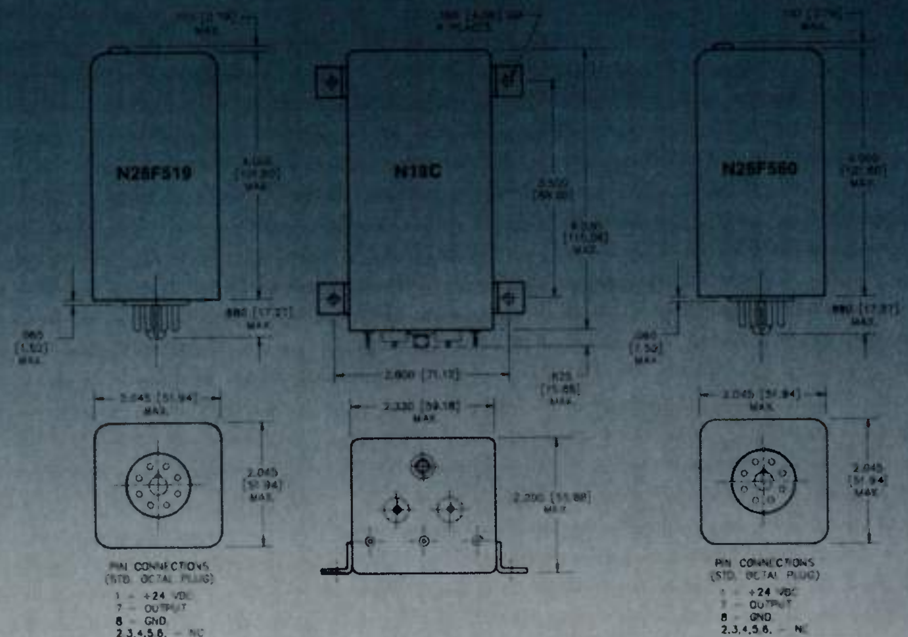

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Design of Wideband Frequency Synthesizers

An Analysis of Type-2, Second-Order Phase-Locked Loop Frequency Synthesizers

By Jeff Blake
Fairchild Weston Systems Inc.

Although classical, continuous-time analysis is commonly used for phase-locked loop (PLL) frequency synthesizers, it is only applicable for loop bandwidths that are no more than just a few percent of the reference frequency. But for high performance frequency agile synthesizers, requiring much wider bandwidths, this technique is far from adequate. This is due to the discrete-time, or sampling nature of all PLLs that incorporate digital circuitry such as dividers and phase detectors. Much has been written to describe what the effect is on loop performance and stability. Some have even attempted to show how to include some sort of fudge factor into the design. The subject of this paper, however, is not how to design around the PLLs sampling nature, but how to design with it, through exact analysis.

It has been considered that the most important factor when designing a hopping synthesizer is the loop bandwidth. This specific statement will be shown to be false. Also, time honored concepts such as the damping coefficient, Z, and natural frequency, ω_n, will be abandoned for more meaningful, physical design constants such as loop gain (K) and τ, the loop filter time constant. It is apparent that K is the popular constant to study. But it will be shown that τ cannot be ignored especially in hopping synthesizers, where the controller must be carefully designed.

Figure 1 shows a common PLL. The phase detector used is a typical phase/frequency detector, with charge pump and shunt R-C loop filter. This gives rise to the phase detector and loop filter transfer functions shown in Figure 1. Letting the loop gain, K, be defined as:

$$K = \frac{K_p \cdot K_v}{N} \tag{1}$$

the open loop transfer function is:

$$G(s)H(s) = \frac{K}{s} \cdot \frac{s\tau + 1}{s\tau} \tag{2}$$

and the closed loop transfer function becomes:

$$\frac{C(s)}{R(s)} = \frac{KN\,(s + 1/\tau)}{s^2 + Ks + K/\tau} \tag{3}$$

The denominator of the closed loop transfer function is known as the characteristic equation. It is the roots of this equation that determine the stability and performance of the loop with the aid of a root locus. It is obvious that the roots are dependant on K, and τ. In Figure 2a, the root locus is shown for K being held constant, and τ varying from 0 to ∞. Figure 2b shows the root locus for τ constant, and K varied from 0 to ∞. Since the roots are always in the left-hand plane for all K and τ, the system described by these equations is unconditionally stable for all loop bandwidths, and all degrees of damping.

The roots of the characteristic equation are given by:

$$\frac{-K}{2} + \sqrt{\left[\frac{K}{2}\right]^2 - \frac{K}{\tau}} \tag{4}$$

and, in general, are complex. They become real when:

$$\tau = 4/K \tag{5}$$

This is the boundary between the underdamped and overdamped step responses, with the boundary itself yielding a critically damped response. In the root locus plots, this boundary is the point of convergence. When designing a hopping synthesizer, a critically damped response is chosen since it yields the fastest response time.

When constructing a PLL, a continuous system is usually never built. Digital dividers are commonly incorporated within the feedback path, interfacing with a digital phase detector. Since information exists only at the logic transitions, the PLL used here is clearly no longer a continuous system, but a discrete-time system.

This discontinuity has been addressed for some time (1, 2, 3). Many attempts have been made to describe this discrete-time behavior by introducing a pure time delay term equal to one reference period (4, 5, 6, 7). Commonly it has been introduced into the feedback path, and called *divider delay,* or *transportation lag.* This model, shown in Figure 3, is not the best one to consider.

The error arises by modeling the discontinuity as an actual time delay: the same delay that would be present in a delay line. Modeling the discontinuity as such was the result of the fact that the logic transitions are spaced by one reference period, thereby stating that there is a time delay equal to that amount. It might be apparent that this represents worst case, and the delay term should be less severe. Appendix A develops an equivalent delay term from the exact analysis by using a narrowband approximation, demonstrating a factor of one half. This result is also independently developed in References 8, 11, and 12. The more precise method is then to accept this discontinuity as a phenomenon due to the sampling nature of the loop, and apply an appropriate model.

To arrive at the appropriate model, it is helpful to examine the system controller and the mechanism by which the VCO is controlled. The two inputs to the digital phase detector, namely the output of the digital divider in the feedback path and the reference frequency, control the DC voltage applied to the VCO. More specifically, a capacitor is charged to the necessary voltage and held there. Translation of logic signals into an analog voltage such as this is the behavior of a zero-order hold (ZOH). Figure 4 shows

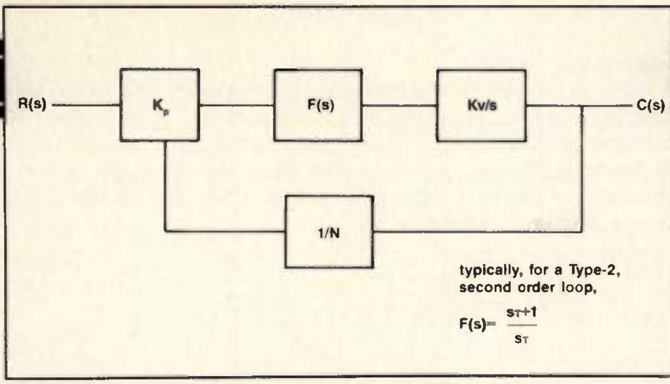

Figure 1. Block diagram for a basic PLL.

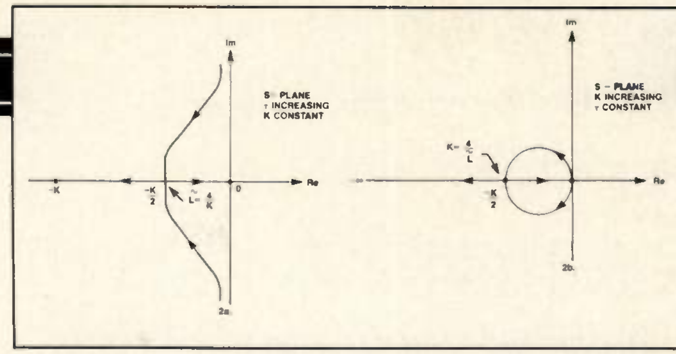

Figure 2a. Root locus for K constant and τ varying.
Figure 2b. Root locus for τ constant and K varying.

the model of the system to be studied. This model (2, 3) is not restricted to explicit sample-and-hold phase detectors.

For this model, the open loop transfer function is:

$$G(s)H(s) = \frac{K_pK_v}{N}\,\frac{s\tau + 1}{s^2\tau}\,\frac{1 - e^{-sT}}{s} \qquad (6)$$

Since this exponential term can complicate the analysis, z transforms are used to vastly simplify things. (This form can be used for computer programs. See Appendix A for a discussion, and Appendices C and D for applications).

Rearranging, the open-loop transfer function,

$$G(s)H(s) = \frac{K}{\tau}\,(1 - e^{-sT})\left(\frac{1}{s^3} + \frac{\tau}{s^2}\right) \qquad (7)$$

Substituting the following transformations,

$$1 - e^{-sT} \longleftrightarrow \frac{z-1}{z}, \quad \frac{1}{s^3} \longleftrightarrow \frac{T^2}{2}\,\frac{z\,(z+1)}{(z-1)^3}, \text{ and}$$

$$\frac{1}{s^2} \longleftrightarrow T\,\frac{z}{(z-1)^2},$$

the new open-loop transfer function is therefore:

$$G(z)H(z) = \frac{KT}{\tau}\,\frac{\frac{T}{2}(z+1) + \tau(z-1)}{(z-1)^2} \qquad (8)$$

(which is in agreement with eq. 5 in Reference 2 and eq. 30 in Reference 10)

Defining the characteristic equation as $1 + G(z)H(z)$ leads to:

$1 + G(z)H(z) =$

$$\frac{z^2 + \left[\frac{KT}{\tau}\left[\frac{T}{2} + \tau\right] - 2\right] z + \left[K\,\frac{T}{\tau}\left[\frac{T}{2} - \tau\right] + 1\right]}{(z-1)^2} \qquad (9)$$

Stability

Using both the open-loop transfer function, and the characteristic equation, a study of the system's stability can be made. In the continuous-time case, for stability, roots of the characteristic equation had to lie in the left-hand complex plane. Due to the z-transformation, the left-half plane has been mapped to the interior of a unit circle. Therefore, a stable system, described by these equations in z, must have its roots within a unit circle.

Figure 5a depicts a typical root locus for a constant K with τ being variable. Figure 5b is a typical root locus for τ being held constant, and K the variable. In Figure 5b, the trajectory of the poles from K = 0 to the convergence point is circular, and whose center is at the open loop zero. Clearly, if the roots along the trajectory are to remain within the unit circle, the center must remain greater than 0. The center is determined by setting the numerator of the open loop transfer function to zero. Namely,

$$\frac{T}{2}(z + 1)\;\tau(z - 1) = 0 \qquad (10)$$

solving for z, we find that

$$z = \frac{2\tau - T}{2\tau + T} \qquad (11)$$

Clearly, for z to be > 0, it is necessary that:

$$\frac{\tau}{T} > \frac{1}{2} \qquad (12)$$

This determines the bounds for the damping of the loop to maintain stability.

To determine the bounds for the loop gain, K, observe the behavior of the root locus in Figure 5b. As K increases, a root will eventually leave the unit circle at z = −1. Substituting z = −1 into the characteristic equation, and solving for K, it can be shown that for stability,

$$KT < 2 \qquad (13)$$

To summarize, the continuous-time equations demonstrate unconditional stability with respect to K and τ, whereas the more precise discrete-time approach yields a conditionally stable system. The bandwidth of a practical loop cannot be increased without bound, nor can the damping be arbitrarily chosen.

Step Response

Since frequency-agile synthesizers are of interest, the response of the system to a frequency step at the input has to be considered. The output frequency of a loop is changed by either stepping the reference frequency, or by changing the divide-by-N number. Egan (12) has shown that both of these stimuli are analogous.

The error transfer function,

$$\frac{E(z)}{R(z)} = \frac{1}{1 + G(z)H(z)} \qquad (14)$$

becomes,

$$\frac{E(z)}{R(z)} = \frac{(z-1)^2}{z^2 + \left[K\,\frac{T}{\tau}\left[\frac{T}{2} + \tau\right] - 2\right] z + \left[K\,\frac{T}{\tau}\left[\frac{T}{2} - \tau\right] + 1\right]} \qquad (15)$$

Substituting the z-transform of a frequency step,

$$R(z) = \frac{\Delta\omega\ T}{N} \frac{z}{(z-1)^2} \tag{16}$$

into the above equation, yields:

$$E(z) = \frac{\Delta\omega\ T}{N}$$

$$\frac{z}{z^2 + \left[K\ \frac{T}{\tau}\left[\frac{T}{2} + \tau\right] - 2\right] z + \left[K\ \frac{T}{\tau}\left[\frac{T}{2} - \tau\right] + 1\right]} \tag{17}$$

Taking the inverse z-transform to get the time response,

$$e(nT) = \frac{\Delta\omega\ T}{N} \frac{a^n - b^n}{a - b} \tag{18}$$

where a and b are the roots of the characteristic equation, namely:

$$a = A + jB,\ b = C + jD. \tag{19}$$

Just as in the continuous-time analysis, the response may be classified into three different categories depending upon the roots of the characteristic equation.

Complex Conjugate Roots — Underdamped Response

Choosing τ such that the roots of the characteristic equation are complex, the response due to a frequency step is underdamped, being a dampened sinusoid in nature. Since, for complex conjugate roots, the real parts are equal and the imaginary parts are opposite in sign, the roots may be rewritten as follows:

$$a = A + jB,\ b = A - jB \tag{20}$$

Substituting back into (18), results in:

$$e(nT) = \frac{\Delta\omega\ T}{N} \frac{R^n}{B} \sin(n\theta) \tag{21}$$

$$\text{where} \quad R = \sqrt{A^2 + B^2}\ ,\ \theta = \arctan\left(\frac{B}{A}\right) \tag{22}$$

A typical response is shown in Figure 6a.

Real, Equal Roots: Critical Damping

Since critical damping yields the fastest settling time for a giv loop bandwidth, this is the most important case. The roots have equal real parts, and zero imaginary parts, namely:

$$a = b = A \tag{23}$$

Substituting back into (18) yields:

$$e(nT) = \frac{\Delta\omega\ T}{N} nA^{n-1} \tag{24}$$

A typical response is depicted in Figure 6B.

Real, Unequal Roots: Overdamped Response

Increasing the damping further, the response becomes more sluggish. The real parts of the roots are now unequal, with zero imaginary parts. The roots may be rewritten as:

$$a = A \text{ and } b = C \tag{25}$$

which yields:

$$e(nT) = \frac{\Delta\omega\ T}{N} \frac{A^n - C^n}{A - C} \tag{26}$$

Figure 6c shows a typical response.

Optimum Design

Since achieving critical damping is necessary to minimize settling time, an equation yielding the necessary τ for a given K will now be generated. Critical damping occurs when the roots of the characteristic equation just become real (point of convergence in the root locus of Figure 5b). Solving for the roots of the characteristic equation,

$$a,b = \frac{-\left[K\ \frac{T}{\tau}\left[\frac{T}{2} + \tau\right] - 2\right]}{2} + \sqrt{\left[\frac{K\ \frac{T}{\tau}\left[\frac{T}{2} + \tau\right] - 2}{2}\right]^2 - \left[K\ \frac{T}{\tau}\left[\frac{T}{2} - \tau\right] + 1\right]} \tag{27}$$

Clearly the roots become real and equal when the radicand (commonly known as the discriminant) is equal to 0. Setting the radicand equal to 0, and solving for τ,

$$\tau = \left[\frac{2}{K} - \frac{T}{2}\right] + \sqrt{\left[\frac{2}{K} - \frac{T}{2}\right]^2 - \left[\frac{T}{2}\right]^2} \tag{28}$$

Appendix B shows that for small bandwidth loops (relative to the reference frequency), the above equation can be approximated by:

$$\tau \approx \frac{4}{K} - T \tag{29}$$

This is quite similar to the continuous time equation except for the reference period term.

Figure 7 is a graph of the normalized loop filter time constant (τ/T) necessary for critical damping, versus the normalized loop gain ($KT/2\pi$), for both the continuous time system (5) and for the discrete-time system (28). Figure 8 shows the percent error expected if τ is chosen using the continuous-time equations, and if τ is chosen using the approximation (29). As can be seen, for a 10 percent loop bandwidth, the continuous-time equation is about 20 percent in error from the correct equation for a critical damping time constant. Whereas the approximation (29) is still good, yielding less than 1 percent error.

If the loop bandwidth were to be increased and the loop filter time constant set to give critical damping in accordance with (28), an absolute minimum in the settling time would eventually be reached. This results when the error response of (15) reverts to a mere delta function (shifted by one reference period). This occurs when the two non-unity coefficients in (15) are zero, namely:

$$\frac{KT}{\tau}\left[\frac{T}{2} + \tau\right] - 2 = 0 \quad \text{and} \quad \frac{KT}{\tau}\left[\frac{T}{2} + \tau\right] + 1 = 0 \tag{30}$$

Solving simultaneously results in:

$$\frac{\tau}{T} = 1.5, \quad \text{and} \quad KT = 1.5 \tag{31}$$

This then gives rise to:

$$E(z) = \frac{\Delta\omega\ T}{N} \frac{1}{z} \tag{32}$$

whose inverse z-transform is:

$$e(nT) = \frac{\Delta\omega\ T}{N} \delta(t - T) \tag{33}$$

This demonstrates that a type-2, second order system theoretically may achieve steady state phase settling in 2 reference periods.

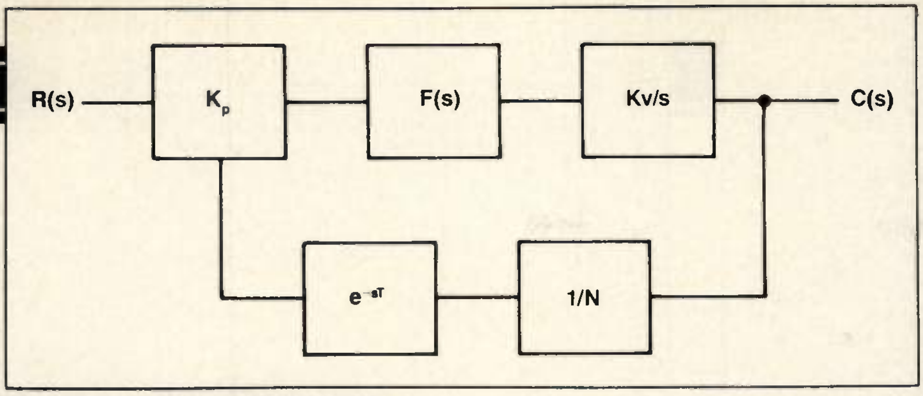

Figure 3. A time delay model.

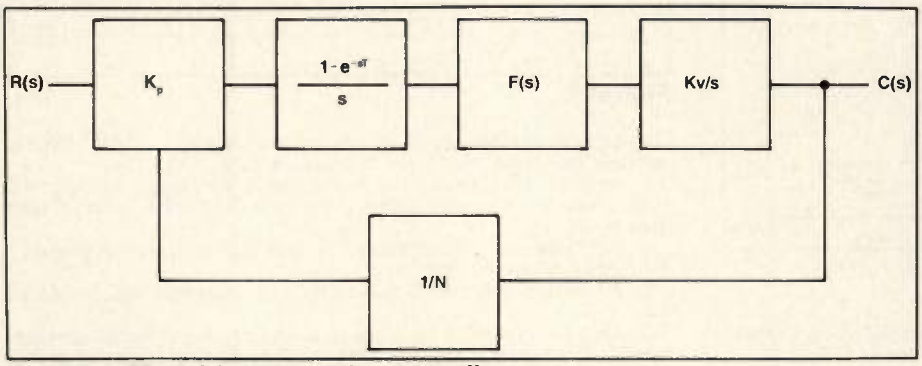

Figure 4. Model incorporating sampling.

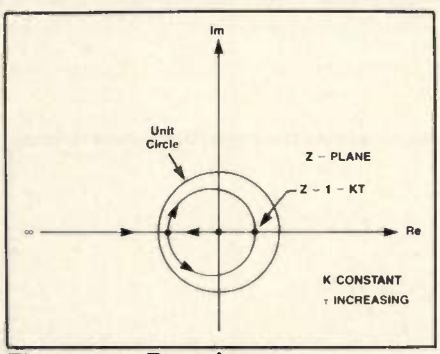

Figure 5a. Root locus.

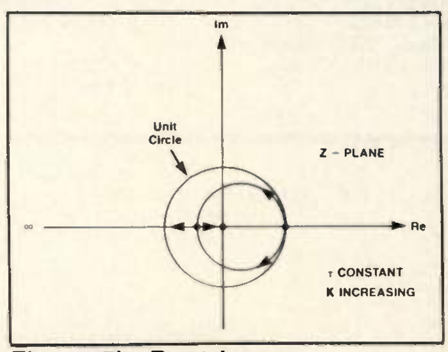

Figure 5b. Root locus.

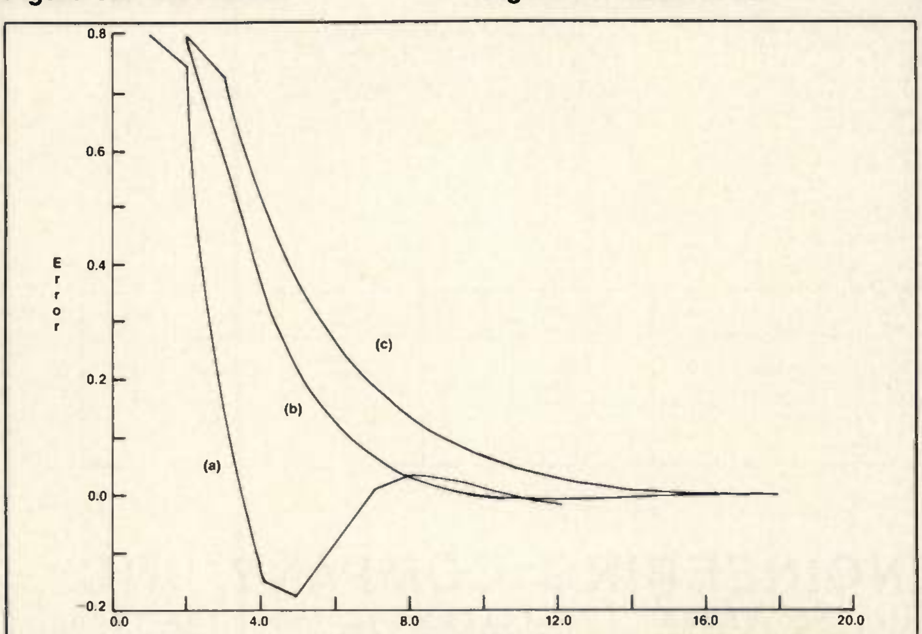

Figure 6. Typical step response.

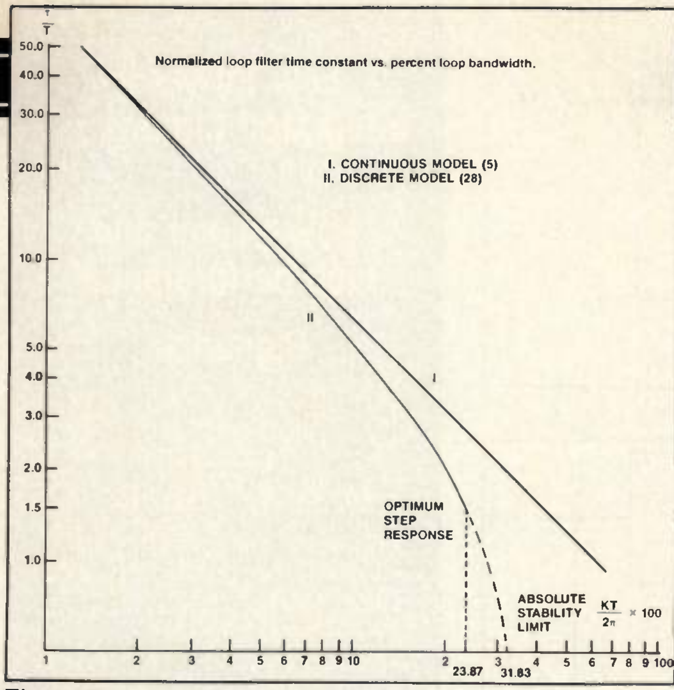

Figure 7.

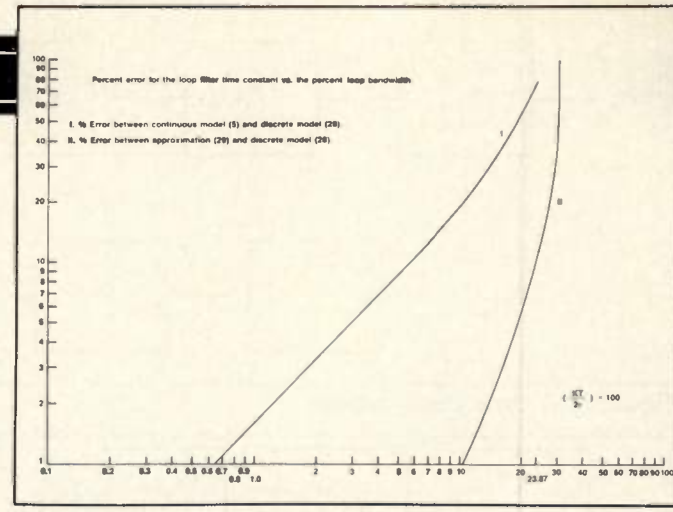

Figure 8.

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About the Author

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Appendix A: Narrowband Models for the Zero-Order Hold

Two narrowband (sT << 1) models for the zero-or-hold term,

$$\frac{1 - e^{-sT}}{s} \tag{A1}$$

will be developed. Before utilizing this term directly (as opposed to using z-transforms), two considerations must be addressed. First, the term must be dimensionless, and secondly, it must have a magnitude of one, at an angle of zero degrees, at DC. Analyzing the zero-order-hold term determines that it has dimensions of seconds, and a magnitude of T, at an angle of zero degrees, at DC. Clearly, dividing by T will render the term dimensionless, with a magnitude of one, at an angle of zero degrees, at DC. Therefore the term to study is:

$$\frac{1 - e^{-sT}}{sT} \tag{A2}$$

Substituting the first three terms of the well known expansion,

$$e^{-x} \approx 1 - x + \frac{x^2}{2} - \ldots \tag{A3}$$

into (A2) results in:

$$\frac{1 - e^{-sT}}{sT} \approx 1 - \frac{sT}{2} \,.. \tag{A4}$$

The first model results from using the expansion for e^{-x} again, namely:

$$1 - \frac{x}{2} \approx e^{-x/2}. \tag{A5}$$

This gives rise to the delay-like model for the zero-order-hold:

$$\frac{1 - e^{-sT}}{sT} \approx e^{-ST/2}. \tag{A6}$$

The second model is generated by using the approximation:

$$1 - x \approx \frac{1}{1 + x}, \text{ for } x << 1. \tag{A7}$$

Applying this approximation to (A4) results in the single-pole model for the zero-order-hold:

$$\frac{1 - e^{-sT}}{sT} \approx \frac{1}{1 + \frac{sT}{2}}. \tag{A8}$$

These two models, (A6) and (A8), may be used as desired to approximate the effect of the discrete-time nature of the loop when doing narrowband continuous-time analysis.

Appendix B: Narrowband Approximation for the Critical Damping Time Constant Equation

If the equation to determine the loop filter time constant that yields critical damping for a given loop gain, (28), is too intimidating, or if its accuracy is not necessary, a simple approximation can be made to significantly reduce it. Rewriting (28) here:

$$\tau = \left[\frac{2}{K} - \frac{T}{2}\right] + \sqrt{\left[\frac{2}{K} - \frac{T}{2}\right]^2 - \left[\frac{T}{2}\right]^2} \tag{B1}$$

Rearranging inside the radical yields,

$$\tau = \left[\frac{2}{K} - \frac{T}{2}\right] + \frac{2}{K}\sqrt{1 - \left[K\frac{T}{2}\right]} \tag{B2}$$

Now for small loop bandwidths, relative to the reference frequency, namely KT << 1, the approximation,

$$\sqrt{1 - x} \approx 1 - \frac{x}{2}, \text{ for } x << 1 \tag{B3}$$

is used to achieve the simple equation:

$$\tau \approx \frac{4}{K} - T \tag{B4}$$

Appendix C: Demonstration that K is Approximately Equal to the Loop Bandwidth

It will be shown that for a given loop gain, K, and with τ chosen for critical damping in accordance with (28), the loop bandwidth is approximately equal to K. The loop bandwidth is defined as the frequency at which the magnitude of the open loop transfer function (6) goes to 0 dB. Rewriting (6) here:

$$G(s)H(s) = K \frac{s\tau + 1}{s\tau} \frac{1 - e^{-sT}}{sT} \qquad (C1)$$

(The T in the denominator resulted from the discussion in Appendix A). Taking the magnitude of (C1) and setting it equal to 1 (0 dB) results in:

$$\frac{K}{\omega^3 T\tau} \sqrt{2\,[1 + (\omega\tau)^2]\,(1 - \cos(\omega\tau))} = 1 \qquad (C2)$$

Table 1 shows the results from solving for ω for a given K, with τ chosen in accordance with (28):

predicted percent loop BW 100 (KT)	actual percent loop BW 100 (ωT)	percent error
0.25	0.257	2.93
0.50	0.515	2.95
1.00	1.03	2.98
2.00	2.06	3.03
2.50	2.58	3.03
5.00	5.15	2.97
10.00	10.24	2.39
12.50	12.74	1.92
15.00	15.20	1.37
17.50	17.64	0.78
20.00	20.04	0.22

This demonstrates that the 0 dB crossover frequency may be approximated, to within a few percent, by K.

Appendix D: Maximize Phase Margin

When settling time is not a primary consideration, τ may be chosen such that the phase margin of the system is maximized for a given K. This is accomplished by taking the angle of the open loop transfer function, differentiating, setting it equal to zero, and solving for τ.

Rewriting the open loop transfer function (6), and incorporating the factor of T due to the discussion of Appendix A,

$$G(s)H(s) = K \frac{s\tau + 1}{s\tau} \frac{1 - e^{-sT}}{sT} \qquad \text{(D1)}$$

Substituting Euler's formula, $e^{jx} = \cos(x) + j\sin(x)$,

into (D1), and taking the angle yields:

$$\theta = \arctan(\omega\tau) + \arctan\left[\frac{\sin(\omega T)}{1 - \cos(\omega T)}\right] - 270° \qquad \text{(D2)}$$

Differentiating with respect to ω gives rise to:

$$\frac{d\theta}{d\omega} = \frac{\tau}{1 + (\omega\tau)^2} - \frac{T}{2} \qquad \text{(D3)}$$

Setting Equation D3 equal to zero, and solving for τ, notice that for a given K, maximum phase margin will occur when:

$$\frac{\tau}{T} = \frac{1}{(\omega T)^2}\left[1 + \sqrt{1 - (\omega T)^2}\right] \qquad \text{(D4)}$$

The admonishment to use caution when designing for maximum phase margin is given because the resulting loop time constant may be significantly removed from the critical damping value. Table D1 demonstrates this by comparing the time constants for critical damping (28), and for maximum phase margin (D4). As can be seen, at a percentage loop bandwidth of about 8.5 percent (KT = .53), the two values coincide.

		τ/T		
% loop BW	KT	Critical eq. (5)	Damping eq. (28)	max pm eq. (D4)
1.0	0.06	63.66	62.66	506.11
1.5	0.09	42.44	41.44	224.66
2.0	0.13	31.83	30.82	126.15
2.5	0.16	25.46	24.45	80.55
3.0	0.19	21.22	20.21	55.79
3.5	0.22	18.19	17.17	40.85
4.0	0.25	15.92	14.90	31.15
4.5	0.28	14.15	13.13	24.51
5.0	0.31	12.73	11.71	19.75
5.5	0.35	11.57	10.55	16.23
6.0	0.38	10.61	9.58	13.55
6.5	0.41	9.79	8.77	11.47
7.0	0.44	9.09	8.06	9.81
7.5	0.47	8.49	7.45	8.47
8.0	0.50	7.96	6.92	7.38
8.5	0.53	7.49	6.45	6.47
9.0	0.57	7.07	6.03	5.71
9.5	0.60	6.70	5.66	5.06
10.0	0.63	6.37	5.32	4.50
10.5	0.66	6.06	5.01	4.02
11.0	0.69	5.79	4.73	3.61
11.5	0.72	5.54	4.48	3.24
12.0	0.75	5.31	4.25	2.91
12.5	0.79	5.09	4.03	2.62
13.0	0.82	4.90	3.83	2.36
13.5	0.85	4.72	3.65	2.13
14.0	0.88	4.55	3.48	1.91
14.5	0.91	4.39	3.32	1.70
15.0	0.94	4.24	3.17	1.50
15.5	0.97	4.11	3.02	1.29
15.9	1.00	4.00	2.91	1.00

Table D1.

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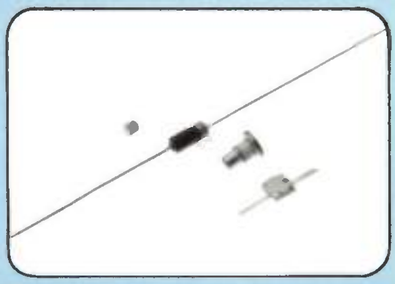

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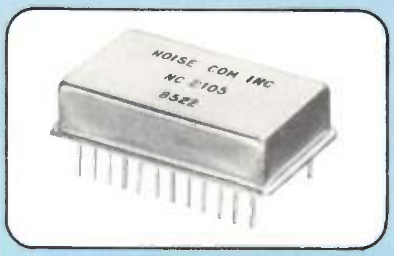

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NC 2103	up to 500 kHz
NC 2104	up to 1 MHz
NC 2105	up to 10 MHz
NC 2106	up to 20 MHz
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CAE Basics for Phase Locked Loops

Understanding Models and Assumptions in PLL Design Software

By Corinn Fahrenkrug
Leybold Inficon

The primary function of a phase locked loop is to produce an output signal which has both zero frequency error and zero phase error from its input signal. Phase locked loops (PLLs) are also useful in applications where coherence is required. The tracking afforded by a PLL allows the generation of a signal synchronized to a reference. Any application which requires the extraction of a signal from a noisy environment or which requires the free running of the signal during periods of dropout benefits from the use of a phase locked loop.

The design of a PLL is often a tedious task of trial and error. It is always a compromise between fast low-error tracking operation and noise response. Software modeling on PLLs is beneficial because it allows a designer to observe the results and potential problems in the design before actually building the system. In order to use or write a software package effectively it is imperative that the designer have a complete understanding of the assumptions used in the model and their potential effects on the calculated values. The designer needs to prioritize the performance information and be aware of the software limitations in generating these performance measures.

The measures shown below are just a few of the parameters that should be included in a software package. Additional or modified performance measures may be appropriate for certain applications.

I. Tracking and Acquisition Performance
- a. Capture range
- b. Hold range
- c. Pull-in range
- d. Pullout range
- e. Lock-up time
- f. Pull-in time
- g. Loop filter bandwidth

II. Stability Performance
- a. Natural frequency
- b. Damping ratio
- c. Phase margin
- d. System bandwidth

III. Noise Performance
- a. Noise bandwidth
- b. Peak jitter magnitude
- c. Peak jitter frequency
- d. Jitter bandwidth

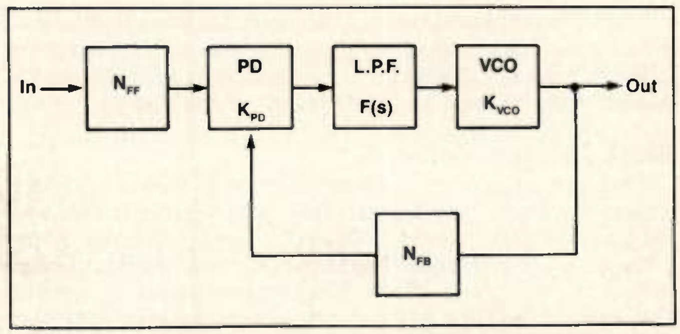


Figure 1. Block diagram for simplified phase locked loops.

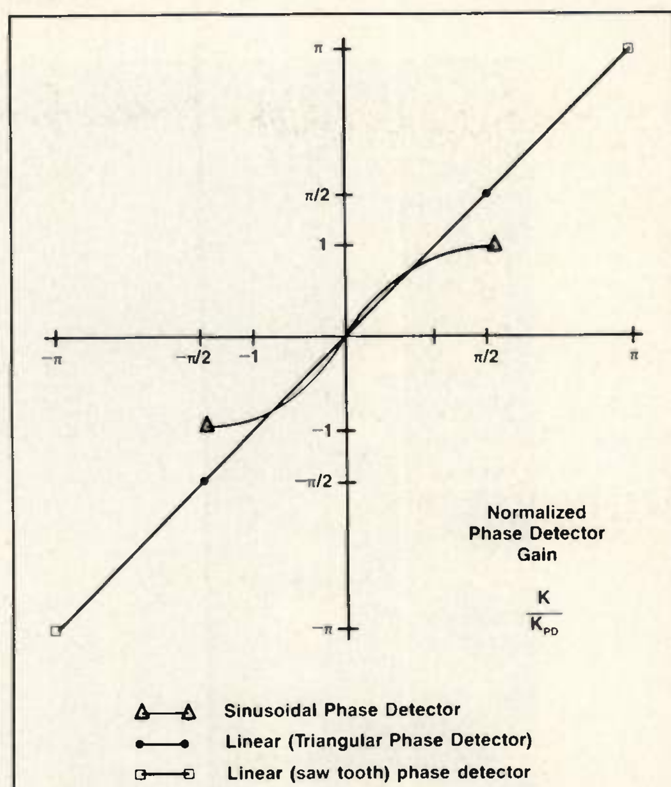


Figure 2. Phase detector gain characteristic.

Software Packages

In many ways the analysis of PLL's is straight forward. Discrepancies between theoretical predictions and actual operation are the result of the presence of noise, linearization errors, or neglected poles. For the simplified software model, these differences cannot be corrected. The purpose of a simplified software model is to be sufficiently general such that it allows analysis of PLL systems used in a variety of applications. This differs from another possible approach which would be to provide a more detailed analysis aimed at PLL systems used for a specific application.

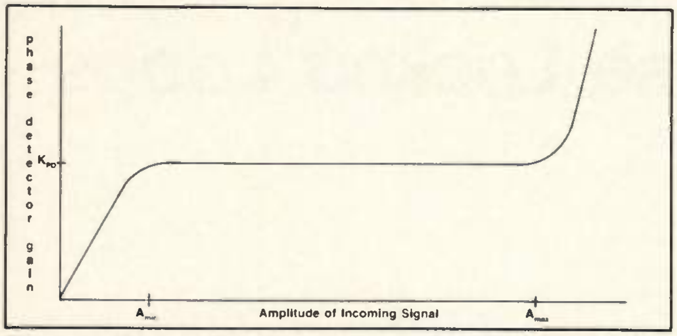


Figure 3. Phase detector gain versus signal amplitude.

The software package should be complete enough to relieve the designer from making numerous calculations involved in the initial PLL design as well as the subsequent recalculations involved in the revision and optimization of the design.

Block Diagram Model

The block diagram model gives the model of systems for which a typical software package is applicable. A generalized block diagram for a PLL is given in Figure 1. To implement this model in the software package, the user would be prompted for information regarding each block. The required inputs include the feed-forward (N_{FF}) and feedback (N_{FB}) counters (each defaulting to a value of one), the voltage controlled oscillator gain (K_{VCO}Hz/V), the phase detector gain (K_{PD} V/radian), and the filter type (F(s)) selected from four choices and the associated resistance and capacitance values.

The recent trend has been towards software modeling of components rather than the overall system. While it is still important to keep a good understanding of PLL operation, the knowledge of PLL components is a new key to selecting an effective software package.

The modeling of each component plays a major role in determining the systems for which the software package can be used. The choice of models for the phase detector, VCO and filter has a significant effect on the accuracy of the predicted performance measures. While certain applications would require the use of very specialized components in the general model, the choices for the modeling of the particular components can be made to minimize the inputs required for calculations, maximize the number of systems which could be analyzed by the software package, and achieve a reasonable degree of accuracy in the calculations.

The Phase Detector

Since the classical PLL theory for analog PLLs assumes the use of sinusoidal phase detectors, it is the type selected as the model in the software. If a linear phase detector is used, the maximum gain of the phase detector will be increased by a factor of $\pi/2$ for a triangular phase detector, and π for a sawtooth phase detector over that of the assumed sinusoidal phase detector. The DC component of the phase detector output voltage as a function of incoming phase error is shown in Figure 2.

Some digital PLLs derive performance measures from this same analog theory. In cases where the software is used to analyze a digital PLL, the calculated values will be applicable with the exception of the evaluation of the hold range. A value for the hold range can be determined by the user by multiplying the software generated value by $\pi/2$ (or π) as described above.

For the sinusoidal phase detector the general expression for output is:

$$V_{PD} = K_{PD}\,\mathrm{Sin}(\theta_{err}) + \text{AC component} \quad (1)$$

where K_{PD} is the gain of the phase detector in (V/radian), V_{PD} is the output of the phase detector and θ_{err} is the phase error between the input signal and the PLL output signal. The AC component is the product of the input (reference) signal and the PLL output signal. It will have a frequency of approximately twice that of the reference signal. The phase error signal will be the baseband (DC component) of the phase detector output. For many of the equations used in calculating acquisition measures, the $\sin\theta_{err}$ term in equation (1) is simplified to just θ_{err}. This assumption is valid as long as the phase error is close to zero, such as in an operating lock loop.

In addition to the output of the phase detector changing with respect to phase error, it is noted that phase detector output is also dependent on the incoming signal amplitude for input amplitudes below some minimum input and above some maximum input. An illustration of this is shown in Figure 3. In many software packages, it is assumed that the incoming signal always falls within the range required to produce a phase detector gain independent of the incoming signal amplitude. This is necessary to insure that amplitude modulation is not interpreted by the phase detector as phase modulation. Many practical circuits make use of an amplitude limiter to keep the amplitude of the signal within the linear range of the phase detector.

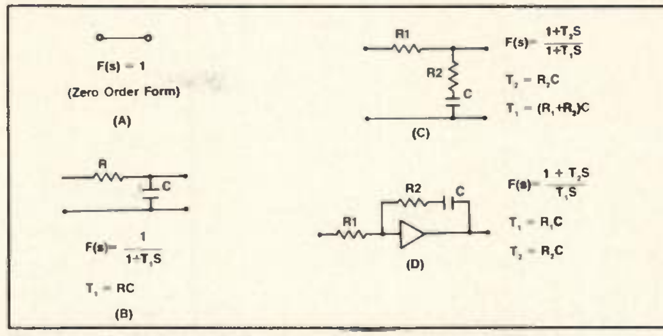
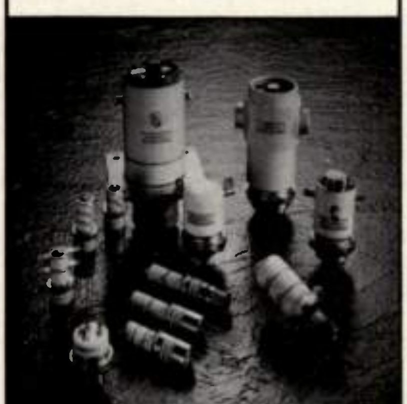


Figure 4. Typical first-order, low-pass filter.

The Loop Filter

The phase detector error is passed through a loop filter to remove the AC component of the error while reducing the effect of jitter due to high frequency noise. In all cases the loop filter is a low pass filter which is usually of the first order. Second order filters are sometimes beneficial because they provide a zero steady state phase error. Note that all operating PLLs have zero steady state frequency error. The filters for such applications may be either passive or active. Four possible loop filters and their transfer functions are shown in Figures 4a-4d. These model should be incorporated in all PLL packages.



Model Number (2)	Impedance Ohms (Power W)	Frequency Range	BNC	TNC	N	SMA	UHF	PC
			UNIT PRICE (4) EFFECTIVE 9-15-86					
Fixed Attenuators, 1 to 20 dB								
AT 50(3)	50 (.5W)	DC 1.5GHz	14.00	20.00	20.00	18.00	–	–
AT-51	50 (.5W)	DC 1.5GHz	11.00	18.00	15.00	14.00	–	12.00
AT-52	50 (1W)	DC-1.5GHz	14.50	20.50	20.50	19.50	–	–
AT-53	50 (.25W)	DC 3.0GHz	14.00	17.00	–	15.00	–	–
AT-54	50 (.25W)	DC-4.2GHz	–	–	–	18.00	–	–
AT-55	50 (.25W)	DC 4.2GHz	–	–	–	14.40 (10 Pc)	–	–
AT 75 or AT 90	75 or 93 (.5W)	DC 1.5GHz (750MHz)	11.50	20.00	20.00	18.00	–	–
Detector, Mixer, Zero Bias Schottky								
CD-51, 75	50, 75	01-4.2GHz	54.00	–	–	54.00	–	–
DM-51	50	01-4.2GHz	–	–	–	64.00	–	–
Resistive Impedance Transformers, Minimum Loss Pads								
RT 50/75	50 to 75	DC 1.5GHz	10.50	19.50	19.50	17.50	–	–
RT-50/93	50 to 93	DC-1.0GHz	13.00	19.50	19.50	17.50	–	–
Terminations								
CT-50 (3)	50 (.5W)	DC 4.2GHz	11.50	15.00	15.00	17.50	–	–
CT-51	50 (.5W)	DC 4.2GHz	9.50	12.00	10.50	9.50	–	–
CT-52	50 (1W)	DC-2.5GHz	10.50	15.00	15.00	13.00	15.50	–
CT-53/M	50 (.5W)	DC 4.2GHz	5.60 (10 Pc)	–	–	5.60 (10 Pc)	–	–
CT 54	50 (2W)	DC 2.0GHz	14.00	15.00	15.00	17.50	–	–
CT-75	75 (.25W)	DC 2.5GHz	10.50	15.00	15.00	13.00	15.50	–
CT-93	93 (.25W)	DC 2.5GHz	13.00	15.00	–	15.00	15.50	–
Mismatched Terminations 1.05:1 to 3:1, Open Circuit, Short Circuit								
MT 51	50	DC-3.0GHz	45.50	45.50	45.50	45.50	–	–
MT 75	75	DC 1.0GHz	–	–	45.50	–	–	–
Feed thru Terminations, shunt resistor								
FT 50	50	DC-1.0GHz	10.50	19.50	19.50	17.50	–	–
FT-75	75	DC-500MHz	10.50	19.50	19.50	17.50	–	–
FT 90	93	DC 150MHz	13.00	19.50	19.50	17.50	–	–
Directional Coupler, 30 dB								
DC 500	50	250-500MHz	60.00	–	64.00	–	–	–
Resistive Decoupler, series resistor or Capacitive Coupler, series capacitor								
RD or CC-1000	1000 (1000PF)	DC 1.5GHz	12.00	18.00	18.00	17.00	–	–
Adapters								
CA-50 (N to SMA)	50	DC-4.2GHz	13.00	13.00	13.00	13.00	–	–
Inductive Decouplers, series inductor								
LD-R15	0.17uH	DC 500MHz	12.00	18.00	18.00	17.00	–	–
LD-6R8	6.8uH	DC-55MHz	12.00	18.00	18.00	17.00	–	–
Fixed Attenuator Sets, 3, 6, 10, and 20 dB, in plastic case								
AT 50-SET (3)	50	DC 1.5GHz	60.00	84.00	84.00	78.00	–	–
AT-51 SET	50	DC 1.5GHz	48.00	64.00	64.00	60.00	–	–
Reactive Multicouplers, 2 and 4 output ports								
TC-125-2	50	1.5-125MHz	64.00	–	67.00	67.00	–	–
TC-125-4	50	1.5-125MHz	67.00	–	81.50	81.50	–	–
Resistive Power Dividers 3, 4 and 9 ports								
RC-3-50	50	DC-2.0GHz	64.00	64.00	–	64.00	–	–
RC-4-50	50	DC 500MHz	64.00	64.00	–	64.00	–	–
RC 8-50	50	DC 500MHz	–	–	–	84.50	–	–
RC 3-75, 4-75	75	DC-500MHz	64.00	64.00	–	64.00	–	–
Double Balanced Mixers								
DBM-1000	50	5-1000MHz	61.00	–	71.00	61.00	–	34.00
DBM-500PC	50	2-500MHz	–	–	–	–	–	34.00
RF Fuse, 1/8 Amp and 1/16 Amp								
FL-50	50	DC-1.5GHz	12.00	18.00	45.50	17.00	–	–
FL-75	75	DC-1.5GHz	12.00	18.00	–	17.00	–	–

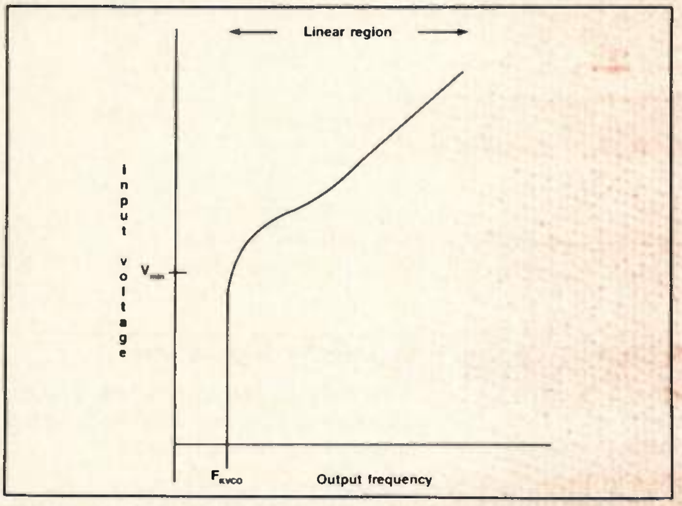


Figure 5. Possible VCO gain characteristic.

A more sophisticated software package might include a second order filter. However, if a second order filter is used, the corresponding PLL is third order. In the case of a third order PLL, iterative searches are required to generate performance and stability measures. The software work required for analysis of a third order PLL is significantly more involved than that for a second order loop.

The Voltage Controlled Oscillator

The filtered phase error signal is the input of the oscillator. Whether a voltage controlled oscillator or a current controlled oscillator is used, the output can be described by:

$$O_{VCO} = K_{VCO}\, V_{PD} + \omega_C \qquad (2)$$

where ω_C is the center frequency of the oscillator and K_{VCO} is the gain constant of the voltage controlled oscillator or current controlled oscillator in radians/(s*volt) or radians/(s*Amp).

The choice of using a voltage controlled oscillator is particularly significant. The basic model of PLL assumes the VCO contributes no poles of any significance to the overall modeling of the system. This assumption is often invalid when the VCO in the PLL is a crystal oscillator (VCXO). The VCXO will often have a low frequency pole which can cause stability problems in a PLL. Further, neglecting this pole in software can generate inaccurate stability and performance measures. This problem can be alleviated by allowing the user to specify an additional pole to be used in the stability calculations.

In addition to the assumption that the VCO introduces no additional poles, assumption that the VCO exhibits a linear relationship between the amplitude of its incoming voltage and the frequency of its outcoming signal is valid. While this linearity is not achieved for all VCOs it is achieved for YIG tuned oscillators and most varactor tuned oscillators. For other oscillators this assumption of linearity is achieved to a fair degree in the normal region of operation. Figure 5 shows the characteristic for a typical VCO specified by Motorola. It is apparent that this characteristic is not completely linear, but for the purpose of the software model it would be assumed to operate in the approximately linear region.

Feedback and Feedforward Multipliers

One final consideration is that of feedback multipliers, and less commonly, feedforward multipliers as shown in Figure 1. The feedback counter multiplies the frequency of the VCO output signal by N_{FB} (where N_{FB} is the feedback multiplier). Therefore the VCO gain, K_{VCO}, must be replaced by $K_{VCO}N_{FB}$ in any equation derived for performance measures containing K_{VCO}. Feed forward multipliers multiply the frequency of the incoming signal by N_{FF}. Therefore, any performance measure given relative to the incoming signal (ex. pull-in range, capture range, etc.) should be divided by the multiplier to give the measure in terms of the frequency of the true incoming signal. Both the forward and the feedback multipliers are potential inputs for a software package.

With these basic constraints on the block elements, the basic closed loop gain equation is:

$$H(s) = K_{PD}\, K_{VCO}/((s/F(s)) + K_{PD}K_{VCO}N_{FB}) \qquad (3)$$

which is derived from basic control theory where $H(s) = A(s)/(1 + A(s)B(s))$ and $A(s)$ is the forward gain, and $B(s)$ is the feedback gain (for multiplier, N_{FB}).

Conclusion

Software modeling of a PLL is beneficial because it allows a designer to observe the results and potential problems in the design before actually building the system. When developing, purchasing or using software, a designer must be aware of the requirements and limitations of a PLL software model. While the software package is no guarantee of the performance in the actual system, a softweare model is a valuable design aid since it saves much of the tedious reiterative hand calculations associated with PLL design.

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About the Author

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Summary of Precalculated Performance Measures

1. Tracking and Acquisition Measures
a. Hold Range

$$F_{HR} = \frac{K_{PD}\,K_{VCO}\,N_{FB}\,F(O)}{2\,\pi\,N_{FF}} \tag{4}$$

b. Capture Range

$$F_{CAP} = \frac{K_{PD}\,K_{VCO}\,|F(\omega_{cap})|}{2\,\pi} \tag{5}$$

where $|F(\omega_{cap})|$ is the magnitude of the transfer function of the loop filter at the capture range boundary, and ω_{cap} is the value of the capture range boundary in radians/second. If we assume that the capture range will be large compared to the corner frequencies of the loop filter, the magnitude of the filter response is approximately that for high frequencies.

For the four filter models considered, the magnitude of the transfer functions at high frequencies are given by:

$$F1(\omega_{high}) = 1 \qquad F2(\omega_{high}) = \frac{1}{T1}$$
$$F3(\omega_{high}) = \frac{T2}{T1} \qquad F4(\omega_{high}) = \frac{T2}{T1} \tag{6}$$

c. Pull-in range

$$F_{PL1} = \frac{1}{\pi\,N_{FF}}\,[\zeta\,\omega_n\,K_{PD}\,K_{VCO}\,N_{FB} - (\omega_n^2/2)]^{1/2} \tag{7}$$

where ζ and ω_n are the damping ratio and the natural frequency of the system.

d. Pullout range

$$F_{PLO} = \frac{1}{2\,\pi}\,1.8\,\omega_n\,(1 + \zeta) \tag{8}$$

e. Pull-in time

$$T_p = \frac{(\Delta\omega)^2}{2\,\omega_n^3} \tag{9}$$

where $(\Delta\omega)$ is the average of the capture and pull-in ranges. This expression does not take into account the phenomenon of hangup which sometimes occurs with a system operating near the capture range boundary. At this boundary, the system may appear to be caught and delay its acquisition of lock. This is the result of the relatively low slope of the phase detector gain at this boundary. Clearly, this is more of a problem for sinusoidal phase detectors than for linear phase detectors. The phenomenon of hangup is discussed in reference 7 (Lindsey, 1986).

f. Lock-up time

$$T_L = \frac{1}{\omega_n} \tag{10}$$

g. Loop filter bandwidth
Filter 2

$$B_F = \frac{1}{2\,\pi\,T1} \tag{11A}$$

Filter 3.

$$B_F = \frac{1}{2\,\pi}\left[\frac{1}{T1^2 - 2\,T2^2}\right]^{1/2} \tag{11B}$$

2. Stability Analysis
a. Natural frequency and damping ratio
Passive Loop Filters 2 and 3
(note that for filter 2, T2 =0)

$$\omega_n = \left[\frac{K_{PD}\,K_{VCO}\,N_{FB}}{T1 + T2}\right]^{1/2}$$

$$\zeta = \frac{1}{2}\,\omega_n\left[\frac{1}{K_{PD}\,K_{VCO}\,N_{FB}} + T2\right]$$

Active Filter 4.

$$\omega_n = \left[\frac{K_{PD}\,K_{VCO}\,N_{FB}}{T1}\right]^{1/2}$$

$$\zeta = \frac{T2}{2}\,\omega_n \tag{12}$$

b. System bandwidth

$$B_{PLL} = \frac{1}{2\pi}\,\omega_U \tag{13}$$

where ω_U is the unity frequency in radians/s calculated in the phase margin section.

c. Phase margin

$[K = K_{PD}\,K_{VCO}\,N_{FB}]$

Filter 1.

$\omega_u = K$
PM = 90°

Filter 2.

$$\omega_u = \frac{1}{\sqrt{2}\,T1}\left[\sqrt{1+4\,(T1\;k)^2}-1\right]^{1/2}$$

PM = 90° − arctan (ω_u T1)

Filter 3.

$$\omega_u = \frac{1}{\sqrt{2}\,T1}\left[T2^2\,K^2 - 1 + \sqrt{(T2^2\,K^2-1)^2 + 4\,(T1\;K)^2}\right]^{1/2}$$

PM 90° − arctan (ω_u T1) + arctan (ω_u T2)

Filter 4.

$$\omega_u = \frac{1}{\sqrt{2}\,T1}\left[T2^2\,K^2 + \sqrt{(T2^2\,K^2)^4 + 4\,(T1\;K)^2}\right]^{1/2}$$

PM = arctan (ω_u T2)

(14)

3. Noise Performance
a. Noise bandwidth

$$N_B \int_0^{\infty} |H(j\omega)|^2 \, d\omega$$

(15)

Fortunately, this expression has been evaluated for the model corresponding to equation (14) including the four possible filter models.

$$N_B = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right]$$

Jitter Information

$K = K_{PD}\,K_{VCO}\,N_{FB}$

Filter 1.

$\omega_{jp} = O$

$J_p = O$

$B_J = K$

Filter 2.

$\omega_{jp} = \omega_n\,(1 - 2\,\zeta^2)^{1/2}$

$$J_p = \frac{1}{2\,\zeta\,\sqrt{1-\zeta^2}}$$

$B_J = \omega_n\,(b + \sqrt{b^2+1})^{1/2}$

$b = (2\,\zeta^2 + 1)$

Filter 3.

ω_{jp} = must be found by iteration

$$J_p = \left[\frac{1 + \left[\dfrac{2\,\zeta\,\omega_p}{\omega_n} - \dfrac{\omega_p}{K}\right]^2}{1 - \left(\dfrac{\omega_p}{\omega_n}\right)^2 + 4\zeta\left(\dfrac{\omega_p}{\omega_n}\right)^2}\right]^{1/2}$$

$B_J = \omega_n\,(b + \sqrt{b^2+1})^{1/2}$

$$b = (2\,\zeta^2 + 1) - \frac{\omega_n}{K}\,(4\zeta - \omega_n)$$

Filter 4.

$$\omega_{jp} = \frac{\omega_n}{2\zeta}\left[\left(\sqrt{1+8\zeta^2}\right) - 1\right]^{1/2}$$

$J_p = (4\zeta)\,\left[(4\zeta - 1) - 3 + 2\sqrt{1 + 8\,\zeta^2}\right]^{-1/2}$

$B_J = \omega_n\,(b + \sqrt{b^2+1})^{1/2}$

$b = (2\,\zeta^2 + 1)$

A(s) = feedforward loop gain
B(s) = feedback loop gain
B_J = jitter bandwidth, Hz
B_L = loop filter 3 dB bandwidth, or unity frequency, Hz
B_{PLL} = PLL system bandwidth, Hz
f = frequency, Hz
F(s) = filter transfer function
F_{CAP} = capture range, Hz
F_{HR} = hold range, Hz
F_P = additional pole entered by user, Hz
F_{PLI} = pull-in range, Hz
F_{PLO} = pullout range, Hz
H(s) = transfer function, closed loop gain
J_p = peak jitter magnitude
K_{PD} = phase detector gain, volts per radian
K_V = voltage controlled oscillator gain, Hz per volt
K_{VCO} = voltage controlled oscillator gain, radians per second per volt ($2\,\pi K_V$)
N_B = noise bandwidth, Hz
N_{FB} = feedback multiplier
N_{FF} = feedforward multiplier
O_{VCO} = output of VCO, radians per second
OLG(insert omega)= transfer function, open loop gain
PM = phase margin, degrees
S or s = Laplace variable, ($s=j\omega$)
T1, T2 = loop filter time constants, seconds
T_L = lock up time, seconds
T_p = pull-in time, seconds
V_{pd} = output of phase detector, volts
ω = frequency, radians per second
ω_C= center frequency of VCO, radians per second
ω_n= natural frequency, radians per second
ω_{jp}= peak jitter frequency, radians per second
ω_u= unity frequency, radians per second
τ_{err}= phase error, radians
ζ = damping ratio

Appendix A: Table of Variables and Constants

A Proximity Warning System for Light Aircraft

By H. Paul Shuch
Microcomm

Our sky appears without limit. In fact, if each of the quarter of a million aircraft in the United States was airborne at the same instant, at the same altitude, over the state of Nevada, each would still have over a square mile of airspace to itself (1). At any given moment, fewer than 2 percent of these aircraft are in flight over all the U.S. (2), yet about 30 times a year, two or more aircraft find themselves occupying the same airspace at the same time. Roughly half of the ensuing midair encounters result in fatalities.

The design presented here, which uses simple RF and audio circuitry, seeks to reduce the risk of aircraft midair collision by providing pilots of light aircraft with stereo CW Doppler radar "ears," extending their senses to detect the position and relative velocity of potentially conflicting air traffic.

In simplest terms, the system has two low power Doppler radar units looking at the forward left and right quadrants of the sky near the aircraft. The outputs of the radars are audio frequency tones with a pitch proportional to the difference in speed between the user's aircraft and the radar target. The pilot wears stereo headphones with the corresponding radar outputs presented to his left and right ears. Using this method, the position of the source can be determined just like familiar stereophonic sound, with the pitch indicating the closing rate.

Background on Collision Avoidance

Current collision avoidance technology, using ground-based radar and ground-bound controllers, requires constant radio communication among participating aircraft and air traffic controllers. Since the early 1960s, development has been under way on a variety of alternative systems which are independent of ground support or control. These have included a receiver to indicate the presence of transponder-equipped aircraft in the vicinity (the Genave Proximity Warning Indicator), aircraft-to-aircraft information transfer using transponders and a low power laser replacement for the rotating beacon.

In addition, numerous proposals have been made which involve ground-based radar and controller participation through real-time or intermittent burst data communications. All of these options involve significant costs and integration into existing systems. The proliferation of home satellite receivers has driven down the cost of space communications, so a number of satellite-based navigation systems have also been proposed, involving the same cost and complexity as other systems.

Doppler radar systems do not suffer from the cost and complexity difficulties of scanning radar, or large data networks. Low cost Doppler systems are in use in security applications and automotive collision avoidance systems. They certainly bear consideration for airborne use.

The BiDCAS Concept

Current technology provides us with a wide variety of effective methods to determine the factors necessary for collision avoidance: target distance, bearing, direction of motion and relative velocity. Systems are already developed using CRT

Waveguide Inside Diameter		5.00 In. (12.7 cm)
OPERATING FREQUENCY		1749 MHz
WAVELENGTH:	Free-Space	6.75 In. (17.2 cm)
	Cutoff (TE11)	8.53 In. (21.7 cm)
	Cutoff (TM01)	6.53 In. (16.6 cm)
	Waveguide	11.05 In. (28.1 cm)

Zo = (Ohms) = 617; VSWR = 1.64 Ref. freespace

MONOPOLE:	Diameter	14 In. (.3 cm)
	Length	1.35 In. (3.4 cm)
	Location	2.76 In. (7.0 cm)

FEED GAIN	dBi	dBd	ANGLE:	3 dB	10 dB
max. avail.	7.3	5.1	e field	40	71 Deg
refl. loss	–.3	–.3	h field	68	122 Deg
effective	7.1	4.9	average	54	97 Deg

Table 1. Analysis of circular waveguide feedhorn.

OPERATING FREQUENCY		=	1749	MHz			
	WAVELENGTH	=	6.8	In.	=	17.2	cm
ANTENNA:	Diameter	=	5	In.	=	12.7	cm
	Efficiency	=	65	%	=	–1.87	dB
	Gain	=	3.5		=	5.5	dBi
	Beamwidth	=	1.35	Rad	=	77.4	Deg
	E.I.R.P.	=	–7.5	dBW	=	22.5	dBm
PATH:	Distance	=	1	Mi.	=	1.6	km
	Attenuation	=				101.4	dB
TARGET:	Diameter	=	2	m	=	200	cm
	Gain	=	1341.833		=	31.3	dBi
	Reflectivity	=	50	%	=	–3.0	dB

TRANSMIT	Power	=	.05	W	=	17.0	dBm
POWER TO TARGET:							
	Isotropic	=	–109.0	dBW	=	–79.0	dBm
	Incident	=	–77.7	dBW	=	–47.7	dBm
	Reflected	=	–80.7	dBW	=	–50.7	dBm
TOTAL PATH LOSS		=				174.6	dB
RECOVERED SIGNAL:							
	At Antenna	=	–182.1	dBW	=	–152.1	dBm
	At Receiver	=	–176.7	dBW	=	–146.7	dBm
RECEIVER:	Bandwidth	=	.1	kHz	=	20.0	dB/Hz
	Noise Factor	=	5.00		=	7.0	dB
	Threshold	=	–177.0	dBW	=	–147.0	dBm
SIGNAL-TO-NOISE RATIO:						.3	dB

Table 2. BiDCAS link analysis.

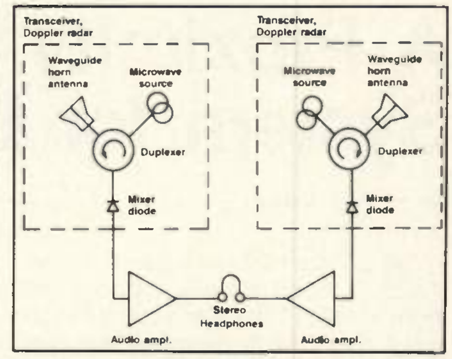

Figure 1. BidCAS system simplified block diagram.

displays, projected "heads up" displays and other visual means. The primary objection to all visual displays is that they discourage constant and thorough visual traffic scan. Verbal information transfer seems far more compatible with the "see-and-avoid" concept, but it is also limited by timeliness and accuracy of interpretation. The author wonders how many times crew members have responded to a call of "traffic at your one o'clock position, three miles" by looking at *three o'clock* and *one* mile.

The weak link in any collision avoidance system is the unambiguous communication of traffic information to the pilot, in a means compatible with performance of his cockpit duties and the continuous visual traffic scan essential to small aircraft flight. Thus, collision avoidance becomes essentially a user interface problem. This is what is addressed by the BiDCAS design.

Studies by the author have shown that binaural hearing enables the position, relative distance and closing velocity of nearby traffic to be communicated without distracting the pilot from his normal duties. Binaural hearing uses relative

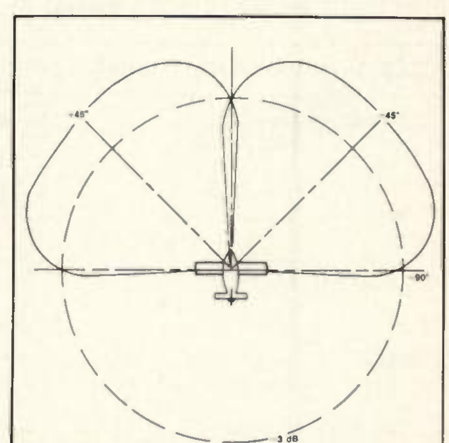

Figure 2. Preferred radiation pattern.

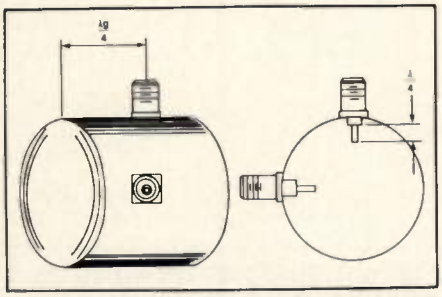

Figure 3. Dual-polarized cylindrical waveguide antenna feed. For circular polarization, the two monopoles are fed in phase quadrature.

amplitude, phase and time delay information between two ears to determine the position of a source. Like stereo recordings, binaural audio has a perceived space with each signal at a different location, enhancing the ability to concentrate on a particular source, even when it is below the noise level.

In the BiDCAS system, a stereo headset enables the user to "hear" the traffic: the position is indicated by the relative strength of the two channels, the amplitude of the signal conveys distance information, and the frequency or pitch communicates the closing rate or relative velocity. The same headset can also be used for radio communications and intercrew conversation through an intercom interface.

In keeping with a general belief expressed by pilots that an effective collision-avoidance alert system must be self-contained and non-cooperative (not dependent on equipment located on other aircraft or on the ground), the BiDCAS concept employs two reflective Doppler radar transceivers, each with a 90 degree azimuth beamwidth, aimed at 45 degrees with respect to the aircraft's longitudinal axis (Figure 1). Such a system provides half-circle coverage (Figure 2), and exhibits its greatest sensitivity to reflections from targets near the pitch plane of the aircraft (near the user's altitude).

Doppler Principles

The change in frequency of electromagnetic waves as a function of relative motion is now known as Doppler shift. The phenomenon was first described by Johann Christian Doppler in 1842, in a paper delivered to the Royal Bohemian Society of Learning, entitled "On the Colored Light of Double Stars and Some Other Heavenly Bodies." Doppler shift varies directly with both the transmitted frequency and the relative velocity between the transmitter and target, and inversely with the speed of light.

For BiDCAS this Doppler frequency represents the system's audio output and must, for the relative velocities of interest, fall within the frequency response range of human hearing. By defining the desired Doppler frequency, the optimum transmit frequency can readily be determined.

Midair collision statistics suggest that protection is most needed in the vicinity of airports, at traffic-level altitudes. Since Federal aviation regulations have established a "speed limit" of 250 knots below 10,000 feet, the maximum relative velocity between two aircraft would be 500 knots. For convenience, we can establish a Doppler frequency of 3 kHz as corresponding to a 500 knot closing rate. Since Doppler shift is nearly linear, a relative velocity of 250 knots will produce a 1.5 kHz difference frequency, 50 knots will yield 300 Hz, etc. This places Doppler

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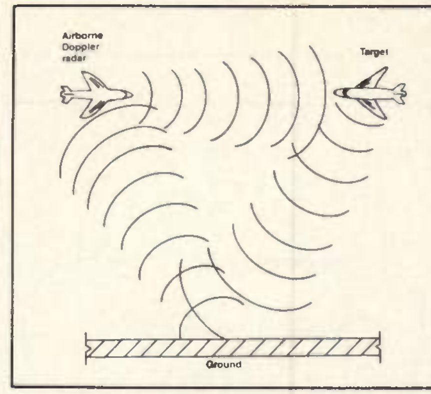

Figure 4. Multipath reception from ground reflections.

shifts for relative velocities between 50 and 500 knots in the audio frequency range for which aircraft communications systems are tailored. The optimum transmitter frequency was determined to be in the vicinity of 1750 MHz. Thus, BiDCAS defines itself as an RF system.

Range Considerations

The required range of a collision alert system is influenced by two mutually exclusive considerations: maximizing warning time, and minimizing false alarms. High sensitivity allows the most time for a pilot to spot traffic and take corrective action, but can indicate the presence of aircraft which pose no hazard at all, distracting the pilot and eroding confidence in the system.

As noted earlier, most midair collisions occur near airports. A three-year study by Chapman (8) found this number to be 63 percent. The radius of a standard FAA Airport Traffic Area is five statute miles (8 km), and it is felt that a similar range would provide adequate protection during the most hazardous phase of the flight, while minimizing distractions en route. At a five mile range, the maximum closing rate of 500 knots affords more than 30 seconds of warning. In visual meteorological conditions, this is not only considered ample time to respond (9), but it exceeds the warning time typically given by the current system of ground-based radar, airborne transponders and radioed traffic advisories.

The maximum range at which a reflective radar system can detect its target, as described by the Range Equation (10) is a function of transmitter power, antenna gain, receiver sensitivity, target effective area and target reflectivity. However, for the BiDCAS system, not all of these factors are within the control of the designer.

Ground based radar achieves its significant range by operating at transmitter power in the thousands of watts. In airborne situations, it is considered good engineering practice to keep the RF power output as low as possible, to minimize interference to other users and other aircraft systems, and to reduce any radiation

BiDCAS Designer Receives Patent, Wins Safety Award

On December 15, 1987, U.S. Patent No. 4,713,669 was issued to H. Paul Shuch for the system described in this article. As is often the case, the patent was issued after about one and a half years of appeals, following the original filing. In addition, the Federal Communications Commission has allocated the frequency of 1607.5 MHz, within the Aeronautical Service's portion of L-Band spectrum, for airborne collision avoidance. This frequency is within 10 per cent of the "optimum" frequency at which the breadboard was tested.

After winning one of the honorable mention prizes in the RF Design Awards contest for its engineering design, the BiDCAS idea was the winner of another contest, the EAA/AVCO Lycoming Safety Achievement Contest. Paul was awarded his prize of a new AVCO/Lycoming O-235 aircraft engine at ceremonies held during the 1987 Experimental Aircraft Association Fly-In Convention at Oshkosh, Wisc.

Mr. Shuch is seeking to license the system for manufacture and sale to the aviation community. Interested persons should contact him directly.

hazard to personnel. Economic considerations may further reduce transmitter power, given the current high cost and low efficiency of solid state microwave active devices.

Directional radar systems with swept antennas can maximize range by employing high gain, narrow beamwidth antennas for transmit and receive. The BiDCAS concept, on the other hand, requires two low gain antennas, each with 90 degree beamwidth to achieve coverage in front of the aircraft. The desired pattern can be readily achieved using circularly polarized cylindrical waveguide feedhorns (Figure 3 and Table 1), with orthogonal transmission and reception senses, taking advantage of the sense reversal upon reflection. However, the wide antenna beamwidths preclude the use of antenna gain to increase range. The use of circular polarization also helps to eliminate nulls and falsing from multipath reception (Figure 4), because each signal reflection produces a polarization sense reversal.

The transceiver duplexer shown in Figure 5 produces the desired dual polarization with a simple quadrature coupler, which can be inexpensively implemented in microstripline. Hislop describes a switching mixer similarly employing such a coupler (11), for the purpose of eliminating the ferrite circulator or mechanical relay traditionally used to couple transmit and receive circuitry to a common antenna. However, that design requires a DC bias change to switch between transmit and receive modes, while this design permits simultaneous transmission and reception.

The use of the hybrid coupler as a polarization duplexer eliminates the need for a costly and bulky circulator. Proper local oscillator injection from the RF source to the mixer diode is controlled by regulating the directivity of the hybrid coupler. In addition to the collision alert system described here, possible applications of the duplexer include microwave intrusion detectors, industrial process control motion sensors, radar altimeters, police speed radars, automatic braking systems, marine radar units and duplex communications transceivers.

Radar sensitivity varies inversely with noise factor and bandwidth. The noise factor of a single-ended Schottky diode mixer, as used here, is on the order of 5, representing a noise figure of roughly 7 dB. The minimum receiver bandwidth is limited to the maximum Doppler frequency difference to be measured (3 kHz). However, the human ear-brain combination has the ability to "zero in" on audio frequency components significantly below the broadband noise threshold. Considering that the user will be concentrating on CW tones within the audio passband, an effective "signal processor" bandwidth of 100 Hz or less may be a more appropriate figure for sensitivity analysis.

Although target cross-section effective area for "small aircraft" is listed as high as 200 square feet (12), this figure seems unrealistically optimistic. General aviation aircraft exist which weigh in at as little as 1000 pounds, although the FAA definition

ANTENNAS:	
ANT1, 2	Cylindrical Waveguide Horns per Figure 5 and Table 2
CAPACITORS:	
C1	1 uF 15 VDC Tantalum
C2, C3	100 pF Chip, ATC 100B or equivalent
C4	Etched microstrip bypass, .18" wide by .86" long
C5	1000 pF Ceramic Feedthru
C6, C7	100 pF Ceramic Disk
C8-C13	0.1 uF Disk
C14-C16	250 uF 15 VDC Tantalum
C17, C18	5 uf 15 VDC Tantalum
DIODES:	
D1	1N752, 5.6 Volt Zener
D2, D3	Schottky Mixer Diode, HP 5082-2835
HYBRID COUPLERS:	
HY1-HY3	Microstrip Quadrature Branch Couplers Series Branches .18" wide by .86" long Shunt Branches .11" wide by .88" long
RESISTORS:	
R1	10 k Ohm 10 turn trim pot
R2	50 Ohm 1/8 Watt Chip Resistor
R3	150 Ohm 1 Watt 10% Carbon Composition
R4, R5	100 k Ohm 1/4 Watt 5% Carbon Composition
R6, R7	2.7 M Ohm 1/4 Watt 5% Carbon Composition
R8, R9	470 k Ohm 1/4 Watt 5% Carbon Composition
R10, R11	4.7 k Ohm 1/4 Watt 5% Carbon Composition
R12, R13	100 k Ohm 1/4 Watt 5% Carbon Composition
R14	Dual Ganged Potentiometer, 10 k Ohm, Audio Taper
R15, R16	100 k Ohm 1/4 Watt 5% Carbon Composition
R17, R18	2.2 k Ohm 1/4 Watt 5% Carbon Composition
R19, R20	100 k Ohm 1/4 Watt 5% Carbon Composition
RF CHOKES:	
RFC1, RFC2	Etched Microstripline, .025" wide, .93" long
MICROCIRCUITS:	
U1	Voltage Controlled Oscillator, Watkins Johnson V801 or Avantek VTO-8150
U2	GaAs MMIC Amplifier, Seimens CGY-40
U3	Low Noise Dual Preamplifier, LM387
U4	Dual 2 Watt Audio Amplifier, LM377

Table 3. Parts list. Refer to schematic diagram in Figure 7.

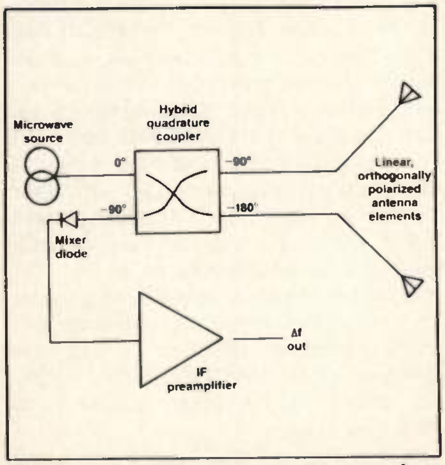

Figure 5. Microwave transceive duplexer for opposite-sense circular polarization.

of "light aircraft" is one 12,500 pounds or less. In the worst case for the proposed system (aircraft converging head-on), a typical aircraft with thin wings and tail would have a radar profile dominated by its spinning propeller disk (Figure 8). With typical propellers about two meters across, a worst-case radar cross-section would be roughly π square meters, or 34 square feet.

Target reflectivity also seems overestimated in traditional radar literature. Reflection of radar signals occurs only when the characteristic impedance of the target differs markedly from the 377 ohm impedance of free space. In fact, stealth technology employs various coatings to match the surface characteristic impedance of military aircraft to that of free space, minimizing reflections. Although no attempt is made here to detect and protect against stealth bombers, the surfaces of wood, fabric and composite materials found on a many general aviation aircraft are less than fully reflective. In the analysis that follows, a reflectivity of 0.5 is assumed.

Link analysis (Table 2) indicates that for a mere 50 mW per transmitter at 1750 MHz, a 7 dB noise figure receiver with 100 Hz effective bandwidth, the antenna described in Figure 3, and a 50 percent reflective target of 2 meters diameter, unity signal-to-noise ratio can be achieved over a distance of roughly one mile. To increase the range to the desired 5 miles, it is necessary to increase the transmitter power above that used in the prototype.

The range restriction applies to a signal-to-noise ratio in excess of unity. However, in addition to the known ear-brain processing advantage noted earlier, there is evidence that binaural presenta-

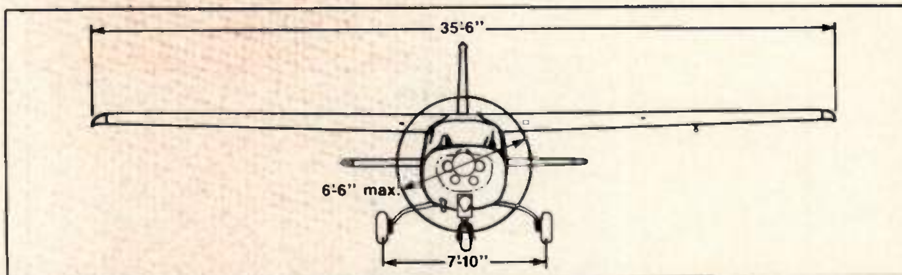

Figure 6. Typical light aircraft frontal radar cross-section.

tion can significantly enhance the readability of weak signals. Krytar (13) has shown that an advantage of up to 16 dB over monaural presentation can be obtained when a signal and interference are each of equal strength in both ears, but oppositely phased. In another binaural communications system (14), Sommer notes that, "broadband noise, either thermal or atmospheric, is perceived in panorama and, although audible, is less distracting because your attention is focused on a signal that appears to originate from some particular direction." Thus, the range of the BiDCAS system may not be as limited as the above calculations suggest.

Flight Hardware

It was initially feared that the physical constraints which the aircraft environment places on antenna geometry might impact binaural performance. However, Campbell (15) reports that, "the antenna spacing required to achieve the binaural advantage does not appear to be at all critical. Spacing may thus be optimized for transmitting pattern or mechanical constraints without compromising binaural receiver performance." Prototype testing has confirmed the system's tolerance to antenna geometry. On the other hand, phase information is important. The use of two independent Doppler transceivers as shown in Fig. 1 produces a noticeable region of confusion at the crossover point, due to the lack of a common phase reference for both channels. This difficulty is readily resolved by driving both Doppler units from a common RF source, as indicated in the schematic diagram of the complete BiDCAS system (Figure 7).

A complete parts list for the prototype system appears in Table 3. The unit employs two linear integrated circuits for audio processing, and two hybrid RF microcircuits to generate the required CW Doppler signal. Since all RF subassemblies are internally matched to a 50 ohm interface impedance, the system is non-critical as to construction and operation. Fabrication uses a microstrip substrate of inexpensive fiberglass epoxy printed circuit material. The total component cost, including the etched couplers and antennas, is under $300 for a single unit. It is expected that a fully operational and airworthy commercial version of this design can be produced at a retail cost of less than $1,000. At this price, few aircraft owners are likely to hesitate at adding this protection against midair collisions.

Summary

Aircraft midair collisions, though in number not a statistically significant occurrence, represent a major area in which safety can be improved through existing technology. The myriad of competing collision avoidance systems proposed and implemented to date have various weaknesses or limitations with respect to their universal use in general aviation aircraft.

A non-cooperative collision alert system has been outlined which can be produced at a low cost, installed on virtually any aircraft, and which produces a novel aural indication of the position of potentially conflicting air traffic. The simplicity of the RF circuitry employed suggests that the unit is economically feasible, and should yield highly reliable, easily interpreted and consistent results. Preliminary testing indicates that the proposed system is worthy of further study.

The design described here is one of the honorable mention prize winners in the second RF Design Awards contest. Since then, it has received even more attention, as noted in the sidebar, "BiDCAS Designer Receives Patent, Wins Safety Award." The circuit implementation has also had one small change, the replacement of the GaAs CGY-40 amplifiers with more readily available silicon bipolar MMICs. rf

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About the Author

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Mr. Shuch is active in aviation as a pilot, with Commercial and Instrument Flight Instructor ratings. He is a volunteer FAA Accident Prevention Counselor and was the founding Chairman of the Santa Clara County Airports Commission. Paul can be reached at Microcomm, 14908 Sandy Lane, San Jose, CA 95124, (408) 377-6137.

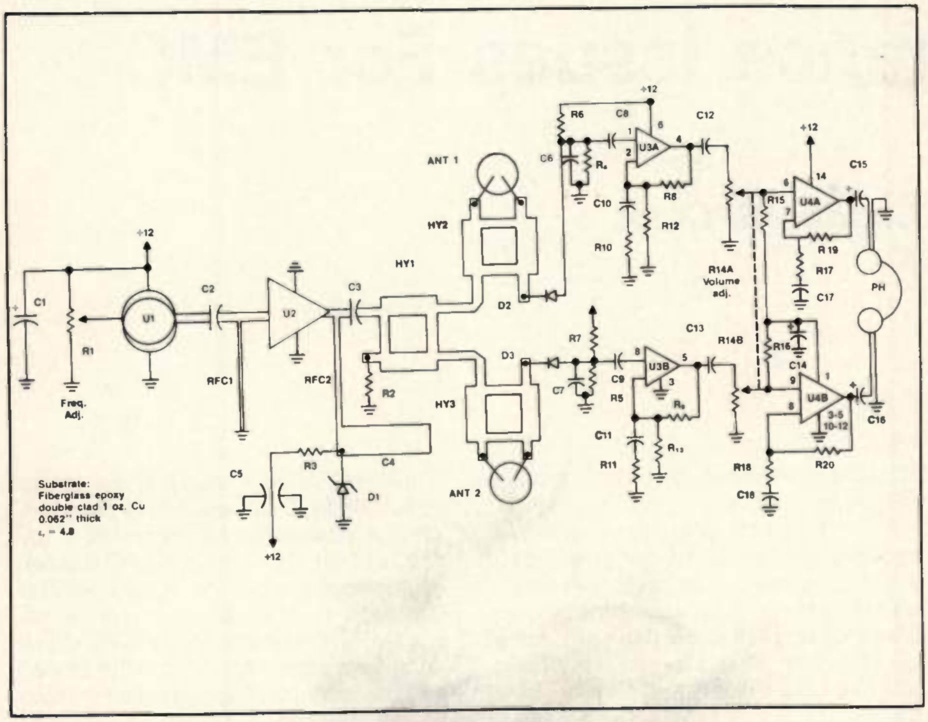

Figure 7. BiDCAS schematic diagram.

Quality Assurance Issues For EMC

Part II: Statistical Process Control (SPC) for Product and EMC Test Sites

By Mike Howard
Norand EMC Test Lab

As was discussed in Part I of this article (April 1988 RF Design*), attention must be given to ensure that the process of compliance of products with EMC test requirements such as FCC Part 15-J and VDE 0871 is in control. Background information was given in Part I to substantiate the requirements for continued compliance. A structured approach and measurement tool was reviewed to minimize noncompliance from the initial engineering unit to final production units. In Part II, a tool called Statistical Process Control (SPC) is used for monitoring both the EMC Test Lab test process as well as keeping track of the manufacturing process as it relates to EMC compliance. SPC is the process of monitoring a process quantitatively and using statistical signals to determine whether to leave the process alone or change it. It can be a valuable tool for the EMC community in preserving compliance. This article provides a discussion on the proper use and implementation of SPC in maintaining compliance of products as a function of providing quality assurance in EMC. Emphasis is placed on testing for variability rather than testing to a specification limit to maintain compliance.*

Statistical Process Control (SPC) involves three key elements. The first is that the process, product, or service must be measured accurately. This can be measured by variables or attributes (i.e. go/no-go). Note that variable data is preferred over the go/no-go method. This data is gathered by the operator who is closest to the actual process being measured.

The next key element is that the gathered data should be analyzed using control charts. The control charts determine how much the process can be expected to vary if it is operating consistently. The charts then indicate if the process is stable or changing. This article addresses X-BAR and R charts only, though other chart types are available for use with SPC.

The third and final key element is that based on the control chart graphs, corrective action should be taken where required. If the process is in control, then the process is left alone. If the process is out-of-control, then corrective action is taken to bring the process back into control.

It is these three key points of SPC that provides a method for providing a high degree of confidence in a test facility's measurement repeatability and accuracy. Also, the ability to verify that the manufacturing process is in check or control for continued EMC compliance is provided. Both processes can be measured at the EMC test lab. Other types of SPC that can be implemented outside of the EMC test lab, such as in production, will be discussed later on in this article. SPC will be addressed separately for both the test lab and the production units audited for continued compliance.

Test Lab SPC

As was presented in Part I, whenever error can be reduced in the measurement task more attention can be given to the

	DATE/TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
READINGS	1																				
	2																				
	3																				
	4																				
	5																				
	6																				
	SUM																				
$\bar{X}=\frac{\text{Sum}}{\text{\# of readings}}$																					
R = highest - lowest																					

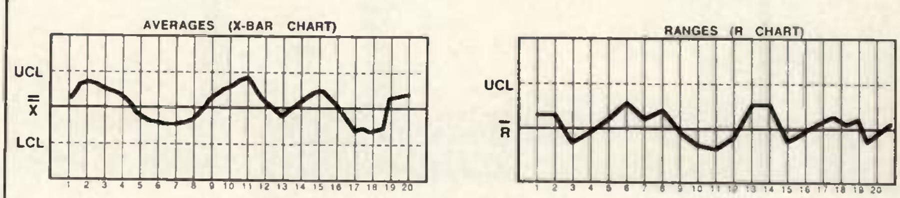

Figure 1. X & R control charts.

EMCO UPDATE

New Product Helps Maintain Test Site Integrity

Generator Provides Reference Standard

How do you know if the integrity of your test site is being compromised? Leaky gaskets, loose cable connections, and stray RF signals are only a few of the things that can cause test site characteristics to change. Sometimes the changes are so gradual, they may go unnoticed for an extended period of time. Until these flaws are corrected, the validity of your test results are in question.

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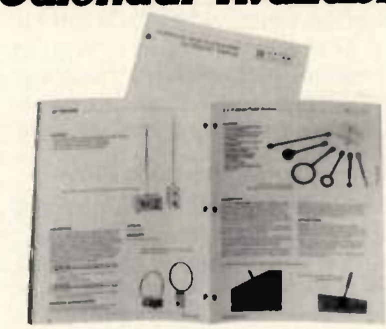

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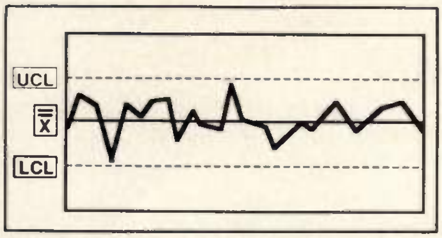

Figure 2. Example of an in-control measurement process.

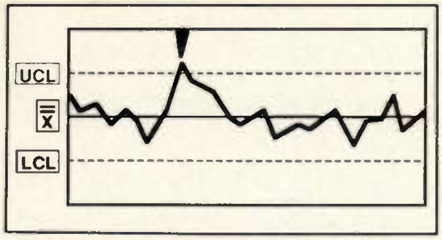

Figure 3. Example of an out-of-control measurement process.

actual product development and analysis for EMC. This will increase user confidence in the final EMI/EMC test results. This is critical when implementing an audit program for continued compliance. The first step is to ensure that the measurement process is in control before the manufacturing process is determined to be in control for audit purposes of EMC. SPC can be used to accomplish this goal for the test lab.

One method to apply SPC to an EMC test lab is to perform weekly measurements of a standard RF source to produce X-Bar and R chart's of the EMI measuring system repeatability. This source should have a stable multi-frequency output and be battery operated. Control charts can also be used to chart the short and long term output stability of this source to further check the overall measuring system repeatability and accuracy. Such a standard test source and its usage has been described in reference 2. A set number of frequencies, typically six or more, are selected for each weekly measurement. The emissions from the standard source at these selected frequencies will not necessarily be of the same amplitude. So it is necessary to normalize these amplitudes by subtracting the average emissions at each frequency for the first 20 data sets or weeks. Next, the average of the selected number of frequencies normalized amplitude is calculated and plotted on the control chart as seen in Figure 1.

An in control process for the measurement task would be representative of the graph shown in Figure 2. Out-of-control measurement processes would be depicted as shown in the graphs of Figures 3 through 5. If such an out-of-control process is detected, the following areas of the measurement task need to be addressed to resolve this undesired condition. Any one or combination of the following items may contribute to an out-of-control process: site cleanliness or abnormalities; RF cable integrity; integrity of metal ground plane and grounding scheme; instrumentation calibration; test procedures used by personnel; integrity of site calibration source; and status of any all-weather covering material used.

The X-Bar and R charts alert the operators closest to the measurement task when the above mentioned items must be investigated and corrected for out-of-control situations during the measurement process. The procedure as outlined may be used on a periodic, daily, or weekly check of the measurement process to keep in check the variables within the measurement process.

Production Run Audit and SPC

For production run audit purposes of products for continued compliance with EMI standards, SPC will provide the methodology to keep in check manufacturing processes that can affect the product's FCC/VDE level of acceptability. In Part I, the 10 dB guardband was used as an initial flag to alert engineering and production of a product in marginal compliance. The 10 dB guardband does not give enough detailed information as to the natural variation of the process in relation to compliance to a particular EMC test standard.

Here, as with the test site, a set number of product emissions at selected frequencies should be used for control charting purposes. Keep in mind, that for continued compliance, all frequencies within the test requirement range must be evaluated for compliance test purposes. But for SPC, only a key set or group of frequencies is required to measure the control of the manufacturing process. The selection of these frequencies should be selected to give an indication of changes that may occur in grounding & bonding; overall shielding effectiveness of the product; workmanship; frequencies unique to certain PCB assemblies or sub-systems (i.e., xtal's, oscillators, or data rates); and tool wear and usage.

Giving attention to frequencies that may be related to the above items will aid in any future corrective actions required on indications from the control charts of out-of-control processes. Along with the selected frequencies for each product, it is necessary to select a reasonable sample size of product for each set of data taken at the required number of intervals during production runs.

SPC can also be used to monitor component or select processes used in the manufacture of a product. An example would be to take sample measurements on the following items.

- Conductivity and shielding effectiveness of conducted coatings used on plastic enclosures.
- Insertion loss measurements of line filters, ferrite beads, etc.
- Ground and bond impedances of critical points and connections.

The control charts of these items can be used with the overall control chart of the product to further aid in determining, when necessary, the out-of-control process.

Control Charts (X-Bar & R)

A detailed explanation on the generation of X-Bar and R charts is not given here, but rather a general overview of the application of these charts for SPC in EMI/EMC compliance issues.

A control chart is a graphic representation of a characteristic of a process, showing plotted values of some statistic gathered from that characteristic, a central line, and two control limits. The control chart is used to determine if a process has been operating in statistical control, and is an aid in maintaining statistical control. The control limits used in the control chart can be used to determine the significance of the variation from one or more events of measurement. Variation beyond a control limit is an indication that a source of variation is affecting the process and that corrective action is required to bring the process back into control. Control charts give people closest to the operation reliable information regarding when action should or should not be taken.

X-Bar refers to the average of values in the events of measurement and R refers to the range of the measurements within a group of events. An example of an X-Bar and an R chart can be seen in Figure 1(3) while an example of a process in control is represented in Figure 2. An out-of-control condition exists anytime an average X-Bar is outside the control limits as seen in Figure 3. This indicates that a special cause is present. When seven or more consecutive average X-Bars are above or below the process average X-Bar, there is an out-of-control condition (Figure 4). Looking at the middle third between the control limits, you should expect to find two-thirds of the X-Bars to be within this area. If not, the distribution is

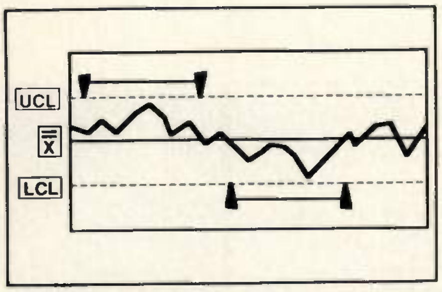

Figure 4. Measurement of an out-of-control measurement process.

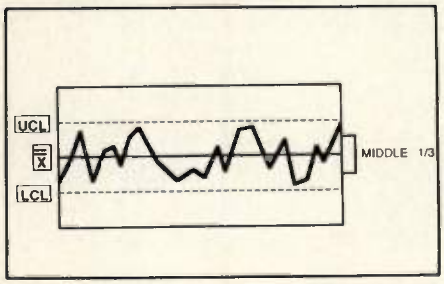

Figure 5. Example of an out-of-control measurement process.

not normal and the process is considered out of control as seen in Figure 5. The same analysis of the process can be used for the range (R) of measurements.

When an out-of-control condition exists within the process, immediate action must be taken. The inputs to the process (i.e. machine, material, method, people, or the environment) has to be looked at in order to solve the out-of-control process. Generally, the process is changing or moving towards a mode of instability and/or unpredictability. The control chart does not define the action to be taken. It can, though, lead the operators in the right direction. Additional problem solving tools such as cause and effect analysis, brainstorming, and peer review are required to aid in finding a solution to the out-of-control condition (4).

Conclusion

Both EMI/EMC testing and the aspect of producing a product for EMC compliance is a process. Statistical Process Control is a tool which can effectively be used to monitor this process for out-of-control conditions and alert the operator/support personnel to take corrective action immediately. By using SPC control charting for the EMC test lab, a significant increase in user confidence in the final EMI test results can be realized. This will also reduce time trying to explain possible errors or out-of-control situations within the test lab, because the control charts will depict the in or out-of-control situations along with any corrective action taken by the lab personnel to regain control of the measurement process. This allows more effective time spent on the design and production aspects of the product process for EMI/EMC compliance. SPC control charting for the product during audit testing can provide invaluable information as to the processes used to ensure compliance. As with any tool, SPC must be used correctly and faithfully on a continued and periodic basis to be fully effective.

Product quality, cost and time savings, and continued compliance is just a small sampling of benefits that can be realized by implementing a comprehensive quality assurance program when considering Electromagnetic Compatibility requirements of todays electronic product. EMC testing and compliance requirements are complex in nature and require the use of several tools and methods, such as SPC, to be successful.

The reader is urged to study the references at the end of this article for detailed use and explanation of X-Bar and R charts for SPC. The author may be contacted for additional information on this subject, as well.

The author wishes to thank Simon Brooks and Bev Reynoldson of Norand Corporation for their assistance in the preparation of the artwork and documentation for this article. rf

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About the Author

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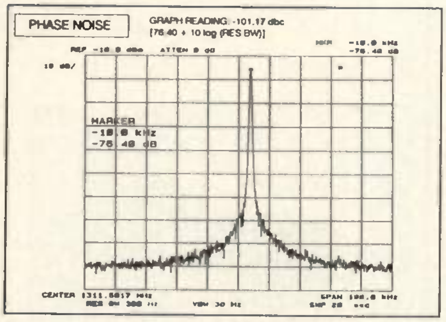
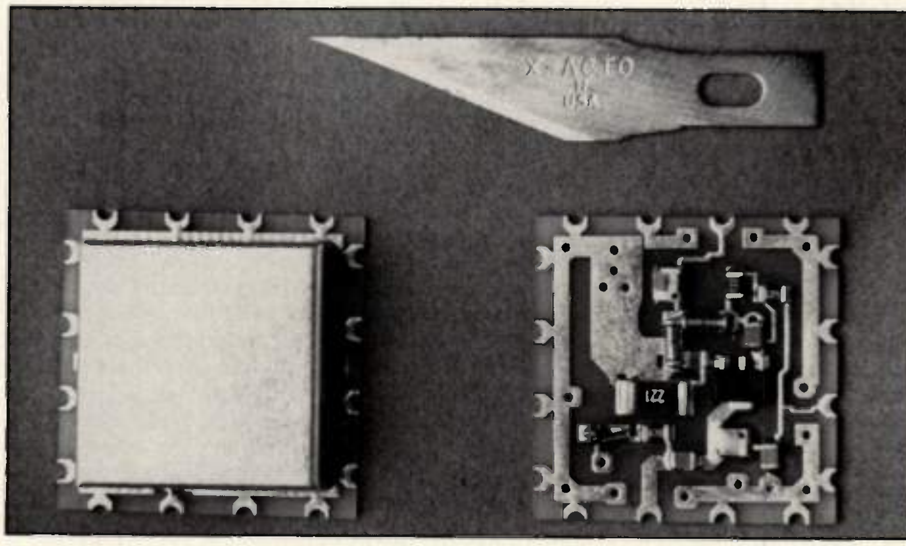




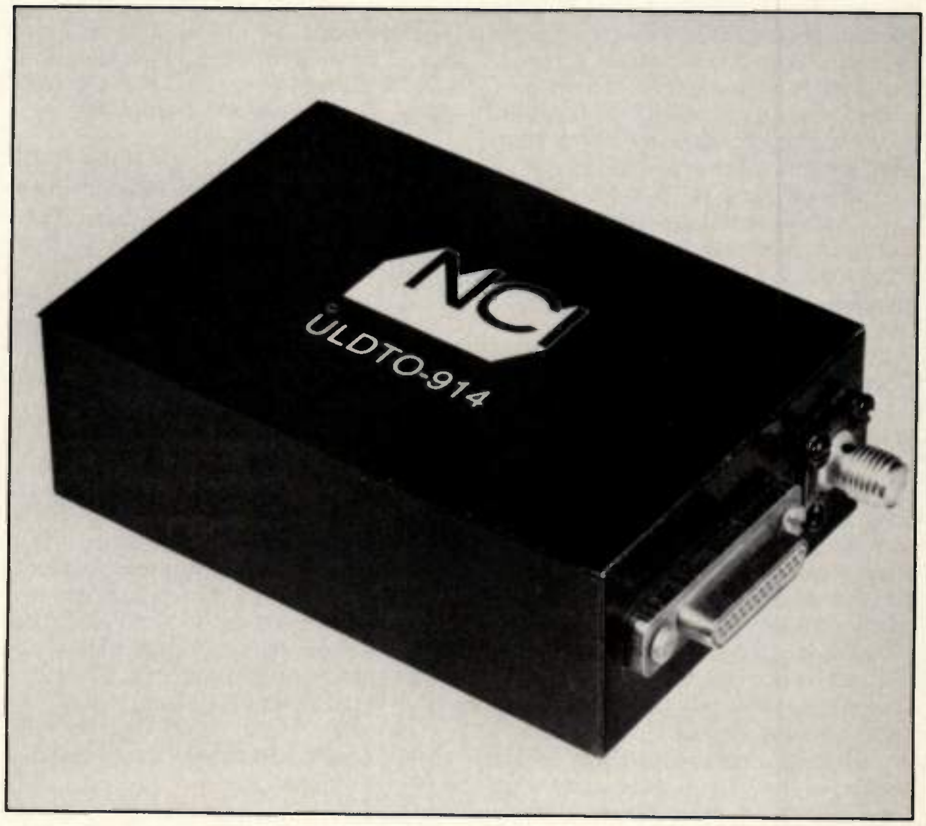
This device, Model C-600SM, has a tuning sensitivity of 36 MHz/V, power output of 11 ±1.5 dBm into 50 ohms, load impedance of 50 ohms, and maximum input capacitance of 50 pF. It requires 15 VDC at 46 mA to operate and can also be operated with a Vcc of 5 V and 15 mA with RF output power of 0 dBm. The operating temperature range is 0 to 70°C and dimensions are 0.81" × 0.81" × 0.25". The price for this VCO is $60 with quantity discounts. **Z-Communications Inc., Ft. Lauderdale, FL. INFO/CARD #220.**

NCI Introduces a Family of DTOs and Synthesizers

The four product lines being featured are the ULDTO, OLDTO, FSDTO and FSS. The ULDTO series closed-loop oscillators are designed for use as sources in highly stable frequency modulators or as sources for phase locked loops. The OLDTO series of open-loop oscillators are for use with phase locked loops and coarse-tuning local oscillators.

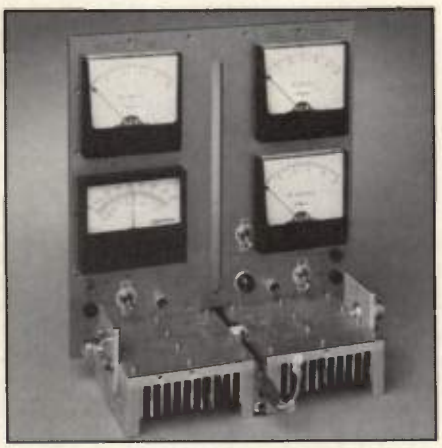
For systems that require rapid acquisition of unstable signals, the FSDTO series of fast set-on oscillators are appropriate. The FSS series frequency synthesizers can be designed with direct, indirect, or digital techniques to optimize phase noise and settling time.

All four products are available in standard configurations or in custom designs. They are available in frequency ranges from 800 MHz to 18 GHz, with power output of 10 dBm to 23 dBm. All conform to MIL-I-45208A, and can be screened to MIL-STD-883. Harmonic output of the DTOs is better than −12 dBc, spurious output is better than −65 dBc and phase noise of the synthesizers is typically −85 dBm 10 kHz from the carrier, and −130 dBc at 1 MHz from the carrier. **NCI, Division of Noise Com, Inc., Paramus, NJ. INFO/CARD #219.**



Universal Test Platform

Acrian introduces the Universal Test Platform (UTP) aimed at providing the RF circuit designer with an off-the-shelf RF power test platform capable of simulating a variety of baseplate/heatsink environments. In its basic configuration, the UTP-1 is a finned heatsink that incorporates a built-in heater to simplify high temperature testing, a built-in thermocouple probe to monitor baseplate temperature, and is fully plumbed for coolant flow to simplify low temperature or room temperature testing.



The UTP-3, another test platform, contains fins, coolant lines, heater, and thermocouple probe as well as a full display panel featuring meters displaying DC collector supply voltage, DC collector current, DC base supply voltage, and baseplate temperature. Also included are on/off switches to control V_{CC}, V_{BB} and the heater. A plunger option to allow the UTP to be used as a press-in transistor test fixture is available. The UTP-1 is priced at $1,650. **Acrian, Inc., San Jose, CA. INFO/CARD #218.**

SMT Inductor Kit

This kit from Coilcraft contains 480 samples of surface mount inductors. The inductances range from 4 nH to 33 uH.

The 10 percent and 20 percent tolerance inductors come in 1008 and 1611 body sizes. The kit, Model C100 costs $125. **Coilcraft, Cary, IL. INFO/CARD #217.**

CW Microwave Counter

The 535B and 538B provide basic frequency counting from 10 Hz to 20 GHz and 26.5 GHz respectively. The 545B and 548B full function counters provide all the functions of the 535B/538B at the same frequency ranges with additional features such as multiple signal selectivity, optional frequency selective power measurement and optional frequency measurement to 110 GHz. The price on these four counters range from $4,950 to $7,900. **EIP Microwave, Inc., San Jose, CA. Please circle INFO/CARD #216.**

CMOS PLL

A linear voltage-controlled oscillator

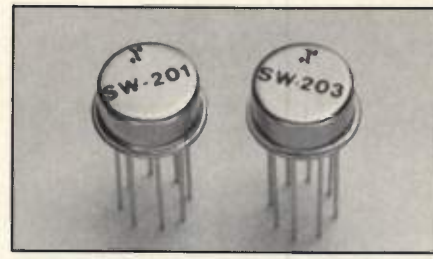
(VCO), a lock detector circuit and two types of phase comparators are built in to the CD54/74HC/HCT7046A phase locked loop integrated circuit from GE Solid State. Users can choose between an exclusive OR phase comparator that requires the signal and comparator frequencies to have 50 percent duty cycles, and an edge-triggered J-K flip flop comparator that places no constraints on signal and comparator duty-cycle. Detection of a locked loop condition is accomplished by a NOR gate and envelope detector. **GE Solid State, Somerville, NJ. Please circle INFO/CARD #215.**

SAW Delay Line

LR600-500, a non-dispersive SAW delay line, offers 500 MHz of bandwidth centered at 600 MHz. This 20-tap device provides 0.2 to 4.0 us delays in 0.2 us steps. Maximum attenuation is 50 dB and allowable drive level is +20 dBm. **Phonon Corp., Simsbury, CT. INFO/CARD #214.**

SPDT Switch

The SW-201 and SW-203 SPDT switches operate in a low insertion loss (0.5 dB at 500 MHz) or terminated high isolation (760 dB at 500 MHz) configuration. The SW-201/203 switches in 3 ns, offers a 1 dB compression of +27 dBm and is packaged in a TO-5 header. Price is $52



in quantities of 5 to 9. **Adams-Russell Electronics Co., Inc., Anzac Division, Burlington, MA. INFO/CARD #213.**

HF MOSFET Power Amplifier

Utilizing modular design and power MOSFET technology, this amplifier operates from 2 to 30 MHz, has 300 W pulsed power output and provides 55 dB linear gain. The Model PA3-30 requires 7" in a standard 19" rack. **Intech, Inc., Santa Clara, CA. INFO/CARD #212.**

GaAs Wafers

M/A-Com introduces a semi-insulating GaAs wafer product. This 4 inch diameter crystal has a deliverable yield of over 75 wafers. Electrical quality and uniformity as well as flatness and thickness variations on 4 inch wafers match industry standards for 3 inch GaAs wafers. These large boules provide large diameter substrates with maximum lot yields. **M/A-COM Advanced Semiconductor Operations, Lowell, MA. INFO/CARD #211.**

RF Amplifier

Amplifier Research introduces the Model 250L with 250 W CW linear and a 750 W pulse output mode. It has a bandwidth of 10 kHz to 220 MHz and a minimum input signal requrement of 1.0 mW max. **Amplifier Research, Souderton, PA. INFO/CARD #209.**

AGC Amplifiers

The "CM" Series of RF and IF AGC amplifiers are SMA connectorized side or bottom pin-out modules. The input frequency ranges from 10 MHz to 1 GHz with bandwidths of 30 percent. AGC range is 0 to 80 dB, slope variation is less than 2:1 and price starts at $595 depending on specification and quantity. **Log Tech, Inc., Newbury Park, CA. INFO/CARD #208.**

EMI/RFI Filter Kit

An EMI/RFI filter engineering design kit containing a broad selection of EMI/RFI filters is available from Murata-Erie. The kit is designed to aid the design engineer during the proto-type phase of circuit development and contains both feed-thru and coaxial filters. It contains over 50 filters, with specifications and attenuation characteristics. **Murata Erie North America, Smyrna, GA. INFO/CARD #207.**

Spectrum/Scalar Network Analyzer

The FSAS combines two 100 Hz to 1.8 GHz instruments into one package. As a spectrum analyzer, it features a 100 dB on-screen dynamic range from −145 to +30 dBm and resolution bandwidths from 6 Hz to 3 MHz. As a scalar network analyzer, the FSAS provides measurements up to 130 dB gain and 120 dB attenuation, and amplitude resolution of 0.01 dB. All functions are IEEE-488 compatible and the price is $44,500. **Rohde & Schwarz, Lanham, MD. INFO/CARD #206.**

Flat Decoupling Capacitor

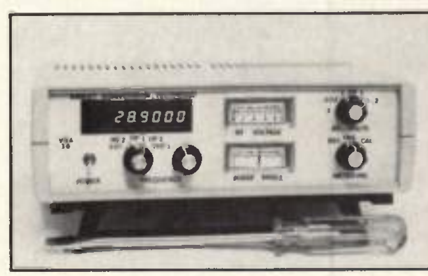
Micro/Q ceramic decoupling capacitors are mounted under the IC, increasing package density. Capacitance ranges from 450 pF to 0.14 uF. Pricing for a 20-pin part in 1000 quantity is 49 cents. Free samples are available. **Rogers Corp., Chandler, AZ. INFO/CARD #203.**

Power Meter

The HP 437B power meter is a general purpose single channel programmable unit. It operates with the HP line of power sensors that cover from 100 kHz to 50 GHz and +44 to –70 dBm. Microprocessor control provides ease for displaying calculated peak power from a keyed-in duty cycle and measured average power. The 1 mW, 50 MHz calibration oscillator port on the front panel supplies 1.2 percent traceable reference accuracy. Instrument accuracy is 0.02 dB or 0.5 percent. Up to 10 separate front-panel setup conditions may be stored for recall. The power meter is priced at $2,500. Two options for rear panel connectors and three new optional power sensors are available. **Hewlett-Packard Company, Palo Alto, CA. INFO/CARD #202.**

RF Network Analyzer

This portable modular automatic vector network analyzer measures linear impedance, VSWR and other parameters.



The frequency range is 100 kHz to 4 GHz and it is made up of tunable frequency sources, a reflected voltage signal sampler, and an amplitude/phase measurement module. It can replace dip and Q meters, VSWR bridges, and various signal generator-spectrum analyzer combinations. **Direct Conversion Technique, Evanston, IL. INFO/CARD #201.**

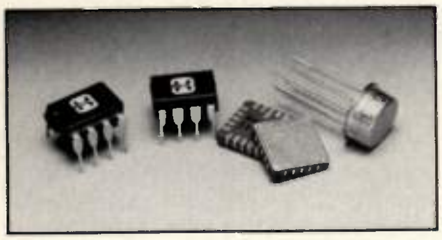
NMR Power Amplifier

Kalmus introduces the Model LP-1000 NMR/MRI pulse amplifier. The frequency range is 10 to 165 MHz while power output from 10 MHz to 125 MHz is 1000 W and 600 W from 125 MHz to 165 MHz. Minimum gain is 60 dB, while input and output impedance is 50 ohms. Third order intermod I.P. is +69 dBm typical, input

VSWR is less than 2:1 while output VSWR is 2.5:1. **Kalmus Engineering International, Ltd., Woodinville, WA. Please circle INFO/CARD #200.**

Monolithic Video Amplifier

A monolithic 33 MHz unity gain bandwidth operational amplifier for video signal processing applications is available from Harris. The HA-2544 offers a slew rate of 150 V per microsecond, 0.04 dB differential gain error, 0.1 degrees of differential phase error and a gain tolerance of 0.2 dB. It is offered in 8-pin TO-99 cans, 8-pin plastic DIP, 8-pin ceramic DIP and 20-pin LCC packages. In quantities of 100, the op amp costs $3.04. **Harris Semiconductor, Melbourne, FL. Please circle INFO/CARD #198.**



IF Preamplifiers

The Model ICFH2104 has been added to the ICFH series of high power IF preamplifiers which span from 20 to 160 MHz. It has a power gain of 30 dB and 3 dB noise figure. The low noise unit provides +15 dBm output power at −1 dB compression for applications requiring high level IF signals. **RHG Electronics Laboratory, Inc., Deer Park, NY. Please circle INFO/CARD #197.**

Phase Locked DROs

The DPLO-XXXX series of fundamental phase locked DROs cover the 1.8 to 18 GHz range. Measured phase noise on a 10 GHz PLO with loop bandwidth of 200 kHz and 50 MHz crystal reference is −94 dBc/Hz at 10 kHz. **Tampa Microwave Lab, Odessa, FL. INFO/CARD #196.**

D-TCXO with 1×10^{-6} Stability

Oscilloquartz introduces the Model 8500 D-TCXO (digital temperature compensated crystal oscillator) — a device that integrates a microprocessor with a VCXO. The frequency ranges from 0.625 MHz to 20 MHz with temperature stability of $\pm 1 \times 10^{-6}$ from −55°C to +95°C. Input voltage is 12 VDC, output signal is 5 V CMOS and aging is 1 ppm for the first year and 0.5 ppm thereafter. **Tauber-Dreyer Corp., Tustin, CA. Please circle INFO/CARD #199.**

INFO/CARD 51

INFO/CARD 52

rf software

Analog Analysis Package

EC-Ace 2.31 has fundamental analog analysis capabilities such as AC, DC, transient, and temperature analysis. It provides sine, pulse, PWL, SFFM, and exponential transient signal generators. The program handles over 100 components and has built-in graphics. The cost is $145 for the IBM PC/XT/AT/PS-2 version. **Tatum Labs, Inc., Ann Arbor, MI. Please circle INFO/CARD #180.**

Updated Version of Superstar

Version 3.2 of Superstar has an expanded S-parameter data base for over 200 active devices including bipolars, MOSFETs, GaAs FETs, HEMTs, hybrids and MMICs. It executes from 5 to 30 percent faster than version 3.1 (depending on systems type) and has EGA and VGA high resolution graphics together with built-in screen dumps to Epson dot matrix printers for Hercules, CGA, EGA and VGA video modes. Optional support for 200 other printers is available. **Circuit Busters, Inc., Stone Mountain, GA. INFO/CARD #179.**

FCC/VDE Software

This package performs all FCC part 15 subpart J and similar VDE measurement requirements. It is designed for use with HP 8568 and 8566 spectrum analyzers with Q-P adaptor and HP 200/300 series computers. The features include open field and conducted measurements, data plotting and tabular printouts, data storage on disk, and data analysis routines. **EMC Consulting, Tucson, AZ. Please circle INFO/CARD #178.**

Performance Analysis and Tune-Up Software

Circuit Master provides performance analysis and an optimization tune-up routine for linear active and passive circuits. It has a library of lumped and distributed components that includes active generators and electron devices, single and coupled transmission lines, waveguides, operational amplifiers, and coupled inductors. Multiport frequency response and impedance data is available in tabular or graphic form. It aids in the design of servo and other feedback systems, filters, amplifiers, transformers, couplers, phase shifters, multiplexers, equalizers, power dividers, chirp networks, and waveguide devices and assemblies. The program is priced at $975. **Hines Consulting Laboratory, Weston, MA. INFO/CARD #181.**

rf literature

Coil and Transformer Catalog

Renco Electronics announces the availability of their catalog which lists coils, inductors, transformers and chokes. It consists of data sheets detailing electrical and physical parameters supported by photos and illustrations of each product. Devices described include toroids, transformers, air cores, subminiature inductors, flat coils, power line, shielded and unshielded inductors, and common mode chokes. Custom inductor design and manufacturing capability is illustrated. **Renco Electronics, Inc., Deer Park, NY. INFO/CARD #176.**

Technical Summary on Libra

This technical summary describes Libra's harmonic-balance simulation techniques that combine linear analysis in the frequency domain with time-domain analysis of nonlinear elements to model nonlinear circuits. The brochure covers the harmonic balance technique used by Libra which offers a high frequency nonlinear analysis capability. Four examples together with graphics are included to demonstrate it's capabilities. **EEsof, Inc., Westlake Village, CA. INFO/CARD #175.**

TMOS Data Book

This revision of the *TMOS Databook* includes logic level power MOSFETs, surface mount DPAKs, GEMFETs (IGBTs) and SENSEFETS in addition to a variety of the previous standard devices. A section on avalanche limitations, commutating safe operating area (CSOA) and dv/dt is included. **Motorola, Inc., Phoenix, AZ. INFO/CARD #159.**

Trimmer and Tuning Device Catalog

Featured in this catalog are air dielectric trimmer capacitors, ceramic dielectric trimmer capacitors, sapphire dielectric trimmer capacitors and microwave tuning devices. The final section illustrates a line of prototyping kits. **Johanson Manufacturing Corp., Boonton, NJ. Please circle INFO/CARD #174.**

Application Note on Frequency-Agile Sources

Characterization of Frequency-Agile Signal Sources demonstrates one of the capabilities of the HP 5371A frequency and time-interval analyzer. The instrument can analyze frequency hopping signals and provides time-sampling capability that allows a signal's changing frequency to be characterized continuously at very high rates. The note discusses switching-transient analysis, settling-time verification, hopping-frequency distribution and the analysis of FM or FSK modulation. An explanation of mixer down-conversion and prescaling to extend the HP 5371A's range to RF and microwave frequencies is included. **Hewlett-Packard Company, Palo Alto, CA. INFO/CARD #172.**

Product Selection Guide

This catalog highlights the specifications on Comlinear's line of operational amplifiers, linear (video) amplifiers, and track and hold amplifiers. A listing of the available data sheets and application notes is included. The final page of this guide lists the company's sales representatives and distributors. **Comlinear Corporation, Fort Collins, CO. Please circle INFO/CARD #173.**

Catalog Describes RF Telemetry Instrumentation

Airborne and ground station transmitters and receivers in P-U-L & S-bands including high efficiency and synthesized broadband video frequencies are described in a short form catalog from Aydin Vector. Typical transmitter specifications include: frequency stability of ± 0.003 percent, output power of 2 to 10 watts with as high as 40 watts optional, linearity of 1 percent BSL method, and FM modulation. **Aydin Vector Division, Newtown, PA. INFO/CARD #171.**

Connector Design Guide

This material specification guide provides the electronic connector designer a framework to identify contact material that optimally meets performance, manufacturing, quality and cost requirements. It assesses the critical design factors and material properties that dictate contact performance: spring force, resistance to permanent set, temperature rise, stress relaxation resistance, and fatigue. The information is then analyzed to determine the alloy and temper best suited to meet overall design and fabrication considerations. **Brush Wellman Inc., Cleveland, OH. INFO/CARD #170.**

Short Form Catalog

K & L Microwave introduces a short form product guide that offers a brief overview of each of it's major product groups.

The products highlighted include filters, crystals, multiplexers, mobile duplexers, crystal oscillators and multicouplers. By completing an attached card, more specific information can be requested on any of the 16 featured groups. **K&L Microwave, Inc., Salisbury, MD. Please circle INFO/CARD #169.**

Test and Measurement Catalog

A catalog featuring the test and measurement product line from John Fluke Mfg. and N.V. Philips is available. It features descriptions, photos and ordering information on over 600 products including oscilloscopes, logic analyzers and GPIB instrument systems, as well as signal generators and counter/timers. Also contained is a list of all Fluke and Philips technical literature available, warranty information, sale and technical contacts, and ordering information. **John Fluke Mfg. Co., Inc., Everett, WA. Please circle INFO/CARD #167.**

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