RF design

engineering principles and practices

March 1992

RF Expo West—Official Show Issue

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Featured Technology
Matching Techniques

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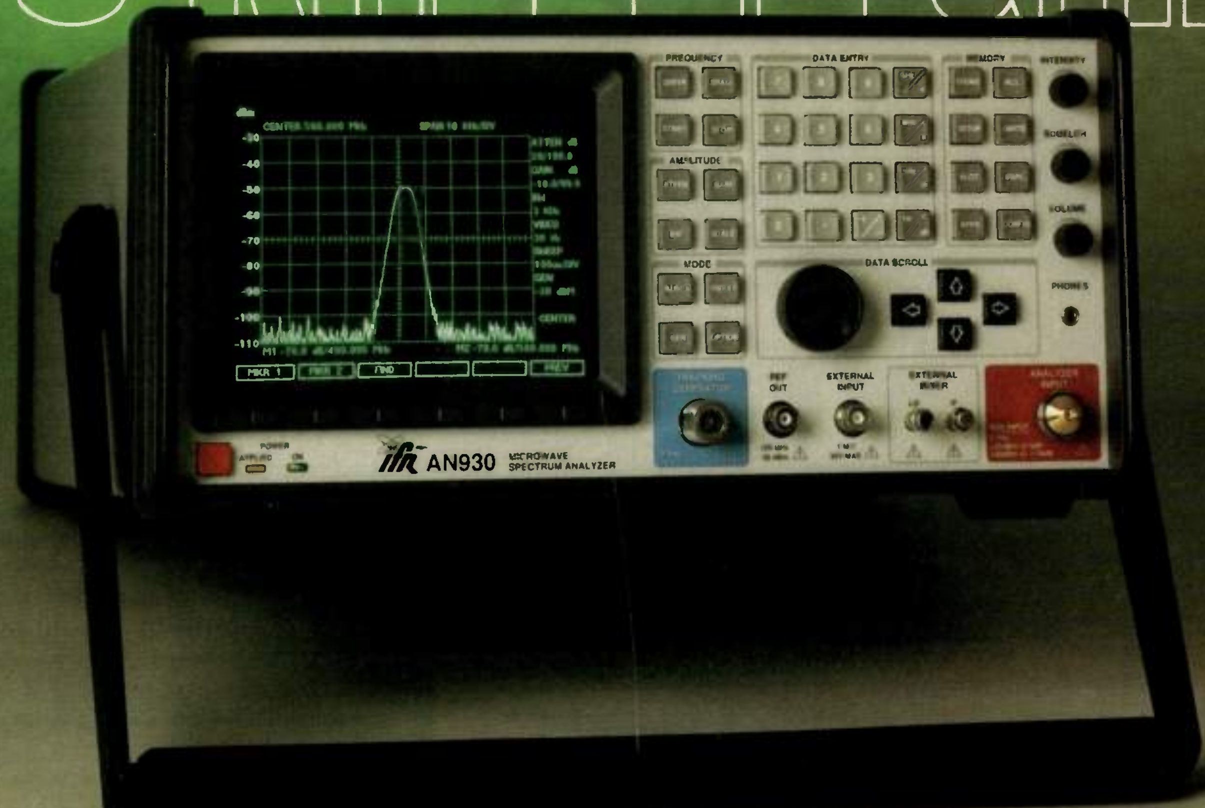
9 kHz-22 GHz



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Featuring low-order, preselected mixing and a highly stable synthesized RF system, the AN930 provides superior amplitude and frequency measurement performance over its entire 9 kHz to 22 GHz frequency range. Support for external mixers extends the AN930 measurement range beyond 22 GHz. A high impedance input permits measurement of baseband signals to 0 Hz and 40 volts peak amplitude.

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STANDARD FEATURES INCLUDE:
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FAX 310/631-8078

DAICO GaAs MMIC Switches

Type	Configuration	Max Freq./GHz	Typ Loss/dB	Typ Iso/dB	Package Style	Comments
P35-4211-0	SPDT-R	2	0.5	26	Chip	Low Cost
P35-4215-0	SPDT-RT	4	0.9	28	Chip	On Chip Term
P35-4226-0	SPDT-RT	6	1.7	30	Chip	
P35-4230-0	SPST-R	12	2.2	23	Chip	
P35-4245-0	DPDT-R	6	0.8	32	Chip	
P35-4250-0	SP4T-R	4	1.1	28	Chip	0.67mm Squared
P35-4252-0	SP4T-T	3	1.0	24	Chip	

DAICO GaAs MMIC Amplifiers

Type	Frequency Range/GHz	Typ Gain/dB	Typ Noise Figure	Typ Power/dBm	Package Style	Comments
P35-4100-0	0.05-3.5	10	6.0	22	Chip	
P35-4101-0	0.5-3.5	9	4.5	22	Chip	Self-Biased
P35-4104-0	0.05-3.0	18	6.0	13	Chip	Low VSWRs
P35-4105-0	0.8-1.8	21	3.5	8	Chip	
P35-4110-0	1-6	7.5	4.6	20	Chip	
P35-4140-0	6-18	5.5	5.5	15	Chip	Pos. Gain Slope
P35-4150-0	2-18	6.0	7.5	15	Chip	AGC
P35-4160-0	3-6	20	2.8	14	Chip	Low VSWRs

This product is manufactured by GEC Marconi Materials, UK and distributed by Daico Industries Inc

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WRH

RF design

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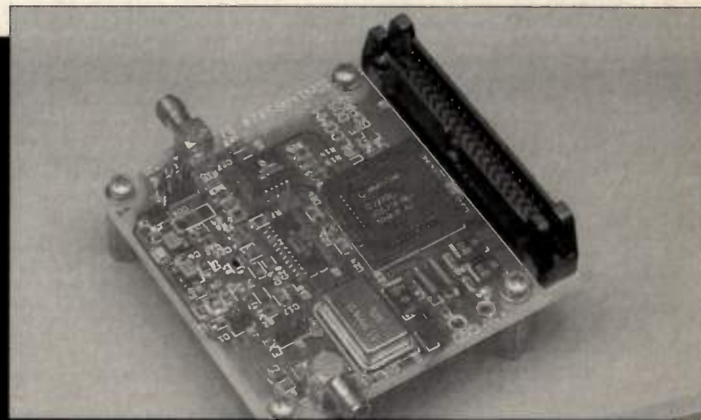
March 1992

featured technology



cover story

design awards

tutorial

departments

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RF editorial

Let's Invest the "Peace Dividend" Wisely

By Gary A. Breed
Editor

By now, it is a foregone conclusion that military spending will continue to be cut, with no foreign superpower able to threaten us head-to-head. We can also safely assume that the Federal government will continue to spend money in all other areas at an unabated pace. We are stuck with irresponsible fiscal management in all three branches of government.

I'd like to add my two cents worth to the discussion of how to handle a significant reduction in military spending, before it all gets frittered away into the proverbial "black hole."

Before we spend any of the money we have saved, be sure some of it is used to pay the mortgage. Voodoo economics has seriously eroded our financial stability. If things get much worse, the Japanese will no longer be such a power —Americans won't have enough money to buy their cars and VCRs! Use some defense dollars to get the debt under control, then spend our taxes more responsibly.

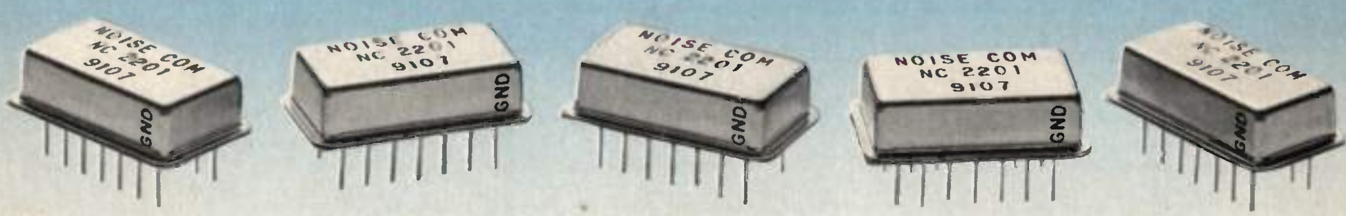
Then, maintain appropriate levels of spending for truly defensive military systems. Electronic surveillance is one such system, requiring the observation and analysis of many different threats around the world. We need to develop efficient, selective systems that don't waste time "reading the mail" on routine communications, but can still locate and zero in on renegade dictators, terrorists and international criminals.

Maintaining a defensive arsenal of weapons and well-trained armed forces is as important as ever. Even if there are no more Desert Storm style wars, there will be U.N peacekeeping forces and occasional threats from belligerent nations. Readiness is essential, 30,000 nuclear warheads are not.

Next, if we are so worried about economic threats from Japan and other Far East nations, why aren't we doing something about it here at home? We should all realize that it no longer is cheap labor that keeps Japan economically strong; it is a combination of long-range planning, smart marketing, goal-setting, manufacturing methods and work habits. Innovation is still the strength of the U.S. Let's invest in a new generation of imaginative products like holographic TV or worldwide handheld telephones, but establish long-term marketing plans and efficient production techniques to keep our overseas competitors from getting rich on ideas we develop.

The RF marketplace that supports us is doing OK. Some applications are great, some are depressed. Fascinating new technology is waiting to be developed. In order to take advantage of the potential markets for these technologies, we have to be willing to do what it takes. We (through our Federal government) must get our financial house in order, establish real priorities on military, foreign and domestic programs, then tax and spend as required rather than as campaign contributors require. The savings from a reduced military budget can help get this process started.

Up to 1000 MHz
Up to +5 dBm
14-pin DIP



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Flatness (dB)	+/–1			
Load impedance (ohms)	50			
Operating voltage (VDC)	12 or 15			
Operating temperature (°C)	–0 to +85			
Temperature coefficient	0.025 dB/°C			
Package	14 pin DIP			

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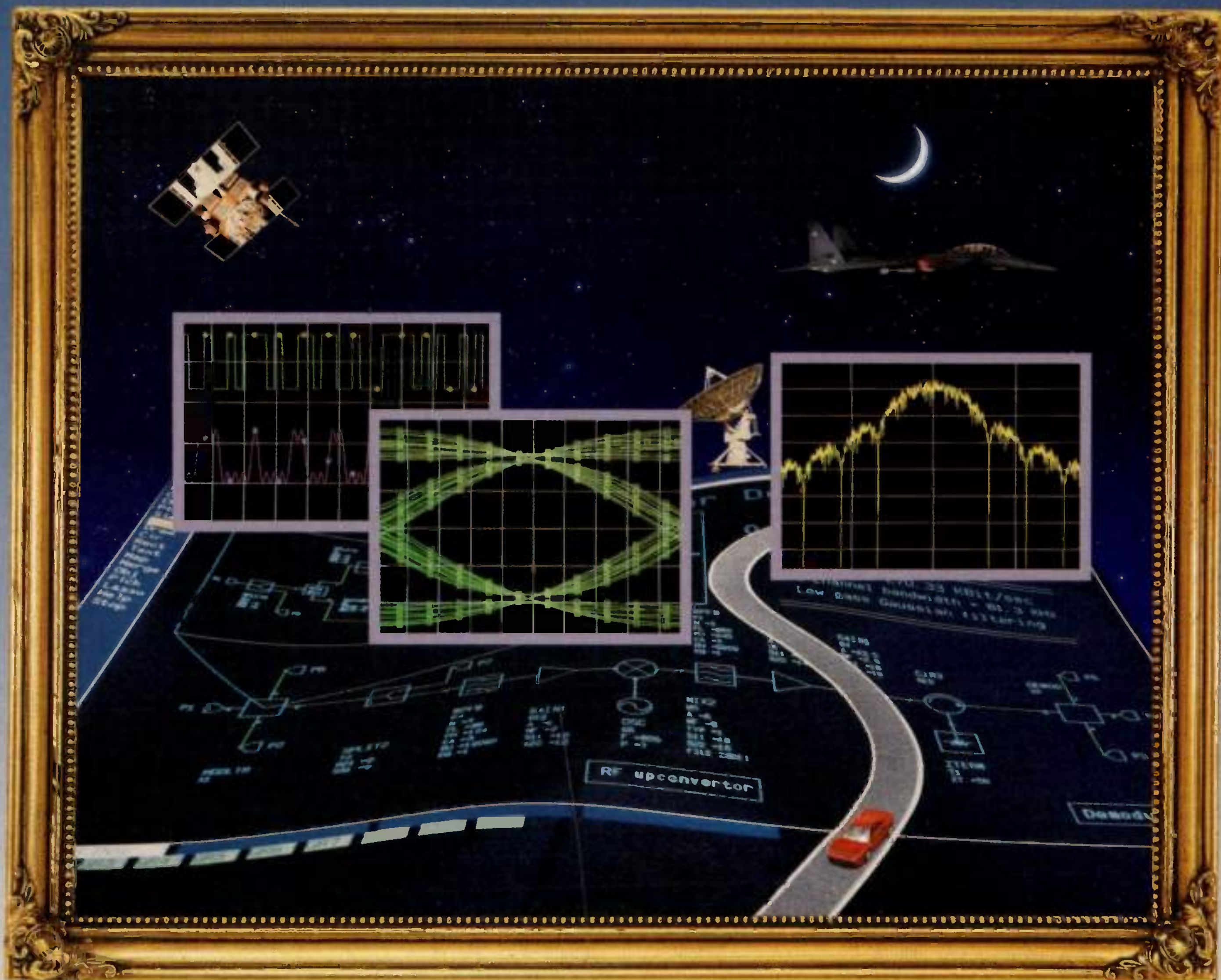

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RF letters

Letters should be addressed to: Editor, *RF Design*, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111. Letters may be edited or excerpted for length or clarity.

Another Remote Control Method

Editor:

After reading "A Low Cost UHF AM Receiver" (*RF Design*, November 1991), I thought your readers might be interested in alternative approach to controlling devices in the home beyond the visible range of a conventional IR remote control. The method is a dual IR/UHF remote control, which is available on some high-end IRDs (Integrated Receiver/Descramblers), the indoor part of a home satellite audio/video system.

For this application, the conventional (and inexpensive) IR remote control was modified by including a UHF oscillator and loop antenna. The oscillator is pulse code modulated by the same digital code that drives the LED. The receiver is a low cost TV tuner, fix-tuned to the UHF oscillator frequency. The incremental cost of this feature is probably under \$15; \$1 for the oscillator and \$14 for the tuner and demodulator. The signal processing requires some software modification, but since the IRD already has a microprocessor there is no additional hardware cost.

With IR remote control already widespread, the addition of UHF signalling is a natural extension.

Michael Neidich
New York, NY

Can Cellular Systems Increase Spectrum Efficiency?

Editor:

The San Francisco Bay area has experienced a series of major catastrophes due to fire and earthquake. Response those disasters exposed problems with land mobile radio systems, which led to the use of alternate forms of radio communications for emergency traffic.

Radio amateurs have played an important role in disaster situations because amateurs and their equipment have a measure of flexibility that land mobile can not equal. Recently, certain agencies have equipped vehicles with both land mobile and cellular telephone equipment. This development merits consideration.

I submit that public agencies can have the flexibility they need with cellular technology. I would further suggest that this can best be accomplished by having one common technology and spectrum for all cellular users.

Clearly, public safety agencies must have priority over other users, especially in an emergency. This priority can be added to the programming of the cellular system and activated by a key or code on the phones used by these agencies. Calls can still have any of the desired features of such systems like scrambling, speed dialing, voice mail, call forwarding, etc. In emergencies, the public safety users can bump civilian users, which parallels existing telephone practice. In major emergencies, portable cells can be brought in to satisfy increased communications load and provide connection to outside systems by wire, fiber optics or satellite.

A major public benefit is that cells could be justified for areas not presently served, supporting both agencies and subscribers. Of course, there will always be a few areas not served. In these areas, amateur radio will continue to serve the public by providing emergency communications when other systems cannot be used.

Giving 800 MHz spectrum to land mobile users was the right idea at the time, but the time has now come to share that spectrum in a cellular system that will best meet the needs of all users.

Robert G. Huenemann
La Honda, CA

An Addendum to our Calendar

In the *RF Design* 1992 calendar mailed with our December issue, we did not have the year of death for Jacques Curie, co-discoverer of the principle of piezoelectricity. In our research, we could not find this information. Our thanks go to reader Phil Pesavento of Henry Radio, who tells us that Jacques Curie died in 1941, according to the book *Piezoelectricity* by Kady, published in 1946.

LOG AMPS 2-18 GHz

FREQUENCY	0.5 to 6.0 GHz
RANGE	− 42 to + 12 dBm
VSWR	1.90 : 1 @ − 20 dBm
OUTPUT RANGE (93Ω)	− 0.33V to − 4.55V peak
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PULSE WIDTH	200 n Sec nominal
PULSE ON PULSE	± 2 dB
PULSE ON CW	± 1 dB

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RF calendar

March

17-19 **Eighth Annual Review of Progress in Applied Electromagnetics**
Monterey, CA
Information: Perry Wheless, Dept. of Electrical Engineering, University of Alabama, PO Box 870286, Tuscaloosa, AL 35487. Tel: (205) 348-1757.

18-20 **RF Expo West 1992**
San Diego, CA
Information: Kristin Hohn, Cardiff Publishing Company, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111. Tel: (303) 220-0600, (800) 525-9154. Fax: (303) 773 -9716.

April

12-16 **NAB '92**
Las Vegas, NV
Information: NAB, 1771 N Street, NW, Washington, DC. Tel: (202) 429-5350. Fax: (202) 429-5406.

21-24 **1992 Conference on GaAs Manufacturing Technology**
San Antonio, TX
Information: Mr. Larry Varnerin, Publicity Chairman. Tel: (215) 758-4061.

22-24 **EMC/ESD International**
Denver, CO
Information: Kristin Hohn, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111. Tel: (800) 525-9154. Fax: (303) 770-0253.

27-29 **40th International Relay Conference**
Chicago, IL
Information: International Relay Conference, Engineering Extension, 512 E.N., Oklahoma State University, Stillwater, OK 74078-0532. Tel: (405) 744 -5714. Fax: (405) 744-5033.

May

12-14 **IEEE Instrumentation and Measurement Technology Conference**
Meadowlands Hilton, NJ
Information: Robert Myers, 3685 Motor Avenue, Ste. 240, Los Angeles, CA 90034. Tel: (310) 287-1463. Fax: (310) 287-1851.

25-27 **International Symposium on EMC**
Beijing, China
Information: Professor Zhang Linchang, Northern Jiaotong University, Beijing 100044.

27-29 **46th Annual Symposium on Frequency Control**
Hershey, Pennsylvania
Information: Mr. Michael Mirarchi or Ms. Barbara McGivney, Synergistic Management Inc., 3100 Route 138, Wall Township, NJ 07719. Tel: (908) 280-2024.

RF courses

Cellular Radio
March 23-26, 1992, Madison, WI
Information: University of Wisconsin - Madison, Francis P. Drake. Tel: (608) 262-2061. Fax: (608) 263-3160.

Microwave/Millimeter Wave Monolithic Integrated Circuits
June 8-11, 1992, Los Angeles, CA
Radiation Hardening of Electronic Systems
June 8-12, 1992, Los Angeles, CA
Information: UCLA Short Course Program Office. Tel: (310) 825-3344. Fax: (310) 206-2815.

Modern Receiver Design
March 16-20, 1992, Washington, DC
April 6-10, 1992, London, England
Ionospheric Radio Propagation for System Planners
March 17-20, 1992, Washington, DC
Lightning Protection
March 19-21, 1992, Orlando, FL
Microwave Radio Systems
March 25-27, 1992, Washington, DC
Broadband Communications Systems
April 6-10, 1992, Washington, DC
Cellular Radio Telephone Systems
April 15-17, 1992, Washington, DC
Analog/RF Fiber-Optic Communications
April 22-24, 1992, Washington, DC
Analyzing Communications System Performance
April 22-24, 1992, Washington, DC
Communications Satellite Engineering
April 27-May 1, 1992, Washington, DC
Advanced Signal Processing
April 27-May 1, 1992, Washington, DC
Mobile Digital Cellular Telecommunications
May 4-6, 1992, San Diego, CA
Grounding, Bonding, Shielding and Transient Protection
May 5-8, 1992, San Diego, CA
Information: The George Washington University, Continuing Engineering Education, Merril A. Ferber. Tel: (202) 994-8522 or (800) 424-9773.

Antenna Analysis, Design and Measurements
March 30-April 2, 1992, Tempe, AZ
Information: Arizona State University, Center for Professional Development. Tel: (602) 965-1740. Fax: (602) 965-8296.

Modern Microwave Techniques
May 11-14, 1992, Bethesda, MD
Antenna Design
June 9-12, 1992, Silver Spring, MD
Radomes
June 9-12, 1992, Bethesda, MD
Antenna Measurement Techniques
June 16-19, 1992, Rockville, MD
Information: Technology Service Corporation, Lynda S. Epstein, Training Coordinator. Tel: (301) 565-2970. Fax: (301) 565-0673.

RF and Microwave Circuit Design I: Linear Circuits
March 23-27, 1992, Garmisch-Partenkirchen, Germany
RF and Microwave Circuit Design II: Non-Linear Circuits
March 23-27, 1992, Garmisch-Partenkirchen, Germany
RF and Microwave Circuit Design: Linear and Non-Linear
May 18-22, 1992 Garmisch-Partenkirchen, Germany
RF and Microwave Component Modeling
May 20-22, 1992, Garmisch-Partenkirchen, Germany
Advanced Digital Communications with Applications to Telephony, Cellular Radio, LANs, ISDN, Fiber Optics and HDTV
March 16-19, 1992, Garmisch-Partenkirchen, Germany
Broadband Telecommunication Networks: MAN, ATM, B-ISDN, Self-Routing Switches, and Optical Networks for Voice/Data/Image/HDTV
March 16-20, 1992, Garmisch-Partenkirchen, Germany
Modern Digital Modulation Techniques
March 16-19, 1992, Garmisch-Partenkirchen, Germany
Information: CEI-Europe/Elsevier, Mrs. Tina Persson. Tel: (46) 122-175-70. Fax: (46) 122-143-47.

Pulsed EMI
April 15-16, 1992, Washington, DC
June 25-26, 1992, Minneapolis, MN
Information: Keytek. Tel: (508) 658-0880.

Electronic Design Techniques and Analysis Required to Meet Electromagnetic Compatibility Requirements
May 6-7, 1992, Farmington Hills, MI
Advanced EMC Printed Circuit Board Design
May 8, 1992, Farmington Hills, MI
Information: JASTECH. Tel: (313) 553-4734.

ELINT Analysis
April 29-May 1, 1992, Washington, DC
ELINT/EW Applications of Digital Signal Processing
April 29-May 1, 1992, Washington, DC
ELINT Interception
March 16-18, 1992, Sunnyvale, CA
Electromagnetic Propagation
March 16-18, 1992, Sunnyvale, CA
Information: Research Associates of Syracuse, John Eckmair. Tel: (315) 455-7157.

The Smith Chart and Its Applications
March 16, 1992, San Diego, CA
Information: Besser Associates, Eva Koltai. Tel: (415) 949-3300. Fax: (415) 949-4400.

DSP Without Tears
March 24-26, 1992, Seattle, WA
May 13-15, 1992, Arlington, VA
Information: Z-Domain Technologies. Tel: (800) 967-5034. Fax: (404) 442-1210.

Introduction to EMI/EMC
May 4, 1992, King of Prussia, PA
Grounding, Bonding, and Shielding
May 5-6, 1992, King of Prussia, PA
Telecommunications EMI/EMC
May 7-8, 1992, King of Prussia, PA
Understanding and Applying MIL-STD-461C
May 11-13, 1992, King of Prussia, PA
EMP Design and Transient Testing
May 14-15, 1992, King of Prussia, PA
Information: R&B Enterprises, Bob Cytron. Tel: (215) 825-1960. Fax: (215) 834-7509.

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Model 710FC

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UP TO

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700LC	1.5W CW	.003-1000 MHz	33dB	25x28x13	3.3kg	100-240V	$ 1,695
704FC	4W CW	.5-1000 MHz	33dB	23x18x09	2.8kg	100-240V	$ 2,195
706FC	6W CW	.5-1000 MHz	36dB	25x28x13	3.3kg	100-240V	$ 3,195
410LC	10W CW	.006-400 MHz	43dB	30x35x13	4.5kg	100-240V	$ 4,600
710FC	10W CW	1-1000 MHz	40dB	30x35x13	7.3kg	100-240V	$ 6,695
727LC	10W CW	.006-1000 MHz	43dB	48x46x13	8.5kg	100-240V	$ 7,750
711FC	15W CW	400-1000 MHz	40dB	30x35x13	5.5kg	100-240V	$ 3,620
720FC	25W CW	400-1000 MHz	40dB	48x46x13	8.6kg	100-240V	$ 5,995
712FC	25W CW	200-1000 MHz	40dB	48x46x13	8.8kg	100-240V	$ 7,350
737LC	25W CW	.01-1000 MHz	45dB	48x46x13	10.5kg	100-240V	$ 9,995
747LC	50W CW	.01-1000 MHz	47dB	48x46x26	26.5kg	100-240V	$22,500
707FC	50W CW	450-1000 MHz	47dB	48x46x13	13.0kg	100-240V	$ 9,995
709FC	100W CW	500-1000 MHz	48dB	44x48x18	22.5kg	100-240V	$19,990
722FC	200W CW	500-1000 MHz	50dB	44x18x31	41.5kg	100-240V	$31,900

Note: Models 727LC, 737LC and 747LC consist of two bands with one common input and output connector, switched with coaxial transfer relay, manually, or by remote. Switching speed 5 milliseconds.

MODEL 704FC

MODEL 707FC

KALMUS
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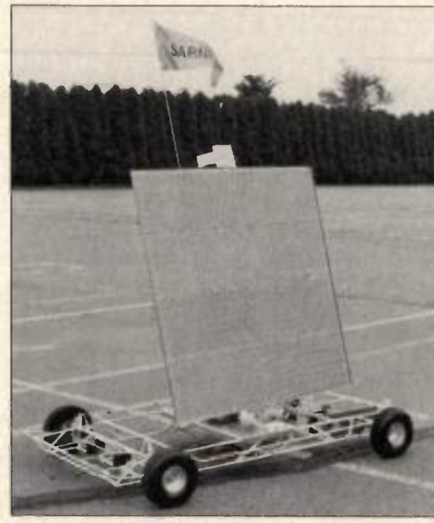
FAX: (206) 486-9657

INFO/CARD 13

Please see us at RF Expo West, Booths #415, 417.

Microwave-Powered Rover Developed

Researchers at the David Sarnoff Research Center have developed a rover that has the ability to receive microwave energy from a distant source and convert it into useful power for locomotion. This vehicle may be the precursor of future vehicles used for manufacturing on the moon. The ability to deliver power from point-to-point without wires will be a prime consideration of implementing a manufacturing station in space. This microwave-powered system avoids the necessity of expensive battery units, which are heavy to transport and require frequent re-charging.



The rover consists of a number of sub-systems. They are: a 1000 element rectifier antenna array operating at 5.8 GHz, a laser tracking system, a micro-wave tracking system, a high power transmitter system and a remote control system. The rover has a maneuvering radius of 200 feet from the remote control and the rectifier antenna is capable of 80 percent power conversion efficiency under closed conditions. For more information, please contact Public Affairs, David Sarnoff Research Center, CN 5300, Princeton, NJ 08543. Tel: (609) 734-2507.

Ham Radio Scholarships Available — The Foundation for Amateur Radio has announced plans to award forty-five scholarships for the academic year 1992-93 to assist licensed Radio Amateurs. Amateurs may compete for these awards if they plan to pursue a full-time course of studies beyond high school and are enrolled in or have been accepted for enrollment at an accredited university, college or technical school. The awards range from $500 to $2,000 with preference given in some cases to residents of specified geographical areas or the pursuit of certain study programs. Additional information and an application form can be requested by letter or QSL card, postmarked prior to May 31, 1992, from: FAR Scholarships, 6903 Rhode Island Avenue, College Park, MD 20740.

Quick Payback for Automatic Data Collection Systems — A recent survey by the Automatic Identification Manufacturers, Inc. reveals that automatic data collection systems fully pay for themselves in 6-12 months. The

survey drew responses from the following automatic data collection technologies: bar code, magnetic strip, voice data collection, optical character recognition, RF identification and RF data collection. RFID applications included systems for time and attendance and work-in-progress. Both types of RFID applications pay for themselves in 6 to 12 months and have an average cost from $11,000 to $25,000. RFDC applications included systems for inventory control, warehousing and distribution. Inventory control systems pay for themselves in 3 to 6 months with an average cost between $51,000 and $100,000. Warehousing and distribution systems also pay back in 6 to 12 months, but cost a bit more, between $101,000 and $400,000.

Oceanographic Probe Finds Dual Uses — A new probe, equipped with a microcomputer and designed to help oceanographers explore remote regions of the seas, may have a future as an environmental watch dog, guarding against illegal polluters. Sensors within the disposable probe could be designed to detect pollution in the water and pinpoint the location by signaling a satellite, which would relay the message to a monitoring station on land. The probe, developed by Battelle Marine Sciences Laboratory, weighs 5 pounds and is 32 inches in diameter. It is placed inside a shell carrier and can be dropped into the ocean from a ship or an airplane. Once in the water, the shell carrier opens, and the probe, weighted by an anchor, begins falling to the ocean floor. The probe is designed to measure such things as water temperature, conductivity and depth. At a predetermined time, the anchor wire is severed and the probe floats to the ocean surface where it transmits its data to a satellite. When used as a pollutant detector, the probe would detach from the anchor, float to the surface and send the information to the satellite.

On-Shore Flow Field Study Contract — Radian Corporation was recently awarded a $257,000 subcontract by Galson Corporation to provide remote atmospheric measurements using radar profiling and acoustic sounding equipment for an on-shore flow field study. To collect the atmospheric measurements, a Radian LAP™-3000 915 MHz Lower Atmospheric Radar Profiler will provide wind and temperature measurements up to about 3000 meters, while three Radian Echosonde® Doppler acoustic sounders monitor atmospheric mixing height conditions up to approximately 1000 meters. Radian's support during the field study includes equipment installation and maintenance, quality assurance, data processing and reporting.

ASTeX Acquires Assets of Gerling Labs — Applied Science and Technology recently announced that it has agreed in principle to acquire the assets of Gerling Laboratories. Gerling is a supplier of industrial microwave power supplies and components. Terms of the acquisition were not disclosed.

Low-Cost Radar Module Contract — Hughes Aircraft Company has delivered the first prototypes of a new unique,

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low-cost, highly reliable X-band active array radar module to the U.S. Air Force under a $13.3 million contract. The prototype modules, which are miniature radar transmitters/receivers that measure 3.82 inches long, 0.49 inches wide, and 0.21 inches high, use Hughes proprietary low temperature cofired ceramics and advanced chip mounting technologies.

Wiltron and Anritsu Merge Sales Organizations — Anritsu and Wiltron recently announced the formation of the Anritsu Measurement Instruments Division and the Wiltron Microwave Measurement Division. These divisions and the new sales organization comprise the Measurement Group. All existing Anritsu and Wiltron sales offices and entities will now become Anritsu Wiltron offices.

Grace Sells Japanese Microwave Business — W.R. Grace and Company has announced that it completed the sale of its microwave products business from its Japan Chemicals Division to E&C Engineering K.K. The transaction was valued at nearly $5 million. Completion of the sale is another step in Grace's plan to divest of non-strategic businesses while focusing on core business areas within specialty chemicals and health care.

Navy Awards Radar Measurement Contract — The U.S. Navy has awarded a $2.9 million contract to Flam & Russell for a mobile, fully polarimetric, frequency agile instrumentation radar capable of recording coherent radar reflectivity data while tracking airborne targets. A wide variety of test scenarios are supported. Frequencies may be randomly or uniformly stepped between 9.2 and 10.4 GHz. The pulse repetition frequency varies between 100 kHz at long ranges to near 300 kHz at short ranges. Data rates of up to 5 megabytes/second are supported. In addition to the radar data, the system also records IRIG time and selected radio conversations between pilots and system operators.

PTI Acquires Hughes Product Line — Piezo Technology has acquired, through license, the designs and manufacturing rights of the RF Circuits Product Line of the Hughes Aircraft Microelectronics Circuits Division. The products licensed include crystal filters and oscillators used on major programs such

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MODEL NUMBER	POWER Watts	GAIN dB	SUPPLY Volts	PRICE
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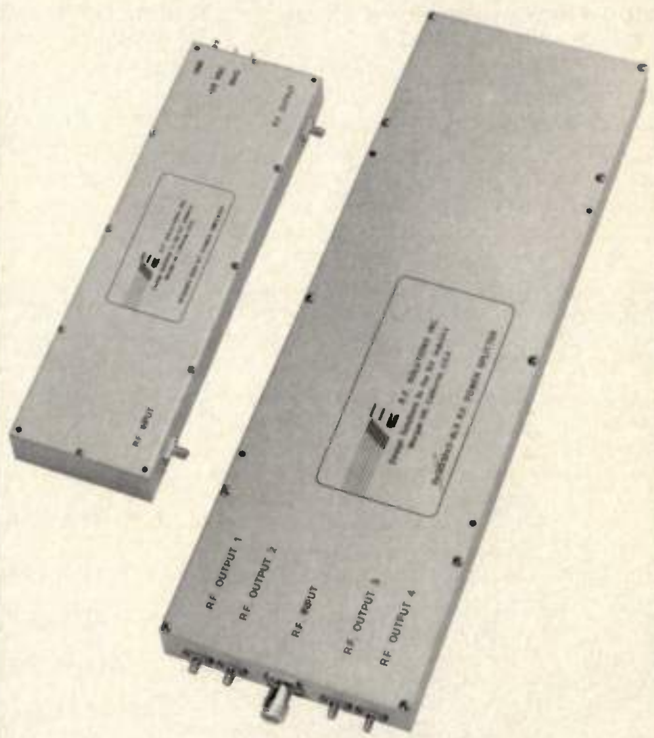
RFP0550-100	100	44	50	$2,100.00
RFP0550-1000	1000	16	50	$5,040.00
FREQUENCY RANGE 50 – 100 MHz				
RFP0800-100P50	50	30	50	$1,485.00
RFP0800-100P100	100	30	50	$1,660.00
RFP0800-100P200	200	30	50	$2,200.00
RFP800-100	600	16	50	$2,424.00
RFP01100-300	300	46	50	$3,150.00
FREQUENCY RANGE 76 – 108 MHz				
RFP0810-600	600	16	50	$1,780.00
FREQUENCY RANGE 75 – 150 MHz				
RFP0800-150P50	50	30	50	$1,485.00
RFP0800-150P100	100	30	50	$1,660.00
RFP0800-150P200	200	30	50	$2,200.00
RFP800-150	500	14	50	$2,424.00
FREQUENCY RANGE 100 – 200 MHz				
RFP0800-200P50	50	30	50	$1,660.00
RFP0800-200P100	100	30	50	$2,900.00
RFP800-200	400	13	50	$3,636.00
FREQUENCY RANGE 225 – 400 MHz				
RFP0204-4	4	20	28	$ 484.00
RFP0204-10	10	30	28	$ 685.00
RFP0204-25	25	30	28	$1,140.00
RFP0204-50	50	40	28	$1,695.00
RFP0204-100	100	40	28	$2,200.00
FREQUENCY RANGE 400 – 500 MHz				
RFP0405-4	4	20	28	$ 435.00
RFP0405-10	10	30	28	$ 616.00
RFP0405-25	25	30	28	$1,026.00
RFP0405-50	50	40	28	$1,525.50
RFP0405-100	100	40	28	$1,980.00
FREQUENCY RANGE 1 – 500 MHz				
RFP00105-4	4	20	28	$1,450.00
RFP00105-10	10	30	28	$2,300.00
RFP00105-25	25	30	28	$2,800.00
RFP00105-50	50	40	28	$3,752.00
RFP00105-100	100	40	28	$5,600.00
FREQUENCY RANGE 500 – 1000 MHz				
RFP0510-4	4	20	28	$2,610.00
RFP0510-10	10	30	40	$3,800.00
RFP0510-25	25	30	40	$4,900.00
RFP0510-50	50	40	40	$6,800.00
RFP0510-100	100	40	40	$9 800.00

STANDARD MODULES



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as the F-14 and F-15 radars, Phoenix missile, STAJ radio, Phalynx radar, and various space programs. PTI also purchased the tooling and equipment necessary for production and moved the operation to its Orlando, Florida location.

Teklogix and Exeter Form Alliance — Teklogix, Inc. and Exeter Software, Ltd. have entered a strategic alliance to co-market RF data communications solutions for distribution center operations. The agreement calls for Teklogix to supply all RF hardware, with Exeter providing the necessary software.

Daico Receives Radar Contract — Daico Industries recently received a $2.4 million contract for Phased Array Radar Multifunction Modules. The modules include Steerable Phase Shifters, Transmit/Receive Switches and Low Noise GaAs FET Amplifiers.

Analog Devices Wins SDI Contract — Analog Devices has announced that it has been awarded a five-year, $9 million contract by the U.S. Army Strategic Defense Command for the development of two radiation-hardened mixed-signal integrated circuits. Under this contract, Analog will develop two ultra-high-performance monolithic analog-to-digital converters, including a low power 10-bit 1-MSPS converter and a highly integrated 12-bit 10-MSPS converter.

TI Places Order with EEsof — EEsof Inc. recently announced a major sale of its electronic-design automation software tools to Texas Instruments Defense Systems & Electronics Group. TI has selected EEsof as their primary vendor for EDA engineering tools to be used in the design of MMIC and hybrid MIC devices. All products in this more than $700,000 contract were shipped in 1991.

CAD Software Changes Name — Effective January 1, CAD Software, Inc has changed its name to PADS Software, Inc. The reason for the name change is to create market awareness and association with the company's PADS product line of EDA tools.

Ancom Now Offering Susceptibility and Immunity Testing — Ancom Electromagnetics Ltd. recently acquired test instruments that allow them to perform fully automated radiated susceptibility and immunity tests of small and large equipment. ANCOM's facilities comprise a certified TEMPEST Test lab, and also offers the full complement of MIL-STD-461 EMI tests.

ARCO Electronics Acquires Microelectronics — Arco Electronics Control recently announced the acquisition of Microelectronics Ltd. in Israel. Microelectronics is a manufacturer of glass, air and porcelain capacitors.

Amador and German VDE Announce Arrangement — Amador Corporation and the German VDE Testing and Certification Institute have announced a new cooperative arrangement for the testing of information technology equipment to product laws of the German government. Under the new arrangement, Amador will now be able to test to German standards without a German engineer present to approve the testing process. Products can then be shipped to Germany with the appropriate approvals already in place.

Scientific Atlanta to Upgrade EUROVISION Network — Scientific Atlanta has been selected by six member countries in the European Broadcasting Union (EBU) to design, manufacture, supply and install the digital/analog earth stations and other equipment needed to upgrade the EUROVISION television network. Scientific-Atlanta will provide the EBU member in each country with large Ku-band uplink stations, ranging in size from seven to nine meters, as well as converters, modulators, amplifiers and computerized control equipment.

Tops in RF Power Modules

In the early 1980's, Motorola pioneered modules for the then-new 900 MHz cellular systems, both in the USA (AMPS) and in Europe (NMT). Motorola was the first company to offer modules for mobile and portable *cellular* radios.

Now...on to greater heights!

Motorola is FIRST again, with a complete line of quasi-linear modules for GSM *digital* cellular—both portables and mobile radios.

Supplier of choice.

Talk about selection! Motorola has a module to fit most cellular radios, each with specified performance limits for those critical parameters needed in today's competitive cellular radio marketplace. These compact modules offer small and less complex system designs, as well as savings in time and overall cost. And like all mobile communications RF products that carry the Motorola name, our newest modules meet rigid standards for physical and electrical characteristics even in extreme operating conditions.

Modules for GSM f = 890 to 915MHZ

Model	P_o Watts	P_{in} m Watts	V_{cc} Volts	Size Package Type Inches
PORTABLES				
MHW903	3	1	7.2	.55 x 1.30 (Surface mount)
MHW953	3	1	7.2	.55 x 1.77 (flange)
MHW904	3	100	7.2	(flange)
MHW909	9	100	7.2	.55 x 1.98 (flange)
MOBILES				
MHW912	12	1	12.5	.55 x 2.39 (flange)
MHW914	14	1	12.5	.55 x 2.39 (flange)
MHW915	14	100	12.5	.55 x 1.98 (flange)
MHW932	32	100	12.5	.81 x 2.65 (flange)

Production is the name of the game.

Whether you need tens, hundreds or thousands of modules, Motorola offers you repeatable performance from unit to unit.

Plus the best quality, delivery and service in the industry.

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PSG1000

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352C

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	PSG1000 Synthesized Signal Generator	AMM2000 Automatic Modulation Meter	352C Spectrum Analyzer
Parameters	10 KHz – 1 GHz Carrier Frequency 10 Hz – 9.99 KHz Synthesized AF + 13 dBm RF Output	250 KHz – 2.4 GHz Carrier Frequency DC/10 Hz – 300 KHz Modulation Rate ± 500 KHz Peak Deviation	300 KHz – 1 GHz Frequency Range 9 KHz – 2 MHz Bandwidth - 100 to +10 dBm Range
Features	AM, FM, PM DC – FM Sinad Meter	AM, FM, PM Low FM Noise AC/DC Operation	AM, FM, Demod Portable AC/DC Operation
Interfaces	IEEE-488 (standard)	IEEE-488 (standard)	Printer (optional)

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... the PSG1000 Signal Generator operates from 10 KHz to 1 GHz with AM, FM, PM, and optional Pulse, plus an audio synthesizer (10 Hz to 9.999 KHz). The PSG1000 features a built-in, automatic SINAD Meter and external DC coupling for AM/FM testing of digital pagers.

For modulation analysis ...
... the AMM2000 Automatic Modulation Meter delivers outstanding versatility and performance with signals from 250 KHz to 2.4 GHz. The AMM2000, designed for lab or field use, offers 1% accuracy for AM/FM/PM, and measures RF and audio frequency/level.

For EMC applications ...
... the 352C Spectrum Analyzer is a low-cost, highly sensitive instrument for lab and field use. With a resolution bandwidth of 9 KHz to 2 MHz, the 352C is ideal for monitoring spurious EMI radiation in the range of 300 KHz to 1 GHz. The 352C features a printer option for permanent four-color records.

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Test Equipment Makers Deliver Cost, Precision and Power

By Gary A. Breed
Editor

The makers of electronic test equipment for the design, manufacture and service of RF products have been working at a feverish pace for the last couple of years. As new RF applications and new methods for their implementation have been developed, test instruments have to be created or adapted to fill specific needs.

Three clear directions can be seen in the recent development of RF test equipment — greater precision in the best instruments, new attention to lower cost instruments, and greater computing power in all instruments.

Computing Power

The personal computer boom has helped drive the cost of processing and control to a minimum, both with microprocessors inside the instruments, and ready availability of PCs for control, data collection, and analysis. Some instruments actually use PC processors. The most recent spectrum analyzer from IFR has what is basically a '386SX and VGA monitor for operation and display. Many recent Hewlett-Packard instruments include an optional keyboard to gain access to their MS-DOS compatible CPUs.

The other advantage of computing power is control of operating functions through software rather than via front panel controls. The ergonomics of such operation is a difficult task — just a few years ago, instruments without traditional front panel controls were often very non-intuitive, requiring hours with an instruction manual before attempting routine operations. Fortunately, this problem was addressed quickly, and the method of using function keys ("soft keys") and well-organized menus has become accepted.

Of course, computation power can be applied to the measurements without requiring an external computer. This makes it possible for extensive markers, performance limits, unique sweep requirements and multi-color displays to be implemented without major changes to the basic instrumentation hardware. The new Wiltron 360B is a major upgrade to the venerable Model 360, with may new features that have been implemented primarily in software.

There are additional computations that provide new insight into circuit operation while under test, such as averaging, mean and deviation, or comparison to standard reference data. New instruments are available that are based on digital computations, like wave analyzers from Stanford Research and Analogic that create extremely high resolution frequency, time and amplitude analysis by means of fast Fourier transforms (FFT), correlation or convolution.

High End Precision

The simple explanation of this aspect of development is that maximum performance will always be a goal of instrument makers. But there is more to the story right now. Precision timekeeping is required for GPS and very high rate data transmission. Precise characterization of components is required to provide accurate models for new, powerful circuit synthesis and analysis software tools. The Microwave Landing System, wind-shear detection radar, and fiber-optic communications systems are among applications which need high precision measurements in their development and maintenance.

In some cases, instrument performance creates its own market. For example, Keithley Instruments Division recently introduced a new line of function generators which use direct digital synthesis (DDS) for high resolution and precise waveform control. Gary Pinkerton, Director of Marketing at Keithley, says, "I'm surprised at the predominance of phase performance demands," referring to vibration analysis and ultrasonic applications that require multiple waveforms with tight synchronization.

Going for Low Cost

Increased attention to competitive product development and manufacturing is another major force driving the test equipment market. Greater capability in production testing lets a company ship a product sooner, with greater confidence in its performance. But, in order to put better instruments on the production line, the cost had to come down. As a result, new signal generators from Fluke, Panasonic, Marconi, Leader and others; sweep systems and scalar analyzers from Wavetek, Wiltron and Hewlett-Packard; and spectrum analyzers at new low prices from Tektronix, Anritsu and Advantest have been targeted at production line customers.

A new type of instrument has shown up at the very low end of the price spectrum. Signal generators, power meters, frequency counters, oscilloscopes, and even spectrum analyzers can be purchased at prices that were not imaginable just five years ago. Many of the manufacturers have been known for "TV service bench" test equipment, and a few are not names that have been associated with instruments at all — B&K Precision, Protek, Hameg, Hitachi, Panasonic, Kenwood, Optoelectronics and Global Specialties, to name a just a few.

These instruments are products of rapidly advancing component technology, with many adapting devices intended for consumer products, cellular systems, and other large-scale applications. These products represent useful RF test equipment at very low prices for users who understand and accept their performance limitations.

Summary

The high pace of activity among test equipment manufacturers is a result of a jump in customer demand for new applications and new price/performance needs. This activity also seems to have considerable inertia, with newly-developed techniques being transferred to existing products, or leading to additional new products. As a result, RF engineers have a greater range of test products to choose for their labs, production lines and service benches. **RF**

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An Exact Method For Impedance-Matching With Short Transmission Lines

By Douglas B. Miron
South Dakota State University

For the impedance-matching problem, most of the emphasis in microwave books is on broadband (multi-octave) networks. In practice, there are a great many design problems that don't require more than 10-20 percent bandwidth, and for which space is a primary consideration. This article presents a method for designing short-line matching networks that gives an exact match at the design center frequency.

At frequencies higher than 1 GHz, lumped capacitors and inductors are generally not available, although there is a transition region in which a limited range of values are available. In the range from 400 MHz to 2 GHz, the designer has a choice of using lumped-element circuits, transmission-line networks, or a mix. Simple networks made up to approximately imitate the lumped-element L-section (1) with short sections of transmission line (2,3) have frequently been used. The range of validity of the short-line approximations is quite limited, so the quality of the match for such designs is often less than acceptable. The method described here produces an all-cascade (no stubs) solution, and will match complex loads and sources.

Because of the periodic nature of the impedance and transfer functions of transmission lines, these networks must be approached with caution. Designs should be examined for spurious responses in the stopbands and be compensated (4-6) or adjusted (2,3) on the basis of analysis programs taking junction discontinuities into account. The plots given in the following sections are for lossless lines, without discontinuity effects.

Basic Equations

A section of transmission line transforms an impedance at one end, Z_L, to another value, Z_{in}, at the other end, according to the equation:

$$Z_{in} = Z_o \frac{Z_L + jZ_o \tan(\beta d)}{Z_o + jZ_L \tan(\beta d)} \qquad (1)$$

in which Z_o is the wave (or characteristic) impedance of the line, $\beta = \omega/v$, ω being the radian frequency of the signal, v the wave speed on the line, and d is the line length. In this article I will let v=c=300 Mm/s so that values for d will be air-speed values. Equation 1 is the basic equation from which the design results of all the following sections are derived, and also the equation to be used for the frequency-response calculations in conjunction with the normalized power given by:

$$P_{norm} = \frac{4R_s R_N}{(R_s + R_N)^2 + X_N^2} \qquad (2)$$

See Figure 1 for the defining circuits.

At a fixed frequency, the designer has two free parameters, the wave impedance, Z_o, and the length d, so that any pair of complex impedances can be matched. To match $R_1 + jX_1$ to $R_2 + jX_2$, let $Z_{in} = R_1 - jX_1$, $Z_L = R_2 + jX_2$, and $U = \tan(\beta_o d)$. By separating real and imaginary parts, one gets two equations for the unknowns Z_o and U which can be solved to give:

$$Z_o^2 = R_1R_2 + X_1X_2 - \frac{X_1 + X_2}{R_1 - R_2}(R_1X_2 - X_1R_2) \qquad (3)$$

$$U = \frac{R_1 - R_2}{R_1X_2 - X_1R_2} Z_o \qquad (4)$$

Some solutions are not physically realizable because Z_o must be positive and real.

A case of special interest is $X_1 = 0$; conversion of a complex load to a real one.

$$Z_o^2 = R_1R_2 - \frac{R_1X_2^2}{R_1 - R_2} \qquad (5)$$

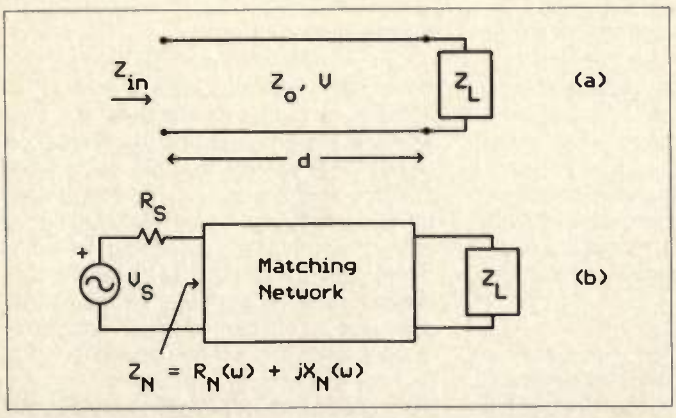


Figure 1. Defining schematics for, a) a transmission line section, b) normalized power.

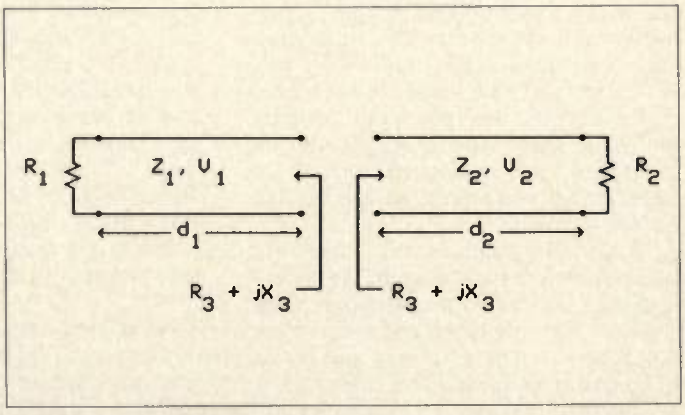


Figure 2. Schematic for the two-line impedance-matching problem.

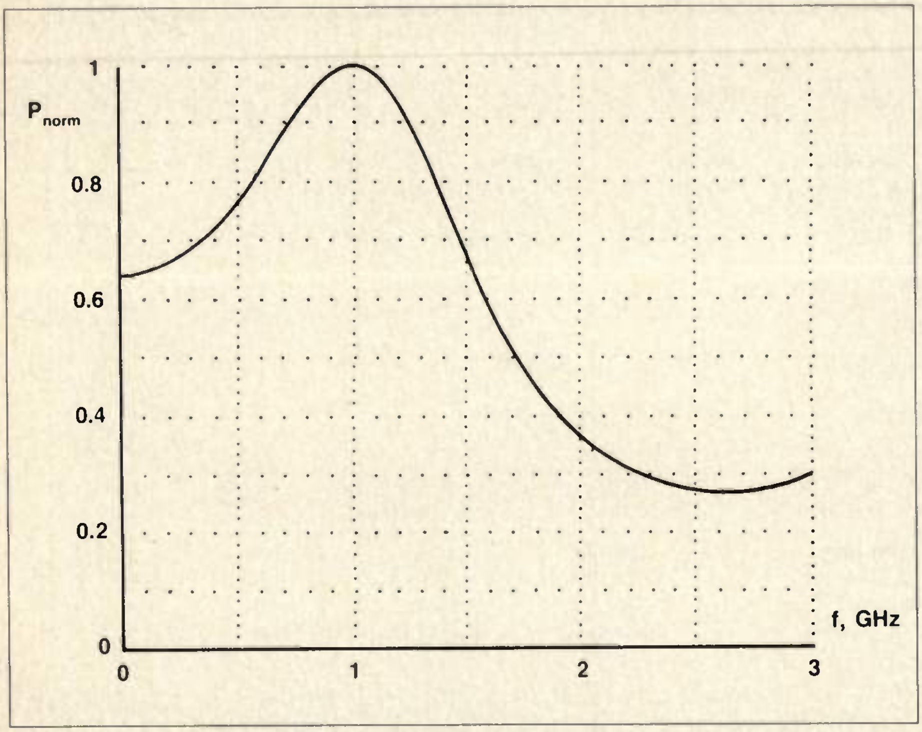


Figure 3. Normalized power transfer for Example 1.

$$U = \frac{R_1 - R_2}{R_1 X_2} Z_o \qquad (6)$$

If X_2=0 also, we have the quarter-wave transformer case for which equation 5 reduces to:

$$Z_o = Z_q = \sqrt{R_1 R_2} \qquad (7)$$

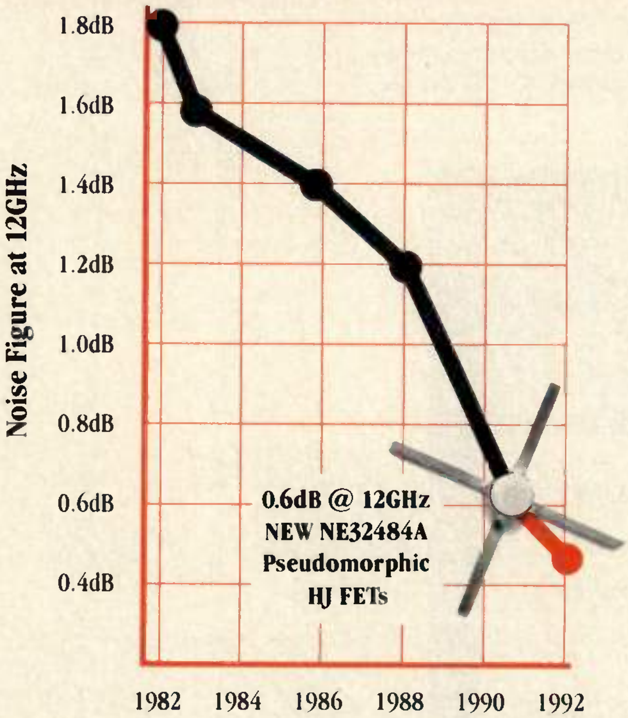
This is an important limiting value for the two-line solution given below.

The Exact Solution for Resistive Terminations

With two lines in cascade, there are four free parameters, the two wave impedances and the two line lengths. To match the resistance ratio and center frequency, we only need two.

From the experience with the approximate solution, we know that the wave impedance values should be the two extremes allowed by the fabrication technology in order to get the shortest total line length. This leaves the line lengths as the two free parameters for design. At the junction of the two lines the impedances looking each way must be complex conjugates, as shown in

Snow Removal Devices



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NE76084	12	1.6	9.0
NE76038	4	0.8	13.0
NE76184A	4	0.8	12.0

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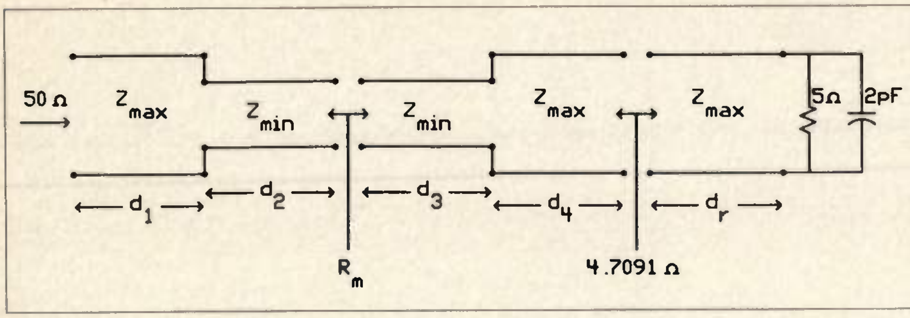

Figure 4. Schematic for Example 2. Starting from the right, the design proceeds by resonating the load with the line d_r, then steps up the impedance to R_m through d_3 and d_4, then steps it down to 50 ohms through d_1 and d_2.

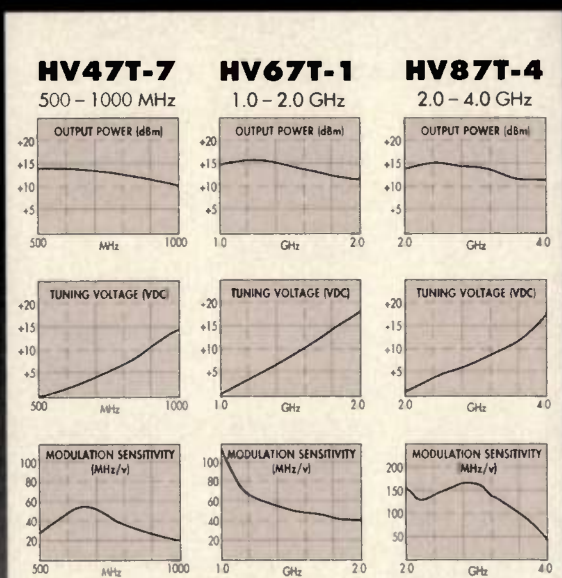

Figure 2. Writing the equations for these impedances, with $U_j = \tan\beta_o d_j$, sweating through some algebra using symmetry and ratios, leads to a quadratic equation which only has one physically-realizable solution. The solutions are expressed as follows. The conditions are:

$$R_1 > R_2,\ Z_1 = Z_{omin},\ Z_2 = Z_{oMAX},\ Z_1 < Z_q < Z_2 \tag{8}$$

Define,

$$A_1 = \frac{R_1 Z_2^2}{R_2 Z_1} - Z_1 > 0 \tag{9}$$

$$A_2 = Z_1\left(\frac{R_2}{R_1} - 1\right) < 0 \tag{10}$$

$$B_1 = \frac{R_2 Z_1^2}{R_1 Z_2} - Z_2 < 0 \tag{11}$$

$$B_2 = Z_2\left(\frac{R_1}{R_2} - 1\right) > 0 \tag{12}$$

$$C_1 = Z_1\left(\frac{Z_2}{R_1} - \frac{R_2}{Z_2}\right) > 0 \tag{13}$$

$$C_2 = Z_2\left(\frac{Z_1}{R_2} - \frac{R_1}{Z_1}\right) < 0 \tag{14}$$

$$D = R_1 + R_2 - \frac{Z_1^2}{R_1} - \frac{Z_2^2}{R_2} \tag{15}$$

$$K = \frac{1}{2C_1}\left(D + \sqrt{D^2 - 4C_1C_2}\right) > 0 \tag{16}$$

The inequalities are given as a check for testing your calculations or program. From these intermediate values the solution for the line lengths is:

$$U_1 = \sqrt{\frac{\frac{B_2}{K} - A_2}{A_1 - B_1 K}},\quad U_2 = KU_1 \tag{17}$$

Rizzi (Reference 3, p. 136) has another version of these results.

Example 1 — A 4:1 Impedance Transformer

Let R_1=200, R_2=50, Z_1=20 and Z_2=120, all in ohms. Let f_o=1 GHz, $\lambda_o = c/f_o = 0.3$, and m=300 mm. The calculations proceed from the above equations:

$A_1 = 2860$
$A_2 = -15$
$B_1 = -119.17$
$B_2 = 360$
$C_1 = 3.6667$
$C_2 = -1152$
$D = -40$
$K = 13.091$

The air-speed lengths are,

$d_1 = 0.015557\lambda_o = 4.6667$ mm for the 20 ohm line

$d_2 = 0.14467\lambda_o = 43.401$ mm for the 120 ohm line

Note that the total length is 48.07 mm while the quarter-wave transformer solution is 75 mm of 100 ohm line. Figure 3 shows the power curve for this solution.

Resonating the Load with a Short Line

Equations 5 and 6 give a solution for a cascade line which converts a complex load to a real one. If one chooses the wave impedance and asks what is the shortest line length needed to produce an unspecified real input resistance, the result can be very similar to series-resonating a capacitive load or parallel-resonating an inductive load. These thoughts imply solving equation 5 for R_1. The solution is,

$$R_1 = \frac{1}{2R_2}\left[R_2^2 + X_2^2 + Z_o^2 \pm \sqrt{(R_2^2 - Z_o^2)^2 + 2X_2^2(R_2^2 + Z_o^2) + X_2^4}\right] \tag{18}$$

Equation 6 still applies for U.

$$U = \frac{R_1 - R_2}{R_1 X_2} Z_o \tag{19}$$

Since there are two possible values for R_1, one must test to see which produces the smallest positive value of U that will represent the shortest line.

Example 2 — Short-Line Solution to a Complex Low Impedance Load Problem

Consider a load consisting of 5 ohms in parallel with 2 pF. f_o=3.95 GHz, and λ_o=75.949 mm, the center of the lower satellite TV band. I will assume microstrip on alumina allows Z_{min}=18 ohms and Z_{max}=91 ohms. Since the load is capacitive, we can try resonating it with a high-impedance line section, imitating series inductance. To use equations 18 and 19, the series equivalent values of the load are R_2=4.7099 and X_2=−1.1689. Choosing Z_o=91 gives R_1=4.7091 and a line length d_r=0.15568 mm.

We now have a real resistance, which I shall call R_2 to match the notation of the last section, of about 4.7 ohms which we want to match to 50 ohms, which I shall now call R_1. The quarter-wave impedance value is,

$$Z_q = \sqrt{50 \times 4.7091} = 15.345 \text{ ohms} \tag{20}$$

and is less than Z_{min}. A possible solution to this problem is to step up to a value higher than 50 ohms with one two-line

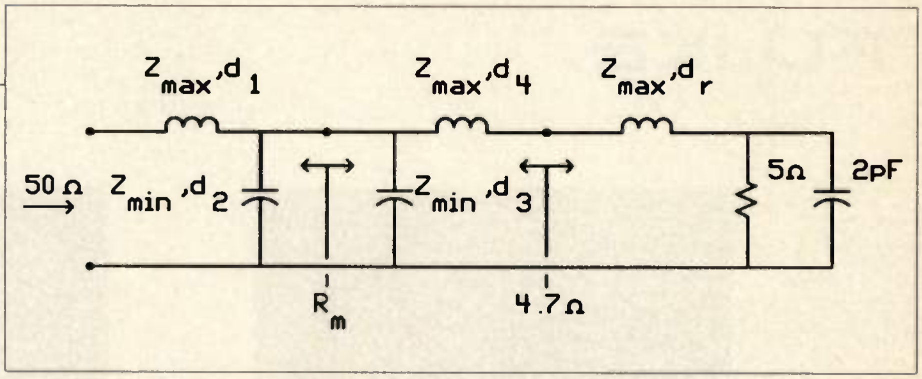

Figure 5. Lumped-element analogy to Figure 4.

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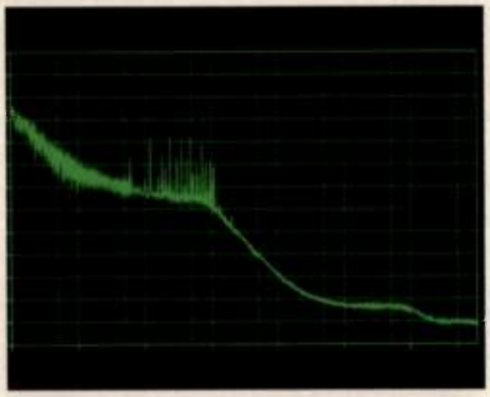

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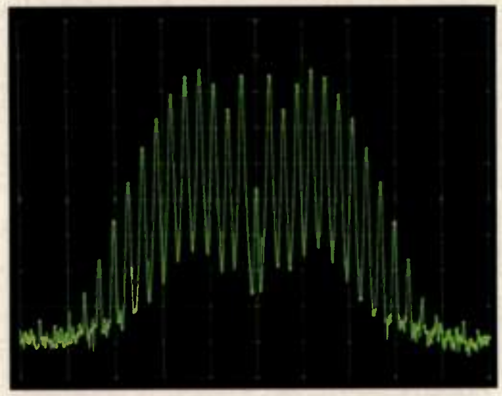

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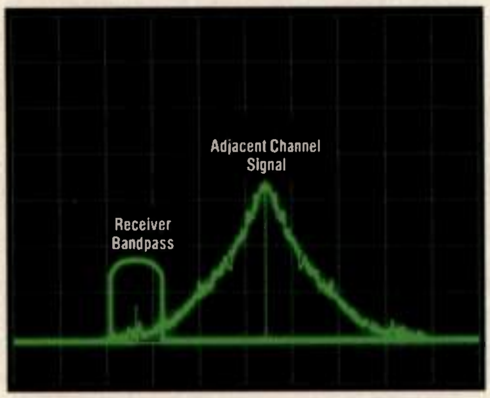

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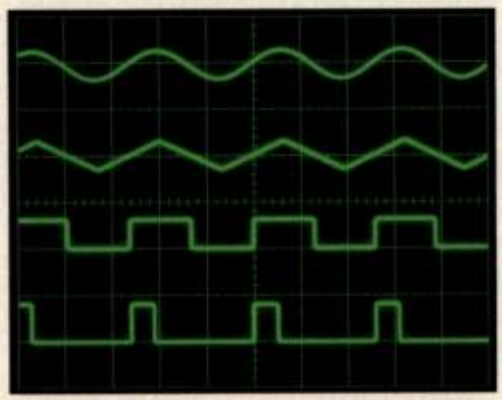

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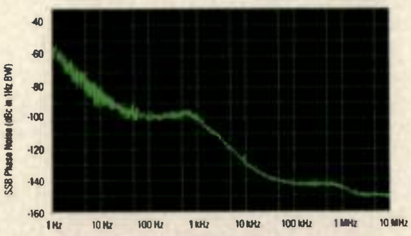

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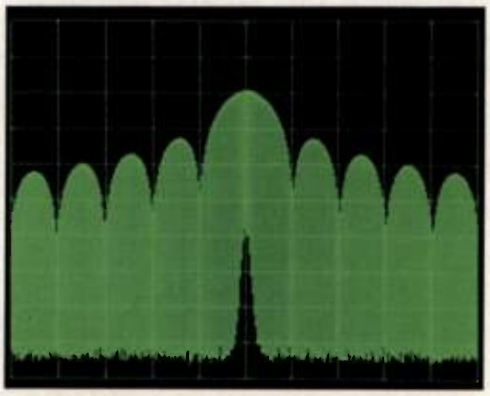

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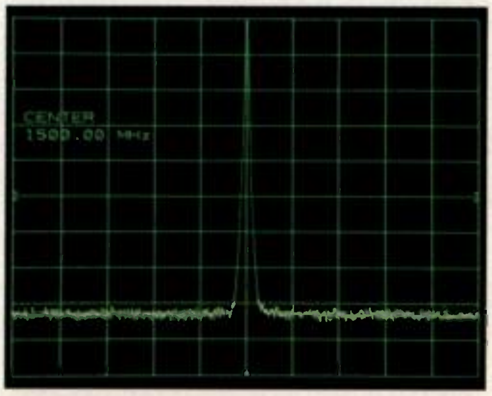

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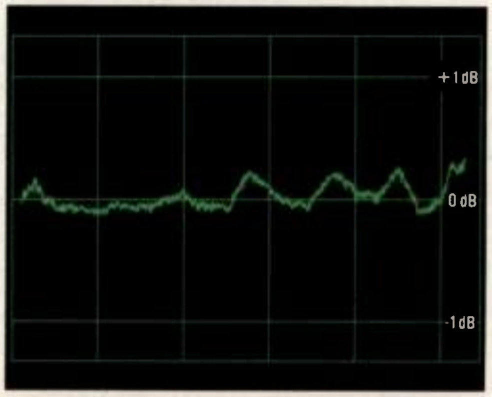

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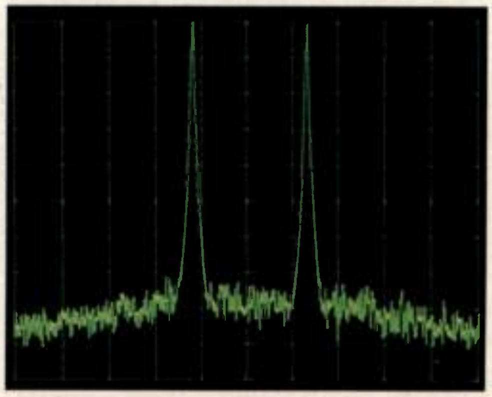

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ct wave, dude.

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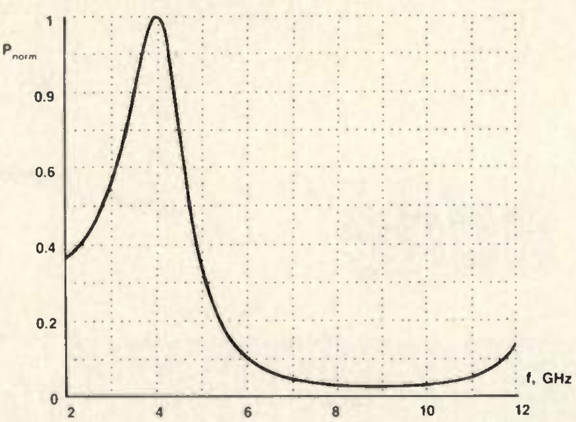

Figure 6. Normalized power transfer for the system of Example 2 and Figure 4.

network and then step down again to 50 ohms with another two-line network. Call this intermediate match value R_m. R_m must be high enough so that the quarter-wave impedance value on the R_2 side is greater than 18 ohms, but not so high that the quarter-wave impedance value on the R_1 side exceeds 91 ohms. These conditions are expressed as:

$$R_m > \frac{Z^2_{min}}{R_2} \tag{21}$$

$$R_m < \frac{Z^2_{MAX}}{R_1} \tag{22}$$

For the present case, the limits on R_m are 68.803 and 165.62 ohms. As one approaches either limit, one of the line sections approaches a quarter wavelength, so to achieve the best balance in the two designs I choose the geometric mean of the two limits, R_m=106.75 ohms. Figure 4 shows the line layout for this solution. The lumped-element analogies to the short-line sections are shown in Figure 5. Familiarity with the lumped-element design process gives us both a guide for choosing the structure of a short-line solution and a handle on the behavior of such a structure when we meet it. From equations 9-17, the lengths are shown in Table 1.

Adjacent sections of the same wave impedance can be combined, so that the 18 ohm middle is d_2+d_3=11.3 mm and d_4+d_r=1.9335 mm. The total air-speed length is 23.485 mm. Figure 6 shows the power response. The solution is a bit longer that $\lambda_o/4$. A quarter-wave-and-stub system is about the same length, and a single-stub solution using Z_{max} for the cascade line and Z_{min} for an open stub at the source end is shorter. However, compensation of cascade line junctions (5) can be more precise than stub junctions (6). This example has shown that a cascade combination of lines can be used to match, in theory, any load to any source using the equations 9-19 and inequalities 8, 21 and 22. However, technology limits can still prevent a realizable solution. For example, if C=20 pF, you will find the resonated impedance too low to find an R_m to satisfy inequalities in equations 21 and 22.

Conclusion

In general there is no best solution to all matching problems. The designer should try alternatives, find the board layout size, frequency response, and manufacturing cost of each before making a choice. The exact short-line solutions and the structure-by-lumped-element-analogy method presented in this article extends the range of possible transmission line solutions for moderate bandwidth problems. ***RF***

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About the Author

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Nonlinear Model Verification For a Medium Power Bipolar Transistor

By Lynne Olsen and Brian M. Kirk
California Eastern Laboratories, Inc.

Models are the basic building blocks for simulating a circuit. Benefits of accurate circuit simulation include reduced time to market because circuits work the first time or require minimal tuning. Reduced fabrication, test and rework costs are also realized. Since simulation results are dependent on the models used, it is important to know how accurate they are. This article presents the methods used at California Eastern Laboratories to develop a nonlinear bipolar transistor model and verify its accuracy.

Ideally, the designer would like the device manufacturer to provide a nonlinear BJT model that can be used for all frequencies, bias conditions and applications, and be compatible with the simulator the engineer is using. Unfortunately, such a model does not exist, although a model can be developed for a narrow bias and frequency range that will fit the actual device with 2 percent or less error. The efforts at CEL focus on providing a model that will simulate the actual device over the widest bias and frequency range possible without sacrificing accuracy. If necessary, more than one model is generated to accurately characterize a device.

Once you have a model, how do you know how good or accurate it is? With no established industry standard for nonlinear model accuracy, this article describes how CEL determines a model's accuracy. Models developed for the NE46100 and the NE46134 are evluated. Actually, only one nonlinear model is developed, a model of the chip (NE46100). The package model (NE46134) then consists of the nonlinear chip model embedded in the 34 package model. For completeness, validation of both the chip and the chip-in-package is presented.

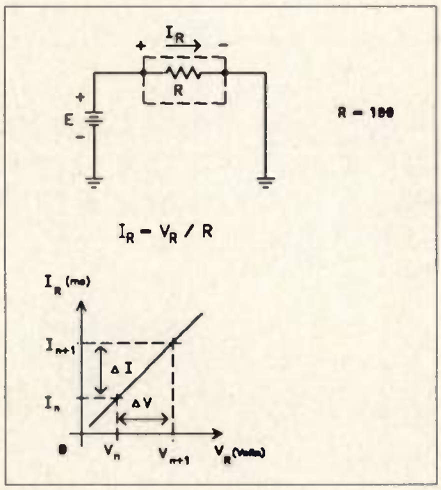

Figure 1. Linear model.

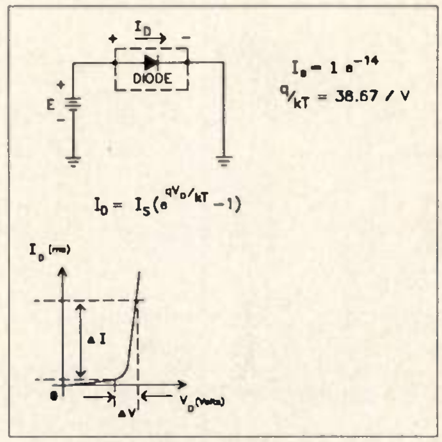

Figure 2. Nonlinear model.

The first comprehensive and publicly available nonlinear simulator was SPICE (Simulation Program with Integrated Circuit Emphasis), developed at the University of California, Berkeley in the late 1960s and early 1970s (1). This simulator incorporated a nonlinear BJT model referred to as the Gummel-Poon model (2). SPICE provides the benefits of simulating and evaluating time domain waveforms, power transfer curves, intermodulation products, harmonics and other non-linear responses. SPICE has only recently become popular within the RF and microwave community. In the past few years, nonlinear simulators have become much more affordable, easier to use and the required hardware has dropped tremendously in price.

Linear Versus Nonlinear Models

To use a non-linear simulator, it is necessary to become familiar with non-

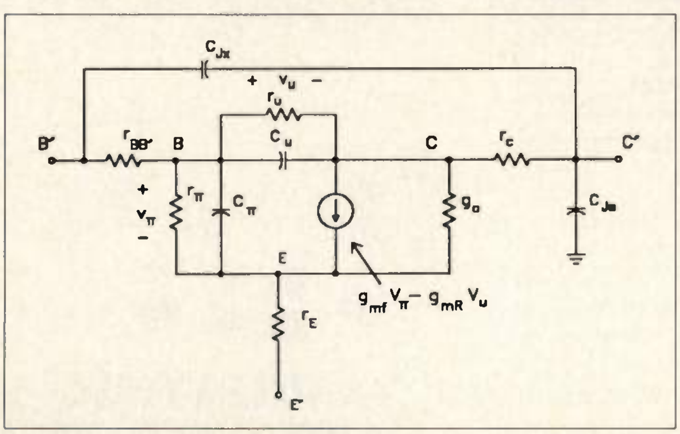

Figure 3. Linear BJT model.

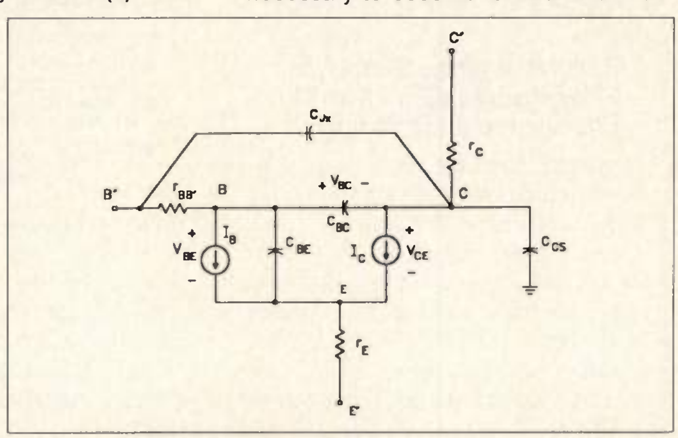

Figure 4. Nonlinear BJT model.

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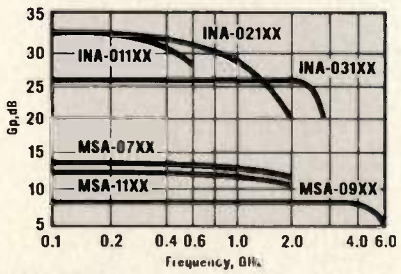

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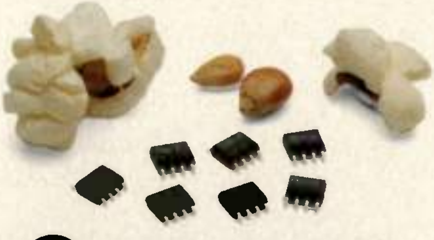

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linear models. Simply stated, a nonlinear model is capable of calculating nonlinear relationships.

We all know that the voltage drop across a resistor (V_R) is related to the current flowing through it (I_R) such that, if the voltage increases by a factor of 2, the current also increases by a factor of 2. This is a linear relationship because a proportional change in voltage yields a proportional change in current. This relationship is illustrated in Figure 1.

To understand a nonlinear relationship, consider an ideal diode and the relationship of the current flowing through the diode (I_D) with respect to the voltage applied across the diode (V_D). By inspection of the graph in Figure 2 we can see that I_D and V_D are not linearly related. By calculation we find that the current through the diode with V_D=0.4 V is $I_D=52\times10^{-9}$ amps and when V_D increases 13 percent to 0.45 V, I_D increases almost 600 percent to $I_D=361\times10^{-9}$ amps. Since the current flowing through the diode does not have a linear relationship to the applied voltage (the relationship is exponential), the diode

PARAMETER	DESCRIPTION	DEFAULT VALUE
IS	Saturation current	1e-16
BF	Ideal maximum forward Beta	100
NF	Forward current emission coefficient	1.0
NE	Base-emitter Leakage emission coefficient	1.5
ISE	Base-emitter Leakage saturation coefficient	0
VAF	Forward early voltage	infinity
IKF	High current Beta roll-off	infinity
TF	Ideal forward transit time	0
XTF	Coefficient for bias dependence of TF	0
VTF	Voltage describing VBC dependence of TF	infinity
ITF	High current parameter for RF	0
PTF	Excess phase at f_{tau}	9
XTB	Forward and reverse Beta TC	
BR	Ideal maximum reverse Beta	1
ISC	Base-collector Leakage saturation current	0
NC	Base-collector Leakage emission	2
VAR	Reverse early voltage	infinity
IKR	High current reverse Beta roll-off	infinity
NR	Reverse current emission coefficient	1
TR	Ideal reverse transit time	0
EG	Energy gap for temperature effectIS	1.11
XTI	Temperature exponent for effect on IS	3
CJC	Base-collector zero-bias depletion capacitance	0
VJC	Base-collector built in potential	.75
MJC	Base-collector junction exponential factor	.33
XCJC	Fraction of CJC connected to internal abse node	1
FC	Coefficient for forward-depletion capacitance	0.5
CJE	Base-emitter zero-bias depletion capacitance	0
VJE	Base-emitter built in potential	.75
MJE	Base-emitter junction exponential factor	.33
CJS	Zero-bias collector-substrate capacitance	0
VJS	Substrate junction built-in potential	.75
MJS	Substrate junction exponential factor	0
RB	Zero-bias base resistance	0
RBM	Minimum base resistance	RB
IRB	Current where RB falls to half minimum	infinity
RE	Emitter series resistance	0
RC	Collector series resistance	0
KF	Flicker noise coefficient	0
AF	Flicker noise exponent	1

Table 1. Gummel-Poon parameters.

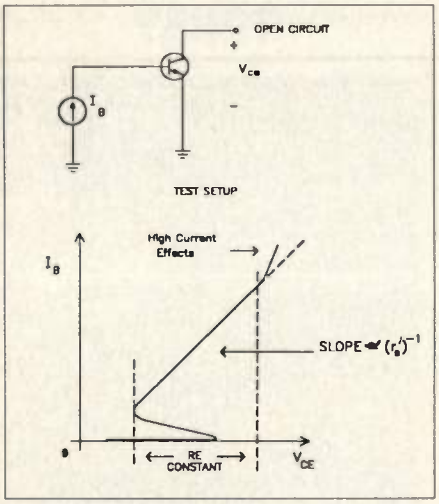


Figure 5. R_E **evaluation.**

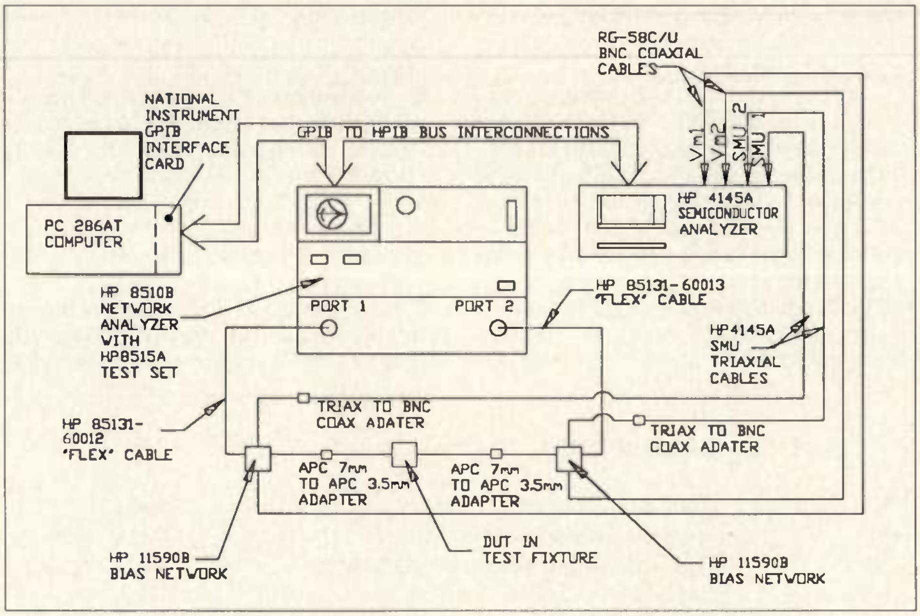


Figure 6. Test setup.

requires a nonlinear model.

From the equations in Figures 1 and 2 it becomes apparent that the equation used to represent the nonlinear response (I_D) is more complex and will generally take longer to solve than the linear equation used to represent I_R in Figure 1. The added complexity of non-linear models is one of the reasons nonlinear simulators have been slower than linear simulators. Another more significant contributor to slow analysis times is the solving of integral-differential equations to sum voltages and

V_{CE} = 10 V, I_C = 50 mA

FREQ (MHz)	S_{11} MAG	S_{11} ANG	S_{21} MAG	S_{21} ANG	S_{12} MAG	S_{12} ANG	S_{22} MAG	S_{22} ANG	K	MAG (dB)
100	0.780	-132	28.079	115	0.029	46	0.548	-99	0.21	29.8
200	0.809	-156	15.218	100	0.033	29	0.425	-131	0.34	26.7
500	0.819	-175	6.206	85	0.041	34	0.387	-159	0.70	21.8
800	0.817	177	3.888	76	0.048	42	0.386	-168	0.96	19.4
1000	0.821	174	3.136	71	0.060	48	0.385	-170	97	17.2
1200	0.821	171	2.596	67	0.063	47	0.388	-173	1.07	14.5
1400	0.814	168	2.236	62	0.068	53	0.394	-174	1.19	12.6
1600	0.819	165	1.976	58	0.075	50	0.401	-176	1.17	11.7
1800	0.816	162	1.769	53	0.084	51	0.413	-178	1.17	10.7
2000	0.819	160	1.565	49	0.094	49	0.416	-179	1.15	9.8
2500	0.815	154	1.290	39	0.116	51	0.439	178	1.14	8.2
3000	0.814	148	1.072	30	0.128	46	0.468	175	1.18	6.7
3500	0.819	143	0.920	22	0.150	44	0.488	173	1.12	5.8
4000	0.806	137	0.803	13	0.168	40	0.519	168	1.14	4.5

Note: S-Parameters include Bond wires

Base	Total 1 wire, 1 per Bond Pad, 0.0259" (658 µm) long each wire
Collector	Total 1 wire, 1 per Bond Pad, 0.0182" (463 µm) long each wire.
Emitter	Total 2 wires, 1 per side, 0.0224" (569 µm) long each wire
Wire	0.0007" (17.8 µm) dia., gold

Figure 7. Part of NE46100 data sheet.

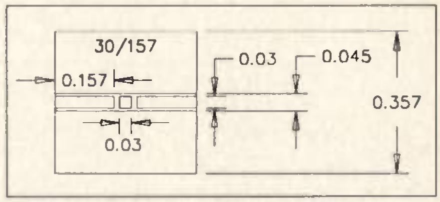


Figure 8. 30/157 chip carrier, top view (0.375 x 0.375 x0.025 inch thick gold plated alumina substrate).

currents with respect to time, which take place in the nonlinear SPICE simulators.

More complex devices such as BJTs require more complex models. Schematic representations of the basic linear and nonlinear BJT models are shown in Figures 3 and 4 respectively. Full understanding and appreciation of these models requires study of the equations that characterize these different models (3).

The Non-Linear BJT Model

Originally there were two separate bipolar models implemented in SPICE; the Ebers-Moll (5) and the Gummel-Poon (2). Later versions of SPICE combined these two models so that the Ebers-Moll large signal DC model is a subset of the Gummel-Poon. If all BJT parameters are specified, the more rigorous Gummel-Poon model is used. If certain parameters are not specified, the simulator will default to the Ebers-Moll model equations.

In this article we will refer to the Ebers-Moll/Gummel-Poon nonlinear models collectively as "the model" unless otherwise specified. Generally speaking, a model is the actual description of the behavior of the component as defined by mathematical equations. In the previous diode example, the model is the equation for I_D.

Model parameters are variables used in the equations to characterize the device. In the diode example, the model parameter is the saturation current I_S.

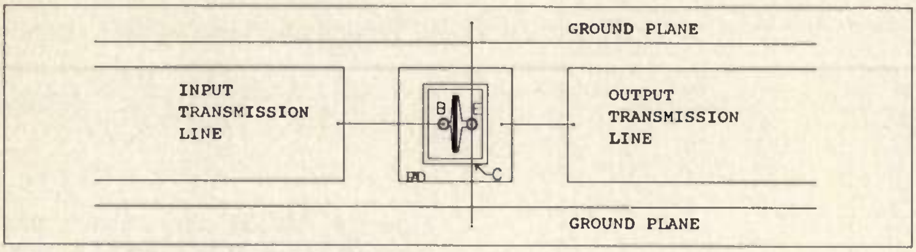


Figure 9. Chip bonding diagram.

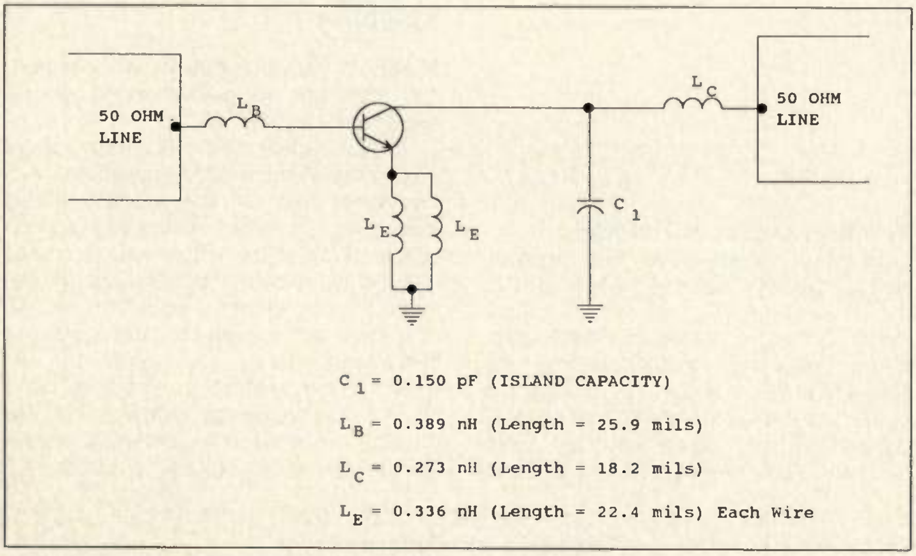


Figure 10. Chip bonding schematic.

This parameter has a value of 1×10^{-14} amps and is referred to as the parameter value.

Another type of parameter encountered in SPICE simulators (but not part of this discussion) is a control parameter. Temperature is an example of a control parameter.

Early versions of the SPICE BJT model used only 11 parameters. Current SPICE simulators use as many as 40 parameters (see Table 1). An in-depth understanding of these parameters is not necessary to use the model, but it is a good idea to understand the basic limitations of the BJT model (6).

One limitation of the BJT model is that there is no bias dependency for the model parameter R_E. To explain the significance of this, refer to Figure 5. If you force a base current I_B and measure the open circuit collector voltage V_{CE}, you are in effect measuring the voltage drop across the resistance between the active emitter region and the emitter terminal, which is defined as R_E in the BJT model. The dominant component of emitter resistance is normally the contact resistance, typically less than 1 ohm. In a circuit simulation using a bias in the constant R_E region, where the slope is constant and approximately equal to $1/R_E$, the model will provide accurate results with respect to R_E. However, if you bias the device in the high current region where the slope is no longer constant, significant error may be introduced.

Bias condition	Chip	Package
5V, 50mA	NE46100A.S2P	NE46134A.S2P
5V, 100mA	NE46100B.S2P	NE46134B.S2P
8V, 50mA	NE46100C.S2P	NE46134C.S2P
8V, 100mA	NE46100D.S2P	NE46134D.S2P
10V, 50mA	NE46100E.S2P	NE46134E.S2P
10V, 100mA	NE46100F.S2P	NE46134F.S2P
12.5V, 50mA	NE46100G.S2P	NE46134G.S2P
12.5V, 100mA	NE46100H.S2P	NE46134H.S2P

Table 2. Measured S-parameter files.

SIMULATOR NAME	VENDOR
P-Spice	Microsim
H-Spice	Meta-software
I-Spice	Intusoft
mwspice, [Libra]	EESOF
[Harmonica]	COMPACT Software
[MDS] Hewlett-Packard	

[ ] brackets indicate harmonic balance simulator, instead of SPICE simulator

Table 3. Compatible simulators.

The NE461 Bipolar Transistor

The NE461 device was chosen for this example because of its useful bias range, wide dynamic range performance, and high output power. Devices are available in a low cost surface mount package (the NE46134 is the NE461 chip in a 34 package) as well as in chip form (4). Key features of this device are:

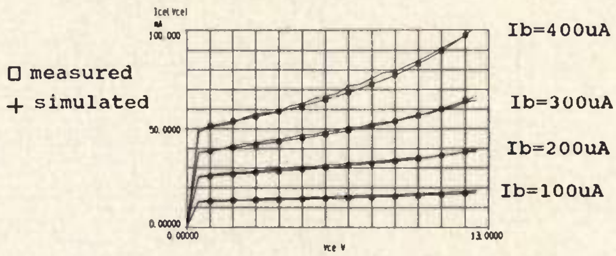


FIGURE 11. Chip (NE46100) DC I-V Curves

Figure 11. Chip (NE46100) DC I-V curves.

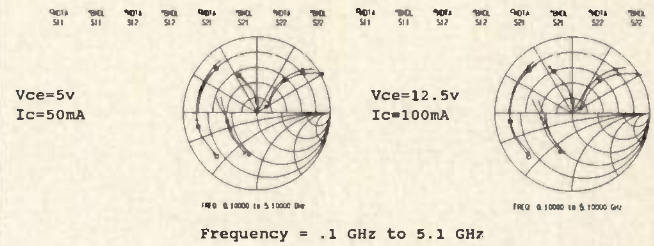


Figure 12. Chip S-parameter plots.

Low cost
  Less than $1.00 (1,000+ qty.)

High dynamic range
  0.5 watts P_{out} at 1 dB compression with 12 V supply
  0.4 watts P_{out} at 1 dB compression with 10 V supply; IP3 >37 dBm
  0.17 watts P_{out} at 1 dB compression with 5 V supply; IP3 >32.5 dBm

Low Noise Figure 1.5 dB nf at 500 MHz
  2.0 dB nf at 1 GHz

Low intermodulation distortion (IMD) −40 dBc 2-tone at 1 GHz (+20 dBm P_{out})

These features make the NE46134 an excellent choice for high volume, low cost consumer and commercial applications. In a transmitter, this device can be used as a driver stage, as a 1/2 watt linear output stage, or combined for higher power outputs. In receiver applications where high dynamic range is required (such as mobile communications), the combination of low noise and high intercept point make this device a good choice for low-noise preamplifier stages.

Measurement, Simulation and Verification

Since a simulation is only as good as the model being used, and the model is only as good as the data from which it is derived, accurate measurements, good test equipment and a repeatable calibration method are essential. First, several devices, both chip and package, were measured to find a typical device. This typical device was then used for more rigorous data collection, model development and verification.

The test setup used to measure both the chip and packaged device DC and S-parameters is shown in Figure 6. The controller hardware is an IBM AT compatible computer using the automated measurement program ANACAT™ from EEsof, Inc. The test equipment consists of a Hewlett-Packard HP8510B Network

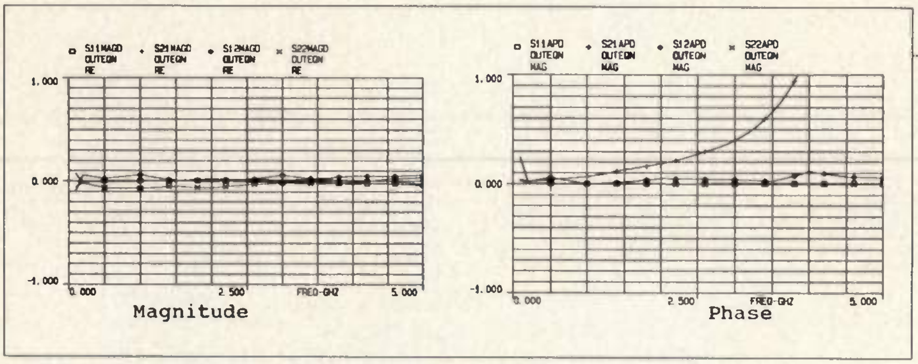


Figure 13a. Chip (NE46100) error graphs, V_{CE}= 5V, I_C= 50 mA.

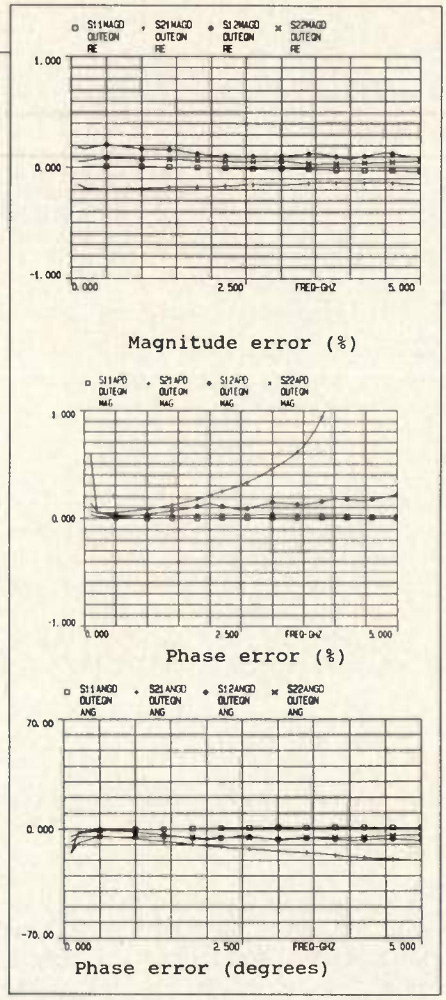


Figure 13b. Chip (NE46100) error graphs, V_{CE}=12.5V, I_C=100 mA.

Analyzer and HP4145A Semiconductor Analyzer. The interface between the controller and test equipment is accomplished with a National Instruments GPIB interface board installed in the AT computer. While the HP8510B measures the S-parameters, the HP4145A provides and measures the DC voltage and current values. Under the control of ANACAT, the device's DC and S-parameter values are measured, with the data collected and saved to a file on the controller's hard disk.

As previously mentioned, the accuracy of the model is only as good as the accuracy of the data from which it is derived. Therefore, this data becomes the reference by which the model accuracy is evaluated. To insure accuracy, two additional sources of data are used for correlation. The first is a power measurement setup independent of the aforementioned S-parameter and DC measurement test setup. P_{in} and P_{out} data from 20 dB below compression up through compression is obtained at different bias levels in a 50 ohm system. The small signal gain is compared to the

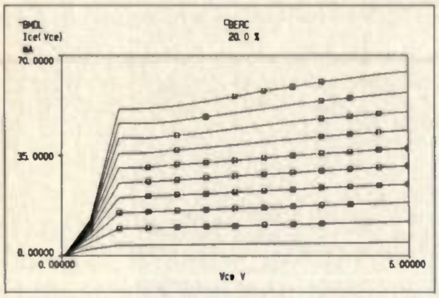


Figure 14. S-parameter error indicators on DC I-V curves.

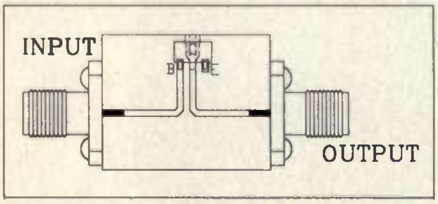


Figure 15. NE46134 test fixture, top view (30 mil thick, Duroid 6006).

50 ohm small signal gain, S21, and should be the same. If any discrepancies exist, testing and troubleshooting ensue until the source of the error is determined and corrected.

The second independent data source is a harmonic and intermodulation measurement test setup. As with the power measurement, data is collected and compared to the computer simulation. Factory data sheets supplied by NEC are also used as an additional source of data for comparative purposes.

	OUTPUT POWER				POWERGAIN			
Pin	Sim P_{out} (dBm)	Meas P_{out} (dBm)	Meas - Sim (dB)	Sim vs Meas (%)	Sim Gain (dBm)	Meas Gain (dBm)	Meas - Sim (dB)	Meas vs Sim (%)
0.0	7.95	8.12	0.17	2%	7.95	8.12	0.17	2%
5.0	12.94	12.90	-0.04	-0%	7.94	7.90	-0.04	-1%
10.0	17.92	17.87	-0.05	-0%	7.92	7.87	-0.05	-1%
15.0	22.85	22.78	-0.07	-0%	7.85	7.78	-0.07	-1%
20.0	27.26	27.14	-0.12	-0%	7.26	7.14	0.12	2%
20.5	27.50	27.50	0.00	0%	7.00	7.00	0.00	0%
21.0	27.68	27.90	0.22	1%	6.68	6.90	0.22	3%
22.0	27.87	28.50	0.63	2%	5.87	6.50	0.63	10%
23.0	27.90	28.96	1.06	4%	4.90	5.96	1.06	18%
24.0	27.96	29.30	1.34	5%	3.96	5.30	1.34	25%
25.0	28.10	29.56	1.46	5%	3.10	4.56	1.46	32%

Table 4. Measured versus simulated power (Frequency = 900 MHz).

Chip Calibration and Measurement

Currently CEL uses the coplanar waveguide (CPW) test fixture developed by Design Techniques™ for measurement of chip devices. The calibration method used for measuring the NE46100 chip is the Open-Short-Load (OSL) technique (7). The OSL calibration technique uses a set of CPW calibration standards consisting of a dual open, a dual short, a dual Z_0=50 ohm load and a Z_0=50 ohm thru used during an in-fixture calibration of the network analyzer. This calibration provides a one tier de-embedded measurement of the device under test (DUT) where the effects of the test fixture and the effects of the input/output transmission lines of the chip carrier are removed.

The CEL "30/157" CPW chip carrier is shown in Figure 8. The 50 ohm

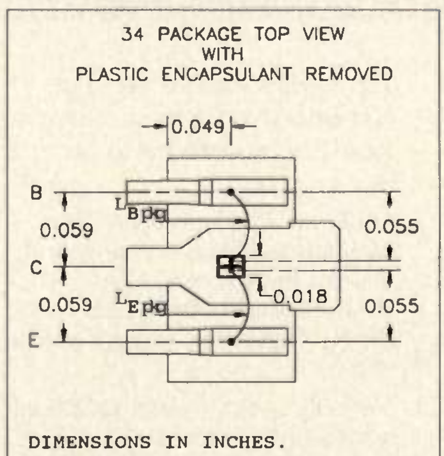
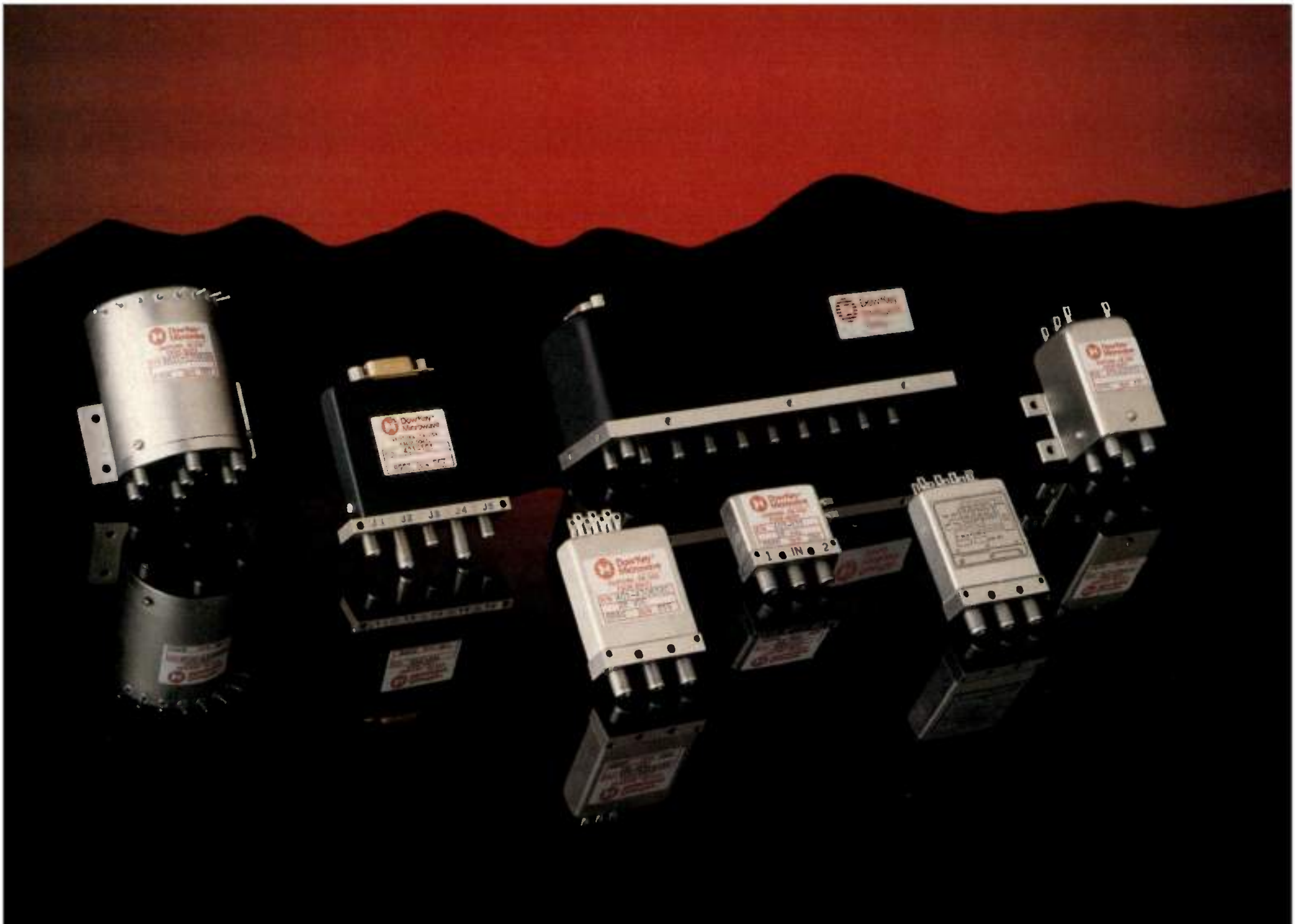


Figure 16. 34 package top view with encapsulant removed.



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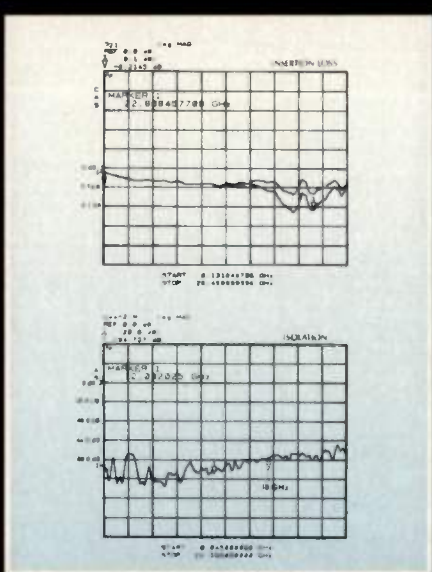

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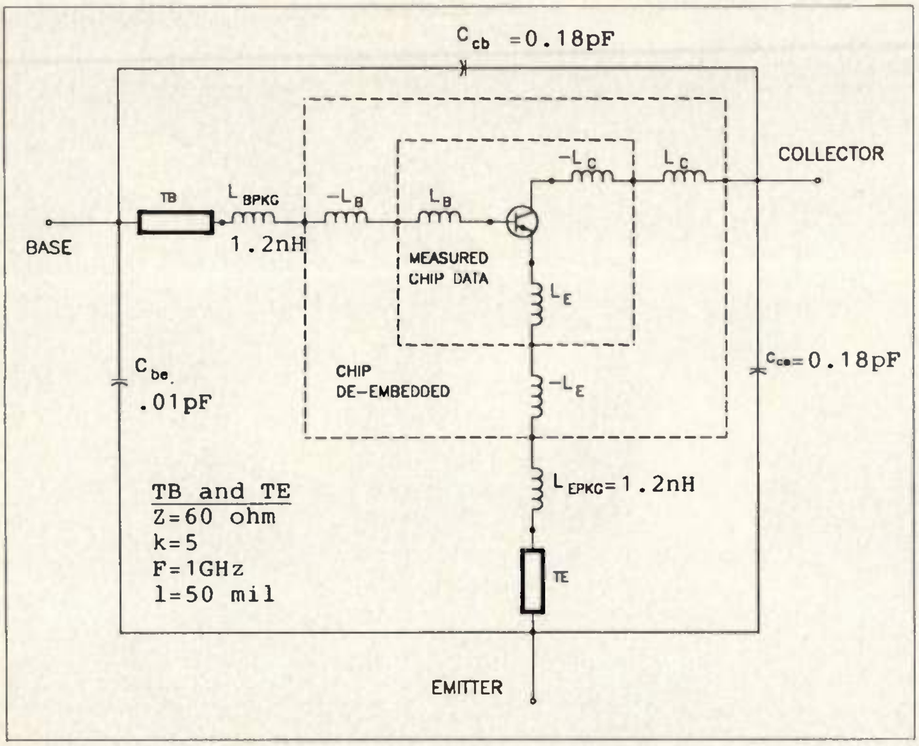

Figure 17. 34 package equivalent circuit.

transmission lines are 0.030 inches wide by 0.157 inches long. Consistent with coplanar waveguide design, the two large metallized areas are located on either side of the input and output transmission lines and form the chip carrier ground planes. In addition, a 0.030 inch square metallized pad, or island, electrically isolated from the ground plane areas and 50 ohm lines, is centered on the chip carrier to provide a mounting surface for the die. Figure 9 shows the bonding configuration for common emitter biasing. The collector of the device, located along the underside of the die, is attached to the island. The base and collector each have a single bond wire connecting the device to the input and output chip carrier 50 ohm transmission lines, respectively. The emitter is grounded through two similar length bond wires to the coplanar grounds on the surface of the chip carrier.

The resultant parasitics are represented schematically in Figure 10. The collector island introduces an additional parasitic capacitance of 0.150 pF, which is mathematically removed by software

Oct. '91

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	SIGNETICS NE604A	SIGNETICS NE614A	SIGNETICS NE605	SIGNETICS NE615	SIGNETICS NE606	SIGNETICS NE616	SIGNETICS NE607	SIGNETICS NE617
Vcc	4.5 - 8 V	4.5 - 8 V	4.5 - 8 V	4.5 - 8 V	**2.7 - 7 V**	**2.7 - 7 V**	**2.7 - 7 V**	**2.7 - 7 V**
Icc @ Vcc	3.3mA @ 6V	3.3mA @ 6V	5.7mA @ 6V	5.7mA @ 6V	**3.5mA @ 3V**	**3.5mA @ 3V**	**3.5mA @ 3V**	**3.5mA @ 3V**
Number of Pins	16	16	20	20	20	20	20	20
Package	Dip,SO	Dip,SO	**Dip,SO,SSOP**	**Dip,SO,SSOP**	**Dip,SO,SSOP**	**Dip,SO,SSOP**	**Dip,SO,SSOP**	**Dip,SO,SSOP**
Input Frequency (Max.)	Same as IF	Same as IF	**500MHz**	**500MHz**	150MHz	150MHz	150MHz	150MHz
Sensitivity Input Pin	**0.22μV**	**0.22μV**	**0.22μV**	**0.22μV**	0.31μV	0.31μV	0.31μV	0.31μV
Rin	1.6KΩ	1.6KΩ	4.7KΩ	4.7KΩ	8KΩ	8KΩ	8KΩ	8KΩ
Mixer Conversion Gain	N/A	N/A	13dB	13dB	17dB	17dB	17dB	17dB
Input 3rd Order Intercept*	N/A	N/A	**+4dBm**	**+4dBm**	-9dBm	-9dBm	-9dBm	-9dBm
Process ft	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz
IF Frequency (Max.)	**25MHz**	**25MHz**	**25MHz**	**25MHz**	2MHz	2MHz	2MHz	2MHz
RSSI Range	**90dB**	80dB	**90dB**	80dB	**90dB**	80dB	**90dB**	80dB
RSSI Temp Comp	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**	**YES**
Conversion Stages	N/A	N/A	Single	Single	Single	Single	Single	Single
Features	- High Sensitivity - High IF Frequency	- High Sensitivity - High IF - Relaxed 604A	- High Sensitivity - High Input/IF Frequency - SSOP 20	- High Sensitivity - High Input/IF Frequency - SSOP 20 - Relaxed 605	- Low Power - Audio Op-Amp on Output - RSSI Op-Amp on Output - SSOP 20	- Low Power - Audio Op-Amp on Output - RSSI Op-Amp on Output - SSOP 20 - Relaxed 606	- Low Power - Audio Op-Amp on Output - Freq Check - Buffered RSSI - Differential Limiter Output - SSOP 20	- Low Power - Audio Op-Amp on Output - Freq Check - Buffered RSSI - Differential Limiter Output - SSOP 20 - Relaxed 607
Applications	- Can be combined with the NE602A to produce a single conversion receiver	- Can be combined with the NE612A to produce a single conversion receiver	- Cellular - High Performance Receivers - Industry Standard	- Cellular - Cordless Phones	- Portable Cellular - Portable Receivers - Cordless Phones	- Portable Cellular - Portable Receivers - Cordless Phones	- Portable Cellular • AMPS/TACS • NAMPS/NTACS - Portable Receivers - Cordless Phones	- Portable Cellular - Portable Receivers - Cordless Phones

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```
.MODEL  NE461  NPN
+ IS=8.7E-16 rb=6 irb=.004 rbm=4 bf=185 nf=.959
+ vaf=30 ikf=.35  ise=.57e-12  ne=1.8  re=.63  rc=3.0
+ br=5  nr=1  var=12.376  ikr=.01789  isc=1e-14  nc=1.95
+ cjc=2.5e-12  vjc=.83  mjc=.33  xcjc=.2  cje=4.9e-12
+ vje=.6  mje=.45 tf=12.9e-12  xtf=1.6  vtf=19.875 itf=.4
+ ptf=0  tr=1.7e-8
```

Figure 18. SPICE model definition.

that models the capacitance as a shunt C element. The bond wires are not de-embedded since the device will have bond wires attached when used in an actual circuit. The bond wire composition and lengths are defined on the NE46100 data sheet (Figure 7) to allow circuit designers to use their own models for the bond wires. A simplification at low frequencies is to use a 0.015 nH/0.001 inch approximation. For example, a 25.9 mil bond wire would have an approximate equivalent inductance of 0.3885 nH. The device is measured in the CPW chip test fixture using the test setup shown in Figure 6.

Chip DC I-V curves were generated by sweeping V_{CE} from 0 V to 12.5 V in 1.25 V steps, and by sweeping I_B from 75×10^{-6} amps to 425×10^{-6} amps in 25×10^{-6} amp steps. S-parameter measurements were made by sweeping V_{CE} and I_B over the same I-V curve ranges, and sweeping frequency from 100 MHz to 5.1 GHz in 100 MHz steps. This generated a tremendous amount of data (over 1 Megabyte) and took several hours. Other data points were taken to develop Gummel plots, R_C, R_E, and bond wire information. The forward and reverse Gummel plots characterize the current flow through the base, collector and emitter while forward biasing the base-emitter and base-collector PN junctions respectively. These measurements provide the basis for verifying the model.

Chip Simulation and Verification

Inspecting the measured and simulated data provides insight into how well the model compares to the actual device. Several plots which aid in assessing the model are: DC I-V curves (Figure 11), Beta plots, capacitance plots (C_{cs} vs V_{CE}, C_{be} vs V_{be}, C_{be} vs V_{be}), S-parameter plots (Figure 12), and frequency dependant error graphs (Figure 13). Gummel plots, power, intermodulation distortion and time domain plots are also used for model characterization and validation but not included here due to time and space constraints.

The DC I-V curves (Figure 11) show very close correlation between simulated and measured data. The S-parameter graphs show good correlation (Figure 12). To better quantify the correlation, CEL has standardized on the error graphs shown in Figure 13. These error graphs provide insight into the frequency dependant nature of the correlation and are usually generated at several different bias conditions. The graphs can be used to yield a single number quantifying the accuracy at

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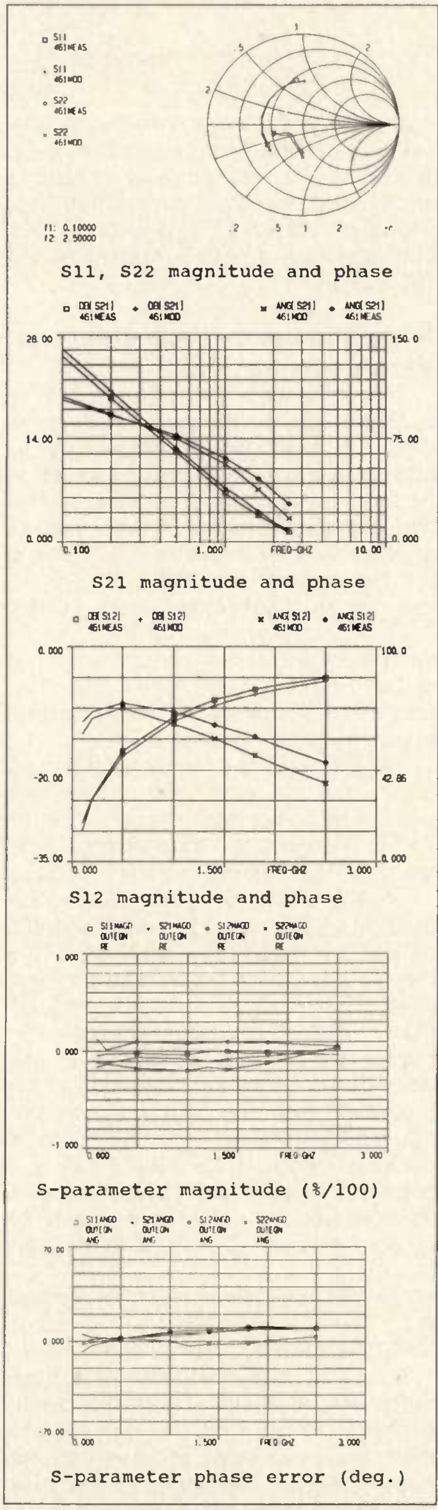

Figure 19. Package (NE46134) S-parameters and error graphs at V_{CE} = 5V, I_C = 50 mA.

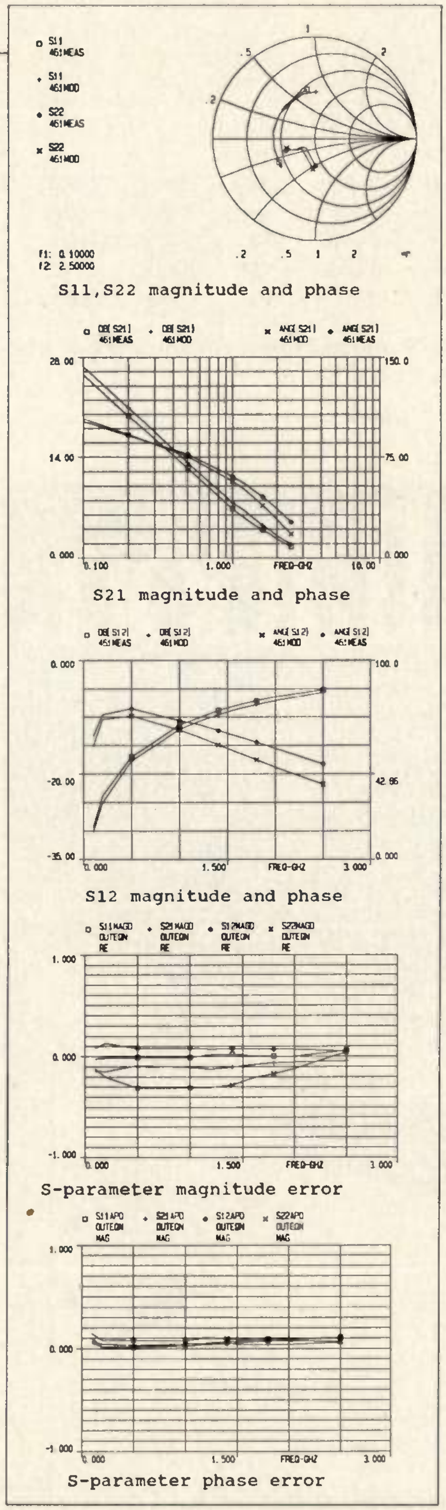

Figure 20. Package (NE46134) S-parameters and error graphs at V_{CE} = 12.5V, I_C = 100 mA.

each bias condition, such as 10 percent peak-to-peak error maximum at V_{CE} =5 V, I_C =50 mA. Errors of less than 2 percent can be obtained if the model parameters are optimized for small frequency or bias variations. Unless you are using the device at a single bias condition and single frequency, however, we do not recommend evaluating a model based solely on an RMS or peak-to-peak error value since it doesn't provide insight as to where the maximum or minimum errors occur.

A unique method of characterizing

	S11		S21		S12		S22	
	(mag)	(ang)	(mag)	(ang)	(mag)	(ang)	(mag)	(ang)
Meas	0.53	127	2.547	-66.0	0.189	-62	0.507	-101
Sim	0.58	139	2.497	-66.6	0.208	-60	0.498	-91
Meas	-0.05	-12	0.050	0.6	-0.019	-2	0.009	-10
(M-S)/M	-9%	-9%	2.0%	-1%	-10%	3%	2%	10%

Table 5. Measured versus simulated S-parameters (Frequency= 900 MHz).

S-parameter accuracy versus bias on a single graph (9) is shown in Figure 14. This graph shows the bias conditions which yield maximum error (measured versus simulated) of 20 percent or less, indicated with a square marker on the DC I-V curve.

Packaged Device Calibration and Measurements

The calibration method used for the packaged device measurements is the APC 3.5 mm OSL technique. A full two-port calibration of the HP8510B is performed using the HP85052A calibration kit. CEL software is then used to mathematically de-embed the effects of the test fixture. The HP8510B APC 3.5 mm two-port calibration error vectors are modified to remove the effects of the test fixture and are then restored as the active HP8510B calibration set. This provides one-tier de-embedded measurements of the package device.

The DC and S-parameter measurements for the packaged device are performed in the same manner as the ANACAT-controlled measurements of the NE46100 chip described previously.

The NE46134 package device is measured with the package leads secured on the test fixture 50 ohm lines with a rexolite hold down block. The package itself is secured on a 30 mil thick RT Duroid 6006 substrate as shown in Figure 15. Since the calibration de-embeds the fixture and the lead lengths protruding from the package, no package lead lengths are included in the 34 package model. If the 0.0315 inch (0.8 mm) lead lengths need to be included, their equivalent inductance would be on the order of 0.05 nH. S-parameters at various bias conditions are available in the NEC/CEL Design Library Version 4.0, files NE46134A.S2P through NE46134H.S2P as indicated in Table 2.

Figure 16 shows the internal configuration of the NE46134 with the plastic encapsulant removed. You can see that there are three tabs, one each for the base, collector and emitter. The base and emitter leads are identical and are represented as transmission lines T_b and T_e in the package schematic of Figure 17. The collector lead is significantly wider than the base and emitter leads and protrudes slightly beyond the bottom side of the package. The collector tab has little or no effect on the measurements in this configuration at these frequencies. Coupling effects between the base-emitter, base-collector, and collector-emitter are represented

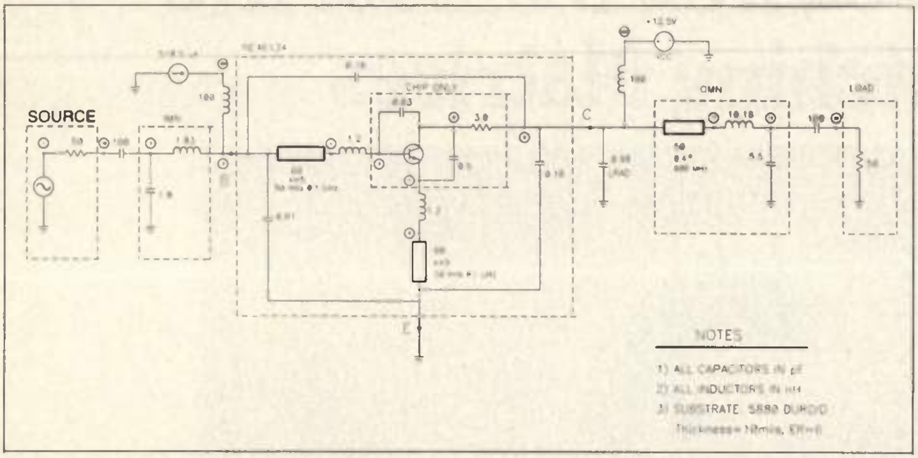

Figure 21. Amplifier schematic.

as C_{be}, C_{cb}, and C_{ce} respectively as shown in Figure 17.

Package Simulation and Verification

The chip has now been fully characterized, and since package parasitics primarily affect high frequency response, S-parameters are sufficient for package model verification. S-parameter data was taken at different DC I-V biases while sweeping frequency from 50 MHz to 2.5 GHz; 2.5 GHz is the high end for the package since the 50 ohm gain approaches unity at this frequency.

The nonlinear model parameters for the NE46100 (chip) were embedded in the package model and entered into a SPICE simulator (Figure 18). This simulation data was compared with the NE46134 S-parameter data at the bias conditions measured above. Figures 19 and 20 show the S-parameter data and error graphs which quantify the accuracy of the model at two different bias conditions (Figure 19: V_{CE} =5 V, I_C=50 mA and Figure 20: V_{CE} =12.5 V, I_C =100 mA). The error graphs would normally indicate less than 10 percent peak-to-peak error, however, since the actual chip in the package is different than the chip used for developing the chip model, some error is to expected since no two chips are exactly alike. The simulated chip model in the package was tuned to verify this assumption, and less than 10 percent error was achieved.

Application Circuit

Verification of the NE46134 model was also done by using the model to design and build an a 900 MHz amplifier with P_{1dB} of 27.5 dB and 8 dB gain. The amplifier was designed using 0.010 inch thick 5880 Duroid with a dielectric constant of 6.0. The high dielectric constant and thin board were used to minimize line lengths.

Figure 21 shows the amplifier sche-

matic. The CHIP ONLY dashed box indicates the nonlinear chip model without bond wires. The NE46134 dashed box contains the 34 package model with the chip model embedded. The package model was developed with the device mounted on a special fixture which didn't introduce any parasitics into the measurement. The actual amplifier design uses typical high volume, low cost fabrication techniques which introduces parasitics and must be accounted for in the design. These parasitics, not shown in the schematic, are represented as a shunt 0.1 pF capacitor at the base of the 34 package (node 3) and a shunt 1.6 pF capacitor at the collector of the 34 package (node 8).

The input matching network (IMN) consists of a shunt 1.8 pF capacitor and a series 1.93 nH inductor. The output matching network (OMN) consists of a series 50 ohm transmission line, a series inductor, and a shunt 5.5 pF capacitor. The IMN and OMN provide the proper gain and power matching to achieve 8 dB linear gain and 27.5 dBm output power (P_{1dB}) at 900 MHz. The DC biasing components and source and load are also shown for completeness.

Measured vs. Simulated Results

A comparison between measured and simulated output power at 900 MHz is shown in Figure 22. A comparison of the tabular data (Table 4) shows the difference between measured and simulated output power to be less than 3 percent for input power levels in the linear region and up through 1dB compression. As the amplifier goes further into compression, the measured gain is 1 to 1.5 dB higher than simulated gain. This is to be expected since the nonlinear chip model was optimized for the linear region of operation over a very wide dynamic bias range; the implementation of the Gummel-Poon model in this application is not as accurate in the high current, high power region. The largest difference between measured and simulated P_{out} is 5 percent: 28.1 dB simulated versus 29.56 dB measured, with 25 dBm input. This output power difference results in a power gain difference worst case of 32 percent, 3.1 dB simulated

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versus 4.56 dB measured, at 25 dBm input.

Simulated S-parameters are within 10 percent of the measured S-parameters except for S11 and S12. The input bias and matching network could be tuned to provide a closer match between simulated and measured S11, at the expense of a higher gain error, S21 (from 2 percent up to 10 percent). S12 converted to dB is −14.5 dB (measured) versus −13 dB (simulated). The 1.5 dB difference (10.3 percent) in isolation is considered negligible.

Additional time could be spent fine tuning the circuit to achieve more exact correlation for this amplifier, but if this were to go into production the next logical step would be to perform a tolerance analysis on the various components of the model and modify the design based on performance, cost tradeoffs and yield goals.

CAD Software Compatibility

The model parameters presented here can be used in most commercial RF and microwave non-linear simulators that support the Gummel-Poon model. Presented in Table 3 is a list of compatible simulators CEL has checked for Gummel-Poon support. A description of the parameters that are different and what to do with them for each simulator can be obtained by contacting CEL or the vendor. If you are using a simulator other than those listed, check with the manufacturer-supplied element catalog, the manufacturer directly, or CEL.

If you use a nonlinear SPICE simulator for predicting the performance of an

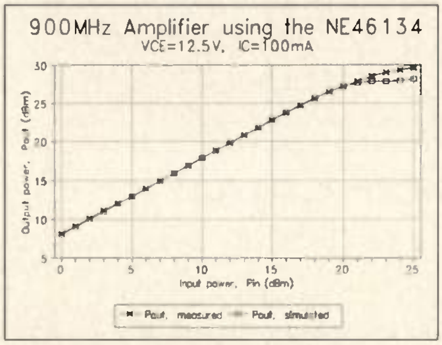

Figure 22. Power response.

amplifier in compression, or for intermodulation distortion, harmonics, and other nonlinear responses, it is imperative that your simulation time extend out far enough to reach steady state.

Conclusions

We have presented a fairly rigorous method for validating a medium power, nonlinear, bipolar junction transistor model to be used in commercially available nonlinear simulation software. This method has been extended from device validation to circuit validation by building working hardware with response correlating closely to the simulated circuit using the NE46134 nonlinear model. ***RF***

Acknowledgement

The authors are grateful to Khanh Luu, Ron Meier, and Huy Tran for assisting with the production artwork, the calibration section and device measurements, and assembly and test of the application circuit, respectively. We also thank EESOF and Hewlett-Packard for their modeling and simulator assistance.

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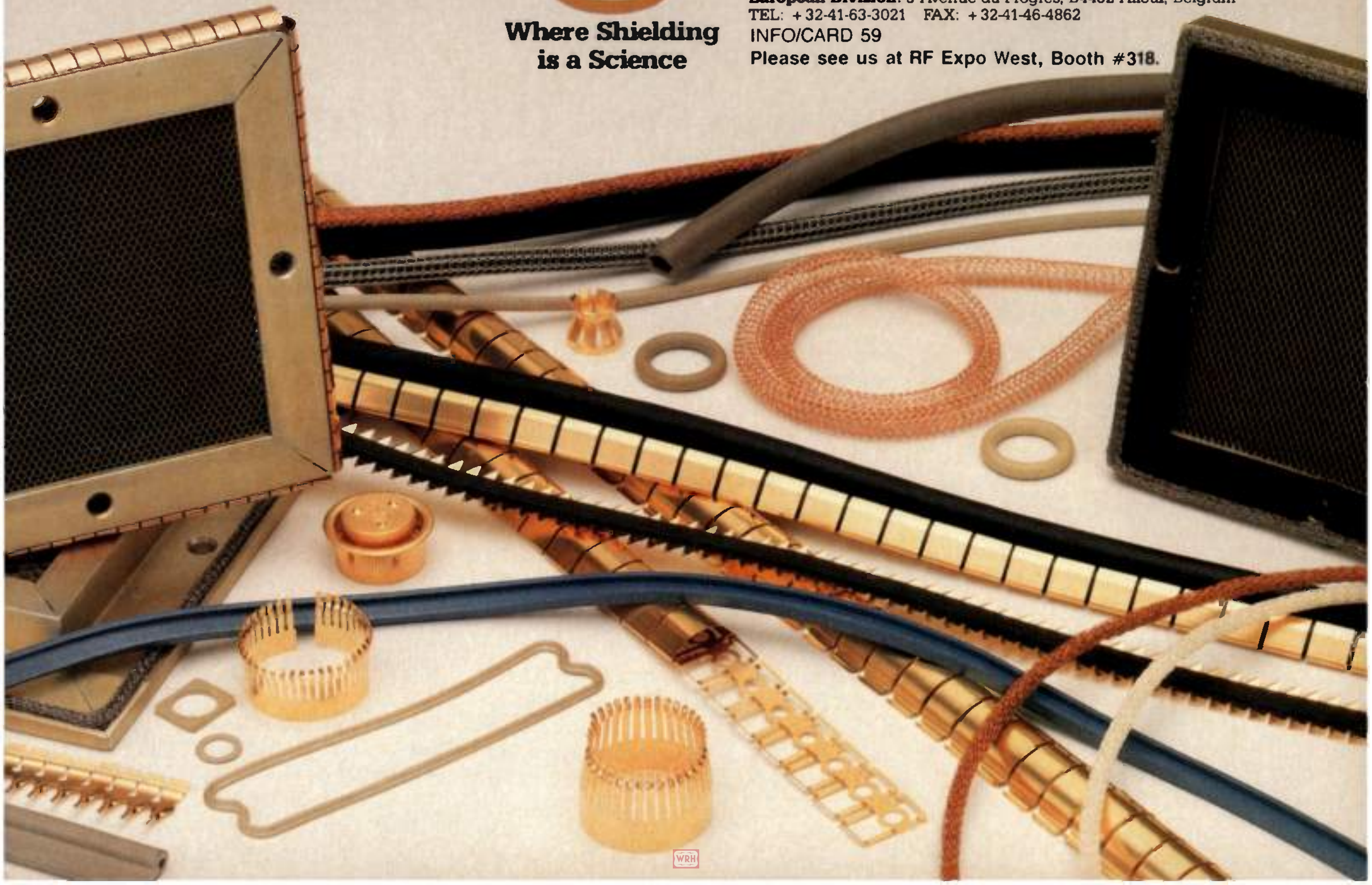

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INFO/CARD 60

QSPLOT Utility Displays S-Parameter Data

By David Lovelace
Motorola, Inc.

QSPLOT is a quick utility to display S-parameter files on DOS computers without having to resort to circuit analysis software. It is most useful when doing a quick comparison of one or more data files, checking to see if measured data is valid, or verifying a file before using.

This utility program can quickly display all of the parameters from one or more, two port S-parameter data files and print the displayed data to a user specified printer on command and even produce HPGL compatible graphic output. QSPLOT will display S11 and S22 in Smith chart format, S12 and S21 in polar format and f_T and G_{MAX} on log frequency charts. Observation and comparison of tabular S-parameter data files by graphical means in these formats is now possible without circuit analysis software.

Table 1 displays an example file and the initiating command format included in QSPLOT. An example of the command: QSPLOT AT?.S2P is shown in Figure 1. This example reflects just one of the capabilities of QSPLOT to display two port S-parameter data. In the example shown in Figure 1, S11 and S22 are plotted on a Smith chart and S12 and S21 are plotted on a polar chart. The polar charts are scaled according to the maximum value of |S12| and |S21| given in the plotted files. The names and paths (if applicable) of the displayed files are given in the center with colors that correspond to those of the plotted data.

Format:	**QSPLOT**	**<PATH< FILENAME(S).EXT**
Where:	**<PATH>** (Optional)	= Location of files to be displayed
	FILE NAME(S).EXT	= Filenames(s) and extension. Note: The file extension must be specified.
Examples:	QSPLOT	TEST.S2P
	QSPLOT	FET.S2P BIP.S2P HBT.S2P
	QSPLOT	C:\SPAR*.S2P
	QSPLOT	B:FETT?.S2P

Table 1. Initiating command format and example files included in QSPLOT.

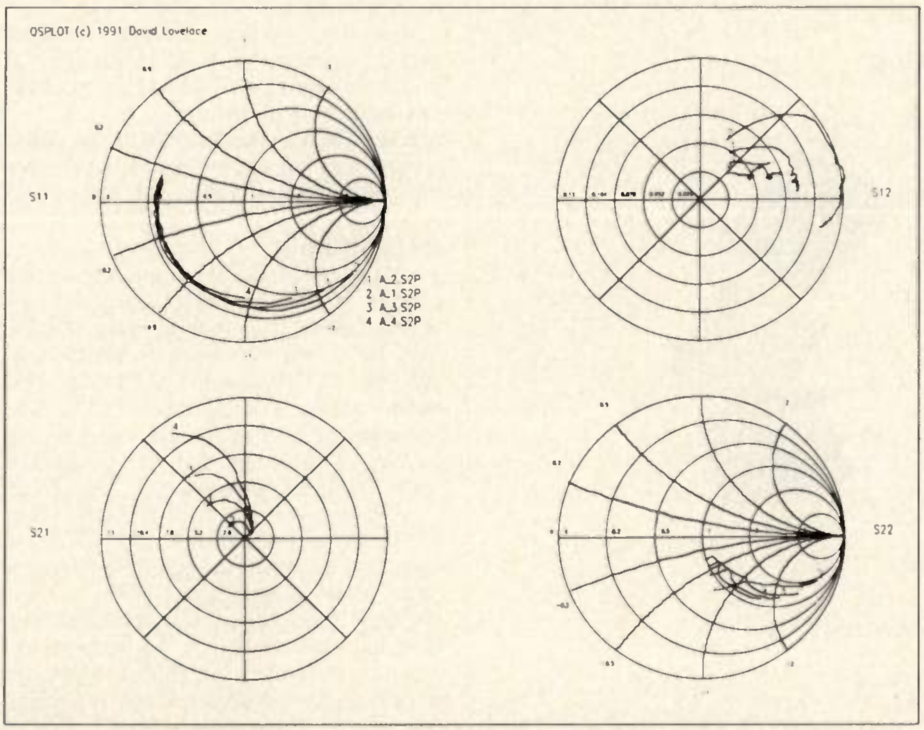

Figure 1. Initial display, all two port S-parameters (Press "<SPACE>").

How to Use

Once QSPLOT is started, the individual S-parameter plots, all four parameters, f_T or G_{MAX} can be displayed, enlarged and printed. Initially, a display of all four S-parameters is given. Enlarging any one of these plots can be done by pressing the keys corresponding to that parameter. Pressing "11" enlarges S11, "12" enlarges S12, "21"enlarges S21 and "22" enlarges S22. Pressing the space bar will cause all four of the S-parameters to be displayed simultaneously and "A" will cause both the plots for f_T and G_{MAX} to be displayed on the same screen. "FT" will cause f_T to be displayed individually and "GM" will display an enlarged view of G_{MAX}. The initial scale used for the y-axis of the log frequency charts is 20 dB. To adjust this scaling, ">" will increase the scale in 5 dB increments and "<" will decrease the scale in 5 dB increments. The "<" and ">" keys only work in the log frequency mode. S12 and S21 polar plots are already scaled. If "p" or "P" is pressed, the current display will be printed. Pressing "l" or "L" will cause

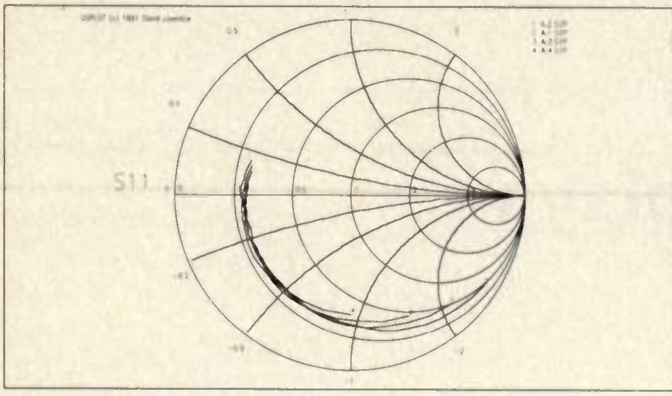

Figure 2. S11 plot (Press "11").

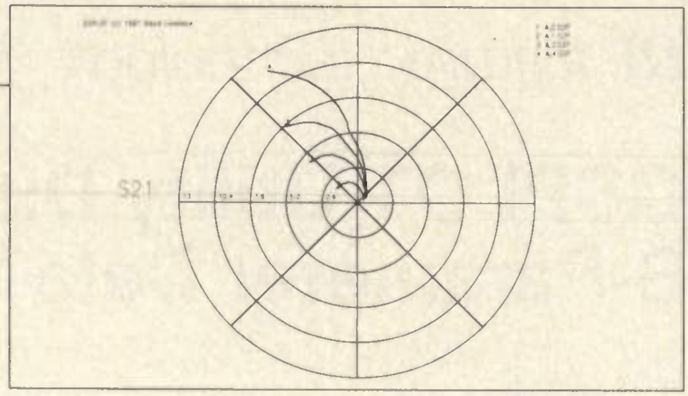

Figure 3. S21 plot (Press "21").

an HPGL file of the present screen to be created. Finally, the ESC key causes the program to terminate. Table 2 shows the valid key sequences used within QSPLOT.

Figures 1 through 6 demonstrate some of the results generated by QSPLOT. Hardware requirements include EGA or VGA display and a math coprocessor. Printers supported are the EPSON FX, MX or LQ modules, Toshiba 24 Pin, HP LaserJet Series and HP DeskJet Series.

QSPLOT requires that the file QSPLOT.CFG is present in the same subdirectory as QSPLOT.EXE. If this configuration file is not present, QSPLOT will create it. QSPLOT.CFG contains configuration data for the user's printer and the selected print options. To change any of the previously set options, erase QSPLOT.CFG then run QSPLOT. This will prompt the user to enter data for the creation of a new configuration file.

Available printer options include printer selection, printer resolution, X and Y dimension scaling factors, portrait or landscape orientation.

Experiments with different printer resolutions may be necessary to obtain the desired clarity and size of printed graphs.

HPGL Output

All the HPGL graphics are generated in files located in the current path in which QSPLOT is being used. These files have the name of HPGLxx.PLT. Where "xx" represents a number between 0 and 99 which QSPLOT automatically generates for the user. When initially started, the first file name will be HPGL0.PLT followed by HGPL1.PLT, . . . up to a maximum of 99 files. If an HPGL file already exists, QSPLOT will name the next HPGL result file sequentially. For example, if HPGL0.PLT through HPGL14.PLT already exist, the next time that an HPGL file is created, it will be named HPGL15.PLT. If a user desires to obtain graphics from a plotter, they should follow these steps:

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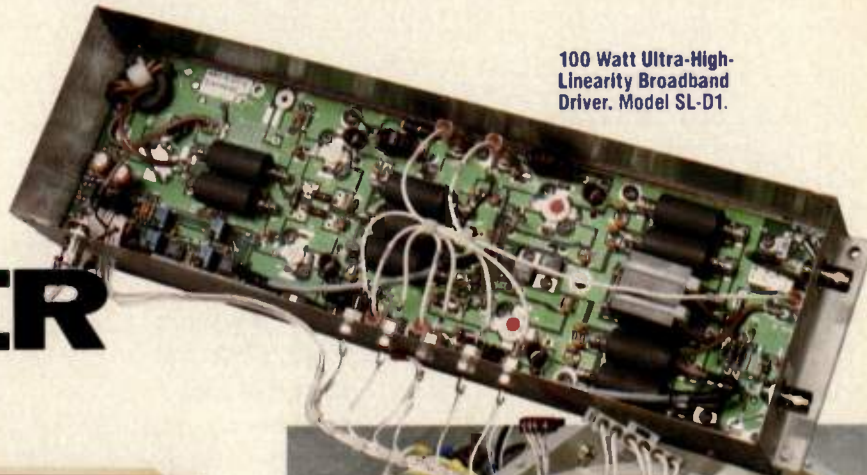

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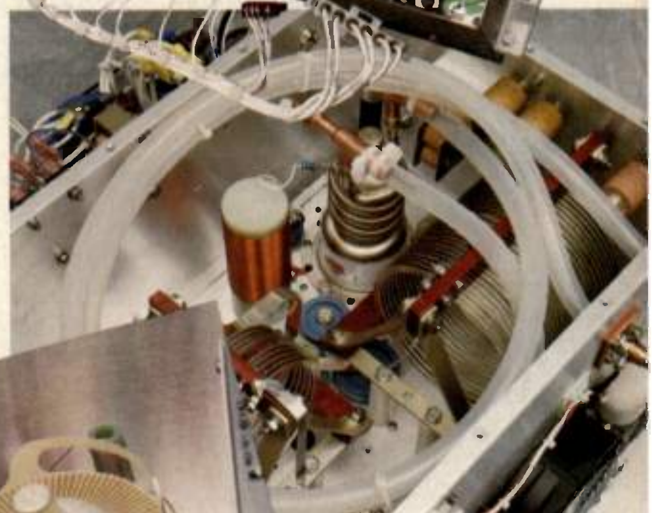

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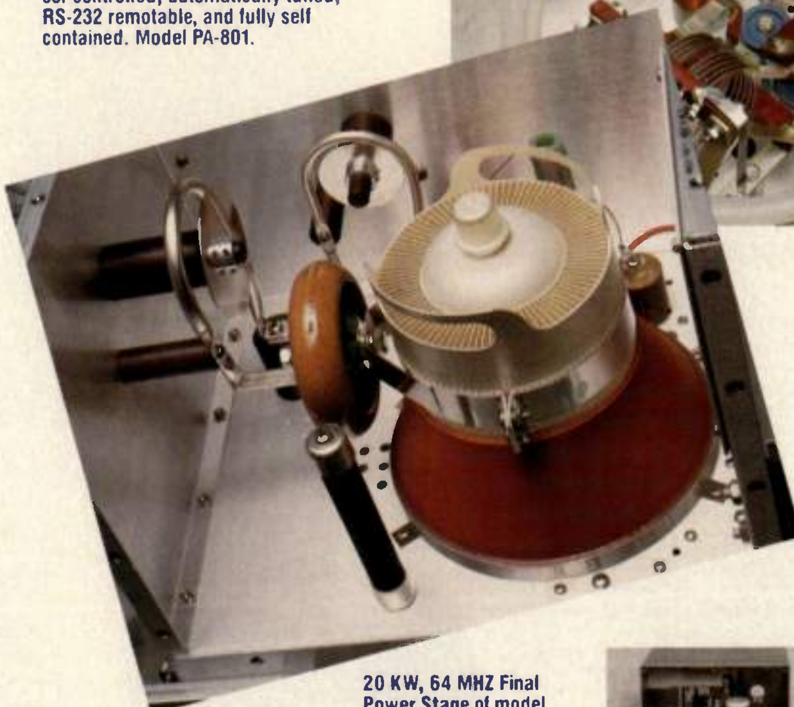

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Command	Function
"11"	Enlarge the S11 plot
"12"	Enlarge the S12 plot
"21"	Enlarge the S21 plot
"22"	Enlarge the S22 plot
"ft" or "FT"	Enlarge the f_T plot
"gm" or "GM"	Enlarge the G_{MAX} plot
"a" or "A"	Display f_T and G_{MAX}
"<" or ">"	Decrease/Increase the log frequency y-axis (Valid only for the f_T and G_{MAX} plots)
[SPACE]	Display all four S-Parameters
"p" or "P"	Print current display
"l" or "L"	Create an HPGL file of current display
"h" or "H"	Help
[ESC]	Quit

Where: "11" denotes a pair of sequential key strokes enclosed within the quotes.

[SPACE] and [ESC] denote pressing the space key or the escape key only.

QSPLOT commands are not case sensitive, therefore any combination of characters such as "ft", Ft", "fT" or "FT" will cause the f_T plot to display.

Table 2. QSPLOT Command keys.

How f_T and G_{MAX} Are Defined in QSPLOT

QSPLOT plots f_T as:

$$f_t = |H_{21}|^2 = \left| \frac{-2S_{21}}{(1 - 2_{11})(1 + S_{22}) + S_{12}S_{21}} \right| \quad (1)$$

Since this plot is a figure of merit that only has meaning when,

$$f_T \geqslant 1$$

QSPLOT only plots for values greater than 0 dB and the presumption can be said for G_{MAX} which only displays values greater than 0 dB as well. G_{MAX} has some other definitions that require more in depth discussion. G_{MAX} is the maximum transducer power gain that is obtained when the input and output ports of the device are conjugately matched. G_{MAX} is a function of stability (K) and is defined as:

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|} \quad K - \quad K^2 - 1 \quad (2)$$

Equation 2 holds only if the device is unconditionally stable (K>1). If the device is potentially unstable (K<1), the definition of Maximum Stable Gain (MSG) is substituted for Equation 2. MSG is defined as:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \quad (3)$$

Which is the equation for G_{MAX} (Equation 2) when K = 1. MSG is a figure of merit that represents the maximum value of GMAX that can be achieved by compensating the device with resistive loads or using feedback to make K = 1. The condition for unconditional stability is:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (4)$$

where

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \quad (5)$$

Table 3. Two port S-parameter data file format.

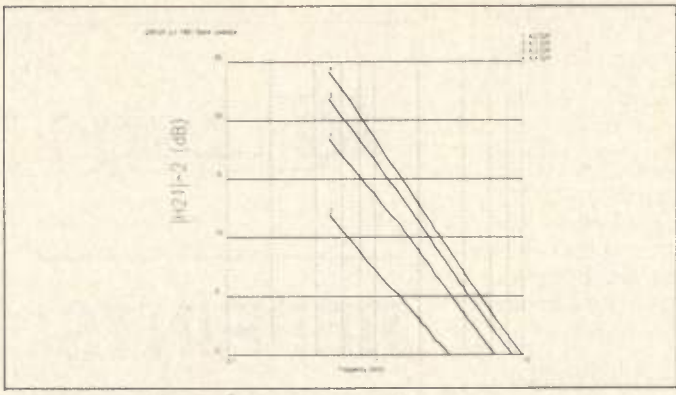

Figure 4. f_T plot (Press "ft" or "FT").

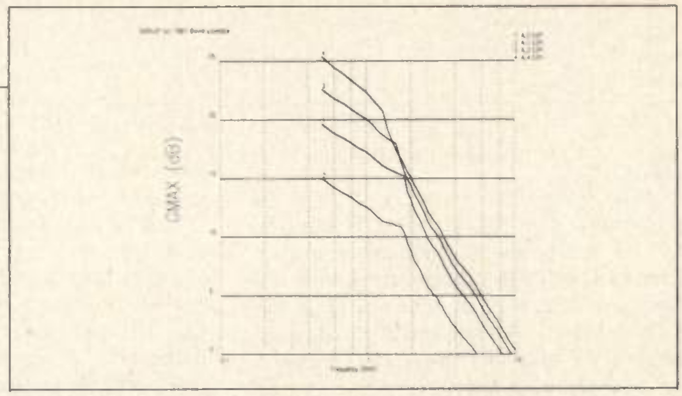

Figure 5. G_{MAX} plot (Press "gm" or "GM").

1. Set the parameters on the COM port with the MODE command. This is dependent on the serial settings of the plotter in use.

Example: MODE COM2:9600,E,7,1
This sets the serial port (COM2:) that the plotter is connected to for a rate of 9600, even parity, seven bits and one stopbit.

2. Copy the desired HPGL file to the plotter.

Example: COPY HPGL1.PLT COM2:

This will copy the HPGL1.PLT graphics to the plotter connected to the COM2: port.

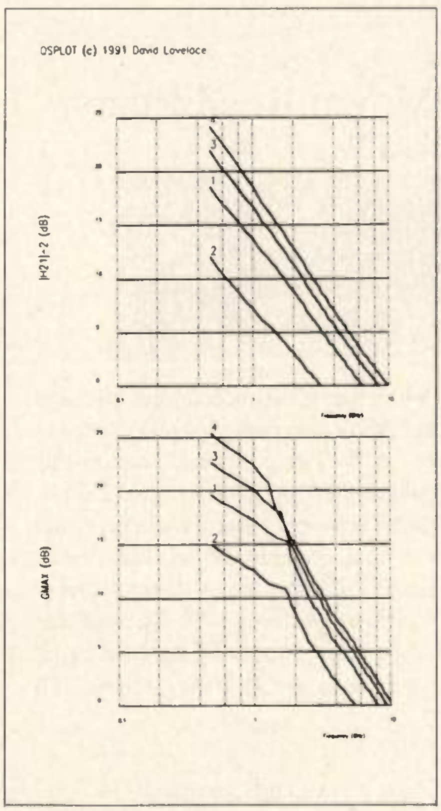

Figure 6. f_T and G_{MAX} plot (Press "a" or "A").

Remarks

The format of the two port S-parameter data file is shown in Table 3. "!" is a comment delimiter used to denote lines with comments within the data file. This is often referred to as the "Touchstone" format which is used by several RF and microwave circuit analysis packages.

QSPLOT was written with Borland's Turbo C++. The graphics drivers for EGA and VGA have been compiled into QSPLOT with the math coprocessor compilation option selected so as to speed upgraphing operations. Unfortunately, the graphics screen dump routine was written by a third party and the licensing agreement precludes the author from including the source code and object files for this aspect of QSPLOT. The source code for QSPLOTL (QSPLOT Light) is included, but does not include the printer source code or the code that reads and generates the configuration file required for printing. There are several sources of already written routines to do graphics screen printing such as the Science and Engineering Tools by Quinn-Curtis which were utilized by the author in QSPLOT.

QSPLOTL may be compiled for use in a computer that is not equipped with a math coprocessor by disabling the math coprocessor option before compilation. Touchstone is a trademark of EESof, Inc.

The latest revision to QSPLOT adds the capability to view input and output stability circles and create files of tabular data for $|H_{21}|^2$, K, G_{MAX}/MSG, conjugate match and stability circles. Also added are conversions from S-parameter to H-, Y-, and Z-parameters.

This program is available from the RF Design Software Service. *See the advertisement on page 145 for ordering information.* **RF**

About the Author

David Lovelace is a staff engineer with the RFIC Development Group at Motorola, Inc. He can be reached at 2100 East Elliot Road, Tempe, AZ 85284. Tel: (602)897-4465. Fax: (602) 897-4477.

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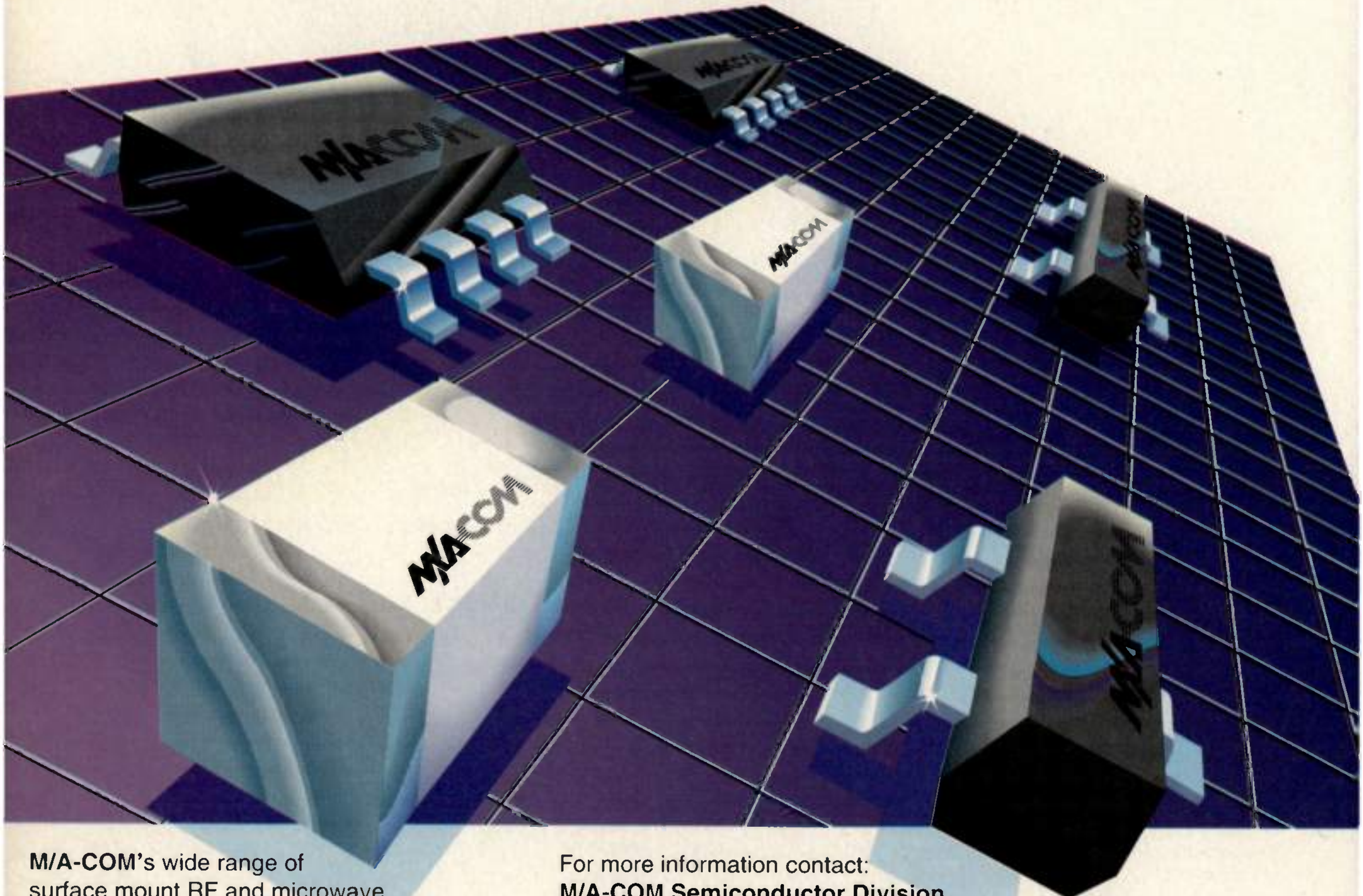

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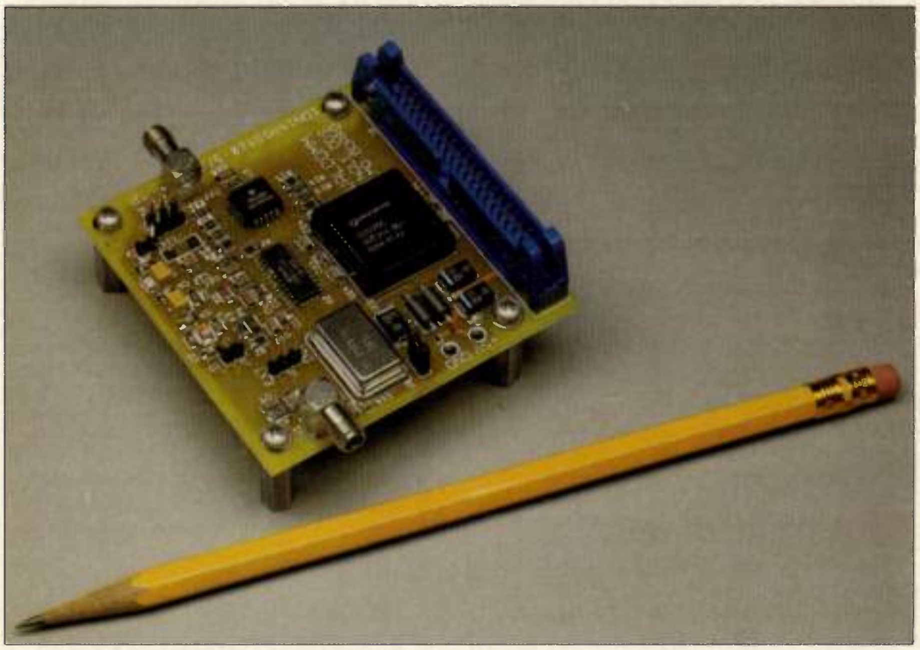
New DDS Keeps Things Simple

By James Madsen
QUALCOMM, Inc

"For never anything can be amiss, when simpleness and duty tender it" — William Shakespeare, A Midsummer Night's Dream.

QUALCOMM's new Q2220 K.i.S.S. (Keep it Simple Synthesizer) DDS adapts advanced 1.0 micron CMOS technology to Shakespeare's timeless truth. The K.i.S.S. DDS is designed to be simple —simple to program, simple to use, simple to frequency modulate, simple to integrate, simple to power, and simple to afford.



The Q2220 is available as a complete synthesizer board, the Q0320-1, with clock, DAC and output filter.

Direct digital synthesizers (DDS) generate a digital waveform, typically a sine wave, by precisely dividing the frequency of a higher speed reference clock signal (see Figure 1). To perform this division, a digital accumulation process adds a fixed delta-phase value to the value of a phase accumulator circuit once per reference clock.

The rate at which the digital accumulator overflows its maximum value is the period of the output waveform. Thus, the period of the waveform is controlled by the digital delta-phase value, also referred to as the "frequency control" value. The digital output values from the accumulator circuit are then converted to a series of digital values that represent a sine wave at discrete time intervals. A standard digital-to-analog converter (DAC) converts this sine representation to the analog domain.

The frequency resolution of the sine wave is a function of the number of bits in the phase accumulator. The spectral purity of the final output signal is a function of the number of bits used in the digital sine conversion process, the number of bits input to the DAC, and the non-linearities associated with the DAC and other analog circuitry. Because the sampled waveform output of the DDS follows the rules of Nyquist's theory, higher frequency images (called "aliases") are also formed in the DDS process. If the fundamental DDS output is the desired signal, then the aliases must be filtered by a suitable low pass filter.

DDS offers numerous advantages over traditional analog synthesis methods: fine frequency resolution, frequency agility, fast switching time, low phase noise and stability. For more information on the theory of DDS, readers are referred to the many articles and application notes which go beyond the intended scope of this article (1,2,3,4,5).

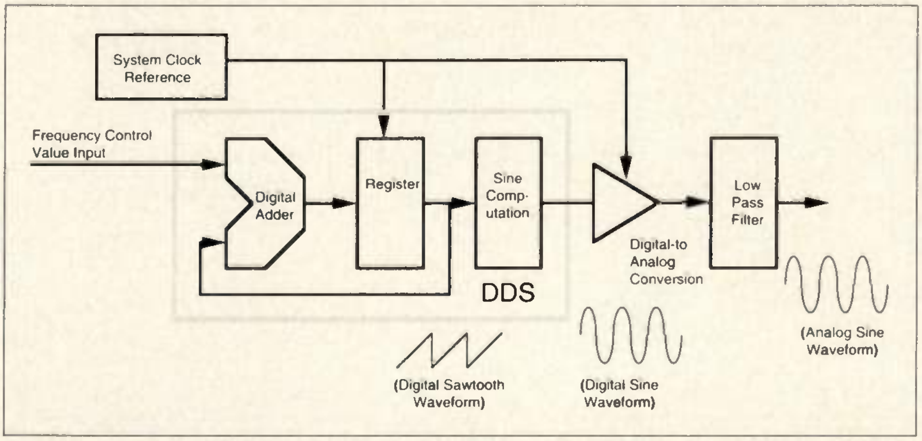


Figure 1. Clock, digital and analog signal flow in the Q2220 DDS.

Making DDS Easier

Despite a wealth of information on direct digital synthesis and the ready commercial availability of single-chip VLSI devices, DDS is still considered an exotic technology by most RF designers.

Existing DDS devices have been seen as too complex in size, power consumption, required support hardware, cost and programming. Moreover, many synthesizer and local oscillator (LO) applications do not require the bells and whistles included on most of today's commercial DDS chips.

RF engineers familiar with phase locked loops, voltage controlled oscillators and other analog techniques need a fresh approach to take advantage of DDS. The value of Qualcomm's Q2220 K.i.S.S. DDS is that it provides a crucial set of competitive advantages for any RF engineer undertaking a new design — faster time to market, lower power budget, smaller size, and lower cost.

The Q2220 has been designed as a basic building block for high volume commercial applications. These applications include portable communication terminals, baseband transmitters and receivers, frequency agile radios, clock generation circuits, frequency synthesizers and digital signal processors.

The commercial uses for DDS seem limitless: HF radios, digital satellite links, very small aperture terminals (VSAT), wireless local area networks (LANs), manpack radios, automated test equipment (ATE), radar, sonar, magnetic resonance imaging (MRI) and global positioning systems (GPS).

K.i.S.S. DDS Architecture

The Q2220 DDS performs direct digital synthesis using a unique combination of features and performance levels that provide very good synthesis performance combined with a very flexible, complete, easy-to-design architecture (see Figure 2). The Q2220 uses a fully parallel digital interface for the control of output signal frequency. This provides the ability to rapidly and easily control the output frequency.

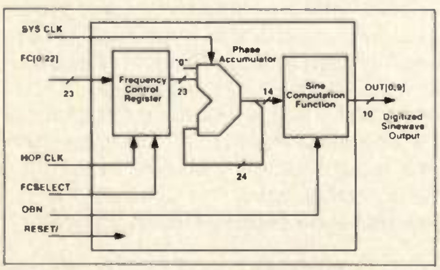


Figure 2. Basic architecture of the Q2220.

The device is packaged in a compact 44-pin PLCC, with the pinout shown in Figure 3. 23 dedicated pins control the output frequency via the frequency control register, which can be loaded asynchronously using the full parallel input and then synchronously activated. Alternatively, the frequency control register can be loaded and activated synchronously with the system clock.

High-speed circuit design allows the device to operate with reference

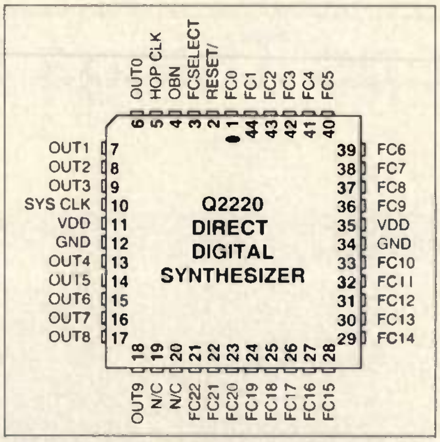


Figure 3. Pin assignments of the K.i.S.S. PLCC package.

frequencies as high as 50 MHz. The rules of Nyquist sampling theory limit the fundamental output frequency to less than half the reference frequency. The design of practical low pass filters further constrains the upper limit of the usable output frequency to about 20 MHz. The lower limit of the output frequency is 0 Hz (see Figure 4).

The Q2220 frequency resolution is a function of the desired reference clock. With a 24-bit accumulator, frequency resolution = reference clock/2^{24}. Therefore, with a 15 MHz reference clock, frequency resolution is <0.9 Hz; or <3.0 Hz at 50 MHz.

The 14-bit sine computation input and

The Q0320-1 DDS Card

A compact 3 inch square (8 cm) turnkey synthesizer based on the Q2220 K.i.S.S. DDS is also available. The synthesizer card includes the DDS, Sony CXD1171M DAC, 33.554432 MHz reference oscillator, buffering for use with external reference clocks, low pass filter elements and connectors (Figure 5). The Q0320-1 card typifies DDS circuit designs.

The card requires only a single 5V supply to operate, with a total power draw of less than 1 W. It includes a 40-pin dual in-line (DIL) header for controlling output frequency, synchronous/asynchronous frequency selection, output formatting, reset and Hop Clock enable, as well as power/ground. Frequency hopping in exact 2.0 Hz binary steps is possible using the on-board reference. The Q0320-1 also includes an input for an external reference, if preferred.

There is a choice of three output signals. The first is an unfiltered sine wave output from the DAC. Using this signal, the alias image of the sine wave can be bandpass filtered to achieve higher frequency outputs.

The second output is the traditional filtered sine wave with a 0-14 MHz bandwidth. This signal is useful for many frequency synthesizer and LO applications.

The third output is a TTL-level square wave. In this mode, the Q0320-1 is a programmable frequency digital clock source; usable for clock recovery and generation circuits, clock rate conversion, or as a programmable source for digital circuits.

The Q0320-1 can be used by itself on the lab bench or in low-to-medium volume OEM applications where it is an economical plug-in synthesizer card.

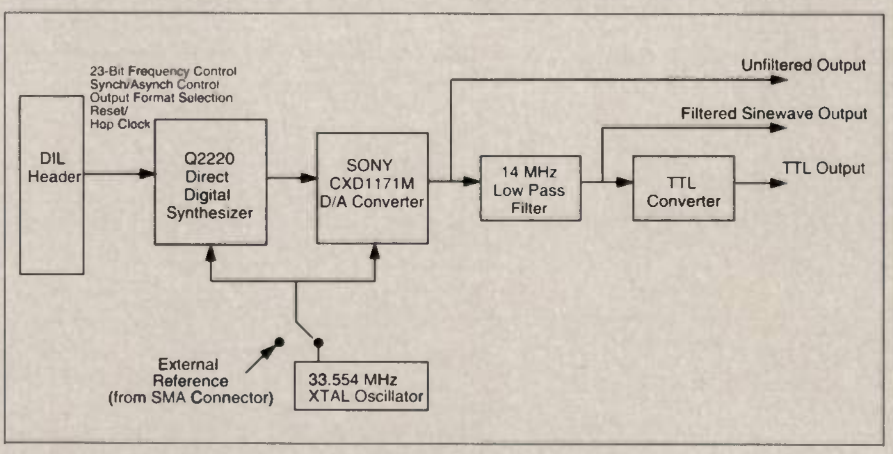


Figure 5. Block diagram of the Q0320-1 synthesizer card.

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	Q2220C-50N	Q2220M-40L
# of DDS Outputs	1	1
Maximum Clock Frequency	50 MHz	40 MHz
Input Interface	Parallel	Parallel
Phase Accumulator Size	24 bits	24 bits
Frequency Resolution	<3 Hz @ 50 MHz	<2.4 Hz @ 40 MHz
# of phase bits to the sine lookup	14 bits	14 bits
# of bits output from device	10 bits	10 bits
Output format	Two's Comp/Offset Binary	Two's Comp/Offset Binary
Clock Latency	5 Clock Cycles	5 Clock Cycles
Standard Package	44-pin PLCC	44-pin CLDCC
Technology	1.0μ CMOS	1.0μ CMOS
Power Consumption	<300 mW @ 50 MHz	<235 mW @ 40 MHz
Operating Temperature	0 to 70C	- 55 to 125C
Availability	From Stock	Fourth Quarter 1992

Figure 4. Specifications of the Q2220 commercial and military versions.

10-bit sine output value provide output spectral purity of better than −60 dBc, depending on the DAC device used for analog conversion.

By fourth quarter 1992, military systems will be able to specify a MIL883C-screened version of the Q2220 DDS in a 44-pin CLDCC package. The MIL version will clock up to 40 MHz from −55 to +125C and 4.5 V $\leqslant V_{dd} \leqslant$ 5.5 V.

Why the Q2220 K.i.S.S. DDS is Simple

Simple to program — The Q2220 uses a fully-parallel frequency control interface which provides total flexibility over the output frequency as well as its rate of change. The parallel interface provides frequency loading in a single clock cycle versus a typical 24-clock delay for serial interfaces.

For a fixed output frequency, the 23-bit frequency control interface can be hardwired by tying the input pins high or low. Alternatively, simple DIP switches or similar techniques can be used to manually control frequency selection. For fast, automatic frequency selection, digital control circuitry can generate the 23-bit frequency value.

The input value can be loaded and activated synchronously with the system clock signal. An asynchronous load mode is also supported whereby the frequency control value is loaded and activated by an asynchronous signal (HOPCLK) which is internally synchronized to the system clock signal.

Simple to use — The Q2220 DDS requires only an external clock reference (0-50 MHz), DAC and low pass filter components to operate. Based on QUALCOMM's ongoing evaluation of DACs, the 40 MHz Sony CXD1171M CMOS DAC has shown to be an excellent low-cost companion to the Q2220 providing typical system-level spurious less than −50 dBc. For even higher performance, more sophisticated DACs (e.g. Sony CX20202) can be specified to

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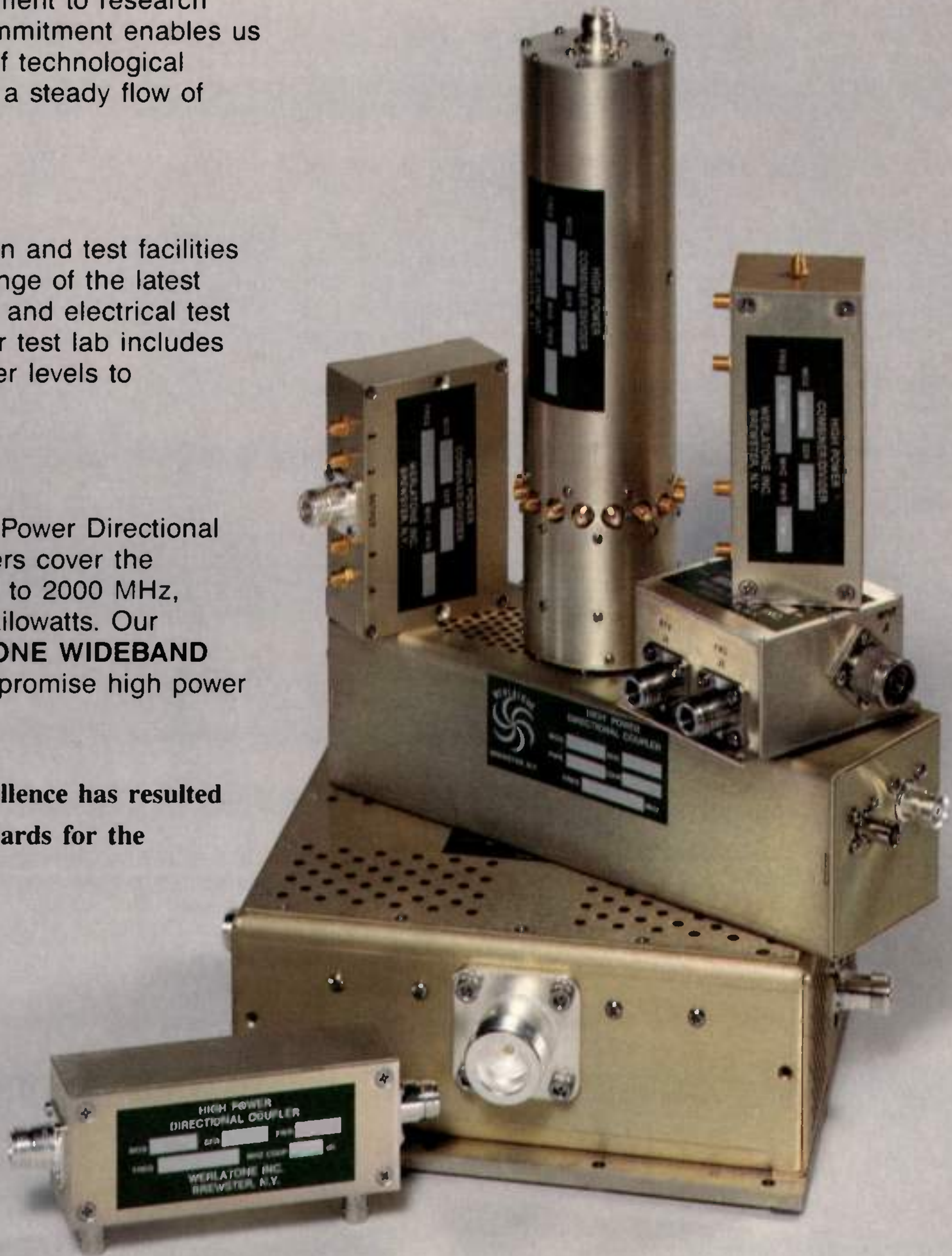

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INFO/CARD 72

achieve spurious levels better than −60 dBc.

Simple to frequency modulate — Frequency hopping, frequency modulation and chirp (linear frequency sweep) are all easily controlled. Because the Q2220 can update frequencies as fast as the clock in synchronous mode, frequency changes as fast as 50 MHz are feasible. Even in asynchronous mode, frequency changes at 33 percent the clock rate are possible. Moreover, pipeline delay is a minimal 5 clock cycles.

Simple to integrate — Designing with the Q2220 requires little associated hardware, which in turn supports tight product design cycle times. The available Q0320-1 DDS Card (see sidebar) is a turnkey synthesizer requiring only +5 V to operate with less than 1 W power consumption.

Simple to power — Whether for handheld terminals, manpack radios or battery powered equipment, power consumption is crucial. With its low power 1.0 u CMOS design, the Q2220 DDS draws less than 300 mW worst case with a 50 MHz reference clock.

Simple to afford — The Q2220 K.i.S.S. DDS has a very low price. Even more importantly, from a system standpoint, the Q2220 provides true value. A good quality straightforward DDS/DAC synthesizer system can be achieved for about $20 in quantities in the low 1000s.

Summary

With the Q2220 K.i.S.S. DDS, RF engineers can finally take advantage of the promise of direct digital synthesis for cost-sensitive, commercial applications. High volume systems which previously found DDS technology to be too expensive or complex can incorporate the small package size, simple interface, high signal quality and low power consumption of the Q2220 DDS IC and Q0320-1 DDS card.

For more information on this product, contact QUALCOMM VLSI Products Division or circle Info/Card #145. **RF**

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2. Earl McCune, Jr., "Digital Communications Using Direct Digital Synthesis," *RF Design*, January 1990.
3. "DDS Technology Fulfills Promise of Speed and Accuracy," *Microwaves & RF*, September 1989.
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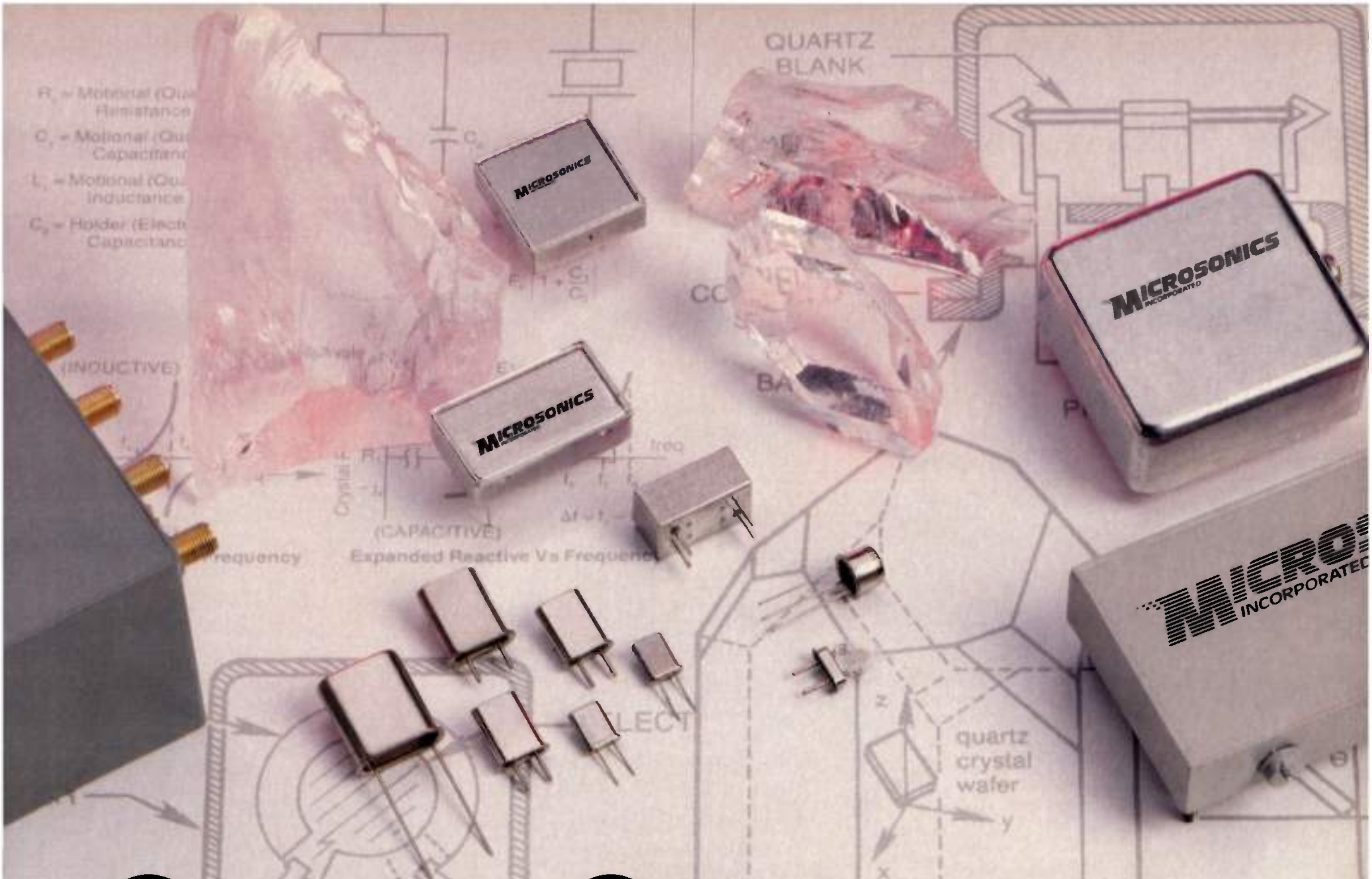
5. "Digital Frequency Synthesis Sharpens Modulator's Tune," *New Electronics*, June 1991.

About the Author

James Madsen is Manager, Business Development for QUALCOMM's VLSI Products Division. He has been with the company for three years and holds a BSME from Massachusetts Institute of Technology and an MBA from Stanford University. He may be reached at QUALCOMM, 10555 Sorrento Valley Road, San Diego, CA 92121, tel. (619) 597-5005, Fax (619) 452-9096.



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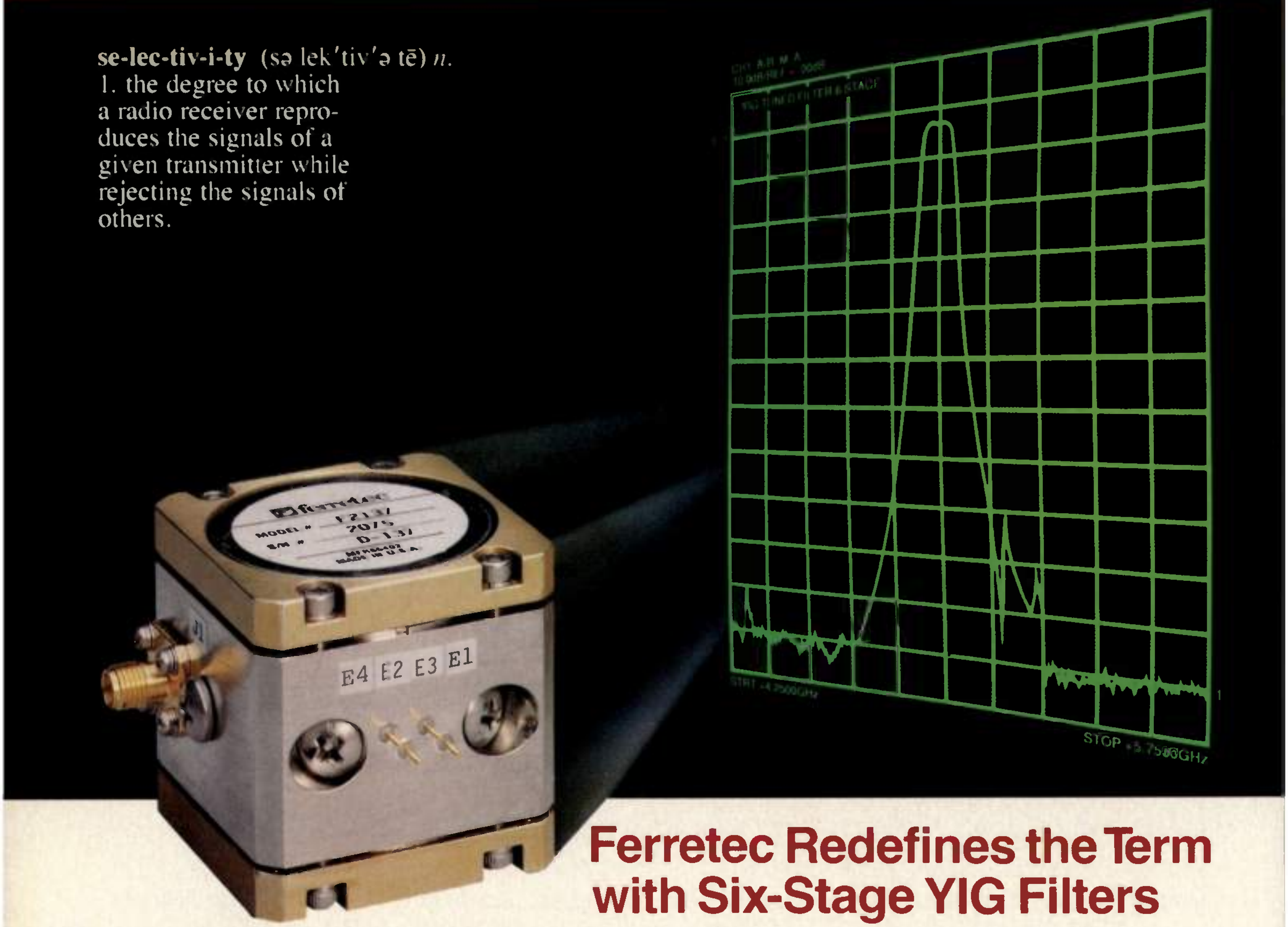

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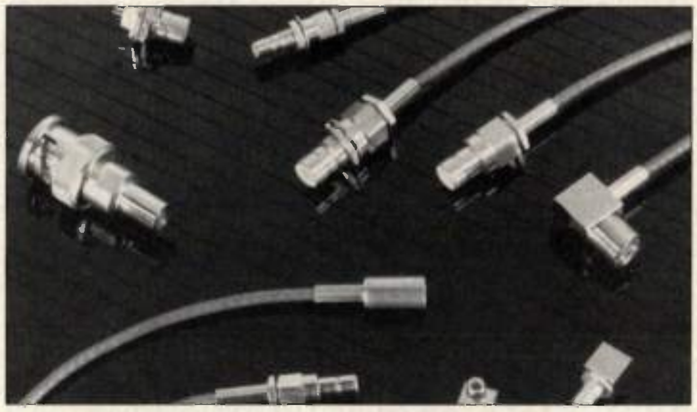
SMB Subminiature Connectors Feature Quick Operation

New SMB subminiature coaxial connectors from AMP Inc. provide high frequency point-to-point or board-to-board interconnection. Featuring quick connect/disconnect capability, this connector line is intended for applications in cellular telecommunications, test and instrument systems, medical electronics, CAD/CAE systems, and computing equipment. Connectors are available in 50 and 75 ohm impedances, and in commercial and military versions. Mechanical features include low mating/unmating force and high reliability.

Low VSWR performance extends to 4 GHz, with contact current rating of 1.5 amp DC and a temperature rating from −65C to +165C. The connectors conform to MIL-C-39012 with a durability rating of 500 cycles. Styles available include straight and right angle plugs, jacks, bulkhead jacks, printed circuit board jacks and adapters. Prices range from $2.50 to $3.25 each, depending on quantity. Delivery time is 8 weeks after receipt of order.

Amp Incorporated
INFO/CARD #186



Network Analyzer Gets Upgrades

Wiltron announces the 360B Vector Network Analyzer, a major upgrade to its previous 360 model. The unit measures S-parameters, gain, phase and group delay characteristics of many microwave components, systems and subsystems. Other features include frequency coverage of 10 MHz to 62.5 GHz in coax and 110 GHz in waveguide, 20 ns pulsed RF testing and noise figure testing. New features include display of a fourth color to overlay traces, additional display markers and limit lines, and other display options. Additional calibration options are included, along with a new Automated Flat Port Power Correction for accurate amplifier compression and absolute power level measurements. New disk storage capabilities have been added and a growing selection of test fixtures provide measurement flexibility.

Wiltron Company
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HF Intercept Receiver/DF Unit

The MD 500 Series of intercept and direction finding (DF) receiver/processors and antennas is announced by Maxim Technologies. The units are designed for fast acquisition and accurate DF of co-channel interference in the unique 2 to 30 MHz HF signal environment. The equipment uses an adaptation of the single-channel interferometer DF technique for accurate and economical operation. Typical accuracy is 1 degree and sensitivity of 0.5 uV/m. The family includes the MD-510A processor and display unit that works with an existing digitally-controlled HF receiver, the MA-501 antenna array (8 eight-foot monopoles) for portable or fixed sites, and the MA-551 mobile DF antenna, occupying only a 14×14×2 inch space.

Maxim Technologies, Inc.
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Quadraphase Modulator Supports High Data Rates

The Model IQM 134-432CD from TRM features a built-in CMOS HCL compatible driver for QPSK modulation of an RF signal at 432 MHz with a bandwidth of 10 percent. Input data rates up to 40 MHz and clock rates to 20 MHz provide modulated outputs with amplitude balance of ±0.5 dB and phase accuracy of ±5 degrees. Conversion loss is typically 8 dB (9 dB maximum) and VSWR is less than 1.5:1. Other center frequency and bandwidth options are available, with or without the driver circuitry. The device is packaged in a 1×1×0.15 inch flatpack with either axial or radial leads. SMT and connectorized packages are also available.

TRM, Inc.
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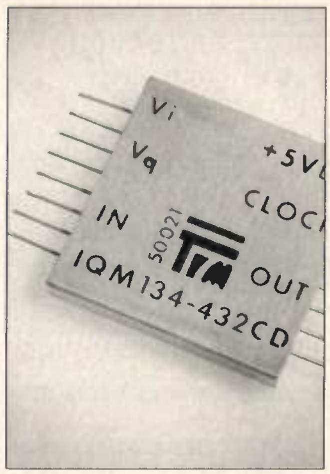

Atomic Clock Keeps Precise Time

Hewlett-Packard's new HP 5071A Cesium II primary frequency standard keeps time to 1 second in 1.6 million years. As a metrology standard, the HP 5071A can be used to calibrate navigation systems, broadcast communications, and astronomical measurements. Cesium-beam technology synchronizes a microwave oscillator to the vibration of Cesium 133 atoms. The new techniques incorporated into this product include an improved Cesium tube design and advanced microprocessor-based controls. These improvements were developed to improve long-term accuracy, as well as provide a fast 30-minute warmup time. Pricing is $54,000, with an optional high performance tube ($\pm 1 \times 10^{-12}$ accuracy) an additional $12,000.

Hewlett-Packard Company
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SEMI-CONDUCTORS

Low Noise Bipolar

The new low noise silicon bipolar transistor B12V105 is introduced by Bipolarics. This device is suited for low power battery applications as an oscillator or amplifier. f_T is greater than 10 GHz with collector currents of 10 to 25 mA. S21 is 19 dB or more at 1 GHz, and is still 16 dB at just 5 mA. Noise figure at 900 MHz is less than 1.6 dB. Various packaging options are available and pricing begins at $0.99 in 1000 qty.
Bipolarics Inc.
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2 ns Comparators

High speed ECL comparators resolve signals as small as 3 mV, with 2 ns propagation delay. The device can be clocked at up to 500 MHz for fast line receivers, threshold detectors and triggers. Separate analog and digital power supplies reduce noise. Pricing (1000s) is $3.98 for the single MAX905CPD, $5.88 for the dual MAX906CPE.
Maxim Integrated Products
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Digital Video MUX

The multiplexing/demultiplexing of digital video components is achieved in the SCX6244EFC developed by the Independent Television Consortium in England, and marketed in the U.S. by Allen Avionics. The chip performs the conversion between multiplexed signals sampled to CCIR Rec. 601 and the 27 MHz parallel interface format of CCIR Rec. 656 (SMPTE RP. 125).
Allen Avionics, Inc.
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Programmable FIR Filter

A single-chip programmable filter processor operates at speeds up to 40 MHz for video and other high speed digital filtering requirements. The MC27HC68 has static programming of filter coefficients, and includes EPROM lookup tables and a quartz lid for reprogramming. In 1000 quantity, a 30 MHz version costs $59.00. A PC-based development system is priced at $1,800.
SGS-Thomson Microelectronics
INFO/CARD #178

1:2 Analog Multiplexer

An analog multiplexer for radar, imaging, HDTV and instrumentation applications is announced by Comlinear. The CLC532 switches in 17 ns, with 80 dB channel isolation, and harmonics −80 dBc. Buffered inputs and outputs provide easy interface. In 1000s, prices start at $13.00.
Comlinear Corporation
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CABLES & CONNECTORS

Flexible Cable Assemblies

C. Itoh Technology introduces a new series of DC-18 GHz flexible cable assemblies in 0.170 inch diameter. and 50 ohm impedance. The cables are temperature tested at −55 to +125C, and have PTFE insulation and jacket. Connector options include SMA (straight and right angle) and type N.
C. Itoh Technology, Inc.
INFO/CARD #176

Micro Connector

A new microminiature connector is introduced by Huber+Suhner. The push-on MMCX connector has a non-slotted outer conductor and operates to 26 GHz with less the 1.15:1 VSWR. Designs are available for flexible and semirigid cables as well as p.c. board mounting.
Huber+Suhner, Inc.
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Cable Matching Services

Storm Products now offers phase and amplitude matching services for their microporous line of cables. Cables may be matched to an absolute insertion phase or to a standard. Typical phase tolerances are ±1 degree/GHz, with tighter tolerances available.
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Field Replaceable Connectors

Solitron/Microwave announces a complete line of field replaceable connectors, including SMA

tow and four-hole flanges, jacks and plugs. Glass seals and various pin terminations are also included.
Solitron/Microwave
INFO/CARD #173

Precision Adapters

Ruggedized SMA connector adapters are introduced by Lucas Weinschel. Male-male, female-female models are available, and all adapters have auxiliary wrench flats for easy torquing with multiple hookups.
Lucas Weinschel
INFO/CARD #172

SUBSYSTEMS

E-Field Antenna

The SAS-220/CR from Antenna Research Associates is a 20-2000 MHz E-field receiving antenna designed around the discone principle. Dimensions are small to maintain a single wide lobe aimed at the horizon. The integral active network will tolerate levels up to 100 V/m. Individual calibrations are available.
Antenna Research Associates, Inc.
INFO/CARD #171

Wireless Network Terminal

A 902-928 MHz spread spectrum data communications unit, GINA (Global Integrated Network Access), is introduced by GRE America. Full power to the allowable 1 watt maximum provides coverage of up to three miles. The unit uses error-checking data packets to assure accurate transmission.
GRE America, Inc.
INFO/CARD #170

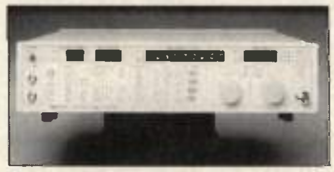
Antenna Ice Detector

A new low cost control unit for antenna de-icing heater control is announced by Environmental Technology. When ice, sleet or snow is detected at temperatures between 18 and 38F, the control is activated for one hour.
Environmental Technology, Inc.
INFO/CARD #169

TEST EQUIPMENT

Synthesized Generator

A synthesized signal generator that is programmable for automatic test applications is announced by Panasonic Factory Automation. The VP-8311A covers 100 kHz to 1.04 GHz with



output levels from −127 to +19 dBm (under 160 MHZ). 55 ms settling time allows rapid measurements, and specifications of .03 percent distortion and −120 dBc phase noise demonstrate the unit's spectral purity. The price is $7200.
Panasonic Factory Automation
INFO/CARD #168

Coaxial Impedance Bridges

Wide Band Engineering Co. has added two new impedance bridges to its line, intended primarily for return loss testing of coaxial cables. Model A56UTD covers 1-900 MHz with 40 dB directivity (1.02:1 VSWR), with minimum of 45 dB directivity up to 500 MHz. Model A56UTD/S has 40 dB directivity to 1000 MHz. Both units come with a precision fixed termination and measured lab data. Each is priced at $792.00.
Wide Band Engineering Co., Inc.
INFO/CARD #167

Enhanced Waveform Analyzer

A new DSP board for the Analogic Model 6100 Waveform Analyzer increases performance by a factor of 300. 8k point FFT is computed and displayed in milliseconds. 16k by 16k cross-correlation analyses take one second. Auto-correlations, convolu-

tions and averaging are computed at high speed. The Model 683 option is priced at $2995, and is user-installable in the Model 6100.
Analogic Corporation
INFO/CARD #166

Comb Generators

The Series 95 Comb Generators from EMF Systems use step recovery diode techniques to generate harmonics spaced from 10 to 1000 MHz, with crystal stabilized drive frequencies. Harmonics of the 1000 MHz version have a level of −12 dBm at 18 GHz. Applications include receiver and antenna testing.
EMF Systems, Inc.
INFO/CARD #165

Event Timing Controller

Guide Technology announces a PC-compatible plug-in board for timing control and monitoring applications. The GT401 contains a fast real-time clock (1 us resolution), four I/O channels for pulse output or time tagging, and three 10 MHz 16 bit timer/counters for general use. Applications include measuring travel time of waves or objects. Price is $995.
Guide Technology Inc.
INFO/CARD #164

Hysteresis Measurement

AC properties of magnetic materials can be measured with the new Walker Scientific AMH-400 Computerized Hystersisgraph. Measurement frequencies

are from 50 kHz to 1 MHz, with a hysteresis loop run in 30 seconds and plotted on a high resolution monitor. Measured parameters include B_r, H_c B_{MAX}, μ_p, peak secondary voltage and phase lag between primary and secondary. Pricing is from $17,900 including a PC/AT compatible computer.
Walker Scientific Inc.
INFO/CARD #163

Pulse Modulator Timing

Flam & Russell announces a new timing unit to provide TTL pulses to its low frequency (0.1-2.0 GHz), high frequency (2-18 GHz) and millimeter wave pulse modulator systems. These products are used in gated-CW instrumentation radars which measure radar cross-section (RCS). A full range of pulse characteristics, plus complete programmability and control features are included.
Flam & Russell Inc.
INFO/CARD #144

AMPLIFIERS

Amplifier for PCN

Wessex Electronics announces five new amplifiers for PCN and other applications in the 1.7-1.9 GHz range. Models provide 2 to 25 watts power output in linear Class A. The ANO-0112S 25 watt unit offers 35 dB gain from 1.805-1.880 GHz with −50 dBc harmonics and −80 dBc spurious signals.
Wessex Electronics
INFO/CARD #143

Power Module for Cellular

Toshiba has introduced an 825 MHz GaAs FET RF power amplifier module designed for U.S. handheld cellular telephone applications. The new S-AU55 offers a small-size (17×12×4 mm) solution for these products, providing 1.12 watts minimum power output with 4 mW input with a 5.8 V supply. The device is priced at $36.50 for 1000-3000 pieces.
Toshiba America Electronic Components
INFO/CARD #162

D-Band Amplifier

A solid-state replacement for TWT amplifiers in the 1.0 to 1.5 GHz band is offered by Systron Donner. The 100-watt amplifier has 40 percent bandwidth and 45 dB minimum small-signal gain.
Systron Donner
INFO/CARD #161

Low Noise Amplifier

A wideband low noise amplifier for 5-300 MHz applications is announced by Miteq. The AU-

1021 has 25 dB nominal gain with 0.5 dB flatness, +20 dBm output at 1 dB compression, and a noise figure of 2.5 dB maximum (2.2 dB typical). 15 V power is required at 175 mA.
Miteq
INFO/CARD #160

DISCRETE COMPONENTS

New Inductor Line

Ohmite manufacturing announces its entry into the inductor component market with a range of miniature high current molded and toroidal RF chokes. Available in values from 10 uH to 1000 uH, models are offered in vertical and horizontal mount configurations. Pricing is in the $1.00 to $2.00 range.
Ohmite
INFO/CARD #159

Capacitors for Switch-Mode Supplies

A series of metallized polycarbonate film capacitors has been introduced by Electronic Concepts. This line offers smaller size over standard components, and are available in 30, 50, 75 and 100 VDC ratings, intended for use in switch-mode power applications.
Electronic Concepts, Inc.
INFO/CARD #158

Axial Lead Chokes

Coilcraft's new 90 Series axial lead chokes are designed for high volume applications. 49 values from 0;.1 to 1000 uH are offered, with 3, 5 and 10 percent tolerances available. The chokes are epoxy coated and are marked with EIA standard color code.
Coilcraft
INFO/CARD #157

SIGNAL PROCESSING COMPONENTS

BAW Delay Lines

Teledyne Microwave announces BAW delay devices for radar altimeter self-test or altitude reference applications. The MBG-2000 Series provide 0.610 us delay simulating a 300-foot altitude. Peak power levels of 0.1 to 0.5 watts are available.

Teledyne Microwave
INFO/CARD #156

Screw-in Terminations

A series of flush-mount screw-in terminations are available to handle 1, 5 or 10 watts. For more secure mounting than press fit models, these terminations lock in with the threads. DC-18 GHz coverage is specified with maximum VSWR of 1.3:1 at 18 GHz. Cost is $10.00 each in 100 quantity.
EMC Technology, Inc.
INFO/CARD #155

SMT Mixer

A tiny .25×.25 inch mixer for 5-18 GHz applications has been announced by Avantek. The PPM-1852L is a double-balanced mixer with a DC coupled IF port with DC-1 GHz bandwidth. LO power requirement is +10 dBm. Pricing is $146.00 in 100-piece quantities.
Avantek, Inc.
INFO/CARD #154

Constant Phase Attenuator

Daico Industries' new CDS0867 is a broadband constant phase attenuator in an SMA connectorized housing. The seven-section unit covers 10-1000 MHz with a LSB attenuation of 0.5 dB, providing 63.5 dB attenuation range. Switching speed is 27 ns and power supply requirements are +5 VDC at 3 mA.
Daico Industries, Inc.
INFO/CARD #153

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✓	Model No.	Frequency Response	SS Gain (dB) Min.	Flatness (dB) Max.	Noise Figure (dB)	PO@ 1dB C (dBm) Min.	IP3 (dBm) Min.	VSWR In/Out	VDC	Current (mA)	Case/ Connector
	Wide Band / Low Noise Amplifiers										
	W50ETC	10KHz—50MHz	24	±.5	5.3 Typ 6.0 Max	+23		2:1	+15	125	E-75/BNC
	W50ATC	10KHz—50MHz	50	±.5	1.3 Typ 1.5 Max	+ 5		2:1	+15	25	C-75/BNC
	W110F	5MHz—110Mhz	55	±.5	1.1 Typ 1.2 Max	+15		2:1	+15	80	C/SMA
	W110H	5MHz—110MHz	30	±.5	1.2 Typ 1.4 Max	+ 5		2:1	+15	30	C/SMA
	W500K	1KHz—500MHz	30	±1	1.7 Typ 2.2 Max	+ 3		2:1	+15	25	C-75/BNC
	W500C	5MHz—500MHz	40	±.5	1.4 Typ 1.6 Max	+10		2:1	+15	50	C/SMA
	W500H	5MHz—500MHz	33	±.5	1.2 Typ 1.4 Max	+ 5		2:1	+15	25	C/SMA
	LF836C	821MHz—851MHz	44	±.5	1.2 Typ 1.5 Max	+19		2:1	+15	150	SPEC/SMA
	W1G2M	10KHz—1000MHz	30	±1	2.0 Typ 3.0 Max	+ 5		2:1	+15	35	C-75/SMA
	W1G2H	5MHz—1000MHz	30	±.5	1.3 Typ 1.5 Max	+ 5		2:1	+15	40	C/SMA
	W15GB3	50MHZ—1500MHZ	30	±.5	1.8 Typ 2.0 Max	+ 5		2:1	+15	50	C/SMA
	W2GH	500MHz—2000MHz	22	±1	4.0 Typ 4.5 Max	+ 5		2:1	+15	30	C/SMA
	WFR1-4GA-14	100MHz—4000MHz	28	±1	3.5 Typ 4.0 Max	+14		2:1	+15	175	A-75/SMA
	Medium Power Amplifiers										
	P150D	35KHz—150MHz	27	±.5	5.0 Typ	+30	+40	2:1	+24	400	H/SMA
	P500A	2MHz—500MHz	37	±.5	4.5 Typ	+30	+40	2:1	+24	500	H/SMA
	P500L	5MHz—500MHz	17	±.7	10 Typ	+30	+40	2:1	+24	420	H/BNC
	P1GB	50MHz—1000MHz	30	±1	5.5 Typ	+30	+40	2:1	+20	800	A-S/SMA
	P2GF-1	1MHz—2000MHz	32	±1	10 Typ	+30	+40	3.5:1	+15	1000	FW1/SMA
	P2GF-2	10MHz—2000MHz	32	±1	7.5 Typ	+30	+40	2:1	+15	1000	FW1/SMA
	P42GA-29	.5GHz—4.2GHz	30	±1.5	6.5 Typ	+29	+39	2:1	+20	1200	FW1/SMA
	High Power Linear Amplifiers										
	P300AM-33	3MHz—300MHz	33	±.5	10 Typ	+33/2W	+43	2:1	+24	1000	Y-B-S/BNC
	P1400M-37	400—1400MHz	20	±1	N/A	+37/5W	+47	2:1	+24	2500	Y-D/SMA
	PF19GA-40	1700—1900MHz	30	±1	N/A	+40/10W	+50	2:1	+24	5000	Y-D/SMA
	P1020-40	1000—2000MHz	27	±1	N/A	+40/10W	+50	2:1	+24	5000	X512/SMA

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cuits with line widths as small as 20 microns. Metallo-organic Au conductor pastes are used in this printing process, with epoxy-graphite material used for lift-off of non-conducting areas.
Electro-Science Laboratories
INFO/CARD #152

RF/Microwave Packages

Hermetic Devices now offers RF/microwave packages for amplifiers, mixers, switches and other products. The company offers in-house machining, metalforming, plating and assembly services.
Hermetic Devices, Inc.
INFO/CARD #151

Fiberglass Laminate

Copper clad laminate from Compositech combines epoxy resin and standard E-glass reinforcement for 30 percent greater flexural strength than typical woven laminates. Continuous, parallel, untwisted fibers contribute to uniform surface characteristics.
Compositech Ltd.
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SIGNAL SOURCES

New VCOs

The Emhiser VCO series offers a minimum of +10 dBm output in models covering from 11 MHz to 4.5 GHz. Various bandwidths up to an octave are offered. High Q hyperabrupt varactors are used for low noise and linearity. TO-8, surface mount, flatpack and connectorized packages are available.

Emhiser Micro Tech
INFO/CARD #149

Frequency Synthesizers

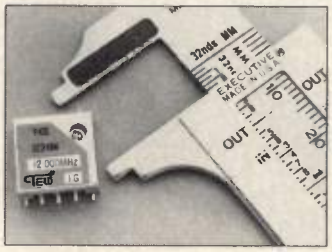
The FSR-90000 series frequency synthesizers are designed for radar and C3I systems, signal simulators and ATE. A typical unit covers 2000-2500 MHz in 25 kHz steps with 1 ms switching speed. Power output is +10 dBm with −60 dBc spurious and −40 dBm harmonics. Higher frequencies are available.
Micronetics
INFO/CARD #148

Wide Deviation VCXOs

Reeves-Hoffman announces the hybrid VCXO series 3159, designed for communications and instrumentation applications. The units are available in 30.0 to 80.0 MHz, with total frequency change of ±160 ppm from nominal frequency. Approximate pricing is $49.00 in 250 quantity.
Reeves-Hoffman
INFO/CARD #147

Miniature VCTCXO

Tokyo Denpa had developed the TXS 1224 voltage controlled temperature compensated crystal oscillator in a surface mount



package occupying 0.7 cc volume. Frequencies in the range of 12.8 to 26 MHz are offered for applications in N-AMPS and dual mode cellular handheld telephones. Pricing is $21.00 in OEM quantities.
TEW North America
INFO/CARD #146

An Improved FM Exciter Using Direct Digital Synthesis

By Thomas Hack
Comlinear Corporation

This article was an entry in the 1991 RF Design Awards contest. It describes a direct digital synthesis FM exciter that offers advantages over traditional analog techniques.

A variety of techniques have been used over the years for producing FM signals for commercial broadcasting. The Armstrong method, direct FM, serrasoid modulation and others have been used, each with some or all of the following tradeoffs. First, the basic modulator may have low deviation and must be followed by a series of frequency multipliers to increase the deviation. In the process, filters are required to extract the proper harmonic from each frequency multiplier stage. Group delay and amplitude characteristics of the filter become important. Circuit complexity can be high. The modulator must also be stabilized either with frequency-locked or phase-locked loops. Aging and temperature coefficients must be dealt with in large portions of the circuit. Finally, integrating all of the analog circuitry into a few chips while getting full functionality and performance is difficult. Reliability, size, cost and weight could be better.

A direct digital synthesis based FM exciter should lessen these problems. Deviation can be made extremely wide without resorting to a chain of frequency multipliers. The upper frequency deviation limit is reached when significant components of the resulting sideband structure exceed Nyquist's bandwidth in the exciter. With sample rates of tens or hundreds of megasamples/second, very large deviations are practical. The center frequency stability of the exciter can easily be made equal to the main reference oscillator. Very little of the required circuitry is analog, so aging and temperature coefficients play a part in only a fraction of the total exciter circuitry. Since most of the exciter is digital and digital circuitry can be densely integrated, the exciter consists of very few integrated circuits and a small handful of analog components. This makes it reliable, small and lightweight. This advantage will increase as more highly integrated DDS components become available.

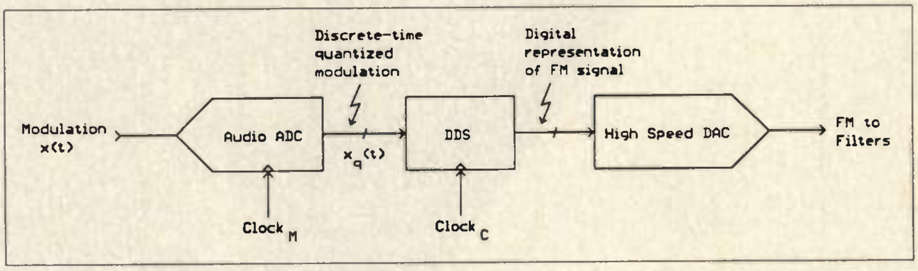


Figure 1. Simplified DDS-based FM exciter.

To test these concepts, a simple monophonic FM exciter with more than 20 kHz audio bandwidth and approximately 75 kHz peak frequency deviation was developed.

Discrete-Time Frequency Modulation

In DDS-based frequency modulation, audio is sampled with an analog-to-digital convertor (ADC) which updates the instantaneous frequency of a direct digital synthesizer (DDS). The DDS sends a digital representation of an FM signal to a high speed DAC where the final analog RF output is produced (Figure 1). Analog filtering follows the DAC, eliminating a variety of sampling artifacts.

The modulation applied to the DDS and the FM signal produced by the DDS are discrete-time signals (sampled). It is desirable to keep the sampling rate of the ADC ($Clock_m$) as low as possible to keep ADC costs low. The FM signal needs to be produced at the DAC at higher sample rates, $Clock_c$, because of a variety of $Clock_m$ products.

Determining the Modulation Sample Rate

At first it might appear that $Clock_m$ could be set strictly from Nyquist's sampling theorem and the maximum modulating frequency. As will be shown in the following simplified analysis (based on single-tone modulation), the required modulation sample rate, $Clock_m$ is actually much higher for a wideband DDS-based exciter.

An FM signal theoretically has infinite bandwidth, but in practice the bulk of the spectral energy occurs in a bandwidth (centered about the carrier in the case of single tone modulation) given by Carson's rule:

$$BW = 2(F_{mod} + F_{dev}) \qquad (1)$$

The FM signal occupies the greatest bandwidth when both the peak frequency deviation, F_{dev}, and the modula-

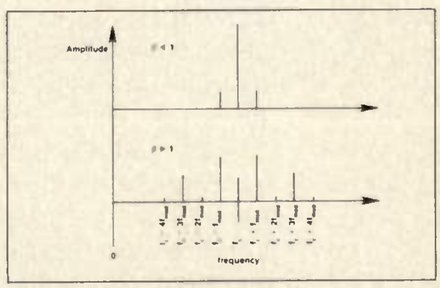


Figure 2. Single-tone FM spectra (simplified).

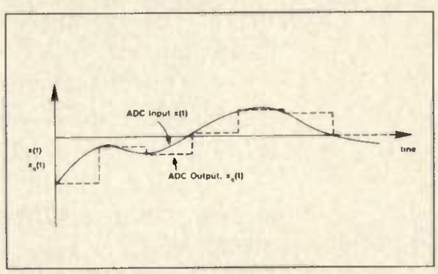


Figure 3. ADC input and output.

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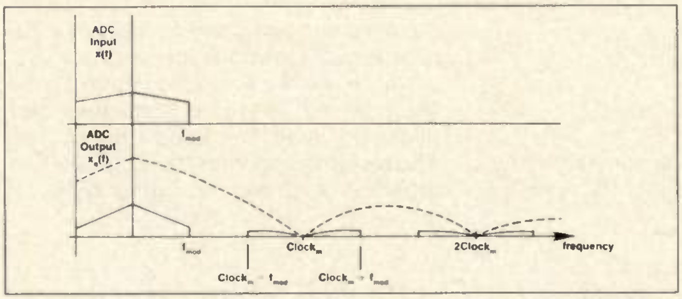

Figure 4. Frequency domain representation of Figure 3.

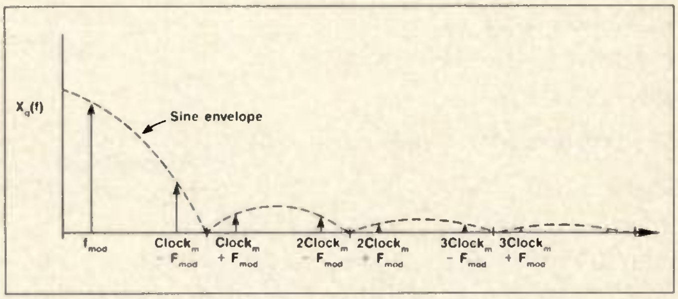

Figure 5. Spectrum for $x_q(t)$ when $x(t) = \sin(2\pi F_{mod}t)$.

tion frequency, F_{mod}, are highest.

The FM spectrum for single tone modulation consists of a carrier and modulation sidebands located at:

$$F_{sideband} = F_c \pm NF_{mod}, \quad N = 0, 1, 2 \ldots \qquad (2)$$

The amplitude of each sideband and the carrier is given by Bessel functions of the first kind:

$$A_N = J_N(B) \qquad (3)$$

where B is the modulation index:

$$B = \frac{F_{pk}}{F_{mod}} \qquad (4)$$

F_{pk} is the peak frequency deviation and F_{mod} is the frequency of the modulating tone. As shown in Figure 2, only the first-order sidebands are significant for low modulation indices. As B is increased, higher-order sidebands become more important. In general, the larger the modulation index, the smaller the amplitude of each sideband (and the carrier). The reason for this is that the total power (in the carrier and the sidebands) stays the same regardless of B but the number of significant spectral lines (sideband and carrier) increases. The result: the same power is distributed over more spectral lines but there is less power (on average), for each.

With the groundwork laid, we can now look at a DDS-based FM exciter. Referring back to Figure 1, the ADC produces the signal $x_q(t)$ from the input x(t). The ADC output can be modeled as the ADC input signal passed through an ideal sampler, a zero-order hold and an amplitude quantizer. Ignoring quantization, a representative signal looks like Figure 3. The same signal when viewed in the frequency domain (Figure 4), consists of the original modulating frequency (main tone) plus images of the modulating frequency and the sample clock. The magnitude of all main signals and images is affected by the frequency response of the zero-order hold:

$$|H(f)| = \text{sinc}\left(\frac{\pi F}{clock_m}\right) \qquad (5)$$

For the single tone modulation, the spectrum $X_q(f)$ looks like Figure 5. This multitone signal produces rich cross modulation terms in the FM spectrum:

$$F_{sideband} = F_c + \sum_{N=-\infty}^{\infty} I_N(F_{mod} + NF_{clockm}) \qquad (6)$$

Some of these terms will fall in the range of frequencies where our desired signal occurs. Fortunately, many of these terms are extremely small and can be temporarily ignored. The main concern is to insure that undesired cross modulation sidebands that fall within the vicinity of the desired FM signal don't have enough power to corrupt the desired signal. Terms which are further away can be filtered out.

Let's simplify the analysis by looking at only F_{mod} and the first alias: $Clock_m - F_{mod}$. We can do this because these produce the only significant cross modulation terms that land close to the desired FM signal. We can describe the resulting two tone FM spectrum by:

$$s(t) = \cos(a + b)$$
$$= \cos(a)\cos(b) - \sin(a)\sin(b) \qquad (7)$$

where,

$$a = \omega c\left(\frac{t}{2}\right) + B_1\cos(\omega_{mod}t) \qquad (8)$$

and

$$b = \omega c\left(\frac{t}{2}\right) + B_2\cos((\omega_{clock} - \omega_{mod})\,t) \qquad (9)$$

B_1 and B_2 are the modulation indices for F_{mod} and the first alias. B_2 will be substantially less than B_1 because the alias is suppressed by the sinc envelope of the zero-order hold (see Figure 5) and because the alias is at a much higher frequency than F_{mod} (see Equation 4). The result of each term acting alone and together is shown in Figure 6. B_2 is

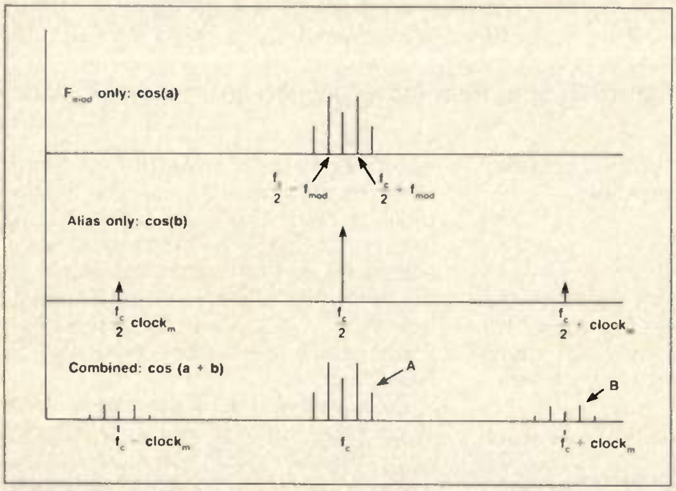

Figure 6. F_{mod} and the first alias acting alone and together.

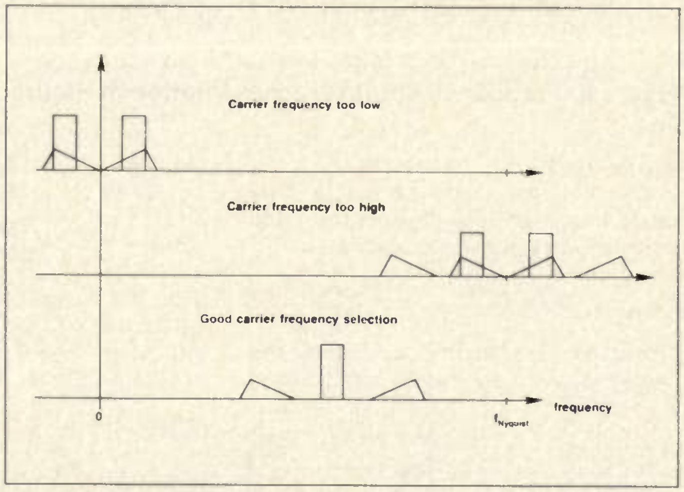

Figure 7. Center frequency selection.

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		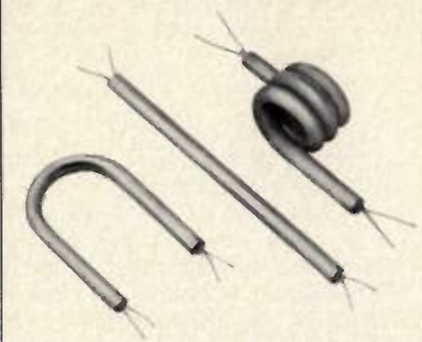 WIRELINE	 WIREPAC
WHAT IT IS	An octave band hybrid	HC2 & JC2 3 dB + .72 − .6 f2/f1 = 2.0 L(inches) = 1850/FMHz	KC2 & LC2 3 dB + .53 − .45 f2/f1 = 2.0 L(inches) = 1970/FMHz
	A narrow band hybrid	HC1 & JC1 3 dB + .32 − .25 f2/f2 = 1.25 L(inches) = 1850/FMHz	KC1 & JC1 3 dB + .22 − .19 f2/f1 = 1.25 L(inches) = 1970/FMHz
	A directional coupler	A 2″ length is a 10 ± 1 dB coupler from 175 to 229 MHz	A 2″ length is a 10 ± 1 dB coupler from 186 to 244 MHz
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	Handles peak power	2000 Watts	2500 Watts
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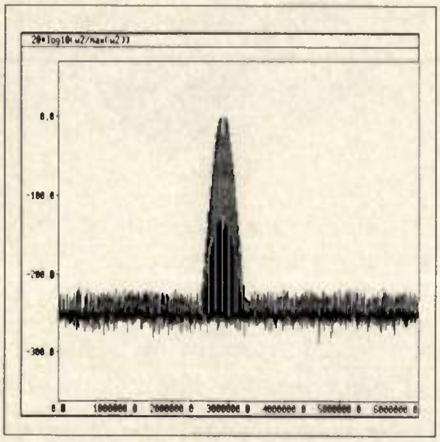

Figure 8. Simulation results. $Clock_m$ = $Clock_c$ = 12.8MSPS, F_{mod} = 20 kHz, Δf = ±75kHz, F_c = 2.9 MHz.

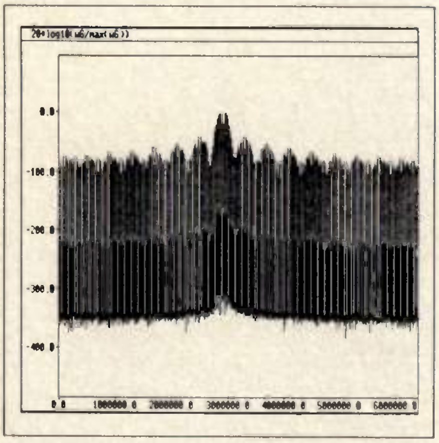

Figure 9a. Simulation results. $Clock_m$ = 400 KSPS, $Clock_c$ = 12.8 MSPS, F_{mod} = 20 kHz, Δf = ± 75 kHz, F_c = 2.9 MHz.

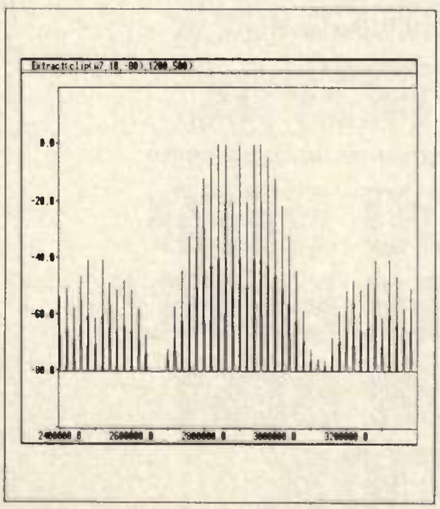

Figure 9b. An expanded view of Figure 9a.

assumed to be much less than 1 (first-order sidebands only).

We can apply Carson's rule to determine when none of the significant sidebands from modulation by the alias ("B"—Figure 6) overlap with the sidebands of the desired signal ("A"—Figure 6). From Carson's rule, A and B have significant sidebands at offsets up to (F_{mod} F_{dev}) from their respective center frequencies. For 20 kHz modulation frequency and 75 kHz peak frequency deviation, this comes to 95 kHz. To prevent overlap, A and B's center frequency must be at least 2 × 95 = 190 kHz apart. Thus from Figure 6:

$$Clock_m \geqslant 190\text{KSPS (minimum value)} \tag{10}$$

In practice, we want to filter out everything but the desired signal. To keep the order of the filter down, $Clock_m$ should be at least twice this value, 380 KSPS, preferably more.

The RF Sample Rate and Carrier Frequency

With limits set for $Clock_m$, let's set some bounds on $Clock_c$, the main clock for the DAC and the DDS. Several conflicting requirements are at work in setting the output sample rate and the carrier frequency. First we want a carrier frequency that is high enough so that no significant lower sidebands reflect about the zero frequency axis and land in the desired channel (Figure 7). On the other hand, if the carrier frequency approaches Nyquist frequency, sidebands might alias and land in the desired channel. Not only does this suggest a minimum $Clock_c$ (to give a Nyquist bandwidth large enough to avoid both problems) — it also implies that a carrier frequency of 1/4 clock would be ideal (since it centers the desired signal exactly in the middle of the Nyquist band).

In practice, however, this is less than ideal. Operation at an output frequency near a submultiple of the RF sample clock brings the spurs close to the carrier where they corrupt the desired signal. A low submultiple (such as 1/4 $Clock_c$) is particularly troublesome. Moving the carrier below 1/4 $Clock_c$ looks good since DACs give better spurious performance at lower output frequencies. With this in mind, set the carrier frequency between:

$$1/5\ clock_c < f_{carrier} < 1/4\ clock_c \tag{11}$$

$Clock_c$ is set to 12.8 MSPS for several reasons. First the ratio $Clock_m/Clock_c$ should be the ratio of two integers. This allows modulation samples to enter the DDS circuit with consistent setup and hold times. If this rule is not followed, significant glitches can occur in the modulation data loaded into the DDS, causing excessive spurs in the FM spectrum. Second, our selected ADC will use a 12.8 MSPS clock so our circuitry is simplified. Third, this clock gives a 6.4 MHz Nyquist bandwidth in the DDS circuitry — more than enough to contain the FM spectrum. For a $Clock_c$ = 12.8 MSPS:

$$2.56\text{ MHz} < f_{carrier} < 3.2\text{ MHz} \tag{12}$$

A 2.9 MHz carrier is almost exactly midway between these two limits so spurs should be well separated from the carrier. It is also an odd multiple of 100 kHz which might be an advantage if this signal were mixed to the FM broadcast band (A 200 kHz phase-locked loop reference frequency can be used in the LO(s) for the mix to final output frequency).

A Computer Simulation

With the modulation sample clock, the RF sample clock, and the carrier frequency determined, it is now practical to simulate the performance of the modulator taking into account all modulation terms. Although we can work purely in the frequency domain using equations developed for multitone modulation (Reference 3), a better approach is to recreate a DDS in software, creating the time record of the FM signal and taking a Fast Fourier Transform (FFT) to get the spectrum. Advantages include:

1. It can exactly model an ideal DDS since the program can match the math operations the DDS hardware performs.
2. Quantization in the ADC and DAC are easily taken into account (if desired).
3. It is much simpler.

If we use periodic modulation, and the modulation frequency, carrier frequency and the modulation sampling clock are commensurate (that is, each completes an integer number of cycles in the time record), leakage problems in computing the FFT can be avoided and unwindowed data can be used. 20 kHz modulation, $Clock_m$ = 400 KSPS, F_c = 2.9 MHz, $Clock_c$ = 12.8 MSPS, and 640 sample points give commensurate data. The result: the spectrum has no spectral

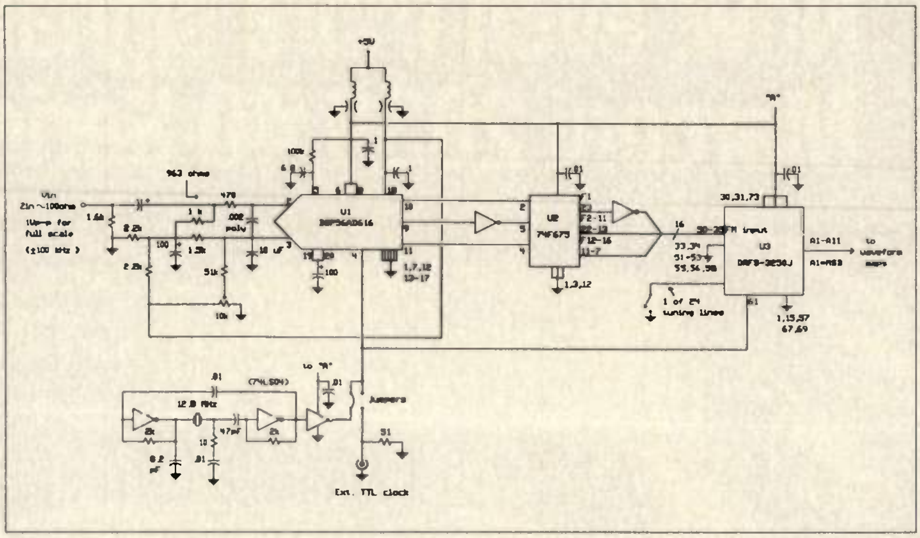

Figure 10a. DDS-based FM modulator.

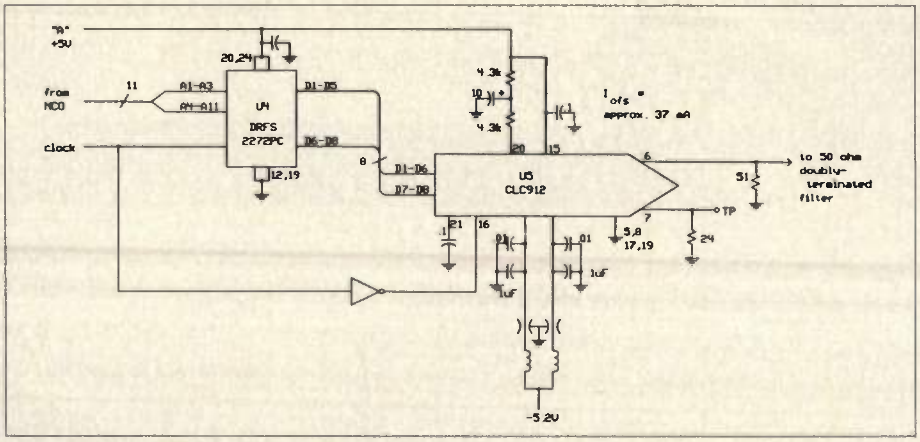

Figure 10b. DDS-based FM modulator.

spreading and no leakage of the spectral lines.

A simple program develops the time record which is imported into a DSP spreadsheet for FFT and other analysis (10 times the required number of sample points are taken for presentation purposes only.)

To test the software, identical modulation and RF sample clocks (12.8 MSPS) were tried. This closely approximates a continuous-time FM signal. Modulation sidebands should cluster only about the main carrier frequency. The result (Figure 8) confirms this with a noise floor set by finite math to approximately −200 to −250 dBc.

Figures 9a and 9b show the spectrum with our proposed modulator (modulation clock = 400 KSPS, RF sample clock = 12.8 MSPS). As predicted earlier, additional sidebands are clustered about offset frequencies which are multiples of the modulation clock. We have simulated 20 kHz frequency, 75 kHz peak deviation, single-tone modulation since this should be close to the worst case from the viewpoint of spectral spreading. With the sample rates chosen, the sampling artifacts are well below the desired signal and should cause little trouble.

Simulation confirms our earlier simplified analysis and quantifies the effects of the various alias sidebands so that suitable bandpass filters can be designed.

Circuit Description

A circuit was developed based on these concepts (Figure 10). Modulation enters U1, a Motorola DSP56ADC16 Sigma-Delta ADC, through a simple first order low pass filter (approximately 170 kHz, −3 dB) and offset adjustment network. This ADC was selected because:

1) It has 12-bit resolution (approximately 74 dB signal to noise ratio) when providing 400 kilosamples/second.
2) Its input sampling rate is much higher than its output sampling rate — in this case 6.4 MSPS, so front-end anti-aliasing filtering is simplified (a characteristic of all sigma-delta ADCs).

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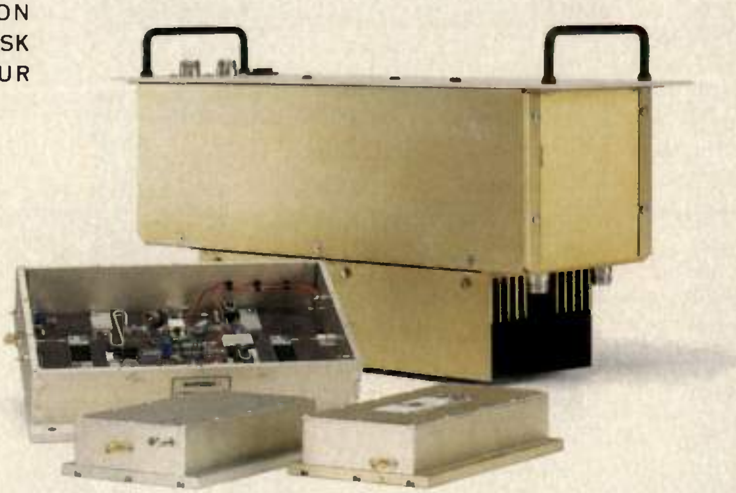

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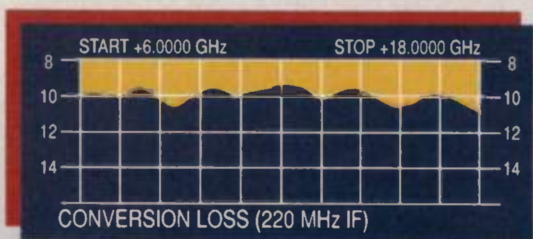

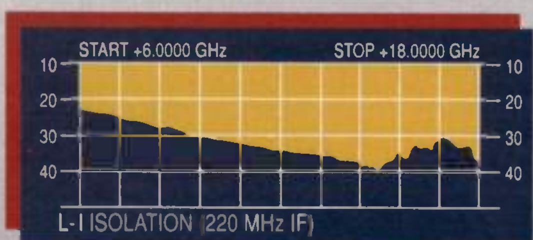

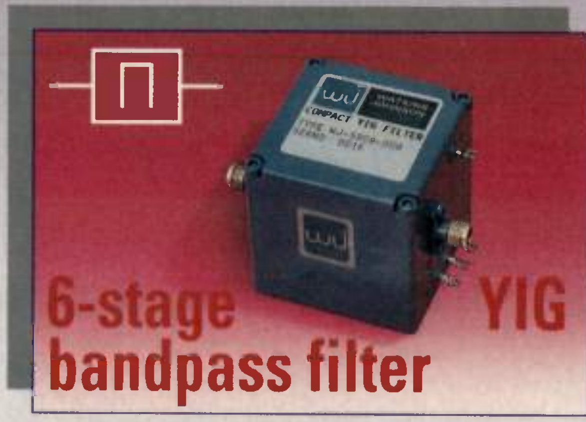

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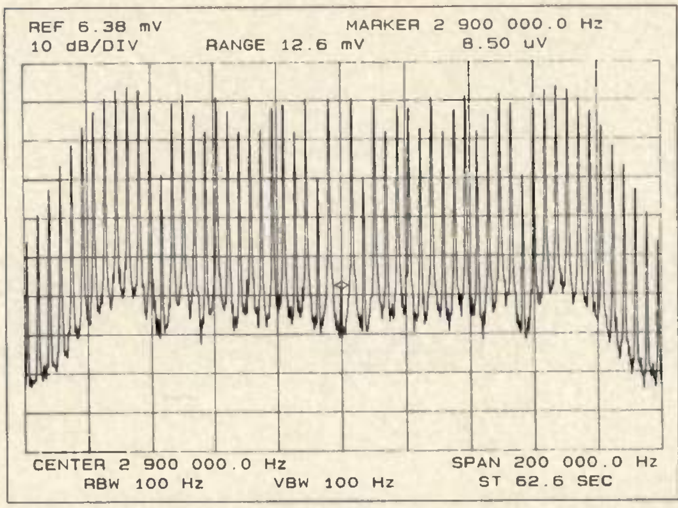

Figure 11. Bessel null testing at 3.5358 kHz. 75 kHz peak deviation.

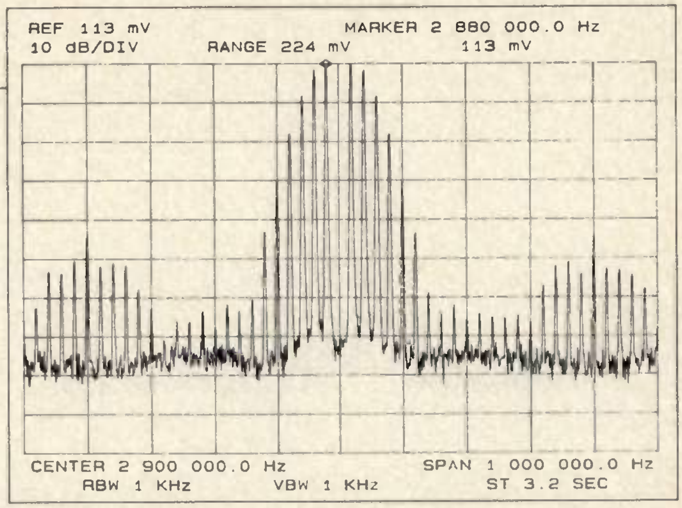

Figure 12. Bessel null testing at 20 kHz. 48.096 kHz peak deviation.

3) It has excellent linearity which translates into low distortion, good frequency response which can be made even better because of its high predictability (once again due to its architecture).
4) It is relatively inexpensive.
Offset circuitry corrects for the offset error in the ADC which can have a small second-order effect on center frequency. The advanced data sheet that was available at the time of this design did not furnish input offset numbers, but the offset circuitry should have more than enough adjustment range (considering the ADC uses a switched-C differential input stage.)

U1 passes a serial data stream representing the modulation to U2 (a 74F6675) where it is converted to parallel form. U6B complements the MSB converting the data from two's complement to offset binary before it is sent to the modulation input of the DDS circuitry (U3). U3, a Digital RF Solutions 3250, was selected because it has a wideband, full-width parallel FM modulation port. This simplifies the interface because it supports extremely fast modulation sample rates.

U3 sends samples of the instantaneous phase of the FM signal to U4 and U4 (a sinewave lookup table) creates a digital representation of an FM modulated sinusoidal signal. With only U4 (8 bit sinewave quantization), spurs are limited to approximately −62 dBc (Reference 4). Adding another IC to get 12 bits quantization improves spurs to the DAC's limit: −65 to −70 dBc at this output frequency, but it isn't necessary.

U5 converts this signal to analog form. After suitable bandpass filtering, a very clean FM signal is produced. A CLC912 was chosen for U5 because it has the sample rate we need, it provides large (40 mA_{pp}) output current, can drive a doubly-terminated 50 ohm transmission line directly, and has excellent spurious performance.

U6 provides a clock for the rest of the circuitry.

Testing the Modulator

All of the spectra shown in this section were taken directly from the unfiltered DAC output. In the final application, a fifth-order Bessel, bandpass filter will be used to remove the spurs and $Clock_m$-related components.

Modulation sensitivity — In the design, if the full scale range of the ADC is exercised ($4V_{pp}$), the peak frequency deviation is ±100 kHz. For ±75 kHz peak frequency deviation, a 3 V_{pp} input should be required. We can check the actual modulator sensitivity using the Bessel-null method. With single-tone modulation, carrier amplitude should drop to zero with modulation indices of approximately 2.4048, 5.5201, 8.6537, 11.7915, 14.9309, 18.0711, 21.2116 and so on (the zeros of $J_0(B)$).

To test the sensitivity at low frequencies, a 3.5358 kHz sinewave was applied to the exciter and the amplitude adjusted until the modulation index was 21.2116 (as observed by the Bessel zeros — see Figure 11). This corre-

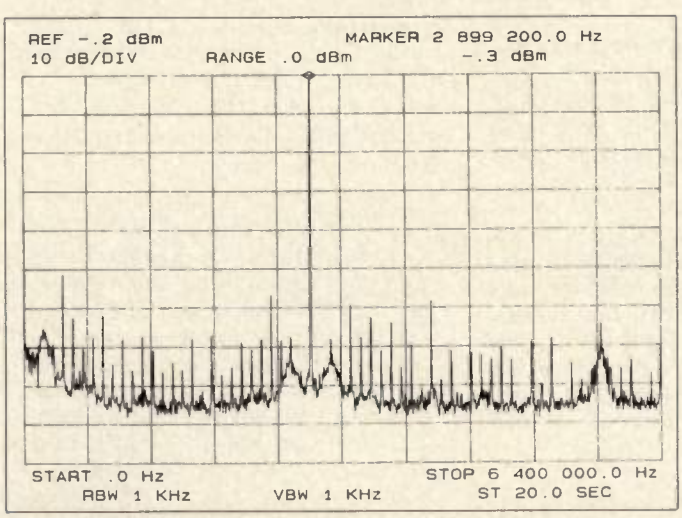

Figure 13a. Spurious performance, no modulation.

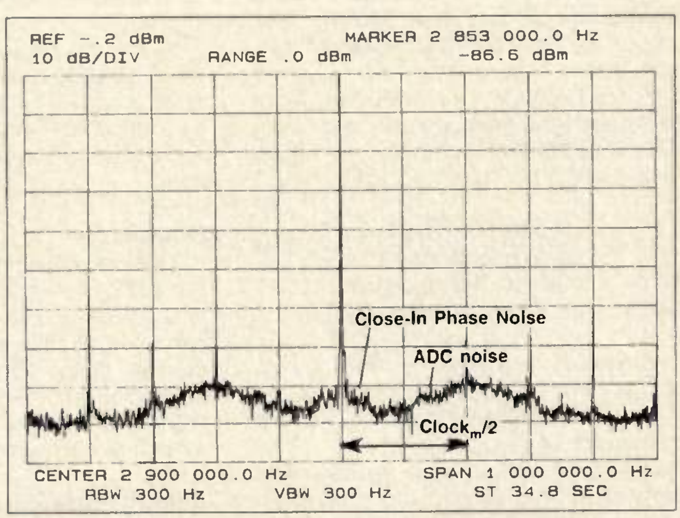

Figure 13b. Expanded view of close-in spurs.

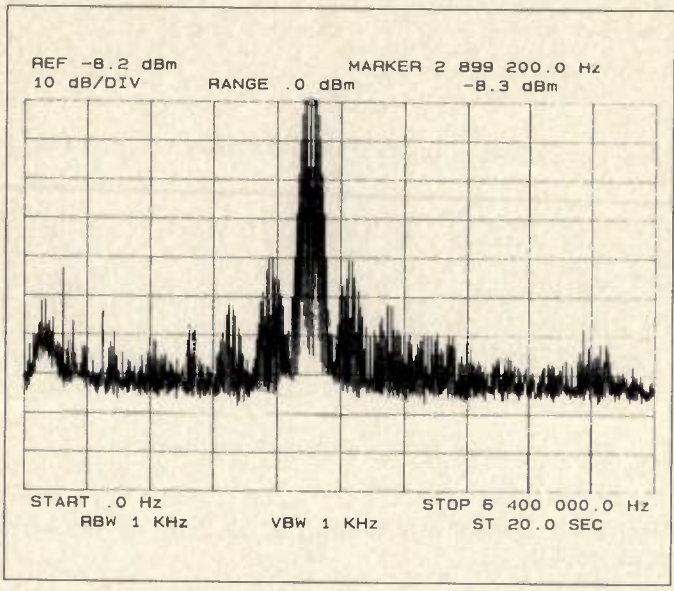

Figure 14. Full deviation, maximum modulating frequency.

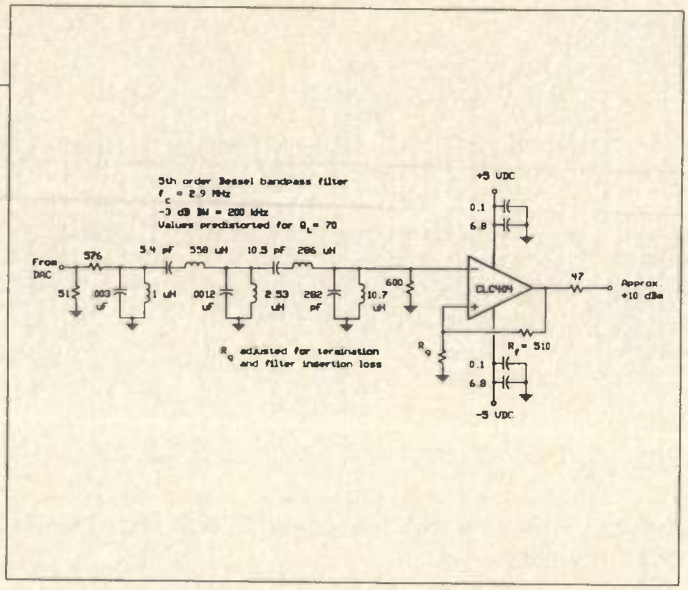

Figure 15. Optional filter and output buffer amplifier.

sponds to a 3.5358 × 21.2116 = 75 kHz peak frequency deviation. The voltage applied was 1.095 V_{rms} (measured with an HP3458 DVM) or 3.097 V_{pp} (sensitivity 3 percent below the theoretical value).

The bulk of this error can be explained by the reference voltage error of the ADC. The reference voltage for the DSP56ADC16 is created from a voltage divider connected to the analog 5 Volt power supply and buffered. If the 5 Volt supply voltage is off, so is the full-scale range of the ADC and the modulation sensitivity. Using an external precision reference can substantially improve the modulation sensitivity accuracy as well as stabilize it against 5 V supply variation. Accuracies of better than 0.1 percent should be achievable with this ADC

Frequency response — To check the high frequency rolloff, the Bessel-null method was applied again, but with a 20 kHz tone producing 48.096 kHz peak frequency deviation of 2.4048 modulation index (Figure 12). This occurred with a 0.72008 V_{rms} or 2.0367 V_{pp} input to the exciter. The modulation sensitivity is less at 20 kHz (compared to 3.5358 kHz) by:

rolloff = (13)

$$20 \log \frac{48.096\text{kHz}\ 1.095\text{V}}{76\text{kHz}\ 0.72008\text{V}} = -0.2\text{dB}$$

Most of this can be explained by the anti-aliasing filter and sinc rolloff in the ADC.

Spurious responses — Figure 13a shows the spurious performance (no modulation applied) over the Nyquist bandwidth of the circuit when a 12-bit quantization lookup table is used. The highest spur is from Clock_m leakage, and is only −52 dBc but this is not a concern because it is at a large frequency offset from the carrier and easily filtered. The spurs which are of most concern are shown in the expanded view about the carrier frequency (Figure 13b). The closest measurable spur occurs at 200 kHz offset and is −68 dBc. This is also reasonably easy to filter out while still preserving the sideband structure of the desired FM signal. Other effects such as close-in phase noise of the DDS and the spectrum analyzer (or possibly flicker noise at baseband), and ADC broadband noise are clearly visible but low enough to not concern us.

Modulation spectrum — Figure 14 shows the spectrum of the exciter with approximately 75 kHz peak deviation and 20 kHz single tone modulation-correlating well with the simulations (Figure 9). With Clock_m-related sidebands approximately −40 dBc (400 kHz offsets), relatively simple bandpass filters produce a very high quality FM signal.

Filtering the output — A simple doubly-terminated Bessel filter works well in this application. To buffer the filter, a CLC404 was selected (Figure 15). It offers superior bandwidth, group delay and distortion.

Summary

This design demonstrates that superior performance can be achieved with a DDS-based FM exciter. Spur levels can be controlled by proper modulation sample clock and RF sample clock selection. With this approach FM transmitters can benefit from all of the well-known advantages of DDS.

Acknowledgements

The author would like to thank DSP Development Corporation for use of their DADiSP Software in this article. The author would also like to thank Earl McCune (Digital RF Solutions Corp.), John (Dan) Byers, Sangil Park, and Mike Brown (all with Motorola, Inc.), and Bill Henderson (Comlinear Corp.) for furnishing samples and/or technical support on their products. *RF*

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About the Author

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A Simple EMI/RFI Detector

John Ayer
National Research Council, Canada

This entry in the 1992 RF Design Awards Contest demonstrates how simple a useful circuit can be. This device was designed to be a "sniffer" for EMI of significant magnitude.

As computers and microprocessors become ubiquitous in every lab, the problems of EMI/RFI affecting their performance become more prevalent. The simple circuit shown in Figure 1 offers an economical way to verify whether an EMI/RFI problem exists in your lab.

The device consists of a microwave diode of almost any style, a sensitive meter and some wire. Performance can be enhanced by selecting the diode for greatest sensitivity and by using a meter with a high internal resistance (above 5 kohms, preferably 15 kohms).

Version 1 uses the interconnecting wires as a loop antenna. If a search of a specific frequency is desired, the size of the loop can be adjusted to resonance for highest sensitivity. With an axial-lead diode, using the entire lead length will result in a loop of about 2.5 inch circumference.

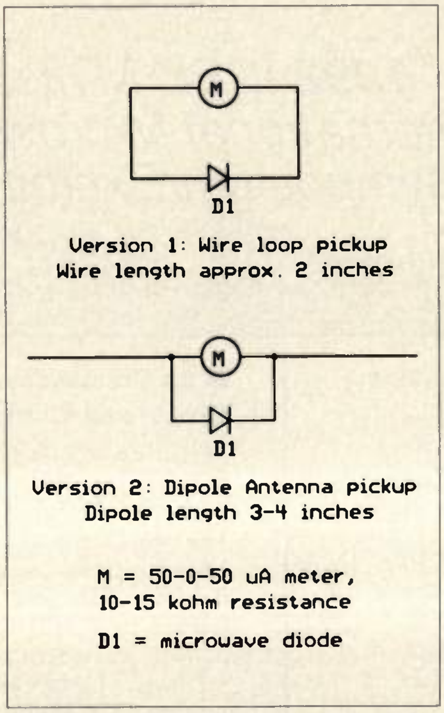

Figure 1. Circuit diagram of the EMI/RFI detector. Version 1 uses interconnections as a loop antenna, while Version 2 uses a dipole element for RF pickup.

Version 2 uses a dipole antenna configuration, placing the diode between the meter terminals and adding wire extensions on either side to make a dipole. Like the loop, this configuration can be "pruned" to resonate at the primary frequency of interest.

The device can be used to detect radiation from loose coaxial and waveguide connections, or from cabinets of power amplifiers and other RF-generating equipment. The circuit also makes a good microwave oven leakage detector. *RF*

About the Author

John Ayer is an Industrial Technology Advisor with the National Research Council, Industrial Research Assistance Program, University of Victoria, Box 1700, Victoria, B.C. V8W 2Y2, Canada. His engineering experience of over 25 years includes research, design, test and measurement, manufacturing and project management in electrical engineering over a wide power and frequency range. He can be reached at (604) 721-1242.

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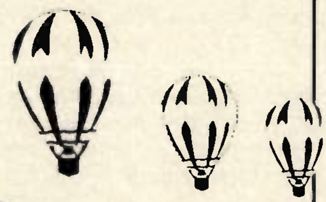

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A 1 GHz Prescaler Circuit

By Ray Robertson
Hewlett-Packard

This contest entry describes a prescaler circuit developed for the HP E1333A, a frequency counter for VXI test systems.

The design goals for this prescaler were good sensitivity, wide dynamic range, low SWR, and low cost. The prescaler chip chosen, a Motorola MC12073, met all these requirements except that the guaranteed input range was only 20 to 200 mV. To obtain a wider input dynamic range, an AGC preamplifier was designed. The circuit is shown in Figure 1.

CR1 and CR2 provide input protection. R2, R3 and R4 form an attenuator to provide a stable input match. CR5, a Hewlett-Packard 5082-3080, is a PIN diode whose RF resistance changes from 2 to 10,000 ohms as forward bias changes from 100 to 0.001 mA. U3, a Mini-Circuits MAR6, provides gain to improve sensitivity. CR4, a Hewlett-Packard 5082-2811 Schottky barrier diode, is used to detect the RF signal. It is used in a forward biased mode so that there is no diode drop to overcome. C7 is the filter capacitor for the detector circuit. CR3 is biased in the same mode as CR4 so that the two components track over temperature. R7 and R5 also function as a voltage divider which sets the RF signal level from U3. U2, R6 and C1 form an integrator that controls the forward bias through CR5, the PIN diode. R1, R9 and C5 filter the RF energy from U2. U1 is the prescaler which feeds into the rest of the counter circuits.

The typical sensitivity is less than 5 mV_{RMS} from 50 to 500 MHz and less than 12 mV_{RMS} up to 1 GHz. The overload point is greater than 3 V_{RMS} below 500 MHz. Above 500 MHz, accurate counts were obtained at levels up to 9 V_{RMS}. This stresses the protection diodes, but the useful dynamic range is typically 50 dB. The SWR is typically less than 1.3 with a power range of +20 to −10 dBm. A 15 kV static discharge does no damage to the circuit. *RF*

About the Author

Ray Robertson has worked as an analog, digital and RF engineer. He holds a BSEE and MSCS from NJIT. He may be reached at 1600 Morning Drive, Loveland, CO 80538. Tel: (303) 663-2185.

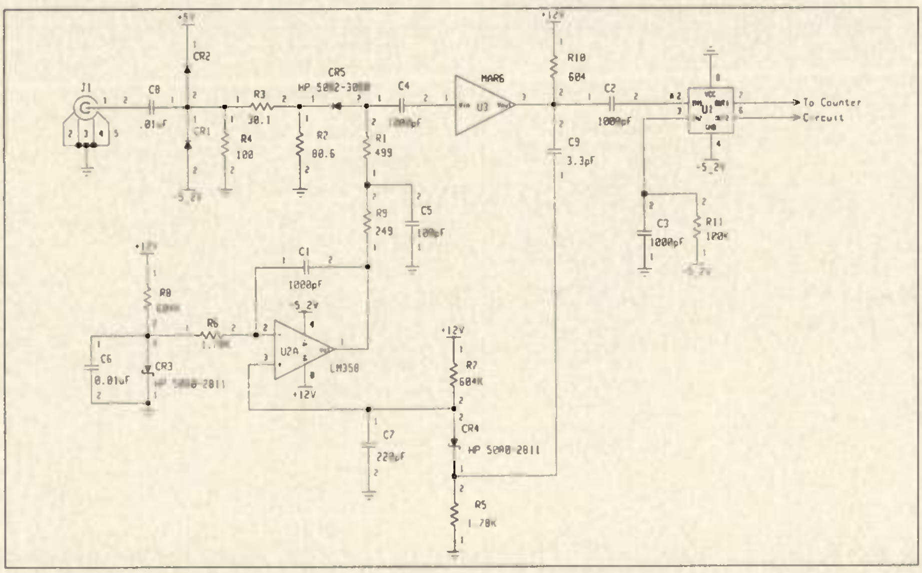

Figure 1. The 1 GHz AGC amplifier and prescaler circuit .

A Program for RF Amplifier Design

By Thomas H. Stanford
Thomas H. Stanford Engineering

This entry in the 1991 RF Design Awards Software Contest aids in the design of single-stage RF amplifiers. The program analyzes a device's S-parameters at a given frequency and plots gain and stability circles on a Smith chart. A lumped-element matching program is part of the program package.

The program RFAMP is written for MS-DOS and compatible computers from IBM and many other manufacturers. To run the program, EGA or VGA graphics capability is required and at least 500 kB of user memory. A hard disk drive is highly recommended, as is a math coprocessor, although this is not required to use the program.

Basic program operation begins with a batch file that installs a runtime module from The Software Bottling Company. This software allows menus to be displayed. The startup file then continues loading the program. When finished with the program, the software removes the memory-resident module before exiting.

Results of the computations can be printed to virtually any printer, since the data is in text format. No graphics or screen dump capability is present in the program. Third-party software is available (such as Pizazz Plus) that can accomplish this if desired.

Computations and Displays

The main design program uses a set of S-parameters along with frequency and gain inputs. Stability and gain circles are plotted (Figure 1) and the user picks the desired load. The input impedance is then calculated and plotted along with the input stability circle. The design data can be copied to the printer in the format shown in Figure 2. This program uses design principles described in several "classic" reference textbooks and technical papers.

At this point, the program can be terminated, or the impedance data can be passed to the matching network program module, which determines a two-element L-network match to 50 ohms. This module can also operate alone. Four possible two-element lumped networks for arbitrary source and load impedances are computed and displayed, either with component values, or with a statement that the configuration will not work for that transformation. Figure 3 is a sample display of the matching results.

The third program function provides a number of utilities for creating and maintaining data files. New files can be entered, listed, edited and saved. Key device parameters can be reviewed, such as gain and stability, and listed to the screen or printer. Also, the S-parameter data can be plotted to a Smith chart to see where they fall, along with output stability circles if you are looking for a part with specific characteristics.

The files can have components embedded in them, such as shunt or series resistors, ground lead resistor, and RLC feedback network. Be sure to save the modified files under new names!

Two conversions are offered, one to switch between common-emitter and common-base (or the other way around). The other option will convert between S and Y parameters, S and Z parameters, plus S and ABCD parameters.

S-Parameters and Stability

For high frequency design, the most accurate and conveniently measured two-port parameters are scattering or S-parameters. These were defined in 1965 by K. Kurokawa and have gained wide acceptance. S-parameters com-

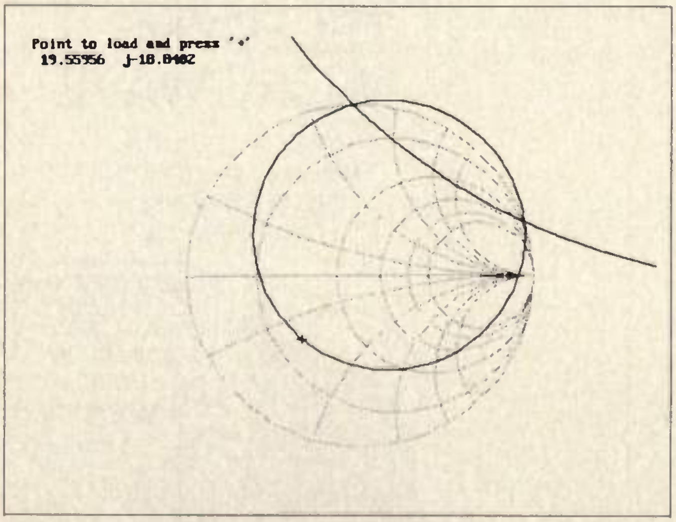

Figure 1. Stability and gain circle plots. The user selects a load on the gain circle.

```
Absolute stability requires K > 1 and |Delta| < 1
or alternately K . 1 and B1 > 0
when S11 and S22 magnitudes are less than 1.

K= .6920314      |Delta|= .1033011      B1= 1.369329
Mag(S11)= .69      Mag(S22)= .31

Output plane gain circle for desired gain of  18  dB is:
Gain circle center is  .2901834  at an angle of  55.1489  deg
Gain circle radius is  .7874334

Output Stability circle center is  4.459196  at an angle of 55.14859 deg
Output stability circle radius is  3.708348

Input relection coeff for the chosen load of  19.55956  j-18.8402  is:
 .5552226  at an angle of  160.0033  deg
Input impedance is  14.70656  j  8.073713  ohms

Input stability circle center is  1.550929  at an angle of  162.2723 deg
Input stability circle radius is  .6806626


Press RETURN to continue...?
```

Figure 2. Design data output.

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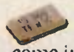

Surface Mount Quartz Crystals come in various packages- ceramic, glass, metal and ceramic base with metal encapsulation. Frequencies range from 10 to 200 MHz. These are ideally suited for microprocessor driven applications in cellular, paging, cordless, SMR and GPS.

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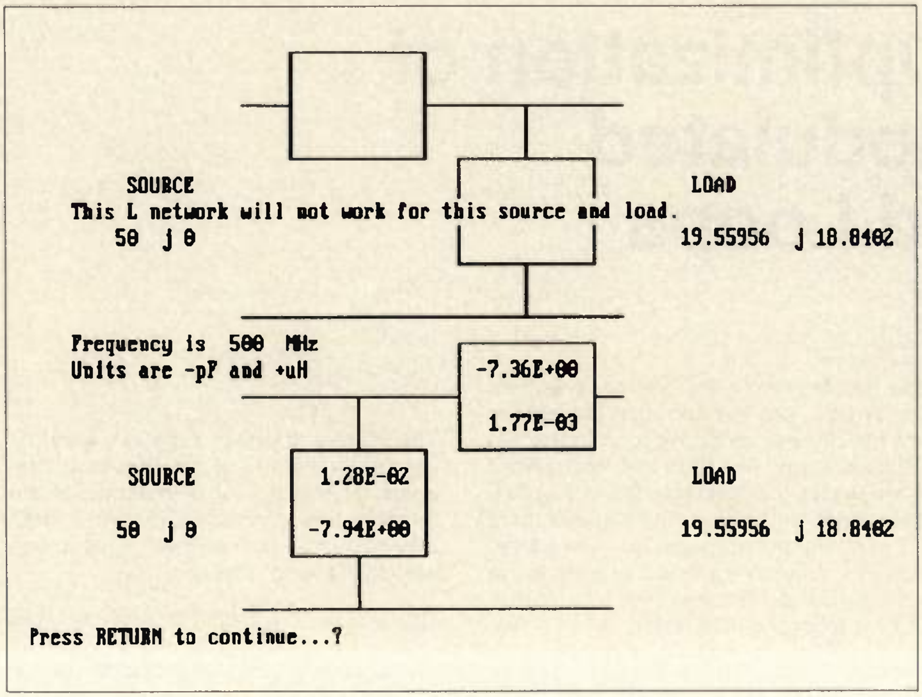

Figure 3. Display of the matching network computations.

pletely and uniquely define the small-signal gain and input and output immitance properties of any linear two-port device. Simply stated, S-parameters are merely insertion gains, forward and reverse, and reflection coefficients, input and output, with driven and non-driven ports terminated in equal impedances, typically 50 ohms.

With basic S-parameter relationships and some algebra, it is possible to determine the input reflection coefficient for an arbitrary load, the output reflection coefficient for an arbitrary source, maximum available gain and stability information. Combinations of source and load impedances, plus the available and desired gain, all affect stability. The program computes and plots constant gain circles and stability circles, allowing the user to select load as far from an unstable region as possible. The quick plotting capability of the program allows the user to check various options for source and load impedances that will allow a stable amplifier to be designed.

This program is available on disk from the RF Design Software Service, including all program files, S-parameter files for 34 NEC devices, and source code for advanced users to examine and modify if desired. A 28-page manual is also provided, with operating instructions, example computations, and tutorial material on S-parameters and stability analysis. Although the author has allowed the program to be freely distributed, permission is not granted for its inclusion in any software sold for profit. The author offers the program as shareware, with the request that users who find it useful pay a registration fee to support updates and improvements. *See page 145 for ordering information.* ***RF***

About the Author

Thomas H. Stanford has a MSEE degree from the University of Washington in Seattle, and has worked in RF/analog design for 14 years and engineering management for five years. His design experience includes HF transmitters, modems, radar, automatic antenna tuning systems, microstrip components, and even some digital systems. He can be reached at 454 West Blueridge Place, Escondido CA 92026.

Design and Optimization of Frequency Modulated Phase Locked Loops

By Farron L. Dacus
Dallas Semiconductor

The phase locked loop is currently the dominant method of frequency synthesis, and will probably remain so for years to come. However, it does have a few weaknesses, such as the difficulty in accurately and smoothly frequency modulating its output. This article will present analysis and design techniques for frequency modulated phase locked synthesis. Though highly useful and relatively easy to develop, these fundamental techniques do not seem to be widely known.

The method presented here, which shall be referred to as the FM PLL, involves summing a modulating signal into the loop control voltage. This method allows wide bandwidth and smooth modulation, but is not without problems. Most of the problems revolve around the loop's tendency to resist the modulation as an undesired error, resulting in unacceptable distortion. An elegant solution to this problem has been described in a previous *RF Design* article (1). Practical design and optimization methods will be presented here.

Normalized Form PLL Analysis

In control systems analysis, and particularly for second order control systems, a standard normalized form for the expression of transfer functions and time domain responses has evolved. Use of this form is extremely convenient for the design of the standard second order PLL, but the common references do not discuss its application to the FM PLL. It turns out that the normalized form is easily extendable to the FM PLL and leads directly to the development of a straightforward design procedure. Let us briefly review it as it applies to the standard PLL. Please refer to Figure 1 for the following discussion.

The PLL is nothing more than a control system. In a control systems sense, the voltage controlled oscillator (VCO) functions as an integrator from input voltage to output phase. It is the output of this integrator that is controlled and, because frequency is by definition the time derivative of phase, the frequency is also controlled. The output frequency is forced to be $N\omega_{ref}$.

In PLL analysis, the steady state output (carrier) may be viewed as a DC operating point. Our interest is in understanding the small signal AC behavior of the loop in response to outside stimuli, such as modulation. The analysis may be carried out in the frequency domain. Though it can be confusing, it is just as valid to analyze frequency variation in the frequency domain as it is to analyze voltage variation in the frequency domain.

Several transfer functions are of interest. The phase transfer function is defined as:

$$H(s) = \frac{\theta_2(s)}{\theta_{ref}(s)} \tag{1}$$

The phase transfer function may be obtained in terms of specific loop variables by solving for it in terms of the relationships defined in Figure 1. This process shall be termed substituting around the loop. The result is:

$$H(s) = \frac{K_d K_o F(s)}{Ns + K_d K_o F(s)} \tag{2}$$

Equation 2 may be placed into normalized form when an explicit form is substituted for the loop filter function F(s). For frequency synthesis applications, the most common filter form is the type 3 active filter (2). This low pass filter acts as an integrator at low frequencies, with a higher frequency zero that prevents loop instability by keeping its phase shift less than 90 degrees. Circuits for this filter are shown in Figure 2. Analysis of the type 3 active loop filter yields its transfer function to be:

$$F(s) = \frac{-(1 + s\tau_2)}{s\tau_1} \tag{3}$$

where:

$$\tau_1 = R_1 C_1 \tag{4}$$

$$\tau_2 = R_2 C_1 \tag{5}$$

It is common in the literature to ignore the negative sign in equation 3, and leave it to the circuit designer to get the

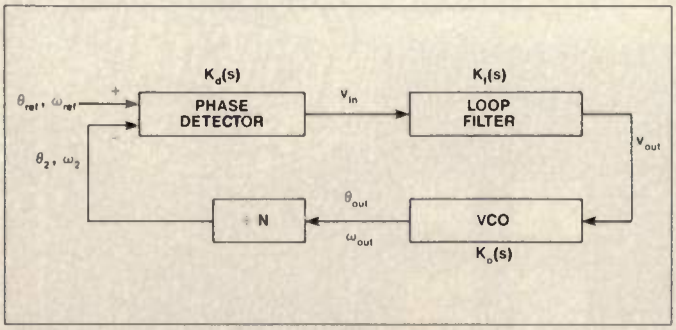

Figure 1. The basic phase locked loop.

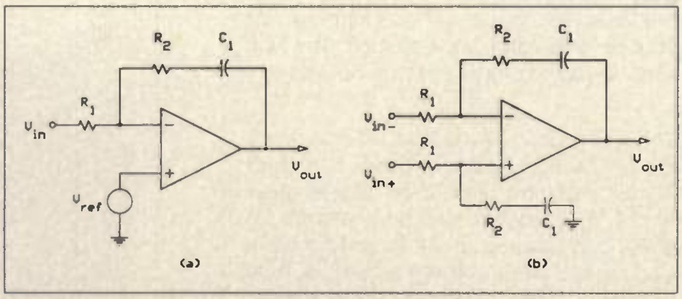

Figure 2. The type 3 active loop filter, a) Single ended input, b) differential input.

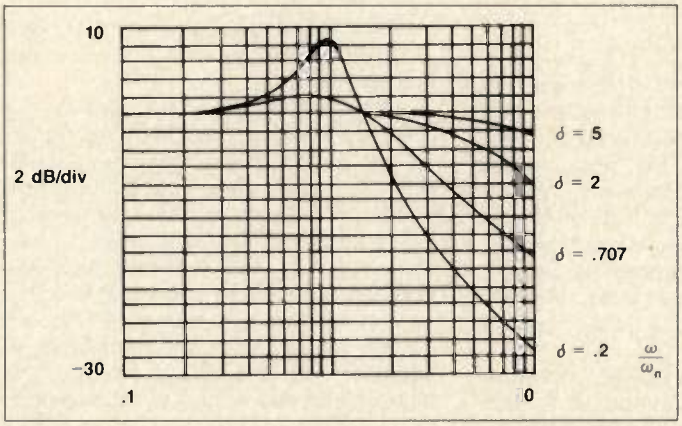

Figure 3. The phase transfer function in normalized form.

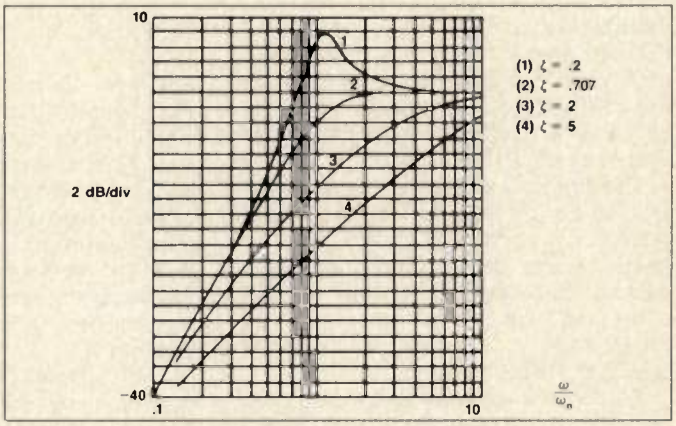

Figure 4. Curves of H (s).

signs right in the hardware to ensure negative feedback. Dropping the negative sign and substituting equation 3 into equation 2 yields:

$$H(s) = \frac{\frac{K_oK_d}{\tau_1 N}(1 + \tau_2 s)}{s^2 + \frac{K_oK_d\tau_2}{\tau_1 N}s + \frac{K_oK_d}{\tau_1 N}} \quad (6)$$

We are now ready to convert to the normalized form. In control theory, the standard normalized form of a second order equation is written as:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (7)$$

In equation 7, ζ is referred to as the damping factor, and ω_n as the natural frequency. Equating coefficients between this equation and the denominator of equation 6 shows that the denominator can be expressed in normalized form if the following definitions are made.

$$\omega_n = \sqrt{\frac{K_oK_d}{\tau_1 N}} \quad (8a)$$

$$\zeta = \frac{\tau_2\omega_n}{2} \quad (8b)$$

Subsituting equations 7 and 8 into equation 6 yields:

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (9)$$

A MathCAD generated set of plots of this low pass function is shown in Figure 3 below. The case $\zeta < 1$ is referred to as underdamped, and the case $\zeta > 1$ as overdamped. The case $\zeta = \sqrt{2}$ is the most common design choice, as it affords the fastest recovery from transient conditions, and is near optimal for loop suppression of oscillator noise (2). The frequency $\omega = \sqrt{2} \times \omega_n$ is referred to as the loop bandwidth.

Another important transfer function is the error transfer function, $H_e(s)$, defined as:

$$H_e(s) = \frac{\theta_{ref}(s) - \theta_2(s)}{\theta_{ref}(s)} \quad (10)$$

Solving for this function and converting to normalized form gives:

$$H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (11)$$

Note that the error transfer function is generally high pass, so that phase error is only allowed to exist above the loop bandwidth. A family of error transfer curves is shown in Figure 4.

Analysis of the FM PLL Using the Normalized Form

With a basic understanding of the normalized form of PLL analysis, we are ready to apply it to the FM PLL. Because we only modulate the PLL in the locked condition, the analysis is of small signal quantities. This will be emphasized by use of the prefix Δ. Since the reference frequency is fixed in the FM PLL system, the small signal component of the reference signal is zero. This allows the reference to be dropped from the block diagram of the FM PLL in Figure 5.

We are critically interested in the transfer from the modulating voltage ΔV_m to the output frequency variation $\Delta\omega_{out}$. Let us define this as the frequency modulation transfer function $H_{fm}(s)$.

$$H_{fm}(s) = \frac{\Delta\omega_{out}(s)}{\Delta V_m(s)} \quad (12)$$

Solving for this function and applying the normalized form yields:

$$H_{fm}(s) = \frac{K_o s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = K_o H_e(s) \quad (13)$$

Like phase error, the loop will only allow modulation to exist above the loop bandwidth. The effects of ω and ζ may be further clarified by the definition of a new figure of merit, the signal to distortion ratio. The definition is arrived at by noting that the ideal FM transfer function is simply K_o. Any loop modifications to this are undesired, and all such modifications appear in the loop filter output, so a sensible definition is:

$$\frac{\text{signal}}{\text{distortion}}(s) = \left|\frac{\Delta V_m(s)}{\Delta U_f(s)}\right| \quad (14)$$

Solving for this transfer function and comparing to the phase transfer function shows that:

$$\frac{S}{D}(s) = \frac{1}{H(s)} \quad (15)$$

Since the signal to distortion may be visualized as an upside down graph of H(s), the effects of ω_n and ζ are clear. A smaller ω_n gives better signal to distortion at any frequency above the loop bandwidth, which was to be expected. However, it is also noted that for frequencies above the loop bandwidth we also get better signal to distortion for a smaller ζ. Most engineers would not have intuitively expected a strongly underdamped loop to have any advantage.

We may conclude that the smallest ω_n and the smallest ζ that are consistent with other system requirements should be used. However, for a small ζ, the designer must be careful about instability.

SPICE Modeling of the FM PLL

The validity of these results may be checked with a SPICE model. For this demonstration, an arbitrary PLL with a carrier frequency of 300 MHz and an ω_n of 1 kHz was chosen. The VCO was given a typical tuning range of 10 MHz over an 8 Volt tuning range. The phase detector is assumed to be a type 4 digital PD with gain $V_{cc}/2\pi$. V_{cc} is assumed to be 5 Volts. If the reference is assumed to be 10 MHz, then the divide ratio N is 30. A SPICE circuit representing this system is shown in Figure 6.

The integrating action of the oscillator is created by the controlled current source E_{osc} and capacitor C_{osc}. The gains of the divider and the phase detector have been combined into the controlled voltage source E_{nkd}. The resistors R_{dum1} and R_{dum2} satisfy the SPICE DC requirements.

A set of transient simulations was run using the damping factors shown with a 10 kHz, 40 mV square wave V_m. The results, shown in Figure 7, support the conclusions just presented.

The Integrator Error Corrected PLL

A fundamental improvement to the FM PLL is described in Reference 1. The working concept is simple but ingenious. If a voltage opposite in sign but equal in magnitude to the modulation induced phase error is summed into the phase detector output, the loop will be prevented from responding to the modulation. Because the VCO acts as an integrator from input voltage to output phase, the proper function is a scaled inverting integration of the modulating voltage. The system is shown in Figure 8. Solving for the FM transfer function yields:

$$H_{fm}(s) = \frac{\Delta\omega_{out}(s)}{\Delta V_m(s)} = \frac{K_o\left(1 + \dfrac{F(s)K_i}{s}\right)}{1 + \dfrac{F(s)K_oK_d}{Ns}} \tag{16}$$

We note that if,

$$K_i = \frac{K_oK_d}{N} \tag{17}$$

then equation 16 reduces to,

$$H_{fm}(s) = K_o \tag{18}$$

Equation 18 represents the ideal FM PLL behavior. Unfortunately there are circuit errors, mostly the variation in K_o over its tuning range, that degrade the necessary match condition (equation 17). However, a very significant performance improvement can still be attained. Even DC modulation is possible, though the integrator and phase detector must be periodically reset, as described in Reference 1.

The effects of mismatch may be quantified by the definition of a new term, the integrator mismatch error, as shown in equation 19.

$$\varepsilon_i = K_i - \frac{K_dK_o}{N} \tag{19}$$

Now the signal to distortion ratio for the corrected FM PLL is shown to be:

$$\frac{S}{D}\text{ (corrected)} = \frac{K_dK_o}{N\varepsilon_i}\,\frac{S}{D}\text{ (simple)} \tag{20}$$

If the VCO gain can be precisely controlled, then the signal to distortion can be made very high at all modulating frequencies. If such control is not possible, then loop parameter optimization becomes important. The smallest possible ζ and ω_n would be used to minimize loop distortion beyond the loop bandwidth. If the system must be modulated within the loop bandwidth, then a more normal ζ of 0.5 to 1.0 would be appropriate.

Limitations of the Error Corrected FM PLL

There are several potential problems to guard against in the design of the corrected FM PLL. Among these are the effects of practical integrator performance, maintaining lock under strong modulation conditions, and prevention of unacceptable sideband levels under modulation.

Integrator drift may be curtailed by limiting the DC gain of the integrator by placing a large value resistor in parallel with the integrating capacitor. This moves the integrator pole from zero to a low frequency we shall label ω_p. We shall refer to this as the bypassed integrator. It may be shown (4) that this system will have minimum distortion and $H_{fm}(s) = K_oC(s)$ when the modulation is coupled into the VCO through the highpass function in the equation below.

$$C(s) = \frac{s}{s + \omega_p} \tag{21}$$

Another potential problem is for the phase error to reach a magnitude where the phase detector exceeds its usable range. Because the correcting integrator prevents the loop from responding to the modulation induced phase error, it may be written by inspection that the phase error is:

$$\theta_e(t) = \int_0^t \frac{K_oV_m(t)}{N}\,dt \tag{22}$$

The system will maintain lock so long as the maximum phase error is kept within the limits of the phase detector. For example, for the type 4 digital phase detector (PD), this limit is $\pm 2\pi$. A useful special case of equation 22 that is handy for a quick check is that of a simple rectangular pulse of modulation. A problem familiar to all designers of high performance synthesizers is the maintenance of adequate spectral purity. A major contributor to unwanted spectral components is the digital phase detector. The classic type 4 PD represents the

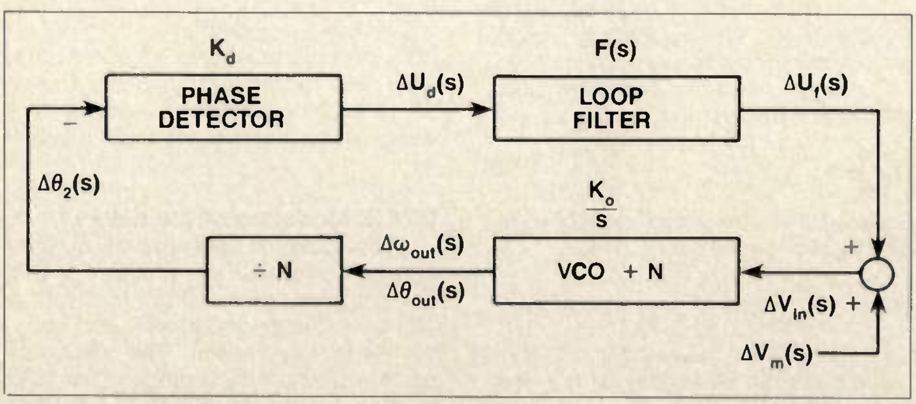

Figure 5. The FM PLL small signal model.

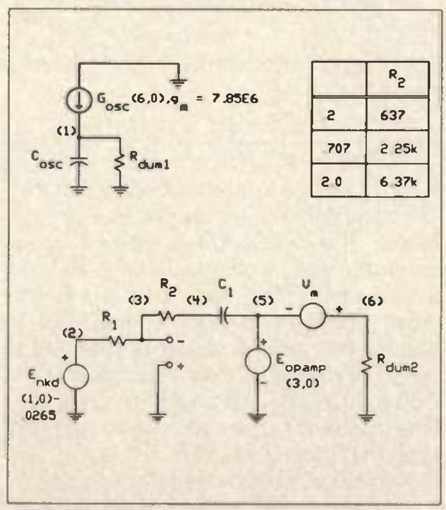

Figure 6. PLL SPICE Model.

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The FS700 LORAN-C frequency standard provides the optimum, cost-effective solution for frequency management and calibration applications. Four 10 MHz outputs from built-in distribution amplifiers provide cesium standard long-term stability of 10^{-12}, with short-term stability of 10^{-10} (10^{-11} optional). Reception is guaranteed in North America, Europe and Asia.

Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, a common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive initially, require periodic refurbishment, another costly item.

The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of ± 360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.

FS700: The optimum frequency management system

SRS

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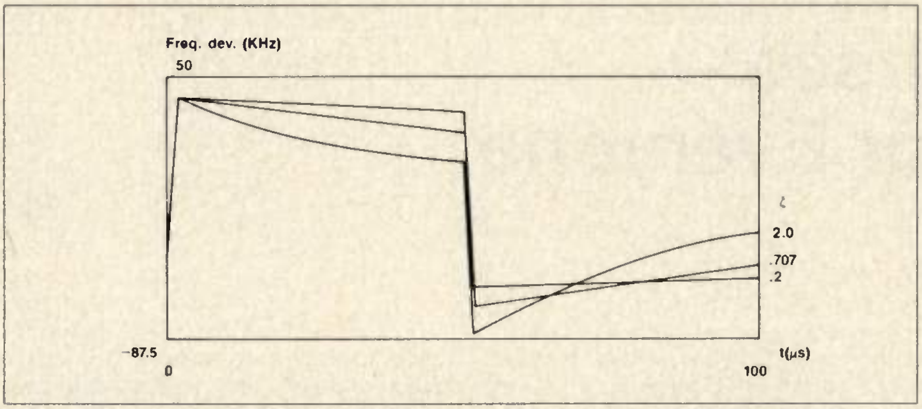

Figure 7. Transient response of the SPICE PLL to FSK modulation.

phase error in pulse width form, so there is undesired energy present at the reference and its harmonics. Some of it gets through the filter to the VCO input, where it causes sidebands. If a noise voltage has frequency ω_m and peak value V_t, then narrow band FM theory (5) shows the sideband to carrier ratio at offset ω to be given by equation 23. Note that this is a magnitude ratio when converting to dB(20 log), and that K_o is in rad/sec/volt.

$$\frac{\text{sideband}}{\text{carrier}}(\omega_m) = \frac{V_t K_o}{2\omega_m} \quad (23)$$

A PLL using the type 3 loop filter will drive the PD pulse width to approach zero, thus forcing the sideband generating harmonics in the PD output to also approach zero. However, modulation imposed on the PLL will widen the pulse width proportionately, making the sideband problem much worse.

For modulation rates much less than the reference frequency the pulse width may be considered to be a continuous variable. The ratio of the PD pulse width rho to the reference period is:

$$\frac{\varrho}{t_{ref}} = \frac{K_o}{2\pi N} \int_o^t v_m(t)dt \quad (24)$$

A complex form Fourier series expansion of equation 24, some simplifying approximations, and substitution into equation 23 will show the sideband to the carrier from the nth PD harmonic to be:

$$\frac{\text{sideband}}{\text{carrier}}(n, t) = \frac{K_o^2 V_{cc} |F(n\omega_{ref})|}{Nn\omega_{ref}} \int_o^t v_m(t)dt \quad (25)$$

Equation 25 is accurate for the first few harmonics, and sets a worst case for higher ones. Determining a worst case for the integral under a specific modulation allows a quick calculation of the worst case sideband to carrier.

If the sideband to carrier is unacceptable, the designer has the option of using a linear PD. The linear PD does not suffer an increase in harmonic content under modulation, but it lacks the wide capture range needed for a wideband synthesizer. Still, it might be the best choice for some applications.

Recently there has been some work done in the area of digital phase detection with reference frequency suppression (6). This type of phase detector would be especially valuable for the FM PLL. Hopefully, these techniques will be incorporated in the future by the major PLL component suppliers.

Conclusion

The FM PLL is a convenient means of obtaining an accurate frequency modulated frequency source. The extension of the normalized form to these sources greatly simplifies their analysis and design. A newly defined parameter, the signal to distortion ratio, is very useful in understanding and minimizing loop distortion.

The integrator error correction method yields a large improvement in distortion, but has a few problems to watch for. Chief among these is the degradation in sideband to carrier ratio, particularly with standard digital phase detection. The methods discussed will allow accurate prediction of performance prior to actual prototyping, thus allowing a decision to be made about the suitability of the FM PLL for a particular application.

RF

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About the Author

Farron Dacus is a senior RF design engineer at Dallas Semiconductor, where he develops RF automatic identification products. His BSEE is from the University of Texas at Austin, and his MSEE the University of Texas at Arlington. He may be reached at (214) 450-5387, or at 4350 S. Beltwood Parkway, Dallas TX 75244.

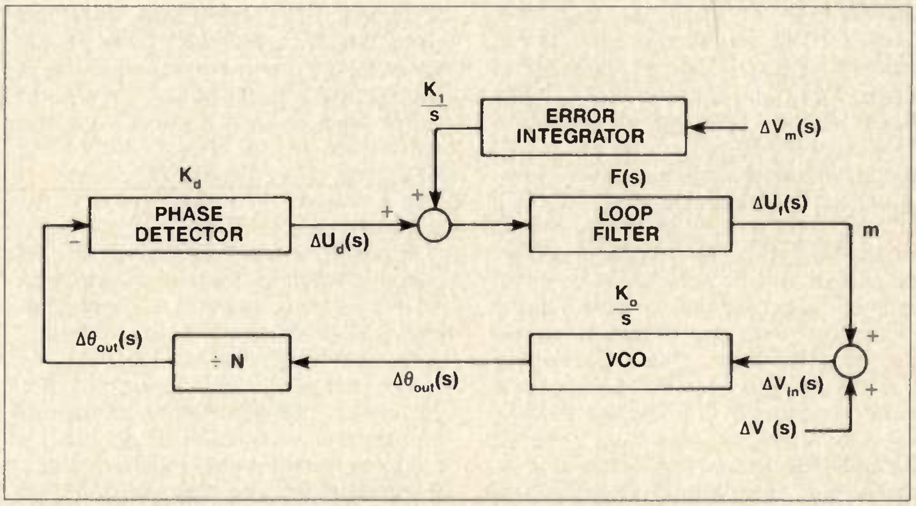

Figure 8. The FM PLL with integrator error correction.

RF Short Courses — Something For Everyone

By Liane G. Pomfret
Associate Editor

Short courses provide a quick way for engineers to learn about a subject. Courses are offered by universities and private companies alike and cover virtually every RF topic. Their continued popularity is encouraging for everyone in the business; evidence that the RF industry remains active.

Despite the recession and last year's gulf war, short courses have maintained strong attendance with only occasional dips in certain topic area. Les Besser of Besser Associates comments, "Enrollment slowed down mid last year, but it has picked up considerably and now it's even better than before." The military oriented courses are on a roller coaster. Dr. Bill Goodin, manager, short course program at UCLA Extension notes, "I'd say the courses that are more defense oriented have suffered a lot. Those that are more commercially oriented haven't suffered as much."

The engineer who attends a continuing education course seems to fit into a certain mold. He or she has about seven to ten years of hands-on experience, and usually holds a Bachelor's of Science. An informal survey at George Washington University found that 50 percent of the attendees had B.S. degrees, 27 percent had Masters, 4 percent had Ph.D.s and 15 percent were non-degreed or held an Associates degree. "The people who come to our training centers have a minimum of seven years in the industry." notes Patricia Bond, supervisor of educational services for EEsof. In addition, an engineer usually attends a continuing education course because he is working on or is about to start work on a project where he lacks experience or knowledge. It is uncommon for an engineer to attend a course just to hear what the instructor has to say. There are always people with more or less experience than the average engineer. But, as Chris Hyde, manager of applications development for Analog Devices says, "There's enough information on either end to make our seminars challenging and interesting for most of the crowd."

A recently graduated engineer would be more likely to attend a course devoted to the basics of RF engineering. "For basic courses, you see a lot of younger engineers," says George Adams, Georgia Tech's Associate Director of Continuing Education. Employers might send them to get them up to speed and help them become productive members of the technical staff as soon as possible. On the down side, employers may not want to invest the money in a new engineer, and so they must wait for a few years to get any sort of outside training. Yet basic courses such as those offered at RF Expos, by UCLA Extension, Georgia Tech and Besser Associates, are useful and cost effective means of training a new engineer or refreshing a more experienced engineer's skills.

The course offerings are virtually limitless. Whether it be a university or a commercial firm specializing in RF courses there is, as the saying goes, something for everybody. David Lohbeck, manager of north central division of TUV Rheinland explains their reasons for offering a seminar on European EMC requirements, "In the U.S. there is quite a misunderstanding as to what the European requirements are. So with our expertise and experience we can then put together these short courses to help people stay up to date on all the changes." Course length can vary greatly; anywhere from one day to two weeks, with the mean being three to four days. Many of these courses also offer credit in the form of Continuing Education Units (CEUs). CEUs are one useful way to track and measure an engineer's performance.

However, these courses can involve a significant cost. The average price for an engineering course is between $500 and $2000, although Analog Devices' 1-day seminars are about $25.

The following are all examples of basic level courses: Radar Basics, RF and Microwave Circuit Design, Electromagnetic Interference and Control and Frequency-Hopping Signals and Systems. These types of courses tend to attract all levels of engineers. They are good refreshers for experienced engineers and get other, less experienced engineers up to speed quickly. The more advanced level courses such as Digital Signal Processing, ELINT, Synthetic Aperture Radar: Design Processing and Applications, and Electromagnetic Characterization of Materials for Antenna/RCS Applications assume that attending engineers have more than a basic understanding of RF principles. Often, the techniques being taught are state-of-the-art technology and the instructors are well known individuals in their field.

Many of the new courses in development and currently being offered have a commercial focus. Universities and companies have recognized that the military market can no longer support the number of short courses it once did. There are courses that have both a commercial and military focus and they will continue to do well. Down the road, there will probably be a reduction in the number of military oriented short courses that are currently offered. But other areas are moving in to take their place. An interesting trend has been noticed by Merril Ferber, director of marketing at George Washington University, "Right now we're seeing a surge in quality and reliability engineering. They seem to be coming in strong." People have begun to realize that they need to learn quality and reliability techniques if they're going to be successful in the current market.

Despite individual ups and downs, short courses continue to do well. Engineers recognize the need to further their knowledge and careers and short courses offer an excellent means of achieving them. So whether you want to brush up on your basics or learn about something totally new, there's no problem finding the right course. **RF**

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An Introduction to Iron Powder and Ferrite Cores

By Gary A. Breed
Editor

The subject of magnetic materials for inductors and transformers cannot be adequately covered in a single article. To provide an introduction to these materials, this tutorial describes some very basic principles, and offers a few practical rules for common applications.

In grade school science class, we observed that a simple electromagnet became much stronger when a bolt or nail was placed in its core. In RF circuits, where inductors are defined by their electromagnetic behavior, iron-based materials can serve the same purpose; concentrating the magnetic lines of force in the core of an inductor. The result is an increase in the inductance over the same coil of wire in air. Useful materials for this purpose have "soft" magnetic properties, which means they do not become permanently magnetized like "hard" materials.

The degree of enhancement of the magnetic field is a function of the permeability (μ) of the core material; a numerical factor that defines the increase in concentration of the magnetic flux due to the presence of the material. The materials discussed here may have permeabilities from 3, only a little more than that of air, to 2500 or more. The ratio of two permeabilities is linear with regard to magnetic flux, but only when both are measured under exactly the same conditions. Magnetic materials are not linear with regard to magnetic flux versus current through the winding (and hence, with increasing flux density). Refer to your college Electromagnetic Fields textbook for a better explanation of permeability, flux density, coercivity, and other terminology (1). Also read the technical explanations contained in manufacturers' catalogs and applications notes to determine how μ is measured for their products.

Rather than describe the physics of these materials in detail, the rest of this article will describe the properties that affect their performance as RF inductors, transformers and chokes.

Iron Powders

This low permeability class of materials is made from iron compounds, mainly oxides. Carbonyl iron materials will have μ values from about 3 to 35, hydrogen reduced iron compounds can have μ values in the 25 to 125 range. Other compounds have been developed as well, with considerable recent effort to create materials with greater temperature stability.

The most common applications of iron powder materials are in toroidal inductor cores and adjustable slug-tuned coils. The doughnut shape of a torus has the advantage of creating a magnetic field that is contained within the core. Without the open ends of a linear winding, a toroidal coil has relatively little radiation. This is true even for air coils, although a core of magnetic material greatly increases the containment of the field around the circle defined by the core. As a result, inductors wound on toroid cores have low interaction with surrounding components and rarely require shielding.

Slug-tuned inductors are coils wound on a tubular forms of plastic, ceramic or other material, with a piece of magnetic material that can move in an out of the coil. The movement may be accomplished either with threaded core material that screws into the coil form, or the material may be a short rod supported by an adjustable mechanism such as a lead screw to move it in relation to the coil. Adjustable inductors using these methods are among the most common RF components.

Besides the self-shielding nature of the toroid coil and the adjustable capabilities of a slug coil, the use of iron

Core Size	26-mix yel/wht u=75 0-1. MHz	3-mix gray u=35 .05-.5 MHz	15-mix red/wht u=25 .1-2. MHz	1-mix blue u=20 .5-5. MHz	2-mix red u=10 1.-30 MHz	6-mix yellow u=8 2-50. MHz	10-mix black u=6 10-100 MHz	12-mix grnwht u=3 20-200 MHz	0-mix tan u=1 50-300 MHz
T-12-—	NA	60	59	43	20	16	12	6,5	3.0
T-16-—	NA	61	55	44	22	19	13	8.0	3.0
T-20-—	NA	90	65	52	27	22	16	10.0	3.5
T-25-—	NA	100	85	70	34	27	19	12.0	4.5
T-30-—	325	140	93	85	43	36	25	16.0	6.0
T-37-—	275	120	90	80	40	30	25	15.0	4.9
T-44-—	360	180	160	105	52	42	33	18.5	6.5
T-50-—	320	175	135	100	49	40	31	18.0	6.4
T-68-—	420	195	180	115	57	47	32	21.0	7.5
T-80-—	450	180	170	115	55	45	33	22.0	8.5
T-94-—	590	248	200	160	84	70	58	32.0	10.6
T-106-	900	450	345	325	135	116	NA	NA	19.0

Table 1. Some typical core materials and A_L values.

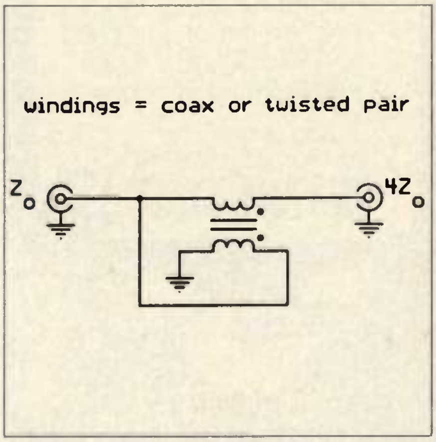

Figure 1. A unbalanced 4:1 transmission line transformer.

powders allows greater inductance with fewer turns of wire. To compute the required number of turns to achieve a desired inductance, manufacturers of these products have established a standard reference, A_L values. A_L is the inductance in microhenries for a 100-turn winding on that core. Each core of different materials and different sizes will have a unique A_L. Table 1 is an abbreviated list of core materials, sizes and A_L values (2,3).

To compute the required number of turns for a given inductance in microhenries, use the following formula:

$$\text{Turns} = 100\sqrt{\frac{\text{desired L (uH)}}{A_L}}$$

Also included in most catalogs is a summary of wire sizes versus possible number of turns on each size toroid core. Table 2 lists this data for just one common core size, the T-37, with 0.375 inch outside and 0.205 inch inside diameter. A rule of thumb is that best results are achieved with a winding that covers approximately 3/4 of the core.

For example, if we want a 1.0 uH inductor on a T-37 core, we might choose 6-mix material, with an A_L of 30 uH/100t. Using the above formula, we would need an 18-turn winding. From the wire size chart, we see that 23 turns of #24 wire will fill a T-37 toroid. The required 18 turns would fill about 78 percent of the core, which is close to our 3/4 rule of thumb. If some allowance for compressing or spreading the windings is desired, smaller size wire should be used.

Ferrites

The class of materials generally called ferrites covers many combinations of iron oxide and other metal alloys. The alloys in RF ferrites typically are nickel-zinc, manganese-zinc, and manganese (4,5). Ferrites can have very high μ, which means that they greatly increase the inductance of a given winding.

Only the lowest permeability ferrites are suitable for simple inductors at RF, although they are often used as cores for low frequency inductors. Often, high-μ ferrites are used where inductance values are not critical, such as RF chokes and EMI suppression.

Ferrite's most common use at RF is for transformers and other coupled functions (6,7). The large increase in inductance provided by these materials means that only a few turns are required to get significant inductive reactance. This reactance can be used to block common-mode currents in transmission line transformers. Related transmission line applications include directional couplers, quadrature hybrids, power dividers and combiners. Figure 1 shows a single-ended 4:1 transformer, a typical application for a ferrite-loaded transmission line. Conventional isolated-winding transformers can also be constructed with relatively few turns.

High inductance per turn has two main advantages: minimum conductor length provides better high frequency response, and fewer turns allows larger conductors and higher currents. With proper selection of the ferrite material, the size and type of conductor, and system impedance, components using ferrites can be extremely broadband; several decades in some applications.

Ferrite cores for transformer applications are often supplied in a two-hole arrangement. This is usually referred to as a balun core because of its use in balanced to unbalanced transformers, the most common of which is 75 ohm coaxial to 300 ohm balanced transformers for television. This physical arrangement makes easy layout possible, and

Wire size	No. turns	Wire size	No. turns
#10	1	#26	31
12	3	28	41
14	5	30	53
16	7	32	67
18	9	34	87
20	12	36	110
22	17	38	140
24	23	40	177

Table 2. Number of turns that fit on a 0.375 inch toroid core.

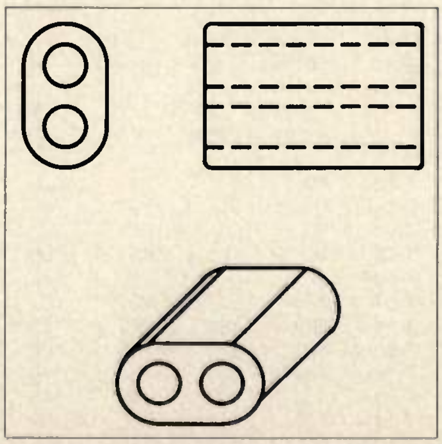

Figure 2. A balun core can simplify transformer construction.

doubles the inductance per turn since the wire passes through the core in each direction (Figure 2).

Limitations

Iron powder and ferrite materials have limitations on frequency of operation, inductor Q, losses, temperature stability, power handling and DC current handling.

Operating frequency and maximum Q are related characteristics which correspond to μ. Magnetic materials offer resistance to the change in magnetic fields as the AC voltage rises and falls. This effect follows the permeability value, so low μ materials will have less effect and be better for higher frequencies. High permeability materials have practical limits on high frequency performance for the same reason.

These limits will be different for inductors, conventional transformers, and transmission line applications since the mechanism of operation is different for each of these. Inductors need high Q and, normally, the best choice is the lowest permeability core that fits wire size and inductance requirements. Conventional transformers can be low Q, and will usually benefit from smaller number of turns. In this case, the user would select a high permeability material that doesn't exhibit excessive loss at the operating frequency. Transmission line transformers rely on the differential currents between conductors, typically either a twisted pair or a coaxial cable. The function of the magnetic material is to provide enough reactance to impede the flow of common mode currents. High permeability is an advantage, but with considerations for power handling, flux saturation and high frequency losses.

Magnetic core materials all are rated by their manufacturers for performance over temperature and for a range of flux densities. Excessive temperature rise will change the characteristics of the core (or even damage it). Magnetic performance is not linear at high flux densities, and materials must be operated within their recommended ranges (8). These limitations on power handling are primarily a function of core material and core size.

As a simple example, a broadband transformer might be constructed on high permeability ferrite to achieve maximum bandwidth. As a low-level device it may be acceptable to have 0.2 dB loss or more, but the same configuration in a high power application could cause excessive temperature rise in the core. Attempting to increase power handling by using a larger core could result in too much inductance in the windings, further degrading performance.

Other characteristics to note include performance well above normal operating frequencies, where these materials tend to be very lossy. This can be used to advantage for suppression of unwanted VHF or UHF responses. It is common to use ferrite beads for suppression of VHF oscillations, but be careful that the added inductance does not affect operation at lower frequencies!

Temperature stability is another area to understand. For critical circuits such as oscillators or very narrow filters, be certain that the inductance value will not have excessive drift with temperature. Some materials have better temperature performance than others. When in doubt, check the manufacturers' temperature curves, or call them for a recommendation regarding your application.

Conclusion

Iron powder and ferrite cores have extremely valuable properties for RF applications. But the proper selection of a material for a specific application is not always simple. Like many areas of RF engineering, there are some common rules of thumb that will help in most cases. But, there are also many additional performance characteristics that must be understood and included in the process of selecting the right magnetic core material for a specific application. If you work with these materials regularly, it is essential to learn how all these characteristics affect performance. *RF*

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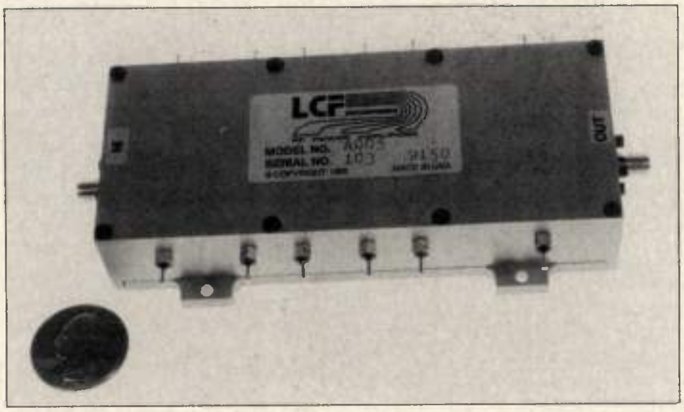
High Efficiency Amplifiers Target Research Applications

A family of miniature high efficiency power amplifiers is introduced, with three models covering 225-400 MHz or 290-400 MHz with 50 percent efficiency, and 225-600 MHz with 40 percent efficiency. Each unit features 35 dB gain with 35 to 50 watts power output, depending on the model. All models measure 4.1×1.4×1.4 inches in ruggedized packaging suitable for missile launch, sounding rockets, geological exploration or atmospheric research applications.
LCF Enterprises
INFO/CARD #250



High Intercept Cellular Mixers

Anzac announces the ESMD-C2HX2 mixer with a guaranteed third order intercept point of +26

dBm with a recommended LO power of +17 dBm. IF response is 20-100 MHz, with an input range of 819-915 MHz, intended specifically for Pan-European GSM base station equipment. Price is $41.85 in 1-9 quantities.
M/A-COM, Inc., Anzac Operation
INFO/CARD #249

Crystal Features Low Aging

World-class crystals with low

aging are announced by EG&G Frequency Products. The 5 MHz and 10 MHz, 3rd overtone crystals exhibit aging better than 3×10^{-10} per day and 5×10^{-10} per day, respectively. They are available in HC-47 holders
EG&G Frequency Products
INFO/CARD #248

900 MHz Power Transistor

The new MRF899 delivers 150 watts PEP at 9 dB gain in the 800 to 960 MHz range, with 26.5 Volt supply. Packaging is the common emitter push-pull configuration. The device is part of a lineup that includes the MRF896 3 watt pre-driver and the MRF897 30 watt driver.
Motorola, Inc.
INFO/CARD #247

Wideband Amplifier

The M50 wideband amplifier covers 10 kHz to 1000 MHz with 10 watts output. The unit is easy to transport, weighing 25 lbs. and packed in a 6.5× 10×14 inch case.
Instruments for Industry
INFO/CARD #246

Standard SAW Oscillators

A new family of standard SAW oscillators is introduced, operating from 300 to 1200 MHz in 100 MHz increments. The devices are designed to be phase-locked over military temperature extremes.
Sawtek, Inc.
INFO/CARD #245

New Capacitor Kits

ATC offers two new Quik Design™ kits containing RF/microwave surface-mount MLCs for circuit designing. The QK 3000 kit contains over 5000 A-case capacitors, and QK 4000 contains over 4000 B-case products. Each kit is priced at $499.95.
American Technical Ceramics
INFO/CARD #244

Signal Processing Components

A new 92/93 catalog covering mixers, attenuators, couplers transformers, modulators and other signal processing components is announced. New products include connectorized wideband amplifiers to 4200 MHz, MMIC wideband amplifiers, DC blocks and complex phasor modulators.
Synergy Microwave Corp.
INFO/CARD #243

Coaxial Resonators

Coaxial line elements are available for frequencies from 300 MHz to 4.8 GHz, offering high circuit Q, temperature stability and fewer environmental effects than equivalent LC circuits. Tape and reel packaging are available for volume manufacturing.
Trans-Tech
INFO/CARD #242

VCXOs for ECL

ECL compatible VCXOs are announced for frequencies up to 250 MHz. Deviations from ±30 ppm to ±200 ppm are available, with control voltage of 0 to −5.2 volts. Initial accuracy is ±10 ppm, with ±3 ppm available at some frequencies.
Oscillatek
INFO/CARD #241

SMT Component Conversion

Conversion of flying-lead components to surface-mounted configurations using the method of welding dissimilar metals is now offered. The consistent lead length and placement improves yield and reliability of finished circuits.
Matrix
INFO/CARD #240

Hopping Filter

K&L Microwave announces a 225-400 MHz rapidly-tunable filter with 6-7 MHz 3 dB bandwidth and 40 watts power handling capability. Rejection is 15 dB at 10 MHz from center frequency.
K&L Microwave, Inc.
INFO/CARD #239

250-400 MHz Oscillators

ECLips logic output oscillators are available in a 14-pin DIP compatible package. High frequency AT-cut crystals are used to provide 100-1000 ppm stability over 0 to 70C. Currently designed frequencies include 250, 266.67, 303 and 400 MHz.
CTS/Frequency Control Division
INFO/CARD #238

Microwave Amplifiers

Amplifiers for the private cable band of 18.1 to 18.6 GHz are introduced, with either WR-51 waveguide connectors or SMA connectors. Both low noise and power amplifiers are available.
Microwave Solutions
INFO/CARD #237

Drop-in Mixers

FEI Microwave announces new drop-in mixers for microstrip applications. The new mixers cover the VSAT bands at 6 GHz and 14 GHz.
FEI Microwave
INFO/CARD #236

New Capacitors

New non-magnetic high-Q porcelain capacitors are introduced by Microelectronics, along with medium and high power ceramic capacitors.
Microelectronics
INFO/CARD #235

Space Qualified Divider

A new 3-way power divider for space applications covers 5.28 to 5.32 GHz with minimum 23 dB isolation, ±0.3 dB amplitude balance, 1 dB insertion loss and ±4 degrees phase balance. 19.5 dB test couplers are included at the input and two outside ports.

Sage Laboratories, Inc.
INFO/CARD #234

Cellular Circulators

Circulators for cellular applications at 800-900 MHz, plus models for 1600-1900 MHz are introduced. These high power (500 watt) circulators exhibit low intermodulation levels and are offered with type N, TNC and SMA connectors.

Ditom Microwave, Inc.
INFO/CARD #233

Switching Subsystems

Integrated switching subsystems are now available, consisting of switches, programmable attenuators and power dividers in a rack-mount enclosure. IEEE-488 and RS-232 control options, plus AC or DC power are options.

JFW Industries, Inc.
INFO/CARD #232

Mil-type Trimmers

7×9 mm ceramic dielectric trimmer capacitors have been added to Sprague-Goodman's line. In seven capacitance ranges from 2.0-8.0 to 7.0-70.0 pF, the trimmers are designed and constructed to meet the requirements of MIL-C-81. Voltage ratings are 350 VDC at 85C and 200 VDC at 125C. Prices start at $0.75 in 1000 quantity.

Sprague-Goodman Electronics
INFO/CARD #231

Artwork Translator

A new low-cost DXF to Gerber translator has been developed specifically for the RF board designer. It can reduce mask generation cost and turn around time.

Artwork Conversion Software, Inc.
INFO/CARD #230

SMD Tuned Circuits

Custom-designed tuned circuits are manufactured in a single chip component. Units can be built at resonant frequencies in the 5 to 400 MHz range. Circuits are available in the standard 1206 chip size, packaged in bulk or on 8 mm tape and reel.

Stetco, Inc.
INFO/CARD #229

1 GHz Spectrum Analyzer

The Farnell model SSA1000A covers 150 kHz to 1 GHz with synthesized frequency. Quasi-peak detection is provided for EMC measurements, and a narrowband AM/FM detector allows signal monitoring. The unit features direct copy of the display to a built-in color printer.

Wayne Kerr/Farnell
INFO/CARD #228

PC-card Preselector

Two models of new PC/AT plug-in module hopping filters are now available. Model PC/AT 1.5-88 covers 1.5 to 88 MHz, and the PC/AT 30-700 covers 30-700 MHz. Each filter has ±1.6 percent −3 dB bandwidth with ±9 percent −30 dB bandwidth, and features 100 ms tuning speed.

Pole/Zero Corporation
INFO/CARD #227

Wideband GaAs IC

A wideband, low noise GaAs amplifier, model BG2011SM-B is announced by Rohm Corp. The ±2 dB band width is 200-1500 MHz, with power gain of 10 dB (typical). Performance is specified at 3 VDC supply voltage.

Rohm Corporation
INFO/CARD #226

New UHF Amplifiers

ENI announces two UHF amplifiers for EMC testing, communications, and other applications. The Model 630L covers 400-1000 MHz with 30 watts, Class A linear. Model 6100 provides 100 watts in Class AB over the same frequency range. Automatic level control, power and VSWR monitoring and an optional GPIB interface are available.

ENI, div. of Astec America, Inc.
INFO/CARD #225

New RF Switches

A new line of switches for commercial telecommunications is announced, for cellular radio, PCN, instrumentation, land mobile radio and other applications in the DC-4 GHz range.

Dynatech Microwave Technology
INFO/CARD #224

Communications ICs

New integrated circuits from Motorola include the MC13155 wideband FM IF for satellite TV and wideband data detection, the MC13135 and MC13136 dual conversion narrow band FM receivers for either quadrature coil ('135) or ceramic resonator ('136) demodulator, and the MC33218 voice-switched speakerphone circuit that supports microprocessor control. Also announced is the MC145191 1.1 GHz PLL frequency synthesizer with on-board 64/65 prescaler and serial interface.

Motorola, Inc.
INFO/CARD #223

EMI Spring Gaskets

Canted coil EMI gaskets will be displayed by Bal Seal. The unique design offers mechanical advantages and maintains shielding performance. Stainless, beryllium copper and plated products are available.

Bal Seal Engineering Co.
INFO/CARD #222

1000W Amplifier

The new Model 1000A100 solid-state broadband amplifier covers 10 kHz to 100 MHz, delivering 1000 watts CW power. The amplifier is recommended for susceptibility testing, and includes automatic leveling, instantaneous full bandwidth, immunity to load mismatch, remote control interface and other operating features.

Amplifier Research
INFO/CARD #221

Laboratory Amplifier

Trontech announces the P2450M-46-PS, a 20 watt Class A amplifier with 36 dB minimum gain and +46 dBm power at 1 dB compression. The unit covers 2445-2455 MHz, and is one of a series of amplifiers for applications in the 500-4000 MHz range.

Trontech Inc.
INFO/CARD #220

Near Field Probes

The CHASE NFPS1 near field diagnostic probe set has been introduced, consisting of two magnetic and one electric field probes for EMI measurement from 9 kHz to 1 GHz. A carrying case, 30 dB preamp and magnetic probe calibration kit are included.

IBEX Group Inc.
INFO/CARD #219

High Power Terminations

A new line of high power 50 ohm loads includes models for 15, 30, 50, 100, 250 and 500 watts. Frequency coverage is DC to 18 GHz with low VSWR and conductive cooling. Connectors offered are SMA or type N, male or female.

Component General, Inc.
INFO/CARD #218

TO-8 Amplifier

Cougar Components introduces the AP2009 cascadable amplifier, with 11 dB gain and +28 dBm power output over 10-2000 MHz. A third order intercept point of +40 dBm and low noise figure of 3.5 dB are additional featured of this device.

Cougar Components
INFO/CARD #217

4 Watt T/R Switch

The AH001R2-12 GaAs MMIC transmit/receive switch capable of handling 4 watts at 1 dB compression (3 watts at 0.1 dB) is introduced, offered in a plastic SOIC-8 package. Applications include PCN and portable cellular equipment.

Alpha Industries
INFO/CARD #216

Low-Loss SAW Filters

High frequency SAW filters with up to 1.5 GHz center frequency have insertion loss of less than 10 dB. A example of this line is the TO-8 packaged FBA 527, centered at 731 MHz, with 2.5 MHz bandwidth and 40 dB rejection.

Thomson-ICS Corp.
INFO/CARD #215

High Speed DAC for DDS

The new AD9720 is a 400 MSPS ECL digital-to-analog converter designed for direct digital frequency synthesis, waveform generation, IF modulation and professional video applications. Key specifications include a 1.5 pV glitch impulse, 4.5 ns settling to LSB and 75 dB of dynamic range.

Analog Devices Inc.
INFO/CARD #214

Low Noise OCXOs

A series of oven controlled oscillators providing +7 dBm output in the 25 through 140 MHz range is announced. Temperature stability is $\pm 5 \times 10^{-9}$ over 0 to +50C and $\pm 5 \times 10^{-8}$ over −55 to +85C. Phase noise at 100 Hz offset is −130 dBc/Hz.
Vectron Laboratories, Inc.
INFO/CARD #213

Custom RF Filters

Bandpass, band reject, highpass and lowpass filters from 2 to 10 poles are available from Raltron as custom designs. Filters from 1 to 150 MHz can be made to spec in as little as two weeks. Small packages, linear phase and other special applications are also offered.
Raltron Electronics Corp.
INFO/CARD #212

Sealed PTFE Trimmers

A new line of sealed trimmers uses PTFE instead of air as the dielectric. Voltage ratings up to 2000 working volts are available, and capacitance to 25 pF is offered. Sizes are 0.23 or 0.30 inch diameter by 0.48 inch long.
Voltronics Corp.
INFO/CARD #211

1 to 2 GHz VCO

VCO model HV67T-1 operates from 1 to 2 GHz with +10 dBm output power. SSB phase noise is typically −105 dBc/Hz at 50 kHz offset. Power required is +15 VDC at 50 mA, with 0 to +20 volts tuning range. TO-8 packaging is standard, with flatpack and connectorized models also available.
Magnum Microwave
INFO/CARD #210

Downconverter/ Carrier Tracking ASIC

The STEL-2130 digital downconverter/carrier and tracker ASIC is introduced. It permits implementation of conventional and spread spectrum modem configurations and performs the final down-conversion from digitized IF to baseband. The chip's digital IF sampling can operate at up to a 40 MHz sample rate with either I/Q input pairs of a single input stream. The ASIC is packaged in an 84-pin, 1.2" square, plastic, leaded chip carrier.
Stanford Telecom
INFO/CARD #209

High Gain Transistors

VHF/UHF transistors are introduced with a power gain of above 10 dB. The BLF547 and BLF548 are n-channel enhancement mode transistors. They develop output powers of 100 and 150 W at 500 MHz and accept a nominal supply voltage of 28 V, and have an efficiency of above 50 percent. The transistors come in a 4-lead balanced flange package with two ceramic caps.
Philips Semiconductors
INFO/CARD #208

Dual Amplifier

A new dual 1.2 GHz RF amplifier circuit uses BiCMOS technology to achieve a wideband frequency response (DC to 1.2 GHz) with standby power of 95 mA. The circuits include 50-ohm matching, internal compensation and biasing, as well as an enable pin. The NE/SA5200 is available in an 8-pin small-outline plastic package with an enable/power-down pin for turning the amplifier off for front-end buffering in receiver applications.
Signetics Company
INFO/CARD #207

Custom Cables

A complete line of flexible and semi-rigid cables is available. A complete line of SSMB and SSMC microminiature connectors are available in addition to SMA, SMB and SMC connectors. Certification of all characteristics, including phase matching, is available.
Applied Engineering Products
INFO/CARD #206

An Active Frequency Multiplier

By Jonathan Bird
Raytheon Company

Many frequency multipliers are passive and require amplifiers on both the input and output because they exhibit a rather large conversion loss. This simple design, an entry in the 1991 RF Design Awards Contest, will generate tons of harmonics if driven with a modest input power with a conversion gain or a small loss, depending on which harmonic is extracted.

The operational amplifier shown is a Harris HA5004 current feedback amplifier, which was featured in an article in *RF Design* magazine in December, 1990. This amplifier has a useful bandwidth of about 100 MHz and will therefore multiply up to about that frequency. This makes the multiplier useful in ranges where normal op amps just could not be used.

The circuit operates the way most multipliers do, by generating harmonics of an input signal and filtering the appropriate harmonic out as the multiplied frequency. This design is different because it uses the feedback loop of an amplifier to achieve these harmonics. This effectively isolates the input circuit from the 'clipping' circuit, a feature which makes the design especially attractive.

The diodes in the feedback loop give the feedback a non-linear characteristic. Rationalizing the design: as the input voltage grows as a function of time, the output of the amp tries to make the inverting terminal equal to the non-inverting (input) terminal through the feedback loop. To do this, it needs only to overcome the diode drops. Therefore, the output voltage is never more than a diode drop (or two) greater than the input voltage. By using high speed Schottky type diodes, the diode drops are only around 0.2 volts. This limits the gain available and also makes the gain non-linear as a function of drive level. This will be explained in greater detail later.

Remembering the Fourier Series for a square wave:

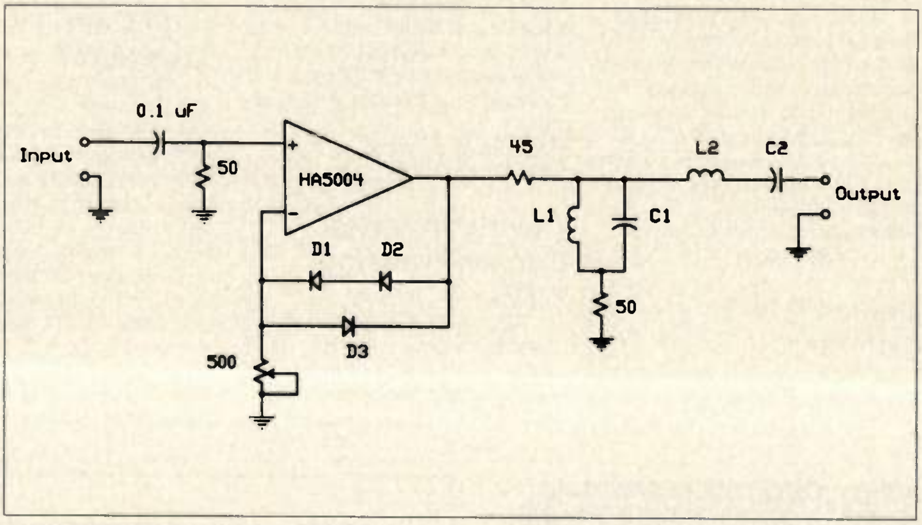


Figure 1. Frequency multiplier circuit.

$$f_1 + \frac{1}{3f_3} + \frac{1}{5f_5} + \frac{1}{7f_7} + \ldots\text{etc.} \qquad (1)$$

A perfect square wave is made up of an infinite series of odd harmonics, each one lower in amplitude than the previous one. Therefore, any circuit attempting to square off a sine wave (as this one does) and extract a higher order harmonic (like a seventh or ninth for example) will have a hard time, due to the increasingly small amplitudes of those harmonics. For 2nd, 3rd, 4th and 5th harmonic applications, this circuit will do a good job. You may be wondering at this point why there are two diodes pointing one way (D1, D2) and one pointing the other way (D3). By allowing more voltage drop in one direction than the other, the waveform becomes asymmetrical. Any waveform which is completely symmetrical will be composed entirely of odd harmonics according to Fourier's theorem. If one wishes to build an effective frequency doubler or quadrupler (therefore needing harmonics), it is necessary to emphasize these harmonics by manipulating the waveform to be asymmetrical. To make an even harmonic multiplier, you can use the design shown. To make an odd harmonic multiplier, remove D1, to retain symmetry. The 500 ohm potentiometer shown allows fine tuning of the circuit by changing the feedback current. This changes where the V_d sits with respect to the knee of the diode V-I curve. I do not recommend actually using a potentiometer, but rather experimenting with different resistor values to achieve the desired results. Proper selection of this component is critical.

Input power	Gain
−10 dBm	9.5 dB
0 dBm	4.2 dB
+10 dBm	1.6 dB
+20 dBm	.5 dB

Table 1. Theoretical gain as a function of drive level.

The output matching and filtering is achieved with a simple diplexer. This part of the circuit doesn't even need to be used when testing the circuit in breadboard applications. Both parts of the diplexer (L1 and C1, L2 and C2) should be tuned to the frequency of the harmonic you wish to keep. In this way, L2 and C2 pass the frequency of interest while L1 and C1 properly terminate all the other frequencies (and reflections from L2 and C2). Of course, this simple diplexer may be replaced with a more effective circuit if necessary.

Just a word about the gain of this circuit. By examining Kirchhoff's laws, it can be proved that the gain of this circuit (without considering effects of the diplexer) is:

$$V_{in} = V_{+} = V_{-} \quad (2)$$

and

$$V_{out} = V_{-}(+0.2) \quad (3)$$

therefore,

$$V_{out} = V_{in} + 0.2 \quad (4)$$

$$\frac{V_{out}}{V_{in}} = \text{Gain} = \frac{V_{in} + 0.2}{V_{in}} \quad (5)$$

This assumes one diode in each direction and V_d of 0.2 volts.

For different input levels, the gain is different, due to the non-linear feedback of the diodes. Table 1 shows theoretical gain as a function of drive level:

Gain is fundamental. Actual power in any harmonic must be extracted using Fourier analysis, or experimentally. An actual conversion gain may not be possible at higher harmonics, due to their lower relative power level. The loss experienced at these harmonics, however, is smaller than with conventional multipliers.

Table 1 shows that more gain is obtained at lower drive levels. Furthermore, more clipping is achieved at lower drive levels because a larger percentage of the output waveform is clipped at lower drive levels than at higher drive levels. While most multipliers work better when supplied with a large drive level, this one works better with a small drive level.

If more gain is necessary, it is possible to place two or three diodes in each direction in the feedback loop, if the diodes are fast enough. This will increase the gain by increasing the diode voltage drops in the feedback loop. Although the gain will still vary as a function of drive level, this may get the amplitude of the higher harmonics up enough to offer conversion gain. Different combinations of diodes in the feedback loop also may change the characteristic shape of the waveform, emphasizing certain harmonics more than others. *RF*

About the Author

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INFO/CARD 111

The PLL Dead Zone and How to Avoid It

By Allen Hill and Jim Surber
Analog Devices, Inc.
Computer Labs Division

The architecture of the phase/frequency detector stage in a phase-locked loop circuit has great bearing on the magnitude of the output signal's phase error in high-speed applications. There are many sets of system characteristics which determine the PLL's ability to lock onto signals with various degrees of phase shift, but this article will concentrate on the characteristics that come into play only when the PLL is in the locked condition and, specifically, those which minimize the phase noise in the VCO's output at high frequencies.

Great pains and exacting calculations are required in the design of the loop filter in order to minimize reference feedthrough and increase the stability of the PLL. Precise loop filter designs will minimize the side-band aberrations from extraneous signals, and the summation effects of the multiplier, but the phase detector stage controls the phase noise stability of the output signal at PLL lock. In the basic PLL architecture, the phase detector stage compares the phase of the VCO's output against that of a reference signal, and generates an error voltage whose mean DC value is proportional to the phase differential between the two. This error signal is filtered to extract the mean DC content, and serves as the feedback control in the VCO. Any aberrations that are present on the DC level naturally will translate into phase distortion at the output of the VCO.

A common type of architecture for the phase detector stage is the digital phase-frequency detector as shown in Figure 1. The commonly-used Motorola MC4044 device is an example of this architecture.

This digital device utilizes flip-flops which allow the PLL to operate as a frequency detector initially upon power-up, and as a phase detector ultimately, to achieve final loop lock. This scheme has the advantage of allowing the PLL to achieve lock at system start-up no matter how far apart the VCO's output and the reference frequency input. When the phase-frequency detector is close to lock, the U output is a pulse train with an average value proportional to the phase difference of the R and V inputs; the D output is locked low. This non-complementary, differential output data, requires a charge pump (normally provided internally to the chip) to transform it into a single-ended signal that can be used to drive a VCO input. When the transitions at inputs R and V coincide, the typical digital phase-frequency detector's U and D outputs are in a steady logic "1" state, indicating loop lock. When there is a change in the phase of the transitions on the R and V inputs, the phase-frequency detector requires a finite period of time to respond and register the change on the U and D output. This time period is due to propagation delays within the various logic gates of the device. This non-linear region on the device's transfer curve is called the "dead zone" and is not generally well-characterized on the typical phase comparator data sheet. However, the dead zone can have a profound effect on phase noise in the PLL when the reference frequency is 10 MHz or higher. Figure 2 displays a typical phase gain plot for a phase-frequency detector operating at 20 MHz.

As is evident in the plot, the non-linear, or dead zone, region of the transfer function may cause the PLL to be non-responsive in the range of ±30 degrees of 0 degrees and is responsible for increasing the phase noise in the PLL's high-speed output signal. This dead zone region may be moved up or down the VCO's input range by injecting offset voltage at the VCO input, but this technique will reduce the PLL's overall phase detection range which defeats one of the original advantages of the digital phase-frequency detector architecture.

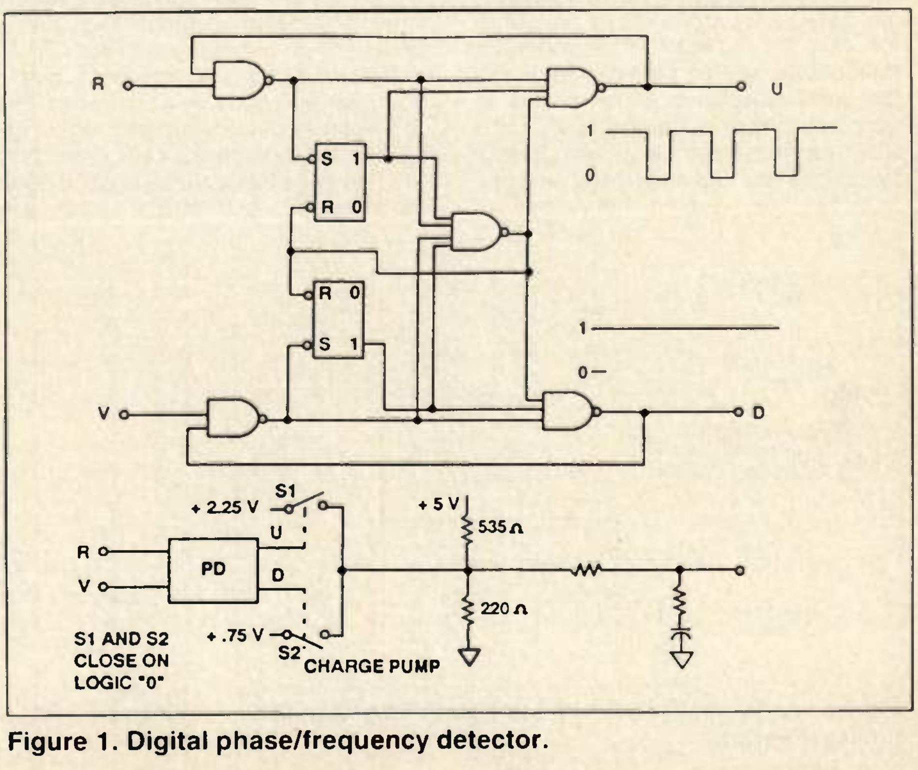


Figure 1. Digital phase/frequency detector.

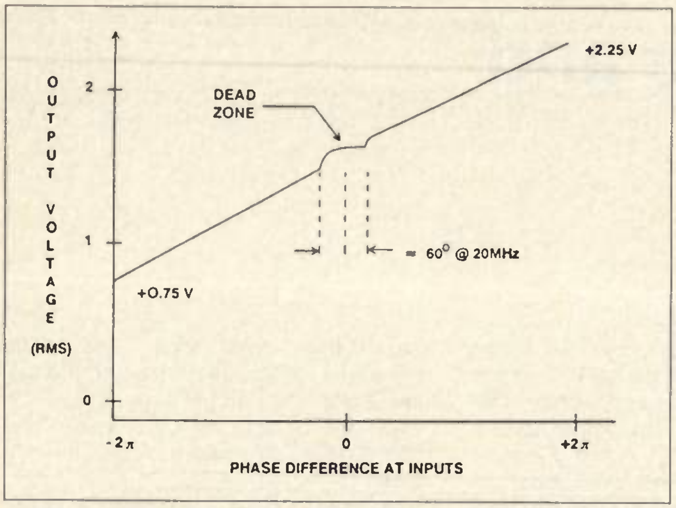


Figure 2. Phase gain plot for digital phase/frequency detector at 20 MHz.

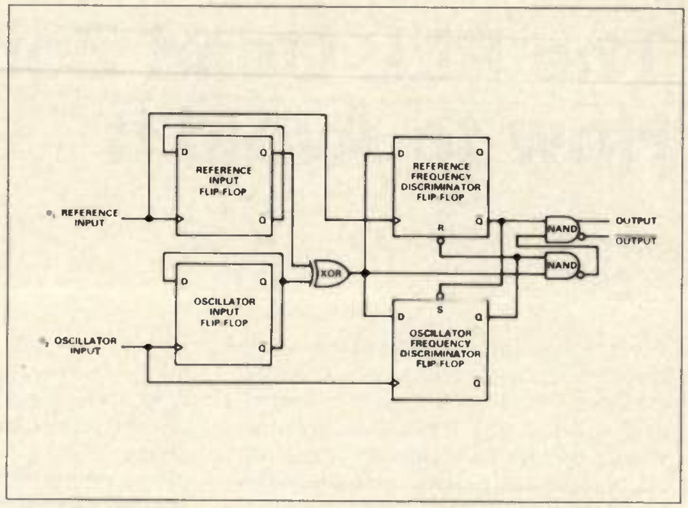


Figure 3. Phase/frequency discriminator schematic.

A second type of digital detector architecture is called the phase/frequency discriminator. The Analog Devices AD9901 is an example of this architecture. As Figure 3 shows, this device employs several more digital gates than are present in the phase/frequency detector, which serve to enhance the performance of the PLL at lock and reduce the effects of the dead zone.

It utilizes four "D" flip-flops, an exclusive-OR gate (XOR), and two nand gates in an architecture that generates a square wave output at lock. At start-up, the detector operates as a frequency discriminator (if the VCO and reference frequencies are far enough apart) and the output flip-flips are clocked low to inhibit the XOR gate and pull-in the VCO. Once the two inputs are close in frequency, the input flip-flops and the XOR becomes active. The function of the input flip-flops is to perform a divide-by-2 function on both the input and reference frequencies. This generates a square wave to drive the XOR gate that is independent of the duty cycle of the input frequency.

The two square waves constitute the inputs of the XOR gate which, in turn, will generate a square wave with exactly 50 percent duty cycle when its two inputs are 180 degrees out of phase. Any difference in the phase of the two inputs results in a corresponding change in the duty cycle of the output of the XOR. Figure 4 shows the timing of the various waveforms within the phase/frequency discriminator at lock.

Note that the discriminator's output is a perfect square wave when the reference input and oscillator inputs are exactly 180 degrees out of phase. With the reference input phase angle leading the oscillator, the XOR's output duty cycle will be less than 50 percent. With the reference input's phase angle lagging the oscillator's, the XOR's output duty cycle will be greater than 50 percent. Therein lies the advantage to this type of phase comparator architecture. By filtering the XOR's pulse train output to extract the mean DC component to drive the VCO, a more stable lock condition is achieved than with the digital phase-frequency detector. The transfer function of the phase-frequency discriminator near lock is shown in Figure 5 and is described mathematically as:

$[K_d (\theta_1 - \theta_2)]/(V/rad)$

Where: K_d is the output voltage range divided by 2π.

An important aspect of the phase-frequency discriminator is that at lock

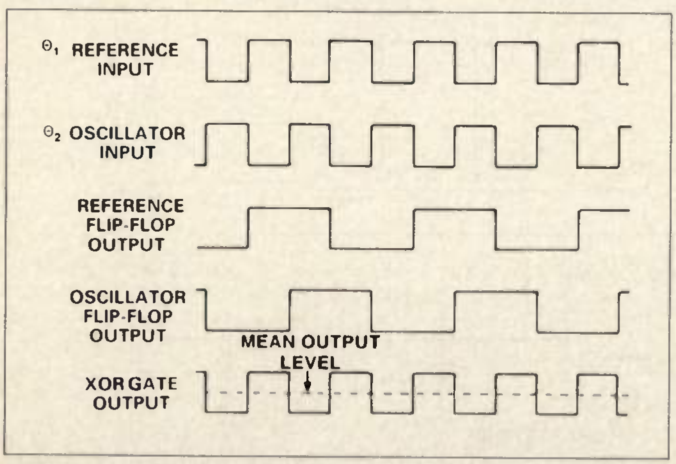


Figure 4. Phase/frequency discriminator, AD9901, timing diagram.

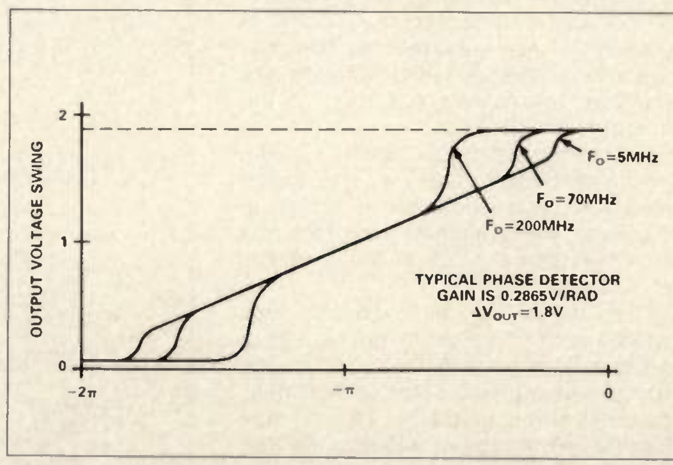


Figure 5. Phase/frequency discriminator phase gain plot.

(reference and oscillator 180 degrees out of phase), the device is operating in a linear mode. Any shift in the phase angle of the VCO output or input reference frequency, will directly change the duty cycle of the phase-frequency discriminator's output. The dead zone associated with the 0 phase angle differential in the previously described phase-frequency detector is eliminated, and any phase variation of the R and theta inputs results in an immediate change in the mean DC value of the output. This architecture results in reduced jitter on the VCO input and minimum phase noise in the output signal.

The actual proof of the negative effects of the dead zone are found in high-speed PLL applications where phase noise contributes significantly to output signal distortion. To characterize the extent of the contribution of the dead zone, we devised two experiments to quantify the PLL's performance using both the detector and discriminator-types of phase comparator architectures. As a test bed for the experiments, we first constructed an 80 MHz PLL circuit (see Figure 6) utilizing a 20 MHz reference signal. The PLL circuit was intentionally designed such that the phase detector stage could be easily interchanged between the Analog Devices AD9901, and the Motorola MC4044-type devices for performance comparisons. Obviously, our primary goal in designing this PLL was not necessarily to achieve the highest dynamic performance possible. Instead, we required a circuit that would facilitate the observation and characterization of the dead zone within the linear detection range of the phase comparator stage at higher PLL frequencies. We analyzed both the output signal of the PLL, and the output of the phase comparator, for dead zone-related anomalies. Each of the experiments and results will be discussed individually with an analysis of the implications of the results.

The PLL was designed to generate a 80 MHz sinewave referenced to a 20 MHz sinewave with special modulation capability added to the VCO input. This combination was determined to be of a high-enough frequency to exacerbate the problems associated with the dead zone, yet simple enough to be easily implemented on the test bench. We used a Colby oscillator to generate the 20 MHz reference frequency because of the requirement for purity and stability of the signal. For the loop filter, we selected a single-pole RC lowpass network because of its simplicity, justified by the fact that we were interested only in the characteristics of the linear detection range and not the performance of the overall PLL. The cutoff frequency of the filter was 1.7 kHz which is much higher than would normally be used in a PLL circuit. However, we required the extra bandwidth because we were intending to modulate the loop with a triangle wave in order to analyze the entire linear detection range of the phase comparator.

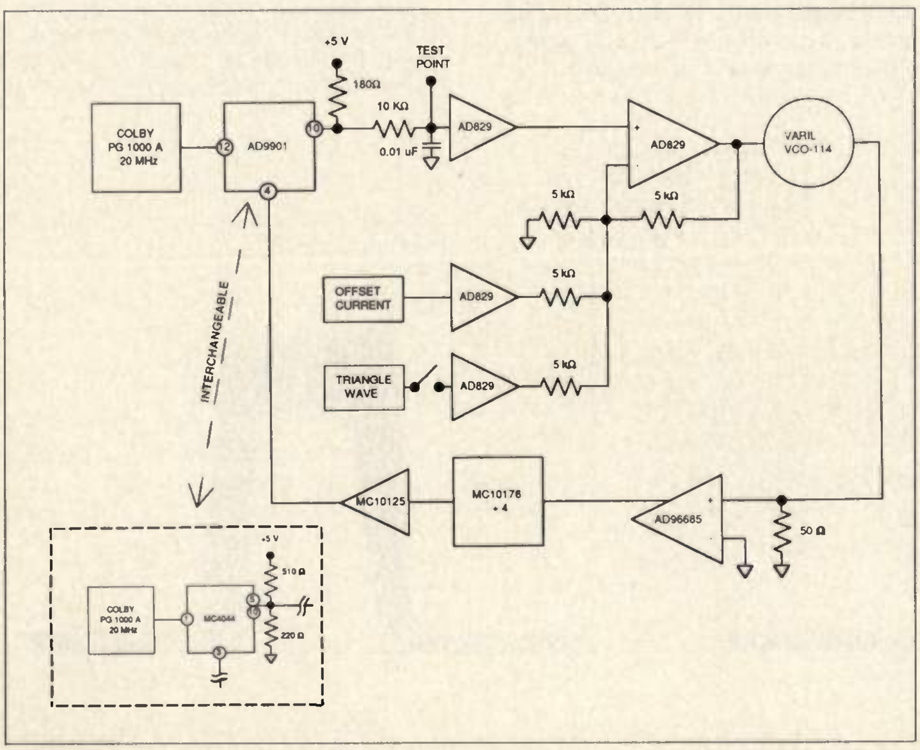


Figure 6. 80 MHz PLL block diagram.

The VCO output was connected to a high-speed ECL comparator which, in turn, drove a divide-by-four counter. A high-speed operational amplifier was connected to the output of the phase comparator to act as a buffer and driver for the VCO input. A current source was connected to the inverting input of the buffer amplifier to allow an offset adjustment of the detection range. A triangle waveform generator, as previously discussed, was also connected to this point in one of the experiments as a means of causing the phase comparator to swing through its entire detection range in a controlled and measurable fashion.

For the purpose of observing the linear detection range of both phase detectors, we used a digital oscilloscope to actually display the dead zone region, at PLL lock, on the lowpass filtered output of both devices. A 12.5 Hz triangle wave was applied to the input of the VCO, via the buffer amplifier, to modulate both phase detectors through their full detection ranges. The oscilloscope test point was at the output of the resistor/capacitor lowpass filter for both phase comparator devices. In this manner, the linear region at lock could be directly observed. Figure 7a shows the actual scope display of the PLL running at 80 MHz with the MC4044 device installed as the phase detector.

The dead zone associated with this architecture is manifested as the flat spot in the linear detection range which occupies approximately 100 degrees of the detection range. With the AD9901 device installed in the same PLL circuit, under the same conditions, Figure 7b shows that the detection range is virtually linear and that all of the effects of the dead zone are conspicuously absent. This latter mode of linear phase detection at loop lock will afford much lower phase noise and faster loop response time in a higher-speed PLL circuit.

As a further measure of quantifying the performance improvements afforded by the AD9901 phase/frequency discriminator, we observed the PLL output, at lock, with a spectrum analyzer. With

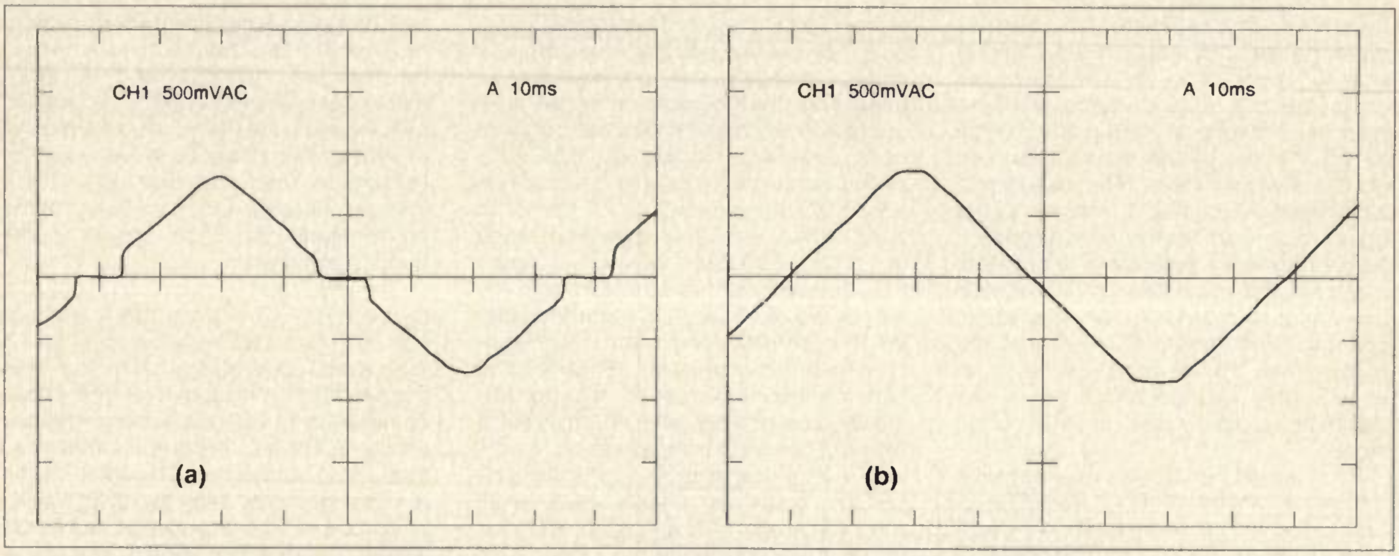


Figure 7. Oscilloscope plot of detection range, a) MC4044 installed, b) AD9901 installed.

the fundamental frequency of 80 MHz, the spectral plot reveals a marked difference in the frequency spread of the fundamental generated by the two types of architectures of phase comparator. Figures 8a and 8b are actual plots from a wide-bandwidth spectrum analyzer showing that the entire lock region for the AD9901 device occupies a frequency spread of approximately 400 kHz.

When the MC4044 device was substituted as the phase detector in the test PLL circuit (see Figure 8b), the spectrum analyzer displayed a fundamental frequency spread, at the lock region, of some 6 MHz. The increased width of the fundamental is due to jitter in the output of the phase detector which is attributable to the presence of the dead zone in the linear detection range.

This analysis served to quantify and characterize the effects of the dead zone in a high-speed PLL circuit. By comparing the operation of the AD9901 and MC4044 interchanged in a high-speed PLL, some of the problems resulting from a non-linear region in the detection range were made obvious. Although this set of experiments was not meant to detail every aspect of the dead zone or the parameters affected in every high-speed PLL application, it should certainly cause the designer to carefully consider alternative architectures when selecting the phase comparator stage. ***RF***

About the Authors

Allen Hill is an applications engineer for the Greensboro, NC division of Analog Devices. He has been with Analog Devices for 10 years. Jim Surber is currently a regional marketing engineer supporting sales and marketing in Japan and the Midwestern United States. Allen Hill can be reached at (919) 668-9511.

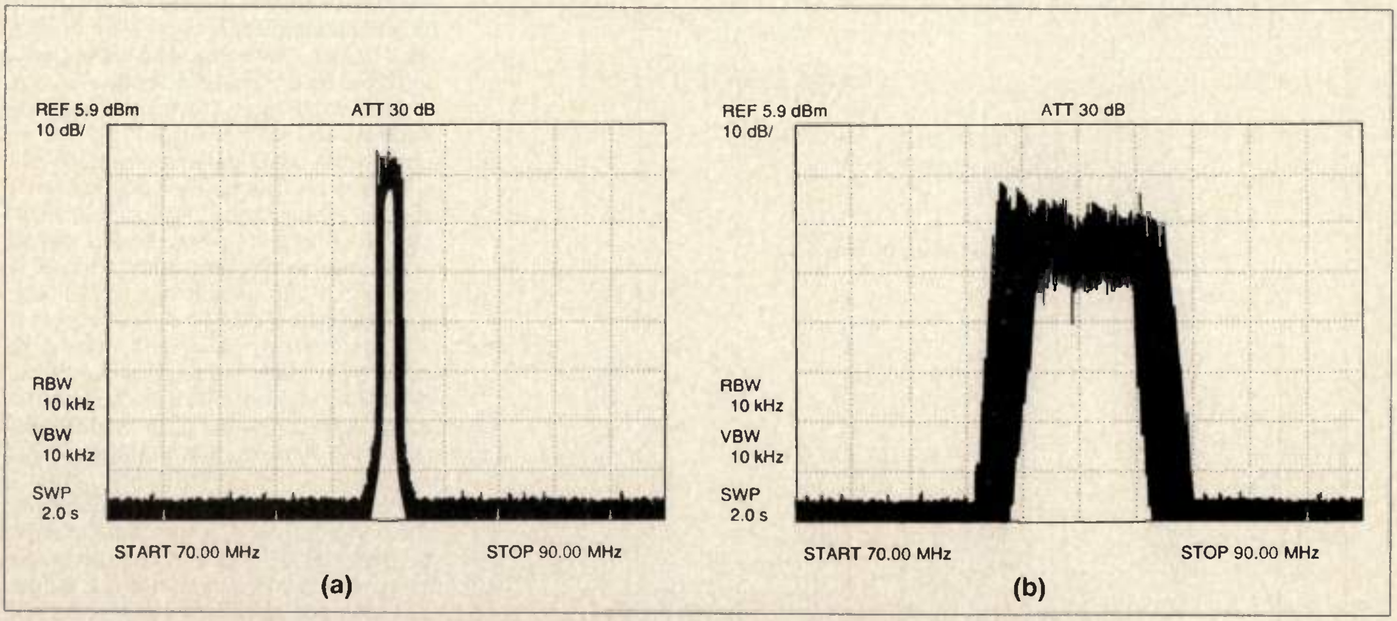


Figure 8. Spectral plot of detection range, a) AD9901 installed, b) MC4044 device installed.

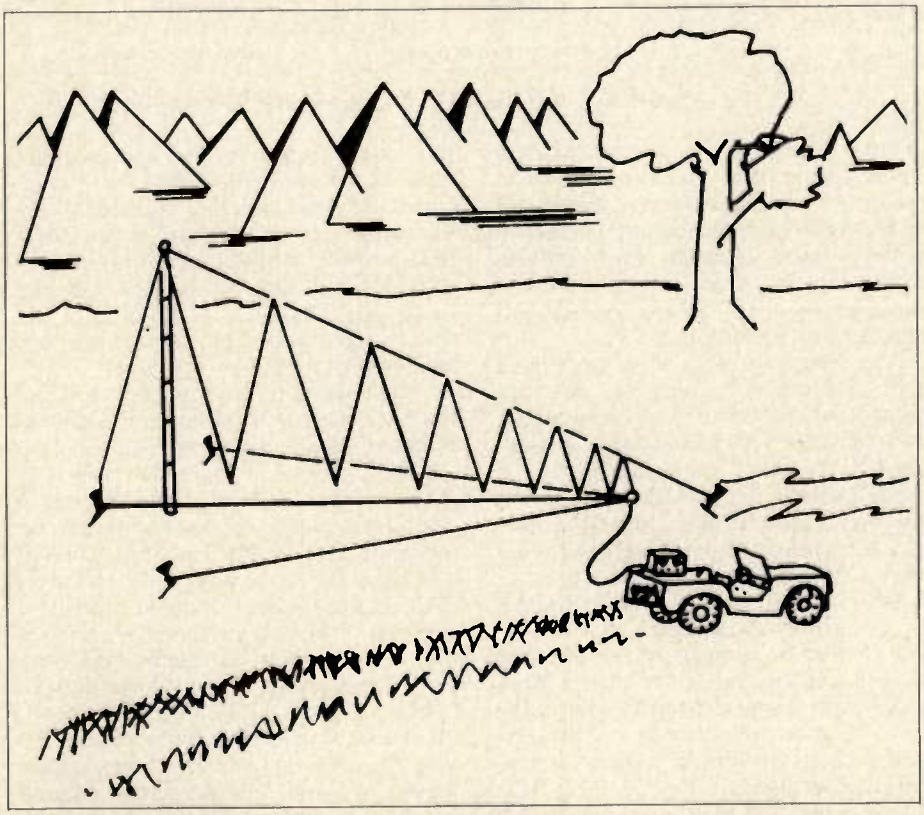
A Field Expedient Broad Band HF Antenna

By Bernard Feigenbaum
U.S. Army CECOM

Trying to design an antenna that is an exact solution for various real world problems is certainly a difficult task. It is better off to assume an antenna configuration based upon intuition and an educated guess and use a computer with Numerical Electromagnetic Code (NEC) to simulate antenna performance. An intelligent set of trial designs and prudent parameter changes suggested by a good understanding of the problem can lead to a considerable improvement over present commercial antenna configurations.

Effective High Frequency (HF) antennas that are compatible with the varied and demanding requirements peculiar to expeditions and military tactical communications are by no means easily engineered. Military HF radios operate over a broad band from 2-30 MHz. The HF communication system must be compact and lightweight to be transportable by vehicle or beasts of burden, such as mule or dog sled, to desolate territories and wilderness areas which often necessitates ionospheric propagation over range paths of many hundreds, even thousands of miles.

The required mobility would suggest small antenna size of light weight, but then the radiation characteristic will be compromised if the antenna is made too small in terms of the wavelength. The necessary broad frequency range, which typically spans three octaves, imposes difficulties on the design of a small and reasonably efficient HF antenna.



The zig-zag antenna deployed in the field.

The king of broadband HF antennas is the log periodic (LP). The trade-off is that this antenna is considered a permanent construction, and therefore, not field expedient. There are a number of commercially available log periodic dipole antennas which are touted to be "transportable" in order to sell them to various government agencies of many nations. Experience with these so called transportable antennas reveals that they are unwieldy, difficult and time consuming to erect and retract, expensive, and because of the very large physical size when erect, they restrict the number of possible sites by political, zoning, logistics, and the grand size of open field required.

There are other types of antennas that are field expedient and their limitations are identified here.

The dipole is not broadband but can be made so by sloping the ends to earth and terminating them with resistors. It will then exhibit a broadband impedance but still suffers from frequency dependent radiation patterns. Therefore, it is not effectively broadband. Moreover, the radiation patterns form nulls at elevation angles that are useful to propagation.

The sloping vee is also made broadband with terminating resistors. This antenna's radiation pattern is sensitive to the angle of the vee and is frequency dependent.

The long wire beverage antenna is the third field expedient antenna. It too is made broadband with terminating resistors. It should be four wavelengths long at the lowest operating frequency which is nearly 2,000 feet at 2 MHz. The radiation pattern is also sensitive to frequency changes.

The Solution

The zig-zag sky-wave antenna has similar impedance and radiation pattern characteristics as the log periodic; but

	CM ZIG-ZAG SKY-WAVE ANTENNA
	CE SOMMERFELD GOOD GND
Antenna Geometry	GW,1,1,1.4,0.,0.,1.7,0.,1.1,.0009
	GW,2,1,1.7,0.,1.1,2.,0.,0.,.0009
	GW,3,1,2.,0.,0.,2.4,0.,1.3,.0009
	GW,4,1,2.4,0.,1.3,2.7,0.,0.,.0009
	GW,5,1,2.7,0.,0.,3.25,0.,1.8,.0009
	GW,6,1,3.25,0.,1.8,3.8,0.,0.,.0009
	GW,7,1,3.8,0.,0.,4.6,0.,2.6,.0009
	GW,8,1,4.6,0.,2.6,5.3,0.,0.,.0009
	GW,9,1,5.3,0.,0.,6.4,0.,3.8,.0009
	GW,10,1,6.4,0.,3.8,7.5,0.,0.,.0009
	GW,11,1,7.5,0.,0.,8.9,0.,5.2,.0009
	GW,12,1,8.9,0.,5.2,10.3,0.,0.,.0009
	GW,13,1,10.3,0.,0.,12.3,0.,7.2,.0009
	GW,14,1,12.3,0.,7.2,14.25,0.,0.,.0009
	GW,15,2,14.25,0.,0.,17.,0.,10.,.0009
	GW,16,2,17.,0.,10.,20.,0.,0.,.0009
Lift antenna 1 meter above gnd.	GM,0,0,0.,0.,0.,0.,0.,1.
Rear connection to gnd.	GW,17,1,20.,0.,0.,20.,0.,1.,.0009
Front connection to gnd.	GW,18,1,1.4,0.,0.,1.4,0.,1.,.0009
Request gnd. plane	GE,1
Gnd. plane constants	GN,2,0,0,0,15.,.01
Generate signal @ seg. #18; 1,0V @ 450Ω	EX,0,18,1,11,1.,0.,450.
Load seg. 17 with 400Ω	LD,4,17,1,1,400.,0.
Signal freq. (set @ 4 MHz)	ER,0,1,0,0,4.
Request Patterns	RP,0,1,73,1110,75.,0.,0.,5.
	RP,0,37,1,1110,−90.,0.,5.,0.
	EN

Figure 1. Metric dimensions.

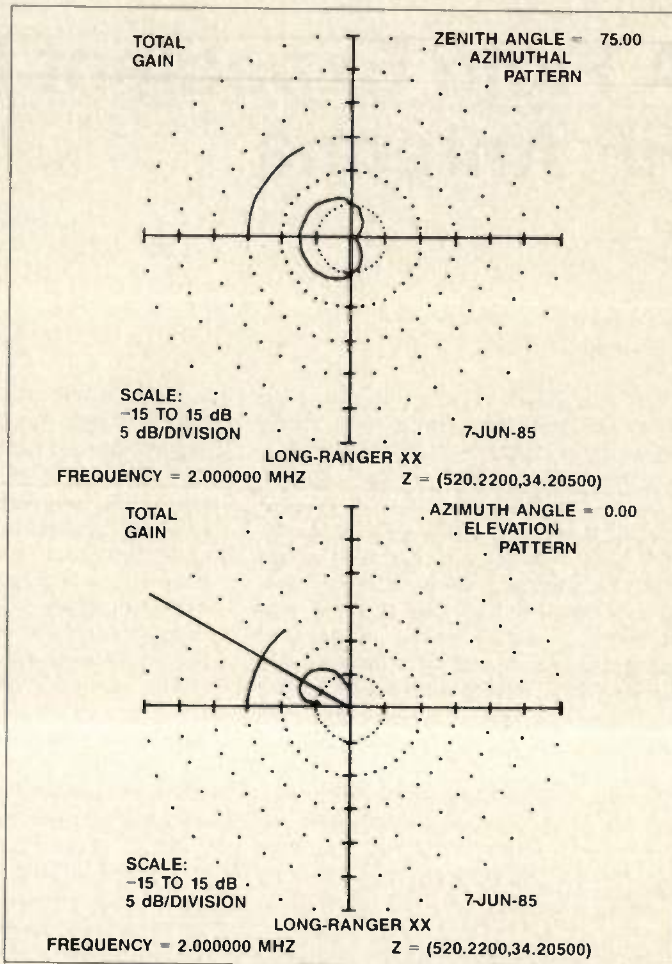


Figure 2. Performance characteristics at 2MHz.

does not have the super gain quality because it is much smaller. However, it has standard gain similar to a standard half wave antenna. Its advantage is that it occupies less real estate than any of the other field expedient antennas. It can be truly said that this is a field expedient, tactical, HF log periodic antenna and the principle behind its operation is the subject of a recent patent.

This recent antenna development is the perfect enhancement for the new generation of frequency agile HF radios. It combines transportability, electrical performance, easy assembly and low cost. The new antenna makes log periodic characteristics available at a fraction of the cost of a full size LP antenna. The cost to purchase, install and maintain a full size LP antenna is enormous.

The invention antenna creates more opportunity for HF radio systems. It was the primary objective of the miniature HF log periodic antenna invention to achieve a broadband, directional, sky-wave design that is extremely small compared to current commercial HF antenna designs. A concurrent objective of the antenna invention was to provide a miniature HF directional antenna that is inexpensive, easy to erect and retract, and has a small footprint.

The foregoing and other objectives are achieved in a preferred embodiment, both patented and copyrighted, wherein ten interconnected, vertical, zig-zag, antenna sections are of a predetermined increasing height. The antenna is terminated by an appropriate resistance so as to maintain the characteristic impedance over the entire frequency range of interest. A counterpoise is utilized to balance the antenna system. Power is coupled to the shortest zig-zag section via a 9:1 broad band impedance matching transformer. The currents that are induced on the antenna cause power to radiate at low elevation angles.

It is a peculiar feature in that, unlike the conventional log periodic antenna, the miniature HF antenna is a non-resonant log periodic directional antenna which achieves a single main beam by virtue of satisfying the Hanson-Woodyard condition; one of the few instances where it is practical to obtain more directivity from an array with reduced inter-element spacing.

The miniature log periodic antenna has constant impedance and radiation characteristics similar to a full size log periodic antenna. Therefore, it is suitable for use with the new breed of frequency agile HF radios employing scanning, automatic link establishment (ALE), automatic channel evaluation (ACE), and multiple channel operation. Even so, it is also excellent for use with single frequency HF radios operating from base camps or long range surveillance units.

The performance of the miniature HF log periodic exceeds the performance of any other HF field expedient antenna used for sky-wave (ionosphere) communications.

The miniature antenna is also superior for transport. The antenna, less the mast, weighs 25 pounds and is stored in a utility bag. The whole system can even fit in the trunk of a car. The miniature antenna can be erected by one man in 45 minutes in fair weather and because of its light weight, it can be erected on soft ground without the need for concrete reinforcements.

U.S. patent no. 4,733,243 was issued for this antenna on March 22, 1988. The antenna is available by means of Technology Transfer agreements between the U.S. Army and industry. *RF*

About the Author

Bernard Feigenbaum is an electrical engineer with the U.S. Army Communication and Electronics Command, Center for Command, Control and Communications Systems. He may be reached at U.S. Army CECOM, C3 Systems, Ft. Monmouth, NJ 07703. Tel: (908) 544-4532.

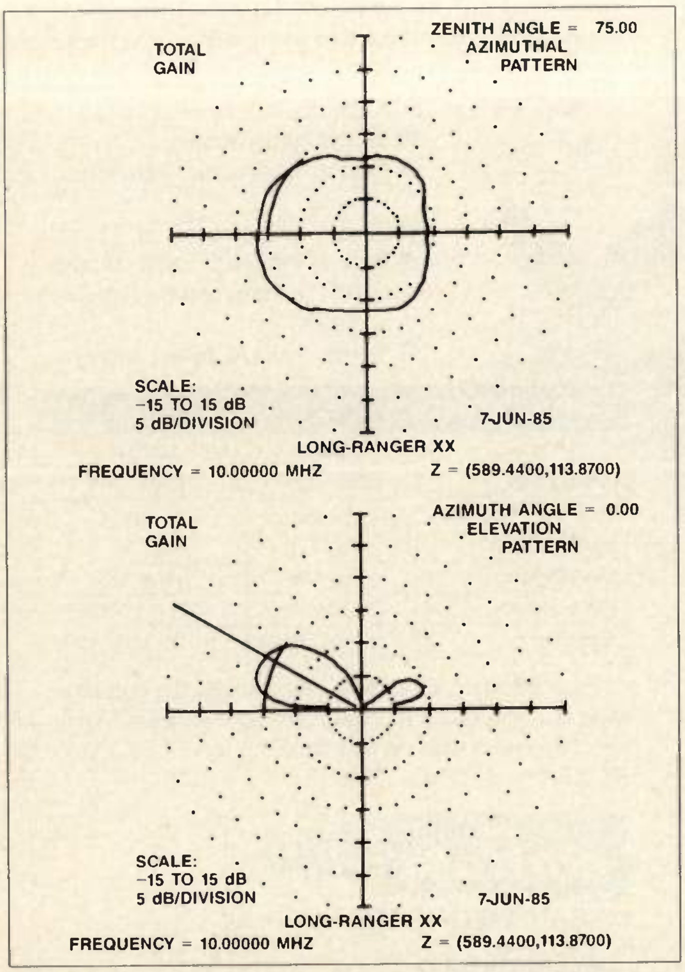


Figure 3. Performance characteristics at 10MHz.

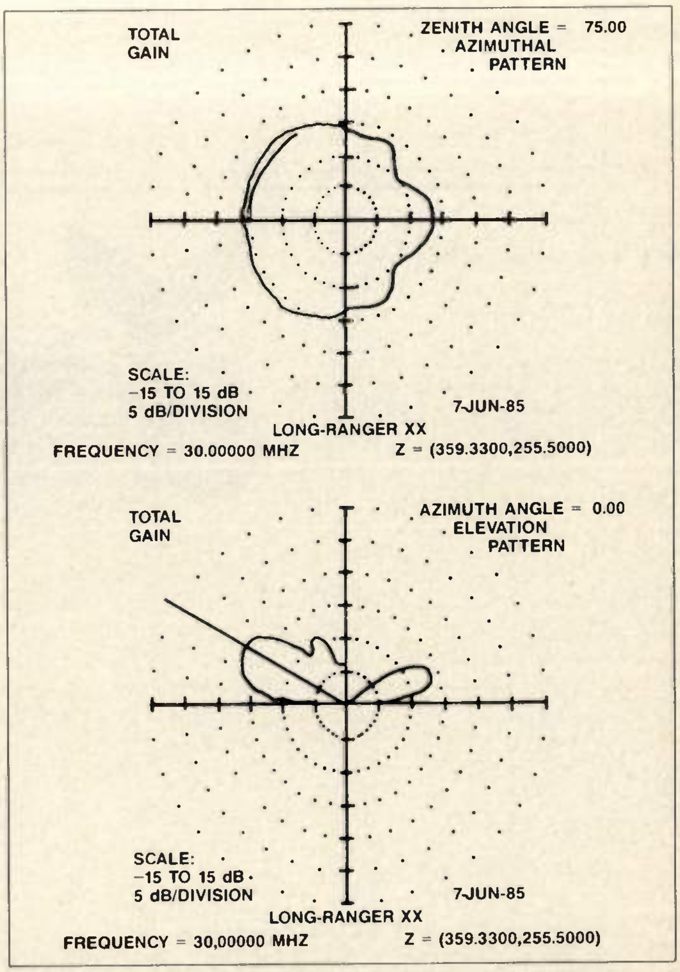


Figure 4. Performance characteristics at 30MHz.

Engineering Considerations for Selection of Analog ASICs

By Carlos Garcia
Harris Semiconductor

To ASIC or not to ASIC? Developing high frequency analog circuits has traditionally been a task left to a handful of experts. The parametric performance of these circuits are often dependent not only on the capability of the components used in the design, but on the interaction with the parasitic impedances encountered in a board level implementation. Performance tradeoffs and optimizations can hopefully be made without costly recycles. The required level of detailed information and predictability of the design components has, in the past, been a barrier to using analog ASICs for high frequency design solutions.

Semiconductor processes which boasted excellent analog performance were jewels to be guarded by IC vendors since product/process life cycles could extend beyond a decade. While this attitude still persists, some analog IC suppliers are adopting a new view. The supplier of the future will understand the necessity to keep pace with the system vendor's fast-changing product requirements. In the area of high frequency analog IC design this means providing the ASIC customer access to process, design, package, and test technology via a CAD framework that encapsulates all of the vendor's knowledge.

Digital ASIC Development

Of course, high frequency analog is not the first design discipline addressed through ASIC solutions. A comparison to the evolution of digital ASIC tools is instructive in that it suggests the development of a different set of fundamental capabilities prior to market acceptance.

The evolution of digital ASIC tools leveraged the fact that the circuit performance could be modeled at the functional level and that the fundamental technology migration was based on advances in process scaling. Circuit simulations were performed during cell design to investigate transient behavior and load sensitivity. However, the designs were relatively tolerant to process variations. Once a library of circuit functions was developed, the push was toward higher levels of abstraction to deal with higher levels of integration and functionality. Today, digital ASIC tools will synthesize a design from a textual description of the desired performance. As digital process technology evolved toward smaller feature sizes and higher levels of integration, libraries required new characterizations to capture changes in speed and drive capability — but the fundamental circuit designs did not change.

The development of ASIC tools for high frequency analog design presents a significantly different set of challenges. While functional levels of simulation (macromodel or behavioral) are useful for investigating system level tradeoffs, they do not even begin to address the level of parametric interaction characteristic of most analog designs. To understand the manufacturability of an analog design, the engineer must understand the second order behavior of the circuit and its sensitivity to load, environmental and process variations. Also, advances in analog technologies cannot be characterized as a reduction in feature size. Improvements in a bipolar device structure are sometimes radical and require an appreciation of the inevitable modeling limitations. This, combined with the varying availability of specific sheet resistivities and specific capacitances, make it relatively difficult to maintain a given schematic when migrating to the next generation technology.

The status of current analog ASIC tools depends on the level of performance one is trying to achieve as measured by operating bandwidth. There are some automatic layout tools for circuits of low to moderate operating frequencies that exploit a regular and structured circuit topology (switched capacitor filters and A/D converter compilers). However, higher frequency designs are typically handled at the device level. While vendors of high frequency analog ASICs may offer a transistor level or a pre-diffused tile array approach, they will almost inevitably stress the accuracy of their verification tools. This goes beyond their transistor models and circuit simulator and may include statistical analysis, optimization, layout to schematic verification, extraction of layout parasitics, and package modeling. The focus is on providing the ability to predict the performance of his design given variations in process and external conditions.

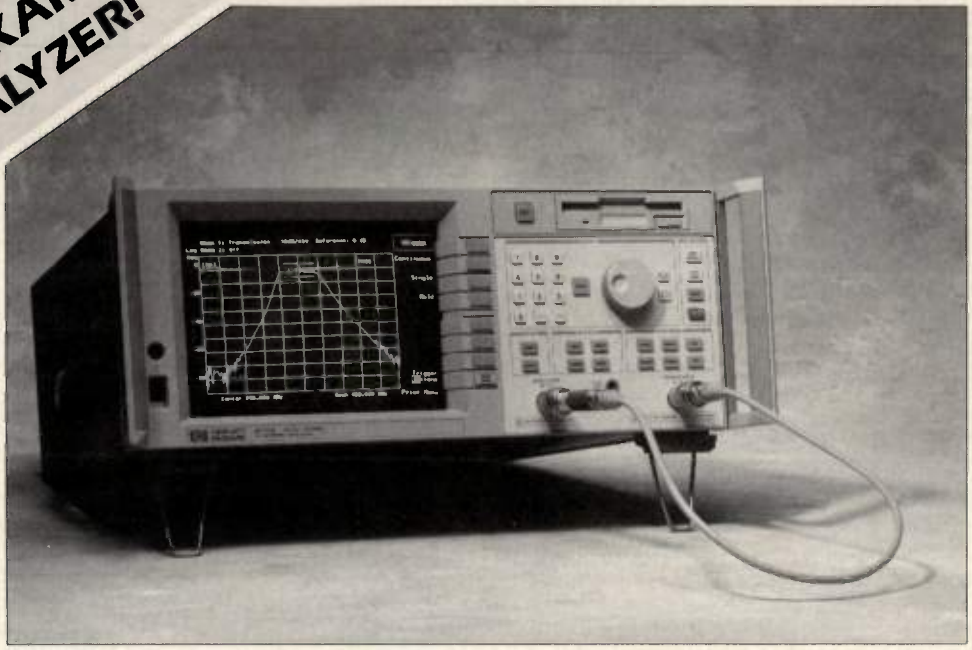
Key Considerations

Performance compromises —The analog customer is understandably hesitant in his decision to choose an ASIC solution. At the system level, high frequency analog solutions are often developed with discrete components. A designer is often willing to accept increased board space and layout parasitics for the benefit of being able to fully verify the circuit's performance in the lab without spending a lot of money. This is a considerable advantage when one considers the parametric sensitivities of analog circuits. But using a laboratory as a development platform has many disadvantages. Debugging breadboards can be a very time consuming activity. Understanding the interaction of one's circuit with a given board layout is essential to a manufacturable design. And then there is the task of optimizing circuit performance given the variability of the various component elements. All of these tasks are certainly achievable when designing with discrete components — if sufficient time is available.

Abandoning the lab completely may also have its disadvantages. Simulating circuit performance is an excellent way to explore parametric circuit sensitivities and many other "what if" questions. The designer must, however, have a thorough understanding of the strengths and weaknesses of the models in use. While models for many levels of abstrac-

The Circuit Design Contest
Grand Prize:

A HEWLETT-PACKARD NETWORK ANALYZER!

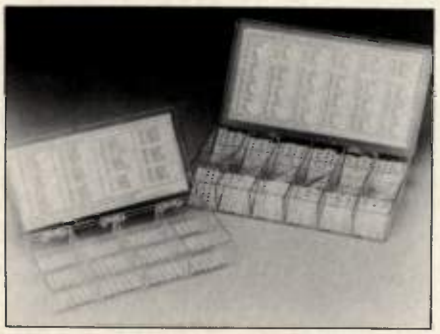


DEADLINE FOR ENTRIES:
POSTMARKED BY MARCH 20, 1992 —
RECEIVED BY MARCH 27, 1991

The Circuit Design Contest Grand Prize is a HP 8711A Network Analyzer from Hewlett-Packard! This analyzer provides insertion loss, gain, power return loss and SWR measurements from 300 kHz to 1300 MHz with 1 Hz resolution and 90 dB narrowband dynamic range, 66 dB broadband. A 50 ms full band sweep means fast measurements, and the built-in reflection test set has 40 dB directivity and 20 dB port match. Internal computing power offers complete marker options (eight of them), direct printer and plotter control, and stored measurement routines. Provided by Hewlett-Packard, Network Measurements Division.

25 Runner-Up Prize Packages!

(selected from both categories)



Communications Specialists, Inc. is providing a chip resistor and a chip capacitor design kit for each runner-up winner. Resistor kit CR-1 contains 1540 pieces, including every 5% standard value from 10 ohms to 10 megohms, plus extra parts in common values. Chip capacitors in the CC-1 kit cover every 10% value from 1 pF to .33 μF, in 0805 and 1206 sizes. These kits are essential for design and repair of SMT circuits.

Coilcraft is providing each winner with Designer's Kits selected from 7 and 10 mm tuneable coils, SMT inductors, fixed inductors, RF chokes and EMI filters. Values from a few nanohenries to over 1000 microhenries are included in these kits. Don't waste time waiting for samples or winding your own coils! These kits make RF prototyping easy.

Signetics Company awards each runner-up with a Demo board for the NE605 FM IF device — with mixer, oscillator, limiting amplifier, RSSI output, quad detector. Includes samples, complete technical data, and the 1992 Signetics RF Communications Handbook. Learn how to use this advanced receiver integrated circuit and experiment with different frequencies and features.

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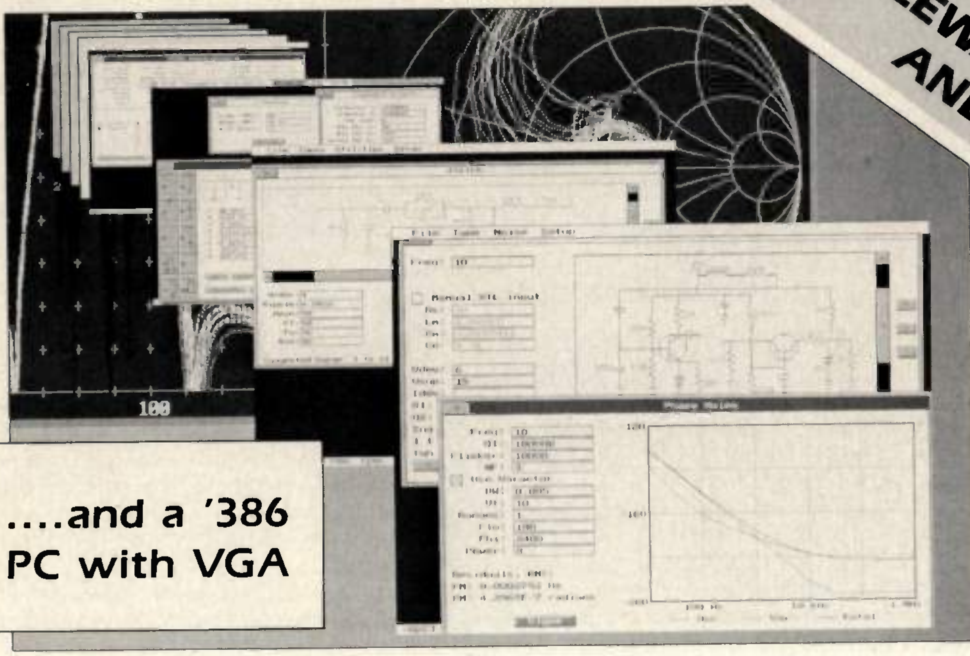
EAGLEWARE RF SOFTWARE AND A '386 PC!



....and a '386 PC with VGA

Send entries to:
RF Design Awards Contest
RF Design magazine
6300 S. Syracuse Way, Suite 650
Englewood, CO 80111

The PC Software Contest Grand Prize begins with a complete set of RF design software from Eagleware, including: =SuperStar= circuit simulator with optimization; the new =MATCH= active or passive matching program; =FILTER= synthesis package for filters and equalizers; =OSCILLATOR= for synthesis of L-C, SAW, crystal and T-line oscillators; and the =TLINE= physical and electrical parameter calculation program.

PLUS — A complete '386 computer system, with math coprocessor, 80 Mbyte hard drive, VGA graphics card, VGA monitor and mouse. System set-up and software installation is included. All this provided by Eagleware.

I. The DESIGN Contest Rules

1) Entries shall be circuits with an RF function, operating in the below-3 GHz frequency range.

2) Circuits entered shall have a complexity equivalent to that of a circuit using 8-10 discrete active devices, or 6-8 integrated circuits. The entry can be a portion of a larger system. This rule is intended to make judging equitable by maintaining a degree of similarity among entries.

3) Entries which emphasize design methods should include an example circuit. Entries demonstrating a test method should include a description of the device or system under test.

4) The entries shall be the original work of the entrant, not previously published. If developed as part of the entrant's employment, entries must have the employer's approval for submission.

5) A maximum of two entries per person is permitted. An entry may have two or more co-authors.

6) Submission of an entry implies permission for publication by *RF Design*. All prize-winning entries will be published, plus additional entries of merit.

7) Winners are responsible for any taxes, duties, or other assessments which result from the receipt of their prizes.

8) Entries must be postmarked by March 20, 1992 and received no later than March 27, 1992.

9) All entries will remain confidential until the publication of the July 1992 issue of *RF Design*.

II. The PC SOFTWARE Contest Rules

1) Each entry shall be a computer program which assists in the design, test, or control of RF circuits.

2) Programs must operate on computers compatible with MS-DOS/PC-DOS or Apple Macintosh operating systems. Any special hardware requirements should be noted (i.e., memory, graphics).

3) Programs should be provided in a form that can be run without special support software. For example, programs written in languages other than GWBASIC/BASICA should be provided in compiled, directly executable form. Programs operating within spreadsheets or mathematics packages cannot be accepted until they are capable of operating stand-alone.

4) Entries must be submitted on disk, along with supporting documentation on theory of operation, references, and operating instructions, and source code. Supporting material must be supplied in printed form.

5) The entries shall be the original work of the entrant, not previously published or distributed (including public access BBS or shareware). If developed as part of the entrant's employment, entries must have the employer's approval for submission.

6) A maximum of two entries per person is permitted. An entry may have two or more co-authors.

7) Submission of an entry implies permission for publication by *RF Design* and distribution by the RF Design Software Service. All prize-winning entries will be published, plus additional entries of merit. Some restrictions on publication and distribution of source code may be acceptable.

8) Winners are responsible for any taxes, duties, or other assessments which result from the receipt of their prizes.

9) Entries must be postmarked by March 20, 1992 and received no later than March 27, 1992.

10) All entries will remain confidential until the publication of the July 1992 issue of *RF Design*.

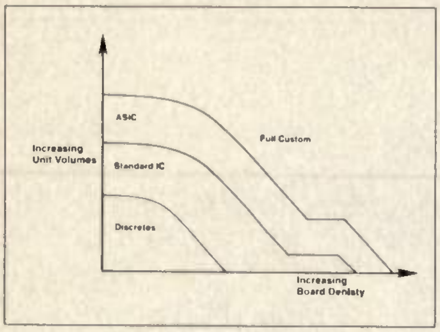


Figure 1. The relative system cost as a function of unit volume and board density requirements.

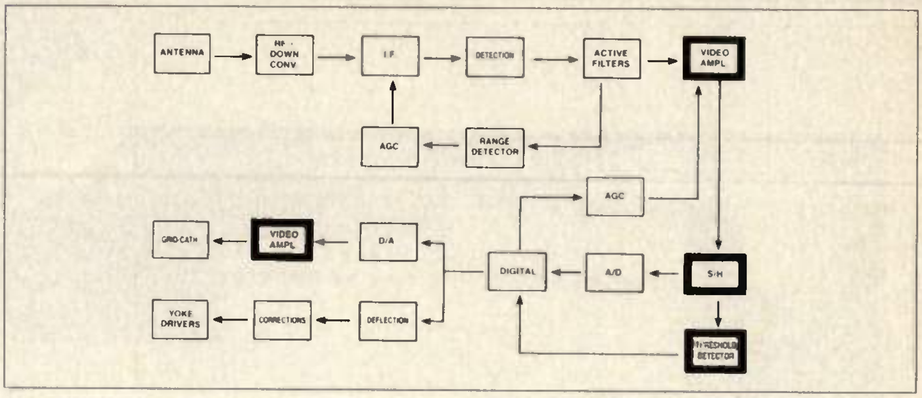


Figure 2. High speed ASIC opportunities in radar subsystem.

tion are available, the designer must always carefully question the right models. Transistor models, generally considered the most accurate, have their limitations as well. These models are usually designed to imitate reality over a constrained set of conditions. It is always important to be familiar with those conditions.

Acceptable limits/parameters and manufacturability — The issue to be dealt with then has to do with understanding the end system requirements and mapping them into a set of requirements to be met by the ASIC vendor. Working at a fairly high level of abstraction, the designer and the IC vendor work through the various detailed specifications and interface constraints. If the level of integration is high, it may be advisable to consider a solution which calls for multiple die. This could be necessary to avoid power dissipation limits for the chosen package or it could be motivated by isolation requirements between sections of the design (i.e. crosstalk, substrate noise, etc). If the process technology is marginal for the design requirements, this discussion will highlight the specifications of interest. This in turn will key the designer to make sure that the appropriate models, data and analysis tools are available. If they are not, and an array is available, the designer may wish to run some "quick turn" experiments to verify the capability of the process. Whatever the resulting actions, the vendor and designer should understand each other's expectations. Time devoted to this phase of interaction has enormous payback since it addresses manufacturability and process capabilities early in the product development.

Time to market — The time required to bring a new product to market is an important figure of merit for any company in a competitive environment. ASIC vendors may offer a variety of design methodologies which usually translate into differences in design and/or fabrication times. An analog array which requires two to four masking levels of personalization may take just a few weeks to process. Conversely, a full custom design might require two to three times as long to process. There are similar differences in design time at the transistor level versus design time when working with predefined macrocells. It is important to note, however, that minimizing the time to market involves more than simply shopping for the ASIC vendor with the shortest wafer fabrication cycle times. Minimum time to market is best achieved by finding an ASIC vendor who is willing to act like a partner in the development process. This implies a sharing of risk and rewards. Matching the ASIC customer's system level expertise with the semiconductor expertise of the ASIC vendor usually results in quicker time to market and new product success.

Resources — The issue of cost considerations involves at least two factors. First, is the issue of replacement, or alternative cost. There are certainly cases when the designer will not be able to find an ASIC solution which can compete with the total solution cost of the discrete implementation. However, the solution cost of a discrete implementation includes more than just component costs. Board space, reliability, and assembly costs all factor into the cost equation. The second consideration is non-recurring engineering cost (NRE). The designer must consider the payback period for the ASIC investment, which can run from tens to hundreds of thousands of dollars in NRE costs. But beware of making any of these decisions without taking a hard look at the partitioning of the design. Increasing the level of integration and properly clustering circuit functions to take full advantage of an IC technology can help overcome some of these issues. In general, as system unit volumes increase, simultaneous increases in board density requirements will favor the cost of semi-custom and full custom solutions.

An often overlooked resource issue is test development activity. If the ASIC fits the form and function of circuits with which the vendor has experience this may not be an issue. If, however, new test techniques are required, it is extremely important to begin test development in parallel with the circuit. Failure to do so will add weeks and maybe months to the development. To avoid this, the ASIC customer should provide a comprehensive list of tests and conditions adequate enough to assure system compliance and vendor compatibility with the test technology.

Expertise — When considering an analog ASIC solution it is also important to match the IC design expertise of the customer to the design system capabilities of the vendor. While physical design verification is a must for all vendors, electrical design tools are the item that can bridge the gap between system and IC design expertise. Harris Semiconductor has paid special attention to this aspect of its design tools. Simulation tools that provide advice on transistor sizing help the designer avoid mistakes that could result in poor frequency response or transistor saturation. Menus are designed to provide guidance in the proper sequence of design activities. Transistor models are geometry dependent and are supported with a statistical database to give the designer the confidence and freedom to optimize each transistor if he or she chooses to do so. And, to close the loop, the ability to extract layout parasitics for resimulation is also provided.

The Risk Evaluation Process

ASIC versus discrete — When considering an ASIC solution as part of the overall system design it is helpful to model the relative system cost as a function of unit volume and board density requirements (Figure 1). All other factors being equal, a model of this nature can define the component design methodology that will lead to minimum system unit cost. Given this model, evaluate the relative risks for a given design when all other factors are in fact not equal. Assume that the task at hand is the design of signal processing electronics for a radar subsystem (Figure 2). The focus will be on blocks of the subsystem capable of manipulating signals in the 30 MHz to 50 MHz range. Depending on the performance levels specified at these frequencies, this could imply a 3 dB bandwidth of >300 MHz. While the details of such a design are certainly beyond the scope of this article, consider the thought process involved in choosing the method of implementation for those parts of the subsystem which provide linear amplification and signal conditioning.

From the block diagram level, the system designer should be able to specify the critical parameters for each component. This should include parameters relating to interface constraints between components (common mode range, output voltage/current capability, load capacitance, data format, etc.). By combining this information with the subsystem's interface requirements, the designer can make a first pass at a partitioning strategy. In this example we will assume that part of the strategy is to combine four linear signal processing blocks that are defined by their specifications for gain flatness, gain compression, acquisition time, and propagation delay. The implementation of this design using discrete components would be feasible. The active and passive components would be readily available from stock, while performance could be verified in the lab. However, as mentioned before, trial and error techniques in the lab are not very efficient. The distribution of the component values would be statistically independent. This could become a cost problem if the match requirements force the use of precision elements.

Also, from Figure 1, the design would be economically marginal for moderate unit volumes and board density requirements. A discrete implementation will maximize the number of leads and board level connections and proportionally lower the reliability of the end product. This reliability concern also translates to a performance concern since the parameters of interest are strongly influenced by parasitics at critical nodes. Parasitic capacitance and inductance due to routing traces and package leads can alter the frequency response of the design. For designs which contain multiple independent circuit blocks, crosstalk or signal isolation may also be limited by these parasitic elements.

Performance levels may be achieved in both discrete and IC technologies but the IC technology has the advantage of reduced parasitic circuit elements. This translates into equivalent performance at reduced levels of power dissipation. Reduced power dissipation has several design-related advantages. Electromigration rules relate interconnect width to operating current. A reduction in power dissipation therefore has the effect of further reducing the parasitic capacitance in a given design. Reduced current levels allow for smaller transistor geometries which result in reduced small signal resistance and capacitance associated with the device. If the active devices in the discrete and IC technologies have similar bandwidths, these advantages result in a valuable performance tradeoff. The designer can match the performance of the discrete solution with lower power dissipation or match the power dissipation and enhance the performance. In any case the MHz/mA figure of merit is improved with the IC technology.

ASIC versus standard IC — When compared to an ASIC, performance differences relative to a standard IC are a bit more subtle; assuming the two were manufactured on a common semiconductor technology. Once again, the emphasis is on understanding the requirements of the potential ASIC product as defined by the system level specification. Performance differences in this case will typically be due to one of two reasons. First, a standard product is typically designed to service a wide range of applications. Performance tradeoffs which make sense for a standard product may be unacceptable for this radar subsystem. An example of this would be a relaxation in the gain flatness specification to enhance the circuits ability to drive large capacitive loads. Often the tradeoff difference can be more radical. Since the circuit functions being considered for integration are buried in a subsystem with well defined input and load conditions, the ASIC designer may not have to burden the design with circuitry intended to protect against generalized fault conditions. This will often make the ASIC implementation of a given circuit function more efficient with respect to silicon die size.

The second issue is one of functionality. If the four signal conditioning blocks to be integrated are two video amplifiers, a sample/hold amplifier, and a comparator, it would be difficult to find a standard product with the appropriate functionality. If functional integration is the only issue, then the economics of the design become the driving factor. If the volumes are low and the board density requirements are moderate, the savings due to board space may not warrant the NRE expenditure associated with ASIC products. The reliability differences due to the use of four IC packages versus one with approximately the same number of pins is negligible. This would obviously change as the level of ASIC integration increased. Finally, from a schedule point of view, use of a standard product IC does have the advantage of eliminating one level of detailed design and therefore has the potential of reducing overall design time.

ASIC versus full custom — The comparison of high speed analog ASIC solutions to full custom requires a bit more definition of what exactly is meant by ASIC. As mentioned earlier in this article, the current status of analog ASIC tools varies with the capabilities of the foundry process and the frequency response requirements of the end product. For products that require hundreds of megahertz of bandwidth, ASIC vendors may perhaps offer three levels of interaction. The analog array, with its two to four levels of customizing, may also be offered with predefined interconnect patterns or tiles which form circuit functions designed by the vendor. Predefined macrocells or "hard coded" macrocells is another option that may be offered by a vendor if the customer wishes to customize all masking levels of the foundry process to take advantage of the performance and layout efficiency of these vendor designs. Third, the ASIC vendor may offer the customer the option to perform a full custom design and layout. This third option gives the customer as much design freedom as in the discrete case but with the added ability of optimizing transistor sizes for the chosen application. The performance benefits gained by having access to all levels of the foundry process is sometimes necessary. In the case of the radar subsystem the performance of the amplifier, sample/hold, and comparator functions may require specific transistor geometry designs. This is common when the design is required to meet simultaneous objectives in speed (small geometry for low capacitance) and dynamic range (large geometries for low overhead voltages). Another example of the benefit of transistor level design is the ability to optimize for noise performance by scaling the device for minimum base resistance. Contrast this form of full custom versus the vendor designed full custom which will undoubtedly carry a higher price tag.

The choice to proceed with a full custom implementation for performance optimization carries the burden of the highest cost and longest development time. Note that the design time may be less or equal to that incurred in the discrete case but the processing time through the foundry will be on the order of two to three months. This burden, however, can be overcome if the system volumes allow the customer to exploit the silicon area efficiency of the full custom approach.

Deciding to go ASIC — So what to do? The production volume for the radar subsystem is expected to be high enough to warrant the development charges for an ASIC. Additional cost savings are to be expected due to smaller and simpler circuit boards, fewer components to purchase and inventory, fewer ICs to insert in boards, and a reduced frequency of field repair. Armed with an understanding of the critical parameters for each functional block as defined by the system requirements, we are prepared to follow through with the integration of two video amplifiers, a sample/hold amplifier, and a high speed comparator.

The gain flatness specification of the video amplifiers forces the bandwidth performance out to 300 MHz and so we expect the minimum requirement for transistor f_t to be about 3 GHz. This is expected to be sufficient for the other circuit functions. A zero time constant analysis will help estimate propagation delay sensitivities to transistor performance. The A/D converter which acts as a load to the sample/hold amplifier (Figure 2) is known to be highly capacitive. This load condition and the desire to maintain the gain peaking characteristics of the video amplifiers to a minimum emphasize the need for small signal transistor modeling accuracy. A listing of the passive element requirements (resistor values and temperature coefficients, capacitor requirements for the sample/hold, etc.) completes the first pass at defining the process and modeling requirements.

The concern over the small signal modeling accuracy and potential dependence on transistor sizing might force the designer into a full custom design methodology. At this point, however, the best action would be to consider a tile array approach to investigate whether the transistor geometry options are adequate and to make some initial estimates of the routing parasitics. The critical accomplishment is to know the design constraints and sensitivities and use these as the standard against which an ASIC vendor will be selected. ***RF***

About the Author

Carlos Garcia is director of engineering for signal processing products at Harris Semiconductor. He received his BSEE from University of Florida and his MBA from the Florida Institute of Technology and has been with Harris since 1979. He may be reached at (407) 724-3548.

High Frequency Device Models

Hewlett-Packard has introduced a high-frequency modeling system that produces accurate nonlinear device models that can be transferred directly to the HP microwave-design system and other circuit simulators. The system provides measurement accuracy and parameter extraction capability for GaAs FETs and BJTs. The HP 85190A system includes the HP 85191A HP Root Model, HP 85192A high-frequency FET models and HP 85193A high-frequency BJT models.

Hewlett-Packard Company
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An updated SPICE Library diskette is available from Analog Devices. The disk contains 88 new models, offering instrumentation amplifiers, voltage references, and matched transistor pairs in addition to operational amplifier models. The disk also includes an analog multiplier model which characterizes the AD734 wideband four-quadrant multiplier IC. The 5-1/4 diskette for IBM PC-compatibles is available for no charge.

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Microsoft Excel-Based Worksheets

A catalog of low cost, Microsoft Excel-based worksheets, macros and charts for RF design engineers is now available from Engineering Solutions. Applications include spectrum analysis, filter performance, phase locked loop and communication system design. Microsoft Excel version 2.X and up is required.

Engineering Solutions
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Matching Network Program

=MATCH=, a matching network synthesis program for IBM and compatible PCs is available from Eagleware Corporation. The program offers a range of matching synthesis techniques from simple narrowband through broadband Chebyshev solutions. Both the source and load may be specified as real or complex and each matching network type and order is independently selected. The approach is unique in its ability to deal with non-unilateral devices. The program requires DOS 3.0 or higher, 640K of RAM and a hard drive. Price is $895, or $595 if used with the =SuperStar= simulator program.

Eagleware Corporation
INFO/CARD #189

Linear Circuit Models

A new data manual and macromodels on disk are available from Texas Instruments. The manual contains almost the entire line of op amps, voltage comparators and building blocks. All of the macromodels are offered in voltage levels to match device data sheet characterizations. In addition, both Level I and Level II macromodels are available this year on two disks.

Texas Instruments
INFO/CARD #188

Graphical X Window Interface

Dynet-X is an interactive graphical X Window interface and analysis tool for enhancing Fortran applications. It can be used to enhance existing Fortran programs by making only minor modifications to the code and also with new programs. Some features include: visual representations of Fortran applications, interactive parameter modification, unit conversions, time-history display of multiple program executions and run-time observation of program parameters.

Dynetics, Inc.
INFO/CARD #187

RF literature

Superconductivity Literature

Keithley Instruments has released a superconductivity technical literature package. Some titles include: "Automating Resistance Measurements on High temperature Superconductors," "Automating Low Resistance Measurements," "New Measurement Methods," and outlines of measurement and test systems. A case study application from a superconductivity research facility and tips on practical applications are also included.

Keithley Instruments, Inc.
INFO/CARD #205

Application Guide

Kilovac has introduced a new product catalog and application guide. It contains 37 new products and includes technical information and application tips. Some of the subjects include: peak pulsed currents that can be passed through closed contacts, direct current power switching, remote power controllers for circuit protection, coil transient suppression, and high insulation resistance relays and reed relay replacements.

Kilovac Corporation
INFO/CARD #204

Transistor Short Form Catalog

A new RF and microwave components catalog from SGS-Thomson describes the company's silicon power transistor and MMIC amplifier product line. Complete product descriptions along with general performance data such as operating frequencies, power, gain, bias, pulse width, duty cycles and package styles are provided. Quality assurance and reliability procedures are also described.

SGS-Thomson
INFO/CARD #203

Mixer Products

A short form catalog from Miteq introduces their microwave mixers, modulators, and low-noise image rejection downconverters. Some special designs include broadest band converters, enhanced image rejection mixers and single sideband modulators, and lowest noise downconverters.

Miteq
INFO/CARD #202

RF and Microwave Components

A new 64-page catalog covering a line of components for microwave and RF applications is available from Murata-Erie North America. The catalog contains detailed specifications on crystal oscillators and filters, dielectric resonators, dielectric resonator-based oscillators and filters, duplexers, isolators, delay lines, LC filters, antennas and subminiature coaxial connectors. Electrical specifications, performance curves and mechanical specifications are provided.

Murata Erie North America
INFO/CARD #201

Data Converter Note

A six-page application note, "Data Converters: Getting to Know Dynamic Specifications," describes the dynamic specifications of data converters. This note reviews relevant A/D architectures, and goes into the dynamic, frequency domain specifications.

Datel, Inc.
INFO/CARD #200

DBS Tuner IC Data Sheet

A data sheet offering complete information on a 950-1750 MHz direct broadcast satellite tuner gallium arsenide integrated circuit is available from Anadigics. The data sheet details the features of the chip-on-chip oscillator, 8 dB noise figure, 9 dB conversion gain, single +5V supply, surface mount package, block diagram, maximum ratings and complete electrical specifications.

Anadigics, Inc.
INFO/CARD #199

Technical Publication

Linear Technology has released its second issue of *Linear Technology*, a technical publication. Notes and applications on the

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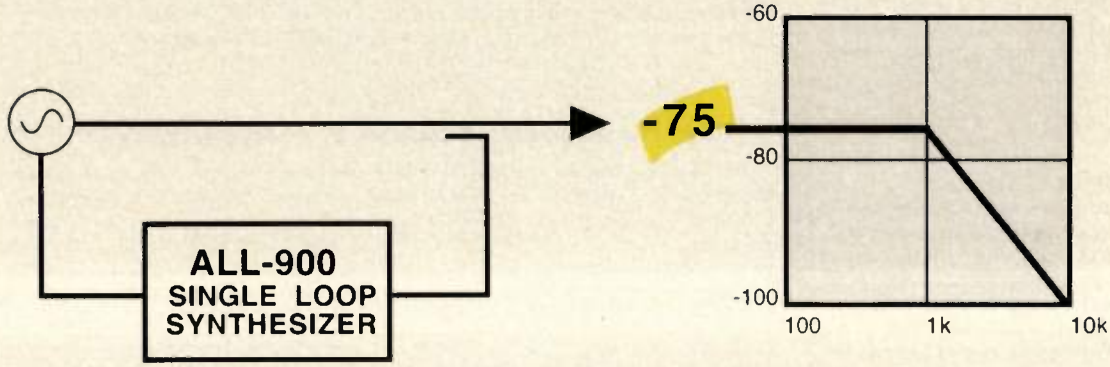

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company's operational amplifiers, including high speed devices and an ultra low-noise, ultra low-drift chopper stabilized op amp are included as well as a story on an A/D converter with on-chip sample and hold.
Linear Technology
INFO/CARD #198

Copper Foil Selection Guide

A two-page data sheet from Rogers is designed to help materials specifiers make the correct choice of copper foil substrates. Differences between electrodeposited and rolled annealed copper foil, including their manufacture, treatment, crystalline structure, and electrical and mechanical properties are described. A quick reference chart, performance characteristics and selection recommendations are also included.
Rogers Corporation
INFO/CARD #197

Interconnect Catalog

A 96-page catalog from Keystone Electronics features numerous new products plus their standard product lines for: printed circuit boards, batteries, interconnects, panels, computers and instruments. Detailed drawings, specifications, and applications data are provided for OEM designers and engineers.
Keystone Electronics Corporation
INFO/CARD #196

Signal Sources Catalog

Communication Techniques has published a new 100 page catalog providing product data and technical information on RF and microwave signal sources and synthesizers. Photographs, typical phase noise graphs and outline drawings are also provided. Application notes and technical articles discuss recent advances in phase locked signal sources and synthesizers.
Communication Techniques, Inc.
INFO/CARD #195

Time Delay and Pulse Instrumentation Catalog

An eight-page catalog of variable time delay instrumentation and broadband power dividers is available from Bishop Instruments. The catalog covers products such as picosecond and nanosecond delay lines and matched impedance low-power signal splitter/adders. It includes specifications and prices.
Bishop Instruments
INFO/CARD #194

Signal Processing Components Handbook

A new reference manual is now available from Mini-Circuits. The 718-page handbook includes articles, answers to questions, definitions of terms, selection guides, conversion charts, performance data specifications and performance curves.
Mini-Circuits
INFO/CARD #193

RF design

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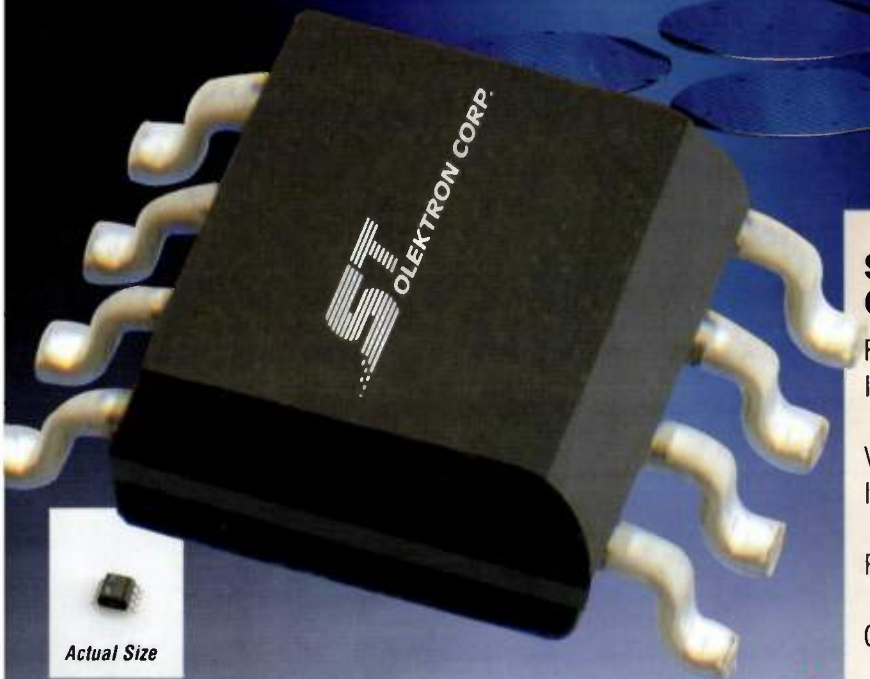

SM-IS-2103 GaAs SPDT Switch Guaranteed Specifications		
Frequency		DC-2000 MHz
Insertion Loss @ 100 MHz		0.7 dB Max
@ 1000 MHz		0.9 dB Max
VSWR		1.15:1 Max
Isolation @ 100 MHz		50 dB Min
@ 1000 MHz		30 dB Min
Rise/Fall Times (50% CTL or 90/10% RF)		2 nsec Typ
On/Off Times (50% CTL or 90/10% RF)		4 nsec Typ
Video Feedthrough (J1 input terminated @ 50 ohms)		20 mV Typ
Input Power for 1 dB Compression		+26 dBm Min
Control Voltages (V1, V2)	V low	-4.0 Vdc Max
	V high	+0.2 Vdc Max
Control Current		-5 Vdc @ 10μA
		-8 Vdc @ 100μA
Operating Temp.		-40 to +85°C
Package Type		8 Lead SOIC

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