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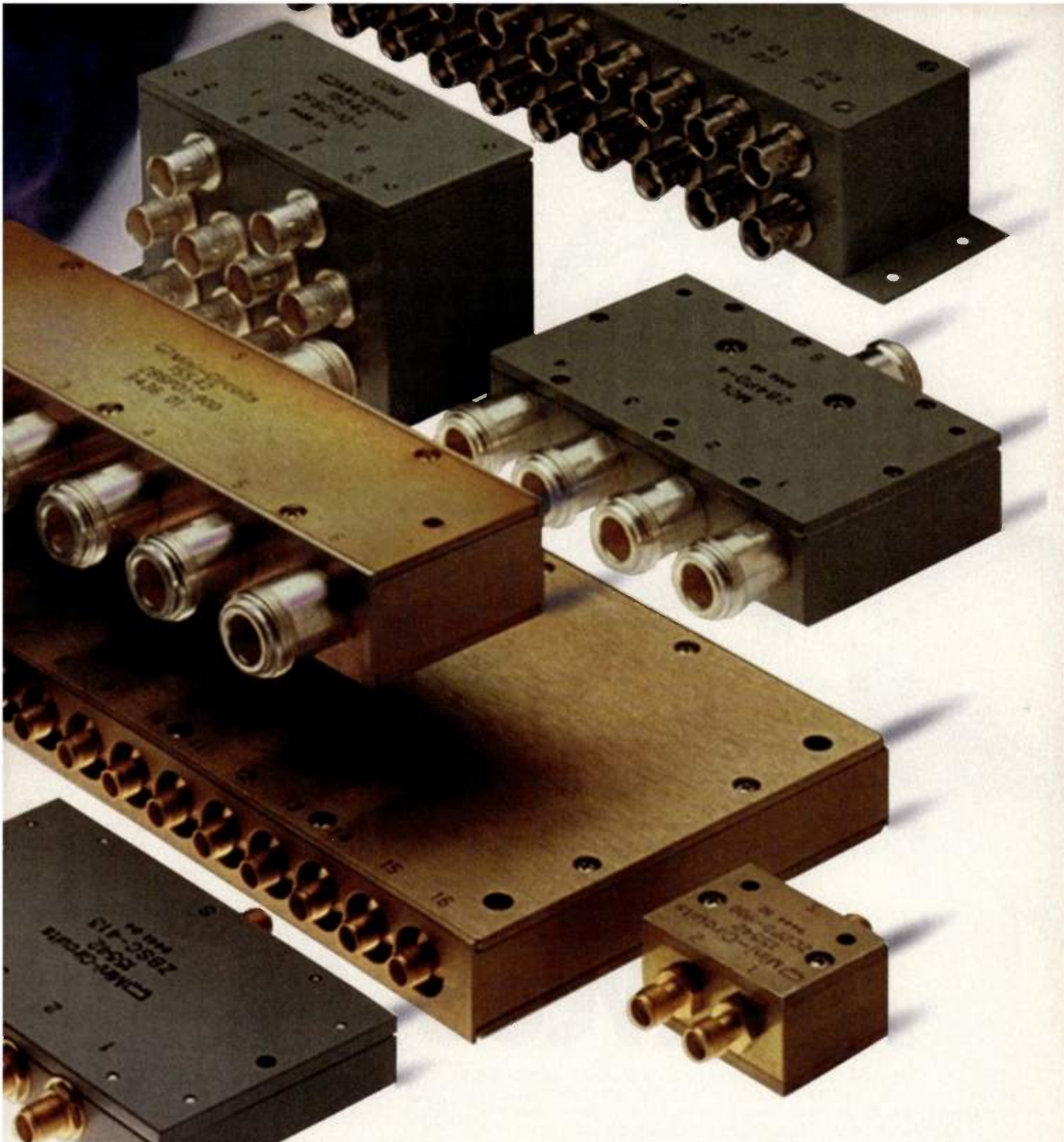

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	POS-50	25-50	-110	-19	20	11.95
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	POS-200	100-200	-102	-24	20	11.95
	POS-300	150-280	-100	-30	20	13.95
	POS-400	200-380	-98	-28	20	13.95
	POS-535	300-525	-93	-26	20	13.95
	POS-765	485-765	-85	-21	22	14.95
	POS-1025	685-1025	-84	-23	22	16.95
NEW	POS-1060	750-1060	-90	-11	30*	14.95
NEW	POS-1400	975-1400	-95	-11	30*	14.95
NEW	POS-2000	1370-2000	-95	-11	30*	14.95

*Max. Current (mA) @ 8V DC.
Notes: Tuning voltage 1 to 16V required to cover freq. range. 1 to 20V for POS-1060 to -2000. Models POS-50 to -1025 have 3dB modulation bandwidth, 100kHz typ. Models POS-1060 to -2000 have 3dB modulation bandwidth, 1MHz typ.
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RF design
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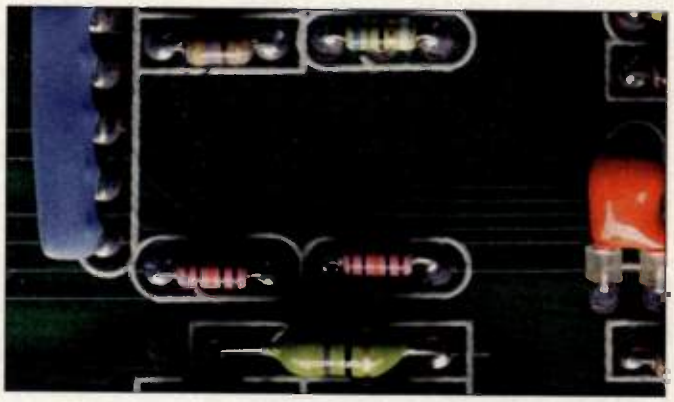
April 1997



cover story — p. 64

featured technology — DSP

departments

Coming in May

- Power amplifiers
- Tutorial: Phase-locked loops
- Cover story: Cellular

RF *editorial*

Growth areas for RF component production

By Don Bishop
Editorial Director

Telecommunications businesses that rely on RF components include paging, cellular, personal communications service (PCS), cordless, local loop, computer area-networks, direct broadcast satellite and geopositioning, to name a few. These businesses use high-technology products. They nearly define a portion of the technology industry, where success is linked so closely to consumer preference, and to price.

PCS is poised to grow dramatically, helping to increase RF semiconductor production. Demand for Ku-band satellite band receivers will grow, too. Telephones and televisions are among America's most popular consumer products. Wireless handsets and direct broadcast satellite offer two new ways to use phones and TVs that have captured the consumer's attention.

I've been tracking developments involving direct audio broadcasting, known as Satellite Digital Audio Radio Service, or S-DARS. Ugh. Who names these things? Audio radio? Is there another kind? Anyway, no one can deny that, along with telephones and televisions, radios have been enormously popular consumer products. I wonder, though, whether many people will buy S-DARS receivers. Maybe if the programming is compelling enough. The FCC scheduled an auction for April 1 to sell two licenses good for multiple channels. Products will follow.

Gallium arsenide (GaAs) technology will continue to benefit as applications move to higher frequencies and adopt linear systems.

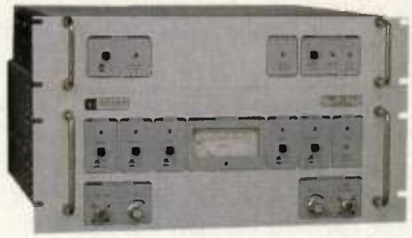
Wireless data is about to explode. It has been about to explode for the past 10 years. As everyone waits, wireless data grows slowly. Infrastructure is lacking. Cellular digital packet data (CDPD) sputters along. RF networks on commercial radio service and private radio service frequencies serve commercial customers with particular requirements. "Killer apps," they say. "Give us killer apps." (Translation: Consumer applications with broad appeal are lacking.) The application of reading business and residential electric and gas utility meters is growing fast.

Fragmentation of standards for wireless local loop is likely to continue. Maybe multiple standards won't have as much effect on individual local loop products as they have on wireless telephone handsets because houses don't move. As far as wireless phones are concerned, though, the fact that service providers use systems with multiple standards and frequency bands will lead to growth in the production of multiband or multistandard wireless handsets.

On the one hand, handset price is kept lower by limiting the flexibility to one analog standard and one digital standard on one band, but utility and consumer satisfaction are improved by including multiple standards and bands. Multistandard, multiband wireless handset manufacturing is for those with engineering innovation and marketing savvy.

This month, we welcome Roger Lesser as associate editor. Previously, Roger edited *Defense and Security Electronics*. Prior to his four years with *Defense and Security Electronics*, Roger spent 20 years in the U.S. Air Force, rising to the rank of lieutenant colonel. You can reach Roger in the Englewood, CO office. His email address is roger_lesser@intertec.com. At the same time, we say goodbye to Pat Werner, whom Roger replaces. Pat returns to freelance work and to writing novels. (She has published 16.) Thanks, Pat, for the fine work during the past year. **RF**

The Only Source For RF Amplifiers For...



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Components Branch

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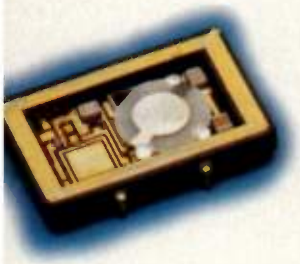

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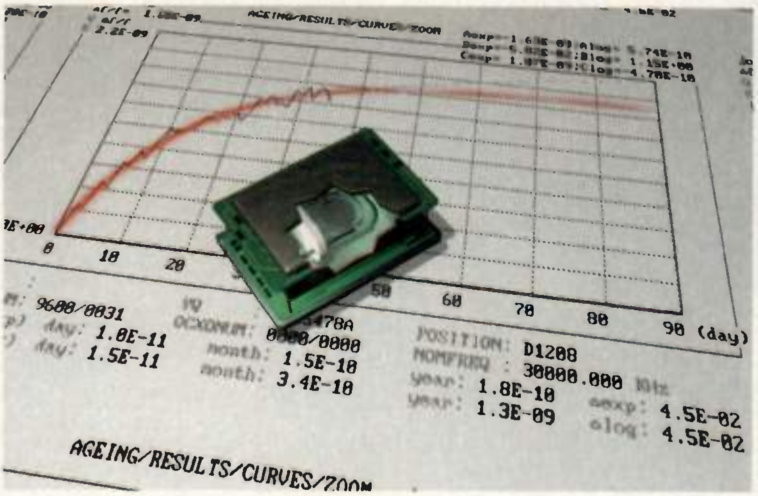

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2	TE5000	3	3.75	20	18.0	-	-	2	1.0	50	1800//+4
4	TE5010	3	3.75	30	14.0	-	-	3	2.0	60	1500//+3
6	TE5020	6	3.75	60	12.5	-	-	4	2.0	70	1500//+3
8	TE5030	6	3.75	60	10.0	90	12.5	5	2.0	80	1500//+3
2	TE5040	3	6.50	20	30.0	-	-	1	1.0	50	2700//0
4	TE5050	3	6.50	30	15.0	-	-	2	2.0	75	3100//0
6	TE5060	6	6.50	60	19.5	-	-	3	2.0	90	3100//0
8	TE5070	6	6.50	60	13.0	80	17.5	4	2.0	100	3100//0
2	TE5080	3	7.50	20	35.0	-	-	1	1.0	50	3000//0
4	TE5090	3	7.50	30	17.5	-	-	2	2.0	75	3300//0
6	TE5100	6	7.50	60	22.5	-	-	3	2.0	90	3300//0
8	TE5110	6	7.50	60	15.0	80	20.0	3	2.0	100	3300//0
2	TE5120	3	15.0	20	70.0	-	-	1	1.0	35	5000//-1
4	TE5130	3	15.0	30	35.0	-	-	2	2.0	60	5000//-1
6	TE5140	6	15.0	60	45.0	-	-	2	2.0	90	5000//-1
8	TE5150	6	15.0	60	30.0	80	40.0	3	2.0	100	5000//-1

21.4 MHz

NO. POLES	TEMEX P/N	PASSBAND dB	PASSBAND ±KHz	STOPBAND dB	STOPBAND ±KHz	STOPBAND dB	STOPBAND ±KHz	LOSS dB	RIPPLE dB-MAX	ULT. REJ. dB-MIN.	TERM. Ω/PF
2	TE5180	3	3.75	15	12.5	-	-	2	1.0	50	850//+6
4	TE5190	3	3.75	30	12.5	-	-	3	2.0	70	850//+5
6	TE5200	6	3.75	60	12.5	-	-	4	2.0	90	850//+5
8	TE5210	6	3.75	60	10.0	80	12.5	5	2.0	100	850//+5
2	TE5220	3	6.50	15	20.0	-	-	2	1.0	50	1300//+2
4	TE5230	3	6.50	30	22.5	-	-	3	2.0	70	1400//0
6	TE5240	6	6.50	60	22.5	-	-	4	2.0	90	1400//0
8	TE5250	6	6.50	60	17.5	80	22.5	4	2.0	100	1400//0
2	TE5260	3	7.50	15	25.0	-	-	2	1.0	50	1500//0
4	TE5270	3	7.50	30	25.0	-	-	3	2.0	70	1600//0
6	TE5280	6	7.50	60	25.0	-	-	4	2.0	90	1600//0
8	TE5290	6	7.50	60	20.0	80	25.0	4	2.0	100	1600//0
2	TE5300	3	15.0	15	50.0	-	-	2	1.0	45	3000//0
4	TE5310	3	15.0	30	45.0	-	-	3	2.0	60	3000//-1
6	TE5320	6	15.0	60	45.0	-	-	3	2.0	90	3000//-1
8	TE5330	6	15.0	60	33.0	80	45.0	4	2.0	100	3000//-1

45.0 MHz

NO. POLES	TEMEX P/N	MODE	PASSBAND dB	PASSBAND ±KHz	STOPBAND dB	STOPBAND ±KHz	LOSS dB	RIPPLE dB-MAX	ULT. REJ. dB-MIN.	TERM. Ω/PF
2	TE9420	3-OT	3	3.75	18	16.0	3	1	40	2000//-1.0
4	TE9310	3-OT	3	3.75	30	12.5	3	1	70	2000//-1.0
2	TE7420	3-OT	3	7.50	18	28.0	2	1	40	3000//-1.0
4	TE7430	3-OT	3	7.50	40	30.0	3	1	70	3000//-1.0
2	TE7440	3-OT	3	15.0	15	47.0	2	1	40	8000//-1.5
4	TE7450	3-OT	3	15.0	30	50.0	3	1	70	8000//-1.5
2	TE7730	FUND	3	15.0	15	50.0	2	1	40	1100//+1.5
4	TE7740	FUND	3	15.0	40	60.0	3	1	70	800//+1.0

70.0 MHz

NO. POLES	TEMEX P/N	MODE	PASSBAND dB	PASSBAND ±KHz	STOPBAND dB	STOPBAND ±KHz	STOPBAND dB	STOPBAND KHz	LOSS dB	RIPPLE dB-MAX	TERM. Ω/PF
2	TE10400	3-OT	3	7.5	18	30	35	-910	2	1	2000//-1
4	TE10410	3-OT	3	7.5	35	25	80	-910	3	1	2000//-1
2	TE10420	3-OT	3	10	15	30	35	-910	2	1	2500//-1
4	TE10430	3-OT	3	10	35	40	80	-910	3	1	2500//-1

90.0 MHz

NO. POLES	TEMEX P/N	MODE	PASSBAND dB	PASSBAND ±KHz	STOPBAND dB	STOPBAND ±KHz	STOPBAND dB	STOPBAND KHz	LOSS dB	RIPPLE dB-MAX	TERM. Ω/PF
2	TE10440	3-OT	3	7.5	18	30	35	-910	2	1	2000//-1
4	TE10450	3-OT	3	7.5	35	25	80	-910	3	1	2000//-1
2	TE10460	3-OT	3	10	15	30	35	-910	2	1	2500//-1
4	TE10470	3-OT	3	10	35	40	80	-910	3	1	2500//-1
4	TE10480	3-OT	3	15	30	50	80	-910	3	1	4000//-1

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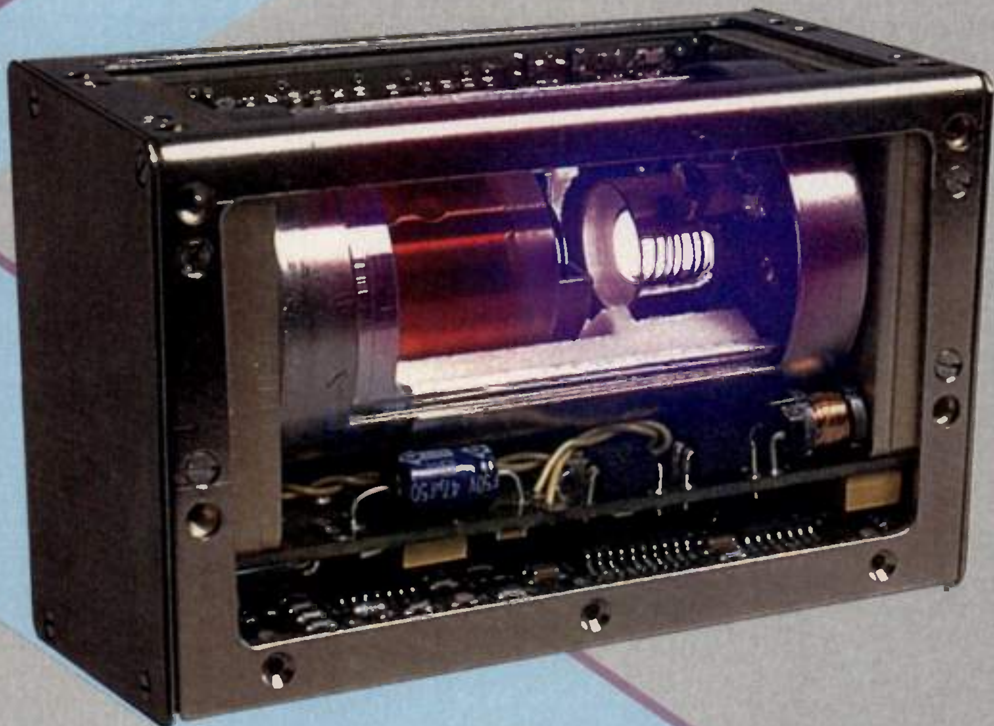

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RF letters

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Kudos for tutorials

Just a short note to tell you that I enjoy the RF tutorial articles and find them quite useful to clip and place in a notebook to answer questions from young engineers who are in my department. When I get questions, rather than launching into a long tutorial on my white board, I give them the pages I have placed in plastic sheet protectors and let them learn by reading an appropriate tutorial.

I particularly enjoyed the article on coaxial cables written by Jim Weir in the August 1996 issue. Jim does a good job of explaining things using anecdotes and simple explanations that don't lose the inexperienced reader. I have seen some of his posts to internet newsgroups and they had a similar flavor. I would like to see additional tutorials from Jim. He does a great job of explaining the basics to the RF novice. Even we "old timers" sometimes learn a thing or two in the process.

Paul J. Dobosz
Reynosa, Mexico

MTT includes HF and VHF

Microwave Theory and Techniques (MTT) has decided to emphasize its interests in the HF and VHF frequency ranges. Radio-frequency engineering involves frequencies as high as 1 GHz and includes not only transmitters and receivers for radio communication, but also RF heating (plasma), medical imaging (e.g., MRI), and RFID. This area is rapidly growing because of the expansion of "wireless" communication systems and devices.

An estimated 26,000+ RF engineers have to date lacked a focal point within IEEE. Related papers have been scattered through various IEEE and trade

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18 new Schottky-Barrier diodes

So many choices! What sounds good this morning? HP makes Schottky-barrier diodes for a wide variety of applications, such as DC-biased detectors, zero-bias detectors, mixers, clamping circuits and ultra-fast ESD protection.

12 new PIN diodes

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SOT-323 package is 40% smaller than standard SOT-23 or SOT-143

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journals. As a result, most RF engineers have not seen a great benefit in being IEEE members.

RF and microwave work use different components (e.g., MOSFETs rather than GaAsFETs), but many techniques (power amplifiers, low-noise receivers, couplers) are analogous. Equally or more important is the attitude that the application of theory has practical limits imposed by stray capacitance and lead inductances. The interests of microwave and RF engineering thus have much in common. Inclusion within MTT will provide a focal point with peer-reviewed publications with long-term availability. How the increased emphasis on HF and VHF is to be handled within MTT has yet to be determined. It is likely that many disciplines will fall within the scope of existing MTT technical committees. Others that are unique to HF-VHF may necessitate the formation of a new, permanent technical committee. An ad-hoc committee has been formed to look into these issues. Anyone interested in helping in this effort should contact me. Special sessions at MTTS '97 in Denver are planned.

Frederick H. Raab, Ph.D.
50 Vermont Ave., Fort Ethan Allen, Colchester, VT, 05446.
Tel. and fax 802-655-9670.

The problem with solutions

With regards to your recent comments on the terms "solutions" and "wireless," I agree wholeheartedly.

It is my opinion that solutions are usually present long before any "problems" exist. Often, solutions never even find problems. In that case, the products under the solution umbrella usually are taken off the market and the companies redirect their efforts towards other, more profitable, product lines. Had these organizations surveyed the market to determine existing needs before they started development of such products, they might not have gone through such futile exercises.

Having spent a few decades associated with commercial broadcasting, land mobile radio (a term I still frequently use) and various forms of RF design, I still can't get used to "wireless" communications. When I hear the term used, I can't help but hark back to the Marconi era (no, I'm not that old!) and think of the basic underpinnings of radio communications. I hope designers do not entertain visions of wideband spark gap technology in today's products!

I theorize that the recent upsurge in the use of these terms is probably the product of a younger wave of marketing people who desire to form their own unique vocabulary to woo customers and impress their peers. Many of them possibly never learned about true wireless history.

I'll give these terms a few more years in which to thrive. If, by that time, they fall into disuse, I will go on using the old terms I have been using for most of my life.

Gregory Muir
Boulder, CO

Stimulating discussions

As you invited, I am putting in my bid for more on [coaxial standards]. Discussions of this type of thing, whether they resolve the issues or not, make you think of the underlying fundamental principles. It is only through a good understanding of the basics that most new ideas develop.

Sometime in 1950, Einstein said that after 50 years of trying he was still no closer to understanding what a photon was. He added, "most people think they know what a photon is, but they are wrong."

Of course all the notions of "fields" and such devices frequently used in RF design are mere mathematical constructs, and although widely useful, can constrain creative thinking if one is allowed to fall into the trap of believing that the model represents reality.

For example, when you try to understand something as simple as how an antenna radiates (or receives), you will find field theory is a description of *how* it all happens, but is most unsatisfactory when it comes to the *why* questions. Why does an antenna have a radiation resistance, for example? What is resisting the electron motion? If you believe the quantum mechanical argument, it is *every* other electron in the universe. On the other hand, field theory permits an antenna to radiate without any outside references. Field theory permits us to obtain most practical designs more easily than quantum mechanics. These models thus have their limitations.

Quantum mechanical explanations of the fundamentals of RF are beginning to mature. This is an exciting era in history to be getting back to fundamentals, and I would like to see *RF Design* take up the challenge.

Neil J. Boucher
Australia

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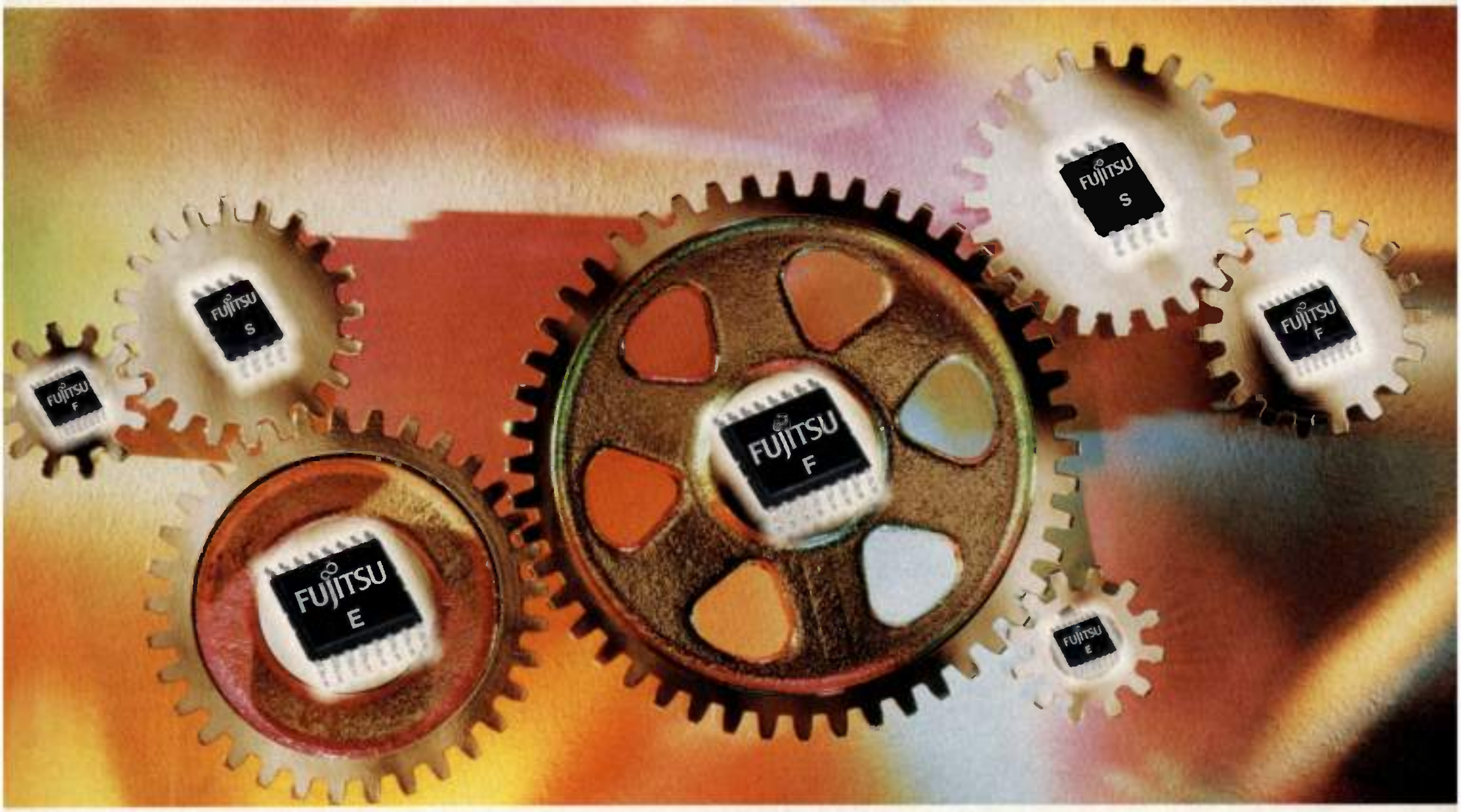

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COMPUTERS, COMMUNICATIONS, MICROELECTRONICS

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RF calendar

April 21–23 **RF Design Seminar Series**—*Las Vegas.* Information: Intertec Presentations, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111. Tel. 800-288-8606 or 303-220-0600; Fax 303-770-0253.

22–24 **International Wireless Communications Expo**—*Las Vegas.* Information: Intertec Presentations, 6300 S. Syracuse Way, Denver, CO 80111. Tel. 800-288-8606 or 303-220-0600; Fax 303-770-0253.
RF Pavilion—Manufacturers exhibits within IWCE. Components, test equipment, software and services for RF equipment manufacturing.

22–24 **Convergence Tech and IC Expo for microelectronics, communications and computer professionals**—*Dallas.* Information: Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045. Tel. 800-877-2668, ext. 243; Fax 310-641-5117.

23–26 **Broadcast Technology**—*Jakarta, Indonesia.* Information: Eileen Lavine, Information Services, 4733 Bethesda Ave., Suite 700, Bethesda MD 20814. Tel. 301-656-2942; Fax 301-656-3179.

May 5–7 **Vehicular Technology Conference for cellular and mobile wireless communications**—*Phoenix.* Information: Wendy Rochelle, Registrar, IEEE Conference Service, 455 Hoes Lane, P.O. Box 1331 Piscataway, NJ 08855-1331. email w.rochelle@ieee.org.

6–8 **Electronics Industries Forum of New England**—*Boston.* Information: Linda Hanson. Tel. 914-779-0696.

13–15 **ID Expo, bar code and automatic data capture trade show**—*Philadelphia.* Information: Advanstar Expositions. Tel. 800-331-5706 or 218-723-9130.

13–16 **Computer and Communication Electronics Design Exposition**—*Dallas.* Information: Reed Exhibition, 383 Main Ave., Norwalk, CT 06851. Tel. 800-840-5614.

28–30 **IEEE International Frequency Control Symposium**—*Orlando, FL.* Information: Wendy Ortega Henderson, National Institute of Standards and Technology. Tel. 303-497-3593; Fax 303-497-6461; email *ortegaw@boulder.nist.gov.*

June 1–5 **Supercomm**—*New Orleans.* Information: Telecommunications Industry Association. Tel. 202-326-7300.

9–14 **Asia Telecom**—*Singapore.* Information: Tom Dahl-Hansen, senior vice-president, Telecom. Tel. +41-22-730-5298; Fax +41-22-730-6444; email *dahl-hansen@itu.ch.*

10–12 **International Microwave Symposium and Exhibition**—*Denver.* Information: Horizon House. Tel. 617-769-9750.

11–13 **Virginia Tech Symposium on Wireless Personal Communications**—*Blacksburg, VA.* Information: Jenny Frank, Conference Coordinator, Virginia Polytechnic Institute, 840 University City Blvd., Pointe West

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Commons, Suite 1, Blacksburg, VA 24061-0350. Tel. 540-231-2958; Fax 540-231-2968; email jacklily@vtml.cc.vt.edu; Web site: *http://www.ee.vt. edu/mprg/ home.html.*

13 **Automatic RF Techniques Group**—*Denver.* Information: Roger B. Marks, Ph.D., Conference Chair, NIST, 325 Broadway, Boulder, CO 80303. Tel. 303-497-3037; Fax 303-497-7828; email *r.b.marks@ieee.org.* Web site *http://www.boulder.nist.gov/ ims/arftg.*

July 14–17 **Image Processing and Applications**—*Dublin.* Information: Sheila Griffiths, Conference Organizer, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, United Kingdom. Tel. +44 (0) 171-344-5475/72; Fax +44 (0) 171-240-8830; email *kmoorley@iee.org.uk.*

30-August 1 **Japanese Information in Science, Technology & Commerce**—*Washington DC.* Information: Japan Information Access Project, 2000 P Street, N.W. Suite 620, Washington D.C. 20002. Tel. 202-822-6040. email: access@nmjc.org

August 18–22 **IEEE EMC Symposium on Electromagnetic Compatibility**—*Austin, TX.* Information: John Osburn, Chairman, or Mark Prchlik, Exhibits. Tel. 512-835-4684; email *97.emc.symp@emctest.com.*

20–22 **Piezoelectric Devices Conference and Exhibition**—*Kansas City, MO.* Information: Pete Walsh, Electronic Industries Association. Tel. 703-907-7547; Fax 703-907-7501.

September 10-12 **RF Design '97 Conference & Expo**—*Santa Clara, CA.* Information: Intertec Presentations, 6300 S. Syracuse Way, Denver, CO 80111. Tel. 800-288-8606 or 303-220-0600; Fax 303-770-0253.

10–12 **RF Design Seminar Series**—*Santa Clara,* CA. Information: Intertec Presentations, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111. Tel. 800-288-8606 or 303-220-0600; Fax 303-770-0253.

14–17 **Signal Processing Applications & Technology and DSP World Expo**—*San Diego, CA..* Information: Denise Chan, Miller Freeman, 525 Market, Suite 500, San Francisco, CA 94105. Tel. 415-278-5231; email *dsp@exporeg.com.*

22–24 **Connector and Interconnection Technology Symposium and Trade Show**—*Anaheim, CA.* Information: EIA Components Group, 2500 Wilson Blvd., Arlington, VA 22201-3834. Tel. 703-907-7547.

25-26 **47th Annual Broadcast Symposium**—*Washington DC* Information: Gerald A. Berman, Administrator, IEEE Broadcast Technology Society, P.O. Box 2126, Rockville, MD 20847-212. Tel. 301-881-4310; email *gberman@cmpconsulting.com.*

RF courses

Arizona State University — *Wireless Digital Communications: Access, signaling and management aspects; mobile, cellular, voice and data networks*—April 28–May 2. Information: Professional Development, ASU, P.O. Box 877506, Tempe, AZ 85287-7506. Tel. 602-965-1740; Fax 602-965-8653.

Besser Associates & Microwave Online Services — *RF and Wireless Made Simple*—May 5–6, Los Altos, CA; May 12–13, Dallas; *RF Measurement Techniques*—May 5–8, Dallas; *Wireless RF System Design*—May 5–9, Dallas; *RF Component Modeling*—May 12–16, Dallas; *Applied RF Techniques I*—May 12–16, Los Altos, CA; *Applied RF Techniques II*—May 12–16, Dallas; *RF Productivity Improvement*—May 14–16, Dallas; May 19–22, Los Altos, CA; *EM Field Simulator Made Practical*—May 15–16, Los Altos, CA; *Nonlinear RF Circuit Design and Modeling with Spice*—May 19–20, Los Altos, CA; *Digital Signal Processing*—May 21–23, Los Altos, CA. Information: Annie Wong, Besser Associates, 4600 El Camino Real, Suite 210, Los Altos, CA 94022. Tel. 415-949-3300; Fax 415-949-4400. RF and Microwave courses are available on the World Wide Web exclusively through RF Globalnet. The courses will be given over a two-to-three week period. *Applied RF Techniques I: Linear Circuits.* Information: Larry Black, Microwave Online. Tel. 303-415-9233; email *larry@mosco.com*; Web site *http://www.rfmicrowave.com.*

Boulder Microwave Technologies — *Introduction to Printed Antenna Design Using Simulation*—June 7, Boulder, CO; *Design of Printed Antennas for Wireless, Mobile, and Space Applications*—July 10–12, Montreal. Information: Boulder Microwave Technologies, Tel. 303-451-9525; Fax 303-541-9609; email *bmtinfo@bmt.com*

California State University, Northridge — *Microwave Antenna Measurements: Far-Field, Near-Field, Compact Ranges; Anechoic Chamber: Design, use and evaluation of anechoic chambers, far-field, near-field and compact ranges; techniques for the determination of antenna radiation patterns, directivity, gain, polorization and impedance; phased array testing and alignment, radar cross-section measurements and radar imaging techniques*—June 3–6. Information: Shirley Lang, California State University, Northridge, 18111 Northridge, CA, 91330-8295. Tel. 818-677-2146; Fax 818-677-5982; email *shirley.lang@csun.edu*

CKC Laboratories — *EMC for Medical Electronics*—April 22–23; *Immunity to ESD*—May 12, Orange County, CA; *CE Mark Design and Compliance Routes*—May 13–14, Orange County, CA; *Core EMC Design*—June 17–18, Hillsboro, OR; . Information: Linda Grunow or Todd Robinson, CKC Laboratories, 5473-A Clouds Rest, Mariposa, CA 95338. Tel. 800-500-4362 or 209-966-5240; Fax 209-742-6133; email *lgrunow@ckc.com.*

Georgia Tech Continuing Education — *Advanced Electronic Warfare Principles*—March 25–28, Atlanta; *Radar Cross Section Reduction*—March 25–28, Atlanta. Information: Department of Continuing Education, Georgia Institute of Technology, Atlanta, GA 30332-0385. Tel. 404-894-2547; email *conted@gatech.* edu; Web site *http://www.conted.gatech.edu.*

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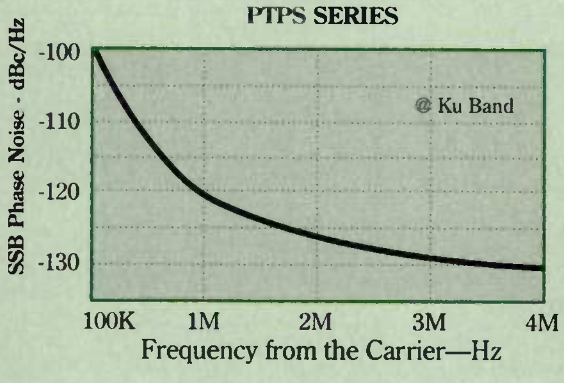

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for Portable Electronics Systems (three-days digital, plus three-days analog)—March 31–April 5; *RF IC Design for Wireless Communication Systems*–May 12–16; *Data Communication ICs*—May 14–16. Information: Mead Microelectronics, 7100 Grandview Drive, Corvallis, OR 97330. Tel. 541-758-0828; Fax 541-752-1405. In Europe, contact Mead Microelectronics, Venoge 7, 1025 St. Sulpice, Switzerland. Tel. +41-21-691-0244; Fax +41-21-691-0245; email *mead@netgate.net* or *valence@mead.ch*; Web site *http://www.netgate.net/~mead.*

Miller Freeman — ICSPAT Online, an interactive, educational forum for signal processing engineers. The virtual conference provides the experience of attending a conference via the World Wide Web. The web site includes the 1996 white papers covering 40 application areas; interactive author Q & A; industry news; guest columnists; interviews with prominent thinkers in the field; a chat forum; design challenge contests; and future conference dates and speaking opportunities. Web site *http:///www.ICSPAT.com.*

National Institute of Standards and Technology — *Boulder*, CO. *Time and Frequency Seminars: Introduction-Level I*, June 23–24; *Fundamentals-Level II*, June 25–27. Information: Wendy Ortega Henderson, National Institute of Standards and Technology. Tel. 303-497-3693; Fax 303-497-6461; email *ortegaw@boulder.nist.gov.*

Northeast Consortium for Engineering Education — *Principles of Electronic Counter-countermeasures*—April 8–10, Atlanta; *Infrared Technology and Applications*—April 15–18 Atlanta; *Phased-array Radar System Design*—April 29–May 2, Atlanta; *Antennas: Principles, Design and Measurements*—May 19–22, St. Cloud, FL. Information: Kelly Brown, Northeast Consortium for Engineering Education, 1101 Massachusetts Ave., St. Cloud, FL 34769. Tel. 407-892-6146; Fax 407-892-0406.

***RF Design* Seminar Series** — April 21–23, Las Vegas, NV; Sept. 9–11, Santa Clara, CA. *RF and Wireless Engineering, Part 1, Practical High-Frequency Filter Design, Digital Modulation and Spread Spectrum for Wireless Communications*–April 21; *RF and Wireless Engineering, Part 2, Oscillator Design Principles, RF Power Transistor and Amplifiers*–April 22; *RF and Wireless Engineering, Part 3, Wireless Technology for Non-Engineers*–April 23. Information: Intertec Presentations, 6300 S. Syracuse Way, Suite 650, Englewood, CO 80111. Tel. 303-220-0600 or 800-288-8606; Fax 303-770-0253.

University of Missouri-Rolla — *Grounding and Shielding Electronic Systems: How to Diagnose and Solve Electrical Noise Problems*—May 1921, Boston; June 25-27, Research Triangle Park, NC, August 13–15, Dallas; *Circuit Board Layout to Reduce Noise Emission and Susceptibility*—May 21, Boston; June 27, Research Triangle Park, NC; August 15, Dallas. Information: Continuing Education Coordinator, University of Missouri-Rolla, 103 ME Annex, Rolla, MO 65409-1560. Tel. 573-341-4132. Fax 573-341-4992.; Web site *http://www.umr.edu/~conted.*

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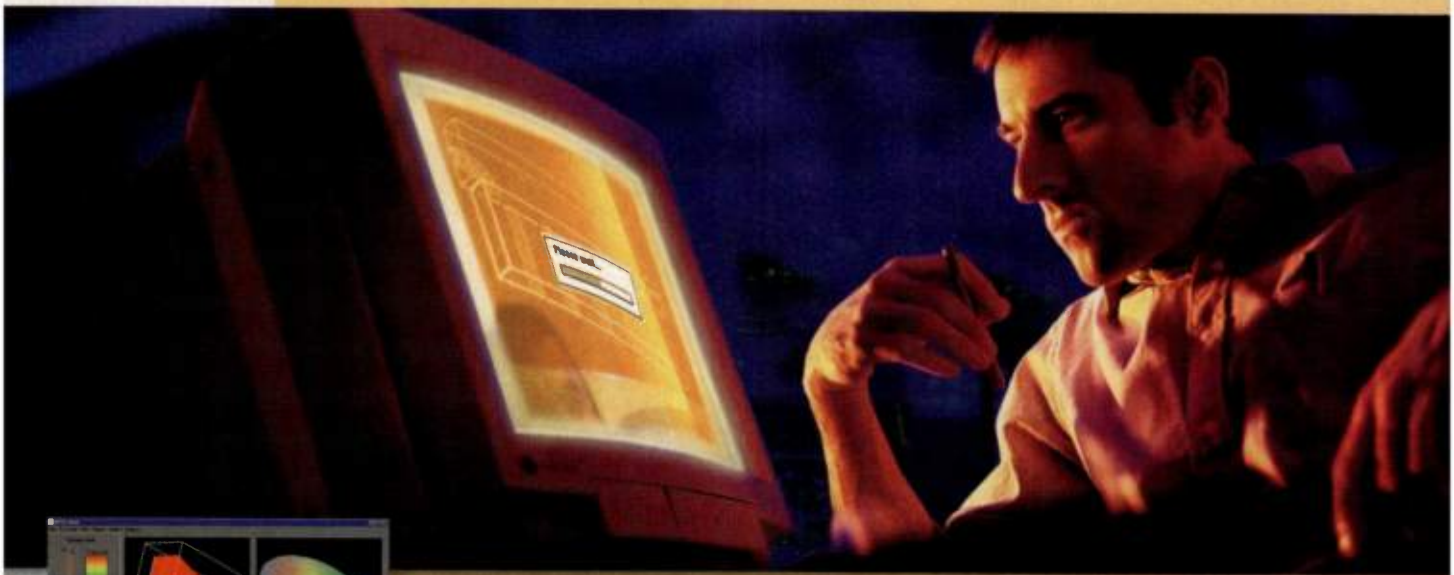

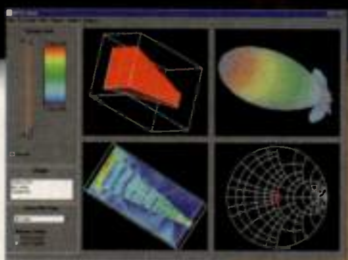

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Wireless LAN interface specification published

The Wireless LAN Interoperability (WLI) Forum, Sunnyvale, CA, a group of more than 20 mobile computing product and service suppliers, has published a draft wireless local area network (LAN) interface specification and interoperability test suite and has selected a test lab. The group showed the first multi vendor wireless LAN interoperability demonstration between products from eight members. The availability of the open specification allows any independent manufacturer to develop WLI Forum compatible products. The technical committee completed the test process for assessing product interoperability and provided the information to Los Angeles-based XXCal, an independent test lab. XXCal will test products using the defined process to ensure full interoperability. Products that pass the WLI Forum tests will earn the WLI Forum compatible designation.

Companies interested in testing at XXCal labs in the United States can call XXCal at 310-477-2902.

MSI software supports telecommunications lab

Mobile Systems International, Dallas, has donated a licensed version of its Planet wireless planning software to the Interdisciplinary Telecommunications Program at the University of Colorado, Boulder. The donation will allow the university to build its own wireless telecommunications lab.

Planet will be used to train students through the university's joint training effort with Telecommunications Engineering Systems and Services.

Contracts:

Micron signs Computer Methods—Micon Communications, Boise, ID, has signed Computer Methods, Livonia, MI, as an authorized systems integrator, to integrate the developing MicroStamp remote intelligence communications (RIC) family of products into systems for their automotive customers. Computer Methods will provide site-specific designs, customized software interface design and development, systems installation and service. Computer Methods specializes in diagnostics systems for vehicle-communications networks.

Strategic relationship for TDK and All American—TDK Semiconductor, Tustin, CA, has entered into a national distribution agreement with All American. The agreement joins TDK's advanced mixed-signal integrated circuit (IC) designs for local area network (LAN), embedded modem and set-top box applications with All American's technical sales engineers to benefit customers in the United States.

MCD to distribute NEC products—MCD Electronics, Hopkinton, MA, will distribute California Eastern Laboratories', Santa Clara, CA, line of NEC optoelectronic products. MCD will

offer NEC photocouplers, optocoupled metal-oxide semiconductor field effect transistors (MOSFETs), photo transistors, positive-intrinsic-negative (PIN) photo diodes and infrared GaAs light-emitting diodes (LEDs) throughout New Mexico, Colorado, Wyoming, Montana, Idaho, Washington, Oregon, Nevada, Arizona and California.

Qualcomm signs LOI to provide triple-mode chipsets to Japan –Qualcomm, San Diego, CA, has signed a letter of intent (LOI) with Asahi Kasei Microsystems (AKM), Japan, to provide a triple-mode chipset for the code division multiple access (CDMA) market in Japan. The chipset uses CDMA digital baseband technology developed by Qualcomm and J-TACS and N-TACS analog baseband technology developed by AKM. The new chipset will provide a system for triple-mode handsets, specialized terminals for digital cellular and other applications.

Measurement Systems developing new design to test tools for HP–Measurement Systems (IMS), Beaverton, OR, has signed an agreement with Hewlett-Packard (HP), Palo Alto, CA, for the development of a suite of integrated DANTES Virtual Test software tools for HP's mixed-signal test systems and the HP 8300 digital integrated-circuit test systems.

Business Briefs

Johnson Data Telemetry acquires E. F. Johnson Data Telemetry Division — Johnson Data Telemetry, Montreal, has purchased the Data Telemetry Division of E. F. Johnson, Burnsville, MN. The purchase allows Johnson Data Telemetry to focus on the growing wireless data communications sector. Johnson Data Telemetry is a worldwide supplier of RF products, which meet U.S., Canadian and International requirements for fixed wireless data applications. These include SCADA and telemetry for utilities, petrochemical, waste and fresh water management and radio frequency data capture and other markets.

Analog Devices and Zilog to design cordless phone chipset — Analog Devices, Campbell, CA, and Zilog, Norwood, MA, have joined forces to co-develop a new chipset for the 900 MHz cordless phone market. Analog Devices will provide radio frequency (RF) technology, and Zilog will supply digital chip and DSP-based software architecture. Analog Devices manufactures precision high-performance integrated circuits for analog and digital signal processing. Zilog develops, designs and manufactures application-specific standard products (ASSPs)

Digital receivers: The new wave for signal analysis

By Rodger H. Hosking

Digital receivers offer significant benefits in performance, density and cost when used to replace conventional analog receiver designs. Digital receivers have revolutionized electronic systems for a variety of applications including communications, data acquisition and signal processing. As a general capability, any system requiring a tunable bandpass filter can benefit from the use of digital receivers. To help you to appreciate the benefits of digital receivers, a conventional analog receiver system is compared to its digital receiver counterpart.

As the block diagram in Figure 1 shows, an analog receiver, the RF signal from the antenna typically is amplified with a tuned RF stage that amplifies a region of the frequency band of interest. This amplified RF signal then is fed into a mixer stage. The other input to the mixer is from the local oscillator with a frequency controlled by the tuning knob on the radio. The mixer translates the desired input signal to the intermediate frequency (IF). The IF stage is a bandpass amplifier that lets only one signal through. Common center frequencies for IF stages are 455 kHz for commercial AM and 10.7 MHz for FM broadcasts. The demodulator recovers the original modulating signal from the IF output using one of several different schemes. For example, AM uses an envelope detector, and FM uses a frequency discriminator. In a typical home radio, the demodulated output is fed to an audio amplifier and then to a speaker. The mixer performs an analog multiplication of the two inputs and generates a difference frequency signal.

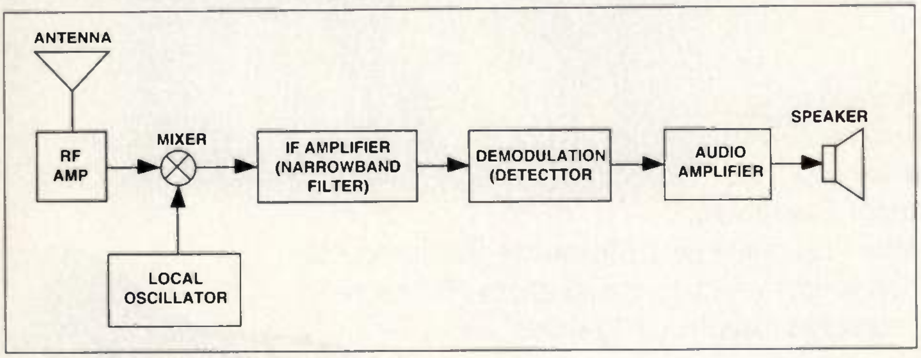


Figure 1. Analog receiver block diagram.

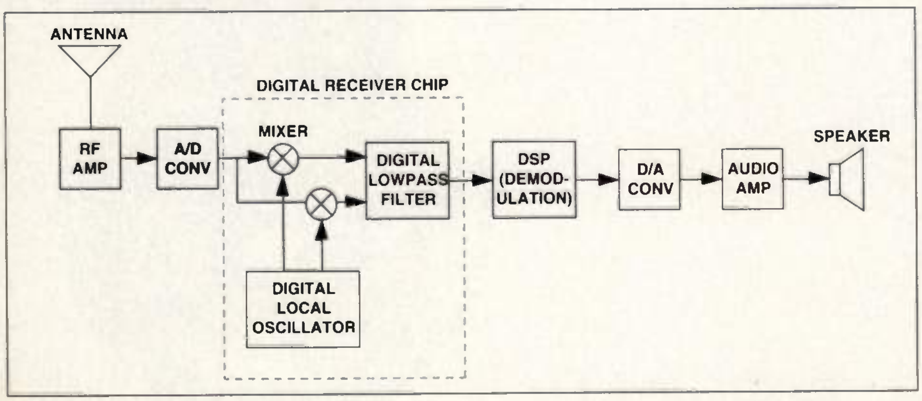


Figure 2. Digital receiver block diagram.

The frequency of the local oscillator is set so that the difference between the local oscillator frequency and the desired input signal (the radio station you want to receive) equals the IF.

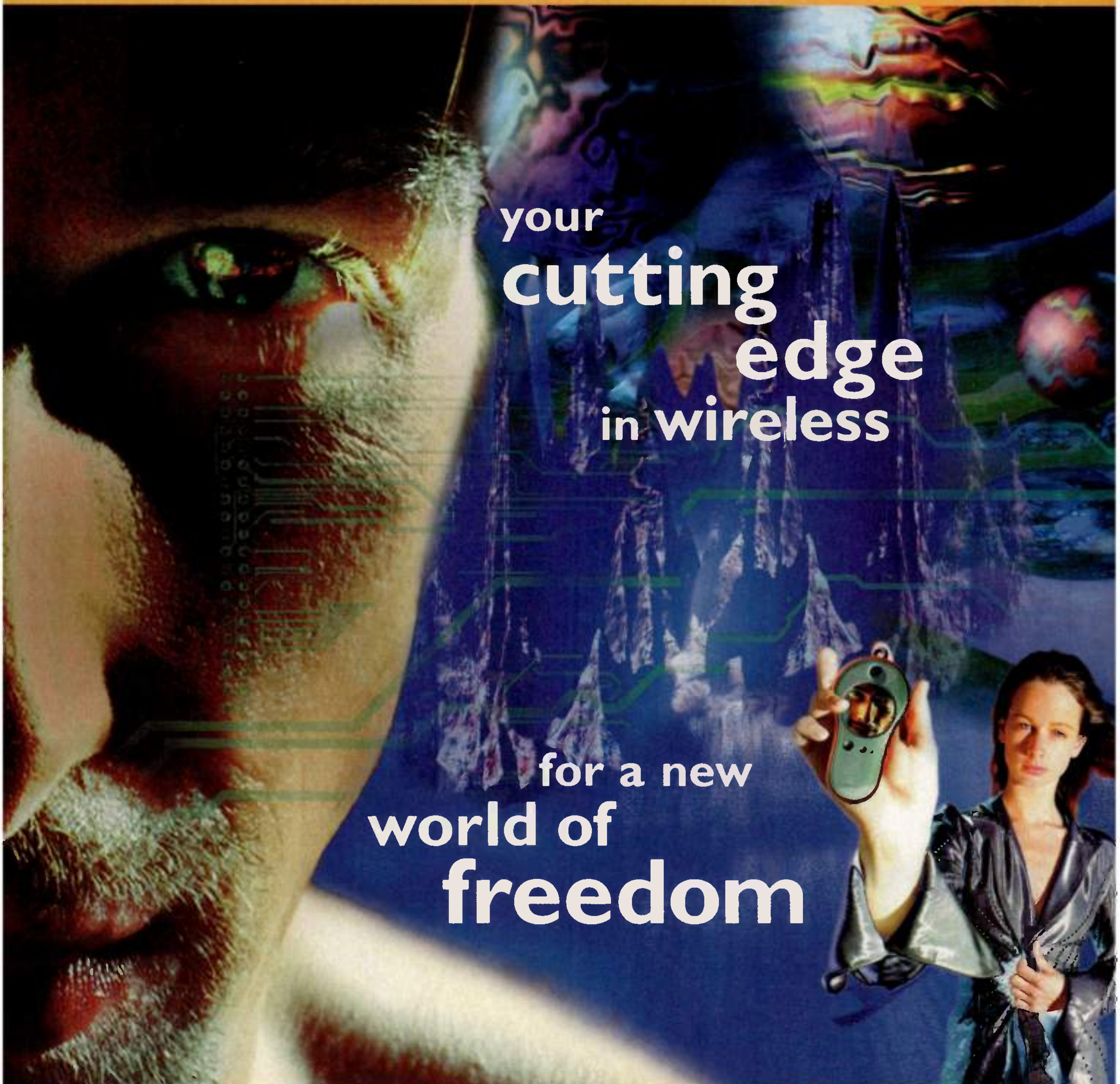
If you wanted to receive an FM station at 100.7 MHz, and the IF frequency is 10.7 MHz, you would tune the local oscillator to 100.7 – 10.7 = 90 MHz. This is called *downconversion* or *translating* because a signal at a high frequency is shifted down to a lower frequency by the mixer. The IF stage acts as a narrowband filter that passes only a "slice" of the translated RF input. The bandwidth of the IF stage is equal to the bandwidth of the signal (or station) that you are trying to receive. For commercial AM, the bandwidth is about 5 kHz, and for FM it is about 100 kHz. This is consistent with channel spacing of 200 kHz for FM and 10 kHz for AM.

Digital receiver

A digital receiver block diagram is shown in Figure 2. Note the strong similarity to the analog receiver diagram. All of the basic principles of analog still apply. In the digital receiver block diagram, an analog-to-digital (A-to-D) converter is used to digitize the RF input into digital samples right after the RF amplifier and an optional RF translator stage. All of the subsequent mixing, filtering and demodulation are performed using digital signal processing elements.

A theorem fundamental to sampled data that lays the foundation for the A-to-D converter requirements is the Nyquist theorem, which states: "Any signal can be represented by discrete samples, if the sampling rate is at least twice the bandwidth of the signal." For example, if we use an A-to-D converter sampling at 70 MHz, then the bandwidth of the analog input must be less than 35 MHz. The following is a test to see what happens if we ignore Nyquist's criterion.

For all input signals lower than $f_s/2$, such as the one at f_o, the Nyquist criterion is met. In fact, any number of sig-



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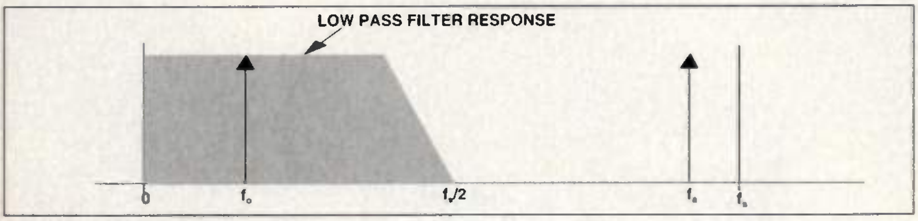

Figure 3. Anti-aliasing filter.

nals can be present in the shaded region, and all will be represented correctly in the sampled data.

But if we have a signal present at say, f_a, which is higher than $f_s/2$, the sampling process will generate an aliased image that will appear in the sampled data at f_s-f_a. This image cannot be distinguished from a true signal that might have been present at that same frequency. Once an aliased image is created in the sampling process, no amount of further processing can distinguish between a true signal and an aliased signal; therefore, it is imperative to prevent aliasing.

The most straightforward way to prevent aliasing is to use a lowpass filter before the A-to-D converter that removes all signals higher than $f_s/2$. The signal at f_a is blocked so the A-to-D converter never sees it. Conveniently for the user, anti-aliasing filters often are included on the same board as the A-to-D converter. Nyquist's criterion also can be met by limiting the bandwidth of the sampled signal using other types of filters. For example, suppose we wanted to receive signals between $f_s/2$ and f_s in the above diagram. If we used a bandpass filter with a passband from $f_s/2$ to f_s, we would meet the Nyquist criterion because the bandwidth is equal to one-half the sampling rate.

Once the sampling is done, the band of signals from $f_s/2$ to f_s is "folded" into the frequency band from DC to $f_s/2$. The half-sampling frequency often is called the "folding frequency." This technique is sometimes called "undersampling." Although this works well in theory, care must be taken in actual practice to ensure that the A-to-D converter supports the higher-input frequencies it must handle. Looking again at the overall block diagram, the digital A-to-D samples coming out of the A-to-D converter are being fed to the next stage, which is the digital receiver chip (in the dotted line as shown in Figure 2). The digital receiver chip (Figure 4) is contained on a single monolithic chip that forms the heart of the digital receiver system.

Inside the digital receiver chip are three major sections: local oscillator, mixer and a decimating lowpass filter.

The local oscillator

The local oscillator is a direct-digital frequency synthesizer (DDS) sometimes called a numerically controlled

ERMES Multipath and Simulcast Paging Test

ERMES (European Radio Message System) specifications (pr TBR 007) recommend testing of receivers in multipath and simulcast conditions. The maximum degradation in sensitivity for combined multipath and simulcast (quasi-synchronous) transmissions under normal conditions is defined to be 15 dB.

To perform the test, refer to the setup illustrated in Figure 1. The two 4-PAM/FM signal generators (A and B) are connected to the receiver under test via Rayleigh fading emulators and a combiner. The signal from generator A is on the nominal RF frequency (ERMES channel 8) and the signal from generator B on the nominal frequency +30 Hz ± 3 Hz. The difference in contribution to the signal strength from the signal generators is 1 dB, the higher signal coming from signal generator A.

The fading emulators are adjusted for the speed of 3 km/h. The fading emulators are set for Rayleigh fading and there is no correlation between the two emulators.

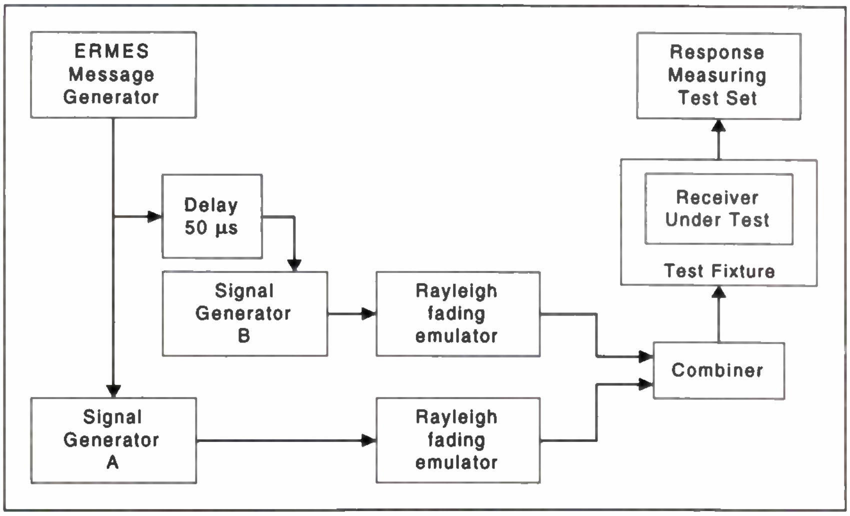

Figure 1. ERMES Receiver Test Configuration with Multipath and Simulcast conditions.

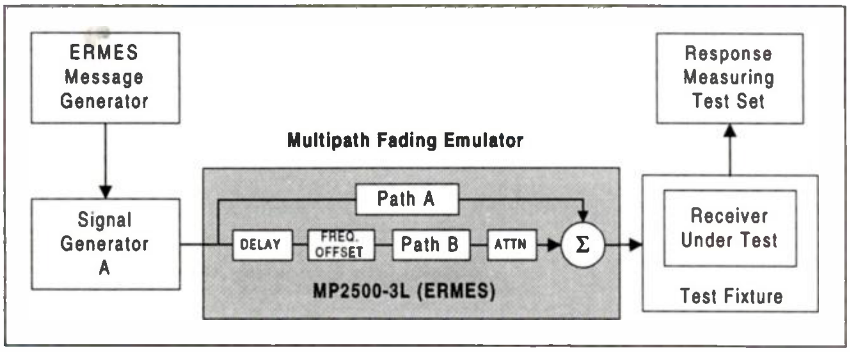

Figure 2. Identical Test Setup with Noise Com's Multipath Fading Emulator, MP2500-3L (ERMES).

The above setup requires two signal generators, a delay line, a combiner, and two fading emulators (or a two-channel fading emulator). There is an alternate solution, however, that can eliminate most of the instrument requirements down to a single channel fading emulator and signal generator.

As illustrated in Figure 2, the measurement setup has been rearranged somewhat using Noise Com's MP2500-3L (ERMES). The output from the signal generator is split into two different paths in the fading emulator. The first path (A) is Rayleigh-faded without any delay or attenuation. The second path (B) is, however, delayed by 50 µs and attenuated by 1 dB; in addition, the signal is frequency offset by +30 Hz. This is easily accomplished by the instrument's graphical user interface software. The two path outputs are combined within the fading emulator and then passed to the receiver under test.

The MP2500-3L (ERMES) also saves the step of measuring the output power of Rayleigh faded signal, thus eliminating the need for a power meter. Its built-in output power setting capability allows the average output power level to be set and maintained even if the parameters are changed in real time.

The versatile multipath fading emulator MP2500-3L (ERMES) is specifically designed for ERMES and other paging applications.

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Multipath Fading Emulator for ERMES MP2500-3L (ERMES)

Multipath fading emulator for ERMES Receiver Testing

The MP2500-3L (ERMES) emulates wireless communication channels with 3 different reflected signal paths for ERMES applications. For testing ERMES receivers, the instrument is an ideal partner for providing realistic channel environments.

The instrument has prestored in its memory all the ERMES specified test parameters. It also provides programmable output power, delay, attenuation, frequency shift (Doppler), and a choice of Rayleigh, Rician, log-normal, Nakagami, and Suzuki fading statistics for each path.

The MP2500-3L (ERMES) includes a built-in 486DX/33 computer and LCD display. A Windows-based graphical user interface simplifies setup and operation.

Ordering Information

Model Number	Frequency Range	Application
MP2500-3L (ERMES)	30-2000 MHz	ERMES

Options:

- Synthesized local oscillators
- Dual duplex interface
- I/Q interface (DC to 13 MHz)
- High-power attenuator
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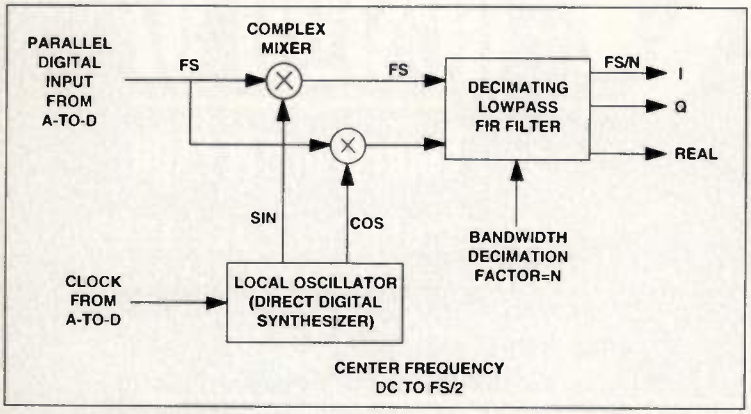

Figure 4. Digital receiver chip.

oscillator (NCO). The oscillator generates digital samples of two sine waves precisely offset by 90° in-phase, creating sine and cosine signals. It uses a digital-phase accumulator and sine and cosine look-up tables. (Note that the A-to-D clock is fed into the local oscillator.)

The digital samples out of the local oscillator are generated at a sampling rate exactly equal to the A-to-D sample clock frequency f_s. The sine frequency is programmable from DC to $f_s/2$ with as many as 32 bits of resolution. The frequency easily is changed by programming the amount of phase advance per sample. Using a 70 MHz sampling clock, the frequency range is from DC to 35 MHz, and the resolution is less than 1 Hz.

The local oscillator has impressive frequency-switching characteristics. When switching between two frequencies, the digital accumulator precisely maintains the phase of the sine and cosine outputs for phase-continuous switching. This allows the local oscillator to perform frequency-shift keying (FSK) and finely resolved sweeps. Transients and settling normally associated with other types of local oscillators, such as phase-locked loop (PLL) synthesizers, are eliminated. Some digital receivers employ a local oscillator with a built-in "chirp" function. This is a fast, programmable and precise frequency sweep that is useful in radar systems.

The mixer

The next principal component of the digital receiver chip is the mixer, consisting of two digital multipliers. Digital input samples from the A-to-D mathematically are multiplied by the digital sine and cosine samples from the local oscillator. Because the data rates from these two mixer input sources match the A-to-D sampling rate, f_s, the multipliers also operate at the same rate and produce multiplied output product samples at f_s. The sine and cosine inputs from the local oscillator create I and Q (in-phase and quadrature) outputs that are important for maintaining phase information contained

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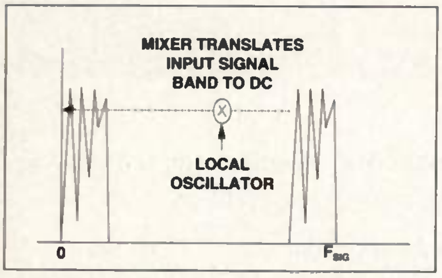

Figure 5. Digital receiver mixer translation.

in the input signal.

From a signal standpoint, the mixing produces a translation or difference frequency signal the same way a conventional analog mixer does. Unlike analog mixers, which generate unwanted mixer products, the digital mixer produces only two outputs: the sum and difference frequency signals.

The difference mixer product in the frequency domain is shown in Figure 5. At the output of the mixer, the high-frequency wideband signals in the A-to-D input have been translated down to DC with a shift or offset equal to the local oscillator frequency. This is similar to the analog receiver mixer except that the analog receiver mixes the RF input down to an IF (intermediate frequency).

In the digital receiver, the precision afforded by digital signal processing allows mixing to work right down to baseband (or 0 Hz.) Overlapping mixer images are rejected by the accuracy of the sine and cosine local oscillator samples and by the mathematical precision of the multipliers in the mixer. By tuning the local oscillator over its frequency range, any portion of the RF input signal can be mixed down to DC. In effect, the wideband RF signal spectrum can be shifted around 0 Hz, left and right, simply by changing the local oscillator frequency. Once the RF signal has been translated, it is ready for filtering.

The decimating lowpass filter

The decimating lowpass filter accepts input samples from the mixer output at the full A-to-D sampling frequency f_s. It uses digital signal processing to implement a finite impulse response (FIR) filter transfer function. The filter passes all signals from 0 Hz to a programmable cutoff frequency or bandwidth and rejects all signals higher than that cutoff frequency. This digital filter is a complex filter that processes both I and Q signals from the mixer. At the output, you can select either I and Q (complex) values or real values, depending on your system requirements.

Figure 6 shows a representation of the filter's action in the frequency domain. The filter passes signals only from 0 Hz to the filter bandwidth. All higher frequencies have been removed. Remember, the wideband input signal was translated down to DC by the mixer and was positioned around 0 Hz by the tuning frequency of the local oscillator. At the filter output, we have selected a narrow slice of the RF input signal, translated it to DC and blocked all other signals. The bandlimiting ac-

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JMS-1MH	+13	2-500	DC-500	5.75	60	45	9.45
JMS-1H	+17	2-500	DC-500	5.90	50	50	11.45
JMS-2L	+3	800-1000	DC-200	7.0	24	20	7.45
JMS-2	+7	20-1000	DC-1000	7.0	50	47	7.45
JMS-2LH	+10	20-1000	DC-1000	6.5	48	35	9.45
JMS-2MH	+13	20-1000	DC-1000	7.0	50	47	10.45
JMS-2H	+17	20-1000	DC-1000	7.0	50	47	12.45
JMS-2W	+7	5-1200	DC-500	6.8	60	48	7.95
JMS-5	+7	5-1500	DC-1000	6.0	35	37	9.95
JMS-5LH	+10	5-1500	DC-1000	6.0	50	35	10.95
JMS-5MH	+13	5-1500	DC-1000	5.7	57	35	11.95
JMS-5H	+17	5-1500	DC-1000	5.9	50	35	12.95
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SKY-60LH	2500-6000	+10	6.2	28	16.95
SKY-60MH	2500-6000	+13	6.2	28	17.95
SKY-60H	2500-6000	+17	6.2	28	18.95
SKY-53R	2800-5300	+7	5.7	28	14.95
SKY-53LHR	2800-5300	+10	5.7	28	16.95
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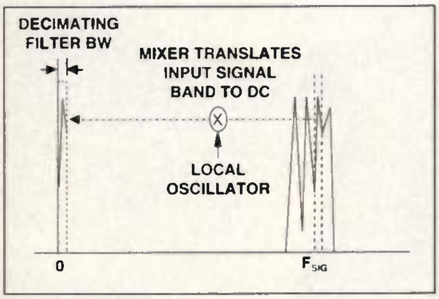

Figure 6. Decimating filter bandlimiting.

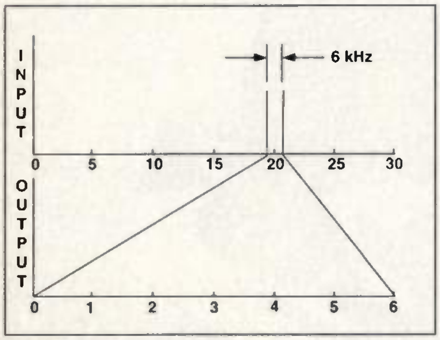

Figure 7. Frequency zoom.

tion of the filter is analogous to the action of the IF stage in the analog receiver except that the decimating lowpass filter operates around DC instead of being centered at an IF frequency.

An actual frequency display is shown in Figure 7. The top figure shows a 30 MHz wideband RF input that was sampled by the A-to-D converter at 70 MHz. Suppose we have a signal of interest at 20 MHz, and we know that the bandwidth of the signal is 6 kHz. By setting the local oscillator to 20 MHz and the bandwidth of the filter to 6 kHz, we can translate the signal and extract only a 6 kHz band as shown in the bottom figure. Because the output bandwidth is limited to 6 kHz, we are permitted by Nyquist's theorem to drop the output sampling rate to just higher than 12 kHz, in this case 14 kHz.

Decimation factor

To set the filter bandwidth, we need to program a parameter called the decimation factor. Because the output bandwidth and the output sampling rate are related directly, the decimation factor also sets the output sampling rate. The decimation factor, N, determines both the ratio between input and output sampling rates and the ratio between input and output bandwidths. Revisiting the previous example, we start with an input bandwidth of 30 MHz, and the result is an output bandwidth of 6 kHz. In this case, the decimation factor was set for a factor of 5,000.

Digital receivers can be divided into two classes, narrowband and wideband, distinguished by the programmable range of decimation factors. Narrowband receivers have a range of decimation factors from 32 to 32,768 for real outputs. Wideband receivers have a range of decimation factors from 1 to 32 for real outputs. When complex output samples are selected, the sampling rate effectively is halved, because a pair of output samples are delivered with each sample clock.

Programming digital receivers

To review, the digital receiver chip performs two principle signal-processing operations controlled by two programmable parameters:

1. Translation of the input signal down to DC controlled by the tuning frequency programmed into the local oscillator.

2. Lowpass filtering in which the bandwidth and output sampling rate are controlled by setting the decimation factor.

Because everything inside the decimating lowpass filter is performed with digital circuitry and digital signal processing (DSP) techniques, there are no undesirable effects normally associated with analog filters used in conventional receivers. There is no initial component tolerance, temperature variation or aging characteristic. Neither calibration nor preventive maintenance is required. This provides excellent channel-to-channel matching for applications in which phase-shift variation between channels is important. The finite impulsive response (FIR) digital filters used are linear phase for well-behaved transient response. The filter bandwidth is programmable over a wide range (1,000 to 1), with absolutely predictable and uniform response throughout. The signal is tailored precisely for DSP by preselecting only the signal of interest by bandlimiting and by providing it to the DSP at the optimum sampling rate.

The output signal is translated, fil-

tered, bandlimited and ready for further processing. The output signal from the decimating lowpass filter is still a sampled time signal that could represent any kind of modulated or unmodulated signal. We could send this signal directly to a D-to-A converter, producing an analog waveform. For straight single-sideband frequency division multiplexed speech, we could connect the D-to-A output to a speaker and listen to the selected voice channel directly. In many systems, such as modem demodulation, further processing is required. Because the sampled receiver output signals now are a lower sampling rate, this additional processing readily can be handled by a DSP.

DSP for digital receivers

Any form of demodulation can be implemented by loading the DSP with the appropriate algorithm. AM can be demodulated with an envelope detector; FM and PM can be demodulated using a phase or frequency discriminator algorithm. The ability quickly to change the local oscillator allows frequency agile modulation schemes to be accommodated as well. Analysis functions include energy detection such as required by scanning receivers, which may be implemented with a fast fourier transform (FFT). Other analysis functions include cryptography, identification of transmitters based on transmission frequency, modulation schemes and other signal characteristics. Once the signal is brought into the DSP arena, automated functions, such as center frequency and bandwidth tuning, can be implemented to track a complex signal that may be moving or hopping. Interesting signals can be stored on hard disk, tape or other media, and the time of the signal event can be logged as well. With this arrangement, when new or proprietary demodulation, processing or analysis schemes are required, no new hardware is necessary. Instead, a new DSP software algorithm is loaded. Think of the digital receiver as a hardware preprocessor for DSP. It preselects only the signals you are interested in and removes all others. This provides an optimum bandwidth and minimum sampling rate into the DSP. Because the number of DSPs required in a system is directly proportional to the sampling rate of input data, by reducing the sampling rate, you can dramatically reduce the cost and complexity of the DSP system that follows. Even if the digital receiver outputs do not require a great deal of signal processing, reduction of bandwidth and sampling rate helps to save time in data transfers to another subsystem; helps minimize recording time and tape or disk space; and speeds up communication channels.

Conclusion

Digital receivers can dramatically reduce the DSP requirements for systems that need to process signals contained within a certain frequency band of a wideband signal. The fast tuning of the digital local oscillator and the easy bandwidth selection in the decimating digital filter make the digital receiver easy to control. Because all of the circuitry uses digital signal processing, the characteristics are precise and predictable, and they will not drift with time, temperature or aging. This also means excellent channel-to-channel matching and no need for calibration, alignment or maintenance. These are the advantages of using digital receivers. RF

About the author

Rodger H. Hosking, vice president of Pentek, was a co-founder of the company in 1986. With more than 25 years experience in the electronics industry, he previously was engineering manager at Rockland Systems and its successor company, Wavetek Rockland. While there, he was responsible for the development of digital frequency synthesizers, FFT spectrum analyzers and digital filter products. He designed the first commercial direct digital frequency synthesizer in 1971 and holds patents in frequency synthesis and FFT spectrum analysis techniques. He has a B.S. physics from Allegheny College, and a B.S.E.E. and an M.S.E.E. from Columbia University. He can be reached at Pentek, One Park Way, Upper Saddle River, NJ 07458. Tel: 201-818-5900; fax 201-818-5904; E-mail rodger@pentek.com. Web site http://www.pentek.com.

Genetic optimization algorithms create high-performance, fixed-point digital filters

By Carter Smith

An RF engineer implementing an analog filter design usually will see deviations from the designed frequency response caused by the necessity of using parts with standard values. A similar situation occurs when a digital signal processor (DSP) designer implements a digital filter in hardware that uses a fixed-point numeric format. This is because in a practical implementation of a digital filter, in hardware such as an application-specific integrated circuit (ASIC) chip or software on a DSP, only a finite number of bits are available for number representation and numeric operations such as multiplication and addition. This finite number of bits can cause the filter not to perform as intended. Designers can use optimization algorithms and design software to create fixed-point digital filter designs that meet specifications at a minimum cost and power.

A finite impulse response (FIR) low-pass filter, such as given in the IS-95 code-division, multiple-access (CDMA) specification, is typically designed using floating point arithmetic. Ideally, the floating-point filter is then converted to a fixed-point arithmetic design. Unfortunately, that causes the filter response to change and violate the filter specifications. This fixed-point filter then is tweaked automatically to meet specifications using some novel genetic optimization techniques. The result is a low-cost, low-power, fixed-point numeric format digital filter design that meets the stringent CDMA wireless phone communications specification using the minimal number of bits.

Floating-point filter specifications

The CDMA specification (IS-95) calls for a baseband low-pass FIR filter. This filter is used to eliminate out-of-band noise and limits the signal bandwidth of the data stream. The desired filter response is that of a low-pass filter, with a passband extending to 590 kHz, a transition band from 590–740 kHz, and a stopband attenuation of greater than 40 dB for the frequency range of 740 kHz and higher. These IS-95 specifications are shown graphically in Figure 1.

In addition to the performance requirements, the CDMA specification also gives a list of FIR filter coefficients for a 48-tap FIR filter. These coefficients will yield a filter that meets the specifications shown in Figure 1, given that the sampling time of the system is set as specified (sampling time step of 0.2034505283333 usec). These coefficients are given in column 2 of Table 1, where k is the coefficient number and h(k) is the coefficient value. (See the IS-95 specification, section 6.1.3.1.10 for details.)

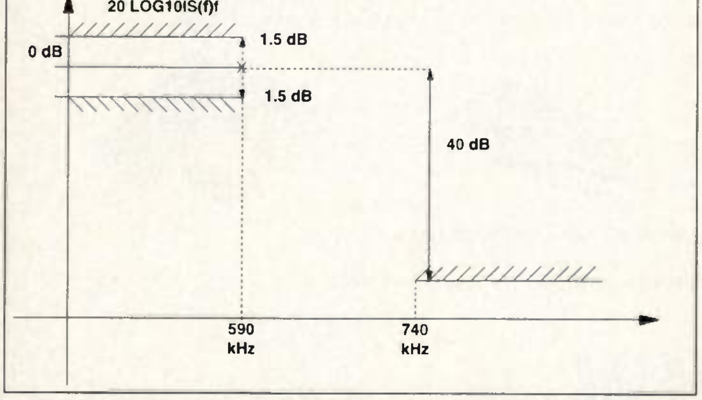

Figure 1. CDMA (IS-95) baseband filter frequency response specification limits.

An FIR filter can be used to implement the desired filter response by using the set of 48 filter coefficients as listed in column 2 of Table 1. An FIR filter can be written in mathematical form as:

$$y(n) = \sum_{k=0}^{N} h(k)x(n-k) \qquad (1)$$

where y(n) denotes the filter output at the n-th time step, x(n – k) denotes the filter input at the (n – k)th time step, and N is the order of the filter (i.e., the number of coefficients that defines the FIR filter).

The filter coefficients in column 2 of Table 1 are as stated in the IS-95 specifications and are not yet quantized to fit a finite number of bits, which is the end goal of our design. Also, because the filter coefficients are symmetric about the center index k=23, 24, the FIR filter will have linear phase [2].

Construction and simulation of the floating-point FIR filter

The next step in our design is to implement the 48-tap FIR filter in a floating-point configuration and simulate it. Because we are using a symmetrical filter for linear phase, we will implement the filter in the direct form. Figure 2 shows a portion of the cascaded FIR filter to demonstrate how it was implemented. The unquantized coefficients listed in column 2 of Table 1 now are loaded into the simulation. The simulation is set up so that all multiplies and adds are carried out in full floating-point precision.

To simulate and test the performance of the filter, we set up a test bench in the simulator. The test bench drives an impulse into the FIR filter then processes the output of the filter using a fast Fourier transform (FFT). The FFT generates the frequency response of the floating-point implementation of the filter we have constructed. The results from the simulation show that the floating-point version of the CDMA FIR filter does indeed meet the specifications discussed previously. (See Figure 3.) This

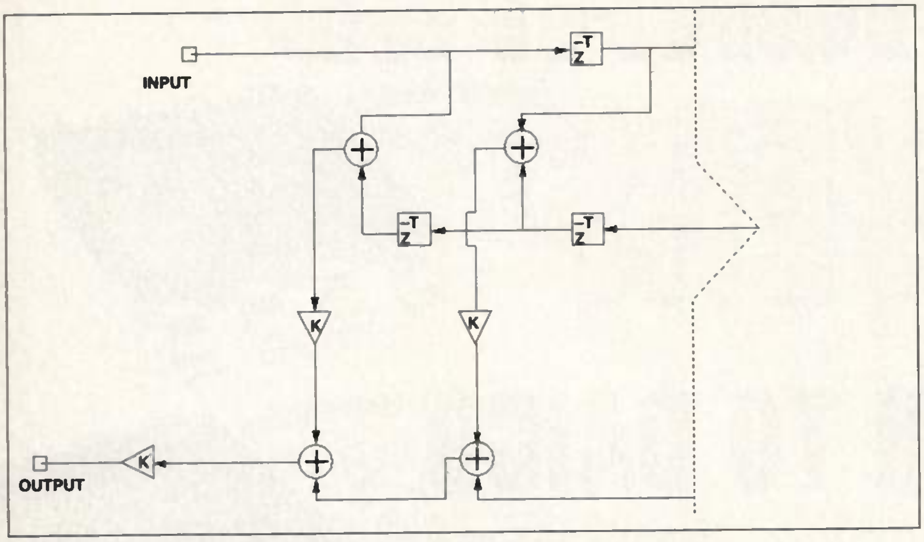

Figure 2. A portion of the FIR filter as constructed in the simulation environment.

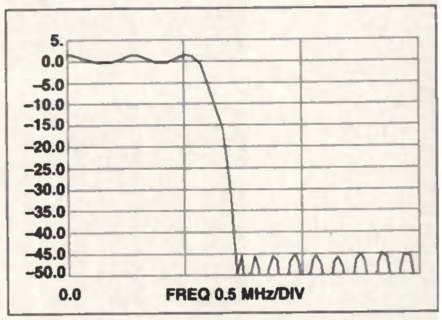

Figure 3. Frequency response of the floating FIR filter implementation.

is to be expected because we are using identical coefficient values to the specification, and floating-point math is used in the simulation model. The next step in the design process is to change the simulation to determine the performance of the filter when fixed-point coefficients and math are used.

Fixed-point implementation of the filter

In our example, only 16 bits (total) are available, 12 bits of which will be used to represent the fractional part of numeric values. The upper four bits will be used to allow sufficient headroom when multiplication and addition are performed. If we take column 2 of Table 1 (floating-point coefficients) and quantize the coefficients to the available number of bits (12), the result is the values shown in column 3 of Table 1. These values are the filter coefficient values closest to the unquantized original coefficients of column 2 of Table 1.

Because we have only 12 bits for representation of the coefficient, the fractional values are changed by quantitization from the floating-point values given in column 2 of Table 1. The fractional resolution with 12 fractional bits is equal to $1/2^{12} = 1/4096 =$ 0.000244140625. Thus, our coefficients will be quantized to multiples of this value. These quantized coefficients are used in the next simulation of the digital FIR filter to determine how the filter performance has been reduced by the quantitization of the coefficients and the fixed-point math.

Checking performance of the fixed-point filter

To check performance of this fixed-point FIR filter configuration, adjust the controls in the simulation. This allows us to examine the filter response with a fixed-point format 2s complement numeric format <16,12> (i.e., 16 bits total of which 12 bits are used to represent the fractional part), with truncation quantization and saturation overflow. Truncation quantitization means that if the result of a mathematical operation uses more resolution (places after the decimal point) than we can support, the number is truncated to simulate how the real fixed-point FIR filter hardware will work. Saturation overflow indicates that when the magnitude of the numbers gets too large, they will clip at the maximum or minimum value rather than wrapping around to a negative value, as the 2s complement number system inherently does.

After setting the simulation control parameters to emulate the desired fixed-point characteristics, it is possible to simulate the fixed-point implementation of the FIR filter. The same test bench used to test the floating-point FIR filter will be used to test the fixed-point implementation of the FIR filter. Figure 4 shows the frequency response of the fixed-point implementation of the

	FIR COEFFICIENTS (PER IS-95 SPEC)	FIR COEFFICIENTS (QUANTIZED TO 12 BITS)	FIR COEFFICIENTS (12 BITS AFTER GENETIC OPTIMIZATION)
k	h(k)	h(k)	h(k)
0,47	-0.025288315	-0.025390625	-0.02539059974
1,46	-0.034167931	-0.0341796875	-0.034667969
2,45	-0.035752323	-0.03564431	-0.03613259
3,44	-0.016733702	-0.016845703125	-0.01684570274
4,43	0.021602514	0.021484375	0.02172851589
5,42	0.064938487	0.06494140625	0.064453125
6,41	0.091002137	0.091064453125	0.09106438126
7,40	0.081894974	0.081787109375	0.081298819
8,39	0.037071157	0.037109375	0.036621094
9,38	-0.021998074	-0.02197265625	-0.021484375
10,37	-0.060716277	-0.060791015625	-0.060302735
11,36	-0.051178658	-0.05126953125	-0.05078125
12,35	0.007874526	0.0078125	0.0073242188
13,34	0.084368728	0.08447265625	0.083984375
14,33	0.126869306	0.126953125	0.12646485
15,32	0.094528345	0.094482421875	0.09448242226
16,31	-0.012839661	-0.012939453125	-0.01269531211
17,30	-0.143477028	-0.1435546875	-0.14306641
18,29	-0.211829088	-0.2119140625	-0.21166991811
19,28	-0.140513128	-0.140625	-0.14038085811
20,27	0.094601918	0.094482421875	0.093994141
21,26	0.441387140	0.44140625	0.44116211063
22,25	0.785875640	0.785888671875	0.78588867126
23,24	1.0	1.0	1.0

Table 1. FIR filter coefficients as specified in IS-95, as implemented in fixed-point numeric format and as optimized to meet specifications.

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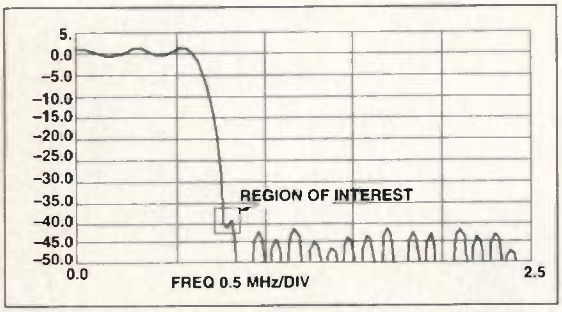


Figure 4. Frequency response of an FIR filter with a fixed-point finite numeric format of <16,12> (16 bits total, 12 bits for fractional representation). This fixed-point filter violates the specifications.

FIR filter. This simulation was done using the fixed-point 2s complement <16,12>, truncation quantization, saturation overflow numeric format.

Results of the fixed-point filter simulation

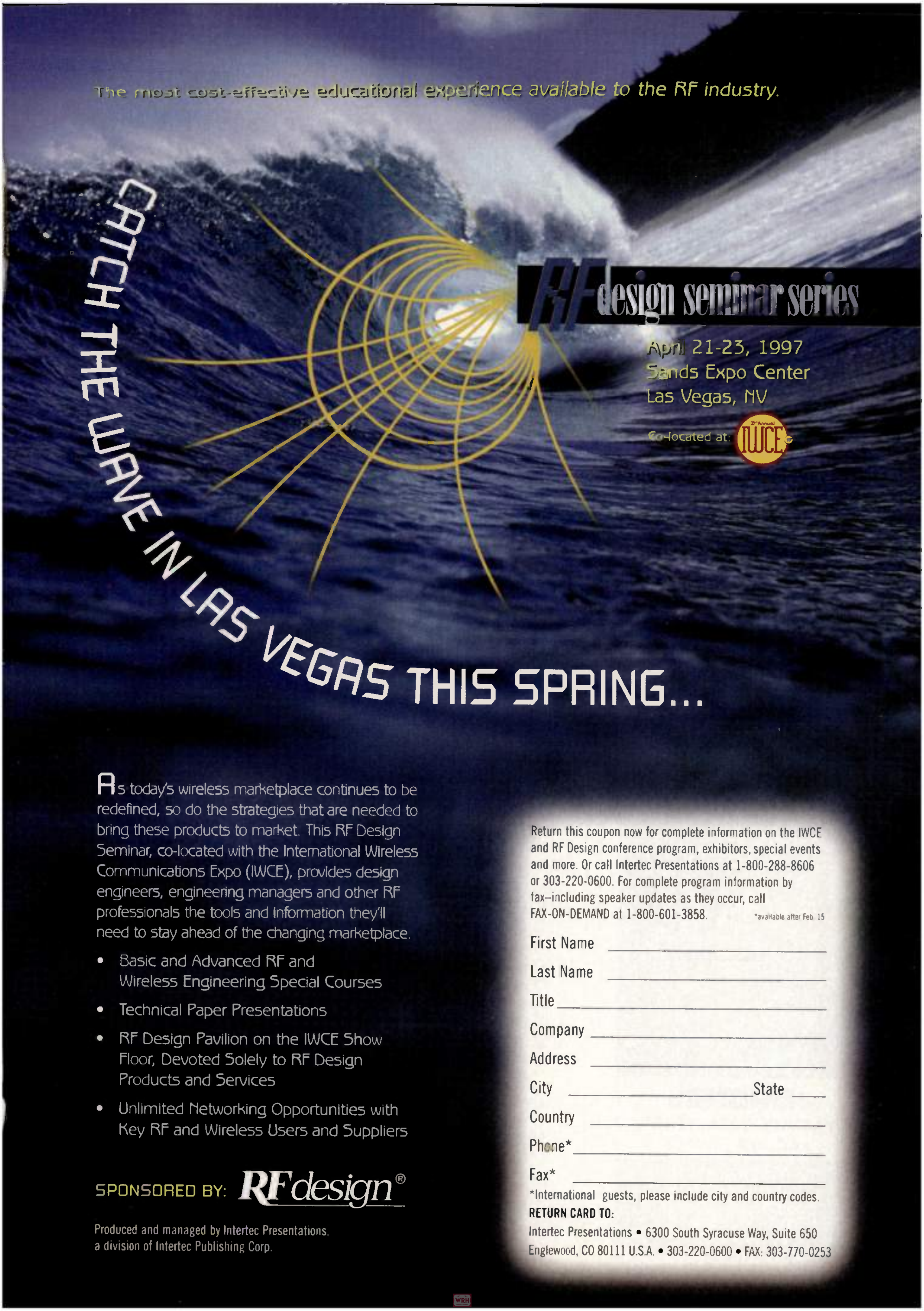
Figure 4 shows that the filter specification is violated for the frequency range of approximately 760–770 kHz, where the filter magnitude response is not attenuated below -40 dB as required by the IS-95 baseband filter specifications.

The area within the box of Figure 4 shows the area at which the specification is violated.

Figure 4 shows that, at about 770 kHz, the filter magnitude response is almost –39 dB, which is 1 dB higher than the required –40 dB value as specified (in IS-95) for frequencies greater than 740 kHz.

The filter response in Figure 4 is distorted from the previous floating-point design (Figure 3), but what caused this change in the frequency response? The change in frequency response is caused by a shift in the location of the zeros in the FIR filter. The shift in the zero locations of the FIR filter is caused by two things. First, the filter coefficients are quantized from floating point to fixed point. This quantitization of the coefficients causes a slight change in the values of the coefficients, which causes a cor sponding shift in the zero locatio Second, when fixed-point math is u for the adds and multiplies of the ters, the cumulative errors also cause the zeros to shift.

From the fixed-point FIR filter sir lation results in Figure 4, it is cl that this implementation of the filte not acceptable, because the stop-b attenuation specification is violated. A designer's typical response to this problem is to add another bit to the number format. Adding another bit two to the numeric format proba will solve the problem, but it comes the price of a more expensive des implementation that will draw m power. In many cases, higher-po and higher-cost implementation not acceptable. The designer need find a method that will allow the us the minimum number of bits, 1 this case, and still meet the per mance goals. Optimi-zation technic are not applied often to this situat but they may be the best way to s



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the problem and still keep a low-cost, *minimum-bit design.*

How optimization can help to solve fixed-point problems

To solve the fixed-point filter implementation problem, the optimization tools in OmniSys will be used to tweak the filter coefficient values. This optimization will create a large number of designs and will select the designs that meet specifications. Details on this fixed-point filter coefficient optimization are explained below.

During the optimization of the fixed-point FIR filter response, the filter coefficients are selected, and the resulting filter response is evaluated, to see whether it meets the desired response. The selection of the filter coefficients is done using the genetic optimizer method available in the simulation tool. In the context of the genetic optimization of the filter response, the selection of filter coefficients is explained below.

Let's assume that the FIR filter is made up of N filter coefficients, which are to be represented in some desired fixed-point 2s complement numeric format. The filter is defined by a set of N nominal filter coefficients. Each filter coefficient is discretized (quantized), i.e., it can take on only a discrete set of numeric values, with the step size between adjacent values determined by the number of bits used for fractional representation. In the initial iteration through the genetic optimizer, an initial population of 30 sets of N filter coefficients is selected randomly, i.e., 30 different FIR filters are created because each set of N filter coefficients defines a different filter response. These sets of N filter coefficients are distributed randomly in a neighborhood of the nominal filter coefficients.

These 30 filter responses are then evaluated against the desired filter response and ranked. The best five filter responses are selected as winners and used in the next iteration as parents by the genetic optimizer. These five sets of N filter coefficients, which define the winning five filter responses in the initial iteration, then are used to generate a new population of 30 sets of N filter coefficients, and the whole process of ranking and selection of winners then is repeated. By cycling through a number of such iterations (or generations), the genetic optimizer is able to provide a better set of filter coefficients and a filter response that is much closer to the desired filter response. Note the analogy of natural selection (survival of the fittest) to the genetic optimizer selection of the fittest set of coefficients for our filter [1].

Setting up the goals for the optimizer

For the optimization process to work properly, first tell the optimizer what the goals are. In this case, we would like the optimizer to create designs that meet the filter specification, using 12 bits to represent the fractional filter coefficient values and 16 bits total for all mathematical operations. Each design will be different only in that the values of the filter coefficients will be altered

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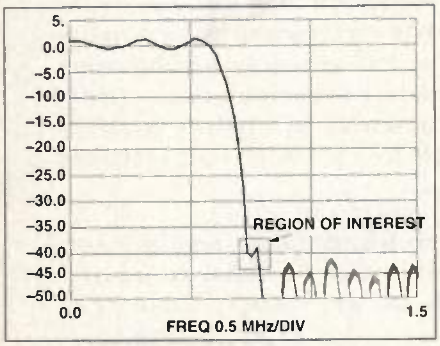

Figure 5. Fixed-point FIR filter frequency responses from four generations of genetic optimization.

using genetic optimization algorithms.

First, the FIR filter coefficients are defined in the simulation schematic in which the nominal value and the discrete range over which each filter coefficient can be adjusted are given. The coefficient step size specified in the EDA tool is set to 1/2^12 = 1/4096 = 0.000244140625 because we have only 12 bits for fraction representation. In other words, the minimum distance between two values of the coefficient is 1/4096. Because the FIR coefficients are symmetric about the k=23,24 index terms, only 24 filter coefficients are specified for use in the optimization. All the filter coefficients are set to be optimizable, except for the coefficients at k = 23, 24 index, where their values are fixed at 1.0 and must not be adjusted.

In the EDA tool, the desired filter response is specified with three optimization goals. Goal 1 defines the frequency range for the passband region of the filter and the desired level of output from the filter at these frequencies (plus or minus 1.5dB). Goal 1 also is assigned a relative weighting of value 2 to indicate that it is most important to meet this goal. Goal 2 and goal 3 are set up in a similar manner to force the optimizer to meet the IS-95 specifications in the transition band and the stop band of the filter.

Simulation results for the optimized fixed-point design

After the optimizer is put to the task of tweaking the filter coefficients, we come up with four generations of designs. (See Figure 5.) The first generation of optimization does not create a design that meets specification. (See Figure 6.) Further generations are necessary to meet our goals.

After the second generation, the filter coefficients are optimized such that the filter specifications are met for the –40 dB attenuation level This is evident in the enlarged view of the area of interest in Figure 6. At the fourth iteration, the attenuation at 770 kHz is at about –40.8 dB, which is 1.8 dB lower than the unoptimized filter response at 770 kHz. Notice that the genetic optimizer's survival of the fittest algorithm gives an FIR filter design that now meets the IS-95 frequency response specification, only using 12 bits to represent the filter coefficient values. There would have been no way for a designer to use equations or intuitively to adjust the values to bring the response in compliance. By using the power of the genetic optimization tech-

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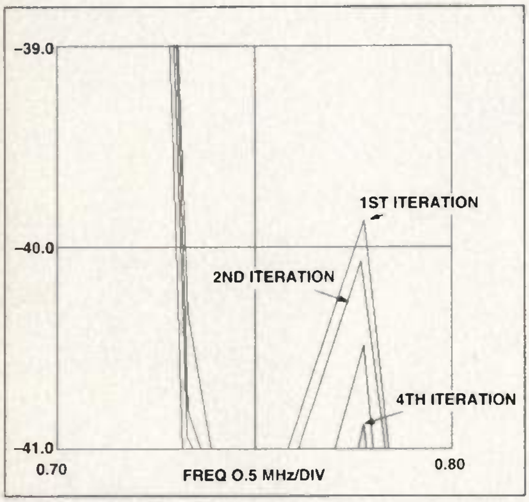

Figure 6. Detail of frequency response of four fixed-point filter designs produced by the genetic optimizer. Each generation of optimization improves filter performance.

niques, a nonintuitive design is created that meets the prescribed goals. Column 4 in Table 1 shows the FIR filter coefficient values derived from the successful genetic optimization process.

Conclusion

Genetic optimization provides an effective tool to help designers of digital filters convert a floating-point filter design to a fixed-point digital filter implementation that uses a minimum number of bits. This novel technique allows filter designers to squeeze out the last bit of performance from a digital signal-processing design, which would not be possible without the help of genetic optimization. Achieving this extra performance from a fixed-point design helps the designer to meet the common design goals of lower cost and lower power designs. And who couldn't use a unique way to make the cost of one's designs cheaper? *RF*

Acknowledgement

Thanks to Victor Soon of HP EEsof for his extensive help with this article.

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Carter Smith is a product manager with Hewlett-Packard EEsof in Westlake Village, CA. He specializes in communications system simulation and DSP. He received a B.S.E.E. in 1986 and an M.S.E.E. in 1990 from California State Polytechnic University, Pomona. His studies in school focused on both RF and DSP. Before joining HP EEsof, Carter worked on a wide variety of projects, including millimeter wave communications systems, baseband signal processors and audio amplifiers.

DSP technology optimizes multi-channel digital receivers

By Toby Haynes

Digital signal processing is rapidly transforming the architecture of wireless communications systems. Although digital technology can provide an elegant design, it is highly dependent on unobstructed data communications among the digital signal processors (DSPs), host central processing unit (CPU) and other portions of the system. Ensuring high data throughput is challenging, but it is being simplified by modular digital receiver architectures.

In their basic forms, analog and digital receivers are nearly identical in that they capture the incoming RF signals the same way. Rather than using an analog demodulator, the digital receiver uses an analog-to-digital converter (ADC) and DSP to downconvert and process the signal.

Digital filtering replaces analog hardware filtering traditionally accomplished by surface acoustic wave (SAW), ceramic or crystal filters. Filtering options are limitless. Performance of even basic digital filters can be as good as the best analog filters, and fewer components are required to achieve it.

Digital drop receivers

To provide high levels of functional integration and to simplify digital receiver design, manufacturers have produced chip sets that, together, form a subsystem called a *digital drop receiver* (DDR) or *digital tuner*.

The DDR is a dedicated signal-processing system that rejects unwanted signals, selects the signals of interest and reduces their data rate (called *decimation*) to baseband so that they may be processed effectively by DSPs. In addition, the DDR uses sophisticated digital filtering that avoids the use of complex analog filter components. The ability to provide filtering digitally makes it easier to provide a certain set of filter characteristics that do not change over time.

Like all digital designs, filters require no adjustment or tweaking to achieve the desired level of performance. This provides significant benefits in component cost, design, manufacturing and test time, which increases production throughput.

Digital downconversion

In current digital receiver designs, the ADC digitizes the intermediate frequency (IF) signal and passes it to DSPs for channel filtering and demodulation. In such a system, the IF bandwidth is limited by the available DSP processing power. Undersampling of the IF commonly is used to keep the sample rate low enough so that DSPs can keep up.

By using digital downconversion ahead of the DSPs, a single processor needs to handle only a fraction of the total IF bandwidth. With this approach, a narrow bandwidth from the digitized 30 MHz-wide IF is extracted by the digital downconverter, which then delivers to the DSP a baseband version at greatly reduced sample rates. The DSP software implements filtering and demodulation of the small number of radio channels within the downconverted bandwidth. By using multiple digital downconverters and DSPs, numerous channels can be received simultaneously from a single digitized IF.

In addition to its obvious benefits, digital downconversion provides exceptional frequency control—down to a fraction of a hertz—and accomplishes frequency changes within a few sample clock cycles. Digital downconversion also has excellent noise performance and allows any bandwidth to be selected through digital filtering without negatively affecting group delay. The in-phase (I) and quadrature (Q) relationship of the complex baseband data stream can be maintained to exactly 90° through these digital techniques.

Digital receiver architectures

There are many ways to configure digital receivers. They almost invariably rely on a building-block approach, the configuration of which depends on the digital signal processing devices chosen. A multichannel, narrowband receiver architecture reflects this approach. It consists of three TIM-40 modules that can be combined in various ways to produce a bus-independent DDR.

Analog input module

The first module in the set digitizes a 3 kHz-to-30 MHz IF signal delivered via a 50 Ω coaxial cable. (See Figure 2.)

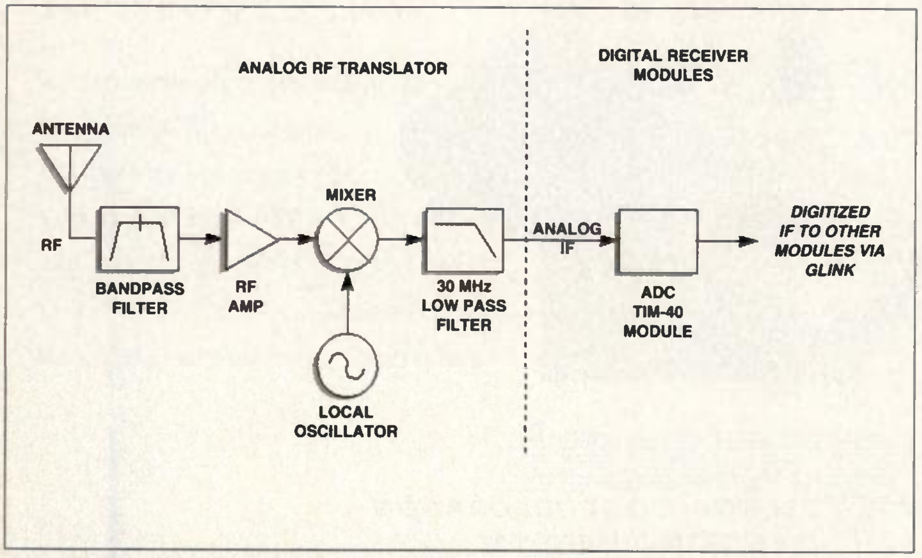

Figure 1. Block diagram showing where analog components end and digital ones begin.

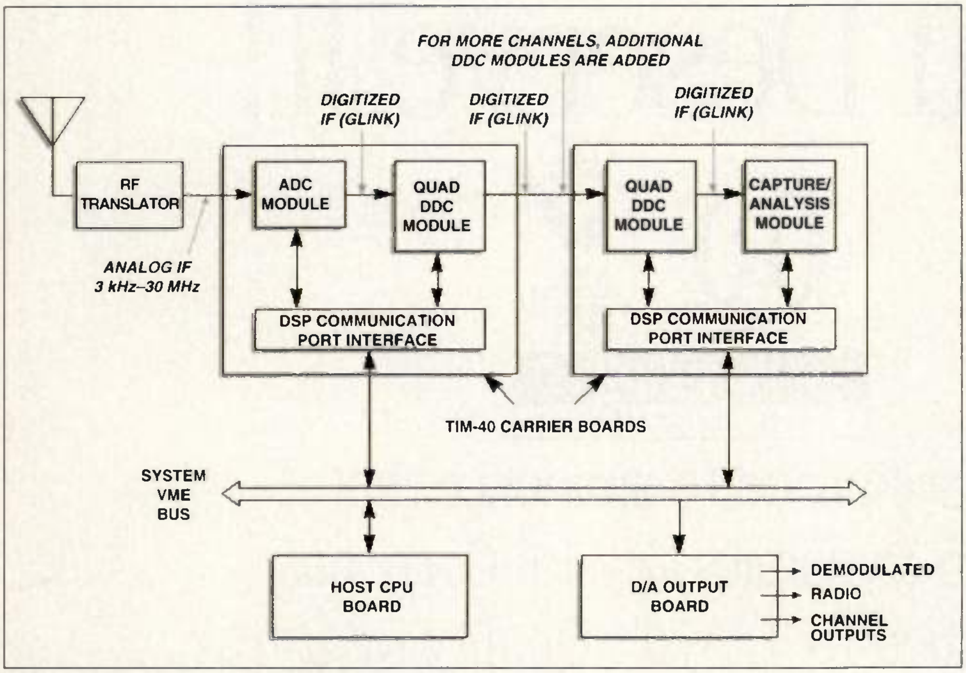

Figure 2. A receiver using digital downconversion.

By digitizing signals closer to the antenna (either the entire 30 MHz HF band, or a 30 MHz IF portion of the band of interest), a traditionally fixed-function analog stage of the radio receiver is brought under software control. Such programmable soft radio designs require not only fewer millions of insturctions per second (MIPS) of processing power than previous technology approaches, but also provide flexibility in support of changing end-user needs.

The IF signal comes from an RF translator that uses conventional analog circuits (local oscillator, mixer and filters) to convert UHF or microwave RF signals from the antenna to frequencies lower than 30 MHz. The IF signal is filtered, and gain control is applied. A clipping monitor detects when the input voltage exceeds a threshold of 72% of full scale (2Vpp), and adds the number of threshold crossings to the 16-bit counter.

The counter is reset and read with a C4x communication port from another module (TIM-40 communications port 1). The C4x then determines the amount of attenuation necessary on the input signal and adjusts the gain controller in 2 dB steps within a 30 dB range. The ADC then samples the conditioned IF signal as high as 70 megasamples per second with 10-bit resolution. The IF signal, now digital, is communicated to other modules over a high-speed (1.4 Gb/s) serial bus called GLink.

GLink serial bus

The A/D data are distributed from the first module to the next using Glink and so forth to create a network of DDCs. The GLink transmitter is capable of transmitting data as far as 6 feet on a 50 Ω coaxial cable. A programmable DDC sync signal is transmitted on GLink to reset each digital down converter module on the GLink network for coherent DDC processing.

Digital downconverter modules

The next module in the system accepts the digitized wideband IF from the ADC module and simultaneously tunes, downconverts and processes four narrowband channels. The downconversion module consists of a double-width TIM-40 module with four Harris HSP50016 digital downconverter chips and two Texas Instruments TMS320C44 DSPs. Two DDCs are controlled by one C44 Global bus, and the other two are controlled by the other C44 global bus. There are also two GLink transmitters and two GLink receivers on the module, which allow the downconverter to receive and retransmit the digitized IF to other down converter modules in the system.

The HSP50016 accepts samples as high as 70 megasamples per second with 16-bit resolution. Input samples are multiplied by a complex sinusoid at a frequency that is programmable from DC to half the input sample frequency. The output is a lowpass-filtered, decimated signal with identical real filters for the I and Q signal components.

Lowpass filtering is performed by a programmable, high-decimation digital filter followed by a finite impulse response (FIR) filter with a fixed decimation rate. Bandwidth selectivity ranges from 507 kHz to 294 Hz, based on an input sample rate of 70 megasamples per second. The output of the downconverter is either a real data stream or a complex quadrature data stream in serial format that can be demodulated or processed digitally.

Each of the HSP50016 downconverters can be tuned to a narrowband signal within the IF bandwidth. The low-sample-rate quadrature baseband signals from the device are sent to the communication ports of the TMS320C44. The DSPs have 512 Kbytes of static random access memory (SRAM), and can execute demodulation or signal analysis algorithms in real time.

The last module in the system provides fast capture and analysis of the entire digitized IF spectrum. It uses a hardware-controlled, double-buffering scheme that allows the module's GLink receiver to stream the incoming digitized IF to one dynamic random access memory (DRAM) bank at the same time the TMS320C44 processes another bank that previously was loaded. The DSP can search for radio signals or perform other functions on the IF signal and can communicate the results to the host computer or other TIM-40 modules hosting C40 or C44 DSPs with SRAM, DRAM or extended data out dynamic random access memory (EDRAM) through communications ports.

An unlimited number of downconverter modules can be used to sample the digital IF on the GLink bus, each one simultaneously downconverting and processing as many as four channels. Because the downconverter module can retransmit IF signals in daisy-chain fashion, an unlimited number of narrowband channels can be received. The capture and analysis module also can terminate Glink, and receive and process the entire IF spectrum. As a

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result, the three modules together can be configured to form a scaleable signal-processing system flexible enough to accommodate a wide variety of system designs. The DDR suite is applicable to VMEbus, PCI and VXI-based systems because it is implemented on standard TIM-40 mezzanine modules, which may be installed on TIM-40 capable carrier boards for any bus architecture.

Future trends

It is exciting to imagine an almost completely digital radio that accepts signals directly from the antenna without intervening analog components. Unfortunately, this scenario is not yet possible for several reasons. For one thing, an ADC would require a large dynamic range to deal with the immense number of signals with which it would be presented.

In addition, the ADC would require an input bandwidth of 2 GHz or even higher, a feat impossible today. Even if it were possible, unacceptable compromises in receive sensitivity, selectivity and image rejection would still be required. For this reason, the digital components are moved down the signal chain to the IF stages. With far fewer unwanted signals to reject, the ADC is less likely to become saturated, needs less dynamic range and still reduces complexity by eliminating analog components in IF stages.

Conclusion

The DDR approach has two main advantages:

1. The coaxial-based digital broadcast of the digitized RF spectrum can be made available to many DSP and DDC systems simultaneously to allow for handling of multiple channels in real time, thus creating a one-tuner-with-many-signals system.

2. The DSPs are equipped with multiple independent communications ports that allow for inter-processor communications as well as data presentation to the host, concurrent with signal-processing activities.

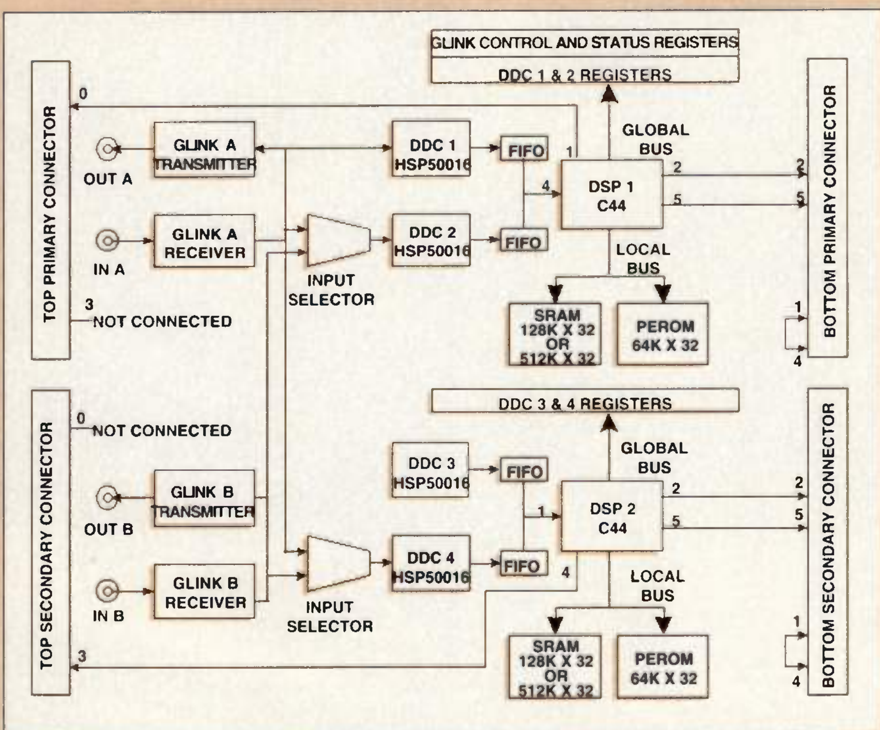
Digital signal processing undoubtedly will play an increasing role in the design of receiver systems for wireless communications. As the number of channels and data rates in wireless services increase, so too will the demand for high-speed DSP architectures to implement them. This demand is likely to be met by highly integrated, modular components that are designed to function optimally together to maintain true real-time signal processing performance. RF

Multiprocessing

One of the keys to achieving real-time signal-processing performance in digital receivers is to harness the power of DSPs in the most effective manner by achieving optimum processor-to-processor communication throughput.

The architectures of some floating-point DSPs are optimized for parallel processing, which facilitates the real-time performance that wireless communication systems require. DSPs designed for scalable parallel processing have multiple high-speed data and memory buses, a number of I/O interfaces and on-chip controllers for inter-processor communication, and instructions that execute in a single cycle. One of the most widely-used DSPs for this application is the TMS320C40 from Texas Instruments. Each of its communication ports operates as much as 20 Mbyte/s, which facilitates uninterrupted inter-processor communication, even when multiple DSPs are used.

Texas Instruments created a system-level specification for multiprocessing modules called TIM-40, which has become the industry standard module architecture for this device. The module contains one or more TMS320C40 DSPs, I/O interfaces and memory, and brings the device's communication ports out to a connector to interface with other modules. The host-to-DSP bus is usually VMEbus, ISA or PCI. TIM-40 modules can be configured in any number to produce the real-time performance required by digital receivers.



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Toby K. Haynes received a B.A.Sc in electrical engineering from the University of British Columbia in 1985. He is a senior technical lead designing DSPs and digital radio hardware for the military, aerospace and commercial (MAC) group of spectrum signal processing. Previously, he designed DSP and VME bus hardware for Motorola's wireless data group. He can be reached at 301-918-2522.

Advances in component integration

By Ernest Worthman
Contributing Editor

Much progress has been made in single-substrate, submicron and deep-submicron manufacturing techniques. As a result, end-user products are cheaper, lighter, smaller and more reliable. However, as with most technological advances, deep submicron component integration has its advantages and disadvantages.

As engineers, designers and manufacturers are painfully aware, competition is stiff, windows of opportunity are short, and cost usually tops the list of priorities. Submicron processes reduce component count, integrate functions, improve reliability and shorten time to market. However, progress in integrating certain functions, such as phase-locked loop (PLL) circuits and oscillators, is slow. Working with submicron designs promises to satisfy the need for speed in the future of high-frequency digital radio.

The idea behind submicron processing is, simply, to get *denser* and *faster*. Many upcoming technologies require spectrum above 1 GHz. (International personal communications services [PCS] start at 1.7 GHz, for example). Building integrated transceiver modules and digital-to-analog converters (DACs) to run at these higher frequencies, without ancillary frequency dividers, oscillators and downconverters, is challenge. Given the option, designers would be happier if they could use RF modules and DACs for front-end processing that work in frequencies used for PCS and keep external components to a minimum. This is one of the promises of submicron component integration. To extend upper frequency limits, new types of substrate and submicron processes are being developed and implemented.

The technology

For example, manufacturing a 2,000-gate submicron chip for 25 MHz is fairly simple. However, gigahertz submicron circuits are only now coming to market. Additionally, certain substrate growth techniques, such as molecular beam epitaxy (MBE), metalorganic vapor phase epitaxy (MVPE) and chemical beam epitaxy (CBE), which promise to offer 0.1 μm gate lengths and state-of-the-art f_T as high as 220 GHz, are still in the experimental stages. More realistically, today manufacturers have successfully designed and are making submicron components with f_T of about 15 GHz.

The complexities of deep-submicron process technologies require not only analysis of designed-in lumped electrical devices (active and passive components), but also analysis of resultant incidental distributed elements (stray reactance, parasitics and interconnect line issues).

The industry likes to use the 0.6 μm transistor gate length as the defining edge for deep submicron. In reality, this attribute really is only one of several that define this process and that affect the lumped and distributed elements.

In many cases, chip performance largely depends on the interconnect architecture, rather than the gate length. In fact, one manufacturer's 0.6 μm process may not perform better than another manufacturer's 0.45 μm process. The best configuration is a full 0.35 μm process and a hybrid that uses 0.5 μm gates with metal interconnect. The latter really is more equivalent to a 0.6–0.7 μm full process because of the interconnect.

The ultimate result of submicron processing is really the result of four factors; *power consumption, interconnect delays, component density* and *device geometry*.

In recent years, when geometries larger than 1.0 μm were prevalent, most of the capacitance encountered was caused by the attached gates. Generally, metal interconnect resistance was not an issue. However, at gate lengths of less than 0.5 μm, it turns out that metal interconnect is responsible for most of the capacitance, mainly because smaller transistors have faster switching times, causing less capacitive loading.

Today, interconnect has become the predominant cause of propagation delay in deep-submicron designs. As process technology is scaled downward, it becomes the unfortunate recipient of some interesting phenomena. On one hand, smaller geometries mean smaller metal lines, which reduces capacitance for a given length of wire. But as wire diameter shrinks, its resistance increases. To compensate, the wire is made thicker vertically than horizontally. This tends to increase capacitance. So, as one issue gets resolved another surfaces. Designers constantly grapple with issues such as the resistance-capacitance merry-go-round. Additionally, although scaling seems to hold true for propagation delays as the process drops below 1.0 μum, there is some question as to whether it will be the same as the scaling approaches the 0.25 μm dimension.

To muddy the waters even further interconnect length also depends upon overall die size, which does not shrink proportionately, if at all. This is because designers often have the size as a constant, or relative to packing functions. Therefore, designers strive to increase the density of components on the die thereby increasing functionality.

When all is finally analyzed, the averaging effect of these "sum of the parts" tends to be greater than the whole, and still produces devices that behave differently than the models often indicate. Designers have made significant advances in the deep submicron process and have compensated for many of the unique problems that deep-submicron manufacturing presents.

For example, experiments are being done at the University of Michigan using InAlAs/INGaAs HEMTs grown on MBE, MOVPE and DBE substrates that have achieved f_T of 220 GHz, using 0.1 um T-gate technology and strained channel In, Al, AS/In, and GaAs HEMTs. Other experimental sites have indicated they have achieved f_T of as high as 330 GHz and beyond. So, significant progress is being made. More

information about these experiments can be obtained by contacting the University of Michigan Electrical Engineering Department or this author.

The good, the bad, and the yet to be defined

Submicron and deep-submicron technologies can do much to improve time to market, yet they are not capable of providing one-chip solutions to all design problems. Even state-of-the-art devices leave a few components out. On the plus side, taking a bit deeper look at this device shows what kind of tolerances can be achieved with submicron processes and single-chip design. For example, one stage of the chip integrates the mixer with a low-noise amplifier (LNA). Because it is fabricated using submicron technology, it has a noise figure of only 6 or 7 dB, which provides a nice, clean mixer stage.

The reason for these nagging problems is simply that certain components do not allow for easy fabrication on silicon substrates. For example, many of today's transceivers use the tunable RF oscillator's varactor diode as the tuning element. Integrating a varactor diode into silicon is not easily done because of the processing and materials needed to manufacture the diode. Varactor diode materials and the processing method are fundamentally incompatible with CMOS and BiCMOS. Additionally, parasitic capacitances exist in such an arrangement, and it requires additional trimming capacitors to bring it into the varactor diode's tuning range.

An earlier solution to this dilemma was to look at ring-oscillators. These devices are CMOS-compatible but dirty with phase noise. Because phase noise is a function of power, reducing phase noise to the level of conventional LC circuits requires extremely high power dissipation capabilities within this type of oscillator. Typically, these designs are limited to RF sections that do not demand processing at extremely low signal levels.

The best solution is to develop a new approach to building a tunable LC circuit that is CMOS compatible and monolithic integration friendly. A recent paper I came across at a web site at UC Berkeley (http://kowloon.eecs berkeley.edu/~boser/vco.html) suggests integrating a tunable LC circuit with micromachined parallel plate capacitors replacing the varactor diode as the tuning element. A condensed excerpt of the implementation is at the end of this article.

Designers face a few other bottlenecks. One is *signal isolation* among the substrate, supply lines and the package itself. Another problem signal isolation between blocks. Typical designs provide only 60–70 dB of isolation, not enough for sensitive RF front-end components.

Another issue is *power*. All things being equal, the higher the speed of the device, the more power it requires ($P = C(V^2F)$, C = load capacitance seen at the output, V = voltage and F = frequency) Power dissipated is a function of I^2R and this occurs on both load and parasitic elements. In deep-submicron technology, circuit parasitics are a significant factor in both power requirements and dissipation. In theory, the current voltage-resistance curve has instantaneous properties. If this were true exact power limits can be determined and the device would function as designed. (Remember to an engineer $e=mc^2 \pm 10\%$.) However, no devices switch in zero time, and all devices have overshoot and settling characteristics must be recognized. In submicron design, parasitic power sinks can have a significant effect on the circuit's performance. Additionally, pad capacitance bond wire and lead inductance significantly alter the real-world instantaneous and RMS voltage-current relationships. The current trend is to reduce the operating voltages of the devices thereby reducing power dissipation which, in turn allows an increase in frequency within the given parameters.

A third issue that beleaguers designers is *clock speeds*. It seems that around 250 MHz speeds and 5 million gates there is sort of a magic figure for releasing the gremlins. In the early days with longer clock pulses and fewer timing objects, it was pretty easy to disregard propagation delay. In today's deep submicron, high-density devices, getting the clock to show up at all the right places (called *skew*) at the right time can become a formidable task. A related issue is sufficient clock drive, or power to operate all of the devices correctly. A 2 GHz clock has a 0.5 ns pulse. Tha includes rise and fall times and settling time. Bump that up to 200 GHz, and the pulse width is...well, you do the math. Additional issues are that if the signal is properly propagated, and if all of the devices switch simultaneously, huge power demands and spikes can be generated. Buffering is often used to overcome delay problems, but it adds stages that add parasitics. Parasitics and other unwanted elements that come with buffering usually load the system. For deep-submicron circuits to operate properly, it is imperative that signals propagate cleanly, that pipeline lengths are optimized and that load balancing is implemented. The fact is that some of these parameters are bumping up against the limits of the best physics and technology currently available.

A final concern is the size of the transistor. The smaller the transistor, the better the performance. However, there is sure to be a limit to how small the transistor can be made and still function according to traditional design characteristics.

A step forward

Although deep-submicron technology is indeed an element paving the way for the next generation of high-speed, high-tech devices, many problems remain to be solved. With each new evolution come growing pains. Sometimes the promise of smaller, faster and lighter blurs the objective, which may not really require everything that is on the plate. Because some of the problems currently surrounding deep-submicron technology (and I've only touched on a few), a hybrid of technologies may develop, as is often the case, before the technology matures.

Another promising technology that is being combined with submicron is low-temperature, co-fired ceramics (LTCC). LTCC technology is used specifically to integrate other components such as the power amplifier, processor, passives and even the antenna, with the IC technology. Look for more about LTCC in an upcoming issue that covers semiconductor material.

*http://kowloon.eecs.berkeley.edu/~boser/vco.html information

The capacitors consist of a 1.0 μm thick aluminum layer deposited on a 1.5 um thick sacrificial layer. Aluminum has been chosen rather than polysilicon for its lower resistance, which is required to achieve a quality factor Q=20 at 1.0 GHz. This technology has the additional advantages of a negligible thermal budget and full compatibility with the aluminum interconnect structure of conventional IC technology. This is a key feature of the technology, because it eliminates the need for a special IC process. It is thus possible to always use the most advanced technology for the electronic circuitry, a critical requirement for RF design, and to fabricate the tunable tank on top of the completed electronics. RF

References

LTCC technology is a process used by National Semiconductor.

A new discourse on crystal oscillator basics

By Waitak P. Lee, Ph.D.

Circuit designers with little experience with crystal oscillator circuits will find three aspects of designing crystal oscillators to be important. The first is the piezoelectric effect in relationship to the crystal models. The second is the basics of oscillator circuits. The third aspect includes actual design examples, including circuit simulation. The results of the circuit simulation are interpreted to explain what to look for in the simulation. With a clear understanding of the crystal models and with the design examples, circuit designers should be able to initiate their own crystal oscillator design.

Crystal oscillator circuits provide the heartbeats for the integrated circuits (ICs) of modern electronic systems. Initially, crystal oscillators were used mainly as frequency standards or references. The importance and widespread use of the crystals started with the advent of microprocessors or computer systems. There are two principle reasons why the crystal oscillators are needed for the computers:

1. As a stable clock frequency.
2. As a frequency standard for wireless communication.

Usually, the computer chips operate at their maximum clock frequencies. When chips are operated at such high frequencies, and if the clock frequency is set higher than the chip's maximum frequency by as little as 5%, the computer chips may not work properly. Computers usually have *time* and *calendar* functions that are provided by the low-frequency *watch crystals*. Crystal oscillators are also needed to provide accurate frequencies to within 1 ppm for wireless digital communication and for Global Positioning System (GPS) equipment.

Piezoelectric effects and crystal models

There are few good explanations of the crystal *equivalent circuit model* in relationship to piezoelectric effects. Piezoelectric materials have the following properties:

1. If the material is strained with a mechanical force, the material will produce surface charges.
2. If an electric field is applied to the material, the material will be strained by the field and subsequently produce surface charges.

Thus, a piezoelectric material will produce surface charges if it is strained by either an electrical force or a mechanical force. Because the operation of the crystal oscillator circuit depends on this effect, and because different materials have different piezoelectric constants, intuitively one can conclude that the larger the piezoelectric constant, the easier it is to start the oscillation.

A crystal is made by inserting a piezoelectric material, e.g., quartz, into a capacitor structure. The capacitor sets up an electric field according to the applied voltage. The electric field strains the crystal and induces surface charges. This crystal can now be thought of as a regular capacitor with two components of capacitance:

$$C_{total} = C_o + C_p \tag{1}$$

where C_o is the regular dielectric capacitance or shunt capacitance of the crystal and C_p is the capacitance due to piezoelectric effect.

Equation 1 can also be expressed as:

$$C_{total} = C_o(1 + K^2) \tag{2}$$

where K^2 is the piezoelectric coupling ratio.

For a given piezoelectric material, the piezoelectric capacitance is proportional to the regular dielectric capacitance C_o, which represents the effect of the capacitor structure.

Now, let us turn to the simple equivalent circuit model shown in Figure 1. This circuit model schematic is often presented in crystal data books. The circuit model consists of a capacitor C_o in parallel with a series inductor-capacitor (LC) resonator. One can identify the shunt capacitance as the C_o of Equation 1, and the C_1 is only a part of the C_p of Equation 1. The L_1 and R_1 need to be determined separately. This model is adequate for most simulation purposes if the model parameters are measured accurately. To simulate third or higher overtone modes, one needs to use the complete LC equivalent circuit model shown in Figure 2. This model shows a shunt capacitor C_o in parallel with series LC resonators. Each resonator represents a frequency mode. From this complete circuit model, the piezoelectric capacitance is the sum of the capacitance of each of the resonators; therefore:

$$C_p = C_1 + C_3 + C_5 + C_7 + C_9 + \ldots \tag{3}$$

All the inductors are identical, and the inductance is a constant; thus:

$$L = L_1 = L_3 = L_5 = L_7 = \text{constant} \tag{4}$$

The result of Equation 4 is that the C_n varies as $1/n^2$; thus:

$$C_n = C_1/n^2 \tag{5}$$

Consequently:

$$C_p = \Sigma\, C_n = \Sigma\, C_1/n^2 = (\pi)^2\, C_1/8 \tag{6}$$

The values of C_n are well-defined and are related to the piezoelectric effect. The often-used term, *motion capacitance*, is misleading. It should instead be called *piezoelectric capacitance*. This explains how the crystal model is related to the piezoelectric effect in the static condition.

A new crystal model explains the

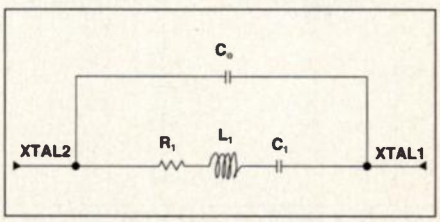


Figure 1. Crystal equivalent circuit model.

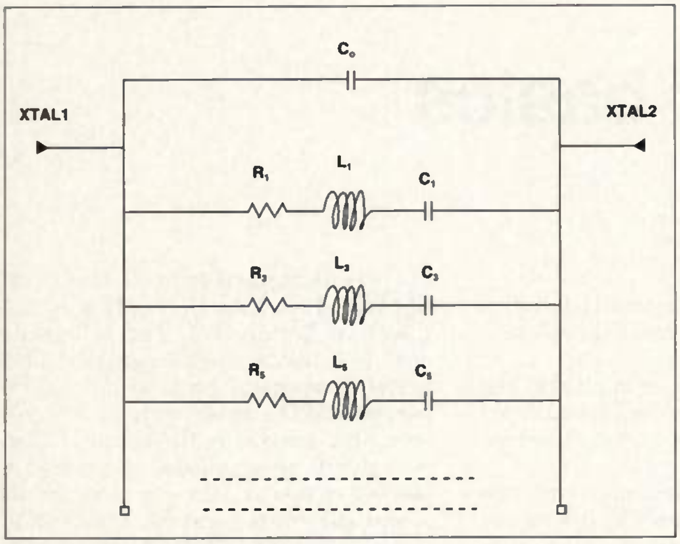


Figure 2. Complete LC ciruit model.

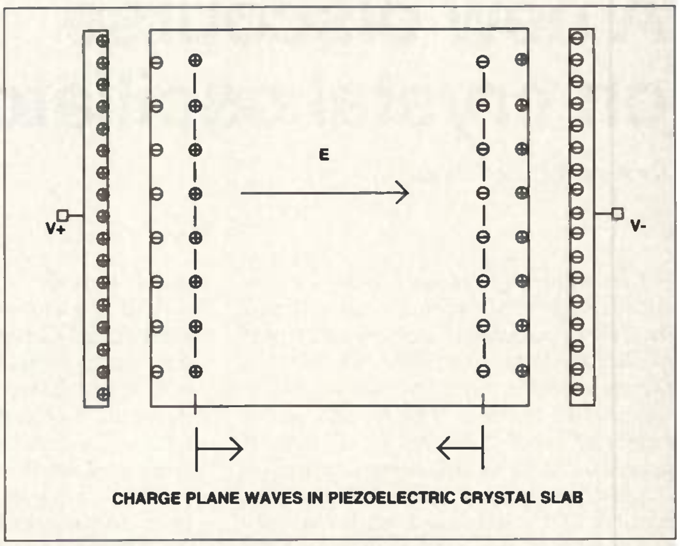


Figure 3. Dynamic behavior of a piezoelectric circuit.

piezoelectric effect under the dynamic condition [1]. This new model is demonstrated to be equivalent to the complete LC equivalent circuit model shown in Figure 2. The new model uses a transmission line instead of LC to model the crystal. The equivalency between the LC model and the transmission line model is known [2].

Consider what happens to a piezoelectric crystal when a voltage is applied across the crystal terminals. A uniform electric field is set up, and the quartz crystal is strained. The crystal is a lattice and consists of many layers. At the instant the field is applied, only the outermost layers on both faces of the crystal can respond mechanically and are strained, because of the stress-free boundary conditions. The result is depicted in Figure 3. On each outer layer of the piezoelectric material, positive and negative surface (or plane) charges are produced. Later, the inner second layers are strained, and they produce both the positive and negative plane charges, too. Dynamically, the sequential straining of more crystal layers produces two acoustic or lattice wave fronts propagating from both sides of the crystal and toward each other. The wave fronts are the strained lattice waves, and they have charges coupled with them. Electrically, one can think of the waves as *charge plane waves*. Moving charges produce electrical current. One can immediately relate this to a transmission line. When the same voltage is applied to both ends of a transmission line, two wave fronts are generated.

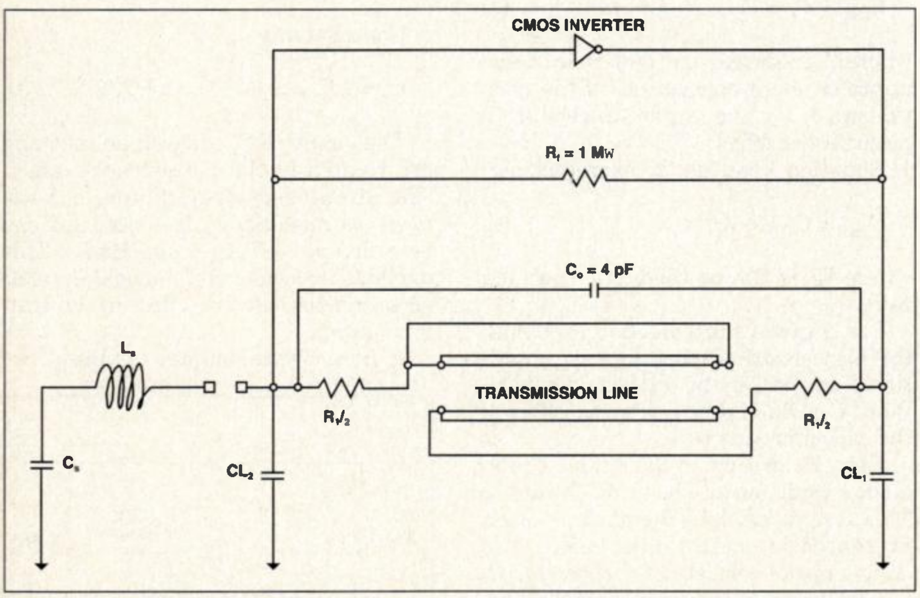


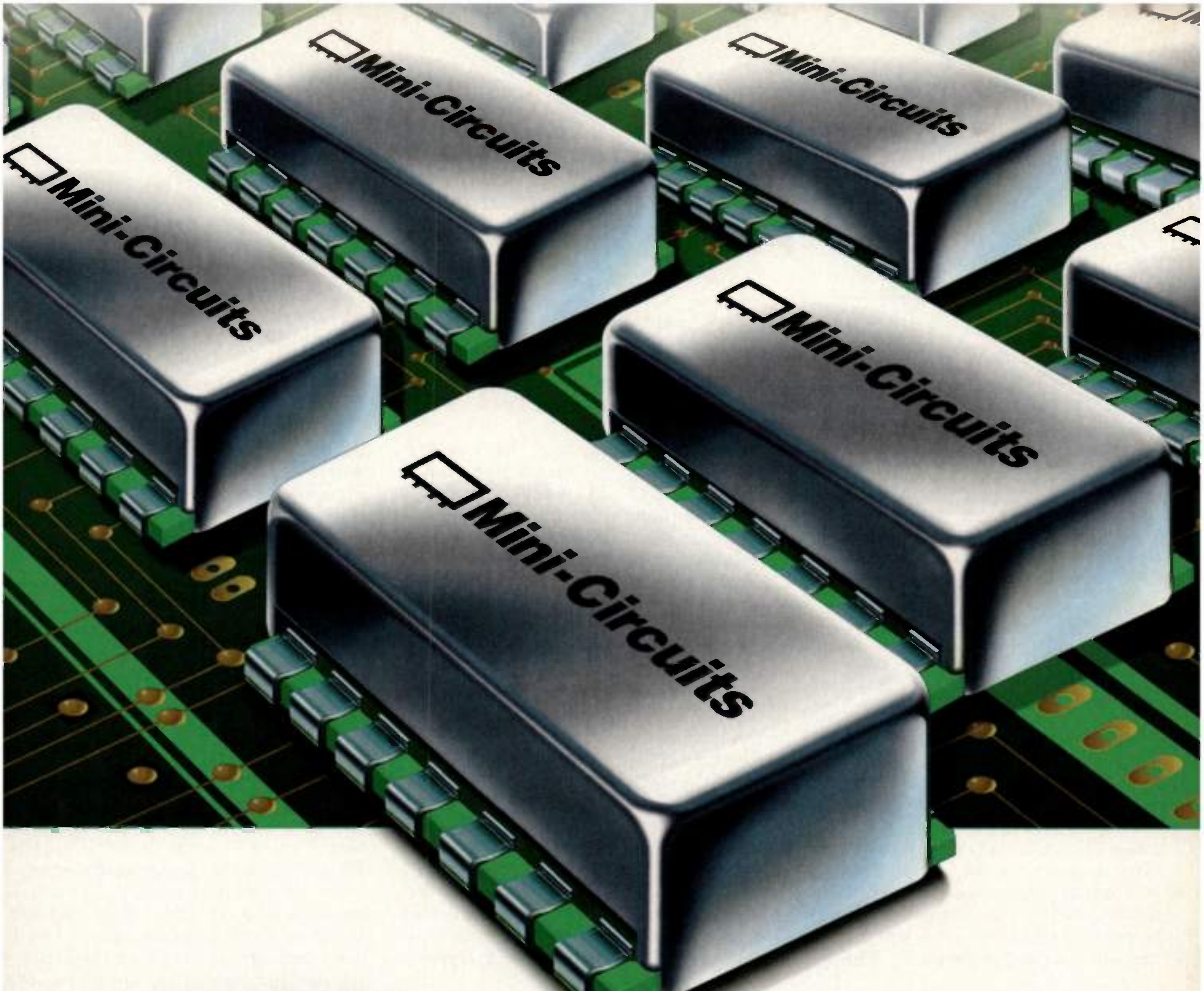
Figure 4. Transmit line oscillator circuit.

The new crystal model, shown in Figure 4, is an oscillator circuit with the transmission line as the resonator. A capacitor is added to account for the shunt capacitance, and two resistors are added for the crystal losses. The parameters for the transmission line can be derived from the crystal's piezoelectric capacitance. It is sufficient to say that, for the transmission line model, the characteristic impedance Z_o is given by:

$$Z_o = \Delta t / C_p \tag{7}$$

where Δt is the delay time of the transmission line, and C_p is the same piezoelectric capacitance.

The delay time is determined from the crystal frequency. If the frequency is 10 MHz, then the delay time is 50 ns. Note that the crystal or the transmission line provides a 180° phase shift, which is half of the period, and thus, a 50 ns delay. Simulations with the transmission line models are demonstrated [1, 2]. Again, the transmission line model is the exact equivalent to the complete LC circuit model. Transmis-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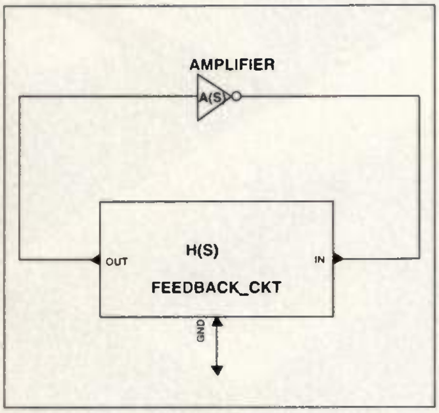


Figure 5. Typical oscillator circuit.

sion lines or coaxials are used as resonators in RF circuits [3].

Measurement method

For measuring the crystal model parameters, use the complete LC equivalent circuit. Furthermore, L and C can be measured directly with an impedance analyzer or a network analyzer. One does not really need a crystal tester [4]. In the LC model, the inductance L is a constant, and the various overtone frequencies are known. What remains to be measured are the capacitances, the sum of which is equal to the piezoelectric capacitance C_p. The net capacitance seen by the impedance analyzer at any measurement frequency is given by:

$$C = C_{total} + C_1/(1 - \omega^2/\omega_1^2) + C_3/(1 - \omega^2/\omega_3^2) + \ldots \quad (8)$$

where ω is the measurement frequency and ω_n represents the various overtone frequencies.

This equation can be readily obtained from the circuit impedance equation of the LC model. All the L_n are eliminated and replaced with ω_n. Equation 8 can be further simplified by substituting C_n with C_1 and ω_n with ω_1. Then Equation 8 has two unknowns, C_o and C_1, and one known, ω_1, as a function of the measurement frequency, ω. C_o is equal to C of Equation 8 at low frequencies. C_1 can be measured by setting the ω around ω_1. From Equation 5, one needs only to measure C_1 for the fundamental mode, which can be used to calculate all other C_n adequately. With C_1, one can calculate $C_p = C_1(\pi)^2/8$, and one can also obtain the transmission line model parameters. For typical quartz crystals, $C_1 \sim C_o/200$ [4]. When the C_o is less than 2 pF, a significant part of the C_o can come from the stray capacitance, other than the dielectric capacitance. The ratio can drop to 1/300. For the watch crystal, the ratio can be as low as 1/500.

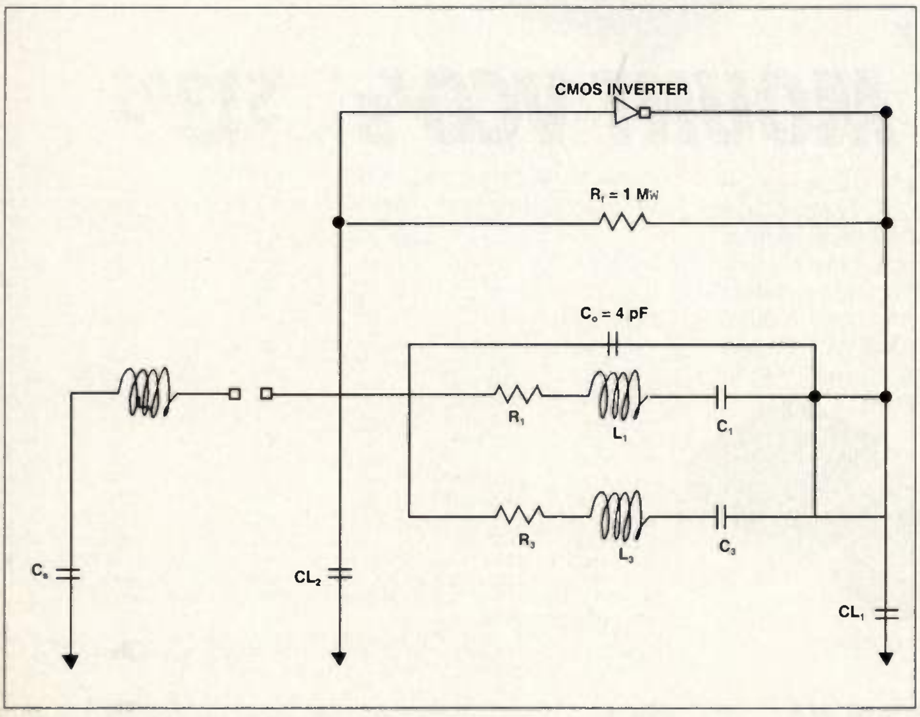


Figure 6. LC oscillator circuit for simulation.

Oscillator circuits

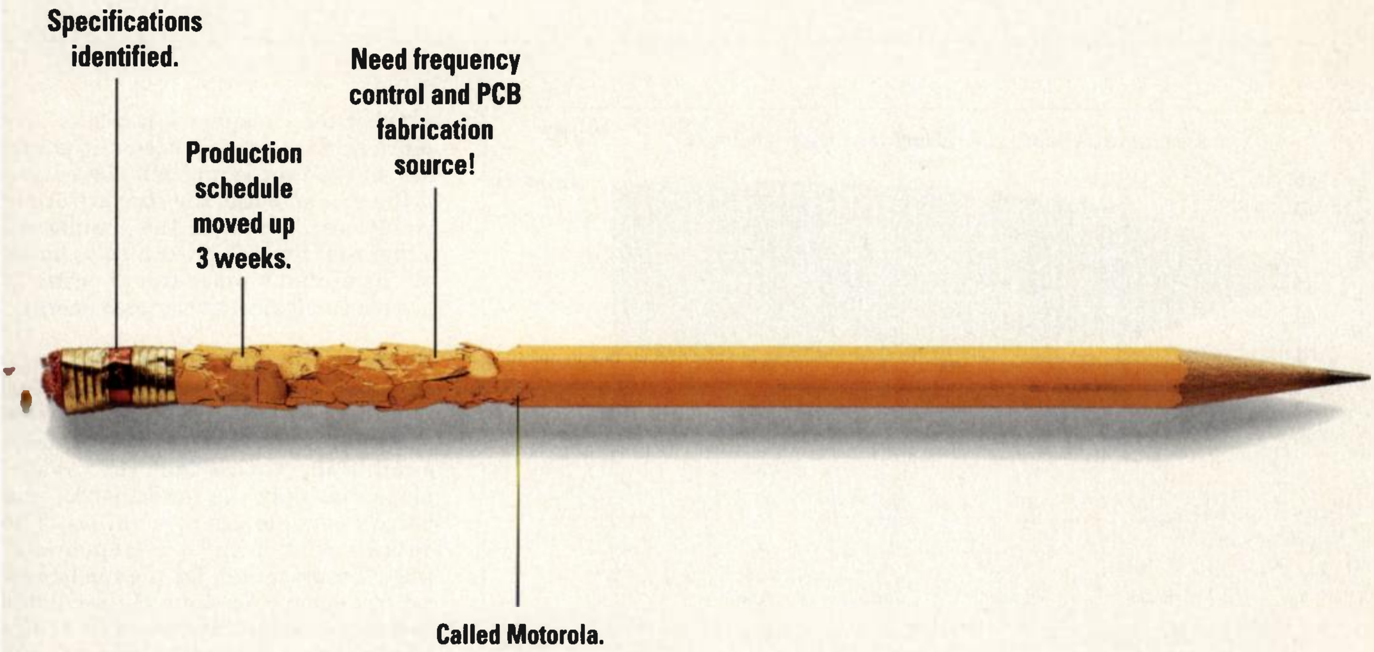
Circuits usually have input signals and output signals. Oscillator circuits can produce output signals without any external input signals. In oscillator circuits, part of the output signals must be fed back to the circuits as inputs. The simple oscillator circuit is shown as an amplifier with a L , R and C network as the feedback circuit. (See Figure 5.) The necessary conditions for the circuit to oscillate are

1. The closed loop gain is greater than one.
2. The total phase shift through the loop is n × 360°.

The amplifier usually has gain greater than one. If it is an inverting amplifier, it also provides a single 180° phase shift. The rest of the circuit has to provide m × 180°, where m is an odd number.

If the feedback network were replaced by a crystal, one would have a crystal oscillator circuit. The closest to this ideal oscillator is the Pierce oscillator. Figure 4 is an example of the Pierce oscillator. Imagine if a crystal were put back in, replacing the transmission line circuit model. The odd number of 180° phase shifts would come from the crystal. From the transmission line model, we know that the crystal is like a delay line with a delay time Δt, as given in Equation 7. For the fundamental mode, the Δt is translated into a 180° phase shift at the resonant frequency. That is why the oscillator oscillates at the frequency of the crystal. For third overtone mode, Δt is the same, but the frequency is three times higher. Thus, the same Δt provides 3 × 180°, and the total phase shift is 3 × 180° + 180° = 2 × 360°, meeting the second oscillation criterion.

Small-signal analysis is used to calculate the closed-loop gain and phase shift. The two criteria are merely the necessary conditions, but not the sufficient conditions to guarantee that the oscillation will start. Circuits meeting these criteria may not oscillate at all. Circuit designers must understand that small-signal analysis calculates the steady-state response of the circuit over a range of frequencies. Oscillation start or oscillation build-up is a transient behavior. The circuit starts from no oscillation, starts oscillating, and finally reaches steady-state oscillation. If circuit designers want to determine



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whether the circuits will oscillate, they must perform transient circuit analyses. In the transient circuit simulation, if there is no noise, the circuit will not go into oscillation. In the simulation, either the circuit is given a noise pulse, or the circuit's resonator is initially given a small amount of stored energy.

Spice circuit simulation

Knowing some details of SPICE simulations can be helpful [5]. Figure 6 shows the crystal oscillator circuit to be simulated. Notice that the crystal model has only the fundamental and third-overtone LC resonators. The entire circuit includes a trap circuit, the LC tank circuit, for the fundamental frequency. Whether the oscillator oscillates at the fundamental or the third overtone depends on this trap circuit. To run the oscillator at the fundamental frequency, the trap circuit must be removed. For simplicity, we can also remove the third-overtone resonator when we run a simulation at the fundamental frequency. The crystal is then represented by the simple equivalent circuit model shown in Figure 1. The SPICE simulation setup is shown in Table 1. (Note that the trap circuit L

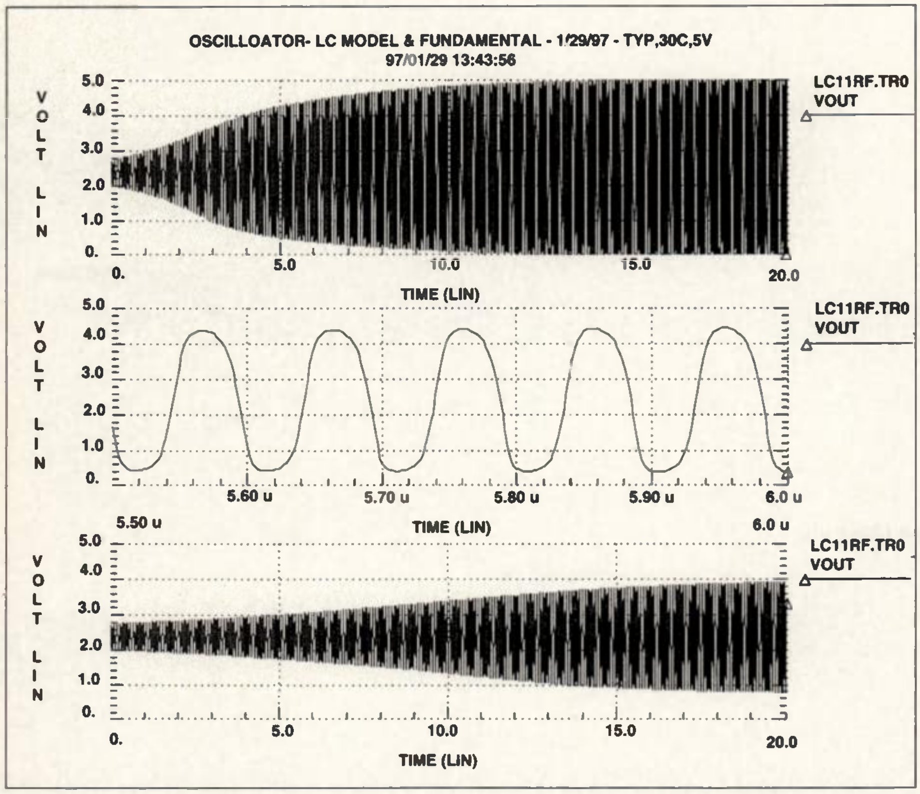

Figure 7. Fundamental oscillation reults. a) V_{out} of the complete simulation. b) expanded V_{out}. c) the effect of R_1 on V_{out}.

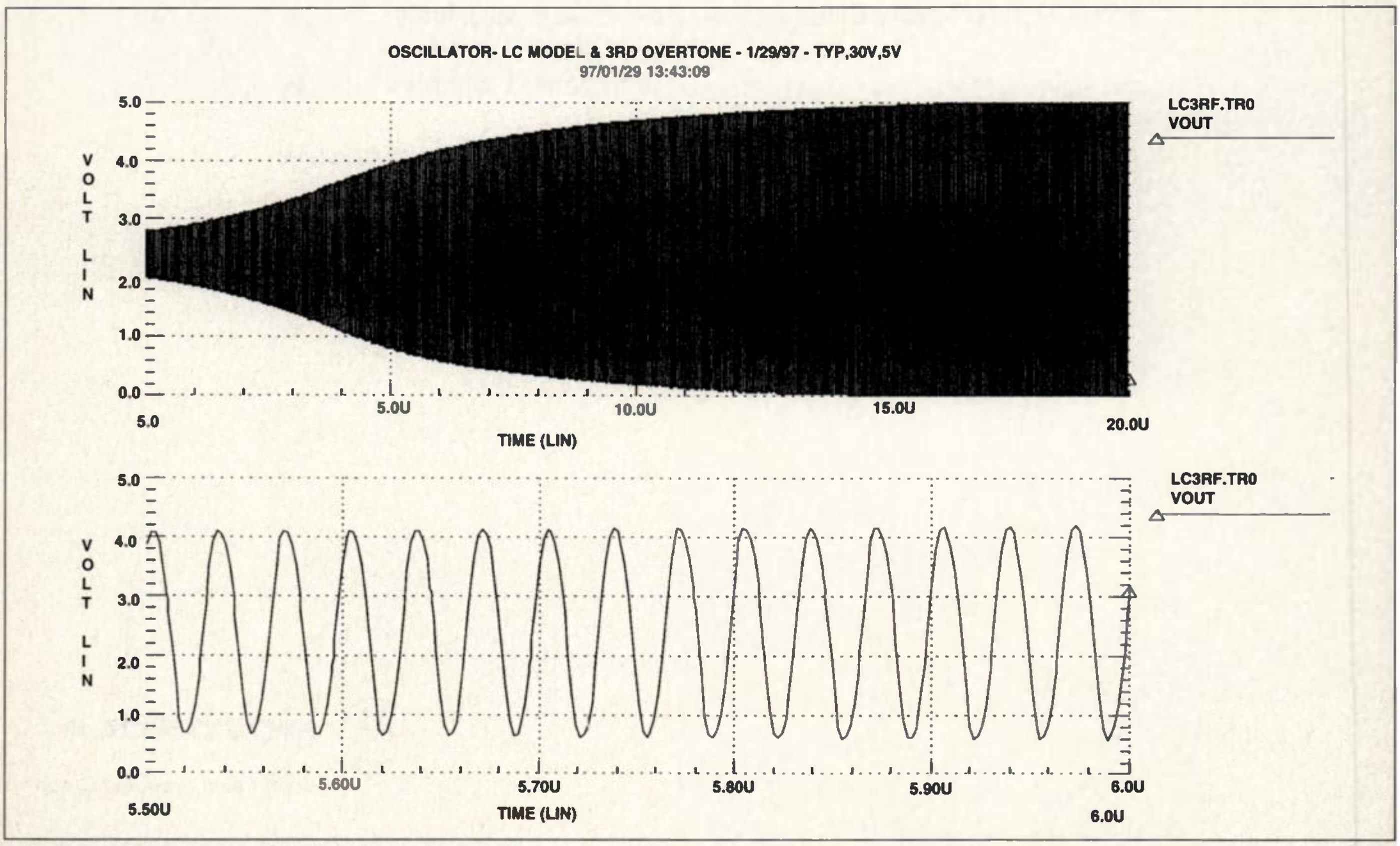

Figure 8. Third overtone oscillation results.

and C and the third-overtone resonator are commented out from the simulation.)

The SPICE simulation uses parameters of a hypothetical crystal. These parameters represent a larger-than-usual piezoelectric capacitance, C_p. The piezoelectric capacitance ratio is 0.16 (vs. some ceramic materials ranging from 0.1 to 0.15), and the ratio for quartz is about 0.006. The larger the ratio, the easier it is to observe oscillation. From the C_p, C_1 and C_3 are calculated. L is calculated from the C_1 and the crystal frequency, which is 10 MHz. To start oscillation in the circuit, capacitors C_1 and C_o are given some initial voltages. The voltages are of opposite polarities and are in a ratio corresponding to the ratio of C_1 and C_o. The voltage in C_1 excites the fundamental frequency resonator, and the voltage in C_o balances out any DC offset caused by the initial voltage in C_1. The initial voltages can be set to different voltages so that the oscillator circuit can be set to any stages of the oscillation.

The simulation results are shown in Figure 7. The top two traces are of the same signal, V_{out}, but with different time scales. Initially, the oscillation growth is exponential. The rate of oscillation growth depends on the total loop gain. An increase in the initial voltages in C_1 and C_o is equivalent to starting the simulation at a later stage of the oscillation. The middle trace shows that the oscillator is running at about a 100 nsec period or at a frequency of 10 MHz. If one uses a quartz crystal instead of this hypothetical crystal, the simulation run must be 10 or 20 times longer to see any growth in the oscillation. Usually, it takes about 50 msec for a crystal oscillator circuit to achieve steady oscillation. A 200 μsec simulation is only about 1/25 of the oscillation buildup time. The circuit will oscillate as long as there is a slow increase of the oscillation.

In the simulation, one can artificially vary circuit parameters to determine which one will affect the oscillation. A feedback resistor, which is too small, will lower the gain of the amplifier. However, if the resistor is too big, it will take a long time after power is turned on before the circuit is biased in the active region. This affects the oscillator start time. The shunt capacitance C_o is essentially parasitic, but one still can remove it from the simulation [5]. Removing the shunt capacitance helps the oscillation to start. If one uses CMOS transistors, the larger the transistors, the larger the gate capacitance. This results in the same detrimental effect on the amplifier gain as the C_o.

Reducing the load capacitance from the specific value also aids the oscillation buildup. As the load capacitance becomes small, the converse is true. The explanation is that the load capacitances at the Xtal_IN and C_o both act as a voltage divider of the negative feedback circuit. When the load capacitance gets too small, or when C_o gets too big, together they reduce the gain of the amplifier. One can also vary the

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capacitance of C_1, but L_1 needs to be adjusted accordingly to keep the frequency the same. The larger the piezoelectric capacitance, the easier the circuit will oscillate.

One most important simulation of the oscillator circuit is to vary the crystal loss, R_1. One can increase R_1 until the oscillation stays at the same amplitude. The third trace of Figure 7 shows the effect of increasing R_1. If the loss becomes large, the oscillation amplitude eventually goes down.

However, the value of R_1 when the oscillation stays flat from the beginning of the simulation to the end can be considered as the *negative resistance margin* of this oscillator circuit and this crystal. The negative resistance margin is a measure of the robustness of the oscillator circuit. The value can be compared with actual experimental measurements.

Finally, to determine the necessary gain of the amplifier to make the circuit oscillate, the amplifier can be replaced by a voltage-controlled voltage source, and repeat the above simulation. It is suggested that circuit designers work with this example and vary different parameters before they try to simulate their own design with the quartz crystal. Readers can find more crystal oscillator circuits from other sources [6].

The same crystal and the same circuit can be made to oscillate at the third overtone. To do this, we include the shunt LC circuit and the third overtone resonator. C_3 is now given an initial voltage instead of C_1. The C_o is given a voltage inversely proportional to the C_o and C_3 ratio. Figure 8 shows the third-overtone oscillation. Similar negative resistance can be obtained from the simulation and compared to test results. Readers are encouraged to simulate the circuit in Figure 4 and to note the differences in how one can manipulate the circuit simulation between a LC model and a transmission line model.

Conclusion

Piezoelectric effects can be easier to understand by studying how crystal models represent these effects. The behaviors of piezoelectric crystals need not be a mystery. Try the circuit example, and work with the various circuit components to gain a better understanding of the functions of each component in an oscillator circuit. Most importantly, the performance of any oscillator circuit can be verified between simulations and tests. Designers can build up their oscillator experience through testing their own circuits. *RF*

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3. D. I. Polidi, "Design Method for a

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*******************************************************************
*                                                                 *
* This setup simulates the series LC model                        *
*                                                                 *
* The crystal is 10 MHz fundamental and 30 MHz third overtone     *
*                                                                 *
*  Co = 4 pF    Cp = Co K**2 = 0.64 pF                            *
*  C1 = 8 Cp/(pi)**2 = 0.5187 pF   L = 0.48828 mH                 *
*  C3 = C1/3**2 = 0.05764 pF                                      *
*******************************************************************
.GLOBAL  VDD VSS BULK
*******************************************************************
.SUBCKT inverter OUT IN nchw=4 nchl=2 pchw=12 pchl=2
Mu2 OUT IN VSS VSS NFET L=nchl W=nchw
Mu3 OUT IN VDD VDD PFET L=pchl W=pchw
.ENDS
*******************************************************************
************ COMPONENTS *******************************************
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RUf Vin Vout 1Meg
CUo Vin Vout 4p IC=-0.52
RU1 Vin Vl1 6
LU1 vl1 vc1 .48828mh
CU1 vc1 vout 0.5187p IC=4
****RU3 Vin vl3 6
****LU3 vl3 vc3 .48828mh
****CU3 vc3 Vout 0.05764p
CU4 Vin VSS 22p
CU2 Vout VSS 22p
****LUS Vin Vint 5.19u
****CUS Vint VSS 48.8p
XU15 vout Vin inverter nchw=336 nchl=1.4 pchw=896 pchl=1.4
*******************************************************************
*******************************************************************
*******************************************************************
* VOLTAGE SOURCES *************************************************
*******************************************************************
VDD VDD 0 5.0V
VSS VSS 0 0.0V
*******************************************************************
* one micron CMOS process electrical parameters                   *
*******************************************************************
.LIB '/tools/meta/models/c10t_hsp' NOMINAL
*******************************************************************
.TEMP 30C
*******************************************************************
.OP
.OPTION POST
.OPTION SCALE=1.0E-06
.WIDTH OUT = 132
.TRAN 1.0N 20u
.PRINT TRAN V(vin) v(vout)
.END
```

Table 1. Spice simulation.

Coaxial-resonator Oscillator," *RF Design* October 1995, p.66.

4. G. Ghannoum and W. P. Lee, "A New Approach for Crystal Model Parameter Measurements," *Proceedings, 17th Piezoelectric Devices Conference & Exhibition*, 1995, Vol. 2, p. 1.

5. T. K. Truong, "SPICE Techniques for Analyzing Quartz Crystal Oscillators," *RF Design*, September 1995, p. 26.

6. E. Henicle , "VCO Design Using Coaxial Resonators," *RF Design*, November 1995, p. 50.

About the author

WaiTak P. Lee received a B.S.E.E. from MIT, and a M.S.E.E. and a Ph.D.E.E. from Carnegie Mellon University. He is a principal ASIC engineer designing various systems in chips. He has been with Rockwell Semiconductor systems divisions for 23 years. He has the responsibility for crystal oscillator circuit designs. He can be reached at peter.lee@nb.rockwell.com

I&Q modulators

Each month, the product forum gives companies manufacturing the products used by RF engineers the opportunity to offer their opinions regarding today's marketplace and trends in the industry without editorial interpretation. This month, the product forum highlights modulators. The information in this section was compiled by Gregg Miller, Technical Editor.

Analog Devices

The explosion of wired, and wireless, digital communications has led to rapid advancements in in-phase and quadrature (I&Q) digital RF modulation techniques. Analog Devices offers CMOS ICs that incorporate direct digital synthesis (DDS), high-speed D/A converters and digital signal processing (DSP) blocks to form complete digital modulator/frequency upconverters on a single chip. The chip supports continuous wave (CW), frequency-shift keying (FSK), quadrature FSK (QPSK), and Quadrature amplitude modulation (QAM) formats. This mixed signal architecture accomplishes the modulation and frequency upconversion function entirely in the digital domain, which has many compelling advantages over traditional analog RF techniques. A few of these attributes are I&Q channel phase matching, fast output frequency hopping, precise carrier tuning capability and digitally-programmable control of all system parameters.

Miteq

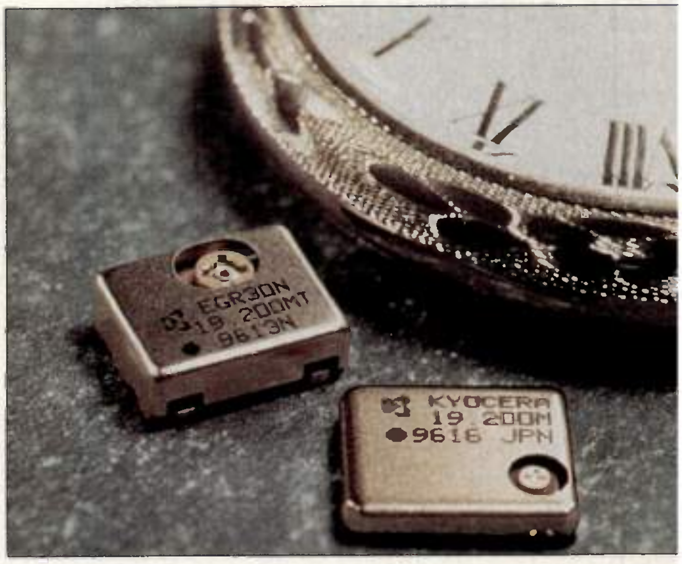
Miteq has developed a microwave mixer design supporting high carrier rejection for use in "direct on carrier" modulation. QAM waveforms are traditionally generated by first linearly mixing or modulating a VHF or UHF carrier oscillator with band-limited I&Q information. The resulting phase and/or amplitude states of the carrier are then multiplied or upconverted by another mixer, local oscillator and sideband filter to the actual transmitted frequency. I&Q modulation has traditionally been done in this manner because lower-frequency, high-isolation mixers tend to yield the best carrier and sideband rejection. High-carrier rejection, bi-phase and QPSK linear modulators for manufacturing or testing of receivers are now possible directly at higher wireless frequencies, without extra frequency conversions.

Mini-Circuits

Customers want smaller, less expensive and more reliable modulators, both analog and digital, for a wide range of frequencies. There has been particular growth in cellular and personal communications services (PCS) areas, but strong demand continues in many other areas. Interest in surface-mount modulators and for low-height surface-mount packages in particular, is increasing. Several new surface-mount, I&Q modulators and demodulators and bi-polar phase-shift keying (BPSK) modulators with transistor-transistor logic (TTL) control help to meet this demand. RF

Surface-mounted, temperature-compensated clock oscillators offer low profile

Surface mounted clock oscillators with temperature compensation feature precision crystal technology in a device with a profile height of 2.4 mm. The oscillators have a frequency stability of ±2.0 ppm with an automatic frequency control (AFC) option. The new devices are part of the KT series and are available in frequencies from 12.8–19.68 MHz with frequency stabilities to ±2.0 ppm between −30°C and +80°C. The KT12 series measures 11.6 × 9.6 × 2.3 mm. The KT11 series measures 11 × 9 × 4 mm. The oscillators combine a precision quartz crystal into a hybrid module with passive and active devices, and are designed primarily for wireless communications such as cellular and personal communications service (PCS) phone sets, base stations and two-way pagers, and for Japanese personal handyphone system (PHS) applications.
AVX Corporation
INFO/CARD 168



Non-magnetic trimmer capacitors

Non-magnetic trimmer capacitors are identical to standard air capacitors except that they are manufactured with non-magnetic materials. These capacitors are available with capacitance ranges from 0.4–3.5 pF to 1.0–30.0 pF. The

capacitors are available in a variety of sizes and in three mounting configurations, including PC mount, turret and ground lug. Applications for the capacitors include nuclear magnetic resonance equipment, medical electronics and other magnetic signature applications. These trimmer capacitors are priced at $24.75 in quantities of 1,000.
Johanson Manufacturing
INFO/CARD 169

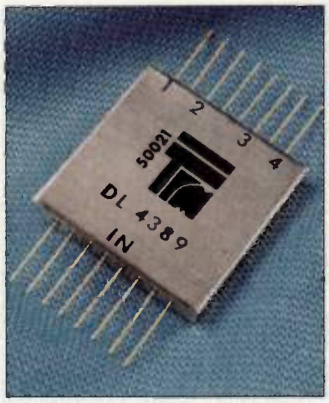
Oscilloscope features increased memory

The 9384AL digital storage oscilloscope (DSO) has four input channels that sample at 1 GS/s into 2

Mbytes of acquisition memory. The 9384AL has an analog bandwidth of 1 GHz and a single-shot sampling rate to interleave all four inputs to achieve up to 4 GS/s sampling into 8 Mbytes of memory. A 1 GS/s single-shot A-to-D conversion per channel on four channels, with 4 GS/s in single channel mode or 2 GS/s when using two channels, is also available. Features include pass/fail testing, waveform processing and interfacing options. Data storage options include internal memories, floppy and a Personal Computer Memory Card International Association (PCMCIA) card.
LeCroy
INFO/CARD 170

Four-way power divider

Model DL 4389 is a four-way power divider which operates over the 800–980 MHz frequency range. Features include an isolation of 18 dB minimum, insertion loss is 0.5 dB maximum and a voltage standing wave ratio (VSWR) of 1.6:1 maximum. Maximum amplitude and phase unbalance is 0.5 dB and 5° respectively.



Power handling is 5 W maximum with an operating temperature of −54°C to +85°C. The DL 4389 measures 1 × 1 × 0.150 in flatpak.
Technical Research and Manufacturing
INFO/CARD 171

Mini VCO for mobile radios

The V240ME01 surface-mount, mini-package, voltage-controlled oscillator (VCO) is

designed for mobile radios. It generates frequencies between 210–270 MHz within a control voltage range of 0.5–4.5 VDC. The V240ME01 draws 19 mA with a supply bias of 5 VDC. Nominal output power is 1.5 dBm into a 50 Ω load with a temperature range of −40°C to 85°C. The V240ME01 comes in a standard, mini-surface-mount (SMT) package measuring 0.50″ × 0.50″ × 0.22″ and is available in tape and reel packaging.
Z Communications
INFO/CARD 172

TEST EQUIPMENT

Broadband, dual-channel frequency synthesizers

The PTS D310 and PTS D620 are broadband, dual-channel instruments each containing two fully independent low-phase noise, low-spurious output, fast-switching frequency synthesizers. Each independent channel can be controlled through a standard 50-pin parallel interface.
Programmed Test Sources
INFO/CARD 173

TETRA signal generator for European radio system

The 2050T is the first generator to meet the adjacent channel power (ACP) requirements for the Trans-European trunked radio (TETRA) system. The 2050T offers better than –70 dBc ACP accross the 100–490 MHz frequency range while maintaining a root mean squared (RMS) vector error of better than 1.5%. Prices for the 2050T range from \$32,000–\$42,000 depending on options and frequency range.
Marconi Instruments
INFO/CARD 174

PCB plotter combines high precision and affordability

The Protomat 91S/VS system permits the fabrication of fine-pitch technology (as small as 100 µm) printed circuit board (PCB) prototypes. The 91S/VS features a variable high-speed motor, from 10,000–60,000 rpm, making possible the milling of fine isolation channels and allowing the use of special materials such as Teflon and Duriod. The system is priced at \$15,750.
LPKF CAD CAM Systems
INFO/CARD 175

Universal power meters with enhanced measurement

The 8540C series of universal power meters combine accuracy, speed, range and measurement capabilities unavailable from any other power meter. The 8540C can automatically measure the average power of pulse modulated or pulse signals that are amplitude modulated during the pulse "on" period, such as with time-division, multiple-access (TDMA) signals. The time gating option can be used to program a measurement start time and duration time to measure the average power during a specific time slot of a burst signal, critical for accurately measuring the average power of formats that must control the power trajectory during a specified potion of the burst signal such as with global system for mobile communications (GSM, formerly Groupe Speciale Mobile) and can also be used with personal handyphone systems (PHS). The 8540C series also can measure the power level of code-division, multiple-access (CDMA) signals for open-loop and closed-loop testing. Prices for the 8540C series universal power meters start at \$3,095.
Giga-tronics
INFO/CARD 176

AWGN generator for CATV, cable modem

Model UFX-BER-CATV is an additive white Gaussian noise (AWGN) generator that tests cable television (CATV) systems and cable modems by injecting noise in the upstream and downstream paths. The generator covers the frequency band from 5–850 MHz.
Noise/Com
INFO/CARD 177

SIGNAL PROCESSING COMPONENTS

Surface-mount lowpass filter

The SL-19 surface-mount lowpass filter features a 1 dB cutoff at 19 MHz and rejects 20 dB minimum at 21 MHz. It measures 1.10″ × 0.60″ × 0.27″ and has a voltage standing wave ratio (VSWR) of better than 2.0:1.
Kel-Com
INFO/CARD 178

PCS-CDMA IF SAW filter

FB F033, a 210.38 MHz surface acoustic wave (SAW) filter, is available in a hermetic surface-mount technology (SMT) package compatible with code-division, multiple-access (CDMA) personal communications services (PCS) phone architectures. The FB F033 features a bandwidth of more than 1.26 MHz at 5 dB and out of band rejection without any triple-transient or second-harmonic spurious.
Thomson Microsonics
INFO/CARD 179

Monolithic directional coupler

Model DC09-73 is a directional coupler available in the 0.81–0.96 GHz frequency range. It features an insertion loss at 0.2 dB typical, –20 dB coupling and typical input and output voltage standing wave ratios (VSWRs) of 1.15:1.
Alpha Industries
INFO/CARD 180

High dynamic range monolithic mixer products

A new family of gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) passive mixer products, model numbers MD54-0003-0006 feature a patented floating field-effect transistor (FET) topology that provides good intermodulation performance while requiring no DC bias. Designed for use where high-level RF signals and wide dynamic range are required in either up or downconversion applications at the 900 MHz and 1.9 GHz frequency bands, the mixers are suited for modulation and demodulation in receivers and transmitters for base station and portable systems. These mixers are available with 18 dBm input IP3 with 5 dBm local oscillator (LO) drive or 24 dBm input IP3 with 13 dBm LO drive.
M/A-Com
INFO/CARD 181

Quadrature modulators for digital mobile radio receivers

The RF 2711 quadrature demodulator recovers signals in IF systems with a frequency range from 0.1–85 MHz and an local oscillator (LO) frequency two times the intermediate frequency (IF). It features an on-board active device for an oscillator, a digitally controlled *power down* mode and a low LO power requirement. The RF 2711 is designed for digital communications systems, spread-spectrum communications systems, general-purpose frequency conversion and ultra high-frequency (UHF) digital and analog receivers.
RF Micro Devices
INFO/CARD 182

Bi-directional fixed attenuator pad

The HFP-510 is a high-powered fixed attenuator offering broad bandwidth (DC–6 GHz) with low voltage standing wave ratio (VSWR). A 10 W bi-directional convection air-cooled fixed attenuator pad, attenuation values range from 0–40 dB. It is also available in a 20 W version (HFP-520).
Trilithic
INFO/CARD 183

Surface-mount attenuator for PCS applications

A broadband, pin diode, analog attenuator for applications in the 100–2,000 MHz frequency range, model PI-820 features a surface-mount ceramic package specifically designed for personal communications service (PCS) applications. The PI-820 features an attenuation range of 0–40 dB and is supplied with specifications guaranteed from 800–2,000 MHz with lower frequency ranges available by changing capacitor values.
KDI/Triangle
INFO/CARD 184

DISCRETE COMPONENTS

Thin-film power chip resistor series

The MSPR series of thin-film power chip resistors maintain a power rating of 500 mW and are available in a 0.045″ × 0.030″ package. Ohmic values on these chips range from 2–250,000 ohms with tolerances to 0.1%.
Mini Systems
INFO/CARD 188

Miniature, high-capacitance, low-impedance capacitors

The LVX series of capacitors feature low impedance and are suited for high-frequency applications such as switching power supplies. The series is available with a capacitance range of 12–15,000 μF, a voltage range of 6.3–63 VDC and a rated life of 2,000–5,000 hours at 105° with ripple current applied depending on case size. The series is priced from 5–75 cents each in quantities of 1,000 depending on values and size.
United Chemi-Con
INFO/CARD 185

High dynamic range power detector modules

Designed for use in amplifier output power detection, antenna voltage standing wave ratio (VSWR) monitoring, automatic test and measurement systems and antenna field strength measurement, the PDM series of power detector modules exhibits enhanced immunity to multi-tone measurement error. The series includes 800–960 MHz and 1,850–1,990 MHz models that feature 35 dB dynamic range and 0–5 V output voltage.
Praxsym
INFO/CARD 186

Surface-mount molded-epoxy inductors

The EC3225 and EC4532 surface-mount inductors measure 3.2 × 2.5 × 2.2 mm and 4.5 × 3.2 × 3.2 mm respectively. Suitable for telecommunication products, test equipment, medical equipment or any application requiring a small surface-mount design, the EC3225 series has an inductance range of 0.12–220 μH and the EC4532 has an inductance range of 0.1–1,000 μH. Both series are available in ±20%, ±10% or ±5% tolerances.
Ecliptek
INFO/CARD 187

Trimmer capacitor has a range of 0.45–3.5 pF

A solid-dielectric trimmer capacitor features a range of 0.45–3.5 pF and positive stops at minimum and maximum with more than seven turns of tuning. It is rated 250 V working and 500 V withstanding and a Q of more than 2,000 at 100 MHz. It is priced at $3.15 each in quantities of 100 and $1.70 in quantities of 50,000.
Voltronics
INFO/CARD 189

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11	25	39	54	69	84	99	114	129	144	159	174	189	204	219	234	249
12	26	40	55	70	85	100	115	130	145	160	175	190	205	220	235	250
13	27	41	56	71	86	101	116	131	146	161	176	191	206	221	236	251
14	28	42	57	72	87	102	117	132	147	162	177	192	207	222	237	252
		43	58	73	88	103	118	133	148	163	178	193	208	223	238	253

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- 24 ☐ Industrial/Academic Laboratories, Consultants
- 27 ☐ Medical Equipment
- 13 ☐ Cellular Systems Equipment
- 23 ☐ Industrial/Commercial Control, Processing Equipment
- 15 ☐ CATV Broadcast Systems
- 08 ☐ Ground Support Equipment, Aircraft/ Missile
- 29 ☐ Education
- 10 ☐ Global Positioning Systems
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- A ☐ DC - 200 MHz
- B ☐ 200 MHz - 500 MHz
- C ☐ 500 MHz - 1 GHz
- D ☐ 1 GHz - 8 GHz
- E ☐ 8 GHz - 18 GHz
- F ☐ 18 GHz - 26.5 GHz
- G ☐ 26.5 GHz - 40 GHz
- H ☐ 40 GHz+

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- 104 ☐ $100,000 and $299,999
- 103 ☐ $50,000 and $99,999
- 102 ☐ $10,000 and $49,999
- 101 ☐ Less than $10,000

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5	19	33	48	63	78	93	108	123	138	153	168	183	198	213	228	243
6	20	34	49	64	79	94	109	124	139	154	169	184	199	214	229	244
7	21	35	50	65	80	95	110	125	140	155	170	185	200	215	230	245
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11	25	39	54	69	84	99	114	129	144	159	174	189	204	219	234	249
12	26	40	55	70	85	100	115	130	145	160	175	190	205	220	235	250
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RF software

Software for high-frequency circuit design

A CD-ROM from Optotek demonstrates features of the company's MMICAD line of computer-aided engineering (CAE) and computer-aided design (CAD) software for high-frequency circuit design for the PC. The CD-ROM includes linear simulation, schematic capture, layout, yield analysis, data acquisition and field-effect transistor (FET) modeling, plus import and export links to other simulators. The MMICAD software is available in both single-user and network versions. MMICAD Layout is designed to automate circuit layout and artwork creation. The software includes schematic capture with bidirectional links to layout and the MMICAD simulator. MMICAD Layout is based on the hierarchical Calma GDS II stream format. The software supports the use of as many as 64 layers and allows designs to be performed with as many as 20 levels of cell hierarchy. A standard Windows format with a hypertext link help system allows quick access to information on commands. The software is available in single-user versions for $1,690 and in network versions for $2,110.
Optotek
INFO/CARD 154

Software includes schematic viewer

With WinDraft's schematic capture version 1.26, any version of WinDraft, including the 100-pin capacity shareware version, will have the capability to act as a "schematic viewer" and view any size sheet. WinDraft's view mode is analogous to Microsoft Word's 6 viewer. It allows a user to view a document without having to purchase a full version of the software. WinDraft 1.26 gives engineers the ability to distribute schematics in a standardized format to anyone, anywhere, even across the Internet. The software will view any size sheet created with a licensed copy of WinDraft Schematics. It has added printing functionality to allow x and y offsets in the print dialog box. User definable attribute fields can be included in the bill of materials. The user can include information such as the module name, part stock number or any other attribute. The library editor allows easier pin mobility when creating or editing parts and configurations. Default module footprints have been added to hundreds of additional parts to facilitate use for PCB layout. Revised Getting Started guide includes netlist information and other information for printed circuit board layout. WinDraft is a suitable front-end for WinBoard PCB layout also from Ivex. Prices range from $99 to $495 depending on the pin capacity. Version 1.26 is a free upgrade to any current WinDraft user. A free share-ware version of both WinDraft and WinBoard can be obtained on the World Wide Web at: *http://www.ivex.com* by downloading "wdshare.exe" and "wbshare.exe." respectively on the anonymous FTP service.
Ivex Design International
INFO/CARD 155

Fixture software automates VNA measurements

Maury Microwave's software tool provides for automated vector network analyzer (VNA) measurements, de-embedding the measurements when fixture characteristics are known and it determines the fixture characteristics. The MT956D software provides graphic and tabular data readout of S-parameters with marker capability for accurate determination of specific points of interest. In addition to providing for de-embedding of device characteristics using developed fixture S-parameter files, the program also includes electrical models of all Maury transistor test fixture inserts, eliminating the need for fixture characterization when this fixture is used. The software supports a variety of Hewlett-Packard and Wiltron VNA, including the lightning series from Wiltron. The instrument drivers are maintained in modules separate from the main program, and the source code for the drivers is provided. This allows the user to edit an existing driver to operate an instrument not currently supported.
Maury Microwave
INFO/CARD 156

Enhancements streamline design process

ACCEL Technologies' version 12.1 of its Windows-based ACCEL EDA schematic entry and PCB layout design focuses on streamlining common design activities throughout the design process, from schematic editing to output generation. Features include component type replacement, schematic

hierarchy, teardropping and printing output by region. An optional interface to Cooper and Chyan Technology (CCT) placement tools has been added. Several changes simplify the import of Master Designer files into ACCEL EDA. The practice of changing the type of placed schematic parts is now accomplished by specifying the new type. One or more parts having the same type can be changed at one time, and all parts of multiple part components are updated simultaneously. For both schematic and PCB users, additional attribute control is provided when they refresh components in a design to match those in a library. The U.S. list price is $995 for ACCEL Schematic and $7,950 for ACCEL P-CAD PCB. ACCEL Tango PCB, the layout product for as many as 400 components, lists at $1,995. CCT AutoPlace and EditPlace modules are priced separately. International pricing is higher and is available through authorized distributors worldwide..
ACCEL Technologies
INFO/CARD 157

TK Solver Release 3 suits automation and mathematical models

TK Solver Release 3 gives a corporate or academic user the ability to link with other applications, such as MS Word and Excel; to call legacy code in FORTRAN and C; and, under UTS's new site licensing plan, to distribute TK and TK models as widely as needed. Release 3 for Windows is a tool for design engineering and sales engineering automation and mathematical modeling. Features include OLE automation support for custom front-end programmability using Visual Basic and other environments; OLE 2.0 support for linking and integration of TK objects with Microsoft Office documents; MathLook for more readable two-dimensional display of equations; external function calls for routines in FORTRAN, C and other compiled languages; wizards for such tasks as list solving, plotting, unit conversion and creating presentation-quality plots; a Greek character palette; adjustable column widths; and tool bar and object bar.
Universal Technical Systems
INFO/CARD 158

Interactive simulation for RF and microwave engineers

Avista Design Systems' Spectre/XL for RF and microwave circuit design provides interactive simulation of nonlinear communications circuits such as mixers, receivers and oscillators, especially the frequency translation of signals and noise. Spectre/XL embeds accurate circuit simulation inside Microsoft Excel. Spectre/XL's instant "what-if" analysis gives high-frequency circuit designers a powerful tool for developing, evaluating and optimizing circuits. The software gives PC-based designers help with the simulation of noise in mixers, receivers and oscillators. The new algorithm is 15–20 times faster, without sacrificing accuracy, for

analyzing "close in" phase noise in oscillators and also for conversion nose in mixers and receiver. These speed-ups are in addition to that provided by Spectre/XL's two-stage "large-signal/small-signal" algorithm for quick and accurate nonlinear analysis.
Avista Design Systems
INFO/CARD 159

SPICE CD-ROM includes models, notes, articles

Intusoft, a manufacturer of SPICE based circuit simulation tools, has released a CD-ROM with information for SPICE users. The free CD-ROM contains SPICE models, applications notes on how to model electronic devices, technical articles on how to simulate various types of designs, and more than a dozen issues of the *Intusoft Newsletter*. Working evaluation versions of Intusoft's analog and mixed signal design tools, magnetics design tools, filter synthesis tools and SPICE modeling tools are included. Much of the CD-ROM's contents can also be found on Intusoft's Web site *http://www.intusoft.com* and on CompuServe at CADD/CAM/CAE vendor forum, Library 21.
Intusoft
INFO/CARD 160

Interactive tutorial covers IEEE Std 1076 VHDL

IEEE Standards Press, a specialty standards publishing program of the Institute of Electrical and Electronics Engineers (IEEE) has released the VHDL Interactive Tutorial: A CD-ROM Learning Tool for IEEE Std 1076 VHDL. Aiding in the comprehension and use of IEEE very high-speed integrated circuit hardware description language (VHDL), this product offers a tutorial on VHDL. An enhancement to IEEE Std 1076-1993,the interactive tutorial is organized into four modules designed to add incrementally to the users' understanding of VHDL and its applications. Integrating these modules with the VHDL Language Reference Manual, IEEE Std 1076-1993 in a hypertext environment, helps users learn the language and makes VHDL more usable. The hands-on tutorial shows clear links between the many levels and layers of VHDL and provides actual examples of VHDL implementation. It describes the construct of the VHDL interface specs, what VHDL is, what it does and how it is implemented. The VHDL CD-ROM tutorial provides an easy-to-use logical method of referencing the standard. This product comes bundled with the Spyglass Mosiac 2.11 browser and is available for use in Windows (3.1 and 95), Macintosh, Sun OS and Sun Solaris environments. In addition to being licensed for single users, annual networking agreements for multiple users on a single server (site) are available for the VHDL Interactive Tutorial CD-ROM.
IEEE Standards Press
INFO/CARD 161

ERA publishes locator and directory

The Electronics Representatives Association (ERA) has published a combined directory that brings together two industry sources of information, the *Electronics Industry Locator* and the *Electronic Representatives Directory (ERD)*. The resource guide will be available through the ERA exhibit booth at industry trade shows.

Published by ERA for many years, the locator is an international guide to professional representation in the electronics industry. It provides detailed listings of ERA member firms in every geographic territory of the United States, Canada, the Caribbean, Europe, the Far East and Mexico. The 1,600 member firms are profiled according to the territory each firm covers, its customer bases, the categories of products handled, names of company officers and managers, number of personnel, branch offices and additional facilities or services.

The ERD is a telephone directory of more than 6,400 electronics industry manufacturers' representative firms. Each listing identifies the rep company's areas of product interest. The ERD includes the 1997 electronics industry calendar, a listing of domestic and international trade shows and conferences. The price for non-ERA member is $50.

Electronics Representatives Association
INFO/CARD 162

Reference book serves power supply designers

SMPS Simulation with Spice 3 is published by McGraw-Hill and is available from Intusoft. The book contains information on power supply modeling, simulation and circuit design techniques. Simulating switched model power supplies (SMPS) is made easier with this guide to using the SPICE-3, software for simulating analog and mixed-signal circuits. Average and transient models are provided for investigating any electrical characteristic of an SMPS.

Chapters include how to model the buck topology, flyback topology, EMI filters, magnetic cores, magnetic circuits; how to overcome convergence problems; how to convert AC waveforms into DC voltage levels; and how to model design considerations such as headroom, stability and ripple rejection for linear regulators; how to use optimizer routines to ensure the best possible designs.

The book is priced at $55. An accompanying disk with SPICE 3 models, schematics and SPICE netlists for all of the circuits used in the book simplifies simulations.

Intusoft
INFO/CARD 163

Digitally-tuned RF filters and preselectors featured

Digitally-tuned RF Filters and Preselectors Catalog presents information on Micropole, Minipole, Maxipole and Powerpole tunable filter product lines. The 25-page catalog covers digital readout controllers and filters; notch filters; digitally tuned, high-frequency preselectors; PC RF preselectors and postselectors (for personal computers), fast switching broad-spectrum preselectors; and low-noise amplifiers.

For RF communications equipment, these filters make suitable receiver preselectors, tunable IF filters, transmit pream filters and multicouplers. For the test bench, they are suitable tracking filters for use with spectrum analyzers and data analyzers and are useful as clean-up filters for signal generators. The catalog presents an introduction to the company's filter design concepts and product family descriptions. Specifications are listed and include passbands, insertion losses, tuning speeds, power ratings, impedances and operating temperature range. The typical performance data presents graphics on group delay response, tune time vs. frequency, inband power ratings and third-order intercept point capabilities.
Pole Zero
INFO/CARD 164

On-line

Product, technical information on Web site—Piezo Crystal's Web site contains product information on quartz crystals and high-performance ovenized crystal oscillators as well as volumes of technical resources of interest to the telecommunications systems engineers. The address is *http:// www.piezo-crystal.com.*
Piezo Crystal Company
INFO/CARD 165

Electronic catalog system on CD-ROM—Component manufacturer AVX has a CD-ROM containing software, product and technical information on its electronic components. The electronic catalog system contains information on MLC and tantalum capacitors, power supply capacitors, resistor chips, arrays and networks, integrated passive components, thin-film inductors, SMT fuses, and other devices. AVX technical papers are included along with information from AVX's technical seminars. The CD complements its web page at *http://www.avxcorp.com.*
AVX
INFO/CARD 166

Online resource site for analog IC users—Linear Technology's Web site provides a search engine that enables the user to locate LTC's technical publications, data sheets, application notes, design ideas and articles from *Linear Technology* magazine and the *LT Chronicle.* The address is *http://www. linear-tech.com.*
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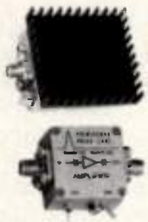

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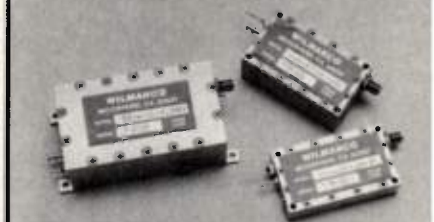

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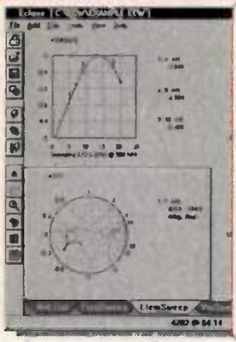

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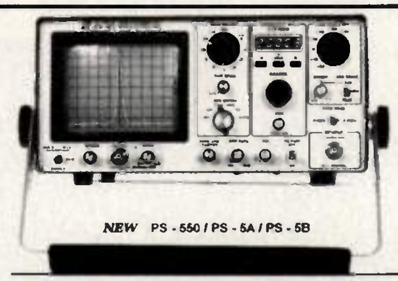

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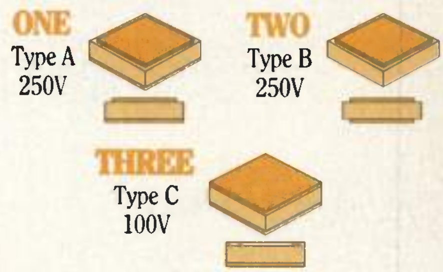

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