July 2001

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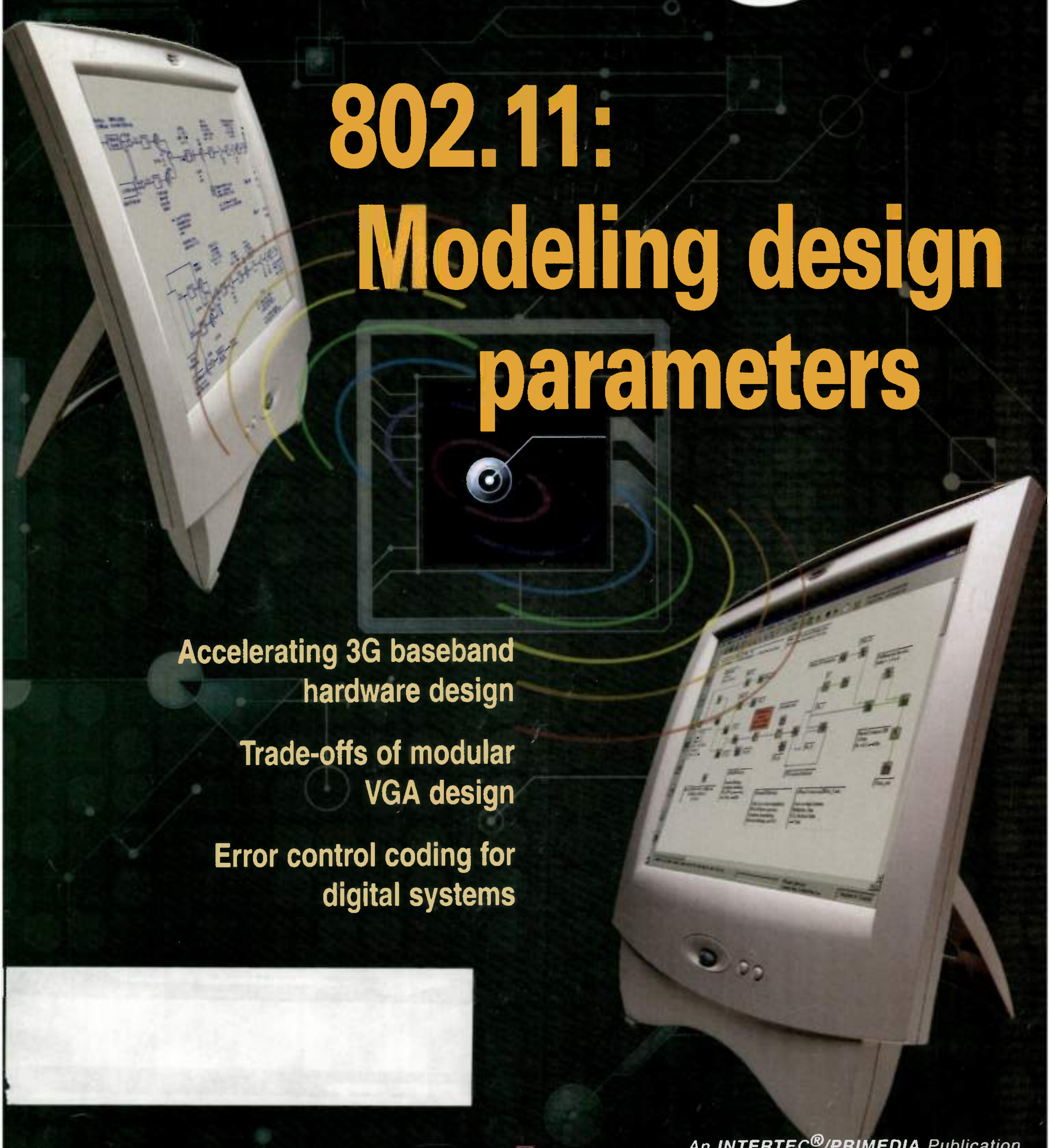

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S4W2	S4W5	N4W5	4	±0.40
S5W2	S5W5	N5W5	5	±0.40
S6W2	S6W5	N6W5	6	±0.40
S7W2	S7W5	N7W5	7	±0.60
S8W2	S8W5	N8W5	8	±0.60
S9W2	S9W5	N9W5	9	±0.60
S10W2	S10W5	N10W5	10	±0.60
S12W2	S12W5	N12W5	12	±0.60
S15W2	S15W5	N15W5	15	±0.60
S20W2	S20W5	N20W5	20	±0.60
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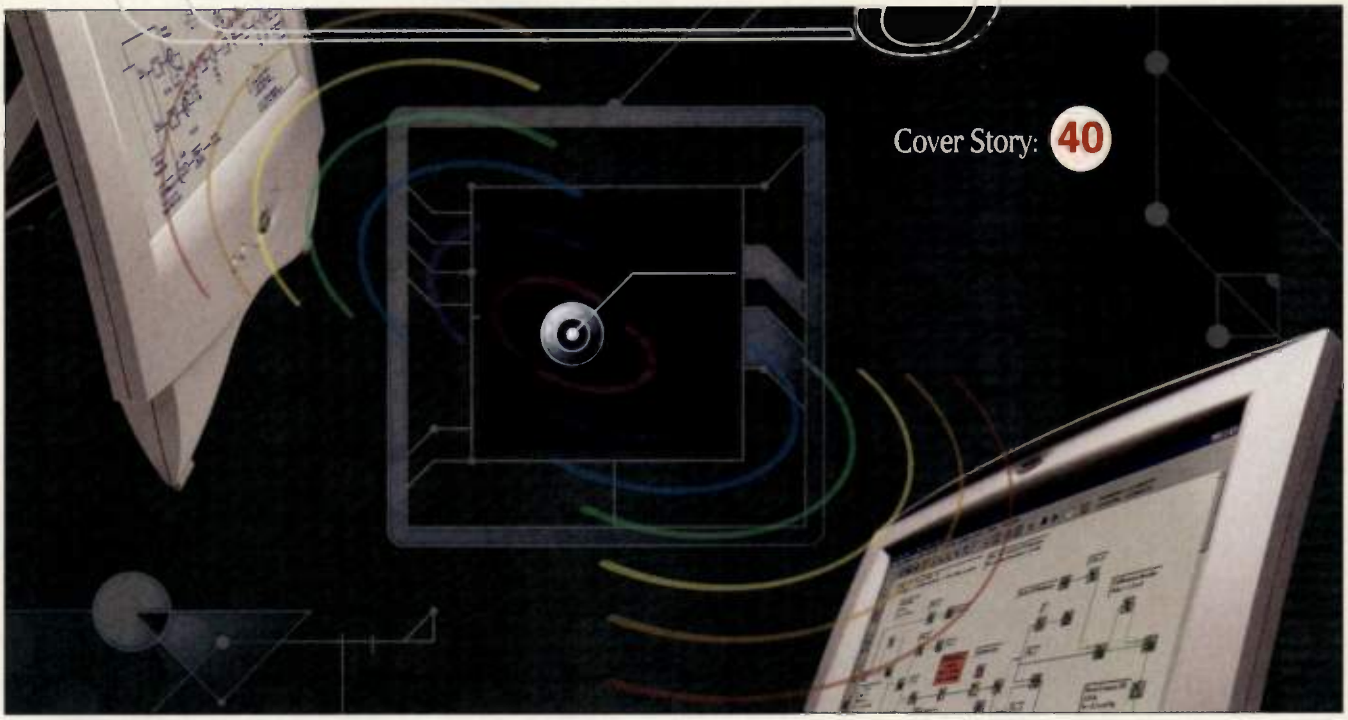

FEATURES

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SOT-89
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TYPICAL SPECIFICATIONS AT 25°C:

Model	Freq.● (MHz)	Gain (dB) 0.1GHz	Gain (dB) 2GHz	Flatness DC-2GHz (dB)	Max. Power Out▲ @1dB Comp. (dBm)	Dynamic Range▲ NF (dB)	Dynamic Range▲ IP3 (dBm)	Thermal Resist. θjc, °C/W	DC Operating Power Current (mA)	DC Operating Power Volt	Price $ea. (25 Qty.)
GAL-1	DC-8000	12.7	11.8	±0.5	12.2	4.5	27	108	40	3.4	.99
GAL-21	DC-8000	14.3	13.1	±0.6	12.6	4.0	27	128	40	3.5	.99
GAL-2	DC-8000	16.2	14.8	±0.7	12.9	4.6	27	101	40	3.5	.99
GAL-33	DC-4000	19.3	17.5	±0.9	13.4	3.9	28	110	40	4.3	.99
GAL-3	DC-3000	22.4	19.1	±1.7	12.5	3.5	25	127	35	3.3	.99
GAL-6	DC-4000	12.2	11.8	±0.3	18.2	4.5	36	93	70	5.2	1.49
GAL-4	DC-4000	14.4	13.5	±0.5	17.5	4.0	34	93	65	4.6	1.49
GAL-51	DC-4000	18.1	16.1	±1.0	18.0	3.5	35	78	65	4.5	1.49
GAL-5	DC-4000	20.6	17.5	±1.6	18.0	3.5	35	103	65	4.4	1.49

●Low freq. cutoff determined by external coupling capacitors. ▲Models tested at 2GHz except GAL-4, -5, -6, -51 at 1GHz.
*Subject to terms and conditions of the warranty published in our current Designer's Guide. Complete specifications, performance data, and reliability report available on our web site.

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RF editorial

Does anyone remember Beta?

By Roger Lesser
Editor
rlesser@intertec.com

Do you realize we've been fighting a technology war since early man "invented" fire? Mankind's history is ripe with example after example of one technology overtaking another. That's good most of the time, but not when it gets in the way of technology advancement. I'm a stereo buff. I wish I could call myself an audiophile, but I only have a "few" dollars sunk into my systems. I have a good friend who is a true audiophile. He has speakers that darn near reach the ceiling, a widescreen television and enough black boxes to make the Pentagon's "dreamland" look like amateur hour. I'm married. Mike lives with a small dog named Mia. You draw the conclusion.

Being a stereo buff means I keep up with the latest advancements. Talk about technology wars. First there was mono, then hi-fi. Then came true stereo, followed by quad systems and then surround. Then along came 5.1, and now 6.1. Then we went from tubes to solid state, and from analog to digital. Now there is a technology war brewing over the new format for CDs. And don't forget our computer comrades: Apples vs. PCs, Windows vs. Apple vs. OS2, etc. And what about competing computer languages? Talk to me about Ada someday. And who can forget the VHS vs. Beta battles? But, not to be outdone, telecom has its own technology turf tussles: CDMA vs. TDMA vs. GSM vs.... Bluetooth vs. Home RF, 3G vs. whatever else is available, Silicon vs. GaAs, etc.

And the winner is...?

So, who is the winner in all this? The end user? Wrong. Often the technology battles get in the way. For example, VHS won, but Beta offered a better picture. Solid state pushed tubes out of the picture, yet tube-driven devices offered better sound quality. (I chuckle when I see ads for solid-state devices that say they offer the "mellowness" of tube amplifiers.) PCs pushed the Apple out, yet Apples were easy to use and (before the Macs) dependable. Apple's operating system was dependable, but along came Microsoft. Windows wins. (And we are all the better for it?) All the competing wireless formats have made a mess of any hope of standardization. I still hold a candle for interoperability. But chances are, even this will get delayed as the battle over how it will be done is fought.

And the point is?

The point to all of this is simple. While the better technology may fade or fail, the pursuit of new advances will always drive us forward. Even if we have to take a step back to make it happen. (The first surround systems lost out to quad, and it was years before surround got back in the game.) As a consumer, I really get bent out of shape when the next technology comes along and promises the world, kills competing technologies and then implodes. (Anybody own a Sony Dreamquest?) So, my design engineering friends, what do you think? How can the best technology be the winning technology? Or is it, and I just don't get it. Did I mention I still play records?

Roger

INFO/CARD 4

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INFO/CARD 3

RF calendar

July

9–12 **Embedded Systems Conference** – *Chicago* – Information: Web site: **www.embedded.com/esc**

10–11 **Wireless Partnerships and Alliances Congress 2001** – *San Francisco* – Information: Web site: **www.iqpc.com**

August

13–17 **IEEE-EMC Symposium** – *Montreal* – Information: Web site: **www.ieee.org.**

21–23 **ITCom and Opticomm 2001** – *Denver* – Information: Web site: **www.spie.org/info/itcom**

September

4–7 **Embedded Systems Conference** – *Boston* – Information: Web site: **www.embedded.com/esc**

24–26 **EDA: Front-To-Back** – *Santa Clara* – Information: Penton Media. Tel. 1.888.947.3734.

24–28 **European Microwave Week** – *London* – Information: Web site: **www.eumw.com**

October

1–3 **34th Annual Connector and Interconnection Technology Symposium** – *Anaheim* – Information: Web site: **www.ec-central.org**

1–4 **Communications Design Conference** – *San Jose* – Information: Web site: **www.CommDesignConference.com**

2–4 **Sensors Expo Fall** – Philadelphia – Information: Web site: **www.sensorsexpo.com**

23–25 **Cleveland 2001 Advanced Productivity Exhibition** – *Cleveland* – Information: SME Customer Service. Tel. 800.733.4763. Web site: **www.sme.org/cleveland**

December

3–6 **Internet World Wireless West 2001** – *San Jose* – Information: Web site: **www.ccievents.com**

11–13 **Bluetooth Developer's Conference 2001** – *San Francisco* – Information: Web site: **www.key3media.com/bluetooth/**

RF courses

Agilent Technologies – *RF and Microwave Fundamentals* – Aug. 29–31, Dec. 4–6; *Network Analysis Measurements* – Oct. 16–17; *Spectrum Analysis Measurements* – Oct. 18–19. Information: Tracey Bull, Eskdale Rd., Winnersh Triangle, Wokingham, UK; Tel. +44.118.927.6741; Fax: +44.118.927.6862; e-mail: *tracey_bull@agilent.com*

University of Missouri-Rolla – *Grounding and Shielding Electronic Systems* – Aug. 8–9, Toronto; *Circuit Board Layout to Reduce Noise Emission and Susceptibility* – Aug. 10, Toronto; Sept. 19, Denver. Web site: **www.umr.edu/-conted>**

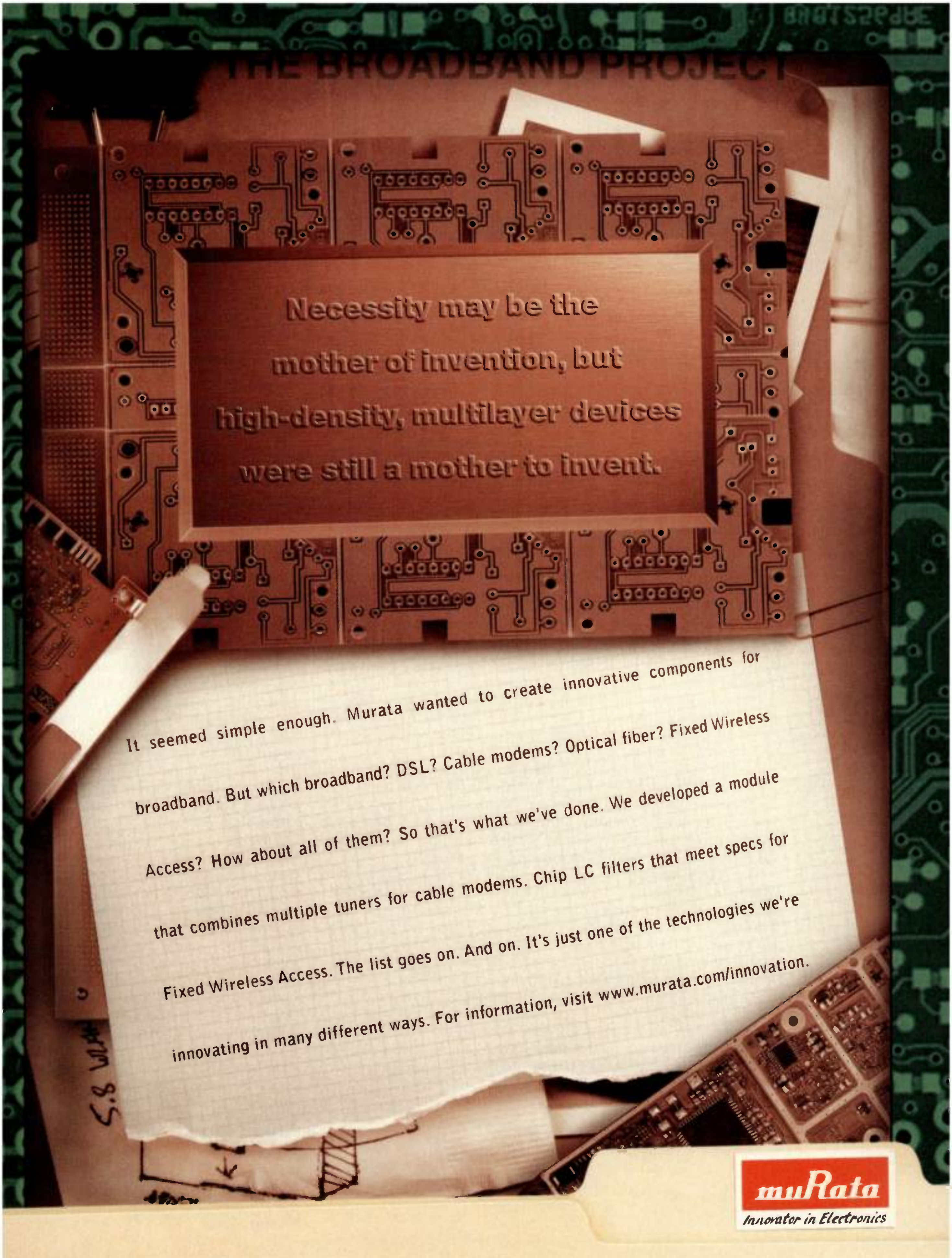
Alexander Resources – *Making Money in the U.S. Wireless Internet Market* – Aug. 8–9, Washington DC. Information: Jeff Stone, Alexander Resources,15851 N. Dallas Pkwy, Addison,TX 75001; Tel. 972.818.8225; Fax: 972.818.6366; e-mail: *jstone@alexanderresources.com*.

Besser Associates – *RF and Wireless made Simple* – Aug. 7–8, San Diego. Information: Besser Associates, 201 San Antonio Circle Building E, Suite 280, Mountain View, CA 94040; Tel. 650-949-3300; Fax: 650-949-4400; e-mail: *info@bessercourse.com*; Web site: **www.bessercourse.com**

UCLA – *Biometric Identification: Theory, Algorithms and Applications* – July 30–Aug. 1; *Digital Signal Processing: Theory, Algorithms, and Implementation* – Aug. 13–17; *Bluetooth: Technology, Applications, and Performance* – Aug. 20–22, Los Angeles. Information: Information Systems and Technical Management Short Courses. Tel. 310.825.3344; e-mail: *mhenness@unex.ucla.edu*; Web site: **www.uclaextenstion.org/shortcourses**

R.A. Wood Associates – *Introductory RF and Microwaves* – Sept. 20–21; *RF and Microwave Receiver Design* – Sept. 24–26; *RF Power Amplifiers, Classes A–S: How Circuits Operate, How to Design Them, and When to Use Each* – Sept. 27–28, Lake George, NY. Information: R.A. Wood Associates, 1001 Broad St. Ste. 450, Utica, NY 13501; Tel. 315.735.4217; Fax 315.735.4328; e-mail: *RAWood@rawood.com;* Web site: **www.rawood.com**

Massachusetts Institute of Technology – *Principles of Optical Sensors* – Aug. 6–10, Cambridge, MA. Information: Tel. 617.253.2101; Fax 617.253.8042; e-mail: *professional-institute@mit.edu* Web site: **www.web.mit.edu/professional/summer**


THE BROADBAND PROJECT
Necessity may be the mother of invention, but high-density, multilayer devices were still a mother to invent.
It seemed simple enough. Murata wanted to create innovative components for broadband. But which broadband? DSL? Cable modems? Optical fiber? Fixed Wireless Access? How about all of them? So that's what we've done. We developed a module that combines multiple tuners for cable modems. Chip LC filters that meet specs for Fixed Wireless Access. The list goes on. And on. It's just one of the technologies we're innovating in many different ways. For information, visit www.murata.com/innovation.
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Taxes for technology?

By Megan Alderton
associate editor
malderton@intertec.com

The 21st century workforce is a different breed than those before it. These days, technical skills are just as important to production as reading and writing skills. From RF design to fast-food, almost all positions require some technical knowledge.

Why, then, is there so little emphasis on techno-skills in schools? Why, then, are high-tech employers having such a hard time finding workers with the skills needed to fulfill their positions?

Funding may be the biggest set-back to quality technical training in education, but what can be done about it remains in question. Gary Beach, publisher of *CIO*, has an interesting idea. And it, or a variation of it, just might work.

In an Internet column titled "No-Shows of Support," Beach recommends the placement of an excise tax on technological items. One-half of 1% on the excise tax on the sales of technological products and services more than $1,000 would be applied to technology education. This approach, Beach said, would ensure that low-income, first-time buyers be exempt. Companies using technology the most — companies that need a tech-trained workforce — would pay the most.

Beach estimates that his idea would raise $2 billion a year. This money would go to the National Education Technology Trust Fund where it would be managed by a bipartisan congressional committee. Each year, he said, every penny collected would be dispersed evenly among the 50 states for faster adoption of technology education.

One could argue, however, (and several did on the *CIO* Web site) that public schools are having a hard enough time turning out graduates competent in *basic* math, science, reading and writing skills. It could also be argued that tech skills are better reserved for higher education than the elementary level. Maybe businesses need to bring education in-house and start doing their own training.

As you are part of the tech workforce, let us know what you think. Would a tech-tax be an infringement on the rights of the consumer; on the rights of free enterprise? Would it be a wasted effort to tech-fund public schools? Or is it the way to go in building a future workforce capable of keeping up with the technological transformations of our world?

Megan

IEEE MTT-S IMS show wrap

Hot time in Phoenix

Both the weather and the amount of new product announcements were hot at this year's IMS show in Phoenix.

While talk was heavy on the "downturn" in the industry, the show floor was buzzing with a surprising amount of new product announcements and exhibitors. It goes to show that things may not be as bad as they seem.

In fact, an abundance of optimism was spilling from the booths concerning the state of the industry. Many of the companies that *RF Design* met with actually said that they were taking advantage of this "down" time to reach potential clients and market sectors they didn't have time to before. Some smaller companies are using the time to get an edge on their competitors, and others are simply going about their business (which means there is still business to go about).

Further evidence of the coming industry recovery was the expansion by some companies of existing facilities or agreements made to facilitate smarter and cheaper production. And who could ignore the amount of product announcements made? From new connector technology to design suites, one couldn't turn a corner without finding something new.

Just to name a few, Mimix Broadband announced a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) two-stage power amplifier optimized for linear operation, and Anadigics introduced two InGaP HBT power amplifiers for use in multimode, multiband CDMA handsets that support 2.5G CDMA applications. Murata Electronics introduced a Bluetooth module developed using low temperature co-fired ceramics (LTCC) technology. And GHz Technology announced its first two designs in a series of lateral diffusion metal-oxide semiconductor (LDMOS) transistors developed for the wireless infrastructure marketplace.

For those who couldn't make it to the show, or those interested in more of the products announced, please visit the *RF Design On the Road* link at **RF Design.com**.

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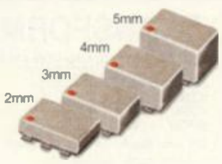

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ADE* TYPICAL SPECIFICATIONS:

Model	Height (mm)	Freq. (MHz)	LO (dBm)	Conv. Loss Midband (dB)	L-R Isol. Bandwide (dB)	IP3 (dBm) @ Midband	Price ($ea.) Qty. 10-49
ADE-1L	3	2-500	+3	5.2	55**	16	3.95
ADE-3L	4	0.2-400	+3	5.3	47**	10	4.25
ADE-1	4	0.5-500	+7	5.0	55**	15	1.99▲
ADE-1ASK	3	2-600	+7	5.3	50**	16	3.95
ADE-2ASK	3	1-1000	+7	5.4	45**	12	4.25
ADE-6	5	0.05-250	+7	4.6	40	10	4.95
ADE-12	2	50-1000	+7	7.0	35	17	2.95
ADE-4	3	200-1000	+7	6.8	53**	15	4.25
ADE-14	2	800-1000	+7	7.4	32	17	3.25
ADE-901	3	800-1000	+7	5.9	32	13	2.95
ADE-5	3	10-1500	+7	6.6	40**	15	3.45
ADE-13	2	50-1600	+7	8.1	40**	11	3.10
ADE-11X	3	5-2000	+7	7.1	36**	9	1.99▲
ADE-20	3	1500-2000	+7	5.4	31	14	4.95
ADE-18	3	1700-2500	+7	4.9	27	10	3.45
ADE-3GL	2	2100-2600	+7	6.0	34	17	4.95
ADE-3G	3	2300-2700	+7	5.6	36	13	3.45
ADE-28	3	1500-2800	+7	5.1	30	8	5.95
ADE-30	3	200-3000	+7	4.5	35	14	6.95
ADE-32	3	2500-3200	+7	5.4	29	15	6.95
ADE-35	3	1600-3500	+7	6.3	25	11	4.95
ADE-18W	3	1750-3500	+7	5.4	33	11	3.95
ADE-30W	3	300-4000	+7	6.8	35	12	8.95
ADE-1LH	4	0.5-500	+10	5.0	55**	15	2.99
ADE-1LHW	3	2-750	+10	5.3	52**	15	4.95
ADE-1MH	3	2-500	+13	5.2	50**	17	5.95
ADE-1MHW	4	0.5-600	+13	5.2	53**	17	6.45
ADE-12MH	3	10-1200	+13	6.3	45**	22	6.45
ADE-25MH	3	5-2500	+13	6.9	34**	18	6.95
ADE-35MH	3	5-3500	+13	6.9	33**	18	9.95
ADE-42MH	3	5-4200	+13	7.5	29**	17	14.95
ADE-1H	4	0.5-500	+17	5.3	52**	23	4.95
ADE-10H	3	400-1000	+17	7.0	39	30	7.95
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BUSINESS BRIEFS

EMS Technologies acquires repeater product line — EMS Technologies, Atlanta, announces the acquisition of CI Wireless, Dallas. The acquisition provides two new product areas for EMS Wireless. The first enables EMS Wireless to extend indoor RF coverage through the use of indoor repeaters and fiber-optic-based RF distribution systems. The second product area, outdoor repeaters, helps carriers to extend their wireless coverage in rural areas or uneven terrain without having to add expensive new base stations. Terms of the acquisition were not announced.

GHz Technology selects Palomar to automate RF component assembly — Palomar Technologies, Vista, CA, announces that GHz Technology, Santa Clara, CA, has selected Palomar's automated assembly systems to help meet growing demand for its products in the burgeoning cellular and PCS arena. In addition to using Palomar's automated die attach and wire bonding equipment, GHz recently added the new HotRail RFA machine to its assembly line.

Silicon Wave selects Agilent 93000 platform for testing of next-generation Bluetooth ICs — Agilent Technologies, Palo Alto, CA, and Silicon Wave, San Diego, announce that the Agilent 93000 SOC series with RF capabilities will be implemented for the development and manufacturing test of next-generation Bluetooth integrated circuits (ICs). The 93000, a single scalable platform, will provide Silicon Wave with the performance necessary for IC design verification and characterization, while allowing it to optimize cost for manufacturing.

Stanford Microdevices announces foundry agreement with RF Micro Devices — Stanford Microdevices, Sunnyvale, CA, announces a foundry agreement with RF Micro Devices, whereby SMDI's RF integrated circuits (RFICs) will be manufactured in RF Micro Devices' 4-inch gallium-arsenide (GaAs) heterojunction bipolar transistor (HBT) fabrication facility, located in Greensboro, N.C.

Mitel Corporation reborn as Zarlink Semiconductor — Mitel Corporation, Ottowa, Canada, introduces its new identity — Zarlink Semiconductor — under which it will deliver communications connectivity solutions to leaders in voice and data networking.

WaveSmith Networks triples size of corporate headquarters facility — WaveSmith Networks, Acton, MA, has opened its new corporate headquarters at 35 Nagog Park in Acton, MA. The new 30,000-square ft. facility is triple the size of the company's previous headquarters. WaveSmith also announces the opening of its sales offices in Denver and Reston, VA.

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- Financial
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In addition to its link feature, the WCA Web site also offers an industry acronym list, job postings, wireless-related articles, and overviews of band plans, fixed wireless broadband, wireless cable and the license-exempt spectrum. WCA press releases are also included, along with a government affairs section and interviews with key wireless players. Those interested in joining the WCA can find out about the association's benefits on the site, as well as fill out an online application.

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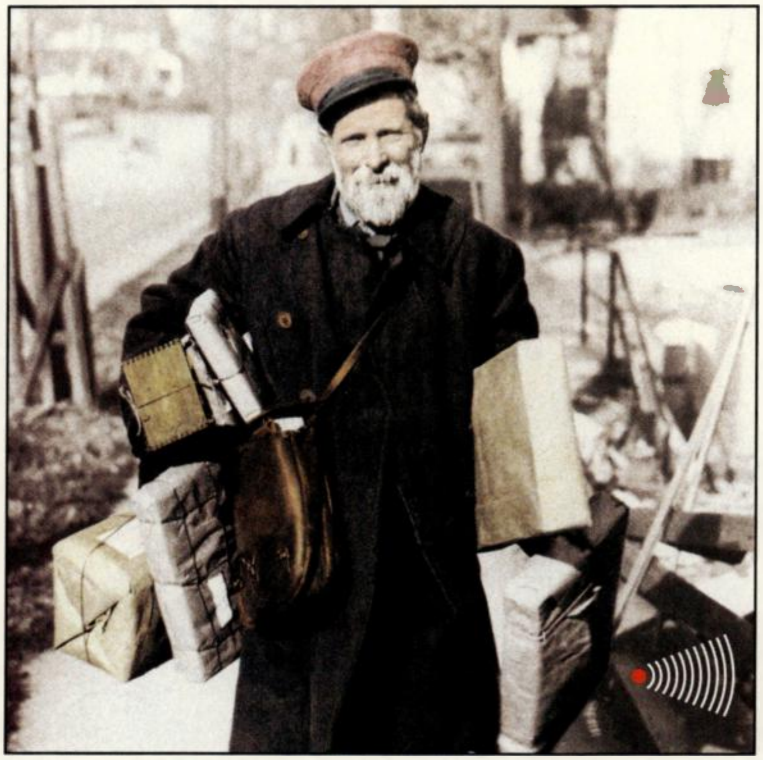


VARIETY

Accelerating baseband hardware design for 3G terminals

Developing hardware for 3G systems is challenging. This technology will improve time-to-market and simplify design.

By Lieven Philips

It's no surprise that the mobile phone market is growing steadily—about 500 million mobile phones are in use worldwide. And, though the market is still primarily voice-based, additional services requiring broad bandwidths are gaining increased attention. As the popularity of these services grows, however, a number of hardware challenges exist in designing the baseband hardware for 3G terminals. Fortunately, there are also solutions.

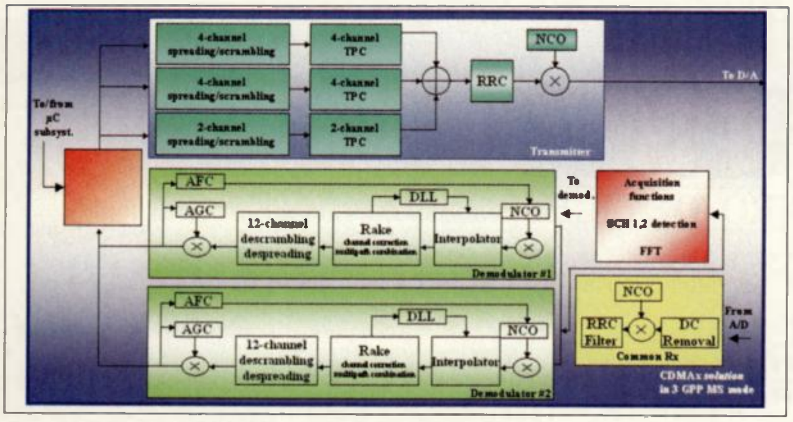


Figure 1. Baseband W-CDMA inner modem architecture.

In Japan, additional features such as banking, stock-exchange transactions, sports and weather information are offered through the i-mode, which grows by 50,000 subscribers every day. Short messaging service (SMS) is tremendously popular in Europe as well. The introduction of wireless application protocol (WAP) has boosted this evolution further, but it suffered from the too-low data rates offered over a traditional GSM network.

The recent introduction of general packet radio service (GPRS) is the necessary stepping stone to true cellular data applications with sufficient user comfort. The 2002 introduction of the universal mobile telecommunication system (UMTS) in Europe will mark the advent of multimedia services offered via cellular terminals. The UMTS standard will surpass global system for mobile communications (GSM) and its GPRS derivative by offering greater flexibility for different applications over one air interface. And it will use spectrum resources more efficiently.

New challenges

Most telecom companies and market analysts anticipate that the evolution to a multimedia-driven mobile market will begin in 2002. On the other hand, the Third Generation Partnership Project (3GPP) and 3GPP2 standards are only now being finalized. As a consequence, 3G baseband component design houses and terminal manufacturers face short development times if they want to introduce their products to the market early.

3G technology is also more complex, both in air interface and in applications. For this reason, a 3G system on chip (SOC) will include more functionality than, say, a GSM baseband application-specific integrated circuit (ASIC). Therefore, the intellectual property (IP) building blocks–or cores–need to include much larger functional entities as compared to current practice. For instance, rather than numerically controlled oscillators (NCOs) or pulse-shaping filters, a complete wideband, code-division multiple access (W-CDMA) transceiver is considered a building block for a baseband SOC (see Figure 1).

Flexible cores are a key element

Flexibility is required to enable engineers to cope with rapid changes in standards as well as to make the product useful across a range of applications and multiservice terminals. When a specific core is required for a particular application, the adopted design method allows fast customization.

Low power challenges

Low power consumption is a basic requirement for hand-held devices. The core achieves this by making the right hardware and software trade-offs for the physical layer (see Figure 2), and by applying low-power design techniques in the circuitry implementation (see Figure 3).

Nowadays, GSM and GPRS baseband architectures are digital signal processor (DSP)-centric, i.e. the DSP core performs the source codec function and the larger part of the physical layer waveform processing. For the near future, powerful DSP cores clocked at several hundreds of megahertz will be available. But, given the 3G waveform complexity and the high data rates to be processed, only a small part of the baseband processing can be handled by such a processor core. In such architectures, most of

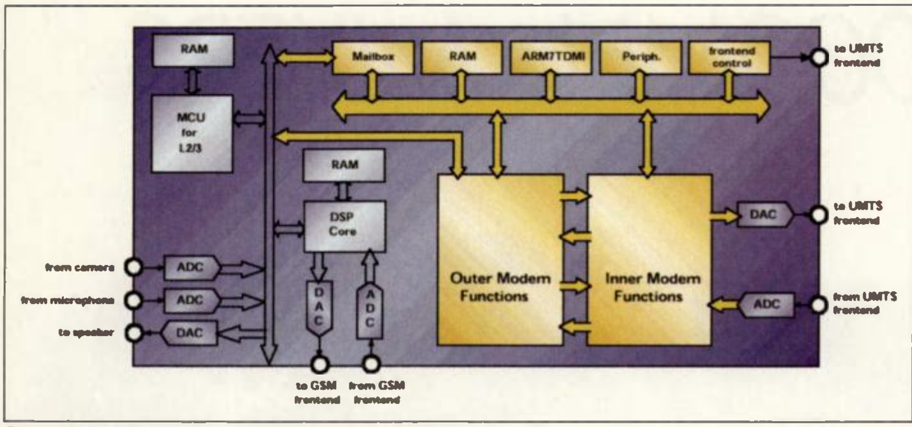


Figure 2. Low-power, flexible 3G baseband architecture.

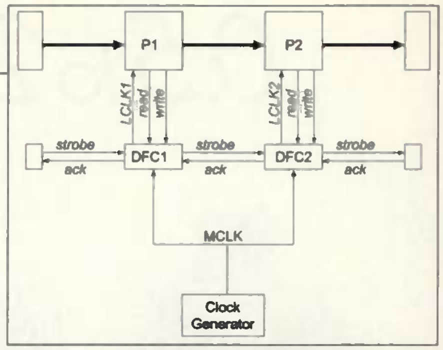


Figure 3. Low power consumption design criterion.

the 3G baseband operations are still to be executed in hardware accelerators (co-processors). This leads to a bus traffic bottleneck, which also contributes significantly to the power consumption. Even with DSP cores optimized for ultra-low power consumption, the power consumption associated with the highly multiplexed data paths and the massive on-chip (or even off-chip) memory needs force visionary 3G chip manufacturers to do it differently.

Low-power challenges – part 2

A more interesting approach, which allows the baseband power consumption to be reduced by at least an order of magnitude, allocates a DSP, clocked at a lower speed (e.g. 13 MHz), for the GSM baseband transceiver implementation and 3G source codec functions. This approach uses primarily reconfigurable hardware for the UMTS/FDD L1 functionality. In this architecture, the ARM (DEFINE) subsystem on top in Figure 3 performs parameter downloading at boot time and run-time closing of slow loops (e.g. for parameterization of different fading algorithms). The advantages over the high-speed DSP core approach are clear: The flexible logic is clocked at moderate speeds (around 20 MHz), and all the registers and small, distributed memories are accessed on-chip. At the same time, a sufficient level of flexibility is provided at a reasonable additional gate count.

Drilling down

Low-power design techniques are also exploited on the circuit level. W-CDMA architectures are multi-rate by nature, hence different clock frequencies are applied in different parts of the transceiver. Moreover, multiple services imply multiple data rates, depending on the activation of the service in the terminal. Also, when a terminal is just roaming, a considerable part of the digital functions should be switched off completely. It is therefore advantageous to have clock frequencies that are self-adaptable as a function of the operational parameters (see Figure 3).

It's in the protocol

Communication between blocks is organized through a handshake protocol. Clocks are ticking only when data have to be transferred, and idle clock cycles do not occur.

Data integrity is secured through the handshaking with the strobe and acknowledge signals.

Advantages of this data flow control (DFC)-based intermodule communications include the self-adaptability for different data rates and parameter configurations, as well as the significant reduction of the load on the high-frequency clock nets. Moreover, idle blocks are automatically switched off, which simplifies the implementation of the power-down modes of the terminal. The good news is that the hardware overhead of the DFC blocks is negligible.

The multiservice challenge

The concept here is based on a hardware approach for reaching the software radio goal: rather than using a high-speed DSP, programmable hardware is used. This particular subsystem is the master of the reconfiguration control and reconfigurability allows one to:

- reconfigure between UMTS/FDD and IS-95.
- select alternative algorithms for channel estimation, searcher and finger management, etc.
- select various interfaces for different radio front-end architectures.
- reconfigure L1 for multiple applications, and the support of multiple services on a single terminal.
- reconfigure for GPS, Galileo (the European navigation satellite system) and S-UMTS (the satellite extension of terrestrial UMTS).
- keep track of the standardization evolution.

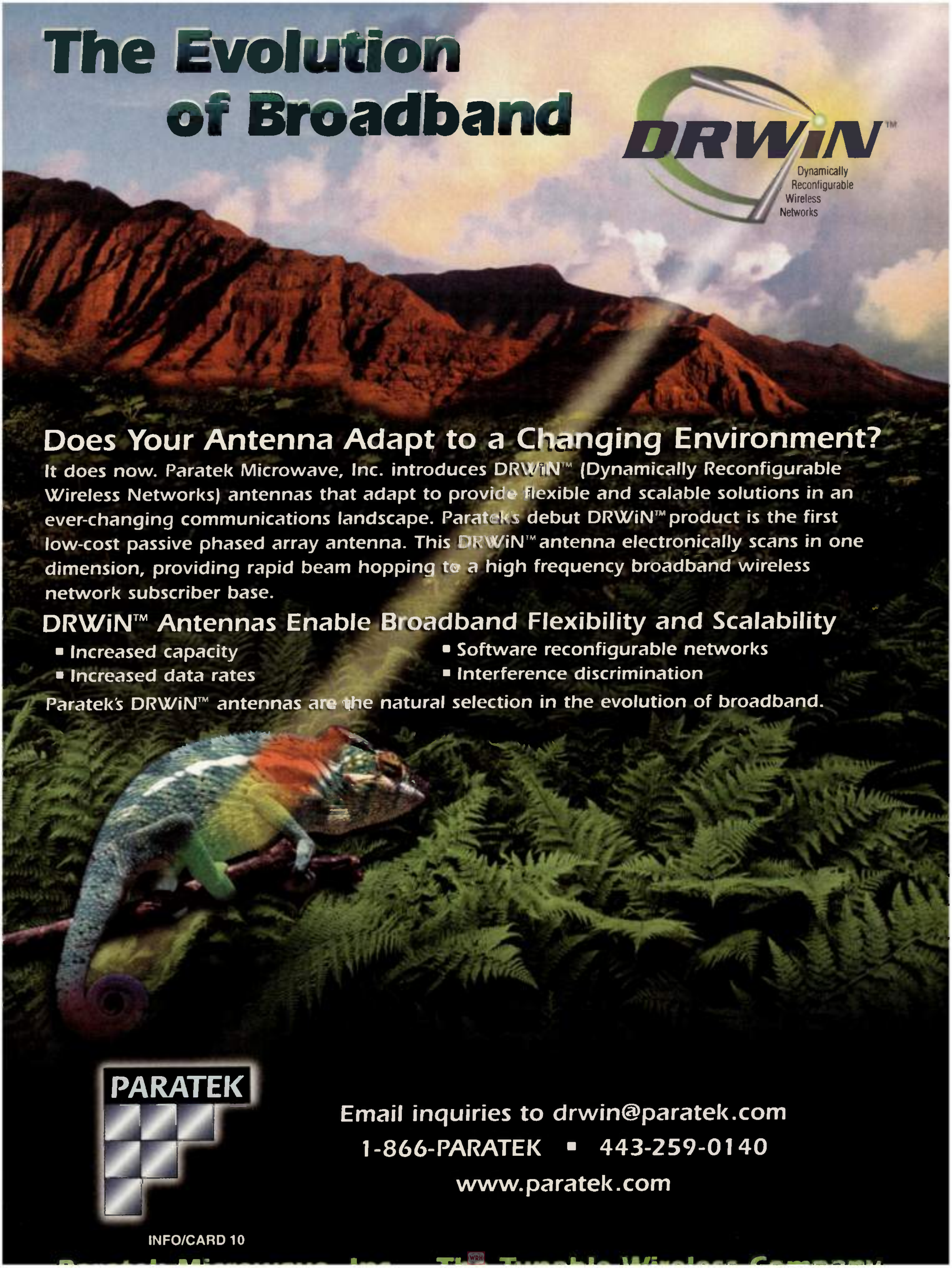
When a specific 3G core is required for a particular application, the modular design facilitates customization of the generic solution in a short time frame. Furthermore, in line with the 3G road map, the extensions to UMTS/TDD and to CDMA2000-compliant transceiver modules will naturally evolve out of the current flexible architecture.

For 3GPP

To realize the 3GPP standard, several auxiliary physical channels must be transmitted and received together with the information-carrying channels. Furthermore, the number of the information-carrying channel's dedicated physical data channels (DPDCH) can vary depending on the data rate and the number of services that run on the terminal. The latter is referred to as multicode transmission. For this purpose, the cores referred to feature a channel matrix in the transmit section and the demodulators to allow a flexible mapping of channels on the logic. The multicode transmission aspect and the flexibility requirements have also lead to a different Rake concept compared to traditional cellular CDMA receiver implementations.

Depending on the application, different environments, multipath characteristics and Doppler characteristics are encountered. In some cases, applications have to function in different circumstances (e.g. a mobile Web browser used indoors and on board a fast train), which means that cell search and channel correction algorithms need to be reconfigurable on-the-fly. The core's demodulator architecture features the necessary flexibility to support this, and the ARM subsystem is in charge of controlling it.

The core architecture also supports the processing of GPS and Galileo satellite signals. Many 3G applications will require accurate positioning in one form or another. For the sake of emergency assistance, a duplex operation (switching between UMTS mode and naviga-



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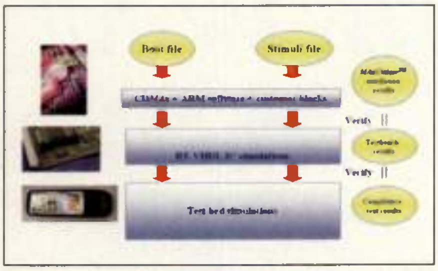

Figure 4. The W-CDMA IP core in the 3G terminal design trajectory.

tion mode) is sufficient. The ARM will control this reconfiguration and will also calculate the navigation solution out of the pseudo-range measurements from the core's receiver correlators. For applications requiring simultaneous communications and navigation, the modular design allows straightforward extension with extra tracking units and duplication of the front-end interface.

Given the aggressive time schedules previously discussed, speeding up the baseband ASIC development is on the wish lists of most 3G component and terminal developers. The support required is not on the algorithm development, but on evaluating and fine-tuning the chosen parameters, optimizing the core for particular applications and simulating the core in the context of the entire baseband SOC.

The race is on

The race for the first 3G terminals has started. The development schedules are aggressive, and the challenges are different from what was required for 2G phone development. Time-to-market, low power consumption and functional flexibility are the main requirements for 3G. The IP core technology discussed here is alternative to one providing the 3G baseband ASIC design teams with the tools to reach these goals.

RF

About the author

Lieven Philips has 11 years of experience in the semiconductor industry. Prior to founding Sirius Communications, Lieven worked as a Philips-resident (Eindhoven, the Netherlands) at the Advanced Software Development Group of IMEC. At IMEC, Lieven was project leader for the support of the Cathedral-1 DSP-Digest design team. He extended the IMEC ASIC CAD tools for the design, simulation and filter optimization of high-precision digital filters for audio and compact disc applications. He holds several patents on the functionality, implementation and design strategy of innovative CDMA circuits and has lectured as an invited speaker at the University of Leuven on wireless communication techniques. He obtained his EE degree, option microelectronics, from the Katholieke Universiteit Leuven. He performed his masters' thesis at Philips on the design of an 18-bit sigma delta converter for digital audio applications. He can be contacted at Sirius Communications NV Wingepark 51B-3110 Rotselaar Belgium. Tel.: +32 16 44 44 02 Fax.: +32 16 44 54 81 e-mail: *philips@siriuscomm.com*

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SME 1400B-17	1-2200	1-2200	1-2000	+17	+27	6.5	30	S-PAK-3
SME 1400B-13	1-2200	1-2200	1-2000	+13	+22	6.5	30	S-PAK-3
SME 1400B-10	1-2200	1-2200	1-2000	+10	+19	6.2	35	S-PAK-3
SMJ 500-17A	2-500	2-500	DC-500	+17	+21	6.0	44	J-PAK-6A
SMJ 500-13A	2-500	2-500	DC-500	+13	+20	6.0	44	J-PAK-6A
SMJ 1500-17B	10-1500	10-1500	DC-1000	+17	+20	6.0	30	J-PAK-6B
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Error control coding in digital communications systems

Reed-Solomon codes – a powerful tool for error detection and correction in digital wireless communications

By Louis Litwin

An important function of any modern digital communications system is error control coding. Such coding is the field of communications that deals with techniques for detecting and correcting errors in a signal. Though used in a variety of systems, error control coding is especially useful in wireless communications systems. Such systems typically operate with a low signal-to-noise ratio (SNR) and suffer from distortion because of a multipath channel. The harsh wireless environment means that the received signal is prone to errors.

Power Notation	Polynomial Notation	Binary Notation
$\alpha^{-\infty}$	0	000
α^0	1	001
α	X	010
α^2	X^2	100
α^3	X + 1	011
α^4	$X^2 + X$	110
α^5	$X^2 + X + 1$	111
α^6	$X^2 + 1$	101

Table 1. Example of GF(8) generated using $F(X) = X^3 + X + 1$. Note that the field wraps around so that $\alpha^7 = \alpha^0 = 1$.

Typical communications systems use several codes that are suited to correcting different types of errors. Reed-Solomon (RS) codes are the most powerful in the family of linear block codes and are arguably the most widely used type of error control codes.

Error control coding

The fundamental concept of error control coding is the addition of redundancy to a signal at the transmitter, and the exploitation of that redundancy at the receiver to detect and/or correct errors. The inclusion of redundancy in the transmitted signal results in a coded signal consisting of more bits than the original uncoded signal. The trade-off for this overhead is the ability to detect, and possibly correct, errors at the receiver. The performance improvement that occurs when using error control coding is often measured in terms of coding gain. Suppose an uncoded communications system achieves a given bit error rate (BER) at an SNR of 30 dB. Imagine that an error control coding scheme with a coding gain of 3 dB was added to the system. This coded system would be able to achieve the same BER at the even lower SNR of 27 dB. Alternatively, if the system was still operated at an SNR of 30 dB, the BER achieved by the coded system would be the same BER that the uncoded system achieved at an SNR of 33 dB. The power of the coding gain is that it allows a communications system to either maintain a desired BER at a lower SNR than was possible without coding, or achieve a higher BER than an uncoded system could attain at a given SNR.

Reed-Solomon codes

RS codes first appeared in technical literature in 1960. Since their introduction, they have seen widespread use in a variety of applications. These applications include interplanetary communications (e.g., the Voyager spacecraft), CD audio players, and countless wired and wireless communications systems.

RS codes belong to the family known as *block codes*. This family is so named because the encoder processes a block of message symbols and then outputs a block of codeword symbols. This method is in contrast to the other major coding family known as *convolutional codes*. Instead of processing message symbols in discrete blocks, a convolutional encoder works on a continuous stream of message symbols and simultaneously generates a continuous encoded output stream. These codes get their name because the encoding process can be viewed as the convolution of the message symbols and the impulse response of the encoder.

To be specific, RS codes are non-binary systematic cyclic linear block codes. Non-binary codes work with symbols that consist of several bits. A common symbol size for non-binary codes is 8 bits, or a byte. Non-binary codes such as RS are good at correcting burst errors because the correction of these codes is done on the symbol level. By working with symbols in the decoding process, these codes can correct a symbol with a burst of eight errors just as easily as they can correct a symbol with a single bit error. A systematic code generates codewords that contain the message symbols in unaltered form. The encoder applies a reversible mathematical function to the message symbols in order to generate the redundancy, or parity, symbols. The codeword is then formed by appending the parity symbols to the message symbols. The implementation of a code is simplified if it is systematic. A code is considered to be cyclic if a circular shift

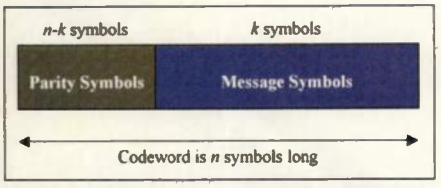

Figure 1. Structure of an (n, k) Reed-Solomon code word.

of any valid codeword also produces another valid codeword. Cyclic codes are popular because of the existence of efficient decoding techniques for them. Finally, a code is linear if the addition of any two valid codewords also results in another valid codeword.

Galois Fields

The theory of error control codes uses a mathematical construct known as finite fields or Galois Fields (GFs). A GF is a set that contains a finite number of elements. The operations of addition and multiplication on this set are defined and the operations behave as would be expected from normal arithmetic. For example, the additive identity element is 0 and the multiplicative identity element is 1. A more rigorous mathematical definition of GFs is beyond the scope of this article but the references contained at the end of this article will provide the interested reader with a good starting point. For the sake of brevity, our discussion of GFs will be limited to what the reader needs to know in order to actually implement an encoder/decoder.

RS codes operate on GFs of order $q = p^m$ where p is a prime positive integer and m is a positive integer. A GF of order q is denoted by GF(q) and it contains q distinct elements. A typical value of q in practical RS systems is $q = 256$. The elements of a GF are typically denoted using the variable α. The elements of GF(8) are shown in Table 1 using different notations. Each line in the table corresponds to a single element in the field. Elements are typically represented using either power or polynomial notation when performing calculations by hand, but binary notation is used when the codes are actually implemented in hardware. All three notations are simply three different ways to represent a given GF element. Multiplication is easier in power notation because the exponents are added. Similarly, addition is easier in polynomial notation.

Numerous books and computer programs exist that list or generate the elements for GFs of various sizes. To implement an RS encoder and decoder, two special hardware blocks will be needed: a GF adder and a GF multiplier.

Galois Field adder

The adder computes the sum of two GF elements by XORing the corresponding bits of each symbol together. For example, the sum of α^3 and α^5 can be found, by hand, using polynomial notation. α^3 is equivalent to $X + 1$ and α^5 to $X^2 + X + 1$. Because of the modulo properties of GFs, addition is the same as subtraction. Thus, $X + X = X - X = 0$. Keeping this property in mind, the addition of α^3 and α^5 can be written as follows:

$$\begin{aligned}&(X + 1) + (X^2 + X + 1)\\ &= X^2 + (X + X) + (1 + 1)\\ &= X^2 + (0) + (0)\\ &= X^2\end{aligned}$$

Thus $\alpha^3 + \alpha^5 = \alpha^2$. This operation would be computed in hardware by XORing the bits of the two symbols together as follows:

$$\begin{aligned}&011 + 111\\ &(0 \text{ XOR } 1)(1 \text{ XOR } 1)(1 \text{ XOR } 1)\\ &= (1)(0)(0)\\ &= 100\end{aligned}$$

Note from the table that the binary notation 100 corresponds to the power notation α^2 found by hand calculations.

Galois Field multiplier

A simple, but inefficient, way to implement a GF multiplier is to take

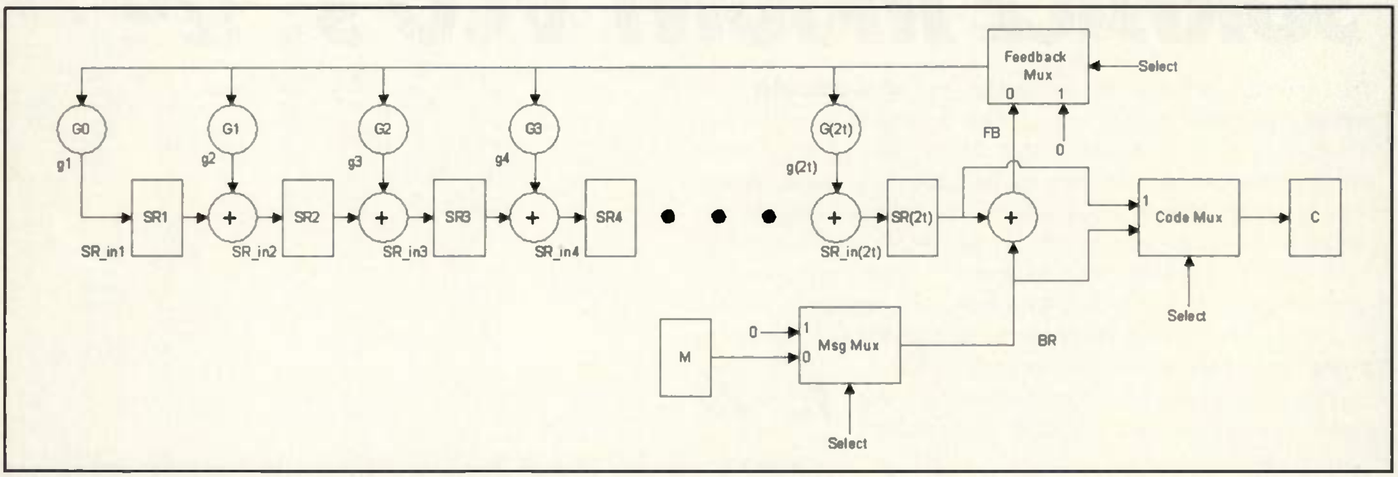

Figure 2. Hardware architecture for a Reed-Solomon encoder (signal names are for effect only).

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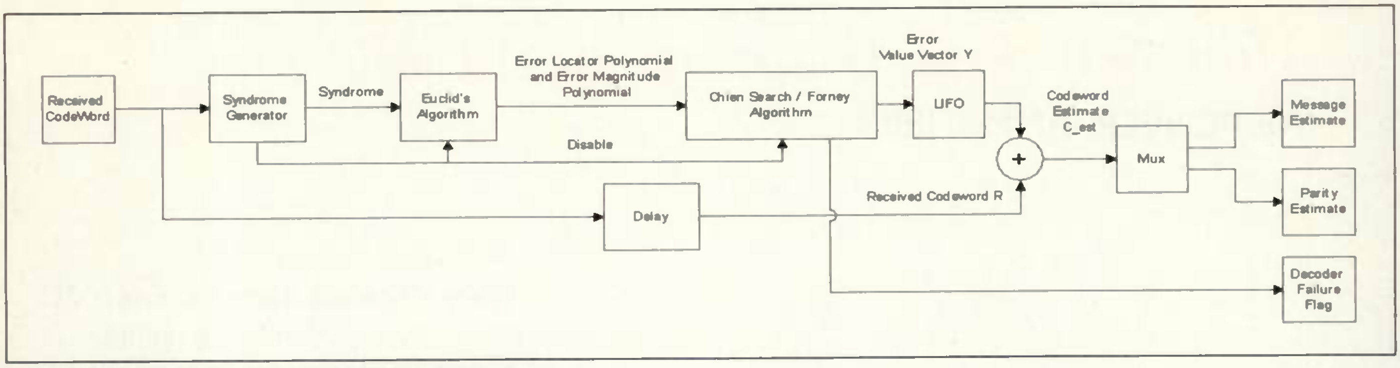

Figure 3. Top-level block diagram of Reed-Solomon decoder.

the inputs in binary notation and use a lookup table to find their corresponding power notations. The powers can be added (e.g., $\alpha^2 \times \alpha^5 = \alpha^7$) and the result can be sent to an inverse lookup table to find the corresponding binary notation for the output. These lookup tables can be stored in read-only memory (ROM), but that is not practical because several multiplier outputs will typically need to be computed during a single clock cycle.

A more efficient solution is to compute the equations by hand and simplify the terms. An RS encoder needs fixed multipliers that multiply an arbitrary input by a constant value such as α^2. The RS decoder needs both fixed multipliers as well as generic multipliers that are capable of multiplying any two arbitrary numbers together. The following example will show how to derive the equations for a fixed multiplier that multiplies its input by α^2.

Denote an arbitrary 3-bit multiplier input by $b_2\alpha^2 + b\alpha + b_0$. The multiplier will multiply this input by the constant α^2:

$$(b_2\alpha^2 + b_1\alpha + b_0)\alpha^2$$
$$= b_2\alpha^4 + b_1\alpha^3 + b_0\alpha^2$$

Recall from Table 1 that $\alpha^4 = X^2 + X$ and $\alpha^3 = X + 1$. By replacing X with α and substituting the result back into the above equation, it can be rewritten as:

$$= b_2(\alpha^2 + \alpha) + b_1(\alpha + 1) + b_0\alpha^2$$
$$= (b_2 + b_0)\alpha^2 + (b_2 + b_1)\alpha + b_1$$

The above equation represents the simplified equation for multiplying an arbitrary input by α^2. For example, the most significant bit (MSB) of the multiplier output is computed by XORing the input bits b_2 and b_0 together. The derivation for the generic multiplier can be found by simplifying the equations after using two arbitrary values for the inputs.

Code parameters

A given Reed-Solomon code is indicated by referring to it as an (n, k) code. The parameter n indicates the codeword length in terms of the number of symbols in the codeword. The parameter k indicates the number of message symbols in the codeword. The number of parity symbols added is thus $n - k$. Figure 1 illustrates the structure of an RS codeword. The error-correcting capability of the code is $t = (n - k)/2$. The code can detect and correct T errors where $0 \leq T \leq t$.

Reed-Solomon encoder

The purpose of the encoder is to generate the codeword based on the message symbols. Because RS is a systematic code, the n message symbols are transmitted as is and the $n - k$ parity symbols are appended to the message symbols to form the code word. The values of the parity symbols depend on the message symbols and they add redundancy to the transmitted codeword. This redundancy is exploited at the receiver

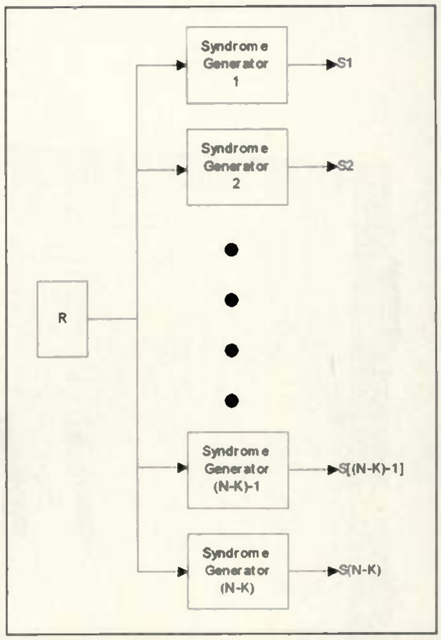

Figure 4. Syndrome is computed using n - k = 2t Syndrome Generators in parallel.

i	g	r	q	r'_{i-1}	ax	b
-1	0	$x^{2t} = x^6$				
0	1	$S(x) = \alpha^{14}x^5+\alpha^{10}x^4+\alpha^3x^3+\alpha^7x^2+\alpha^9x+\alpha^{12}$		$\alpha^{11}x^5+\alpha^4x^4+\alpha^8x^3+\alpha^{10}x^2+\alpha^{13}x$		
1	$\alpha x+\alpha^{12}$	$\alpha^3x^4+\alpha^2x^3+\alpha^2x^2+x+\alpha^9$	$\alpha x+\alpha^{12}$	$\alpha^9x^4+\alpha^8x^3+\alpha^8x^2+\alpha^6x+\alpha^{12}$	αx	α^{12}
2	$\alpha^{12}x^2+\alpha^{11}x+\alpha^{14}$	α^{11}	$\alpha^{11}x+\alpha^6$		$\alpha^{11}x$	α^6

Table 2. Example of Euclid's algorithm in GF(16). At the end, $\Lambda = \alpha^{12}x^2 + \alpha^{11}x + \alpha^{14}$ and $\Omega = \alpha^{11}$.

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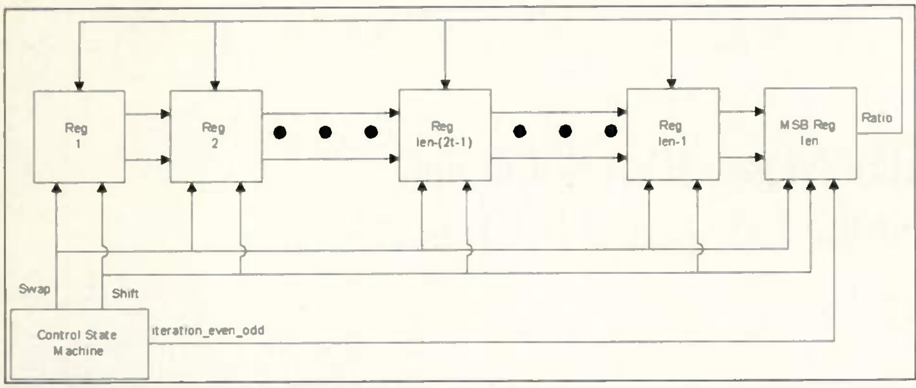

Figure 5. Top-level of Euclid block.

to detect and correct errors.

The parity symbols are computed by performing a polynomial division using GF algebra. The steps involved in this computation are as follows:

- Multiply the message symbols by X^{n-k} (This shifts the message symbols to the left to make room for the $n-k$ parity symbols)
- Divide the message polynomial by the code generator polynomial using GF algebra.
- The parity symbols are the remainder of this division. These steps are accomplished in hardware using a shift register with feedback. The architecture for the encoder is shown in Figure 2.

The encoder first clocks the k message symbols from the message input M into the shift register and simultaneously clocks them out as the first k symbols of the codeword. Once the last message symbol is clocked into the shift register, the $n - k$ parity bytes are located in the shift registers $SR1$ through $SR(2t)$. The rest of the codeword is formed by clocking each of the $n - k$ parity bytes out of the shift register to the codeword output C.

Three muxes are used in the encoder (Msg Mux, Feedback Mux, and Code Mux) and all three are controlled by the same *Select* signal. *Select* is 0 for the first k cycles starting with the cycle that the first message symbol is clocked in, and it is 1 for the remaining $n - k$ clock cycles.

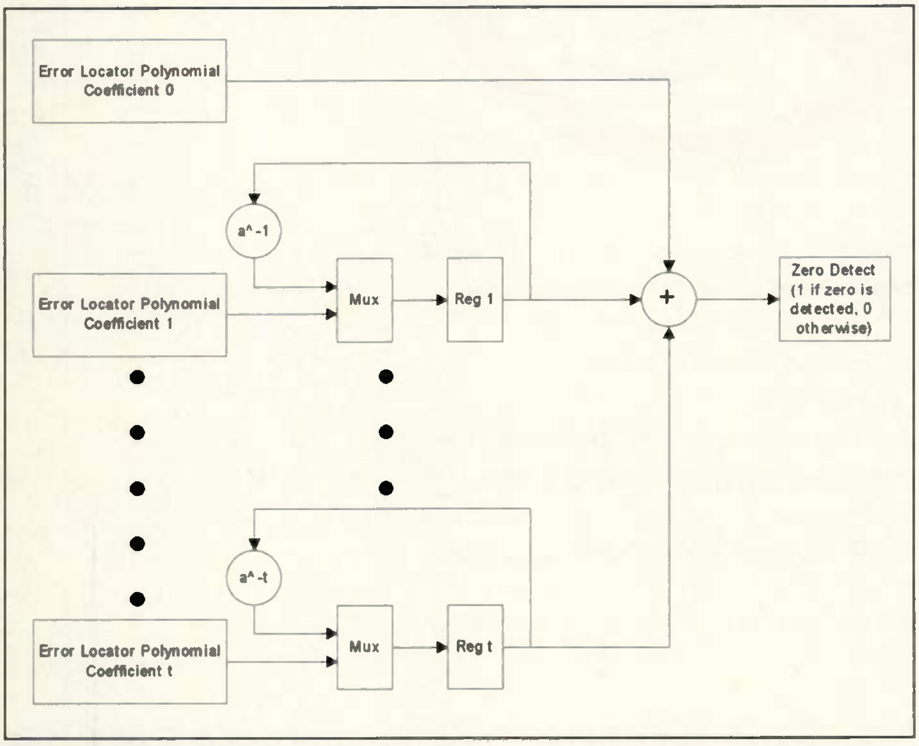

Figure 6. Chien Search block searches the error locator polynomial Λ(x) to find the roots. A 1 is sent out when a root location is found, and a 0 is sent out otherwise. The locations of the 1s correspond to the error locations x_i.

Reed-Solomon decoder

The purpose of the decoder is to process the received code word to compute an estimate of the original message symbols. There are three main blocks to the decoder: the Syndrome Generator, Euclid's Algorithm, and the Chien/Forney block. The output of the Chien/Forney block is an estimate of the error vector. This error vector is then added to the received codeword to form the final codeword estimate. A top-level block diagram of the decoder is shown in Figure 3. Note that the error value vector Y comes out of the Chien/Forney block in reverse order, and it must pass through a last-in, first-out (LIFO) block before it is added to the received codeword $R(x)$.

Syndrome generator

The first step in the decoder is to compute the syndrome. The syndrome consists of $n - k$ symbols and the values are computed from the received code word. The syndrome depends only on the error vector, and is independent of the transmitted code word. That is, each error vector has a unique syndrome vector. However, many different received code words will have the same syndrome if their error pattern is the same.

The purpose of computing the syndrome first is that it narrows the search for the actual error vector. Originally, a total of 2^n possible error vectors would have to be searched. However, by finding the syndrome first, this search is narrowed down to looking at just 2^{n-k} possibilities.

The syndrome can be computed mathematically by dividing the received code word by the generator polynomial

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using GF algebra. The remainder of this division is called the syndrome polynomial $s(x)$. The actual syndrome vector $S(x)$ is computed by evaluating $s(x)$ at α through α^{n-k}. However, this method is not efficient from a hardware standpoint. The alternative method typically used in hardware is to directly evaluate the received code word $R(x)$ at α through α^{n-k}.

The Syndrome Generator module computes the syndrome S by evaluating the received code word $R(x)$ at α through α^{n-k}. That is, $R(\alpha)$ through $R(\alpha^{n-k})$. In the RS code $n - k = 2t$, and thus there are $2t$ syndrome values to compute: [$S1$ $S2$ $S3 \ldots S(2t)$]. These values are computed in parallel as shown in Figure 4. The first syndrome generator evaluates the received code word at α to form $S1$, the next generator evaluates the received code word at α^2 to form $S2$, and so on.

The Syndrome Generator module will also contain hardware that checks for an all-zero syndrome. If all of the syndrome values are zero, then there are no errors and the Euclid's algorithm block and the Chien/Forney block are disabled. The received code word then becomes the codeword estimate.

Euclid's algorithm

Euclid's algorithm processes the syndrome S(x) to generate the error locator polynomial $\Lambda(x)$ and the error magnitude polynomial $\Omega(x)$. That is, it solves the following equation that is referred to as the Key Equation:

$$\Lambda(x)\,[1 + S(x)] = \Omega(x) \bmod x^{2t+1}$$

The algorithm used in RS decoding is based on Euclid's algorithm for finding the greatest common devisor (GCD) of two polynomials. Euclid's algorithm is an iterative polynomial division algorithm (for the actual steps, contact the author).

Hardware implementation

The top-level block diagram of the Euclid's algorithm block is shown in Figure 5. This architecture uses two types of registers. Each of the registers contains two sets of internal registers. These register sets are referred to as A and B (upper and lower registers, respectively). The number of registers is $len = 2t + 10$.

After the syndrome values are computed, the Euclid block begins its processing. The control state machine is responsible for controlling the operation of the block. Each register set (A and B) will contain two polynomials. These polynomials are stored such that their most significant coefficients are on the right, and their least significant coefficients are on the left (for the precise steps performed by the blocks, contact the author).

Chien Search

Once the error locator polynomial $\Lambda(x)$ has been computed, it needs to be evaluated to find its roots. The Chien Search (CS) algorithm is used to find these roots (see Figure 6). The CS is a brute force algorithm that evaluates the polynomial for all possible input values, and then checks to see which outputs are equal to zero. If an error occurs in posi-

tion i, then the following equation equals zero:

$$\sum_{j=0}^{t} \Lambda_j \alpha^{-ij} = 0$$

where $i = 0 .. (n-1)$

The CS evaluates the above equation for all the values of i and j and counts the number of times that the equation is equal to zero. The locations of the zeros are the error locations, and the number of zeros is the number of symbols in error.

There are $(t + 1)$ stages of the CS that are implemented in hardware. Each of these stages (where a stage consists of a multiplier, mux and register) represents a different value for j in the above CS equation. The search is run for n clock cycles (each clock cycle represents a different value of i in the above equation) and the output of the adder is examined to see if it is equal to zero. If it is equal to zero, the Zero Detect block will output a 1, otherwise, it will output a zero. The output of the Chien Search block is thus a string of n bits that have values of either 0 or 1. Each 1 represents the location of a symbol in error.

For the first clock cycle, the mux will route the error locator polynomial coefficient into the register. For the remaining $(n-1)$ clock cycles, the output of the multiplier will be routed via the mux into the register. The exponents of the multipliers have negative values. However, these values can be precomputed using the modulo operator. The exponent of $\alpha - i$ is equal to $(-i \text{ modulo } n) = (-i \text{ modulo } 255)$. For example, α^{-1} equals α^{254}, α^{-2} equals α^{253}, and so on.

Forney algorithm

The Forney algorithm is used to compute the error values Y_i. To compute these values, the Forney algorithm needs the error locator polynomial $\Lambda(x)$ and the error magnitude polynomial $\Omega(x)$. The equation for the error values is:

$$Y_i = \frac{\Omega(x)}{\Lambda'(x)}$$

for $x = \alpha^{-i}$ where α^{-i} is a root of $\Lambda(x)$

The computation of the formal derivative $\Lambda'(x)$ is actually quite simple, as will be demonstrated in the following example. Assume $\Lambda(x) = \alpha^4X^3 + \alpha^3X^2 + \alpha X + \alpha^2$. $\Lambda'(x)$ thus equals:

$$\sum_{j=0}^{t} \Lambda_j \alpha^{-ij} = 0$$

The derivative is formed by taking the coefficients of the odd powers of X, and assigning them to the next lower power of X (which will be even). However, in hardware, it is actually easier to find $x\Lambda'(x)$. This x has the effect of shifting the derivative coefficients to the next higher power of X (i.e., the power of X that the coefficient originally belonged to). Thus, the denominator of the Forney algorithm is found as follows using the same $\Lambda(x)$ as the above example.

$$x\Lambda'(x) = \alpha^4X^3 + \alpha^3X^2 + \alpha X + \alpha^2$$
$$= \alpha^4X^3 + 0X^2 + \alpha X + 0$$
$$= \alpha^4X^3 + \alpha X$$

In hardware, this $x\Lambda'(x)$ term is found by zeroing out every other term of the original $\Lambda(x)$ polynomial. If the denominator of the Forney equation is modified by multiplying by the x term, then the numerator must also be multiplied by x in order for the equation to still work. Thus, the actual Forney equation implemented in hardware is:

$$Y_i = \frac{x\Omega(x)}{x\Lambda'(x)}$$

The $x\Omega(x)$ polynomial is then evaluated along with the $x\Lambda'(x)$ polynomial using the same type of hardware as used for the CS. However, in order to form $x\Omega(x)$, the coefficients of $\Omega(x)$ are shifted to the left by one location. To evaluate $\Omega(x)$, the Ω_0 coefficient would be added with the Ω_1 coefficient times α^{-1}, the Ω_2 coefficient times α^{-2} all the way up to the Ω_t coefficient times α^{-t}. To evaluate $x\Omega(x)$, the Ω_0 coefficient is multiplied by α^{-1}, the Ω_1 coefficient by α^{-2} all the way up to multiplying the Ω_t coefficient times $\alpha^{-(t+1)}$. The output of these multipliers is then summed.

The numerator is then multiplied by the denominator using an inverse multiply. The inverse multiply contains a lookup table that finds the inverse of the denominator. For example, if the denominator was α^3, the inverse is α^{-3}. This can then be expressed as:

$$\alpha^{-i} = \alpha^{(-i \bmod n)} = \alpha^{(-3 \bmod 255)} = \alpha^{252}.$$

continued on page 88

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An 802.11 DSSS system simulation

Cost, time-to-market and reliable design are important factors in the competitive unlicensed product market. Accurately modeling these products is a must in meeting the low-cost challenge.

By Stephen H. Kratzet

Simulating parameters for hardware modeling before manufacture is no longer an option in today's cost-competitive environments. High speed computers and complex software make modeling reliable, efficient, and accurate.

Modeling and simulating the RF sections of an 802.11 direct-sequence, spread-spectrum (DSSS) system, Bluetooth, HomeRF, or other unlicensed product is an excellent way to minimize design errors, reduce the product development time and contain costs.

Designers encounter many issues, problems and procedures working with 802.11 DSSS RF subsystems.

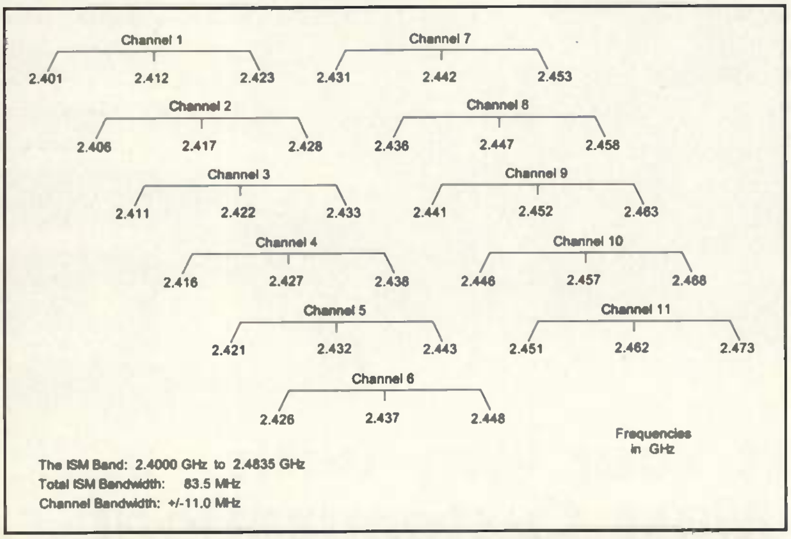

Figure 1. The IEEE 802.11 specification designates 11 22-MHz-wide channels for DSSS WLANs.

For reference, the filters, amplifiers, and mixers used in this system simulation have their parameters set to values representative of a commercially available wireless local-area network (WLAN) chip set.

Preface: pertinent IEEE 802.11 specifications

The 802.11 specification allows a data rate of 1.0 Mb/s or 2.0 Mb/s. A 1.0 Mb/s differential binary phase shift keying (DBPSK) modulation is used here. A Barker spreading code of 11.0 Mb/s is used for each of the data bits, which is a ratio of 11:1 (Barker code vs. data). This results in a channel width of 22 MHz.

The transmitter conforms to the IEEE 802.11 spectral mask requirements for transmission. The side lobes are at least 30 dB down from the main lobe. The output power to one of the 11 possible channels is +17.5 dBm.

ISM band channels for direct sequence

The simulated system uses most of the ISM band from 2.4 GHz to 2.4835 GHz. Figure 1 shows 11 22-MHz-wide channels that cover the range of 2.401 GHz to 2.473 GHz. The channels are on 5.0 MHz centers.

In a multiple-cell network topology, overlapping and/or adjacent cells using different channels can operate simultaneously without interference if the spacing between the center frequencies is at least 30 MHz. Europe and Japan each have a different frequency allotment in the ISM band.

(Note: An entirely different specification, 802.11b, allows 25 MHz channel spacing and allows two additional data rates of 5.5 and 11.0 Mb/s, using eight-chip complementary code keying (CCK) instead of the Barker code.)

802.11 system overview

In Figure 2, the transmit in-phase and quadrature (Tx_I and Tx_Q) digital signal level inputs are applied to the modulator IC. The rate of these I and Q signals is 11.0 Mb/s. In the modulator IC, the I and Q inputs pass through a 7.7 MHz, five-pole, lowpass Butterworth filter to provide pulse shaping and control of spectral mask. The filtered I and Q signals are then applied to a quadrature modulator. (In reality, the local oscillator (LO) for the quadrature modulator is external to the IC, but this example shows the LO as if it were part of the IC.) The quadrature-modulated 280 MHz IF signal exits the IC to pass through a 17 MHz-wide surface acoustic wave (SAW) bandpass filter before entering the up-converter IC. After the up-conversion to 2.442 GHz, there are several filters and amplifiers in the chain before the RF is sent to the transmitter antenna.

At the receiver, several filters and amplifiers exist before the 2.442 GHz RF is down-converted to a 280 MHz receiver IF. A second 17-MHz-wide SAW filter is used before the IF enters the quadrature demodulator IC. Once inside the IC, the IF is applied to a pair of limiting amplifiers before going to the quadrature demodulator. A two-pole LC filter exists between the limiting amplifiers. The demod-

continued on page 44

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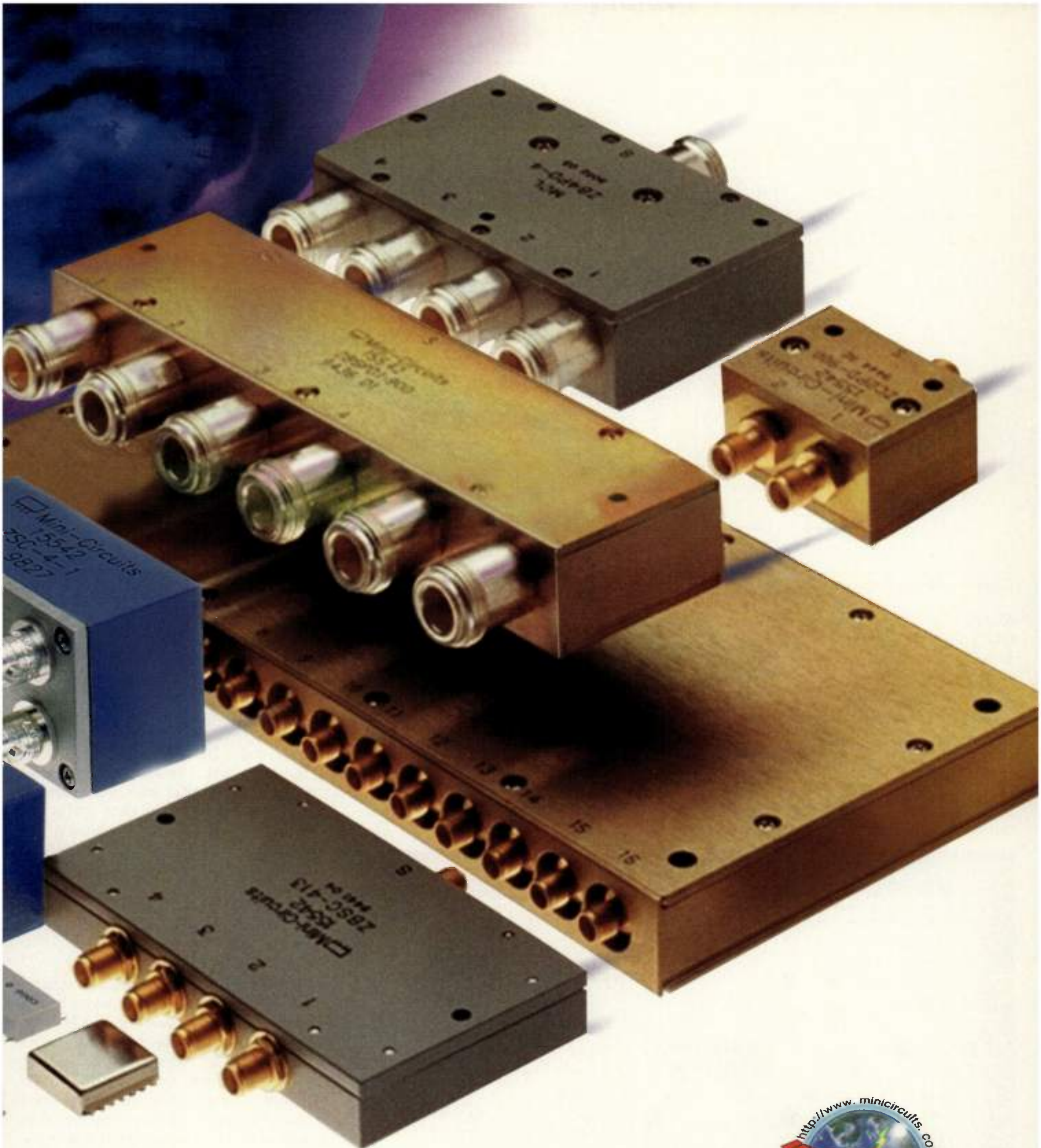

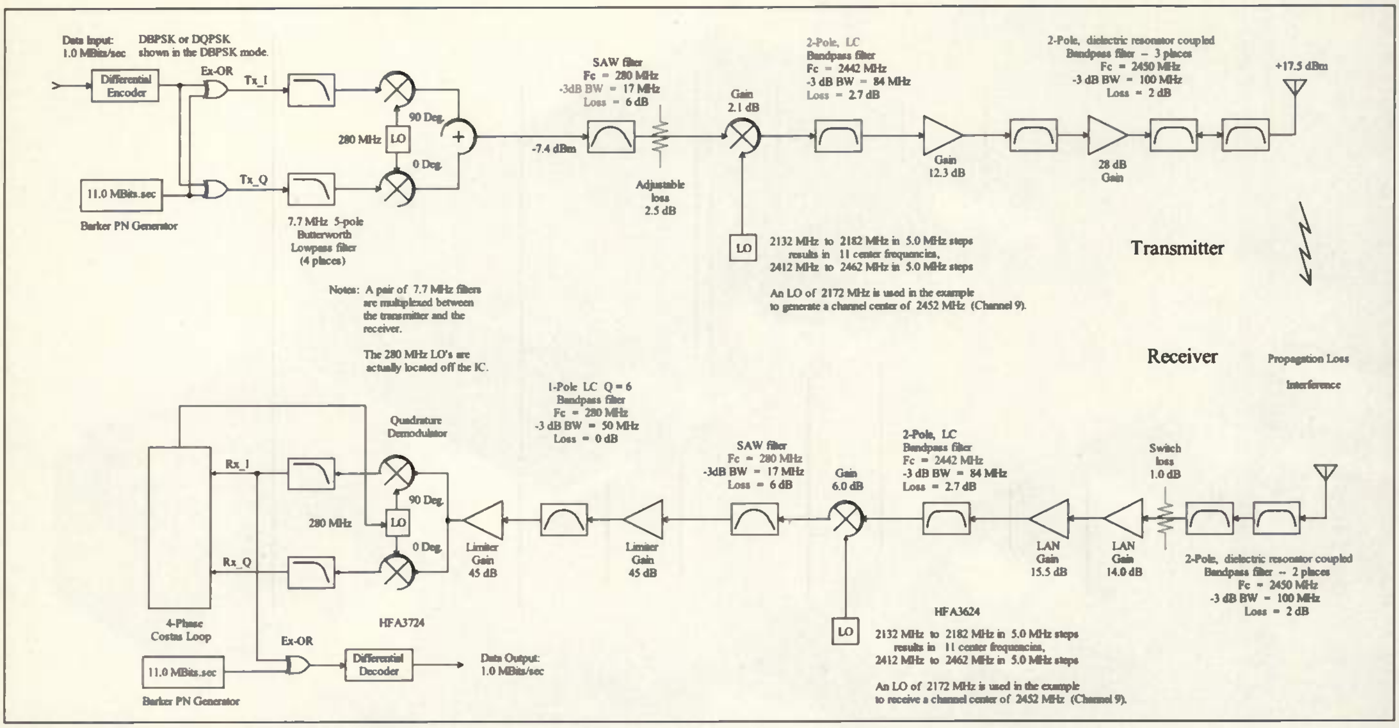

Figure 2. A block diagram of the 802.11 system.

ulated receive in-phase and quadrature (Rx_I and Rx_Q) signals are then filtered by the same pair of 7.7 MHz lowpass filters that were used in the transmitter section of the IC.

The Rx_I and Rx_Q are normally connected to a third IC, a baseband processor. However, it will not be used in this example. Instead, the receiver's quadrature demodulator will become part of a four-phase Costas loop. The demodulated Rx_I data are then processed by an exclusive-OR gate and differential decoder.

PN data and Barker code generation

In Figure 3, the output of the data PN token 0 represents the 1.0 Mb\s data input to the system. It is connected to a differential encoder comprised of an exclusive-OR gate and a delay token. The delay time is equal to the width of 1 bit, 1.0 µsec for 1.0 Mb/s. The other input to each exclusive-OR gate is an 11.0 Mb/s Barker code. The exclusive-OR gate will spread the data by modulating it with the Barker code.

Token 113 is a metasystem that generates a Barker PN code sequence having a rate of 11.0 Mb/s. The 11-bit Barker code, 10110111000, has special properties for use in a correlation process. The Barker code generator is an 11-bit shift register that shifts the data pattern as required. As shown, the Tx_I and Tx-Q signals are identical. The input signals are delayed in time so they will line up with the receiver's output.

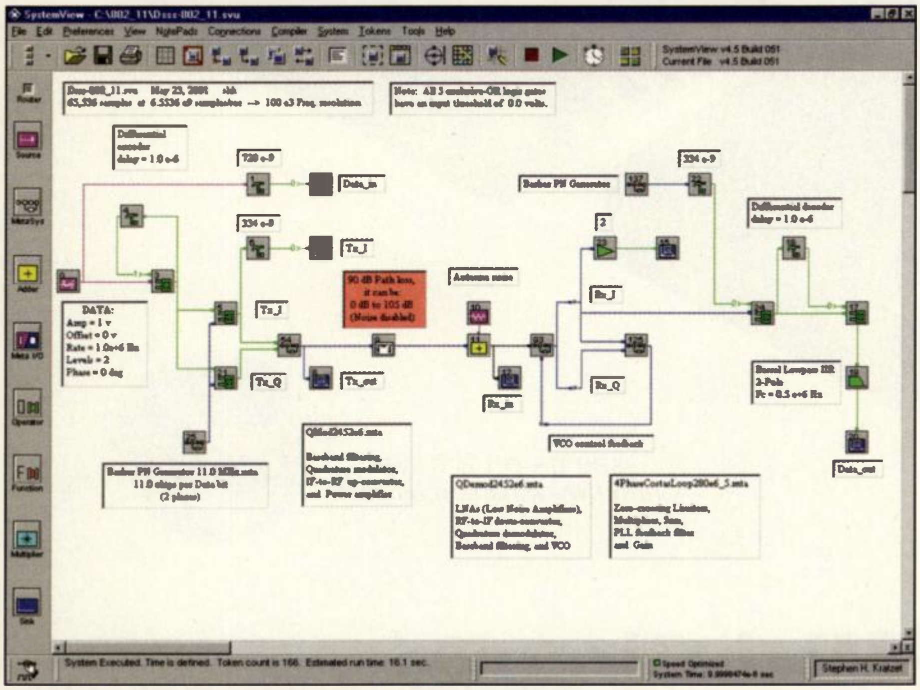

Figure 3. An overall view of the 802.11 system, DSSS-802_11.svu.

Baseband pulse shaping and the quadrature modulator

The transmitter portion of the system is contained in the metasystem token "Qmod2452e6.mta" (see Figure 4).

The first thing the I and Q inputs see is a quadrature modulator, "QMod280e6.mta" (see Figure 5). The modulator accepts digital signal level "I" and "Q" inputs that are connected to a pair of NOT gates operating as non-inverting buffers. The two buffer tokens are used to simulate the input comparators on the IC. The buffers output square waves before any filtering takes place. This output drives the filters at a constant 550 mV peak-to-peak. The 7.7 MHz, five-pole Butterworth filters are used to reduce the side lobes to about 36 dB below the main lobe at the output of the modulator. These filters are used to meet the IEEE

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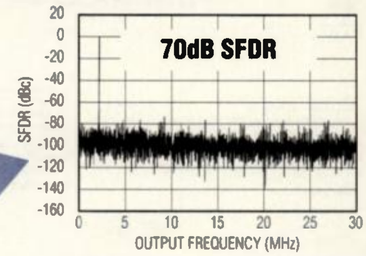

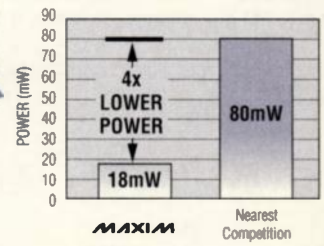

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MAX5181/MAX5184	10	1	72	N/A	N/A	I_{OUT}/V_{OUT}
MAX5182/MAX5185	10	2 (Alternate Phase)	70	N/A	N/A	I_{OUT}/V_{OUT}
MAX5186/MAX5189	8	2 (Simultaneous)	58	±1	±0.2	I_{OUT}/V_{OUT}
MAX5187/MAX5190	8	1	60	N/A	N/A	I_{OUT}/V_{OUT}
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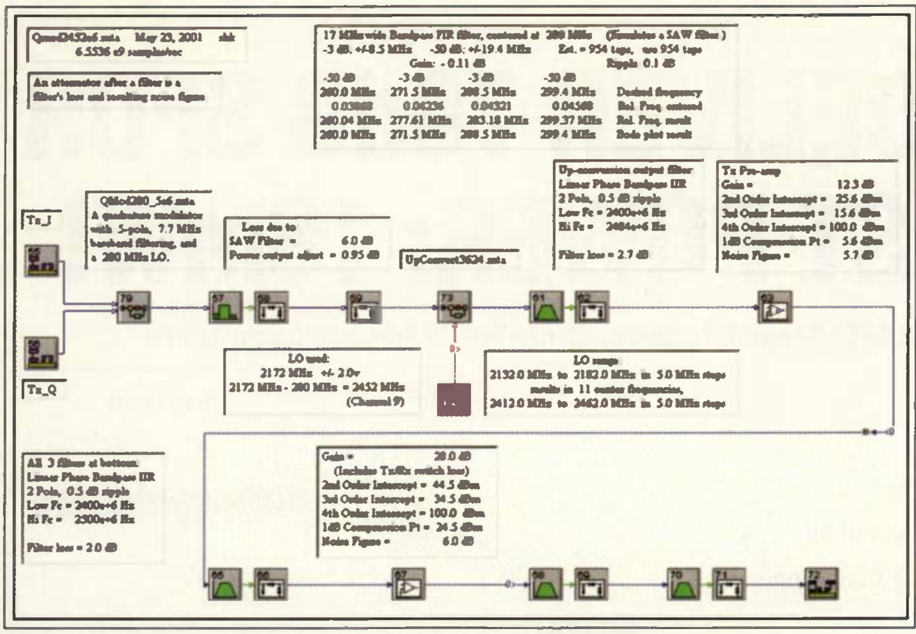

Figure 4. The quadrature modulator and IF-to-RF up-converter Qmod2452e6.mta.

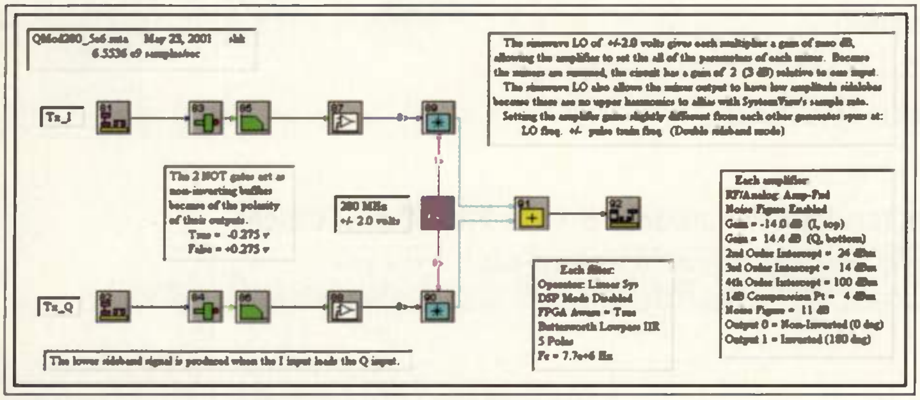

Figure 5. The quadrature modulator metasystem: Qmod280e6.mta.

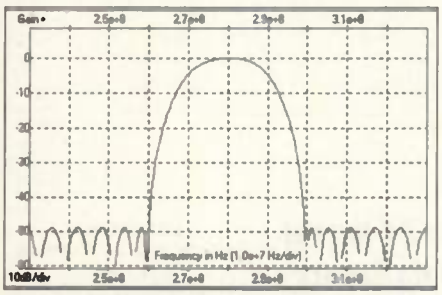

Figure 6. Frequency response of the 954-tap, FIR filter.

802.11 spectral mask requirements of a −30 dB side lobe maximum at the transmitter output. Downstream, the non-linearity of the various mixers and amplifiers will cause this −36 dB value to grow toward the −30 dB value.

Transmitter SAW filter simulation

The SAW filter is modeled by using a 954 tap, bandpass finite impulse response (FIR) filter. The frequency response of this filter is shown in Figure 6.

The output of the quadrature modulator goes to a SAW filter with a center frequency of 280 MHz, and a bandwidth of 17 MHz. The particular device chosen for this application has the following specifications, interpreted from their graphs:

Center frequency: 280.0 MHz
Loss at: −8.5 MHz = −3.0 dB
Loss at: +8.5 MHz = −3.0 dB
Loss at: −19.4 MHz = −50.0 dB
Loss at: +19.4 MHz = −50.0 dB
Passband ripple: = 1.0 dB
Insertion loss: = 10.0 dB max
Passband delay: = 0.234 µsec

The filter specification lists a maximum loss of 10.0 dB. An attenuator is used after the filter to insert a typical loss of 7 dB and the resulting noise figure into the system. This attenuator-after-filter plan is used for most of the filters in the system. The second attenuator after the FIR filter is used to adjust the power output of the channel to +17.5 dBm.

Transmitter IF-to-RF up-converter

After the FIR (SAW) filter, the 17-MHz-wide IF is up-converted to a 2.442 GHz RF carrier. A metasystem, TxUpConvert3624.mta (see Figure 7) uses the parameters from the data sheet for the desired mixer. Its gain plot may be seen in Figure 8. For the simulation, an analog two-pole, 0.5 dB linear phase filter is used.

Between the up-converter and the transmitter power pre-amp, there is a two-pole, LC bandpass filter with the following specifications:

Center frequency: 2.442 GHz
Loss at: −42.0 MHz = −3.0 dB
Loss at: +42.0 MHz = −3.0 dB
Loss at: −440.0 MHz = −20.0 dB
Loss at: +440.0 MHz = —
Passband ripple: 1.5 dB
Insertion loss: 2.7 dB max

Transmitter power pre-amp

The pre-amp is part of the same IC that has the IF-to-RF up-converter. It is followed by a two-pole filter. Between the transmitter power pre-amp and the power amplifier, there is a two-pole, dielectric resonator-coupled bandpass filter. An analog two-pole, 0.5 dB linear phase filter is used to simulate this filter. The bandpass filter, for RF LAN use, has the following specifications:

Center frequency : 2.450.0 GHz
Loss at: −50.0 MHz = −3.0 dB
Loss at: +50.0 MHz = −3.0 dB
Loss at: −280.0 MHz = −20.0 dB
Loss at: +280.0 MHz = —
Passband ripple —
Insertion loss: 2.0 dB max

A gain plot of this pre-amp output filter is similar to the filter in Figure 8. This same filter is used twice more in the path to the transmitting antenna.

Transmitter power amplifier

The power amplifier is a stand-alone IC. It is followed by two, two-pole filters, in series. The frequency spectrum at the transmitter's output is shown in Figure 9. The two nulls are ±11.0 MHz away from the 2.452 GHz center frequency. The side lobes are down about 30 dB relative to the peak. This completes the transmitter chain.

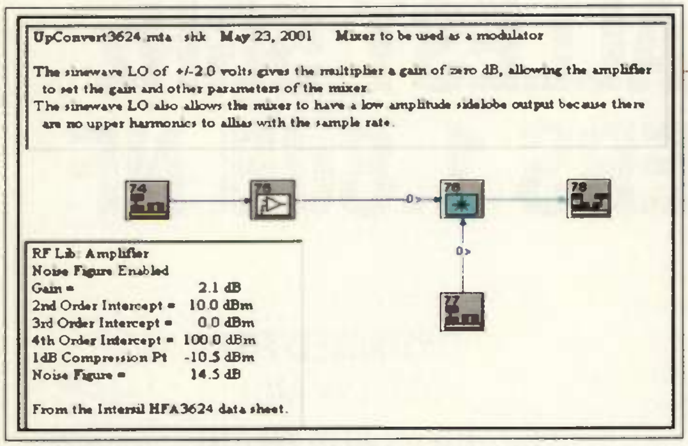

Figure 7. Transmitter IF-to-RF up-converter metasystem, UpConvert3624.mta.

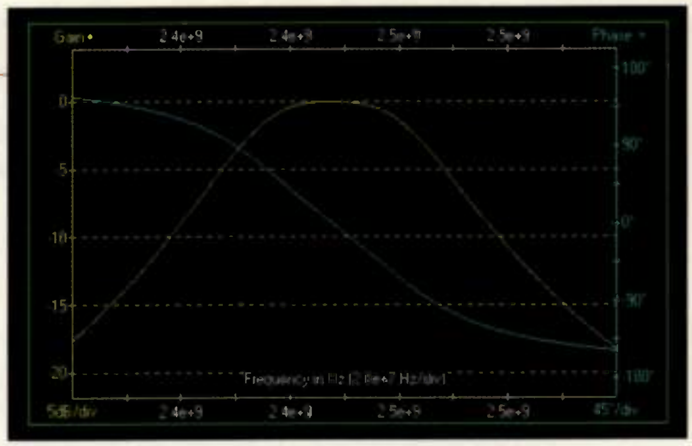

Figure 8. Bode plot of the two-pole up-converter output filter.

Path loss and antenna noise at the receiver's input

In Figure 3, an attenuator token, set to a loss of 90 dB, is used to simulate the path loss between the transmitter and receiver.

The receiver's input noise is modeled using an adder token with a thermal noise source token set as follows.

Resistance: 50Ω
Temp: 300° K

This noise represents a receiver with a front-end noise temperature of 300°K (27°C or 80.6°F) due to the antenna. This is also a convenient place to inject interference test signals.

Receiver input filters and LNAs

The input to the receiver (Figure 10, RxQdemod2442e6down.mta) uses the same two filters used at the transmitter's output. Also, there is a loss due to a Tx/Rx switch. Two low-noise amplifiers are in series; the second is an RF/IF converter IC.

As in the transmitter, there is another two-pole LC bandpass filter between the output of the second LNA and the input to the RF/IF converter IC. The LO for the active mixer uses a pulse train token. At the mixer's output there is a SAW (FIR) filter with a 280 MHz center frequency. It has the same specifications as the FIR filter in the transmitter.

The output of the FIR (SAW) filter goes to a pair of limiting amplifiers and then a quadrature demodulator (Figure 11, RxQdemod280e6_5.mta).

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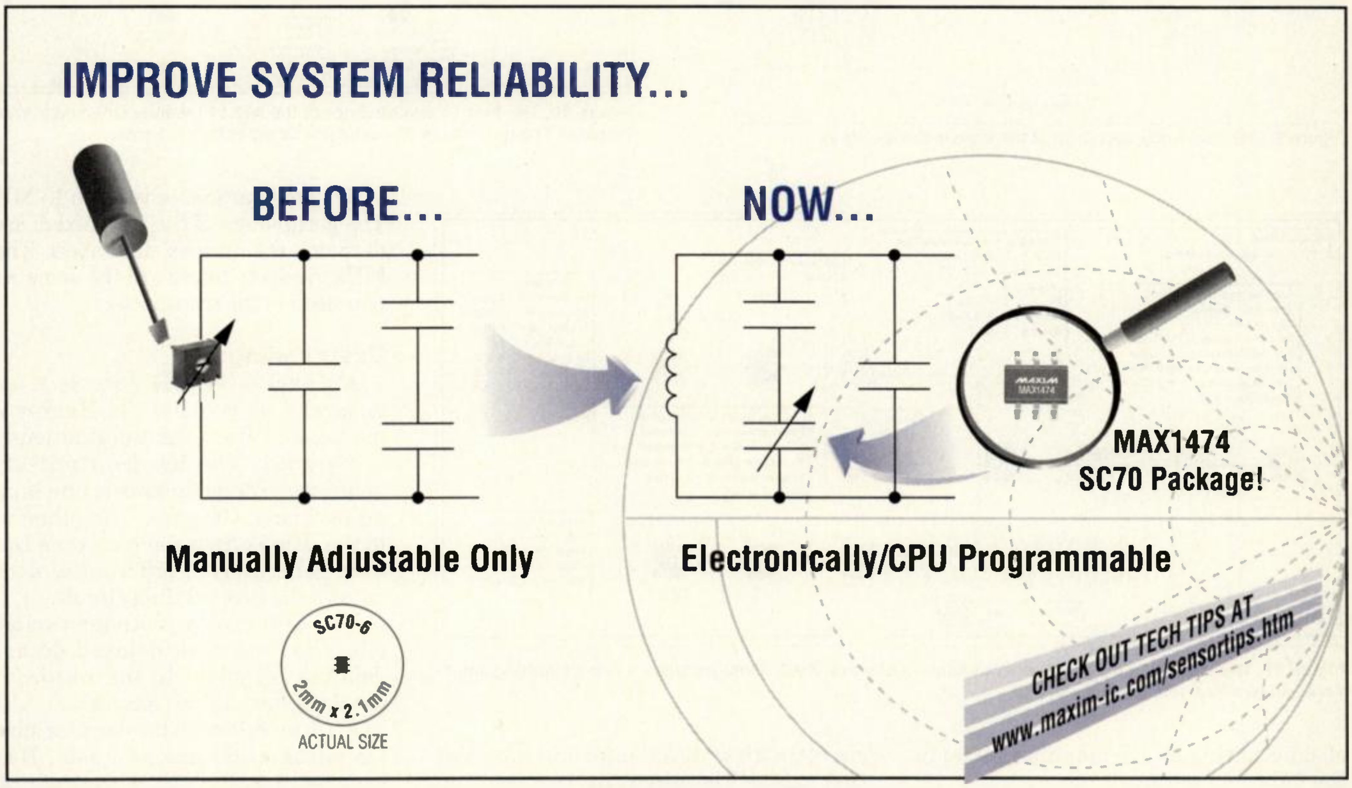

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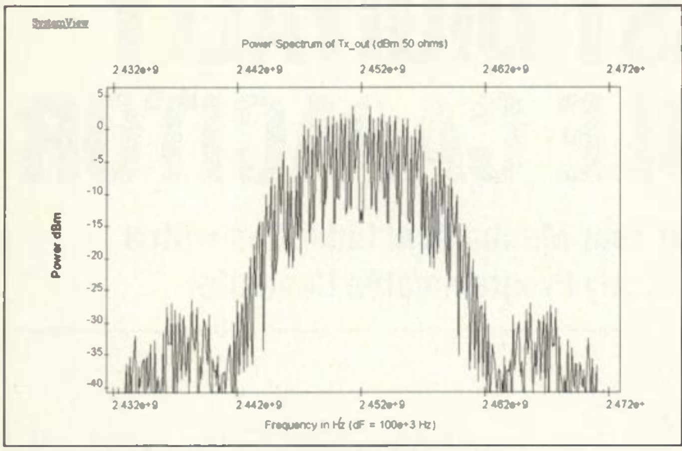


Figure 9. The frequency spectrum at the transmitter's output.

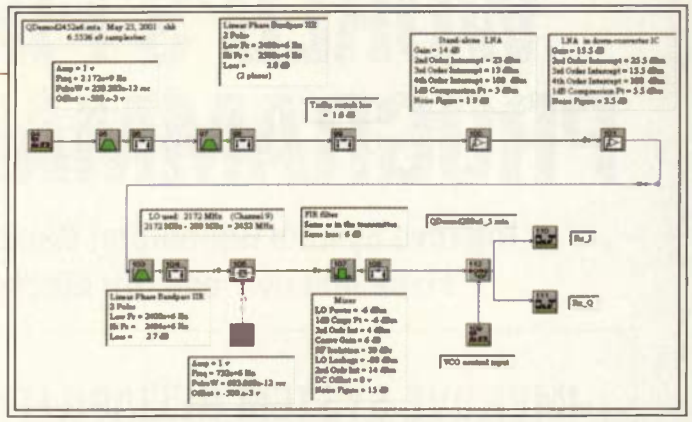


Figure 10. The first down-converter of the 802.11 receiver Qdemod2452e6.mta includes The quadrature demodulator Qdemod280e6_5.mta.

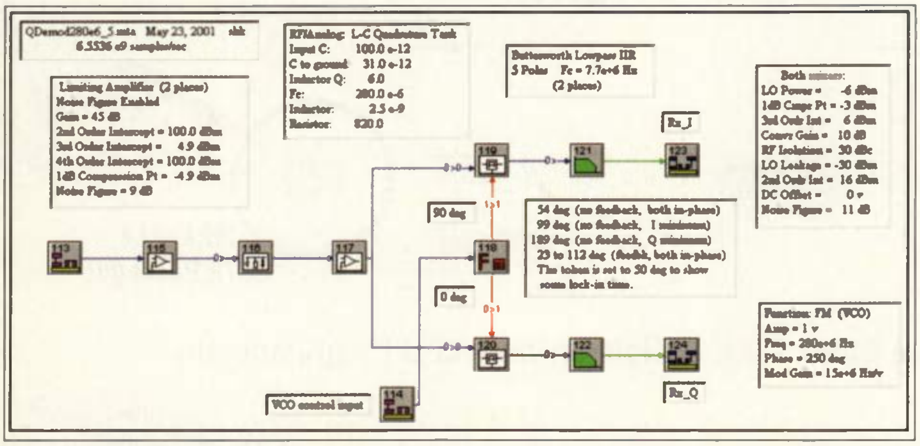


Figure 11. The receiver's quadrature demodulator Qdemod280e6_5.mta includes a pair of limiting amplifiers and two five-pole lowpass filters.

eled by setting an RF amplifier token to the following parameters:

Gain: 45.0 dB
3rd order Int: 4.9 dBm
N.F.: 9.0 dB
1 dB compression point: –4.9 dBm

The 1 dB compression point of –4.9 dBm gives a clipped output of ±200 mV. (The application note 9746 shows a LC circuit with a differential input/output that is used between the two limiting amplifiers.) A RF LC-quadrature tank token is used for this LC filter between the two amplifiers. The values in Figure 12 accomplish the task of a 48 MHz bandwidth (–3 dB) with some gain at the center frequency (Figure 13).

In Figure 11, the FM token is the voltage-controlled oscillator (VCO). The VCO's gain parameter is set to 15 MHz/V. The parameters of the two mixers are set to match the device's' data sheet. The 7.7 MHz, five-pole filters are the same as the pair used in the transmitter.

Despreading

An exclusive-OR gate is used to despread or remove the Barker code modulation from the information-bearing signal. The Rx_I output of the quadrature demodulator is one input to an exclusive-OR gate. The other input to the gate is from the receiver's Barker code generator. A differential decoder follows the despreading circuit.

The differential decoder exclusive-ORs the data with delayed data. The delay is set equal to the reciprocal of the data rate, 1.0 e^{-6} seconds.

A filter follows the decoder circuit. Its parameters are two-pole, Bessel, lowpass, 0.5 MHz (1/2 of the data rate).

The entire system will function without the differential encoder and decoder, however, the received data may or may not be inverted. This puts an unnecessary burden on the baseband processing. When the differential encoder and decoder are used, the data information will always have the correct polarity.

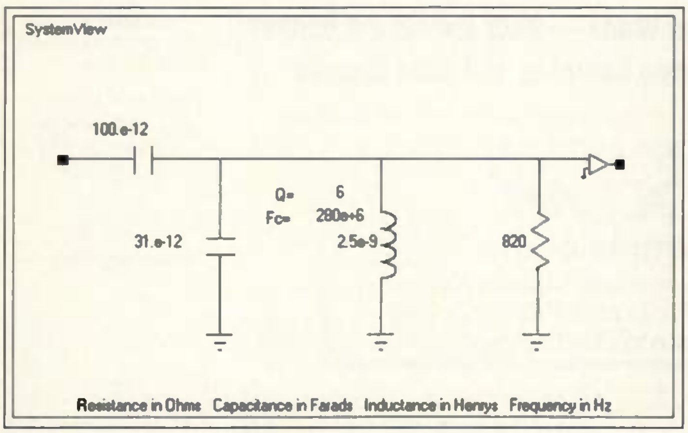


Figure 12. RF LC-quadrature tank token.

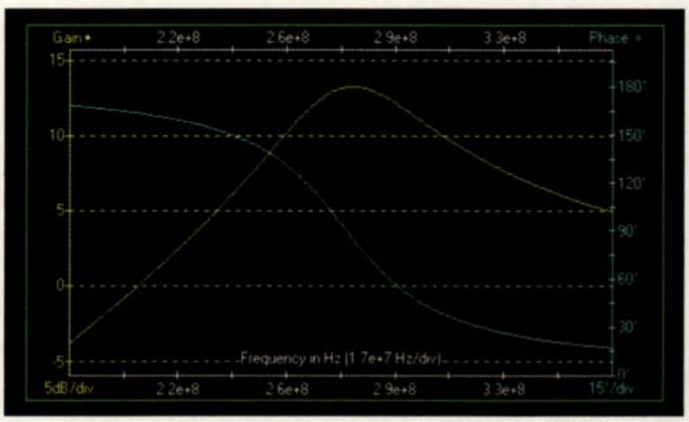
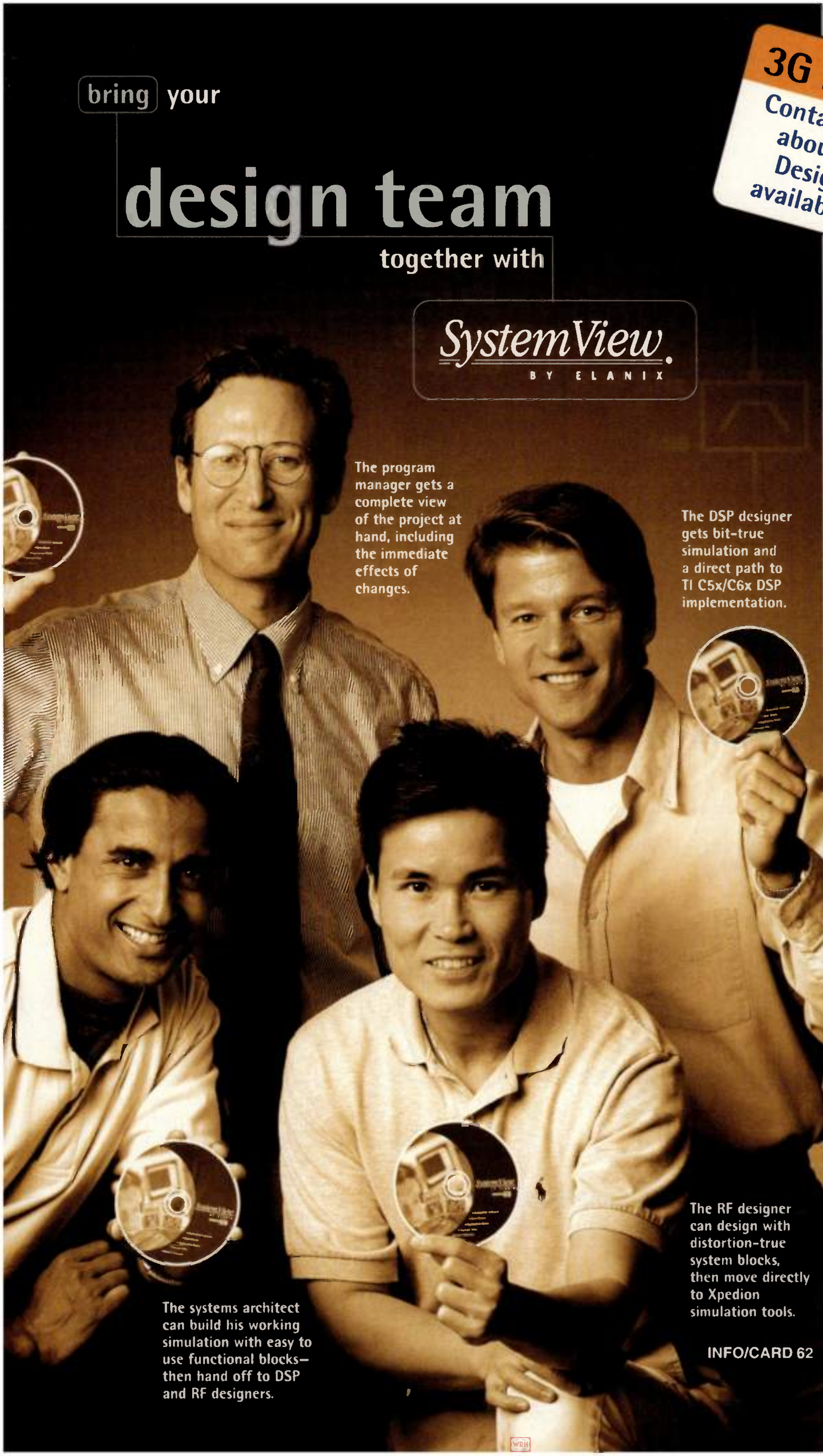


Figure 13. The bandpass center is 280 MHz with -3 dB points at 259 MHz and 307 MHz.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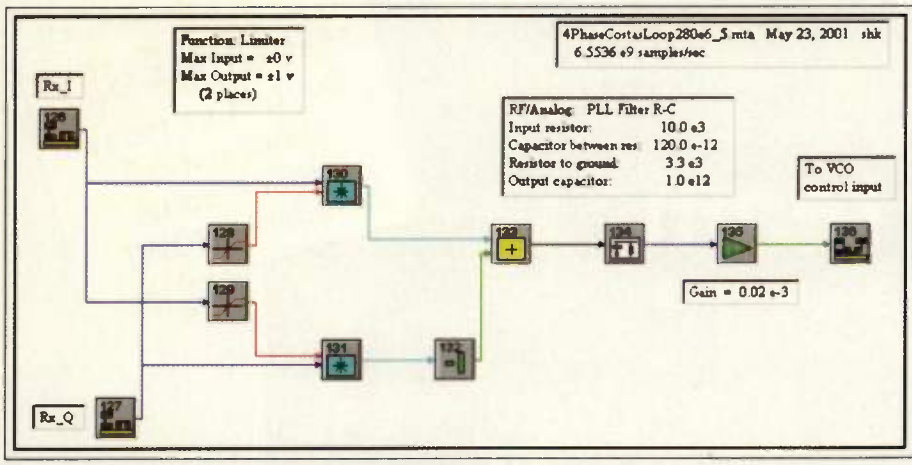

Figure 14. The four-phase Costas-loop demodulator phase detector metasystem 4Phase Costas Loop280e6_5.mta.

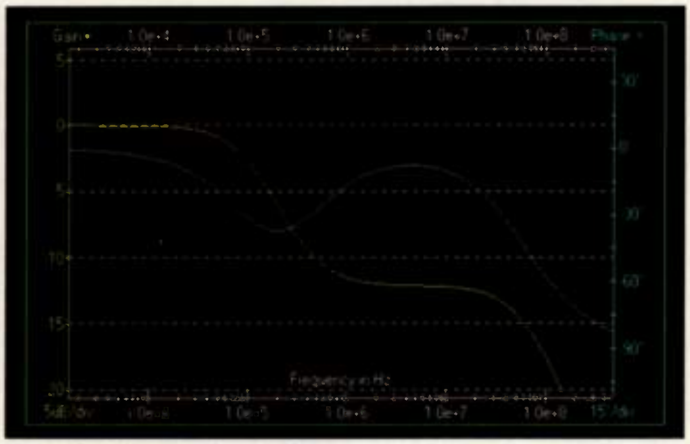

Figure 15. Bode plot of the PLL filter.

Four-phase Costas loop

The four-phase Costas loop operation is similar to a PLL. In Figure 3, the Rx_I and Rx_Q outputs of the quadrature demodulator connect to the four-phase Costas loop phase detector in Figure 14. (Actually, the four-phase Costas loop is the combination of the quadrature demodulator and the processing in Figure 14.) Figure 15 is the Bode plot of the PLL filter after the summing token. The RC parameters are set to produce a low-pass filter with a –3 dB point of 0.1 MHz, and an ultimate loss of –12 dB. The output of the phase detector is an error signal that drives the VCO.

Simulation results

Simulation of the full system takes only 16.3 seconds on an 866 MHz Pentium III computer. The simulation results are shown as three plots in Figure 16. The top and middle plots have the same elapsed time of 10 µsec.

The top plot is an overlay of the rectangular 1.0 Mb/s data_in signal and the smooth, filtered, data_out signal. The middle plot is an overlay of the 11.0 Mb/s Tx_I and Rx_I signals. Close inspection of the middle plot will reveal the 10110111000 pattern of the Barker code.

The bottom plot is the power spectrum of the received signal, Rx_in, with a path loss of 90 dB. The visible part of the transmitted spectrum is 22 MHz wide, while the –30 dB side lobes are below the noise floor. The remaining task in the processing is to make a hard decision on the received data bits and perform a bit-error-rate (BER) analysis. The BER is the standard figure of merit for digital communications systems. The system parameters can be "tweaked" to produce minimum BER (maximum range).

Conclusion

The simulation of the RF portion of an 802.11 WLAN system has been detailed. The parameters were based on existing chip sets and commercially available parts. The simulation engine allows for accurate representation of the system components.

RF

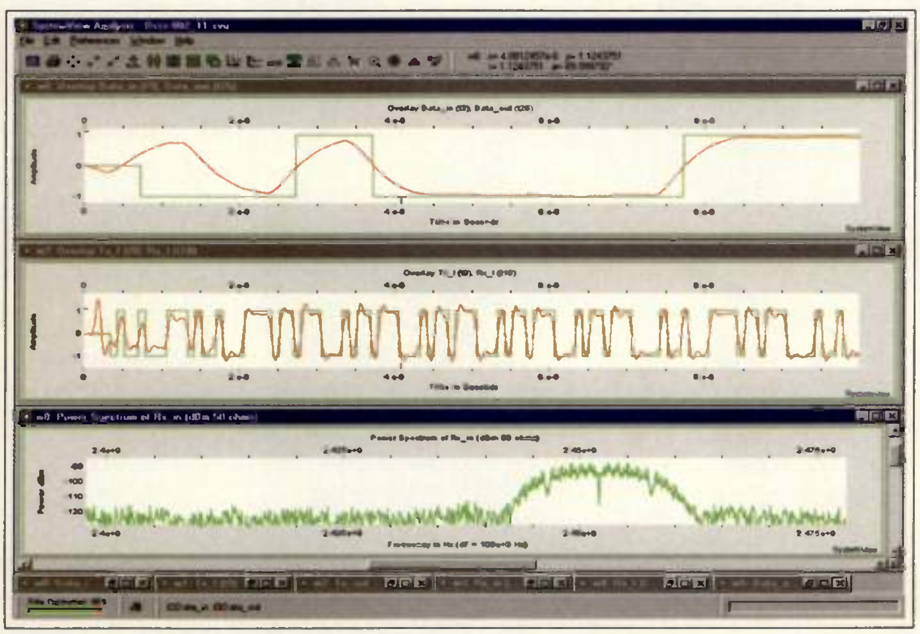

Figure 16. The results of the 802.11 simulation.

About the author

Stephen H. Kratzet is director of electronic design at Elanix. Kratzet joined Elanix in 1992. He is responsible for managing Elanix's RF analog, digital and DSP hardware designs. Prior to his work at Elanix, Kratzet worked for electronics consulting group Mullet Associates for 12 years. Prior to that, he spent 12 years at Solatron, designing automatic assembly and test machines. Kratzet can be reached at Elanix, 5655 Lindero Canyon Rd., Ste. 721, Westlake Village, CA 91362. Tel. 818.597.1414. e-mail: *Stevek@elanix.com*

Designing an RF modular variable-gain amplifier

A flexible modular VGA design for use in modern communications devices.

By Louis Fan Fei and Ming-Ju Ho

The RF variable-gain amplifier (VGA) is a major building block in modern high-frequency communications devices. It is used in the transmitter (Tx) and the receiver (Rx) stages for a number of functions.

Different applications put different requirements on the VGA, and an integrated VGA is often either under-designed or over-designed for a variety of applications. It is difficult to find one VGA that will fit all the applications. This is why modular design is popular. The modular VGA design approach has a trade-off , as shown in the example below.

Design approach and trade-off

In the modular VGA, the amplifier block and gain-control (GC) block are clearly defined. The amplifier block is used only for power amplification, and the GC block is used only for adjusting the power level.

When each block is designed and tested successfully, the building block can be repeated several times to fit various requirements. For example, say each amplifier stage provides 10 dB gain, while each GC stage provides 20 dB control range. If the application requires a 20 dB gain VGA with a 40 dB control range, it is easy to use two amplifier blocks and two GC blocks to meet the requirement.

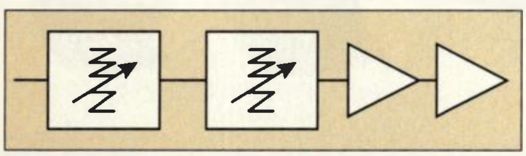

Figure 1. A VGA with amplifier blocks after the gain control blocks (component parameters are listed at the end of this article on page 62).

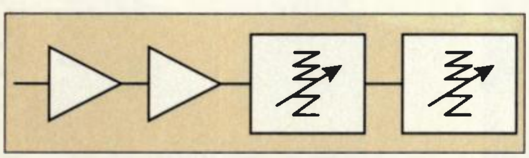

Figure 2. A VGA with amplifier blocks before the gain control blocks (component parameters are listed at the end of this article on page 62).

The main trade-off is the permutation of the amplifier and gain control stages. In the Tx, a VGA is typically used before the PA. The Tx VGA requires a high-output 1 dB compression point and the amplifier stage should be behind the GC stage. Because the GC stage attenuates the input RF signals, it essentially increases the input 1 dB compression point of the amplifier by the attenuation level. On the other hand, the VGA is also used as a low-noise amplifier (LNA) in Rx. The noise factor (NF) of the overall RF system strongly depends on the NF of the LNA. Therefore, the gain stage should be in front of the attenuator stage.

A 20 dB gain VGA with 40 dB control range illustrates the design trade-off. In Figure 1, the two amplifier blocks come after the two GC blocks. In Figure 2, the order is reversed.

The amplifier block and the GC block are the same. The only difference is the arrangement of the blocks. The RF performance, however, is different. The comparison is in Table 1. It should be observed that the configuration in Figure 1 is better suited for the Tx, while the arrangement in Figure 2 is well-suited for the Rx.

Variable-gain amplifier differences on NF and IIP_3 are already obvious. When the gain control kicks in, the differences of NF and IIP_3 between the two configurations are even greater.

One modular VGA design example at 2.45 GHz is presented. The Tx requires a PA driver with maximum gain greater than 15 dB and a dynamic range of 40 dB. The amplifier block and GC block are designed separately before they are cascaded together.

GC block

The GC block or the voltage-controlled amplifier (VCA)[1, 2] can be designed in a number of ways. The three main configurations for a VCA are the constant-impedance approach6, the resistive-line approach[7] and the π-configured attenuator approach[4,5].

The variable resistance approach can be done with either a metal semiconductor field-effect transistor (MESFET) or a positive intrinsic negative (PIN) diode. Each design approach focuses on different design parameters. In this particular design, the resistive line approach using a PIN diode is presented.

The building blocks of the resistive line approach are a quarter-wave transmission line (TL) and a shunt resistor (a PIN diode in this design).

The quarter-wave transformer is a popular way to transform impedance. The design equation is simple:

$$Zout = \frac{Z_0^2}{Z_{in}}$$

The impedance of one end (Z_{in}) of the transformer is inversely proportional to the impedance at the other end (Z_{out}). For example, if $Z_{in} = 1\Omega$ and the TL has a characteristic impedance (Z_O) of 80Ω, Z_{out} will be 6400Ω, which is a high impedance that will reflect most of the incoming RF signal. The typical values of Z_O of the TL range from 50Ω to 90Ω.

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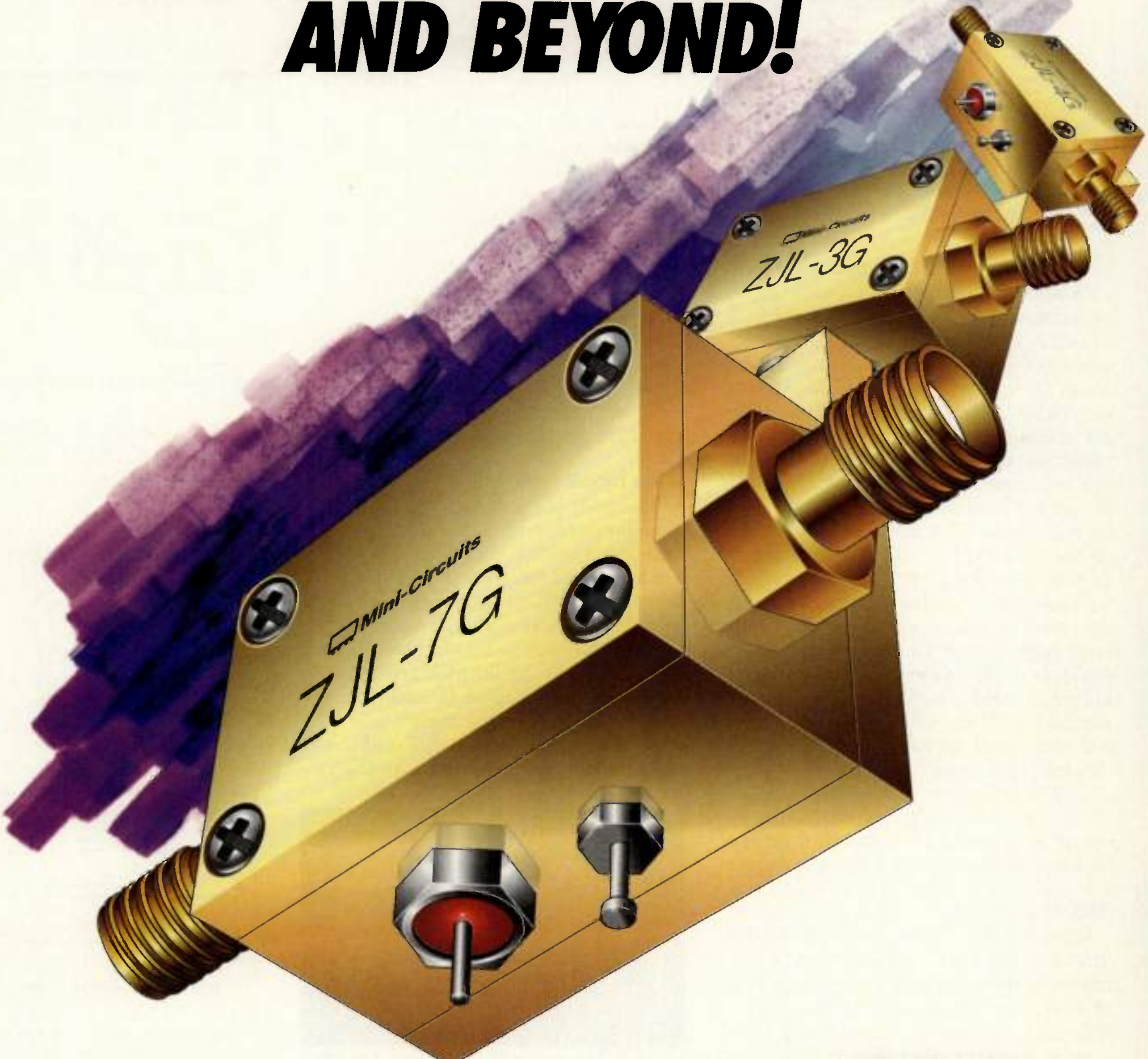

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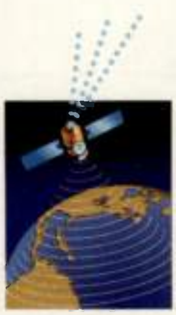

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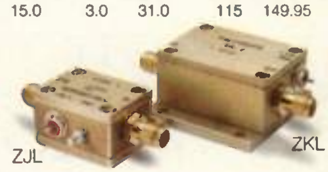
SPECIFICATIONS

Model	Freq (MHz)	Gain (typ) Midband (dB)	Gain (typ) Flat (±dB)	Max. P_{out}[1] (dBm)	Dynamic Range (Typ @2GHz[2]) NF(dB)	Dynamic Range (Typ @2GHz[2]) IP3(dBm)	I(mA)[3]	Price $ea. (1-9)
ZJL-5G	20-5000	9.0	±0.55	15.0	8.5	32.0	80	129.95
ZJL-7G	20-7000	10.0	±1.0	8.0	5.0	24.0	50	99.95
ZJL-4G	20-4000	12.4	±0.25	13.5	5.5	30.5	75	129.95
ZJL-6G	20-6000	13.0	±1.6	9.0	4.5	24.0	50	114.95
ZJL-4HG	20-4000	17.0	±1.5	15.0	4.5	30.5	75	129.95
ZJL-3G	20-3000	19.0	±2.2	8.0	3.8	22.0	45	114.95
ZKL-2R7	10-2700	24.0	±0.7	13.0	5.0	30.0	120	149.95
ZKL-2R5	10-2500	30.0	±1.5	15.0	5.0	31.0	120	149.95
ZKL-2	10-2000	33.5	±1.0	15.0	4.0	31.0	120	149.95
ZKL-1R5	10-1500	40.0	±1.2	15.0	3.0	31.0	115	149.95

NOTES:
1. Typical at 1dB compression.
2. ZKL dynamic range specified at 1GHz.
3. All units at 12V DC.



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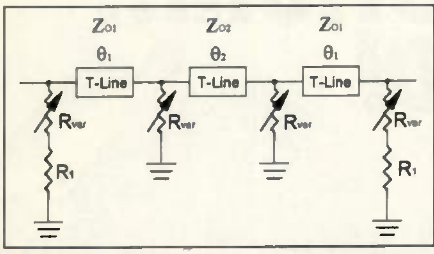

Figure 3. A variable attenuator using four shunt diodes.

To obtain variable attenuation using this approach, the fixed value Z_{in} is replaced with a variable-resistance PIN diode. A typical shunt-configured PIN diode can archive maximum attenuation about 20 to 30 dB at 2.45 GHz. In this particular design, a dynamic range of 50 dB is desired. Any number of variable resistors can be used, depending on the desired range of attenuation. Four shunt diodes are used in this design, as shown in Figure 3. The middle two shunt diodes provide the bulk of the attenuation by reflecting incoming RF signals.

However, a reflective VCA is not desirable in most applications, especially in high-power Tx applications. The reflected RF energy needs to be absorbed inside the VCA to provide low return loss. This will require its internal resistance to be different from its external resistance.

The designer can vary the values of R_1, Z_{O1}, Z_{O2}, θ_1 and θ_2 to trade off size, dynamic range and input/output return loss. In this design, the following values are used: $R_1 = 50\Omega$, $Z_{O1} = 70\Omega$ $Z_{O2} = 95\Omega$, $\theta 1 = \theta 2 = 90°$. Note that the use of a fixed resistor in series with a PIN diode at the input and output of the network results in lowered distortion at maximum attenuation because the incoming RF signal dissipates in a passive device, rather than a diode.

A low-cost, plastic-package PIN diode is used. Parasitic diode elements (package inductance and capacitance, junction capacitance) are significant at 2.45 GHz. The reduction of the effects of package parasitic inductance can turn an ordinary design into a high-performance circuit. The parasitic inductance cancellation scheme does not have to be complicated. The main contributors are package leads, bond wires and via-hole inductance. The inductance can be canceled by simply using a shortened radial microstrip stub (capacitive impedance), in place of the via holes, to resonate out the parasitic inductance. The dimension of the radial stub is determined during simulation. The schematic, layout and test result is shown in Figures 4, 5 and 6, respectively.

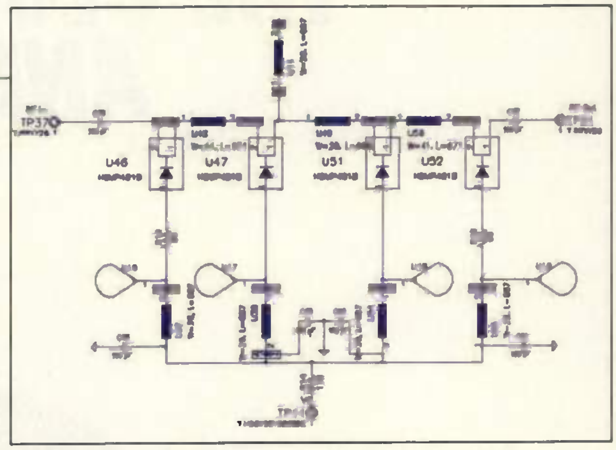

Figure 4. The schematic, layout and test result (1 of 3).

As shown in Figure 6, the attenuation range of the VCA is from −2 dB to −50 dB with good port matching for all the attenuation range.

Gain block design

The gain block is based on Agilent's pseudomorphic high electron mobility transistor (PHEMT). PHEMTs were chosen because they are known for their high OIP_3 and ultra-low NF. The high OIP_3 is desirable in this design.

The transistor is biased with V_{ds}=4 V DC and I_{ds}=60 mA for high OIP_3. Active bias circuitry is used to stabilize the bias point. The actual design is simple with feedback technique[8]. Feedback is added at the source to improve the stability and to reduce the matching complexity. The feedback is performed with two pieces of TLs at the source. Then simple *LC* matching is provided at the input and output to further improve matching performance. The design is shown in Figure 7. The test results are shown in Table 2.

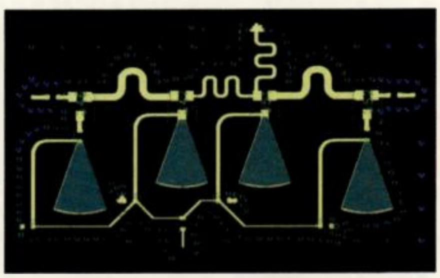

Figure 5. The schematic, layout and test result (2 of 3).

Complete VGA

The PA driver requires maximum gain greater than 15 dB and dynamic range of 40 dB. After comparing the requirement with the test results of each building block, it should be easy to conclude that one GC block and two amplifier blocks are needed for the complete VGA.

	Config. 1	Config. 2
Overall NF	5.63 dB	1.67 dB
Overall OIP	29.27 dBm	19.61 dBm
Overall IIP_3	13.27 dBm	3.61 dBm
Max gain	16.0 dB	16.0 dB

Table 1. Comparison of the values of the two configurations.

The modular VGA approach offers maximum flexibility and optimum performance for different applications.

RF

Figure 1 and 2 component. parameters:
CG block:
Insertion loss = 2 dB
GC = 20 dB
OIP_3 = 25 dBm
Each gain block:
OIP_3 = 30 dBm
Gain = 10 dB
NF = 1.5 dB

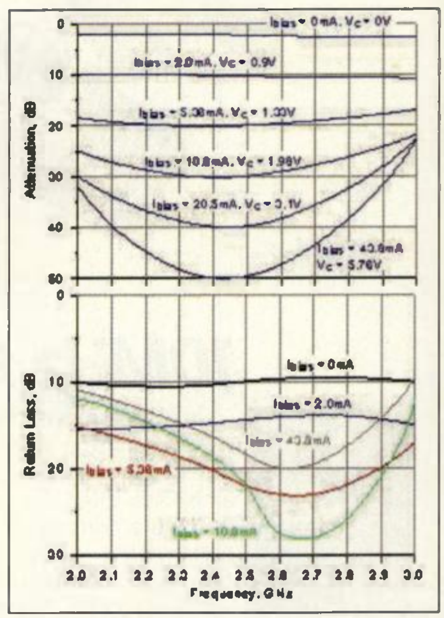

Figure 6. The schematic, layout and test result (3 of 3).

References

[1] "Application of PIN diodes," Agilent Technologies Application Note AN922.

[2] "Design with PIN diodes," Alpha Industries Application Note APN1002.

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Description: RF Switch Connector. One of the most exciting microwave products to come along in years. This low cost test switch has virtually universal RF and microwave design appeal. It solves many design and production test problems at a low cost. Applicable to all RF applications under 3GHz (3000MHz). Test probes: Works with Lab test probe MXGM76RL1000 and mass production test probe MM126030. Reel size/Stock quantity: 1000 pcs. 1 reel. Order PN: MM8430-2600TB1

Murata PN:
LFSN25N19C2450B
New Global PN:
LFB322G45SN1A504
Description: 2450MHz Band Pass Filter, Miniature (3.3 x 2.5mm) ultra low cost Ceramic LC Chip type BPF. This low cost BPF makes an ideal interstage filter. Small enough and low cost enough to be used in several positions on the same board! Reel size/Stock quantity: 2000 pcs. 1 reel. Order PN: LFSN25N19C2450B

Murata PN:
MQE920-2450
Description: 2450MHz miniature (7.8 x 6mm) surface mount VCO. For use in all 2.4GHz Wireless LAN applications. Low cost. Reel size/Stock quantity: 3000 pcs. 1 reel. Order PN: MQE920-2450-T7

Murata PN:
DFC21R57P002HHA
New Global PN:
DFCB21G57LDJAB
Description: 1.57GHz Band Pass Filter (BPF) for GPS applications. Ceramic Monoblock miniature low cost surface mount. Used as the primary RF filter by the USA's leading manufacturers of commercial GPS receivers, this filter has performance and low cost in a standard miniature package. Ceramic BPFs like this form the backbone of Murata's Microwave product line. Since 1950, ceramic electronic components have been Murata's key focus. Reel size/Stock quantity: 2000 pcs. 1 reel. Order PN: DFC21R57P002HHA-TA2120

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Visit our website and register for your FREE MM8430-2600 and LFSN25N19C2450B (New Global PN: LFB322G45SN1A504) samples

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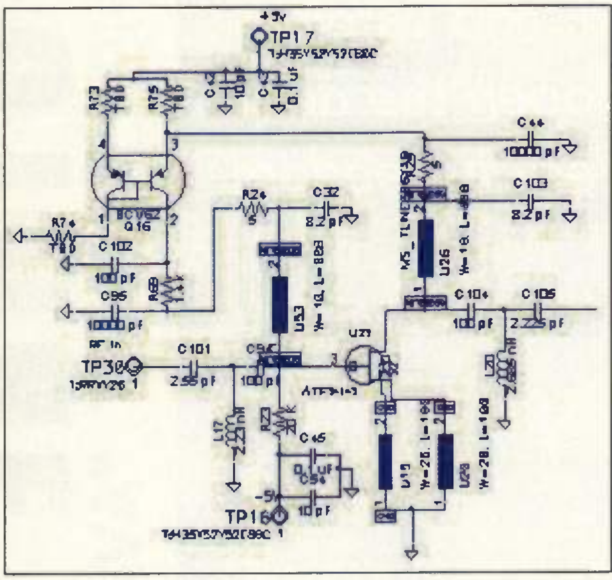


Figure 7. Gain block design.

NF:	1.05 dB
OIP_3:	30 dBm
Gain:	12.5 dB
Input R_L:	–11 dB
Output R_L:	–11 dB
Stability:	Stable at all frequencies

Table 2. Typical test results.

[3] Jack Lepoff and Raymond Waugh, "The PIN Diode - A Tutorial," Proceedings of the RF EXPO WEST, Santa Clara, California, February 1991.

[4] Raymond W. Waugh, "A Low Cost Surface Mount PIN Diode Pi Attenuator," *Microwave Journal*, Vol. 35, No. 5, May 1992.

[5] Louis Fan Fei, "A Low-Cost, Compact, Pi-Configured PIN Diode VCA," *Applied Microwave & Wireless*, November 2000

[6] Louis Fan Fei, Raymond W. Waugh, "A VCA Using the Constant Impedance Approach," *Applied Microwave & Wireless*, January 2001.

[7] Louis Fan Fei, Raymond W. Waugh, "A VCA Using Resistive Line Approach with Parasitic Inductance Cancellation Circuit," *Applied Microwave & Wireless*, January 2001

[8] Guillermo Gonzalez, "Microwave Transistor Amplifiers," John Wiley & Sons, Inc., 1998.

About the author

Louis Fan Fei is a RF design engineer at Agere Systems (formerly Lucent Technologies Microelectronics group) in Atlanta. He has been with Agere since July 1998. He received his B.E.E and M.S.E.E degrees from Georgia Tech in 1996 and1998. He also worked as an intern for Hewlett Packard's Colorado Springs division in the summer of 1997. He can be reached at *ffei@agere.com*.

Ming-Ju Ho received his M.S. and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology in 1991 and 1996. Currently, he is a distinguished member of technical staff at Agere Systems' wireless communications and networking division, Atlanta He can be reached at 404-253-1844, or *hymjho@agere.com*.

Components catalog focuses on OEM, MRO

Jameco Electronics announces a 192-page catalog featuring thousands of ICs and other electronic components, tools, test equipment and computer products suitable for OEM and MRO applications. More than 425 new products have been added, including: ICs, transformers, computer cables, tools, motherboards, switch boxes, connectors, books, converters, power supplies, hubs, fuses, LEDs/ displays, and soldering equipment. Jameco has also expanded its selection of brand-name products, including Fluke test equipment, Gordos I/O module mounting boards, Amphenol adapters and connectors, Entrelec power supplies, terminal blocks, Millennium rechargeable batteries, Tripplite UPS systems, Parallax basic stamp kits, and Omron relays, relay sockets and switches.

Jameco Electronics
INFO/CARD 115

Product guide details inductor specs

Gowanda Electronics introduces a new comprehensive product catalog that addresses technical specifications, design details, custom products and designer kits for the company's four major categories of inductors, including surface-mount RF inductors, surface-mount power inductors, leaded RF inductors and leaded power inductors. Views of application-specific devices and Web site information are also provided. Included in the catalog are more than 14 new products introduced over the last year, including the CC series of surface-mount inductors, the CMF2 surface-mount common mode filter and Power Pod surface-mount inductor. Applications include use in test and measurement equipment, medical and diagnostic equipment, industrial automation and control equipment and instrumentation.

Gowanda Electronics
INFO/CARD 116

Catalog features stocked coaxial cable assemblies

Avnet is stocking more than 150 coaxial cable assemblies for test and measurement and production applications. These cables are suitable for communications infrastructure and test. The new Avnet Semflex stocked cable catalog includes coax cables with single, double and triple shielding. Some cables are also available with stainless steel armor. Frequency response is as high as 50 GHz on the test & measurement cables and 18 GHz on the production cables.

Avnet
INFO/CARD 117

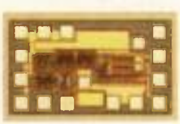
NEW PRESCALERS

With InGaP GaAs HBT Technology!

- DC TO 13 GHz Performance
- Single Positive Supply
- Selectable Output Power Bias Option *For Chips*
- Wide Input Power Window: -15 to +10 dBm
- Ultra Low SSB Phase Noise: -145 to -153 dBc/Hz @ 100 KHz
- For High Volume VSAT, Microwave Radio, and Optical Applications

Description		Frequency Range (GHz)	SSB Phase Noise @ 100 KHz	Part Number
÷2	High Efficiency Med. Output Power	DC - 11.0	-148 dBc/Hz	HMC361
		DC - 10.0	-148 dBc/Hz	HMC361S8G
÷2	High Frequency High Output Power	DC - 13.0	-145 dBc/Hz	HMC364
		DC - 12.5	-145 dBc/Hz	HMC364S8G
÷4	High Efficiency Med. Output Power	DC - 12.0	-149 dBc/Hz	HMC362
		DC - 12.0	-149 dBc/Hz	HMC362S8G
÷4	High Frequency High Output Power	DC - 13.0	-151 dBc/Hz	HMC365
		DC - 12.5	-151 dBc/Hz	HMC365S8G
÷8	High Efficiency Med. Output Power	DC - 12.0	-153 dBc/Hz	HMC363
		DC - 12.0	-153 dBc/Hz	HMC363S8G

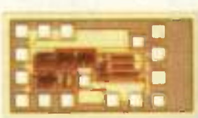
Divide-by-2



HMC361

HMC361S8G

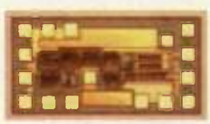
Divide-by-2



HMC364

HMC364S8G

Divide-by-4



HMC362

HMC362S8G

Divide-by-4

HMC365

HMC365S8G

Divide-by-8

HMC363

HMC363S8G

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VISA We Accept

Software optimizes design performance

Cadence Design Systems announces PSpice(R) Advanced Analysis, which enables analog/mixed-signal circuit engineers to use sophisticated design methods on the Windows NT and 2000 platforms. The new product allows users to optimize performance and improve quality of designs before committing them to hardware. The PSpice Advanced Analysis option provides integration with Cadence's Concept(R) HDL and Orcad Capture(R) industry-standard PCB design capture tools. The software is suitable for large-volume consumer products. In analog circuit design, there is a phase when the design topology and the specifications are known, but the final component values have not yet been determined. The PSpice Advanced Analysis solution enables engineers to pick up the design at that point and take it to the next level.

Cadence Design Systems
INFO/CARD 118

Circuit simulator handles flat, hierarchical designs

Celestry Design Technologies' new large-capacity, transistor-level circuit simulator handles flat and hierarchical designs and offers timing, power, noise and reliability analysis. UltraSim is a sign-off simulator that offers simulation of one billion-transistor memory circuits and provides full-chip capacity for memory, logic and mixed-signal designs with built-in reliability simulation. It eliminates the need to use multiple simulators, analysis tools and additional power and reliability tools. UltraSim is a SPICE-precise simulator that handles large flat and hierarchical designs. It offers power and reliability analysis, accurate device models and easy integration into an existing design flow. UltraSim run times match or exceed known alternatives with near SPICE accuracy. UltraSim can be used on all types of designs and styles.

Celestry Design Technologies
INFO/CARD 119

Design kits support Microwave Office

United Monolithic Semiconductors (UMS) announces new design kits supporting the Microwave Office from Applied Wave Research (AWR). The design kits support UMS' processes accessible under its Open Foundry Service mode. Design kits are available for the 0.25μ PHEMT low noise process (PH25) and for the 0.25μ power PHEMT process (PPH25). These technologies are suited for RF to millimeter-wave applications such as broadband wireless access, automotive sensors and ISM wireless. The libraries for Microwave Office include UMS' proprietary, fully scalable models allowing spread analysis and improving production yield optimization. Also included are smart cells that keep the physical layout tied to the actual simulated schematic. Models provide temperature behavior, large and small signal features, high-frequency noise and 1/f noise performance.

United Monolithic Semiconductors
INFO/CARD 120

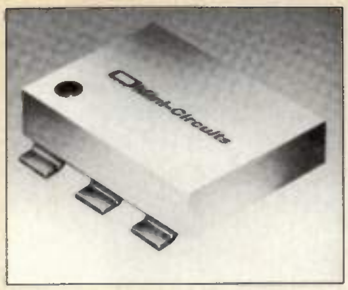
ANRITSU MG3690A

Anritsu introduces the MG3690A synthesizer, offering a single instrument for clean RF and microwave signal generation. The unit features performance-to-price ratio for CW generation and pulse modulation applications as high as 40 GHz. The device is able to combine the bandwidths of separate RF and microwave signal generators with the spectral purity and frequency stability of a phase-locked source. The unit has the ability to achieve crystal-oscillator-like phase noise over the 0.1 Hz to 40 GHz frequency range, making it suitable for a variety of laboratory and production applications previously requiring separate synthesizers. The system achieves frequency resolution of 0.1 Hz over the full frequency range, with leveled output power adjustable in 0.01 dB steps from –120 dBm to +17 dBm. Full-band, low phase noise is achieved by integrating a digital downconverter (DDC) into the system. The DDC generates 10 MHz to 2.2 GHz single sideband phase noise characteristics. The SSB phase noise of the system is –107 dBc/Hz at 1 kHz offset from a 60 Hz carrier. For a 40 GHz carrier at the same offset, the phase noise rises to –92 dBc/Hz. Actual performance is typically 10 dB better than guaranteed specifications. The system has been designed for use as a continuous wave (CW) source of single RF and microwave frequencies or as a digitally swept source, sweeping frequency, power, or both. As a CW source, it features as many as 20 independent markers to set independent CW frequencies. When used as a sweeper, the system allows sweep widths to be set from as narrow as 1 kHz to as wide as 40 GHz. The number of sweep steps can be adjusted from 10 to 10,000, with every frequency step in the range phase locked. A list sweep mode can be controlled via the front panel or by OPIB. In this mode, as many as four data tables with 2,000 nonsequential frequency/power sets can be stored in memory and then addressed as a phase-locked step sweep. In addition, it can perform a basic frequency-hopped or frequency-agile function controlled via OPIB. As many as 3,202 data points of power or frequency can be stored and recalled from non-volatile memory. For rack mount applications, it offers a compact 13.3 cm package and a high-output power that assures adequate signal strength to the device under test (DUT), even after ATE switching and cabling losses.

Zero to 40 GHz single-instrument signal synthesizer

Anritsu
INFO/CARD 121

Wide-band SMT matching pad mixer.

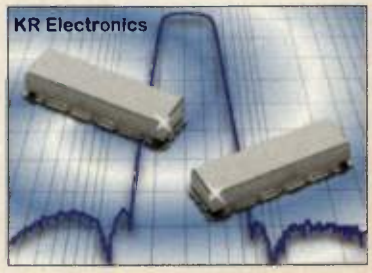


Mini-Circuits introduces a wide-band, surface-mount matching pad engineered for the DC to 3.0 GHz frequency band. Optimized to meet the stringent performance requirements of 50Ω to 75Ω wide-band matching, the ALMP-5075 provides 5.7 dB +0.2 dB nominal attenuation with + 0.1 dB typical flatness and a tight 1.2:1 return loss (typ.). The low-profile height is 0.080". An evaluation board P/N: TB-25 is available.

Mini-Circuits
INFO/CARD 122

Specifications at a glance:
- DC to 3 GHz
- 5.7 dB nominal attenuation
- 1.2:1 return loss
- +0.1 dB typical flatness

Surface-mount bandpass filter



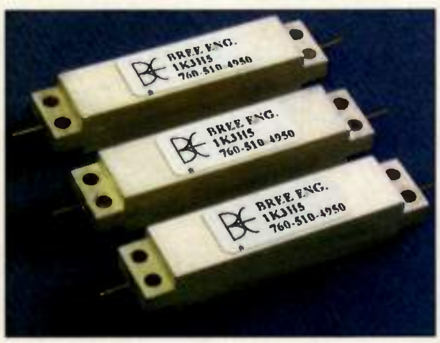
KR Electronics introduces a small, high-performance, surface-mount, elliptic bandpass filter. The filter is supplied in a surface-mount package measuring 0.5 x 1.5 x 0.3 inches. The KR 2395 has a 70 MHz center frequency with a 1 dB bandwidth of 12 MHz. The filter has excellent symmetry, quick transition to the stopband, and high stopband attenuation of typically more than 60 dB. The filter can be customized for other center frequencies and bandwidths.

KR Electronics
INFO/CARD 123

Specifications at a glance:
- 70 MHz center frequency
- 1 dB bandwidth of 12 MHz
- Stop-band attenuation of >60 dB, typical

Asymmetrical filter bank

Bree Engineering introduces a bank of three filters that uses a non-symmetrical skirt selectivity response to minimize size and costs while maximizing specialized custom requirements. The filter bank covers the 950 to 3150 MHz range in three bands, each just under one octave. Passband flatness is less than 1 dBc, insertion loss at band edge ranges from less than 1.5 dBa in the lower bands and 2.5 dBa at the higher bands. Upper skirt selectivities are optimized for 50 dBc minimum at 1.08 times the upper passband.



Bree Engineering
INFO/CARD 124

High-power T-switch for space applications

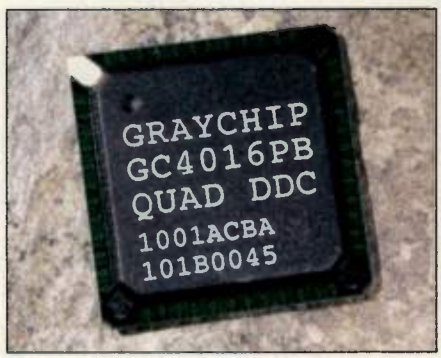
Dow-Key Microwave debuts its 5111HAJ-730322-3, high-power, low-distortion T-switch for space-based applications from 2.5 to 4.8 GHz. It moves high-power signals from one port to another and is rated for peak RF power levels as high as 560 W, with an average power level of 140 W. Using "break-before-make" switch contacts, the switch is used for cold-switching operations. It requires 25 µs or less to switch internal signal paths.

Specifications at a glance:
- 2.4 to 8 GHz
- 1.25:1 max insertion loss
- 60 dB min isolation:
- 140 W RF power handling (max)
- < 25 ms switching time

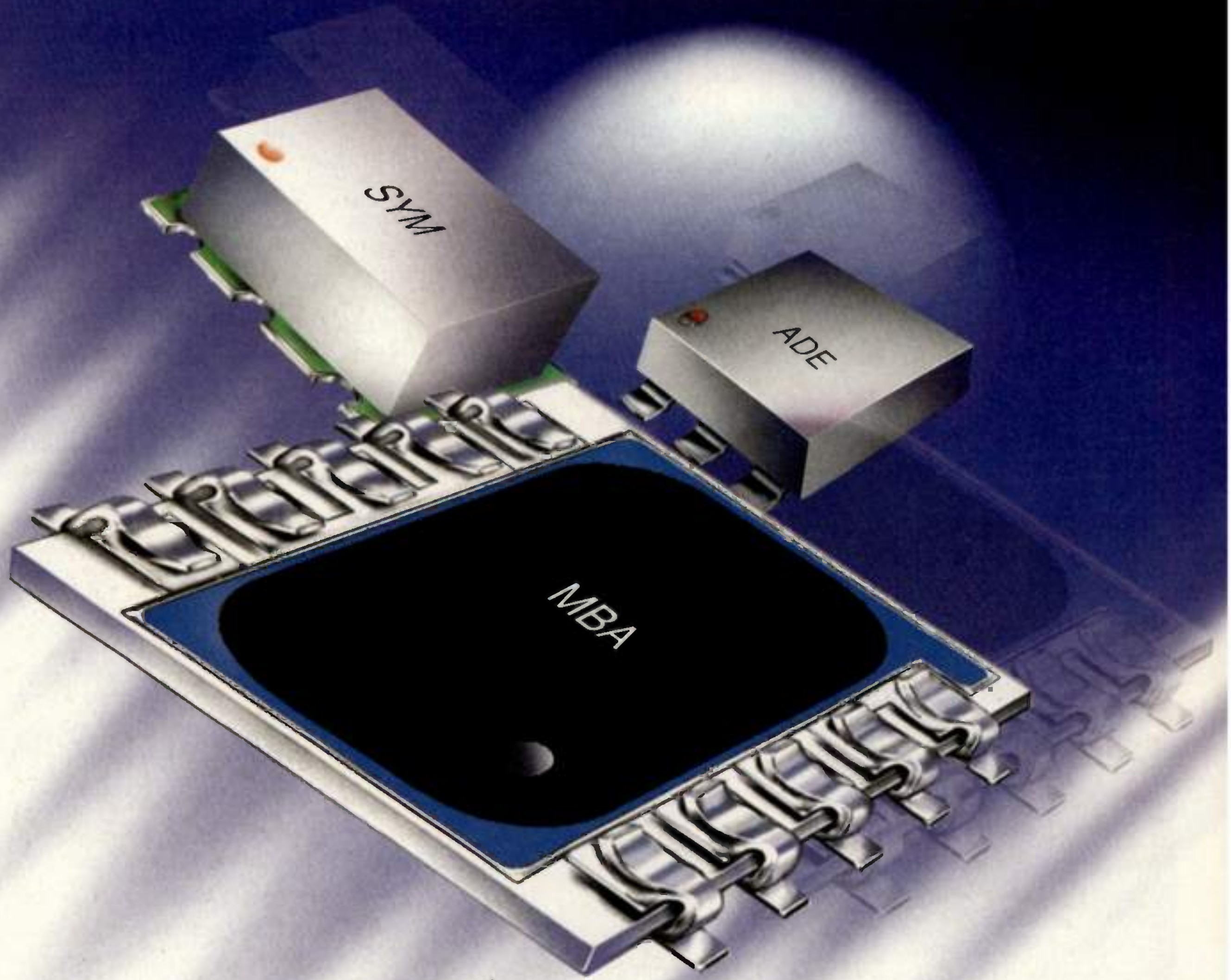
DowKey
INFO/CARD 125

Quad multistandard digital downconverter

Graychip announces the GC4016, an enhanced-performance, four-channel digital downconverter chip. The device is a suitable building block for implementing multistandard, software-defined radios for cellular base station systems. Standards supported include GSM, IS-95, IS-136 and EDGE, as well as third-generation UMTS/CDMA2000. The device provides four digital receiver channels, each capable of digitally downconverting and filtering signals of interest from wideband sources at sample rates to 100 MHz. The channel outputs are centered at baseband, and typically drive a general-purpose DSP chip for subsequent demodulation and processing. A 16-channel base station receiver system can be implemented with four GC4016 chips and a single A/D converter. The device offers 115 dB of spurious free dynamic



WIDEBAND
HIGH IP3 MIXERS



+4 to +17dBm LO from $6.95 (ea. Qty. 10)

Now you can obtain *spectacular wideband IP3 performance* at a value price with Mini-Circuits team of MBA, ADE, and SYM mixers. Optimized to deliver the highest IP3 for a given LO drive, these affordable surface mount mixers range from 32dBm IP3 for +17dBm LO power...to 15dBm IP3 for LO down to +4dBm. In terms of E Factor (IP3 Figure Of Merit), these mixers go as high as 1.5 providing superior intermodulation suppression from 5 to 5900MHz while at the same time achieving low conversion loss and high isolation. You'll also be pleased to know the Blue Cell™ MBA model covers your higher frequency designs with superb temperature stability, high repeatability, and ultra-thin 0.070" profile. Now, high IP3, higher performance, and value pricing have merged. The result is Mini-Circuits wideband high IP3 mixers...the *clear* choice!

Mini-Circuits...we're redefining what VALUE is all about!

Typical Specifications:

Model	Freq. (MHz)	LO Level (dBm)	IP3 Midband (dBm)	E Factor*	Conv. Loss Midband (dB)	Price $ea. Qty. 10
ADE-10MH	800-1000	+13	26	1.3	7.0	6.95
ADE-12H	500-1200	+17	28	1.1	6.7	8.95
• MBA-591L	4950-5900	+4	15	1.1	7.0	6.95
SYM-25DLHW	40-2500	+10	22	1.2	6.3	7.95
SYM-25DMHW	40-2500	+13	26	1.3	6.6	8.95
SYM-24DH	1400-2400	+17	29	1.2	7.0	9.95
SYM-25DHW	80-2500	+17	30	1.3	6.4	9.95
SYM-22H	1500-2200	+17	30	1.3	5.6	9.95
SYM-20DH	1700-2000	+17	32	1.5	6.7	9.95
SYM-18H	5-1800	+17	30	1.3	5.75	9.95
SYM-14H	100-1370	+17	30	1.3	6.5	9.95
SYM-10DH	800-1000	+17	31	1.4	7.6	9.95

*E Factor = [IP3 (dBm) – LO Power (dBm)] ÷ 10. See web site for E Factor application note
ADE models protected by U.S. patent 6,133,525
• MBA Blue Cell™ model protected by U.S. patents 5,534,830 5,640,132 5,640,699.

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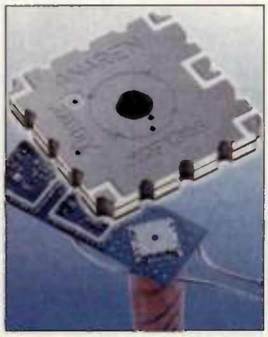
range and supports nibble-wide SHARC link port interfaces and a 24-bit parallel data output option.
Grayhip
INFO/CARD 126

Quadrifilar helix feed network

Anaren announces its surface-mount, quadrifilar helix feed network ("quad-feed") component for satellite radio receivers. The miniature 2.320 to 2.345 GHz quadfeed – part number XQF1306 – combines four signals from a quadrifilar helix antenna into one coherent output signal for amplification to the radio receiver. The device is designed to be compatible with both the XM and the Sirius satellite radio networks.



Anaren
INFO/CARD 127

PCS high-power drop-in circulator

NARDA's new drop-in circulator provides high isolation with higher power handling and operates over the 1.93 to 1.99 GHz frequency range. Designed for a maximum insertion loss of 0.35 dB, this circulator offers a minimum isolation of 25 dB and a maximum VSWR of 1.12:1. Power handling for this drop-in circulator is 120/100 W peak/average. The operating temperature range for model NAR-2799 is 0° C to +85° C.

NARDA
INFO/CARD 128

Want to know the secret of success in the land of Linux and Nokia? It's APLAC. An industrial-strength simulation technology that combines the functionality of Spice with the utility of an advanced RF simulator. APLAC, and only APLAC, provides the accurate IC- and board-level models and precise methods to analyze non-linear circuit behavior demanded by top RF and analog designers. The only approach up to the complex design challenges ahead: 3G, Bluetooth, and beyond.

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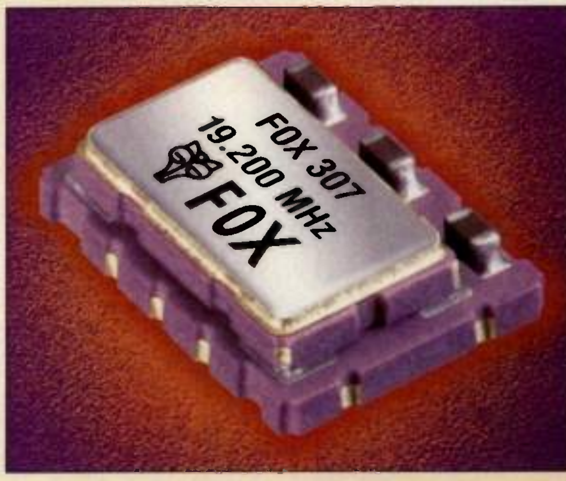
The Freedom To Do Things Right. INFO/CARD 12

Compact TCXO for portable and wireless applications



Fox Electronics introduces a new series of temperature-controlled crystal oscillators (TCXO) designed for the smaller sized, industry-standard footprint of portable and wireless equipment. The Fox 307 series of TCXOs measures 7 x 5 mm x 1.9 mm high, making them suitable for SMD applications with tight space constraints. The devices use the industry's standard pinout configuration and require a 3.0 VDC power supply. The new TCXOs have a current drain of less than 2 mA and feature a low phase noise of less than −140dBc/Hz at 100 kHz. The devices have a voltage control function with a frequency deviation of ±5ppm, ±15 ppm over a voltage control range of 1.5 VDC ± 1VDC. Stock is standard in the following frequencies: 12.8, 13.0, 14.4, 16.8, 19.2, and 19.8 MHz.

Specifications at a glance:

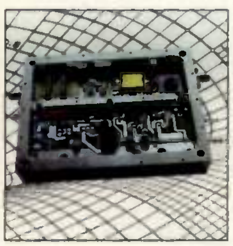
- 12.8 to 20 MHz frequency range
- ±2.5 ppm frequency stability
- −30 to +85° C temperature range
- −140 dBc/Hz phase noise @100 kHz
- ± 5 ppm frequency deviation

Fox Electronics
INFO/CARD 129

AMPLIFIERS

6.3 W microwave amplifier

Microwave Solutions introduces the model MSH-4716803-TC amplifier. The device can deliver 38 dBm (6.3 W) of power, has an IP3 of 49 dBm & 2nd harmonics below −40dBc typ. These amplifiers are well-suited for point and point-to-multipoint systems at 3.4 to 3.6 GHz. They include a temperature compensation circuit that has a ±1.5 gain window. Typical gain is 49.0 dB, with a flatness of °±1.0 dB. The I/O VSWR is 1.5:1 and the maximum current is 3.8A at +12.0 VDC. The amplifier has been designed to meet high thermal stress conditions, and all units include an internal voltage regulator and reverse-polarity protection.



Microwave Solutions
INFO/CARD 130

Small-footprint Bluetooth amplifiers

SiGe Semiconductor's expanded family of Bluetooth Class 1 power amplifiers includes the PA2423G miniature amp and PA2423L miniature fully encapsulated package amp. The devices reduce form factor, while providing efficient power output to enhance performance of Class 1 Bluetooth applications such as cellular handsets, wireless headsets, laptops, and peripheral devices. The devices achieve +22.5 dBm output power with 45% PAE when operated in class AB mode. This enhances operation of Class 1 Bluetooth applications because the devices can overcome insertion losses as high as 2.5 dB between the amplifier output and antenna input.

SiGe Semiconductor
INFO/CARD 131

Low-noise, high-gain SiGe HBT amplifier

Stanford Microdevices announces the SGA-8343, a versatile silicon germanium (SiGe) low-noise amplifier with high gain and high linearity across the entire DC to 6 GHz band. The SGA-8343 provides low-noise performance (0.9 dB @ 0.9 GHz and 1.1 dB @ 1.9 GHz) with high gain (24 dB @ 0.9 GHz and 19 dB @ 1.9 GHz). The unit is easily matched and features a third-order output intercept point of +28.5 dBm.

Stanford Microdevices
INFO/CARD 132

InGaP HBT power amplifiers support 2.5G CDMA

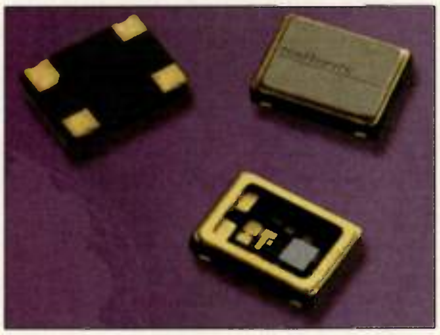
Anadigics introduces two InGaP HBT (indium gallium phosphide heterojunction bipolar transistor) power amplifiers (PAs) for use in multimode, multiband CDMA handsets that support 2.5G CDMA applications. The AWT6105 and AWT6106 provide high linearity and high efficiency in a small module package. The AWT6105 is designed for cellular CDMA, CDMA-1X and AMPS applications in the 824 to 849 MHz range; and the AWT6106 is targeted for PCS CDMA and CDMA-1X

applications operating at 1.85 to 1.91 GHz. Both devices combine all of the necessary passive components for full compensation and 50Ω input/output matching. They are +3.5 VDC devices with a 6 mm x 6 mm footprint, 1.6 mm profile, and low leakage. The AWT6105 demonstrates 37% power added efficiency, while the AWT6106 provides 35% power added efficiency.
Anadigics
INFO/CARD 133

SIGNAL SOURCES

Low-jitter family of programmable oscillators

SaRonix announces its new line of surface-mount programmable oscillators, the PrO S8002C ceramic series. These low-jitter oscillators can be programmed by local distributors to meet the immediate needs of design engineers in a matter of 24 to 48 hours. Operating at 3.0 and 3.3 VDC, the devices keep period jitter (RMS) to a noise-free level of 50 ps max 33+ to 90 MHz, 100 ps max 5+ to 33 MHz, and 167 ps max 1 to 5 MHz. Operating at 5 V, the PrO S8002 holds jitter to 17 ps typ. 42 ps max 33+ to 125 MHz and 33 ps typ. 100 ps max 1 to 33 MHz. The programmable S8002C offers precise rise and fall times, tight symmetry, and frequency stability (±25, ±50 or ±100 ppm over all conditions) approaching that of conventional oscillators. They are available on 16 mm tape in 500 piece reels in a 5 x 7 x 1.8 mm ceramic, surface-mount package.



Saronix
INFO/CARD 134

Low-profile clock oscillators for Intersil Prism chipsets

The SWO11 series clock oscillators measure 5 x 7 mm with 1.0 mm overall height and are specifically designed for the Intersil Prism chipsets. Frequencies are 44.0 MHz and 48.0 MHz with frequency stability of ±25 ppm over 0° C to +70° C for the Prism 2.0, 2.5 and 3.0 Prism chipsets, and 80.0 MHz with ±20 ppm over 0° C to +70° C frequency stability for Prism 5 chipsets.
Mercury Crystals
INFO/CARD 135

Alternative to YIG-based Modules

APA Wireless Technologies announces the next-generation YRO (RF) module, which is a mass-pro-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ducible alternative to YIG-based technology. The YIG Replacement Oscillator (YRO) technology improves the reliability, speed and economy of broadband fixed wireless communications. It enables telecommunications providers to pack greater amounts of data into existing frequencies at lower cost than current RF technologies. Silicon-based, YROs are capable of rapid frequency changes, from sub-millisecond to 100 µsec switching speed, depending on configuration.

The devices have a broad range of applications, including frequency synthesizers, up- and down-converters, phase-locked oscillators, microwave, test equipment, radar and LMDS/MMDS.
APA Wireless
INFO/CARD 136

Low-jitter port card clock IC

Silicon Labs announces the Si5364 SONET/SDH precision clock integrated circuit (IC) for port cards. The device is a complete, high-performance clock generation device capable of producing the ultra-low jitter reference clocks required by today's 2.5 Gbps, 10 Gbps and 40 Gbps optical port cards. This single IC provides Stratum 2/3/3E-compliant protection switching and produces four output reference clocks with less than 0.25 ps (Typ RMS) jitter in OC-192 applications. The Si5364 requires 10 times less board space than existing products. The Si5364 single IC can deliver the ultra-low jitter clock generation once only achievable using discrete analog phase-locked loop (PLL) implementations using crystal- or surface acoustic wave (SAW)-based voltage-controlled oscillators. The Si5364 operates from a single 3.3 or 2.5 VDC supply over the full industrial temperature range.
Silicon Laboratories
INFO/CARD 137

TCXO uses DSP techniques

The Max1 series Maxo brand digitally assisted TCXO uses digital signal processing techniques to achieve the stability of an oven-controlled crystal oscillator, with the lower

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- 50 ppb stability
- 0° to 50° C temperature range
- <15 mA current drain at 5VDC

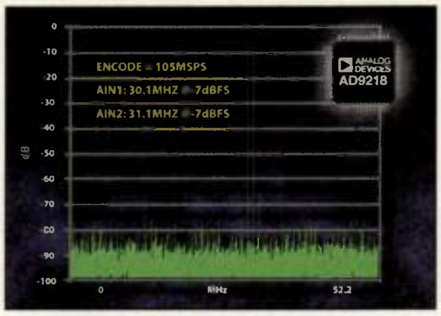
power consumption and smaller size of a TCXO. A stability of 50 ppb is achieved over an operating temperature of 0° to 50°C, with a current consumption of less than 15mA at 5 V. The device achieves Stratum III specification for aging and stability over temperature.

M-tron Industries
INFO CARD 138

DIGITAL HARDWARE

Fast 3 VDC 10-bit A/D converter

Analog Devices announces the AD9218 dual 10-bit monolithic sampling A/D converter optimized for low power, small package size, and ease of use. The device samples at conversion rates of as much as 105 Ms/s and the



dual ADC channels can be operated independently of one another for maximum application flexibility. It requires only a single 3.3 VDC (3.0 to 3.6 VDC) power supply and an encode clock for full performance operation. The digital outputs are TTL/CMOS-compatible and a separate output power supply pin supports interfacing to 3.3 or 2.5 VDC logic. User selectable options are provided to offer a combination of independent channel power-down modes, digital data formats and digital timing schemes.

Analog Devices
INFO/CARD 139

8-bit, 200 Ms/s A/D converter

SPT announces the SPT7720, an 8-bit 200 MSPS analog-to-digital converter. The device offers low power dissipation (430 mW) and high bandwidth (500 MHz). It is designed to operate in environments that need to digitize complex signals, yet are constrained by power and price issues such as digital instrumentation, communications and video displays. It features a high sample rate (200 MSPS) and superior linearity (ILE/DLE at ±0.5 LSB typ.) to accurately represent complex analog signals.

Signal Processing Technology
INFO/CARD 140

SEMICONDUCTORS AND ICs

New architecture improves chip speed, power, and yield

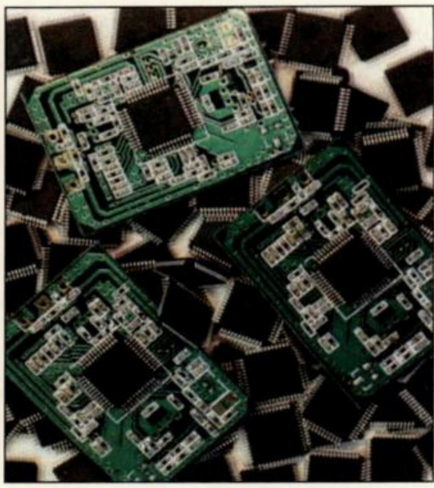
Simplex and Toshiba announce a new semiconductor architecture with the potential to deliver simultaneous improvements of 10+% greater chip performance, 20+% less power consumption, and 30+% more chips per wafer. Dubbed the X Architecture, this approach to chip design can make use of diagonal interconnects, or wiring, for advanced integrated circuits (ICs) possible. The two companies have completed the design of a RISC processor core as the first X Architecture design. Liquid routing technology, based on gridless, octilinear routing, makes X Architecture chips practical and achievable. This approach to routing — with the interconnect unconstrained by a grid and able to move in any of eight directions — enables more direct connection between any two transistors on a chip, close or far, resulting in an average 20% reduction in wire length over the chip.

Simplex Solutions
INFO/CARD 141

SUBSYSTEMS

Addition to LC series RF module line

NUMA Technologies has added the NT2904 full-duplex "Chip-Ceiver" in TQFP-48 case to its line of modules.



The device operates from 130 to 1000 MHz in FM/FSK/ASK (carrier detect), audio or 120 kb/s data mode. Applications include high-end consumer audio, wireless headsets and WLAN.
NUMA Technologies
INFO/CARD 142

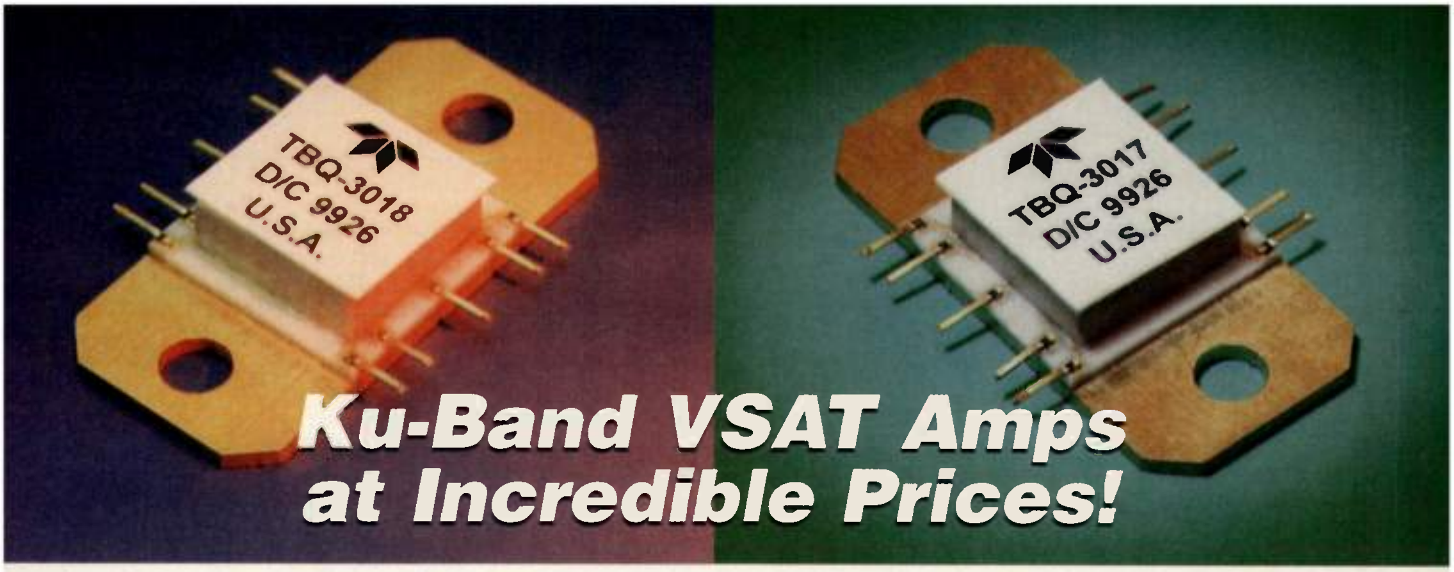
Totally integrated GaAs pHEMTS

Mimix announces a totally integrated gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) receiver on a single chip. This device is a three-stage, low-noise amplifier (LNA) followed by an image reject fundamental mixer using Lange couplers to improve bandwidth. Using 0.15 micron gate length GaAs pseudomorphic high electron mobility transistor (pHEMT) device model technology, the receiver covers the 17 to 27 GHz frequency band. It has a typical small signal conversion gain of 10 dB, with a typical noise figure of 3.5 dB and 15 dB typical image rejection across the band. The XR1000 is well-suited for wireless communications applications such as millimeter-wave point-to-point radio, local multipoint distribution services (LMDS), SATCOM and VSAT applications.
Mimix Broadband
INFO/CARD 143

Specifications at a glance:
- 17 to 27 GHz frequency range
- 10 db small signal conversion gain
- 15 dB image rejection

Integrated dual-band, tri-mode CDMA module

RFMD announces the RF3404, a fully integrated dual band tri-mode receive module incorporating low-noise amplifiers (LNAs), SAW filters and mixers for code-division, multiple-access (CDMA) handset and personal digital assistant (PDA) applications. Using a high level of chip integration, two miniature RF SAW filters and integrated passive components, this module can decrease the required bill of materials (BOM) for the receiver section of a dual-band handset from a typical 25 external components down to three. This allows manufacturers to reduce product size, simplify the supply chain, decrease assembly costs, shorten engineering and product cycle times, and improve factory yield. The device contains the receive chains for both the cellular



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and PCS bands. Each chain contains an LNA, RF image SAW filter, mixer preamplifier, mixer, LO input amplifiers and an LO transmit VCO buffer amplifier. The module is designed with an optional LO frequency divider, which provides the flexibility to use either single or dual VCO architectures. It is offered in a land grid array laminate module package.

RF Micro Devices
INFO/CARD 144

TEST AND MEASUREMENT

Microwave signal generator for broadband design

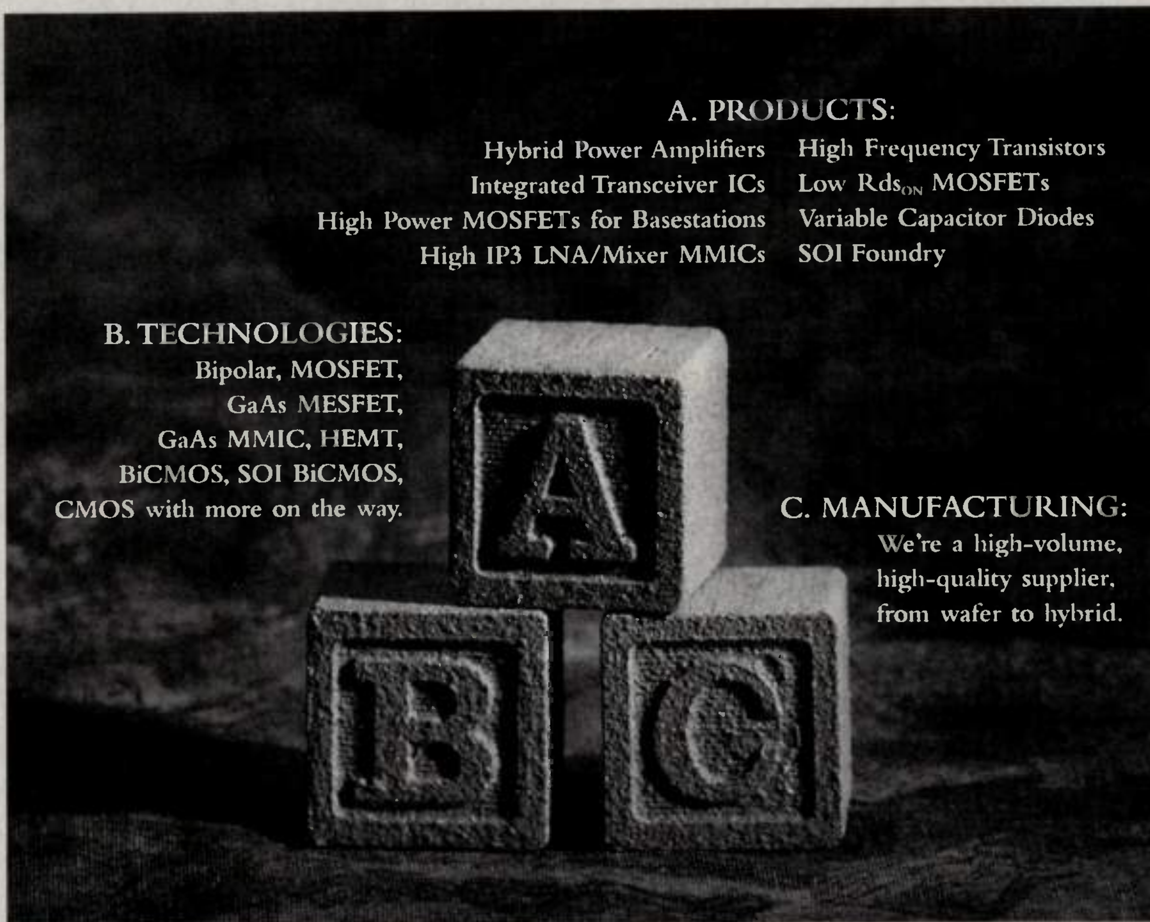
Agilent Technologies introduces the two-series Performance Signal Generator (PSG) system. The PSG-L series is optimized for local oscillators (LOs). The PSG-A Series is optimized for analog modulation. Both series are available in 20 GHz and 40 GHz models. The PSG series provides 20 dBm at 20 GHz and 14 dBm at 40 GHz, eliminating the need for external amplifiers and reducing overall equipment and test costs. The accuracy level of the PSG series (±0.7 dB) reduces test uncertainties and improves production throughput. Standard products have phase-noise performance of –90 dBc/Hz at 1 kHz offset and –112 dBc/Hz at 10 kHz offset and a 10 GHz carrier. The PSG provides improved performance, with option UNJ, of –110 dBc/Hz at 1 kHz offset and –112 dBc/Hz at 10 kHz offset and a 10 GHz carrier.

Agilent Technologies
INFO/CARD145

Protocol test system emulates CDMA Network

Spirent Communications debuts the AirAccess C2K Protocol Test System, a performance analysis system that aids cdma2000 mobile-device manufacturers and service provides in the development and deployment of products and services. It combines Windows-based application software with test instruments to provide complete emulation of a multi-cell cdma2000 network. Dynamic state machine emulation and an intuitive GUI allow for interactive testing without requiring the generation of complex programs or scripts. A real-time protocol processive engine meets the most complicated testing requirements, including multi-frequency handoff scenarios and high-speed packet data applications. A flexible architecture allows customers to interface with their unit under test at baseband and RF. The baseband interface provided by the system allows manufacturers to begin testing at the earliest stages of development,t before an RF front-end is integrated into the product.

Spirent Communications
INFO/CARD 146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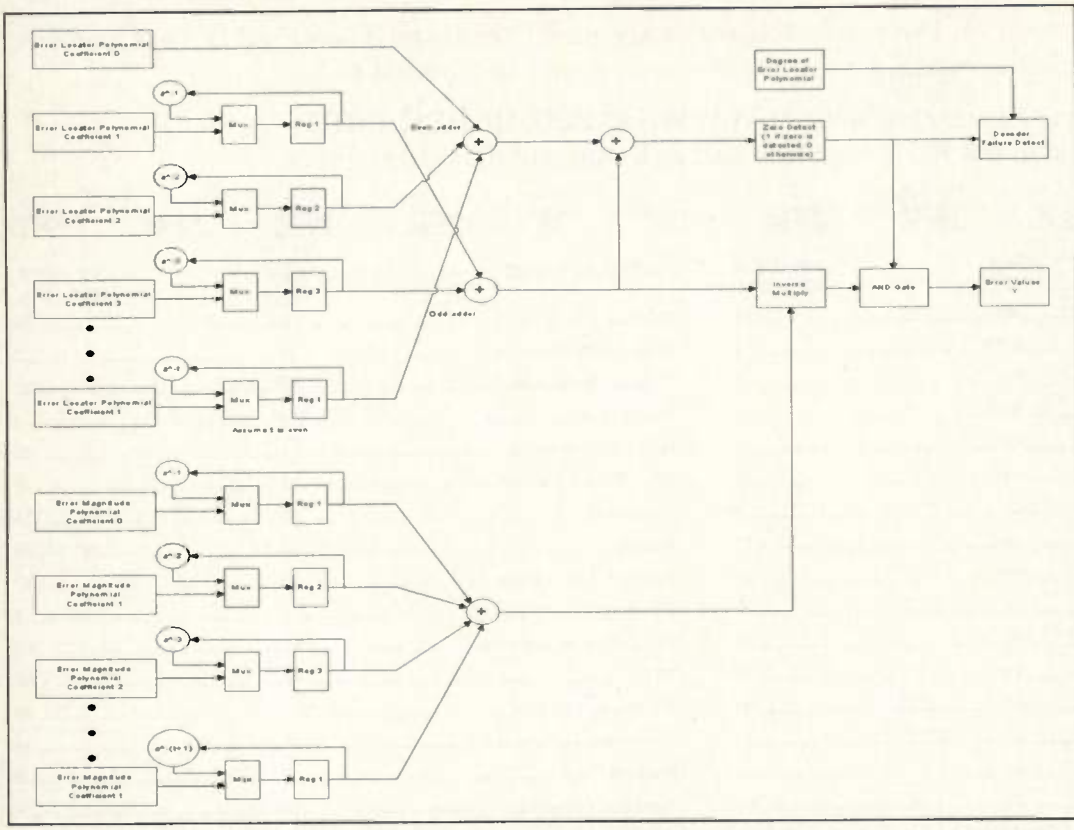

Figure 7. Combination of the Chien Search and the Forney algorithm. Outputs are the error value vector Y and the decoder failure flag is asserted if the degree of the error locator polynomial $\Lambda(x)$ does not equal the number of errors found by the Chien Search.

Since the same type of hardware is needed for both the Chien Search and the Forney algorithm, the two functions can be combined in the same block. The Chien Search is shown in the top of Figure 7. The output of the adder for the odd stages is also used in the Forney algorithm, shown in the lower part of the Figure 7. The sum of the odd stages represents the denominator of the Forney equation. This value is inversed in the Inverse Multiply block and then multiplied by the numerator value that is formed from evaluating the error magnitude polynomial. The output is ANDed with the zero detect output since the error values are only valid for the actual error locations (and they should be set to zero otherwise).

A decoder failure is detected by comparing the degree of the error locator polynomial Λ(x) to the number of errors found by the Chien Search module. If the two values are not equal, then a decoder failure has occurred, the decoder failure flag is asserted and the codeword estimate is the received codeword. The degree of Λ(x) is the power of the highest non-zero coefficient of the polynomial. Note that the decoder failure detection is not guaranteed to work if there are more than t errors. Most of the time, it will detect when more than t errors have occurred, but there will still be some cases that are not detected.

Error correction

The output of the Chien/Forney block is the error vector. This vector is the same size as the codeword. The vector contains non-zero values in locations that correspond to errors. All other locations contain zeros. The errors in the received codeword are corrected by adding the received codeword to the error vector using a Galois Field adder. Because the error vector is generated in the reverse order of the received codeword, a LIFO must be applied to either the received codeword or the error vector to match the order of the bytes in both vectors. The output of the adder is the decoder's estimate of the original codeword.

Conclusions

This article discussed the algorithms and architectures needed to implement a Reed-Solomon encoder and decoder in hardware. The theory of Galois Fields and Reed-Solomon codes is a vast area, and the literature listed in the References section provides a good starting point.

RF

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About the author

Louis Litwin is a m ember of the technical staff with Thomson Multimedia Corporate Research where he is working on 3G CDMA technology for mobile applications. Litwin received his M.S. degree in Electrical Engineering from Purdue University in 1999, and his B.S. degree in Electrical Engineering (summa cum laude) from Drexel University in 1997. He has published over 20 papers on the topics of digital communications and digital signal processing, and he has several patents pending that are related to digital communications. His professional interests include wireless digital communications with a particular focus on adaptive equalization, error control coding and synchronization.

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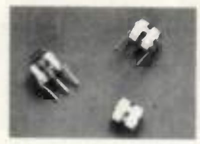

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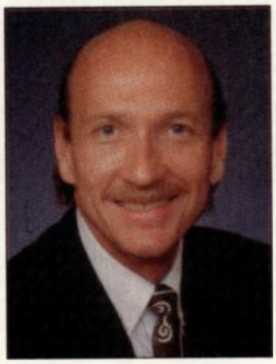

by Ernest Worthman
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As most of you who read my column know, I am pretty much a skeptic — not only with technology, but with the implementation of technology as well. This skepticism comes mostly from my parallel years of working in the computer industry, especially with the wireless industry and Microsoft's innumerable Windows versions.

Early on, that is, before consumer wireless became so popular, wireless was confined to those that understood how it worked and what its shortcomings were. Ditto for the computer industry. That made both technologies work well under its constraints.

Well, along came Bill Gates, who did a number on the computer industry by taking it to the masses. And along came the Motorola, Nokia, et al, who took wireless communications to the masses.

Needless to say, the computer is about as flaky as it gets, and the same goes for consumer wireless. I've discussed that in many a past column.

I recently came across a story about wireless in a magazine called *The Industry Standard*. The article was pretty bold about the current problems with the industry, pointing to five hurdles that it faces.

Hurdle #1 — *3G technology will sell itself.* OK, yeah, it would if it worked. One, among a number of issues, is power. Current battery technology cannot support 2 Mb/s connection speeds. It would deplete the present battery footprint in a matter of minutes, and they would get a tad warm in the process.

Also, in a recent offering by NTT DoComo, trial 3G handsets were operating at speeds of less than 200 kb/s. Shortly thereafter, NTT DoComo did a recall of 1600 handsets for various problems, one of which was heat generation.

Hurdle #2 — *i-mode is the solution.* Well, the i-mode guys did manage to figure out how to be compatible with hyper-text markup language (HTML). They also figured out how to generate revenue for content. But...the consumer is cheap. He isn't willing to pay a whole lot for content. So, unless you have a large customer base, a couple of bucks a month for content isn't going to cover the costs.

Also, the I-mode model depends on all of the revenue going back to content providers. However, mobile operators want a piece of the pie as well. We'll see how this shakes out.

Hurdle #3 — *Bluetooth will create a whole new level of devices that will stimulate even further demand for wireless connectivity.* Hmmm...where have we heard that before? Bluetooth has been analyzed to death, and anyone in the industry knows about issues such as interference, the lack of infrastructure, compatibility issues with 802.11x and integration costs. Moreover, any high school freshman with a scanner and some basic software knowledge can crack a Bluetooth network.

Hurdle #4 — *The wireless world is ready, willing and eager to embrace m-commerce.* Whew...whoever came up with that one has to be smoking some funky stuff.

There is a ton of fluff about how mobile commerce will be used to do everything from pay bills, trade stocks, shop, make dinner and theater reservations, and pay the baby sitter. Truth is, it's mostly short messaging service messages (SMS). So far, the promised Web-like system on all the pundits' lips has failed to materialize. And, ditto for the security issues such as those that plague Bluetooth.

If you go back to hurdles one and two, they have to be resolved before this one even gets off the runway.

Mambo...er hurdle #5 — This is the proverbial "Which came first, the chicken or the egg?" argument. Conventional wisdom says that you've gotta have something there to entice the consumer. This means building out the infrastructure and offering killer services on it.

Companies have just spent $130 billion to buy spectrum. This means that there is tremendous pressure to reduce the debt incurred. But the question "Will they come if you do build it?" has some merit. Unless the system is user-friendly, reliable (99% of the time) and it offers value, there is real concern that all those services could go the way of ISDN.

If things don't get a jump start soon, a lot of players will be talking to banks (Deutsche Telekom has more than $50 million in debt burden due to spectrum purchases, and it has almost destroyed its credit rating). Furthermore, to build the infrastructure will add at least $100 billion to the 3G bill. Even major players like Siemens don't expect more than 15% of Europeans to be using 3G applications by 2005 (I think this may be optimistic).

So, all that being said, is the forecast for 3G all gloom and doom? Of course not. The biggest issue is whether the technology will do what is promised. If so, there are big bucks to be made. If not, well, remember the recent dot-com industry.

There is also a real concern that 3G spectrum will be used only to carry excess voice traffic — hardly a moneymaker for anyone.

But, as my last word, I just found out that Ericsson has debuted a Bluetooth pen called the Anoto. It automatically synchronizes everything it writes and can send the things it registers as an e-mail, short message or fax — if used on paper with a special pattern printed on it.

For a '70s generation guy, this could be the greatest thing since Ginkgo biloba.

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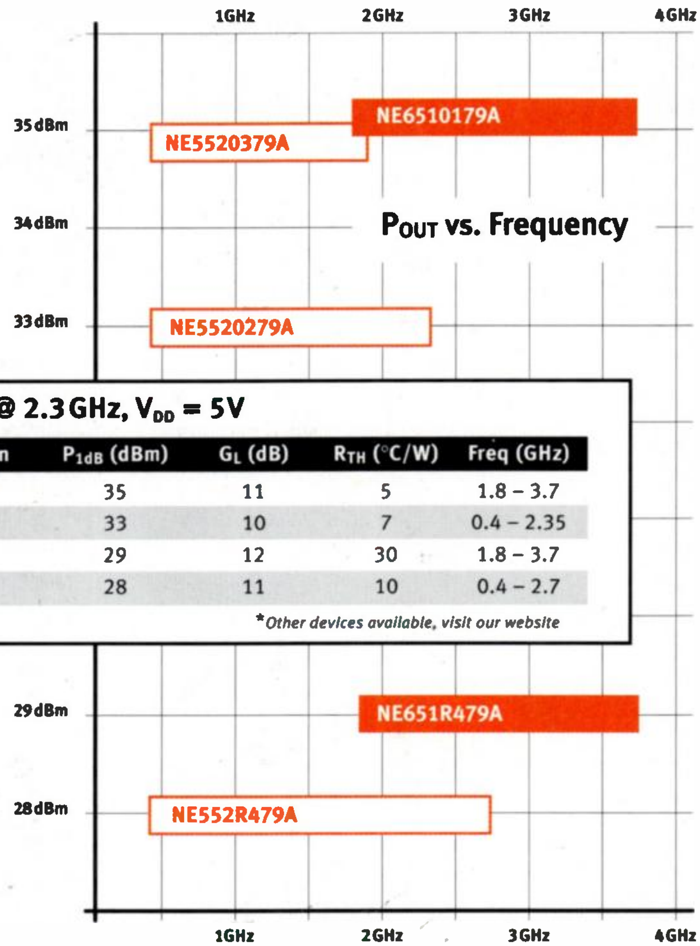

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