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IN THIS ISSUE



FEATURES

Featured Technologies:

Amplifiers

Concepts and implementation of a GSM PA/ front-end module — Advantages of high-level integration in GSM front ends.

- By Atanas Pentchev, Paul Swinkels and Guido Paola



26

Integrated Subsystems

Crest factor analysis for complex signal processing — Understanding the complexities of summing digital signals. - By Brad Andersen

Cover Story:

(58)

68

Encryption Technologies

Securing wireless communications — Cryptography – today's hot topic for wireless network users.

- By Paul Lesso, PhD

Tutorial:

Software Integration design — the heat is on for systems on a chip — A design methodology for efficient implementation of complex DSP algorithms in FPGAs. — By Johannes Steensma

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IN THIS ISSUE

DEPARTMENTS

0	
	Editorial10
0	Calendar/Courses14
+	Regulatory Update16
U	Editorial Forum/News18
0	Literature
	Software
	Top Product of the Month
	Product Focus <i>EMI/RFI</i>
	Products
	Glossary
	Get the Data Now
	Classifieds103
	RF in Ernest106





ON THE WEB

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INFO/CARD 8

RF editorial Wireless plays a role in the tragedy



By Don Bishop Editorial Director dbishop@primediabusiness.com

At this writing, a little more than 48 hours has passed since four airliners were hijacked on the morning of Sept. 11. Three were used to attack and destroy the New York World Trade Center and to damage the Pentagon in Washington. The destruction took the lives of thousands and injured a number yet uncounted in an action that the President has called an act of war.

By the time you read this, much more will be known about those who planned the hijackings and our nation's response than we know today. What seems clear even this early is that among other important factors, wireless and encrypted communications may have helped those who planned and carried out the attacks. Wireless communications also is helping those with a responsibility to protect lives and property, to rescue the injured and recover the dead, and to pursue those responsible for the attacks.

We regret that the fruits of wireless communications equipment design and development might be applied to attack our centers of commerce, military control and political leadership. Whether the delivery of high technology into the hands of those who want to use it for harmful purposes is inevitable in a free society has been debated and will continue to be debated. Off-the-shelf wireless communications technology and encryption software is more sophisticated than some of the most sensitive and restricted technology of years past.

At the same time, wireless communications devices are being used to support rescue and recovery operations and military readiness.

On a small scale, an individual wireless carrier's store in Manhattan handed out phones for New Yorkers fleeing collapsing buildings to use in calling relatives and friends—and let people sleep in its store overnight. On a larger scale, within 36 hours of the attack, Nextel Communications lent 2,000 combination wireless phones and two-way radios with unlimited airtime to federal, state and local government agencies and to emergency service provider organizations such as the American Red Cross in New York, Washington and Boston, and Nextel and Motorola, its phone manufacturer, pledged 10,000 more.

Wireless systems under development will facilitate remote video and robotic searches. These systems will also assist in the disposal of weapons of mass destruction without exposing public safety workers or soldiers to personal risk.

As we look to the military for protection and perhaps some form of retaliation, we are reminded of its need for wireless communications and the pressure to reallocate some of its frequencies for commercial applications. The Department of Defense now may find more support for its resistance to a reallocation.

Close to home, we're fortunate that all of Primedia's employees in New York and Washington are reported safe. Primedia Business, this magazine's publisher, has contributed to the American Red Cross and the September 11 Fund established by the United Way and the New York Community Trust. This is one small way that we can show our support for the victims, the rescue crews and others. We extend our sympathy to those who may have lost loved ones or friends in the Sept. 11 tragedy.

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- 26–28 5th Intl. Japan 3G Mobile Systems Singapore – Information: IBC Asia Ltd. Tel. 065.835.5102; Fax 065.733.5087. e-mail: cassie.mah@ibcasia.com.sg

DECEMBER

- 3-6 Internet World Wireless West 2001 San Jose – Information: Web site: www.ccievents.com
- 11–13 Bluetooth Developer's Conference 2001 San Francisco – Information: Web site: www.key3media.com/bluetooth/
- 11–13 Streaming Media East 2001 New York Information: First Conferences. Tel. 888.301.8890.

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AGILENT TECHNOLOGIES – RF and Microwave Fundamentals – Dec. 4–6; Network Analysis Measurements – Oct. 16–17; Spectrum Analysis Measurements – Oct. 18–19. Information: Tracey Bull, Eskdale Rd., Winnersh Triangle, Wokingham, UK; Tel. +44.118.927.6741; Fax: +44.118.927.6862; e-mail: tracey_bull@agilent.com

ALEXANDER RESOURCES – 3G Wireless: Promises & Realities – Oct. 29-30, Washington DC. Information: Jeff Stone, Alexander Resources, 15851 N. Dallas Pkwy, Addison, TX 75001; Tel. 972.818.8225; Fax: 972.818.6366; e-mail: jstone@alexanderresources.com.

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- 11–14 International Radar Symposium India Bangalore – Information: Web site: www.irsi2001.com
- 29–30 TechCON2001 Bangalore Information: Internet Wireless Initiative of India. e-mail: priya@integramicro.com

JANUARY 2002

- 8–11 Consumer Electronics Show 2002 Las Vegas – Information: Web site: www.cesweb.org
- 22–24 Photonics West San Jose Information: Web site: www.spie.org/exhibitions/pw
- 28-31 COMNET Conference Washington DC Information:

Web site: www.idgworldexpo.com

JUNE 2002

28–31 COMNET Wireless – Las Vegas – Information: Web site: www.idgworldexpo.com

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 UCLA – Multirate Signal Processing in Transmitter and Receiver Designs – Nov. 14–16; Communications Systems, Using Digital Signal Processing – Nov. 26–30, Los Angeles. Information: Information Systems and Technical Management Short Courses.
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UNIVERSITY OF WISCONSIN MILWAUKEE – Semiconductors & Computer Concepts – Oct. 18–19, Schaumburg, IL; Nov. 8–9, San Diego. Information: Tel. 800.222.3623; Fax 800.399.4896; Web site: www.uwm.edu/dept/ccee

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RF Washington watch

FCC auction opens door for designers

by Delaney M. DiStefano

The largest FCC auction ever

On Oct. 30, 2001, the Federal Communications Commission will auction off 15,514 licenses, the largest number of licenses sold in an auction since the FCC began auctioning spectrum. This auction is titled "Lower and Upper Paging Bands Auction," or "Auction 40." In addition to the UHF and VHF paging channels, which make up the bulk of the licenses offered in this auction, the remaining 929 and 931 MHz paging licenses left unsold in Auction 26 will also be re-auctioned.

"The opening of messaging and fixed wireless services are of particular interest to the design sector because they offer a new opportunity in times of a scaled-back economy."

> This is an important auction for many operators because the FCC has continued its policy of spectrum flexibility and will allow a multitude of services on what were traditionally one-way paging channels. Among those services now allowed are one-way messaging, two-way messaging and fixed wireless services.

Opportunity knocks

The opening of messaging and fixed wireless services are of particular interest to the design sector because they offer a new opportunity in times of a scaled-back economy. Of special interest to many operators is the ability to use the offered channels, especially the UHF and VHF channels, as trunking control channels in existing two-way systems. If you are looking to see what may happen in this spectrum, it would likely benefit you to watch this auction.

Many people are aware of the spectrum crunch due to the 800 MHz channel consolidation taking place. The consolidation has resulted in the lack of available, exclusive channels in major and secondary markets throughout the United States. Many operators are looking for a solution, and this may be the one.

Internet-based bidding a first

Auction 40 also marks the first time we will be using the Internet as the bidding platform. This is an ambitious plan on the part of the FCC. Previously, a dial-up system was used in which there was no gray area, as is a potential with Internet bidding. Bidders would dial into the FCC, log in using four different passwords, and place their bids. With the Internet-based system, bidders simply go to an FCC auctions Web site and log in from there. It will be interesting to see how the many irks of the Internet will play out in how the bids arrive at the FCC.

To protect bidders, the FCC will implement a passcard ID system. Each bidder will receive a passcard in the mail prior to the auction. The card has a display on it in which an ID number appears. The ID number changes about every two minutes. This system, says the FCC, will ensure security.

It is impossible to determine how long an auction will last. In any FCC auction, all licenses in all markets are eligible to be bid until the auction closes. In most instances, an auction closes when a round goes by in which no one places a bid. This auction is likely to last longer than most recent auctions. The sheer number of licenses available, coupled with the new Internet format, will no doubt add to its length.

For anyone familiar with the previous bidding software, the new Internet format looks completely different. What is also different is how one will be able to monitor the auction. Before, the FCC had what it called an auction-tracking tool with which one could manipulate the round result data to gain information or incite into the auction bidding trends. Now, with the Internet-based software, it appears to be more difficult to gain a broad look at the bidding trends across the country or among the bidders themselves. It is not clear why this new system was designed in a way that will limit bidders from gaining, at a glace, information that was once previously available. To be fair, it may be the large volume of licenses available that is the limiting factor. Regardless, I am looking forward to what will likely be a challenging auction for both the bidders and the FCC.

RF

About the author

Delaney M. DeStefano is a senior associate with the law firm of Schwaninger & Associates, P.C. DeStefano is a member of the New York State and District of Columbia Bars and a member of the FCC Bar Association. DeStefano's primary practice is in wireless telecommunications. She is a veteran of several FCC auctions.



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RF news

God bless America



By Roger Lesser Editor rlesser@primediabusiness.com

I'm sorry that this is not going to be my usual tongue-in-cheek approach to issues affecting the world of design and communications. The events of the cowardly terrorist attacks in New York and Washington DC have made any thoughts I had meaningless at this point.

As I write this, the attacks are barely four hours old and it has truly had an impact on me. It has had an impact on all of us.

My son, Ben, worked a block from the World Trade Center towers just a few months ago. Ben is now a reporter for a newspaper in New Jersey and watched from his office window as the first tower collapsed. His telling me this caused me to pause and say a prayer for his safety and for those in the towers. As he told me about what he saw, I reflected back to two years ago when I stood with Ben and my wife and daughter at the top of one of the towers. We marveled at the view and at the splendor of New York. Now the towers are gone.

I thought also of my colleagues and of those companies, agencies and others we do business with everyday who work in New York. Again, I take pause to pray everyone, and their family and friends, are safe.

As you may know, I'm a retired Air Force Lt. Col. When I heard of the attack on the Pentagon, I was immediately brought back to the time I spent in those hallowed halls. The best and the brightest our country, and our military, has to offer make it to that building. And now many have lost their lives in defending our freedoms.

I am horrified. I am angry. But I am proud. I'm proud of my country. I'm proud of our military, police, firefighters, doctors, nurses and EMTs. I'm proud of the technology that you, the designer, have given these people to save lives. And, I hope, bring justice to those who caused the senseless attacks.

This is a defining moment for Americans (and the world). As a history buff, I have read many books concerning the attack at Pearl Harbor. The one thing that has always struck me is the words of Admiral of the Japanese fleet, Yamamoto. You've heard it before, I'm sure. But let me remind you. He said, "I fear we have awakened a sleeping giant." As was the case in 1941, the United States is no longer a sleeping giant.

You, as a designer engineer, and the company you represent will be an important asset to our military and security forces. Remember, we no longer have the military-based industries we had 10 years ago. Also, remember we have one-third less military forces than we did 10 years ago. The federal government, specifically the military and security forces, will depend on you and the commercial-off-the shelf technologies you develop. Command, control and communications (C³) will be where you will have the most impact.

I'm not one for the melodramatic, but I was honored with three flag presentations while I was in the service. I plan to fly one of them everyday.

Mobile commerce market young, but growing

Still yet to be a financial success for most carriers around the world, mobile commerce is a work in progress, according to Cahners In- Stat Group, Scottsdale, AZ. The research firm estimates that, on a global basis, 9.2 million wireless subscribers were m-commerce users at the end of 2000, representing a total value of \$264 million.

Despite these figures, m-commerce has come a long way in its brief existence as a value-added WAP service. Valuable lessons learned by carriers, content providers, wireless application service providers and others in the value chain will help m-commerce transactions to grow slowly during the next five years, Cahners said; except in Japan, where \$2.3 billion in transactions are forecast by 2005.

The main reason for the slow uptake of m-commerce, according to Cahners, is that services launched before they were ready. To improve the state of m-commerce, the firm said, it will be necessary to avoid repeating the mistakes that have already been made.

Mobility must go mainstream for WLAN success

The world wireless local area network (WLAN) market is searching for mainstream acceptance in network access. According to new research by Frost and Sullivan, San Jose, CA, WLAN providers will have to get just that to realize their full profit potential.

The report, *World Wireless Local Area Network Industry*, projects that by 2007, annual shipments will reach over 20 million units and exceed \$1.5 billion in revenues. Companies with the most potential for success in this market will be those who can best demonstrate the benefits of wireless LANs over their wired counterpart.

WLAN technology won't be able to match the speeds of wireline LANs, the report said. However, a wireline solution is incapable of attaining the mobility and convenience of a wireless network

Forward-thinking wireless LAN vendors are fine-tuning their offerings to make them simpler for end-users to install and maintain. It's only a matter of time before participants' survival depends not only on providing a hardware, Frost and Sullivan said, but also an overall networking system encompassing all areas, including hardware, software, manageability and security.

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	SYM-25DLHW SYM-25DMHW SYM-24DH SYM-25DHW SYM-22H	40-2500 40-2500 1400-2400 80-2500 1500-2200	+10 +13 +17 +17 +17 +17	22 26 29 30 30	1.2 1.3 1.2 1.3 1.3	6.3 6.6 7.0 6.4 5.6	7.95 8.95 9.95 9.95 9.95
	SYM-20DH SYM-18H SYM-14H SYM-10DH	1700-2000 5-1800 100-1370 800-1000	+17 +17 +17 +17	32 30 30 31	1.5 1.3 1.3 1.4	6.7 5. 75 6.5 7.6	9.95 9.95 9.95 9.95

*E Factor = (IP3 (dBm) – LO Power (dBm)) = 10. See web site for E Factor application noise ADE models protected by U.S. patents (533:525. MBA Blue CetI™ model protected by U.S. patents 553:4830 5640/32 5640699.

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Aethercomm amplifier selected by Northrop-Grumman — Aethercomm, San Marcos, CA announces that it has been selected by the Northrop-Grumman Corporation, Glen Burnie, MD to design, develop and manufacture the high-power solid state LO driver amplifier for an airborne application. Aethercomm is a supplier of high-power SSPA s for military, commercial and satellite communications customers.

TMS Selected by Raytheon to develop test methodology for Tondelayo 5.8 GHz wireless LAN chipset – Turnkey Manufacturing Solution, San Diego, a multinational company specializing in providing *Continued on page 22*

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RFIC test services, recently announced that it was chosen by Raytheon, Marlborough, Massachusetts to develop the test methodology for Raytheon's Tondelayo Wireless LAN (WLAN) chipset. TMS was chosen because of its highfrequency RFIC test expertise.

Repeater Technologies receives \$11 million order to supply repeaters for China's national WCDMA network - Repeater Technologies, Sunnyvale, CA announces that it has a received an order worth \$11 million to provide its OA850C network repeaters to Capitel Group of Beijing, for China Unicom. Capitel, Repeater Technologies' long-standing distributor in China, will supply these repeaters to that nation's second largest telecom firm, China Unicom, with nearly 30 million subscribers. China Unicom will use these repeaters to enhance coverage as it builds out its CDMA network.

Ericsson licensing phone technology – Ericsson, Stockholm, Sweden, announces it will license its mobile phone technology to other manufacturers of phones and wireless devices. Ericsson Mobile Platforms began operation Sept. 1 with 800 employees. The headquarters will be Lund, southern Sweden, and Ericsson will maintain control of the new technology-licensing company. Ericsson plans to license complete component specifications, printed circuit board layouts and software. It will also help customize products for customers' devices.

APLAC distributor appointed for Singapore, Malaysia & Thailand markets – APLAC Solutions Corporation, Helsinki, Finland has signed a distributorship agreement with PCB Graphtech Pte of Singapore, authorizing PCB Graphtech to represent APLAC Solutions' products and collateral services in Singapore, Malaysia and Thailand.

Oki signs deal with North Communications to bring VoIP to **Brazil** — Oki Network Technologies' (Oki NT), Sunnyvale, CA announces that it has signed a deal with North Communications, one of Brazil's largest VoIP, telecommunications and network service providers. Under terms of this agreement, North Communications will act as the primary source in Brazil to resell and service VoIP solutions to the largest IT market in Latin America.

Fujitsu Compound Semiconductor, Nortel Networks team — Fujitsu Compound Semiconductor, San Jose, CA, announces that Fujitsu Quantum Devices and Nortel Networks, San Jose, CA, have agreed on joint specifications for high-performance receiver devices for use in 10 Gb/s optical communications products. This agreement on joint specifications between FQD and Nortel Networks provides customers with two sources for high-performance devices with common package outline and pin allocation for common board layout.



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Concepts and implementation of a GSM PA/front-end module

Advantages of high-level integration in GSM front ends.

By Atanas Pentchev, Paul Swinkels and Guido Paola

The ultimate goal of the wireless industry is to give everyone an inexpensive and reliable means of communications anywhere, anytime and to anyone. The pursuit of this goal and operation in a highly dynamic and competitive environment, challenges handset manufacturers with continuous expectations to offer phones with increased functionality and performance levels. It also challenges manufacturers to reduce size and weight and to increase talk times.



Figure 1. The two integration concepts.

Also, the emerging new cellular standards predicate the demand for multimode, multiband sets with ever-increasing complexity. The designers are tasked with meeting these requirements, while simultaneously reducing cost and time-to-market.

In that vein, one of the enabling factors for achieving the leading edge in this competitive environment is the use of cheaper components with extended degrees of integration in all stages of signal processing - RF/IF, baseband and digital.

Current levels of integration

The level of component integration used in different sections of the GSM mobile sets is still divergent. Currently, the highest level is achieved in the baseband (BB) section. Typically, the handsets contain two BB ICs (excluding the discrete memory chip): a BB processor and an application-specific analog interface. In the RF/IF path, however, the situation is not the same.

Today, there are a number of different transceiver IC architectures. They typically combine the components of the receiver chain with local and transmitter frequency VCOs, synthesizers, analog PLL loops, IQ modulation/demodulation and power control loops.

The next generation of highly integrated ICs, which combine all of these functions, is beginning to appear on the horizon. The advantages of this higher level of integration, however, are not as explored in the transmitter chain and in the implementation of the front-end functions. The dualband GSM handsets still contain, as separate components, the power amplifier (RFIC module), the front-end module (combining the diplexer and Tx/Rx switches), directional couplers and the power detector.

Scenarios for further front-end integration

Two scenarios are foreseen for the evolution of the dual- or triple-band GSM architecture. This evolution depends on the device and on which core might be chosen for future integration of the frontend and transmitter functions of this future GSM architecture

The first one is based on the expansion of the switchplexer's functionality. This is done by incorporating the Rx SAW filters⁷, and eventually the directional couplers, in the module. The switchplexer modules are miniature, high-performance units, built on sophisticated low-temperature co-fired ceramic (LTCC) substrates. These modules are constructed of more than 10 dielectric layers with differing thickness. The implementation of the additional functions is relatively straightforward, but including these functions would increase the size of the module, and could have a negative impact on the net cost benefit.

The other evolutionary track revolves around the PA module and increases gain functionality. The integration of the power control components (directional couplers, detectors and controller IC) in the PA module significantly simplifies the design of the power-control loop. One force working against this

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GAL-4	DC-4000	14.4	13.5	±0.5	17.5	4.0	34	93	65	4.6	1.49
GAL-51	DC-4000	18.1	16.1	±1.0	18.0	3.5	35	78	65	4.5	1.49
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Figure 2. A block diagram of the module.

integration is that the functions of the power controller IC have already been included in other ICs, so the direct cost benefits are not obvious. Also, the handset makers have to be convinced that they do not need the ability to tune the control loop anymore. The same holds for the integration of the transmit VCOs in the PA. These functions will be increasingly integrated in the transceiver ICs as they develop.

Another advantageous integration step, starting with the PA, is the implementation of the switchplexer's functions. The accomplishment of this step presents a significant engineering challenge because it has to make use of the much simpler substrate of the PA. The consecutive steps in these two integration concepts are shown in Figure 1.

Design objectives and limitations

The unit discussed in this article is a prototype of the first member of a PA/ FE module family that offers a significant increase in functionality. The module is intended to replace almost all of the building blocks used in the traditional dual-band GSM transmitters' architectures: PA, low-pass filters, and directional couplers, as well as power detectors and the switchplexer. It could be used with custom-designed and offof-the-shelf transceivers and power controllers.

The objectives pursued with this developmental concept, grouped by category, include:

• Functionality — power amplification, multiplexing of extended global system for mobile communications (EGSM) and digital communications systems (DCS) frequency bands, Tx/Rx switching and monitoring of the output power level. • Price — clearly competitive to the combination of a GSM/DCS PA, coupler + detector and switchplexer module.

• Performance – equal to the performance level offered by "state-of-theart," separate front-end and Si PA modules.

• Size — 13.75 x 11mm (~150 mm²), land grid array second-level interconnect technology, plastic cap.

• Ease-of-use — self-contained (none, or a significantly limited number of components on the main PCB). No external tuning required.

To meet these cost objectives, the accepted set of technologies for this development was limited to technologies, presently used in the standard PA modules:

• MOBi3 technology (a double polysilicon bipolar technology with $f_T = 25$ GHz, $f_{max} = 40$ GHz and breakdown V_{CE0} >5.5 VDC) for implementing the active devices, the driver RFICs and output transistors.

• Two complementary passive integration and interconnection technologies: LTCC and passive integration on high ohmic (>3k\Omega/cm) silicon substrate. The LTCC substrate consists of five dielectric layers (ϵ_r =9.5) with total thickness of 550 μ m and C_u metalization.

• PIN diode dies for switching elements in the Tx/Rx switches.

Top-level overview

The module based on this design consists of two power amplifier line-ups and a front-end circuit (Figure 2). The amplifiers are biased ($V_{supply,nom} = 3.5$ VDC) through separate input pins, but they share common control signals: V_{BAND} and V_{APC} . The foremost is a logical one, which enables the selected lineup. The low level (below 0.7 VDC) activates the 900 MHz amplifier. A V_{BAND} level above 1.7 VDC selects the 1800 MHz line-up. The V_{APC} signal (0.2 – 2.2 VDC) controls the gain, and, respectively, the output power level of the active amplifier. In both PA line-ups, circuits are provided for monitoring the output power level. These circuits produce current signals, which are proportional to the actual collector current of the final stages of both line-ups and, consequently, to the output power. Those circuits use a DC bias separated from the PA's supply voltage.

The FE part, which occupies ~40 mm^2 of the substrate, is constituted of two PIN-diodes SP2T switches and a diplexer. Two control signals select between the Rx and Tx states of the switches. In the high state of the control signals (2.8 VDC), the Tx states are active, and the consumed currents are about 9 mA.

Power amplifiers/detectors

The two power amplifier line-ups have identical configurations. They include a driving RFIC, a single-ended last stage and an output-matching circuit implemented on a passive silicon die. The RFICs contain two RF stages, a part of the interstage matching circuit and biasing networks, which settle the quiescent currents of all RF transistors in function of V_{APC} voltage. The design of a similar RFIC is described in more detail in². The IC designs used in this module include additional band switches, used to enable the V_{APC} signal in the amplifier selected by V_{BAND} .

The interstage matching circuits between the RFICs and the final stages are implemented with discrete capacitors and inductors integrated in the LTCC substrate. To increase the overall gain of the DCS line-up, a prematching metal-oxide semiconductor (MOS) capacitor is used³.

On both of the output power amplifier device (PAD) dies, circuits for sensing the collector currents are implemented. They consist of single transistor cells, connected in current mirror configuration to the rest of the PADs. Additional networks for RF decoupling and inverting the slope of the detected current are also included. The slope inverter allows the current, delivered by the mirror transistor, to be pushed in a load connected to the ground. Therefore, the voltage developed on the load will be proportional to the PAD's

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Figure 3a. Detector signal performance over temperature variation.



Figure 3b. Power detector performance.

collector current and, respectively, to the output power. The module is compatible with the power controllers designed for use with diode detectors.

The ratio between the emitter areas of the mirror transistors and the PADs are chosen in such a way that the currents are in the same range: ~ 0.5 mA to 10 mA for the GSM and DCS channels. In the operating range of the output power, the sensitivity of the power detectors varies from 30 to 200 μ A/dB. At the lower power level (-5 to 5 dBm), at which the power control loop also has to be operational, the sensitivity is still higher than 10 μ A/dBm.

Good thermal coupling between the mirror and the RF transistors contributes to the stability of the detector's performance over temperature (Figure 3a). Another important parameter – the dependence of the detected signal on the PA's supply voltage – is shown in Figure 3b.

All of the capacitors, and most of the inductors, integrated in the outputmatching networks of the PAs are integrated on the passive silicon dies. This approach provides significant savings on the occupied substrate area and also increases the accuracy and repeatability of the integrated components. The matching circuits are designed to suppress the second and third harmonics to a level lower than -50 dBc. In combination with the switchplexer, the simulated harmonics levels were less than -75 dBc for GSM and -70 dBc for the DCS band. This allowed avoidance of separate low-pass filters and a decrease of the insertion loss in the Tx channels of the front end by 0.2 dB (The module transmitter characteristics, output power and efficiency, are shown on Figure 4 and Figure 5, respectively, for GSM and DCS bands).

Front-end design

Several front-end architectures have been evaluated, not only in terms of performance – insertion loss, isolation between the channels and harmonics suppression – but also in the production yield and sensitivity to components and processes spread.

Most of the attention has been paid to two diplexer structures: one consisting of simple low- and high-pass filters, the other incorporating a combination of different low-pass and stop-band filters in the GSM branch and high-pass and stop-band filters in the DCS branch^{4,5}. Although the second type is superior in some of the mentioned parameters, the use of the simple lowpass/high-pass design has been chosen. This choice proved to be more tolerant to the inaccuracy of the LTCC process, used as an integration technology for the entire diplexer circuit. Both of the Tx/Rx switches are built up according to the conventional scheme consisting of a series and a shunt PIN diodes separated by a $\lambda/4$ line.

The major challenges faced in the implementation of the chosen FE architecture (see Figure 6) were related to the composition of the LTCC system. In this case, only five dielectric layers had uniform permeability and almost constant thickness. This LTCC substrate is







Figure 4b. GSM-band module transmitter characteristics, efficiency vs. VAPC

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Figure 5a. DCS module transmitter characteristics, load power vs. VAPC-

not well-suited for integration of capacitors, nor is it suitable for implementation of real three-dimensional RF structures using multiple 50Ω transmission lines located on different layers and shielded with ground planes.

How the challenges were met

The first problem - integration of capacitors - was especially important for the design of the series capacitors, constituting the high-pass filter in the

DCS branch of the diplexer. To preserve the proper high-pass response, a major requirement is to keep the value of their parasitic capacitance to ground minimal. A conventional design of a series plate capacitor, integrated in the used LTCC substrate at a maximal distance from the ground plane, would have at least 20% shunt capacitance.

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A significant improvement of the DCS-band performance of the diplexer has been achieved by minimizing the

GSM-Tx

Input

parasitic capacitances and the length of the interconnects. This results in a broadband, low-loss performance of the DCS channels.

The second limitation, originated from the attributes of the used LTCC substrate, is the useful range of characteristic impedances (Z_0) , feasible with stripline transmission lines. The highest impedance, achievable with stripline with maximally distant ground planes and minimal allowed $(100 \ \mu m)$ width of the inner conductor, is about 45 Ω . The investigation of the loss mechanisms in the used LTCC technology⁶ has shown that the cross-section of narrow strips (less than 200 μ m) is rhomboidal, rather than rectangular, which decreases the effective RF conductivity and causes relatively high losses in the narrow striplines.

To overcome this problem, the approach has been to minimize the losses by implementing the $\lambda/4$ transmission lines with lower characteristic impedance and simultaneously obtain good impedance matching of the Rx channels.

The PIN-diode dies used offer a good compromise between low off-capacitance ($C_{OFF} < 0.3 \text{ pF}$) and reasonable onresistance ($R_{ON} < 2\Omega$). The necessary performance of these PIN diodes has been obtained by mounting them as a naked die to avoid the parasitic capacitance's increase of diode packaging. The same diodes have been used both for series and shunt applications.

Usually, a resonant circuit, parallel to the series diodes, is used to increase the isolation of the diodes in series switches. The use of the high-performance bare PIN diodes made it possible to implement a simpler switch design that doesn't need such resonant circuits to obtain sufficient isolation.

The receiver characteristics of the FE are shown on Figure 7 and Figure 8, respectively, for GSM and DCS bands.

Performance summary

The major transmit and receive characteristics of the module are presented in Table 1 (page 36). The table includes the averaged parameters of both commercially available double-band, LTCC FE modules, as well as the ones described in this design. The comparison shows that the proposed PA + FE design has been successfully adopted to the simple LTCC



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Switch



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NC302L	10 Hz – 3 GHz				
NC303	10 Hz – 8 GHz				
NC401	100 MHz – 18 GHz				
NC406C	18 GHz – 110 GHz				

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MODEL	FREQUENCY RANGE	OUTPUT ENR			
NC502/15	0.2 MHz – 1 GHz	31 dB			
NC503/15	0.2 MHz – 2 GHz	31 dB			
NC506/15	0.2 MHz – 5 GHz	31 dB			
NC513/15	0.2 MHz – 2 GHz	51 dB			

Broadband Amplified Noise Modules

- Designed for circuit board mounting.
- Provide a high-level noise output.
- Available in 24- and 14-pin packages.



NC2000 SERIES Standard Models					
MODEL	FREQUENCY RANGE	OUTPUT			
NC2101	100 Hz – 20 kHz	0.15 Vrms			
NC2105	500 Hz - 10 MHz	0.15 Vrms			
NC2201	1 MHz – 100 MHz	+5 dBm			
NC2601	1 MHz – 2 GHz	-5 dBm			

Broadband Noise Generators

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MODEL	FREQUENCY RANGE	OUTPUT POWER			
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UFX7108	100 Hz – 500 MHz	+10 dBm			
UFX7112	1 MHz – 2 GHz	+0 dBm			
UFX7218	2 GHz – 18 GHz	-20 dBm			
UFX7911	5 MHz – 1 GHz	+30 dBm			

fx7000 series





system and, as a result, the performance level of the Rx channels of the combined PA plus FE module is comparable to the stand-alone FE modules.

The overall performance of the Tx channels is already comparable to the combination of the specification figures of separate state-of-the-art PA and FE. It's important to realize, however, that in a practical situation with a separate PA and FE, significant additional losses can also occur due to the coupler, which has to be included for power detection. The matching between PA, coupler and FE can also cause significant mismatch losses and will require major engineering efforts.

The harmonics suppression in the DCS band of this prototype is not yet sufficient, but can be easily optimized.

Conclusions and future potential

The design discussed in this paper proves the feasibility of the concept for further increase of the integration level in GSM front ends by implementing functionality in the PA module that was typically accomplished by stand-alone switchplexers and directional coupler/power detector units. The unit is completely self-contained and requires no external tuning or additional components.

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Several paths are possible for the future evolution of this concept.

The first one is toward further miniaturization, maintaining the already- achieved functionality. The small number of the discrete components (four PIN diodes, two SMD inductors, two resistors and six capacitors) used in the FE circuit is a good precondition for reduction of the area occupied by the FE substrate area to about 25 to 30 mm². Reduction of the whole module dimensions to less than 100 mm² is also achievable.

A second possible evolutionary path is integration of the power controller

> 0.0C 0.0B



MI

Figure 7b. Measured GSM receiver characteristics of the FE.

IC in the module.

A third possible path is the integration of the RF SAW/BAW filters of the receiver paths. There is potential to simplify the construction of the switches and significantly increase the overall performance of the Rx channels. This, however, depends on advances and new concepts in SAW/BAW filters⁷.

For instance, maintaining the existing SP2T configuration of the DCS switch and connecting its Rx output to a SAW/BAW diplexer (which discriminates between the DCS and PCS Rx frequencies) will modify the current dualband, front-end architecture to a tripleband solution.

Considering these evolutionary scenarios provide an interesting angle for considering the potential and the flexibility of the front-end integration approach used in the discussed module design.

Continued on page 36

A





Figure 8a. DCS receiver characteristics of the FE: measured and deembedded insertion loss.



		Parameter	Avarage Characteristics of stand alone FE modules	Performance of PA+FE module
		Ins. Loss [dB]	0.9	n.a.
		Pload [dBm]	n.a.	35
	Тх	Efficiency [%]	n.a.	40
		Max. Level 2nd Harm.	n.a.	-36 dBm
W		Max. Level 3rd Harm.	n.a.	-30 dBm
S		Atten. @ 2nd Harm.	35 dB	n.a.
Ш		Atten. @ 3rd Harm.	35 dB	n.a.
	Rx	Ins. Loss [dB]	0.7	0.9
		V.S.W.R		1.2
	In-band Tx-Rx Isol. [dB]		30	28
	Cross-band Tx-Rx Isol. [dB]			21.5
		Ins. Loss [dB]	1.3	n.a.
		Pload (dBm)	n.a.	32.4
	Tx	Efficiency [%]	n.a.	34
		Max. Level 2nd Harm.	n.a.	-20 dBm
		Max. Level 3rd Harm.	n.a.	-25 dBm
S		Atten. @ 2nd Harm.	30 dB	n.a.
		Atten. @ 3rd Harm.	40 dB	n.a.
1-1-1	Rx	Ins. Loss [dB]	1.1	0.8
		V.S.W.R		1.2
	In-	band Tx-Rx Isol. [dB]	22	26
	Cros	s-band Tx-Rx Isol. [dB]		22.5

Table 1. Averaged parameters of both commercially available double-band, LTCC FE modules and the proprietary module.

Continued on page 38

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About the author

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[5]. T. Watanabe, K. Furutani, N. Nakajiama, H. Mandai, "Antenna switch duplexer for dual band Atanas Pentchev is a member of the technical staff with Philips Semiconductors in Nijmegen, The Netherlands, where he is working on the development of power-amplifier modules for mobile sets. He graduated from Budapest Technical University in 1983. Pentchev has more than 15 years of radio engineering experience in the development of military and consumer electronic equipment. His professional interests focus in design of on-system and device-level of transceivers intended for use in radars, point-to-point radios, satellite and mobile terminals. He can be reached at:

Atanas.Pentchev@Philips.com

Paul Swinkels is the development manager for power-amplifier modules at Philips Semiconductors in Nijmegen. He has worked as an IC designer, project manager and marketing manager with Philips Semiconductors since 1986. He received his masters degree in electrical engineering from the Eindhoven Technical University, the Netherlands in 1986. He can be reached at: Paul.Swinkels@Philips.com

Guido Paola is development engineer at Philips Semiconductors in Nijmegen. He works with power amplifier modules and front-end integration. He received his masters degree in electrical engineering from the University of Catania, Italy in 2000. He can be reached at: *Guido*.*Paola@Philips.com*

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RF integrated subsystems

Crest factor analysis for complex signal processing

Understanding the complexities of summing digital signals.

By Brad Andersen

As the 21st century gains momentum, more and more of today's communications systems are using designs based on digital modulation techniques. This has increased the practice of summing several baseband signals for systems such as CDMA. Such techniques result in composite signals with large crest factors (the ratio of peak amplitude to the rms level of the signal), which can significantly affect the signal quality.

The filtering processes used in the signal generation also result in an increase of the resultant signals' crest factor. Signal fidelity is critical in many such systems, necessitating careful attention to maximizing dynamic range. In particular, optimally employing the dynamic range of digital-to-analog and back converters (DACs and ADCs) is crucial. Also important is the number of bits used for the digital signal processing functions.



Figure 1. Baseband signal process block diagram.

The road to optimal design criterion

The designer would like to operate at the highest possible operating level to maximize the signalto-quantization noise-level ratio (SNR). To prevent spectral splatter, the designer must not allow the signal to saturate, or worse, rollover. In the RF domain, this type of problem will cause distortion of the modulated waveform in the form of higher levels in the frequencies adjacent to the signal's occupied bandwidth and/or other spurious signals.

Tools for better design

In this article, methods will be developed for analyzing complex digital signals to establish the worst-case crest factors. These methods consider the effects of summing signals of different crest factors and different gains, as well as the effects of filtering, including interpolation filtering. With these tools, the designer can determine the precise back-off required to prevent saturation, while maximizing the SNR. For example, a spreadsheet program could be used to determine the signal's crest factor and SNR at all points within a design.

These methods will also show the designer how to determine how many bits will be required to achieve a specified SNR, and reveal interesting results such as that the worst-case crest factor has a root-sum-square behavior. Results will show that, due to digital filtering, the crest factor expansion is similar to the inverse of the noise bandwidth of the filter. The resulting RF envelope crest factor is also developed.

The analysis presented is based on the IS-2000 (cdma2000 or C2K) standard. An instrument was developed and is used to emulates a working base station for testing IS-2000-compatible mobile phones. It provides the ability to provide IS-2000 signals, plus the ability to add an additive white Gaussian noise (AWGN) signal to the composite signal. The analysis techniques were used to guarantee proper sizing of all data paths used in the CDMA baseband generation circuitry. This system is designed to provide the IS-2000 forward-modulation signals to test IS-2000 mobile phones with a number of testing scenarios.

A typical baseband signal processing scheme for IQ modulation of an RF carrier is shown in Figure 1. Each in-phase and quadrature (I and Q) signal is a summation of independent signals with individual scalings. These are summed together and filtered. The filtering may include interpolation to increase the effective sample rate of the signal, simplifying the analog reconstruction filter. Other signals can be summed followed by another stage of interpolation filtering. An AWGN signal is shown as the additional signal for the case of the test set mentioned above. These resulting signals are then used as the I and Q inputs of an IQ modulator to modulate a carrier or intermediate frequency signal.

Independence of signals is mentioned several times, but in actuality, uncorrelated signals generally satisfy the requirements for the resulting conclusions.

To examine the resulting crest factor for the signals of interest throughout the system, methods for determining the crest factor after various signal processing functions are developed. The basic assumptions are given for the signals in the analy-

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S4W2	S5W5	N4W5	4	±0.40
S5W2	S5W5	N5W5	5	±0.40
S6W2	S6W5	N6W5	6	±0.40
S7W2	S7W5	N7W5	7	±0.60
S8W2	S8W5	N8W5	8	±0.60
S9W2	S9W5	N9W5	9	±0.60
S10W2	S10W5	N10W5	10	±0.60
S12W2	S12W5	N12W5	12	±0.60
S15W2	S15W5	N15W5	15	±0.60
S20W2	S20W5	N20W5	20	±0.60
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Figure 2. The crest factor of a sum of two signals as a function of their relative levels.

sis. In the given example, the analysis technique and the considerations will be addressed as well.

Variables and signal analysis

• Baseband signal:

Given: x_i are independent, discrete random variables with zero mean. Crest factor for a bounded, zero mean discrete random variable x can be defined as:

$$C = \frac{\max(|\mathbf{x}|)}{\sigma_{\star}}, \text{ or in dB},$$

20 log 10 (C) dB or 10 log 10 (C²) dB

where :

$$\sigma_x^2 = \sum x_i^2 p_x(x_i),$$

and x_i are the discrete values x may exhibit and $P_x(x_i)$ is the probability of x_i occurring.

• Crest factor of a sum of independent random variables:

The signals in the I channel are used to develop the equations to determine the crest factor:

$$y = \sum_{i=1}^{n} x_i$$

For independent signals, it is wellknown that the power of the resulting signal is the sum of the individual signal's rms power. Thus:

$$\sigma_y^2 = \sum_{i=1}^N \sigma_x^2$$

and the peak level is the worst case situation of adding the peak of each



Figure 3. The baseband filter model.



Figure 4. Interpolation/polyphase filter conversion.

input signal is:

$$\max(y^2) = \left(\sum_{i=1}^N \max(|x_i|)\right)^2$$

Thus, the crest factor is:

$$C_{y}^{2} = \frac{\left(\sum_{i=1}^{N} \max(\mathbf{x}_{i}|)\right)}{\sum_{i=1}^{N} \sigma_{z}^{2}}$$

Summing distributed signals

Consider adding gain scaling to the signals being summed, again referring to Figure 1, with the a_i independent identically distributed (i.i.d.). Let the crest factor of a_i be C_a . And, a_i is the signal *i*, an independent and zero mean, and g_i is the scaling factor for the *i*th signal.

The xi have the identical crest factor as the ai, but each xi may have a different variance, σx_i^2 .

Next, look at determining the crest factor for the sum:

$$y=\sum_{i=1}^N x_i=\sum_{i=1}^N g_i a_i$$

Because the a_i are identically distributed, the previous results may be applied:

$$\max(y|) = \sum_{i=1}^{N} \max(x_i|) = \sum_{i=1}^{N} |g_i| \max|a_i| = \max|a| \sum_{i=1}^{N} |g_i|$$

The variance of y is given from before as:

$$\sigma_{y}^{2} = \mathbf{E} \{Y^{2}\} = \mathbf{E} \left\{ \left(\sum_{i=1}^{N} (\mathbf{x}_{i}) \right) \right\} = \sum_{i=1}^{N} \mathbf{E} \{\mathbf{x}_{i}^{*}\}$$
$$= \sum_{i=1}^{N} \mathbf{E} \{g_{i}^{*} a_{i}^{*}\} = \sum_{i=1}^{N} g_{i}^{*} \mathbf{E} \{a_{i}^{*}\} = \sum_{i=1}^{N} g_{i}^{*} \sigma_{z}^{*}$$
$$= a_{a}^{*} \sum_{i=1}^{N} g_{i}^{*}$$

Therefore, C_y^* is given by:

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Figure 5. Polyphase filter representation.

$$C_{y}^{2} = \frac{\max (|\boldsymbol{a}|^{2}) \left(\sum_{i=1}^{N} |\boldsymbol{g}_{i}|\right)^{2}}{\sigma_{a}^{2} \sum_{i=1}^{N} \boldsymbol{g}_{i}^{*}} = C_{a}^{2} \frac{\left(\sum_{i=1}^{N} |\boldsymbol{g}_{i}|\right)^{2}}{\sum_{i=1}^{N} |\boldsymbol{g}_{i}^{*}|}$$

The crest factor of the sum is multiplied by an expansion factor that is a simple function of the gains. It is always greater than or equal to one.

Worst-case signal combinations

It is interesting (and handy) to determine what set of gains produces the worst-case crest factor. First, consider a sum using two signals with different crest factors. What are the gain settings that will maximize the resulting signal's crest factor? By using calculus to find maximum value of a function, the condition for maximum crest factor can be found using the following summing equation:

$$C_{A}^{2} = \frac{(C_{1}\sigma_{1} + C_{2}\sigma_{2})^{2}}{\sigma_{1}^{2} + \sigma_{2}^{2}}, \text{ since}$$

$$C_{1} = \frac{P_{1}}{\sigma_{1}} \text{ and } P_{1} = C_{1}\sigma_{1}$$

and rearranging terms:

$$C_{A}^{2} = \frac{C_{1}^{2} + C_{2}^{2} \frac{\sigma_{2}^{2}}{\sigma_{1}^{2}} + 2C_{1}C_{2}\sqrt{\frac{\sigma_{2}^{2}}{\sigma_{1}^{2}}}}{1 + \frac{\sigma_{2}^{2}}{\sigma_{1}^{2}}}$$

This analysis shows that the maximum crest factor for the sum of two signals occurs when:

$$\frac{\sigma_1}{\sigma_2} = \frac{C_1}{C_2}$$
 or $\frac{\sigma_1}{C_1} = \frac{\sigma_2}{C_2}$

When this condition is satisfied, the resulting crest factor is found to be:

$$C_{1}^{2} = C_{1}^{2} + C_{2}^{3}$$

(Note the similarity to the root sum squares.)

Figure 2 shows the crest factor of a sum of two signals as a function of their relative levels. The peak value occurs when the ratio of the rms levels equals the ratio of the crest factors, as discussed above. It may also be observed that when the summed signal is made up primarily of one of the input signals, the crest factor approaches that signal's crest factor, as would be expected.

The crest factors used in the plot are two signals summed together: signal 1,



Figure 6. One-half of the example baseband modulate signal.

CF = 11.8 dB; and signal 2, CF = 13.33 dB. The peak crest factor is
$$15.64 \text{ dB}$$
 when the ratio is 1.53 dB ($13.33 - 11.8 \text{ dB}$).

By using mathematical induction, the condition for maximum crest factor when summing N signals can be found. The maximum crest factor for the sum of N signals with different crest factors occurs when the signals satisfy:

$$\frac{\sigma_i}{C_i} = \frac{\sigma_j}{C_j}$$

for any *i* and *j*. Hence:

$$C_{sum}^2 \leq \sum_{i=1}^N C_i^2$$

achieves equality when the signals satisfy the specified ratios. And the maximum crest factor for the sum of N signals, each with the same crest factor, occurs when all the gains are equal. In this case, the crest factor expansion is given by:

$$C_{y}^{2} = C_{o}^{2} \frac{g^{2} \left(\sum_{i=1}^{N} 1\right)^{2}}{g^{2} \sum_{i=1}^{N} 1} = C_{o}^{2} \frac{N^{2}}{N} = C_{o}^{2} N$$

Hence, the maximum crest factor for the sum of N i.i.d. signals, each with the same crest factor, is \sqrt{N} , or (10log₁₀ N) greater than the crest factor of an individual signal.

Baseband filtering

Given an input signal stream y(n)where n is the time variable with the following characteristics:

- * Zero mean.
- * y(n) i.i.d. y(m), $n \neq m$.
- * Each y(n) has crest factor C_y .

Figure 3 represents the baseband filter model. Due to the independence of the successive y(k), the inputs to the filter's summer satisfy the conditions previously used. Observe by inspection that:

$$C_{t}^{2} = C_{\pi}^{2} \frac{\left(\sum_{i=0}^{M-1} h_{i}\right)^{2}}{\sum_{i=0}^{M-1} h_{i}^{2}}$$

Note that this expansion factor is closely related to the reciprocal of the equation for the noise bandwidth, B_N , of a low-pass digital filter:

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INFO/CARD 54

All Diagonal, CF = 1	Worst Case Levels	Typical IS-95 Setup	cal Traffic: Axial. CF=1.414 5 Setup Others: Diagonal. CF=1		Typical IS-2000 Setup
Channel	Level (dB)	Level (dB)	Channel	Level (dB)	Level (dB)
Pilot	-10	-7	Pilot	-12.04	-T
Sync	-10	-16	Sync	-12.04	-16
Paging	-10	-12	Paging	-12.04	-12
Traffic1	-10	-15.6	Traffic1 (CF=1 414)	-9.03	-15.6
Traffic2	-10	-15.6	Traffic2 (CF=1 414)	-9 03	-15.6
Traffic3	-10	-15.6	Traffic3 (CF=1 414)	-9.03	-15.6
Traffic4	-10	-15.6	Traffic4 (CF=1 414)	-9.03	-15.6
Traffic5	-10	-15.6	Traffic5 (CF=1.414)	-9.03	-15.6
Traffic6	-10	-15.6	Traffic6 (CF=1.414)	-9.03	-15.6
OCNS	-10	-2.62	OCNS	-12.04	-2.62
CE of different signals & components	CE (dD)		CF of different signals & components	CF (dB)	
Disgonal signals & components			Diagonal signals	0	
Diagonal signals	0		Axial signals	3	
Noise signal. v_N	10		Noise signal, v_N	10	100000000000000000000000000000000000000
Noise signal after F2. v_{NP2}	13.71		Noise signal after F2. v_{NF2}	13.71	
Filter F1 Expansion Factor	6.97		Filter Fl	6.97	
Filter F2 Expansion Factor	3.71		Filter F2	3.71	
Convolved Filter F12 Expansion Factor	7.22		Convolved Filter F12	7.22	-
Location of determined CF	CF(dB)	CF(dB)	Location of determined CF	CF(dB)	CF(dB)
Sum of signals r	10	8 27	Sum of signals. Va	9.61	8.89
Output of Filter FL y	16.97	15.25	Output of Filter F1. y_{F1}	16.58	1586
	17.33	15.5	Output of Filter F2, y _{F2} , w/o noise	16.83	1611
Output of Filter F2, v_{F2} , wo holse	14.22	15.5	σ.,	17.44	16.25
Sum of signal & noise, v_s with $\frac{\sigma_N}{\sigma_N}$ as shown	17.76	15.86	Sum of signal & noise, v_s with $\frac{N}{\sigma_{F1}}$ as shown	$\frac{\sigma_N}{2} = 6.58 dB$	$\frac{\sigma_N}{m} = +1dB$
σ_{p_1}	$\frac{dW}{\sigma_m} = -6.97 dB$	$\frac{-M}{\sigma_{m}} = \pm 1dB$	Output of Filter F2 an and using	1955	1707
Output of Filter F2 v. w poise	18.82	17.6	Compared Filter F2, v_{F2} , we noise	10 Gum	17.92 Gum
compared a rate of 2, 5p2, we note	$\frac{\sigma_{NF2}}{\sigma_{nF12}} = -351 dB$	$\frac{\sigma_{MP2}}{\sigma_{mP2}} = +1dB$		$\frac{\lambda \sigma_1}{\sigma_{aF12}} = -3.12 dB$	σ _{en1} +1dB

Table 1. Crest factor at points within the topology.

$$B_{*} = \frac{\sum_{i} h_{i}^{2}}{\left(\sum_{i} h_{i}\right)^{2}}$$

However, the crest factor expansion factor uses the sum of the absolute values of the filter's coefficients, where the noise bandwidth uses the sum of the filter's coefficients. Hence, the crest factor expansion factor is always greater than the reciprocal noise bandwidth factor.

Interpolation filters

The effects on crest factor by interpolation filters may be analyzed as follows: Start with a general form for an interpolating filter and transform it into a polyphase representation (see Figure 4). Then apply the previously developed crest factor analysis to the resulting filter topology. Given:

$$H(z) = \sum_{j=0}^{DE-1} h_j z^{-j}$$

H(z) has (DE) coefficients (may have to zero the pad to get an integer multiple of D). This interpolation filter can be transformed into a polyphase representation as shown in Figure 5.

Each branch of the polyphase filter uses coefficients from the original filter in the following manner, e.g., the d^{th} filter:

$$H_{d}(z) = \sum_{i=0}^{E-1} h_{d,i} z^{-i} = \sum_{i=0}^{E-1} h_{iD+d} z^{-i}$$
for $d = 0$ to $D - 1$

The input sequence y(k) has the same characteristics as the previous analysis. To determine the crest factor, the peak value is the maximum absolute value from among the branch filter outputs. The peak value is found by examining each path's filter: Peak_d = peak value of branch d. The maximum possible output value squared is then given by:

$$\max_{d} \left[\left(Peak_{d} \right)^{\theta} \right] = \max_{d} \left[\left(\sum_{i=0}^{d-1} |h_{d,i}| \right)^{2} \right] \max |y|^{2}$$

And, the average output power (or variance) is the average of the branch filter outputs given by:

$$\sigma_{j}^{2} = \frac{1}{D} \left[\sum_{i=0}^{\frac{D}{2}-1} h_{0}^{2} \cdot i + \sum_{i=0}^{\frac{D}{2}-1} h_{1}^{2} \cdot i + \dots \sum_{i=0}^{\frac{D}{2}-1} h_{D-1}^{2} \cdot i \right] \sigma_{j}^{2} = \frac{\sigma_{j}^{2}}{D} \sum_{i=0}^{\frac{D}{2}-1} h_{i}^{2}$$

Therefore, the crest factor is:

$$C_{f}^{2} = C_{y}^{2} \frac{\max_{d} \left[(Peak_{d})^{2} \right]}{\sigma_{f}^{2}}$$
$$= C_{y}^{2} D \frac{\max_{d} \left[\left(\sum_{i=0}^{k-1} h_{d,i} \right)^{2} \right]}{\sum_{i=0}^{Dk-1} h_{i}^{2}}$$

The denominator is the summation of the coefficients squared of the filter H(z). The numerator will depend on

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110	MAX3381E	+2.35 to +5.5	2/2	±15	±15	+1.8V, +2.5V, +3.3V, +5.0V	250k	Yes, Vcc > 3.1V	1μΑ	Yes
	MAX3237E	+3.0 to +5.5	5/3	±15	±15	+3.0V or +5.5V	1M	Yes	10nA	
	MAX3238E	+3.0 to +5.5	5/3	±15	±15	+3.0V or +5.5V	250k	Yes	10nA	Yes
	MAX3248E	+3.0 to +5.5	5/3	±15	±15	+1.8V, +2.5V, +3.3V, +5.0V	250k	Yes	10nA	Yes

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INFO/CARD 55



Figure 7. Special case 1: the diagonally aligned IQ constellation.

how the polyphase filters' coefficient magnitudes sum together.

An example system

This example is based on the IS-2000 standard. It allows the summing of two sets of inputs, diagonally and axially aligned IS-2000 signals with different crest factors. The diagonal signals are so called because the complex I and Q signals result in a constellation at diagonal points in the IQ plane. This is illustrated below as special case 1.

Special case 2 illustrates the axial signals. The axial signals result in a four-point constellation on the I and Q axes of the IQ plane. The I and Q components are not independent from one other, but each (I or Q) comprises independent streams of data.

The summed IS-2000 signals are filtered with the IS-2000 baseband interpolating filter. This output is summed with an AWGN signal with a subsequent filter that sets the noise bandwidth and further interpolates the signal. This system is used to produce the forward modulation signals for testing IS-2000 mobile phones. Figure 6 presents only one-half of the baseband modulation signal (I or Q) because each half is processed separately and identically.

Filter F1 $(H(z)4^{\uparrow})$ (see Figure 6) is patterned after the one specified in IS-2000, which sets the bandwidth of the IS-2000 forward channel signals and interpolates the data by a factor of four. Filter F2 $(G(z)8^{\uparrow})$ (see Figure 6) is used to set the bandwidth of the AWGN signal and interpolates the data by a factor of eight. This simplifies the reconstruction filter following the DACs that convert the digital



Figure 8. Special case 2: the axially aligned IQ constellation.

baseband I and Q signals to analog format.

The noise signal employed is a truncated Gaussian amplitude distribution and i.i.d. with a crest factor of about 10 dB. Although this may appear low for a noise approximation, the effective crest factor of the noise is increased by the filtering applied. The mobile unit's own receiver processing further increases the effective noise crest factor. All this allows for a noise source with a relatively low initial crest factor.

I and Q alignment - special cases

The IS-2000 signals have two alignments for the I & Q signals, and they have different crest factors.

• Special case 1: the diagonally aligned IQ constellation (see Figure 7).

From this, it can be seen that the I (or Q) signal has the following characteristics:

$$\delta = 8 = \frac{+1}{-1}$$

and equally probable, thus max

 $(\delta) = 1, \sigma_{\delta}^2 = 1, \sigma_{\delta} = 1 \Rightarrow C_{\delta} = 1, i = 1 \text{ to } J$

Also, the I and Q channels are independent (uncorrelated).

• Special case 2: The axially aligned constellation (see Figure 8).

Here, the I or Q components have the following characteristics:

$$\infty = \begin{cases} +1, pdf = 0.25 \\ 0, pdf = 0.5 \\ -1, pdf = 0.25 \end{cases}$$

Then,

$$\max_{\alpha} ||a|| = 1$$

$$\sigma_{\alpha}^{2} = \sum_{n=1}^{\infty} \alpha^{2} p(\alpha)$$

$$\sigma_{\alpha}^{2} = \frac{1}{4} (-1)^{2} + \frac{1}{2} (0)^{2} + \frac{1}{4} (+1)^{2} = \frac{1}{2}$$

$$C_{\alpha}^{2} = \frac{\left[\max_{\alpha} |\alpha|\right]^{2}}{\sigma_{\alpha}^{2}} = \frac{1}{\frac{1}{2}} = 2$$

$$C_{\alpha}^{2} = 2 \cdot C_{\delta}^{\pm}$$

The I and Q constituents for axial signals have a 3 dB higher crest factor than that for diagonal signals.

Unfortunately, the I and Q channels are not mutually independent. Whenever the I channel is non-zero, the Q channel is zero and vice-versa. This is only a consideration when the crest factor of the RF envelope signal is considered later.

The crest factor of the signal as it progresses through the stages of the modulation path can be determined by examining the various signals separately and then combining them using the analysis technique previously developed. Figure 9 models the signal flow that is under examination.

The solution steps

From the definition of crest factor, peak_x = $C_x \sigma_x$, then:

$$C_{\alpha}^{2} = \frac{\left(\sum_{i=1}^{J} |C_{4}\sigma_{6}| + \sum_{i=1}^{K} |C_{\alpha}\sigma_{\alpha}|\right)^{2}}{\sum_{i=1}^{J} \sigma_{6}^{2} + \sum_{i=1}^{K} \sigma_{\alpha}^{2}} = \frac{\left(C_{\delta}\sum_{i=1}^{J} \sigma_{6} + C_{\alpha}\sum_{i=1}^{K} \sigma_{6}\right)^{2}}{\sum_{i=1}^{J} \sigma_{6}^{2} + \sum_{i=1}^{K} \sigma_{\alpha}^{2}}$$

Solve for crest factor at output of H(z)

$$C_{F_1}^{2} = C_a^{2} D \frac{\max_{d} \left(\sum_{i=0}^{E-1} |h_{d,i}| \right)^{2}}{\sum_{i=0}^{DE-1} h_{i}^{2}}, D = 4$$

Solve for crest factor at input of G(z)

$$C_{s}^{2} = \frac{(C_{r_{1}}\sigma_{r_{1}} + C_{v}\sigma_{v})^{2}}{\sigma_{r_{1}}^{2} + \sigma_{v}^{2}}$$

Solve for crest factor at output of G(z)

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Figure 9. Crest signal modulation path flow.

$$C_{r_1}^{**} = \frac{(C_{w'12}\sigma_{w'12} + C_{vr_2}\sigma_{vr_2})^2}{\sigma_{vr_1}^{**} + \sigma_{vr_2}^{**}}$$

Because the output of H(z) is no longer uncorrelated data, it cannot be used as the input to G(z) with the technique previously presented here. The model of the circuit must be changed to combine the two filters for the IS-2000 signals before summing with the noise after it has been filtered with G(z). Using the noble identities, the following transformation can be made to shift H(z) to the right of the 8x upsampler. Then G(z) is convolved with $H(z^8)$. This allows computing the crest factor of the IS-2000 signals at the output of G(z), (y_{aF12}) . After the noise signal is passed through, G(z) is available to add to the IS-2000 signal for the final crest factor calculation (see Figure 10).

Example systems' crest factors

Table 1 illustrates what crest factors are encountered at various points in the topology for some different signal gain settings and signal types. First, the conditions for all diagonal signals are examined with the worst-case situation, then a typical setup is used in IS-95 (cdmaOne) testing. Second, the condition where some of the signals are axially aligned is examined, again with the worst-case situation. Then a typical setup is used in IS-2000 testing.

All diagonal and typical IS-95

The levels used for the worst-case situation satisfy the maximum crest factor criteria at the point the signals are summed together. This is shown by the different ratios

σ

σ

used in the two locations where the noise and signal are summed together, namely before and after Filter F2. The typical setup uses the same ratio, +1 dB, as is specified for several IS-98 tests.

Diagonal, axial and typical IS-2000

Note the levels used for the worstcase situation. They are adjusted to meet the max crest factor criteria; the ratio of levels equals the ratio of crest factors. Note also that the worst-case diagonally aligned signals have a larger crest factor than the worst case with six axially aligned among the 10 signals. However, the IS-2000 typical case with the axially aligned traffic signals has a slightly larger crest factor than the IS-95 situation with the diagonally aligned traffic signals.

Complex summation, translation to RF

The crest factor of the baseband signals has been examined, so it is necessary to discuss the crest factor of the modulated RF signal. The RF signal is modulated by using an IQ modulator, where the baseband signals are applied to the I & Q inputs. To more easily examine this process, an equivalent model using complex representation is used.

Referring to Figure 11:

$$S(t) = I(t) + jQ(t)$$

$$Y(t) = S(t)e^{j(mt+0)}$$

$$W(t) = \operatorname{Re}\left[S(t)e^{j(mt+0)}\right]$$

First, find the average values:

$$E \{S(t)\}^{2} = E \{S(t)S'(t)\}$$
$$= E \{I^{2}(t) + Q^{2}(t)\} = \sigma_{1}^{2} + \sigma_{2}^{2} = 2\sigma^{2}$$

Note that the rotation by the complex exponential does not change the mean square value:

$$E_{q}[W(t)]^{2} = E\left\{\left(\frac{(Y)(t) + Y'(t)}{2}\right)^{2}\right\}$$
$$= \frac{1}{4}E_{q}[Y(t)]^{2} + (Y'(t))^{2} + 2Y(t)Y'(t)] \rightarrow$$
$$E_{q}[Y(t)]^{2} = 2E_{q}[e^{j(0(t+3))}]E_{q}[S(t)]^{2}] = 0$$

Similarly,

$$E \{(Y'(t))^2\} = 0$$

Therefore,

$$\mathbf{E} \mathbf{\Psi}(t)^{2} \mathbf{y} = \frac{1}{2} \mathbf{E} \{ \mathbf{Y}(t) \mathbf{Y}^{*}(t) \}$$
$$= \frac{1}{2} \mathbf{E} \{ \mathbf{Y}(t) \}^{2} \mathbf{y} = \frac{2\sigma^{2}}{2} = \sigma^{2}$$

Now find the peak value:

$$\max\left[\left(W(t)\right)^{2}\right] = \max\left[\left(\operatorname{Re}\left(Y(T)\right)\right)^{2}\right]$$
$$= \max\left[\operatorname{Re}\left(S(t)e^{j(t(t+0))}\right)^{2}\right]$$

But the complex exponential has magnitude 1 and simply rotates the complex signal S(t) at frequency ω_c . So the maximum instantaneous squared value of the output occurs when the maximum magnitude amplitude of the signal occurs and the complex exponential has simultaneously rotated it to be along the real axis. This yields:

$$\max\left[\left(W(t)\right)^{2}\right] = \max\left[\left|S(t)\right|^{2}\right]$$
$$= \max\left[I^{2}(t) + Q^{2}(t)\right]$$

If I(t) and Q(t) are independent:

$$\max \left[I^{2}(t) + Q^{2}(t) \right] = \max \left[I^{2}(t) \right]$$
$$+ \max \left[Q^{2}(t) \right]$$
$$C_{t}^{2} = \frac{\max \left[I^{2}(t) \right]}{\sigma}$$

Therefore:

$$\max\left[I^{2}(t)\right] = C_{i}^{2}\sigma^{3}$$

and:

$$\max\left[Q^{2}\left(t\right)\right]=C_{Q}^{2}\sigma^{2}$$

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Figure 10. Crest signal modulation path flow: G(z) convolved with $H(z^{e})$.

Peak crest factor

Next the peak crest factor for the RF signal, W(t), is addressed:

Peak
$$C_{v}^{2} = \frac{\max[(W(t))^{2}]}{E_{q}(W(t))^{2}}$$

= $\frac{C_{v}^{2}\sigma^{2} + C_{q}^{2}\sigma^{2}}{\sigma^{2}} = 2C_{v}^{2}$ (since $C_{v}^{2} = C_{q}^{2}$

This is the ratio of the instantaneous peak voltage squared to the average output power, but for translated signals (IF or RF) it is customary to consider the crest factor for the envelope signal. Because most RF devices are characterized with sinusoidal signals at either specified or measured power levels, having the crest factor as a function of a sinusoidal signal's power level is more appropriate.

Envelope crest factor

To determine the envelope crest factor, first determine the power of a sinusoidal signal that has the same peak voltage as the modulated signal's peak voltage. This value is then divided by the average power of the modulated signal. The result is defined as the translated signal's envelope crest factor. (Envelope C_w equals the power of the sinewave with the peak value of the modulated signal divided by the average power of the modulated signal.), or:

$$C_{w^{2}} = \frac{\left(\frac{\max(|W|)}{\sqrt{2}}\right)^{2}}{\sigma_{w^{2}}}$$
$$= \frac{\frac{1}{2}\max(|W|^{2})}{\sigma_{w^{2}}} = \frac{1}{2}(2C_{v}^{2}) = C_{v}^{2}$$

Thus, the envelope crest factor of the RF signal is the same as the crest factor of the baseband quadrature components when the I and Q channels are uncorrelated.

Continued on page 54



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Correlated signals

What happens when the signals are correlated? Consider when I and Q are the same — perfectly correlated. Repeating the analysis yields the same result. The envelope crest factor is the same as the crest factor of I(t) (and Q(t)). In general, it is asserted that the envelope crest factor is never greater than the crest factor of the individual I and Q components. However, there are signals with an envelope crest factors.

A prime example of this is the axially aligned signal. Recall that the I and Q components have a crest factor of $\sqrt{2}$ (or 3 dB). However, this signal is just a 45° rotation of the diagonally aligned signal that has a crest factor of 1. By inspection, the envelope crest factor of this signal is 1, while its I and Q crest factors are $\sqrt{2}$. Hence, the envelope crest factor is 3 dB lower than that of the I (or Q) crest factor. This occurs because, when the I channel has a non-zero value, the Q channel value is zero and vice-versa. While it has not been



Figure 11. Complex summation and translation to RF.

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NGA-486	DC-8.0	17.5	39.5	14.5	4.5	4.2, 80	118
NGA-586	DC-6.0	19	38	19	4.5	5.0, 80	121
NGA-686	DC-4.0	19.2	35	11	6.1	5.9, 80	121



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proven, it is believed that these cases set the extremes, i.e., the envelope crest factor is never greater, nor 3 dB less, than the I (and Q) channel's crest factor.

Conclusion

It has been shown how to determine the worst-case crest factor for a signal formed by summing multiple independent and uncorrelated signals with arbitrary crest factors and gains. This is useful in determining the dynamic range necessary at any point in the digital signal processing data path.

The examination has included how to deal with digital filtering and interpolation along with crest factor and gain effects. The examples that were given show how the crest factor for a

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About the author

Brad Andersen is a development engineer in the product development department at Agilent Technologies in Liberty Lake, WA. He has been involved in analog and digital circuit design for the past 17 years, primarily for test equipment for cellular phones. Prior to working at Agilent, he worked at Bell Laboratories in Whippany, NJ. He received an MSEE at Washington State University in 1978. He can be contacted by telephone at 509.921.3570, or at Agilent Technologies 24001 E. Mission Ave. Liberty Lake, WA 99019-9599



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Securing wireless communications

Cryptography – today's hot topic for wireless network users.

By Paul Lesso, PhD

As wireless devices pervade deeper into our lives, it becomes increasingly important to maintain security. For example, the wired equivalent privacy protocol (WEP) used with 802.11b (the IEEE standard for wireless LANs) was recently shown to be easily broken. Such a security breach is a wake-up call to the wireless industry to implement effective secret communications. Cryptography is an ideal candidate.

Cryptography - past, present and future

Cryptography can be used in either software or hardware, but as bandwidth increases and the need for embedded encryption develops, hardware-based cryptography is preferred.

Cryptography, in Greek, literally means "hidden writing," or the art of changing plain text (the



Can wireless communications be secure? The key is cryptography.

message) into cipher text (an unreadable message). Cryptography has a long and ancient history, starting in ancient Roman times. One of the earliest ciphers used was the so-called Caesar code, which simply replaced a letter in the alphabet with another letter, shifting a set number of letters along the alphabet. For this code, an A becomes a D, a B becomes an E and so on. For shifted code, the alphabet reads as follows:

Plain text: A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

shifted text: D E F G H I J K L M N O P Q R S T U V W X Y Z A B C

The basic crypto tools

While modern cryptography is a vast and complicated field, the basics of are easy to understand. Cryptography includes four commonly used tools: a cipher, a key exchange mechanism, a hashing core and a random-number generator.

• Cipher

Ciphers are what most people think of when they hear the word cryptography. Given a known key, a cipher can either encrypt (turn plain text into cipher text) or decrypt (turn cipher text into plain text). The security of the system lies in the key being kept secret — only someone with the key can decode the message. Because the same key is used to encrypt and decrypt, this form of encryption is known as symmetric encryption.

Ciphers come in two types: block and stream. Block ciphers operate on a block of plain text to produce a block of cipher text, whereas stream ciphers produce an output that is logically exclusive-ored with the plain text to produce cipher text. Most modern cryptography is based around block ciphers for two reasons: more analysis into the design of block ciphers has been carried out, and block ciphers can be modified for use as a stream cipher if needed.

Key exchange mechanism

To use the ciphers described above, the people sending the messages must agree on the key to be used with the cipher. However, if the people wishing to communicate have no secure lines to send the keys over, it is a seemingly impossible task to use cryptography securely. This was an insurmountable problem in cryptography for a long time. The problem was first overcome via the Diffie-Hellman algorithm, which allowed users to exchange keys over an insecure line using modular exponentiation¹. An example Diffie-Hellman key is shown in Table 1.

Users agree on a generator, g, and a modulus n (which can be made public).

An eavesdropper can intercept I_a and I_b , but to calculate the key K from these two numbers represents a substantial computational task.

The Diffie-Hellman algorithm was a major step

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Block diagram of typical encryption flow.

forward for cryptography; it had not been possible to agree on a key over insecure lines without an eavesdropper being able to determine the key. However, this key exchange had to be performed for every two users on the net.

Stepping up the food chain

The next major step was the development of the RSA algorithm from RSA Security. For this algorithm, each user had a public and a private key. The public and private keys were mathematically related and a message enciphered using a public key could only be deciphered using the associated private key. The security of the system relied on the private key being kept secret so the public key could be freely distributed.

Public key cryptography is also known as asymmetric encryption because one key is used to encrypt the data and another is used to decrypt the data. Most real cryptography systems are hybrid systems, i.e. they use both symmetric and asymmetric encryption. Asymmetric encryption is used to exchange the key used for asymmetric encryption, and the bulk of the data is sent using symmetric encryption algorithms. This is because symmetric algorithms (such as defense encryption standards (DES)) are much faster than asymmetric algorithms (such as RSA).

Hashing – the digital fingerprint

A hash is a one-way function that can be used to create a digital "fingerprint" of data. This fingerprint is a number that is similar to a checksum for the data. If the file is modified in any way, then the hash value will also change.

Commonly used hash functions include SHA-1, which creates a 160bit hash of a message of any size. These functions are used to create a checksum that can be recalculated later to ensure that the data have not been modified. If the file has been modified, then the calculated hash will be different. In cryptography, hash functions are used (as detailed below) for authentication.

Random number generator

Random numbers are used in cryptography for the keys used to encrypt data. If it is possible to guess the random numbers being used, then it is possible to guess at the keys being used for encryption. Creating truly random numbers is an incredibly difficult task. Due to the difficult nature of generating random numbers, a pseudo-random number generator (PRNG) is used. The PRNG generates a series of numbers that should be indistinguishable from a sequence of random numbers.

Several techniques are used to generate random numbers. They range from the simple linear feedback shift registers (LFSR), which are a series of flip-flops and XOR gates, to the complex Blum-Blum-Shub PRNG, which uses prime numbers and modular arithmetic. Most PRNGs use an initial seed, which should come from a physical source, such as hard-drive latency or PLL jitter.

Example cryptographic transaction

When a message is sent, there are two objectives. First, it is important to ensure the message can only be read by the intended recipient. It is also important to ensure that the message has not been altered in any way.

For example, user A can send a message to user B by encrypting the message using user B's public key. Only user B can decrypt this message even if other users receive it. However, user A also wants to ensure that the message is not modified en-route. Authentication allows user B to be certain that user A sent the message and that is has not been modified. To authenticate the message, user A must hash his plain text message and then encrypt this hash using his private key. This seemingly illogical step allows user B to verify that user A did send the message. If user B can decrypt the hash using user A's public key, then it was encrypted using user A's private key, which only he has.

User A then sends his privately encrypted hash and publicly encrypted message to user B. On receipt, user B can then decrypt the message using his private key and regenerate the message hash. They can also decrypt the encrypted hash using user A's public key, then compare the two hash values. This authenticates that user B sent the message and confirms the integrity of the message.

Cryptography and wireless

For wire-based networks, physical security was often adequate. A wire running from points A to B would be good

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User 1	User 2
Generate random # A	Generate random # B
Calculate $I_a = g^{\wedge} A \mod n$	Calculate $I_b = g^A B \mod n$
Transmit I _a	Transmit Ib
Calculate $K_a = I_b^{\wedge} A \mod n$	Calculate $K_a = I_b^{A} \mod n$
$(K = K_a = K_b = g^{(A*B) \mod n})$	

Table 1. How the Diffie-Hellman key works.

enough to defeat eavesdroppers, and cryptography would be added if it was felt that anybody else had access to that wire. However, for wireless applications where data are beamed, it is difficult to ensure that only the intended recipient receives the data. For many cases, it does not matter — if you are just playing a wireless game between two telephones, who cares if other people can intercept the data? However, if you are beaming sensitive documents or carrying out personal conversations, the situation is different - especially with the merging of 3G and e-commerce. Nobody would walk down the street handing out their credit card details to complete strangers. But, without cryptography, that is essentially what would happen within e-commerce and wireless networks. Thankfully, the situation is not that bad - many different cryptographic protocols are used in conjunction with wireless networks to preserve users' privacy.

WEP security analysis

A paper was recently published detailing an attack against the Wired Equivalent Privacy protocol². The protocol is part of the official 802.11b standard and is used to ensure that data can be sent securely at any speed. This protocol used the proprietary RC4 cipher developed by Ron Rivest (the R in RSA) in 1987. RC4 is a widely used stream cipher that consists of two parts: a key scheduling algorithm and a pseudo-random number generator. Due to its simplicity and perceived security, RC4 has become a popular cipher.

The paper by Flurhrer, Mantin and Shamir details two weaknesses in RC4: A series of weak keys in which a small part of the key affects a large number of bits in the output, and a flaw in the keyscheduling algorithm. For 802.11b, the key used was fixed, and there was an attack allowing a determined user to get access to the data using nothing more than a desktop computer with an 802.11 card. The attack exploited the fact that a fixed, secret key was used. The time to bypass the encryption grows linearly, rather than exponentially, with key size. While this attack is not the end for RC4-based protocols, it does raise awareness of security issues and the shortcomings of WEP. For some users, enough security to stop casual eavesdroppers is sufficient. However, for secure traffic, another cipher will have to be used.

This has led to this question: If RC4 can be easily broken, which ciphers currently cannot and will not be breakable for the foreseeable future? One answer comes from the National Institute of Standards and Technology (NIST), the federal standards body that was responsible for the Data Encryption Standard (DES), the most widely used cipher in the world.

DES vs. AES

Currently, the federal standard for encryption is DES. IBM originally designed DES in 1974. It was based on a cipher called LUCIFER, which was written by Horst Feistel, who designed the general cipher models around which DES is based. DES was designed to be implemented in hardware and does not have the strength needed by modern cryptography. Triple DES (TDES) was introduced to solve the problem of the small key size, but the implementation was still mainly suitable for hardware.

It is now 27 years later, and NIST has identified the requirement for a new cryptography algorithm to replace DES. Requests for algorithms were tendered and five algorithms made it to the last round. Of the finalists, a cipher developed by a European team called Rijndael was selected to become the new federal standard, known as the Advanced Encryption Standard (AES). Several of the requirements that this standard had to fulfill were:

• It has be suitable for implementation in software or hardware.

• It has to have provision for use with larger key sizes.

• It has be suitable for high bandwidth networks.

In keeping with most modern algorithms, the algorithm picked for AES So, why will DES (the current standard) be replaced by AES? The answer is not a simple one. There is a need for a faster algorithm with a larger key size, as DES can no longer be considered completely secure. In 1999, a \$250,000 machine made by the EFF managed to break DES encryption in less than four days. However, that machine would still take roughly 10³¹ years to exhaustively test each TDES key. To put those numbers into context, the age of the universe is estimated to be 10¹⁰ years, so that is a billion, billion, billion, billion, billion, billion, billion times longer than the ages of the universe. DES and hence, TDES have been heavily analyzed, and in more than 25 years, no flaws have been found in the design. This means the algorithm is well-respected and trusted. DES' only weakness comes from its small key size, not from any flaws in the algorithm.

If it isn't broken, why fix it?

The main reason to change to AES is the need for a faster, more secure algorithm that is equally suited to software and hardware implementation. As broadband networks take off, it can be estimated that a high-end hardware AES solution should be able to encrypt 25 Gb/s of data. Conversely, a small, low-power hardware AES solution should be able to encrypt data at 290 Mb/s. The cryptographic community has extensively examined the AES algorithm, and no flaws have been discovered in the algorithm. However, the algorithm has only been analyzed for more than a year and has not received the large amount of cryptographic analysis and trust that DES has.

AES has yet to be fully ratified by NIST, but this should happen in the next few months. The draft specification documents are available, and it



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is unlikely that there will be any major modification to the algorithm. The only obvious change in the future might introduce the use of keys of different length.

A final word

The cryptography for wireless networks should be adequate to prevent casual eavesdroppers from overhearing conversations and determined hackers from getting your bank details. The cryptography solution must be transparent to the end user. Users will not be satisfied by a cryptography solution that results in a dramatic drop in performance. AES is coming and should be fully ratified by NIST in the near future. As the "wireless revolution" continues, the demand for cryptography will continue to rise.

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About the author

Paul Lesso is a senior consulting engineer for Tality. He holds a PhD in physics from St. Andrews, Scotland University. His main areas of interest are cryptography, computer arithmetic and DSP. In 1999, Lesso was a joint winner of the National Physical Laboratory (NPL) international award for world-class metrology. He can be contacted at: *plesso@tality.com*.

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Integration designthe heat is on for systems on a chip

A design methodology for efficient implementation of complex DSP algorithms in FPGAs

By Johannes Steensma

eature-rich, application-pervasive modern electronics increasingly require some form of digital signal processing. Today, mobile phones, hearing aids, Internet telephones, medical imaging systems, voice-activated appliances and toys, televisions, video recording and audio systems are heavily DSP-based.

Simultaneously, the heat is on to make these systems ever smaller, frequently integrating the entire system functionality on a single piece of silicon, or system-on-a-chip (SoC). After all, nobody wants a hearing aid the size of a Palm Pilot.



Figure 1. Method for optimizing RAM and ROM in memory.

Let's talk digital signal processing

DSPs take analog data, convert it to a digital format, process it, filter it, packetize it and/or transmit it, and then turn it back into an analog format for human consumption. They do so by using complex algorithms. Moving these complex DSP algorithms into SoC requires new design methodologies that are just beginning to emerge.

Most SoCs are implemented in custom applica-

tion-specific integrated circuits (ASICs). However, with the advent of large system-level field-programmable gate arrays (FPGAs), SoC designs are also making their way into FPGAs. Putting a system on an ASIC is a challenging proposition. Putting one on an FPGA is more challenging because of the structure of FPGA architectures.

Form factors and functions

A design optimized for an FPGA is generally different from that which would be used in an ASIC. This is because the two types of devices are structured differently. In contrast to gate arrays that have a single gate as the basic logic unit, FPGAs have the equivalent of 20 to 40 ASIC gates per logic unit, each typically containing a four-input look-up table (LUT), carry logic, muxes and a flip-flop (register). Newer FPGA architectures also have blocks of random access memory (RAM) distributed throughout the array or located on the periphery of the device. Although FPGA logic units can be used to implement memory, doing so is usually siliconinefficient and expensive. As a result, it is important to achieve the most efficient use of the on-FPGA memory. Sadly, most FPGA design and logic synthesis tools provide little or no support for the embedded static RAM (SRAM) blocks. Until now, they have had to be designed-in manually, taking a lot of extra time and effort.

From algorithm to RT level

Virtually all DSP-based system designs are developed purely as software in some variation of the C-language, using floating-point math and commercially available design tools. These programs are initially developed, executed and debugged using fast PCs or DSP processors. However, DSP processors are large, expensive and power-consuming. Eventually, these designs must be implemented in hardware, frequently with the objective of shrinking them into a single high-performance IC that consumes as little power as possible.

Unfortunately, while software is written in C, hardware designs are written in hardware description languages such as Verilog and VHDL. Historically, the design methodology for implementing a C-language DSP algorithm in hardware has been to manually re-render the algorithm in a fixed-point format and then manually rewrite it again in a register-transfer (RT) level hardware description language. This is a daunting task that can take weeks or months. What's more, because the architecture of the hardware design is explicit in any RT-level description, this methodology does not allow the designer to explore alternative hardware architectures to ensure that the hardware design is optimal for the particular application (e.g. low-power, high-performance).

When FPGAs are the silicon medium, the design challenge becomes greater because the logic structures are fixed and the available on-chip memory is limited.

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F 232 Rev D

Enter architectural synthesis

A new class of EDA tools has been introduced in the past year that helps designers define hardware architectures for FPGAs and ASICs from SystemC or the American National Standards Institute- (ANSI) C software. Such software provides the designer with complete control of the process and can specify which resources will be used to execute the DSP programs. These can include arithmetic logic units (ALUs), multipliers, adders, RAM, ROM, registers and special custom resources that execute entire algorithms (e.g. fast-Fourier FFT or discrete cosine transforms – DCT) in a single clock cycle. When the optimum architecture is found, the tool automatically generates the RT-level Verilog or



INFO/CARD 69

VHDL. However, the original design remains in the C-language so it may be re-used and its hardware architecture re-optimized for other applications.

For example, a high-performance hardware architecture can be created from a C-language Viterbi algorithm for a high-speed satellite application. Then, without any modification, the same C-language Viterbi algorithm can be re-rendered in a low-power architecture for a mobile phone. The C-language algorithm never changes; only the hardware architecture does.

A technique called dataflow analysis is used during architectural synthesis to automatically identify and exploit data dependencies in the code. Operations are assigned to the datapath resources to maximize parallelism in the hardware design. The architectural synthesis tool then generates a hardware architecture that includes a very long instruction word (VLIW) controller and datapath resources, and schedules the algorithmic operations on the hardware resources. The designer may modify the architecture, scheduling or resource allocation at will. Once the designer is satisfied, the tool automatically generates the RT-level Verilog or VHDL hardware description.

In contrast to HDL-based designs, which can take weeks or months for a single iteration, C-language-based design can be iterated in as little as a few minutes using architectural synthesis. Because design iterations are so fast, designers have the freedom to explore and analyze many architectures to achieve an optimized design.

Putting DSP algorithms in FPGAs

DSP algorithms have several characteristics that affect their implementation in hardware, and especially in FPGAs. First, they are computationally intensive and require lots of registers. Second, they tend to use non-standard word widths (e.g. 13 or 33 bits) that frequently do not fit in the fixed memory architectures of on-FPGA SRAM (e.g. 8, 16, 32 bits). Third, because they must perform repetitive calculations on samples or frames in real-time, they demand high processing throughput. If the processing of the first sample or frame is not completed in time, the next one will be lost. Finally, DSP algorithms must often store the results of one frame or sample for comparison to the next frame or sample. Because

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FPGAs have limited memory, these storage requirements can force the use of external, and slower, off-chip memory. As a result, on-FPGA memory is at a premium and needs to be conserved whenever possible. These characteristics mandate special design techniques and tools for FPGA implementations.

The nature of DSPs

The computationally intensive nature of DSP algorithms means they rely heavily on the use of registers to store intermediate values. In fact, every datapath resource (ALU, multiplier) in a DSP-like architecture is likely to have at least one register file associated with it. Implementing a one-bit register in a gate array takes about eight or nine gates. PGAs, however, have pre-defined flip-flops included in their high-level logic units. Many devices have one flip-flop per logic cell (LC) or logic element (LE). Registers that are larger than one-bit can be built by chaining together several logic units.

If the registers are specified in the HDL description as registers, the logic

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synthesis tool will synthesize them directly into the registers in the logic units on the FPGA. For example, a 16 x 16 multiplication will need two 16bit registers to store the left and the right operands. Each 16-bit register can be created by chaining together 16 LCs or LEs and using the flip-flop in each logic unit to store one bit of the 16-bit words. This solution requires 32 logic units to store the multiplication. However, this can be an expensive solution because, in most cases the logic resources are no longer available for logic operations. In other words, using logic elements just for their register can waste valuable logic resources.

A more efficient means of implementing the 16-bit registers is to use a single LUT for each one. Because each LUT can be configured as a 16-bit RAM, a single LUT can be used to store each 16bit operand. Depending on the software, it can evaluate the number and size of the required registers in the design and optimizes their implementation between built-in and LUT RAM registers. In this example, the software reduces the number of LUTs required for the two 16-bit registers from 32 logic units to only two logic units – a 93% improvement.

Implementing the register in this way can waste all the other resources in the logic element (e.g. the LUT, carry logic and muxes). Because an FPGA logic element contains the equivalent of between 25 and 40 gates, at least 15 equivalent gates of logic resources can be wasted if the registers in the FPGA logic units are used to implement registers in the design. Again, depending on the software, this use of LUT RAM for registers, when appropriate, can be automated.

For the utmost in efficient design, the latest generation of software has tools that look at all the register files in the hardware architecture and optimizes their implementation in the LUT RAMs and/or logic unit registers. For example, A | RT's 3GPP turbocoder IP core in has 1,504 one-bit registers. If these one-bit registers were specified as such in the HDL description of the design, it would require 94 VitrexII slices just for the implementation of the

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registers, plus about 4,700 additional slices to implement the datapath logic and microcode ROM. The coder requires only 3,071 slices and 16 block RAMS in an XCV400E.

Non-standard word widths

DSP algorithms are typically developed using floating-point math because it is infinitely accurate. However, when the algorithms are implemented in hardware, they are converted to a fixed-point representation to conserve silicon. Because every bit in every word takes up silicon, the fixed-point words are kept as small as possible.

The words must also be wide enough, with enough precision to achieve the behavior of the floatingpoint algorithm within the specified dynamic range and signal-to-noise ratio. The smallest possible fixed-point word width that has enough bits to provide an accurate result may not be a standard eight, 16 or 32 bits wide. The fixed-point words could be any width, 23, 17, or 51 bits. Depending on what is required at any point in the execution of the algorithm, the word width may change within the same algorithm. Using a non-standard word width to perform the arithmetic will result in a variable value that must be stored in a non-standard word width.

Storing variables with unusual word-widths is not a problem in an ASIC because the designer has complete flexibility to configure the silicon any way he likes. In an FPGA, however, the on-chip memory is configured in fixed standard widths of one, two, four, eight, 16, or, in some cases, 32 bits, that are implemented in discrete blocks of 4096 bits or 2048 bits, depending on the software. Storing words that do not fall within these standard architectures can result in a less-than-optimal use of the FPGA memory. In fact, it can be wasteful.

Example A

Suppose a designer specifies a 33-bitwide word in the HDL description. Because the widest possible word in either a particular FPGA is only 32 bits wide, a 33-bit word won't fit in a single ESB or Block RAM. The default solution would use two 32-bit wide SRAM blocks, with the first 32 bits of each word stored in the first RAM block, and the 33rd bit of each word stored in the other RAM block. For every 33-bit word that is stored that way, 31 bits of memory are wasted — an expensive proposition.

A more efficient option is to use a combination of LUT RAM and Block RAM or ESBs to store the words. Because FPGA LUTs can be configured as SRAM with 16 one-bit words each, a LUT RAM can be used to store the 33rd bit of each word.

Although designers can and do configure FPGA memory manually to achieve a better result, the process can be time-consuming — and the result can be less than perfect. Again, software that automates the process by searching the code for the various words to be stored, and computing an optimized combination of LUT RAM and larger RAM blocks to minimize the amount of memory used offers the most efficiency.

Continued on page 76

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Example B

In this example, the tool would configure the memory to store the first 32 bits of the 33-bit word in a 32-bit wide block of RAM and store the 33rd bit in a LUT RAM. In this case, such software would reduce the required amount of RAM by nearly 50% from the worst-case implementation. This feature is particularly important in algorithms that must store massive amounts of data, such as adaptive differential pulse code modulation (ADPCM) or speech recognition.

Repetitive calculations

DSP designs are packed with multiple algorithms, such as FFTs butterflies or DCTs, that must be executed thousands of times a second. Parallelizing these operations is mandatory to achieve the required throughput in any implementation. With a maximum realistic clock of 80 MHz, FPGAs are much slower than 200 MHz ASICs or 400 MHz DSP processors and throughput becomes even more critical. A speech recognition algorithm that requires 90% of a 500 MHz Pentium III will require massive parallelization to execute in even the fastest FPGA.

Architectural synthesis allows designers to achieve the highest level of parallelism by letting them create special resources, based on complex Ccode algorithms or super instructions, (e.g. FFTs or DCTs), that execute in a single or a few clock cycles. For example, an FFT butterfly that requires two multiplications, an add and an accumulation would take at least four clock cycles to complete using conventional ALUs, multipliers and registers. By creating a special resource from a super instruction that includes the two multiplications, the addition and the accumulation, the butterfly FFT can be executed in a single cycle instead of four. Software is now available that automates the creation of these single-cycle, multiple-instruction resources at the designer's request. It then automatically searches the Ccode for any instance of the super instruction and instantiates the special resource to execute that code segment in just one clock cycle. Much larger super instructions can also be implemented in single-cycle special resources, using modern software.

Freeing up FPGA memory usage

The implementation of any algorithm in hardware requires that a controller and microcode be created to schedule the execution of the datapath operations on the hardware resources. The microcode can become long in complex designs, taking up a substantial amount of the FPGA's limited memory resources. At the same time, certain algorithms that must compare the value of the previous sample to the value of the current sample can require substantial amounts of memory to store the data. Because on-FPGA memory is limited, conserving memory can be paramount. If there is not sufficient onchip RAM, an external memory will be required that will degrade performance and increase board size, power consumption and system costs. Minimizing the storage requirement for the microcode can make the difference between a



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Fortunately, the LUT architecture of FPGAs can be exploited to reduce the total memory requirements for microcode storage. Frequently, there is enough overlap within the instructions that not all the bits are required to identify them. For example, in a design with 13-bit instructions, it may be possible to identify each unique instruction using just four of the bits. In this situation, the code can be stored as four-bit words and then decoded prior to execution using the FPGA LUTs. One LUT is used to decode each of the bits in the original instruction word.

The memory savings can be significant. In a complex design, the microcode can be as long as 5,000 lines. In the hypothetical example with the 13-bit instructions, 5,000 lines of code would require 65,000 bits of SRAM for storage. That is the equivalent 16 of the block RAMs in a Virtex, or 32 of the ESBs in an Altera APEX. By using LUTs to create small decoders, and storing the instructions in four bits of memory each, the required memory can be reduced to only 20,000 bits, plus 13 LUTs, a 70% reduction in the memory required for the code.

Conclusion

Implementing DSP software in hardware can be a daunting task. The predefined logic structures, fixed memory architecture, limited on-chip memory and slow throughput of FPGAs make this task even more difficult when an FPGA is the target medium.

Architectural synthesis tools can substantially improve the silicon efficiency of SoC implementations by automating and optimizing the configuration of register files and on-FPGA memory. These tools can also achieve high levels of throughput required of DSP applications by helping the designer introduce an extraordinary degree of parallelism in the hardware implementation - a critical requirement in slow FPGAs.

RF

About the author

Johannes Steensma is Adelante Technologies' vice president of engineering in the United States where he manages the development and deployment of complex DSP algorithms for 3G, VoIP, DVB, wireless LAN in high-performance, low-power intellectual property (IP) cores for ASIC and FPGA implementation. He received his MSEE degree from the University of Twente, The Netherlands, in 1989 and his Ph.D. (summa cum laude) in Applied Sciences from the Katholieke Universities in Leuven, Belgium, in 1994. He was a researcher at the Interuniversity Microelectronics Center (IMEC) from 1990 to 1994 where he worked on test techniques for high speed customized data path architectures. From 1995 to 1996, he served as a design consultant in the field of digital signal processing for the Center of Microelectronics (CME) in the Netherlands. Steensma co-founded Dedris Embedded Algorithms, which was acquired by Adelante Technologies in 1999. He can be reached at:

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RF TRANSFORMERS

CIRCULATORS, ISOLATORS COMBINERS AND SPLITTERS COUPLERS DOUBLE AND SINGLE BALANCED MIXERS LOW PASS FILTER, BAND PASS FILTER ANTENNA SWITCHES, DIPLEXER



Hitachi Metals America, Ltd. 2101 S. Arlington Heights Rd., Suite 116 Arlington Heights, IL 60005 Tel: (847) 364-7200 Fax: (847) 364-7279 www.hitachimetals.com

INFO/CARD 104

Software analyzes, simulates 3G mobile radio

Rohde and Schwarz offers a laptop version of an analysis and simulation software for third-generation mobile radio. The NetHawk product family can be used in development, production and installation of base stations. The systems supports a number of transmission techniques including GSM, GPRS, EDGE and UMTS. It comprises plug-in cards and software that can be installed on the customer's laptop or PC, which makes it suitable for stationary use in laboratories or production lines, as well as for mobile applications. If required, Rohde and Schwarz can enhance this measurement software for wireline transmissions with a suitable signal generator and spectrum analyzer for measurements on the air interface. A complete system for production and commissioning of base stations is available.

Rohde and Schwarz www.rohde-schwarz.com customersupport@rsd. rohde-schwarz.com

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- Specials our specialty virtually any SMA, N, TNC, BNC, SMB, or SMC delivered in 2-4 weeks
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- Our 56 Standard adapters can satisfy virtually any combination of requirements, between SMA, TNC, N, 7mm, BNC and others.
- Extensive inventory of passive RF/Microwave components including attenuators, terminations and dividers.



NEMAL ELECTRONICS INTERNATIONAL, INC.

12240 N.E. 14TH AVENUE NORTH MIAMI, FL 33161 TEL: 305-899-0900 • FAX: 305-895-8178 E-MAIL: INFO@NEMAL.COM URL: WWW.NEMAL.COM

Data acquisition tool for Windows-based PCs

Dasytec USA introduces DASYLab Version 6c. Improvements to the software include a data source synchronization with multiple time bases, worksheet documentation tools, support for more data acquisition devices, new function modules, enhanced features in many function modules, and expansion of the variable and string concept. A new test sequence manager provides an overview of multiple sequential tests, using variables to communicate program status and branching. The tool is good for discrete multistep tests, allowing the operator to automate the test sequence and operation based on actual test results and operator input.

Dasytec USA www.dasylab.net info@dasylab.net

Software aids in CAD management, sharing

Cyco Software announces a new version of AutoManager WorkFlow, which

Want to find out more?

For more information on all products noted in the product sections of *RF Design*, go to RF Design online for direct links. Look under the special sections listing on the left navigation bar.

will feature full support for AutoCAD 2002. AutoManager WorkFlow 6.3 will enable CAD professionals to manage and share their design data faster and more efficiently. CAD professionals are challenged to manage crucial design and engineering data from different sources and share that information across the engineering enterprise. With the integration of the complete AutoCAD 2002 suite, designers and other CAD professionals will continue to be able to easily view, manage, exchange and publish all their existing and new AutoCAD data in this new version. AutoManager WorkFlow 6.3 includes support for AutoCAD's new standards manager, associative dimensioning, block management tools, and laver tools.

Cyco Software www.cyco.com info@cyco.com

Package provides rich power supply testing environment

Chroma Systems Solutions introduces an enhanced version of its power test environment, the PowerPro III. This new software package is suitable for the production floor and offers the flexibility, customization and sophistication necessary for advanced design labs. With fast test speeds and userselectable analysis routines, The PowerPro III is suited for design verification, as well as high-volume incoming inspection, production test, burn-in, environmental stress screening (ESS) of power supplies, converters, VRMs, battery chargers, and power entry modules. PowerPro III is an openarchitecture test executive that encompasses tools necessary for power product testing. More than 50 standard tests are in the library, allowing fast and simple assembly of test programs. PowerPro III software can be modified by the user as necessary. Chroma has designed all routines, soft panels and functions to be compliant with National Instruments VISA drivers.

Chroma Systems Solutions www.chromaate.com freds@chromausa.com



www. labtechcircuits .com

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- Mixed dielectric multilayers

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RF product of the month

128 MBIT MOBILE RAM

Infineon Technologies has developed 128 Mbit mobile RAM. Designed specifically for use in battery-powered handheld electronic products, the mobile RAM is a low-power synchronous dynamic random access memory (SDRAM), mounted in a space-saving, fine-pitch ball grid array (FBGA) package that is DBEER 200 fully compliant with the new joint electron device engineering council (JEDEC) standard. Compared to standard thin small-outline package (TSOP)-mounted SDRAM, the form factor of the RAM is reduced by more than a factor of three, with the FBGA occupying a footprint of just 8 mm x 9 mm. Power consumption can be reduced by as much as 80% compared to standard 128 Mbit SDRAM, depending on the operating conditions and system design. Additional power saving functions include an operating voltage of 2.5 VDC and I/O voltage of 1.8 VDC or 2.5 VDC, as well as a special power management as specified by the recent JEDEC standardization of the low-power SDRAM devices. Mobile RAM represents a significant step in the program to maximize battery life size, weight and total system cost of the next generation of personal digital assistants, smart phones and digital still cameras. Infineon's product roadmap for mobile RAM includes the 128-Mbit part in x8 and x16 organizations, as well as plans to introduce a 256-Mbit version in 2002. The 128-Mbit mobile RAM is suited for a growing number of higher-end systems. The next-generation mobile-RAM will provide this memory density by using just two FBGA devices. Later this year, Infineon will offer mobile-RAM samples both in the new JEDEC-standardized 54-ball FBGA package, and in standard TSOP-

Specifications at a glance:

- 128 Mbit capacity
- 2.5 VDC operation with 1.8 VDC I/O voltage
- FBGA packaging
- JEDEC standard

(1) Infineon

128M Mobile-RAM

mounts to simplify system evaluation for customers working with development hardware laid out for the larger package. All production volume of the RAM will be mounted in the FBGA. Features of the RAM

include: 8M x 16 organization, 54-ball, temperature compensation of refresh rate, partial array select and 256M density in preparation.

> **Infineon Technologies** www.infineon.com company.info@infineon.com

Compact, high-density memory for wireless products



Announcing the first annual RF Design Editor's Choice Product of Cire Year

Coming in the December 2001 issue of RF Design

RF product focus — EMI/RFI

Spanner head EMI filters

Tusonix has developed a π -circuit, spanner head filter that allows for sophisticated multiposition assemblies. This suppression filter can be inserted quickly into the chassis



and connected by machine lead wire wrap without the use of solder. Its slender design also makes some of the most compact mounting assemblies possible, offering a lead spacing of 0.200 inches (5 mm). These filters have a cylindrical body of 0.196 inches (4.70 mm) diameter and are available with capacitance values from 100 pF to 5500 pF with minimum insertion loss (per MIL-STD-220) up to 70dB at 10GHz. The filter is designed for projects where cost

and space savings are essential. Common applications for this filter involve power amplifiers, microwave equipment, frequency generators and virtually any application where signal lines require a space-efficient filter design. **Tusonix**

www.tusonix.com sales@tusonix.com

Noise source offers evaluation of EMC test areas to 7GHz

Schaffner introduces a high-frequency broadband source for evaluation of anechoic chamber and open-area test site EMC measurements. The comparison noise emitter, CNE 6507, is a continuous spectrum-radiated noise source with a useable output from 1.5 to 7 GHz.



EMC test best-practice dictates regular use of a reference source to check consistency of site measurement instrumentation across the entire test spectrum. This system offers the ability to make consistency checks to 7 GHz. The rugged, portable unit can be used for carrying

out checks in GTEM cells, anechoic chambers and openarea test sites. Powered by a rechargeable battery pack, it requires no power cables, which could distort emission fields. Batteries last for seven hours (continuous use) and can be easily replaced in the field, if necessary, for minimal downtime.

Schaffner www.schaffner.com Usasales@schaffner.com

Low-profile RFI/EMI shielding gaskets

Tech-Etch introduces two low-profile BeCu gaskets, offering RFI/EMI shielding effectiveness to 100 db attenuation. The gaskets measure 0.08" high. Stick-on mounting pro-



vides a fast installation and may be used at ambient temperatures from -67° F to 300° F. Item numbers are 60P21 and 125G32. They are suit-

able for bi-directional applications, require only a low closing force, and provide 360° of snag-free operation. **Tech-Etch**

www.tech-etch.com sales@tech-etch.com

Highly conductive shielding fabric

Holland Shielding Systems has developed a highly conductive fabric that needs minimal pressure to achieve an electrically conductive contact. This fabric can be used for cable wrap, EMI shielding and gas-



kets. The required closure force to guarantee good shielding performance of the gasket is low, placing less stress on parts. The tolerances can also be looser, which can help manage production costs. The fabric is available on rolls with a width of 10 to 1400 mm for applications such as cable shielding, shielded tents and wall covering for Farady-cages. It can also be delivered in a flameretardant version. The company also offers complete gaskets with a size between 0.7 and 60 mm. **Holland Shielding**

www.hollandshielding.com info@hollandshielding.com

Integrated high/low frequency filter

KOA Speer Electronics introduces a full line of standard and enhanced T filter networks for the suppression of EMI/RFI at low and high frequencies. The filters combine filtering capabilities, stability and reliability with a symmetrical design that allows for the filtering of bi-directional signals. The TFA and TFB series filter networks can replace as many as 24 discrete components,



thus saving board real estate and offering a component cost advantage. Each network has a resistance range of 10 Ω to 10 k Ω and capacitance range of 10 pF to 220 pF. Resistance tolerances of \pm 5%, \pm 10% and \pm 20% are offered, with a TCR of \pm 250 ppm/°C for each circuit type. Body style options include wide SOIC, QSOP and TSSOP. KOA Speer electronics www.koaspeer.com

Continued on page 88

MICRO-MINIATURE DIRECTIONAL COUPLERS \$199

5-2000MHz world's smallest couplers

Measuring only 0.15"x0.15" square, the DBTC series from Mini-Circuits is quite simply the smallest 5 to 2000MHz directional coupler series on Earth! Available in 9 to 20db nominal coupling values, these patented 50&75 ohm couplers integrate Blue CellTM design techniques for very flat response, low insertion loss, and multi-decade broad bandwidths. All-welded connections improve reliability, and automated production delivers high unit-to-unit performance repeatability. Preserve precious board space, and capital as well. Specify Mini-Circuits DBTC directional couplers...priced at only \$1.99 each (qty. 25)!

Mini-Circuits...we're redefining what VALUE is all about!

Coupling	Model	Freq. (MHz)	Ins. Loss (dB) Midband Typ	Directivity Midband	(dB) Typ
9dB	DBTC-9-4	5-1000	1.2	18	
12dB 13dB	DBTC-12-4 DBTC-13-4	5-1000 5-1000 5-1000	0.7 0.7	20 21 18	
13dB	DBTC-13-5-75	5-1000 1000-1500	1.0 1.4	19 17	
16dB	DBTC-16-5-75	5-1000 1000-1500	1.0 1.3	21 19	
17dB	DBTC-17-5	50-1000 1000-1500 1500-2000	0.9 1.0 1.1	20 20 14	
18dB 20dB	DBTC-18-4-75 DBTC-20-4	5-1000 20-1000	0.8 0.4	21 21	
	Protected by U.S.	Patent 6140887.	Additional patents pur	iding	BLUE CELL

DESIGNER'S KITS

K1-DBTC (50 Ohms) 5 of ea. DBTC-9-4, 12-4, 13-4, 17-5, 20-4. Total 25 Units \$49.95 K2-DBTC (75 Ohms) 5 of ea. DBTC-10-4-75, 13-5-75, 16-5-75, 18-4-75. Total 20 Units \$39.95





P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 For quick access to product information see MINI-CIRCUITS CATALOG & WEB SITE The Design Engineers Search Engine Provides ACTUAL Data Instantly From MINI-CIRCUITS At: www.minicircuits.com

ISO 9001 CERTIFIED

Custom EMI/RFI filters

PEI offers a series of shields designed to protect components from RFI/EMI, and to provide electrical grounding. PEI offers custom CDW bend lines, logos and RF cans with easy-access removable top covers. Shielding options for circuit-board applications include: one-piece or twopiece construction and flat, formed or easy-access configuration. Standard materials include tin-plated brass, copper, and stainless steel as well as SAE 1010 and nickel-silver (other materials and finishes are available upon request), etched holes or patterns for component cooling (at no additional charge). CDW (controlled depth/width) etch to hand-form at specific angles PEI's manufacturing process complies with MIL-I-45208 standards. Applications for PEI's new line of shielding products include aerospace, defense and commercial electronics; communications equipment; medical and biomedical equipment; and appliances. PEI

www.photofabrication.com

RF-absorbent flexible material

API Delevan announces a new line of RF-absorbent flexible ferrite. The product suppresses EMI noise that radiates from active RF components and to protect sensitive circuit board designs that are affected by external interference. The Flexible Ferrite pro-



vides effective EMI suppression in the 10 MHz to 3 GHz frequency range with electrical resistance from 106 Ω to 108 Ω . The material is useful in achieving compliance with the most recent FCC and CISPR requirements. The material is available in tubular and sheet forms. The FFAM Series comes in four sheet sizes from 100 x 100 mm to 400 x 400 mm and six thickness ranges from 0.25 mm to 2.5 mm. The material can be die-cut for gasketing applications and is also available with optional non-conductive UL-recognized adhesive backing. The FFAT Series is the flexible tubular form available in four diameters. all in one-meter lengths. FFAT effectively eliminates EMI and RH problems on external power, data and signal lines

API Delevan

www.delevan.com apisales@delevan.com

SMA field-replaceable connectors to 27 GHz

Molex is now offering SMA fieldreplaceable connectors for high performance and low loss from DC to 27 Ghz. Applications for these connectors are hermetic and non-hermetic, including microwave devices (amplifiers, transmitters/receivers, filters, oscillators), test equipment and telecommunications equipment. Stainless steel and passivated, the connectors have Teflon insulators and beryllium copper contacts that are gold-plated. These connectors also include substantial vibration, shock and thermal features

Specifications at a glance:

- DC to 27 GHz
- VSWR rating of 1.05 ± 0,0045
- Insertion loss of 0.03 x f(GHz)

adhering to MIL-Type standards. The design has a raised boss at the flange end of the connector that provides an EMI/RFI gasket to reduce leakage. The products have a VSWR rating of 1.05 ± 0.0045 (fGHz), -(120 -fGHz) db RF leakage level, and an insertion loss of 0.03 times the square root of f(GHz). The connector, which is not an integral part of the package, allows easy replacement by simply removing the mounting screws with a screwdriver. Due to the low-loss characteristics, additional applications include vertical PCB connectors for applications to 18 GHz. Additional accessories can be

provided, including hermetic seals, launch pins and dielectric insulators, pins with tabs and pins with tabs and dielectric insulators. **Molex**

www.molex.xom

amerinfo@molex.com

Chip-on-board filtered D-sub connectors

Spectrum Control introduces the Series 100 chip-on-board (COB) EMIfiltered D-subminiature connector. This series is designed as a filtering method for the elimination of EMI. The COB connector design incorporates chip capacitors surface-mounted on an integrated PC board. The 0.318" footprint of the new filtered connector allows it to be used as a drop-in replacement for unfiltered designs.

Specifications at a glance:

- 5 A max current rating
- 100 to 5600 pF capacitances
- UL94V-0 thermoplastic
- Insulation resistance of 500 $\text{M}\Omega$

The connectors feature a dielectric withstanding voltage of 250 VAC (for five seconds), and a current rating of 5 A. Capacitance values include 100, 220, 470, 820, 1500 and 5600 pF with an insulation resistance of 500 M Ω . These connectors are available in 9-, 15-, 25- and 37-position male or female contacts and are compatible with full-metal shell cable connectors. Right-angle-mounted designs are currently in production, with vertical mount and solder cup termination designs soon to be released. The connector uses #4-40 threaded insert mating hardware and integral boardlocks for secure posting prior to soldering. The connector housings are constructed of UL94V-0 rated thermoplastic for durability. The connectors are for use in network servers, firewalls, routers, test and diagnostic equipment, medical monitoring equipment, and I/O interfaces on computers and portable wireless devices.

Spectrum Control www.spectrumcontrol.com spectrum@spectrumcontrol.com



High Performance Electromagnetic and Network Simulation and Optimization Tools

From: Zeland Software, Inc., 39120 Argonaut Way, PMB 499, Fremont, CA 94538, U.S.A., Phone: 510-623-7162, Fax: 510-623-7135, E-mail: zeland@zeland.com, Web: http://www.zeland.com

Products:

IE3D Planar and 3D Electromagnetic Simulation and Optimization Package FIDELITY Time-Domain FDTD Full 3D Electromagnetic Simulation Package MDSPICE Mixed Frequency Domain and Time-Domain SPICE Simulator COCAFIL Cavity coupled wavguide filter synthesis package

Applications:

Microstrip, CPW, striplines, suspended-strip lines, coaxial Lines, rectangular waveguides, high speed digital transmission lines, 3D interconnects, decoupling capacitors in digitial circuits, PCB, MCM, HTS circuits and filters, EMC/EMI, wire antennas, microstrip antennas, conical and cylindrical helix antennas, inverted-F antennas, antennas on finite ground planes, and other RF antennas.

Important Announcements:

- The IE3D 8.0 is released. The most important features added into the IE3D 8.0 are: (1) Boxed Green's functions
 for structures in enclosures; (2). Periodic Green's functions for large antenna phase arrays; (3) Multiple robust
 advanced iterative matrix solvers (AIMS) for accurate and fast simulations of large structures using much less
 RAM. The IE3D has complete modeling and design capability for patch antennas, wire antennas, microwave
 and RF circuits, MMICs and RFICs, multile layered PCBs and BGA structures. The IE3D also has robust and
 efficient advanced symbolic electromagnetic optimization.
- The FIDELITY Release 3 has complete SAR analysis features for the wireless applications. It will offer multiple frequency independent head models.
- The MDSPICE 2.1 is released. The MDSPICE 2.1 features robust s-parameter based time domain simulation for non-linear circuits in both analog and digital circuit design. Its results normally meet the casuality condition with accurate time delay prediction. The MDSPICE also features wide band SPICE model extraction.
- The COCAFIL is released. The COCAFIL allows precise modeling and synthesis of waveguide filters.

IE3D and FIDELITY Simulation Examples and Display

An 8 by 8 patch array modeled with all coupling included on the IE3D 8.0 using 100 MB RAM



IE3D modeling of an inverted-F antenna with finite thick plate and finite size ground plane







The forward and backward radiation from a hern antenna modeled on the FIDELUTY



The human head models without frequency limitation

on the FIDELITY for SAR research

FIDELITY modeling of a cylindrical helix antenna



Zeland Software, Inc. provides excellent technical support and services. Zeland Software, Inc. is also the north American exclusive representative for the LINMIC product from Jansen Microwave GmbH

RF products

Low-dropout, small-footprint regulator

Micrel introduces a small-footprint 750 mA, 2.5 VDC regulator for 1.8 or 1.65 VDC conversion. The device features a low dropout voltage and a MSOP-8 footprint. The MIC3975 operates with minimum headroom and offers a

Specifications at a glance:

- 300 mV dropout voltage
- •750 mA output
- Fixed and adjustable output voltages
- · Logic-enable input
- · Error flag alert for output fault

d r o p o u t voltage of 300 mV at its full load of 750 mA. The main applications for the device include powering 1.65 or 1.8 VDC digital ICs from



a 2.5 VDC $\pm 10\%$ system bus or 2.5 VDC digital ICs from a 3.3 VDC $\pm 10\%$ system bus. For applications requiring more than 750 mA, Micrel also offers the MIC39 10x, MIC3915x, MI3930x, and MIC3950x LDOs, which can support continuous currents of 1.0 A, 1.5 A, 3.0 A, and 5.0 A, respectively. All of these devices are designed to support the low-voltage digital ICs manufactured on 0.25 μ and 0.18 μ process technology. The MIC3975 is offered in MSOP-8 packaging using Micrel's uCap design to achieve miniature size, high stability and improved reliability. Applications include distributed power applications, fiber optic modules and digital IC power.

www.micrel.com lwong@micrel.com

AMPLIFIERS

Three-stage 17 to 27 GHz GaAs pHEMT MMIC amplifier

Mimix Broadband announces a GaAs MMIC three-stage gain block amplifier, which can be operated with all three stages biased in parallel. The gain block amplifier covers the 17 to 27 GHz frequency bands with a typical small signal gain of 22 dB with a typical noise figure of 3 dB across the band. The XB1000 can be biased for low-noise performance or high-power performance and is suited for wireless communications applications such as millimeter-wave, point-to-point radio, local multipoint distribution services (LMDS), SATCOM and VSAT applications.

Mimix Broadband www.mimixbroadband.com

3.4 to 3.6 GHz, 8 W SSPA

Stealth Microwave introduces the model SM3436-38 SSPA. The amplifier operates from 3.4 to 3.6 GHz, has a P1dB of +39 dBm (typ.), and has an OIP3 of +50 dBm (typ.) Linear gain is 45 dB \pm 0.5 dB. This small GaAs FET module, (6.5 l x 3.7 w x 2.0 h) operates from +12 V and consumes only 3.4 A. Standard features include > 20 dB of gain control, over/reverse volt-



age protection, logic on/off, and thermal protection with auto reset. Available options include forward power detection and output harmonic filtering. Stealth Microwave www.ssbtech.com

sales@ssbtech.com

0.8 to 2.5 GHz 150 W HPA

The model 5102 from Ophir is a small, lightweight, high-power, solidstate amplifier with a minimum linear



power of 120 W across the 800 to 2500 MHz band. Applications include multiband PIM testing, device testing and TWTA replacement.

Ophir www.ophirrf.com sales@ophirrf.com

High IP3, low-noise amplifier

Mini-Circuits introduces an 1850 TO 1910 MHz low-noise coaxial amplifier with high IP3. Typically, these medium-power amplifiers operate with 21 dBm maximum power output at 1 dB compression, ultra-low 0.9dB noise figure, and a high, +37-dBm, IP3 to help suppress noisy intermodulation products. Gain is 16.5 dB typical





140-2150MH: HIGH IP3 MIXERS PERFORM AT VALUE PRICE

Mini-Circuits has unveiled a collection of SM mixers incorporating patented technology to deliver the highest IP3 for low, medium, and high LO power levels. With IP3 as high as +38dBm, HUD and HJK models require no DC power, which simplifies circuit layout and makes them very easy to use in 140-2150MHz applications. Additional features include very low conversion loss down to 6.7dB, high isolation up to 47dB, and 1dB RF compression point 3dB higher than LO power.



2WAY-90° SPLITTERS ARE FEATURE RICH 340 TO 2400MHz

A new family of low profile 2way-90° SM power splitters operating within the 340 to 2400MHz band is available from Mini-Circuits. This patented QBA series contains 7 models incorporating Blue Cell[™] technology for superb temperature stability, ultra-low profile down to .050", and low cost. Features include high power capability up to 50W, high isolation up to 28dB, and low insertion loss down to 0.25dB (all typ). Leads are solder plated and internal connections welded.



50mA MMIC AMPLIFIERS PROVIDE HIGH RELIABILITY DC-4GHz Mini-Circuits has introduced a family of 5 different 50mA "GAL" model MMIC amplifiers for reduced bias current requirements in DC to 4GHz applications. With up to 15.9dBm (typ) output power, these InGaP HBT 50 ohm amplifiers are housed in a miniature SOT-89 package with exposed metal bottom for excellent heat dissipation and low thermal resistance. Ideal for today's compact designs such as cellular and PCS. 50 piece Designers Kit with test fixture available.

WIDEBAND HIGH IP3 MIXERS PERFORM WITHIN 5 TO 2500MHz

Realize very high IP3 performance over broad bandwidths within 5 to 2500MHz while at the same time achieving low conversion loss and high isolation by selecting from Mini-Circuits team of nine high IP3 "SYM" mixers. Typically at midband, these level 10, 13, and 17 (LO) mixers display IP3 as high as 32dBm to help suppress intermodulation products in crowded cellular, ISM, and PCS bands. Units measure 0.500"x0.375"x0.230" and operating temperature is -20°C to +85°C.





I TO 30dB SMA M-F ATTENUATORS AVAILABLE IN DESIGNERS KITS Mini-Circuits low cost family of DC to 6000MHz VAT fixed attenuators are now available in 3 convenient Designers Kits. *Kit No. K1-VAT* features 1ea. of 3, 6, 10, 20, and 30dB attenuation values and is priced at only \$49.95. *K2-VAT* includes 1ea. of values 1 thru 10dB (in 1dB steps) priced at \$99.95. And *Kit K3-VAT* contains 2ea. of the 3, 6, and 10dB models for only \$59.95. Rugged unibody construction measures 1.42" long (.370" diameter) and power rating is 0.5W (at 70°C ambient).



0.5-2500MHz TRANSFORMER SERIES HAS IMPEDANCE RATIO TO 9:1

Mini-Circuits has recently announced a low cost family of miniature RF transformers for use in the 0.5 to 2500MHz band. Thirteen "TCM" models with 1, 2, 3, 4, 8, and 9:1 impedance ratios exhibit excellent amplitude and phase unbalance for balanced to unbalanced transformation, good return loss, and broad band coverage. Small 0.150"x 0.160" x 0.160" open case design has plastic base with solder plated leads, and applications include push-pull amplifiers and impedance matching.





P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 For quick access to product information see MINI-CIRCUITS CATALOG & WEB SITE The Design Engineers Search Engine Provides ACTUAL Data Instantly From MINI-CIRCUITS At: www.minicircuits.com



with +0.2 dB (typ) flatness. The units are equipped with 50 W SMA-female connectors. Mini-Circuits www.minicircuits.com sales@minicircuits.com

SIGNAL SOURCES

Small, low-power PLL for digital, military apps

Elcom offers a series of 0.5 to 26 GHz phase-locked oscillators. These oscilla-



tors are used to phase-lock microwave DROs to a crystal reference (10 MHz to 800 MHz range). The MPDRO series requires only a single loop for phase

Specifications at a glance:

- 0.5 to 26 GHz output frequency
- +12 dBm ±2 dBm power out
- <125 dBc phase noise</p>
- 12 to 24 VDC operation

locking, thus minimizing size and power consumption. The units feature low phase noise, low DC power consumption (<200 mA) and a wide operating temperature range of -45° to $+75^{\circ}$ C. The device is packaged in a 2.25" x 4.1" x 1.2" housing. The MPDRO units are suitable for use in military, digital radios, SATCOM and instrumentation applications. Elcom Technologies www.elcom-tech.com sales@elcom-tech.com

Miniature, low-profile SMT VCO

Tellurian announces a line of miniature, low-profile, surface-mount clock oscillators. The T4000 is designed for a range of applications, including telecommunications, wireless, networking (LAN/WAN), cellular hand sets, and other systems that require a stable



frequency in a space-efficient SMD configuration. Housed in a hermetically sealed 5 x 3.2 mm ceramic package, the T4000 has a seated height of 1.1 mm. The series covers a range of frequencies from 1 to 40 MHz. Units are supplied on tape and reel and are compatible with IR reflow and standard automatic pick and place equipment. The devices are HCMOS- and TTL-compatible and feature tristate enable and disable functions. The oscillators maintain 45%/55% waveform stability. Operating temperature range is -40° C to $+85^{\circ}$ C.

Tellurian Technologies www.telluriantech.com info@telluriantech.com

Industry-standard SMD SPXOs offer low aging

C-MAC has launched a range of simple packaged crystal oscillators (SPXOs) with tight aging properties, targeted chiefly at specialist applications in the industrial and OEM sectors. The CFPS-7 exhibits low jitter, making it suitable for Stratum 4 clock generation in SONET/SDH telecommunications equipment. The oscillator's crystal is packaged separately from the rest of the device, therefore, contamination from adhe-



sives and other circuitry is eliminated. This restricts aging effects to no more than 10 ppm over 15 years. It uses an overtone frequency source, and offers low jitter for telecommunications applications: typically 0.6 ps rms at 155.52 MHz with low-pass and highpass cut-off frequencies of 12 kHz and 5 MHz, respectively. Frequency stability is ±30 ppm or ±50 ppm all causes over 15 years for operating temperature ranges of 0 to +70°C and -40° C to +85° C, respectively.

C-MAC Micro Technology www.cmac.com jkingston.cmac@attglobal.net

Ultra-small, ASIC-based PLL

Vectron introduces a new ultrasmall VCXO-based PLL designed to simplify a wide variety of clock recovery and data retiming, frequency translation, clock smoothing and clock switching applications. The CD-700 features a phase-locked loop



ASIC with a quartz-stabilized VCXO for superior stability and jitter performance. The device can reduce design time, increases circuit reliability and reduces board space. The input data rates range from 8 kb/s to 65 Mb/s, the output has a tri-state option and can be either 3.3 V or 5 V. The device is hermetically sealed in a ceramic SMD package measuring 5.0 x 7.5 x 2 mm. Applications include DWDM, switching, wireless base station, ATM, SONET/SDH, XDSL, network communications, digital audio/video and PBX systems.

Vectron International www.vectron.com

vectron@vectron.com

Surface-mount LVPECL/ LVDS oscillators

M-tron announces the UVC series 5 x 7 mm SMT oscillators. Available in frequencies between 750 kHz and 650 MHz, these clock oscillators provide either LVPECL- or LVDS-compatible outputs in a standard 5 x 7 mm lead-

Specifications at a glance:

- 750 kHz to 650 MHz frequency
- ± 20 ppm stability
- -40 to +85° C temp. range

less ceramic package. The devices offer all-inclusive stability as low as ± 20 ppm over -40 to +85° C with tri-state and tight (45/55%) symmetry. Low jitter and phase-noise performance make the UVC applicable for SONET/SDH/ATM, optical carrier, DWDM, WDM, gigabit Ethernet, and fibre channel applications.

M-tron Industries

www.mtron.com sluchtel@mtron.com

siucntei@mtron.com

Broadband mmWave mixer

Alpha Industries introduces the AM028SI-A2, a broadband mmWave mixer. The device's 26 to 33 GHz frequency range, low conversion loss, wide IF bandwidth, and surface-mount package make the mixer suitable for high-

Specifications at a glance:

- 6 dB conversion loss
- 6 GHz IF bandwidth
- 26 to 33 GHz bandwidth

volume broadband mmWave applications such as LMDS, digital radio, VSAT, and sensors. Incorporating the Alpha-2 package technology into the AMO28S 1-A2 gives the mixer cost advantages compared to bare die alternatives. The rugged surface mount design eliminates the need for expensive microelectronic assembly, eases handling, and makes it more reliable. It offers excellent repeatable electrical performance with solder attachment, eliminating the need for tuning. The single-package design also reduces parts count. Because it is a fundamental-LO mixer, it has improved linearity compared to sub-harmonic mixers. Alpha Industries

www.alphaind.com sales@alphaind.com

TX/RX

High-power TV circulators

UTE has released a series of highpower, low-loss circulators available for the VHF and UHF channels. the CT-1584-D is rated at 3 kW (average) and 10 kW peak power over the full channel 7-13 band. The CT-1325-N series is rated at 500 W (average) and 5 kW

Specifications at a glance:

- UHF/VHF models
- Up to 10 kW power rating
- SMA/EIA connectors

peak over the UHF channels. Three units cover the 470 to 806 MHz ranges. Using DIN 7/16 connectors the power increases to 1 kW CW and 5 kW peak. For stripline applications, CT-1615-S series operates at 250 average power in the UHF bands. This series can also be provided with SMA connectors. Custom devices are available for other frequency ranges and 7/8 EIA flanges. UTE Microwave

www.utemicrowave.com info@utemicrowave.com

Integrated digital, mixedsignal & RF functions

Honeywell introduces a line of highly integrated, low-cost RF attenuators and switches for cellular, PCS and GSM base station, handset and 2.4 GHz WLAN applications. Each chip incorporates active MOSFET devices for RF, digital and mixed-signal functions, which, when compared to Gallium Arsenide (GaAs), greatly reduces RFIC

Specifications at a glance:

- 5 and 6 bit attenuation
- Single/dual rail operation
- DC to 4 GHz operation
- <2 dB insertion loss (typ)

size, external parts, power consumption and cost. The SOI CMOS process allows for easy integration of passive components including inductors, capacitors, resistors and varactors; single or multiple power supplies; and linear power capabilities onto each attenuator and switch. The line includes six attenuator and four switch standard configurations. Their flexible 5- and 6-bit attenuators have single- or dual-rail operation, low DC power consumption, 3.3 to 5 VDC wide supply rails, serial or parallel interfaces, 50 Ω impedance and MLF packaging. Frequency performance ranges from DC to 4 GHz with a high attenuation accuracy (±0.30 dB + 3% of



setting) and a typical insertion loss of <2 dB.

Honeywell SSEC

www.mysoiservices@honeywell.com grenville.hughes@honeywell.com

SP3T RF mechanical switch

Narda introduces a low-cost, singlepole, three-throw RF mechanical switch that offers high performance and long-term reliability with a guaranteed operation of one million cycles per switch position. The MS SMA 033



is a normally open model that operates from DC to 3 GHZ and is available from stock. Narda

www.dept26.com

Ku band diplexer

Microwave Filter Company introduces the Model 14510 diplexer, which provides the simultaneous transmission and reception of Ku-band applications. The unit passes the full 500 MHz



uplink and downlink bands, 14.0 to 14.5 QHZ and 11.7 to 12.2 QHz, respectively. The diplexer offers >0.5 dB insertion loss and <16 dB return loss across the full 500 MHz operating bands, with a mutual isolation of greater than 85 dB. For special applications, the unit can be configured with optional connector types, flange orientations and partial or channelized frequency scenarios.

Microwave Filter www.microwavefilter.com mfcsales@microwavefilter.com

Electro-mechanical switch

Teledyne introduces a new electromechanical switch that operates at 75 Ω within the DC to 3.0 GHz frequency range. The SPDT switch is designed for applications in the communications, test and measurement, aerospace and industrial markets where high speed and high data rates are significant. The CCR-33M10, is a single-pull, double-



throw electro-mechanical switches. The switch is offered in both failsafe and latching actuation operating from a +5, +12, or +28 VDC supply power. Operating range is -25° C to $+65^{\circ}$ C. Additional specifications include: actuator current of 90 mA, max. @ +28 VDC and +20° C; and switching time of 20 msec., max. c +20°C. Options include: indicator circuits, special actuator voltages, UL compatible drivers and power connectors. The switch is packaged in an industry-standard housing measuring 1.50" x 1.30" x 0.50."

Teledyne Wireless www.teledynewireless.com switches@teledyne.com

132 x 64 pixel monochrome graphics display module

Densitron has developed an LCD module capable of surviving extreme temperatures from -20° C to $+70^{\circ}$ C, and high humidity (90% RH). It has an MTBF in excess of 50,000 hours with current consumption of only 96 μ A for typical "normal" mode at 3 VDC. The DV5520 is suitable for incorporation into battery-powered industrial applications

where a harsh environment is likely to be encountered, such as on process control equipment, mobile data collection devices, and handheld instrumentation. Measuring 53 mm (w) x 65 mm (h) and 2.8 mm in thickness, the DV5520 has an effective display area of 50 mm x 30 mm. The display is a high-contrast FSTN type in reflective mode with a 132 x 64 dot (8-line, 22-character) display, and incudes an LCD drive controller chip mounted directly to the LCD glass panel. Features include: display on/off, normal/reverse display, and power save. The 8-bit microprocessor interlace allows direct connection to both the 8080 and 6800 microprocessors.

Densitron

www.densitron.com sales@densitron.com

SUBSYSTEMS

ISM band transceiver module

Radiotronix introduces a modular RF product that completely encapsulates a 900 MHz full-duplex audio/data transceiver into a single hybrid component. These embedded wireless modules allow any engineer to design wireless products. The only external RF component required is an antenna. No production tuning adjustments are required. No RF experience or special test equipment is needed. The EWM-900-FDTC operates in the 902 to 928 MHz unlicensed frequency band. In data mode, a pair of transceivers can send and receive data at rates up to 1 9.2 kbaud over distances of 1,000 feet. In audio mode, a pair of transceivers can send and receive voice over distances to 1,500 feet. The transceiver is programmed using a simple serial interface. The module's footprint is 1.22" x 0.83" x 0.4" and can be assembled to the customer's PCB using standard through-hole assembly techniques.

Radiotronix

www.radiotronix.com stevem@radiotronix.com

256 Kb I²C serial EEPROM

Microchip announces a 256 kb I²C serial EEPROM that fits in an 8-lead TSSOP package. The 256 kb and 128 kb 12C EEPROM devices are now available in either an eight-lead TSSOP or 150 mil SOIC package using industry-standard printouts. These higher-density memory devices offer smaller packages that

Specifications at a glance:

- 256 kb density EEPROM
- 64 byte page write ability
- Random and sequential reads
- -40° C to +85° C temperature

were previously reserved for lowand mid-density EEPROM devices. The 256 kb I²C EEPROM devices, 24AA256, 24LC256 and the 24FC256, have a page-write capability of as high as 64 bytes of data and are capable of botrandom and sequential reads up to the 256 K boundary. Functional address lines allow as many as eight devices on the same bus, for as much as 2 M bit total address space. The devices have a 1.8 to 5.5 VDC operating voltage and -40° C to +85° C industrial temperature range.

Microchip Technologies www.microchip.com

CDMA RF synthesizer

Silicon Labs debuts the Si4135 CDMA RF synthesizer, the newest member of the company's Criterium RF synthesizer family. The singlechip Si4135 is based on CMOS RF architecture and meets the stringent phase-noise performance requirements of the IS-95 and AMPS cellular standards. The synthesizer eliminates the need for more than 40 external components, including RF VCOs, decreasing required board space by as much as 90% over traditional solutions and providing cost savings. The Si4135 is designed for single-band, dual-band, dual-mode and tri-mode CDMA/AMPS handsets and other IS-95 wireless data applications in the United States and Korea. The single-chip RF synthesizers integrate three VCOs, loop filters, reference and VCO dividers and phase detectors in a low-profile CMOS IC. The Si4135 synthesizes frequencies for the U.S. PCS and cellular bands, performing RF synthesis at 1.719 to 1.780 GHz and 954 to

980 MHz, and IF synthesis at 420.76 and 170.76 MHz. The Si4135 also synthesizes RF frequencies from 1.620 GHz to 1.650 GHz for the Korean PCS band, and an IF frequency of 440.76 MHz.

Silicon Laboratories www.silabs.com sharon.lear@silabs.com

SPACE/MILITARY

Hybridized PLL synthesizer for military applications

EM has developed the HLX-series phase-locked frequency synthesizer. The device is hybridized and hermetically sealed for use in military and other high-reliability applications.



Available from 50 MHz to 3800 MHz, the product is provided with exceptional phase noise characteristics in fixed-frequency or programmable frequency bands, with octave bandwidths. Packaged in a 0.8" square surface-mount housing, the HLX-Series meets the screening requirements of MIL-STD-883.

www.emresearch.com

TEST AND MEASUREMENT

Analyzers with multiple platform testing capability

Anritsu Company introduces GPRS and HSCSD measurement software for its MT8801C and MT8802A radio communications analyzers. The analyzers support CPRS, HSCSD, and GSM 400, as well as major global cellular standards such as GSM 900/1800/1900, PHS, PDC, IS-136, DECT, AMPS, and IS-95 in a single handset tester. The analyzers offer measurement flexibility, accuracy and capability for handset manufacturers, and is suitable for R&D and manufacturing. The software allows the analyzers to set up multi-slot calls, in both the uplink and downlink directions, and performs numerous RF measurements. An optional variable downlink slot power feature gives the



user control over the level and content of each downlink slot, for realistic simulation of multislot environments. Additional transmitter tests that can be performed include RACH burst capture to measure the accuracy and timing of RACH bursts, and adjacent-channel power to monitor spurious emissions. A GPRS test mode command places the mobile under test into a known transmission state for repeatable transmitter (Tx) measurements. An optimized transmitter test function can be initiated so only those measurements required are performed, saving production time. Anritsu

www.us.anritsu.com

MATERIALS/ PACKAGING

High-impedance power package

Zentrix announces a new family of high-impedance power packages for use in RF and microwave applications. H.I.P. packs provide the enabling high dissipation package platform for microwave device manufacturers to create 100+ W, 2+ GHz LDMOS FETs with 10+ Ω input and output impedances. Zentrix Technologies

www.zentrix.com lvalenzu@zentrix.com

DC to 23 GHz leaded packages for VSAT apps

StratEdge introduces an LCC family of DC to 23 GHz amplifier packages for C-and Ku-band VSAT applications.

These ceramic packages feature two or more RF leads and multiple DC leads, providing easy and cost-effective attachment to the next level of the system, while maintaining the integrity and electrical performance of the integrated circuit. The package combines a copper composite base with a patented microstrip-embedded microstripcrosstrip transition design. This composite metal base provides thermal conductivity and expansion compatible with GaAs (gallium arsenide) chips. A plastic cap lid with epoxy preform finishes the structure and provides protection for the device.

StratEdge www.stratedge.com info@stratedge.com

FIBER OPTICS/IR

Slim line family of IrDAcompliant transceivers

ZiLOG introduces a low-profile module that will allow designers to add infrared connectivity to the thinnest PDAs, cell phones and other handheld portable devices. Housed in a miniature 9.1 mm x 3.4 mm package, the ZHX1810 measures 2.75 mm high. Designed to operate using the IrDA-Data standard, the device combines an IRED emitter, a PIN photodiode detector, a digital AC-LED driver and coupled receiver/decoder in a single package. Three external components are required for a complete serial infrared (SIR) solution. It operates with a minimum link distance of 1 meter and supports transmission speeds from 2.4 to 115.2 kb/s The device's external metal shield adds extra RFI/EMI protection, and a tab on the metal shield improves solder retention, so the module is less likely to separate from the printed circuit board if the PDA or cell phone is dropped. ZiLOG

www.zilog.com kmalanczuk@zilog.com

INTERFACE/ INTERCONNECTs

Low-loss 7-16 DIN connector

RF Connectors offers its 7-16 DIN series coaxial connector designed for use with LMR-600 low-loss cable from Times Microwave and WBC-600 low-

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loss cable from CommScope. The RFD-1604-2L2 is a 7-16 DIN male crimp connector featuring a silver-plated body and contact for optimum inter-modulation distortion reduction and Teflon insulation for its preferred dielectric performance. The RFD-1631-2L2 is the 7-16 DIN female crimp termination designed for use with LMR-600 and WBC-600 cables.

RF Connectors

www.rfindustries.com rf@rfindustries.com

SEMICONDUCTORS/ ICs

Next-generation ELM series transistors

GHz Technology announces its first series of next-generation avionics transistors designed to handle onboard communications in more crowded air corridors. A series of bipolar common base pulsed devices make up the extended length message (ELM) transistors designed for use in next-



generation Mode-S systems, with a high duty burst that allows the aircraft to exchange longer, more varied data to other members on the network regarding its altitude, position and speed. The series include MDS350L and MDS550L, high-power transistors. The MDS transistors complement the company's 0912-25 and 0912-7 transistors to complete the ELM series. Designed for use in high duty bursts in L-band (1030/1090 MHz), the ELM transistors can send 16 message segments repeated within 2.16 milliseconds. GHZ Technologies

www.ghz.com

Second-generation MOS monolithic IC family

Vishay announces a series of MOS monolithic integrated circuits (MOSMICs) that will allow designers to upgrade the performance of UHF and VHF tuners at no additional cost. Serving as a low-noise RF input stage, the new "X" devices provide improved automatic gain control (AGC) and cross modulation behavior compared to previous-generation MOSMICs. Six new MOSMIC devices, each available



in three surface-mount package types, offering a typical transadmittance specifications from 24 ms to 40 ms. All six high-gain (>20 dB at 800 MHz) devices feature integrated protection diodes and an on-chip biasing network, eliminating the need for a number of external passive components. Because MOSMICs can be switched off directly by the PLL in tuner circuits, external switching transistors can be eliminated as well. **Vishav**

www.vishay.com margarete.seeharsch@vishay.com

RF glossary

GLOSSARY OF TERMS USED IN RF DESIGN

2G - second generation wireless systems 3G - third generation wireless systems A/D - analog-to-digital AC - alternating current ACPR - adjacent-channel power ratio ADC - analog-to-digital converter AGC - automatic gain control ALU - arithmetic logic unit AMPS - advanced mobile phone system ANSI - american national standards inst. AODV - ad-hoc on demand distance vector ASIC - application-specific integrated circuit ASK - amplifier shift keying ASP - application service provider ATM - asynchronous transfer mode AWGN - additive white gaussian noise BER - bit error rate BPSK - binary phase shift keying CCRR - co-channel rejection ratio CDMA - code-division multiple access CDPD - cellular digital packet data CGI - common gateway interface CMOS - complementary metal-oxide semiconductor COTS - commercial off-of-the-shelf CMRR - common-mode rejection ratio CPE - customer premise equipment CW - continuous wave DC - direct current DCS - distributed communications system or digital cellular system DCT - discrete cosine transfer DDS - direct digital synthesis DECT - digital european cordless telephone DSP - digital signal processor DUT - device under test EEPROM - electrically erasable programmable read-only memory EMC - electromagnetic compatibility **EMI** – electromagnetic interference ESD - electrostatic discharge ETSI - european telecommunications standards institute FCC - federal communications commission FDD - frequency division duplex FEM - finite-element method FER - frame error rate FET - field-effect transistor FFT - fast fourier transform FHSS - frequency-hopping, spread spectrum FIFO - first-in, first-out FIR - finite impulse response FSK - frequency shift keying FPGA - fine-pitch ball grid array GaAs - gallium arsenide GaN - gallium nitride Gb - gigabit

GB - gigabyte GFSK - gaussian filtered frequency shift keying GMSK - gaussian minimum shift keying GPIB - general-purpose interface bus GPRS - general packet radio service GPS - global positioning system GSM - global system for mobile communications HBT - heterojunction bipolar transistor HDR - high data rate HEMT - high electron mobility transistor HSCSD - high-speed circuit-switched data HTTP - hypertext transfer protocol I and Q - in-phase and quadrature I/O - input/output IC - integrated circuit IF - intermediate frequency IM - intermodulation IMD - intermodulation distortion InP - indium phosphide IP - internet protocol ISM - industrial, scientific, and medical JEDED - joint electron device engineers council JSP - java server pages LAN - local area network LCC - leadless chip carrier LDMOS - laterally diffused metal oxide silicon LMDS - local multipoint distribution service LNA - low-noise amplifier LO - local oscillator LOS - line of sight LPF - low-pass filter LSI - large scale integration LTCC - low-temperature co-fired ceramic MDS - multipoint distribution systems MMAC - million multiply accumulate operations MMDS - multichannel multipoint distribution service MMIC - monolithic microwave integrated circuit MOSFET - metal-oxide semiconductor field-effect transistor MOU - minutes of use MSPS - million samples per second NRZ - non-return to zero NTC - negative temperature coefficient **OEM** - original equipment manufacturer PA - power amplifier PAR - peak-to-average ratio PCB - printed circuit board PCM - pulse code modulation PCMCIA - personal computer memory card interface association (now simply referred to as PC card) PCS - personal communications system PDA - personal digital assistant PDC - pacific digital cellular PECL - positive emitter-coupled logic

PHEMT - pseudomorphic high-electronmobility transistor PIM - personal information management PLL - phase-locked loop PPM - parts per million **PSK** - phase shift keying QAM - quadrature amplitude modulation QPSK - quadrature phase shift keying RAM - random access memory RFI - radio frequency interference RFIC - radio frequency integrated circuit RFID - radio frequency identification RMS - root-mean-square ROM - read-only memory SAR - successive approximation register SDH - synchronous digital hierarchy SDRAM/SORAM - synchronous dynamic random access memory SEU - single-event upset SiC - silicon-carbide SIR - serial infrared SMA - standardization management activity SMD - short message delivery SMR -specialized mobile radio SMS - short messaging service SMT - surface-mount technology or surface-mount toroidal SNR - signal-to-noise ratio SOIC - small-outline integrated circuit SONET - synchronous optical network SPDT - single-pole double-throw SSPA - solid state power amplifiers TCP - transmission control protocol TCXO - temperature-controlled oscillator TDD - time division duplex TDMA - time-division multiple access TETRA - trans european trunked radio TSOP - thin small outline package TTL - transistor -transistor logic UART - universal asynchronous receiver transmitter UDP - user datagram protocol UMTS - universal mobile telecommunications service UNII - unlicensed national information infrastructure UTRA - UMTS terrestrial radio access VCO - voltage-controlled oscillator VCSEL - vertical cavity surface-emitting laser VCXO - voltage-controlled crystal oscillator **VOFDM** - vector orthogonal frequency division multiplexing VSAT - very small aperture terminal (satellite service) VSWR - voltage standing wave ratio WAP - wireless application protocol W-CDMA - wideband code-division multiple access

WLAN – wireless local area network XDSL – another name for an ISDN BRI channel

PGA – pin grid array

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Agilent		2
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Ansoft	63	9
Aplac		7
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Future Electronics		
Gigatronics		25
WL Gore		
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COMPANY NAME	PAGE NO.	READER SVC. NO.
Maxim		
Micrel		57
Mini-Circuits	4,5 ,7, 19	27,28,43,44,41,42
		34,35,58,59,39,40
	60,61,69,87,9115,1	6,76,77,47,48,50,51
	IBC	
MITEQ		60
Murata		x
Nemal		
Noise.com	x	1
Phonon corp		
PTS		61
Renaissance Electronics		
RF Micro Devices		
Rockwell Collins		
Spirent Comm (TAS)	9	64
Sprague Goodman		8
Stanford Microdevices		
Surcom		65
Synergy		
T-Tech		
Ultra RF		
Unity Wireless		
Varil		4
Voltronics Int.		
WJ Communications		
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RF Engineering Manager: 3-5 years engineering management experience in antenna or RF related products, 5 years design experience in Wireless Communication field, and BSEE required. Manage Engineering Department for Base Station Company RF Engineer who can direct engineering activities to include design, test, prototypes, and interface with manufacturing. Must be hands-on player who can also oversee CAD, EE, ME and test technician functional reports.

RF Power Amp Design: Design and develop high-efficiency low-voitage SiGe power devices and amplifiers for cellular/PCS applications. Requirements include MS or PhD and experience in MMIC or RFIC design and test along with 5+ years experience in bipolar and GaAs power amp design.

RFIC Designers: Hands-on engineers specializing in GaAs, SI, SiGe etc. circuit design. Design centers are located throughout the US and internationally. The companies we represent will sponsor citizenship. All our client companies are successful RFIC technology leaders. All levels of engineering technology positions are open. Design, applications, project engineering, manufacturing/production. BSEE or equal experience minimum.

Senior RF Engineer/fiber-optic communications products: Must be able to design and analyze RF circuits and subsystems in the frequency range from DC to 10 GHZ. Responsible for generating schedules and meeting deadlines. Perform hands-on testing and evaluation of new designs. Provide proper documentation. Transition designs to manufacturing, 10-15 years of relevant "hands-on" experience in circuit /system design and product development BSEE (MSEE preferred) Proficiency with the RF CAD tools, ADS, Series IV, Spice, Touchstone, Eagleware, EM simulators. Familiarity with SONET and Gigabit Ethernet is a plus.

Sr. Scientist SAW Devices: Responsible for the research and development of new or modified process formulations and equipment, requirements and specifications in the manufacturing and evaluation of Surface Acoustic Wave (SAW) devices. Conceive, plan and execute projects involving understanding, defining, and selecting new concepts and approaches for new or improved processes in SAW devices. PhD/MS.

Senior Broadband Modem Design Engineer: Candidate will be responsible for the design and implementation of next generation broadband wireless access modern at speeds of 100 kb/s to 40 Mb/s, using MQAM or OFDM modulation schemes. Required candidate must have a BSEE (MSEE desired) with 5+ years RF data communications designs experience. Knowledge of TDD/FDD/TDMA techniques is preferred.

Principal Design Engineer RF IC design in the Wireless Communications and/or Broadband technologies. Experience in designing on multiple technologies such as HBT GaAs, S/Ge, B/CMOS, B/polar, is highly desirable. RF Design Engineer Design of RF transceivers used in digital radios in the 2-6GHz frequency range. BSEE

minimum, MSEE preferred. 3+ years of board-level RF and analog circuit design experence. Experience with amplifiers, filters, mixers, PLLs and their integration into radio



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RF in ernest

Industry update – show me the money



by Ernest Worthman technology editor eworthman@primediabusiness.com

As many of you who read my column know (when I'm not being satirical or having a heyday with the industry "experts"), I tend to be both conservative and realistic in my assessment of technology. Back about a year ago (November 2000) I took a shot at the prognosticators' incessant promulgation of the impending wireless explosion.

As the century turns – In January and February, I took aim at the supposed proliferation of ASPs (which never materialized). In April I ranted about the realities of reliable wireless communications; and in May, I tried my best to address life after the high-tech bloodletting. But through it all, I've always taken either a (as Roger describes it) "curmudgeon" approach or, as I like to think, a "lets get real" approach.

But having been in high technology since I stuck my finger in a light socket when I was eight years old (twice, just to make sure), I've seen technologies come and go. But what good is experience if you don't learn from it? This is the reason for my "I'll believe it when it works" attitude.

As the year turns – Now that the economy is back on reality's track, I think we all have a much better understanding of the capabilities of technology as well. Over the last few months, virtually all players within the high-tech industry have had a reality check — nobody was 100% right, and nobody was 100% wrong. But almost everybody was caught with their sheets full to the wind when the wind died.

So now, budgets have been revised, work forces have been adjusted and expectations have been grounded. And while it isn't totally over, cooler heads are starting to prevail; the mass hysteria of the past year or two is gone.

Every cloud – There now exists a window of opportunity. Since the mostly vaporware, capital-sucking dot-coms are gone, development can move in the direction that will really advance the high-tech infrastructure.

Several promising areas need R&D funds and serious consideration. While the wireless Web holds promise, it suffers from a lack of interface technology. As I have said over and over, keying in www.findadate.com while driving 60 mph on the freeway just isn't going to cut it. We need development in voice recognition, heads-up displays and/or cranial implant technology to put the pedal to the metal. And we need to get moving with new storage technologies and micro-electrical-mechanical systems (mems).

3G also holds promise, but it suffers from a lack of standards, bandwidth and a universal platform.

To make the wireless Web and xG systems workable, we need to move on with the development of atomic-level computers and single-molecule, nonvolatile storage with speeds and densities hundreds to millions of times higher than what we have now. This is where the VC money needs to go.

Reality eventually wins out – Some good news is on the horizon that indicates the worst is over. Cahners In-Stat Group believes that total worldwide handset semiconductor revenue will increase from \$14.6 billion in 2001 to \$21.7 billion in 2002. And a speaker from the Progress & Freedom Foundation's seventh annual Aspen Summit can be quoted as saying: "I'm really bemused by the gloom and doom that's out there. Not only is it the end of the world, but it's the end of the world forever. We need to get a grip of what has happened here...now some sanity is returning to the world."

And, there are signs that VC and development money is going to be returning to the wireless industry soon as well. Although the VCs are more diligent in their research and are getting real about what is doable and what is chaff (read: dot-coms), a quote from *Red Herring* magazine read: "With the future of wireless hinging on infrastructure, the startups that continue to get funding are the ones laying the foundation for next-generation networks. Whether it's a company that fills gaps in cellular coverage, a software developer that ties wide area networks (WANs) to wireless networks, or a startup that builds wireless voice or data networks into office buildings." — and I agree.

It's inevitable – The fact is that it is impossible to stop the technological juggernaut. But sometimes it needs to catch its breath and separate the wheat from the chaff. Money just doesn't sit. By nature, it seeks opportunity. Things will start to pop again soon. Solid doable technology will surface from the ashes and rise on its merits. The real issue is the ability to see through the hype to what the doable technologies are and employ levelheadedness.

So, now I think we are at a crossroads. Everyone is taking a hard look at what is real and what is vapor. I'm hoping that the lessons of the late '90s were welllearned, and that the cooler heads popping up will prevail. If so, maybe by the end of this decade, I'll finally be able surf the wireless Web within my heads-up display, using just plain speech, anywhere in the world.



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