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G G S6r G G G 4 G G 51 G G 51	DC 3000 DC 4000 DC 4000 DC 4000 DC 4000 DC 4000	22 1 12 2 1 14 4 1 18 1 1 20 6 1	73 1.8 35 61 7.5	+24 +0.3 +0.5 ±10 ±1.6	2 8 18.2 17 5 18 0 18 0	27 4.5 40 35 35	18 35 5 34 35 35	136 93 93 78 103	16 70 65 65	35 50 46 45 44	.99 1.49 1.49 1.49 1.49 1.49

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ON THE WEB

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- Improved monthly manufacturer's links pages
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RF editorial

Can't we all just get along?

By Roger Lesser Editor rlesser@primediabusiness.com

I received an e-mail from a reader asking me when I thought there would be "universality" in wireless communications. I was ready to reply that there would never be. But the question got me to thinking, is that true? Is there a possibility of interoperability?

I can recall a presentation I went to a few years ago concerning the International Telecommunications Union's (ITU) effort to bring interoperability to wireless communications. Remember the great debate over the 3G "standard?" I remember quizzing the speaker about the reality of this ever happening. A single standard was too idealistic in my mind. He held out hope but admitted it would be a real challenge. And it was.

Is it the carrier's responsibility?

Can consumers get a device that will work no matter where they are? Let's think this through beginning with the carriers. The carriers (I would use service provider, but I'm still waiting on one that does that) are the ones that mandate what they want in a handset. It's through them that the handset manufacturers design devices to meet the carriers' requirement. The handset manufacturers then turn to the component providers and designers to provide the component and subsystems. So, it's the carriers. Right?

Maybe. Maybe not.

Is it the handset manufacturers?

Can it be the folks behind the various standards? Let's think this through. Various manufacturers developed various technologies to work in various parts of the world. Why would they want to yield to someone else's standard? They wouldn't. That's why we ended up with a "family" of standards as the ITU put it. So it's the manufacturers that are behind the lack of interoperability. Right? Well....

Is it the component manufacturers?

Can it be the component manufacturers? They tell me that they position themselves to support the various standards, but it is a case of supply and demand. There is no real demand for interoperability, so the effort to product components is minimized. I caveat this knowing that a number of components are available that will work across multiple platforms. Yet, there is no real motivation for component manufacturers to push interoperability.

Is it the designer's responsibility?

Who does that leave that can be part of the lack-ofinteroperability food chain? The designer? No, designers



place their efforts where they will produce profit for the company, so designers can't be blamed. That leaves us with one other possible villain - The consumer.

Why are the consumers not demanding it?

Consumers drive the marketplace. Or at least that is what I was taught in college. Consumers create the demand. But how do they do that? Well, they must first see a need based on personal experience. They travel to other cities or counties and find their wireless devices don't work. They then go back to the carriers to ask why. Right? According to a number of the carriers I talked with, they really don't see may complainants. (Really?) Yet, if enough folks did complain, you have demand. Right? Well...

Is it back to the carriers?

Another alternative is for the carriers to create the demand by educating the consumer. How do they do that? Advertising can be an alternative. (What a concept.) Look at all the Cingular ads running on television these days as an example. They are there to create a demand. And the ads seem to be working. So, if a carrier wanted to promote interoperability, and asked a handset manufacturer to build a handset that was, and the handset OEMs went to the component producers and asked for multiplatform capability, this would be the answer. Right?

Too many question and not enough answers

While a lot of questions surround the question of interoperability, there seem to be few answers. While 3G may offer some interoperability, or inter-standard roaming as one 3G wizard called it, it may be too little too late. Also, Bluetooth, Home RF and Wi-Fi are all facing the same issue. Each wants to be the answer, yet all are the problem.

I've noted before in this column that I think interoperability is a linchpin in wireless telecom. Yet, I'm amazed at the lack of attention it gets.

So, gentle reader who asked the question, will there be universality? Only at McDonalds. Not in telecom.



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VC0793-600T	400-800	0.0 - 20.0	-104 dBc/Hz	+12 V	+7 dBm	0.5 x 0.5 x 0.18 in.
VC0793-1500T	1000-2000	0.0 - 20.0	-99 dBc/Hz	+12 V	+7 dBm	0.5 x 0.5 x 0.18 in.



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RF calendar

MARCH 2002

12–16 Embedded Systems Conference – San Francisco – Information: www.esconline.com

18–20 CTIA Wireless 2002 – Orlando – Information: wireless2002.ctsg.com/

APRIL 2002

24–26 RF Safety Seminar at IWCE –

Las Vegas – Information: www.iwceconexpo.com

29–2 Embedded Processor Forum 2002 –

San Jose – Information:

www.mdronline.com/epf

May 2002

7-9 Wireless Edge – Santa Clara – Information:

www.sys-con.com/wirelessedge

 14 Wireless Design Conference 2002 – London – Information:
 193.130.109.223/

JUNE 2002

- 2-7 IEEE-MTTS Seattle – Information: ims2002.org
- 23–26 WCA –

Boston – Information:

www.IWCA.com

24–27 COMNET Wireless – Las Vegas – Information: www.idgworldexpo.com

SEPTEMBER 2002

17–20 PCIA Global Xchange – New Orleans – Information: pciaglobalxchange.com

24–27 European Microwave – Milan, Italy – Information: eumw.com



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www.conted.gatech.edu

MIT – Design of Analog Integrated Circuits – June 24-28; Fundamentals of Lasers, Fiberoptic and Their Unique Applications - July 15-19, Cambridge, MA. Information: MIT Professional Institute. Tel: 617.253.2101; Fax: 617.253.8042. professional-institute@mit.edu; web.mit.edu

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	AFD3-010020-14-SP	1-2	34	1.25	1.4	2.0:1	+10	120
	AFD3-022023-12-SP	2.2-2.3	30	0.50	1.2	1.5:1	+10	100
	AFD3-023027-12-SP	2.3-2.7	30	0.50	1.2	1.5:1	+10	100
	AFD3-027031-12-SP	2.7-3.1	30	0.50	1.2	1.5:1	+10	100
	AFD3-031035-12-SP	3.1-3.5	30	0.50	1.2	1.5:1	+10	100
	AFD3-037042-12-SP	3.7-4.2	30	0.50	1.2	1.5:1	+10	100
	AFD3-040080-35-SP	4-8	24	1.25	3.5	2.0:1	+10	150
	AFD3-020080-40-SP	2-8	23	1.50	4.0	2.0:1	+10	150
	AFD3-040120-55-SP	4-12	18	1.50	5.5	2.0:1	+10	150
	AFD3-080120-50-SP	8-12	18	1.25	5.0	2.0:1	+10	150
	AFD1-010020-23P-SP	1-2	11	1.00	4.0	2.0:1	+23	275
	AFD2-010020-23P-SP	1-2	25	1.50	3.5	2.0:1	+23	400
	AFD3-020027-23P-SP	2.0-2.7	22	1.25	4.5	2.0:1	+23	350
	AFD3-027031-23P-SP	2.7-3.1	22	1.25	4.5	2.0:1	+23	350
	AFD3-031042-23P-SP	3.1-4.2	22	1.25	4.5	2.0:1	+23	350
	AFD3-040080-23P-SP	4-8	20	1.25	5.5	2.0:1	+23	350
	AFD3-020080-20P-SP	2-8	18	1.50	6.0	2.0:1	+20	350
	AFD3-080120-20P-SP	8-12	15	1.50	6.5	2.0:1	+20	350
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RF news

Make room for the ladies

By Megan Alderton associate editor malderton@primediabusiness.com



Let's face it. In the past, wireless has not been known to boast high numbers of female engineers.

Try typing women and high-tech on your Web browser. My search engine yielded 611,785 results. (The numbers vary from day-to-day, I'm sure.) Bluetooth, another oft-surfacing topic in the past few years, turned up 270,012. The subject of women (or the significant lack thereof) in the high-tech workforce, then, must be monumental. Not to say that the Web is the most credible source for information, but we'll let it act as a pseudoscale for now.

Fortunately, in the two years I've worked for *RF Design*, I have noticed a significant influx of women's associations surfacing in the high-tech field. The impact these organizations have on the industry may change the scope of wireless for the longhaul (and may find future tradeshow floors looking a little more co-ed).

I was lucky enough to attend the launching dinner of the Women's Wireless Network (WWN) at the Wireless Communications Association (WCA) show in Boston last year. The WWN is an international organization sponsored by the WCA whose mission is to provide an opportunity for female professionals to network, support and recognize one another. The organization focuses on increasing the presence of women and fostering their personal and professional growth within the fixed wireless industry.

Another association celebrating the growing number of women in the tech field is the IEEE Women in Engineering Committee (WIE). The WIE recognizes women's outstanding achievements in electrical and electronics engineering through IEEE Awards nominations, and also promotes IEEE Member Grade advancement for women to the grades of Senior Member and Fellow. Scopes of interest within the WIE include the gathering and dissemination of information regarding the status of women in the industry; initiatives for, by and on behalf of women in engineering; and ways to improve the climate for women in the IEEE and the workplace.

Many more of these organizations exist, and I expect we will see many more to come. Also worth noting are some of the other industry initiatives designed to pique the high-tech interest of the female masses — and with these we may see the membership numbers of women's associations skyrocket.

In January, the Women's Bureau at the U.S. Department of Labor announced a new initiative called *The Women and Girls in Technology Initiative* (WGIT). Through the WGIT Initiative, a series of technology virtual conference calls will provide networking opportunities for women, as well as access to information on issues, programs, policies and initiatives related to careers in the fields of science, math, engineering and technology. Similarly, the UK has been addressing the issue through funding initiatives and networking programs as well.

For more information on women's wireless initiatives and organizations, see the 611,785 results your Web browser yields — or just go to **www.rfdesign.com**.

Megan

Economy threatens world discrete diode markets

After a period of phenomenal growth due to booming telecommunications and data communications industries, the world market for discrete diodes is constricting, according to a report by Frost and Sullivan, San Antonio.

The current economic downturn has weakened demand from key application sectors, leaving suppliers with large excess inventories. The result, Frost and Sullivan said, could be further erosion of prices that will force manufacturers to rethink business strategies.

The report, World Discrete Diode Markets, reveals that this industry generated revenues totaling \$2.61 billion in 2000. After short-term restriction of returns, total revenues from small-signal, zener, transient protection, and radio frequency (RF) and microwave diode markets will rise steadily through 2007.

To combat price erosion, the ill effects of an economic downturn, and challenges from competing technologies, market participants will have to identify new opportunities to secure income, Frost and Sullivan said. At the same time, the multiplication of electronic devices in automobiles will drive demand for diodes and provide new growth opportunities.

Cadence, Agilent form wireless, wireline alliance

Cadence Design Systems, San Jose, and Agilent Technologies, Palo Alto, CA, have signed a multi-year technology alliance. This partnership is expected to develop and market complete integrated solutions to speed IC design for the wireless and wireline communications industries.

The companies have initiated codevelopment of a more integrated design flow involving the Cadence Analog Design Environment and Agilent Advanced Design System (ADS) software to improve interactivity. Jointly developed technologies, beginning with a tighter integration of these technologies, are expected to become available in the second half of 2002.

In future phases, Cadence and Agilent plan to expand the design flow to incorporate additional electronic design, verification and test technologies from both companies. The result should be a complete systems-to-IC design implementation solution.

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		1000-1500	1.4	17
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BUSINESS BRIEFS

Eagleware's Genesys software powers Sennheiser's RF development of audio products – Eagleware, Norcross, GA. announces that Sennheiser, Old Lyme, CT, will use Eagleware's Genesys design software to bring high-end wireless microphones and headsets to the communication and entertainment industries. Genesys RF synthesis, simulation and layout software enables Sennheiser to respond rapidly to customer demands by reducing time-to-market.

Philips Semiconductors joins Flarion Technologies' flash-OFDM Alliance Program — Philips Semiconductors, San Jose, announces that it has joined with wireless infrastructure companies to support Flarion Technologies', Bedminster, NJ, flash-OFDM Alliance program. As application-specific integrated circuit (ASIC) supplier for the Flarion flash-OFDM technology, Philips will design and manufacture ASICs that support sustained mobile data rates as high as 3Mb/s.



Site provides 802.11 source

With the initiation of 802.11 Planet, a Wi-Fi focused trade show, in June 2001, INT Media Group also launched an 802.11-focused Web site of the same name.

802.11 Planet offers a source for 802.11 business and technology information, featuring news, insights, reviews, tutorials on subjects such as security and interference issues, discussions, events and a glossary.

Information on the 802.11 Planet trade show and expo is detailed and show registration is available online as well.

The site also offers archived information and links to several other *Internet.com* sites, including *ThinkMobile* and *Wireless Authority*.

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Analyzing abrupt microstrip transitions

Discontinuities in transmission lines or device terminations are prime candidates for mismatch errors and EMC/RFI emissions. Understanding how they affect amplifier design saves money and headaches.

By Barney Arntz

C lass AB power amplifiers and devices operating in the cellular and PCS bands (up to 2.2 GHz) are usually fabricated on Teflon-based materials having a board thickness of 20 to 60 mils and a dielectric permitivity of 2.2 to 6.

The power devices themselves are large, occupying a good portion of a wavelength, with drain leads about 1/2" wide. Output impedances for bipolar and LDMOS devices in the 10 to 125 W region usually display one to four Ohms real, with an equal amount of imaginary, impedance. Given those typical constraints, the matching networks at 2 GHz are almost always based on one or more low-imped-



Figure 1. One- and two-hop designs for the drain match.

ance transformer lines, often with a $Z_{\rm o}$ below $10\Omega.$ These transformers are only a quarter-wavelength long if the output impedance of the device is real, which is virtually never the case. Rather, they are somewhat shorter than a quarter wave, and often

much wider than they are long. Further, they have very large steps in width before they get to a 50Ω line. These extreme discontinuities present problems when analyzing the circuits with a Smith chart and cascaded, "pure" transmission-line approach. Pure means that the lines are modeled as distributed two-port networks with a real Z_{o} .

The circuit

Analyzing a typical circuit with both a pure transmission line method and an electromagnetic (EM) method shows that work with the above-mentioned approach is prone to extreme errors – to the point of not being useful. The EM method takes into account the end effects and transitions such as capacitive fringing and the current funneling from a wide to a narrow line. Because the device impedances (more specifically, the optimum conjugate matches for the device) are calculated with the actual geometry using deembedding, a much closer match can be made with the EM method.

Limitations of a typical circuit

Figure 1 shows a matching network for a device whose optimum load impedance is $2 - j4\Omega$ at 2.14 GHz. The optimum load impedance would normally be determined from a load pull measurement, considering tradeoffs such as efficiency, intermodulation performance, peak power and others deemed critical^A. Generally, the measurement would be done with a given modulation type at the maximum expected operating power. For this example, it can be said (carefully) that the device has an output impedance that is equal to $2 + j4\Omega$, with the following understanding:

• The real device is highly nonlinear, not only over the RF cycle, but also over the envelope cycle. Furthermore, just defining impedance becomes difficult, to say nothing of measuring it.

• If it were possible to measure the output impedance under power conditions by applying a high level of RF power to the device and looking at the reflected signal, that impedance would be a complex function of the power. And it would be quite different from the conjugate of the optimum load under modulated conditions.

Having said that, the "device output impedance," called a phantom impedance, is mapped on a Smith chart or into an EM simulator as if it were a linear parameter. This practice allows the design of a matching network which is by definition optimum – and it can be done in either direction relative to the signal flow. That is, looking into the input of the matching network and loading the output of the matching network with 50Ω , or looking into the output of the device (using the phantom impedance) and working backwards to arrive at 50Ω . This "linearization" of the problem fully takes into account the non-linear load line characteristics of the device. These issues are discussed thoroughly in the literature¹.

Figures 1 and 2 show the physical arrangement of the circuit and two electrical models with the pure transmission line method (only the "one-hop"

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VAT-3	HAT-3	3 3	0.15 0.12	1.15 1.1
VAT-5	HAT-5	5 5	0.10 0.08	1.15 1.1
VAT-6	HAT-6	6 6	0.10 0.02	1.15 1.1
VAT-7	HAT-7	7 7	0.10 0.05	1.15 1.1
VAT-8	HAT-8	8 8	0.10 0.04	1.20 1.1
VAT-9	HAT-9	9 9	0.10 0.02	1.15 1.1
VAT-10	HAT-10	10 10	0.20 0.03	1.20 1.1
VAT-12	HAT-12	12 12	0.10 0.05	1.20 1.1
VAT-15	HAT-15	15 15	0.30 0.05	1.40 1.1
VAT-20	HAT-20	20 20	0.75 0.18	1.20 1.1
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design is shown in its physical form). For the one-hop design, a 9Ω line length of 65° is required to do the match. For the two-hop design, a cascade of a 5.7 Ω line and a 35 Ω line is used. The two-hop design has somewhat better bandwidth because it remains in a tighter pattern in the Smith chart, staying within the lower Q "footballs" (not shown). This is true whether the reactive part of the device is fixed (in ohms) over the frequency band or whether it is modeled with an inductor, fixed in henries over the band. Despite the better bandwidth, however, the two-hop design is often not used. This is mainly because it is considerably larger than the one-hop design (142° compared to 65°), and



Figure 2. Electrical models for the match.

because it requires a lower impedance line (5.7 Ω compared to 9 Ω). A lower impedance line is synonymous with a wider line, which not only takes up more space, but also increases the possibility of moding issues and unequal current distribution across the width of the output tab, discussed below. For this article, a single-hop design is used for the analysis.

Figure 3 shows an EM simulation of the current flow for a generalized matching network having a large width-to-length ratio, and also having a large step to the 50 Ω . Four phases of the RF cycle are shown, roughly 90° apart. Note that current flows in opposite directions at the same time in the same conductor, emphasizing the space-time nature of transmission line designs. For Figure 3, the cell size was increased by a factor of four (to eight), relative to those used for impedance analysis, for visual clarity with limited picture sizes. This did not markedly change the current distribution, despite of the fact that the 50Ω line is only one



Figure 3. Current flow in the matching transformer at four phases. The relative line length of the arrows shows the current density.

cell wide (using simulation software from Applied Wave Research).

Port 1 is 500 mils wide, on the left. The transformer is 1080 mils wide. Deembedding is done by extending the port into the board by a few board thicknesses to remove the effects of the boundaries. The deembedding delineation is not shown for clarity.

Issues that arise

•The current distribution along the width of the line at port 1 (the device package) is not uniform (largely due to the step in the line from 500 to 1080 mils).

 The current must neck down from the 1080-mil-wide line to 40 mils. A good deal of current is in the form of an excess standing wave, as evidenced by current flowing diagonally back and forth from the device to the two outer corners (see the arrow). The excess standing wave is what is above the normal standing wave, which results from the basic impedance transformation, as shown by a pure transmission line analysis. In a three-dimensional circuit (sometimes called 2.5D) such as this, these are the equivalent of open stubs attached to the main line, which increase the VSWR. The excess standing wave has a large effect on the impedance, as will be shown (also, the losses go up considerably).

In lumped-element LC circuits, the term "circulating current" is used to describe current that is neither present at the input or output, but circulates between the L and the C, having values many times that of the port currents. In this respect, that effect is somewhat analogous to the transmission line network analyzed here".

• How wide can the transformer be and still act as a transmission line with the signal propagating in the desired direction? What effect is there if there are signals traveling perpendicular to the main signal flow, with the outside edges of the line acting as open stubs that are perpendicular to the desired flow? This question is of particular concern if the width of the line is more than a quarter wavelength, as it is in the examples. Simple transmission line theory starts out with the assumption that the conductor widths and spacing are small in relation to the wavelength². However, larger widths can be worked with, especially if the board thickness is small in relation to the wavelength. Finally, it should be remembered that the length of the transformer is less than a quarter wavelength.

The wide step in the literature

Much work has been done on the case of wide steps in microstrip

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Figure 4. Circuit analyzed in the Literature.

lines. Reference 3 summarizes some of this work.

The circuit of Figure 4 shows what is analyzed in the references and shows the lumped-element equivalent model for the transition. In 3, results for the excess capacitance (which apparently is from the fringing of the electric field) are given in the form of graphs, one for a dielectric permitivity ε_r of 2.3 and one for an ε_r of 9.6. The work of several analysts is included over limited regions of operation. The graphs are normalized to the board height h, and include results for W1/h of up to 10:1.

Measurements of the excess capacitance have also been done⁴, although reference 3 notes that there are not enough data to check against more recent calculations. Closed-form expressions for the excess capacitance have been given by⁵, which do not show the capacitance per se but rather the effective line length extension of W1 (extended in the direction of the main current flow), which would result in the proper correction.

Others⁵ have calculated the series inductance shown in Figure 3. The results are summarized in 3, in the form of graphs, with comparison to measurements. As with the excess capacitance, the graphs are normalized to the board height h, and cover the range of W_1/h up to 6:1, for various^B W_2/h .

First, the total inductance is calculated, then it is split up between L_1 and L_2 in proportion to the impedances of the two line sections. The excess inductance effectively reduces the length of the wide part of the line, in contrast to what the excess capacitance does. For the range of examples analyzed in this paper, the inductive effect dominates, and the overall effect of the transition is that the wide part of the line appears shorter electrically than it is physically. However, caution must be used in simplifying the problem to a line-length adjustment.

Overall, the data for calculating the excess capacitance and inductance are



Figure 5. Real part of the input impedance to a wide transmission line that has an abrupt transition to 50Ω.

sketchy and cover a limited range. For the examples here (see Figure 3), the step ratio to the 50Ω portion of the line is roughly 25:1 and is beyond the limits of the graphs in 3. If gross extrapolation (3:1 or more) is attempted from the graphs, in addition to some interpolation (because the excess capacitance is only given for two different permitivities ε_r), values of 240 pH and 0.275 pF are realized at 2 GHz. When inserted into a pure transmission line model, these lumped elements are small, and the results do not come close to what the EM analysis shows.

EM analysis vs. simple analysis

The software is used to calculate the impedances and the current distribution for a range of output matching net-



Figure 6. Imaginary part of the Input Impedance to a wide line that has an abrupt transition to 50Ω (see text for arithmetic sign).

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Figure 7. Method for calculating the current distribution at the input port.

works, for cases where the frequency is 2140 MHz and the board material is R6006 with a permitivity εr of 6.15. The board thickness is 0.025 inches and the microstrip dimensions are varied. Once the problem is set up, changing the dimensions and recomputing takes only seconds.

The cell dimensions were 20×20 mils for the impedance analysis, 40×40 for the current distribution pictures (which show relative current values), and 10×40 mils for calculating the current distribution across the width of the input port. For the latter, a four-cell (40 mil) finger was moved across the width, and this finger was assigned a separate port in parallel with the rest of the input port.

Figures 5 and 6 show the results of calculations for the EM analysis and for the pure transmission-line analysis, for some single-hop matching networks. Normalization of a problem such as this with so many variables is difficult at best. Only a single frequency, board height and permitivity are shown.

Doing a normalization would be useful if taken to the point of nomographs or closed-form expressions. But as seen in the literature, even a single step of 3:1 is difficult to reduce to normalized results. Adding to the difficulty of doing a normalization for this problem is the fact that the currents are not laminar and the line lengths going away from the wide step are not infinite (as is referenced in the literature), but rather shorter than the line width itself. Thus, individual problems should be analyzed with the software.

The line widths and lengths in the figures cover networks that are in the general region of about 0.5 to 20Ω real and 1 to 20Ω imaginary, at the input of



Figure 8. Current distribution across device output tab for a 180-mil-long line.

the network. The matching networks (i.e. wide transformer) are less than 90° in length L, and are terminated in 50 Ω , making them capacitive at their inputs. This is required to complete the conjugate match for devices that have inductive (positive imaginary) phantom output impedances, which is virtually all power devices in this frequency region. Figure 6 shows the negated imaginary part of the input impedance so that it could be plotted on a log axis.

Current distribution

Figure 7 shows how the current distribution across the input to the matching network was calculated. The input port is divided into three units and put



Figure 9. Current distribution across the device output tab for a 300-mil-long line.



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Figure 10. Current distribution when the line width and device tab are equal.

electrically in parallel. The port is driven with a constant voltage source (in general, the convention for EM software is to drive a port with uniform voltage across its width and let the current fall out). Because the current is not uniform across the width, it could almost be said that the impedance of the port is not uniform. However, the current at the various points is highly dependent on that of its neighbors, so there is no independence and the concept of a nonuniform impedance cannot exist. The overall port impedance is calculated the normal way: voltage divided by the total current.

The second port (i_2) is a four-cell wide finger that is moved away from the centerline by an amount d, and the three currents are measured. Four cells widths were used rather than just one or two to avoid any issues of quantization error. In the simulation, small resistors were put in series with each ammeter (not shown) to avoid potential singularity issues (non convergence), although that may not be necessary. The source was +33 dBm with an impedance of 0.01Ω , essentially making it a voltage source^c. Port 2 is loaded with 50Ω .

Figures 8 and 9 show the resulting current distribution for two line lengths L and for four widths W_1 . It can be seen that the current approaches a large value at the edges of the transformer (the current at the extreme edge is not plotted because no matter how small the cells are, there is a quantization issue at the last couple of cells). For widths much more than 800 mils, significant current nonuniformity exists, especially for the case where L is 300 mils. In one sense, it would seem that there would be less of a nonuniformity problem with the longer line because the current has more space to spread out and narrow down again. However, the large currents at the edges are due to the moding (resonance along an axis other than the desired signal flow) described above, where the current circulates back and forth across a diagonal line towards the outer corners.

Also note in Figure 8 the strange nonmonotonicity of the current for the case of the widest line. This was tested for trueness by changing many parameters; it's a real phenomenon, and this reiterates the need to analyze specific problems with an EM method. Figures 8 and 9 have the same scaling on the vertical axis for comparison purposes.

When the current distribution at the actual die of a power device is to be considered, the bond wires have to be added into the analysis, as well as a part of the device lead that extends into the package. Although not shown here, adding these additional parts of the circuit to the analysis showed that the current is more evenly distributed than it is at the device package.

Finally, Figure 10 shows the current distribution when the transformer width is the same as the device tab (500 mils in this case). The line is long enough so that the current funneling effects at the transition to 50Ω are not felt at the device (Port 1). This type of matching network is typical of what might be used in a load pull system.

The effects of the transition from wide to narrow are subtracted out in a TRL or other calibration, so the line length of the wide part is not particularly critical. So, the current at both ports is evenly distributed and laminar. This circuit, however, is not matched to 50 Ω . Its purpose is to get the impedance that the network analyzer sees somewhat closer to 50 Ω (for example 20 Ω), compared to the device itself (in the few ohm region).

Conclusions

Many of the high-power matching networks that are implemented on microstrip are done without full consideration of the effects of the step discontinuities, which include the effects of alternate or inadvertent (e.g. diagonal) moding, current funneling from wide widths into a narrow 50Ω line and uneven current distribution across the tab of the output device. These issues arise when, among other things, the matching transformers are significantly shorter in length than they are in width, and when the line width is a significant portion of the wavelength.

It has been shown that a Smith chart design approach to such networks in the 2 GHz region with typical geometries is completely inadequate and can result in errors in impedance of 3:1 without much difficulty, relative to what might be measured by the vendor using a load-pull system.

The load-pull measurement would normally have equal current distribution across the device tab, flowing out in a more or less laminar fashion. This is because the matching network has a line width equal to that of the tab.

Microstrip matching lines that are wider than the device tab have an effective change in width after the launch, perhaps by factors of 1.5: or 2:1. An uneven distribution can show up at the device die, reducing its P1dB point. A more extensive EM analysis, one that would include the bonding wires inside the device, would show the extent of that problem.

A single-hop match from the device impedance right to 50Ω , with one transformer, has not only the advantage of shorter length, but has a maximum line width that is less than that of a two-hop design. The reduced width is of critical importance for the range of problems analyzed here, even at the expense of reduced bandwidth.

It has also been shown that closedform expressions and/or nomographs are



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Unique inductive feedback LNA design

In first-stage, low-noise amplifiers, optimum noise and optimum return loss performance are often compromised by impedance matching. This load impedance mismatching and inductive feedback design offers some relief.

By David VanStone

First-stage, low-noise amplifier (LNA) designs often require both low-noise and low-input voltage-standing-wave ratios (VSWR). Unfortunately, the source reflection coefficient required for an input conjugate match ($\Gamma_{\rm M}$) and the source reflection coefficient required for minimum noise ($\Gamma_{\rm OPT}$)



Figure 1. A plot of the input impedance of the simulated amplifier and the source-reflection coefficient required for an input conjugate match.

are rarely equal. As a result, the designer is faced with having to find a compromise input match that sacrifices both optimum noise and optimum input return-loss performance. However, for most field-effect transistors (FETs) and bipolar junction transistors (BJTs), there is a combination of source inductance and load reflection coefficient that will produce $\Gamma_{OPT} - \Gamma_{M}$ coincidence. Under this condition, an amplifier can be designed that exhibits minimum noise and minimum reflected power at the input.

But this desirable condition extracts a price by presenting a poor match at the output and achieving lower power gain. However, the designer can transform the load into reflection coefficients somewhere between those producing optimum noise figure and those producing a simultaneous conjugate match and, thereby, achieve an acceptable compromise between noise figure, gain and output return loss. This article will discuss how combining a series inductive feedback with a unique, load-reflection coefficient can produce an amplifier with improved noise figure and input-matching performance compared to that produced by traditional design techniques.

The use of either emitter or source inductance feedback to increase the input resistance and increase the k-factor of a bipolar or field-effect transistor is well documented. Refer to references 1 to 3 for thorough theoretical and practical coverage of this technique. However, for convenience, a cursory review of theory and practice follows.

Background: series inductive feedback

A small amount of inductance, in series with the emitter or source, has three predominant effects:

- Increased input resistance
- Increased in-band k-factor (increased in-band stability)
- Decreased gain

Secondary effects include changes to input reactance and small shifts to Γ_{OPT} . Typically, the inductance is inserted by grounding the transistor through a short length of transmission line. The inductive reactance of the stubs is usually no greater than 10 Ω and line lengths are typically 0.1" or less with characteristic impedances of 50 Ω or greater. This kind of lossless feedback (assuming an ideal inductor) has no effect on the minimum noise figure of the device. Because it increases input resistance, source inductance usually moves the reflection coefficient required for an input conjugate match closer to Γ_{OPT} .

To illustrate the effects of source inductance, a pseudomorphic, high-electron-mobility transistor (PHEMT) amplifier (using an advanced Curtis quadratic model) was simulated with different amounts of source inductance. Figure 1 plots the input impedance (points 2 through 6) and the source reflection coefficient required for an input conjugate match ($\Gamma_{\rm M}$, points 7 through 10) as a function of source inductance. Constant-noise figure circles are also plotted; the 0.43 dB noise figure circle is labeled N_1 and the minimum noise figure ($F_{\rm MIN}$) is 0.42 dB. As the source trace length increases, corresponding to increased source inductance, $\Gamma_{\rm M}$ moves closer to $\Gamma_{\rm OPT}$ (located at the center of circle N_1).

As the source inductance is increased, the k-factor

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Inductor length (inches) $(Z_0 = 50\Omega)$	Inductance (nH)	Z _{in}	$\Gamma_{\rm S}$ for simultaneous conjugate match	Noise figure circle
0.0	0	point 2	no match point, $k < 1$	n/a
0.025	0.22	point 3	point 7	N5, 1.2 dB
0.05	0.44	point 4	point 8	N4, 0.72 dB
0.075	0.66	point 5	point 9	N3, 0.58 dB
0.100	0.88	point 6	point 10	N2, 0.52 dB

Data table for Figure 1.

at higher frequencies eventually falls below 1. This effect limits the amount of source inductance that can safely be used. In Figure 2, the k-factor of the simulated amplifier is plotted for source inductance values of 0 nH to 0.44 nH.



Figure 2. *K*-factor plots for source inductance values of 0 to 0.44 nH. Inductor lengths vary from 0 to 100 mils in 25 mil steps.

Design Example 1

An LNA was designed for the 1710 MHz to 1785 MHz band with both ports matched (simultaneous conjugate match). In order to produce a k-factor of 1 or greater at all frequencies, a source inductance value of 0.25 nH was used together with a 51 Ω resistor at the output, grounded through a quarter-wave shorted-stub at 1745 MHz (see Figure 3). The simulation yielded the following results at midband:

Gain: 18.3 dB Input return loss: 27 dB Output return loss: 23.1 dB Noise figure: 0.91 dB Stability: unconditional at all frequencies

The amplifier has respectable performance, but the noise figure is nearly 0.5 dB greater than F_{MIN} , which is 0.42 dB. A technique for achieving both minimum noise figure and high-input return loss is developed in the next section.

Background: load impedance tuning

The basis of the technique is the interaction between the load reflection coefficient and the input reflection coefficient of an amplifier. This relationship is expressed in the following equation:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{1}$$

If a value of $\Gamma_{\rm L}$ can be found that will make $\Gamma_{\rm IN} = \Gamma^*_{\rm OPT}$, or equivalently $\Gamma_{\rm M} =$ $\Gamma_{\rm OPT}$, then a minimum noise-figure match and a conjugate match can be obtained simultaneously. (Recall that $\Gamma_{\rm M} = \Gamma_{\rm IN}^*$.) For some sets of S parameters, no value of $\Gamma_{\rm L} \leq 1$ exists that will produce this condition. In these cases, the S parameters can be modified by using an appropriate amount of seriesinductive feedback. A value of $\Gamma_{\rm L}$ that is ≤ 1 can usually be found using S parameters of a transistor that has been stabilized using source inductance.

A MATLAB program was written that will find the load-reflection coefficient (if one exists) that will make $\Gamma_{\rm M} = \Gamma_{\rm OPT}$ for a given set of S-parameters. The program is listed in Appendix A (see page 82).

Before running the MATLAB program, it may be best to determine how much source inductance, if any, is required to produce $\Gamma_{\rm M} = \Gamma_{\rm OPT}$. This can be determined by mapping the Γ_L plane onto the Γ_{IN} plane. Mapping capability is included in most simulation programs, but a simple mapping program can be readily written. It should map the unit circle of the Γ_L plane (Γ from 1 $\angle 0^{\circ}$ to 1 \angle 360°) to the $\Gamma_{\rm IN}$ plane using equation 1 and the S- parameters for the amplifier configuration under study. The image of the unit circle will usually be a smaller circle on the Γ_{IN} plane. This circle, which may extend beyond the perimeters of the conventional Smith chart, must enclose Γ_{OPT}^* for the condition $\Gamma_M = \Gamma_{OPT}$ to occur with a passive load impedance, $\Gamma_L \leq 1$. Figure 4 shows plots of four Γ_L -to- Γ_{IN} mappings using values of source inductance from 0 to 0.44 nH. For the PHEMT device under study, a source inductance of at least



Figure 3. (a) K-factor plot of stabilized PHEMT amplifier and (b) basic stabilized amplifier topology.

0.1 nH is required to produce $\Gamma_M = \Gamma_{OPT}$ with a $\Gamma_L \leq 1$.

Design example 2

The second design example will use the MATLAB program to help design an LNA with a minimum noise figure match and minimum reflected power at the input (conjugate match).

The same PHEMT is used as in the first example, with the same amount of source inductance and the same stabilizing network at the output. The S parameters of this network are found using the simulation program. These parameters, along with the value for Γ_{OPT} , are input to the MATLAB program. The program then finds a value for Γ_L of $0.34 \ensuremath{\angle} - 143^\circ$. When this load impedance is presented to the output of the amplifier, Γ_M will be equal to $0.27 \ensuremath{\angle} 116^\circ$, which is Γ_{OPT} for this device at this frequency.

Impedance-transforming networks were designed and the amplifier was simulated. The simulation yielded the following results at midband:

Gain: 16.5 dB



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Figure 4. Unit circles mapped from the $\Gamma_{\!L}$ plane to the $\Gamma_{\!N}$ plane.

Input return loss: 30.3 dB Output return loss: 6.6 dB Noise figure: 0.51 dB Stability: unconditional at all frequencies

When we compare these results to those of the first example, we note the following changes to the amplifier's performance:

1.8 dB reduction in gain 0.4 dB improvement in noise figure Output return loss degraded by > 16 dB

The design trades off gain and output return loss for improved noise-figure performance. If the insertion-loss of the input noise-matching network is kept low by using low-loss components, this technique allows the designer to attain an amplifier noise figure close to F_{min} .

If the sacrifice of gain and output match using this technique is unacceptable, a "compromise" between the minimum noise technique and the simultaneous-match technique can be found. This involves plotting both the loadreflection coefficient required for a simultaneous conjugate match and the load-reflection coefficient required for $\Gamma_{OPT} - \Gamma_{M}$ coincidence on the same Smith chart. A straight line (see Figure 4) connects the two points.

Now, pick a value for Γ_L along this line and, using equation 2, find the source-reflection coefficient required for

a conjugate input match (Γ_{M}).

$$\Gamma_{M} = \left[S_{11} + \frac{S_{12}S_{21}\Gamma_{L}}{1 - S_{22}\Gamma_{L}} \right]$$
(2)

As the load reflection coefficient moves from point 1 to point 2, gain and output return loss will improve as noise figure degrades. By trial-anderror, a Γ_L will eventually be found that produces an acceptable compromise between gain, noise figure and output return loss.

Design example 3

An amplifier was designed using this technique, again using the same PHEMT with the same amount of source inductance and the stabilizing network as in the first two examples. The load-reflection coefficient that produces $\Gamma_{OPT} - \Gamma_M$ coincidence and the load-reflection coefficient for a simultaneous conjugate match are plotted as shown in Figure 4. A load-reflection coefficient of $0.21 \angle 102^{\circ}$ (point 3 on Fig. 5) was eventually tried that, by using equation 2, yielded a Γ_M of $0.46 \angle$



Figure 5. Point 1 is the load-reflection coefficient that produces $\Gamma_{\text{OPT}} - \Gamma_{\text{M}}$ coincidence. Point 2 is the load-reflection coefficient for a simultaneous conjugate match. Γ_{L} (point 3) is a compromise load-reflection coefficient, 0.21 \angle 102°.


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For sales or technical support, contact **336.678.5570** or **callcenter@rfmd.com**. Visit us at CTIA Wireless 2002 Booth # 2873 143°. The simulation yielded the following results at midband:

Gain: 17.9 dB Input return loss: 23 dB Output return loss: 11.6 dB Noise figure: 0.66 dB Stability: unconditional at all frequencies

Compared to Example 1, there is only 0.3 dB lower gain and a 3 dB difference in input return loss. The output return loss of 11.6 dB was deemed by the author as an acceptable compromise in obtaining a noise figure of 0.66 dB, an improvement of 0.25 dB over Example 1.

Conclusion

This article has presented a method for obtaining the optimum noise figure



from an amplifying device while also achieving an excellent input match. The method requires a good computer simulation program, a Smith chart and the simple MATLAB program written by the author. This technique will find an application anytime a designer needs to squeeze out the last bit of noise performance from a transistor amplifier that is preceded by a device requiring a good termination.

RF

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About the author

David VanStone works at Motorola's GTSS Wireless Systems Group as an RF Design Engineer. He designs and develops low-noise front ends for base station receivers. His previous experience includes designing microwave synthesizers and low-noise crystal oscillators. He holds a B.S.E.E. from Illinois Institute of Technology. He can be reached at 847.632.5829 or by e-mail at dvansto1@email.mot.com

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The changing landscape of RF and fiber optics

A preview of what technologies, techniques and materials tomorrow's wireless designer will need to support frequencies well into the EHF spectrum.

By Dwight Streit

he explosion of broadband and wireless telecommunications is driving a move to the use of ever-higher frequencies and operating speeds. In the wired world, OEMs are racing to develop the next generation of fiber optic (FO) equipment that will operate at 40 Gb/s and provide the infrastructure for bringing the cost-effective bandwidth needed for streaming video, full-duplex video conferencing and other multimedia applications. In the wireless arena, broadband systems have been operating in the Ka band (20 to 30 GHz) frequencies and higher. Now V and W bands (60 GHz and beyond), previously the sole domain of military communications applications, are emerging as commercial alternatives.



Figure 1 Electron velocity as a function of electric field for Si, GaAs, and InP materials. The InP material family offers the highest mobility for both low and high fields.

The wider bandwidths and demanding requirements on jitter, delivered voltage and power dissipation of these new circuits create a challenging design environment for RF designers. Ultimate solutions will require the designer to understand and use a number of new technologies and techniques, including new material systems such as Indium phosphide (InP) and silicon-germanium (SiGe), higher levels of circuit integration and new packaging and testing regimens. Perhaps most importantly, designers will need to understand the strong interaction among material choice, chip design, and packaging effects and their combined impact on overall product performance.

RF performance challenges facing the designers of tomorrow's high-speed circuits are beyond the capabilities of silicon, the most commonly used semiconductor material in today's communications applications. Next-generation devices will most likely be based on a range of compound semiconductor materials, among them SiGe, gallium arsenide (GaAs), and InP. Each material system offers advantages and disadvantages to the RF device designer.

First up – SiGe

SiGe is a silicon derivative in which a SiGe alloy is used to improve carrier transport in the base of standard silicon bipolar transistors. This lowers the base resistance and improves the base transit time of the transistor. And it ultimately improves the frequency performance when compared to standard silicon devices of the same geometry. Therefore, much of the circuit complexity and fabrication cost structure of silicon can be extended to higher frequency components. SiGe achieves high frequency performance by feature size reduction, increasing internal fields and current density, and significantly lowering breakdown voltage. As a result, SiGe operating voltages are typically limited to 1 VDC or less for applications above 30 GHz - a challenge for any RF system designer.

It is a particularly serious limitation for optoelectronic interfaces such as modulator drivers where voltages in excess of 5 VDC are required to drive even moderate lithium niobate modulators.

And, while improvements in process technology continue to shrink SiGe transistor geometries and raise their cutoff frequency (f_T) specifications, there appear to be fundamental physical limitations as to how far this technology can be extended. Current SiGe processes limit effective operating frequencies somewhere in the range of 30 to 40 GHz, a problem for 40 Gb/s transmission systems using RZ modulation or forward error-correction (FEC) bandwidth overhead.

Let's move on to GaAs

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GaAs heterojunction bipolar transistors (HBTs) are the standard for power amplifiers in today's cell phones, while GaAs high-electron mobility

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transistors (HEMTs) are the standard for Ka-band power amplifiers in cellular infrastructures.

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As shown in Figure 1, InGaAs lattice matched to InP is used to improve low field transport due to its small electron effective mass. Although InP has a somewhat higher electron effective mass, its conduction band structure provides higher electron velocities at much higher fields compared to GaAs and InGaAs. As a consequence, using InP in high field regions of the device profile can significantly improve device performance.

One of the critical design parameters for HBTs in GaAs and InP is turn-on voltage (see Figure 2). The 0.67 eV bandgap of InGaAs base in InP HBTs offers inherently lower turn-on voltage specifications than equivalent GaAs



Figure 2. InP's lower turn-on voltage offers advantages to the RF designer.

devices. Such low turn-on voltages allow for increased efficiency of operation for power amplifiers, which helps lower power dissipation. While not critical for fiber optic applications, lower turn-on also lowers the battery voltage requirements (hence, extends the operating time) for handheld wireless applications.

In terms of breakdown voltage, both GaAs and InP have significant advantages over SiGe (see Figure 3). GaAs can have a 10 to 12 VDC breakdown



Figure 3. InP has significantly higher breakdown voltage as a function of cutoff frequency than either GaAs or SiGe.

voltage at cutoff frequencies below 50 GHz. This has been an ideal characteristic for power amplifiers and highspeed digital circuits used in today's RF systems and products, but more leeway will be required for tomorrow's devices. An InP HBT with a single base-emitter heterojunction offers slightly better breakdown characteristics. But an InP double heterojunction HBT with an InP collector achieves the highest breakdown specifications for any bipolar transistor technology for cutoff frequencies in excess of 160 GHz. This characteristic will be a key performance enabler in advanced high-efficiency amplifiers, as well as microwave and digital circuits for fiber-optic applications.

Finally, InP is the only semiconductor material system for optical components that detect or emit light at the 1.3 to 1.5 micron wavelength characteristic of most telecommunications fiber optic systems. As a result, InP HBTs can be constructed with integral PIN photodiodes, lasers and modulators. This property will ultimately facilitate the fabrication of monolithic singlechip, FO subsystems (such as receivers or transceivers) to power the fiber backbone at 40 or even 80 Gb/s. Because assembly and packaging typically comprise 60 to 80% of the cost of current semiconductor optoelectronic devices, monolithic transceivers offer the possibility of substantial cost reduction for tomorrow's high-speed infrastructure.

Circuit and component integration

Twenty-first- century RF designers are working to build a complete 40 Gb/s OE receiver — including a photodiode, a transimpedance amplifier (TIA) and a limiting amplifier — on a single chip using InP. In effect, they are being challenged to employ all the rules of millimeterwave design while wearing the hat of an analog designer. Ultimately, this will involve forwardthinking testing methodology and packaging strategy so that customers are provided with features that make the module assembly and testing easier.

But such circuit integration also requires the designer to be skilled in analog, digital and mixed-signal techniques. Modulation of the signal onto the optical carrier in a FO application is inherently analog in nature, with an analog signal being converted from digital at the transmitter and back to digital at the receiver. As a consequence, RF components are on both sides of the link that requires mixed signal design. The laser or modulator driver must take low-level signals and linearly amplify them with minimal distortion. The photoreceiver generally uses a limiting amplifier to "square up" the received analog signal before it is handed off to a clock and data recovery chip. InP is particularly well-suited for these mixed-signal applications because of its high breakdown voltage, bandwidth and transistor threshold uniformity.

Optical front-end components will require 3 dB bandwidths approaching 48 GHz, noise density of less than 12 $pA/(Hz)^{1/2}$, and output voltages of 0.5 VDC peak-to-peak. For modulator drivers, the specifications are even more stringent, and include bandwidths of greater than 48 GHz, output voltages greater than 3V peak-to-peak, and rise times of less than 7 ps. To round out the challenges, in some configurations



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New InP designs and solutions

The performance challenges facing designers of advanced fiber optic circuits for operation at 40 Gb/s and



Figure 4. New processing techniques reduce parasitic capacitance and extend cutoff frequency.

above are significant. The impact of parasitic capacitance on the overall electrical impedance within the circuits at these operating frequencies can significantly affect overall device performance and efficiency.

For instance, reducing the parasitic capacitance of the base-collector junction in an InP HBT can significantly increase the cutoff frequency (f_T) of the transistor and improve high-speed digital performance. To address this, a technique was developed for minimizing this capacitance. This technique uses undercut etch techniques to essentially create a cantilevered base profile that is uniform across the entire device and wafer (see Figure 4). Increasing the undercut actually increases f_T by as much as 30 GHz in a device originally designed with a cutoff frequency of 165 GHz.

The ripple effect

New circuits for power amplification face similar challenges. Here, providing higher bandwidth is directly linked to delivering outstanding linearity and improved noise-rejection characteristics. Using the improved turn-on characteristics offered by an InP HBT with a specially tailored InP collector has already provided a device for microwave applications with an f_T of 80 GHz or better at 70kA/cm² with B_{veeo} > 18 VDC. This is far beyond the capabilities of available GaAs devices and more than sufficient for Ka-band power amplifier applications.

New circuits for implementing onchip photo-detectors are also becoming available for FO applications. For example, a typical design would integrate an InP SHBT with an InGaAs collector to serve as a PIN diode with a wideband InP HBT distributed transimpedance amplifier. This offers an attractive trade-off between performance and packaging challenges as well as a lower cost solution for 40 Gb/s fiber optic applications (see Figures 5 and 6). Such a monolithic photoreceiver provides a bandwidth of 47 GHz with a 38 dB- Ω transimpedance.

Packaging

Packaging of the new generation of high-speed devices can become a challenge both in terms of power dissipation of the die and additional parasitics introduced by lead frames and interconnects. In general, the designer must pay careful attention to package layout to reduce chip interconnect inductance and control package-induced resonances. Thermal management, particularly in packages that contain optical components, is a significant design constraint as well.



Figure 5. A 40 Gb/s integrated InP SHBT photoreceiver die.

InP devices are much more efficient than their GaAs equivalents and exhibit a smaller die size for similar power ratings. The improved efficiency does reduce the total thermal load, but because of the smaller die size, the packaging designer still must frequently deal with significant thermal fluxes through the footprint of the chip. Compounding this problem is the fact that smaller feature size for InP functions leads designers down the path of integrating more functions on a single die, which can increase thermal dissipation problems. More challenging than thermal management is the RF performance of the packaged part. Skill in electromagnetic modeling simulation software is mandatory for optimizing performance because of the interaction of the package, chips and chip interconnects.

For example, to optimize high-speed interconnects, inductive parasitics must be minimized. This is addressed by minimizing the length of the interconnect (a layout problem) and sizing the interconnect appropriately. Multiple wire bonds or ribbon bonds are used because a larger surface area reduces inductance.

Capacitive compensation structures may also be added near the bonds to further reduce inductance. This all must be accomplished in a package that accommodates low-cost assembly techniques while eliminating or controlling cavity modes that can mar the performance of an otherwise great die.

Furthermore, while reducing interconnect inductance and package cavity modes drives designers to smaller sizes, these are not the only factor for consideration.

In wideband and RF amplifier circuits, it becomes essential to decouple the device from the power used to drive it. Standard on-chip capacitors are not large enough to meet the requirements at the low-frequency (kHz) end of the frequency band, so the use of a discrete, wideband blocking capacitor is desired between amplifier gain stages. A similar blocking capacitor is combined with an inductor to create a "T," which is used for DC inputs.

Present practice calls for using a discrete "bias T" at each DC input, which is both size- and cost-prohibitive. Here, the designer has to develop techniques that incorporate this decoupling circuit within the package to make advanced component solutions more economically viable (see Figure 7).

Circuit testing

Testing of monolithic microwave integrated circuits (MMICs) operating at their highest limits of performance poses unique challenges to RF designers and requires that designers work closely with test engineers. Today, commercially available instruments are just becoming available to handle circuits switching at 40 GHz, and the rise and fall times embodied in many InP devices are often faster than that of the test equipment. To directly measure

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Figure 6. Frequency response of a monolithically integrated InP SHBT PIN photodiode-TIA.

rise and fall times, one needs test equipment with rise and fall times at least four times faster than the device under test to measure the actual rise/fall with negligible test equipment contribution. This implies one would need test equipment with 2 ps rise/fall times to test devices that achieve 8 ps rise/fall times.

One useful technique in testing advanced devices compares the resultant waveforms with the original stimuli and, in effect, backs out the measurement to confirm proper operation. This process of backing out the value via the root sum square (DRSS) is currently the easiest way to approximate the rise/fall times in the time domain. Such an environment





Figure 7. Inductors required for high-speed components are often the driver in package sizing. Shown is a modulator driver die next to a conical inductor.

is not unlike that found when analyzing several filters operating in series. It presents accurate results of device operation, particularly as experience grows.

In addition to rise/fall times, jitter is an issue at 40 GHz where a resolution of 1 ps RMS is equivalent to 6 ps peak-topeak (6 sigma), which is more than 20% of the bit period. This jitter error, introduced by the test instrument, must be compensated for to obtain the true measured jitter of the device under test.

Conclusion

As 21st century technology develops, the interaction between the market pull for new applications and the technology push of new materials and capabilities is somewhat like the old railroad handcar, with the RF designer at the fulcrum between the two handles. RF designers must respond to both the customer-driven requirements for performance and the host of technology-driven choices in processes and materials available to meet those requirements, meshing them smoothly if the handcar is to advance.

RF

About the author

Dwight C. Streit, Ph.D., is president of Velocium, a TRW company. Prior to his role with Velocium, Streit was vice president and executive director, advanced semiconductors, for TRW Space and Electronics. Previously, he served as director of the telecommunication products organization within TRW's telecommunication programs division, where he was responsible for managing development and production of telecommunication products for commercial applications. He earned a bachelor's degree in electrical engineering and chemistry from California State University, Los Angeles before earning a master's degree and a doctorate in electrical engineering from the University of California, Los Angeles. He is a recipient of six TRW Chairman's Awards for Innovation, four distinguished patent awards and 12 TRW IR&D roll of honor awards. He has published more than 300 technical papers and has more than 20 patents issued or pending. He is a member of the National Academy of Engineering and a fellow of the Institute of Electrical and **Electronics Engineers.**



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Designing an RFIC CMOS upconversion mixer

Software to help the engineer design and implement a CMOS mixer on an RFIC platform issues, tradeoffs and solutions.

By Stephen Long

Designing a mixer to work within a radio frequency integrated circuit (RFIC) is challenging. Differing performance specifications must be prioritized based on the application. Some specifications are for receive applications with a wide range of input signal levels where maximum linearity under large signal conditions is often more critical than the noise figure.

On the other hand, for transmit applications where the signal levels can be controlled, the design strategy shifts to tradeoffs between noise and intermodulation distortion (IMD) behavior to achieve the largest useable dynamic range.

In this discussion, a transmit mixer is used to illustrate many of the tasks required to design a quality RFIC. The application is an upconversion mixer intended for a base station transmitter power amplifier section (Figure 1). The design is based on a Gilbert-cell, metal-oxide semiconductor field-



Figure 1. The upconversion mixer for the base-station transmitter power amplifier application.

effect transistor (MOSFET), double-balanced differential mixer with an input IF signal centered at 200 MHz and an output of 1.8 GHz. The example uses 0.35 mm MOSFETs with a default devicemodel parameter set. For other applications, the appropriate verified model would be substituted.

In this example, the intrinsic mixer performance was evaluated. The design was then modified to improve conversion gain and image rejection by tuning the mixer output. Finally, a differential-tosingle-ended converter was added to provide the proper interface to an off-chip bandpass filter.

The Gilbert cell mixer

Figure 2 shows a MOSFET version of the device. The lower FET differential pair serves as a transconductance amplifier, while the upper FETs provide a fully balanced, phase-reversing current switch. A DC bias generator (not shown) keeps the MOSFETs in their active region.

The large signal-handling capability of the mixer depends mainly on the linearity of the transconductance amplifier. This is measured by determining the maximum input voltage, V_{1dB} , that causes a 1 dB compression in the conversion gain (in some cases, use power, P_{1dB}). The maximum linear input voltage range can be increased by increasing the values of the source-degeneration resistors (R_s). Additionally, source inductance can also provide beneficial degeneration, but only with a low-input IF frequency of 200 MHz. In such a case, however, the required inductance values would be too large for RFIC implementation and resistors must be used, even though they add noise.

The load resistors could also cause gain compression if the voltage swing at the drains is large enough to cause the output to clip under large-signal drive conditions. The double-balanced design rejects IF and LO feedthrough to the output (as long as the output is taken differentially) because the LO component at the output is a common-mode signal and the RF output is differential.

Design sequence

A mixer used for base station transmit applications requires high linearity and low noise to minimize the amount of spurious power spread into adjacent channels. The performance of this example mixer was optimized in the following sequence:

1. Determination of LO amplitude. The mixer commutating switch must be fully activated, as excess distortion can be produced with a weak-conducting or slowly activated switch. The conversion transducer gain and 1 dB gain compression input level were used to determine when the LO voltage was sufficient.

2. Evaluation of the influence of source and drain resistance on the 1 dB compression level, giving insight into the principal mechanisms that limit linearity.

3. Determination of how the added noise of the mixer affects the minimum signal level, thus limiting dynamic range. This is necessary to evaluate the tradeoffs between noise, gain and gain compression.

4. Evaluation of how the two-tone, third-order IMD power and the noise figure affect the mixer dynamic range relative to the input voltage. Because the designer has control over the input voltage in transmit applications, the optimum dynamic range - the mixer's "sweet spot" for best performance must be determined. If a fixed signal level is specified, the mixer must be designed to provide the best

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Figure 2. The MOSFET Gilbert-cell active doublebalanced mixer.

dynamic range at that signal level.

5. Finally, testing the mixer under a realistic signal input, such as a CDMA source, to emulate a multicarrier environment. This is a more severe test than the two-tone IMD. It is also much more time consuming to simulate because a large number of symbols must be used for accurate results.

Once the basic resistively loaded Gilbert cell mixer was characterized, two modifications were used to improve performance. First, the mixer drain nodes were tuned with inductors and a capacitor for resonance at the output frequency. This improves conversion gain if inductors with reasonable Q can be fabricated. It also decreases the amplitude of the undesired output image signal because of its bandpass transfer function. The image must be removed anyway, and its presence can only degrade the distortion of the output stage by increasing the peak voltage present at its input.

The other change was to convert the differential signal to single-ended. Because the output of the mixer must be filtered off-chip with a surface acoustic wave (SAW) filter before further amplification, a single-ended output is more efficient. The circuit must have good common-mode rejection to suppress LO feedthrough and good linearity so that it doesn't degrade dynamic range.

Determining LO voltage

Once the topology was established, the first step in designing this mixer was to determine a suitable LO voltage. The LO level should provide a reasonable compromise between conversion gain and LO power but should not limit the 1 dB gain-compression input voltage. The MOSFETs forming the commutating switch (upper level) must be driven hard enough to present a low series resistance to the load. An LO power sweep and an N dB gain compression analysis can be used to evaluate the dependence of gain compression on the LO drive.



Figure 3. Differential mixer simulation setup.

The simulation setup for the initial mixer design is shown in Figure 3. For simplicity, the mixer is implemented as a sub-network. As such, the mixer itself can be replaced or modified as necessary throughout the design process while maintaining the basic simulation setup. Mixer parameters are accessible outside the sub-network and are passed to the mixer design for analysis. In this example, drain voltage (V_{DD}), drain resistance (R_D), current-source control width (Wcsp), transconductance and switch MOSFET widths $(W_1 \text{ and } W_2)$, source-degeneration resistance (R_s) , and source-degeneration inductance (L_s) are all available for parameter sweeps.

The simulations showed that the input power at which gain compresses by 1 dB (P_{1dB}) does not have a strong dependence on LO voltage, but conversion gain does depend somewhat on LO voltage (Figure 4). As more gate voltage is applied to the upper pair of



MOSFETs, their series resistance becomes lower relative to the drain resistance and, thus, the conversion gain is higher. A conversion loss worsened at the higher output RF frequency of 1.8 GHz, but this could be improved by tuning the RF output of the mixer.

Gain compression evaluation

Next, gain compression was evaluated. The 1 dB gain compression input power and input voltage were found for a range of swept parameters. For this example, we wanted to know the influence of $R_{\rm S}$ and $R_{\rm D}$ on $V_{\rm 1dB}.$ The $R_{\rm S}$ sweep used an $R_{\rm D}$ of 100 $\Omega,$ and the $R_{\rm D}$ sweep set used an $R_{\rm S}$ of 30 $\Omega.$ Conversion gain was measured at the 1 dB compressed level.

 V_{1dB} , rather than P_{1dB} , is used as the input signal level parameter. In an RFIC mixer, where the input might not be matched to a source impedance, the input voltage is a more important metric of gain compression than the input power because available power assumes a conjugate match between source and load. Also, in a multisignal environment, the peak input voltage can be quite large at the instant in time when all signals add in phase. It is this peak voltage that determines the distortion limits of the mixer. For example, two-tone IMD simulations predicted a 1 dB compression power that was 6 dB lower than predict-

LO Power dBm	LO voltage @LO freq	1.0 dB gain compression input power level (dBm)	Conversion gain
0.000	0.589 / -22.529	-6.825	-9.721
2.000	0.743 / -21.791	-6.891	-9.305
4.000	0.938 / -21.168	-6.924	-8.993
6.000	1.182 / -20.657	-6.957	-8.753

Figure 4. Simulations showing the effects of LO voltage on the input power at which gain compresses by 1 dB, and conversion gain.



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Figure 5. The effects of input voltage on dynamic range.

ed by single-tone simulations because the peak voltage was twice as high for the same power per tone.

It is also noteworthy that the conversion power gain varies inversely with the value of RD. In the simulation, the external load resistance was set to $2R_D$ so that the output power (power absorbed by the load) was also the available output power, $P_{out} = V_{out2}/R_D$. The voltage gain would be expected to follow R_D/R_S , but increased less rapidly than anticipated, probably due to the output RC time-constant bandwidth limitations.

Determining noise tradeoffs

The next step was to evaluate how DC bias current (I_bias) and source resistance affect the mixer noise figure. The mixer's single-sideband noise figure (SSB NF) was simulated as a function of DC bias current through the Gilbert cell (mixer core). The DC current was varied by sweeping the width of the PMOS current source (W_{csp}) and the mixer current mirror width (W_{cs}) using a parameter sweep.

The SSB NF was appropriate because only one input frequency was applied to the mixer, but wideband noise at the image frequency and from LO harmonics was included in the signal-to-noise calculation. The simulation showed that the NF was reduced with increasing I_bias, but reached a point of diminishing returns. Thus, a width of 50 μ m for the current source was selected as a compromise between power and noise.

The SSB NF was also found to strongly depend on the source resistance. This was expected because the thermal noise contributed by the resistor is directly in the input voltage loop of the differential pair. Thus, there needs to be a tradeoff between V_{1dB} and NF to obtain the largest dynamic range of the mixer.

The carrier-to-noise ratio limits the

dynamic range at low input signal power levels. The noise power for a minimum detectable signal (S/N = 1) depends on both NF and the noise bandwidth. This bandwidth is normally set by an external SAW filter between the mixer and the driver amplifier. The filter is also required to reject the output difference ($F_{LO} - F_{in}$) image frequency at 1.4 GHz.

The conversion gain (or loss in this case) may also increase the noise figure because the drain resistor's thermal noise is input-referred through the gain. If the design goals require it, a tuned output should be investigated to eliminate some of this noise.

At higher input signal levels, the dynamic range of the mixer is limited by distortion. The third-order IMD products are the most damaging because they show up in-band and cannot be rejected by the filter. A two-tone, third-order IMD simulation with an RF power sweep was used to display the carrier-to-IMD power ratio. The IMD power present in the output increases at three times the rate of increase of input power. Thus, the difference between output power and IMD power shrinks with increasing input.

Dynamic range vs. input voltage

Determining the effect of input voltage on dynamic range required the output from two simulations: IMD RF power sweep and the SSB NF (see Figure 5). The dynamic range is controlled by the least of these two conditions (see Table 1):

Rs	D _R (dB)	V _{in} (V) (differential)	NF (dB)		
10	57.7	0.017	6.5		
20	57.3	0.025	8		
30	56.4	0.031	9.2		
40	56.0	0.039	10.3		

Table 1. Dynamic range vs. input voltage.



Figure 6. The differential amplifier stage used to the differential output to single-ended.

• $DR = P_{out} (dBm) - MDS (dBm)$ (noiselimited for low input levels). • $DR = P_{out} (dBm) - P_{IMD} (dBm)$ (distortion-limited for higher input levels).

The dynamic range peak depends on the noise bandwidth. For narrower bandwidths, the noise floor drops and the peak D_R increases but shifts to lower differential input voltage.

Because of the base-station application, where the transmitter should be capable of covering an entire frequency band, a 30 MHz noise bandwidth was chosen.

Tuning mixer drain nodes

The low conversion gain of the resistively loaded mixer caused higher noise due to the drain resistors. By resonating the output at 1.8 GHz, the conversion gain was increased and the gain at the image (1.4 GHz) was reduced. A comparison between the resistively loaded case and the tuned case showed an increase in conversion gain of about 3.5 dB.

To find the resonant frequency of a specific design, perform an RF frequency sweep. From that, it is possible to calculate how much capacitance is contributed by the drain-to-substrate junction and absorb it into the resonator.

Gain reduction due to inductor Q

In bulk silicon processes, on-chip inductor Q is limited by metal losses and substrate conduction. An ordinary digital IC process produces low Q in spiral inductors. CMOS or BiCMOS RFIC processes can achieve higher Q inductors by using thicker dielectrics and thicker metal. Q values in the range of 5 to 15 are typical.

Unfortunately, for realistic unloaded inductor Q values on the order of 5, the benefits of tuned output are diminished.



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Figure 8. A single-ended mixer modified to evaluate the designed mixer.

Figure 7. Noise figure and conversion gain contours.

The conversion gain is improved by about 4 dB, but the noise figure is improved by only 0.5 dB. A tuned output would be of greater benefit on a CMOS RF analog, silicon-on-insulator (SOI), or gallium-arsenide (GaAs) process, where higher Q values can be obtained.

Differential-to-S-E conversion

Bidirectional

INTEGRATION

The next step in the design was to convert the RF output from differential to single-ended with an active balun. Rather than taking one output from the mixer, this conversion is required to maintain a differential output, which is necessary for rejection of LO feedthrough. A single-ended output is sufficient to drive the SAW filter that is needed between the mixer output and the driver stage. Although passive baluns can be made for 1.8 GHz frequency devices, placing an active balun on-chip provides cost and size benefits.

The differential amplifier stage shown in Figure 6 converts the differential output of the tuned mixer to a single-ended output. The gate capacitances of the differential-to-single-ended (D2SE) stage can be absorbed into the resonator at the mixer drain nodes. Also, the D2SE stage must be designed so that it does not dominate the IMD generation of the mixer. R D2SE can be adjusted to set the V_{1dB} level.

The output driver can use an off-chip load resistance with an open-drain output connection, as suggested by Figure 6. The load resistance would then be determined either by the filter impedance or by a transmission line impedance, which would then dictate the bias current for the D2SE converter stage. The device widths must also be chosen so that they can handle the necessary drain current and provide adequate

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Figure 9. The dynamic range peak at 57.5 dB is obtained at a input level of 14 mV.

voltage gain. The addition of a source follower to the output is another option.

Design evaluation

For the initial design evaluation, it was easier to measure the differential output so that tradeoffs and comparisons could be made between the differential tuned mixer and the mixer with an output buffer. Once the design was complete, the mixer could then be evaluated in a single-ended configuration.

The SSB NF simulation was performed again with parameter sweeps for $R_{\rm S}$ and $R_{\rm ind}.$ Figure 7 shows that there is little noise sensitivity to $R_{\rm ind};$ however, it strongly affects the conversion gain. $R_{\rm S}$ affects both NF and conversion gain as well as the carrier-toIMD ratio vs. IF input voltage. The mixer TOI/IMD simulation was performed again for an R_s of 10, 20, and 30 Ω . The dynamic range slowly improves for smaller R_s , but is dependent on the noise bandwidth.

To speed up the process, a stock schematic intended for evaluation of single-ended mixers was copied from the menu and modified as shown in Figure 8. The tuned mixer with the D2SE output stage was then inserted from the component library. Unused inputs were terminated, the input was grounded and the output terminated in a large resistance. To obtain a differential LO, a transformer and source were copied from a differential test schematic and pasted into this schematic. An active LO single-ended-to-differential stage could also be designed and added to the mixer.

Again, NF and IMD vs. RF power sweeps were performed for a range of RS values from 10 to 30Ω . This was combined to determine dynamic range, plotted in Figure 9. An R_s of 10Ω produced the best result: a peak dynamic

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Test and measurement catalog available

Keithley Instruments announces a 400-page, full-color 2002 test and measurement products catalog. The catalog provides engineers with detailed information and specifications for Keithley's electronic test and measurement instrumentation and data acquisition hardware and software. Keithley's product offering includes digital multimeters, switch and measure systems, switch and control products, broadband signal routing systems, power sources, SourceMeter instruments, optoelectronic test solutions, semiconductor systems, low current/high resistance products, low voltage/low resistance products, and PCI/ISA plug-in boards. Product selection guides and updated page design will help engineers find products in the catalog quickly. The 2002 catalog features more than 30 new products, including a high-speed picoammeter, the Model 6485, and the Model 2750 multimeter/switch system for multipoint measurement and control. For semiconductor applications, there are two new single-insertion DC/RF parametric test systems.

Keithley Instruments www.ketihley.com product_info@keithley.com

Databook lists reed relays, sensors, switches

Meder Electronic offers a comprehensive, 290-page catalog that describes a wide range of reed relays, sensors and switches, along with numerous application examples. The Meder Reed Relays, Reed Sensors and Reed Switches Catalog is a primer describing how these products operate and how they are designed to solve everyday problems in a range of industries. Featuring a product selection guide, this databook includes complete technical specifications and offers numerous application examples illustrating the benefits of this technology. **Describing applications ranging** from household appliances to automotive sensors, computer peripherals, medical instrumentation, telecommunications, flow control. security systems, automatic test equipment, and toys, the 90-page Meder Reed Relays, Reed Sensors

and Reed Switches Catalog also includes a line of products for highvoltage switching applications. Meder Electronic www.meder.com sales@meder.com

Brochure describes quick-turn capabilities

Tech-Etch's latest brochure explains how photoetching enables rapid turnaround for both prototypes and full production runs of flexible circuits for telecommunications, medical and computer applications. It describes the company's specialized photochemical outlining process which yields production quality flexible circuits to specification. Photoetching produces an edge completely free of slivers, nicks and burrs, while allowing windowed leads and back side access. The color brochure describes Tech-Etch's capabilities for multilayer, fine-line and adhesiveless flex circuits, in addition to beryllium copper conductors, cantilevered leads and .004" diameter microvia processing for higher density two-layer circuits. Selective plating enables different attachment methods on the same circuit. PowerFlex is offered when circuits require up to .020" thick copper in high current applications. Complete ordering information is also provided. **Tech Etch**

www.tech-etch.com

CD-ROM product catalog features RF cable assemblies

Semflex announces a new product catalog on its RF and high-performance cable assembly products in CD-ROM format for use on PC platforms. The CD-ROM catalog presents detailed performance characteristics, schematics and photos and includes a program for designing custom cable assemblies for the user's specific application. Semflex

www.Semflex.com

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On the Web

PCB site goes live for learning, collaboration

Cadence Design Systems announces specctraquest.com, a new online community for printed circuit board (PCB) engineers and designers to learn more about - and collaborate on - high-speed design issues. Topics such as constraint development, simulation, modeling, power delivery system design, constraint-driven placement and routing, and achieving signal integrity are covered. Experts and novices can benefit from technical content provided by Cadence engineers, partners and community members. Open discussion boards encourage members to share problems and solutions to their real-time, high-speed design challenges, which are discussed in an open and collaborative environment. **Cadence Design Systems** www.specctraquest.com

Web site offers enhanced support

Unitive introduces its new corporate Web site with enhanced customer support and service functionalities. The new site, which can be found at www.unitive.com, enables customers and prospects to send their request for proposal (RFP) and design questionnaires online resulting in quicker responses. The site also features enhanced product and technical information. It also contains downloadable design guidelines and new white and technical papers on topics such as wafer-level packaging and electroplating. Unitive

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DC - 18 GHz	VN18	TM18	SL18	SF18				
DC - 26 GHz	VN26	TM26	SL.26	SF26				
DC - 40 GHz	VN40	TM40	SL40					
DC - 50 GHz	VN50	TM50	SL50					
Max. Frequency		26.5 GHz						
Inner Conductor		Stranded						
Dielectric		PTFE Tape						
Outer Conductor	Super Flexible Copper GrooveTube by MegaPhase							
Finished Outer Diameter	0.625 in. 15.88 mm	0.285 in. 7.24 mm	0.500 in. 12.70 mm	0.285 in. 7.24 mm				
Ruggedization	Metal Braid over Metal Armor	Metal Braid	Metal Braid over Metal Armor	Metal Braid				
Outer Jacket	PET Braid	Polyolefin	Neoprene	Polyolefin				
	1.5 in	0.5 in	1.5 in	0.5 in				

38.1 mm

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specifications. SMA connectors are used for the input/output ports with a pin type feed-through capacitor with ground post for the DC input. Four holes on the bottom flange allow easy mounting of the amplifier to any surface. High dynamic range amplifiers need to simultaneously provide low noise performance and high output power. The noise figures and output compression

performance of these devices are achieved by implementing blue cell LTCC technology. Noise figures in the 2 dB range, coupled with the +25 dBm output compression level, result in excellent dynamic range. Determining the spurious-free dynamic range at a given output power is one of the better ways to judge the performance of any



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Coventor upgrades Architect MEMS design software

Coventor has upgraded its Architect software to version 2001.3. It is available as a tool for MEMS device designers and developers in the optical, RF and biotechnical industries. CoventorWare 2001.3 includes, all within Architect: three new



udes, all within Architect: three new behavioral models – triangle plates, triangle electrodes, and four point stops for designing mirrors, switches, and other devices; new rectangular-plate behavioral model with stress and stress gradient; active valve behavioral model for top-down design of microfluidic devices; beam behavioral model that supports buckling and stress gradients; elec-

tro-mechanical behavioral models that support three mechanical layers; meshing of angled sidewall structures and biasing mesh along different directions, allowing more robust analysis; faster (up to 500x) and more accurate squeeze film and slide damping analysis. The MemDamping module rewrite allows easier meshing and setup as well as automatic macromodel extraction. MemCap includes analysis of lossy dielectric behavior, up to 10x an increase in the redraw speed of layout editor. **Coventor**

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Ansoft EM simulation software offers 64-bit features

Ansoft introduces HFSS 8.5, which implements key sections of code using 64-bit features. The result is a 64-bit EM simulator and a tenfold increase in

tor and a tenfold increase in the size and complexity of the structures. The 64-bit version can consider the frequency variation of any arbitrary material property using a significantly improved method for importing geometries from mechanical design packages such as Pro/Engineer and AutoCAD. An advantage of the



64-bit version is its ability to break the 2 GB limit of 32-bit EM. With HFSS 8.5, more traces and irregularly shaped power/ground planes may be considered for more complete prediction of signal integrity for rise times of less than 25 ps. Ansoft also enhanced HFSS 8.5 with the ability to automatically consider the broadband frequency variation of material properties, such as dielectric constant and loss, as well as considering frequency-dependent material properties critical at microwave/millimeter-wave frequencies.

Ansoft www.ansoft.com.

TDK Systems debuts wireless development tools

TDK introduces its Go Blue wireless software development toolkit, designed to support Bluetooth software developers creating and testing new applications for the Palm OS. Included in the toolkit are two TDK Systems USB adapters, one USB 4way hub, a CD with all software including install, router app, TDK Systems Palm drivers, Widcomm Bluetooth protocol stack, PID switch, Pocket Studio, help and installation documentation and references to online help. The kit uses TDK Systems' USB adapters to provide the Bluetooth links that enable the evaluation of applications. The tools are used in conjunction with the palm operating system emulator (POSE), used to create fully integrated Palm applications. The package allows as many as 127 USB adapters to be virtually connected to individual POSE sessions via a single PC. This allows the development and debugging of true Bluetooth applications, stressed to full Piconet capacity.

TDK Systems www.tdksys.com

Elanix Wi-Fi library adds IEEE 802.11b

Elanix announces the release of its Wi-Fi 802.11b library. The new library adds IEEE 802.11b specification requirements to the existing 802.11a functions in the SystemView



Communication Design Suite. The library incorporates all IEEE 802.11b capabilities. It supports both framegeneration and individual component level and allows rapid analysis of different design approaches, accelerating the design and implementation process. The library includes lowlevel functional blocks for individual modulators/demodulators as well as high-level 802.11b packet generation. Optional features in the IEEE 802.11b specification are fully supported in the Wi-Fi library, including packet binary convolutional coding (PBCC), short physical layer protocol data units (PPDU) format and channel agility (frequency hopping). Key features of the Wi-Fi 802.11b library include a full slate of 802.11b modulators/demodulators, 2 Mb/s differential quadrature phase-shift keying (DQPSK), 5.5 Mb/s and 11 Mb/s complementary code keying (CCK), 5.5 Mb/s and 11 Mb/s packet binary convolutional coding (PBCC), long and

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A FBT H G FT	10-4200	0.15	0.6	0.6	N/A	N/A	N/A	1 13 1	EQ QL
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FBIC 1G	10-1000	0.15	03	0.3	27	33	30	1 10 1	1 ne car
FRIC 3G	10,000	0.16	0.3	1.0	27	30	35	1.60.1	35.95
of BIC 1GW	0.1.10.0	0.15	03	03	2'	32	301	1 10 1	35, 95
FBTC JGW	01.000	0.15	03	1.0	24	CID	35	1.60.1	46.05
•JEBT 4R2G	10-4200	0.15	0.6	0.6	32	40	40		111.05
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AWR announces EDA suite

AWR announces the Visual System Simulator 2002 (VSS2002) communications systems design suite. The suite enables system engineers to perform top-down analysis of analog and digital communications systems. It can accurately characterize radio frequency (RF) impairments. VSS2002 software is seamlessly integrated with AWR's Microwave Office 2002 circuit design suite, enabling bottoms-up analysis to be performed where the transistor level effects are

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- Supports AM, FM, OFDM, PSK, MSK, QAM and others
- Real-time tuning mode
- Over 230 core elements and mathematical primitives
- Supports 3G, IS95, GSM, EDGE, 802.11, and other emerging standards

incorporated at the system level through system/circuit co-simulation. The product's discrete time simulation engine and extensive model libraries provide a solution for analyzing systems from the channel through the RF and digital signal processing (DSP) subsystems. It is



designed for analyzing wireless communications systems, high-speed wire-line, and electro-optical systems. It uses built-in measurements and signal generators that support virtually any modulation scheme, including: AM, FM and orthogonal frequency division multiplexing; phase-shift keying; mask-shift keying; quadrature amplitude modulation and others. Users can easily assess the impact of specifications by using a unique "real-time tuning mode" that immediately displays the impact of parameter changes by updating measurements in real time. VSS2002 software includes a comprehensive library of more than 230 core elements and mathematical primitives that can be used to build an accurate representation of the most complex communications systems. The library includes: encoders/decoders (including Viterbi, Reed-Solomon, convolutional and others); modulators/demodulators and filters. Application-specific libraries are optional and support 3G, IS95, GSM, EDGE, 802.11 and other emerging standards.

Applied Wave Research www.appwave.com info@mwoffice.com

CST introduces Design Studio Version 2

CST introduces version two of its design environment. Major improvements include an enhanced parametric modeling in connection with a powerful optimization. The open architecture of all CST tools allows them to embed any tool or can be embedded in any tool, as long as this other tool is based on OLE technology. This architecture also supports the optimization even across the borders of tools of different vendors. The library of analytic models has been significantly extended, reducing the need to use other simulators in many common cases. In addition, the user can easily build up his own collection of library elements, which can be placed into the RF design via drag and drop. With the enhanced VBA macro language, both the new CST Design Environment and CST Microwave Studio further support the automatization of commonly performed tasks and provide full control of the simulation process across various simulation tools.

Computer Simulation Technology www.cst.de

Agilent offers automated fault diagnosis software

Agilent Technologies introduces, as a standalone product, software that automates functional test diagnostics of circuit boards and electronics sub-systems during assembly. Fault Detective 2.0 eliminates the time and expense of manual diagnoses, increasing diagnostic accuracy and quickly providing insight into the root causes of recurring product failures. The solution represents a technology advancement in an area of electronic manufacturing that has been resistant to automation. Functional test diagnostics account for as much as 10% of electronic manufacturing costs, which derive largely from inaccurate manual diagnoses and technician time. Fault Detective's initial accuracy rate is about 80%, and this can increase as the diagnostic model is refined. It also eliminates the time required for manual diagnoses, which can sometimes take hours for complex devices and several minutes for less complicated, high-volume products. When a manufacturer's functional test system registers a failure, it activates Fault Detective, which delivers diagnostic results within seconds. Fault Detective programming is easy to learn and can be reapplied to new manufacturing lines.

Agilent Technologies www.agilent.com

Eagleware Genesys V8 features enhancements

Eagleware announces the eighth release of its Genesys suite of design software, Genesys V8. This latest release adds several innovative enhancements, including Test Link automated instrument interface. Advanced T/Line synthesis, and S/Filter support of distributed transmission lines. The Test Link interface imports data directly from network analyzers, spectrum analyzers and noise figure meters; the Advanced T/Line converts simple electrical lines to physical lines; and the S/Filter Advanced Direct Filter Synthesis adds distributed capability. Other new features include tuning to standard values for passive components and a symbol editor for quick and easy creation of custom schematic symbols. Also, the company's Layout printed circuit board tool has been extensively updated to include X-ray and hollow views, parts list/bill of materials. DXF import, and Gerber improvements. **Eagleware**

www.eagleware.com



Linearity, Power... and Price A powerful HBT amplifier combination.

Sirenza Microdevices' highly linear GaAs HBT amplifiers deliver ¹/₄-watt power with a third-order intercept point as high as 44 dBm. And the prices make them the best buy around.

The SXA-389 runs on 5 volts and offers on-chip active bias control and excellent DC power efficiency.

It offers IS-95 channel power of 19 dBm and WCDMA channel power of 16.5 dBm at -45 dBc adjacent channel power. Designed specifically as a driver for infrastructure equipment and customer-premise equipment in the 400–2500 MHz cellular, ISM, WLL, PCS and WCDMA bands, it's priced at just \$4 each in quantities of 10,000.

SOT-89 Package shown actual size The SXA 289 and SXT-289 amplifiers cover the 5–2000 MHz and 1800–2500 MHz bands with a rare combination of efficient ¹/₄-watt power with high linearity in a low-cost, surface mountable SOT-

89 package. Both products feature SMDI's high-reliability HBT technology and deliver high OIP3 performance of better than 40 dBm. The price in quantities of 10,000 is just \$3.50 each.



For more information, visit us at www.sirenza.com • 800.764.6642

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Alternative to phase-locked DRO synthesizers

EM Research has released the Thor-Series phase-locked frequency synthesizers. The devices are suitable for use as miniaturized replacements for phase-locked dielectric resonator oscillators (PLDRO). Supplied as VCObased fixed-frequency or serially programmable, precision phase-locked frequency oscillators, they cover the frequency range (in bands) from 50 MHz to 12 GHz. The products use internal or external frequency references for high stability and exhibit low phasenoise characteristics. Housed in an aluminum package with removableshell SMA connectors for surfacemount or PCB applications, they can operate over the temperature range of -40 to +85° C and can be hermetically



sealed for use in military or other highreliability applications. Package dimensions are 2.5" x 1.1" x 0.3" (excluding connectors and mounting feet). EM Research www.emresearch.com

sales@emresearch.com

MILITARY/ AEROSPACE

RAD hardened A/D converter

Maxwell Technologies introduces the 9042 12-bit, monolithic A/D converter microcircuit, featuring a greater than 100 krad (Si) total dose tolerance. All necessary functions, including trackand-hold and reference, are included on the chip. The device is space-qualified and specifically designed with a wideband front end for multichannel receivers. The 9042 runs off of a single +5 VDC supply and provides CMOScompatible digital outputs at 41 Ms/s. It maintains 80 dB spurious-free dynamic range over a bandwidth of 20 MHz. The chip features a typical signal-to-noise ratio of 68 dB. It comes in a 28-pin RAD-PAK flat package and is

Specifications at a glance:

- 12-bit monolithic converter
- 100 krad (si) tolerant
- 68 dB S/N
- 80 dB dynamic range

available with screening up to class S. The product incorporates radiation shielding in the microcircuit package, which eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit.

Maxwell Technologies www.maxwell.com mlanning@maxwell.com

High-stability 20 GHz microwave synthesizer

Elcom debuts the MFS-18.00/20.00 microwave frequency synthesizer. The synthesizer consumes 350 mA at +15 VDC and 650 mA at +5.25 VDC. The device measures 7.7" x 5.5" x 0.73" and employs a single module design implemented with CMOS, ASICs, advanced MMICs, and a dedicated microprocessor. Ruggedized and field-tested for operations over a temperature range of -15 to +70° C, the synthesizer exceeds the requirements of IESS 308, Eutelsat and MIL-STD188-146 (wider temperature range is optional). Its phase-noise is -92 dBc at 10 kHz and -97 dBc at 100 kHz, which makes this high-frequency MFS model suitable for applications in SATCOM converters, instrumentation and military applications. Elcom

www.elcom-tech.com

TEST AND MEASUREMENT

Jitter test solutions for 2.5 and 10 Gb/s FO systems

Agilent Technologies introduces two new jitter solutions for R&D engineers who test compliance with SONET/SDH specifications on 2.5 Gb/s and 10 Gb/s optical communications products. Features and benefits of the Agilent JS-1000 include: compliance testing to Bellcore GR-1377 and ITU-T 0.172 jitter measurement standards; architecture that is

Specifications at a glance:

- 50 micro UI intrinsic jitter
- ~0.2 dB repeatability
- 0.005 dB resolution
- 0.1 dB accuracy

extendable to 40 Gb/s and other future measurements; compliance to the 80 MHz modulation bandwidth requirements of the ITU-T 0.172 and Bellcore GR-1377-CORE standards; and a wide range of output formats and graphs that assist diagnosis. Agilent Technologies www.agilent.com.

Spectrum analyzer monitors remote base station

Morrow Technologies announces a vector spectrum analyzer that can be permanently mounted in a cellular base station. The VC900 gives a service provider continuous remote access to important base station parameters such as ACPR, channel power and statistical power measurements, as well as standard spectrum analyzer functions. It can also perform modulation domain measurements such as polar plots, eye diagrams, rho, code and channel power. The system covers the 800 to 1000 MHz cellular bands, and can be configured with three inputs for



monitoring three sectors of a base station. It can be operated remotely via a LAN, telephone modem, a wireless modem, or the Internet. All of these communication methods are supported internally by the VC900 with no other hardware or software. The analyzer can also activate alarm contacts when a monitored parameter is no longer within specified limits. **Morrow Technologies** www.vigilcom.com

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AMPLIFIERS

Aethercomm announces the SSPA 5.0-6.2-20, a high-power, C band, solid state power amplifier that operates from 5.0 to 6.2 GHz. It offers a minimum of 20 W of linear RF power at 65° C base plate temperature. Saturated output power is greater than 30 W across the band. It offers a typical small signal gain



of 40 dB minimum at P1dB. Input VSWR is better than 2.0:1. Output VSWR is less than 2.0:1. DC high speed switching circuitry turns the PA on and off in 500 ns. It is biased class A and operates from a +28 VDC supply with a quiescent current of 8 amps, typical. It also comes in a +12 VDC version. Second and third harmonics are 50 dBc at P1dB. Noise figure is less than 5.0 dB at 25° C. It is housed in a modular case that is 6.0" x 8.0" x 1.0". Operation from -40 to +85° C is standard.

Aethercomm www.aethercom.com sales@aethercomm.com

Tri-band LNA for EDGE/DCS/PCS

RF Micro Devices introduces the RF2417 tri-band LNA for EGSM/DCS/PCS multi-band handset applications. The device is a highly integrated, low-power, tri-band LNA. All three input and output ports include onchip matching to minimize the external component count. In the 900 MHz EGSM band, the 2.7 VDC LNA offers a low 1.6 dB noise figure and 17 dB gain. In the 1800 MHz DCS and 1900 MHz PCS bands, the device provides 1.9 dB noise figure and 17 and 19 dB of gain, respectively. It offers a 23 dB gain



reduction mode and three-mode control pins to control gain and band selection. This SiGe HBT BiCMOS device consumes 4.0 mA in EGSM mode and 5.5 mA in DCS and PCS modes. The RF2417 is assembled in a 3 mm x 3 mm 16-pin leadless plastic package. **RF Micro Devices** www.rfmd.com

SIGNAL PROCESSING

Family of linear RF mixers

WJ Communications announces a new family of linear RF mixers. Performance highlights of the SMJdiode mixer line include; high IP3 (linearity) performance (up to +29 dBm),

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broadband frequency coverage (covering 500 kHz to 2400 MHz), low LO power versions, low conversion loss and high isolation.

WJ Communications www.wj.com

SAW filters offer reduced size and weight

Toshiba debuts a new line of miniature RF SAW filters. By integrating chip-scale packaging, a 40% size reduction and 60% weight reduction, is



achieved. The devices offer the same electrical performance as SAW Filters offered in larger packaging, giving designers smaller form-factor mobile devices. Targeted for the U.S. and European mobile communications markets, the SRF942NLC61 family supports the EGSM 900 MHz frequency range, while the SRF1842NFC61 family supports the DCS 1.8 GHz range. The devices also offer designers a choice of interface options. These include 4-pin for single-ended output types, as well as 5- or 6-pins (depending on model) and balanced output types. **Toshiba America**

www.toshiba.com

SEMICONDUCTORS/ ICs

MOSFETs with highspeed intrinsic diode

APT announces an expansion to its power MOSFET line to include FREDFETs – MOSFETs with the intrinsic diode optimized for low reverse recovery charge and improved commutating dv/dt capability. The devices feature low gate charge and internal chip gate resistance, low $R_{DS(on)}$, low thermal resistance and increased power dissipation rating and low intrinsic diode reverse recovery charge. FREDFETs are fabricated with APT's patented metal on polysilicon gate structure for an internal chip gate resistance that is one to two orders of magnitude lower than comparable industry-standard polysilicon gate devices.

Advanced Power Technology www.advancedpower.com custserv@advancedpower.com

High-gain, high-linearity power amplifier

Fujitsu announces the FMM5049VT power amplifier. Featuring high linear gain (33.0 dB) and 41.0 dBm output power, this MMIC complements the



existing FLLxxxx(yy)-2C Series of GaAs FET PA products. The device is designed for 2.2 GHz W-CDMA applications and also provides performance for PCS/PCN applications in the 1.8 to 1.9 GHz frequency range.

Fujitsu Compound Semiconductor www.fcsi.fujitsu.com

TX/RX

Cable assemblies with insertion-loss equalizers

Kaman Aerospace debuts high-performance microwave assemblies with either integral or insertable in-line insertion-loss equalizers. The new higher-reliability equalizers provide an inverse loss equalizer that can be individually tuned to accuracies of less than \pm 0.25 dB at any given frequency.

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The design of the equalizer allows the system to dissipate absorbed energy as heat. The compact size of the equalizers allows them to be incorporated as an integral part of some of Kaman's connectors or as an independent in-line unit for add-on applications. Kaman Aerospace

www.stablecable.com

High-isolation, non-reflecting switch for base stations

Alpha Industries' new GaAs IC SP4T switch combines high isolation to provide greater signal path separation to reduce RF leakage with non-reflecting ports. This eliminates the need for external termination while providing 50Ω output impedance. Covering the frequency range of DC to 3.5 GHz, the AS204-80 provides low loss for greater signal strength and better system performance in base station switch matrices. The new switch features a +5 VDC integrated driver to simplify circuit lavout and reduce space requirements. Key

Specifications at a glance:

- 45 dB isolation
- 0.5 dB insertion loss
- SSOP-16 packaging
- DC to 3.5 GHz frequency

specs, operating at 0.9 GHz, include 45 dB isolation, 0.5 dB insertion loss, and at 1.9 GHz 37dB isolation, and 0.55 dB insertion loss. It is available in a miniature SSOP-16 plastic package.

Alpha Industries

www.alphaind.com sales@alphaind.com

220 to 325 GHz VNA extension modules

A new pair of vector network analyzer (VNA) frequency extension modules, covering 220 to 325 GHz, is being introduced along with a precision waveguide calibration kit. The models V03VNA-T/R and V03VNA-T are compatible with any



microwave VNA currently marketed that supports external frequency extension. Vector network analysis applications in the 220 to 325 GHz range are emerging in several areas, including R&D efforts on new 600 GHz and 1 THz semiconductors, NOAA/NASA space-born radiometers for weather prediction and earth resource management, Defense Department space communications and reconnaissance, and characterization of second and third harmonic responses in fiber-optic applications at 80 GHz and higher. Also, there is funded effort underway in millimeter-wave, vector network analysis-based DNA studies of biologics. These two new models are part of a family of frequency extension modules cover-



ing 33 to 325 GHz in all of the waveguide bands from WR-22 through WR-03. Oleson Microwave Labs www.oml-mmw.com

VAT line of DC to 6GHz fixed attenuators

Mini-Circuits has released the VAT family of wideband DC to 6 GHz fixed attenuator series. The devices deliver nominal attenuation from 1 to 10 db, in dB steps, plus 12, 15, 20, and 30 dB.



Equipped with SMA-type male/female connectors, the rugged unibody construction measures only 1.42" long (0.370" diameter) and can handle 0.5 W power (at 70°C ambient). The devices are suitable for impedance-matching and signal-level adjustment applications. Designer kits are also available. **Mini-Circuits**

www.minicircuits.com sales@minicircuits.com

FIBER OPTICS

SM VCOs for 40 Gb/s networking systems

Agilent Technologies offers a family of SMT VCOs for high-speed 40 Gb/s fiber optic communications systems. These embedded clocks synchronize data and voice communications systems to operate at U.S.-standard SONET or European-standard STM transmission rates. Agilent's new SMT VCOs deliver standard SONET frequencies of 19.906 GHz and 39.813 GHz, with differential outputs, making them compatible with the MUX and DEMUX ICs for 40 Gb/s applications. They use Agilent's silicon bipolar and GaAs PHEMT technologies, and operate at 5 VDC bias with a 0 to 5 VDC tuning range. They are also available at slightly higher frequencies for systems FEC, and can be packaged with SMA/K-connectors.

Agilent Technologies www.agilent.com

1.6 Gb/s per channel parallel optic modules

W. L. Gore announces volume availability of its nLIGHTE 1.6 Gb/s paral-



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APPENDIX A – The MATLAB Program

%Program calculates the load reflection coefficient for coincident gamma_opt and gamma source

fprintf('\nInput S parameters to calculate Load Gamma. This gamma will force GammaOpt = GammaMS or GammaIn = $GammaOpt^* \n');$ S11mag = input('\nEnter S11 magnitude: '); S11ang_deg = input('Enter S11 angle: '); S21mag = input('Enter S21 magnitude: '); S21ang deg = input('Enter S21 angle: '); S22mag = input('Enter S22 magnitude: '); S22ang_deg = input('Enter S22 angle: '); S12mag = input('Enter S12 magnitude: '); S12ang_deg = input('Enter S12 angle: '); GammaOptMag = input('\nEnter gamma_opt magnitude: '); GammaOptAng deg = input('Enter gamma_opt angle: '); S11ang_rad = S11ang_deg * 2 * pi / 360; S21ang_rad = S21ang_deg * 2 * pi / 360; S22ang_rad = S22ang_deg * 2 * pi / 360; S12ang rad = S12ang deg * 2 * pi / 360; LoadGammaMag = 0.01;LoadGammaAng_deg = 0; % convert S22 to rectangular S22real = S22mag*cos(S22ang_rad); S22imag = S22mag*sin(S22ang_rad); % convert S11 to rectangular S11real = S11mag*cos(S11ang_rad); S11imag = S11mag*sin(S11ang_rad); Convergence = 0;while (LoadGammaMag < 1) & (Convergence == 0) while (LoadGammaAng_deg < 360) & (Convergence == 0) % find source gamma LoadGammaAng_rad = LoadGammaAng_deg * 2 * pi / 360; GsNumeratorMag = S12mag * S21mag * LoadGammaMag; GsNumeratorAng = S12ang_rad + S21ang_rad + LoadGammaAng_rad; Dmag = LoadGammaMag * S22mag; Dang = LoadGammaAng_rad + S22ang_rad; DmagRect = Dmag * cos(Dang) + i * Dmag * sin(Dang); GsDenominatorRect = 1 - real(DmagRect) - i*imag(DmagRect); %Divide numerator by denominator GammaS1Mag = GsNumeratorMag / abs(GsDenominatorRect); GammaS1Ang = GsNumeratorAng - angle(GsDenominatorRect); % convert to rect. GammaS1Rect = GammaS1Mag * cos(GammaS1Ang) + i * (GammaS1Mag * sin(GammaS1Ang)); SourceGammaRect = (S11real + real(GammaS1Rect))+ i*(S11imag + imag(GammaS1Rect)); SourceGammaRect = conj(SourceGammaRect); SourceGammaMag = abs(SourceGammaRect); SourceGammaAng_rad = angle(SourceGammaRect); SourceGammaAng_deg = SourceGammaAng_rad * 360 / (2*pi); if abs(SourceGammaMag - GammaOptMag) < 0.01 & abs(SourceGammaAng_deg - GammaOptAng_deg) < 1 Convergence = 1;fprintf('\nLoad reflection coefficient for GammaOpt/GammaSource coincidence: %1.3f < %3.1f\n', LoadGammaMag, LoadGammaAng_deg); else LoadGammaAng_deg = LoadGammaAng_deg + 1; end end LoadGammaMag = LoadGammaMag + 0.01; $LoadGammaAng_deg = 0;$ end if Convergence == 0fprintf('\nNo convergence. No value of load impedance will force GammaOpt=GammaMS.\n'); end % END PROGRAM

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Europe: Stephen Bell 2nd Floor, Hillcrest House, Woodcoat Road Wallington, Surrey, SM6 OLT, U.K. Tel. +44.208.669.2700; Fax: +44.208.669.9372 e-mail: stephenbell@email.msn.com lel optic modules for today's scalable networking systems. The modules are 12-channel 850 nm VCSEL-based parallel optical links that transfer an aggregate bandwidth of 19.2 Gb/s (1.6 Gbps/channel) up to 300 meters while occupying less than 20 mm of board width. The devices are compatible with Gore's durable, state-of-the-art Flex-Lite fiber optic ribbon interconnects or with standard FDDI grade 62.5 mm multimode ribbon fiber. W. L. Gore & Associates www.gore.com

SUBSYSTEMS

GaAs MMIC mixer with integrated LO and IF amps

Hittite Microwave introduces a high-linearity down-converter receiver IC designed to support WCDMA applications where a high third-order intercept (OIP3) point is required. A passive mixer, coupled with a high dynamic range IF amplifier, achieves



INFO/CARD 110

Specifications at a glance:

- OIP3 of +29 dBm
- Input IP3 of +19 dBm
- Up to 10 dB typical SB noise
- For WCDMA applications

an OIP3 of +29 dBm, and an input IP3 of +19 dBm. The HMC421QS16 provides a gain of 8 dB and 10 dB typical single sideband noise. This design requires no external Baluns and minimal off-chip components. The HMC421QS16 is suitable for use in MMDS, WLL, WLAN and cellular infrastructure applications. Hittite Microwave www.hittite.com

Dedicated low-power

microcontroller

Xemics announces the release of the XE88LC06 for smart radio applications. The system operates 2.4 to 5.5 VDC with a constant current requirement (300 uA/Mips). It includes an 822 bits microcontroller with 1 clock cycle multiplication, 22 kB of MTP Flash memory, 520 bytes of RAM, counters, UART, numerous IO, and PWM. Additionally, four low-power comparators are available for detecting external signal or doing simple analog-to-digital conversions. Asynchronous digital communication can be made via the integrated 115 kbaud UART or using synchronous protocol software drivers available from Xemics' Web site. It operates with less than 2 uA in low-speed mode, making it perfect for both monitoring and battery-powered devices. It directly connects to any one of the Xemics XE1200 ultra low-power radio transceiver series. Complete development tools, as well as application and software examples, are available. XEMICS

www.xemics.com



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PRODUCT

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K & L Microwave, Inc. introduces its new Mini-Max TM series of microminiature filters. The units

feature a package height of only .240 inches with a choice of ceramic or lumped component chip and wire technology for use in high performance applications. With a leaded surface mount configuration, K&L now offers the smallest most compact miniature filter available.

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ANSOFT www.ansoft.com



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Gore introduces GORE-S H I E L D SMT EMI gaskets, high performance EMI shielding gaskets that can also

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LINDGREN RF ENCLOSURES www.lindgrenrf.com



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RAYTHEON RF COMPONENTS www.raytheonrf.com



MITEQ offers a new line of "aluminum nitride" (AIN) power resistors, terminations and attenuators for

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Godzilla vs. King Kong



by Ernest Worthman technology editor eworthman@primediabusiness.com

Ah the classic, timeless battles – Godzilla vs. King Kong, VHS vs. Betamax, Apple vs. IBM, and Louis vs. Schmeling, to name a few. And now, along comes Bluetooth vs. 802.11.

Of late, and probably due, in part, to the general malaise of the high-tech industry, there has been little to get excited about with either technology. But, in all fairness, this segment of the market seems to be the lead dog in the pack. That could bode well once the recovery gets up ahead of steam.

Depending on which side you work for... — As an editor, I am presented with a lot of soap boxing. Sometimes it's promotional; sometimes it's competitor bashing. Occasionally, it's even honest. I want to think I can sort through it all and grasp what is really going on.

Wi-Fi says... — If you're in the 802.11 (also known as Wi-Fi) camp, there has been a pretty steady stream of visible 802.11b (the 2.4 gig) stuff. Almost every week, I see advertisements for wireless LAN (WLAN) products in flyers and on the shelves of technosuperstores. This tells me that this technology has reached a couple of milestones. First, it actually seems to work. Second, it has met a price point that consumers seem to accept (although this consumer still thinks a \$200 access point is a bit high, but it can be found for less if you are a prudent Internet shopper).

Wi-Fi looks solid in performance, at least from what people who play with it tell me. It appears interference-resistant and reliable. Like most wireless technologies, however, its distance claims are greatly exaggerated.

But if I had to play the pessimist, I'd say that Wi-Fi may be sorry down the road for having such a narrow focus (after all, the "E" in WECA, the Wi-Fi sanctioning alliance, stands for Ethernet). In the drive to become the defacto W-LAN standard, it may paint itself too tightly into the WLAN corner. It may backfire down the road if there is any inkling of challenging Bluetooth, HomeRF or WAP. WLAN may be its mantra but...Oh well, maybe I'm just thinking out loud. **Bluetooth says...** — Last year Bluetooth was probably the most overhyped technology since digital TV (DTV). It just didn't do what it was supposed to (although eventually, it and DTV will). We all know about its insufficient speed and range, high power consumption, too much interference, security issues and a need for system designers using BT chips to know RF technology. It was also touted as all things to all applications.

Well, reality has set in and the Bluetooth camp has put the binders on while looking for a workable position. I think it may have found it as a low-cost cable replacement. I would love to have Bluetooth as a link between my digital camera and my computer. Or as an ad-hoc, mobile interconnect between my laptop, desktop, camera, MP3 (ugh!) player, PDA, cellphone and wireless headphones.

I think this is where the money is. And, I'm seeing some Bluetooth devices start to appear that support some of these.

I also still think Bluetooth has the opportunity to corner the smart appliance market. It has better name recognition and support than HomeRF or WAP, but taking lessons from the early mobile phone market, the industry will have to show the consumer the value of smart appliances (and that it won't substantially add to the appliance's price) before this gets hot.

Finally, I think Bluetooth can evolve into the wireless networking arena (it's already aiming for the personal area network (PAN) niche). It won't be as robust as WLAN, especially when WLAN data rates climb into the 50+ Mb/s level, but it offers promise for the wired home (as a PAN). Bluetooth, however, must ice its black eyes and prove itself. The next generation of Bluetooth looks like it will be based on the IEEE's 802.15.3 standard, offering 20 Mb/s data rates and backward compatibility with current Bluetooth technology. It's good that there is movement in that direction. I think it is necessary. It will solve some of the Bluetooth issues and offer a wider platform.

Ern says... — I believe 2002 will be a critical year for both of these technologies (but only if, like the pundits say, the recovery starts this year — personally, late this year, if at all). However, opportunity knocks. The Bluetooth and WLAN alliances have a breather. They can take this lull and use it to refine, develop and tighten the technology so that when it does pop, their horses are fed and hot. Maybe King Kong and Godzilla *can* coexist.

Em 2

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