

Product of the Month

Linear Technology's direct conversion quadrature demodulators

Product Focus

Unlicensed Technologies



SEPTEMBER 2003

RF DESIGN

RF AND MICROWAVE TECHNOLOGY FOR DESIGN ENGINEERS

Technique and technology advances making their way into aerospace electronics

Increased integration and functionality are reducing size, weight and power requirements

Test and Measurement
WCDMA handset performance testing

Broadband Technology
Intelligent tools solve Bluetooth in-vehicle interference issues

Secure Communications
Low-power techniques for mobile cryptographic solutions

Amplifiers Multitone IMD replaces multiple carriers in MCPA performance trials

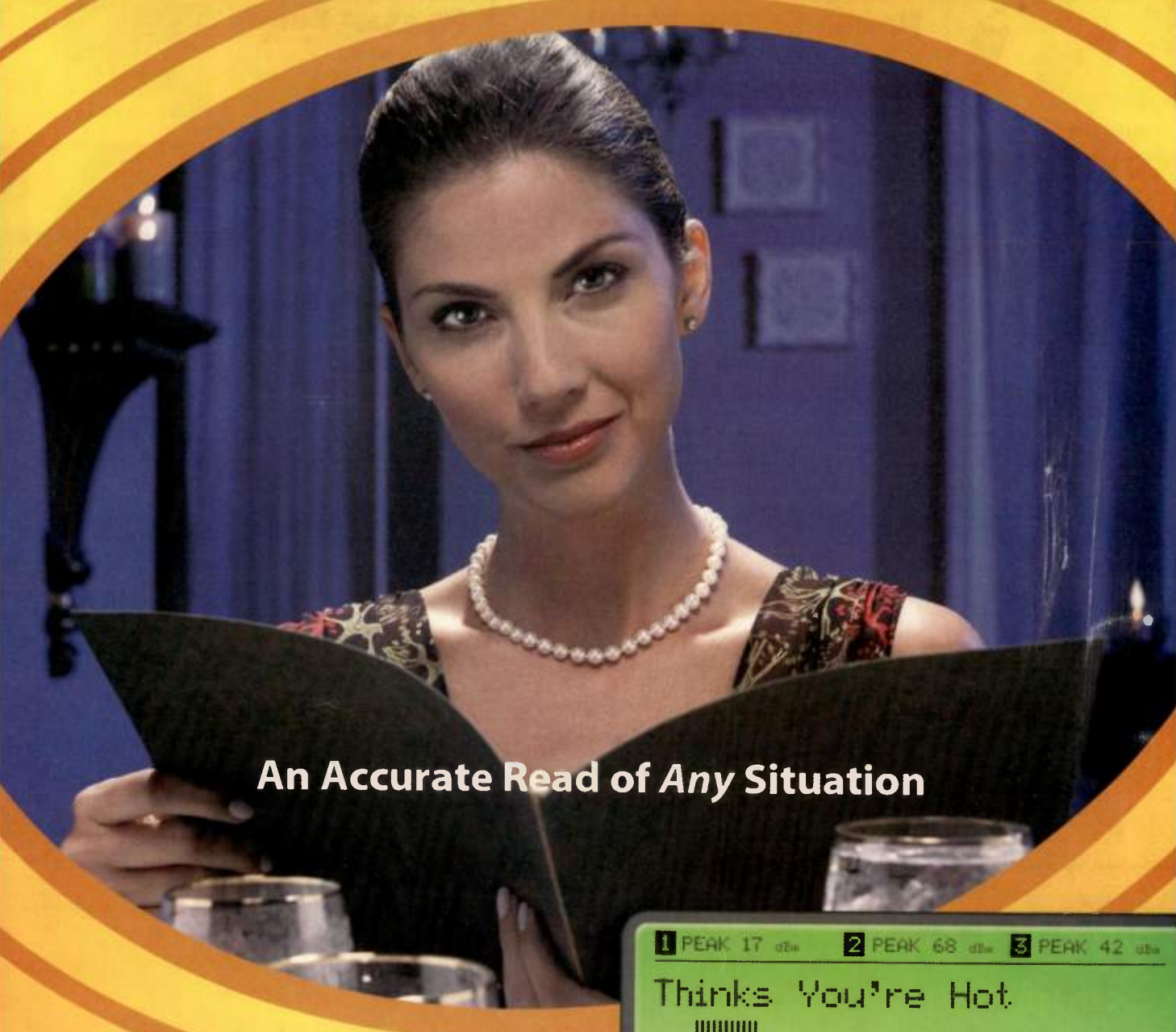
Integrated Subsystems
A downconverter circuit for DCS-1800 applications

A PRIMEDIA Publication

RF FUNDAMENTALS

Training materials for all types — a review of Noble Publishing's instructional CDs — By Keith Vick

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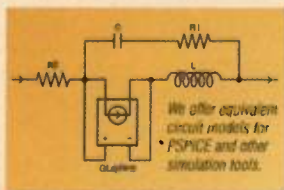
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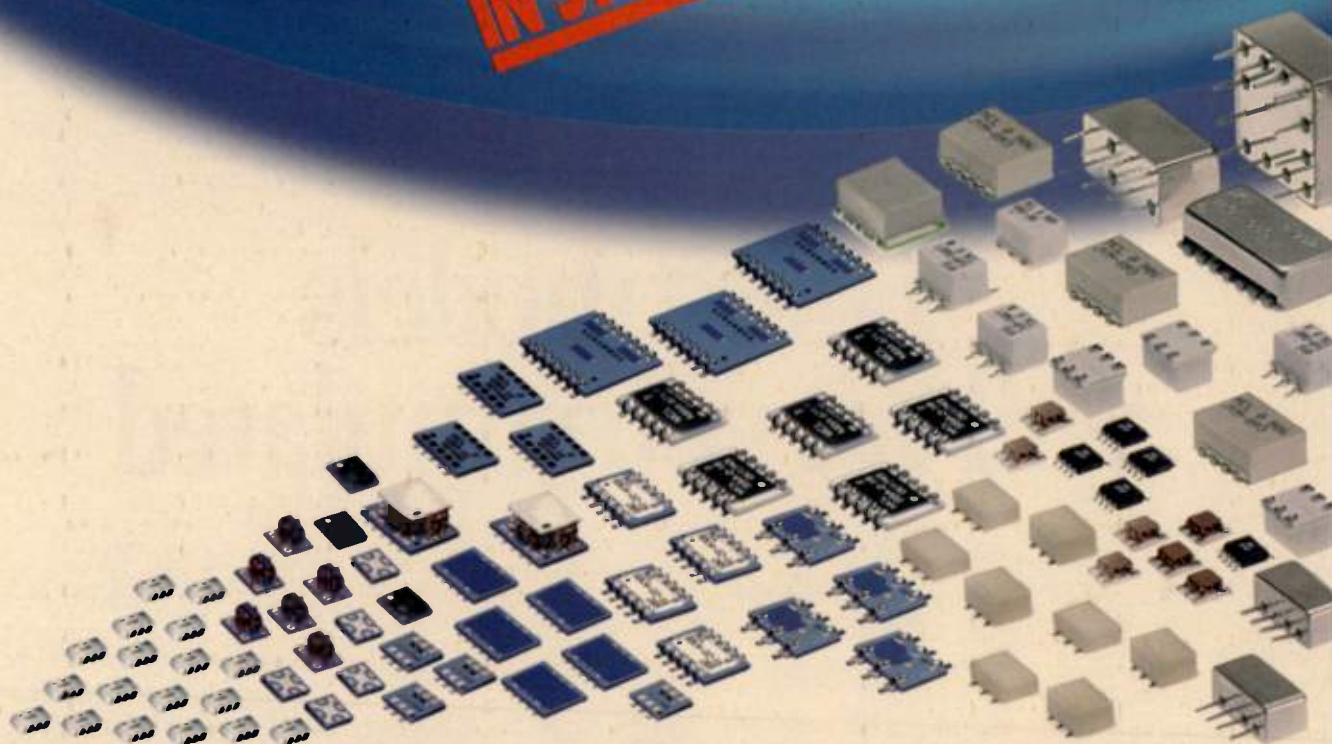
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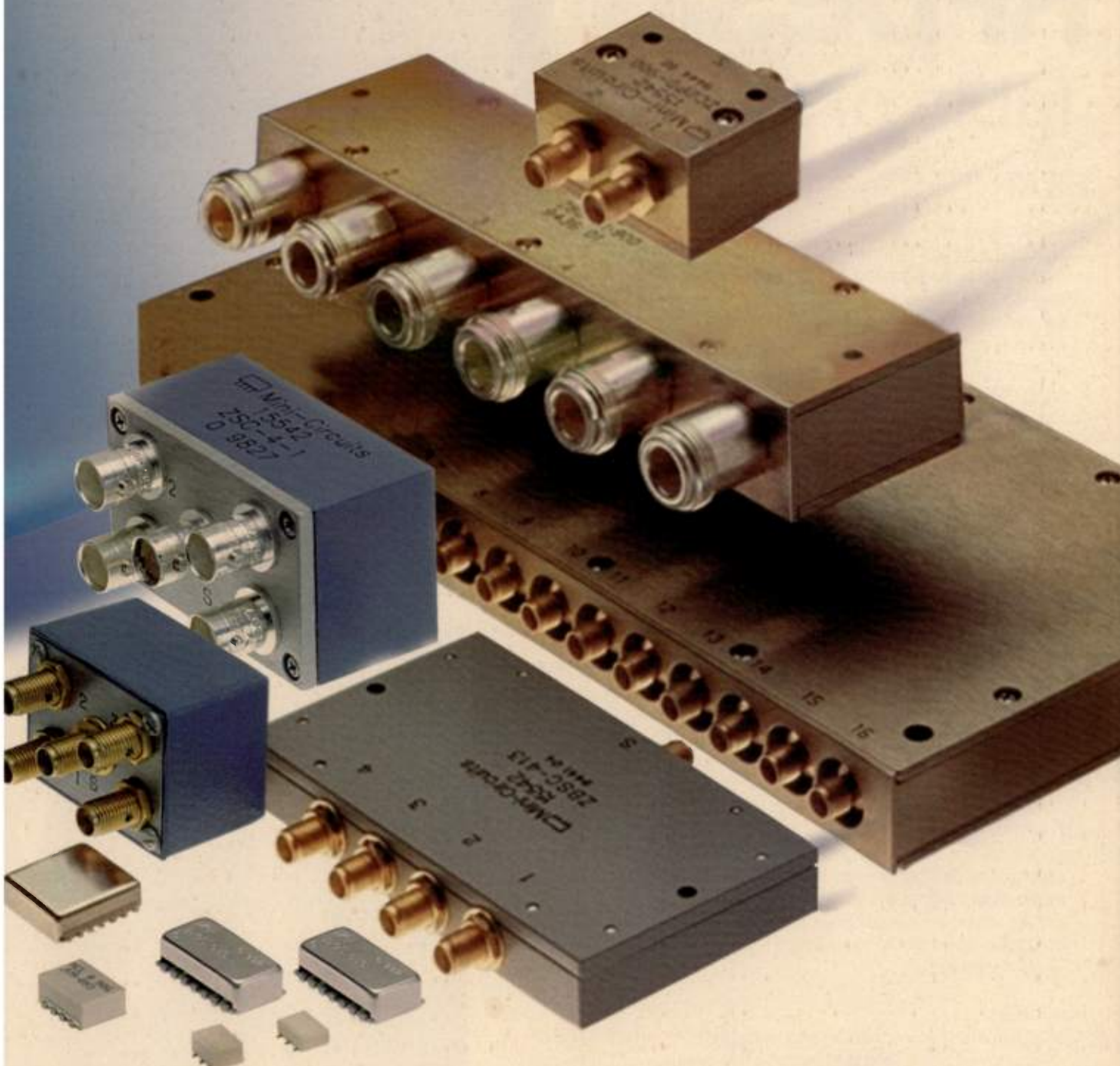
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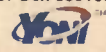
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— *By Rob VanBrunt*

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— *By Todd Moore*

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— *By Marta Iglesias*

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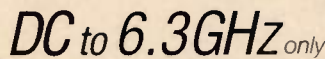
An integrated down-converter circuit in 0.8 μm SiGe technology for DCS-1800 applications — Frequency converters are an important part of most RF front-ends. This article describes a downconverter circuit for DCS-1800 applications.

— *By E. Hernández, R. Berenguer, J. Meléndez, N. Rodríguez, and J. Aguilera*



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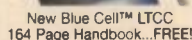


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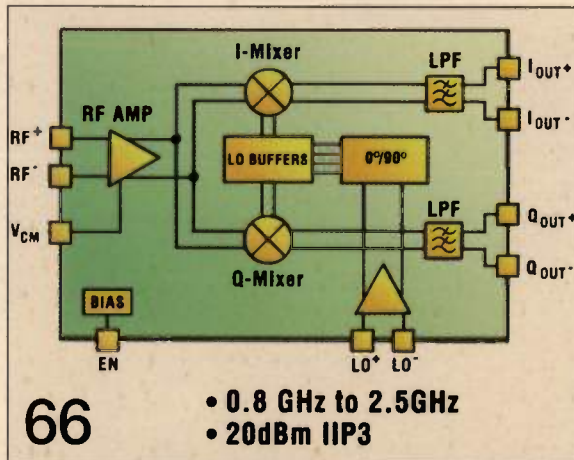
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Training materials for all types — a review of Noble Publishing's instructional CDs
— By Keith Vick



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	MCA1-60LH	10	1700-6000	6.3	30	8.45
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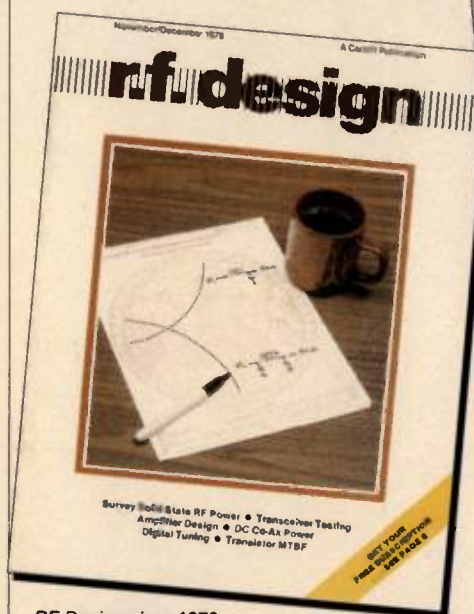
The new *RF Design*

Welcome to the new *RF Design*. Obviously, we've made quite a few changes to the magazine's style and design. I'll run through a quick tour to point out all of the changes, and highlight things that have not changed.

First, the cover. Big change. Easily the biggest change. We updated the style to reflect modern design, and moved components around to give readers more information about the contents of each issue.

ored headers. *RF Design* presents practical, straightforward, tutorial-style articles to help design engineers with every day problems, and we changed our design to reflect that style.

If you've paid attention over the last nine months, you'll have noticed that we virtually eliminated our monthly news and business brief sections. We feel those time-



RF Design circa 1978

The most obvious change is probably the tag line. Previously, *RF Design* was known as the publication that covered "Engineering RF & Wireless Products. . . DC to Light." The new tag line, "RF and Microwave Technology for Design Engineers," reflects our long-standing coverage of both RF and microwave topics. While *RF Design* has covered both frequency ranges for years, there was an industry belief that we only covered low-frequency issue.

Another obvious change is the addition of separate graphics for the cover story and product sections. Because products drive this industry, we added space and graphics to highlight our "Product of the Month" and "Product Focus" sections. Readers can now tell at a glance what product made our monthly blue ribbon section, and what topic is covered in the product focus.

Inside the magazine, we tried to make things as simple and straight forward as possible. You will notice that the articles have few of the traditional business-to-business graphics, including color-coded sections and bright, multi-col-



ly topics are best covered on the rfdesign.com Web site. We also added a column by our tech editor, Keith Vick. This month, Keith reviews Noble Publishing's latest instructional CD series and electronic publications.

One thing that has not changed is our dedication to covering the issues that affect the wireless design industry. It may be a better package, but the content engineers have relied on for 25 years will remain. We will continue to bring you daily news, product releases and current industry events online, and practical articles and product profiles between the pages.

Look for more, although less drastic, changes to *RF Design* in the coming months, including an updated Web site and a new quarterly publication dedicated to defense electronics.

And as always, I welcome your magazine and industry comments and criticisms.

Todd Judd Erickson

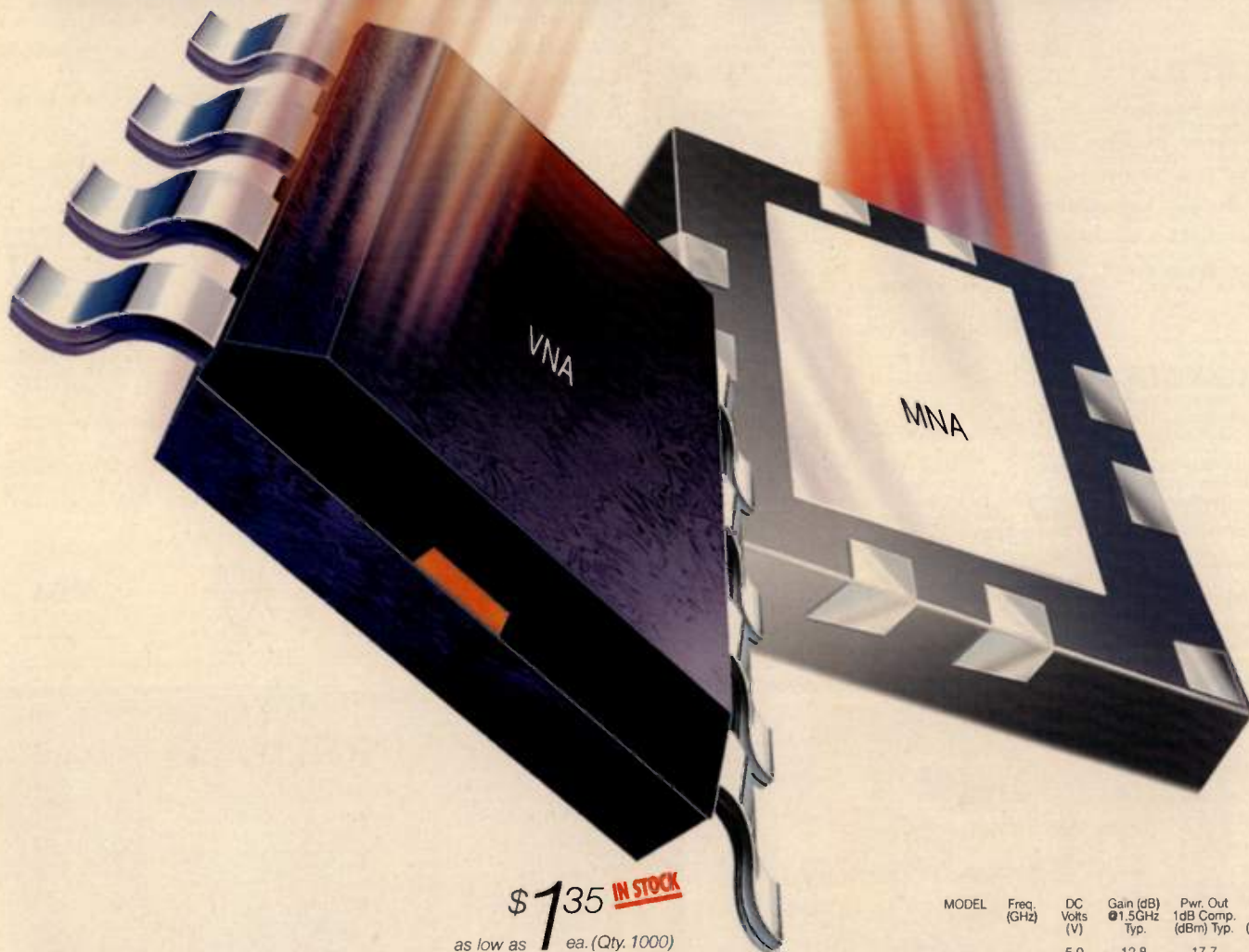
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RF Design September 2003

500MHz-5.9GHz

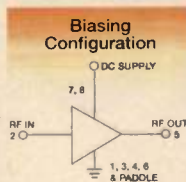
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MNA-7	1.5-5.9	5.0 2.8	15.9 13.7	15.6 12.7	2.25
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VAT-3	HAT-3	3	3	0.15 0.12	1.15 1.1
VAT-4	HAT-4	4	4	0.15 0.08	1.15 1.1
VAT-5	HAT-5	5	5	0.10 0.06	1.15 1.1
VAT-6	HAT-6	6	6	0.10 0.02	1.15 1.1
VAT-7	HAT-7	7	7	0.10 0.05	1.15 1.1
VAT-8	HAT-8	8	8	0.10 0.04	1.20 1.1
VAT-9	HAT-9	9	9	0.10 0.02	1.15 1.1
VAT-10	HAT-10	10	10	0.20 0.03	1.20 1.1
VAT-12	HAT-12	12	12	0.10 0.05	1.20 1.1
VAT-15	HAT-15	15	15	0.30 0.05	1.40 1.1
VAT-20	HAT-20	20	20	0.75 0.18	1.20 1.1
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WCDMA versus GSM: handset performance testing

While WCDMA technology may be on the brink of widespread rollout, its successful commercial deployment is gated upon the availability of wireless handsets that can provide a user experience that exceeds current GSM products. WCDMA test solutions must characterize the performance breakpoints of the all-new air interface technology, as well as evaluate the device's performance over a wide range of representative scenarios.

By Rob VanBrunt

Wideband Code Division Multiple Access (WCDMA) technology is on the brink of widespread rollout. This technology will initially complement and then eventually replace current Global System for Mobile Communications (GSM) systems as the mostly widely deployed air interface technology in the world. The successful widespread commercial deployment of WCDMA is gated upon the availability of wireless handsets that can provide a user experience that exceeds what is currently offered on the GSM networks. Legacy GSM handset test methodology was focused on conformance tests used to validate the underlying components of the air interface technology. However, the successful launch of WCDMA services will require a more progressive, integrated approach to evaluating the performance of WCDMA user equipment (UE). WCDMA UE test solutions must characterize the performance breakpoints of the all-new air interface technology, as well as evaluate the device's performance over a wide range of scenarios representative of the user's experience. Using the proper performance analysis solutions can reduce time to market and ensure customer satisfaction.

As was the case with GSM, the rollout of the WCDMA air interface technology is gated upon the availability of handsets that both interoperate with network infrastructure and provide a level of performance that ensures a satisfactory user-experience. In addition, the deployment bar has been set higher for WCDMA, as an abundance of mature GSM user services and third-generation (3G) hype have raised the market's expectations. Couple these factors with a more complex UE development process and increased pressure to shrink time to market and it becomes apparent

that UE developers and network operators must look for new, innovative ways to optimize product development and launch.

Handset development phases

Over the last 10 years, wireless handsets have evolved from voice-only telephony devices on proprietary platforms to voice and data-capable devices implemented on open mobile computing platforms possessing high-speed wireless connectivity. The development process used to realize and launch wireless devices has also grown more complex and distributed.

As shown in Figure 1, the development of a mobile device undergoes many overlapping stages.

Each stage has unique requirements for design verification and performance analysis tools. At a high level, these stages can be grouped into four phases: core platform development, product realization, product deployment and optimization, and application development.

Core platform development: This phase is either executed in-house from the ground up by a handset manufacturer or is performed by a third party technology provider that supplies turn-key reference designs. In either case, this phase includes the specification and implementation of the handset's physical layer (Layer 1) transmission scheme and access stratum call processing stacks (Layer 2 and Layer 3). The core platform development does not usually include the handset's final physical form factor or the user interface.

Product realization: Regardless of whether the core platform development was home grown or outsourced, handset manufacturers build a wide product portfolio of handset models leveraged on this underlying platform.

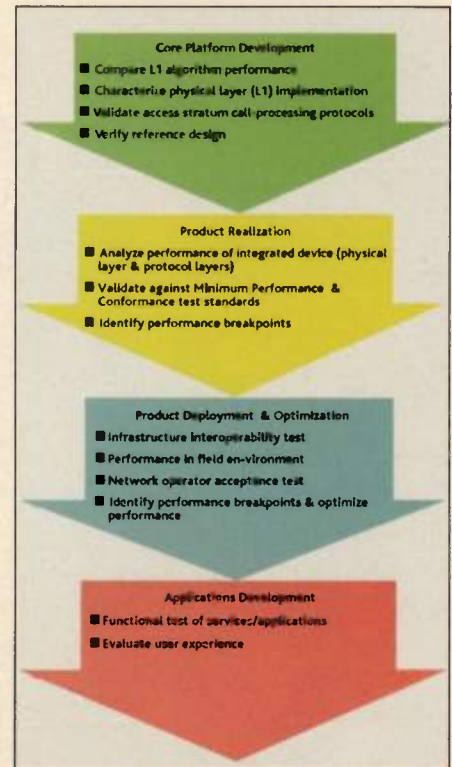


Figure 1. Performance analysis phases during UE product development.

Thus, the core platform undergoes a one-to-many transformation as it is used as the basis for a range of low to high-end devices, as well as devices targeted at specific geographic markets. The final form factor and specific user interface is implemented in this phase. During this phase handset manufacturers perform lab-based parametric and functional verification of the integrated handset to internal specifications and self-testing to industry minimum performance/conformance standards.

Product deployment and optimization: As a specific handset model approaches its launch date, a large suite of tests is performed both in the field and by third parties. This includes interoperability tests with infrastructure manufacturers, conformance validation to 3GPP specifications by independent test labs, and acceptance tests by network operators. During this phase, handset manufacturers optimize the performance of the device by adjusting physical and signaling layer characteristics based on analysis of the handset's performance in various test and user scenarios.

Application development: This is a relatively new phase in the handset product life

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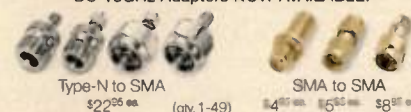
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S6W2	S6W5	N6W5	6	±0.40
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S8W2	S8W5	N8W5	8	±0.60
S9W2	S9W5	N9W5	9	±0.60
S10W2	S10W5	N10W5	10	±0.60
S12W2	S12W5	N12W5	12	±0.60
S15W2	S15W5	N15W5	15	±0.60
S20W2	S20W5	N20W5	20	±0.60
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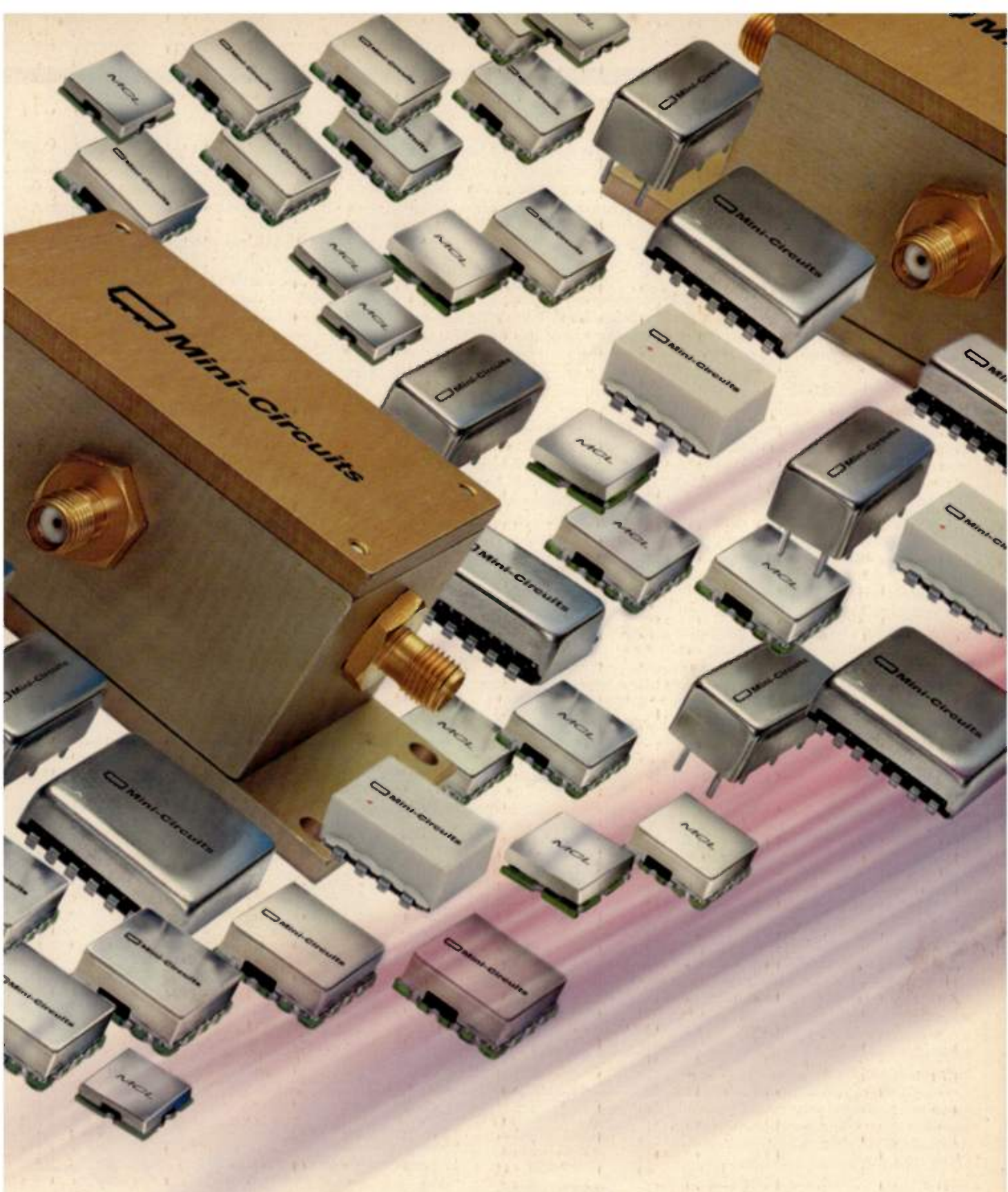
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cycle as mobile devices now feature an open platform on which third party applications, such as interactive gaming, can run. This phase plays a prominent role in the end-user's satisfaction with the handset as applications and user services are a key differentiator for manufacturers and network operators. This phase typically runs in parallel with the earlier three phases. Applications are developed and evaluated by original equipment manufacturers, third-party software application developers, and network operators.

WCDMA versus GSM

Although the GSM mobile development process has evolved over the past decade, it is important to compare the processes at the inception of each technology to have an appreciation of the challenges facing WCDMA deployment today. When the initial wave of GSM handsets appeared in the early 1990s, the product realization and performance analysis requirements were much different than today's WCDMA UE product development cycle.

Initially, underlying GSM handset hardware and software was developed for specific handset models rather than for generic platforms and, thus, the end-to-end product development process was much simpler and more centralized. A far smaller range of models was expected in the market.

Today's network operators demand a wide range of models to address markets spanning from the adolescent to high-end corporate user. There is a strong focus on accelerating time to market as devices have a much shorter shelf life since handset styles and features change as quickly as fashion trends.

The GSM air interface standard was created with voice as the primary application. WCDMA, on the other hand, includes support for voice, high-speed packet data, and multimedia applications. These applications are employed on a wideband-CDMA-based air interface and a completely different radio network. The UMTS specifications are orders of magnitude more complex than the GSM standard with the support of new applications and a new WCDMA radio network engineered for 3G.

The underlying WCDMA air interface is much more performance sensitive and its operation shares many more similarities with its rival CDMA2000 than its predecessor GSM. To achieve link-level performance gains over GSM's equalization and frequency hopping techniques, WCDMA uses rake receiver technology for diversity gain. The ability of the rake receiver to mitigate multipath interference and to perform soft-handovers must be evaluated over a variety of real-world conditions.

Overall WCDMA system capacity, a criti-

cal metric for network operators, has a soft limit dependent on interference levels and interference mitigation. WCDMA employs a fast power control scheme — 1500 Hz on both up and downlink — to deal with CDMA's inherent near-far interference issues. GSM, which features a hard capacity due to its fixed frequency reuse scheme, employs a very slow (2 Hz) power control scheme. Thus, finding the key performance breakpoints of the WCDMA air interface implementation has a direct correlation to WCDMA system capacity and network operator revenue.

With fewer features and a smaller number of infrastructure vendors, initial GSM interoperability tests required a smaller scale of test scenarios prior to launch. WCDMA's complex "future-proof" air interface standard allows many different ways to perform similar mobile functions, greatly increasing the change for signaling interoperability mismatches between handset and infrastructure.

Finally, early GSM handsets were built on a closed platform that did not allow the range of complex, high-bandwidth services and applications expected to be deployed on today's multimedia mobile devices. But over the years, a wide variety of mature user services have been deployed on GSM networks. WCDMA must initially, at least, equal and eventually exceed the services and performance available on GSM networks to accelerate subscriber adoption.

While the respective initial launches of

GSM and WCDMA share common trials and tribulations, the WCDMA design verification and performance analysis process must evolve to meet today's market requirements.

WCDMA performance analysis evolution

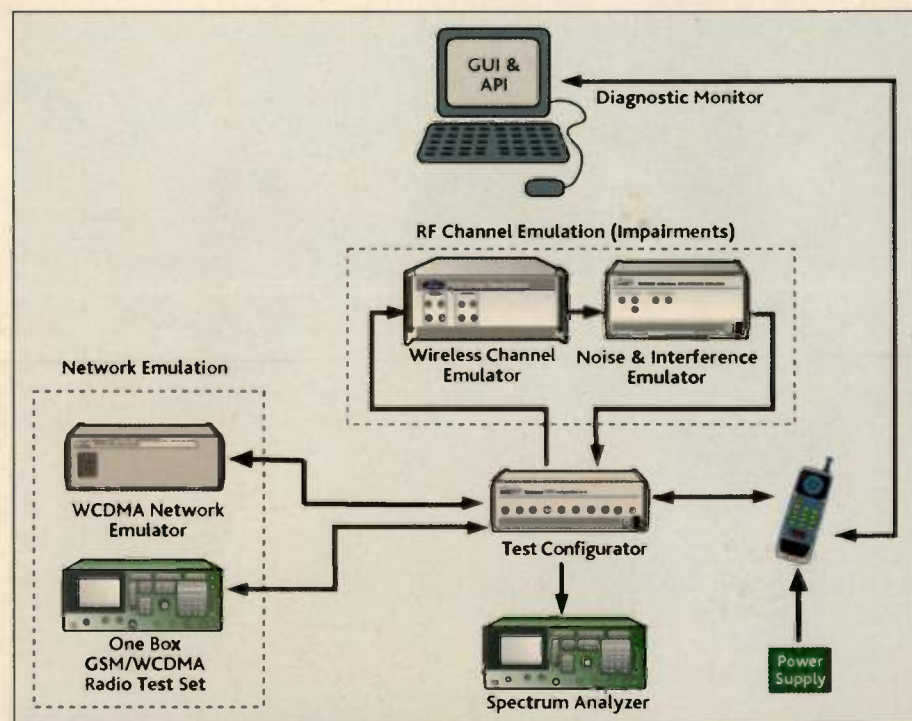
To meet the complex challenges associated with the deployment of WCDMA services, the development and design verification process for WCDMA UE's must evolve in several key ways.

Integrated test approach

Given that today's more complex handsets must reach the market faster with fewer issues, it is critical to employ an integrated approach to device verification during the product development lifecycle. It is highly desirable to push design verification as far back into product development as possible. This way design issues can be uncovered earlier and with less negative impact.

Since the overall design process has become more distributed across geographic locations, it is highly desirable to share common test tools between development and deployment stages and user groups to align test plans and results analysis. This also enables product evaluators further downstream in the cycle, such as network operators, to share test conditions and results with design engineers looking to recreate problems and to optimize product performance.

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advantages over unique, home-brew solutions. Commercial solutions can be easily replicated across development sites and between companies. To be effective, integrated test systems must include the key components shown Figure 2, enable manufacturers and network operators to focus their attention on analyzing product performance rather than developing unique custom test solutions.

Complementary mobile diagnostic monitoring tools are also useful to capture a hand-

set's detailed performance metrics during both lab and field tests simplifying the comparison of test results.

Inherent to utilizing common solutions across the product development cycle is that a wide range of users with unique areas of expertise will need to be able to operate the tools. Legacy GSM conformance test systems based on complex scripts require extensive protocol knowledge to operate and create new test scenarios.

These systems typically only address one

phase (such as the signaling protocol test) of the overall test requirement, making them inefficient and expensive. Next-generation WCDMA test systems address parametric physical layer performance analysis, as well as functional performance analysis of signaling protocols and user services.

Performance analysis

As discussed earlier, the WCDMA air interface is a much closer relative of CDMA2000 than it is to GSM. Both CDMA2000 and WCDMA employ CDMA technology that is highly performance sensitive. The evaluation handset characteristics such as rake receiver performance in the presence of dynamically changing multipath delay spread, or the transmitter's ability to respond rapidly to power control messages, is critical to predicting real-world performance. The ability to pass the minimum performance criteria outlined in conformance standards merely serves as a common baseline for qualifying potential handsets.

Network operators are concerned with predicting the quality of the end user's experience and with overall network capacity. These metrics require the handset to be evaluated past the specifications found in conformance standards to identify performance breakpoints under representative real-world conditions.

While systematic evaluation of each layer of the handset implementation is part of a structured test methodology, the functional performance of a handset must be analyzed, as well.

While voluminous, WCDMA conformance test specifications do not specify how the user interface of the handset should react to a call-waiting event, or how to display an incoming SMS message. Conformance test specifications cannot predict the latency of interactive gaming conditions under harsh mobile environments. However, these are critical elements of user/handset interaction that directly affect subscriber satisfaction.

Once the WCDMA industry is able to achieve basic interoperability and the air interface begins to mature, the focus will quickly shift to more extensive test methods to evaluate the functional performance of handsets from a user's perspective.

Test automation

More thorough testing prior to deployment, and a reduced time to market, are competing objectives that handset manufacturers must try to optimize in union with one another. Analyzing each of the individual layers of a handset implementation past minimum performance requirements generates a multitude of test scenarios. Functional testing is essential to verifying how the layers interact in user scenarios, but also makes the required test campaign grow even larger.

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As handset model turnover rate increases, the market window for a given handset design is shrinking. A handset launched several weeks late can have a negative impact on the handset manufacturer in the order of millions of dollars or Euros. To accelerate the launch of new handsets, manufacturers and network operators must take advantage of the tremendous efficiencies made possible through the use of test automation.

Test automation enables tests to be

launched and executed without the need for user intervention. This enables efficient use of valuable test equipment and human resources. Tests can be run 24 hours a day, seven days a week, to ensure maximum test coverage.

In addition to automating test execution, next-generation, integrated test systems automatically handle the translation of test settings into instrument settings, calibration and verification execution, and report generation and analysis.

To fully benefit from the gains possible through automation, the burden of handset control must also be removed from the user and be performed by the host system controller. Test platforms that enable flexible and powerful handset interfacing, also known as an *application programming interface* (API), enable key-strokes to be automatically emulated to initiate mobile-originated actions while simultaneously monitoring handset performance.

Conclusion

Given market expectations and the sophistication of the technology, WCDMA manufacturers and network operators are facing challenges much greater than experienced during the initial rollout of GSM service.

WCDMA handsets and their associated product development processes have increased in complexity and product launch windows are shrinking. In addition, advanced multimedia services have created an enhanced expectation of user experiences. To optimize the product realization process and to accelerate deployment, manufacturers and network operators must evolve their test methodology.

Using integrated, automated test solutions focused on performance analysis will enable more comprehensive evaluation of the end user's experience while still meeting time to market expectations.

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AC2205	100-2200	12.0	1.9	13.5	28/48	5	50
AC2208	200-2200	19.0	2.0	18.0	28/34	8	50
AR2538	10-2500	21.0	3.5	26.0	40/54	15	185
AC2554	1000-2500	25.0	1.9	15.5	26/45	5	72
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ABOUT THE AUTHOR

Rob VanBrunt currently supports product marketing activities for Spirent Communications Inc.'s (www.spirentcom.com) wireless performance analysis solutions division. His primary responsibilities include translating market direction, customer requirements, and new technology parameters into product offerings.

VanBrunt joined the company in 1990. During his tenure with Spirent, VanBrunt has held several positions within the organization, including director of business development, and product development manager. Van Brunt has written numerous trade articles on the advancement of wireless technology, including 3G technologies such as CDMA2000, and WCDMA.

VanBrunt graduated with honors from Rutgers University in 1989 with a bachelor's degree in electrical engineering. He is pursuing a master's degree in electrical engineering, specializing in RF propagation and wireless networks. VanBrunt can be reached at rob.vanbrunt@spirentcom.com

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By Ed Troy

There was a time when electronics for space and aerospace applications were very different from electronics for commercial applications. Aside from the obvious cost difference, electronics for aerospace applications were typically a few years behind electronics found in commercial applications. This was largely due to the fact that aerospace electronics had to be extremely reliable and, thus, only "tried and true" devices and technologies were used.

Unless a device or technology had years of history, its reliability was questioned. Thus, there always seemed to be a wide difference between commercial electronics and aerospace electronics.

Thanks largely to the cellular telephones, satellite television, and the popularity of GPS, today's aerospace electronics are truly state-of-the-art, and as technologically current as any commercial or industrial electronics. When new technologies and techniques are introduced into truly massive markets, such as cellular and the others mentioned, the reliability of these new technologies are thoroughly tested and evaluated in a very short period of time.

In the early 1980s, conventional wisdom was that GPS would only be used in military systems, and perhaps commercial aviation, since they were the only two segments of the market that could afford the estimated \$25,000 for even the least expensive receiver.

That all changed in the early 1990s when GPS receivers were slated to become the primary means of navigation for all segments of aviation, and when receivers could be purchased for the consumer market for prices ranging from a few hundred to a few thousand dollars. Today anyone can buy a GPS

receiver for less than \$100.

One of the primary drivers of this technology is the cellular market. Rapid advances in cost and size reductions have been made possible by the integration of large amounts of functionality into individual integrated circuits. A few years ago, if you wanted to design a receiver, you needed hundreds of parts, ranging from mixers and oscillators, to amplifiers and switches. Today, you can buy a complete receiver on a single integrated circuit. All that must be added is some peripheral components, such as capacitors, resistors, and inductors.

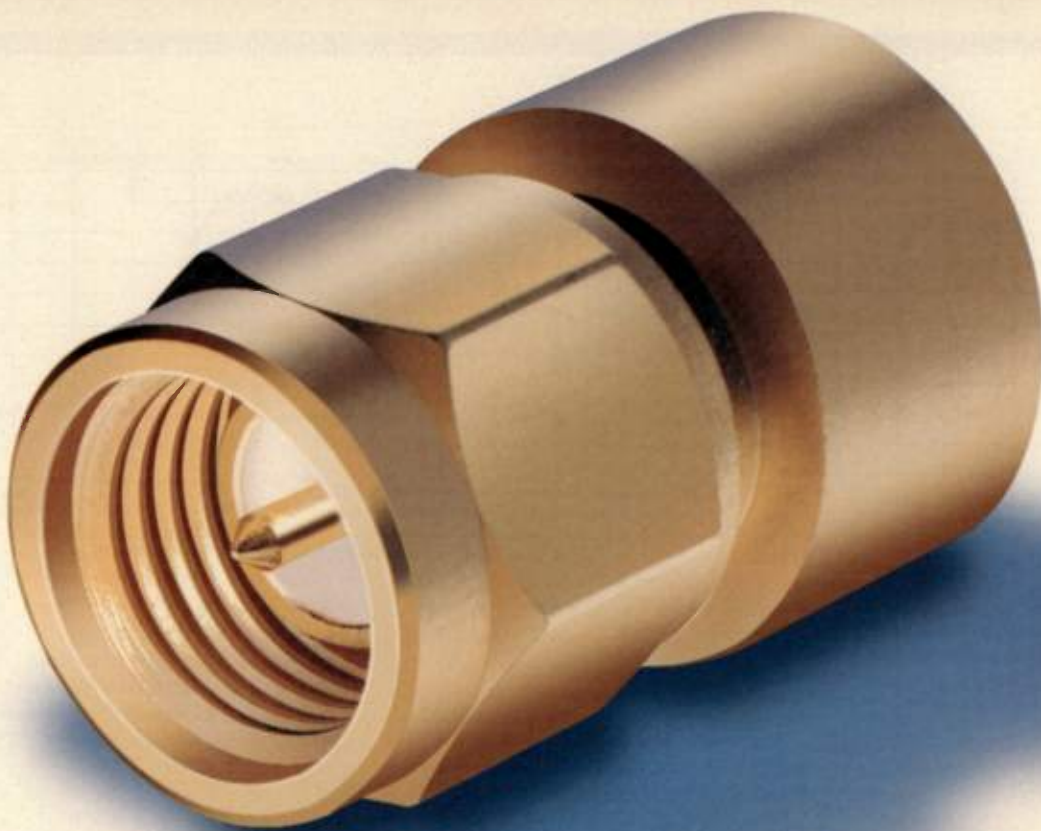
Interconnections

The increasing integration of functionality into increasingly complex and useful integrated circuits has had another advantage, however, that is critical to the aerospace electronics industry. Since one of the most common failure points in a circuit is the interconnections between components, if you reduce the total number of interconnects, you increase the reliability.

This fact is especially important when the systems are subjected to the extreme environments often seen by aerospace electronics. Since the overall mean time between failures (MTBF) is a function of the reliability of each



Figure 1: Old 10 W HFQT810, and new HFQT605 5 watt transmitter.



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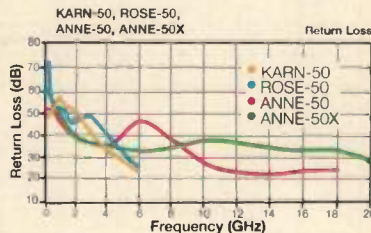
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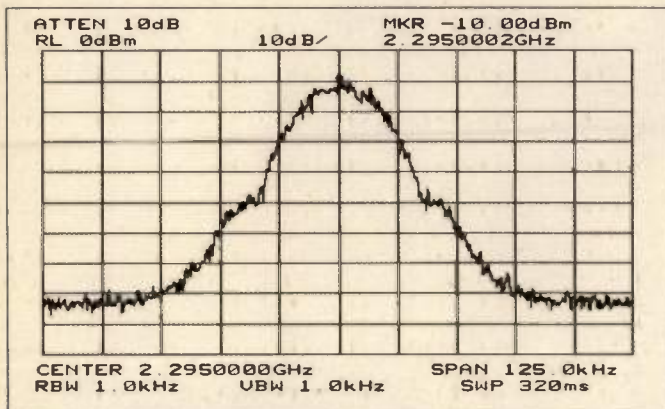


Figure 2: 25 kbps GMSK signal before nonlinear amplification.

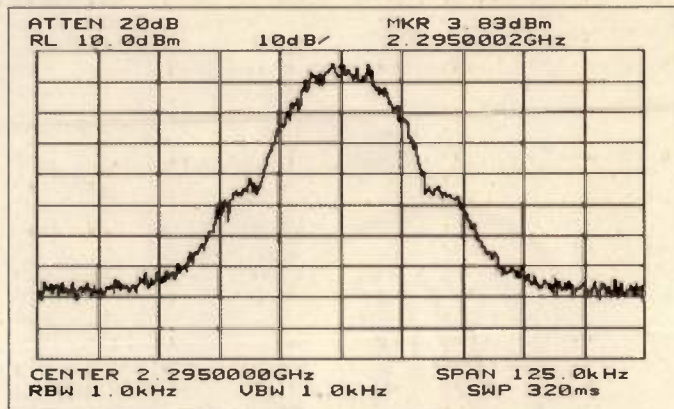


Figure 3: 25 kbps GMSK signal after nonlinear amplification.

of the individual components, if the overall number of components is reduced, the reliability increases. As you squeeze more and more functionality onto a given integrated circuit, you reduce the size and weight of the overall system. This, obviously, is an advantage for any electronic system that is destined for a space or aerospace application.

There have been other significant changes in the space and aerospace electronics technologies, however, and they relate to advances in signal processing and modulation techniques. Again, much of this is related to advances brought about by cellular technologies, as well as the rising popularity of wireless computer networks.

One of the biggest problems for the cellular industry has been accommodating all of the users in a given geographical area with limited spectrum. In the wireless data industry, the problem is to provide more usable bandwidth. Just as cellular phones have evolved from simple FM radios using analog modulation techniques, to radios that use complex digital modulation techniques to squeeze more and more users into a given spectrum allocation, radios destined for space and aerospace applications have evolved in a similar fashion.

One excellent example that shows how sig-

nificantly advanced modulation techniques can improve spectral efficiency is the Fehrer patented quadrature phase shift keying (FQPSK).

Using this technique, the spectral efficiency of a telemetry transmitter — used, for example, in an F/A 22 — can be doubled. This means that a transmission that had previously required 10 MHz of spectrum now only needs 5 MHz of spectrum^{2,3}.

An example of how electronics for aerospace applications have gotten both smaller, lighter, and more spectrally efficient, is the comparison of Herley Industries Inc.'s (www.herley.com) HFQT810 synthesized variable rate FQPSK telemetry transmitter, and its newest FQPSK transmitter, the HFQT605. As shown in Figure 1, the new transmitter is significantly smaller than the old transmitter. The old transmitter was also 10 watts, while the new transmitter is 5 watts, but this is not the major reason for the significant size reduction.

Generally, QPSK is not considered to be a spectrally efficient method of modulation. This is especially true when the transmitter must use a nonlinear amplifier to save over all power. This is one reason why gaussian minimum shift keying (GMSK), and other

forms of frequency modulation, are often preferred in applications, such as cell phones, where power is supplied from batteries, and the life of the battery is a critical consideration. Figure 2 shows a 25 kbps GMSK signal before being put through a nonlinear amplifier.

Figure 3 shows this same signal after being put through a nonlinear amplifier.

As you can see, there is very little spreading of the signal. This is because in the case of frequency modulation, the amplitude of the signal does not go through any major transitions. This cannot be said for most forms of phase shift keying.

Figure 4 shows a conventional QPSK signal before being sent through a nonlinear amplifier.

Already, you can see that it is not as spectrally efficient as the GMSK signal. And after that signal is sent through a nonlinear amplifier, the spectral efficiency degrades even further, as shown in Figure 5.

In the case of FQPSK, however, this spectral spreading problem does not exist. In fact, as shown in Figure 6 and Figure 7, respectively, the signal is even more spectrally efficient than GMSK, and there is no additional spreading after the signal is sent through a nonlinear amplifier.

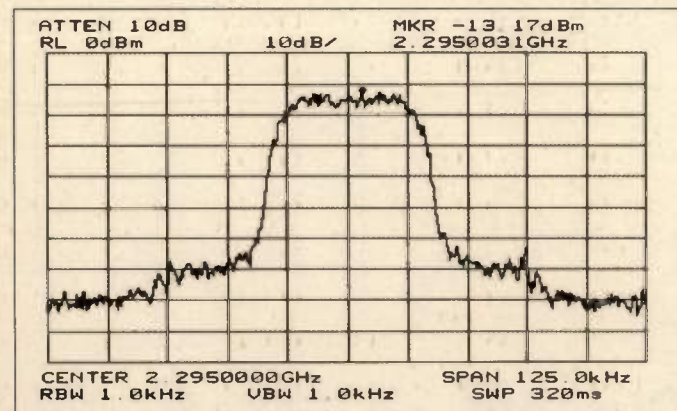


Figure 4: 25 kbps QPSK signal before nonlinear amplification.

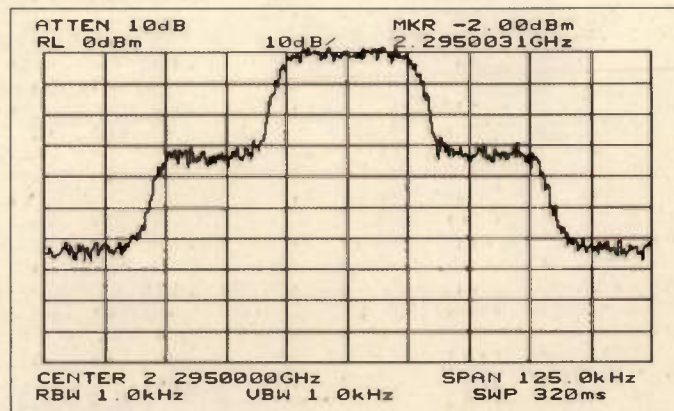


Figure 5: 25 kbps QPSK signal after nonlinear amplification.

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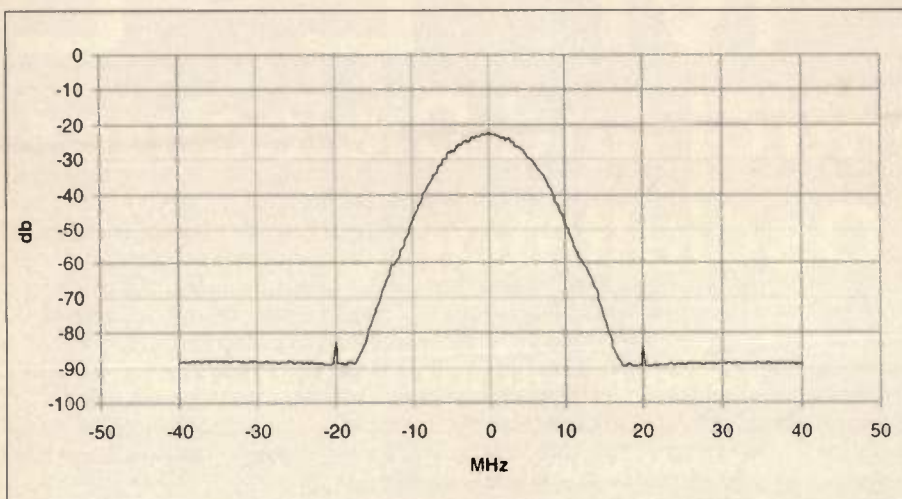


Figure 6: 20 Mbps FQPSK signal before nonlinear amplification.

Feher-patented quadrature phase shift keying (FQPSK)

This spectral efficiency is made possible by the modulation technique patented by Dr. Kamil Feher known as *FQPSK*. In this technique, wavelets are used in a very clever way to ensure that the QPSK signal does not go through any amplitude transitions as the various bits of information are transmitted. In QPSK, information is transmitted two bits at a time. Table 1 describes the four possible data bytes and their corresponding phases.

These are shown graphically in Figure 8.

When looking at Figure 8, the proper way to interpret the graphic is to think of the length of the line from the origin to the dot as the amplitude of the signal, and the angle of the line as the phase of the signal.

Thus, a "11" is represented by a signal with magnitude 1 and an angle of 45 degrees. In the same way, a "00" should be thought of

I data	Q data	Phase
1	1	45
0	1	135
0	0	225
1	0	315

Table 1. The four possible data bytes used for QPSK, and their corresponding phases.⁴

as a signal with an amplitude of 1, but a phase of 225 degrees.

The interesting concept is what happens when you transition from, for example, a "11" to a "00." With traditional QPSK, the signal would have to follow the line through the origin from a magnitude of 1 at a phase of 45 degrees, to a magnitude of 1 with a phase of 225 degrees.

During that transition, the signal would pass through the origin, thus going through an

amplitude of 0. This creates a severe amplitude change, producing a wide spectrum, like any pulse amplitude modulated signal.

Of course, the waveform can be filtered to lessen the amplitude changes, and by doing so reduce the width of the spectrum, but it still produces a wide spectrum. And, if this signal is then fed into a nonlinear amplifier, the spectrum that was saved by the filtering of the waveform is regrown.

Even in the situation where the transmitted bytes go from "11" to "01", for example, the amplitude of the signal will still go through a reduction to approximately .707. This is not quite such a major change in magnitude, but it is still a magnitude change, and as a result, will produce a wide spectrum.

A further look at the graph in Figure 8, and a little imagination, might suggest a solution to the problem. What if the signal was encoded in such a way that the transmitted waveform could never transition through 0 amplitude?

This would prevent the pulse-like spreading created by a transition directly from, say, "11" to "00," or "01" to "10." Furthermore, what if the waveform was forced to follow a circular trajectory from, for example, "11" to "01," or "10" to "11," as shown in Figure 9?

Now, there are no amplitude transitions, and, thus, no spectral spreading, or regrowth, after nonlinear amplification. It is, intuitively, relatively easy to see what has to be done in the case of transitioning from "11" to "01," or "10" to "11." What is not so intuitive, however, is how it gets from "11" to "00," or "01" to "10?" This is where wavelets come into play.

Most complex modulation schemes use an I/Q modulator to create the final signal. With the I/Q modulator, there are two waveforms that are multiplied together to produce the final waveform. These waveforms, like any other waveform, consist of magnitude and phase information. Looked at another way, at any given instant in time, these waveforms have a definite amplitude.

The final waveform has an amplitude that corresponds to the instantaneous product of the amplitudes of the I and Q waveforms. The *trick* used by FQPSK is to pick those waveforms so that at any given instant, the final, modulated waveform has a constant amplitude.

In other words, if the I channel waveform was at its maximum at one given instant, the Q channel waveform would be at its minimum at that moment. There are only 16 possible transitions for a byte consisting of two bits — "00" to "00," "00" to "01," "00" to "10," etc.

Because of this, a look-up table can be created that contains the 16 necessary waveforms for the I and Q channels. Then, depending on the data and the data transitions, the appropriate waveforms are selected and applied to the I and Q channels.

If these basis functions are properly cho-

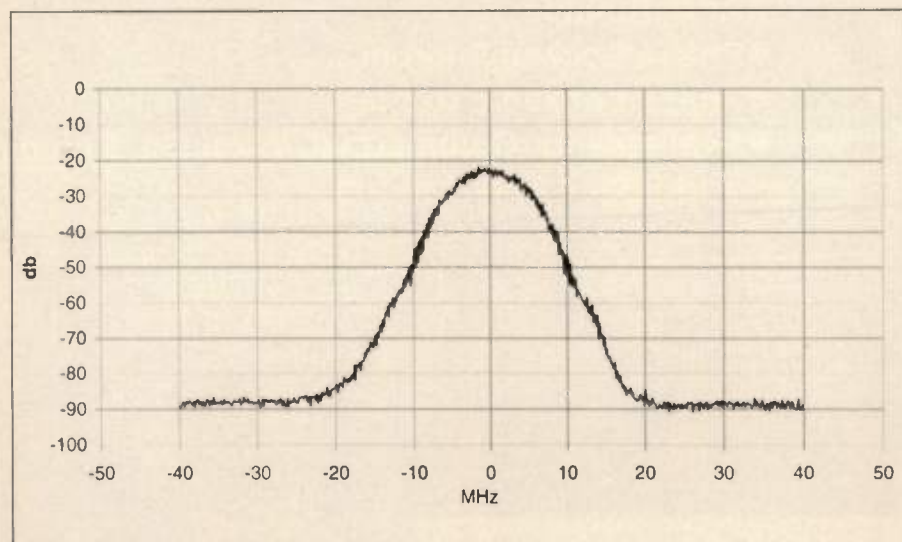


Figure 7: 20 Mbps FQPSK signal after nonlinear amplification.

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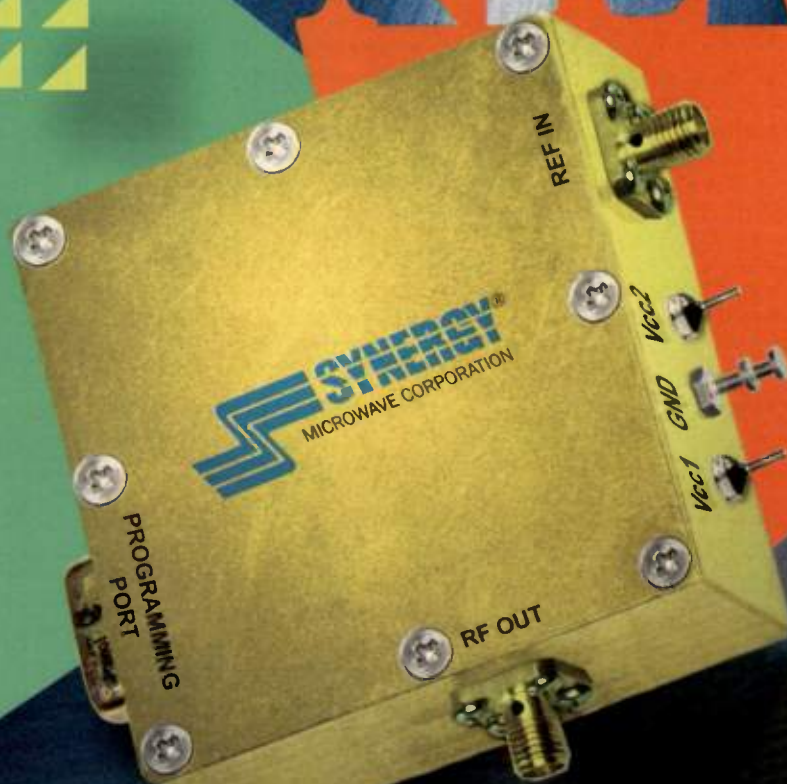
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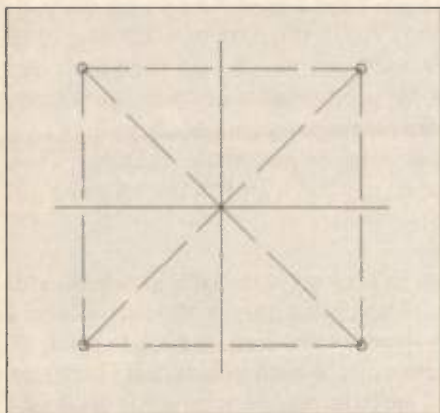


Figure 8: Simple QPSK constellation and transitions.

sen, the system follows an almost perfect circle, as shown in Figure 9, and there are no amplitude variations. Thus, the system uses a minimal amount of spectrum, and no spectral regrowth is seen when it is passed through nonlinear stages of amplification.

GPS translator

Another interesting use of technology is the GPS translator. This product is mounted on a missile, and allows for precise tracking

of that missile by interpretation of the translated GPS signals.

In a normal GPS system, there are two signals, the L1 signal, at 1575.42 MHz, and the L2 signal, at 1227.6 MHz. These signals can be used to accurately locate an object in latitude, longitude, and altitude. However, the most precise accuracy is obtained by using differential GPS.

In differential GPS, the signals from a GPS constellation is monitored at a known (accurately surveyed) location. Under the assumption that another GPS receiver is receiving signals from the same constellation of GPS satellites, and that it is within a few hundred miles of the reference station, the precise location of that other GPS receiver can be determined by subtracting out the errors in latitude, longitude, and altitude that are being measured by the reference receiver. (After all, they are both receiving the same signals and those signals are passing through a similar electromagnetic path, and thus they should have virtually identical errors.)

The GPS translator works by taking the GPS signals received by the missile, and frequency shifting those signals to a standard telemetry band. Then, that data is transmitted to the tracking station in real time. There, it

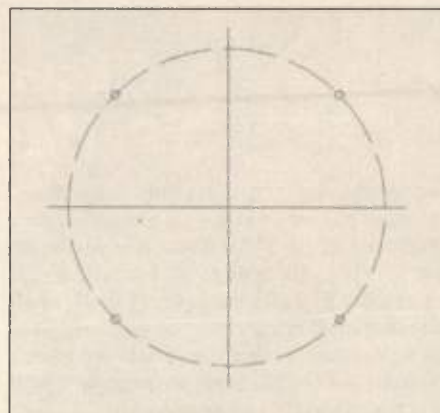


Figure 9: FQPSK constellation and transitions.

can be stored for later analysis, as well as compared with GPS data received by the reference station, to produce a real time, highly accurate position for the missile.

While this sounds almost trivial, it is extremely complex. For one thing, GPS signals are spread spectrum signals, and they are widely spread. In fact, they are spread so widely that a GPS signal is well below the level of the background thermal noise.

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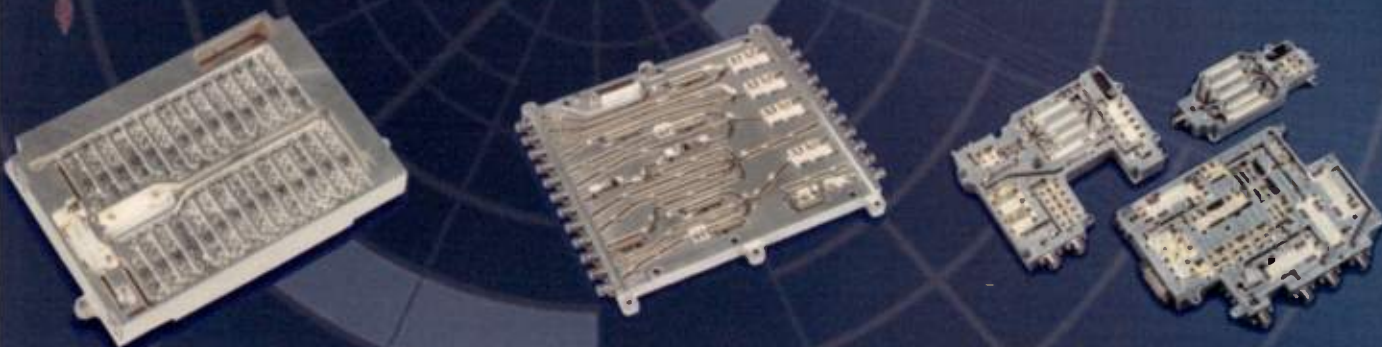
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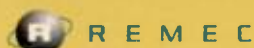
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ful after they are de-spread. This means that the system must be designed in such a way that virtually no extra noise is added to the signal. The more noise the system adds, the more difficult it becomes to eventually de-spread the signal and determine useful position information.

Also, if the highest degree of accuracy is to be obtained, the precise phase characteristics of the signal must be preserved. This further complicates the translator system.

Other complications include the fact that the missile is a highly dynamic vehicle. For this reason, multiple GPS antennas must be placed onto the missile and the various signals from these antennas must be multiplexed and inserted into the data stream.

In the case of the Herley Industries GPS translator system, there are four antennas that get multiplexed into three data channels, and these three data channels are then translated into a telemetry band, amplified, and sent to

the tracking station for analysis.

These two systems demonstrate the cutting edge of aerospace electronics. They make extensive use of the latest technologies in the areas of laterally diffused metal oxide semiconductors (LDMOS) devices, integrated sub-circuits, and modern ceramic and saw filter technologies, as well as the one of the most spectrally efficient modulation techniques available today to systems where power efficiency is a critical concern.

Both of these systems demonstrate the rapid migration and adoption of technologies and techniques that were made possible, in large part, by the technological advances brought about by the cellular and wireless data markets.

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Acknowledgements

The author expresses his appreciation to Neal Kresge and Vern Moore, both of Herley Industries Inc. (www.herley.com), for providing some of the data in this article.


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Ed Troy is an engineering consultant with over 28 years of experience in the design, development, simulation, analysis, and prototyping of electronic circuits and systems. He received a B.S.E.E. in 1975, and an M.S.E.E. in 1997, both from Lehigh University, where he also performed doctoral-level research.


He started consulting in 1983 on a part-time basis, and has been a full-time consultant for the last 14 years. Most of his work is in the area of RF, microwave, and analog circuit and system design and development. He has a full suite of software, as well as a fully equipped laboratory, allowing him to work to 26.5 GHz. He can be reached at etroy@aeroconsult.com.

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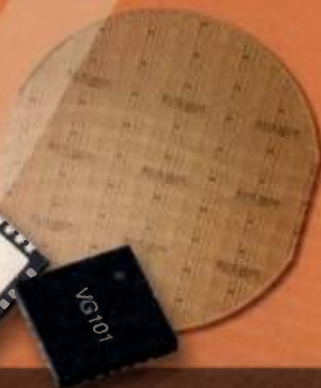


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Bluetooth shifts up a gear: Intelligent tools solve in-vehicle RF range and interference issues

In-vehicle broadband services offer a huge potential market for Bluetooth technology. But interference from existing in-vehicle RF devices can be detrimental to Bluetooth broadband signals and existing interference defenses may not provide adequate protection. Channel quality driven data rate (CQDDR) is a Bluetooth option that promises to ensure optimum data throughput.

By Ken Noblitt

Hands-free mobile phone operation in vehicles offers a huge potential market for Bluetooth, and kits are already finding their way into both after-market solutions and embedded designs. Alongside hands-free mobile phone operation, future Bluetooth applications in-vehicle will include Internet access, wireless additions to the infotainment system, vehicle personalization and even vehicle diagnostics.

To make all of this possible, there are problems that must be overcome.

Other RF devices, such as car stereos, global positioning system (GPS) navigation equipment, satellite digital audio radio services (SDARSes), GSM transceivers and other electrical devices, that are already in-vehicle can cause interference or be susceptible to interference.

Also, think of a car as a reflective *tin-can*, where radio waves are reflected within the vehicle cabin, which results in a phase shift that, with superposition, can effectively cancel out or corrupt the wanted signal.

All this RF activity can be detrimental to the data throughput of an in-vehicle wireless system. As the applications for Bluetooth expand, Bluetooth modules are likely to become more widespread around the car, further compounding the potential interference risk.

Existing interference defenses

Bluetooth already has an existing arsenal of defenses to combat interference designed into the standard. But the unique and difficult conditions within a car have forced designers to sharpen their swords to lessen the considerable potential effects of interference.

One of Bluetooth's standard weapons is frequency hopping, which requires both the receiver and transmitter to tune/hop to one of its 79 different channels 1,600 times per second in a predetermined pattern.

This provides a good level of immunity to interference. If a data packet is lost or received incorrectly, no acknowledgement will be returned, and a retransmission will be

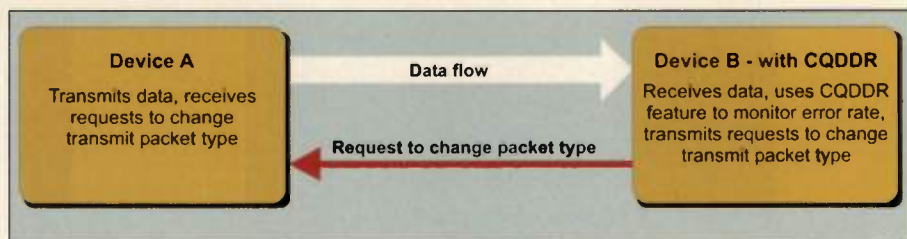


Figure 1. Effective bandwidth plotted against increasing BER.

sent at the next available time slot.

By utilizing frequency hopping technology, and with care taken to separate the Bluetooth antennas from other sensitive in-cabin receivers or transmitters, interference can be minimized. But even with these measures in place, a high amount of in-vehicle RF activity can be detrimental to data throughput and link reliability.

less equipment operating in the same band (such as Wi-Fi).

The Bluetooth standard offers a range of data packet types, known as *DH* and *DM*. *DH* types have higher payloads; *DM* types support only medium payloads, but include forward error correction for integrity in noisy operating conditions.

All have cyclic redundancy checks (CRCs)

To ensure a good user experience, packet types must be chosen not just on the basis of how much data is waiting to be sent, but also on the ambient error conditions, which can greatly vary in a vehicle cabin.

Channel quality driven data rate (CQDDR)

Channel quality driven data rate (CQDDR) is a Bluetooth option that ensures that products will achieve the optimum data throughput.

Most Bluetooth products support all data packet types. However, if the IC's firmware decides to employ a type that doesn't match the noise environment, a designer can end up with a very inefficient communications link. This is because of noise, caused for example, by users pushing products beyond their limits for range and noise immunity, and other wire-

less equipment operating in the same band (such as Wi-Fi). The payloads of *DM* packets are divided into blocks of 10 bits, with an additional five bits for forward error correction. These can be used to detect and correct all one-bit errors, and to detect and reject all two-bit errors in each 10-bit block.

Although *DH* packets, particularly *DH5*, seem to give the best performance, in the real world things aren't so simple. To ensure a good user experience, packet types must be chosen not just on the basis of how much data is waiting to be sent, but also on the ambient error conditions, which can greatly

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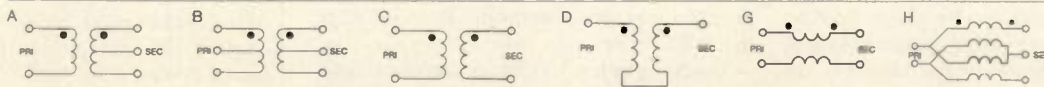
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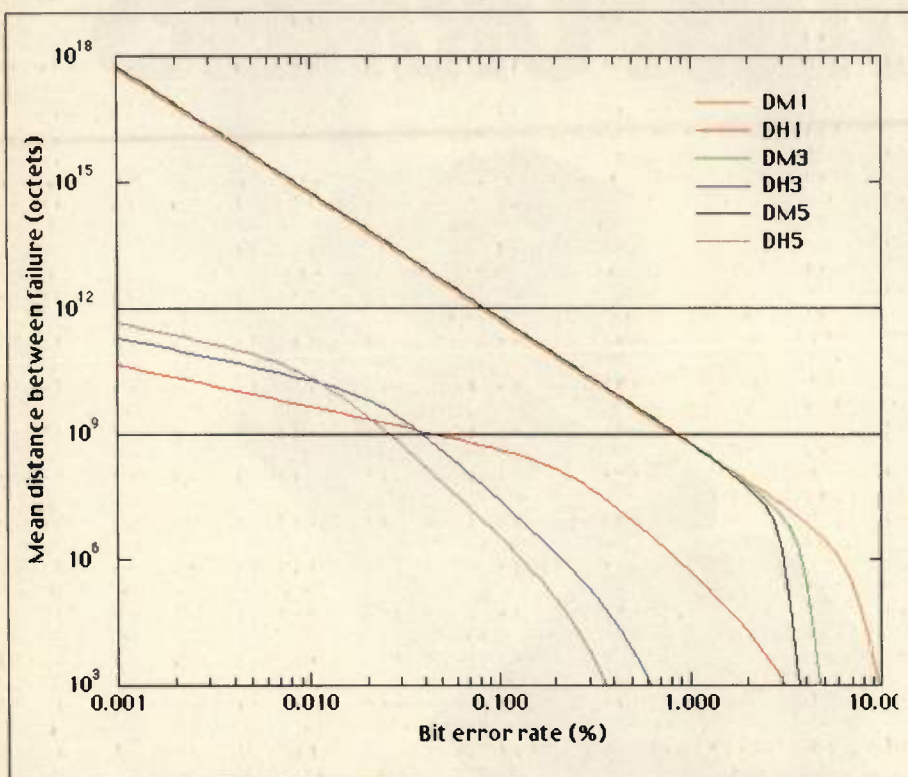


Figure 2. CQDDR lets Bluetooth device dynamically switch packet types according to link conditions.

vary in a vehicle cabin. There are several possible ways this can be achieved within the current specification.

Designers of each layer of the stack can choose either to add an extra layer of error detection, and optional correction, to their layer, or they can pass on the data unmodified.

The former allows them to make a stronger reliability guarantee than the layer below, whereas the latter keeps the layer overhead low.

A simplistic baseband implementation may choose the packet type purely on the number of octets it has waiting to be sent. This means that when there are many octets waiting, it will choose DH5 packets, as these have the largest payload.

In laboratory conditions, this may look like a good solution, but users will ultimately be frustrated. At a bit error rate (BER) of 0.04 per cent, for example, DH5 packets have only a 33 percent chance of being received without error.

CQDDR allows a receiving device to negotiate with the transmitter to change the transmitted packet type according to the conditions experienced at the receiver.

In particular, the overhead for error correction (as opposed to mere detection) is high. Typically, all the data sent by a layer must be buffered in that layer until it is acknowledged (implicitly or explicitly) by the other side. As flow progresses up the stack, the data transfer latencies get higher, and, hence, the amount of buffering increases.

In other words, it will take an average of three attempts to send a packet — reducing potential maximum bandwidth from 723 kbps to just 241 kbps.

On the other hand, DM5 packets show virtually no degradation from their maximum bandwidth of 477 kbps until 10 times that BER.

There is a mechanism built into the

Bluetooth scheme (version 1.1 of the Bluetooth specification), which, if correctly implemented, solves range and constant interference issues, that being CQDDR.

CQDDR allows a receiving device to negotiate with the transmitter to change the transmitted packet type according to the conditions experienced at the receiver. It requires access to packet and BER statistics to make an intelligent trade off between bandwidth and data integrity. With CQDDR, if one side finds that it's receiving packets with many errors, it tells the other side to switch to DM packets. If the link clears up, then it can allow the other side to use DH packets again.

Surprisingly few companies have implemented CQDDR in their firmware in spite of the great improvements it brings to data transfer and link reliability in environments, such as a vehicle cabin.

The incredible amount of in vehicle functionality that Bluetooth could enable requires thought and foresight to implement. By taking care to consider the entire vehicle system, automotive designers can avert many of the problems associated with implementing a Bluetooth system.

Interference control is a vital element for any RF designer, and the vehicle environment only magnifies this factor. With a number of safeguards already put into place in the Bluetooth standard, designers are almost there. CQDDR offers the opportunity for automakers and OEM suppliers to ensure interference is not an issue and to deliver on Bluetooth's promise of a multifaceted wireless connectivity.

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Ken Noblitt is the technical development director for CSR Inc. (www.csr.com). He holds an M.S.E.E. from Southern Methodist University, a B.S.E.E. from The University of Texas at Arlington, and has 22 years of experience in many different spread spectrum systems in the commercial, government and military sectors.

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Low power design techniques for high-speed programmable Infosec systems

System-on-a-chip (SoC) ASIC technology is one of the most effective ways to produce high-speed, low-power products. Various techniques can be used to reduce the power consumption of SoC designs, however, many may not be adequate to meet programmable Infosec device requirements. This paper will consider specific low-power techniques for different classes of algorithms.

By Todd Moore
and Rick Schmalbach

Many of today's high assurance embedded systems require highly capable, high-speed cryptographic solutions. Many applications need to sustain lengthy mission profiles using standard, commercial battery technology (such as unmanned aerial vehicles, smart sensors, smart munitions, and handheld soldier radios). Low power consumption is essential to the success of these missions by maximizing the application's battery life. This paper will describe various techniques that can be used to meet these programmable Infosec systems' requirements.

FPGA power consumption

Programmable Infosec solutions typically have been composed of large FPGA-like programmable elements capable of implementing a variety of cryptographic algorithms. These programmable elements require complex structures that need large numbers of gates. Incorporation of these elements inflates the die size, increases cost, increases power, and reduces the maximum operating frequency.

The dynamic power consumption on FPGAs can be separated into three parts: datapath, synchronization and off-chip power.

- Datapath corresponds to the combinational blocks and associated interconnection power.
- Synchronization is the consumption by registers, clock lines and buffers.
- Off-chip power is the fraction dissipated in the circuit output pads.

Knowledge of the relationship between these components for a given FPGA technology is fundamental in calculating an FPGA-based system's power consumption¹.

The power consumption of the datapath interconnection (programmability) is the highest of the three parts and will increase lin-

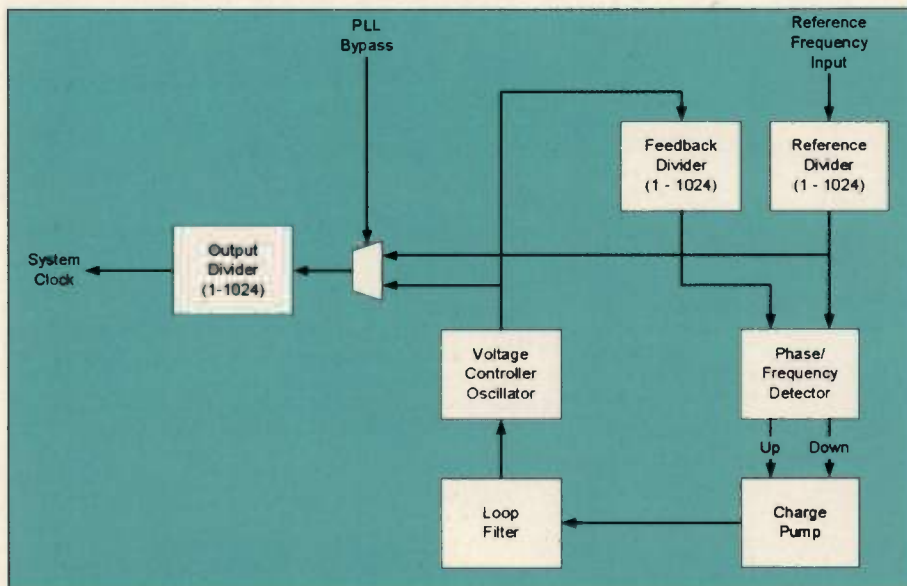


Figure 1: Clock generator block diagram.

early based on the input clocking frequency. Various techniques (including pipelining and partitioning) can be applied to an FPGA design to reduce this datapath power consumption¹. Even though an FPGA-based design provides the highest degree of flexibility and programmability, it also consumes the largest amount of power.

System-on-chip designs

One alternative to an FPGA-based design is a system-on-chip (SoC) application specific integrated circuit (ASIC). The SoC ASIC provides the optimal mix between hardware and software, allowing functional components to be partitioned to provide the best mix of speed and power enhancements.

In particular, components that can gain from the benefits of hardware implementation will be implemented in hardware accelerators and discrete logic. Software is written to provide the necessary hardware initialization and configuration, but many time-extensive, number crunching operations (such as power-hungry) are provided by the hardware.

Overall, the power-budget of a SoC ASIC will be much less than an FPGA-based design. The tradeoff is that programmability will be limited to the flexibility of the hardware accelerators. Lower power consumption (and subsequent higher speeds, in some cases) may be an acceptable compromise for many power conscious applications. Additional hardware interfaces, as well as

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software functionality, will help offset any programmability concerns.

Power reduction techniques

Various techniques can be used to reduce the power consumption of SoC ASIC designs, including dynamic frequency control, dynamic power management and the ability to idle embedded processors.

An SoC ASIC external reference clock and internal clock generator can be used to provide dynamic frequency control. The reference clock frequency is proportionally related to the SoC ASIC's power consumption (e.g. lower reference clock frequency results in lower power consumption).

The reference clock is provided by the system (host) and can be scaled (externally) based on the intended mode of operation. An internal clock generator can also be used to scale system clock frequencies (and power consumption) dependent on the desired mode of operation. This internal clock generator will contain a PLL used for setting the internal clock rate.

The PLL logic contains three programmable dividers designated as reference, feedback, and output. The maximum and minimum values of the reference clock frequency input and the VCO output affect the phase jitter, which affects the ASIC's performance. Figure 1 shows a sample PLL-based variable clock-generator circuit.

Disabling, or *turning-off*, the internal clock to unused or idled functional SoC ASIC sub-

blocks will decrease the amount of power consumed. For example, every piece of logic hardware (or gate) that is clocked will consume some amount of power. By applying the appropriate amount of dynamic clock control or power management, the amount of power consumption can be reduced signifi-

Various techniques can be used to reduce the power consumption of SoC ASIC designs, including dynamic frequency control, dynamic power management and the ability to idle embedded processors.

cantly for a specific mode of operation.

Dynamic power management requires some degree of up-front planning and organization. The SoC ASIC needs to be divided into the appropriate functional blocks to ensure that the maximum benefit can be achieved by disabling a specific piece of the hardware design.

The SoC ASIC will need to contain the logic necessary to control power up, power down, and reset of individual function blocks. This may include a clock tree register that enables or disables the clock to a specific functional block.

Each functional block can be powered down by setting the appropriate power down bit in

this register that disables the clock to that block. Each functional block can also be initialized to a known state by setting the reset bit. Dynamic power management is an internal SoC ASIC function controlled by external software.

Some SoC ASIC designs contain an embedded processor. Software is written for

this processor to perform the necessary configuration and control operations. Most modern-day embedded processors contain an instruction that will place the processor into an idle, or *sleep*, state. Once the processor enters this state, only an external stimulus (such as defined interrupt) can wake-up the processor.

The processor will consume a very minimal amount of power while in the idle state. This low power consumption is a benefit for SoC ASIC designs assuming that no, or limited, software intervention is required for a particular function.

Once the SoC ASIC has been configured, the processor can idle itself and only be utilized during specific times (such as initialization or mode change). A complete up-front system design and hardware/software partitioning is required to reap the maximum benefits of processor idling.

These techniques can be generically applied to SoC ASIC designs, but may not be adequate in themselves to meet programmable Infosec device requirements. The SoC ASIC approach may need to be extended to programmable Infosec devices by dividing the composite set of cryptographic algorithms into classes and applying optimal hardware/software tradeoffs.

Infosec considerations

A SoC ASIC approach can be applied to today's cryptographic algorithms to meet Infosec device requirements. By reviewing the requirements for various cryptographic algorithms, the maximum benefit from the SoC ASIC technology and low power consumption can be achieved.

Cryptographic algorithm functionality can be broken down into several types of classes, parallel and serial. Other unique cryptographic functions, including pattern detection, shift-registers, multiplication, randomization, hash, permutation and combining can be optimized in hardware.

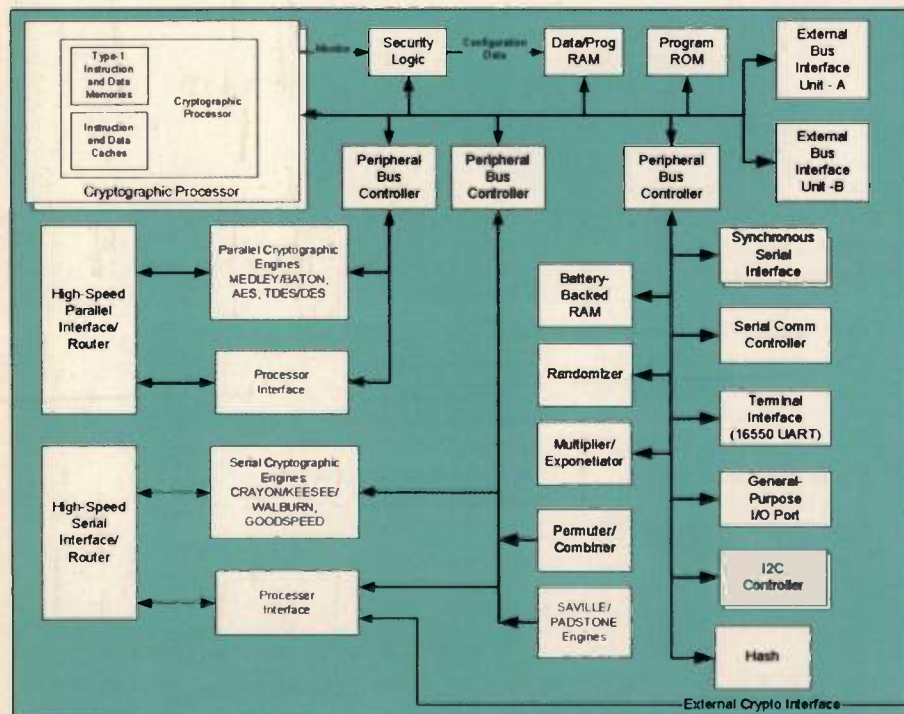


Figure 2: Detailed ASCII block diagram.



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The appropriate segmentation of each cryptographic algorithm will ensure that the optimal engine interface can be designed, thus reducing the amount of required software intervention. Optimizing interfaces to a specific cryptographic engine will reduce the time needed to perform various types of bit manipulation. For example, data conversion from a serial to a parallel interface is both time and power consuming. Cryptographic engine segmentation will produce the maximum clock and power control.

Dynamic frequency and clock control, processor idling and functional grouping are common techniques to provide low power consumption for SoC ASIC designs.

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Cryptographic engines can be grouped into two types of classes: parallel and serial. Parallel engines are designed to interface directly with first-in-first-out (FIFO) buffers to provide high-speed data throughput. Serial engines interface to serial channels using a selector or router with various serial transceivers. In general, legacy algorithms relied on serial engines where newer algorithms use parallel engines.

Interactions between various cryptographic engines of the same class should utilize a common bus with a common controller. Each class of cryptographic algorithm should have its own bus controller. This architecture allows various cryptographic engine classes to be disabled (not clocked) for minimum power consumption.

Hardware functions required by both the parallel and serial engines should also reside on their own unique bus structure. A particular cryptographic engine class may only need some hardware functions. In this case, the hardware function should be optimized for that cryptographic engine. For example, a permuter/combiner function is only required for serial cryptographic engines and should be optimized for their use.

The parallel and serial engines may also provide connectivity to a processor to allow the processor to manipulate a particular data or traffic stream. For example, allowing the processor to generate or decode cryptographic preambles or packet header information. This type of processor intervention should be limited as there is a direct correlation between processor intervention and higher power consumption.

Cryptographic ASICs

An example of a partitioned cryptographic engine SoC ASIC is shown in Figure 2, a Harris Corp. SoC ASIC (referred to as the *Raven ASIC*) Sierra II module programmable, embeddable cryptographic Infosec module.

The Raven ASIC contains redundant RISC processors and partitioned serial and parallel cryptographic hardware accelerators. The processors perform the overall control functions, command decode processing and data flow to and from the peripherals and input/output ports.

The ASIC was designed with power consumption in mind. Through the proper classification of the cryptographic engines and basic power management design techniques, the Raven ASIC provides lower power consumption.



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tion in many applications. The ASIC's clock rate can be dynamically varied to the minimum necessary rate for a specific application (function). The ASIC was designed (partitioned) such that the clock can be turned off to circuit blocks that are not in use. The RISC processors can be disabled when not in use.

Conclusion

Through the proper partitioning and classification of hardware and software require-

ments, optimal SoC ASICs can be designed and developed. Dynamic frequency and clock control, processor idling and functional grouping are common techniques to provide low power consumption for SoC ASIC designs. □

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Rick Schmalbach has been involved in the design and development of Infosec systems for over 20 years, primarily in the areas of link encryption and tactical communications. He is currently leading the system design and certification effort on the Sierra II programmable cryptologic module for Harris Corp., and is involved in developing Sierra II applications.

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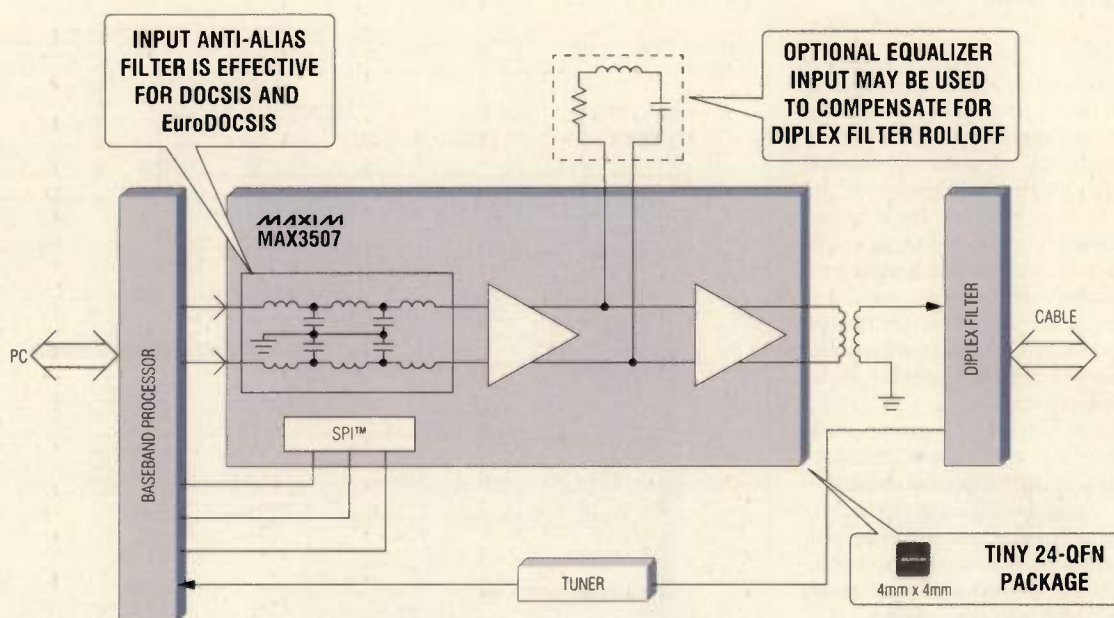
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Multitone IMD offers clearer picture of MCPA performance

Characterizing distortion is essential when evaluating multicarrier power amplifier (MCPA) performance. Typically, these amplifiers must be evaluated using multiple carriers as stimulus to more realistically simulate service conditions. As an alternative to multiple carriers, multiple tones with the proper phase relationships can be used to accurately represent multicarrier signals.

By Marta Iglesias

Characterizing distortion is essential when evaluating multicarrier power amplifier (MCPA) performance. Traditional two-tone tests for intermodulation distortion (IMD) or single-carrier adjacent channel power ratio (ACPR) measurements are not sufficient to evaluate MCPAs. These amplifiers must instead be evaluated using multiple carriers as the stimulus, which more realistically simulate conditions the amplifiers will encounter in service. However, the test set-up for multicarrier ACPR measurements typically requires multiple sources along with other components.

As an alternative to multiple carriers, multiple tones with the proper phase relationships can be used to accurately represent multicarrier signals. By using new digital multitone signal generation techniques, and following prudent measurement methodologies, these complex amplifiers can be evaluated more easily, at less cost, and with high repeatability.

Amplifier measurement

In digital communications systems, a digitally modulated signal with the appropriate signal format is used as the stimulus in an amplifier measurement system. ACPR is the ratio between the transmit power in the desired channel and the undesired power it has "splattered" into an adjacent channel.

The power statistics of some digital modulation schemes can vary depending on the signal's configuration. In CDMA systems, for example, the peak-to-average power ratio statistics of the signal vary with the number of code channels, and code channel number assignments. These power statistics can be depicted by the complementary cumulative distribution function (CCDF) curve, which directly affects ACPR measurement results.

Multicarrier signals have more demanding CCDFs than single-carrier signals and require

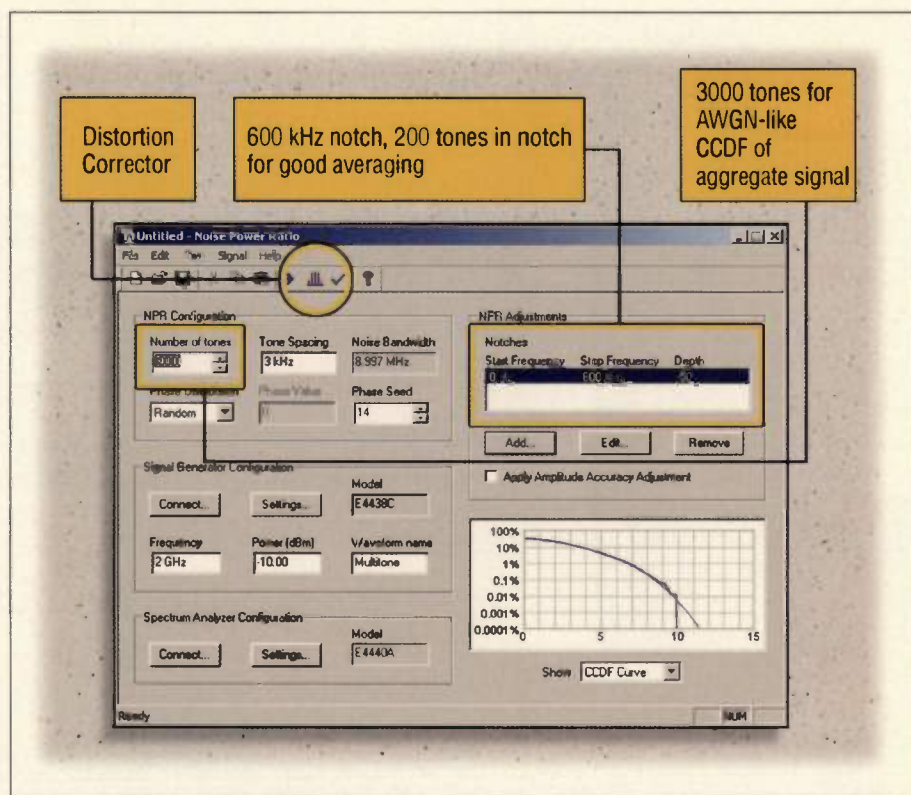


Figure 1: Stimulus configuration using the digital tone-generation approach to test a GSM MCPA for 14 carriers and an additional carrier off in the center.

MCPAs with more linear performance. For example, the spectrum measurement and CCDF of a GSM signal with 16 carriers that have random phases and data shows that while the peak-to-average power ratio of a GSM signal is close to zero, the CCDF of a 16-carrier GSM signal approaches a 10 dB peak-to-average power ratio for a 0.001 percent probability.

Since ACPR is influenced by peak-to-average power ratio, single-carrier ACPR measurements cannot provide a realistic measure of the real performance of MCPAs,

and, instead, multicarrier signals are needed. However, because of the high cost and the complexity of a multicarrier measurement setup (often requiring several sources, as well as combiners, isolators and band stop filters), multitone IMD measurements are often used as an alternative to multicarrier ACPR measurements.

Generating tones

There are two basic ways to generate multitone signals. The analog approach, which has been widely used, requires one signal source



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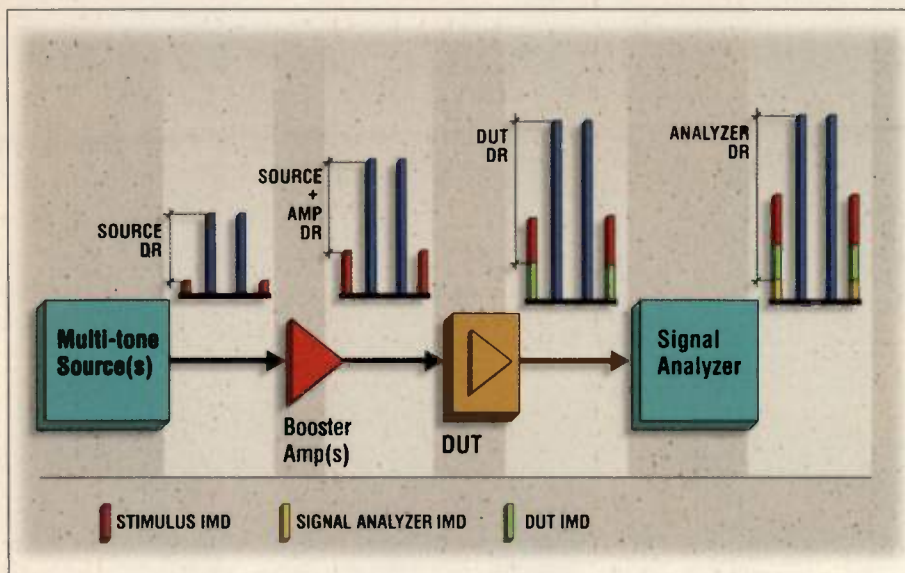


Figure 2: The effect of different devices on measurement dynamic range.

for each tone. Each source can be independent, or all sources can be orchestrated with a controller. Obviously, the latter approach is preferred, since controlling so many sources manually is a frightening prospect.

In contrast, the digital approach generates multiple tones from a single source. The digital technique allows pre-distortion to be used to improve the dynamic range of the source, and provides very repeatable measurements.

There are two possible ways to generate analog signals. In the first, separate analog sources are used and LO drifting of the different sources is leveraged to create the phase randomization necessary to create spectral distribution similar to that of additive white gaussian noise (AWGN). This approach is viable, but it means long measurement times as the carriers slowly drift and build the CCDF curve.

An alternate method is to use analog sources within a system in which the phase can be set to random and the rate of phase change of each tone can be controlled to produce the randomization necessary to obtain an AWGN distribution in a reasonable time. However, this still does not provide a very repeatable signal, and multiple measurements still must be averaged to provide repeatable results.

In contrast, the digital technique employs a digital signal generator in combination with signal studio for enhanced multitone software or signal studio for NPR software, and a spectrum analyzer.

The signal generator can produce thousands of tones with random phase distribution at high spectral density to approximate the CCDF of AWGN or the CCDF of the multicarrier signal of interest. The multitone signal must be configured with a notch that

has hundreds of tones that represent one of the channels.

Signals with a lower number of tones can also be used if a random phase set that provides the CCDF of interest (typically close to

tain period, the measurement is much more repeatable than analog techniques.

An example of the stimulus configuration using the digital approach is shown in Figure 1. In this case, the device under test is a GSM MCPA with 15 carriers (14 carriers with one carrier off in the center) and 600 kHz separation. The signal generator produces 3,000 tones with a tone spacing of 3 kHz over a frequency range of 9 MHz. Each carrier is represented by 200 tones (600 kHz). The notch is created over 600 kHz, so it covers 200 tones, and represents one of the carriers.

The distortion in the notch must be integrated (equivalent to averaging the distortion in the 200 tones), which will reduce the measurement variance. This is because the IMD at a single frequency consists of the vector sum of all the third-order two-tone and three-tone terms at that frequency.

The large number of tones used at the same amplitude makes it possible to assume that for each IMD tone in the notch there will be the same number of third-order two-tone and three-tone terms. However, the phases of the fundamental tones are random, so the third-order terms will add as vectors in a different way for each IMD tone. As a result, their

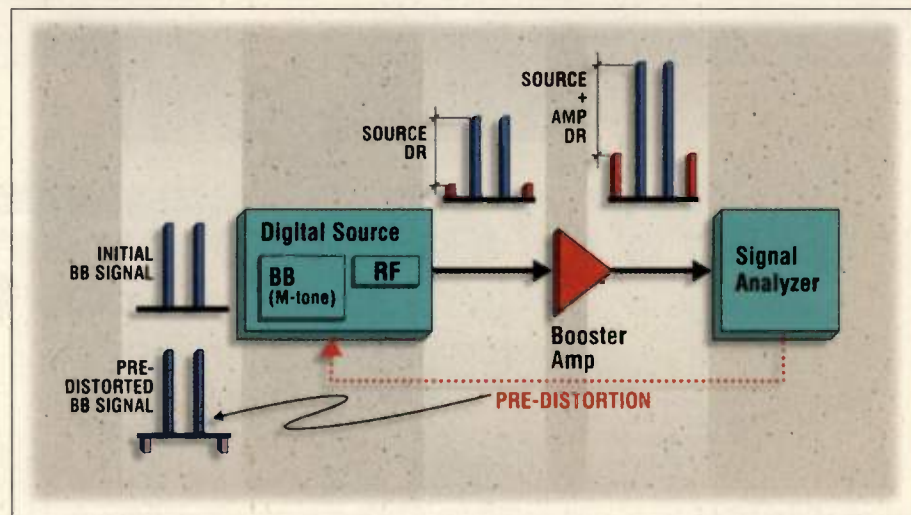


Figure 3: During the calibration stage of the digital approach, the distortion products at the output of the source and booster amplifier are measured and used to pre-distort the stimulus signal.

the CCDF of the multicarrier signal or of AWGN) is carefully chosen.

The test is made by measuring the distortion in the frequency band of interest. Integrating the distortion power over the band of interest basically provides the averaging of all the distortion tones in the notch, which reduces the measurement variance.

Averaging the distortion over several measurements can also be used to further improve repeatability. In addition, since the stimulus signal is generated digitally, and it has a cer-

tain amplitudes will vary. Placing many tones in the notch allows all possible phases to be integrated over frequency.

Gaining dynamic range

The second challenge in multitone distortion tests is how to make the measurement with enough dynamic range to avoid measurement uncertainty caused by instrument distortion. The measurement dynamic range is limited by both the source and the signal analyzer, as shown in Figure 2. Although, for

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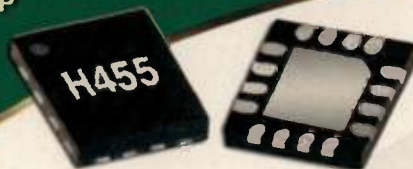
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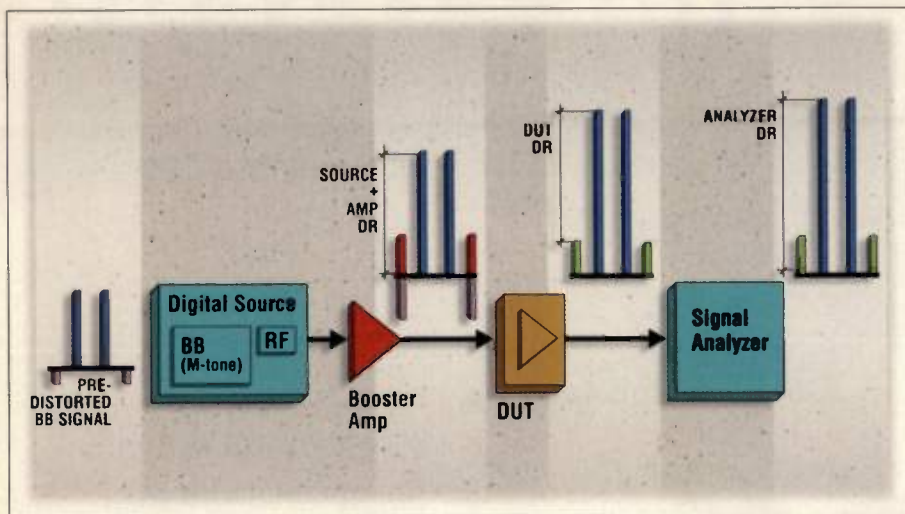


Figure 4: With the digital approach, the distortion products at the output of the source and booster amplifier are 180 degrees out of phase and subtract, resulting in a stimulus that has the dynamic range needed to feed the DUT.

the purpose of illustration, the distortion from each device has been placed linearly on top of the distortion of the following device, the distortion from the different devices will not necessarily add in-phase.

Digital signal source generation allows pre-distortion to be used so the dynamic range can be improved by measuring and compensating for the IMD generated by the source and any booster amplifier used.

The measurement is performed in two stages. In the first "calibration" stage, shown in Figure 3, the baseband signal (which has no distortion) and the distortion from the source (generated by the RF section) and booster amplifier are measured.

The attenuation in the signal analyzer is set so its distortion does not contribute to the distortion from the source and booster amplifier it is measuring. The distortion measured by the signal analyzer is used to pre-distort the

stimulus signal.

The baseband pre-distorted signal will then consist of the initial wanted tones and 180-degree out-of-phase distortion products intended to cancel the source and booster amplifier distortion. The calibration cycle must be repeated until the required dynamic range (the level of distortion relative to the level of the fundamental) is reached at the output of the booster amplifier or at the output of the source, if no booster amplifier is used. Pre-distortion also corrects for the power levels of each fundamental tone, which enhances the measurement repeatability.

In the measurement phase, shown in Figure 4, the 180-degree out-of-phase distortion products at the output of the source and booster amplifier subtract from the distortion generated by the source and booster amplifier.

Now the resulting stimulus signal has the required dynamic range at the output of the

booster amplifier. The attenuation in the spectrum analyzer is set to minimize distortion generated within the analyzer. The effectiveness of calibration is demonstrated in Figure 5, which shows the improvement in the stimulus signal used earlier (3,000 tones, 200 tones in the notch). The spectrum shows part of the notch before and after calibration.

From a spectrum analysis point of view, the best dynamic range will be obtained by choosing the optimum mixer level for the measurement.

The two-tone case is the simplest case to analyze. Figure 6 shows a spectrum analyzer's dynamic range chart example for two-tone IMD. The absolute maximum dynamic range occurs when the IMD is nearly equal to the displayed average noise level (DANL). However, this might not be the best mixer level to use because the analyzer's IMD will be coherent to the DUT's IMD and the DANL will be incoherent. The coherent distortion has a larger effect on measurement uncertainty than incoherent distortion.

To achieve 1 dB of uncertainty (for example, 0.9 dB of error from the spectrum analyzer's generated IMD and 0.44 dB of error from its DANL), the analyzer's IMD must be at least 20 dB below the DUT's IMD, while the DANL must be only about 4 dB below the DUT's IMD.

To calculate the maximum useable dynamic range for 1 dB uncertainty, and the optimum mixer level for 1 dB uncertainty, the IMR and DANL lines must be offset by 20 dB and 4 dB respectively, as shown by the dotted lines in Figure 6. The coherence-versus-incoherence phenomenon moves the optimum mixer level to the left (lower mixer level) and effectively reduces the available dynamic range.

To ensure to maximum dynamic range, a good operating point is to have an error bud-

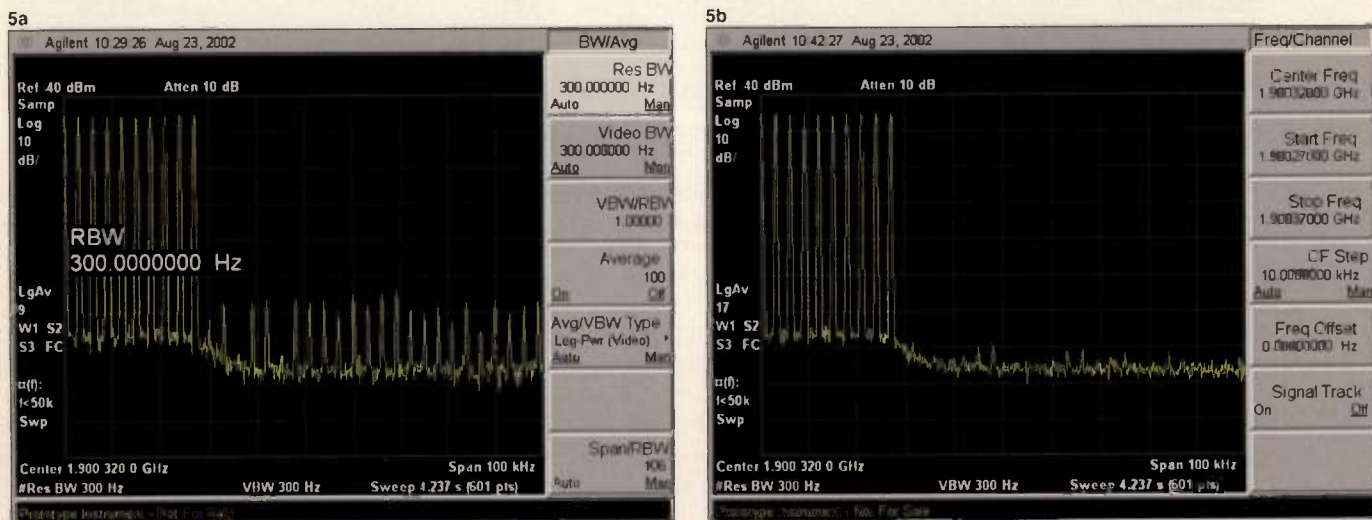


Figure 5: The improvement in the stimulus signal before (5a) and after (5b) calibration is significant.

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					250 ns PULSE (dB Max.)	500 ns PULSE (dB Max.)	2µs PULSE (dB Max.)
GAGC-65-21-4-6	21.4	6	65	25	≤± 2.5	≤± 2	≤± 2
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AFCP-8-30-10	30	10	0.5	0.4	75
AFCP-16-60-20	60	20	0.25	0.2	60
AFCP-20-70-24	70	24	0.20	0.18	60
AFCP-28-140-40	140	40	0.15	0.125	60
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DAFC-21/6	21.4	8	1.5	350	150	100	15
DAFC-30/10	30	5	2	250	125	75	10
DAFC-35/14	35	7	2.5	250	125	75	10
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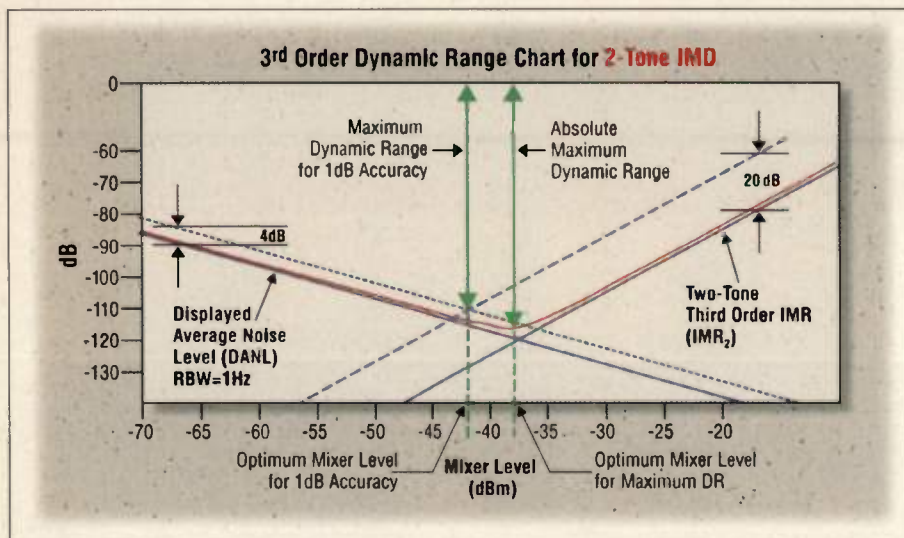


Figure 6: A spectrum analyzer dynamic range chart for two-tone IMD.

get in which 90 percent of the error is allocated to the coherent distortion (such as the spectrum analyzer's IMD) and the remainder of the error budget is allocated to the incoherent distortion (such as the spectrum analyzer's DANL). The contribution to dynamic range from the analyzer's phase noise might also be of concern if the measurement is made at frequency offsets close to the main tones.

For example, for the three-tone case (assuming independent and random phases with uniform distribution), the power level of the IMD at the frequencies immediately above and below the main tones is five times (7 dB) greater than the two-tone case.

Therefore, an offset of 7 dB should be added to the two-tone IMR line to obtain the three-tone IMR line for the IMD at the fre-

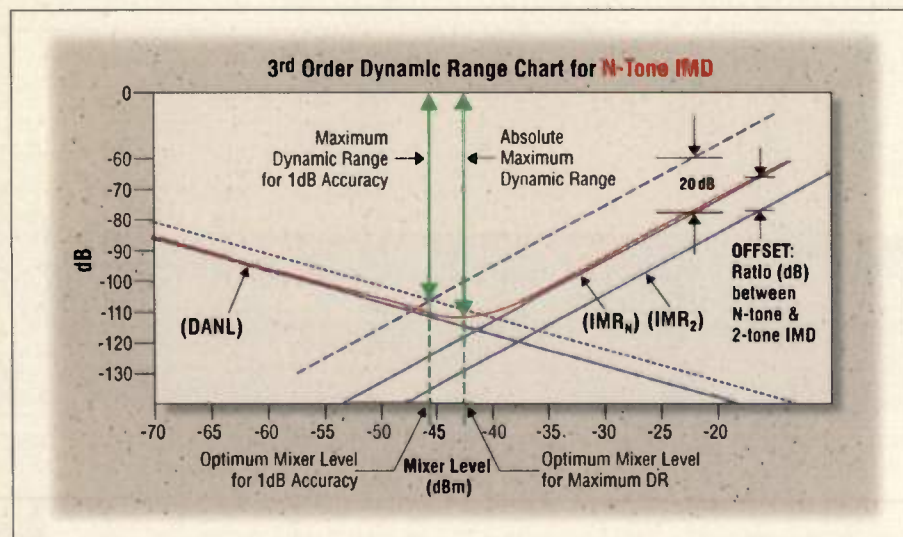


Figure 7: A spectrum analyzer dynamic range chart for multitone IMD built from the chart in Figure 6.

The analyzer's dynamic range chart for a multitone IMD measurement can be built from the two-tone measurement dynamic range chart (Figure 7).

An offset must be added to the two-tone IMR line (IMR_2) to obtain the IMR line for N tones (IMR_n). The offset is the ratio between the n-tone IMD power at the frequency of interest and the two-tone IMD power.

quency immediately above or below the frequencies of the main tones.

The phase relationship among the tones will affect the peak-to-average power ratio and offset level. In general, the higher the peak-to-average power ratio, the higher the IMD, and, therefore, the higher the offset for the IMR line.

If the frequency of interest is not a discrete

frequency offset, but it has a certain bandwidth, the offset will be a function not only of the frequency offset, but also of the bandwidth over which the distortion power needs to be integrated.

The resulting offset could also be negative (the IMR line could be below the two-tone IMR line) if the IMD integration bandwidth falls out of the area with the highest distortion. When integrating across a bandwidth, the DANL line will increase by about 2.5 dB plus 10 times the log of the ratio of the bandwidth of integration to the noise bandwidth in which DANL is measured.

Summary

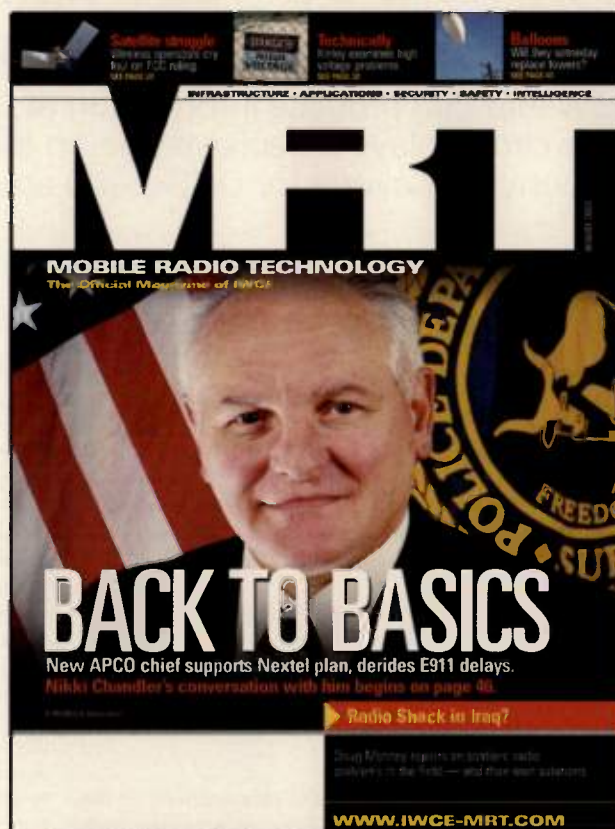
As is probably obvious from discussions in this article, the designer faced with characterizing the performance of an MCPA has a considerably more difficult task than when characterizing single-channel amplifiers used in the past.

Not only are simple two-tone tests inadequate, but the choice of the signal used to stimulate the amplifier under test must simulate the conditions the amplifier will experience in service as accurately as possible. Two-tone CW signals used for this purpose have proven to deliver results that, in some cases, allow amplifiers to be deployed that simply cannot perform adequately when stressed.

Generating multicarrier signals or multiple tones, when performed with multiple signal sources, can be expensive and produce a test system with a maze of cables and connections that must be switched. Generating multitone signals digitally dramatically reduces this complexity, allows pre-distortion to be used to improve dynamic range, enables an appropriate time-domain profile to be established, and creates an overall stimulus environment that is extremely realistic and repeatable, as well as highly configurable.

ABOUT THE AUTHOR

Marta Iglesias holds a B.S.E.E. degree from the Universitat Politècnica de Catalunya in Spain. She has performed technical support for RF and microwave spectrum analyzers, and currently is a wireless applications marketing engineer for Agilent Technologies Inc. (www.agilent.com), where she is responsible for understanding the test needs of the wireless communications industry. She can be reached at marta_iglesias@agilent.com.



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An integrated downconverter circuit in 0.8 μm SiGe technology for DCS-1800 applications

Frequency converters are an important part of most RF front-ends. As there are no ADCs with several bits that can process information at GHz frequencies, the frequency downconverter circuit plays a decisive role on every receiver. This article describes a downconverter circuit for DCS-1800 applications.

By E. Hernández, R. Berenguer,
J. Meléndez, N. Rodríguez, and J. Aguilera

Frequency converters are an important part of most RF front-ends. As there are no ADCs with several bits that can process information at GHz frequencies, the frequency downconverter circuit plays a decisive role on every receiver. Besides, the implementation of a direct conversion topology to baseband or low IF allows an optimal integration due to the reduction in the use of discrete components. In Figure 1, a block diagram of the direct conversion topology can be seen. The integrated components presented in this article are gray shaded and marked with a dotted line.

As seen in Figure 1, a mixer, which is active and based on the Gilbert cell, and a differential cross-coupled oscillator with integrated LC tank form the presented downconverter circuit.

Of course, frequency conversion must be done without introducing noise or degrading the signal, thus, there are two important specifications in the performance of the downconverter circuit: the oscillator should have low phase noise and the mixer should present high linearity. Besides, if the oscillator phase noise fulfills the requirements of DCS-1800, it is verified that there will not be inter-channel interferences.

To improve the phase noise of the oscillator, a good quality factor tank circuit was designed¹. A balanced inductor and two PN junction varactors form this tank circuit. The way to improve the linearity of the Gilbert cell mixer without too much degradation in conversion gain and noise figure is to use a

class-AB input stage².

Although the technology used to implement the circuits is a 0.8 μm SiGe, the oscillator was integrated with only MOS transistors, as will be explained later. On the other hand, the mixer was designed with HBT transistors, except for the current source, which has been implemented with MOS transistors.

The oscillator's design

As explained below, the configuration used is a differential cross-coupled with integrated LC tank. The oscillator's schematic is shown in Figure 2.

Topology selection

The first remarkable characteristic of the oscillator is that it was implemented with MOS transistors. The limitations of the technology made impossible the use of HBT transistors due to their low base-emitter breakdown voltage, which was approximately 1 V. This implies that the maximum output power of the oscillator is around -6 dBm³.

As mentioned in N. Rodríguez's 2002 Ph.D. dissertation, "Mezcladores Integrados en Tecnologías SiGe y BiCMOS para Frecuencias inferiores a 1.8 GHz⁴," Gilbert-cell-based active mixers in the technology have an optimum performance with a LO power around 0 dBm. As it is impossible to obtain such output power using HBT transistors, it was decided to design the VCO with MOS transistors, even though MOS transistors include higher high-frequency noise.

After selecting a MOS topology, among the possible architectures that employ these transistors, the cross-coupled CMOS was selected due to its best ratio between phase noise and power consumption when working in the current limited region^{5,6}. It

will be demonstrated that with this architecture, a proper design of the tank allows fulfilling the restrictive DCS-1800 phase noise requirements without an excessive increase in power consumption.

Moreover, two tail capacitors were added in parallel with the biasing current source because their presence can improve the phase noise of the oscillator⁶. Simulations show that, not only is the phase noise improved, but the output power is also increased with an insignificant reduction of the oscillation frequency.

To select the value of these capacitors, there is a trade-off between the improvement in phase noise and output power, the sensitivity of the oscillator to supply voltage variations⁶, and the occupied area.

Passive elements design

Since, as derived from the Leeson model¹, the VCO phase noise performance depends highly on the quality factor of the tank circuit, it is necessary to design passive elements with quality factors as high as possible.

Due to the fact that at the frequency of interest (1.8 GHz) inductors usually dominate the quality of the tank¹, this section will

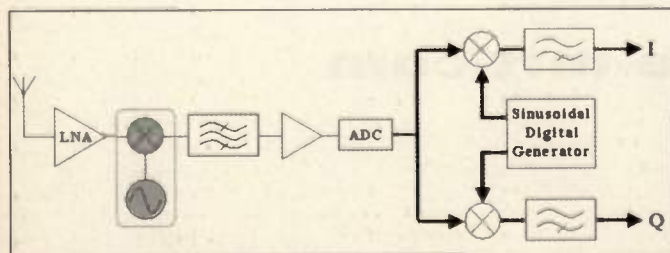


Figure 1: Block diagram of the direct conversion receiver.

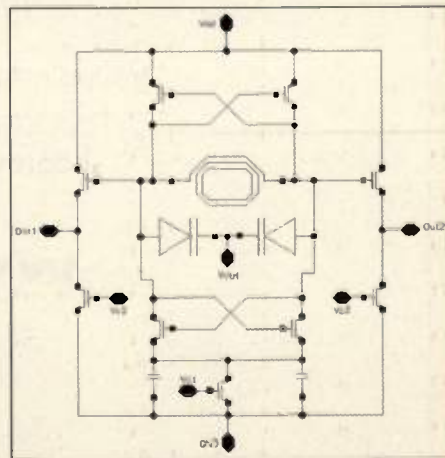


Figure 2: CMOS architecture of the oscillator.

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16dB	DBTC-16-5-75	5-1000 1000-1500	1.0 1.3	21 19
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Radius	Width	Spacing	N° Turns
105 μm	10 μm	1.9 μm	3.5

Table 1: Geometrical characteristics of the balanced inductor.



Figure 3: Microphotograph of the balanced inductor.

emphasize the design of the inductor. To design a differential oscillator, the inductor configuration must fulfill the symmetry requirements. Thus, the choice must be made between the use of two standard inductors symmetrically placed, or a balanced inductor.

The standard technology used includes a highly conductive P-type substrate, thus, substrate losses will have an important effect in the quality of the inductor.

The way to decrease these losses is to reduce the inductor's area. A balanced configuration was selected for the inductor because balanced inductors present more coupling effects between their turns. Thus, a bigger inductance can be obtained using the same area with two symmetrically placed standard inductors, so substrate losses will be reduced. Furthermore this inductance is obtained with less metal length, and the inductor's resistance is lower than one in a standard inductor^{3,7}.

An additional advantage that comes from using a balanced inductor is avoiding the parasitic coupling that occurs between the two inductors symmetrically placed.

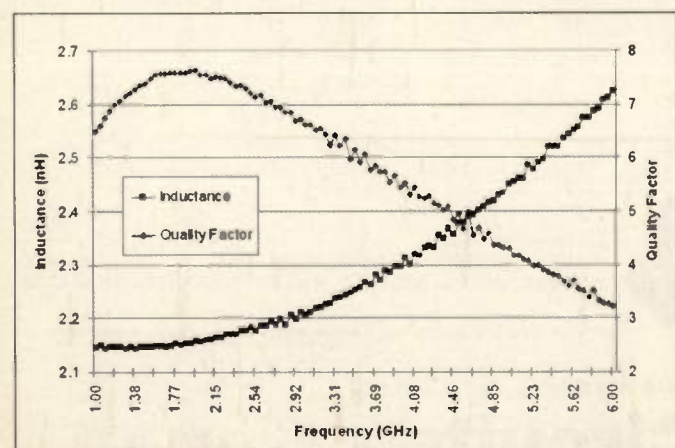


Figure 5: Measured results for the inductor.

Dimensions	N° P+ islands	P+ island size	P+/N+ distance
210 * 230 μm^2	27 * 30	3.6 * 3.6 μm^2	1 μm

Table 2: Geometrical characteristics of the varactor.

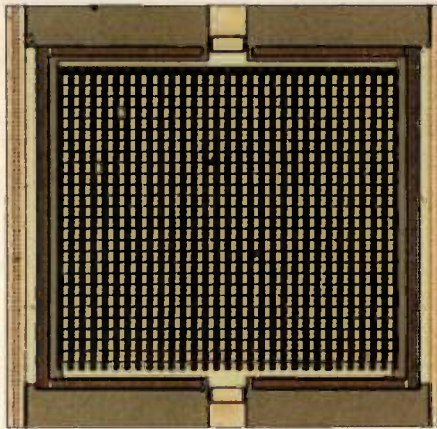


Figure 4: Microphotograph of the varactor.

As explained before, substrate losses will be important, affecting the quality of the inductor, however, resistive losses are as much important as substrate losses.

To reduce these ohmic losses, two improvements were made. The first was to connect, in parallel (except in the underpasses), the two available metal layers to diminish the series resistance of the coil. The second was to design the spiral hollow to avoid the high resistance of the inner turns due to proximity effect¹.

The geometrical characteristics of the designed balanced inductor are presented in Table 1 and a microphotograph is shown in Figure 3. As seen in Figure 5, at the frequency of interest, it has an inductance of around 2.15 nH, with a quality factor of 7.6.

The second element in the tank circuit is the varactor. In this particular case, the integrated varactor is based on the variable capacitance that appears in a P-N junction when it is reverse biased. The varactor consists of P+ islands diffused in an N-well and surrounded by a N+ zone. In this way, the depletion zone

appears around all of the P+ diffusion so the capacitance is higher, which explains the capacitance variation⁸.

To increase the varactor quality, some improvements were made:

- N+ contacts have been included in the N-well because they are useful to decrease the series resistance of the device.
- The distance between P+ and N+ diffusions was reduced to the minimum. This way, the N-well resistance is decreased. Being this minimum distance of 1 μm higher than the maximum length of the depletion zone, the avalanche breakdown is avoided⁸.
- The P+ islands are square and have the minimum side length allowed by the technology. This way the series resistance of the varactor can be minimized⁹.
- Another important parameter is the width of the metal track that connects diffusions of the same type. If this width is increased, the resistance of the track will be decreased but the parasitic capacitance will increase and the auto-resonance frequency will decrease. Simulations give a trade-off solution of 1.2 μm ⁸.
- Finally, a N+ buried layer was included under the N-well zone to provide a low impedance way for the current⁸.

The geometrical characteristics of the varactor are presented in Table 2 and a microphotograph is shown in Figure 4. As seen in Figure 6, at the frequency of interest, it has a capacitance variation between 3 pF and 5 pF with a quality factor between 35 and 60.

The measurement system used for the characterization of the passive elements consists of the Hewlett Packard Co. (www.hp.com) HP8719ES vector network analyzer and the Cascade Microtech Inc. (www.cascademicrotech.com) ACP40 GSG microprobes. To calibrate the measurement system the SOLT method was used. Finally,

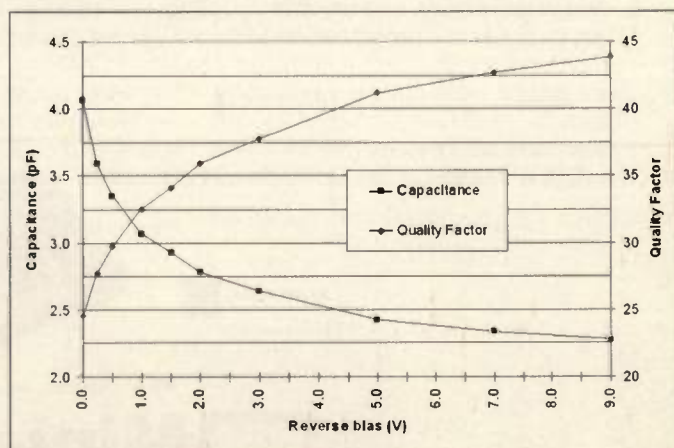


Figure 6: Measured results for the varactor.



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Figure 7: Equivalent conductance of the tank circuit.

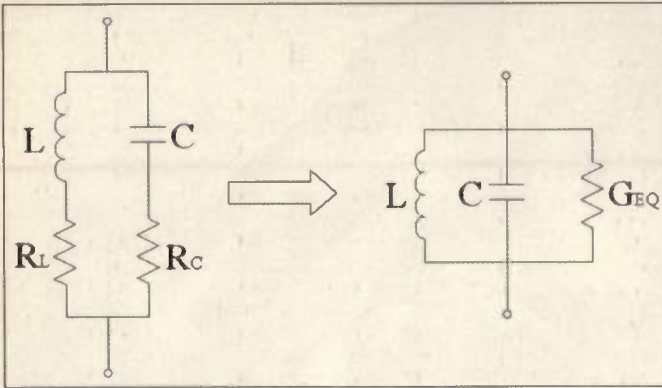


Figure 7a presents the calculated equivalent conductance of the tank, using Equation 1.

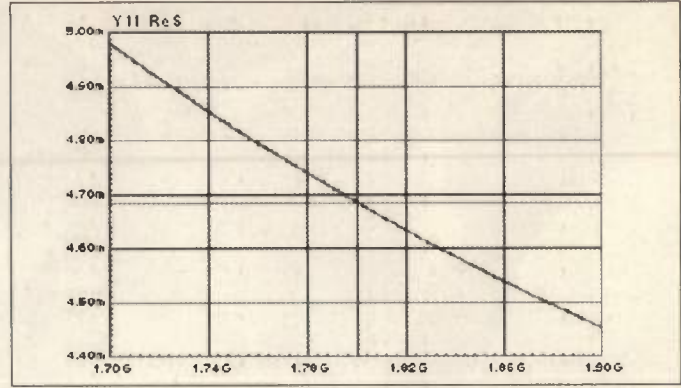


Figure 7b presents the variation of this conductance in the frequency range of interest. This conductance must be compensated by the active circuit. Starting from the obtained value, the rest of the oscillator will be designed.

the *Four Step De-embedding Method*¹⁰ was used to remove the parasitic effects introduced by the measurement structures.

The measured results of the passive elements are presented in Figure 5 and Figure 6.

Once the passive components are measured and characterized, using Equation 1, the equivalent conductance of the tank can be calculated, as seen in Figure 7a.

$$G_{EQ} \approx \frac{1}{(R_L + R_C)(\omega C)^2}$$

Oscillator design

The negative conductance generated by the CMOS oscillator active circuit can be obtained as a first approximation, as seen in Equation 2. It can be calculated as a much more complex and accurate expression taking into account the parasitic capacitances and the channel admittance of the transistors⁸.

$$G_A \approx -\frac{g_{mNMOS} + g_{mPMOS}}{2} = g_m$$

$$\text{and } g_m \approx \sqrt{\frac{K' I_D W}{L_{eff}}}$$

Knowing the equivalent conductance of the tank, the transconductance for each of the transistors of the active circuit can be obtained. It is normal to include a security factor around 2 or 3 in the negative conductance of the active circuit¹. As the transconductance of a transistor can be approximately obtained with Equation 2, it can be seen that there is a trade-off between an increase in the tail current (and, thus, in the power consumption) and an increase in the transistor width (and, thus, a decrease in the oscillation frequency and the gain at high frequencies).

Once the tank circuit is modeled and the active circuit is designed, the phase noise can be calculated. With Equation 3, an approximation to the phase noise of the oscillator can be obtained¹.

$$PN @ \Delta f = 10 \log \left[\frac{kTR_{eff}(1+A)f_0^2}{0.5\Delta f^2 V_A^2} \right]$$

With this equation, the estimated phase noise of the oscillator at 100 kHz from a 1.8 GHz carrier is -107.9 dBc/Hz.

Mixer design

The downconversion mixer operates in the direct conversion receiver presented in Figure 1 with the signal from the LNA. To avoid intermodulation problems due to unwanted signals, the mixer should present as high a linearity as possible.

The gain of the LNA is high so the noise figure of the mixer is not a critical parameter. Besides, the conversion gain of the mixer must be high enough to compensate for the loss of the filters that come after it. The linearity improvement usually implies a worsening in the gain and noise figure of the circuit⁴. Then it becomes necessary to reach a trade-off solution between linearity, gain and noise figure.

The most widely used downconversion mixer is the Gilbert cell¹¹, which, being active, has enough conversion gain, but is not linear enough for our application. The only way to achieve acceptable levels of gain and linearity in a Gilbert cell is to turn the standard RF input stage into a class-AB stage with resistive degeneration⁴. The schematic of this mixer is shown in Figure 8.

The mixer presented in Figure 8 was designed with SiGe HBTs because of their gain. However, the current source was implemented with MOS transistors due to their better noise and stability characteristics.

Equation 4 represents the conversion gain of the mixer, where V_T is the thermal voltage and R_{OUT} is the mixer's output resistance. As the gain depends on the transconductance of the input transistors (M_1 , M_2 or M_3) it depends on the bias current of each branch (I_1 or I_2).

$$A_v = \frac{4}{\pi} g_m R_{OUT} = \frac{4}{\pi} \left(\frac{I_1}{V_T} \right) R_{OUT}$$

Equation 5 represents the noise of the mixer, where r_b is the base resistance of the transistors, Z_s is the source impedance, and $\beta(\omega)$ is the transistor's current gain, which is frequency dependent.

The first term represents the contribution of thermal noise to the total noise; the second and third terms represent the contribution of collector and base currents shot noise, respectively.

$$V_n^2 = \left\{ \left(\sqrt{4kTr_b} \right)^2 + \left(V_T \sqrt{\frac{3q}{I_1}} \right)^2 + \left(Z_s \sqrt{\frac{3qI_1}{\beta(\omega)}} \right)^2 \right\}$$

The way to decrease the noise of the mixer is to decrease the base resistance, increasing the area of the input transistors. To further reduce this resistance, the transistors used have double base contact. Also, an increase in the bias current improves the noise, but it has one disadvantage, which is that the input impedance matching becomes worse⁴.

The RF and IF ports must be matched to 50Ω. The output matching is achieved by placing two series resistors (R_{S1} and R_{S2}). The input matching is obtained with a trade-off between the biasing current, the input transistor's width, and the degenerative resistor's values².

To avoid degrading linearity, the LO power level must guarantee the appropriate switching performance in the mixer core. In this design, mixer LO power level is close to 0 dBm.

Due to this quite high value, the isolation between the LO input and the IF output must be high to avoid feed-through and interference problems. To suppress the LO signal at the IF output, the differential Gilbert cell was used. In addition, other ways of increasing LO-IF isolation, maximizing the layout symmetry, or using common centroid techniques have been used.

Layout considerations

Once the oscillator and the mixer have been designed, the final step to implement the down-converter circuit is to lay them out together.

The microphotograph of the downconverter circuit is presented in Figure 9. The chip area is about 1900 x 700 μm². In the layout,

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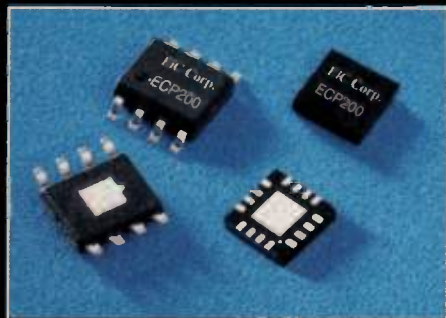
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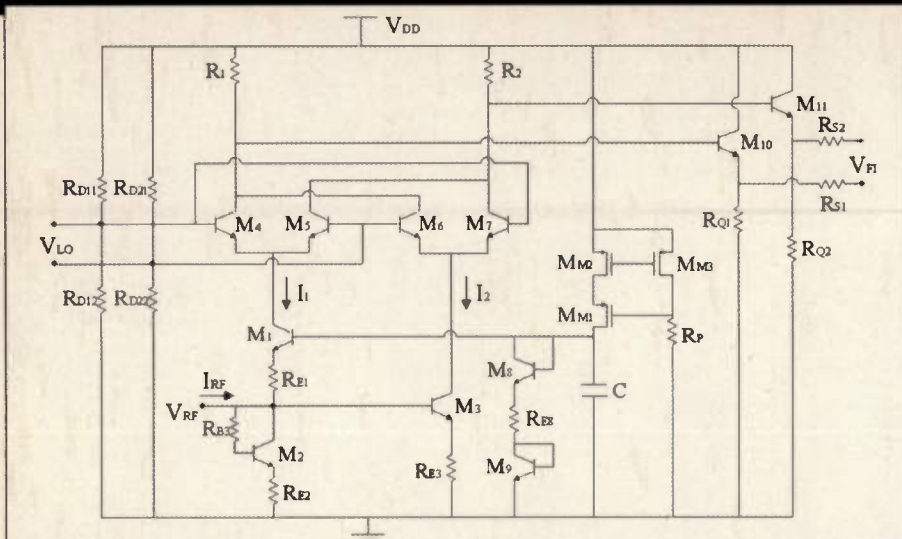


Figure 8: Architecture of the class-AB mixer.

some capacitors between the DC voltage pads and ground were added to stabilize the supply voltage, eliminating the high frequency variations in this voltage, which can adversely affect the circuit response.

Another consideration is that several substrate contacts connected to the ground pad were added around the transistors to provide a stable substrate voltage. Finally, the layout was designed with the maximum symmetry to reduce the phase noise of the oscillator⁶ and increase the LO-IF isolation.

As seen in Figure 9, between the oscillator and the mixer two pads were included. This is to fill the need of feeding back the oscillator's output signal to the loop of the PLL. Moreover, two series capacitors have been included to isolate the oscillators' output DC level from the input of the mixer.

There is another important characteristic that must be taken into account — the parasitic resistance introduced by the metal tracks that connect the passive elements of the tank circuit with the active circuit.

In Figure 10, the phase noise variation — when the parasitic resistance of the metal tracks increases the inductor or varactor resistance — is presented. The biggest phase noise variation occurs when the inductor's resistance increases, so special care must be taken when designing the connections of the inductor.

To minimize the resistance of the metal tracks, the two metal layers connected in parallel were used. The track width must be a trade-off between the parasitic resistance, which increases the phase noise, and the parasitic capacitance, which decreases the output frequency and tuning range.

Measurements

The downconverter circuit's response was measured with the HP E4407B spectrum analyzer. For the supply and control voltages, the Cascade Microtech DCQ-05 PPGPP and ACP40 GSG microprobes were used. The

supply voltages of the mixer and the oscillator are independent. For the input RF and output IF signals, the Cascade ACP40 SGS microprobes were employed.

The measurement of the phase noise response of the VCO at a frequency of 1.8 GHz is presented in Figure 11. This measurement was done for a core current of 8 mA, and the optimum performance of the oscillator was obtained with it. With this current, the oscillator is operating in the current-limited region, but near the limit of the voltage-limited region⁶.

As seen in Figure 11, the measured phase noise at 100 kHz offset from the 1.8 GHz carrier is -103.8 dBc/Hz. As it can be observed, the previously calculated approximation -107.9 dBc/Hz is good, but optimistic because it gives a value around 4 dB better than the real phase noise. This difference can be attributed to the parasitic resistance of the metal tracks, which connect the passive elements of the tank circuit.

The whole downconverter circuit's measurements were done with the same current of 8 mA in the oscillator's core. Figure 12 shows the mixers output frequency variation when the voltage is applied to the varactor changes.

As seen in Figure 12, there are two biasing points where the output frequency is 36 MHz: $f_{IN} - f_{LO} < f_{IN}$ and $f_{LO} - f_{IN}$ when $f_{LO} > f_{IN}$.

Measurements show that the phase noise response, and the rest of the mixer characteristics, are worse when $f_{LO} > f_{IN}$, so all the following measurement results have been obtained with a control voltage of 4.5 V. These results are presented in Table 3.

As seen in Table 3, the design goals were achieved. The gain is not very high, but enough to compensate for the loss of the low IF filters. The noise figure is relatively high, but as the LNA has high gain, this result is acceptable. The IP3 is high enough for our application and higher than the one of a standard Gilbert cell. Finally, the input and output matching is good.

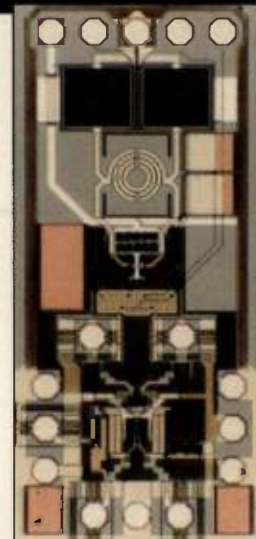


Figure 9: Microphotograph of the downconverter circuit.

Conclusions

A fully integrated core low power consumption VCO, which achieves the restrictive phase noise specification for DCS-1800, was designed. The measured phase noise is -103.8 dBc/Hz at a 100 kHz offset from a 1.8 GHz carrier.

The oscillator was designed using 0.8 μ m MOS transistors. The ability of the CMOS technology to achieve good phase noise results, if a proper LC tank is designed, was demonstrated.

It was also demonstrated that a careful design allows obtaining mixers based on Gilbert cells with enough conversion gain and linearity. A class-AB input stage should be used to improve the linearity. After laying the oscillator and the mixer out together, the resultant downconversion circuit fulfills the specifications of a baseband or low IF direct conversion receiver for DCS-1800.

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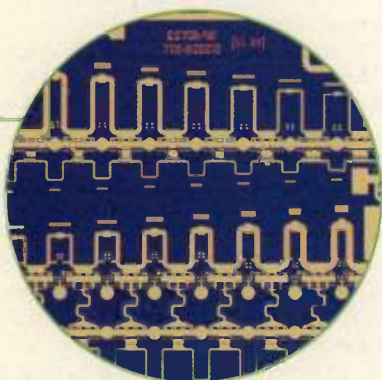
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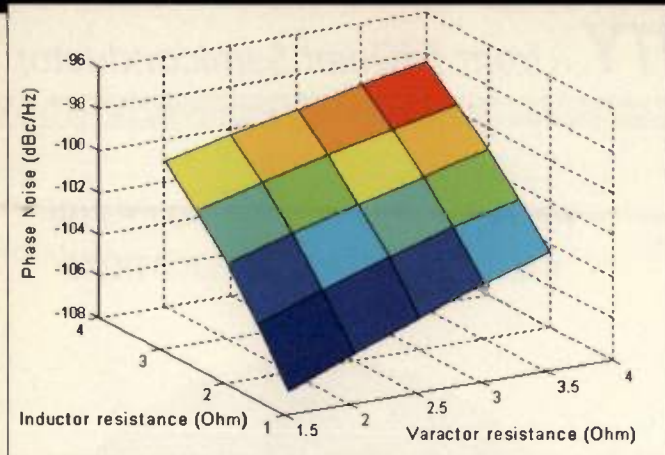


Figure 10: Phase noise variation with parasitic resistance.

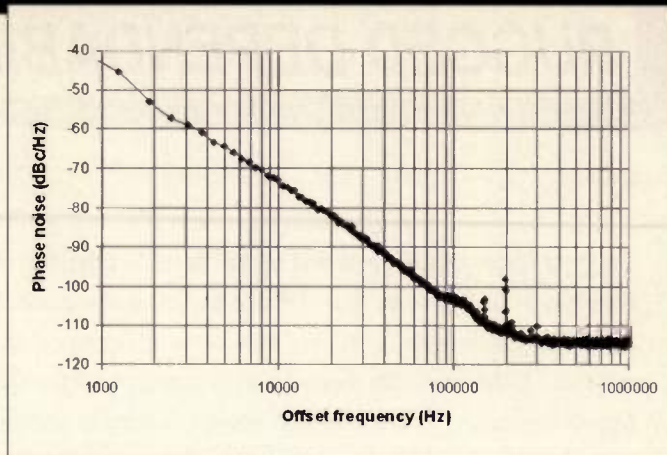


Figure 11: Phase noise of the oscillator.

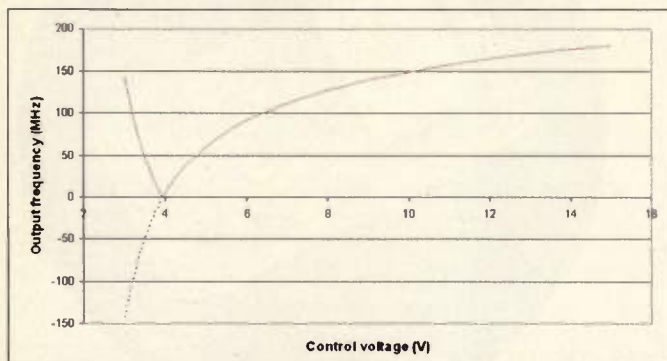


Figure 12: Output frequency variation.

Conversion gain	7.7 dB
Noise Figure	13.2 dB
OIP3	16.6 dBm
LO IF isolation	32.9 dB
Power consumption	28 mA * 5 V
RF VSWR	1.13
IF VSWR	1.17

Table 3. Measurement results of the downconverter circuit.

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ABOUT THE AUTHORS

E. Hernández received the B.S. and M.S. degrees in electronic engineering from ESI of Navarra University in 1999. He also joined the TECNUN's RF integrated circuit design group, San Sebastian, Spain, in 1999. Hernandez obtained his Ph.D. degree in monolithic voltage controlled oscillators for RF applications in December 2002, then joined the Gipuzkoa Center for Technical Research (CEIT) as an associate researcher. His main interests also include the design and characterization of passive components and mixers in standard low cost technologies. He can be reached at ehernandez@ceit.es.

R. Berenguer received the B.S. and M.S. degrees in electrical engineering from ESI of Navarra University in 1996. In 1999, he joined CEIT as an associate researcher. He received his Ph.D. in 2000. His research interests include CMOS and BiCMOS RF circuit design for low cost and highly integrated front ends. He can be reached at rberenguer@ceit.es.

J. Meléndez received his M.S.E.E. degree in 1998 and his Ph.D. degree in industrial engineering in 2002 from Universidad de Navarra. He researched the development of a low power CMOS Low IF digitization GPS front end. His current research interests include system design level of RF transceivers for domestic applications and VCO development for WLAN applications

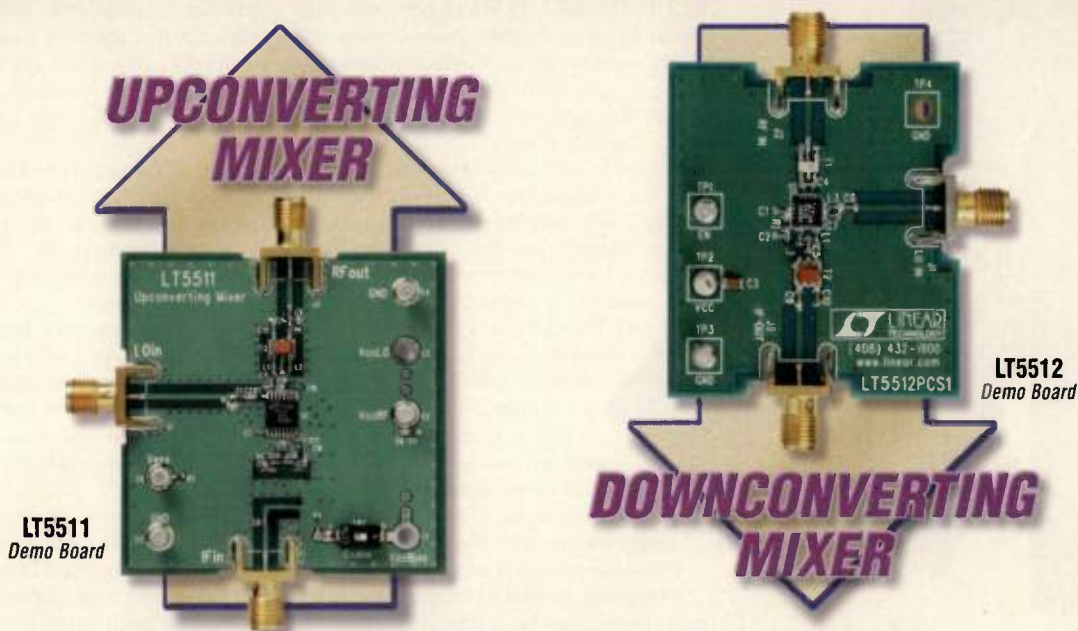
in SiGe technology. He can be reached at jmelendez@ceit.es.

N. Rodríguez received her M.S. degree in telecommunication engineering in 1998 from UPNA (Pamplona Spain) and her Ph.D. degree in industrial engineering in 2002 from Tecnun, University of Navarra, San Sebastian Spain. As part of her research work, she designed active and passive mixers in CMOS, BiCMOS and SiGe technologies for RF front ends. Her current research interests include the integration of SiGe and CMOS devices into RF receivers for WLAN applications. She can be reached at nrodriguez@tecnun.es.

J. Aguilera received his B.S. and M.S. degrees in electronic engineering from ESI of Navarra University in 1999. He joined ESI as associate researcher in 1999, as well. In March 2002 he joined CEIT and received his Ph.D. in April. His work involves improving the quality of integrated inductors for RF applications from the geometrical design point of view. He has also worked in several RF projects for Infineon Technologies AG, Austriamicrosystems AG and Xignal Technologies AG. In December 2002, he joined Modis International to work for Philips Research labs in Eindhoven, the Netherlands. He is currently working in the implementation of a software for RFIC optimization in Philips IC design flow. He can be reached at aguilera@natlab.research.philips.com.

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IIP2	+52dBm	NA
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Direct conversion quadrature demodulators

Linear Technology Corp. introduced two new direct conversion quadrature demodulators that promise to simplify radio design for cellular basestations and microwave and satellite links.

The LT5515 and LT5516 direct conversion quadrature demodulators deliver high linearity, providing more flexible system design and wide spur-free dynamic range, the company says. On a single chip, the devices integrate the functionality of a signal splitter, two high linearity down-converting mixers, a precision local oscillator quadrature generator (0 degrees/90 degrees), and 260 MHz bandwidth output buffers with single-pole, low pass filters on each of the outputs.

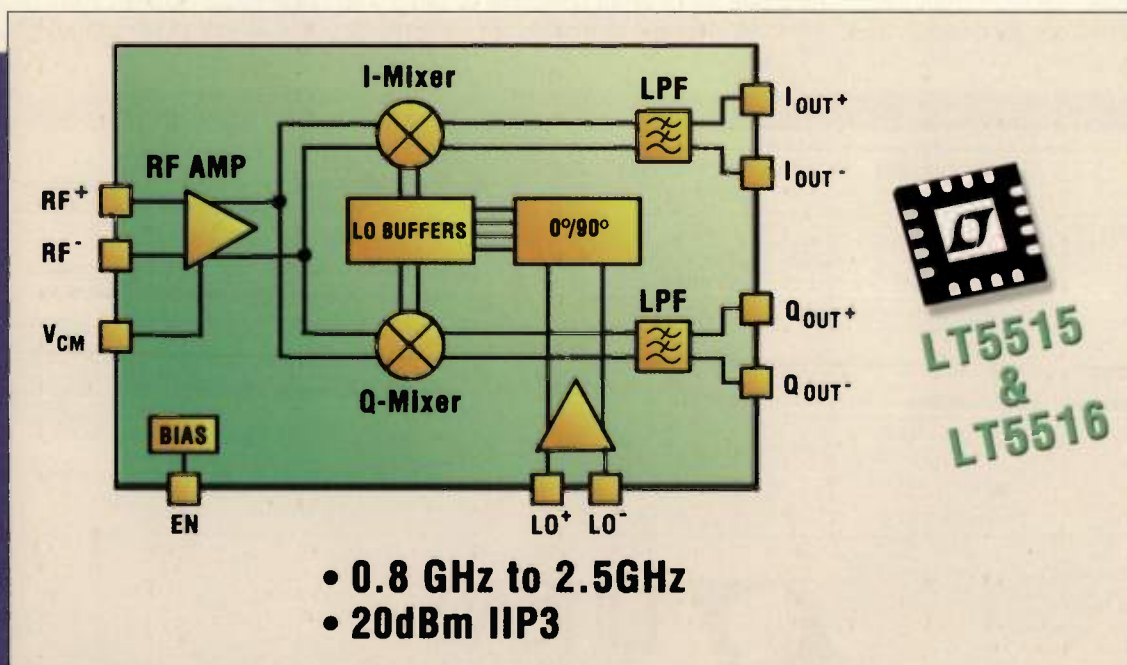
The LT5515 and LT5516 have applications in cellular infrastructure and in microwave and satellite links, where they directly convert an RF signal to baseband in-phase (I) and quadrature-phase (Q) components. The devices' matched I and Q channels ensure precise gain and phase matching, so that significantly less calibration is required, the company says. The direct conversion receiver ICs also eliminate the need for additional intermediate frequency (IF) stages, local oscillators, and associated filtering.

The devices address two different and adjacent frequency bands. The LT5515 operates over an input frequency range of 1.5 GHz to 2.5 GHz, and the LT5516 operates with RF input from 0.8 GHz to 1.5 GHz. Both devices are designed for high linearity applications, including wireless infrastructure of all types, such as basestations for GSM, CDMA, WCDMA and fixed wireless communications, as well as for satellite and microwave receivers, high-performance radios, and instrumentation.

The high linearity of the LT5515 and LT5516 provides excellent spur-free dynamic range, for example in a RF receiver, even with fixed gain front-end amplification. These direct conversion receivers can eliminate the need for intermediate frequency (IF) signal processing, as well as the corresponding requirements for image filtering and IF filtering. Channel filtering can be performed directly at the outputs of the I and Q channels. These outputs can interface directly to LPFs or to a baseband amplifier.

The LT5515 and LT5516 are offered in 4 mm x 4 mm QFN packages. Pricing starts at \$6.75 each for the LT5515 and \$7.40 each for the LT5516 in 1,000 piece quantities.

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www.linear.com



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- **Integrated Limiters**
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OPERATING FREQUENCY [MHz]	MODEL NUMBER	GAIN (dB, Min.)	GAIN FLATNESS (±dB, Max.)	VSWR IN/OUT	NOISE FIGURE NF ₁ NF ₀ NF ₂ [dB, Max.]			OUTPUT POWER (dBm, Min.)
0.001 - 500	AU-1534	30	0.5	2.0:1	1.3	1.4	1.5	+8
0.01 - 200	AU-1442	35	0.5	2.0:1	1.2	1.2	1.2	+5
0.01 - 200	AU-1447	56	0.5	2.0:1	1.2	1.2	1.2	+12
0.01 - 250	AU-1559	11	0.5	2.0:1	4.2	4.2	4.2	+16
0.01 - 400	AU-1565	54	0.75	2.0:1	1.2	1.2	1.3	+14
0.01 - 500	AU-1310	30	0.5	2.0:1	1.3	1.4	1.5	+8
0.01 - 1000	AU-1402	18	1.0	2.0:1	6.0	5.0	5.0	+16
0.01 - 1000	AM-1300	27	0.75	2.0:1	1.4	1.6	1.8	+8
0.01 - 1000	AM-1431	35	0.75	2.0:1	1.4	1.6	1.8	+8
0.1 - 2000	AM-1364	9	1.5	2.0:1	6.0	6.0	6.0	+10
1 - 200	AU-1464	35	0.5	2.0:1	1.2	1.2	1.2	+6
1 - 400	AU-1421	24	0.5	2.0:1	2.4	2.4	3.1	+17
1 - 500	AU-2A-0150	30	0.5	2.0:1	1.3	1.4	1.5	+8
1 - 500	AU-3A-0150	44	0.5	2.0:1	1.3	1.4	1.5	+10
1 - 500	AU-4A-0150	60	0.75	2.0:1	1.3	1.4	1.5	+10
1 - 1000	AM-2A-000110	26	0.75	2.0:1	1.4	1.6	1.8	+6
1 - 1000	AM-3A-000110	35	0.75	2.0:1	1.4	1.6	1.8	+8
5 - 200	AUP-1568	26	0.75	2.0:1	5.0	4.5	4.5	+28
5 - 300	AUP-1495	11	0.75	2.0:1	15	9.0	9.0	+28
5 - 300	AUP-1496	23	0.75	2.0:1	8.0	7.0	7.0	+28
5 - 300	AU-1021	24	0.5	2.0:1	2.7	2.8	2.9	+20
5 - 300	AUP-1479	36	1.0	2.0:1	2.5	2.7	2.9	+28
5 - 1000	AM-1475	36	0.75	2.0:1	1.4	1.6	1.8	+15
5 - 2000	AM-1573	18	1.5	2.0:1	4.0	4.0	4.0	+21
5 - 2000	AM-1590	36	2.5	2.0:1	3.8	3.8	3.8	+20
5 - 2000	AM-1591	48	2.5	2.0:1	3.8	3.8	3.8	+20
100 - 1000	AM-1412	35	0.75	2.0:1	1.4	1.6	1.8	+14
100 - 2500	AM-1585	26	2.0	2.0:1	3.6	3.6	3.6	+20
200 - 2000	AM-1569	20	1.5	2.2:1	4.2	4.3	4.6	+14
1000 - 2000	AM-1477	37	1.0	2.0:1	1.8	2.1	2.4	+15



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PRODUCT HIGHLIGHTS

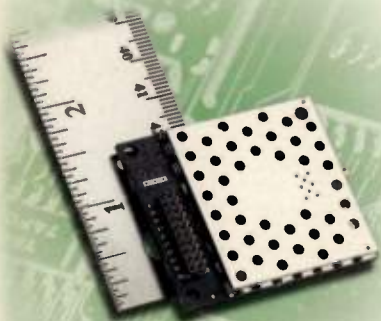
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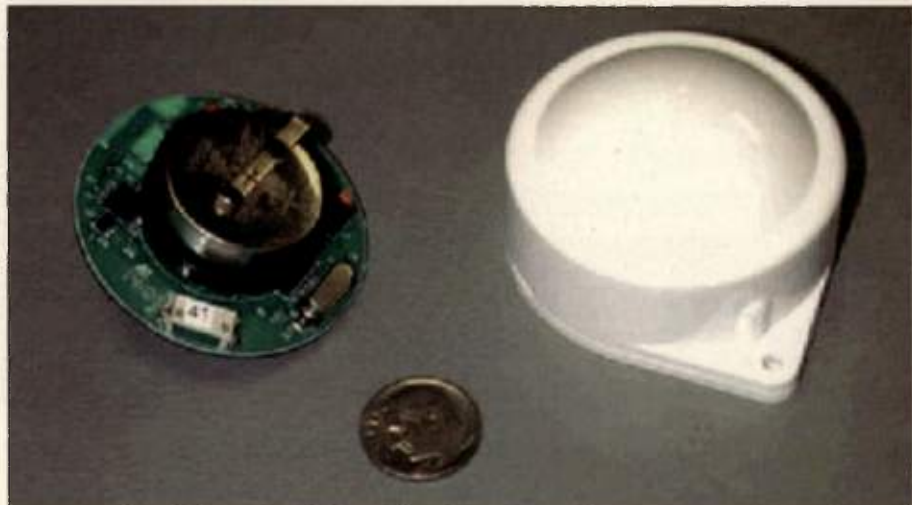
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Product Focus Unlicensed Technologies

Precision location system

Multispectral Solutions Inc. announced the grant of equipment authorization from the FCC for the company's PAL650 UWB precision asset location system. The PAL650 utilizes ultra wide bandwidth pulses to provide sub foot precision for the 2 and 3 D location of tagged objects. The UWB tag itself is about half the size of a golf ball and can transmit continuously for nearly four years on a single cell battery. The PAL650 is designed for tracking equipment and personnel in hospitals, factories and other highly cluttered environments. **Multispectral Solutions Inc.**
www.multispectral.com



Flip chip assembly

TriQuint Semiconductor Inc. announced its collaboration with Amkor Technology, Inc. to commercialize a low cost flip chip assembly process for GaAs semiconductors based on TriQuint's CuFlip bumping technology. Using CuFlip copper bumps, electrical connections once made by wire bonds are now possible by directly linking contact points on a semiconductor die to the module ceramic or laminate substrate, the company says.



TriQuint has already introduced the CuFlip process in the ultra small 6 mm x 6 mm TQM 7M4009 GSM power amplifier module (PAM).

The CuFlip process is compatible with standard laminate substrate materials. Semiconductors manufactured for CuFlip assembly require substantially less processing compared to products intended for wire bond assembly, resulting in lower cost due to high

er yield, faster cycle time, reduced work in progress, and lowered capital equipment expenses, the company says.

The repeatability of a CuFlip based module is increased compared to an equivalent wire bond module due to better control of the interconnect process resulting in improved RF performance, the company says.

TriQuint Semiconductor Inc.
www.triquint.com

Amkor Technology Inc.
www.amkor.com

PLL circuit design software

Analog Devices Inc. announced the availability of ADIsimPLL version 2.0, the next generation of its software development tool for PLL circuit design.

Using ADIsimPLL, a designer can observe detailed performance data for a PLL design, make changes to the design, and re simulate the design based on the new data, all within minutes, the company says.

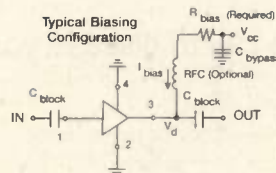
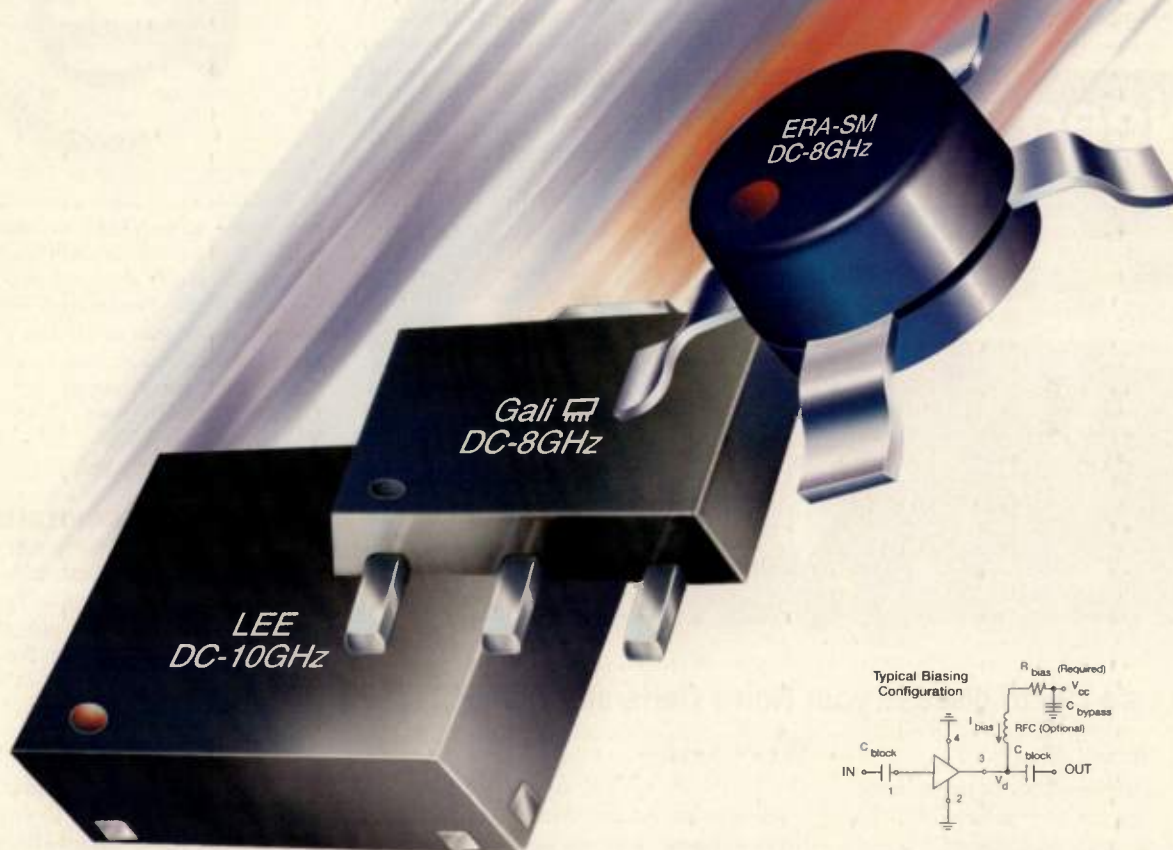
This simulation tool is offered as a free download from ADI's Web site and cuts design cycles by up to 80 percent by removing iterations from the design process, thereby resulting in faster time to market for communications product, the company says.

ADIsimPLL version 2.0 includes the ability to model all newly released PLLs from Analog Devices. In addition, ADIsimPLL

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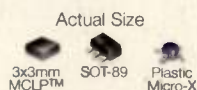
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features a new PLL wizard that includes short-form selector guides for choosing the PLL chip and VCO device. Version 2.0 is backward compatible and can read its predecessor's files; displays phase jitter results in degrees, seconds or error vector magnitude; and includes enhancements to the loop filter synthesis routines and transient simulation, the company says.

Analog Devices Inc.
www.analog.com

Tri-band internal antenna

Centurion Wireless Technologies Inc. announced the tri-band D-Puck internal antenna that simultaneously supports 802.11a, 802.11b and 802.11g applications.

The D-Puck is a tri-band micro antenna for portable devices such as laptops and PDAs, as well as fixed devices such as WLAN access points and cable modem gateways.

The D-Puck supports the 802.11 standards at 2.4 GHz to 2.5 GHz and 5.15 GHz to 5.875

GHz. Roughly the size of a computer chip, the D-Puck can also be used as the internal companion to an external antenna to enable antenna diversity.



The D-Puck features mixed polarization, and is an internal planar inverted F antenna (PIFA) that requires a small ground plane to radiate efficiently at a gain of +3 dBi in all operation bands. The antenna weighs 2 grams and has dimensions of 16 mm x 16 mm x 6 mm. It comes in tape and reel packaging for high volume manufacturing.

Centurion Wireless Technologies Inc.
www.centurion.com

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The CNG series allows carrier to noise (C/N) or carrier to interference (C/I) ratios to be easily programmed in a user specified occupied signal bandwidth. The instrument can automatically track and remove signal variations to maintain a precise noise ratio. At the heart of the instrument is a temperature stabilized "smart" noise attenuator with 0.015dB resolution and 95dB dynamic range.

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Model	Frequency range
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CNG-70/140	50MHz - 180MHz
CNG-800/1000	800MHz - 1000MHz
CNG-870/1750	870MHz - 1750MHz
CNG-800/2400	800MHz - 2400MHz
CNG-1700/2400	1700MHz - 2400MHz
CNG-2200/2700	2200MHz - 2700MHz
CNG-800/2700	800MHz - 2700MHz

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Broadband Noise (WGN) Series	
Model	Frequency range
WGN-1/200	1MHz - 200MHz
WGN-5/1005	5MHz - 1005MHz
WGN-800/1000	800MHz - 1000MHz
WGN-870/1750	870MHz - 1750MHz
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WGN-100/3000	100MHz - 3000MHz

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Bluetooth collaboration

Synopsys Inc. announced that it is collaborating with STMicroelectronics N.V. on an embedded Bluetooth solution. The companies say the collaboration will provide joint customers with a low-cost, low-power solution, by extending Synopsys' DesignWare BlueIQ Bluetooth core to support STMicroelectronics' STLC2150 radio IC.

The joint solution includes the Synopsys Bluetooth Development Kit, featuring the DesignWare BlueIQ core, and the STMicroelectronics' STLC2150 radio.

Synopsys' DesignWare BlueIQ Core is a synthesizable IP core that includes a complete Bluetooth link manager and baseband controller. It can be targeted to ASIC processes or FPGAs. The core is optimized for low power and easy integration into new and existing designs and includes a 6811-compatible 8-bit microcontroller that completely offloads the host CPU of all real-time Bluetooth activity, the companies say.

The DesignWare BlueIQ core support for the STMicroelectronics STLC2150 radio will be available at no additional cost to DesignWare BlueIQ licensees and is scheduled for general availability in the third quarter of calendar 2003.

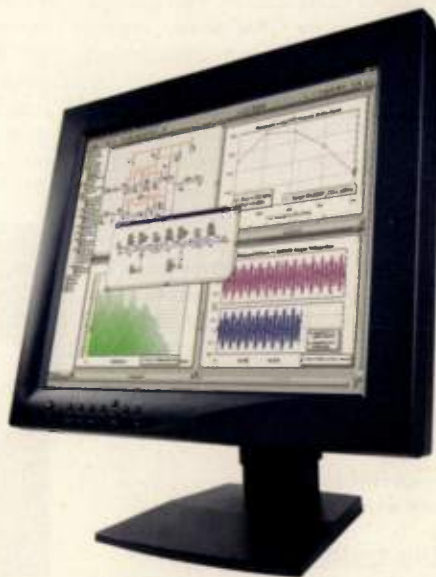
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Circle 6 or visit freeproductinfo.net/rfd

WRH

Amplifiers

Power amplifier module

Skyworks Solutions Inc. introduced a power amplifier (PA) module with a 6 mm x 6 mm x 1.2 mm module for tri band GSM/GPRS cellular handsets. The SKY77321 provides handset manufacturers with a single component solution for GSM phones, regardless of geographic region or frequency band, the company says.

The module consists of an EGSM900, DCS1800 and PCS1900 PA block, and 50 ohm fully matched input/output ports to reduce the number of external components required for a tri band design. It also supports Class 12 GPRS multislot operation.

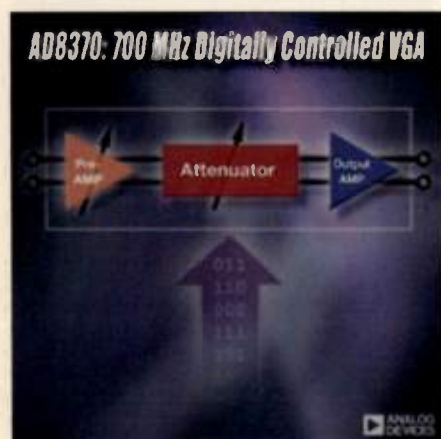
Skyworks' devices are based on a 50 GHz gallium arsenide (GaAs) heterojunction bipolar transistor (HBT) process technology and support GSM handset operation in more than 180 countries.

The SKY77321 PA module is available now. Modules are priced at \$2.75 in quantities of 10,000.

Skyworks Solutions Inc.
www.skyworksinc.com

Variable gain amplifier

Analog Devices Inc. introduced the AD8370, a high linearity, fully differential, digitally controlled variable gain amplifier (VGA) designed for wireless and wired communication networks.



The AD8370 provides a 700 MHz band width (3 dB), enabling the amplifier to be used at intermediate frequencies (IF) up to 380 MHz. The AD8370 enables designers to select between two gain control ranges (a high gain mode adjustable from 6 dB to 34 dB, and a low gain mode adjustable from 11 dB to +17 dB) through a 3 bit serial interface.

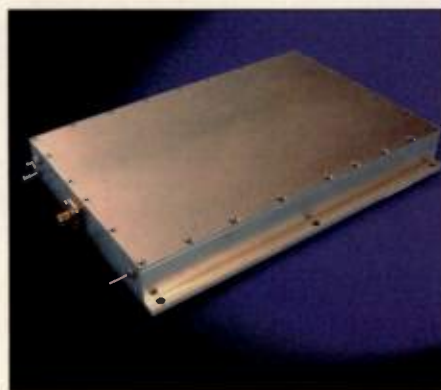
The AD8370 amplifier comes in a compact 16 pin TSSOP package and operates over the temperature range of 40° C to +85° C.

Samples and pre production quantities are available for immediate shipment, priced at \$4.20 per unit in 1,000 piece quantities.

Analog Devices Inc.
www.analog.com

Solid state power amplifier

Aethercomm introduced the SSPA 10.7 11.7 30, a high power, X band, solid state power amplifier that operates from 10.7 GHz to 11.7 GHz. At 25° C, the saturated output power is 35 W, small signal gain is 44 dB with noise figure at 4 dB, the company says. Both input and output VSWR is 2.0:1 maximum. This amplifier operates from 40° C to +65° C base plate temperature.



This SSPA is ideal for X band radar and communication systems that require high reliability, excellent linearity and high power in a rugged and compact module, the company says.

Aethercomm
www.aethercomm.com

Digital Systems

DAC with interpolation filters

Maxim Integrated Products Inc. introduced the MAX5858, a dual, 10 bit, 300 Mps DAC with integrated digital interpolation filters. This device integrates two, 10 bit DAC cores, 2x/4x programmable digital interpolation filters, divide by N clock output, and an internal reference.

The MAX5858 also features digital control of channel gain matching to within ±0.4 dB in 16 0.05 dB steps. At a 20 MHz output frequency (165 MHz sample rate), the spurious free dynamic range (SFDR) is 75 dBc. The adjacent channel leakage ratio (ACLR) is 69 dBc when the output frequency is 30.7 MHz.

The MAX5858 is available in a 48 pin TQFP package specified for the industrial temperature range (40° C to +85° C). Prices start at \$11.80 in 1,000 piece quantities.

Maxim Integrated Products Inc.
www.maxim ic.com

Digital analog converter

Analog Devices Inc. introduced a new digital analog converter (DAC) with a conversion rate exceeding 600 Msps. In addition, this device also features noise performance of 161 dBm/Hz for output frequencies between 100 MHz and 300 MHz and 169 dBm/Hz at 20 MHz output. The AD9726 provides a fast low voltage differential signaling (LVDS) input interface. The AD9726 is intended for use in high frequency, high bandwidth broadcasting and communications applications, such as MMDS (multipoint multichannel distribution service), and LMDS (local multipoint distribution system) in addition to other industries. The AD9726 is priced at \$35.00 per unit in 1,000 piece quantities.

Analog Devices Inc.
www.analog.com

Fiber Optics

Optical filter

Aegis Semiconductor Inc. announces the introduction of a new optical filter. The filter, tunable over the 35 nm of C band, was built using the company's active thin films technology platform, which enables the manufacturing of tunable components at the size, reliability, and price of passive components, the company says. Evaluation samples of the multi cavity tunable filter will be available this fall for lead customers.

Aegis Semiconductor Inc.
www.aegis semi.com

10 mW laser diode modules

California Eastern Laboratories (CEL) announced the availability of two new 10 mW DFB laser diode modules from NEC Corp. Developed for CATV and metro transmission systems, the new NX8563LA Series modules feature an extended 20° C to +85° C temperature range and, under small signal modulation conditions, bandwidth that exceeds 2.5 GHz.

Due to the intrinsic low chirp characteristic of the DFB design, NX8563LA series lasers are ideally suited for digital transmission at 1550 nm, the company says. Based on standard single mode fiber with non zero dispersion, the maximum dispersion penalty is less than 2 dB at BER = 10⁻¹⁰ for total dispersion of up to 1800 ps/nm for the NX8563LAS, and 4320 ps/nm for the NX8563LA.

Both are housed in a hermetically sealed, 14 pin butterfly packages with single mode fiber and SC APC connector. They feature an internal isolator and thermo electric cooler, and meet Telcordia GR 468 CORE qualification.

California Eastern Laboratories
www.cel.com



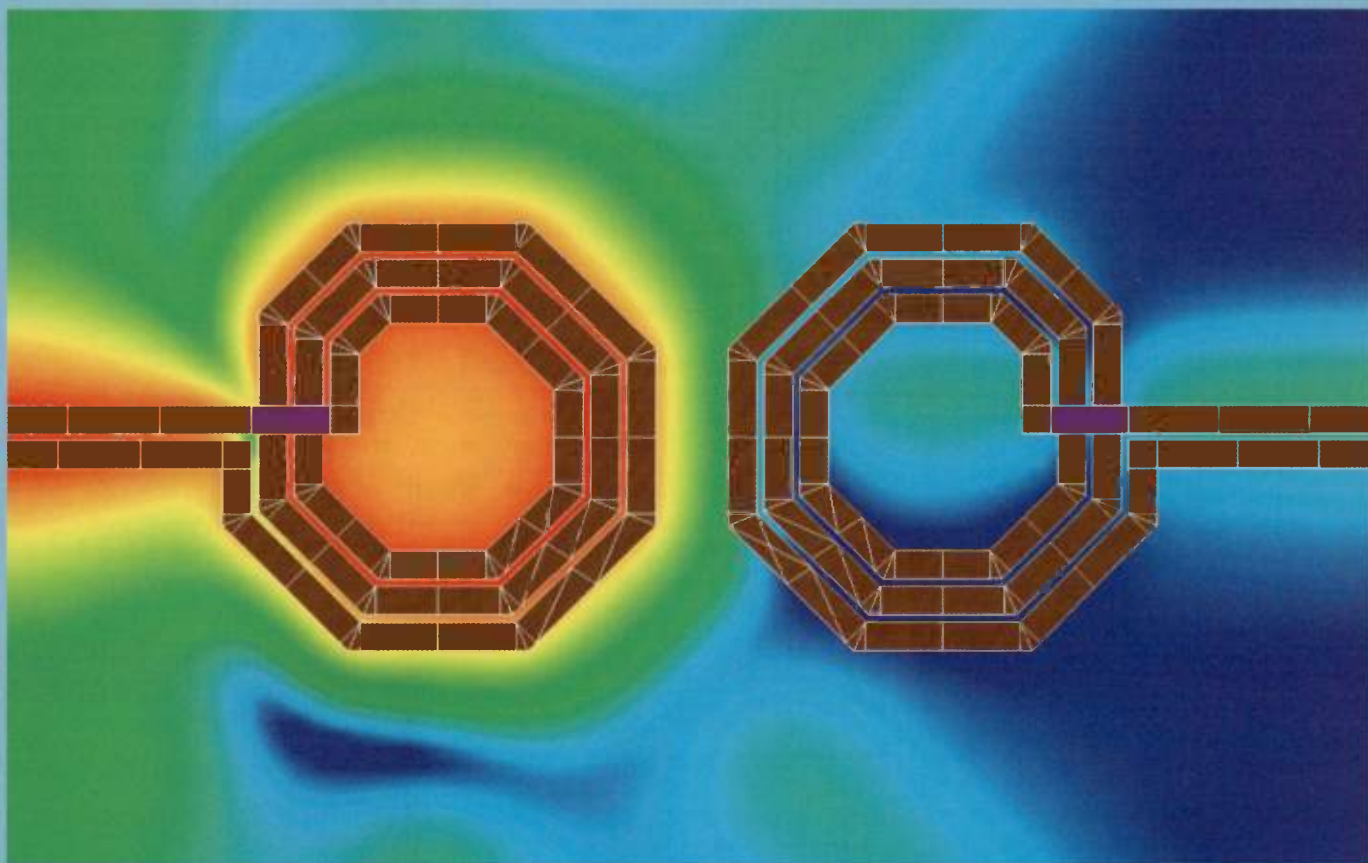
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Web Site: <http://www.zeland.com>

Circle 52 or visit freeproductinfo.net/rfd

Integrated Subsystems

Transceiver module

Maxstream Inc. introduced its 9XCite 900 MHz wireless transceiver module, which provides FCC-approved, frequency hopping spread spectrum or single channel TTL (or RS-232/422/485) communications.

The 9XCite requires no set-up, operates from 2.85 VDC to 5.50 VDC, provides long range with receiver sensitivity of -108 dBm, extends battery life using power-down mode of 20 A, and delivers data throughput rates of 9600 bps and 38400 bps, the company says. Pricing starts at for \$37 in quantities of 1,000 and is available now.

Maxstream Inc.
www.maxstream.net

Single-chip transceiver

Maxim Integrated Products Inc. introduced an 802.11b, single-chip transceiver with an integrated power amplifier and transmit/receive switch. The MAX2822-based RF PCB area measures 200 mm². Typical applications include PDAs, cellular smartphones, compact flash, secure digital (SD), and other embedded module applications.

The MAX2822 delivers 17 dBm linear power at the PA output, with a total power control range of 20 dB, while meeting 802.11b adjacent and alternate channel requirements.

An integrated PA power detector, with ± 0.5 dB accuracy, allows implementation of a closed-loop power control function. The transceiver utilizes a direct conversion (or zero-IF) architecture, eliminating the need for an external RF image-reject bandpass filter and an external IF SAW filter.

The MAX2822 operates over a 2.7 V to 3.0 V supply range and is available in a 48-pin QFN (7 mm x 7 mm) leadless package. Prices start at \$5.91 in 10,000 piece quantities.

Maxim Integrated Products Inc.
www.maxim-ic.com

GSM/GPRS module

Spreadtrum Communications Inc. announced the production of its GSM/GPRS module SM5100 that incorporates all baseband, radio frequency hardware and software needed for a full feature GSM/GPRS terminal, the company says. It offers all-in-one voice communication and high-speed data transmission via GPRS class 10. The SM5100 GSM/GPRS module uses the Spreadtrum baseband chipset SC6600 and its own protocol stack software. The Spreadtrum module and chip are in volume production.

Spreadtrum Communications Inc.
www.spreadtrum.com

Interconnect/Interface

Military-standard connectors

Northrop Grumman Corp. announced the introduction of its new Blindmate RF connectors, designed to the interface dimensions of Military Standard 348. The connector was developed by Winchester Electronics, a business unit of Northrop Grumman's Component Technologies sector.

The BMA Blindmate connectors are designed for use in Blindmate applications where multiple RF connectors need to be mated simultaneously. Typical applications include wireless base station infrastructure equipment, microwave subsystems, test and measurement, and military radar and satellite communication equipment.

The connector's blindmate capability is accomplished by the slide-on, non-locking BMA interface, designed to allow a maximum of .02-inch radial and .06-inch axial misalignment.

Northrop Grumman Corp.
www.ngcomptech.com

10 Gbps laser diode module

California Eastern Laboratories announced the availability of a new un-cooled, 1310 nm, directly modulated laser diode module from NEC Corp. Designed for 10 Gbps transmission applications in which high density mounting and power consumption are a concern, NEC's new NX8340 series modules are the world's first 10 Gbps AlGaInAs un-cooled DFB laser diodes to be fabricated using Al oxidation-free all-selective MOVPE without semiconductor etching, the company says. The NX8340 series module is available now.

California Eastern Laboratories
www.cel.com

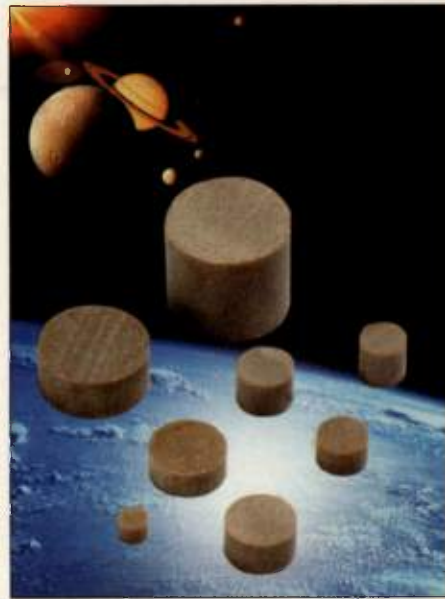
Materials

Microwave ceramics

Temex introduced a new range of microwave ceramics dedicated to space applications. The E3000 range was designed to make complete oscillator assemblies extremely stable throughout the rigorous environments experienced in space, the company says.

The E3000 family is targeted specifically at space and military applications requiring temperatures ranging from -55° C to +125° C. The new ceramic material gives a high dielectric constant to around 35 aiding size reduction while maintaining a high Q factor for stable DRO designs.

The E3000 range is manufactured to provide a wide selection of temperature coefficients, all with tight frequency tolerances, the



company says. There are currently six options available with temperature coefficients ranging from 0 ppm/degree C to 10 ppm/degree C, all offering a Q factor of 4,000 at 10 GHz.

Temex
www.temex.net

Passive Components

Coaxial terminations

Meca Electronics Inc. released new medium power loads optimized for low reflections to 3 GHz. The company's 404-F3 series and 480-F3 series coaxial terminations dissipate 35 W and 50 W average, respectively, at 5 kW peak through natural air convection with maximum VSWR of 1.05:1 to 1 GHz, 1.10:1



to 2 GHz and 1.15:1 to 3 GHz.

The 35 W 404 F3, and 50 watt 480 F3 series are offered in N male, SMA male, BNC male and TNC male connectors. Higher frequency versions are also available with low VSWR to 8 GHz.

Meca Electronics Inc.
www.meca.com

Satellite Communications

Satcom amplifiers

MK Milliwave Technologies, a division of Mast Keystone Inc., launched a new line of low noise satcom amplifiers, designed specifically for the harsh demands of satellite communications. Standard X and Ku bands are



available, and the amplifiers incorporate the latest GaAs MMICs and hybrid circuitry configurations, the company says. The units have a WR 75 input, 35 dB of SSG, 9 GHz to 10 GHz, 1.0 Nf at +50° C, +15 P 1 dbm of power and a TNC output.

MK Milliwave Technologies
www.mkmilliwave.com

Semiconductors

RF receiver

Micrel Semiconductor Inc. announced its new MICRF008 RF receiver, which, according to the company, eliminates the need for production tuning.

The product incorporates a patented sweep



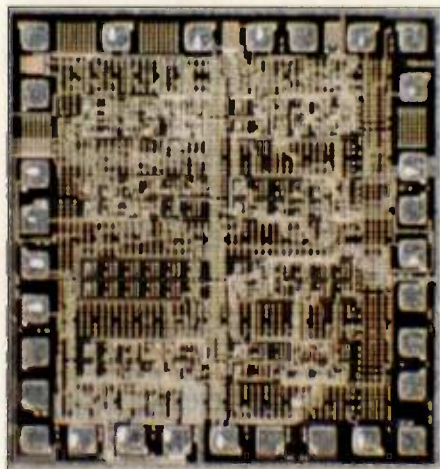
mode, which enables the superheterodyne receivers to sweep a relatively wide RF band width, in effect emulating the wide capture bandwidth of a superregen receiver.

In thousand piece quantities, the MICRF008 in 8 pin SOIC packaging is priced at \$1.29 each. Samples are from stock, and an evaluation board is available.

Micrel Semiconductor Inc.
www.micrel.com

GaAs FET device biasing solution

PIVC LLC introduced an integrated solution to the biasing of GaAs FET devices often used in millimeter wave amplifiers, without requiring knowledge of the GaAs FET gate voltage versus drain current characteristics.



The HBC 1 provides tight clamping of gate voltage to prevent damage to the MMIC being biased. The device is fully functional over the full military temperature range, and temperature is easily monitored via the temperature sense voltage. A logic level on/off feature allows the gate to be turned on and off, thus minimizing power consumption by the MMIC. The HBC 1 is available in die form (3.77 mm²), as well as a 14 pin ceramic SOIC package.

PIVC LLC
www.pivc.com

Signal Processing

LTCC filters

Mini Circuits introduced its new LFCN low pass filters and HFCN high pass filters, which the company says delivers high rejection outside the passband and virtually eliminates PC board space demand.

A number of model sizes were introduced, starting at the 0.12 inch x 0.06 inch hermetically sealed package. The company says the

MINI-CIRCUITS LTCC Filters DC-10 GHz



LTCC construction offers superior temperature stability, excellent performance repeatability, and high power handling capability.

Mini Circuits
www.minicircuits.com

Signal Sources

2.5 V HCMOS oscillator

Fox Electronics Inc. introduced the F340 series oscillator. The product is designed to consume half the power of previous oscillators and have a small footprint. Measuring 3.2 mm x 2.5 mm x 1.2 mm, the new 2.5 V HCMOS oscillators are available in frequency stabilities of ± 100 ppm, ± 50 ppm, ± 25 ppm, and ± 20 ppm, and a frequency range from 1.8 MHz to 50.0 MHz (1.8 MHz to 32 MHz at 10 mA, and 32 MHz to 50 MHz at 12 mA).



Standard operating temperature for the series is 10° C to +70° C, with an extended temperature range of 40° C to +85° C available on most models. Output symmetry is 45 percent to 55 percent at 50 percent VDD over the frequency range.

The new F340 series features a standby function for extended battery life, and comes standard in a 2,000 piece tape and reel. Pricing for the new oscillator with a stability of ± 25 ppm and a frequency of 40 MHz starts at \$3.44 per unit in quantities of 2,000.

Fox Electronics Inc.
www.foxonline.com

Voltage controlled SAW oscillator

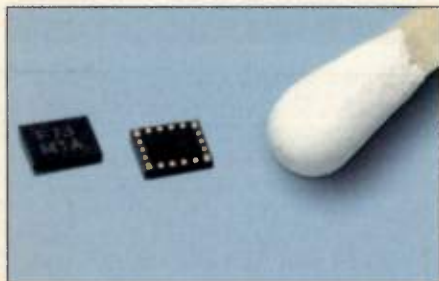
Connor Winfield Corp. introduced its new VSPLD63TE voltage controlled SAW oscillator (VCSO), which the company says provides design engineers with the lowest cost alternative for SONET equipment at 622.08 MHz.



Low jitter in the SONET bandwidth is less than 0.5 pS, and overall jitter is less than 3 pS. The oscillator has an overall total frequency tolerance of 120 ppm with an absolute pull range of ± 30 ppm minimum. With its low jitter and economical cost, this oscillator is a significant alternative for the SONET and SDH telecom equipment OEMs. This new VCSO has the lowest jitter for a 622.08 MHz oscillator in a 9x14 mm, low profile surface mount package, the company says. The pricing is at \$35.00 each in 1,000 quantities. **Connor Winfield Corp.**
www.conwin.com

Dual PLL frequency synthesizers

Fujitsu Microelectronics America Inc. introduced a new series of dual PLL frequency synthesizers, featuring power supply current as low as 2.5 mA at 2.7 V. The company says the new MB15F7xUV series provides the low noise and rapid hopping intervals required by the new generation of wireless communications systems, such as CDMA, WLAN and fixed wireless access.



Each member of the series can operate with a 2.4 V supply voltage, and offers selectable charge pump currents — either ± 1.5 mA or ± 6 mA. A high sensitivity on chip prescaler can accept a minimum of 15 dBm

input signal level at 50 ohm termination.

The new series includes four dual PLL synthesizers operating at frequencies between 0.35 GHz and 6 GHz, packaged in 18 pin bump chip carrier (BCC18) packages that measure only 2.4 mm x 2.7 mm x 0.45 mm. The members of the new dual PLL synthesizer series include:

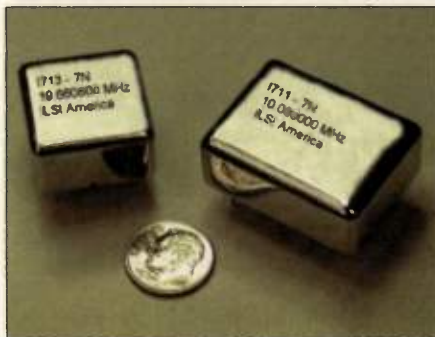
- the MB15F72UV, with operating frequencies of 0.35 GHz and 1.3 GHz, and 2.5 mA current consumption;
- the MB15F73UV, with operating frequencies of 0.6 GHz and 2.25 GHz, and 3.2 mA current consumption;
- the MB15F74UV, with operating frequencies of 2 GHz and 4 GHz, and 9 mA current consumption; and
- the MB15F76UV, with operating frequencies of 1.5 GHz and 6 GHz, and 8.5 mA current consumption.

Pricing starts at \$1.00 each in 10,000 unit quantities.

Fujitsu Microelectronics America Inc.
www.fma.fujitsu.com

TCVCXO series

ILSI America Inc. announced three new series of high stability TCVCXOs. The 1711 and 1712 series are in the "Euro Package," with the 1711 designed for TTL/HCMOS outputs and the 1712 for sine wave.



The 1713 series output is TTL/HCMOS, and is in a 1.0 square inch package. The 1714 series output is TTL/HCMOS and is in a DIP package. All three series offer frequency range from 1 MHz to 100 MHz and stabilities of ± 1 ppm over a temperature range of 0° C to +50° C at 20 MHz. Pricing is from \$12 each in quantities of 1,000.

ILSI America Inc.
www.ilsiamerica.com

Test and Measurement

Microwave synthesizer

Giga tronics Inc. announced the introduction of its new 2400 series microwave synthe-



sizer. The low noise, high power, and fast switching features of the 2400 Series Synthesizer make it an ideal test solution for a wide range of CW, swept, and stepped frequency applications in both R&D and manufacturing environments, the company says.

The 2400 series is capable of a switching frequency in less than 400 microseconds, over the entire frequency range, suitable for antenna characterization, T/R module evaluation, or RFIC manufacturing, the company says.

The synthesizer series offers two distinct models: The 2400L comes with a front panel keyboard and display, ramp frequency and power sweep, and USB interface. The 2400AL comes with a blank front panel, rear RF output, and GPIB interface. The 2400AL optimized for the ATE environment. Each model is available in three frequency ranges: 10 MHz to 8 GHz, 10 MHz to 20 GHz, and 10 MHz to 40 GHz. List pricing starts at \$17,000 with customer shipments expected to begin in August.

Giga tronics Inc.
www.gigatronics.com

Tx/Rx

Phase shifters

Planar Monolithics Industries Inc. introduced a number of digital phase shifters that operate up to 20 GHz. One model, number PS 360 90 2 202F, is a temperature compensated, 2 Bit, 360 degree digital phase shifter operating from 1.7 GHz to 2.3 GHz having phase shifts of 45 degrees, 90 degrees, 135 degrees, 270 degrees, and 360 degrees, with phase error of 7 degrees over the entire frequency band. This unit is TTL controlled and operates on +5 VDC at 50 mA and 5 VDC at 50 mA. It measures 2.0 inches x 2.0 inches x 0.50 inches.

The company also introduced a 3 dB quadrature hybrid, part number QC 052 YR3, that, when a signal is applied to any port, the hybrid will split that signal equally between the ports on the side away from the input with the port adjacent to and on the same side as the input port remaining isolated.

The direct port and the coupled port will be 90 degrees out of phase. What is most significant about the QC 052 YR3 is that it is in a 500 MHz to 2.0 GHz hybrid/coupler with a 1.45 inches x 0.75 inches x 0.22 inches pack-

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- Synthesizers for SATCOM
- Fast-tuning communication synthesizers



AMPLIFIERS TO 60 GHz

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- Power to 10 watts
- Temperature compensated
- Cryogenic



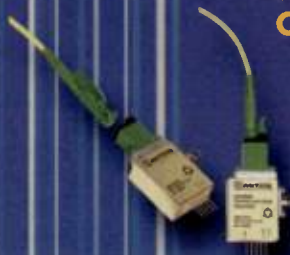
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age, and the SMA connectors are removable for surface mounting.

Planar Monolithics Industries Inc.
www.planarmonolithics.com

Subminiature solid-state switch

American Microwave Corp. introduced a subminiature, absorptive SP4T solid state switch that operates from 1.2 GHz to 1.4 GHz with a minimum isolation of 60 dB and maximum insertion loss of 2.1 dB.

The VSWR is 1.5:1 both on and off, while the total switching speed is less than 300 ns. The input RF power handling is +16 dBm, the DC power supply is ± 5 VDC and the size is 2.0 inches x 1.0 inch x 0.19 inches. The switch was developed to replace obsolete parts no longer available to defense or commercial industries.

American Microwave Corp.
www.americanmicrowavetech.com

Hybrid ring divider/combiner

Meca Electronics Inc. introduced a high power, hybrid ring divider/combiner designed to cover wireless bands from 1.7 GHz to 2.0 GHz, with average RF power handling capability of 1,000 W (5 kW peak) when an external termination is used at the isolation port.



The 700-3 (2-way, N-Female) is ideally suited for high power dividing or combining applications and measures 4.29 inches diameter x 1.56 inches. The divider/combiner provides 25 dB isolation, VSWR of 1.20:1 and insertion loss of less than 0.1 dB.

The unit is equipped with brass N-Female connectors, gold plated copper contact pins, virgin electrical grade PTFE insulation within the connectors, and an aluminum housing for shielding. Operating temperature range is -65° C to +150° C.

Meca Electronics Inc.
www.e-meca.com

20 W high-power limiter

Planar Monolithics Industries Inc. introduced a high power limiter, the PMI model number LM-20M80M-10-20W, that operate from 25 MHz to 80 MHz with an input power level of 20 Watts. Insertion loss is 0.5 dB



maximum, it has a VSWR of 1.5:1 typical and 1 Fsec recovery time. The output limiting is +15 dBm maximum. The size is 1.0 inch x 1.0 inch x 0.40 inches.

Planar Monolithics Industries Inc.
www.planarmonolithics.com

Thin-film chip attenuators

State of the Art Inc. (SOTA) introduced a new line of thin film chip attenuators utilizing (AlN)aluminum nitride. Case sizes 0706, 1005, and 1512 are available with several different termination styles in addition to styles available for wire bonding and epoxy mounting.

These devices are available with attenuation factors of 1 dB to 20 dB in 1 dB increments with a frequency range from DC to 20 GHz. Attenuation stability is typically better than ± 0.5 dB over the entire frequency range.

Packaging options include waffle pack and tape and reel. Pricing for these components is under \$1.39 in production quantities.

State of the Art Inc.
www.resistor.com

Wi-Fi/Bluetooth

Single-chip WLAN transceiver

Airoha Technology Corp. announced the Airlink AL2210; what the company is calling the industry's most integrated single chip WLAN transceiver with an embedded power amplifier (PA) for WLAN RF applications based on Jazz Semiconductor Inc.'s (www.jazzsemi.com) SiGe technology. The single chip transceiver is highly integrated with on-chip components such as a VCO, LNA, oscillator, and balun.

Airoha Technology Corp.
www.airoha.com.tw

www.rfdesign.com

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Ivo Bolsens, Ph.D., Vice President and Chief Technology Officer, Xilinx

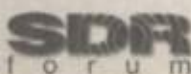
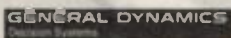
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Training materials for all types — a review of Noble Publishing's instructional CDs

By Keith Vick

I recently received a set of instructional CDs from Samuel Dennis Ford of Noble Publishing Corp. (www.noblepub.com).

Having been brought up on instructional CDs from the PC industry I fully expected to yawn and roll my eyes at the presentation of the material. However, I was pleasantly surprised and impressed by the presentation and content of the CDs.

In particular, the "RF Fundamentals" CDs were excellent presentations of both the background theory and practice. Randy Rhea's CDs were interesting due to the liberal use of slick graphics and presentation.

The important thing to keep in mind if you are considering purchasing the CD sets is that they appeal to two different and specific types of markets.

RF Fundamentals I and II

"RF Fundamentals I," by Less Besser of Besser Associates (www.bessercourse.com), covers many topics beginning with the basics of complex mathematics, high frequency models of passive components and eventually ends up in more advanced topic of small signal amplifier design. In most of the lessons, the individual topics end with coverage of a real-world example. The "RF Fundamentals I" course set is followed by "RF Fundamentals II."

The screen presentation is that of screens showing video, course navigation and notes. The upper left quadrant of the screen with a video presentation alternating between footage of Les and notes he scribbles.

The right side is a more formalized presentation of his scribbles and notes. The lower left hand side consists of the navigation menu of the course. This arrangement is highly suited for easy navigation of the topics. The CD didn't seem to mind my rather dilettante style skipping around and amicably oblige my requests with minimal skipping or hesitation.

The CDs are priced at \$595 for "RF Fundamentals I," and \$595 for "RF Fundamentals II." Obviously, the pricing needs to be considered in context of investing in engineers by an organization.

I highly recommend the set as a library item for engineers to check out in addition to initial training materials for new engineers joining an organization. I know that I would have appreciated a formal set of painless training materials to introduce me to RF concepts.

The Basic RF and Microwave Design series

The publication I reviewed is "Basic RF and Microwave Design" series by Randy Rhea. This CD is part of a series of publications that are single servings of a particular topic. The CD I reviewed was that of "Q from A to Z."

It covers the topic of Q, or component quality. The real value of the CD is the in the thoroughness of the examination of the topic and how it relates to topics such as the Smith chart and resonators. The clarity of definition of different types of Q and adhering to the definition is very helpful in following the course.

The presentation of the material was slicker than "RF Fundamentals."

Although the overall appearance of the screens were rather nice, and the organization precise, the actual navigation proved to be somewhat clumsy. I don't know if it is because of my rather weak 600 MHz Intel Celeron laptop, or the processing requirements of the program, but the video skipped and there were annoying delays when navigating around the course.

The pricing of the "Q from A to Z" CD is \$79. There are other CDs covering topics such as "Lumped Element Transforms" and "Filter Design by Transmission Zeros." The CDs are single servings in depth examination of topics, so the interested market is going to be different than that of "RF Fundamentals."

The market for "Q from A to Z" is that of an engineer that isn't quite satisfied by the information he or she gets from text books, and would like a nice presentation that covers a topic clearly and concisely.

I believe that CD series are excellent additions to a company's technical library resource. The CDs can be easily checked out and reviewed by engineers enough to justify their meager costs. When one considers that part-time engineering education can cost thousands of dollars per course at a local university, these CDs are positively bargains because they are available on demand and with limitless viewings.

Keith Vick
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