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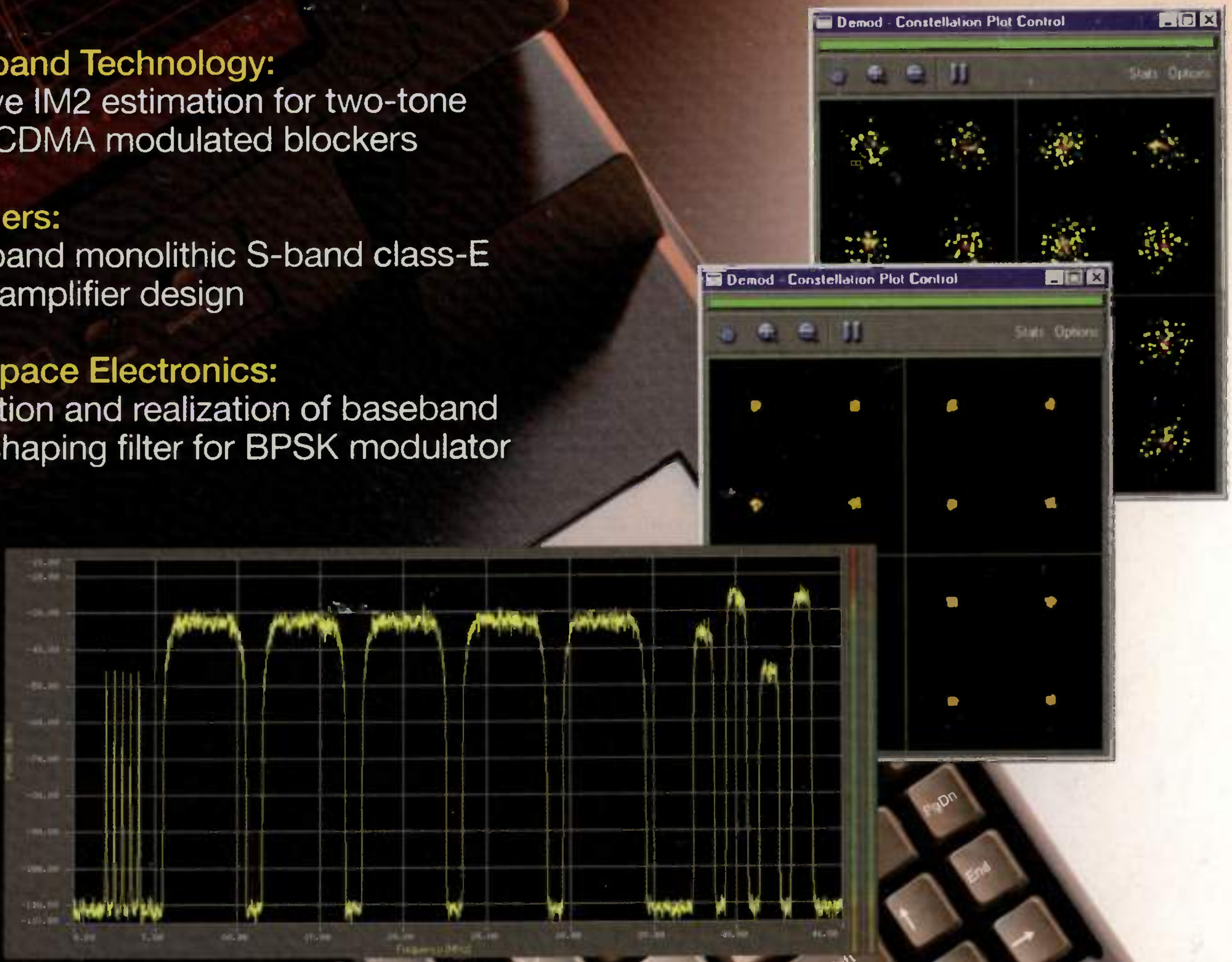

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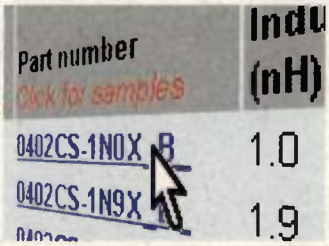

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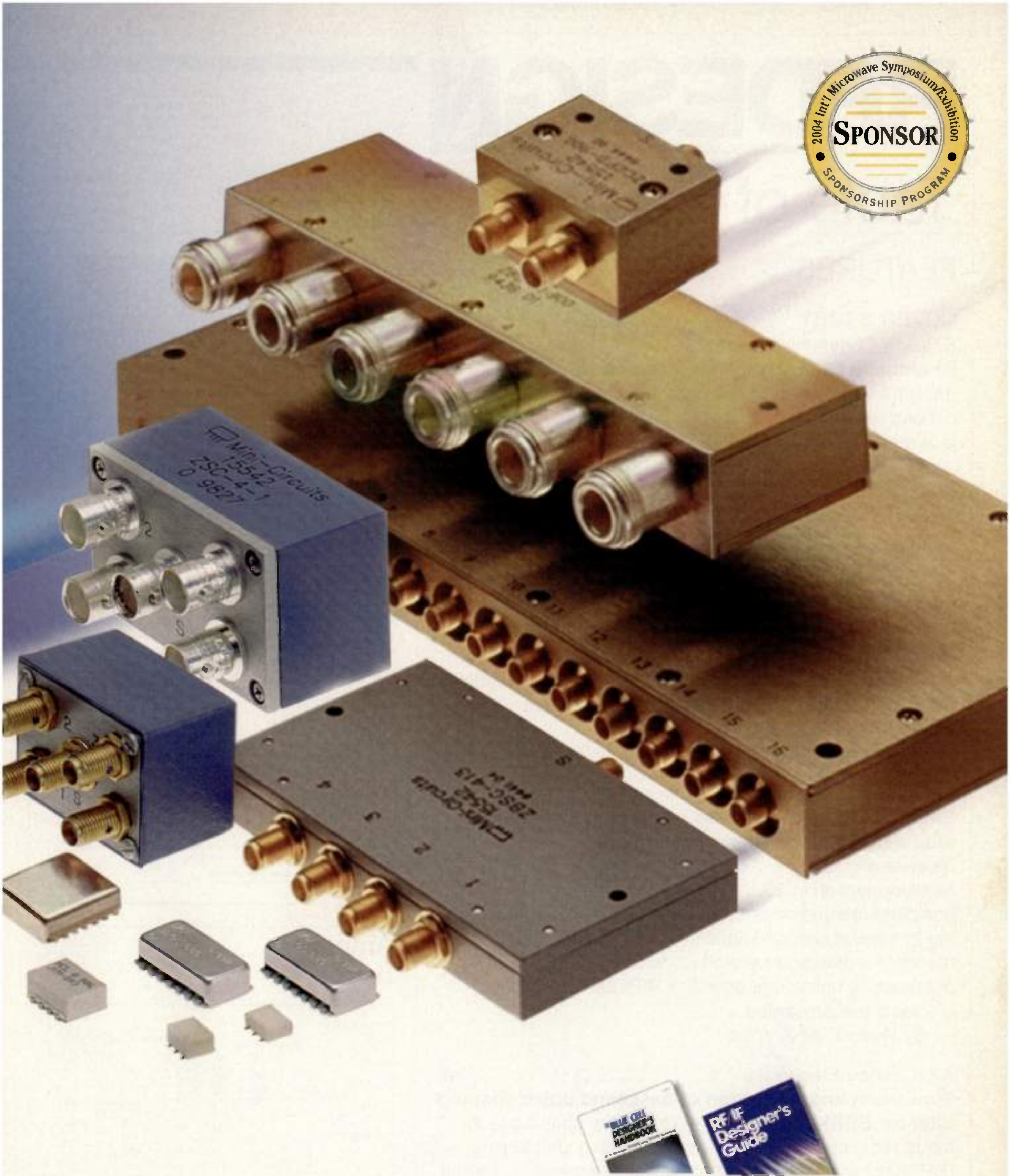

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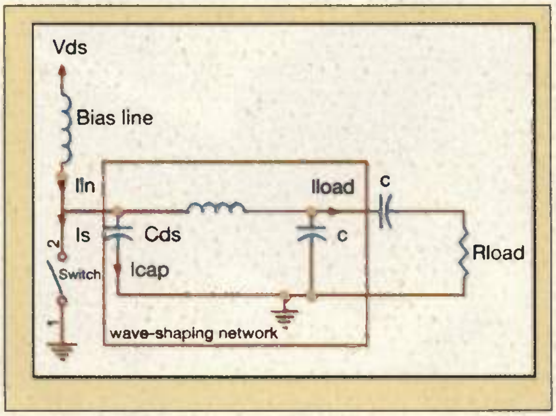

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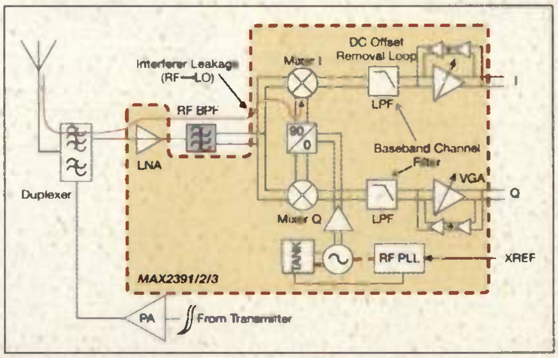

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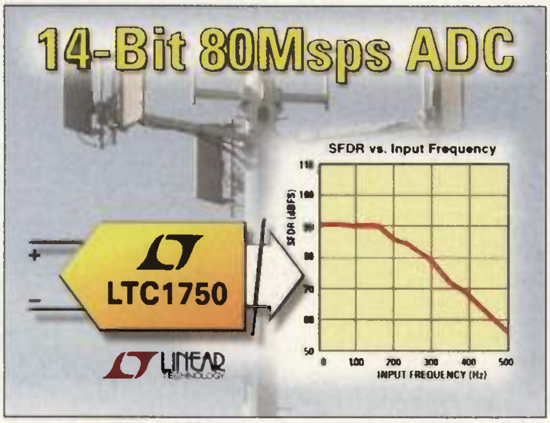

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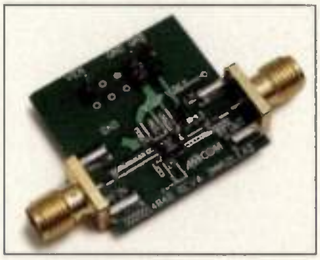

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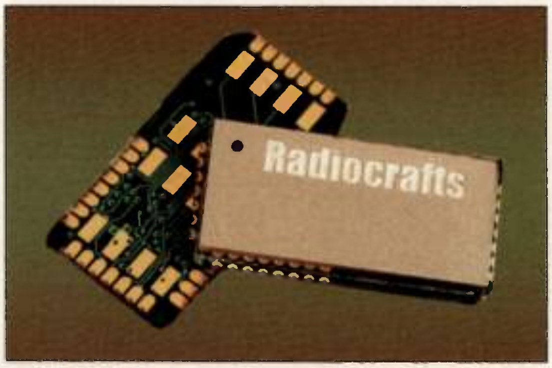

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VAT-3	HAT-3	3	3	0.15	0.12	1.15	1.1
VAT-4	HAT-4	4	4	0.15	0.08	1.15	1.1
VAT-5	HAT-5	5	5	0.10	0.06	1.15	1.1
VAT-6	HAT-6	6	6	0.10	0.02	1.15	1.1
VAT-7	HAT-7	7	7	0.10	0.05	1.15	1.1
VAT-8	HAT-8	8	8	0.10	0.04	1.20	1.1
VAT-9	HAT-9	9	9	0.10	0.02	1.15	1.1
VAT-10	HAT-10	10	10	0.20	0.03	1.20	1.1
VAT-12	HAT-12	12	12	0.10	0.04	1.20	1.1
VAT-15	HAT-15	15	15	0.30	0.05	1.40	1.1
VAT-20	HAT-20	20	20	0.75	0.18	1.20	1.1
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Editor's Notes

Accelerating the adoption of radio-frequency identification or RFID

While radio frequency identification (RFID) is no immediate threat to the popular UPC bar codes that we all have known for decades, the latest burst of activity in this sector suggests that RFID is coming soon. And is progressing faster than analysts predictions. Compliance mandates issued by giant retailers like Wal-Mart and Target, as well as the U.S. department of defense (DoD), along with other government and industrial organizations, has provided sufficient fuel to accelerate its adoption and push it on to the shelves of stores, product assembly lines, inventory management in the defense establishments, anti-terrorism solutions, baggage handling at the airports, and a host of other applications. Furthermore, as it evolves, it is likely to create many new applications that were unthinkable with traditional bar codes.

Thus, it is not surprising to see attractive market projections made by several research firms. For instance, according to Venture Development Corp., global shipments of RFID systems (hardware, software, and services) reached nearly $965 million in 2002 and is expected to touch nearly $2.7 billion by 2007. Similarly, according to a study by Allied Business Intelligence Inc., the RFID market will jump from $1.4 billion annually last year to as much as $3.8 billion in 2008. By the same token, International Data Corp.'s study indicates that spending on RFID technology used to track goods in retail supply chains will grow to nearly $1.3 billion in 2008. Last year, about $91.5 million was spent on chip-based tags and related hardware, software and services, according to IDC.

Although, these market projections look appealing, there are many hurdles that must be overcome before the technology makes any noticeable gains in the commercial world. Some experts are of the opinion that price of RFID tags will play a significant role in driving the technology into mainstream applications and are looking at 5 cents in large volumes as the price point for RFID tags. Incidentally, with 5 cents as target, a consortium in Japan has undertaken a project to develop inexpensive chips for use in RFID tags. Meanwhile, leveraging its self-adaptive silicon technology, analog and mixed-signal IC developer Impinj has readied a low-cost, long-range, field rewritable system called Zuma. Unprecedented, it enables users to write data to tags at long range, thereby greatly enhancing the functionality and value of RFID deployments in the supply chain. As a new entrant into this arena, the developer promises to comply with a single, open, worldwide RFID standard.

But, lower price alone will not play a major role in its success. "Five cent tags are a component to the overall success of RFID but they are not one of the top five most important elements," says Erik Michielsen, principal analyst at ABI Research. He adds, "Without proper commitment, planning, and partnering, inexpensive RFID hardware is not sufficient to make a sustainable long-term difference with consumer packaged goods suppliers looking to benefit from RFID."

Consequently, as makers struggle to lower cost, developers such as tag creators, scanner manufacturers, software middleware developers and system integrators must work closely to expedite the standardization process. For without a standard and universally interoperable tags and readers, the chances are dim.

Realizing the importance of a standard in gaining momentum, last October EPCglobal was established as a non-profit joint venture of the standards organizations EAN International and the Uniform Code Council Inc. EPCglobal is overseeing the development of the electronic product code (EPC) standard. Many companies have become members of the EPCglobal's hardware action group, as well as software action group, to expedite the development and rapid ratification of a global, interoperable EPC standard using ultra-high frequency (UHF) RFID technology. In fact, the group is working on a new generation UHF Gen2 standard.

While in the United States EPCglobal is working toward a standard RFID solution, overseas International Organization for Standardization (ISO) is doing its part to generate a universal RFID specification. Even today, different regions around the world are using a variety of frequency bands to address the problem. It's about time that these organizations work closely, so that the end result is a common standard for tags, readers and writers, and other service providers. It also is a better chance for the technology to proliferate around the globe much faster than expected. The market potential is enormous.

It will be interesting to see how the RFID solution evolves in the next few years and co-exists with traditional bar codes.

Ashok Bindra

Ashok Bindra, Editorial Director

3G deployment better late than never

Despite many years of delays, it seems to be better late than never for 3G wireless deployments, reports In-Stat/MDR. The high-tech market research firm reports that, despite all the problems associated with 3G, a fair number of operators have launched commercial services and many other carriers have purchased infrastructure equipment, but have yet to deploy 3G commercially.

3G is fulfilling its promise of offering the increased capacity, lower-cost infrastructure that carriers have wanted all along. For this reason, 3G has been a partial success for those carriers that are spectrum constrained, and this generally is in Japan. For Europeans, 3G is helping to keep costs low. A few carriers in Europe have started offering 3G voice service at lower prices than other carriers.

"Although the press has long been publishing stories about the doom and gloom of 3G, the reality is that 3G is happening, although maybe a bit later and smaller than many had hoped," says Allen Nogee, a principal analyst with In-Stat/MDR. "3G infrastructure is shipping, 3G licenses are being used, and there are a fair number of 3G handsets available. If there is one big missing aspect of 3G, it would have to be subscribers, especially outside of South Korea and Japan."

The delays in the rollout of 3G can be attributed to many factors, but the main three would be the lack of good inexpensive handsets, technical issues, and a general lack of consumer interest. Note that good handsets are starting to appear in greater numbers, and most of the technical issues have been resolved. The last piece of the puzzle to fall in place is demand for 3G from the consumer. It is this last aspect that may be the biggest challenge for 3G. However, as uses for the new technology grow, and demand for its unique services increase, 3G will grow into a valuable service, and will not only be nice to have, but a necessity.

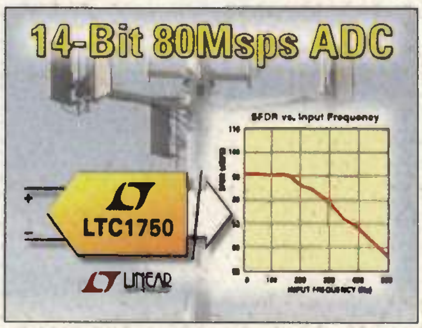
The report, "3G Deployment Status: Better Late Than Never?" (#IN0401274GW), looks at some of the issues related to deploying 3G throughout the world, and contains the status of almost 200 3G carriers who have, or will soon deploy 3G, and includes the air-interface they use, the dates and amounts of recent 3G infrastructure contracts awarded, who they purchase infrastructure from (when known), and estimates of the number of W-CDMA Node B's they purchased in 2002 and 2003. Carriers are sorted by launch date, country, and air-interface deployed.

For more information, visit www.instat.com.

Speedier 14-bit ADC eases base station design

A new 80 Msps, 14-bit analog to digital converter (ADC) from Linear Technology provides designers of cellular base stations with an improvement in dynamic performance, according to a company press release. The LTC1750 simplifies the design and reduces the cost of cellular base stations by eliminating the second intermediate frequency (IF) downconversion stage. The device provides wide input bandwidth and excellent dynamic performance for direct IF digitizing applications. The LTC1750 undersamples up to 500 MHz input frequencies and delivers 84 dB spurious free dynamic range (SFDR) with 140 MHz inputs and 74 dB SFDR with 350 MHz inputs. The device's wide bandwidth and AC performance make it suitable for use in cellular base stations and broadband software radios, where it can directly digitize the first IF and eliminate the second IF downconversion stage.

The ADC offers the flexibility to configure the input and the output specifically for the application. An on-chip programmable gain amplifier (PGA) allows multiple input ranges to optimize the performance. The larger input range offers low noise, and the smaller range lowers the gain requirements on the drive circuitry, making it easier to meet the IP3 requirements. If the input ever goes out of range, there is automatic indicator on the overflow pin. A separate digital output supply pin allows connection to low-voltage DSPs, FIFOs or logic as low as 0.5 V.



Linear Technology offers the 80 Msps, 14-bit analog to digital converter.

For more information, visit www.linear-tech.com.

EM Microelectronic develops ISO 18000-6A and EPC code structure-compliant IC

EM Microelectronic, a company of the Swatch Group has developed a UHF RFID integrated circuit, EM4223, which is fully compliant with the international standard ISO18000-6A and EPC 64-bit and 96-bit code structure.

The EM4223 is a high-performance 128-bit read-only UHF circuit with a robust anti-collision protocol. It is frequency-independent from 865 MHz to 2.5 GHz and is compliant with worldwide radio regulations. It works with very low radiated power in the United States, as well as Europe and Japan. The IC has been designed using EM advanced CMOS technology optimized for RFID and will be produced in EM's own fab in Switzerland. The circuit layout has been conceived for easy assembly by antenna manufacturers.

The IC can read tags at a distance above 15 meters when using an optimized transponder antenna. It also has an enhanced anti-collision protocol, which performs without saturation effect. With other RFID chips, it may happen that the reader saturates and is not able to read more than a certain number of tags because the transmission channel becomes saturated.

"The saturation limits of the transmission channel of EM4223 are extended to such a point that a reader is able to read more than 1000 tags simultaneously present in the field," said Mougahed Darwish, president of the management board of EM Microelectronic. "Due to its high-speed,anti-collision feature, it is also possible to read 200 EM4223 tags per second. This high throughput will set new performance benchmarks, especially when operating under the prevailing ETSI regulation."

EM4223 tags can also enter and/or leave the field without corrupting the anti-collision protocol itself, ensuring that all tags are read. This key feature is particularly important in logistics applications where tracked items are always in motion.

The Application Family Identifier (AFI) is a segment of the memory, in addition to the user memory, which defines families of items to be tracked as per ISO18000-6A. AFI allows a direct selection mechanism, enhancing the anticollision throughput and reducing the data flow on the network. With this feature embedded in EM4223, it is possible for a reader to make a reading only on one specified type of item while included as part of a group of different items. For instance, this feature is useful in the case of a pallet containing different types of goods and one wants to read only one type among all of the goods.

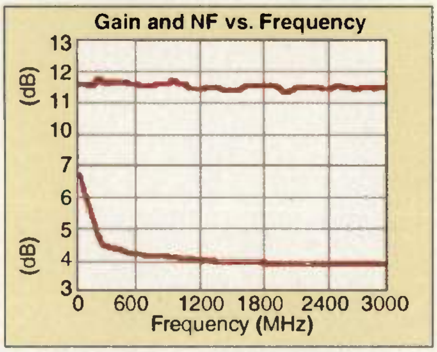
The Electronic Product Code (EPC) is a unique ID number that identifies a specific item in the supply chain. The EM4223 complies

with the current EPC code specification with the possibility to encode the EPC64 or EPC96. The most popular EPC96 is the GTIN number, but any other can be placed within the 128-bit user data segment of EM4223.

For more information, visit www.emmicroelectronics.com.

Surface-mount VGA covers wide frequency range

Microwave Technology's MPS-002701-84 variable gain amplifier (VGA) offers an exceptionally broad frequency range for a surface-mount VGA. While some other, comparable surface-mount VGAs operate up to 2 GHz, this amplifier operates with good gain flatness from 3 MHz to 2700 MHz (see the figure). Moreover, the VGA is operational down to nearly 100 kHz. Capable of replacing existing devices built in the TO-5 metal can, the MPS-002701-84 comes in a ceramic SOT-8 that measures 0.160 by 0.200 inches.



The MPS-002701-84 VGA exhibits good gain flatness over a broad frequency range.

The GaAs FET amplifier operates with +5-V bias and features an IP3 of 34 dBm, a P1db of 20 dBm, and a 30% power-added efficiency all typical values. Small signal gain is 11.5 dB typical and noise figure is 5.0 dB typical from 100 MHz to 2700 MHz. The part also offers 50-Ohm output impedance. Many of this VGA's specs including gain vs. control voltage are similar to those of the company's MPS-003001-87. However, the latter device specifies operation from 20 MHz to 3000 MHz and features more costly, fully hermetic packaging.

In low volumes, the MPS-002701-84 is priced around $40, which is said to be one-third of equivalent competitive units.

For more information, see www.mwtinc.com or contact the company at 510-651-6700.

RF LDMOS transistors come in plastic packages

To lower the cost of silicon RF transistors by almost 25 percent, Allentown, Penn.-based Agere Systems has packed five high-performance RF LDMOS transistors in lead-free overmolded plastic packages. Developed in cooperation with Amkor, the plastic-packaged transistors are capable of continuous operation at 200°C junction temperature. They are suitable for wireless base station amplifiers.

Agere announced its entry into this business last year. This year the company is announcing availability of low-cost plastic RF transistors. By comparison, ceramic is a more expensive material and has been the main substance for RF transistors for the last several years. Because of cost pressures, RF transistor suppliers are slowly transitioning to plastic.

A key feature of this package is that it uses a die attach with high thermal conductivity, according to Agere's analog group CTO Peter Gammel. In addition, the package offers lower thermal resistance between the transistor die and its heat sink. Thus, it improves reliability and requires less thermal derating.

The following Agere chips are being offered with overmolded plastic packaging: AGRA10, AGR09030, AGR09045, AGR09060 and AGRB10. The first four listed can be used across frequencies ranging up to 1 GHz. The AGRB10 can be used in frequencies spanning from 1 GHz to 2.7 GHz. These five new LDMOS devices range in power from 10 W to 60 W.

For more information, visit www.agere.com.

Company raises $1 million for product development

Wispry, an Irvine, Calif.-based fables developer of tunable RF components and modules for the wireless applications has raised $1 million in funding to expand product design and development as well as its sales and marketing efforts. Tech Coast Angels invested more than $900,000 in this round of funding.

Wispry's products are implemented using micro-electromechanical systems (MEMS) technology. MEMS-enabled products provide RF system manufacturers with unique performance, cost and power consumption characteristics. Wispry's initial products are RF-MEMS switches for mode switching, antenna diversity and configurable power amplifier applications. MEMS switches can reduce space, cost and achieve a combination of high isolation and low insertion loss, which will reduce power consumption, increasingly important in consumer electronics ranging from cell phones and PDAs to game controllers.

For more information, visit www.wispry.com.

Ember buys 802.15.4 radio technology; targets Zigbee market

Ember Corporation, Boston, Mass., has purchased a deep portfolio of 802.15.4 RFIC technology from Cambridge Consultants Ltd. (CCL) and has hired the engineering team that developed it.

These strategic moves enable Ember to offer radio, network and software in an integrated 802.15.4/"ZigBee" package that will serve the rapidly emerging market for low-cost, low-power networking applications.

The market for ZigBee chips is expected to reach half a billion units by 2008, according to analyst Kirsten West of West Technology Research Solutions. "The potential size of these new wireless markets totally dwarfs anything we have seen so far with early consumer wireless standards," West said.

The CCL deal gives Ember:

- Exclusive rights to CCL's 802.15.4 single-chip architecture, which supports low-power radio communications in demanding environments such as industrial facilities.
- A license to use CCL's library of low-power radio components; and a wide range of digital communications intellectual property.
- Two years of CCL's integrated circuit development services to accelerate product development.

Paired with Ember's embedded mesh networking intelligence, CCL's radio technology will create a single-chip platform for mesh networking applications such as building security, heating, cooling, lighting and ventilation; inventory control; industrial controls; and transportation infrastructure safety monitoring. CCL is one of the world's top developers of wireless applications, integrated circuits and intellectual property for low-powered, embedded radio.

"This acquirement proves our commitment to the market and to consolidating key intellectual property–networking and radio–in one product," said Ember CEO Jeff Grammer. "Companies developing 802.15.4-based products need radio and networking technologies that interoperate seamlessly, instead of spending valuable development time stitching them together."

The development team, which is now part of Ember, will be the core of an expanded European presence based at CCL's facilities in Cambridge, UK. Ember Europe now becomes the "fabless" silicon arm of Ember Corporation. The subsidiary also includes Ember's existing UK sales and service staff and former CCL associate director Jim Schoenenberger, who takes the position of director of business development.

For more information, visit www.ember.com.

Broadband channel simulator for robust satellite link designs

Impairments in broadband satellite communications signals occur, but by simulating these impairments in a real-time environment, a broadband communications system design can be proven and optimized prior to production.

By Jack Anderson

In the real estate market, there are three priorities: location, location and location. In the broadband satellite communications arena, the top three priorities would be data, data and data. In mainstream, down-to-earth communications systems such as DSL, cable modems, WiFi and even cellular, high-speed access to information is fast becoming a must-have and is highly addictive. Anyone who has worked from a dial-up modem connection after getting accustomed to broadband knows what this means.

Data rates in satellites are an element of the overall capacity of the satellite. Multiple transponders, transponder bandwidths, carrier frequency, transponder receive sensitivity, transponder transmit power, communication signaling schemes, and communication data structures all contribute to the capacity equation. A recent industry study indicates that from 1990 to 2002, the average number of equivalent 36 MHz transponders on geosynchronous satellites increased from 26 to 48 transponders per satellite launched. This same study showed that the average power levels for these satellites increased by 350%, the design life increased from 10 years to almost 14 years, and the satellite size and complexity increased by factors of 2 to 5 times[1]. Shin Satellites' iPSTAR, a new generation of Internet Protocol (IP) satellites, boasts a total capacity of 40 Gbps, which they claim is a 40 times increase over current satellite capability.[2] Hughes Network Systems' SPACEWAY has a 800 Mbps downlink data rate per spot beam[3] and includes sophisticated on-board processing, dynamically switched spot beams, bandwidth-on-demand allocation and TDMA formatting. SPACEWAY will set the bar for fielded commercial satellite technology when launched this summer.

The advanced broadband communications satellites being developed today are costly to design, manufacture and deploy. Most will be placed in geosynchronous (GEO) orbits. They require a significant initial capital outlay years before they are placed into service and start to see revenue returns. To this extent, the satellite designers try to maximize payload capacity, so that once in service, the satellite operator will achieve the greatest revenue stream. It is part of the fundamental return-on-investment (ROI) business calculation—the more capacity, the more potential sales.

In an ideal world, all design parameters would be maximized to obtain the highest possible capacity and performance. In the real world, real trade offs in these parameters

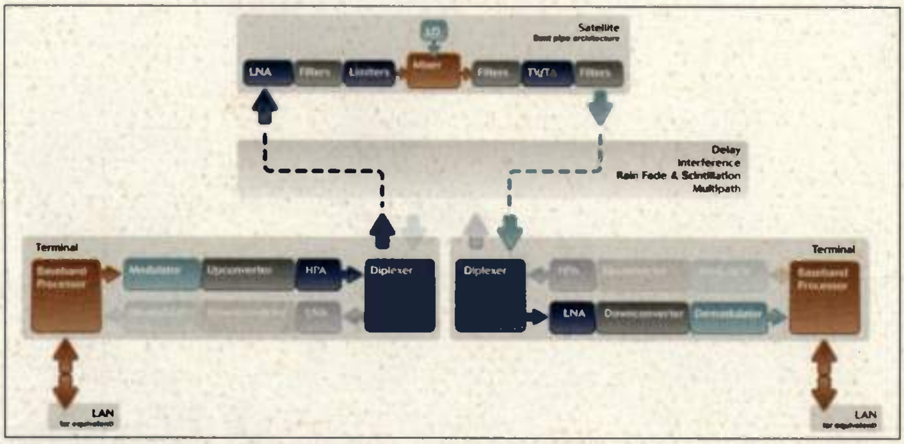


Figure 1. Notional diagram of satellite communication link.

Impairment	Cause
Thermal Noise	Amplifier NF, Channel
Phase Noise	LOs, PLLs, Ref Oscillators
Passband Amplitude Distortion	Filters, Amplifiers
Group Delay Distortion	Filters, Amplifiers
AM-AM/AM-PM Distortion	Amplifiers
I/Q Balance	Mixers, DACs, ADCs
Polarization Errors	Antenna Elements
Adjacent Channel Interference	Amplifiers, Mixers
Rain Fade	Channel, Environment
Multipath	Channel, Environment

Table 1. Channel impairments and associated causes.

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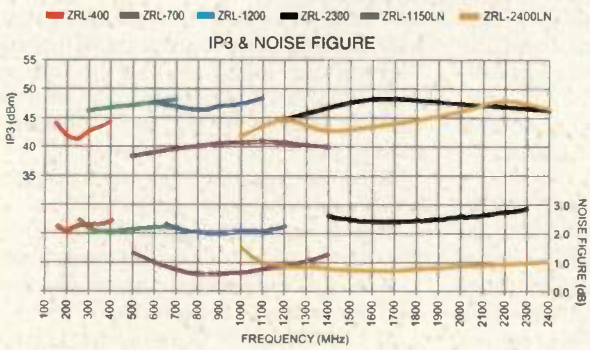

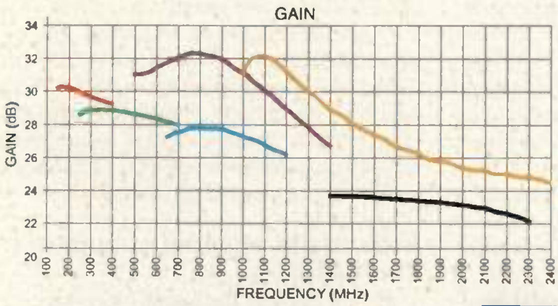

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Model	Freq. (MHz)	Gain (dB)	Noise Fig. (dB)	IP3 (dBm)	Max. Pwr. Out @1dB Comp. (dBm)	Price $ea. (1-9)
ZRL-400	150-400	30	2.5	42	25.0	119.95
ZRL-700	250-700	29	2.0	46	24.8	119.95
ZRL-1150LN	500-1400	31	0.8	40	24.0	119.95
ZRL-1200	650-1200	27	2.0	46	24.3	119.95
ZRL-2300	1400-2300	24	2.5	46	24.6	119.95
ZRL-2400LN	1000-2400	27	1.0	45	24.0	139.95

DC Power 12V DC, Current 550mA, Dimensions: (L) 3.75" x (W) 2.00" x (H) 0.80"

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Figure 2. Celerity CS80072 broadband channel simulator.

must be carefully considered and modeled to ensure design goals are achieved. For example, as the carrier frequencies go up, the available bandwidth increases, but available technology to generate the downlink power decreases. And while higher bandwidths will support faster data rates, the lower power decreases the signal-to-noise ratio (SNR) at the receiver, which will limit the effective data rate achievable through the system. The trend in downlinks moving from L band (2.4 GHz) and C band (6 GHz) to Ku band (14 GHz) and Ka band (30 GHz) also bring with it the challenges of increased atmospheric attenuation, pronounced rain fade and scintillation.

In addition to the move to Ku and Ka bands, other trends in the industry include:

- Increased transponder bandwidths from standard 36 MHz to 72 MHz and beyond.
- Changes in signal modulations from standard BPSK and QPSK to 8PSK, QAM, concentric PSK or Star QAM, and even OFDM[4].
- Frequency-hopped carriers.
- More robust coding, including turbocodes.

So what does this mean to the satellite design engineer?

As advanced communications satellite designs push the envelope to maximize data rates and capacities, they can leave little margin for error. Any parameter or real-world effect not analyzed or accounted for could offer surprises that lead to degraded performance and corresponding loss of revenue. The converse is that the system may be overdesigned, putting too much margin in each parameter due to unknowns or worst-case estimates, adding unnecessary cost in price, components, weight, and complexity. Many parameters and variables need to be considered, and the entire communications channel must be analyzed—both satellite and ground terminals. Figure 1 is a notional diagram of a complete satellite link for a traditional "bent pipe" configuration, showing the major components. The satellite portion shows only one transponder slice. In reality, from 30 to 50 transponders could be on the satellite.

Figure 3. Major functions of an ideal broadband channel simulator.

Each component has its non-ideal performance, which can lead to an overall degradation in the system. A representative list of degradations, also called impairments, along with the component causing the impairment is shown in Table 1. The first and most basic impairment is thermal noise. With the carrier power it sets the carrier-to-noise ratio (CNR) or SNR in a channel. When SNR and bandwidth are specified, Shannon's law defines the maximum channel capacity in bits per second, a limit that is never achieved. Many papers have been written on this subject, and exhaustive theoretical studies have been performed to predict the raw bit error rate (BER) of the communications system as a function of modulation, coding and SNR.

Not as well understood but important to the overall system performance and capacity are the other impairments listed in Table 1. As the broadband system designs extend the bandwidths up to hundreds of megahertz, move to higher-order modulations, and apply powerful error correction schemes, they push the performance close to the digital boundary between low error rates and unacceptably high error rates, making it critical to accurately simulate all impairments realistically in the channel to ensure an optimal design.

Accurate results may require hours of computing time, even on the fastest processors, leading to a limitation in the number of cases simulated and the combination of impairments tried.

Design simulation and test tools

Several approaches are available to the satellite system designers to aid in the design process. Computer modeling and simulation tools provide the designers insights into overall performance, with models that take into account a number of channel impairments. These are used to develop the basic designs and to estimate performance. This software runs on desktop computers and advanced workstations. Accurate results may require hours of computing time, even on the fastest processors, leading to a limitation in the number of cases simulated and the combination of impairments tried. There is also the chance that the models do not accurately reflect the real world.

At the other extreme, experimental satellites have been built and launched to test new communications technology and concepts in the real world using real hardware and software. These satellites include ACT, Artemis, Kopernikus, N-Star, Superbird, and Italsat F1. Satellites are costly to produce, but have been valuable test beds in refining technology and defining techniques for the broadband satellites designs of today. While satellites are the pinnacles of real-world test beds, their performance is fixed by design, leaving little flexibility to change any specification on demand. As such, impairments cannot easily be modified to test the effects on overall system performance.

Satellite channel simulators combine the best of both worlds in test and simulation, offering the advantages of accuracy and real time. One example is the Celerity CS80000 Broadband Channel Simulator (BCS) family from Aeroflex, shown in Figure 2. These simulators are laboratory instruments that create real-world channels with impairments in a controlled, accurate and repeatable manner. Because these are real-time systems with broadband RF inputs and outputs, actual hardware terminals can be used during testing. This real-time testing allows a much larger number of test cases to be run than with the software models, so that more exhaustive testing is achieved. The features are:

- Stable, repeatable simulation with defined controllable impairments.
- Real-time and full-bandwidth channels that support real hardware and fast test times.
- Worst-case scenario simulations with any combination of impairments.
- Lab instrument that minimizes costly drive testing or real satellite test times.

Other development test tools include Broadband Signal Generators (BSG) and Broadband Signal Analyzers (BSA). While not channel simulators, these instruments generate realistic satellite signals and environments with impairments as well as record and analyze signal channel performance.

Broadband channel simulators: The basics

Figure 3 shows the major functions of an ideal broadband channel simulator. These functions closely emulate the actual channel

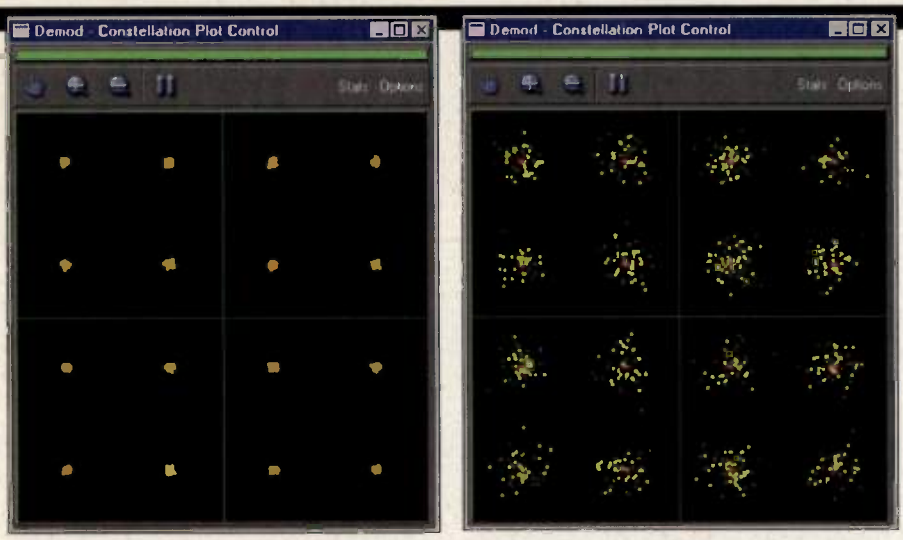

Figure 4. Constellation of 16 QAM signal with 50 dB SNR and with 20 dB SNR.

and impairments, plus offer the speed, accuracy, and flexibility to quickly try many combinations of settings.

Channel simulators must have *sufficient bandwidth and dynamic range* to meet the channel requirement. Without intentionally added impairments, they should faithfully pass the signals with minimum degradation. For many satellite systems, the minimum dynamic range for the simulator would be about 40 dB. For satellite communications systems that use advanced modulations, higher dynamic ranges may be required. Testing with Aeroflex channel simulators have shown that modulations up to 64 QAM can be successfully used with 40 dB dynamic ranges with minimal degradation.

Testing with Aeroflex channel simulators have shown that modulations up to 64 QAM can be successfully used with 40 dB dynamic ranges with minimal degradation.

Channel delay is also important. Long delays are a key part of the satellite channel. For geosynchronous satellites, the 22,300-mile average distance between the earth terminal and the satellite causes a 120-millisecond delay in uplink or downlink signals. If one hop (up and back) or two hop links are to be modeled, delays up to 600 milliseconds are needed. This is important when testing IP schemes to ensure that they work with the long satellite delays, especially in bent pipe configurations. Standard terrestrial IPs that use carrier sense multiple-access/collision detection (CSMA/CD) will not work if the delays are too long to resolve collisions, and must be modified and tested for GEO satellite use.

Dynamic delay and dynamic Doppler are required to simulate satellite or ground motion. Geosynchronous satellites are not stationary but are positioned with a slight offset from the equatorial plane (inclination), so their relative motion as viewed from the earth is a long figure eight moving mostly north and south over a 24-hour period. This motion causes delay and Doppler shifts in the signal. The delay change can be as much as 1 millisecond for a 2° inclination. The Doppler frequency shift depends on the carrier frequency, but is approximately 1 kHz with a Ku-band carrier for a 2° inclination. Low earth orbit (LEO) and medium earth orbit (MEO) satellites exhibit far greater dynamic delay and Doppler, as they move across the sky from horizon to horizon with each pass.

Iridium LEO satellites operate at altitudes of about 485 miles, orbiting the earth every 100 minutes. Delay changes of 2 milliseconds to more than 5 milliseconds occur when in view, with corresponding high Doppler frequency shifts. Dynamic delay is important in a channel simulator because the delay change actually shifts the symbol timing of digital signals, forcing the terrestrial terminal's receiver-demodulator to buffer signals in memory to operate with a fixed bit rate output network. Too much delay change can cause these buffers to overflow or underflow, with a resultant dropping of data. A key requirement in a channel simulator is the ability to change delay dynamically without glitching the phase of the signal. Tools for creating and controlling the delay and

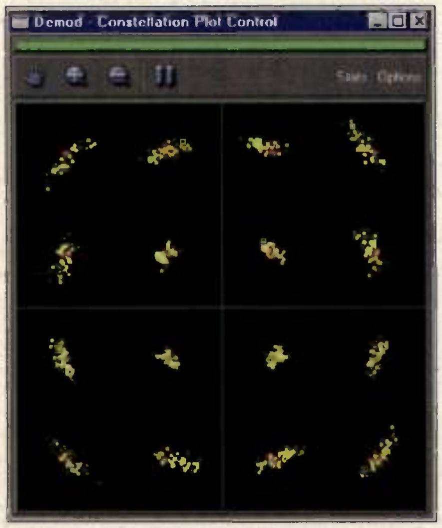

Figure 5. Phase noise effects.

Figure 6. Passband amplitude and phase variation effects on 16QAM signal (without equalization).

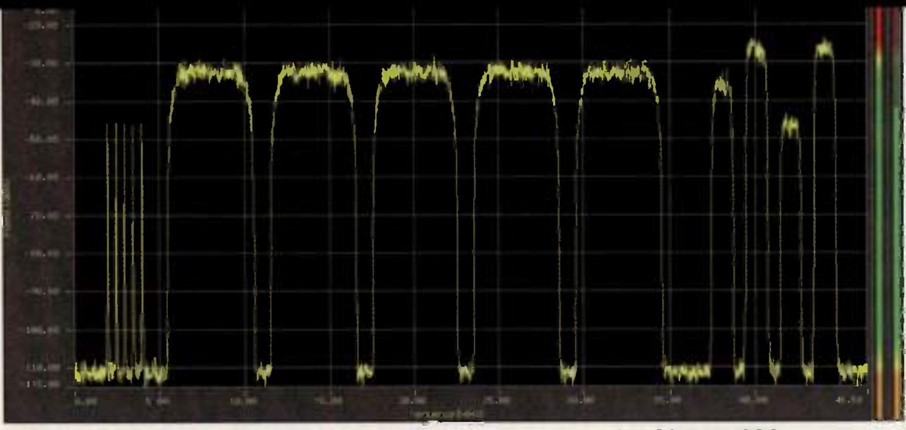

Figure 7. Realistic channel loading and interference simulation using CS25040 BSG.

Doppler scenario files over a 24-hour period are also important.

Two synchronous channels should be available in the channel simulator, with independent dynamic delay and Doppler controls. Many communications links operate in duplex mode, where the two terminals are interacting. Two simulator channels allow the flow of data in both directions to support this mode.

Simulators need to have statistically accurate additive white Gaussian noise (AWGN) generators that cover the channel bandwidth with precise control of noise power densities.

Broadband channel simulators: Advanced capabilities with realistic impairments

Now that the simulator basics are covered, the number of impairments available and the realism and control of the impairments prove the simulator's real value to the developer. The ideal simulator should simulate as many of the impairments shown in Table 1 as possible. Thermal noise is a good starting point, as its effects on system performance are well understood. But other factors such as I/Q imbalance, phase noise, phase and amplitude distortion, gain linearity, channel loading, multipath, and interference further degrade the real-world system performance, and must be considered to optimize designs and avoid performance pitfalls.

Thermal noise has already been discussed as to the impact it has in a communications channel. Simulators need to have statistically accurate additive white Gaussian noise (AWGN) generators that cover the channel bandwidth with precise control of noise power densities. This is summed into the channel, and allows accurate SNRs to be created and BERs to be measured. Figure 4 shows a constellation plot for an ideal 16 QAM signal operating at 50 Msymbols per second and 50 dB SNR, plus a constellation with the same signal with a 20 dB SNR. The noise causes the tight cluster of points designating a symbol to spread out, increasing the probability that a decision error will be made.

Phase noise, like thermal noise, is unavoidable in communications systems and occurs whenever frequency devices are used. Phase noise is seen as sidebands around a carrier and is often measured in 1 Hz to 1 MHz offsets. The higher RF carriers, faster time bases, and wider loop bandwidths used for the broadband systems generate higher phase noise with continuous and spurious phase noise distributions. Figure 5 shows the constellation plot of the 16 QAM with phase noise starting at -40 dBc/Hz 100 Hz from carrier and tailing off to -90 dBc/Hz 1 MHz from carrier. Simulators, such as the CS80072, with precision control of phase noise distributions allow communications links to have the communication channel's phase noise specification tested and validated.

With broadband RF components, it is difficult to maintain passband amplitude flatness and phase linearity over the signal bandwidth. *Deviations in flatness and phase linearity* (also represented as group delay distortion) will degrade the complex broadband signals. Equalization is almost always applied as part of the demodulation process to minimize these effects. The equalizer designs of broadband systems can be confirmed using the channel simulator. Figure 6 shows the effects of 2 dB of passband ripple on the constellation of the 16 QAM signal, and the effects of 10° of passband phase deviation on the constellation.

Broadband satellites support multiple broadband signals in the channel, separated either in time (TDM), frequency (FDM), or both. *Gain transfer distortions* that include AM/AM and AM/PM distortion can degrade the system performance by causing multiple-carrier intermodulation and signal distortion. Traveling wave tube amplifiers (TWTA), a common choice for the high-power downlink transmit amplifier in satellites, can have significant gain transfer distortion even with linearizers. This distortion is the main reason why traditional satellite modulations are limited to QPSK or OQPSK. Channel simulators that simulate AM/AM and AM/PM would allow development and testing of new modulation techniques in advanced communications channels.

Simulators that inject *broadband channel loading and interference*, such as that shown in Figure 7, can uncover intermodulation problems as well as test for receiver selectivity and adjacent channel interference.

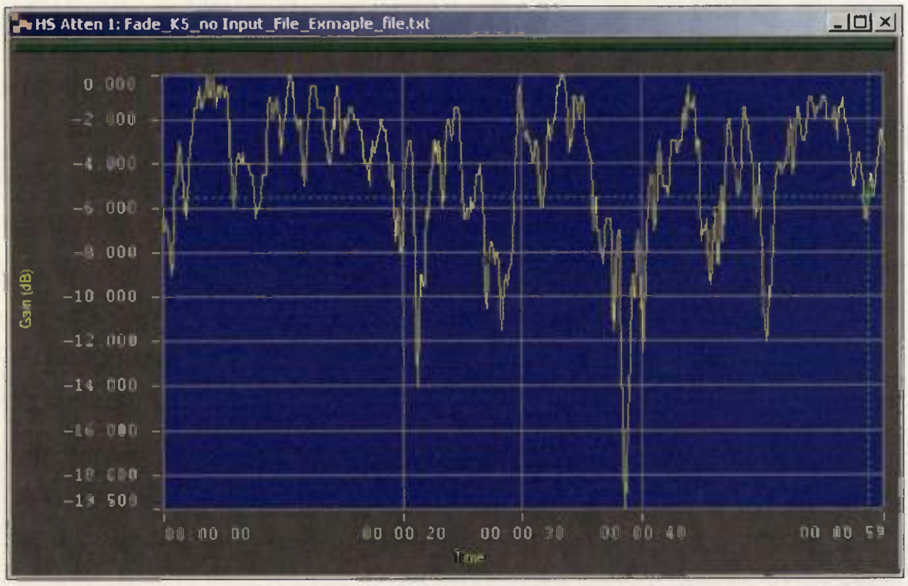

Figure 8. Received power over 60 seconds with a Ricean simulator module.

Simulators can also add co-channel interference that falls on top of the signal of interest to simulate cross polarization leakage. The multiple signal environment used for channel loading shown in Figure 7 was created using Aeroflex's CS25040 Broadband Signal and Environment Generator, which can generate up to 160 MHz bandwidth environments.

Ricean multipath effects result when the direct signal path and a number of reflected paths, with the proper simulated signal impairments, are combined at the receiver. This causes fluctuations in the received signal power (and phase and passband flatness depending on the severity). Higher frequency bands and directional antennas tend to limit these effects in most non-mobile broadband systems, but some multipath must be anticipated depending on the earth terminal placement. Simulators with accurate Ricean distributions and controls for the amount of reflected signal power (K) and fluctuation rate are useful in evaluating the effects of Ricean fading on system performance. In addition to the Ricean modules, high-speed, glitch-free attenuators can simulate rain fade and $1/R^2$ loss accurately over long scenarios. Figure 8 is the plot of received signal power over a 60-second period from a Ricean simulator module with a K = 5 setting.

Finally, *I/Q imbalance* needs to be considered in broadband communications systems design. Broadband modulators and demodulators are commonly designed with baseband I and Q paths. As signal bandwidths increase in broadband systems, it becomes increasingly difficult to maintain I/Q balance across the entire signal bandwidth, resulting in I/Q gain, I/Q phase, and I/Q DC offset imbalances. I/Q modulators and demodulators are part of the terrestrial terminals and regenerative satellite payloads. If severe enough, I/Q imbalance results in errors in the demodulated data and a higher BER. While simulators are useful for simulating these effects, other tools like broadband signal and environment generators can generate complex signals with adjustable precision I/Q imbalance for testing.

Conclusion

The effects of thermal noise, I/Q imbalance, phase noise, phase and amplitude distortion, gain linearity, channel loading, multipath, and interference must all be considered to optimize the system-wide design and avoid performance pitfalls. Challenges abound, but with the proper simulation and real-time real-world test tools and careful attention to these impairments, designs can be proven, performance optimized, and problems minimized prior to system production. RFD

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Broadband monolithic S-band class-E power amplifier design

This efficient broadband monolithic class-E power amplifier operates at S-band and employs a 0.3 μm x 1000 μm pHEMT device. The amplifier's measured performance shows a peak power-added efficiency (PAE) of 90% and a peak output power of greater than 23 dBm at 3.25 GHz.

By Reza Tayrani

Highly efficient microwave and RF power amplifiers are required for many commercial as well as defense system applications. These include wireless LANs, cell phones and telecommunication systems as well as advanced airborne active phased array radar systems. The choice of technology, design methodology and manufacturing cycle time are major cost contributors in these systems. A simple and accurate design can be successful for realization of switching mode, class-E high-efficiency power amplifiers in the S band.

The design of class-E amplifiers is based on using a series or parallel resonant load network. The current and voltage time-waveforms at the active device output terminal are optimized in such a way as to minimize the DC power dissipation within. The active device acts as a switch, driven by the RF input signal to on and off conditions. The ideal AC load lines for switching transistors (class D, E, F)

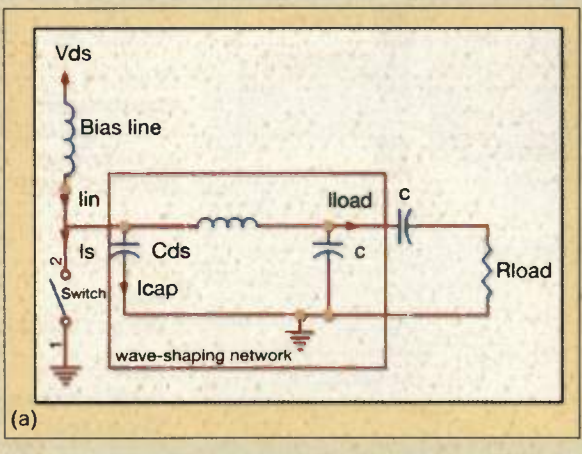
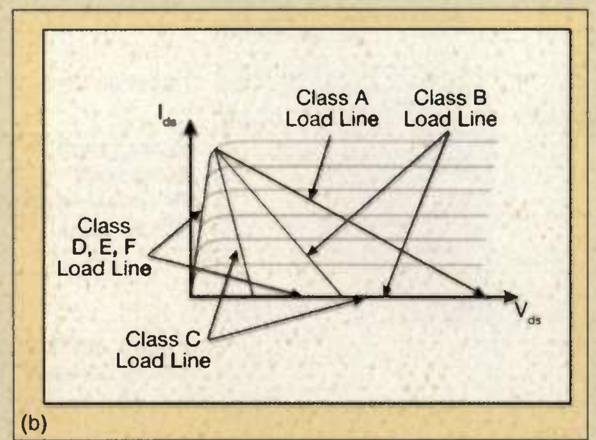


Figure 1. (a) Ideal switching amplifier circuit (shunt load). (b) Ideal transistor load lines for several classes of operation..



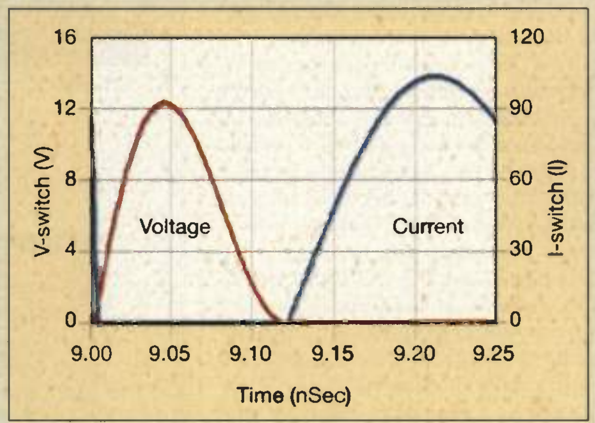


Figure 2. Switch voltage and current waveforms for circuit (1a).

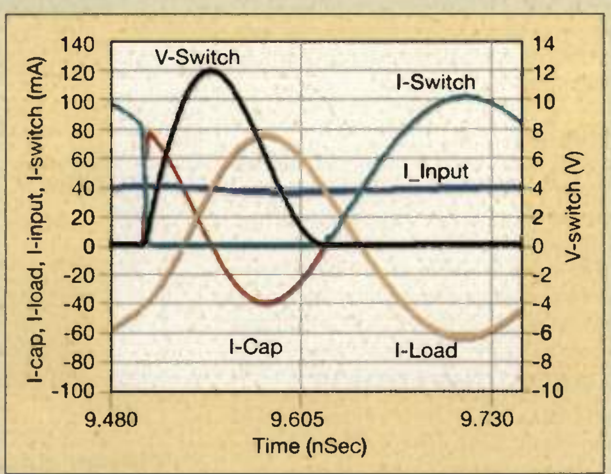


Figure 3. Current-voltage waveforms for circuit (1a).

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ZX10-2-42	1.9-4.2	23	0.2	34.95
ZX10-2-71	2.95-7.1	23	0.25	34.95
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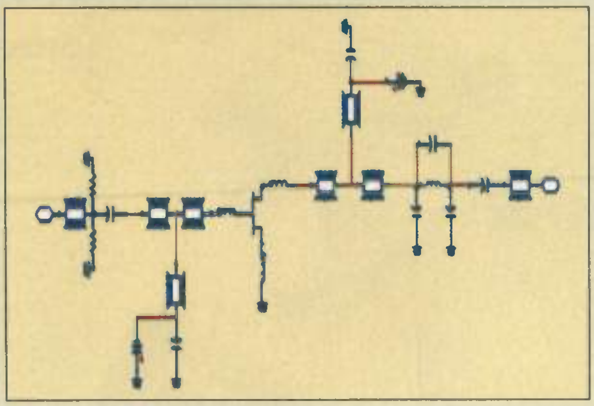

Figure 4. S-band Class-E amplifier circuit.

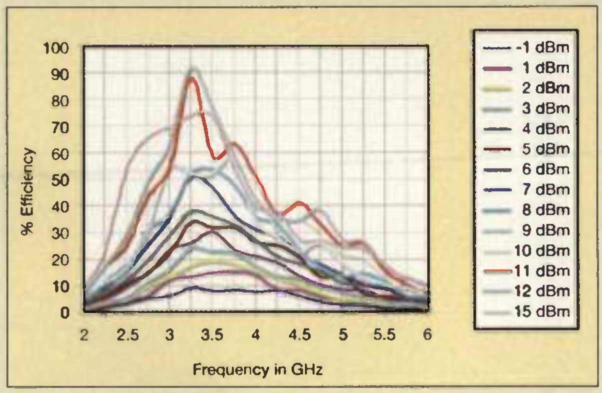

Figure 7. Measured PAE vs. frequency bias (Vds=5V, Vgs=-1V).

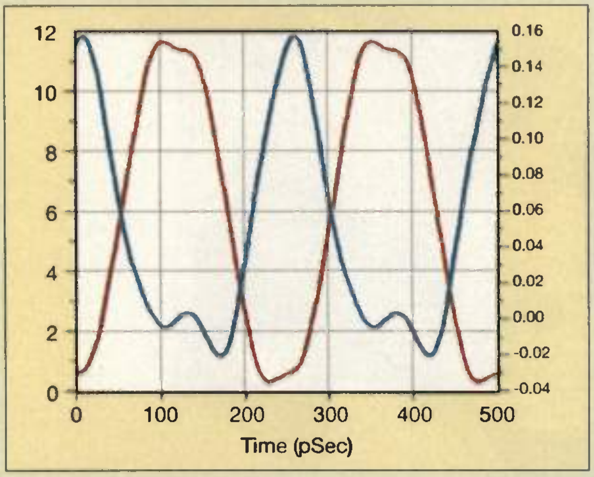

Figure 5. Simulated waveforms of the class-E amplifier.

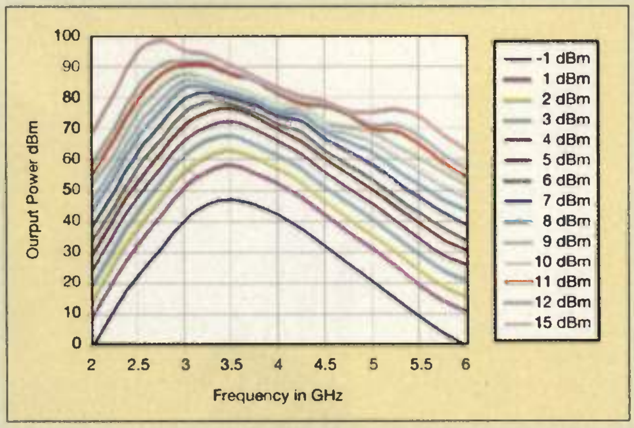

Figure 8. Measured output power, vs. frequency bias (Vds=5V, Vgs=-1V).

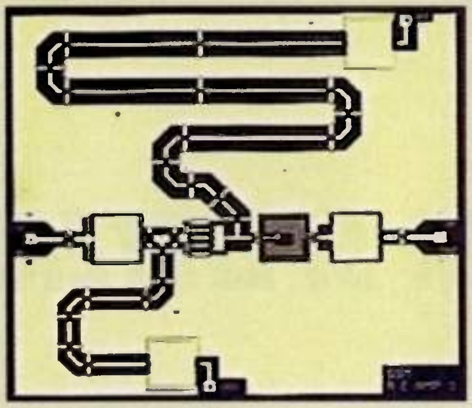

Figure 6. MMIC amplifier chip.

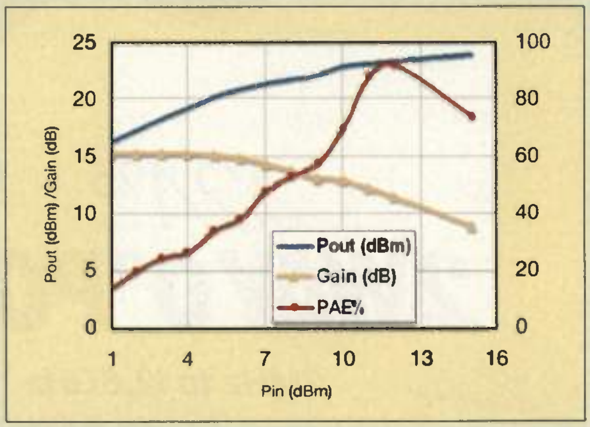

Figure 9. Measured output power, PAE, and gain vs. input power at 3.25 GHz.

are shown in Figure 1(b). It can be seen that the operating point moves along the Vds and Idss axes; i.e. the device is either off (in the saturated region) or on (in the linear region). Under this ideal switching operation, the output voltage and current waveforms at the device output terminal do not simultaneously exist and, therefore, the dissipated energy within the device is zero, leading to 100 percent theoretical power conversion efficiency.

With the advent of active-device performance, non-linear modeling and monolithic circuit technology in the last few years, significant progress has been made toward the development of high-efficiency RF and microwave components. In the case of class-E high efficiency power amplifiers, the circuit designers have pushed the useful operating frequency of these circuits to ever-higher frequencies [1-3].

With this design, we have made a special effort to optimize the amplifier's lumped-element load network in a coplanar waveguide (CPW) environment for the highest PAE attainable while maintaining a minimum of 23 dBm output power. All aspects of non-linear device modeling and circuit simulations, including time domain analysis, harmonic balance (HB) analysis and large signal stability analysis, were performed using Agilent ICCAP and ADS simulators respectively [4].

Design methodology

The detailed analysis and derivation of the ideal load networks for class-E amplifiers are fully discussed elsewhere [1]. Knowing the device drain to source capacitance (C_{ds}) and the drain voltage (V_{ds}), an approximate maximum frequency (f_{max}) for class-E operation can be obtained. Similarly, assuming a load

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resistance of 50 Ω, approximate values for the circuit elements (L and C) of the shunt load network shown in Figure 1(a) can be obtained by using the following expressions:

$$f_{max} = \frac{I_{max}}{56.5 C_{ds} V_{ds}},$$

$$L = \frac{0.28}{\omega^2 C_{ds}} \left[\sin\theta + \cos\theta_0 \sqrt{\frac{\omega_s C_{ds} R}{k_0 \cos\theta}} - 1 \right]$$

$$C = \frac{1}{\omega_s R} \sqrt{\frac{\omega_s C_{ds} R}{k_0 \cos\theta_0 - 1}}$$

where $k_0=0.28$, $\theta_0=49.05°$, $\omega=2\pi f_{max}$.

Having obtained the starting values for the load network, a time-domain simulation was performed to optimize the current and voltage waveforms at appropriate terminals of the ideal class-E circuit shown in Figure 1(a).

Figure 2 shows the simulation results for the circuit after optimization of the load network. The voltage waveform across the switch rises slowly at switch-off and falls to zero at the end of the half-cycle. It also has a zero rate of change at the end of half-cycle, thereby ensuring a "soft" turn-on condition. The voltage across the switch when it is off is defined by the integral of the current flowing through C_{ds}. The phase shift introduced by the LC circuit adjusts the point at which the current is diverted from the switch to the capacitor C_{ds}. Therefore, to ensure class-E operation, it is essential that the integral of capacitor current over the half-cycle is zero and that the capacitance current has dropped to zero by the end of the half-cycle. Figure 3 shows that the optimized current and voltage waveforms comply with the aforementioned criteria for the class-E amplifiers.

The majority of the existing non-linear pHEMT models available in the commercial circuit simulators are not suitable for modeling class-E circuits. For accurate modeling of switching mode amplifiers, the model should have the following important properties:

- bias dependency of drain-to-source $C_{ds}(V_{ds},V_{gs})$ and gate-to-drain C_{gd} (V_{ds},V_{gs}) capacitances.
- bias dependency of input channel resistance R_i (V_{ds},V_{gs}).
- bias dependency of output channel resistance $R_{ds}(V_{ds},V_{gs})$.
- a two current generator dispersion model for accurate simulation of R_{ds}.

Any non-linear models that model the dispersive behavior of the output resistance by a simple-series resistor-capacitor network, connected in parallel to the standard output network, should be used with care. In such a case, the loading effect of the series resistor-capacitor network on the output resistance should be removed.

After careful observation of the available non-linear models, we decided on the Eesof GaAs HEMT (EEHEMT) model [1] as a suitable choice for the non-linear simulation of class-E amplifiers. The most distinguishing features of this model for class-E are the ability to model R_{ds}(Vds, Vgs) and its dispersion effect, as well as the bias dependency of the device capacitance.

The design objective was to develop a highly efficient class-E monolithic amplifier operating over 3-5 GHz using a 0.3 μm x 1000 μm pHEMT device. The design process starts by generating the large signal S-parameters of the device over the desired RF input drive and frequency band, while the device stability is assured by conventional circuit techniques. The next stage is to design the input-matching network for the amplifier by providing a conjugate match to the large signal S11 over the frequency band of interest. Figure 4 shows the final circuit of the CPW monolithic microwave IC (MMIC) amplifier.

Figure 5 depicts the simulated voltage and current waveforms at the pHEMT output terminals. The waveforms confirm the switching-mode behavior of the pHEMT, a condition that is necessary for class-E operation of the amplifier.

Measured performance

The completed MMIC amplifier is shown in Figure 6. A primitive layout was used in this first iteration to ensure the accuracy of the complex load. Figure 7 depicts the measured amplifier PAE for different RF input drive levels. PAE of greater than 70% over 3.0-3.7 GHz is obtained for 15.0 dbm input power drive, and a peak PAE of more than 90% is obtained at around 3.25 GHz when the amplifier is driven by only 12.0 dbm of input power.

Likewise, Figure 8 shows the measured amplifier output power for different values of RF input drive levels (-1-12 dBm) over 2-6 GHz. As it can be seen, a broadband output power is obtained indicating the broadband capability of class-E operation. At 3.25 GHz, the output power is more than 23.0 dBm for an input drive level of 12.0 dMm. Figure 9 highlights the measured output power, PAE, and gain vs. input power at 3.25 GHz. A maximum PAE of 92%, and an output power of greater than 23 dBm is obtained at P_{in}=12 dBm. RFD

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ABOUT THE AUTHORS

Reza Tayrani received his B.Sc., M.Sc. and Ph.D. degrees in electrical engineering from Kent University, Canterbury, England, in 1974, 1977 and 1985, respectively. He is currently an engineering fellow at Raytheon Microwave Center, Space and Airborne Systems, El Segundo, Calif., engaged in the research and development of GaAs and SiGe MMICs and their related devices. Tayrani has designed and developed many MMICs based on MESFETs, HEMTs, pHEMTs, and HBTs for microwave and millimeter-wave applications. His current areas of interest are high-efficiency switching mode monolithic power amplifiers, advanced SiGe MMICs, broadband sampling circuits and miniature switched filters. Tayrani has published more than 46 technical papers and holds six patents. He can be reached at rtayrani@raytheon.com.

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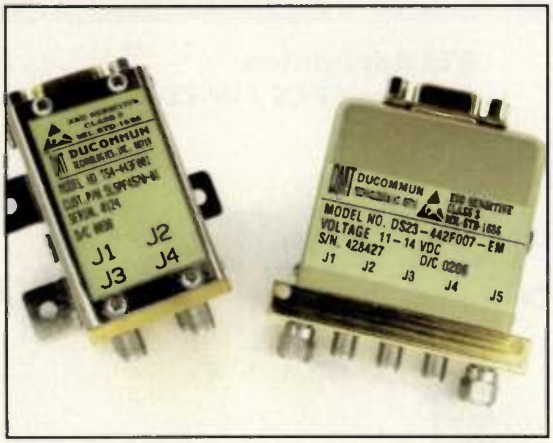

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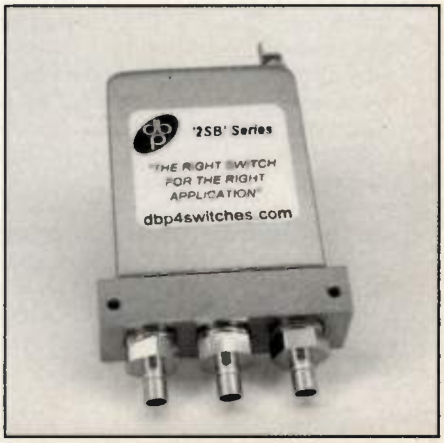


Effective IM2 estimation for two-tone and WCDMA modulated blockers in zero-IF

Direct-conversion receiver architecture is currently the choice for the radio receiver section in 3G WCDMA handsets. It facilitates the complete integration of the radio section on chip, resulting in a lower cost and smaller radio. The IIP_2 requirements of a direct-conversion or zero-IF receiver, in the presence of uplink and downlink WCDMA modulated blockers, are presented.

By Walid Y. Ali-Ahmad

As third-generation (3G) wireless networks are currently expanding in Japan (IMT-2000), in Europe (UMTS) and in the United States (CDMA 2000), the need for low-cost, low power consumption, and low form factor user equipment (UE) is becoming important for the commercial development of 3G mobile handsets. The direct-conversion receiver architecture with the proper use of silicon process, circuit design techniques and architecture implementation represents a promising system solution for high integration platforms for 3G handsets. A fully integrated zero-IF receiver solution for 3G radios (Figure 1) is commercially available, and the receiver second-order input intercept point (IIP_2) requirement is a key specification for the direct-conversion receiver solution.

As seen in Figure 1, direct-conversion or zero-IF receiver architecture enables the pathway for a full on-chip integration of the receiver as the signal is directly demodulated to baseband I and Q signals. In a 3G WCDMA full-duplex (FDD) operation mode, only an external duplexer is needed for separation between RX and TX sections. Furthermore, the post low-noise amplifier (LNA) RF filter is needed in a FDD radio to reject out-of-band blockers and transmitter leakage at demodulator input due to limited finite duplexer TX-RX isolation. In a zero-IF receiver IC, channel selectivity is achieved at baseband by on-chip low-pass filters. Following the channel filtering, I/Q signals at baseband are amplified by variable gain amplifiers (VGAs) before they get digitized in the analog baseband section of the radio modem IC. Design considerations for direct-conversion receivers have been studied thoroughly [1, 2].

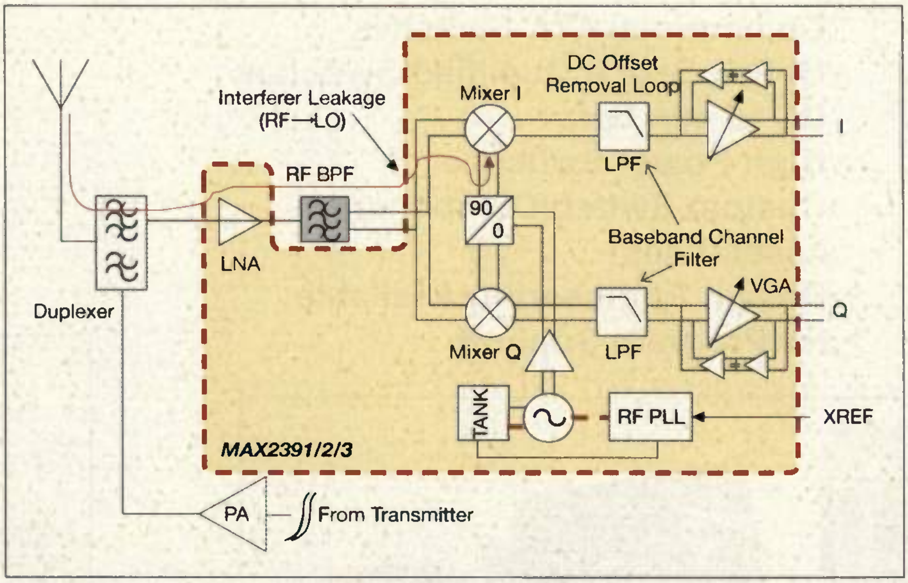


Figure 1. Direct-conversion receiver IC for 3GPP FDD handset radio.

Second-order distortion effects

In a zero-IF receiver, second-order intermodulation products (IM2) have been shown to present a problematic source of interference [1], and care must be taken to minimize the level of these products in the receiver's baseband channel. In a zero-IF receiver, the front-end second-order nonlinearity demodulates the AM components of an amplitude-modulated blocker down to baseband. Because these second-order IM2 products consist of the squared version of the blocker envelope, the bandwidth of these undesirable spectral components at baseband can be up to twice the bandwidth of the blocker's amplitude envelope. Depending on the desired signal modulation bandwidth at baseband, the IM2 products will contribute partially or fully to the degradation of the overall receiver's jamming margin.

The IM2 distortion products are those that occur in the downconverter section of a zero-IF receiver. This is due to the fact that the low-frequency IM2 products in the LNA are normally filtered out by AC coupling or bandpass filtering between the LNA and the mixer blocks. Many mechanisms are responsible for the generation of IM2 products in a zero-IF receiver [3]. However, two main IM2 generation mechanisms are important:

- *RF self-mixing:* It is due to the non-perfect hard-switching I-V characteristic of the commutating stage in a zero-IF receiver mixer and due to the RF signal leaking into the LO port because of parasitic coupling.

The non-perfect hard-switching happens in a mixer when it is driven with low LO powers, and hence, it behaves more like a linear multiplier. As a result, in the presence of an RF to LO leakage component at the LO port (Figure.1), the zero-IF mixer's output contains a signal that is proportional to both the square of the input signal and the RF-to-LO coupling factor. So second-order IM2 products are generated at baseband. This is detrimental to receiver performance when the RF signal leaking to the LO port is a strong blocker.

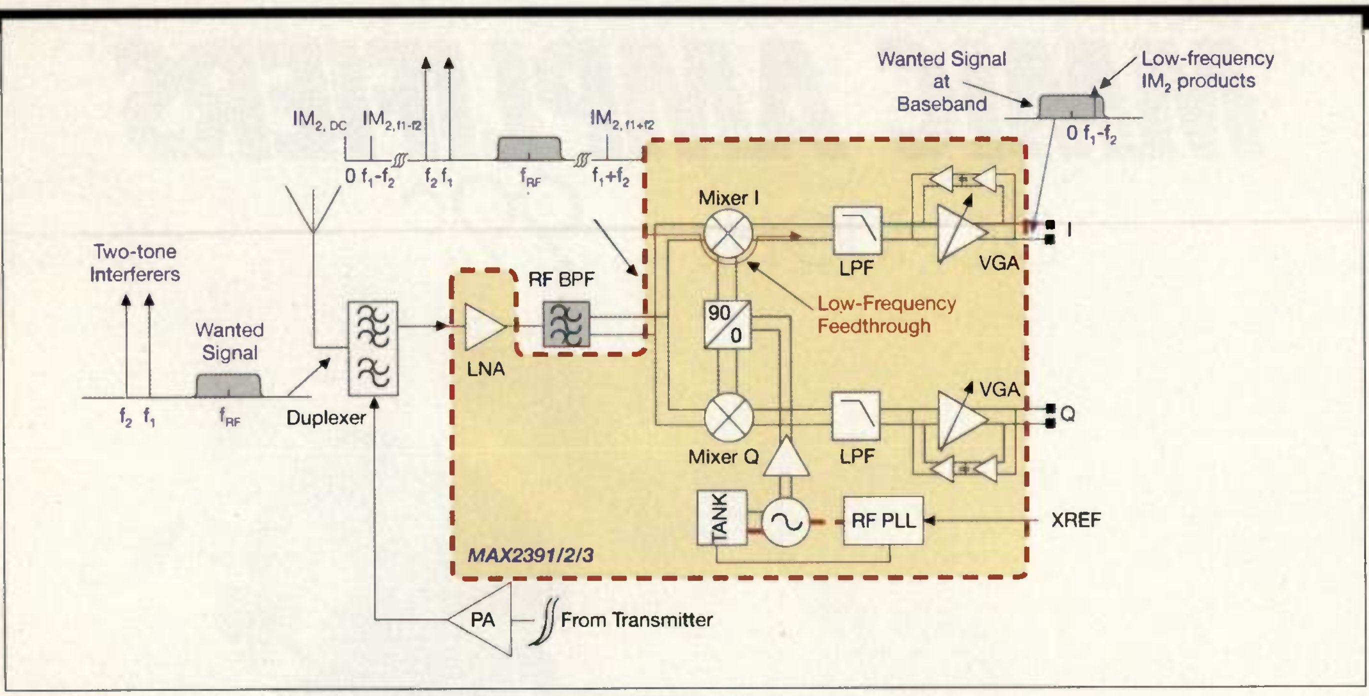


Figure 2. Second-order intermodulation distortion due to two-tone blocker in zero-IF receiver.

■ *Downconverter RF stage second-order non-linearity and LO stage switching-pairs mismatches*: On the introduction of a strong continuous wave (CW) or modulated blocker at the I/Q mixer's inputs in a zero-IF receiver, the second-order non-linearity in the active devices of the mixer transconductor or RF stage will generate low-frequency IM2 products. These products along with the desired RF signal and the blocker will be part of the transconductor stage output currents. In a perfectly balanced mixer with perfectly matched devices in the switching pairs or LO stage and perfectly matched mixer loads, the equivalent differential IM2 products are translated to high frequencies and the equivalent common-mode IM2 products are canceled out at the mixer differential output. However, in reality, the mismatches that exist in the LO stage devices in addition to the deviation of the LO duty cycle from 50% result in a direct low-frequency leakage gain that is presented to the low-frequency IM2 products. As a result, these products get translated to I/Q mixers baseband outputs

It is important to note that in the points discussed above, we assume that the downconverter section in a zero-IF receiver is the main limiting block in IM2 products suppression. This is true if the baseband stages following the I/Q mixers have high common mode suppression (> 60dB).

IIP_2 Derivation

The weakly non-linear characteristics of a receiver front-end can be presented as (Eq. 1):

$$V_o(t) = a_1 \cdot V_i(t) + a_2 \cdot V_i(t)^2 + a_3 \cdot V_i(t)^3 + \cdots$$

To express the IIP_2 based on two-tone derivation, the input signal to the receiver as shown in Figure 2 is expressed as $V_i = A\cdot\cos(\omega_1 t)+\cos(\omega_2 t)$, with a total two-tone power equal to A^2/R. The second-order distortion products at the receiver front-end are derived as: (Eq. 2)

$$a_2 \cdot V_i(t)^2$$
$$= a_2 \cdot A^2 \cdot [1+\cos((\omega_1-\omega_2)t)+\cos((\omega_1+\omega_2)t)$$
$$+(\cos(2\omega_1 t)/2)+(\cos(2\omega_2 t)/2)]$$

The resultant output IM2 products at (f_1+f_2) and (f_1-f_2), including the resulting DC offset, are expressed as (Eq. 3):

$$a_2 \cdot A^2 \cdot [1+\cos((\omega_1-\omega_2)t)+\cos((\omega_1+\omega_2)t)]$$

The total power in the output IM2 products presented in Equation 3, referred to system impedance R, is calculated as (Eq. 4):

$$|a_2|^2 \cdot A^4 \cdot \left(\frac{1}{R}+\frac{1}{2R}+\frac{1}{2R}\right) = 2\cdot|a_2|^2\cdot\frac{A^4}{R}$$

By definition, at the IIP_2 power level, the total input signal power is equated to the total power in the output IM2 products (Eq. 4) after being referred to the input by dividing by the gain factor, $|a_1|^2$. As a result, we can write that (Eq. 5):

$$A_{iip2}^2/R = 2\cdot\left|\frac{a_2}{a_1}\right|^2\cdot\frac{A_{iip2}^4}{R} \Rightarrow IIP_2$$
$$= IIP_2^2 \Big/ \left(\left|\frac{a_1}{a_2}\right|^2\cdot\frac{1}{2R}\right) \Rightarrow IIP_2 = \left|\frac{a_1}{a_2}\right|^2\cdot\frac{1}{2R}$$

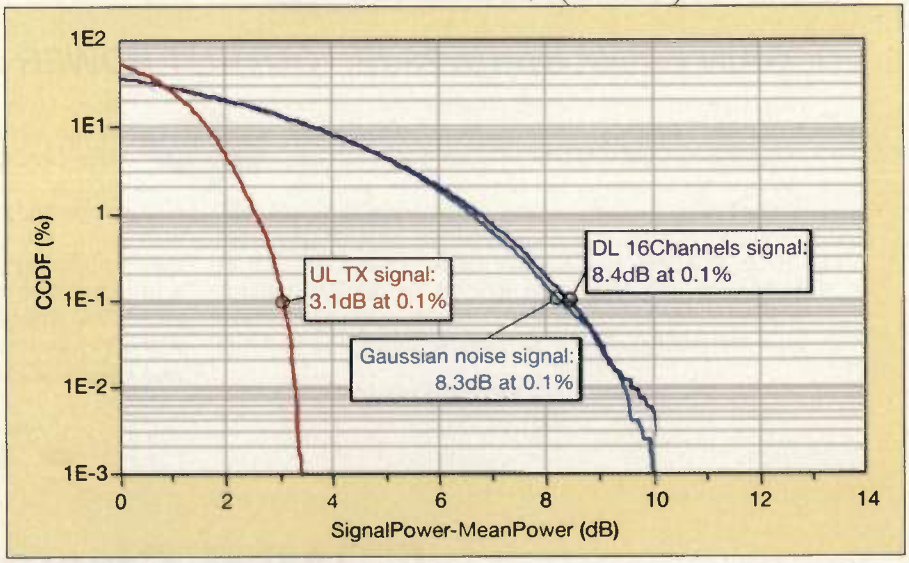


Figure 3. CCDFs of UL reference channel and DL 16-channel blocker.

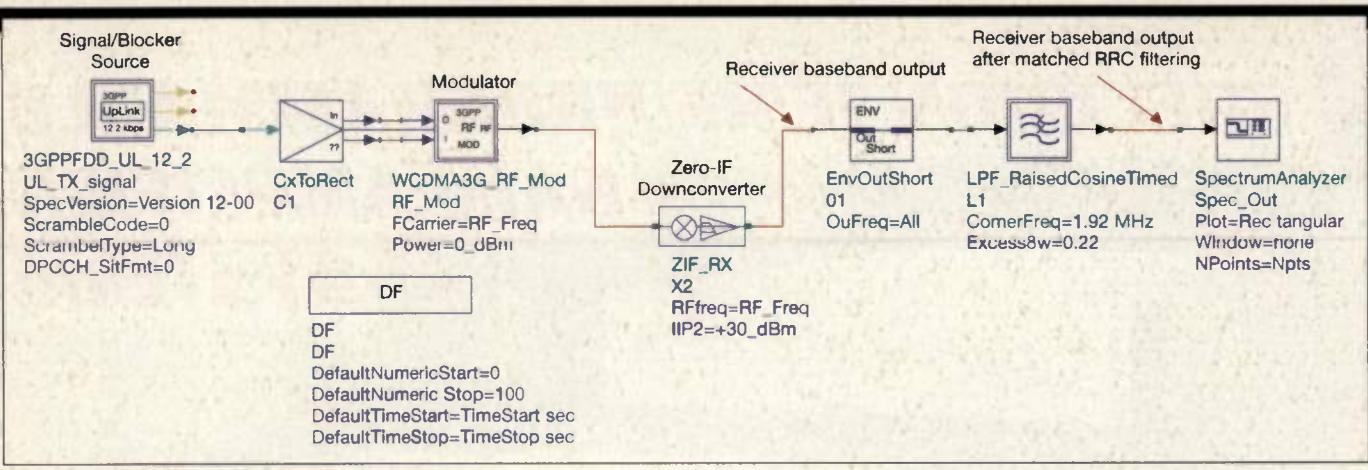


Figure 4. ADS template for IM2 products estimation.

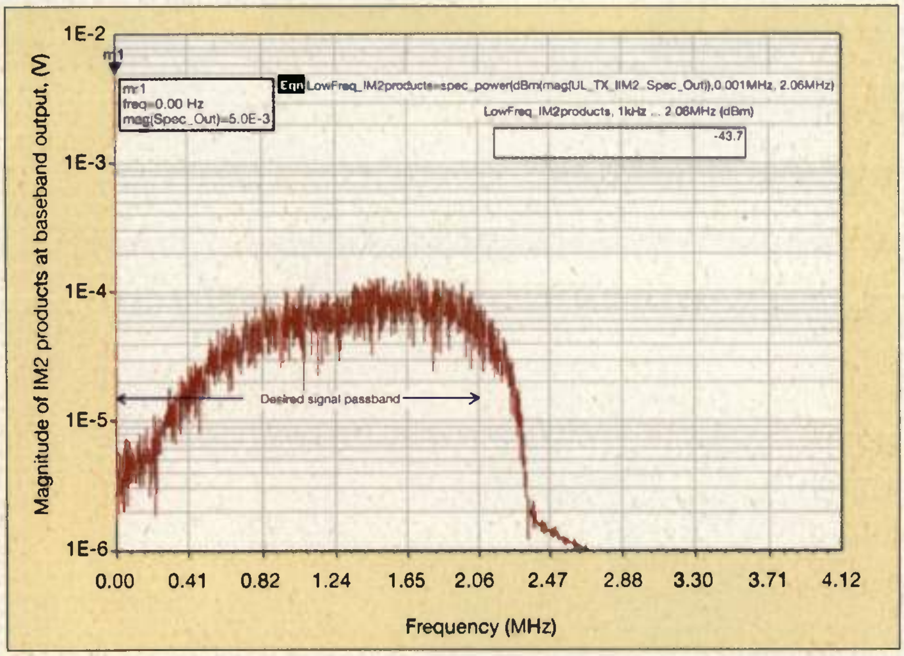


Figure 5. Simulated RRC-filtered IM2 products at zero-IF receiver output due to UL TX blocker.

The total power level of the IM_2 products (Equation 4) referred to the receiver input, based on a total two-tone input power equal to $P_{2T}=A^2/R$, can be expressed as (Eq. 6):

$$P_{IIM2} = 2\cdot\left|\frac{a_2}{a_1}\right|^2 \cdot \frac{A^4}{R} = \frac{P_{2T}^2}{IIP_2} \Rightarrow P_{IIM2}(dBm)$$
$$= 2\cdot P_{2T}(dBm) - IIP_2(dBm)$$

It is important to note that in Equation 4, the resulting IM2 products total power level is composed of 50% (-3dB) IM2 product at DC, 25% (-6dB) IM2 product at f_1-f_2, and 25% (-6dB) IM2 product at f_1+f_2. Therefore, the power level of the IM2 product at f_1-f_2 can be derived from equations (4) and (6) as (Eq. 7):

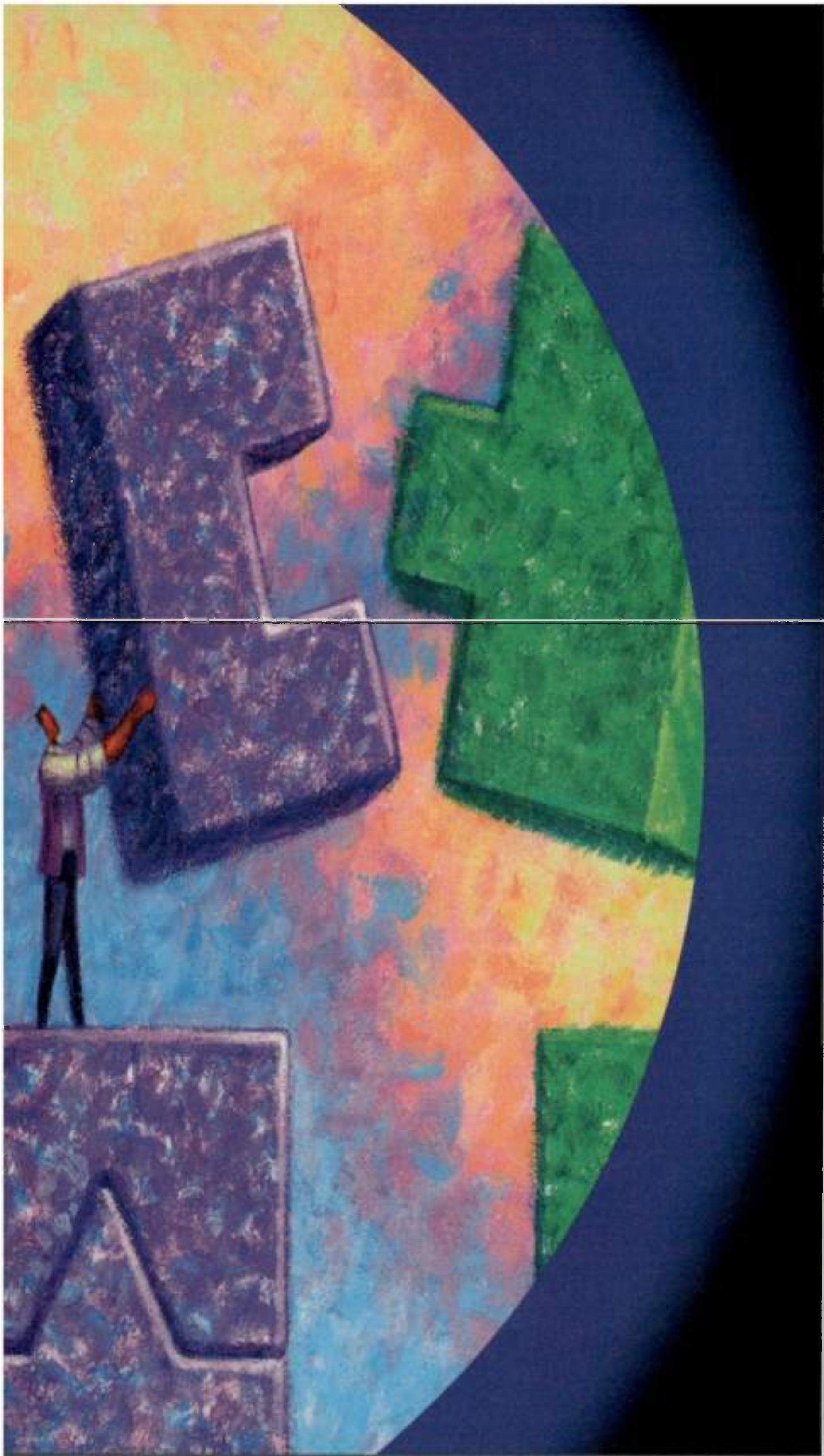
$$P_{IIM2,(f1-f2)}(dBm)$$
$$= 2\cdot P_{2T} - IIP_2 - 6dB \Rightarrow P_{IIM2,(f1-f2)}(dBm)$$
$$= 2\cdot P_{1T}(dBm) - IIP_2(dBm)$$

where power level per tone (P_{1T} at f_1 or f_2) is 50% of the total two-tone power, $P_{1T}(dBm) = P_{2T}(dBm) - 3dB$.

Effective low-frequency IM2 products

In a 3GPP WCDMA radio, the worst-case interferers at receiver input are not two-tone type but wideband, digitally modulated type blockers. Hence, it is important to estimate the effective low-frequency IM2 products based on a modulated blocker to derive the required receiver IIP_2 for a certain desired bit error rate (BER) performance. Therefore, it is necessary to understand the nature of the modulated blocker, specifically its non-constant envelope since it gets stripped off the RF blocker in the front-end second-order non-linearity and gets translated to baseband, including a squared version of the envelope. The two major modulated blockers in a 3GPP WCDMA receiver are presented in 3G standard test cases 7.3.1 and 7.6.1 [4]. The first test case, 7.3.1, specifies the minimum required sensitivity for BER<10^{-3} while the transmitted uplink signal (UL) is at maximum power level (+24dBm) at antenna. The second test case, 7.6.1, specifies the minimum required receiver signal level at antenna connector for BER<10^{-3} in the presence of a modulated downlink (DL) -44dBm blocker at 15 MHz offset from the desired signal, while the transmitted UL power at antenna is +20 dBm.

The UL reference measurement channel (12.2 kbps) structure, which represents the transmitted UL signal at the antenna of a 3G WCDMA handset, is described in table A.1 of the 3GPP standard document [4]. It consists of a dedicated physical data channel (DPDCH) and of a dedicated physical control channel (DPCCH). In the radio modem section, both DPDCH and DPCCH channels are spread to 3.84 Mcps, scaled to appropriate power ratio (DPCCH/DPDCH = -5.46 dB), HPSK scrambled, and filtered by a 1.92 MHz root-raised-cosine (RRC) filter with roll-off factor a = 0.22 [5]. On the other hand, the forward-channel modulated blocker at 15 MHz offset from the desired channel consists of the common channels needed for tests as specified in Table C.7 and 16 dedicated data channels as specified in Table C.6 in [4]. The signal is QPSK encoded, spread to 3.84 Mcps, complex scrambled, and filtered by a RRC filter similar to that used for UL signal [5]. Both signals have a -3 dB bandwidth equal to 3.84 MHz at RF, and 99 percent of the total signal power is within a bandwidth of 4.12 MHz (-6 dB BW). To understand the nature of the envelope of either the modulated UL TX signal or the modulated DL 16-channel signal—and to estimate the effective IM2 products due to each one of them in a WCDMA Zero-IF receiver—it is important to study first the power statistics of each signal, which is represented by the complementary cumulative distribution function (CCDF). The CCDF provides the peak-average power ratio (PAR) of the signal vs. probability. Figure 3 shows ADS [6] simulated CCDFs of the UL trans-



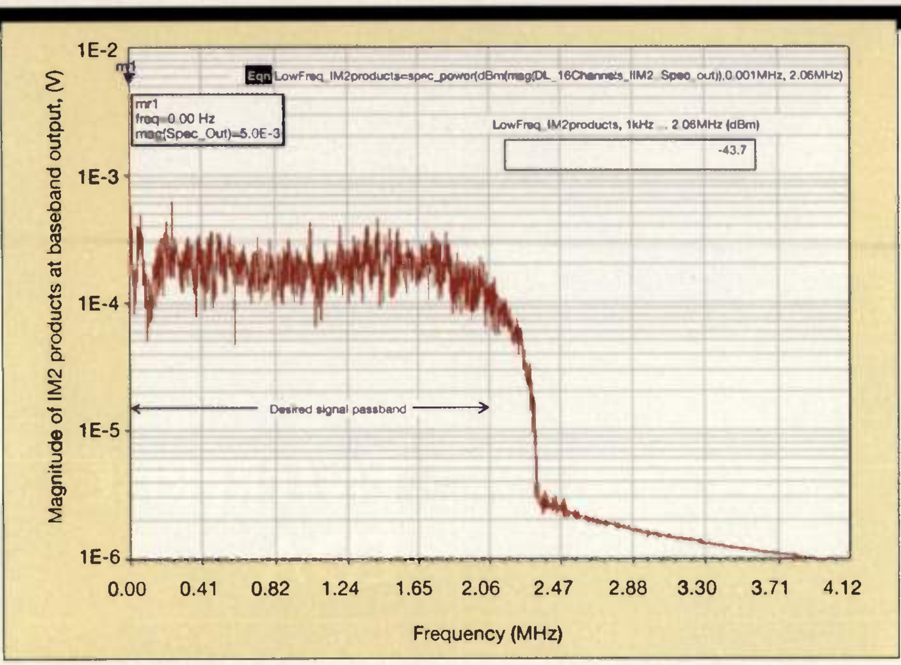


Figure 6. Simulated RRC-filtered IM2 products at zero-IF receiver output due to DL 16-channel blocker.

mitted signal and the DL 16-channel signal compared to the CCDF of a Gaussian noise signal.

Figure 3 shows the PAR at 0.1 percent probability of the UL reference channel, based on one transmitted DPDCH, is equal to 3.1 dB. On the other hand, the DL blocker at the 15 MHz offset, which contains 16 dedicated traffic channels, has an 8.4 dB PAR at 0.1%, which is almost equal to that of a Gaussian noise signal. It will be shown later that the effective low-frequency IM2 products estimation will differ between the two standard test cases because of this PAR discrepancy between the two different blockers.

An ADS IM2 simulation template was created to investigate the IM2 products due to a modulated blocker at the input of a WCDMA zero-IF receiver (Figure 4); the IM2 products were filtered by an RRC filter, which is matched to the base station transmitter RRC filter. The resulting low-frequency IM2 products were measured in simulation in the 0 Hz to 2.06 MHz desired signal bandwidth at baseband, which is half the signal's 99%power BW at RF.

In Figures 5 and 6, simulated IM2 products' magnitude spectrums at the baseband output of a zero-IF downconverter after matched RRC filtering are presented for the WCDMA UL reference measurement channel (12.2kbps) and for the WCDMA DL 16-channels blocker, respectively. In the ADS template and for simulation purposes only, we used a modulated blocker power equal to 0 dBm and a zero-IF downconverter IIP_2 equal to +30 dBm. The resulting low-frequency IM2 products' power level for a 0 dBm WCDMA UL TX signal, integrated over the desired signal passband of 1 kHz ... 2.06 MHz, is equal to -43.7 dBm. The DC offset due to second-order non-linearity is equal to 5 mV, which is equivalent to -33 dBm into 50 W (Figure 5). On the other hand, the resulting IM2 products' power level for a 0 dBm WCDMA DL 16-channel blocker, integrated over the desired signal passband of 1 kHz ... 2.06 MHz, is equal to -33.1 dBm. The resulting DC offset due to second-order non-linearity is also equal to 5 mV (Figure 6). Going back to Equation 6 and assuming a two-tone blocker total power level of 0 dBm at the zero-IF downconverter input, the total IM2 products' power level, referred to receiver input, is calculated as $P_{IIM2}(dBm)=2\cdot P_{2T}(dBm)-IIP2(dBm)=-30dBm$, of which -33 dBm is the resulting DC offset level and -36 dBm is the power level of the IM2 product at f_1-f_2, based on Equations 4 and 7, respectively. We can conclude that the integrated low-frequency IM2 products' power level over the 1 kHz to 2.06 MHz band due to a 0 dBm UL TX blocker is 7.7 dB lower than the low-frequency, f_1-f_2, IM2 product power level due to a two-tone blocker with 0 dBm equivalent power level. Similarly, the equivalent total low frequency IM2 product power level due to a 0 dBm DL 16-channel blocker is 2.9 dB higher than the low-frequency, f_1-f_2, IM2 product power level due to a 0 dBm two-tone blocker. The total effective IM2 product power levels based on the previous results are summarized in the following equations:

For the UL reference channel or TX blocker case (Eq. 8),

$$
\begin{aligned}
&P_{IIM2,UL\_TX}(dBm)\\
&=2\cdot P_{UL\_TX}(dBm)-IIP_2(dBm)-13.7dB\\
&=2\cdot P_{1T}(dBm)-IIP_2(dBm)-7.7dB
\end{aligned}
$$

For the DL 16-channel blocker case (Eq. 9),

$$
\begin{aligned}
&P_{IIM2,DL\_16Ch}(dBm)\\
&=2\cdot P_{DL\_16Ch}(dBm)-IIP_2(dBm)-3.1dB\\
&=2\cdot P_{1T}(dBm)-IIP_2(dBm)+2.9dB
\end{aligned}
$$

In Equations 8 and 9, the power level per tone (P_{1T} at f_1 or f_2) is 50% of the total power level (P_{2T}) of a two-tone blocker having the same power level as that of the modulated blocker,

$$P_{1T}(dBm)=P_{2T}(dBm)-3dB=P_{UL\_TX/DL\_16Ch}(dBm)-3dB$$

It is important to note that the -13.7 dB reduction factor relative to the total IM2 products' level estimate in Equation 8 is similar to the factor obtained in the results presented in [7]. Furthermore, the results presented by Equations 8 have been verified through lab measurements done on a zero-IF receiver device with the part number shown in Figure. 1. The measured IM2 products at baseband due to UL TX blocker (Figure 7) show similar spectrum characteristics to the simulated IM2 products shown in Figure 5. The measured spectrum components close to DC in Figure 7 are larger than the corresponding simulated components in Figure 5 because of the additional downconverted phase noise close to DC in the actual measured zero-IF receiver.

In the following section, the required minimum IIP_2 for a WCDMA zero-IF receiver for both test cases 7.3.1 and 7.6.1 will be derived based on Equations 8 and 9, respectively. All IIP_2 calculations are done referred to the receiver LNA input.

-3GPP standard test case 7.3.1:

- In FDD mode, the estimated maximum UL TX signal leakage at the LNA input is -24 dBm ($P_{UL\_TX,\ LNA}$ = PA power at duplexer - duplexer_isolation$_{TX\rightarrow RX,\ min.}$ = +26dBm – 50dB = –24 dBm). The worst-case insertion loss (IL) of the duplexer before the LNA is assumed equal to -2 dB. In 3GPP IMT band radio handsets, the TX leakage frequency offset relative to the desired RX signal frequency is 190 MHz.
- It was shown in [8] that for a required traffic channel sensitivity of -117 dBm/3.84 MHz, the required minimum E_b/N_t, after decoding and despreading of the desired traffic channel, is 7 dB. In test case 7.3.1, which specifies the minimum required traffic channel sensitivity for BER<10^{-3}, N_t is assumed to be purely noise (N_o) due to receiver NF. For a chip rate of 3.84 Mcps and a user bit rate of 12.2 kbps, the processing gain is G_p = 10.log(3.84 Mcps/12.2 kbps) = 25 dB. We can calculate that the maximum allowable noise power (P_N) due to receiver NF is P_N = $P_{Sensitivity}$ + G_p - E_b/N_t = –117 dBm + 25 dB – 7 dB = -99 dBm.
- At minimum sensitivity level, it is required

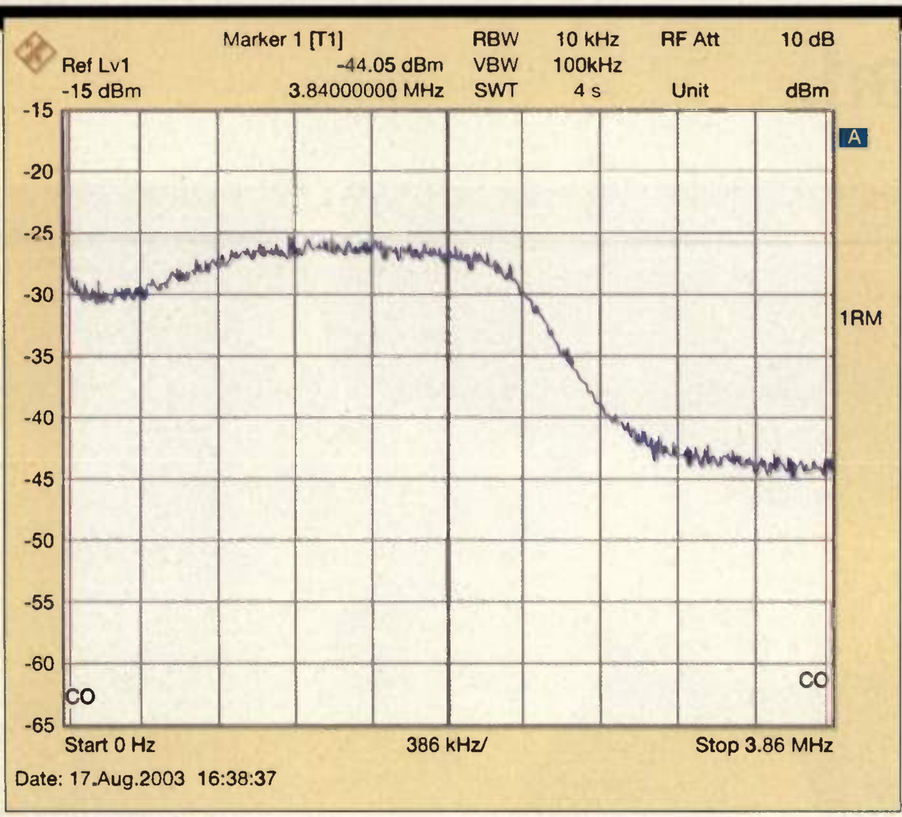


Figure 7. Measured IM2 products, *without RRC filtering*, at zero-IF receiver output due to UL TX blocker.

that the low-frequency IM2 products due to UL TX leakage blocker do not desensitize the receiver. The resulting DC offset due to IIP_2 has no effect since in a WCDMA zero-IF receiver, DC offsets are typically rejected on-chip. If we assume that the total power level of low-frequency IM_2 products needs to be at least 11 dB lower than P_N (maximum of 0.3 dB receiver desensitization), we can estimate the maximum allowable input IM2 due to UL TX leakage blocker, referred to receiver LNA input:

$P_{IIM2,UL\_TX} = P_N - 11dB - IL_{duplexer} \leq -99dBm - 11dB - 2dB = -112dBm.$

■ The receiver $IIP_{2,TX}$ at Tx offset (190 MHz), *referred to receiver LNA input*, is calculated using Equation 8:

$$P_{IIM2,UL\_TX}(dBm) = 2 \cdot P_{UL\_TX,LNA}(dBm) - IIP_{2,TX}(dBm) - 3.7dB$$
$$\Rightarrow IIP_{2,TX}(dBm) \geq +50dBm$$

-3GPP Standard Test Case 7.6.1:

■ In this test case, the desired signal is 3 dB above minimum sensitivity specified in test case 7.3.1. Hence, the maximum allowable noise+interference power level is -96 dBm, which is 3 dB higher than the level calculated in the previous test case. Assuming the same level of receiver noise (-99 dBm), the maximum allowable interference power level is therefore 96 dBm -3 dB = -99 dBm.

■ The total interference power due to the WCDMA DL 16-channel blocker at 15 MHz offset from the desired signal is assumed to be divided mainly among phase noise reciprocal mixing (25% or -6 dB), blocker level at receiver output after on-chip filtering (25% or -6 dB), and low-frequency IM2 products due to this blocker (50% or -3 dB). Hence, we can estimate the maximum allowable input IM2 products' level due to DL blocker, referred to receiver LNA input: $P_{IIM2,DL\_16Ch} = P_N - 3dB - IL_{duplexer} \leq -99dBm - 3dB - 2dB = -104$ dBm. The low-frequency IM2 products due to the UL TX leakage signal have been neglected because the UL TX power in this test has been reduced by 4 dB relative to the level specified in test case 7.3.1.

■ In this test case, the specified modulated blocker level is equal to -44 dBm at the antenna. With -2 dB IL in duplexer, the level of the blocker at LNA input, $P_{DL\_16Ch,LNA}$, is -46 dBm.

■ The receiver $IIP_{2,(15MHz)}$ at 15MHz offset, *referred to receiver LNA input*, is calculated using Equation 9:

$$P_{IIM2,DL\_16Ch}(dBm) = 2 \cdot P_{DL\_16Ch,LNA}(dBm) - IIP_{2,(15MHz)}(dBm) - 3.1dB$$
$$\Rightarrow IIP_{2,(15MHz)}(dBm) \geq +9dBm$$

-3GPP Standard Test Case 7.6.1:

It is important to note that the required zero-IF receiver $IIP_{2,TX}$ at the UL TX frequency offset is much tougher than the required $IIP_{2,(15MHz)}$ at the DL 16-channel blocker frequency offset, when all are referred to LNA input. When translating the $IIP_{2,TX}$ requirement to the I/Q mixers inputs, this will impose the need for the mixers' $IIP_{2,I/Q\_mixer}$ to be larger than +60 dBm. However, this requirement can be relaxed by the use of the post LNA filter, which provides selectivity at the TX leakage offset frequency [9].

Conclusions

This paper presented simulations, calculations, and measurements, which were done to estimate the required zero-IF receiver IIP_2 in the presence of a modulated WCDMA blocker. Depending on the envelope nature of the modulated blocker, it has been shown that the resulting low-frequency IM2 products' level at baseband can be lower or higher than the low-frequency IM2 beat tone level due to an equivalent two-tone blocker. RFD

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CRO2273A	2240 to 2306	0.5 to 4.5	22	0 ± 2	-110	-15	5	20	-10 to 85	<1	<1
CRO2275A	2250 to 2300	0.5 to 4.5	15	1.5 ± 1.5	-114	-10	5	20	-10 to 75	<1	<1
CRO2343A	2310 to 2376	0.5 to 4.5	23	1 ± 2	-110	-10	5	20	-10 to 85	<1	<1
CRO2580A	2560 to 2600	1.0 to 4.5	23	3 ± 3	-111	-15	5	20	-40 to 85	<1	<1
CRO2851A	2851 to 2851	0.5 to 4.5	5	6.25 ± 2.25	-114	-16	5	18	-40 to 85	<0.5	<0.5
CRO2925A	2900 to 2950	0.5 to 4.5	5	5 ± 2	-109	-20	5	22	-40 to 85	<2	<2
CRO3040A	3040 to 3040	0.5 to 4.5	6	7 ± 2	-115	-15	5	19	-40 to 85	<0.5	<0.5
CRO3100A	3070 to 3120	0.5 to 4.5	20	3.5 ± 2.5	-112	-7	5	21	-40 to 85	<1	<1
CRO4260A	4250 to 4270	0.5 to 4.5	10	3.5 ± 3.5	-107	-10	5	21	-40 to 85	<1	<1
CRO6030A	6020 to 6040	0.5 to 4.5	20	3 ± 3	-98	-30	5	22	0 to 70	<3	<1

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Simulation and realization of baseband pulse shaping filter for BPSK modulator

This pulse shaping technique reduces side lobe levels of bi-phase shift keying (BPSK) modulation and spectral spike elimination. Useful for space communications, the technique can be implemented in a practical way. This technique will be used in GEO satellites in the near future.

By D.Venkata Ramana, Surendra Pal and A.P.Shiva Prasad

With the continuing growth of communications and the increasing number of users, frequency bands are becoming more and more congested. To cope with this frequency congestion, many authors have studied methods to increase bandwidth use [1,2].

Significant RF spectrum limiting can be obtained in three ways. Here, the location of filter plays a key role. The various locations include:

- filter after power amplification.
- filter at intermediate frequency (IF).
- filter at baseband.

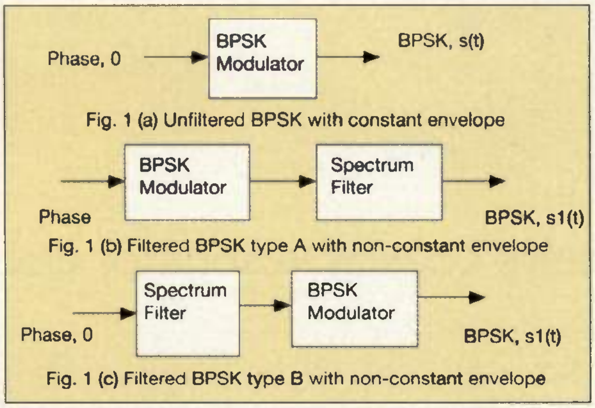

Figure 1. Various filter location configurations for BPSK spectrum .

Post power amplifier (PA) filtering is attractive to spectrum managers because all unwanted emissions, which are outside the filter's passband, are eliminated. Theoretically this filter location provides maximum control over emissions.

For effective spectrum management, the IF filter's bandwidth needs to be adjusted to each mission's maximum telemetry data rate.

However, it would be difficult for post PA filtering to improve RF spectrum use in most space missions. Filters can be either stripline or waveguide bandpass filters, which are generally used in microwave applications. For reasonable insertion losses, such filters are constrained to bandwidths ranging from 1.5% - 2% of the transmitted frequency. It should be noted that the filters that have somewhat lower insertion loss tend to be large and heavy.

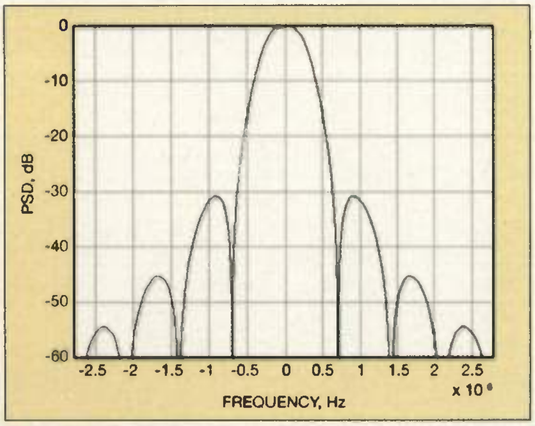

Figure 2. Simulated PSD of BPSK spectrum using new pulse shaping filter.

Filtering at IF is attractive because the filter operates at low power levels and does not reduce transmitted RF power. It is also small and lightweight and does not introduce the spectral spikes inherent in baseband filtering. For effective spectrum management, the IF filter's bandwidth needs to be adjusted to each mission's maximum telemetry data rate.

Baseband filtering is advantageous because the filters operate at low power levels, are lightweight, do not reduce transmitted RF power and are small and simple (lowpass rather than a bandpass). Baseband filtering of phase-modulated signals suffers from the disadvantage of introducing spikes into the RF spectrum [2]. Despite this limitation, baseband filtering is the only practical method to limit the transmitted RF spectrum for the purpose of improving bandwidth efficiency.

Pulse shaping

In general, the MPSK (M'ary phase shift keying) spectrum consists of a main lobe representing the middle of the spectrum and various side lobes located on either side of the main lobe. Shaping the spectrum should satisfy two criteria: The main lobe should be as narrow as possible, and the maximum side lobe level should be as small as possible relative to the main lobe [3].

In recent years, studies have shown that PSK modulation is particularly suited to digital satellite communications. The power spectra of a PSK signal has a $\left(\frac{\sin x}{x}\right)^2$ characteristic that may interfere with adjacent

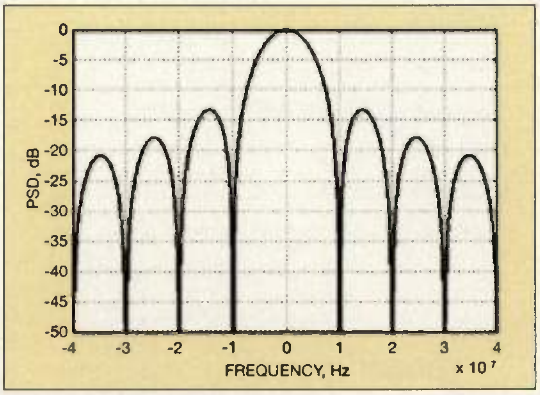

Figure 3. Unfiltered BPSK spectrum.

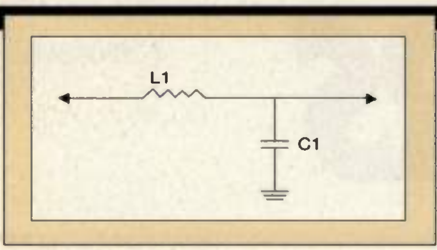

Figure 4. Gaussian filter.

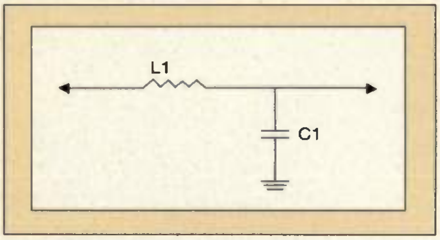

Figure 5. New pulse shaping filter.

channels. To suppress the out-of-band interference, it may be necessary to remove the side lobes by filtering at the transmitter. Here we consider pulse shaping for BPSK spectrum.

The block diagram of the unfiltered BPSK spectrum configuration is shown in Figure 1a. In a similar way, the block diagram of the filtered BPSK configuration is given in Figure 1b. Here, the spectrum filter is placed after the modulator. To realize spectrum shaping, the phase signal goes through a pulse-shaping filter before being modulated as shown in Figure 1c. The change of the position of pulse shaping filters can produce a change of simulation results. Pulse shaping filters are used to narrow bandwidth and improve bandwidth use. However, pulse shaping can introduce distortions and can increase the risk of intersymbol interference (ISI). These distortions make the design of an optimal receiver difficult.

Many designers have tried various pulse-shaping methods [4,5]. Several types of filters such as 5th-order Butterworth, 3rd-order Bessel and square-root-cosine are used. Pre-modulation pulse shaping with different modulation schemes, such as pulse-code modulation (PCM), BPSK, quaternary phase-shift keying (QPSK) and Gaussian filtered minimum shift keying (GMSK) have been studied. In this approach, a simple pre-modulation filter has been employed to achieve low side lobe levels. Here, we considered a Gaussian filter (N=2) and a new pulse shaping filter (N=2) and compared both. In low bit rate applications (500 kbps), pulse-shaped BPSK modulation has been chosen for space communications.

Simulation work

The transfer function of the proposed new pulse-shaping filter is given by

$$H(W) = \frac{1}{1 + [0.7067W(L_1C_1)^{0.5}]^{2N}} \qquad (1)$$

where W= 2pf , p=22/7, N=order of the

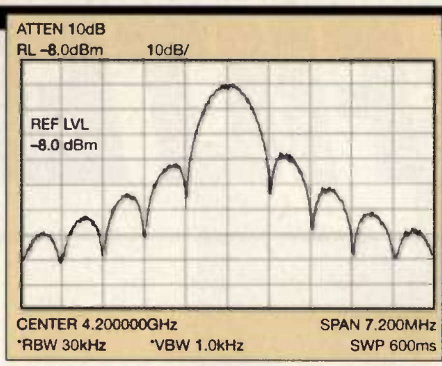

Figure 6. PSD of BPSK spectrum with new pulse shaping filter, BT=0.5.

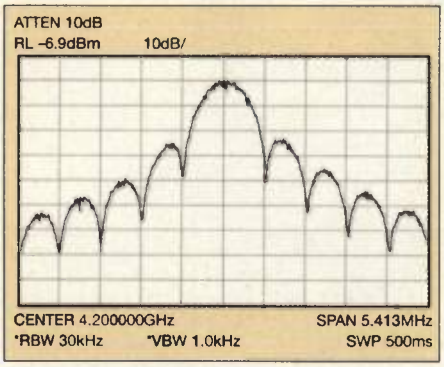

Figure 7. PSD of BPSK spectrum with new pulse shaping filter BT=0.7.

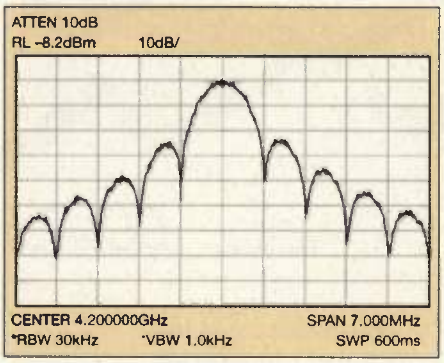

Figure 8. PSD of BPSK spectrum with Gaussian filter with BT=0.5.

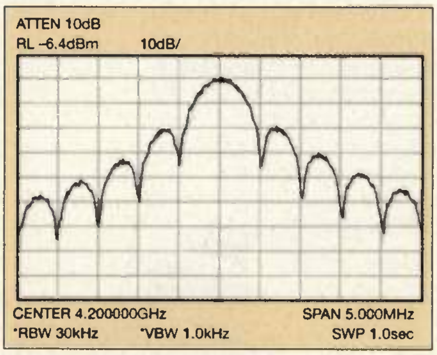

Figure 9. PSD of BPSK spectrum with Gaussian filter with BT=0.7.

filter. The simulated spectrum is shown in Figure 2.

The spectral density of NRZ random data is given by [6]

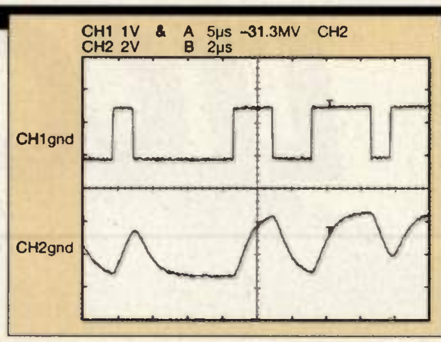

Figure 10. Input data and shaped data for Gaussian filter (BT=0.4).

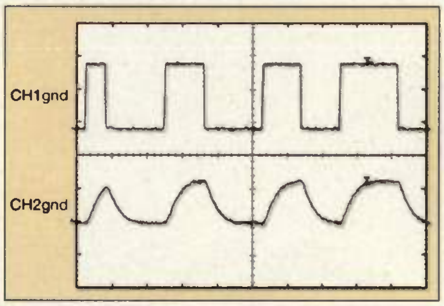

Figure 11. Input data and pulse-shaped input data of new filter.

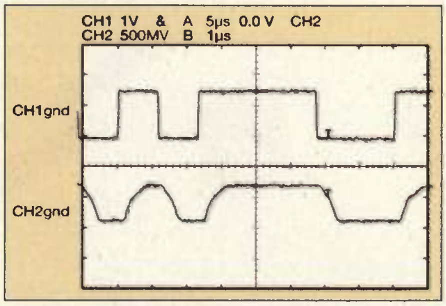

Figure 12. Input data and demodulated data of new pulse shaping filter (BT=0.4).

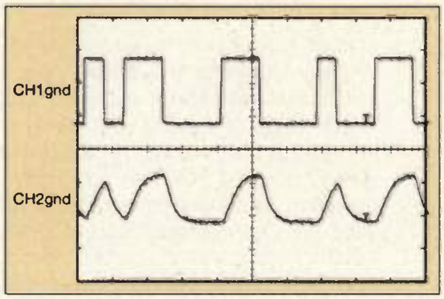

Figure 13. Input data and demodulated data of Gaussian pulse shaping filter (BT=0.4).

$$S(f) = 2\,(T_bA)^2\left[\frac{\sin^2(\pi f T_b)}{(\pi f T_b)^2}\right] \qquad (2)$$

where Tb is the bit period, A is the amplitude of the signal and f is the frequency in Hertz. The modulated spectrum is given by

$$S_{TX}(f) = \frac{1}{2}\,[S(f-f_{RF}) + S(f+f_{RF})] \qquad (3)$$

The PSD for an unfiltered BPSK signal is given by [6]

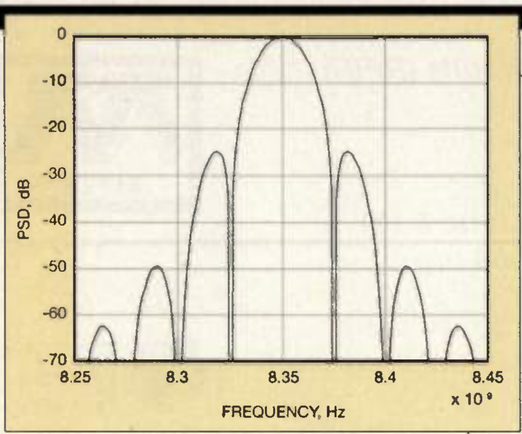

Figure 14. Simulated PSD of proposed window function.

$$S_{TX}(f) = (AT_b)^2\left[\frac{\sin^2[\pi(f-f_{RF})T_b]}{[\pi(f-f_{RF})T_b]^2} + \frac{\sin^2[\pi(f+f_{RF})T_b]}{[\pi(f+f_{RF})T_b]^2}\right] \quad (4)$$

The theoretical power spectral density (PSD) for an unfiltered BPSK signal is shown in Figure 3. Note that the sharp transitions in the time domain lead to a relatively wide power spectral density that rolls off quite slowly. The first null occurs at a frequency equal to the data rate away from the carrier. The amplitude of the first lobe is only 13 dB down from its value at the carrier frequency, and second side lobe level is at 18 dB.

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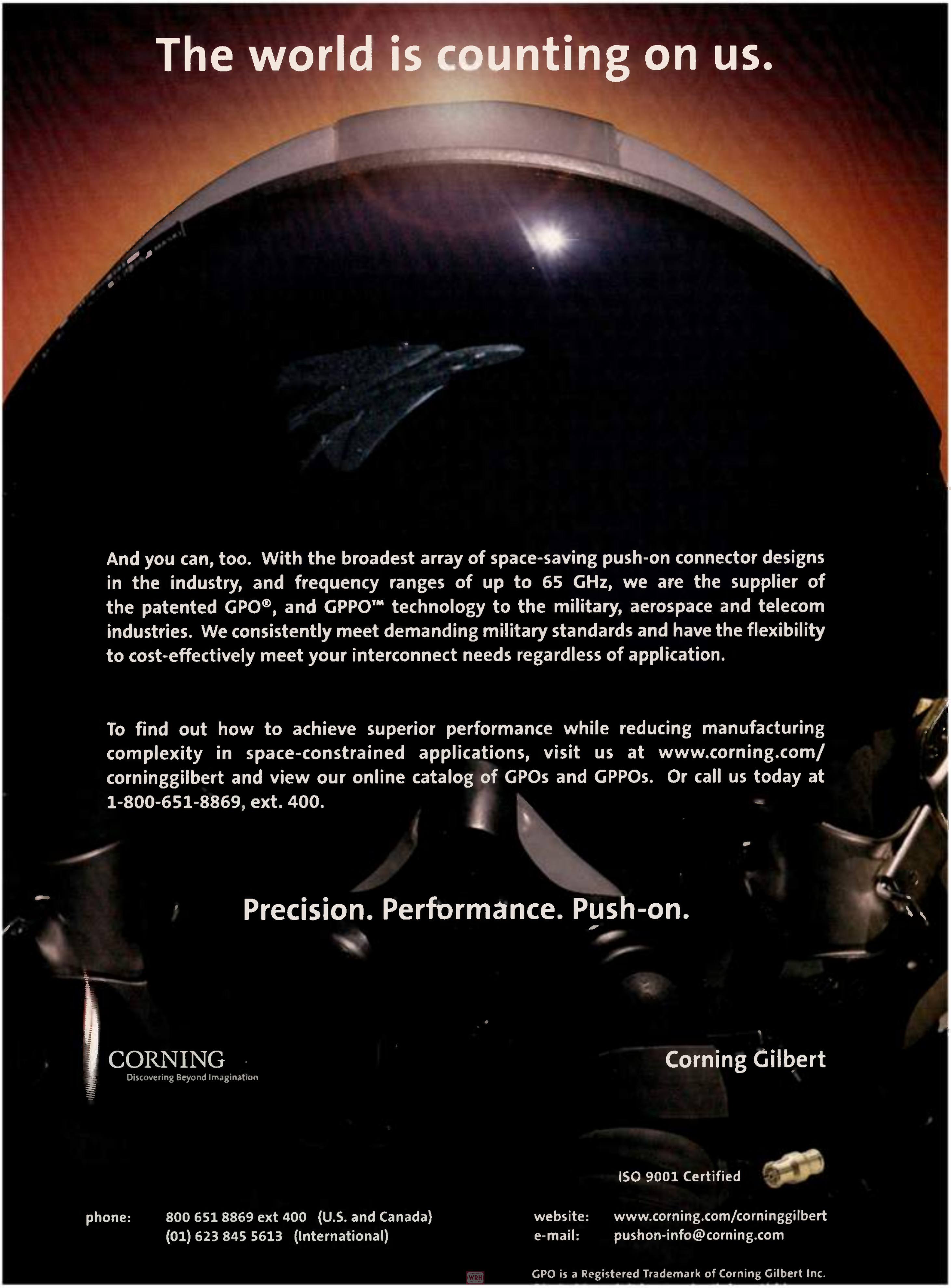
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Experimental work

In this experiment, a M/s Merrimac BPSK modulator unit has been used to study the modulated spectrum using pulse-shaping techniques. Here, we compared a Gaussian filter (N=2) [Figure 4] and a new pulse-shaping filter (N=2) [Figure 5] designed with a cutoff frequency of 350 kHz. The PSD of BPSK spectrum with new pulse shaping is shown in Figures 6 and 7 for BT= 0.5 and 0.7, respectively. Gaussian pulse shaping filter with bandwidth and time product (BT) = 0.5 and 0.7 is shown in Figures 8 and 9, respectively. One can notice from the above figures that the side lobe levels are less in new pulse shaping filter compared to Gaussian pulse shaping filter.

The shaped NRZ data using Gaussian pulse shaped filter are shown in Figure 10, and shaped NRZ data using new pulse shaping filter are shown in Figure 11. The demodulated data are shown in Figure 12 for a new pulse shaping filter and Figure 13 for a Gaussian filter. The demodulated data quality is good for a new filter as can be observed from demodulated plots. It can be clearly seen that the new pulse-shaping filter has shown advantages over the Gaussian filter for N=2.

New window function

After studying several window functions [7] and modifying their parameters successively by several iterations, a new window function was evolved. This window provides low side lobe levels. The simulated PSD of proposed window is shown in Figure 14.

The proposed window function equation in frequency domain and time domain are given by

$$\omega(f)=\frac{\tau_b}{2}\left[\frac{Sin(\pi f\tau_b)}{\pi f\tau_b}\right]^2\left[\frac{1}{1-(f\tau_b)^2}\right] \qquad (6)$$

$$W1\,(t)=\frac{1}{2}\left(1+\frac{t}{T}\right)-\frac{SinW_0t}{4\pi},\ -T<=t<=0$$

$$W2\,(t)=\frac{1}{\ }\left(1-\frac{t}{\ }\right)+\frac{SinW_0t}{\ },\ 0<t<=T \qquad (7)$$

where T is equal to tow.

From Figure 15, notice that the first and second side lobe levels are -25dB and -50dB, respectively. This reduction in side lobe levels helps in reducing the interference with other systems.

Conclusion

Test and simulation results indicate that the side lobe levels are less in new pulse shaping filter compared with a Gaussian filter (N=2). Consequently, the new technique can be applied to future GSAT satellite programs. RFD

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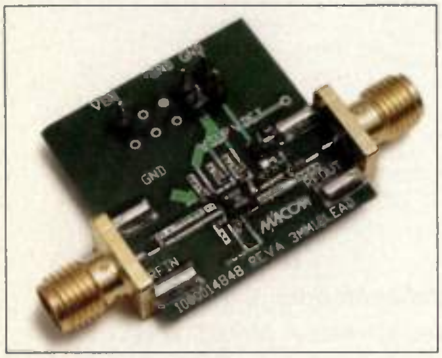
SiGe power amplifiers

M/A-COM has introduced four silicon germanium (SiGe) power amplifiers designed



for "smart PA" gain along the TX/RX (transmit/receive) path of new DECT (Digital European Cordless Telephones), WLANs (wireless local area networks) and 2.4 GHz 802.11 b/g applications. Their features include integrated power detection, standard lead-free 3 mm FQFP-N packaging, single-supply 2.4 V operation, and a three-stage architecture optimized for linearity, efficiency and low-power consumption.

The MAAPSS0075 is an 802.11 b/g-compliant linear power amplifier that delivers 26.5 dBm of output power (P1dB at 3.3 V) with 32 dB of gain. Its typical 400 mA current consumption is 33 percent less than competitive offerings. Like its counterparts, it features an on-chip power detector that precludes the need for building additional feedback circuits for bias trimming. Its micro-amp power shutdown mode dramatically improves battery life. The amplifier is a three-stage device designed for WLAN 2.4 GHz linear applications and is housed in a lead-free 3-mm FQFP-N.

The MAAPSS0081 is optimized for worldwide (WDECT) applications that require linear operation at 2.4 GHz with 26 dBm of saturated output power. Its low power mode drops current consumption from 400 mA at power saturation to 150 mA at 17 dBm. Ramp power control ensures 45% power-added efficiency, stability and high linearity over its entire operating range. It too operates from a single +1.4 V to 4 V supply and is housed in an industry-standard 12-lead 3 mm FQFP-N package.

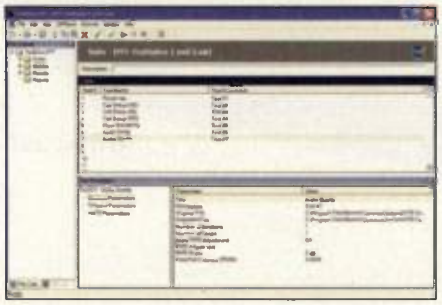
The MAAPSS0066 is characterized and tested as an RF power amplifier for more mainstream ISM and WDECT applications. It delivers 25 dBm power gain, 25 dBm saturated power output and stability across its operational boundaries.

The MAAPSS0082 is tailored for PHS (Personal Handy System) applications between 1.89 GHz and 1.92 GHz. Its features include 23 dBm linear output power, 31 dB power gain, 280 mA current drain at 23 dBm, and lead-free 3 mm 12-lead FQFP-N packaging.

M/A-COM Inc.
(800) 366-2266
www.macom.com

PTT over-the-air test system

Spirent Communications has released its Push To Talk Over-The-Air (PTT-OTA) Test



System. Spirent's PTT-OTA Test System meets the test challenges associated with CDMA networks and handsets that support Voice-over-IP (VoIP) PTT.

The PTT-OTA Test System is flexible and scalable and will enable users to progress from an over-the-air test system to a fully integrated, automated lab-based test solution.

The PTT-OTA system combines Spirent's TestDrive test executive software for overall system control and test management, Spirent's Universal Diagnostic Monitor (UDM) for automated mobile device control and monitoring, and Opticom's OPERATM voice quality software package to create a scalable solution that meets the analysis needs of both lab and field users.

Spirent Communications
(800) 927-2660
www.spirentcom.com

Variable attenuator

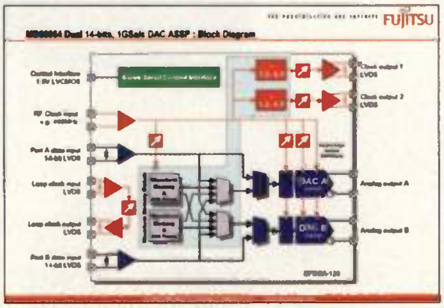
Hittite Microwave Corporation has announced a single-control, 450-2200 MHz voltage variable attenuator for applications in NMT, cellular, PCS & 3G wireless infrastructure.

With up to 48 dB of attenuation range, and +20 dBm of input IP3 throughout its entire attenuation range, the HMC473MS8 is suitable for RF transmit and receive chain applications in virtually all wireless infrastructure applications. The MSOP8 SMT-packaged attenuator requires no external components, and operates from a +3.3 V supply and a single 0 to +3.0 V control voltage.

Samples and evaluation PC boards are available from stock for sampling or sale.

Hittite Microwave Corporation
(978) 250-3343
www.hittite.com

CMOS 14-bit DAC



Targeting next-generation GSM, WCDMA and UMTS-based direct-IF, multicarrier systems, **Fujitsu Microelectronics America Inc.** has unveiled MB86064, a dual 14-bit digital-to-analog converter (DAC) featuring conversion rate of 1 GSamples/s. Previous high was 800 Msamples/s. The new 14-bit 1 Gsamples/s DAC is implemented in 0.18 micron CMOS process.

Instrumental to supporting the increased data rate is Fujitsu's market-leading introduction of double data rate (DDR) LVDS interfaces on high-performance DACs. Combined with its loop-clock facility, this enables cost-effective, realizable solutions when combined with either FPGA or ASIC data

300MHz-12GHz

LTCC MIXERS

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For Commercial, Military, and Industrial Use, Mini-Circuits proudly introduces the MCA1 series of Low Temperature Co-fired Ceramic (LTCC) frequency mixers. Highly reliable, only 0.080" in height, and tough as nails, these patent pending mixers have all circuitry hermetically imbedded inside the ceramic making them temperature stable and impervious to most environmental conditions. The process also gives you high performance repeatability and very low cost. There's a variety of broadband models and LO power levels to choose from, so you can use these mixers in a multitude of designs and applications. And MCA1 mixers are ideal for the COTS program! Just check all the specs on our web site. Then, choose the model that best fits your needs. Our team is ready to handle your requirements with quick off-the-shelf shipments, custom designs, and fast turn-around/high volume production.

Mini-Circuits...we're redefining what VALUE is all about!

New Blue Cell™ LTCC
164 Page Handbook...FREE!

Model	LO Level (dBm)	Freq. Range (MHz)	Conv. Loss (dB)	LO-RF Isol. (dB)	Price $ ea. (Qty. 10)
MCA1-85L	4	2800-8500	6.0	35	9.45
MCA1-12GL	4	38800-12000	6.5	38	11.95
MCA1-24	7	300-2400	6.1	40	5.95
MCA1-42	7	1000-4200	6.1	35	6.95
MCA1-60	7	1600-6000	6.2	30	7.95
MCA1-85	7	2800-8500	5.6	38	8.95
MCA1-12G	7	3800-12000	6.2	38	10.95
MCA1-24LH	10	300-2400	6.5	40	6.45
MCA1-42LH	10	1000-4200	6.0	38	7.45
MCA1-60LH	10	1700-6000	6.3	30	8.45
MCA1-80LH	10	2800-8000	5.9	35	9.95
MCA1-24MH	13	300-2400	6.1	40	6.95
MCA1-42MH	13	1000-4200	6.2	35	7.95
MCA1-60MH	13	1600-6000	6.4	27	8.95
MCA1-80MH	13	2800-8000	5.7	27	10.95
MCA1-80H	17	2800-8000	6.3	34	11.95

Dimensions: (L) 0.30" x (W) 0.250" x (H) 0.080"

Detailed Performance Data & Specs Online at: ***www.minicircuits.com/mixer2.html***

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The Design Engineers Search Engine *Provides ACTUAL Data Instantly From MINI-CIRCUITS At:* ***www.minicircuits.com***

ISO 9001 ISO 14001 CERTIFIED

385 Rev E

See our 244 page [illegible] in EEM ([illegible] Master) generators. Completion of characterization prior to production approval has also led to an improvement in quoted ACLR performance. The figure, when generating 4 UMTS carriers at 276 MHz, has increased to 74 dBc, using a DAC conversion rate of 737 MSamples/s. At 1 Gsamples/s conversion, the power consumption is 750 mW. The device also boasts a host of features ranging from on-chip vector memories to segment shuffling.

The improved 14-bit DAC is priced at $120 each in 1000-unit quantities.
Fujitsu Microelectronics America Inc.
(408) 737-5600
www.fma.fujitsu.com

Linear 2 W amplifier

Stealth Microwave has introduced the SM1925-33, an amplifier designed to meet the needs of low-cost service providers working in the PCS, IMT2000, UMTS, ISM and

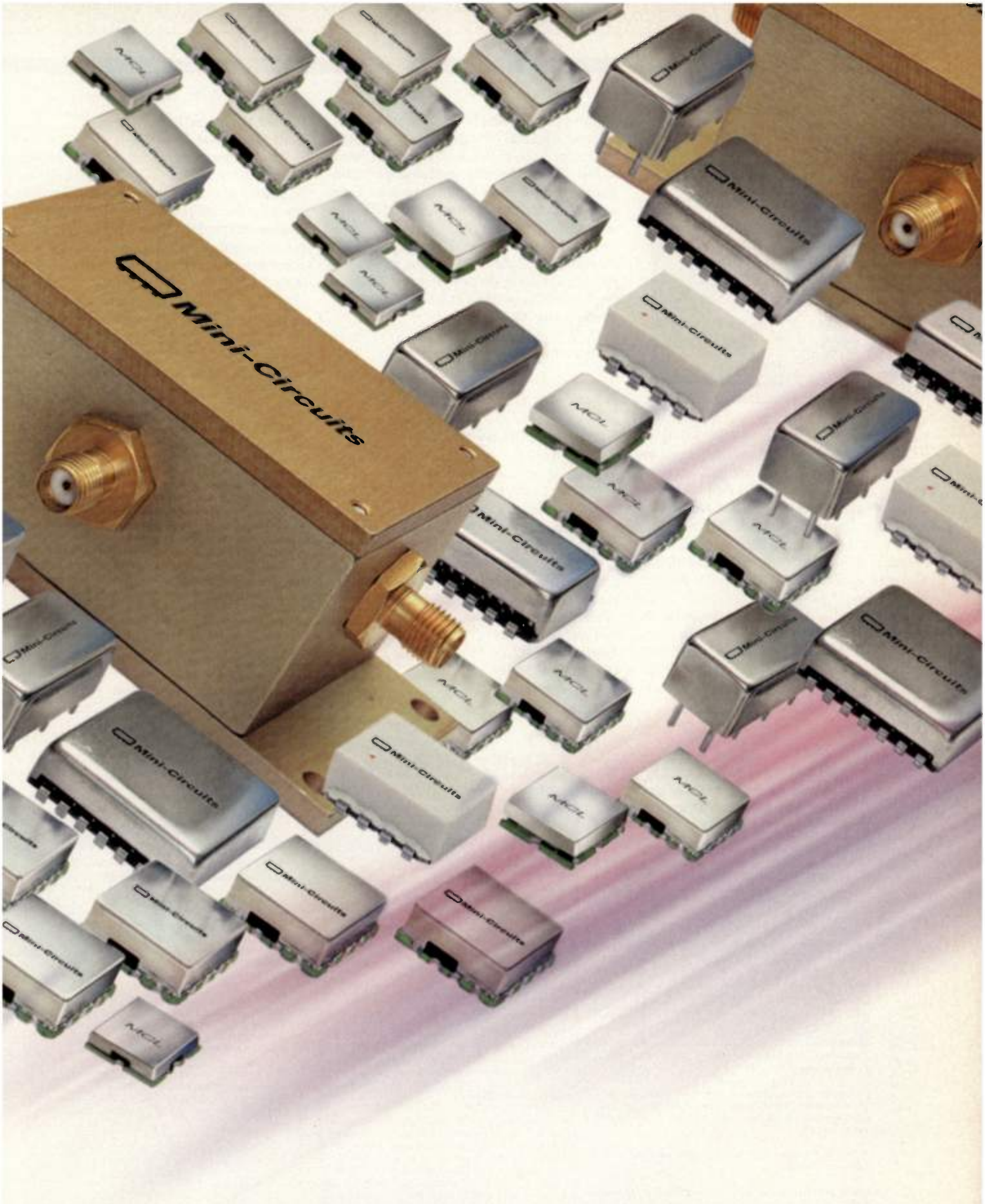
WCS markets. This design supplies a minimum P1dB of 2 W and covers 1900 to 2500 MHz. Linear gain is 34 dB with a ±0.4 dB flatness across the band, and VSWR in/out of 1.5:1. The unit consumes ~1.3 A of quiescent current and has internal voltage regulation that allows for operation between +8 to +12 V. Standard features include logic on/off control and thermal protection with an automatic reset. The overall module measures 4.7 inches x 2.0 inches x 0.54 inches.
Stealth Microwave Inc.
(888) 772-7791
www.stealthmicrowave.com

Video module

Adimos has developed a proprietary wireless multimedia connectivity solution for consumer appliances. Called wireless video module WVM1100, the semiconductor chips incorporated in the module deliver quality multimedia transmission over a wireless channel between any multimedia source (DVD, VCR, set-top box and media servers) and a multimedia display (plasma TV, LCD TV, home projectors, projection TV).

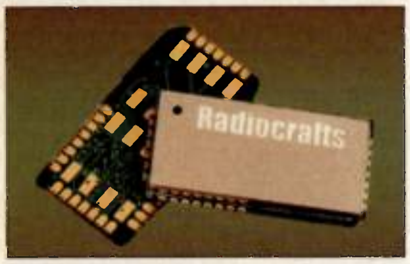
Using CMOS ASIC and SiGe-based power amplifier IC, the WVM offers a range of up to 75 meters. It incorporates fully standards-compliant wireless and video compression technologies, with complete software drivers and straightforward user interfaces. Plus, it implements embedded noise and interference management technology.

Key features include IEEE 802.11a 5 GHz wireless communications; a modular RF section that can be easily replaced to comply with different country spectrum requirements; MPEG-2 standard video compression and decompression, wireless bit rates of 6, 12 and 24 Mbps; video bit rates of 4, 8 and 14 Mbps; automatic adaptation of video bit rate and wireless link bit rate, can be set to fixed video bit rate and wireless link bit rate; and proprietary air protocol with re-transmit algorithm and buffer management algorithm. In addition, it offers automatic discovery and decision procedure for wireless channel selection with overall propagation delay of <1s. Furthermore, to ensure privacy and protection of video rights, it also includes security and encryption features. Operating from a 3.3 VDC supply, the WVM dissipates 5 W.
Adimos
(510) 209-4793
www.adimos.com


Mini-Circuits
MCL

Integrated Subsystems

RF modules with embedded protocol



Radiocrafts AS has introduced a series of small-form RF modules. The RC1040, RC1080 and RC1090 series of modules have a half a square inch footprint and are two-way radio solutions with an embedded protocol. The shielded modules made for surface mounting measure 12.7 mm x 25.4 mm x 3.5 mm. Data buffering, addressing and error check are all handled by the embedded RC232 protocol. A standard UART serial bus is the interface to the host.

Typical applications include home, building and industrial automation, automatic meter reading, remote control and telemetry, fleet and asset management. The modules are designed for operation in the license-free bands in Europe at 433 and 868 MHz respectively, whereas RC1090 operates under FCC regulations for use in the United States and Canada at 902-928 MHz. The modules are multichannel transceivers with up to nine channels, 10 dBm output power and -100 dBm sensitivity at 19.2 kbps.

The modules are suitable for pick and place automatic assembly for volume production and are available on tape and reel. Volume pricing (>50k) is down at USD 20.

Radiocrafts AS
(+47) 970 86 676
www.radiocrafts.com

Design Software

Signal circuit synthesis tool

Eagleware has introduced SIGNAL CONTROL, an add-on module to Genesys. The SIGNAL CONTROL module synthesizes signal circuits that traffic the flow of power through a network. A module add-on to the Genesys version 2003.10, it is capable of laying out circuits with the input of desired characteristics such as topology and frequency range. The signal control 37 structures include couplers, splitters, combiners, baluns and attenuators.

Eagleware
(678) 291-0259
www.eagleware.com

Models for Schottky and varactor diodes

Modelithics has introduced a complete library of non-linear diode models for Schottky and varactor diodes. The new library is the company's first library of active component models. Most of the diode models are substrate-scalable, meaning that they accurately represent the component on a wide variety of popular substrates. The diodes represent components from leading vendors including Infineon, Toshiba, On Semiconductor, and Alpha, and are compatible with Agilent's ADS. The Modelithics Diode Libraries will also be available for Applied Wave Research Microwave Office and Eagleware GENESYS in the near future.

Modelithics
(813) 866-6335
www.modelithics.com

RLC extractor

Ansoft Corporation has released the Q3D Extractor v6, the next generation of 3D parasitic extraction technology. Q3D Extractor assists in the design of nets and interconnect components in integrated circuit (IC) packages (i.e., leads, bond wires), on printed circuit boards (PCBs) and in the connection path between them (i.e., connectors, cables, sockets, transmission lines).

The technology features the Ansoft Desk-

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• Phase-locked cavity oscillators
• Phase-locked coaxial resonators
• Synthesizers for SATCOM
• Fast-tuning communication synthesizers
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• Power to 10 watts
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MITEQ
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100 Davids Drive
Hauppauge, NY 11788
TEL.: (631) 436-7400 • FAX: (631) 436-7430
Circle 37 or visit freeproductinfo.net/rfd

top, an intuitive, easy-to-use, design environment already familiar to HFSS v9 and Ansoft Designer customers. The new environment integrates all electromagnetic-field simulations required for the extraction of 3D RLC parameters and automatically generates equivalent circuit models.

Q3D Extractor v6 will be available for general commercial release in March 2004.
Ansoft Corporation
(412) 261-3200
www.ansoft.com

Design environment

Agilent has updated the RF Design environment in release C. The updates include the following features:

RFDE 2003C-Wireless Test Benches: Wireless Test Benches can directly verify Cadence-based RF circuit schematics with various baseband architectures.

RFDE 2003C-RFDE Momentum: EM-based models generation using Momentum is integrated with RF Design Environment 2003C.

RFDE 2003C-Verilog-A Compiler: Verilog-A Compiler enables the simulation of Verilog-A models in ADS/RFDE, with simulation times comparable to built-in models.
Agilent Technologies
(800) 452 4844
www.agilent.com

Interface and Interconnects

50Ω cables

Belden Electronics Division has announced the addition of RF500 and RF600 cables to its line of RF coaxial cables. These large, low-loss, 50Ω coaxial cables are engineered for transmission quality and reliability, plus they exactly meet industry size standards with diameters of 0.500-inches (RF500) and 0.590-inches (RF600).

RF500 and RF600 coaxial cables feature copper-clad aluminum conductors, foamed high-density polyethylene (FHDPE) insulation, an aluminum foil and tinned copper braid composite shield, and a choice of either PE or PVC jacket. The cables are also 100% sweep tested for VSWR and exhibit phase stability over both temperature changes and repeated flexing conditions, resulting in signal integrity and electrical performance.

These cables are available in three versions: with weatherproof PE jackets (Product #7976A and 7977A); with PE jackets that include a water-blocking gel embedded in the shield for additional protection in wet environments (Product #7976WB and 7977WB); and with flame-retardant PVC jackets and a UL listing for interior riser applications (Product #7976R and 7977R).
Belden Electronics Division
(800) 235-3361
www.belden.com

QMA connector

RF Connector Division of RF Industries Inc. has announced a QMA series connector designed similar to the SMA internal configuration with a snap-on interface. It needs no tooling for mating and unmating. The connector features a sliding snap-lock mechanism that works by sliding the shell back and releasing to lock both connectors in place. This can

eliminate space between connectors.

After they are mated, the QMA connectors can be rotated 360 degrees. Designed to mate with all QMA jacks, they offer electrical performance up to 6 GHz.

Both the RQA-5010-C, for RG-58/U and LMR-195 cable, and the RQA-5010-X, for RG-8/X and LMR-240 cable, feature albaloy plated brass bodies, Teflon insulation, spring copper alloy outer contacts and gold plated pins.

RF Industries, Inc.
800-233-1728
www.rfindustries.com

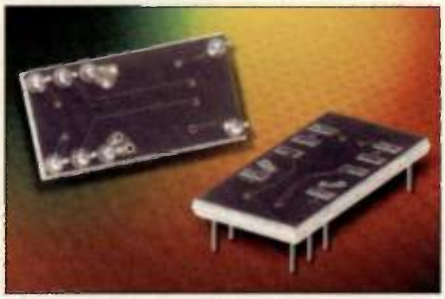
HD-ready video patch jack

Trompeter's enhanced J314 series dual patch jacks are for TV broadcast and production facilities. Available as individual units or loaded into panels, the patch jacks include the J314W and J314WT (terminated and non-terminated versions) jacks as well as a smaller J314MW and J314MWT jacks for the miniWECo plug standard.

The enhanced J314 series is designed with a forked actuator to enable multiple contact points for robust normal-through interconnection in high non-conductive particulate environments. The 75 Ω design offers extended bandwidth of 1 MHz to 3GHz with return loss performance of 20 dB at 2.2 GHz in the normal-through condition. The J314 series provides self-wiping action upon plug insertion, an approach that eliminates the need for heavy and complex dust control plungers and multiple actuators.

Trompeter
(800) 982-2629
www.trompeter.com

SOIC adapter



Aries Electronics now offers SOIC adapters that provide an upgrade from older Aromat HB2E relays to surface-mount TXSS relays while keeping the same PBC layout.

Available on 0.300 inch (7.62 mm) DIP centers, the new adapter can be mounted on PCBs with a PCB hole diameter of 0.028 inch +/-0.003 inch (.71 mm +/-.08 mm). The adapters are available with eight leads.

The adapters are constructed of 0.062 inch (1.57 mm) thick FR-4 with 1 ounce of copper traces on both sides. The pins are 360 ½ hard brass alloy, per UNS C36000 ASTM-B16085, and pin plating is 200 μ (5.08 μm) minimum tin/lead 93/7, per MIL-P-81728 over 100 μ (2.54 μm) minimum nickel, per QQ-N-290. Operating temperature is 221°F (105°C).

Pricing for 1000 pieces is $5.40 each with delivery from stock to three weeks.

Aries Electronics
(908) 996-6841
www.arieselec.com

Materials

Composite preforms

TechFilm has provided a product for electrical conductivity and electrical insulation properties in one preform. The "Composite Preform" materials are formulated to meet ASTMD 3850 as well as MIL. 883 section 3.8.5.1 outgassing specifications.

TechFilm products have many uses in manufacturing including BGA packages, circuit boards, EMI shielding, enclosures, hybrid microelectronics assemblies, laminating films, semiconductor packaging and devices, smart cards, substrate attach and many other high-performance industrial products.

Techfilm Services, Inc.
(888) 832-4345
www.techfilm.com

Semiconductors and ICs

Downconverter RFIC

Hittite Microwave Corporation has released a new downconverter RFIC that is designed for use in wireless infrastructure applications in the 800-1000 MHz band, including those based on GSM, CDMA, GPRS and EDGE standards.

The integrated mixer coupled with an IF amplifier, enables the HMC377QS16G to achieve an input IP3 of +15 dBm, while providing 14 dB of conversion gain and an excellent noise figure of 11 dB. An integrated LO buffer amplifier accepts a range of LO drive levels, from 0 to -10 dBm and can be driven directly from a frequency synthesizer output. The LO to IF & RF to IF isolations of 70 dB and 90 dB, respectively, may help to reduce the filtering requirements within the receiver. The mixer supports IF frequencies from 50 to 250 MHz and operates from a single +5.0 V supply.

Samples and evaluation PC boards are available from stock for sampling or sale.

Hittite Microwave Corporation
(978) 250-3343
www.hittite.com

90 W LDMOS for 860 to 960 MHz

Infineon Technologies' PTF080901E GOLDMOS is a field effect transistor for EDGE and CDMA applications in a thermally enhanced package. This 90 W, LDMOS single-ended transistor delivers 45 W average output power under EDGE conditions with 40 percent efficiency and 18 dB gain. Typical CW performance gives an impressive 120 W typical output power with 60 percent efficiency and 17 dB gain. Added to this performance is a low thermal resistance with a 0.52 °C/W. Capable of handling 10:1 VSWR at 28 V, 90 W CW, it has thermal stability and low HCI drift. The transistor uses full gold metallization and integrated ESD protection.

Infineon Technologies NA
(408) 776-0600
www.infineon.com/rfpower

RF receiver IC

California Eastern Laboratories has introduced NEC's UPB1009K a single-chip double-conversion RF-to-IF I-Q frequency translator designed to provide a complete RF front end for GPS receivers. It is compatible with W-CDMA, GSM and PDC systems. An integrated solution, it combines a low-noise amplifier, VCO, PLL, IF AGC amplifiers, IF filtering, I-Q demodulators, I-Q IF amplifiers, and a 4-bit A/D converter, all in a single, compact 44 pin QFN package.

The on-board fractional N PLL can use four TCXO reference frequencies, enabling it to share the TCXO with other functional blocks like the CPU, the voice RF receiver or the baseband IC. This multiple system reference clock enables the IC to share the TCXO function across a variety of different handheld communications platforms.

In stock and available now, the UPB1009K is priced at $4.30 in 50K quantities.

California Eastern Laboratories
(408) 988-3500
www.cel.com

Gallium arsenide HBT process

TriQuint Semiconductor, Inc. has introduced its high-volume TQHBT3 InGaP heterojunction bipolar transistor (HBT) process fabricated in its 150 mm Oregon wafer manufacturing facility. This process can enable designers of RF amplifiers for cell phone, WLAN, WiMax and broadband power applications to achieve increased gain, power level and efficiency for a given device size due to higher transistor performance.

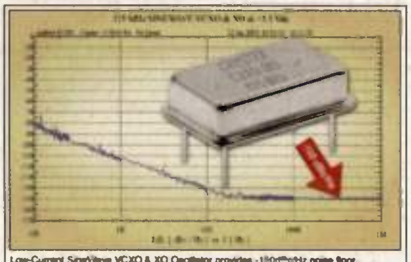
TQHBT3 features TriQuint's flexible three layer metal system with over 6 microns of gold thickness. Die size for a given power level or function can be reduced, leading to lower part cost and printed circuit board area used. TQHBT3 features 2-micron and 3-micron emitter width transistors.

The preliminary process features a Vbe of +1.15 V, 130 Beta and 40 GHz Ft. The maximum available gain is greater than 22 dB at 6 GHz with a 3 micron emitter. The VSWR is 70:1 at 5 V supply. The breakdown voltage equals 24, 7, and 14 V.

TriQuint Semiconductor
503/615-9000
www.triquint.com

Signal Sources

VCXO oscillator



Low-Current SineWave VCXO & XO Oscillator provides -150dBc/Hz noise floor
Crystek Crystals Corporation CRY-012

Crystek Crystals Corporation has launched a low-current sine wave oscillator providing -150 dBc/Hz noise floor and consuming only 8 mA typical and 15 mA max current at 3.3 V. The output level is 0 dBm min into 50 Ω, and harmonics are lower than -20 dBc.

The oscillator is offered in 3.3 V and 5 V models, and in VCXO version (Model CVXO-083/085) and clock version (Model CCO-083/085). Both versions are packaged using industrial-standard 14-pin DIP package.

The oscillator generates frequencies between 10 MHz and 330 MHz. The low current consumption is useful in low-current budget applications. Extended temperature operating range of -40°C to +85°C and other custom specifications are also available.

The oscillator is priced starting at $20.00 each in volume, depending on specification.

Crystek Crystals Corp.
(800) 237-3061
www.crystek.com

Test and Measurement

GPRS network analyzer

Astellia has introduced the OCEANCIGALE GPRS, which supplies a number of multilevel Key Performance Indicators (KPI) on the effective network throughput and on the quality of service. Since the information is available from the PCU (Packet Control Unit) level down to the cell level, problems can be traced from an entire group of IMSI (International Mobile Subscriber Identity) down to a single one and at any critical part of the network per APN (Access Point Name). Operators can track, analyze and monitor element failures and optimize network performance even when data are ciphered, as this analyzer is capable of deciphering hundreds of thousands of ciphered IMSI.

ASTELLIA
(011.33) 2 99 04 80 60
www.astellia.com

2.7 GHz PXI RF vector signal generator

National Instruments' 2.7 GHz NI PXI-5670 RF vector signal generator is the latest addition to the company's RF product line, which also includes the NI PXI-5660 RF vector signal analyzer and Modulation Toolkit and Spectral Measurements Toolkit for LabVIEW 7 Express. The PXI-5670 module offers 16-bit resolution arbitrary waveform generation at 100 Msps (400 Msps interpolated), up to 256 MB of memory and 22 MHz real-time bandwidth.

This RF vector signal generator offers signal generation from 250 kHz to 2.7 GHz and can produce analog and custom digital modulation as well as standard digital modulation formats such as ASK, FSK, MSK, PSK and QAM.

The toolkit also offers functions to inject impairments into a communications system including IQ gain imbalance, quadrature skew and additive white Gaussian noise (AWGN). Visualization functions include trellis, constellation and two- and three-dimensional eye diagrams. NI-RFSG is a fully functional instrument driver and works with a variety of application software including LabVIEW 7 Express, LabWindows/CVI and C.

The generator is a combination of the NI PXI-5610 2.7 GHz RF upconverter, the NI PXI-5421 16-bit arbitrary waveform generator and the NI Modulation Toolkit.

The vector network analyzer is priced from $12,995

National Instruments
(800) 258-7022
www.ni.com

Autocorrelator for laser diagnostics

Spectra-Physics has introduced the PulseScout, a new autocorrelator for ultrafast laser diagnostics.

The PulseScout gives customers the ability to measure laser pulse durations ranging from 20 femtoseconds to the picosecond regime, and can be configured for wavelengths from 420 nm to 1600 nm. With two user interchangeable detector modules, the autocorrelator extends to measure pulse widths from both, low energy, high (MHz) repetition rate oscillators and high energy, low repetition rate amplifiers. Equipped with an integrated spectrometer, the PulseScout enables simultaneous measurement of both, the temporal and spectral components of ultrafast laser pulses.

The PulseScout is a suitable diagnostic accessory for the new Eclipse femtosecond amplifier from Spectra-Physics as well as traditional Ti:sapphire-based lasers and amplifiers, optical parametric amplifiers (OPAs) and oscillators (OPOs).

Based on technology usng piezoelectric scanning, the PulseScout makes alignment of the autocorrelator head with the input laser beam simple by only requiring the centering of an internal reflection on the cross hairs of a translucent window mounted above the input aperture.

The PulseScout is completely self-contained with no requirement for oscilloscopes or computers for operation. A microprocessor-driven compact control unit with onboard LCD operates the autocorrelator head and the optional spectrometer through simple on-screen menus. Autocorrelation trace and spectrum can be displayed and analyzed on the screen, or downloaded to a remote computer via an RS-232 interface. All controller settings can also be set remotely through the same RS-232 interface allowing total integration into a computer-controlled experiment or test setup.

Spectra-Physics
650-961-2550
www.spectra-physics.com

Broadband signal analyzer

Aeroflex Incorporated has added new signal measurement capabilities to its Celerity CS35000 Series Broadband Signal Analyzer and Recorder family (BSA). The Celerity BSA family is a modular test system designed to capture, analyze and record high-speed broadband signals. This analyzer is configurable up to 600 MHz.

For design and testing of analog or digital broadband signals or signal environments, the analyzer offers a single-instrument approach for performing simultaneous measurements of frequency, time and multiple demodulation parameters. The BSA encompasses the test capabilities of a spectrum analyzer, deep memory logic analyzer, oscilloscope and signal analyzer—all in one instrument. All signals are displayed in one window where the user can monitor up to 12 displays at once, all updating in real time.

The BSA includes software to analyze demanding broadband signals with digital speed and precision. Advanced software features and DSP-based analysis modules provide the latest tools to measure and characterize signals captured in BSA hardware or loaded from stored signal files.

In addition to the existing PSK and QAM demodulation modules, Aeroflex now offers the CS35000 Series with a wide variety of software analysis modules, allowing more in-depth analysis of broadband signals.

Engineers can measure and capture signals in the BSA with new software modules for FSK, MSK and AM/FM demodulation, for adjacent-channel power and multiple channel power, for radio-specific analysis including SINCGARS and LINK 16, and for statistics, EVM, and symbol rates. New BSA software features, in addition to the existing frequency spectrum display and time and modulation analysis capabilities, include parameter strip-chart display, parameter-based triggering, parameter logging, frequency-based analysis, simultaneous parameter analysis, time tagging on logged data and analysis on real-time or captured signals acquisition, analysis and recording applications.

Products are specified by bandwidth, dynamic range, signal memory, and options such as frequency downconversion, low phase noise sample clock, disk storage, multiple channels, mixed signals, and remote control.

Prices range from U.S. $65,000 for a basic configuration to $350,000 for the highest-performance instrument with software options.

Aeroflex Incorporated
(516) 694-6700
www.aeroflex.com

Tx and Rx

C or Ku Antenna

Patriot Antenna Systems' 3.8 meter C-band or Ku-Band transmit/receive antenna has four port feed assemblies. Many customers require the extra link margin that a larger antenna like a 3.8 meter can provide, for the hub station in their VSAT networks, a video uplink, or an SCPC central station. Every Az/El fixed Kingpost antenna is fully "upgradeable" in the field to a dual-axis motorized antenna with 180° H to H mount.

The form factor is a stretch-formed 3.8 meter antenna with kerf panels. This antenna allows for installation without the need of a crane or a lifting device.

Patriot Antenna Systems
(800) 470-3510
www.patriotsystems.com

Flange mount drop-in isolator

REC's L series features up to 15 percent bandwidth in the 8.0 to 40.0 GHz range. The isolator is suitable for military and space applications and made of steel housing that is gold-plated for better RF performance. This temperature-stable device has a typical loss of <0.4 dB and a VSWR and isolation of >20 dB. It measures 0.25 x 0.50 x 0.18.

Renaissance Electronics Corporation
(978) 772-7774
www.rec-usa.com

GaAs HBT multiplier

Hittite Microwave Corporation has introduced a 9.9 – 12.7 GHz Active X2 Frequency Multiplier that is suitable for use as an LO multiplier in microwave radio, VSAT, radar and ECM applications, as well as in OC-192 clock recovery circuits.

The HMC369LP3 provides +4 dBm of output power that varies minimally vs. input power, supply voltage and temperature. All undesired fundamental and sub-harmonics are suppressed to 30 dBc with respect to the output signal level, while the low additive SSB phase noise of -142 dBc/Hz at 100 kHz offset helps the user maintain good system noise performance. The multiplier is housed in a 3 mm x 3 mm leadless QFN SMT package and consumes only 46 mA from a +5.0 V supply.
Hittite Microwave Corporation
(978) 250-3343
www.hittite.com

WLAN power dividers

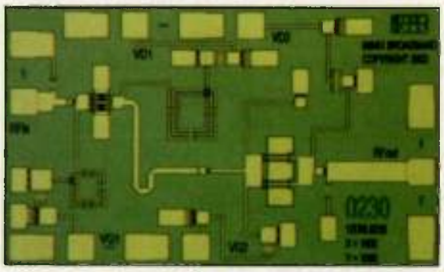
JFW Industries has announced broadband two-way, four-way and eight-way power dividers designed specifically for WLAN applications. The 50PD-519 (two-way), 50PD-520 (four-way), and 50PD-521 (eight-way) operate from 2 to 6 GHz with a maximum insertion loss of 3.6 dB (3.4 dB typical). Each model will handle up to 5 W of continuous RF power and maintains a minimum isolation of 20 dB. SMA connectors are standard with custom designs available.
JFW Industries
(317) 887-1340
www.jfwindustries.com

Helical bandpass filters

Temwell has introduced a series of helical bandpass filers available per customers' specification. The helical bandpass filters have a frequency range of 44 to 2550 MHz and are available in 75 or 50 Ω impedance. The insertion loss ranges from 1.0 to 8.0 dB.

The bandpass filters are available immediately with a minimum order of 10 pieces.
Temwell
886-2-25652500
www.temwell.com.tw

Two-stage GaAs MMIC doubler



Mimix Broadband Inc. has released a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) two-stage doubler that can be used to drive fundamental mixer devices. Using 0.15 micron gate-length GaAs pseudomorphic high electron mobility transistor (pHEMT) device technology, this doubler converts input signals in the 9 to 14 GHz frequency range to output signals in the 18 to 28 GHz frequency range. This device has +12 dBm output drive.

This doubler, identified as 12DBL0230, is ideal to drive Mimix's XR1002 receiver, and is well suited for wireless communications applications such as millimeter-wave point-to-point radio, local multipoint distribution services (LMDS), SATCOM, and radar applications.

The manufacturer performs 100 percent on-wafer RF, DC and output power testing on the 12DBL0230, as well as 100 percent visual inspection to MIL-STD-883 method 2010.

The chip also has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process.

Engineering samples are available today from stock, and production quantities are available six to eight weeks ARO.
Mimix Broadband
(281) 988-4600.
www.mimixbroadband.com.

Amplifiers

Wideband power module

Stealth Microwave Inc. has introduced a wideband power module. The SM2040-37 is a 2.0 to 4.0 GHz solid-state GaAs amplifier designed for multipurpose use in military and wireless markets. This module has a linear gain of 37 dB and 5 W of output powerat the P1dB compression point. It operates from a single supply voltage of +12 V at 2.7 A of quiescent current. Features include over/reverse voltage protection, thermal protection with auto reset, and TTL logic on/off control. Forward power detection is available as an option.

The amplifier comes standard as a 5.0 inch x 2.5 inch x 0.8 inch module with six thru-holes.

Stealth Microwave Inc.
(888) 772-7791
www.stealthmicrowave.com

MMIC amplifiers

Mini-Circuits has introduced MMIC amplifiers that are usable to 4 GHz. These high 25 dB gain amplifiers feature both a high IP3 of +38 dBm and a low 2.9 dB NF. Even after passing grueling operating life tests of 5000 hours at elevated ambient temperature of 125°C, these new rugged units still offer protection against unwanted transient supply voltages. Offered at a low price of $2.35 each (quantity 25) and $1.35 each (quantity 1000). Available from stock.

Mini-Circuits
(718) 934-4500
www.minicircuits.com

Driver amplifier 800 – 3800 MHz

Hittite Microwave Corporation has improved the performance of the previously released HMC308. The HMC308 is a 800 – 3800 MHz, fully matched GaAs MMIC amplifier that is suitable for use as a transmit chain driver amplifier, or as an LO buffer amplifier driving high IP3 passive mixers in cellular/PCS/3G, fixed wireless and WLAN applications.

The HMC308 is a versatile, cascadeable driver amplifier that operates from a single +3 V or +5 V supply, has integrated DC blocks on both RF ports, and requires no external components. When biased with +5 V, the amplifier provides 18 dB of gain, and +20 dBm of saturated output power, while consuming 53 mA of current. This ultra small SOT26 SMT-packaged amplifier is a low cost, broadband device ideal for area-constrained designs.

Samples and evaluation PC boards are available from stock for sampling or sale.

Hittite Microwave
(978) 250-3343
www.hittite.com

Power amplifier

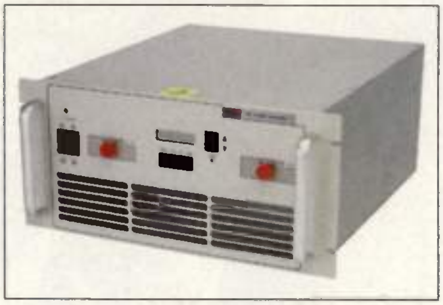
OPHIR RF's amplifier, model 4022, is a high-power amplifier that produces 200 W of CW power over the instantaneous frequency range of 2.7 GHz – 3.2 GHz.

This unit was designed for S-band radar applications, such as military radar, airport surveillance and maritime navigation radar.

The 4022 comes standard with RF input overdrive protection, as well as the ability to withstand an infinite load VSWR mismatch, all in a 5U high rack-mount chassis.

OPHIR RF
(310) 306-5556
www.ophirrf.com

VHF and UHF amplifiers and integrated bandswitch



Vishay Intertechnology Inc. has released the first parts in a new family of dual-MOSMIC (MOS Monolithic Integrated Circuit) devices that combine two MOSMIC amplifiers, one intended for use in VHF applications and the other for UHF applications, and an integrated switch in the industry-standard SOT363 plastic package.

Each of the devices released features two different MOSMIC amplifiers with common source and Gate 2 leads. The first MOSMIC stage, which features a fully internal, self-biasing network-on-chip, is designed to provide for optimal cross-modulation performance and low-noise figures at lower VHF frequencies. The second MOSMIC stage is intended to provide superior gain and noise figure performance at the higher frequencies of the UHF range. It features a partly integrated bias for easy Gate 1 switch-off with PNP switching transistors inside PLL integrated circuits.

The devices' integrated band switch not only reduces the number of lines on the printed circuit board, but also lowers the number of external components required. Integrated antiserial diodes between the gates and source protect against excessive input voltage. The drain output pin of each stage is opposite to the corresponding Gate 1 pin in an "SOT363(L)" pin configuration. Both the TSDF12830YS and TSDF32830YS offer a high AGC range with a soft slope and a main AGC control range of 3 V to 0.5 V.

Samples and production quantities of the new dual-MOSMIC devices are available now with lead times of eight weeks for larger orders. Pricing for U.S. delivery in 100,000-piece quantities starts at $10.00 per 100 pieces.

Vishay Intertechnology Inc.
(401) 738-9150
www.vishay.com

Controller monitor

Dallas Semiconductor has introduced the DS1870, an LDMOS power-amp biasing and monitoring solution. The device optimally biases two LDMOS power amps over temperature and drain voltage/current variations. It also manages system monitoring. The high level of integration reduces component count, layout area, and speeds up the design of LDMOS power-amp modules.

Dual 256-step potentiometers enable optimal gate-bias operation for two LDMOS power amplifiers. The summation of two lookup table entries controls each potentiometer. The first lookup table adjusts for temperature variation in 2 degrees Celsius increments, while the second lookup table adjusts for variations in drain voltage (or other external parameters). The voltage range of the potentiometer output can be adjusted to provide fine resolution control.

Monitoring functionality is enabled by a 12-bit analog-to-digital converter (ADC) with three muxed analog inputs, plus VCC monitor and temperature sensor. A fault signal can be generated in response to an out-of-tolerance condition in any of these parameters. In addition, 32 bytes of user EEPROM are available for manufacturing or vendor data.

Communication with the devices is achieved over an I(2)C interface. Three address pins enable up to eight devices on a common serial bus. The DS1870 is available in a 16-pin TSSOP and operates from a 4.5 V to 5.5 V power supply over a -40 degrees Celsius to +95 degrees Celsius temperature range.

Dallas Semiconductor
(408) 737-7600
www.maxim-ic.com

Digital Systems

14-bit ADC

A new 80 Msps, 14-bit analog to digital

converter (ADC) from **Linear Technology** can provides designers of cellular base stations with a dramatic improvement in dynamic performance, according to the company. The LTC1750 eliminates the second intermediate frequency (IF) down-conversion stage. The device provides wide input bandwidth and dynamic performance for direct IF digitizing applications. The ADC undersamples up to 500 MHz input frequencies and delivers 84 dB spurious-free dynamic range (SFDR) with 140 MHz inputs and 74 dB SFDR with 350 MHz inputs. The device's wide bandwidth and AC performance are ideal for use in cellular base stations and broadband software radios, where it can directly digitize the first IF and eliminate the second IF down-conversion stage.

This ADC offers the flexibility to configure the input and the output specifically for the application. An on-chip programmable gain amplifier (PGA) allows multiple input ranges to optimize the performance. The larger input range offers low noise, and the smaller range lowers the gain requirements on the drive circuitry, making it easier to meet the IP3 requirements. If the input ever goes out of range, there is automatic indicator on the overflow pin. A separate digital output supply pin allows connection to low voltage DSPs, FIFOs or logic as low as 0.5 V.

Pricing for 1000-piece quantities begins at $32.30 each for the LTC1750.

Linear Technology
(408) 432-1900
www.linear.com

Video add-on multiplexers

Transparent Video Corporation (TVC) has helped cut costs for stations seeking to upgrade to HDTV or increase ENG signal output by introducing two add-on multiplexers.

The MegaMux STL-4000 and MegaMux ENG-4000 add-ons provide digital capability to studio-transmitter links and quadruple the output of ENG transmissions, without the cost of buying additional microwave transmission equipment. Both MegaMux systems are supposed to improve bandwidth performance and expand the capability of existing equipment.

The MegaMux STL-4000 permits broadcasters to produce digital performance with existing studio-transmitter links. The compact, rack-mount system features advanced MPEG encoding, decoding and multiplexing technology, combined with mutlilevel, digital RF modulation.

The all-in-one design is easy to install and improves the performance of legacy STL equipment by converting the NTSC video signals to an MPEG-2 stream at approximately 6 megabits per second for SD programs and 19.34 megabits per second for HD. The MegaMux STL-4000 then multiplexes the signals to provide multiple program support over a single RF carrier.

Studios can transmit NTSC or PAL video and the DVB-ASI HDTV transport stream to the transmitter site simultaneously-without installing additional microwave transmitter links.

The MegaMux ENG-4000 does the job of four microwave radio links by compressing four channels of composite video and four channels of stereo audio, boosting the bandwidth capacity of ENG units by 400 percent without sacrificing video or audio quality. Its multiple signaling capabilities operate within parameters of proposed FCC bandwidth-reduction regulations.

The self-contained rack-mount system transmits multiple video NTSC signals over

a single analog system. The MegaMux ENG-4000 is a complete four-channel real-time MPEG-2 encoder multiplexer.
Transparent Video Corporation
(650) 508-8699
www.transparentvideo.net

WiFi and Bluetooth

Cavity filters for WiFi/802.11b networks

Digital Communications Inc. (DCI) has released a line of filters aimed at cleaning up RF interference issues in Wi-Fi/802.11b networks. DCI's line of cavity filters enable WISPs and other wireless Internet providers to minimize service-affecting interference issues while extending coverage. DCI has designed these filters to be efficient and easy to install.

With indoor and tower-mountable outdoor options available, DCI's filters can clean up 2.4 GHz ISM channels by attenuating ±25 MHz from the center frequency with 40 dB of rejection or better. These filters can be tuned to pass the whole 802.11b band, from 2400 to 2483 MHz, or specific channels, typically 1, 6 or 11, rejecting service-affecting interference from out-of-channel. Also available is an eight-pole waterproof amplified channel filter, offering 20 dB gain on the transmission path and 20 dB gain on the receive path, which allows for greater coverage without any loss of performance in the users data rate.

The cost of an eight-pole waterproof filter is $379.
Digital Communications Inc.
(306)781-4451
www.dci.ca

Publications

Antenna CD ROMs

Noble Publishing has introduced a series of CD ROMs for professionals involved with antenna design. The three CD ROM set includes the titles Introduction to Antenna Fundamentals, Performance of Fundamental Antenna Elements and Advanced Antenna Considerations I. The lectures are authored by Dr. Steven Best.

Introduction to Antenna Fundamentals introduces basic antenna concepts and definitions used in the antenna industry. Antenna characteristics such as VSWR, radiation patterns, directivity, gain, polarization, axial ratio, and EIRP are defined, and their impact on wireless system performance is discussed. The course also describes different antenna types, including resonant antennas, frequency independent antennas, aperture antennas, arrays and electrically small antennas.

Performance of Fundamental Antenna Elements describes the basic performance characteristics of elementary antennas such as the dipole, loop and slot.

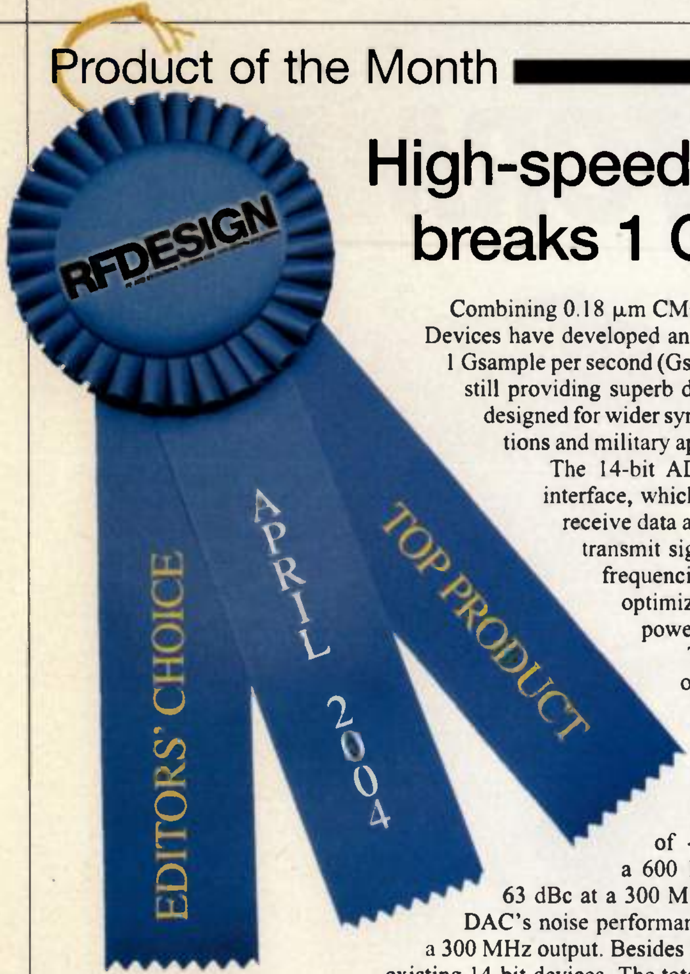
Advanced Antenna Considerations I is intended to provide a better understanding of the properties of some more complex antennas used in a variety of different communication systems.

The three CD set is available immediately for $258.00.
Noble Publishing
(770) 449-6774
www.noblepub.com

Designer's Guide

Hittite Microwave Corporation has released its 9th edition *Designer's Guide* catalog detailing more than 250 products. This publication includes 54 new RFIC and MMIC product data sheets, as well as quality/reliability, application and packaging/layout information on more than 1900 pages. New features for 2004 include an expanded application notes section detailing 10 new product & application notes.

Full specifications are provided for more than 250 components including: power and linear amplifiers, gain blocks, LNAs, attenuators, frequency dividers/multipliers, mixers, modulators, switches and VCOs.
Hittite Microwave Corporation
(978) 250-3343
www.hittite.com



High-speed 14-bit DAC breaks 1 Gsps barrier

Combining 0.18 μm CMOS process with patent-pending switch current array, designers at Analog Devices have developed an unmatched 14-bit digital-to-analog converter (DAC) that has broken the 1 Gsample per second (Gsps) barrier. At 1.2 Gsps, the AD9736 sets a new data rate benchmark, while still providing superb dynamic range and good power efficiency, claims the manufacturer. It is designed for wider synthesis bandwidth and higher IF generation in instrumentation, communications and military applications.

The 14-bit AD9736 provides a fast low-voltage differential signaling (LVDS) input interface, which enables high conversion rates over a wide bandwidth. This allows it to receive data at a high speed, while maintaining low distortion and noise, simplifying the transmit signal chain and enabling high-quality synthesis of wideband signals at IF frequencies up to the Nyquist rate. In addition, the high-speed 14-bit DAC is optimized for low power consumption to deliver significant improvement in speed, power and performance.

To double the incoming sample rate from ASICs or FPGAs capable of operating at up to 840 Msps, the AD9736 features a 2X digital interpolation filter. This allows users to take full advantage of the data converter's sample rate with existing digital technology, while future-proofing the design. A novel clock-to-data synchronization scheme simplifies the interface timing and enables the extreme sample rate to be realized.

Some key performance specs include intermodulation distortion (IMD) of -74 dBc at an output frequency of 255 MHz and better than -65 dBc up to a 600 MHz output frequency. While spurious free dynamic range (SFDR) is 63 dBc at a 300 MHz output frequency and 53 dBc at 600 MHz, sampling at 1.2 Gsps, the DAC's noise performance is excellent, with noise spectral density of -158 dBm/Hz synthesizing a 300 MHz output. Besides high noise performance, its power consumption is substantially lower than existing 14-bit devices. The total power consumption is 380 mW at 1.2 Gsps with the interpolation filter bypassed and 550 mW with the interpolation filter enabled.

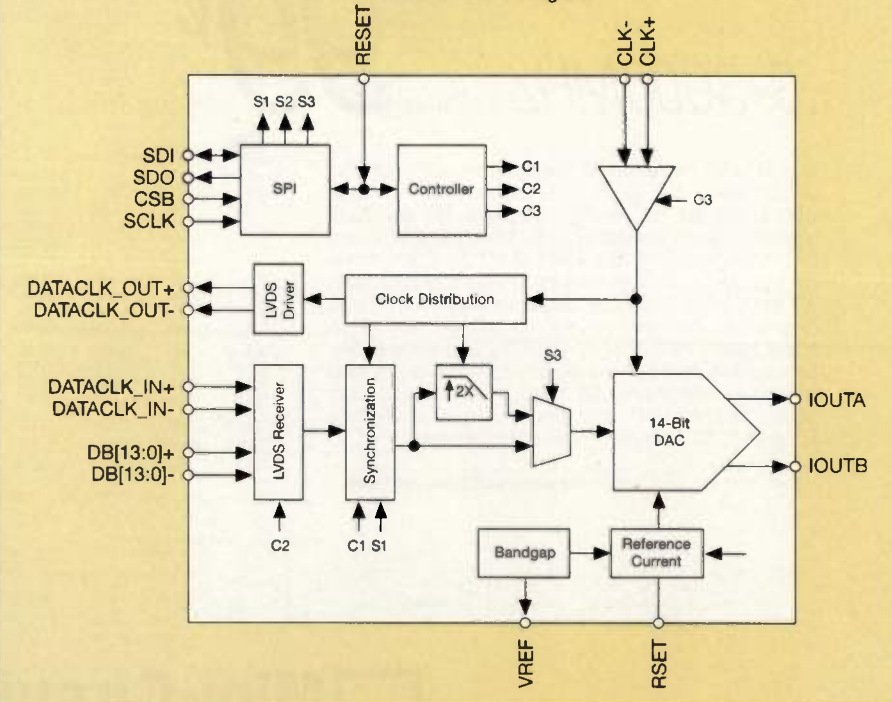
Like all high-speed DACs from ADI, conversion in the AD9736 is initiated on the rising edge of each input clock at the full DAC sample rate. Sampling only on the rising clock edge eliminates potential performance problems related to clock duty cycle sensitivity. According to the supplier, DACs that sample on both rising and falling clock edges can exhibit feedthrough of the half-rate clock if a nearly perfect 50% duty cycle is not maintained. Even small variations in duty cycle can create a significant half-rate spur and images that degrade SFDR performance over the Nyquist bandwidth. The AD9736 clocking architecture renders it largely insensitive to clock duty cycle variations.

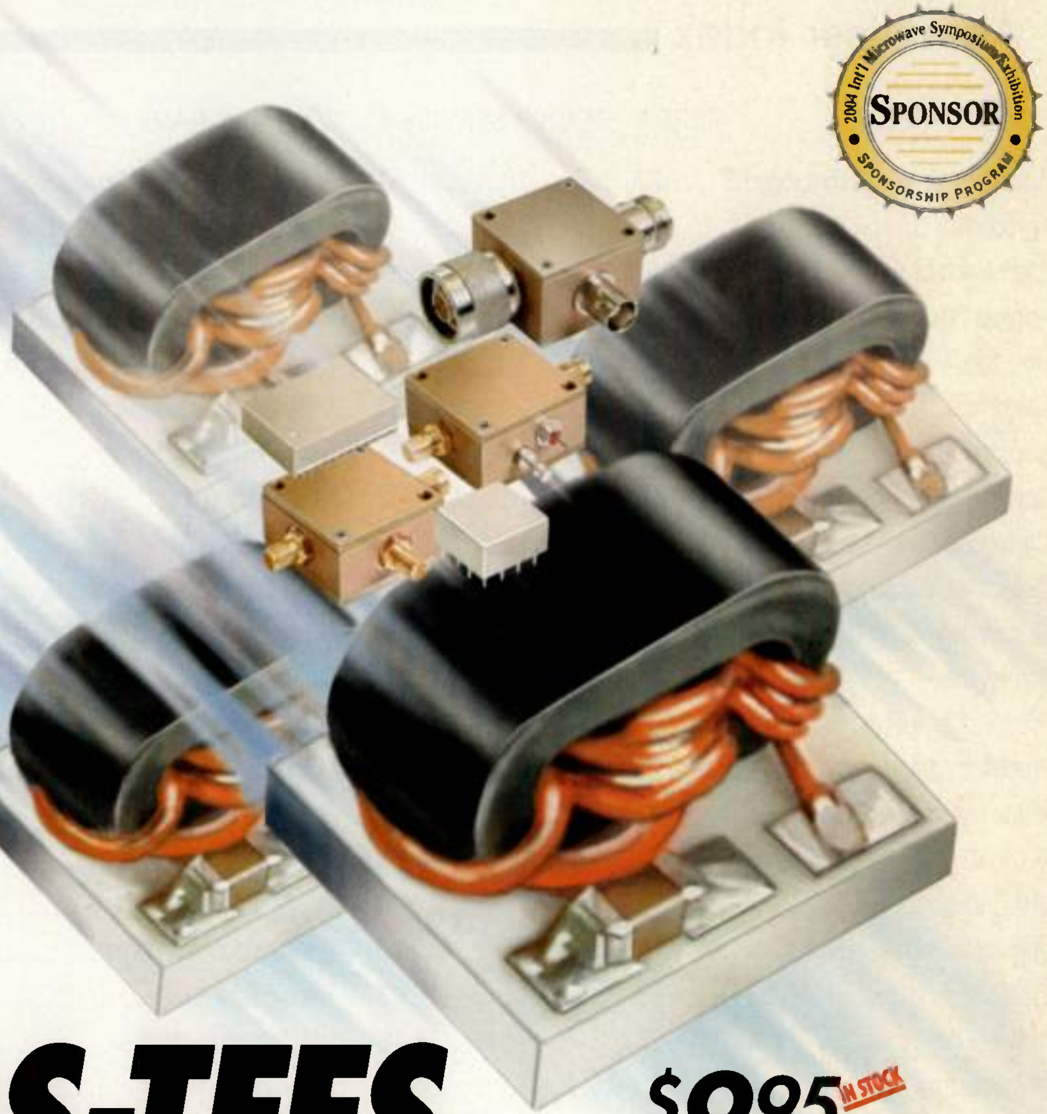
Supporting a double data rate (DDR) mode, the converter includes a serial port interface (SPI) that provides for programming many internal parameters and also enables read-back of status registers. Implemented in 0.18 μm CMOS process, the AD9736 uses dual supplies—1.8 V for digital and 3.3 V for analog functions. The DAC's output currents can be programmed over a range of 10 mA to 30 mA and can be easily configured for various single-ended or differential circuit topologies.

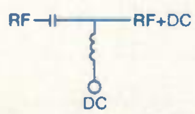
Sampling now, the AD9736 will be in production in the fourth quarter. It is offered in 800 Msps and 1.2 Gsps speed grades. For reduced package parasitics, it is housed in a 160-pin ball grid array (BGA) package. In 1000-piece quantities the AD9736-1200 is priced at $59.50.

Analog Devices Inc.
(781) 937-1428
www.analog.com/AD9736

AD9736 Block Diagram







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TYPICAL SPECIFICATIONS

Model	Freq (MHz)	Insertion Loss (dB)	Isolation (dB)	VSWR (:1)	Price $ea. Qty.10
•TCBT-2R5G	20-2500	0.35	44	1.1	8.95
•TCBT-6G NEW	50-6[illegible]00	0.7	28	1.2	11.95

TCBT Actual Size .15"x.15" *LTCC*
•*Patent Pending*

Model	Freq (MHz)	Insertion Loss (dB)	Isolation (dB)	VSWR (:1)	Qty.1-9
JEBT-4R2G	10-4200	0.6	40	1.1	39.95
JEBT-4R2GW	0.1-4200	0.6	40	1.1	59.95
PBTC-1G	10-1000	0.3	33	1.10	25.95
PBTC-3G	10-3000	0.3	30	1.13	35.95
PBTC-1GW	0.1-1000	0.3	33	1.10	35.95
PBTC-3GW	0.1-3000	0.3	30	1.13	46.95
ZFBT-4R2G	10-4200	0.6	40	1.13	59.95
ZFBT-6G	10-6000	0.6	40	1.13	79.95
ZFBT-4R2GW	0.1-4200	0.6	40	1.13	79.95
ZFBT-6GW	0.1-6000	0.6	40	1.13	89.95
ZFBT-4R2G-FT	10-4200	0.6	N/A	1.13	59.95
ZFBT-6G-FT	10-6[illegible]0	0.6	N/A	1.13	79.95
ZFBT-4R2GW-FT	0.1-4200	0.6	N/A	1.13	79.95
ZFBT-6GW-FT	0.1-6000	0.6	N/A	1.13	89.95
ZNBT-60-1W	2.5-6000	0.6	45	1.10	82.95

NOTE: Isolation dB applies to DC to (RF) and DC to (RF+DC) ports

For DC current ratings and performance data, see data sheets online at: **www.minicircuits.com/bias.html**

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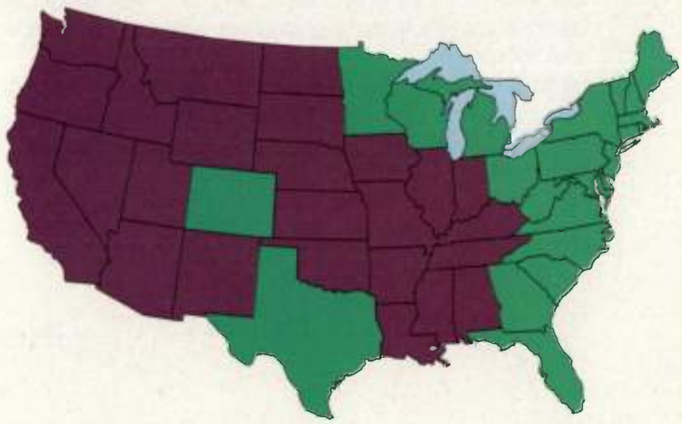

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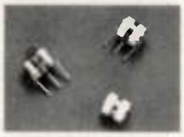
- AC Protector UL1449



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- **Utech Electronics**
  800-268-8832
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Circle 204 or visit freeproductinfo.net/rfd

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Characterizing [S]-parameters of 75 Ω circuits with 50 Ω lab equipment

By James Liu and Brian Whitaker

RF engineers working with cable, terrestrial or satellite TV applications are frequently required to make S-parameter measurements on these circuits. But how do you measure [S]-parameters of 75 Ω device under test (DUT) on a 50 Ω vector network analyzer (VNA)? If the situation warrants the cost, the answer is to buy lab equipment designed specifically for measuring 75 Ω circuits. Otherwise, using a minimum loss pad (MLP) to transform the conventional 50 Ω test port impedance to the 75 Ω DUT provides an inexpensive, easy way to get reasonable measurements.

When an IC manufacturer specifies the input return loss ($|S11|$) of a new cable TV LNA, the measurement is necessarily referred to 75 Ω. That is to say, if $|S11| = -30$ dB (reflected power is only one part in a thousand—essentially a perfect match), the idea is that when driven with a 75 Ω source impedance, the device input will allow virtually all of the power to be transferred to the LNA.

The same tuner input will *not* offer good return loss when driven from a 50 Ω source impedance, like those of the typical VNA, signal generator, NF meter, etc. Directly connecting this perfectly matched TV tuner input to a 50 Ω VNA will yield an $|S11|$ measurement something close to -14 dB—with reflected power now one part in 25. So with this same 50 Ω VNA, how can we verify that the TV tuner input is as good as we say it is?

A matching circuit is required. It should have flat frequency response and the lowest insertion loss possible. The industry-standard answer to this is the MLP, a simple resistive network of Figure 1. The key feature of this network is that it transforms a 75 Ω DUT load impedance into 50 Ω for the measurement instrument and transforms the 50 Ω source impedance of the instrument to the native 75 Ω impedance of the DUT. In this way, reflections are removed, the response is flat, and the loss of the network is easily backed out of the measurement to get to the DUT. The math required to transform Z_{LOAD} into Z_{LOAD}' is straightforward. The resulting expression for $Z_{LOAD'}$ describes the cascaded impedance of the MLP and the DUT, as seen from the measurement port (R_{SOURCE}). Turning the equation around and solving for Z_{LOAD} in terms of Z_{LOAD}' offers a way to back out the effects of the MLP and to determine the true Z_{LOAD} from the measurement data taken at Z_{LOAD}'. The result is provided below:

$$Z_{LOAD} = \frac{Z_{LOAD'}(R_1 + R_2) - R_1 R_2}{R_2 - Z_{LOAD}'}$$

A sanity-check calculation proves sound. Assume we just made an impedance measurement of a 75 Ω resistor through the MLP. The assumption is that the VNA will measure $R_{LOAD}'=50$ Ω (infinite return loss), and we expect the math to tell us that this result came from a load resistor of 75 Ω. Let $R_{LOAD}'=50$ Ω, and we see that with $R_1=43.3$ Ω and $R_2=86.6$ Ω, we get $Z_{LOAD}=75$ Ω as expected.

This simple expression could be made more useful by breaking up the real and imaginary components and using a spreadsheet to do the calculations on the bench.

In a practical example, let's say we want to measure S21 of a cable/terrestrial TV LNA like Maxim's MAX3558 Quad LNA. The DUT is inserted in the test setup with MLPs at the input and output, as in Figure 2. Calibrate the VNA as usual, not including the MLPs in the cal. Connect port 1 to the 50 Ω side of one MLP, and connect the 75 Ω side to the LNA input. Do the same for one of the outputs and port 2 on the VNA.

Make the S21 (forward gain) measurement. The VNA will indicate a gain at 500 MHz near -5 dB. Back out the 12.0 dB insertion loss from the two MLPs and their connectors/adapters, and we see the LNA is providing a 75 Ω power gain of about 7 dB.

At frequencies above several hundred MHz, a PCB-mounted MLP built from 0402 resistors brings measurement accuracy into question. Parasitic effects break the assumption that this network is purely resistive—cases like this require a more complicated approach to the problem. One method would be to fully characterize the MLP, and use a Smith Chart to more accurately back out the effects of the matching circuit. Another solution is to use an inductor-based transformer to do the impedance transformation with much lower loss. RF transformers are described in terms of their impedance transformation ratio, not the turns ratio, so find one described as "75:50."

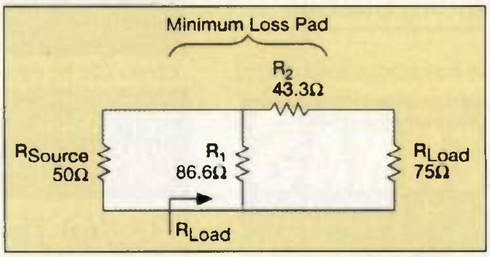

Figure 1. Minimum loss pad used to match a 75 V DUT to a 50 V test port. Insertion loss is 5.72 dB at low frequency.

For most general lab applications below 1 GHz, a PCB-mounted minimum loss pad built from 1 percent 0402 or similar resistors offers a quick and easy means to test a 75 Ω circuit with 50 Ω lab equipment. In most cases, the only correction factor required is the insertion loss of the MLP—5.7 dB plus any addition connectors. Difficult calculations or Smith Chart work is often not required to make basic [S]-Parameter measurements. RFD

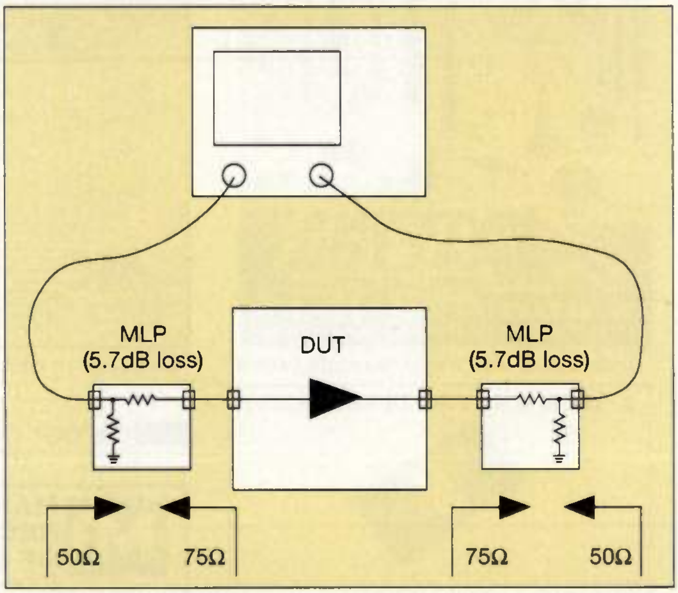

Figure2. Testing MAX3558 Quad cable/terrestrial LNA with a 50 V VNA, using two MLPs for impedance transformation.

ABOUT THE AUTHORS

James Liu and **Brian Whitaker** are wireless strategic applications engineers at Maxim Integrated Products, Sunnyvale, Calif.

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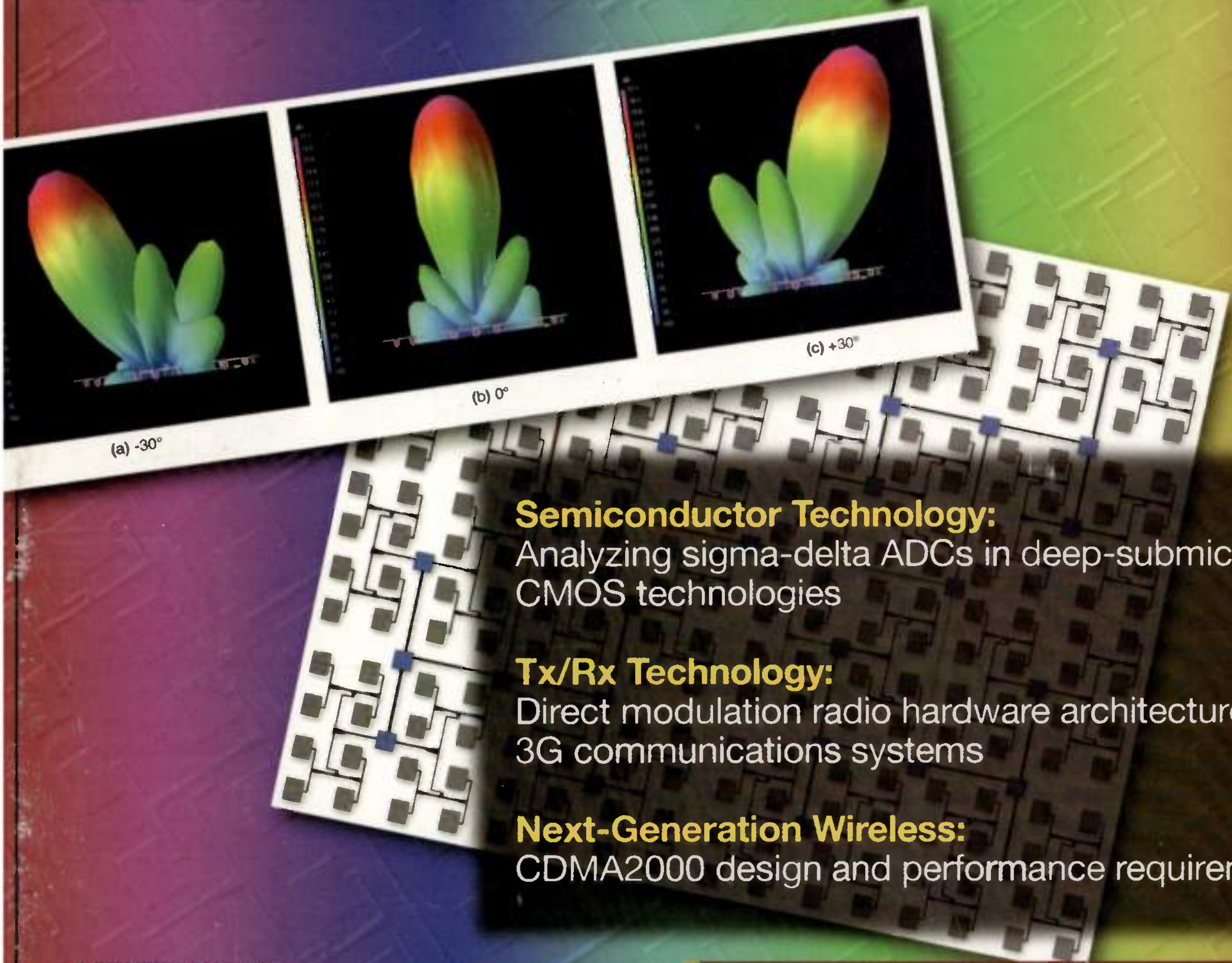

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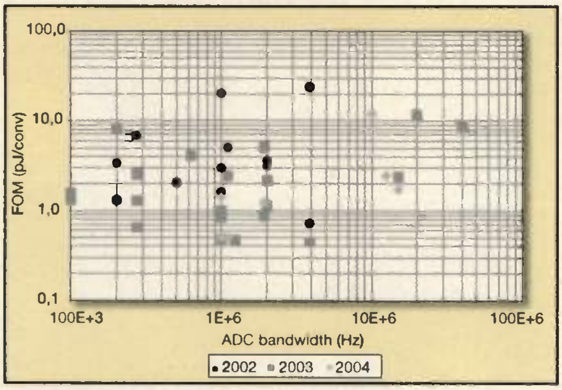

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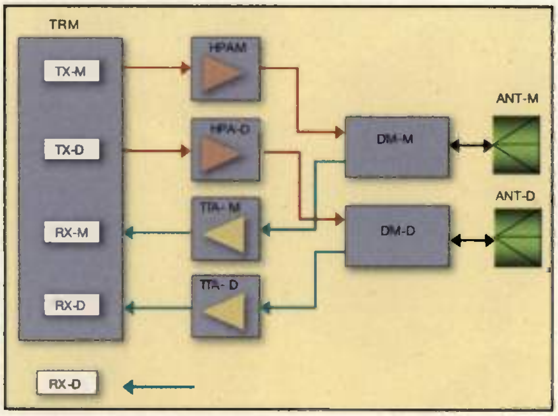

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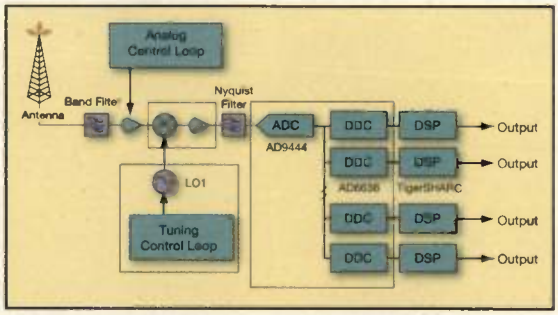

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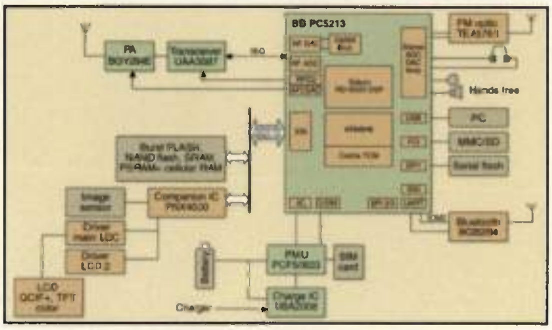

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VLF-105	DC-105	180	250	VLF-1525	DC-1525	1750	2040
VLF-120	DC-120	195	270	VLF-1575	DC-1575	1875	2175
VLF-225	DC-225	350	460	VLF-1700	DC-1700	2050	2375
VLF-320	DC-320	460	560	VLF-1800	DC-1800	2125	2425
VLF-400	DC-400	560	660	VLF-2250	DC-2250	2575	2850
VLF-490	DC-490	650	780	VLF-2500	DC-2500	3075	3675
VLF-530	DC-530	700	820	VLF-2600	DC-2600	3125	3750
VLF-575	DC-575	770	900	VLF-2750	DC-2750	3150	3875
VLF-630	DC-630	830	1000	VLF-2850	DC-2850	3300	4000
VLF-800	DC-800	1060	1275	VLF-3000	DC-3000	3600	4550
VLF-1000	DC-1000	1300	1550	VLF-5000	DC-5000	5580	6600
VLF-1200	DC-1200	1530	1865	VLF-6000	DC-6000	6800	8300
VLF-1400	DC-1400	1700	2015	VLF-6700	DC-6700	7600	9300
High Pass							
VHF-650	710-2490	650	480	VHF-1760	1900-5500	1760	1230
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VHF-880	950-3200	880	640	VHF-1910	2000-5200	1910	1400
VHF-1200	1220-4600	1180	940	VHF-2000	2260-6250	2000	1530
VHF-1300	1400-5000	1300	930	VHF-2100	2200-6000	2100	1530
VHF-1320	1400-5000	1320	1060	VHF-2275	2450-7000	2275	1770
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CMOS extends its reach to millimeter waves

Radio frequency (RF) ICs continue to benefit from advances in CMOS process technologies. Over the years, we have seen monolithic CMOS transceiver chips handling wider bandwidths to address the needs of cellular handsets. And packing more on-chip to offer system-on-a-chip (SoC) solutions for a variety of cellular and wireless bands. In reality, CMOS RF SoC chips are incorporating all the radio building blocks including the power amplifier, phase-locked loop (PLL) filter, and the antenna switch. Thus, CMOS continues to make strong inroads into the microwave territory, going well beyond 5 GHz. Now, the availability of unlicensed bands around 7 GHz and 60 GHz is motivating designers to make a giant leap and migrate deeper into this turf. These bands are intended to facilitate emerging applications like point-to-point wireless LANs, broadband Internet access, as well as automotive applications like short- (24 GHz) and long-range (77 GHz) radars for collision avoidance.

Operation in these frequency bands was once the exclusive domain of III-V-compound semiconductors, such as gallium arsenide (GaAs) and indium phosphide (InP). However, aggressive scaling and corresponding improvements in CMOS and silicon germanium (SiGe) technologies is making history. What may have been considered unthinkable a decade ago is now becoming a reality. And that was demonstrated at this month's IEEE International Solid-State Circuits Conference (ISSCC) in San Francisco, Calif. Researchers from around the world convened here to show that the CMOS and BiCMOS trend in millimeter wave ICs is real.

For the first time, scientists from National Taiwan University described two essential building blocks—a voltage-controlled oscillator and a broadband amplifier—for creating a robust 60 GHz radio in a conventional CMOS technology. In fact, this 0.13 µm-based push-push VCO is designed to cover a band of 110 GHz to 170 GHz. At 114 GHz out signal, it features a phase noise of -107.6 dBc/Hz at 10 MHz offset and power consumption of only 8.4 mW. Likewise, the broadband-cascaded multistage distributed amplifier was implemented in standard 90 nm CMOS technology. It achieves better than 7 dB gain with a bandwidth of 70 GHz, 10 dBm output power for 1dB compression at 30 GHz, 9.3 dBm IIP3 at 40 GHz and 6.4 dB average NF from 1 GHz to 25 GHz.

Similarly, researchers from UCLA displayed a 60 GHz direct-conversion CMOS receiver in 0.13µm CMOS consuming 9 mW from a 1.2 V supply. It provides a voltage gain of 28 dB with a noise figure of 12.5 dB. This direct-conversion receiver incorporates folded microstrip lines to create resonance at 60 GHz in a common-gate low-noise amplifier and active mixers.

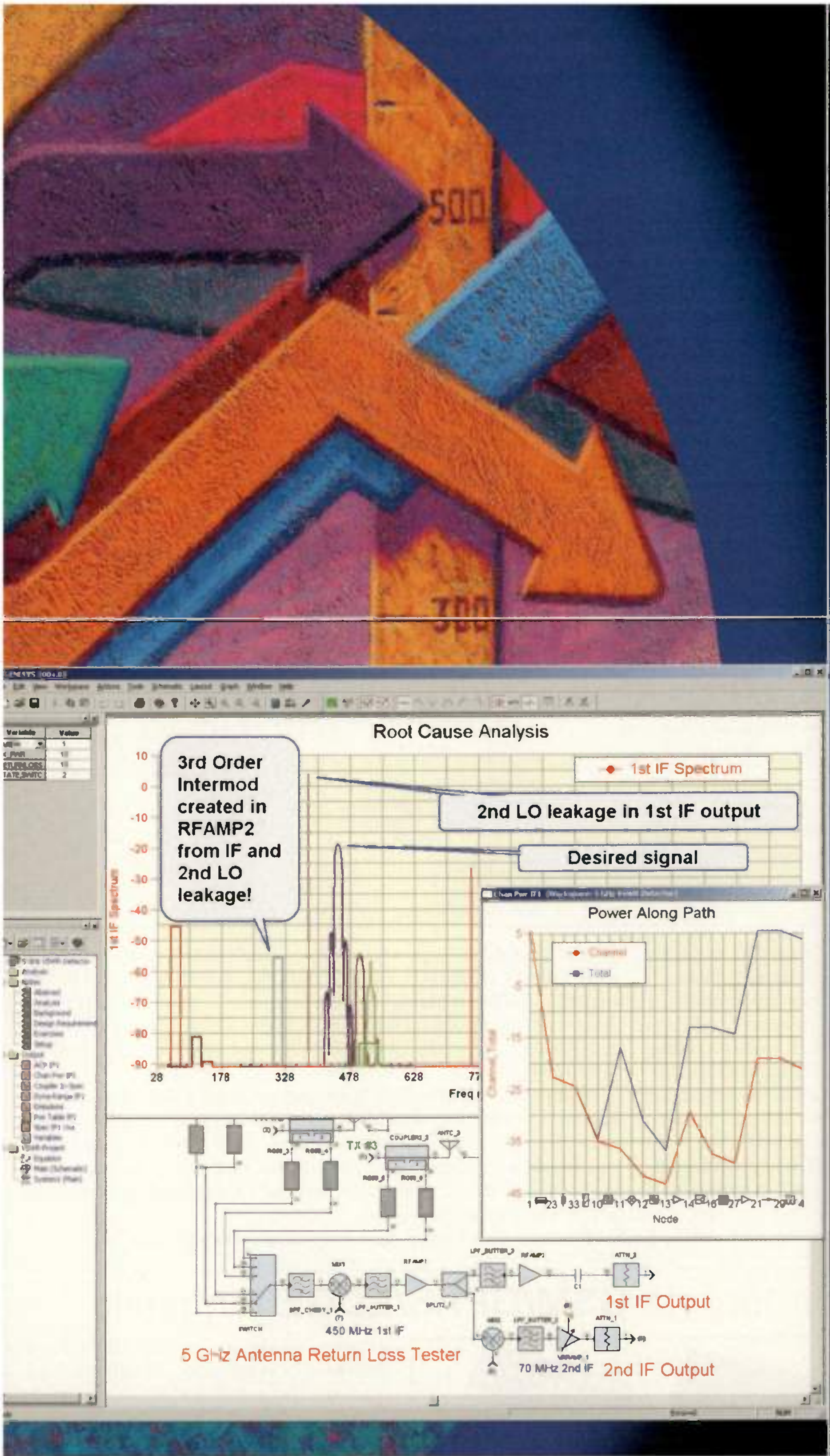
Toward that goal, researchers from California Institute of Technology in Pasadena, Calif. showed that to support 500 Mbps QPSK signal with bandwidth in excess of 400 MHz, a 24 GHz phased-array transmitter could be built in 0.18 µm CMOS. In essence, the California Institute developers presented a fully integrated four-element phased-array transmitter at 24 GHz with on-chip power amplifiers. It has a beam-forming resolution of 10°, a peak-to-null ratio of 23 dB, and isolation between paths of 28dB. Each CMOS PA can deliver up to +14 dBm into a 50 Ω load.

For 60 GHz wireless applications, researchers from Germany's IHP disclosed a BiCMOS PLL with a lock range of 53.3 GHz to 55.7 GHz. It operates from a 3 V supply except for a first divide-by-two stage, which requires a 5 V supply. Total power consumption is 895 mW. In a joint paper by University of Toronto, Canada, Delft University of Technology, The Netherlands and IBM, the developers demonstrated a three-stage 21 GHz to 26 GHz SiGe BiCMOS power amplfier with 21 dBm output power. The PAE at 24 GHz is shown to be greater than 12.5%.

These presentations indicate that CMOS will continue its march into the microwave and millimeter wave turf slowly but steadily. And, the performance will only get better with time. However, for critical functions, it will depend on SiGe technology.

Ashok Bindra

Ashok Bindra, Editorial Director



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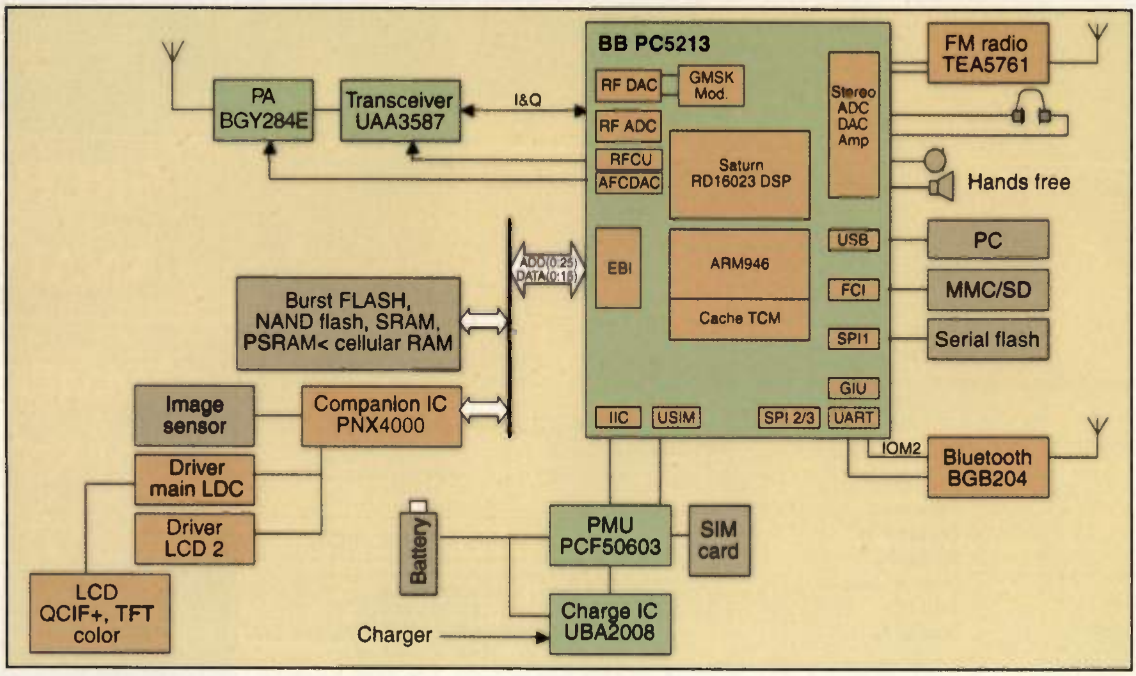
Cellular system solution powers Samsung's mobile handsets

Royal Philips Electronics has taken its EDGE cellular system solution to production. According to Philips, Nexperia cellular system solution 6100 family will be available in mobile handsets from Samsung, the first user of the 6100 system solution.

According to market research firm IDC, worldwide mobile phone shipments rose 23% between the third quarter of 2003 to the third quarter of 2004 to reach 164.1 million units. This growth is due in large part to replacement trends. EDGE has become an attractive high-speed wireless option for handset makers looking to advance the user experience for data applications, such as video streaming and real-time audio, from previous generations. The Nexperia cellular system solution allows manufacturers to deliver integrated, cost-effective handsets to market quickly while optimizing multimedia performance.



Validated for EDGE class 10, the 6110 solution supports data transfers with fast downlink speeds of up to 220 kbps. The inclusion of an ARM9 baseband and the LifeVibes multimedia suite makes it possible to stream 3GPP or MPEG4 files in 15 frames per second in quarter common image format (QCIF), making it ideal for TV on mobile. The solution also enables high-quality QCIF video recording at 15 frames per second without the need for an external coprocessor. The playback of MP3 and AAC audio files, as well as the generation of stereo polyphonic sounds, makes use of the fully integrated stereo capabilities. Built-in mono interference cancellation (MIC), a version of single-antenna interference cancellation (SAIC), improves voice quality, decreases the number of dropped calls and increases data transmission speeds.

The integrated LifeVibes software suite further supports certified, JTWI-compliant Java with JSR 135 Mobile Multimedia API (MMAPI), OMA DRM 1, revolutionary full-duplex speakerphone functionality including noise cancellation, and voice clarity features for the enhancement of speech intelligibility.

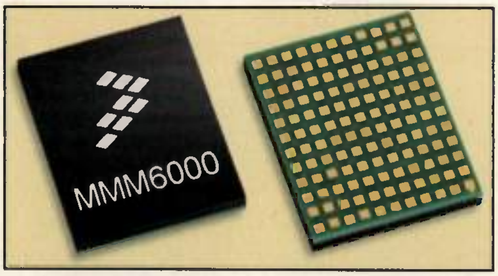
The 6100 cellular system solution comprises a quadband class 12-capable EDGE chipset, including cellular baseband (PCF5213), RF SiP (UAA3587), power amplifier (BGY284E), power management unit (PCF50603), integrated discretes and software. The bill of materials (BOM) is highly competitive due to component integration. Hardware extensions include the Nexperia Mobile Image Processor (PNX4000), FM radio (TEA5761UK) and Bluetooth 1.2 module (BGB204).

Philips' EDGE system solution has achieved full interoperability test (IOT) validation, which ensures reliability and compliance with networks. The solution comes with a developer's kit, providing customers with immediate access to the platform to develop their own applications, as well as a self-guided training pack and complete set of documentation.

For more information, visit www.semiconductors.philips.com.

Compact radio solution targets GSM/GPRS/EDGE terminals

Freescale Semiconductor has readied an RF subsystem that combines a transceiver (MMM6000) and front-end power amplifier module (MMM6027) to create a complete radio solution for GSM, GPRS and EDGE terminals. Offering antenna-to-bits functionality in a less than 250 mm² board space, it delivers a manufactured radio with low current and small size.



The transceiver is DigRF compliant, and provides direct conversion receive architecture that integrates the low-noise amplifiers (LNAs), as well as the receive and transmit voltage-controlled oscillators (VCOs). The transmit section is based on a polar modulation architecture with direct modulation of the VCO by a fractional-N synthesizer, and allows for a filter-free transmit lineup. An on-chip transmit/receive sequencer generates appropriate timing events for the transmitter calibration and the EDGE/GMSK transmit/receive burst; therefore, limiting the RF hardware dependency of the L1 engine software to an absolute minimum. The MMM6000 provides all of this functionality in a compact 9x11mm package.

The MMM6027 front-end power amplifier module integrates the rest of the radio subsystem. It provides power amplification, power coupling, power detection, low-pass filtering, output power control,

and antenna switching functions. The MMM6027 is specified to operate with both GMSK and 8PSK modulation schemes and is optimized to perform with the MMM6000 transceiver. Two modes of power control are supported with the MMM6027: bias control for GMSK modulation and input power control for 8PSK modulation. All of this functionality is provided in a small 8x8mm package.

Both devices are part of Freescale's i.275 Innovative Convergence platform solution, but due to the industry standard DigRF interface, this solution can interface with other digital basebands in the marketplace. In essence, the key benefits of this solution include:

- Complete antenna-to-bits functionality—no separate analog baseband required.
- Highest level of integration providing extremely compact 250 mm² board area.
- Polar-lite architecture provides complete closed loop control for manufacturability ease and extremely low current consumption.
- Complies with industry standard DigRF interface for ease of design.
- Embedded microcontroller to provide less dependency on Layer 1 software and simplifying software programming.

For more information, visit www.freescale.com/wireless.

Active mixers offer exceptional linearity

Two new RF active mixers from Linear Technology feature low power and high performance, making them suitable for wireless infrastructure transceiver and portable radio applications. The LT5525 and LT5526 consume only one-half the power of other high-performance mixers, while delivering excellent linearity to meet the requirements of cellular and wireless repeaters, pico-base stations, point-to-point wireless links and mobile radios.

The LT5526 features an input third order intercept (IIP3) of 16.5 dBm at 900 MHz, and a noise figure (NF) of 11 dB. This performance is complemented by a conversion gain of 0.6 dB. Moreover, the LT5526 requires only -5 dBm local oscillator (LO) drive, and its port-to-port LO leakage is exceptionally low at -65 dBm, reducing external filtering requirements. The LT5526 has fully differential inputs and outputs, and operates over a very wide bandwidth ranging from 100 kHz to 2 GHz. The device has the capability for use as either a downconverting mixer or as an upconverting mixer in many applications.

The LT5525 features an on-chip RF input transformer, and offers internal 50 Ω impedance matching at both the RF and the LO inputs. These inputs can be driven single-ended, without external impedance matching components, thus facilitating ease of use and reducing costs. The LT5525's IIP3 is 21 dBm at 900 MHz, and 17.6 dBm at 1.9 GHz. At 900 MHz, the NF is 14 dB and the conversion gain is -2.6 dB. The LT5525 requires only -5 dBm LO drive, and offers high port-to-port isolation.

Both the LT5525 and LT5526 operate from a single supply voltage, ranging from 3.6 V to 5.3 V. Typical operating current is 28 mA. The devices can operate at a supply voltage as low as 3 V with reduced linearity performance. These devices are offered in a 16-pin 4 mm x 4 mm surface-mount QFN package.

For more information, visit www.linear.com.

RF CMOS design kit creates on-chip spiral inductors

Semiconductor foundry service provider UMC and EDA software supplier Ansoft Corp. have developed a parameterized spiral inductor design kit based on full-wave simulation. The kit enables RF CMOS designers to create and simulate custom inductor geometries by directly linking Ansoft's HFSS™, Ansoft Designer™ and Nexxim™ with UMC's CMOS process parameters.

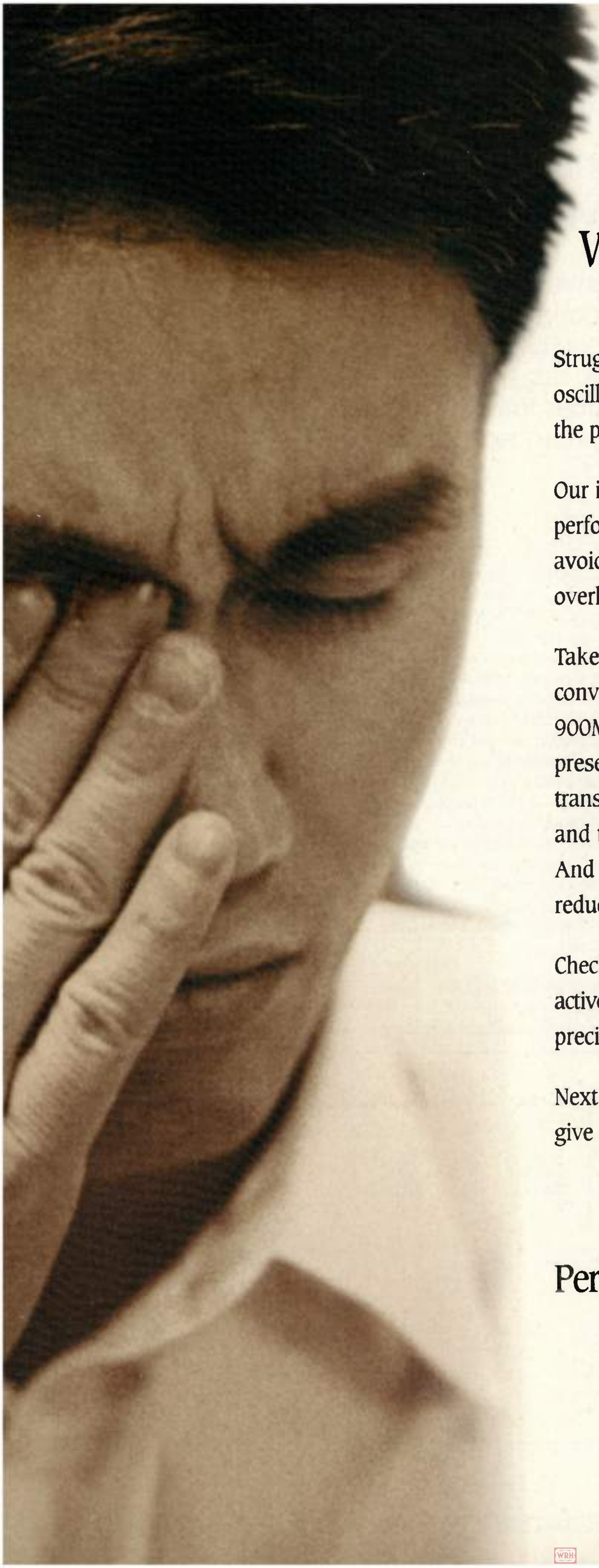
The spiral inductor kit is built upon UMC's electromagnetic design methodology (EMDM), which allows engineers to easily and accurately create any RF structure and gives designers the flexibility to innovate new geometries by editing parameters such as diameter, number of turns, width and spacing of traces from a dialog box in HFSS. In the kit are ready-to-solve, fully parameterized HFSS projects for circular, square, hexagonal and octagonal coils in the regular, stacked, transformer and balanced configurations with all vias and underpasses included. Using EMDM along with the spiral inductor design kit, users can compute the inductance and quality factor (Q) for spiral inductors, rapidly develop a custom library including proximity effects, and use them in circuit and system simulation. EMDM makes it practical to synthesize new inductors and rapidly back annotate this information into circuit schematics and standard layout tools, according to Ansoft.

"Our collaboration with Ansoft allows our customers to design, simulate, and optimize spiral inductors on silicon substrates, relieving a major bottleneck of the RF CMOS design flow. Furthermore, we encouraged Ansoft to provide a path to back annotate to backend layout tools, making it practical to innovate new designs and pass the results to standard layout tools," said Albert Yen, manager of UMC's mixed-mode and radio frequency technology program.

The UMC spiral design kit with document is available for the 0.15 μm and 0.18 μm RF CMOS process at no charge to UMC customers. According to the partners, individual spiral geometries have been simulated and validated vs. laboratory measurements. Together, the developers in Taiwan have simulated more than 300 spiral geometries to ensure design kit accuracy.

Furthermore, UMC has designed a 2.4 GHz low noise amplifier (LNA) circuit as a test case for RFIC design. The purpose of the project is to validate the models and design flow. The LNA layout was simulated using the new design kit spirals and full layout extraction was performed. Proximity effects for closely spaced spirals and the associated mutual coupling and substrate coupling was calculated using HFSS and results for simulations with and without proximity effects have been reported, showing that additional performance and design margin may be obtained using this modern EM-based RFIC design flow.

The release of the spiral inductor design kit is part of a larger collaboration between Ansoft and UMC to develop an EM-based design flow for RF CMOS circuits. The flow is being validated by design and simulation of a direct-conversion ultrawideband (UWB) radio. The goal is to demonstrate radio design, simulation and fabrication using Ansoft tools and UMC's foundry process. Ansoft and UMC are designing, fabricating and testing the circuits. The result will validate the EMDM design flow for high-performance radio circuits, validate UMC's process for UWB circuits, and provide a reference design for UMC and Ansoft customers, said the partners.



Analyzing sigma-delta ADCs in deep-submicron CMOS technologies

Sigma-delta (ΣΔ) analog-to-digital-converters are critical components in wireless transceivers. This study shows that a continuous-time, single-loop, single-bit ΣΔ ADC is suitable for wireless applications demanding less than 5 MHz conversion bandwidth (GSM Bluetooth, W-CDMA, etc.). On the other hand, for applications that require bandwidth conversion higher than 5 MHz (WLAN), the use of a CT single-loop, multibit ΣΔ ADC is recommended.

By Yann Le Guillou

In wireless systems, the desired channel must be selected in the presence of strong adjacent-channel interferers. This requires wideband analog-to-digital converters (ADC) that can digitize both the desired and adjacent-channel interferers, resulting in high-dynamic range (DR) requirements. Meanwhile, the advances in the CMOS process, combined with its economical advantages, is driving the integration of a complete wireless transceiver in baseline CMOS. The demand for greater throughput leads to digital modulation schemes of greater complexity combined with a greater signal band.

As a result, there is a strong trend to digitize wideband receivers. In this perspective, oversampled ΣΔ ADC modulators are suitable because the adjacent-channel interferers fall into the same band as the shaped quantization noise (Figure 1). Then, the same digital filter filters out both the quantization noise and interferers. Furthermore, ΣΔ ADCs provide an effective way to implement high-resolution ADCs without stringent matching requirements or calibration.

A block diagram of a ΣΔ ADC is shown in Figure 2. Basically, the digital output of the modulator contains a representation of the input signal plus a quantization noise that is shaped so that the noise is small in the band of interest and large elsewhere[1].

To gain more insight into the choice of a suitable ΣΔ ADC topology for a specific application, the 2002-2004 period was surveyed and analyzed through publications. All selected publications related to ΣΔ ADCs are based on measurement results and not on simulation. The former discussion is based on single loop and cascaded loop analysis, multibits and single-bit usage as well as continuous-time and discrete-time ΣΔ loop filter implementation.

ΣΔ ADC trend in 2002-2004

A common figure of merit (FOM) used to compare ADC design is calculated according to the formula:

$$FOM = \frac{Power}{2^{ENOB}.2.signalband} \qquad \text{Eq. 1}$$

where ENOB is the effective number of bits, calculated according to the peak signal-to-noise-and-distortion-ratio (SNDR):

$$ENOB = \frac{SNDR|_{dB} - 1{,}76}{6{,}02} \qquad \text{Eq. 2}$$

The FOM is expressed in picojoules per conversion (pJ/conv.)

The power number specified in the publications is questionable. Sometimes a paper includes reference source, onboard oscillator and biasing circuitry in addition to the ΣΔ ADC's core. This can be inaccurate, but because the ΣΔ ADC's power core is usually the dominant factor, the inaccuracy is believed to be small and will not significantly corrupt the FOM.

As illustrated in Figure 3, since 2003 there has been a trend to increase the bandwidth conversion. The main reason is the

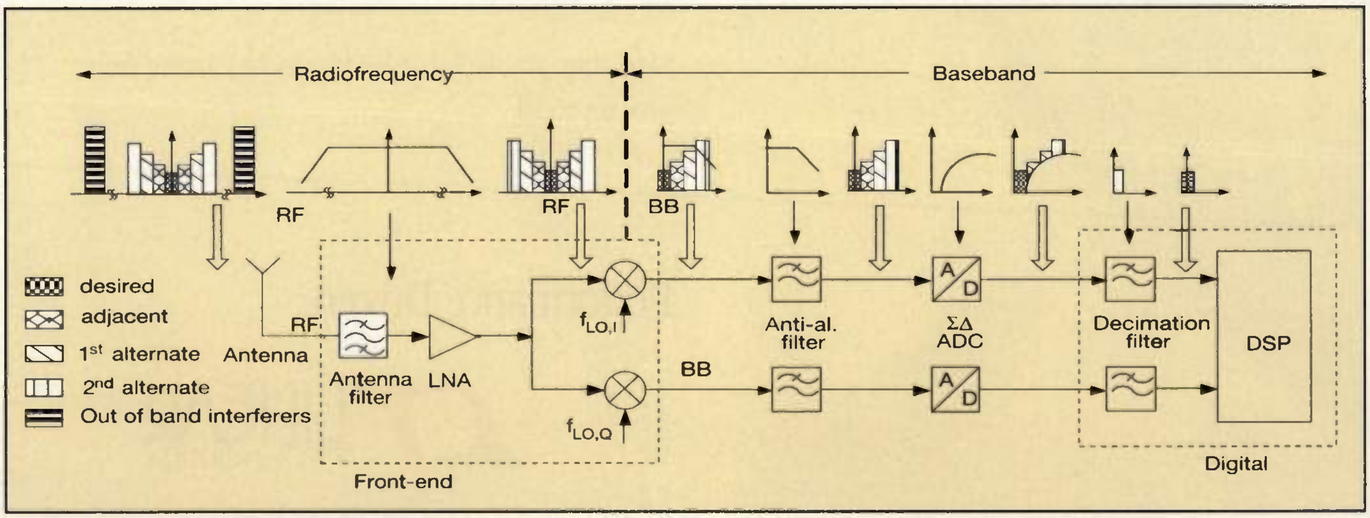


Figure 1. Direct conversion receiver with ΣΔ ADC.

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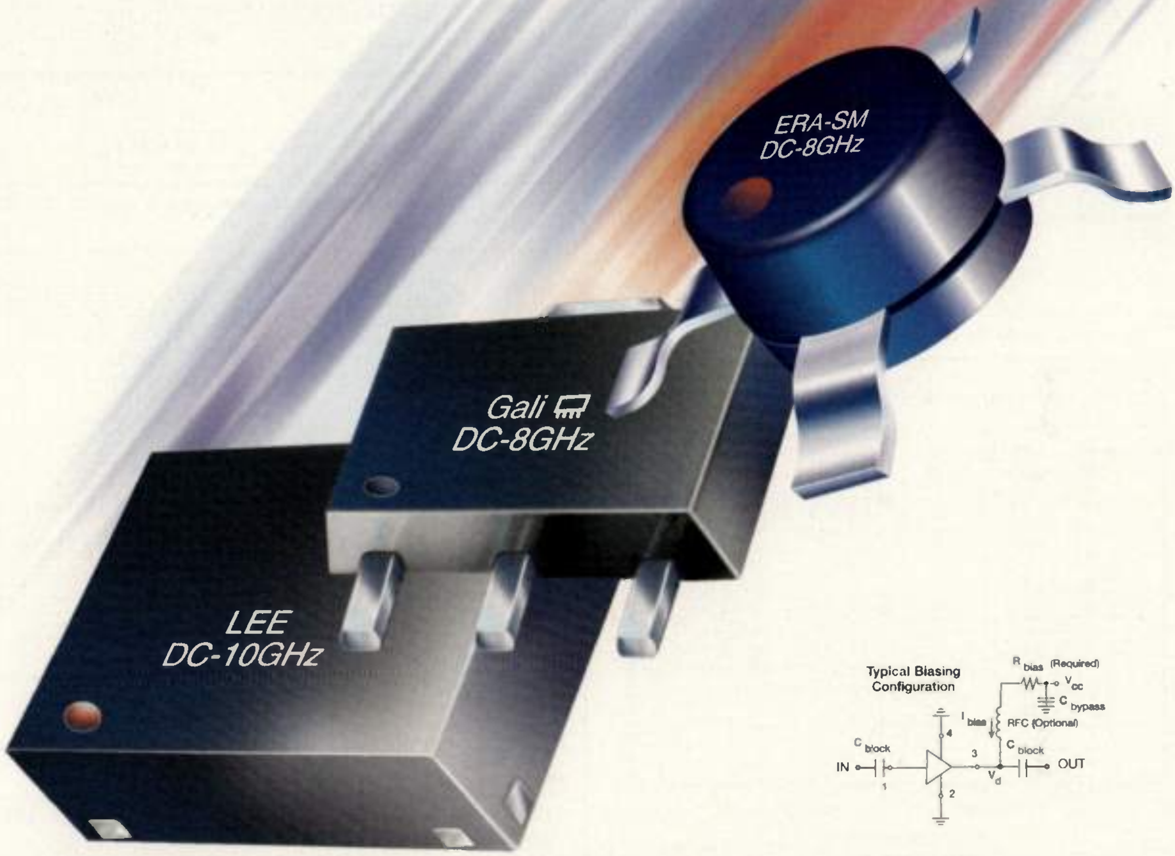

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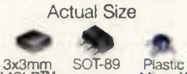

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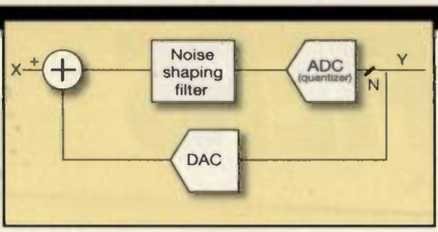


Figure 2. Sigma-delta ($\Sigma\Delta$) ADC block diagram.

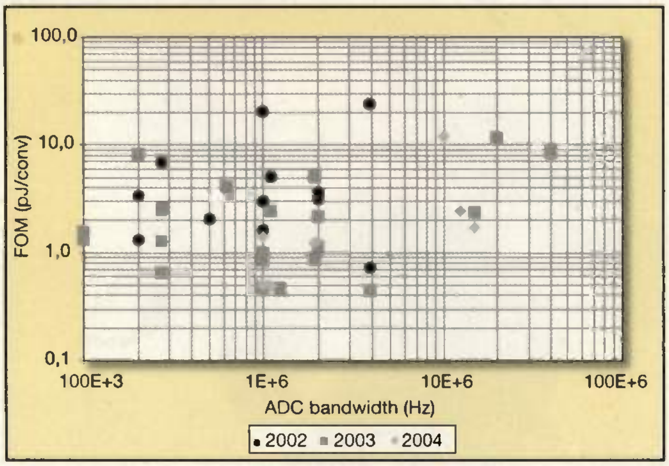


Figure 3. Surveying $\Sigma\Delta$ ADCs bandwidth limits.

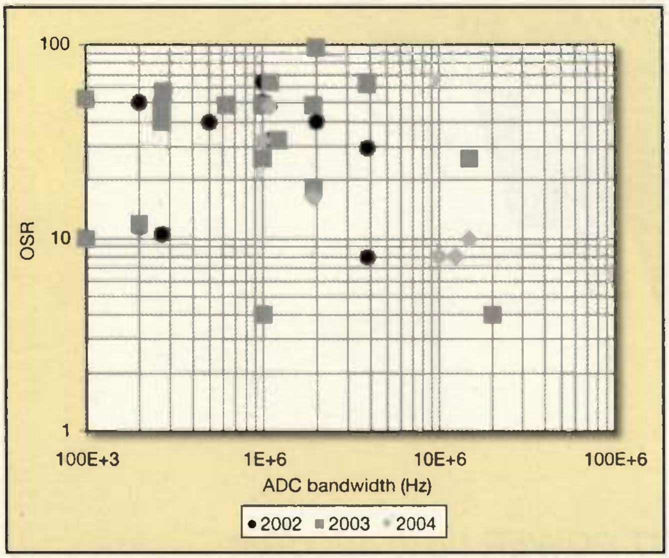


Figure 4. $\Sigma\Delta$ ADC OSR distribution as a function of bandwidth requirement from 2002 to 2004.

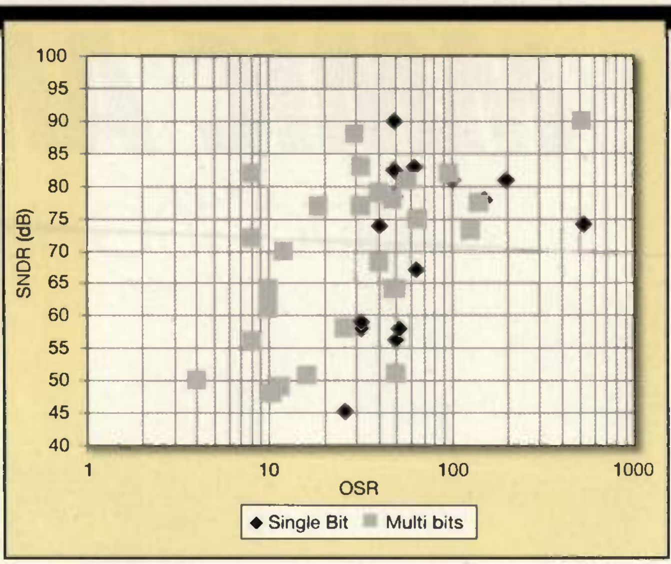


Figure 5. SNDR distribution of single bit and multibit $\Sigma\Delta$ ADC with respect to OSR.

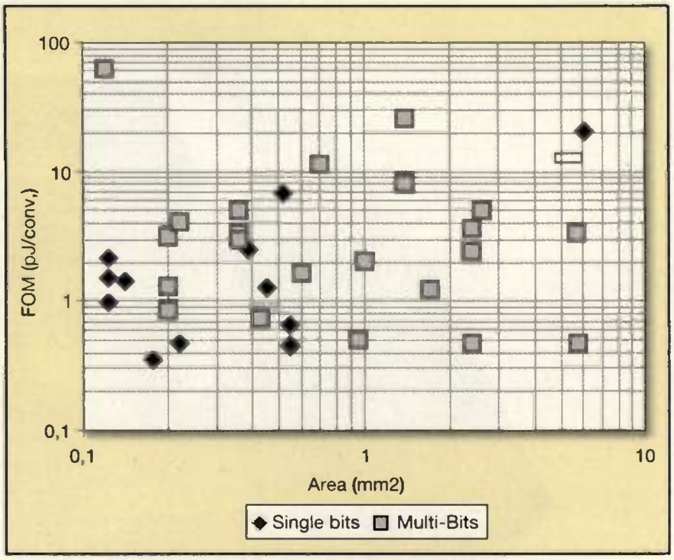


Figure 6. FOM distribution of single bit and multibit $\Sigma\Delta$ ADC with respect to area.

emergence of more signal-band, demanding wireless standards such as IEEE 802.11. Despite the increase of conversion bandwidth, the FOM remains between 1 and 10 pJ/conv. Thus, according to Equation 1, the power consumption has been scaled down as well. The increase of conversion bandwidth and the decrease of power are two contradictory design targets. The simultaneous fulfillment of these two targets is a result of advances in process technology and circuit topologies. In addition, Figure 3 shows that when the signal band is smaller than 10 MHz, then the $\Sigma\Delta$ modulator's FOM is limited by circuit noise—while it is mainly dominated by the technology performances when the signal band is larger than 10 MHz.

Typically, the sample frequency is limited to hundreds of megahertz for reasonable achievement and power consumption consideration in CMOS technologies. Consequently, as illustrated in Figure 4, an oversampling ratio (OSR) between 40 and 50 is acceptable for low (GSM) and moderate (Bluetooth and W-CDMA) bandwidth applications. However, for more demanding bandwidth applications such as WLAN, the OSR is typically lower than 10.

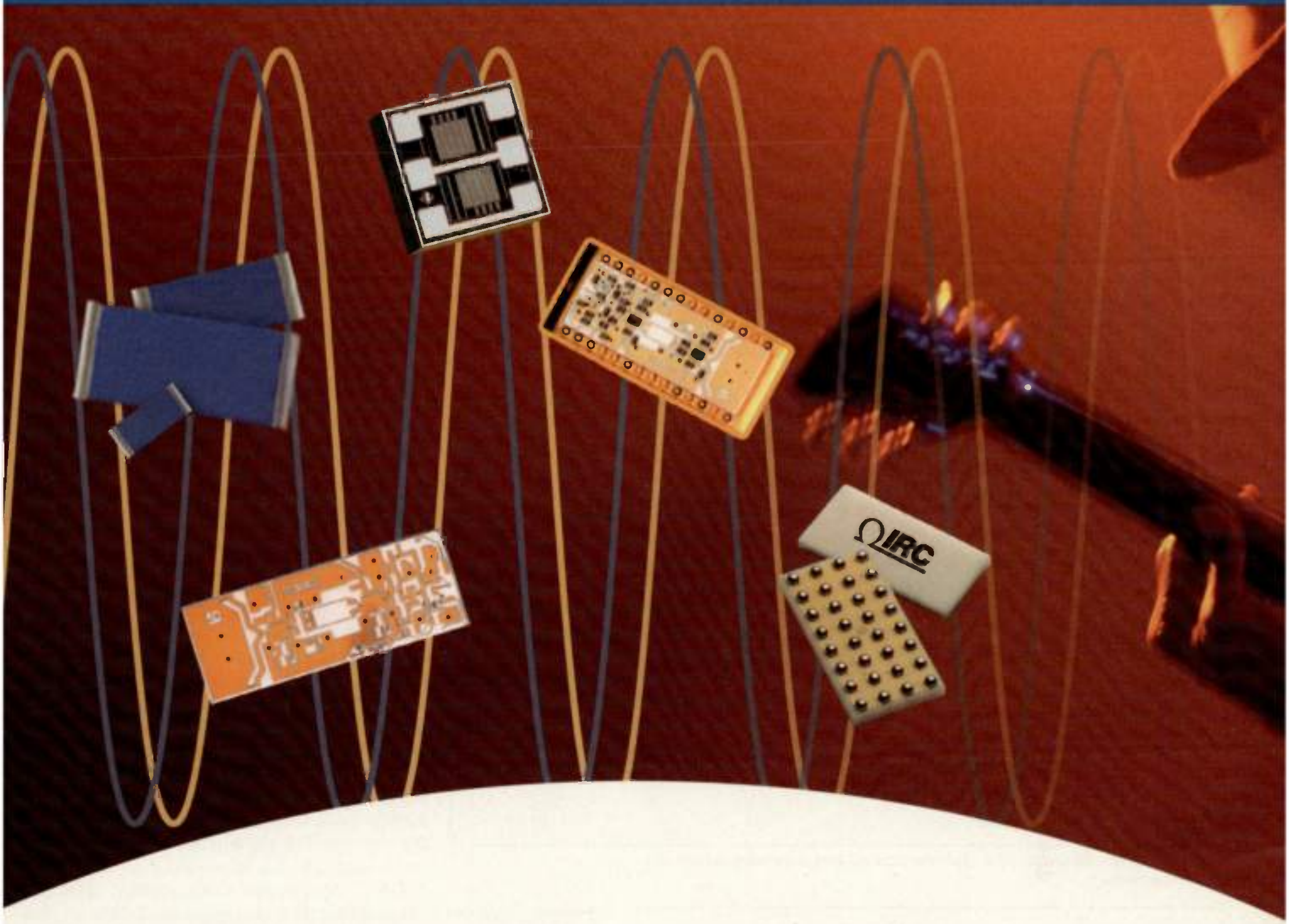
Multibits vs. single bit quantizer

The ADC resolution at a low OSR can be improved by using a higher-order loop filter, and/or by increasing the internal quantizer resolution. For single-bit, single-loop modulators, the integrator's gain must be reduced to preserve the loop stability. Therefore, simply increasing the loop filter order at a low OSR will result in a poor SNR improvement.

To achieve high resolution at a low OSR multibits internal quantization is widely used as illustrated in Figure 5. Since multibit quantizers have a more linear gain than single-bit quantizers, the stability of multibit, single-loop $\Sigma\Delta$ modulators is significantly improved. As a result, more aggressive noise transfer function can be designed, with the benefit of extra dynamic range for every additional bits n of [2]:

$$DR \propto 20.\log_{10}(2^n - 1)dB \qquad \text{Eq. 3}$$

Alternatively, increasing quantizer resolution enables us to use a lower noise-shaping filter for a given OSR. Unfortunately, it is necessary to double the number of comparators for each additional bit of quantizer resolution. Obviously, this costs silicon area as well as power dissipation and thus degrades the FOM for a given resolution as illustrated in Figure 6.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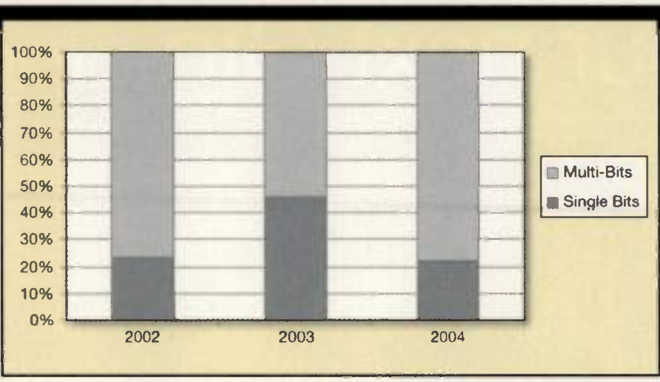

Figure. 7 Multibit and single-bit ΣΔ ADC distribution over 2002-2004 period

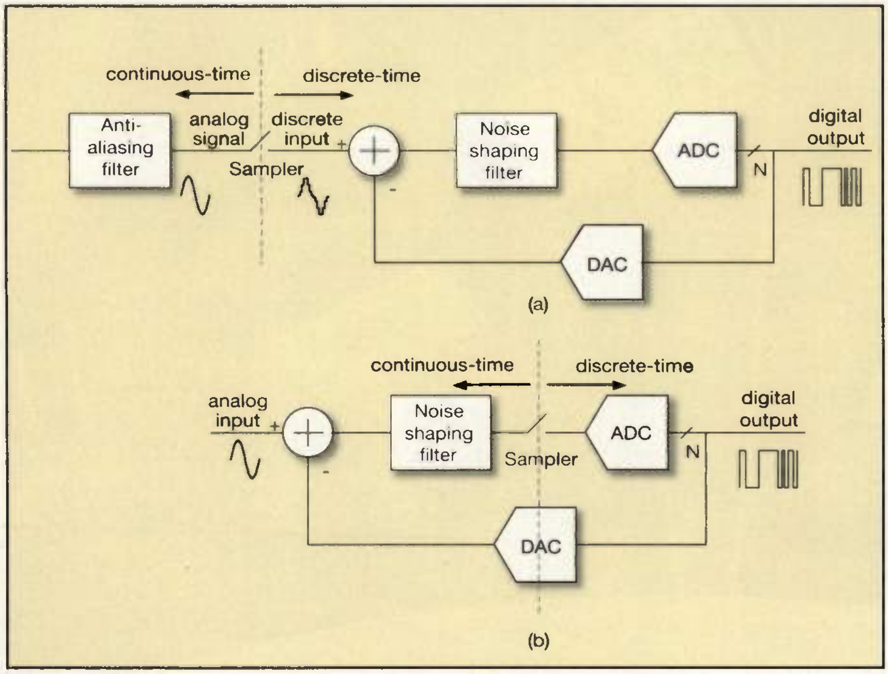

Figure 8. Block diagrams of a discrete-time (a) and continuous-time (b) ΣΔ modulator.

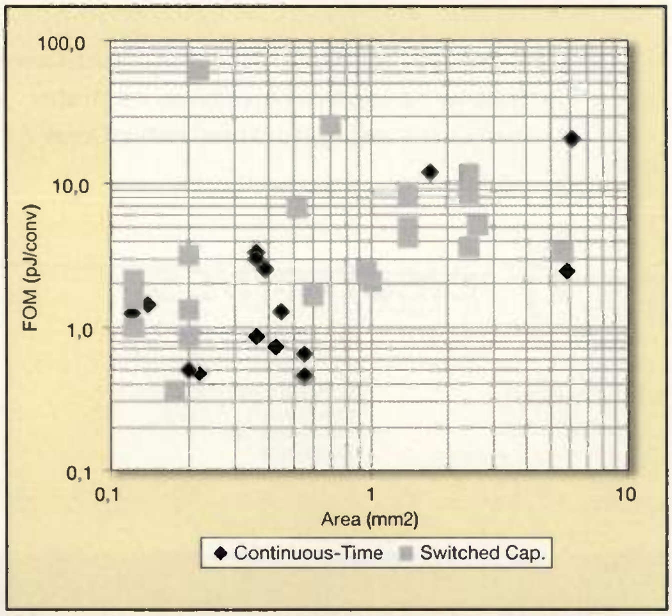

Figure 9. CT and DT ΣΔ ADC FOM distribution with respect to area.

In addition, multibit SD ADCs are sensitive to non-idealities such as mismatch in the feedback digital-to-analog converter (DAC), as these errors are added directly to the input signal and are thus not noise-shaped.

Nevertheless, deep-submicron technologies feature excellent matching characteristic as high as 11 bits or 12 bits of resolution. Hence, careful layout and design can fulfill linearity requirements of an internal-feedback DAC, provided that the ΣΔ ADC is lower than 12-bit resolution, which is typically the case for W-CDMA.

For a ΣΔ ADC's resolution that exceeds the matching possibilities of CMOS or Bi-CMOS, this problem must be addressed. The solution consists of using dynamic element matching (DEM). DEM converts the DAC element errors to high-frequency noise. Thereby, highly linear oversampling DACs can be built with only moderate matching requirements for the DAC element. DEM techniques have been developed since 1998, starting with randomization of the DAC elements [4]. The methods are continuously improved with respect to implementation efficiency and order of shaping. Since the presentation of [5] in 1995 and the disclosure of the ADC design in [6] in 1997, these techniques have been well established in the sigma delta design community, allowing efficient and robust implementation of sigma-delta ADC's with resolution of more than 14 bits and bandwidth beyond 1 MHz[7][8][9].

The digital complexity introduced by DEM—and more precisely the area and the power consumption penalty—is not believed significant since the mainstream CMOS process area is shrunk by L_{min}^2, i.e. 50%[10] every three years. In addition, the power consumption in digital CMOS circuits scales with the square of the supply voltage[11], that roughly decreases by 20% at each technology node[10]. As a result, the superior DR performances at a low OSR make multibit ΣΔ modulators attractive for WLAN applications. Consequently, it is not surprising that in 2004 multibit design represented 78% of the published ΣΔ modulators (see Figure 7).

However, a detailed look at Figures 5 and 6 shows that single bit should be preferred to multibit ΣΔ ADCs when the conversion bandwidth is lower than 5 MHz (GSM, Bluetooth, W-CDMA) because they achieved better FOM and are less silicon area-consuming.

Continuous-time vs. discrete-time

As illustrated in Figure 8, in an ΣΔ modulator loop, it is possible to build up the noise-shaping filter as a discrete-time (DT) or a continuous-time (CT) circuit.

DT ΣΔ modulators are implemented using switched-capacitor (SC) circuit techniques. In SC circuits, amplifiers with high gain-bandwidth product (GBW) satisfy the settling requirements. Typically, the GBW is seven times higher than the sampling frequency. By nature, CT ΣΔ modulators are not sensitive to settling behavior. As a result, CT ΣΔ modulators can potentially operate at higher clock frequency and/or with less power consumption. Note that in a CT ΣΔ modulator, the loop filter provides additional anti-aliasing filtering, which is beneficial when having to handle large interferers. In SC circuits, the in-band noise is bounded by the capacitor size. Consequently, and as illustrated in Figure 9, CT modulators have smaller FOM and are less silicon area-consuming than DT counterparts. Contrary to a CT modulator, in a DT modulator, large glitches appear

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LIFD-3010P-80BC	30	-80 to 0	±0.5	100	25
LIFD-6020P-80BC	60	-80 to 0	±0.5	50	25
LIFD-7030P-80BC	70	-80 to 0	±0.5	30	25
LIFD-16040-80BC	160	-80 to 0	±1.0	30	25
LIFD-300100-70BC	300	-70 to 0	±1.0	20	15

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LCPM-3010-70BC	30	-70 to 0	10	±0.5	±3°
LCPM-6020-70BC	60	-70 to 0	10	±0.5	±3°
LCPM-7030-70AC	70	-65 to 5	10	±0.5	±5°
LCPM-16040-70BC	160	-65 to 5	10	±1.0	±3°

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FMDM-30/6-3BC	30	6	1000	±3	120
FMDM-60/16-4BC	60	16	250	±3	90
FMDM-70/36-10AC	70	36	50	±2	50
FMDM-160/35-15BC	160	35	100	±2	30
FMDM-160/50-15AC	160	50	40	±2	25
FMDM-750/150-20BC	750	150	20	±3	20
FMDM-1000/300-50AC	1000	300	10	±5	7

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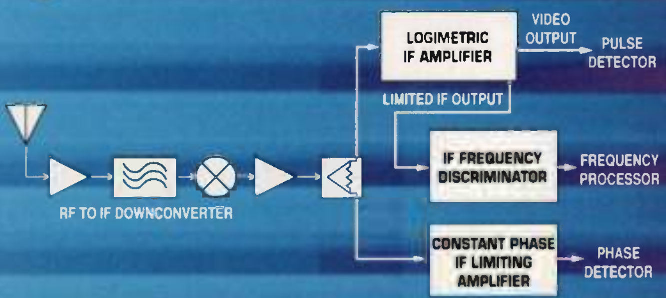
AGC-7-21.4/10AC	21.4	10	-70 to 0	10	±0.5
AGC-5-70/30AC	70	30	-50 to 0	-4	±0.5
AGC-7-160/30AC	160	30	-70 to 0	8	±1.5
AGC-7-300/400AC	300	400	-65 to 0	3	±1.0

For additional information, please contact Boris Benger at (631) 439-9502.



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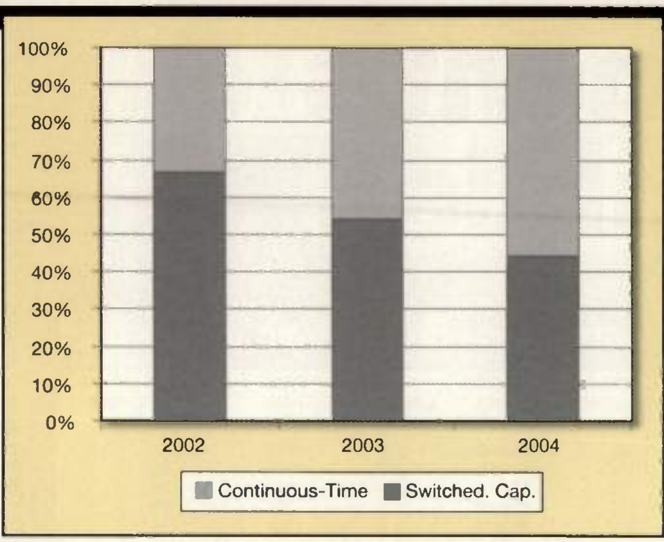

Figure 10. CT and DT ΣΔ ADC distribution over 2002-2004 period.

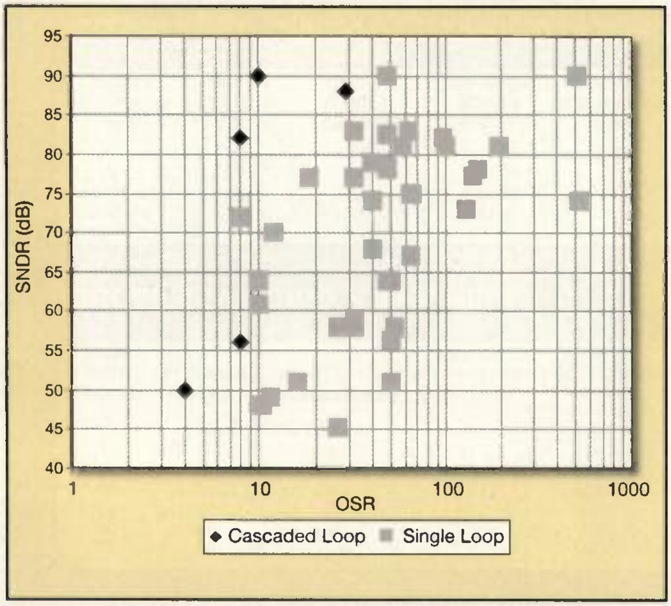

Figure 11. SNDR distribution of cascaded and single loops ΣΔ ADC with respect to OSR.

on the op-amp virtual ground node of op-amps-RC integrators due to switching transient. Therefore, a CT modulator achieves better linearity performance. When the ΣΔ modulator is integrated into a complete wireless transceiver in baseline CMOS, glitches generated in DT modulators can potentially couple to other critical blocks of the receiver, such as voltage-control oscillators (VCO), LNA and mixers, and can seriously degrade the receiver sensitivity. Today, CT modulators are preferred to DT modulators, whatever the application. This trend is illustrated in Figure 10, where continuous-time implementation represents 55% of the published ΣΔ modulators in 2004, whereas it was representing one-third in 2002 (see Figure 10).

However, it is well known that the clock jitter of the feedback DAC is critical in the SNR degradation of a CT single-bit feedback DAC. Some solutions should exist to circumvent the jitter effect. For example, going to an N-bits ΣΔ ADC will reduce the quantization step by 2^N-1. Consequently, the DAC charge transfer fluctuation per clock period due to jitter will also decrease by 2^N-1. However, this solution is silicon area-consuming.

A more interesting solution consists of implementing an SC DAC while keeping a continuous-time loop filter. As demonstrated in [12], a return-to-zero clock scheme configuration associated with a settling

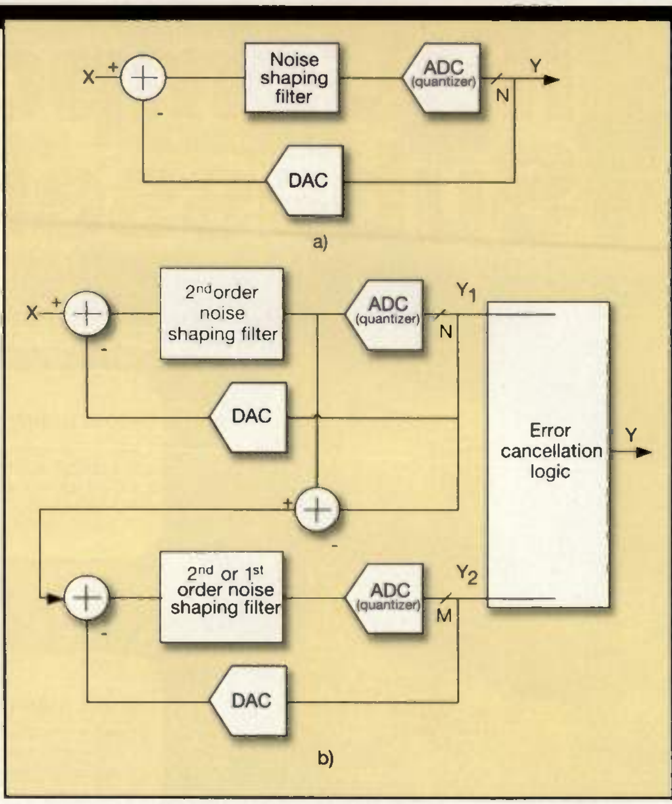

Figure 12. Single loop (a) and cascaded loop (b) ΣΔ modulator.

time constant of the SC DAC eight times smaller than the clock period enables the decrease of jitter sensitivity by 4 dB. This latter solution is preferred for wireless applications that do not require more than 5 MHz conversion bandwidth because it optimally trades off the CT and DT advantages

In a DT modulator, the time constant's variations of the noise-shaping filter achieve excellent matching since they rely on capacitor ratio. However, this is not the case in CT modulators where the time constant's variation is between 25% to 30% due to R and C spreads. This can seriously degrade the SNR performances. Nevertheless, some on-chip biasing techniques that consist of compensating the temperature dependence of hole or electron mobility in silicon enables the design of accurate time constraints despite process and temperature variations[12]. Another solution widely used for op-amp RC integrator time constant tuning makes use of switchable capacitor arrays [13]. In this case, a calibrator is used to measure the fabricated RC product with a reference clock frequency. From this, a digital code word is generated, which is used to select elements in programmable arrays of capacitors that form the tuning elements of the filter integrators. Both solutions are robust and do not introduce too much circuit complexity.

Single loop vs. cascaded loop

Cascaded loops, also called MASH structure, are popular for high-dynamic range applications at low OSR (see Figure 11) because they facilitate higher-order ΣΔ loops that do not suffer from stability problems.

However, cascaded modulators rely on good matching properties between analog and digital transfer functions. When the quantization noise of the first-stage quantizer is not fully cancelled in the digital error cancellation logic bloc (see Figure 12b) due to a non-ideal matching, leakage noise appears at the output of the modulator, rapidly decreasing the SNR performance. Typically, the leakage noise depends on analog circuit non-idealities, such as insufficient op-amp dc gain and gain factors spread over the temperature and the process variations. Moreover, cascaded loops are characterized by an


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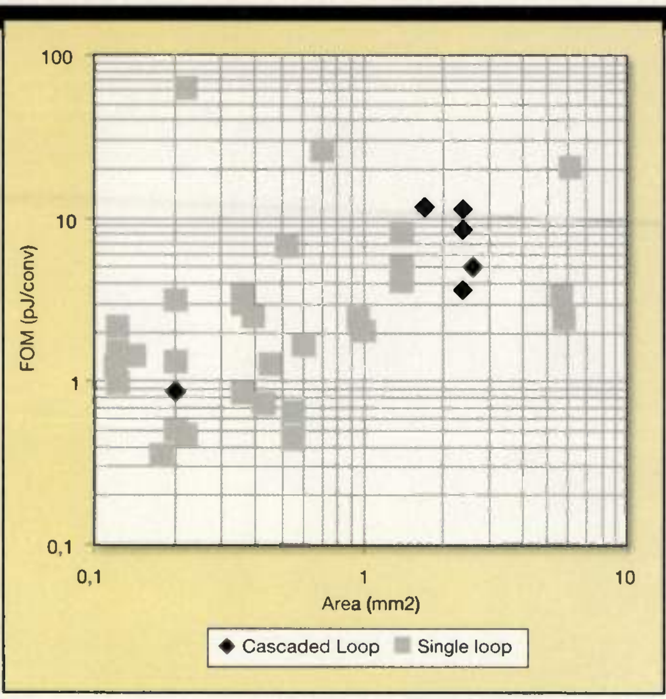

Figure 13. Cascaded and single loops ΣΔ ADC FOM distribution with respect to area.

inherent loss in dynamic range due to internal signal scaling. These two factors impose constraints on the minimum size of analog components to the detriment of the parasitic capacitance and associated current consumption. Therefore, as illustrated in Figure 13, cascaded loops have larger FOM and are more silicon area-consuming than single-loop structures.

As illustrated in Figure 14, the cascaded loop fraction of published ΣΔ modulators in the 2002-2004 period is decreasing by 2% every year and represents only 11% in 2004. One of the main reasons is the difficulty in designing op-amps with high dc gain in deep-submicron technologies.

Conclusion

The published ΣΔ ADCs for wireless applications have been reviewed for the 2002-2004 period. Since 2003, there has been a strong trend to increase the bandwidth conversion while keeping reasonable clock frequency. This means that the OSR tends to decrease. As a result, multibit ΣΔ loops are preferred for bandwidth-demanding applications such as WLAN. However, single-bit ΣΔ modulators are recommended for wireless applications that require less than 5 MHz conversion bandwidth because they offer better trade-offs for power, area and circuit complexity. Moreover CT ΣΔ modulators are suited for a low-cost integration because they provide anti-aliasing filtering without silicon-area penalty and can potentially operate with less power consumption than DT implementation. At least, single loop topology is preferable in low-voltage, low-power designs because it is less sensitive to analog circuit non-idealities, such as insufficient op-amp dc gain that tends to decrease at each CMOS technology node. RFD

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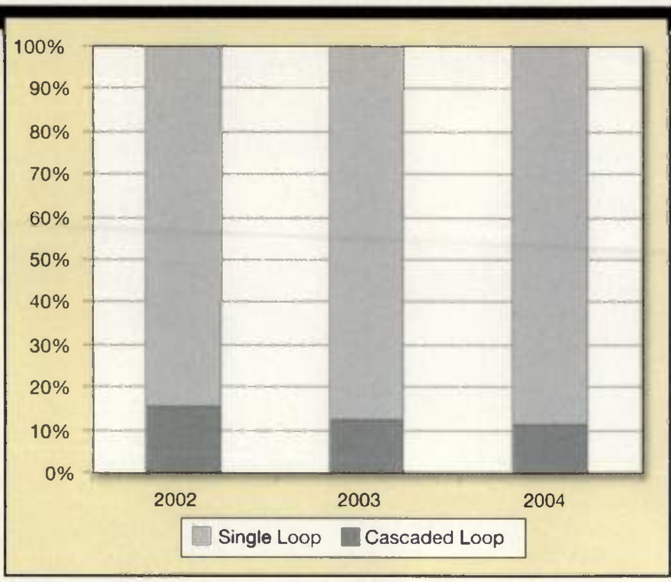

Figure 14. Single loop and cascaded loop ΣΔ ADC distribution over 2002-2004 period.

ABOUT THE AUTHOR

Yann Le Guillou is an innovation engineer for Philips Semiconductors' Innovation Centre for RF technologies. He joined Philips Semiconductors Caen, France in 1999 and has been involved in various design project including multiband transceivers fo-0-r GSM/EDGE, fractional-N synthesizers, and Sigma-Delta analog-to-digital converters. Le Guillou is a graduate of Ecole Superieure d'Electricité (Supélec), Paris, France, with a degree in electrical engineering. He is finishing his PhD related to the integration of Sigma-Delta ADCs in cellular transceivers.

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Direct modulation radio hardware architectures for 3G communications systems

The base station transceiver system (BTS) is one of the most expensive network elements in the wireless network infrastructure and directly impacts the cost of the overall network design and deployment. The requirement for increased capacity and higher data rates will inevitably lead to increased cell deployments. To maintain costs at an acceptable level, telecommunications equipment manufacturers (TEMs) will continue to seek more cost-effective solutions to their infrastructure hardware.

By Patrick Naraine

The cost of the BTS is affected by its key functional elements that include antenna, radio transceiver, signal processing subsystems, and support and control hardware and software. An example of a BTS configuration is shown in Figure 1. The BTS uses main branch modules and diversity branch modules. Diversity receiver systems are common in 2G systems, and the 3G specifications[1] also define options for transmitter diversity. As shown in Figure 1, the transmit/receive module (TRM) will contain duplicate transmit and receive sections. For wide area cell sites the receivers will generally be connected to the antennas via a duplexer module (DM) and tower top assembly (TTA). The TTA consists of a low noise amplifier (LNA), which is essential to compensate for cable losses from the antenna to the TRM. The TTA may be equipped with bypass switches (for low noise amplifier protection) and pre-selector filter. On the transmit side, driver power amplifiers (PAs) within the TRM will generally feed high-power amplifiers (HPAs) before passing through the duplexer and antenna.

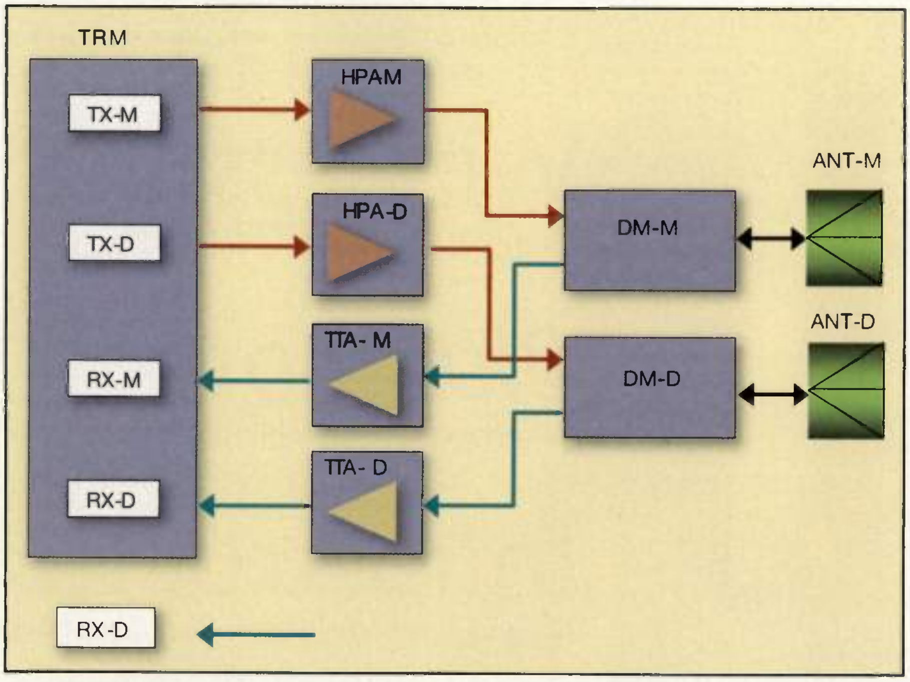

Figure 1. Base station architecture for diversity receive and transmit paths.

This article focuses on the receiver and transmitter modules (typically four modules per TRM per sector) and discusses methods of reducing their cost without compromising system performance. The article will focus on the direct conversion receiver (DCR) and direct conversion transmitter (DCT) architecture, since these architectures provide significant costs and size advantages without sacrificing performance. Compared to handset designers, base station designers have been slow in adapting DCR and DCT technologies, but increased pressures for costs and size saving, and continued improved performance will help to accelerate the conversion of base station design.

Table 1 Examples of ACLR1 budget for a WCDMA direct conversion transmitter.

Exp.	Baseband	Modulator	Driver PA	HPA	Tx Total	Comments
1	-65	-60	-53	-46	-45	Less demands on baseband modulator and driver PA linearity.However, HPA needs more backing off from P1 db point, and could lead to lower power efficiency.
2	-69	-63	-55	-45.5	-45	Medium linearity demands on the modulator and driver PA. Good compromise solution.
3	-77	-72	-60	-45.1	-45	Places more stringent linearity demands on the baseband, modulator and driver PA.

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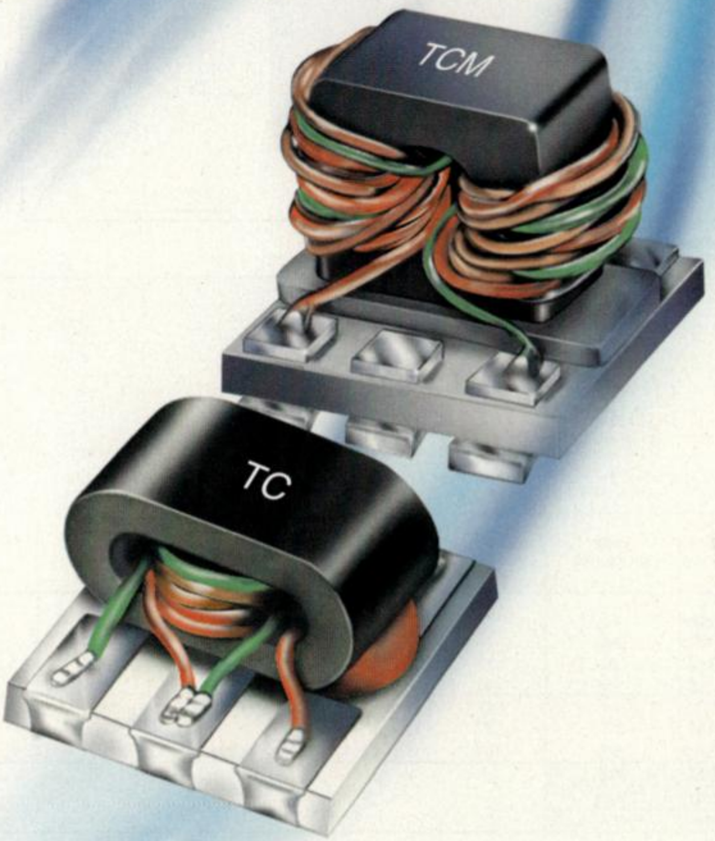

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TC1-1T	1A	0.4-500	1-100	1.19
TC1-1	1C	1.5-500	5-350	1.19
TC1-15	1C	800-1500	800-1500	1.29
TC1.5-1	1.5D	.5-2200	2-1100	1.59
TC1-1-13M	1G	4.5-3000	4.5-1000	.99
TC2-1T	2A	3-300	3-300	1.29
TC3-1T	3A	5-300	5-300	1.29
TC4-1T	4A	.5-300	1,5-100	1.19
TC4-1W	4A	3-800	10-100	1.19
TC4-14	4A	200-1400	800-1100	1.29
TC8-1	8A	2-500	10-100	1.19
TC9-1	9A	2-200	5-40	1.29
TC16-1T	16A	20-300	50-150	1.59
TC4-11	50/12.5D	2-1100	5-700	1.59
TC9-1-75	75/8D	0.3-475	0.9-370	1.59

LEADS Plastic Base (actual size)

MODEL	Ω Ratio & Config.	Freq. (MHz)	Ins. Loss◆ 1dB (MHz)	Price $ea. (qty. 100)
TCM1-1	1C	1.5-500	5-350	.99
TCML1-11	1G	600-1100	700-1000	1.09
TCML1-19	1G	800-1900	900-1400	1.09
TCM2-1T	2A	3-300	3-300	1.09
TCM3-1T	3A	2-500	5-300	1.09
TTCM4-4	4B	0.5-400	5-100	1.29
TCM4-1W	4A	3-800	10-100	.99
TCM4-6T	4A	1.5-600	3-350	1.19
TCM4-14	4A	200-1400	800-1000	1.09
TCM4-19	4H	10-1900	30-700	1.09
TCM4-25	4H	500-2500	750-1200	1.09
TCM8-1	8A	2-500	10-100	.99
TCM9-1	9A	2-280	5-100	1.19

Dimensions (LxW): TC .15" x .15" TCM .15" x .16" ◆Referenced to midband loss.

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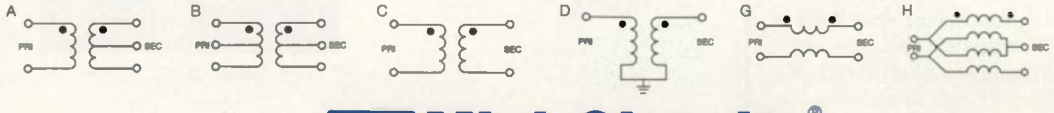

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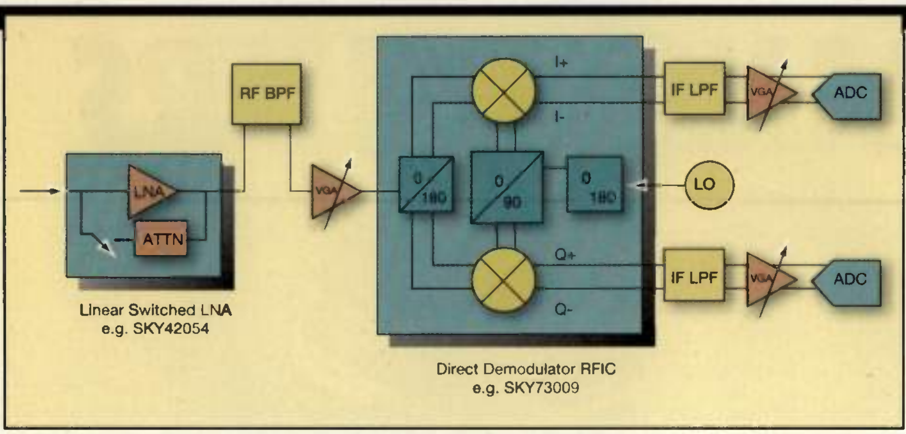
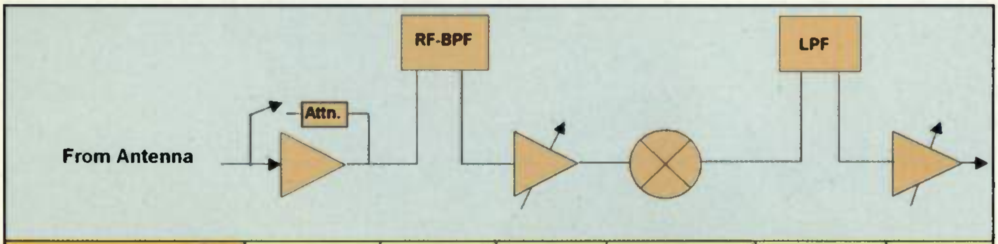


Figure 2. Direct conversion receiver architecture.



Stage: Device: Example Part No.	1 LNA SKY42054	2 RF Filter	3 AGC	4 De-Mod SKY73009	5 LPF	6 IF-AGC
Gain (dB):	14	-3	20	-8	-3	50
NF (dB):	2.6	3	5	16	3	5
IP_{1dB} (dBm):	6	33	10	13	33	-40
IIP3 (dBm):	16	43	20	25	43	-50
Cas Gain (dB):	14	11	31	23	20	70
Cas NF (dB):	2.6	2.7	3.1	3.1	3.2	3.2
Cas IIP3 (dBm)	16.0	15.8	8.2	-6.2	-6.2	-7.1
Total Rcv Gain (dB)	70.0					
Total Noise Figure (dB)	3.2					
Total IIP3 (dBm)	-7.1					

Figure 3. Example of RF performance budget for 3G direct conversion receiver.

standards. Examples of WCDMA base stations will be given, however, similar analysis could be adopted for the other two 3G systems.

3G direct conversion receiver

The DCR has become increasingly acceptable for applications requiring multiband flexible operation, with size, power and cost constraints. The DCR is able to meet these stringent requirements since it requires fewer components (mixer, filter and amplifiers) leading to lower power, size and cost. The DCR converts the RF signal directly to baseband, eliminating the need for various mixers, image-rejection filters and amplifiers. Figure 2 shows an example of a DCR, which could be adapted for use in 3G base stations. The first element in the receiver chain is the low noise amplifier (LNA). The main function of the LNA is to minimize the overall receiver noise figure. A switched LNA is proposed to handle large input signal dynamic range without driving the rest of the receiver chain into compression. An RF bandpass filter (BPF) follows the LNA. The BPF provides attenuation to any out-of-band interfering signals, and spurious signals generated by the receiver. The filtered input signal is level controlled using a variable gain amplifier (VGA) or a variable attenuator and amplifier combination. The signal is then sent to a demodulator RF integrated circuit (RFIC) where it is demodulated into in-phase (I) and quadrature-phase (Q) baseband signals. The demodulator signal lines are implemented as differential pairs to provide high immunity to noise. I and Q signals from the demodulator are then low-pass filtered (LPF) and amplified by a low-frequency automatic gain control (AGC). The low frequency AGC is critical to maintaining I and Q signal levels within the input operating range of the analog-to-digital converter (ADC).

The receiver (Figure 2) provides a relatively simple architecture with low parts counts. However, the main design challenge, which must be addressed for any DCR, is direct current (dc) offset[2].

The mixing of a local oscillator (LO) signal, which has leaked or coupled to the RF input, with the incoming RF signal, can generate significant dc voltage levels within the receiver. Dc offset can be minimized by maximizing the LO to RF isolation and through harmonic mixers[3]. It is critical to closely match the amplitude and phase response of mixers and amplifiers in the demodulator I-Q paths. A silicon bipolar complementary metal oxide semiconductor (Si-BiCMOS) demodulator, SKY73009 has been designed and tested to achieve amplitude and phase balance within 0.3 dB and 1°, respectively. This demodulator also provides a superior LO-to-RF isolation of 50 dB, essential to maintaining low dc offset signals within the receiver. Systems using lower-performance demodulators, will require more sophisticated and expensive dc-calibration techniques[4].

The DCR shown in Figure 3 uses a switched LNA (part of a front-end receiver RFIC) and the Si-BiCMOS demodulator RFIC described above. With these key components, the RF analysis shows a resulting cascaded noise figure of 3.2 dB and cascaded gain of 70 dB. For most 3G base station

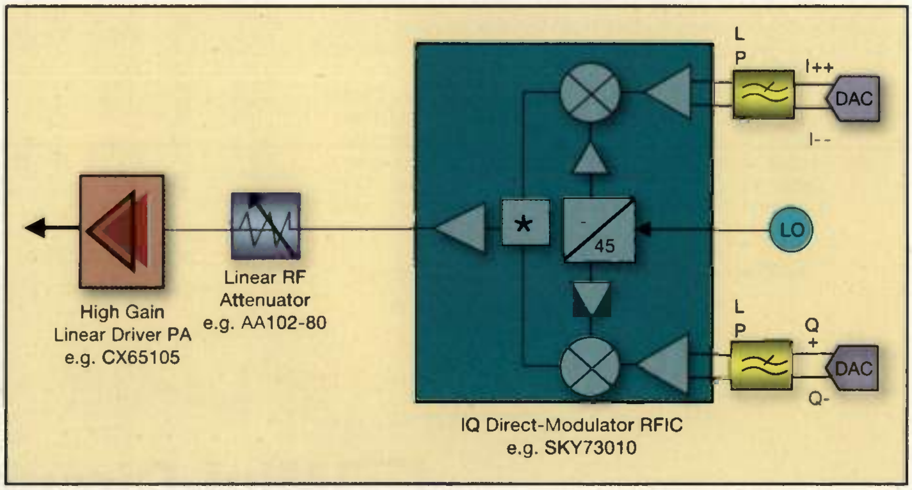


Figure 4. Direct conversion transmitter architecture.

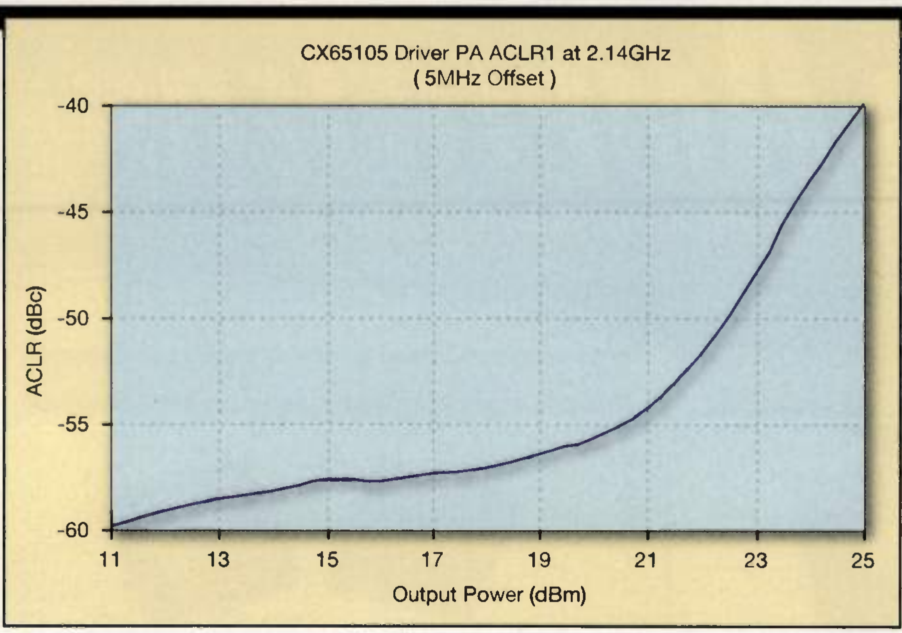


Figure 5. Example of driver PA ACLR1 response using WCDMA test signal 1.

implementations (depending on noise figure of TTA and cable losses), a cascaded noise figure of less than 5 dB is acceptable, so the receiver architecture proposed above can provide an additional system margin of 1.9 dB.

3G direct conversion transmitter

Base station transmit diversity is allowed in the 3GPP specifications[1]. With proper alignment (to reduce cross-coupling and to increase branch isolation) and timing synchronization, transmitter diversity can provide improvements to the system signal to noise ratio (SNR) and mitigate multipath and signal fading effects. However, diversity will add to systems implementation cost, size and power consumption. The use of low-cost RFIC components and direct conversion architectures will help mitigate these negative impacts of diversity transmitters.

The direct upconversion transmit architecture shown in Figure 4 is becoming more common due to its low part count and power consumption.

With direct conversion architectures, DACs provide the transmit I-Q signals. I-Q signals from the DACs can be low-pass filtered to remove any aliasing, harmonics and spurs introduced by the DACs. The filtered I-Q signals can then be directly modulated and upconverted to RF frequency using a direct quadrature modulator. The modulator must have adequate amplitude and phase matching between the I-Q branches to minimize corruption of the modulated signal information or error vector magnitude (EVM). The total allowed EVM for a WCDMA base station transmitter is 17.5% using quadrature phase shift keying (QPSK) modulated signals. Systems engineer will allocate most of the EVM systems budget to the HPAs (to improve power efficiency). Therefore, little or no EVM contribution will be expected from the modulator. Direct quadrature modulators are available with amplitude and phase imbalance less than 0.3 dB and 3° respectively, and should contribute less than 5% to the EVM budget.

Signal leakage from LO to RF port needs to be minimized, since in most direct conversion systems the LO and RF input signals are at the same frequency and RF filtering after the modulator will be ineffective in suppressing any LO-RF leakage. Today, direct quadrature modulator RFICs can be obtained with LO to RF isolation of greater than 50 dBc, second-order input intercept point (IIP2) of greater than 60 dBm and NF level of less than -153 dBm/Hz. These RF performance values ensure the modulator will not significantly impact the spurious emissions of the overall transmitter chain.

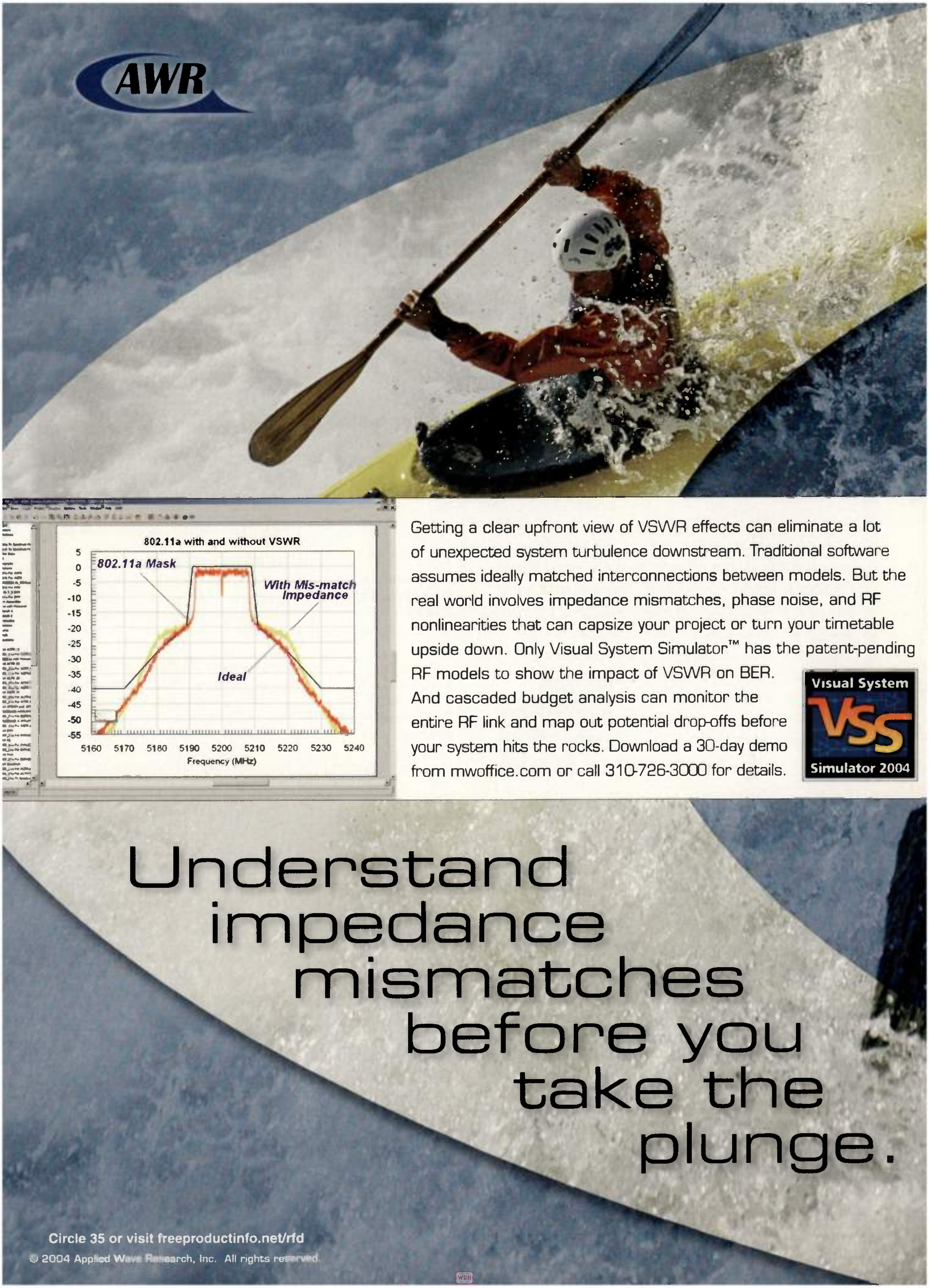
The upconverted signal can be level controlled to compensate for part-to-part, diversity-to-main branch and temperature gain variations. The variable attenuator will need to handle input power levels of -10 dBm to +10 dBm (typical output levels from modulator), without contributing to the system nonlinearity. The AA102-80 variable attenuator will operate in most common wireless bands (0.5 GHz to 2.5 GHz) and has an input third-order product intercept point (IP3) of more than +45 dBm. The settable attenuation range is more than 30 dB with 1 dB step size.

After level control the transmit signal may then be amplified by a linear driver before being fed to the final high-power amplifier (HPA). The driver needs to have sufficient high gain (typically 20 dB to 35 dB) and linearity to suit the overall system requirements. With higher gain driver amplifiers, the number of required stages on the HPA can be reduced, resulting in significant cost and power efficiency savings. High-performance linear drivers are available with RF gain of more than 25 dB and output third-order product intercept point (OIP3) of more than +40 dBm.

A key requirement for any WCDMA transmitter is the adjacent-channel leakage power ratio (ACLR). The 3G specifications[1] call for ACLR1 (one channel or 5 MHz frequency offset) of less than -45 dBc and ACLR2 (two channels or 10 MHz offset) of less than -50 dBc. ACLR measurements are typically conducted with the defined test model 1, which comprises 64 dedicated physical

Stage: / Device: / Example Part.	1 LPF	2 Modulator SKY73010	3 Attenuator AA102	4 Driver PA CX65105	5 HPA
Gain (dB):	-1	28	-5	24	25
NF (dB):	1	10	5	6	8
IP_{1dB} (dBm):	41	-25	25	6	25
IIP3 (dBm):	51	-15	44	21	35
OP_{1dB} (dBm):	40	3	30	30	50
OIP3 (dBm):	50	13	49	45	60
ACLR1 (dBc) at Output Power:	-75	-65	-75	-57	-47
Cascaded Gain (dB):	-1	27	22	46	71
Cascaded NF (dB):	1	11.0	11.0	11.0	11.0
Cascaded ACLR1(dBc):	-75.0	-63.9	-63.9	-56.1	-46.5
Input Power Level (dBm):	-30.0				
Total Gain (dB):	71				
Total Output Power (dBm):	41.0				
Total NF (dB):	11.0				
Total ACLR1(dBc):	-46.5				

Figure 6. Example of RF performance budget for 3G direct conversion transmitter.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channel (DPCH) signals at 30 ksps and spreading factor of 128. The power levels and timings for the 64 DPCH signals are randomly distributed to simulate a realistic signal environment. The test signal power level timings are defined in the 3G spec document[1].

The ACLR budget must be carefully distributed among the various non-linear sections of the transmitter chain. Examples of how an ACLR budget could be distributed amongst the main transmitter sections are shown in Table 1.

The typical ACLR performance of a high gain linear driver amplifier is shown in Figure 5.

3G transmitted signals will have peak-to-average ratio (PAR) in excess of 10 dB when measured at the 0.01% cumulative complementary distribution (CCD) point. The high PAR of the 3G signals place stringent linearity demands on the power amplifiers. The ACLR Figure 5 shows the amplifier will typically require 8 dB back off from its P1dB point to achieve an ACLR1 of -45 dBc. The ACLR vs. output power response is linear with a slope of approximately 3:1 between -45 dBc and -55 dBc. However, at lower ACLR points the noise floor of the amplifier becomes important and limits the ACLR rejection level. For ACLR budget examples shown in Table 1, the linear driver can provide output power of 22 dBm, 20.5 dBm and 11 dBm for examples 1, 2 and 3 respectively. Example 3 is the least preferred configuration since it places stringent demands on baseband components, modulator and driver PA, and will lower the available output power from these sections, and in turn place a higher demand on the gain requirements of the HPA.

Figure 6 shows an example of a transmitter chain block and level, which could be used to achieve total ACLR1 of greater than the standard specification of -45 dBc[1] with linear output power of +41 dBm. The transmitter ACLR1 budget closely reflects the allocation shown for Example 2 in Table 1. RFD

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Patrick Naraine holds a BSEE and MSEE from the McMaster University of Hamilton, Ontario, Canada. He was technical payload manager of Canada's first remote sensing satellite built for the Canadian Space Agency in 1996. He then joined Nortel Networks where he was in charge of RF system designs for AMPS, TDMA and EDGE base station transceivers. From 1999 to 2002 he worked at AT&T Wireless on the system design, testing and deployment of the first U.S. commercial fixed wireless voice and high-speed Internet system. Now he works on system designs for RFICs, MMICs and PAMs at Skyworks Solutions Inc. -Contact him at patrick.naraine@skyworksinc.com.

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MODEL NUMBER	GAIN (dB)	P1dB (dBm)	OIP3 (dBm)	GAIN (dB)	P1dB (dBm)	OIP3 (dBm)
		1 GHz			2 GHz	
ECG001	21	12.5	25	19	12.5	26
ECG004	16	13.5	28	16	13	27
ECG006	15	15.5	32	14	15	30
ECG002	20	15.5	29	19	15	29
SCG002	21	15.5	29	20	15	29
ECG005	22	18	34	21.5	17.5	32
ECG040	15	18.5	35	14	18	34.5
ECG055	19.5	18	34	19	18	32
EC1119	15	18.5	36	13.5	18.5	33
ECG050	19	19	34	17	18.5	31
EC1019	20	19	34	18	19.5	31
EC1078	20	21	37	17	20	33
ECG003	20	24	39	19	23	36
ECG008	15	24	40	14.5	23	37

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CDMA2000 design and performance requirements

Various heterodyne solutions have continued to flourish through incarnations of transceiver designs, each generation adding new control loops or components to improve the architectures. While communications standards such as CDMA2000 provide challenging performance requirements, the trends are for deep cost reduction, highly integrated solutions and flexibility.

By Bill Schofield and Brad Brannon

To reduce the costs of code-division, multiple-access systems, circuit stages are being integrated or reduced wherever possible, with an eye toward digitizing as soon as possible. This has resulted in strong interest in architectures such as direct conversion for high-performance receivers.

Direct conversion offers simplicity and a minimum of components consisting of an RF gain stage, in-phase and quadrature (IQ) demodulator and digitizing circuitry. This technique, in use for user equipment, is still a few years away from the provider side. In the meantime, intermediate frequency (IF) sampling is the preferred architecture, offering a compromise between performance and cost.

In addition to lowering cost, another benefit of IF sampling is that it offers great flexibility. The two main categories of analog filters are a band filter and a Nyquist filter. The band filter selects the band of interest, and the Nyquist filter prevents aliasing in the following analog to digital converter (ADC).

Beyond this, filters are implemented digitally in digital downconverters (DDC), such as Analog Devices' AD6636. In addition to downconversion, a DDC also provides programmable channel filtering and other critical functions such as gain control and power estimation. Because DDCs are digital and fully programmable, they can be changed to meet the needs of the standards currently being received. Although this is software-selectable, the manufacturer determines these characteristics as part of the firmware that is installed during the assembly and test process. Because it can be determined during manufacturing, a single basic design may be used for several deployments, reducing the costs associated with inventory, assembly and test.

While IF sampling and direct conversion are often used to reduce direct and indirect product costs, they do not come without technical challenges. Most notable is that with fewer stages, the required gain and filtering must take place with fewer devices, resulting in the need for devices with a lower noise figure (NF) and higher third-order intercept point (IP3) performance. Fortunately, as the demands for performance have increased, semiconductor device performance has met the challenge and enabled the reduced topologies.

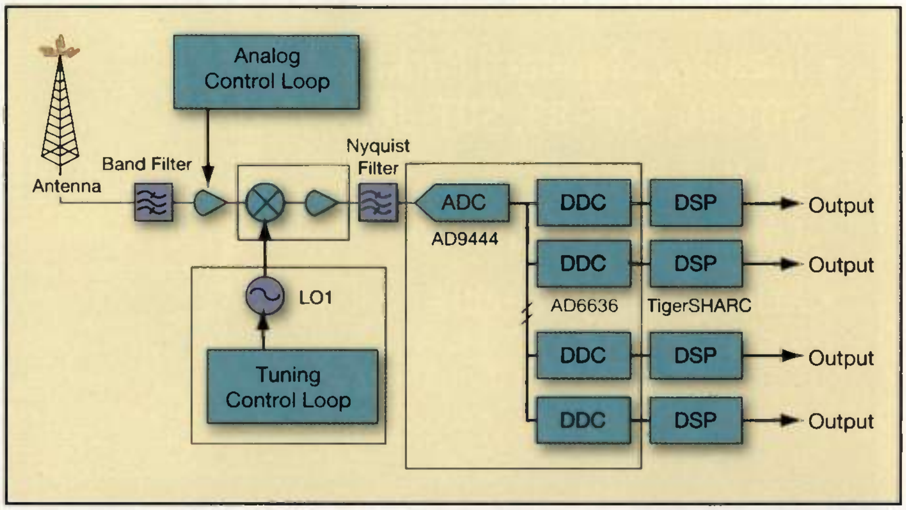

Figure 1. Multicarrier Rx signal path.

Table 1. Signal levels of RF front end.

	Antenna Level	Nyquist Filter Input (Mixer Output)	ADC Level
Thermal Noise	-174 dBm/Hz	-126 dBm	-136 dBm/Hz
Desired Signal	-117 dBm/1.25 Mhz or -178 dBm/Hz	-142 dBm	-152 dBm/Hz
NB Blocker	-30 dBm	+15 dBm	+5 dBm

Looking at a multicarrier application in CDMA2000, the minimum performance is defined by a sensitivity of -117 dBm/1.25 MHz. In addition, narrowband signals 87 dB or larger must also be tolerated in some bands. This places the largest signal somewhere around -30 dBm. While these are minimum specifications, many receivers typically outperform these numbers by many decibels. Because many of these systems are multicarrier, the large signals cannot be allowed to desensitize the receiver to the smaller desired signals. Therefore, gain control must be minimal or absent. Therefore, it is desirable for a fixed gain to be used. As shown in Figure 1, the ADC is the last analog element in the chain. Given a full scale on the ADC of about +5 dBm, the maximum conversion gain can be estimated. If the largest signal at the antenna is -30 dBm and the ADC can only tolerate a +5 dBm signal, this limits the gain to 35 dB, maximum. Current, state-of-the-art devices can produce this gain with an NF of about 3 dB.

Is this enough gain? To determine the answer, it is necessary to ensure that the noise floor of the front end (everything up to the ADC) is greater than the input-referred

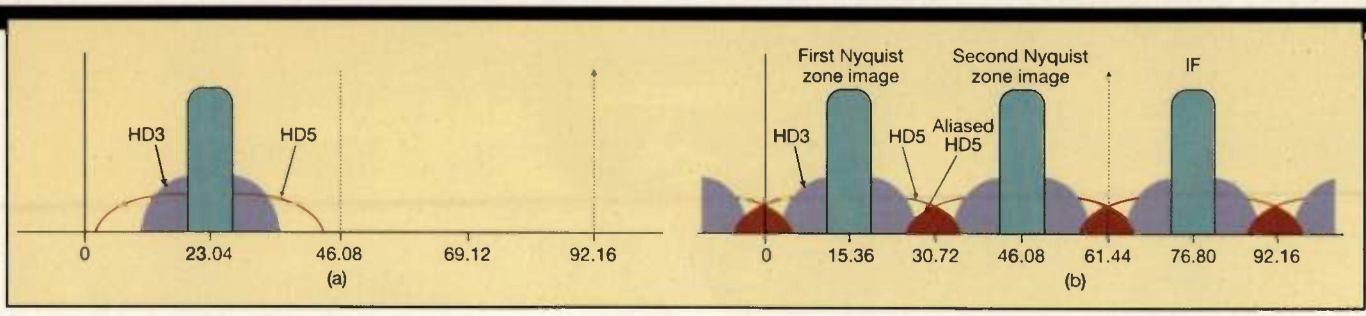

Figure 2. PA linearization observation path sampling.

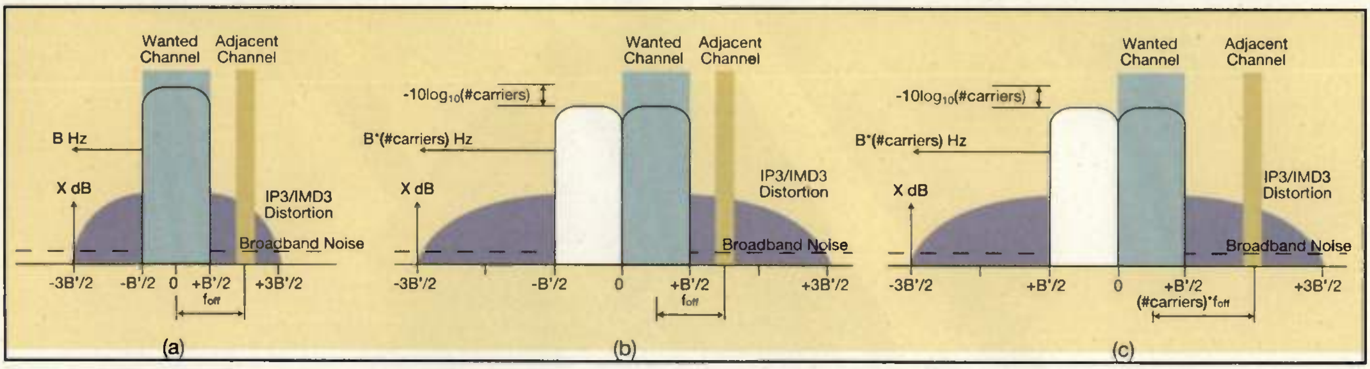

Figure 3. Multicarrier adjacent-channel power ratio.

noise floor of the ADC. The noise from the front end is

$$noise_{FE} = 10\log\left(\frac{kTBW}{0.001}\right) + Gain + NF$$

$$noise_{FE} = -174dBm/Hz + 35dB + 3dB$$

$$noise_{FE} = -136dBm/Hz$$

The noise floor of a typical 14-bit ADC, such as the AD9444, is

$$noise_{ADC} = -145.9dBm/Hz$$

Because the front-end noise density is much higher than that of the ADC, the ADC will not significantly contribute to overall sensitivity of the receiver. However, if additional sensitivity is desired, either an automatic gain control can be used or the 8 dB margin can be reduced or a combination of the two.

As shown in Table 1, signal levels can be high. It is not uncommon for IF output levels to approach levels as high as +15 dBm to overcome the loss of following analog filters such as the Nyquist filter shown in the example. Because these levels are so high, third-order intercepts can become a problem. In traditional receiver architectures this problem can be mitigated by distributing the gains and losses over more stages, but in a multicarrier IF sampling and direct conversion radio, this is often not possible. For a case in point, the Nyquist filter is often implemented as a surface-acoustic wave (SAW) filter. Because SAW filters have such high losses, their input levels must often be driven hard to overcome their loss. If the filter were a lower loss version, the input drive level could be greatly reduced and IP3 performance would be easier to meet.

Noted in Table 1 is the fact that the signal-to-noise ratio (SNR) of the desired signal (expressed in energy density) is about -16 dB. Because CDMA2000 uses correlation to detect the signal of interest, negative SNRs are acceptable as long as the correlation gain is high enough. For CDMA2000, the correlation gain is about 21 dB, resulting in an effective SNR of +5 dB for this example.

The transmit side poses even more challenges. Because of regulatory requirements and specifications found in the standards, complex feed forward and/or feedback loops must be used. Architectures become driven not only by costs, but by specifications such as code domain power, ρ/error vector magnitude and adjacent-channel power ratio. The standard for CDMA2000 (Section 4 of 3GPP2 C.S0010-B) defines a nominal test model having a pilot, sync, single paging channel and six traffic channels. Code-domain power (CDP) can be considered code-domain noise; if there is too much then the receiver's ability to de-correlate channels is reduced. For an SR1/RC3 carrier, the code-domain power shall be less than 27 dB. CDP can be calculated using error vector magnitude (EVM) and spreading factor (Walsh code).

$$CDP = 10\log_{10}(EVM^2/SF)$$

Antenna power amplifiers' operating points are set so that signal crests are below the amplifier's maximum unsaturated output power. Depending on the type of information being transferred, a carrier can have high peak-to-average ratios (PAR) if the component signals add in-phase; combining multiple carriers further increases the probability of phase alignment, increasing the PAR. The increased PAR lowers the efficiency of the power amplifier for a fixed linearity. A single nominal test model carrier has 9.6 dB PAR for a $10^{-4\%}$ probability, and a composite waveform of six adjacent carriers has 12.9 dB PAR. Peak-to-average power reduction (PAPR) engines, such as the AD6633, can be used to increase power amplifier (PA) efficiency by trading modulation accuracy for compression, *without* adding out-of-band distortion. The AD6633 compresses a six-carrier waveform by up to 6 dB.

For greater efficiency, digital pre-distortion PA linearization moves the PA into saturation while compensating for the resulting distortion. Third-order intermodulation products in the forward path of a PA linearization loop will occupy a bandwidth three times that of the signal, centered on the signal, with fifth order occupying five times the signal bandwidth. The digital-to-analog converter (DAC) must have the same bandwidth to cancel the distortion. For six adjacent carriers, 37.5 MHz is needed for fifth-order cancellation. In the observation path, the RF is down-mixed and digitized to baseband where it is averaged with a digital signal processor, which also computes new pre-distortion coefficients. One possible digitization approach mixes down close to dc using an ADC nyquist bandwidth equal to the distortion bandwidth. For six adjacent carriers, a 92.16 MSps ADC is sufficient (Figure 2a). Alternatively, a down-mix to a low IF followed by an undersampling ADC captures the third-order components without aliasing with higher orders aliasing in band; for an IF of 76.8 MHz, a 61.44 MSps converter is sufficient (Figure 2b). The ADC's distortion should be lower than the desired antenna distortion, typically ≤70 dBc spurious-free dynamic range. The samples are averaged so the ADC's noise can be relaxed to -135 dBm/Hz, which is about 60 dB SNR.


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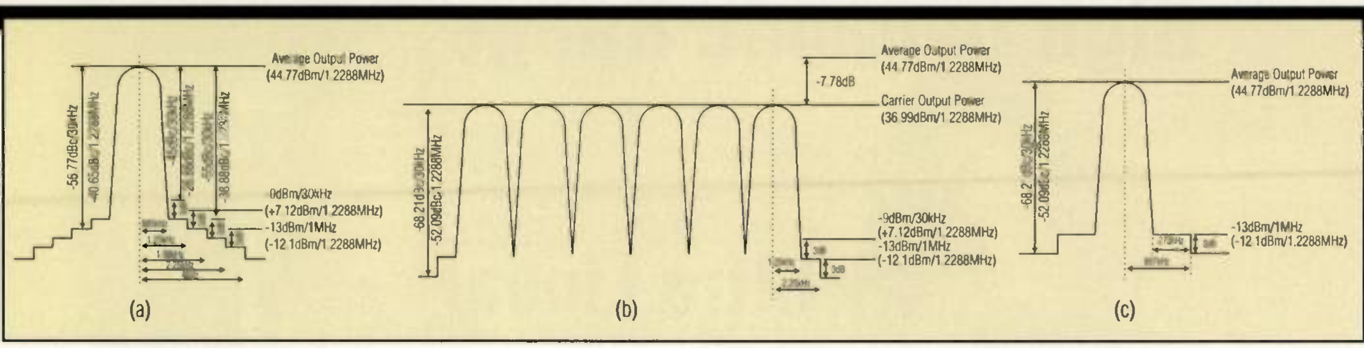


Figure 4. Multicarrler llnearity level plan.

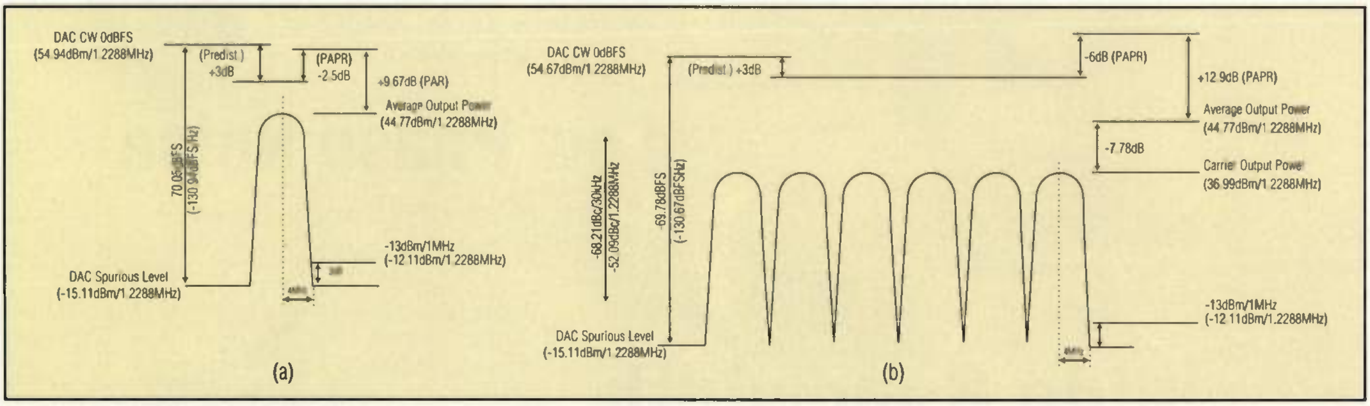


Figure 5. Multicarrier noise level plan.

Literature suggests that digital pre-distortion and PAPR can improve the PA's effective IP3 by +15 dBm.

Within three times the signal bandwidth, the ACPR at a frequency offset, F_{off}, is dominated by IP3 distortion. Beyond that, noise dominates (Figure 3a). For the same PA power, adding a carrier reduces the per carrier power but keeps the distortion power at F_{off} the same, degrading ACPR by 10log(n), where n is the number of carriers (Figure 3b). The same ACPR as the single carrier F_{off} is achieved at n times F_{off} (Figure 3c). To refer a multicarrier ACPR to a single carrier, divide the multicarrier frequency offset by number of carriers, n. The ACPR for a single carrier, dominated by IP3, is estimated by [1]:

$$\mathrm{ACPR} \approx 16.12 + 10\log_{10}\left(\frac{P_o^2\,\square f}{48 \cdot \mathrm{OIP3}^2 B}(3 - '\,_o)^2(3'\,_o^2 - 8'\,_o + 9)\right)$$

Using the above observations and equation, one can refer multicarrier linearity specifications to a single carrier and calculate signal chain requirements.

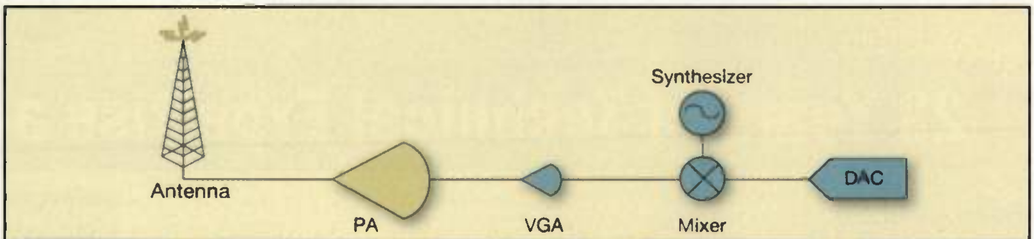
The 3GPP2 specification defines the waveform quality, ρ, using a single pilot channel and requires it be >0.912. Composite ρ is a better measure of system modulation accuracy, and if determined by component linearity, the below equation provides a good approximation.

$$` = 1 - \frac{4P_o}{3\mathrm{OIP3}}$$

The above approximation links to EVM by,

$$\mathrm{EVM}(\%) = 100 * \sqrt{\frac{1}{`} - 1}$$

which can be used to approximate the CDP, as detailed above.



PA	
output power	45
input power	5
Gain	40
IIP3	40
OIP3	80
NF	8
total OIP3(dBm)	75.15
Rho	0.9987

VGA	
output power	5
input power	-15
Gain	20
IIP3	24
OIP3	44
NF	8
noise (dBm/1MHz)	-15.12
EVM (%)	3.5906

Mixer	
output power	-15
input power	-15
Gain	0
IIP3	18
OIP3	18
NSD	-155
2.25MHz offset (dBm/1MHz)	-15.22
CDP (dB)	-46.96

DAC	
output power	-15
input power	-15
Gain	0
IIP3	31.5
OIP3	31.5
NSD (dBm/Hz)	-155
IMD3	75
PAR overhead	10
0dBFS (dBm)	-5
NSD (dBFS/Hz)	-150

Synthesizer	
NSD	-152
4MHz offset	

Figure 6. Simplified transmit signal chain.

The 3GPP2 emissions requirements determine linearity, wideband noise and dynamic range requirements of the converters. To illustrate the requirements, a worked example of a 30 W PA, using PAPR and pre-distortion linearization for six carriers at an RF of greater than 1 GHz with category A emission requirements will be considered.

Consider first the linearity requirements for a single carrier (Figure 4a). The first requirement is -45 dBc/30 kHz from 885 kHz to 1.25 MHz. The second is a -45 dBc/30 kHz requirement at 1.25 MHz offset or -9 dBm/30 kHz, whichever is the more stringent. The next limitation is at 1.98 MHz, but since a single carrier's third-order distortion does not occupy 1.98 MHz, the defining limitation on a single carrier's linearity, for a 44.77 dBm/1.2288 MHz carrier, is the -9 dBm/30 kHz requirement. For six carriers (Figure 4b), per-carrier power is now 36.99 dBm/1.2288 MHz, occupying a distortion bandwidth of 7.479 MHz from the edge of the outermost carriers. The -9 dBm/30 kHz at 1.25 MHz is a requirement for multicarrier, but this does not define the linearity. A requirement starting at 2.25 MHz offset of -13 dBm/1 MHz defines the linearity requirement. With 3 dB margin over the specification, the ACPR requirement becomes

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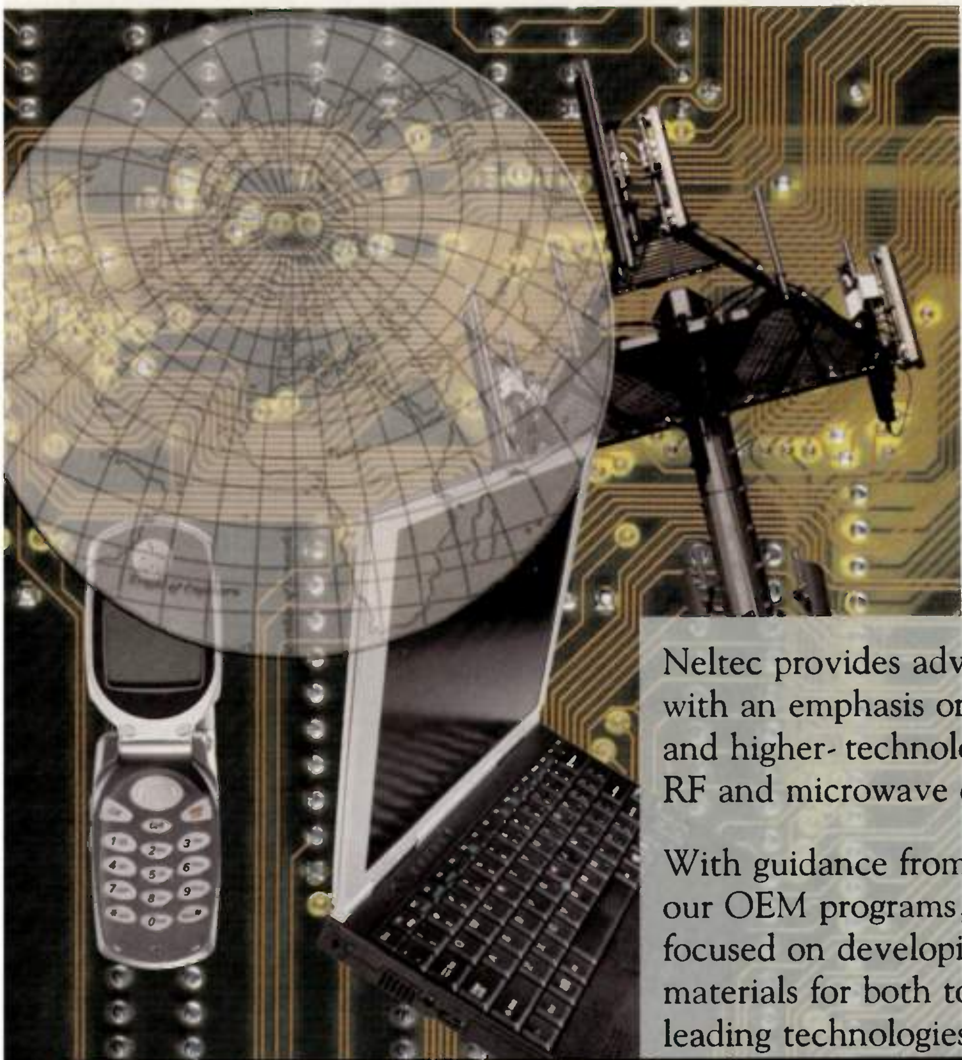

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-68.21 dBc/30 kHz at 2.25 MHz offset. Referring back to the single carrier case, (Figure 4c) dividing the frequency offset from the edge of the carrier by six gives a linearity requirement of -68.21 dBc/30 kHz at 887 kHz frequency offset. This is a harder linearity requirement than the single carrier case.

Consider the noise requirements. The single carrier case, Figure 5a, has a 9.67 dB peak-to-average ratio with 2.5 dB reduction for peak-to-average power reduction and 3 dB extra dynamic range for digital pre-distortion, giving a peak of 54.94 dBm/1.2288 MHz. Category A emission limits the noise to -13 dBm/1 MHz at a 4 MHz offset. With 3 dB of margin, this requires 70 dB of dynamic range or -130.94 dB/Hz noise power spectral density. The six-carrier case, Figure 5b, has 12.9 dB of peak-to-average ratio, but this can be reduced by 6 dB with peak-to-average power reduction. Allowing 3 dB extra dynamic range for digital pre-distortion puts the peaks at 54.67 dBm/1.2288 MHz, about the same as the single carrier peak.

The six-carrier requirement of -16 dBm/1MHz at 2.25 MHz offset determines the linearity. The wideband noise is defined by the -16 dBm/1 MHz category A emissions plus margin requirement. Looking at a simplified signal chain (Figure 6), modulators typically have an output power of -15 dBm. With 20 dB variable gain amplifier (VGA) gain, the PA needs 40 dB to deliver +45 dBm from the DAC. With PA linearization, a +15 dBm PA output third-order intercept point (OIP3) improvement can result. Modulators typically have an OIP3 of approximately +18 dBm, and VGAs have OIP3s exceeding +20 dBm for 20 dB gain. The cascaded OIP3 at the PA output is +75.15 dBm and suggests that the overall OIP3 is dominated by the PA and is insensitive to DAC linearity. This OIP3 gives -15.22 dBm/1 MHz at 2.25 MHz offset.

The modulator will typically have a noise contribution of about -155 dBm/Hz. Setting the DAC and synthesizer contributions to -155 dBm/Hz and -152 dBm/Hz, respectively, means that to achieve the wideband noise requirement of -16 dBm/1 MHz, with this gain planning, requires the VGA and PA to have an NF of 8 dB. With this level plan, the DAC's mean output is at -15 dBm. With 10 dB due to peak-to-average overhead, this puts the DAC's full scale output at -5 dBm. The DAC's dynamic range needs to be -150 dBFS/Hz. The AD9779 is suited to this signal chain. An approximate ρ of 0.9987 and a code domain power of -46.96 dB will result.

The requirements for high rate packet data access, 1x Evolution-Data Only (1xEV-DO), are detailed in the 3GPP2 specification C.S0032-0. The limitations on emissions are the same as discussed in this document, but the waveform quality factor, ρ, is improved to 0.97. So the system has to be more linear with similar noise requirements. As shown by the simplified signal chain design, the linearity is dominated by the PA and will have minimal impact on the converter performance requirements. RFD

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ABOUT THE AUTHORS

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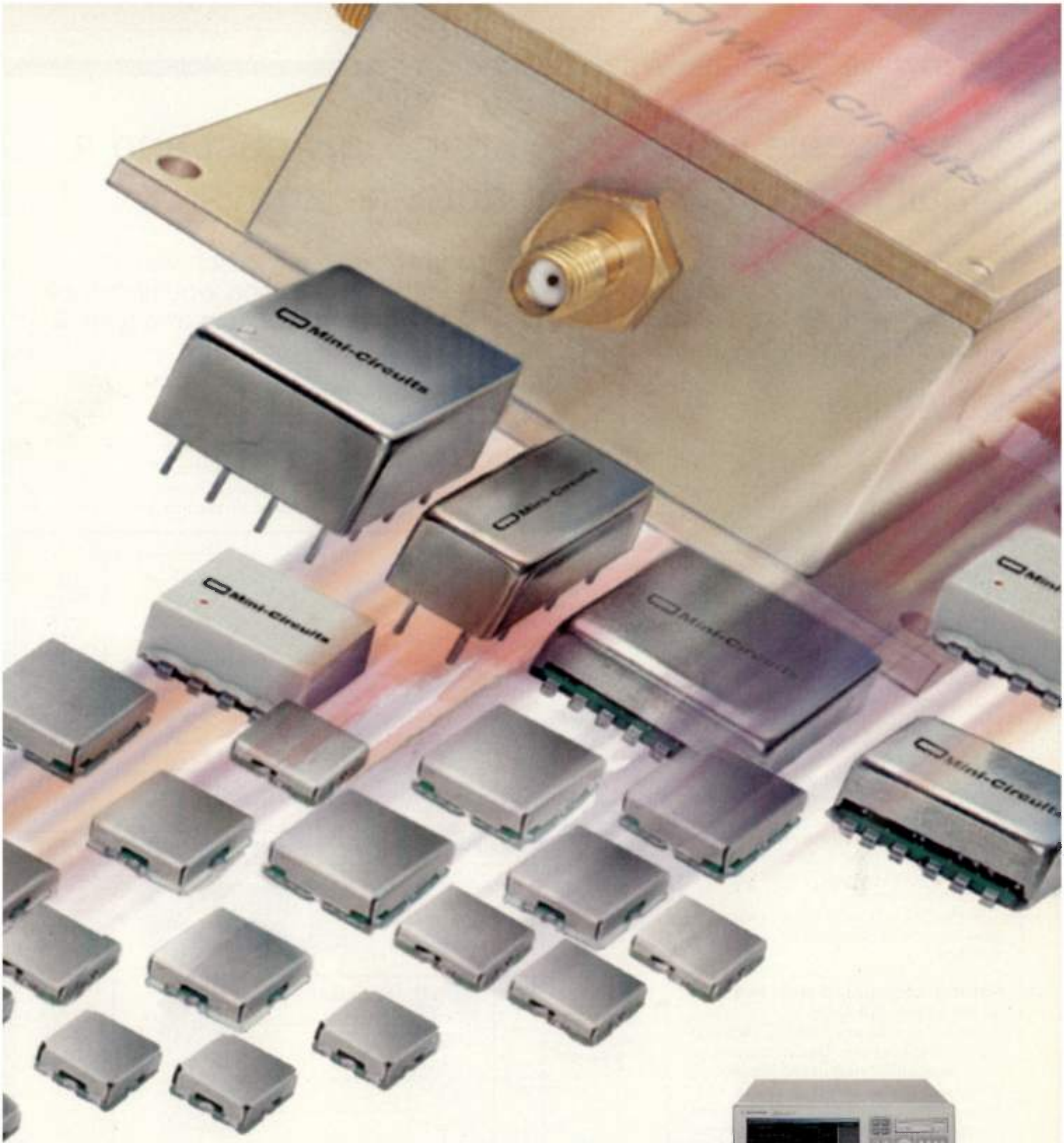
Mini-Circuits

Wafer-scale integration brings low cost and a small footprint to active antenna arrays

Fabricating a 256-element steerable antenna array on an eight-inch wafer is quite a feat, given the multitude of issues—steering the antenna, optimizing the RF paths and the like. By addressing these and other matters, one at a time, it becomes clear that realization is well within reach.

By Fred Mohamadi

Tremendous interest is developing with regard to the use of Si-substrate technology for SHF, RF and microwave applications. Wafer scale integration using Si substrate makes it possible to fabricate cell array units in a module that comprise antenna and RF circuitry for beam-forming applications[1-3]. These technologies will, in turn, make possible the deployment of low-cost, steerable arrays for military and commercial applications.

However, there are a number of challenges in the design and fabrication of such arrays. They include the fabrication of Si-based substrate RF blocks and the distribution of RF signals to each element. Then there are issues such as the impact of signal attenuation and crosstalk, the accuracy required in phase resolution, and beam-width management. Finally, there are the questions of noise cancellation, dc signal distribution, and the control capability of beam forming for tracking and beam steering.

We will address these various issues and provide a number of suggestions for dealing with them.

Getting acquainted with the wafer scale module

The wafer scale array module (WSAM) described here provides transmit and receive functions at a bandwidth of 5%. The module is designed to scan ±30 degrees at a 3 dB drop-off from maximum-emitted radiated power (ERP). In one possible scenario the module would deliver 10 W to 40 W ERP broadside to the WSAM—assuming the module is operating at 3.3 V.

The WSAM consists of a 16 by 16 element antenna and its associated electronic circuitry. The total number of elements is 256. Fabricated on an 8-inch (200 mm) CMOS or Si-Ge wafer, the antenna elements are spaced 8 mm apart.

Just how many elements can be successfully placed on an 8-inch wafer is an important issue. This is depicted in Figure 1, which illustrates the impact of pitch on the maximum number of elements that can be placed on a 6-inch or an 8-inch wafer. The trade-off between antenna gain (dBi) and separation, in mm, is also a design constraint because placing antenna elements closer than a quarter wavelength apart diminishes the gain of the array.

The metal routing architecture is another constraint since every single element that is traced to the central feed line must present exactly the same signal traveling distance.

Wafer scale technology can accommodate a number of antenna array options. For

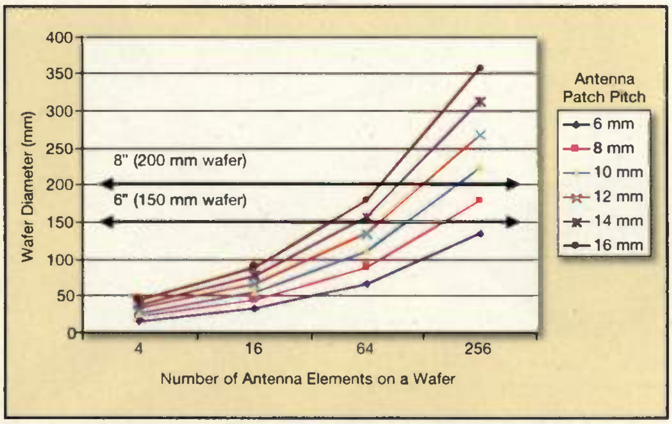

Figure 1. Maximum number of elements vs. antenna element pitch.

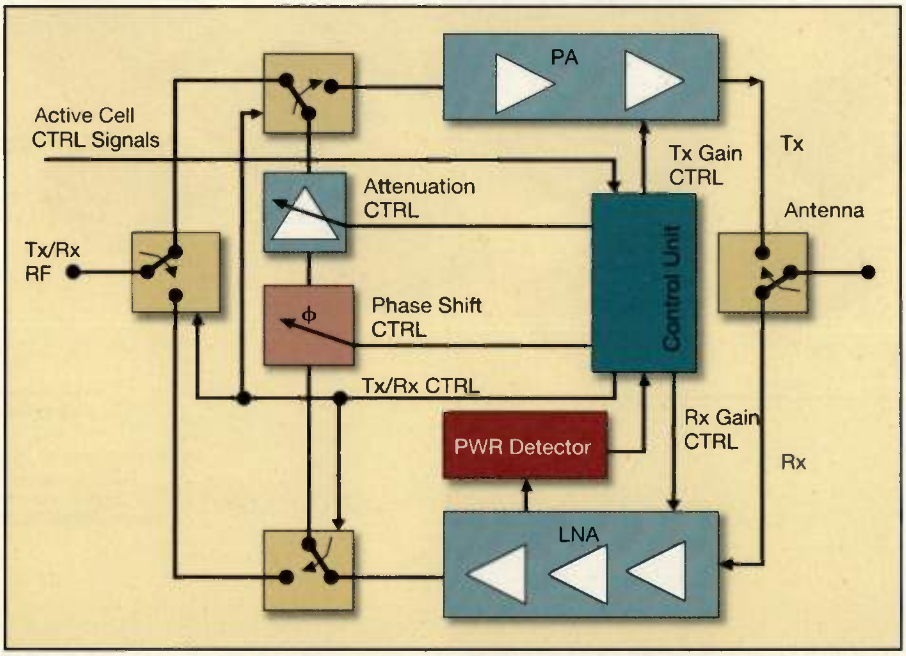

Figure 2. Antenna array element RF module for Tx/Rx functions and controller's local management functions.

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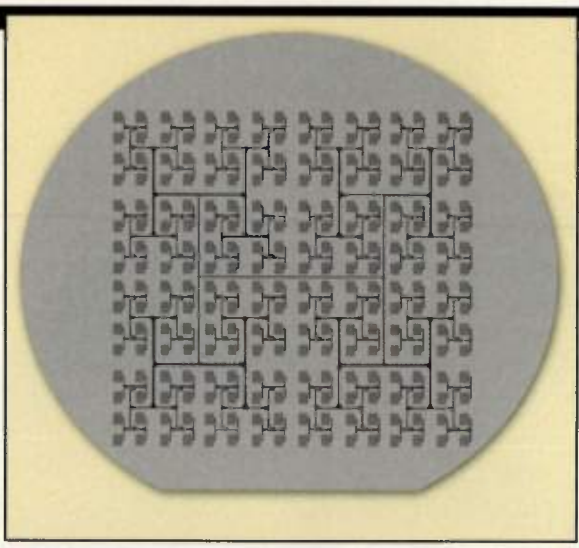

Figure 3. Wafer scale module with RF interconnect network and antenna array in separate planes.

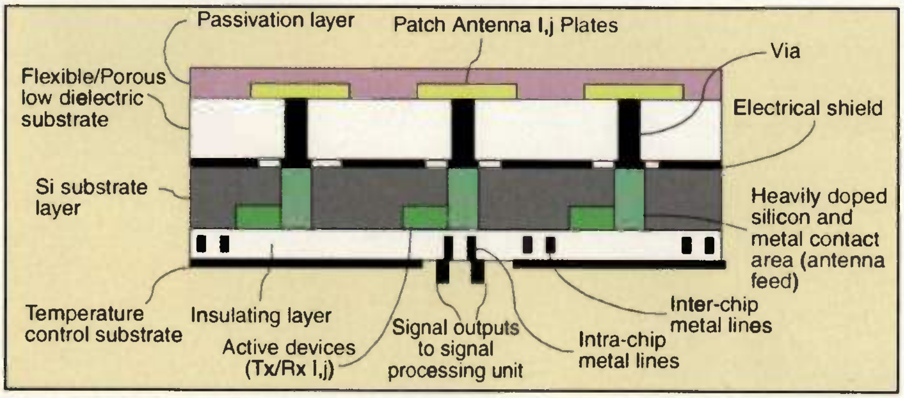

Figure 4. An implementation of the patch antenna array on the Si substrate.

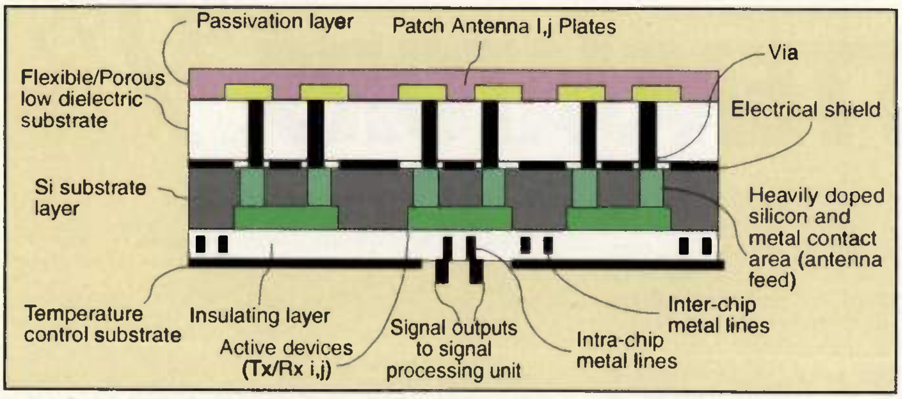

Figure 5. An alternative implementation of the dipole antenna array on the Si substrate.

instance, an eight-inch wafer can be used for 64-element array with 15 mm pitch (separation plus antenna size) corresponding to a 10 GHz RF signal. Alternatively, a 1024-element array operating at 40 GHz could be built on an eight-inch wafer substrate. This would maximize the gain of the antenna array.

As for the array architecture, the WSAM uses a so-called "tile" array configuration in which the radiating element layer and the signal distribution layer are parallel to each other. The radiating element layer can be either a CMOS or a Si-Ge RF device layer. The layers are interconnected using a special manufacturing process discussed later in this article. A block diagram of the WSAM is shown in Figure 2 and the module's form factor is illustrated in Figure 3.

With regard to the RF portion of the module, it consists of a 256-network line RF signal divider. In our example a 2-micron-thick, metal layer 5 is used. Included in each cell are a low noise amplifier (LNA), a programmable power amplifier (PA), and analog switches to select Rx or Tx modes, an attenuator, and a phase shifter unit, as well as a controller.

Managing the module

The WSAM must communicate with an external electronic unit (baseband and MAC functions). Here is where the mixed signal-based controller plays a number of important roles. It addresses power management based on a peak detection mechanism at the receiver. There is a PA gain control to optimize efficiency, pre-distortion capability to address linearity, and a LNA gain control to optimize SNR performance. The controller also operates a 3-bit, digitally controlled phase shifter. The controller plays additional roles, for there is an optional field to address LNA gain control, and Tx or Rx switch selection. Finally, there is a power management function to address sleep mode operation.

As for power distribution, the necessary regulated and selected bias voltages are fed to the gate and drain of the PA, to the LNA, the analog switches, the phase shifter, attenuator circuit, and controller unit.

The wafer scale integration concept is illustrated in Figure 3. The module comprises three main layers—a radiating element layer, a device layer and a signal distribution layer. The radiating element layer can consist of 256 microstrip patches, or dipole, elements. To provide low resistance thermal paths that ensure effective heat dissipation, a layer of heat-conducting material can be used to coat the active device side of the wafer.

An important consideration is the maximum allowable current density of 10^5 amperes/cm^2, as governed by the electromigration design rules. This sets an upper limit of 2 mA per micron length for a 2+-micron-thick Al-Cu line. The RF interconnection layer consists of coplanar waveguide (CPW) or shielded microstrip transmission lines and distributed signal reshapers and repeaters.

If we look at the performance of the isolated antenna elements, here are some typical specifications. In one application, an isolated element provides a bandwidth of 5% for a 2:1 VSWR at 7 dB gain. The element is excited through a metal rod connected to a via that is filled with a deposited metal layer. After proper phase shifting, the element connects to an output of an analog RF switch powered by a PA. Similarly, in receive mode, this element can deliver collected radiation to the input of the RF switch feeding the LNA, before properly phase shifting it.

As for the power amplifier, it could be a three-stage, 50-micrometer to 200-micrometer, gate-width amplifier that delivers 200 mW at 20 dB gain and 25% efficiency. The phase shifter provides at least three bits of switched line lengths with 3 degrees rms maximum variation. The phase-shifting device has less than 5 dB insertion loss (ideally below 1 dB) at room temperature. The RF switches, LNA, PA, phase shifter and the controller are all included in the die. Once it has been adequately shielding and thereby isolated to prevent electromagnetic coupling to active devices, the die fits under the antenna plate.

Now that we have an overview of the

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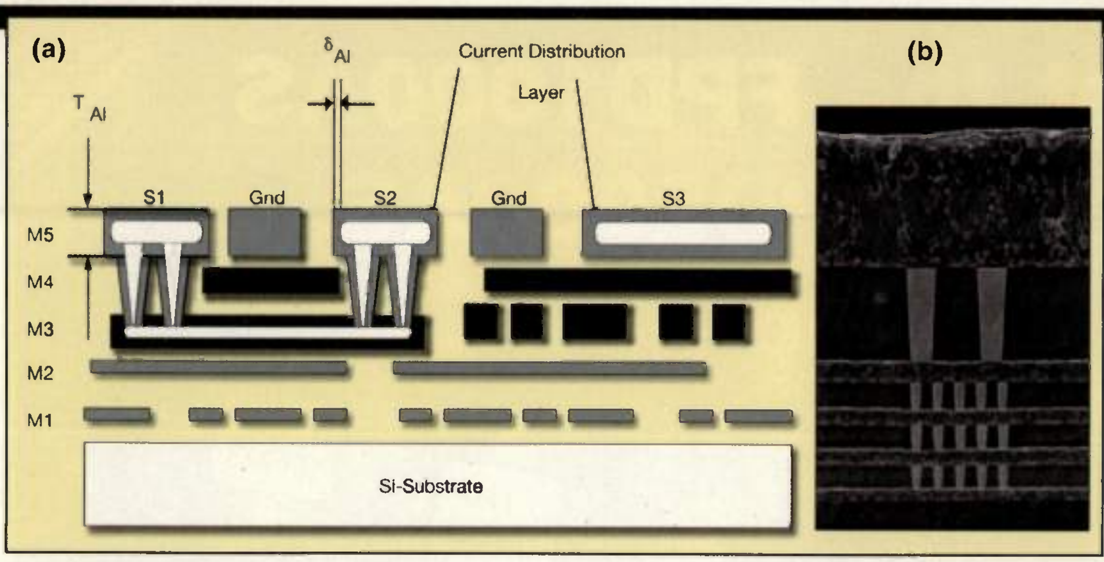

Figure 6. Cross-section of a five-layer metal Si substrate process: (a) impact of skin depth on current distribution; (b) actual metalization scheme.

WSAM, we can go on to examine the fabrication steps, in detail.

Wafer scale integration using a Si-substrate

The proposed WSAM implementation is shown in Figure 4.

1. Prior to any standard process step, a heavily doped, deep conductive junction is formed as a contact junction for the antenna feed. This is similar to a deep-diffusion junction process employed in the manufacture of double-diffused or tripled-diffused CMOS (DMOS) high-voltage devices. The deep junction is used to separate, and thereby effectively isolate the antenna feed lines from the active devices—which are the LNA, the phase shifter and the PA. This junction also provides a low-resistance, signal-path region that is essential for minimizing insertion loss to the antenna plates, patch or dipole. The deep junctions will be accessed through the backside of the wafer. The antenna plates will then be fabricated.

2. The active devices are manufactured using standard Si-substrate, CMOS or Si-Ge processes.

3. Passivation of the active devices is accomplished by first applying a low-temperature, deposited porous silica SiOx. Then a thin layer of Nitridized oxide (SixOyNz) is applied as the final layer of passivation. Thickness of the sealing layer is a fraction to a few micrometers.

4. The top layer of the active devices is coated with a thermally conductive material, taped to a plastic adhesive holder, and then flipped to expose the unprocessed side of the


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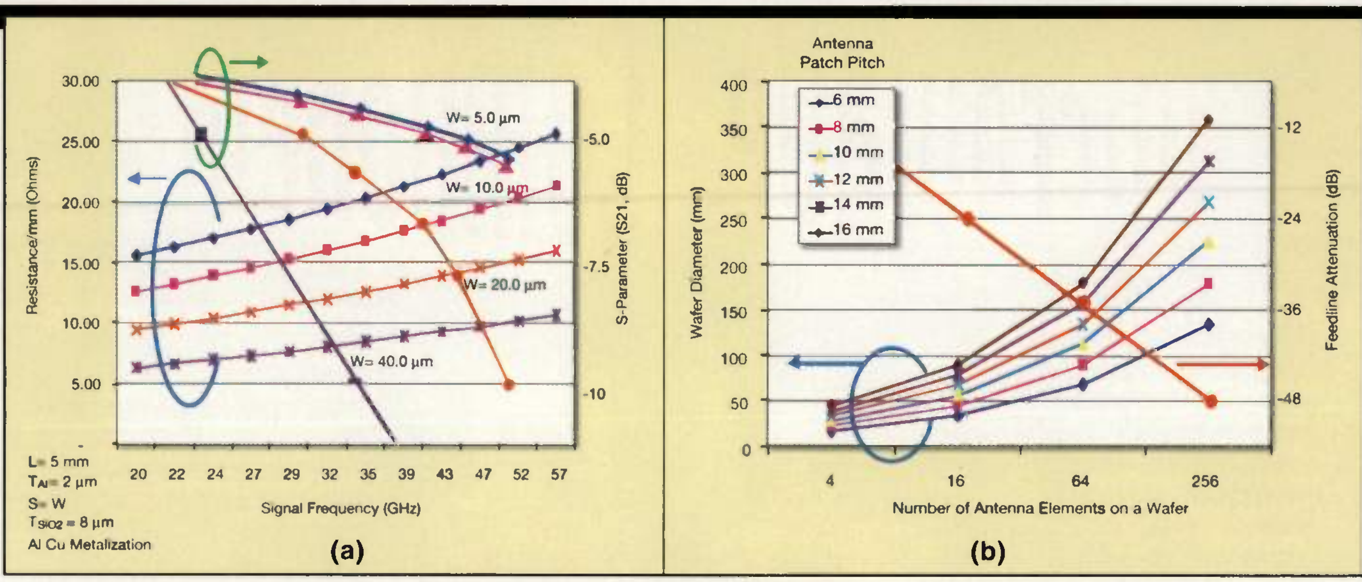

Figure 7. An interconnection line imposes limitation on wafer scale integration: (a) insertion loss as a function of RF frequency (L= 5 mm); (b) Feedline attenuation as a function of integration of antenna elements on a wafer (L= 90 mm).

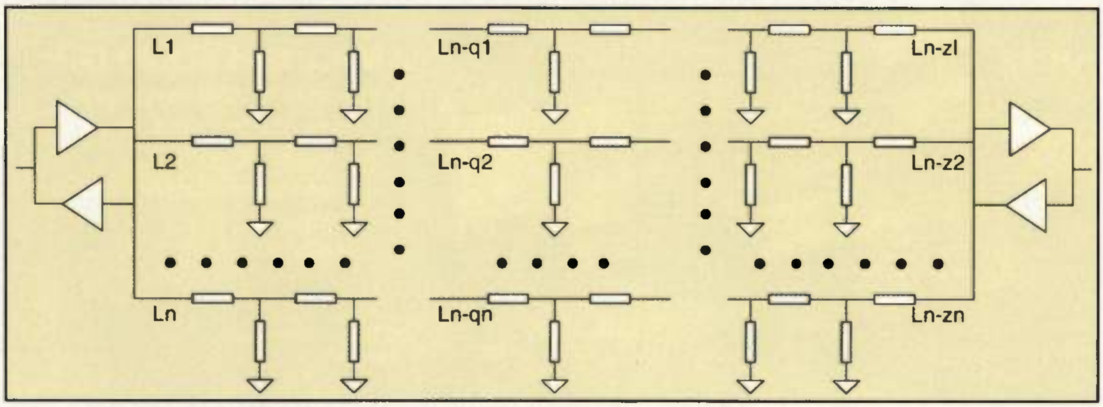

Figure 8. Combining, decombining and shuffling the RF signal paths.

wafer (backside of the wafer).

5. The wafer thickness is then reduced by grinding the backside of the wafer to a thin layer, no more than a few hundreds of a micrometer thick.

6. An additional layer of metalization is sputtered, evaporated, deposited, or alternatively coated using conductive paints. This layer forms a reflective plane for directivity and shields the active devices from antenna radiation. It also provides contact fillers to the heavily doped Si that connects to the feed lines of the antenna patch or dipole layers. The deposited material at the backside of the wafer is patterned as metal lumps on top of the highly doped Si contact-to-antenna feed circuitry. These metal lumps ease the penetration of via rods that will form Ohmic contacts with the feed circuitry and connect to the antenna plates, thereby preventing cracking of the Si substrate.

7. The target alignment patterns that were

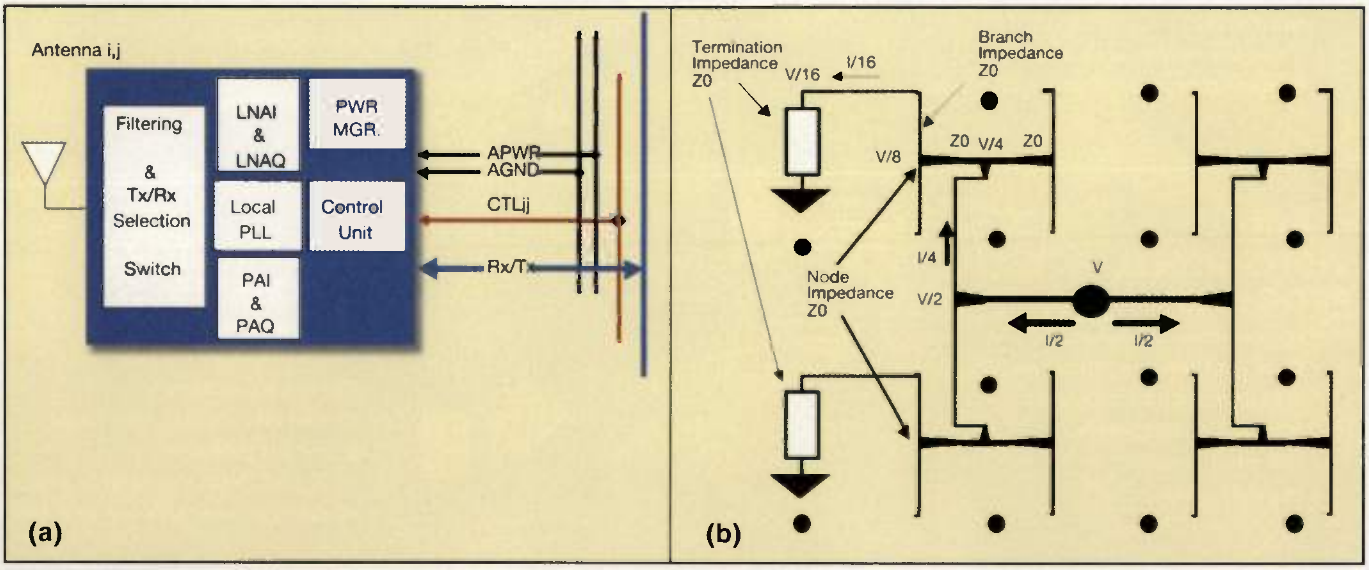

Figure 9. An example of an antenna array cell unit and centralized signal distribution: (a) functional block diagram of a unit cell with dc lines, RF Tx/Rx, and digital control lines; (b) RF Rx/Tx distribution from a central feed to a unit cell.

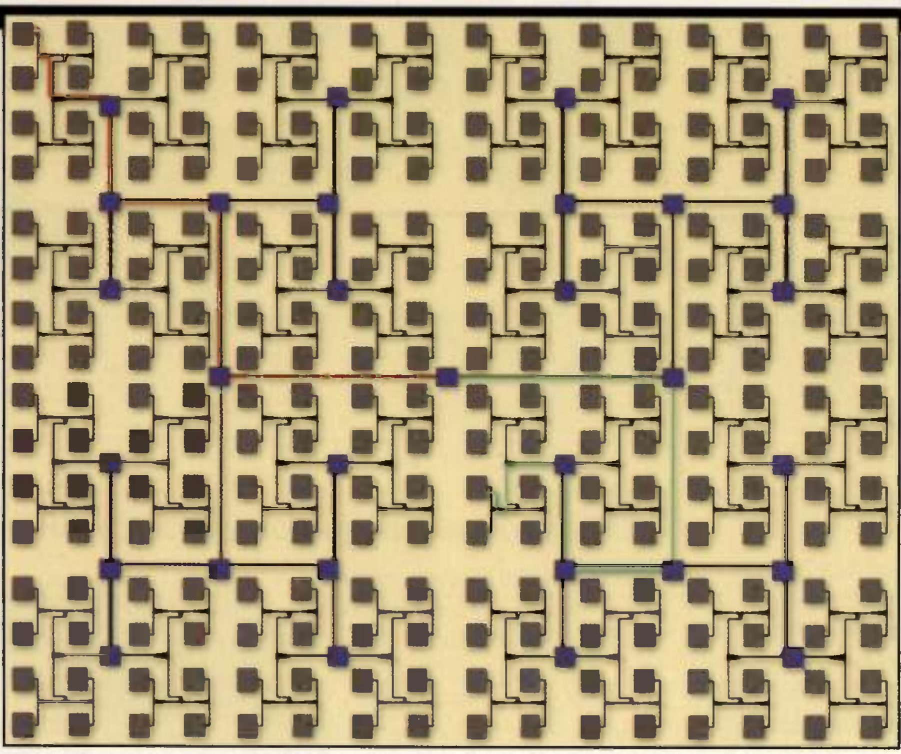

Figure 10. Antenna array with distributed amplifiers, array and RF feed lines in two different paths.

etched during the normal manufacturing process of the silicon wafer are then used to precisely locate the vias—the metal layer that connects the antenna to the feed lines in the Si substrate. This process can use an infrared alignment scheme, as is frequently employed in the manufacture of some MEMs devices.

8. A layer of porous material, or honeycomb structure, separates the antenna layer from the shield and Si substrate. This material has a low dielectric constant so that it effectively decouples the antenna from the substrate, thereby ensuring satisfactory antenna efficiency.

9. A top plate of thin Teflon or a similar material with a low dielectric constant is used as a substrate for the antenna plates. As an option, a very thin layer of high dielectric material, such as Ta_2O_5, can be used to reduce horizontal surface waves.

10. Dipole or patch patterns, as well as alignment patterns, are defined in the deposited metal layers on top of the Teflon layer.

11. Precision rods are inserted to form through-hole contacts and to complete the antenna-to-feed electrical connections. Alternatively, the vias can be precision drilled and filled with conductive material to form highly Ohmic contacts.

12. A final passivation layer is applied on top of the antenna layers to provide impedance matching to free space and to protect the devices.

13. The connectors to the RF Rx/Tx unit and controller are then brought up to the external area for beam steering/tracking

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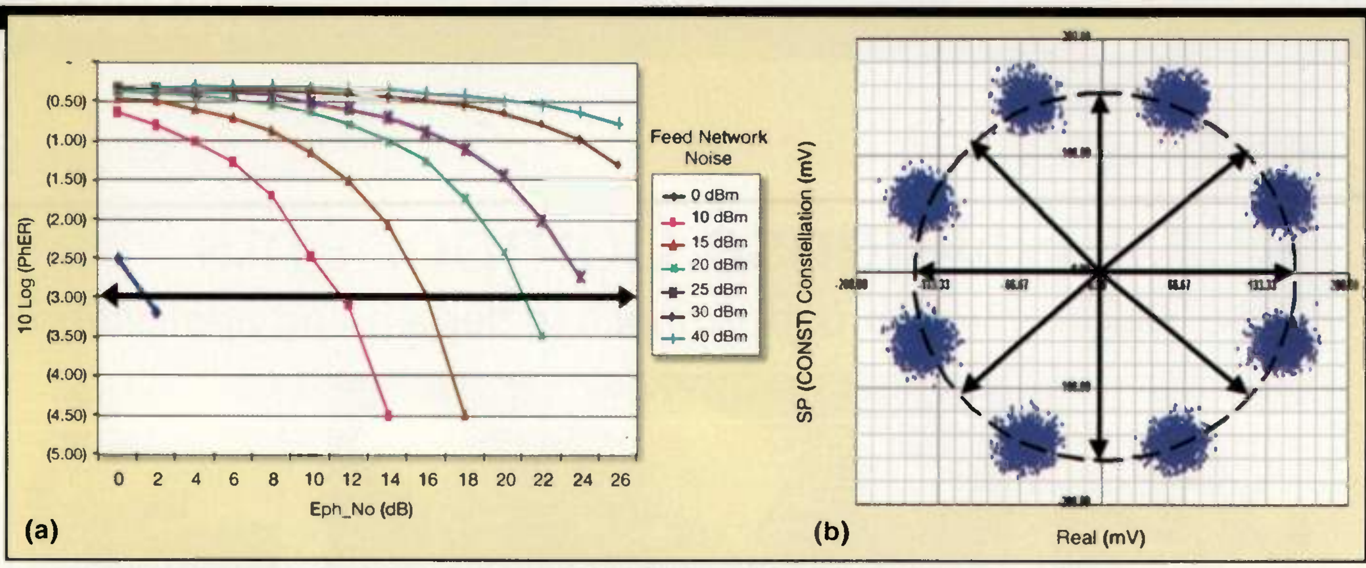

Figure 11. Simulation results of tolerable jitter: (a) phase error rate for various noise levels; (b) phase resolution diagram.

and for the signal processing associated with the beam-forming algorithms.

14. Finally, the finished wafer is flipped and the RF connectors are attached.

There are, of course, alternative manufacturing processes and one is shown in Figure 5. Here the deep conductive junctions are formed from the backside of the wafer and then the front side devices are fabricated with the standard semiconductor manufacturing process previously described. The rest of the process is also identical to the previously mentioned manufacturing flow. Shown in Figure 5 is an alternative implementation of the cell antenna that uses a dipole antenna.

Signal distribution limitations and proposed solutions

It turns out that the limitations imposed by the metal routing, so essential for high-density and high-speed semiconductor products, have been a subject of study for decades[4]. Another hindrance to performance is the low-resistivity substrate, used to improve yields and suppress latch-up. Nonetheless, such substrates contribute significant, high-frequency losses. So it is no surprise that the silicon substrate has been the major limitation in X-, K- and Q-band applications. Fortunately, the current trend of metal

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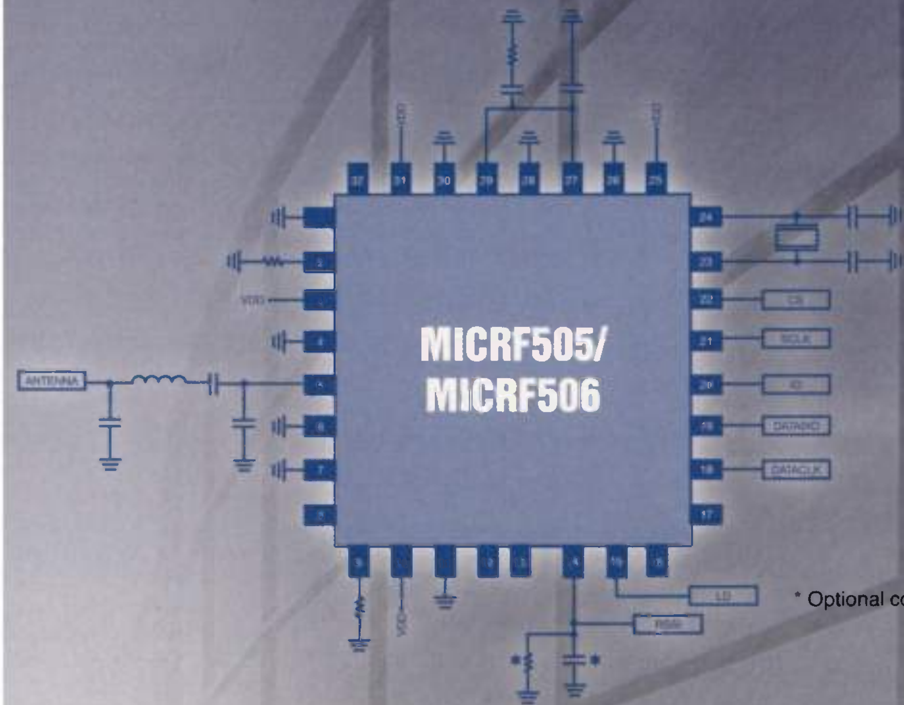

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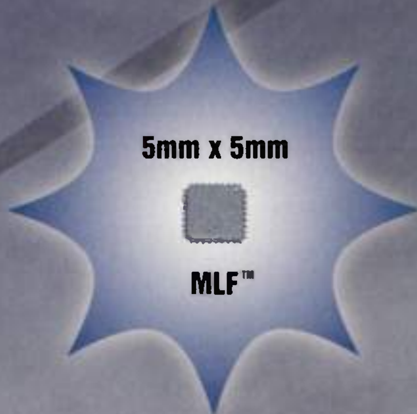

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technology scaling alleviates this concern, as illustrated in Figure 6.

As depicted in Figure 6b, the bottom metal layers scale to smaller pitches to enable denser routing. Whereas the top metal layers scale to larger pitches to enable thicker lines for improved power and high-frequency RF handling—as well as a lower global routing loss. The interlayer dielectric thickness is almost twice the metal thickness. This minimizes interlevel shorts and reduces capacitance. As a result, the top metal layers are situated further away from the silicon substrate, thereby reducing the losses associated with the substrate. At present, the current trend is for the distance from the top-level metal to the silicon substrate to be approximately 1.5-micrometers per metal layer.

Let us look next at the effects of line width and associated skin depth. The impact of skin depth on signal attenuation has been modeled to address the resistance of metal lines as a function of frequency of the signal[5-10]. Shown in Figure 7a is the impact upon the S-parameters of coplanar waveguides fabricated with 2-µm thick, aluminum metalization. To demonstrate the impact of insertion loss and line resistance as a function of frequency, a top layer has been used. The results indicate that feed line signal attenuation is serious, as seen in Figure 7b. In fact, for a 256-element active antenna cell, power deterioration is -48 dB. Also quite pronounced is the impact of capacitive coupling to the substrate and inductive coupling to the ground lines. The insertion loss worsens from -5 dB to -10 dB for a 5-mm length line with various trace widths and spacings, as denoted in Figure 7a. It should also be noted that for a WSAM, which must feed 256 active cells, the signal-distribution line loss remains significant for line lengths up to approximately 100 mm.

Minimizing jitter

The control of jitter by removing intersymbol interference (ISI) and crosstalk is an important part of any proposed integration scheme because the jitter issue is a critical factor in meeting the required bit error rate (BER) in most digital communication applications. However, the issue is less important in radar applications where a reflected continuous wave signal is used to calculate the distance and velocity of an object.

Precision timing deterioration and random phase shift, cause significant jitter in the delivered signal. By far, this has the worst impact on beam forming. This means that increments of phase shift need to be accurately managed in each cell—to better than 2° to 3° rms per available phase increment.

One way to reduce jitter is to employ re-timing circuitry. However, the use of a PLL-based re-timer in each cell results in more complexity in circuit design and also demands very high bandwidth processes—such as IBM's 8HP, or even its 9HP process technology. Despite the precision phase management that can be achieved with PLL in the RF signal paths, its use can introduce design risks. What's more, it can lead to excess power consumption, given the high data rates that must be employed.

To further address jitter management, future designs may use a PLL-based, re-timer with each split section. As shown in Figure 8 the line interweaving minimizes jitter whereas the distributed amplifiers behave as signal boosters, thereby compensating for the resistive line loss.

The signal-carrying RF lines need to be combined or recombined at each split

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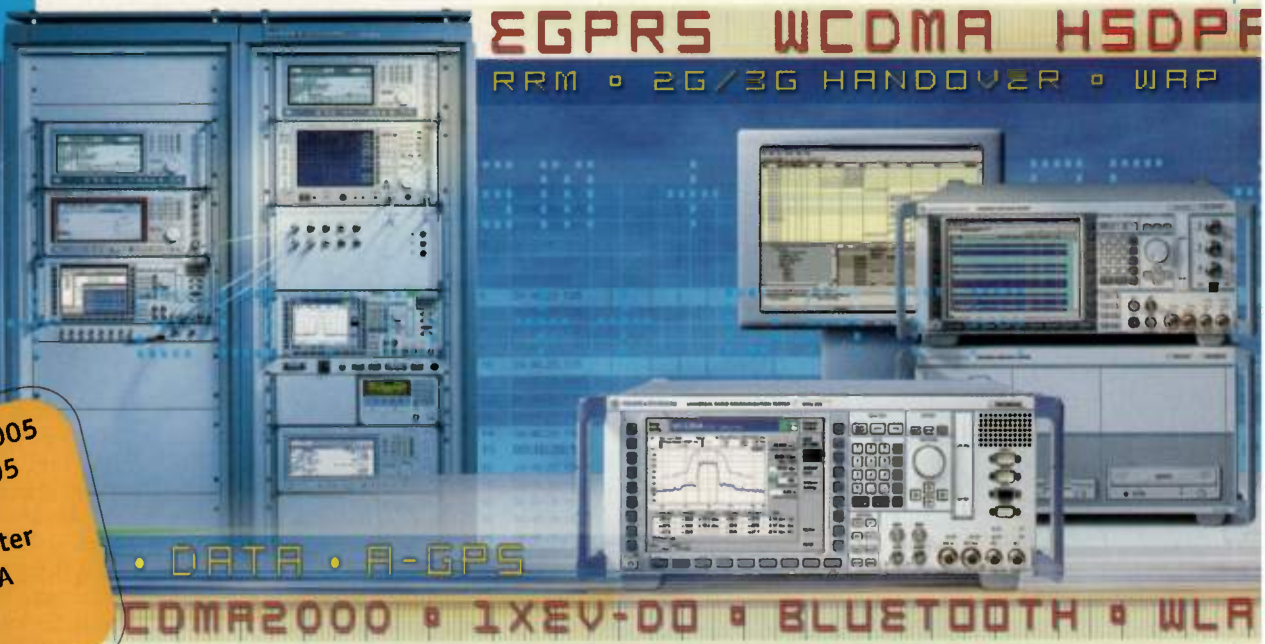

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section. These steps can be accomplished by employing RF signal repeaters that are realized with distributed amplifiers, as depicted in Figure 8. The RF signal is reshaped to compensate for the line loss, replacing the traditional Wilkinson-type combiners and decombiners in combination with distributed amplifiers.

This methodology splits each of the wide, RF-carrying line into multiple, thinner lines so that each can be optimized, thereby make a minimal contribution to the net resistance. This is essential because the effective current density is three to five times the skin depth. The combining takes advantage of distributed amplifiers that provide sufficient bandwidth to compensate for the insertion loss. When compared with current passive combiners, the enhancement realized with this approach is substantial.

Signal delivery to each cell

The concept of RF signal delivery to each cell, including the branching (splitting) junctions is illustrated in Figure 9. The dc and control lines are distributed in a similar routing direction. However, they use all metal layers—metal layers 1 to 5—so that the isolation realized with the low Ohmic grounds can be managed. An enhancement to the proposed approach would be to design a voltage regulator at each splitter/branching so that ripple effects and noise accumulation on the dc power lines would be minimized.

The concept of including distributed amplifiers and active combiner/decombiner blocks for RF paths at each splitting junction, colored in blue, is depicted in Figure 10. Similarly, dc supply enhancements can be addressed by including a band-gap voltage regulator. Also, a large supply-to-ground distributed capacitor could be connected in parallel to filter out high-frequency noise.

For a three-bit shifter, phase shift increments are eight discrete phases: -180, -135, -90, -45, 0, 45, 90, 135, 180 (same as -180). In this case, the incremental phase is 3.0 picoseconds for a 40 GHz bitstream. In order to assure a 70% eye opening for satisfactory signal detection, the maximum tolerable total jitter must be less than 1 picosecond. As a result, the total jitter limitation, including rise and fall time on the precise location of the beam, the signal-to-noise (SNR) of the RF data path, and the active circuitry must be less than 1 picosecond. Based upon an initial evaluation illustrated in Figure 11, it can be concluded that for a phase error rate of better than 10^{-3} and a SNR of better than 20 dB, the maximum tolerable jitter noise in the feed system must be less than 15 dBm.

Shown in Figure 12 is a simulation for a 16-element, sub-array radiation that uses the implementations previously described. The gain of the sub-array is 3 dB to 4 dB less than the maximum attainable as a result of spacing the elements at slightly less than a half-wavelength apart. However, this compromise enables the implementation of 256 active antenna cells on a WSAM.

Conclusion

As we have discussed, attenuation of the RF signal and jitter deterioration, as a result of crosstalk and ISI, are the key areas of focus for an optimized design of a WSAM. Distributed amplifiers, spatial phase balancing and crosstalk cancellation are also crucial to improve the signal-to-noise ratio of the delivered RF signal to the active antenna elements. In the future, advanced CMOS and Si-Ge processes will enable the use of adaptive equalization at the antenna-element receiver, at the retimers

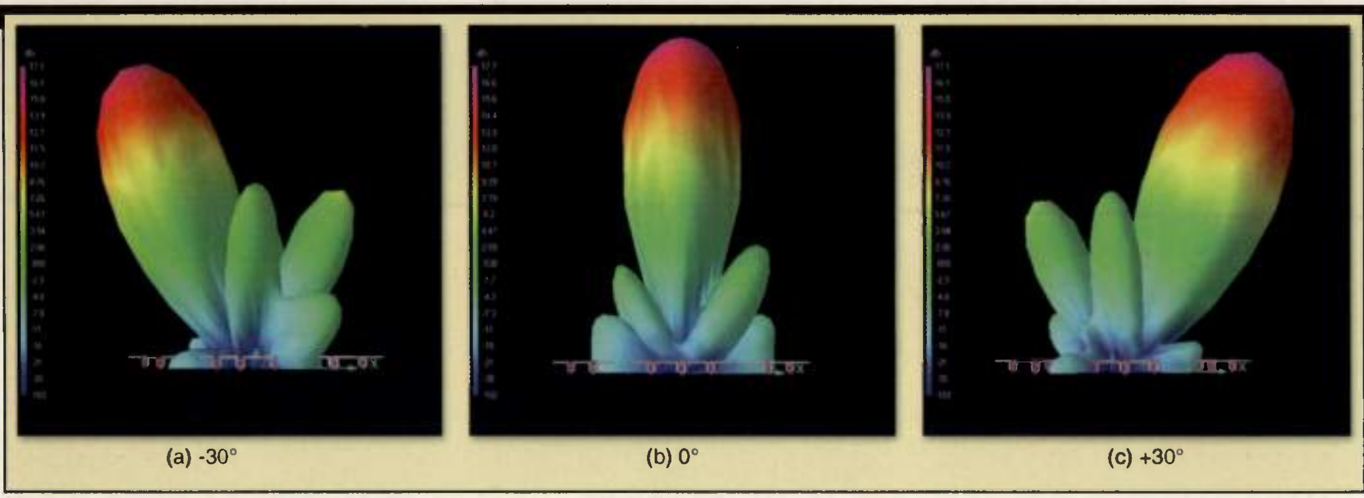

Figure 12. Simulation results of a 16-element array beam forming: (a) -30 degrees; (b) 0 degrees; (c) +30 degrees.

and at the corporate-feed split points to enhance signal quality and thereby provide ultratight control of jitter. And as we have explained, jitter management is crucial for proper phase-shifter management. RFD

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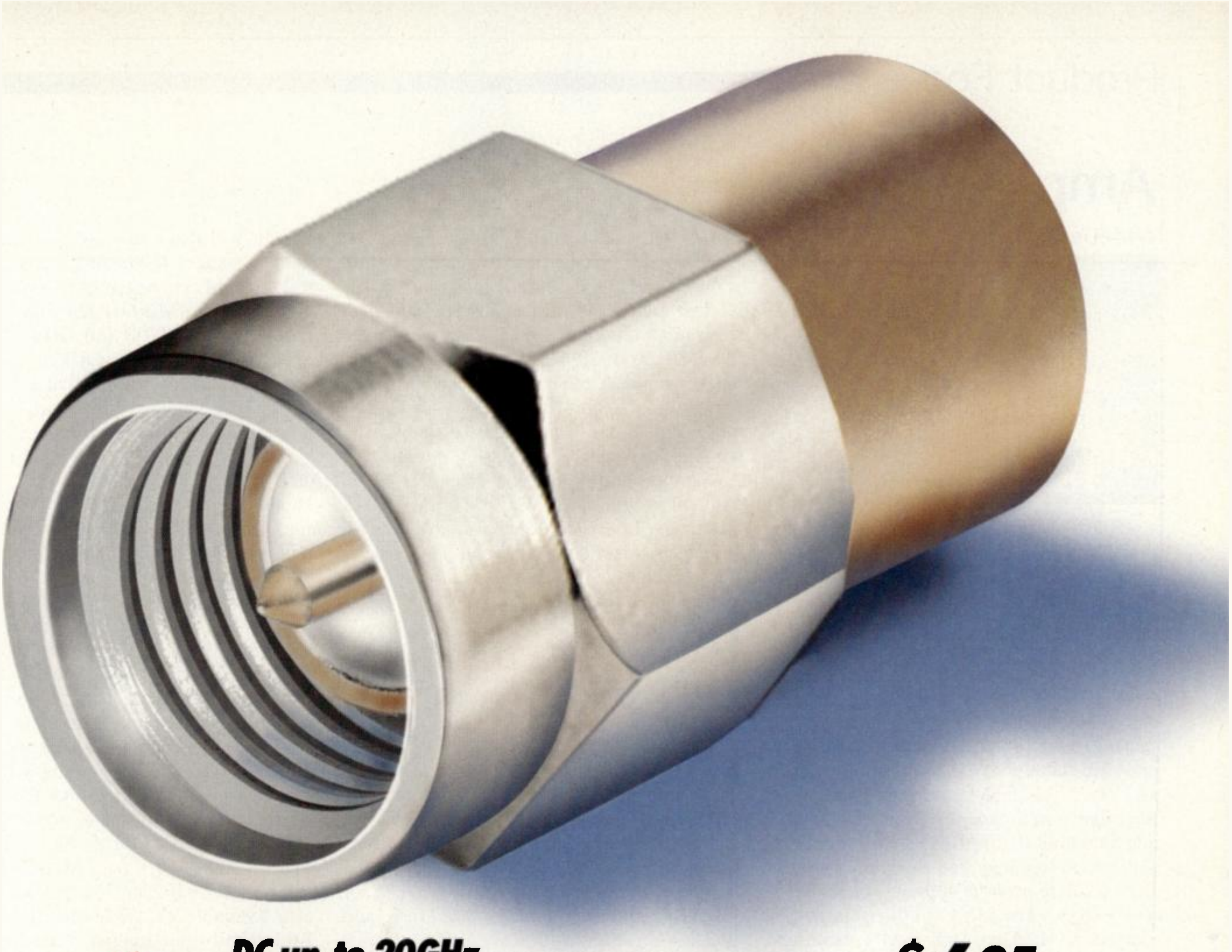
ABOUT THE AUTHOR

Fred Mohamadi is the CEO of TiaLinx Inc. He earned his Ph.D.E.E at Stanford University and an MBA at Santa Clara University. Active in the communications semiconductor business for more than 24 years, he holds seven patents and has published a large number of technical articles.



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LOUIS-50	DIN 1.0/2.3 Male	DC-2	0.125	28	21	—	—	—	—	—		11.95
ROSE-50	SMB	DC-6	1	33	30	25	20	—	—	—	—	9.95
KARN-50	Type N	DC-8	2	32	28	25	22	20	—	—	—	11.95
KARN-50-18	Type N	DC-18	2	35	30	30	28	26	20	18	—	13.95
ANNE-50L	SMA	DC-12	1	35	35	30	26	21	18	—	—	6.95
ANNE-50	SMA	DC-18	1	37	34	30	28	28	26	20	—	9.95
ANNE-50CN	SMA with Chain	DC-18	1	37	34	30	28	28	26	20	—	11.95
ANNE-50X	SMA	DC-20	1	37	34	30	30	30	30	26	20	13.95

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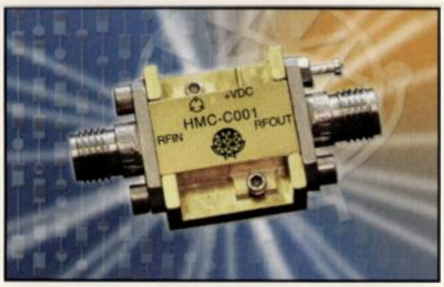
Amplifiers

Wideband LNA module



Hittite Microwave Corporation has introduced the first product in its new Connectorized Module product line. The HMC-C001 wideband LNA module is suitable for military EW/ECM, space, test equipment, wideband telecom, microwave radio, and industrial applications from 2 GHz to 20 GHz.

The HMC-C001 is a GaAs MMIC pHEMT low-noise distributed amplifier module that delivers a typical small signal gain of 15 dB and gain flatness of ±0.5 dB from 2 GHz to 18 GHz. The high dynamic range LNA module offers a mid-band noise figure of 2.0 dB and an output P1dB of +13.5 dBm, while its self-biased topology consumes only 65 mA from a single positive supply between +9 V and +15 V. The HMC-C001 is internally matched to 50 Ω, unconditionally stable, and has integral voltage regulation, overvoltage protection, and dc-blocked RF ports.

The HMC-C001 uses miniature, hermetically sealed housing. Field-replaceable SMA connectors are provided to allow mating with standard coaxial cable assemblies. For drop-in microstrip or coplanar circuit applications, the RF connectors can readily be removed, allowing the RF and dc pins of the module to be connected directly to a printed circuit board (PCB).

Hittite Microwave
(978) 250-3343
www.hittite.com

UMTS power amplifier module

Agilent Technologies Inc. has introduced a power amplifier (PA) module that extends battery life in mobile phones by us much as 30 minutes. The PA module is designed around Agilent's E-pHEMT (enhancement-mode pseudomorphic high-electron mobility transistor) process technology for efficiency and operates from a single-polarity power source.

The Agilent ACPM-7881 PA module features typical PAE of 46%. Higher PAE provides increased battery life even in phones with a variety of power-consuming multimedia features. The PA's high-output power capability (+28.5 dBm) overcomes power losses involved with dual-band (UMTS/GSM), single-antenna handset designs. The encapsulated surface-mount package is 4 mm x 4 mm with a 1.1-mm thickness.

The module is fully matched to 50Ω at both input and output and operates over the UMTS2100 1920 MHz to 1980 MHz frequency range. It can be operated at bias levels down to 1 V. The ACPM-7881 has 50 mA quiescent current and it can operate from voltages as low as 3.2 V (3.4 V optimal).

Samples and production quantities of the Agilent ACPM-7881 WCDMA E-pHEMT power amplifier module are available through Agilent's direct sales channel. The price is $1.30 each in 10,000-piece quantities.

Agilent Technologies
(800) 452 4844
www.agilent.com

Dual-band WLAN power amplifier

Anadigics Inc. has introduced the AWL6950 dual-band 4 mm x 4 mm indium gallium phosphide heterojunction bipolar transistor (InGaP HBT) power amplifier (PA). This PA supports the 2.4 GHz and 5 GHz bands, which allows wireless local area network (WLAN) equipment manufacturers to use a single PA for 802.11b, 802.11a, 802.11g, 802.11a/b, and 802.11a/b/g applications.

The AWL6950 provides an error vector magnitude (EVM) of 3.5% at 20 dBm in the 2.4 GHz band and 19 dBm in the 5 GHz band. The PA exhibits 31.5 dB of linear power gain at 2.4 GHz and 30 dB of linear power gain at 5 GHz. This PA offers an electrostatic discharge (ESD) protection of greater than 1 kV.

The amplifier has an integrated CMOS-voltage compatible on/off circuit for each band of operation. The PA also integrates temperature- and voltage-compensated output power detectors in the 4 mm x 4 mm package. The compact overall size enables use in applications of the smallest form factor including mini-PCI express, PDAs and cellular handsets. The AWL6950 complies with the European Union's Restriction of Hazardous Substances (RoHS) standard.

The AWL6950 is priced at $2.00 each in quantities of 100,000 units. Samples are available.

Anadigics Inc.
(908) 668-5000
www.anadigics.com

X-band, Ka-band amplifiers

M/A-COM has announced a family of Ka-band triplers, X-band variable gain amplifiers and Ka-band power amplifiers. The M/A-COM amplifier and tripler family uses a weight- and space-saving design that uses the latest advances in housing materials for the military and avionics market.

The MAAMML0016 (24 GHz to 30 GHz) and MAAMML0017 (30 GHz to 36 GHz) are Ka-band connectorized amplifiers. Built-in circuitry ensures that power supply sequencing can be in any order, for both power up and power down.

The MAAMML0018 (8 GHz 12 GHz) is an X-band variable gain amplifier. A variable attenuator is followed by an X-band amplifier. This allows total unit gain to be adjustable over a >= 28 dB range, from an applied control voltage.

The MAAMML0019 (8 GHz to 10 GHz to 24 GHz to 30 GHz), MAAMML0020 (9 GHz to 11 GHz to 27 GHz to 33 GHz) and MAAMML0021 (10 GHz to 12 GHz to 30 GHz to 36 GHz) are X to Ka-band connectorized triplers. The units consist of a tripler followed by a Ka-band amplifier and bandpass filter (BPF). The amplifier restores output signal strength, and the bandpass filter reduces out-of-band products.

The MAAMML0016, MAAMML0017, MAAMML0018, MAAMML0019, MAAMML0020, and MAAMML0021 are also available as space-qualified versions. Additionally, alternative frequency ranges, gain, output power, and supply rail configurations are available. Contact M/A-COM with your required specifications.

M/A-Com
(800) 366-2266
www.macom.com

Low-cost MMIC amplifiers

Mini-Circuits' new family of 'LEE' MMIC amplifiers offer high reliability and broadband at a low cost. These amplifiers have excellent electrical performance, with up to 17.3 dBm flat output power to 10 GHz. Five models are being introduced in this new family. They are housed in a leadless 3 mm x 3 mm low-profile MCLP package with exposed metal bottom for grounding and heat dissipation. Besides reliability, they

LOW NOISE, HIGH IP3

AMPLIFIERS

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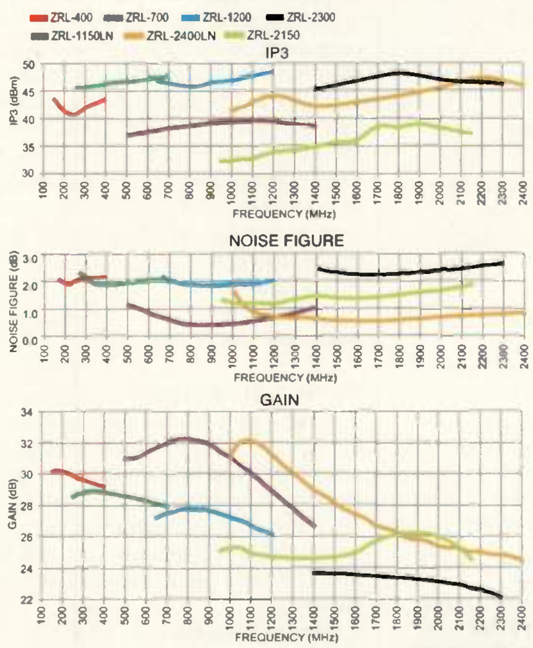

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Using Mini-Circuits award winning ZRL amplifiers, you're ready to handle just about all your high dynamic range applications across the entire 150-2400MHz band! Thanks to Low Temperature Co-fired Ceramic (LTCC) technology and balanced amplifier design, these ZRLs provide rock-solid reliability, are extremely rugged, and phenomenally low in cost. Get ahead of your competition with ZRL amplifiers from Mini-Circuits!

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SPECIFICATIONS (Typical) T=25°C

Model	Freq. (MHz)	Gain (dB)	Noise Fig. (dB)	IP3 (dBm)	Max. Pwr. Out @1dB Comp. (dBm)	Price $ea. (1-9)
ZRL-400	150-400	30	2.5	42	25.0	119.95
ZRL-700	250-700	29	2.0	46	24.8	119.95
ZRL-1150LN	500-1400	31	0.8	40	24.0	119.95
ZRL-1200	650-1200	27	2.0	46	24.3	119.95
ZRL-2150	950-2150	25	1.5	33	22.0	119.95
ZRL-2300	1400-2300	24	2.5	46	24.6	119.95
ZRL-2400LN	1000-2400	27	1.0	45	24.0	139.95

DC Power 12V DC, Current 550mA (ZRL-2150 current: 280mA).
Dimensions: (L) 3.75" x (W) 2.00" x (H) 0.80"

Detailed Performance Data & Specs Online at: **www.minicircuits.com/ZRL-SERIES.pdf**

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provide excellent repeatability. Designed for the cellular, PCS, communication receivers and transmitters, as well as for satellite communication and military applications, the pricing starts from $1.19 each, in quantities of 25.

Mini-Circuits
(800) 654-7949
www.minicircuits.com

Dual-band PA module for 3G

TriQuint Semiconductor has introduced the TQM7M60001 dual-band UMTS power amplifier module (PAM) in a 4 mm x 4 mm x 1.1 mm form factor. The module is designed to support cost-effective GSM/EDGE/UMTS (HSDPA) compressed-mode phone architectures with one antenna.

The TQM7M6001 power amplifier module features a biasing circuit optimized for low idle current consumption (below 30 mA), which results in increased handset talk time in UMTS mode. Its linearity (7 dB margin to ETSI-requirements for UMTS) offers sufficient margin for applying additional transmit channels for large-scale data transmission rates, enabling 3G phones for HSDPA (high-speed download packet access).

TriQuint Semiconductor
(503) 615-9000
www.triquint.com

AM/FM amplifier

Microtune has introduced a one-chip AM/FM amplifier, the MT1120, designed for integration into vehicle window-mounted antennas, small roof antennas or other integrated antenna systems.

The MT1120 integrates, into one device, the FM amplifier, AM amplifier, and automatic gain control (AGC) functions for the FM and AM bands. It amplifies the radio signal, compensating for the reduced performance of in-glass or small roof-mount antennas. The MT1120 offers large signal-handling capability and low-noise performance. These features, combined with its integrated AGC functionality, yield improved sensitivity and performance under difficult reception conditions, such as those resulting from weak signals or overload.

In addition, the application flexibility of the MT1120 permits system providers to optimally match varying antenna structures with different radio configurations. The amplifier is also designed to conform to the applicable specifications of major worldwide carmakers, enabling it to support automotive radio systems across global markets.

The MT1120 can amplify signals with frequencies in the 0.15 MHz to 6.2 MHz range for AM and 76 MHz to 162.4 MHz range for FM. External components determine the gain of the AM and FM amplifiers and can also be modified to extend the operating frequency of the MT1120.

Microtune
(972) 673-1600
www.microtune.com

Power amplifiers

Crescend Technologies LLC has developed an amplifier for two-way radio communications. This latest amplifier, with a C5 chassis, has been engineered to deliver reliability through advanced design techniques. The C5 employs thermal management, VSWR protection and closed loop power control.

Crescend Technologies LLC
(847) 908-5400
www.crescendtech.com

Active Components

Bipolar power transistors

The PH1090-700B from **M/A-Com** is an NPN common base Class C pulse power transistor designed for IFF and other avionics applications in the frequency band of 1030 MHz to 1090 MHz. Saturated output power exceeds 700 Wpk at 32 μs pulse width and 2% duty cycle. Guaranteed gain is 7.5 dB at 50% collector efficiency, and under rigorous Modes-S pulse burst conditions, the device delivers more than 450 Wpk saturated output power with 55% collector efficiency.

The silicon bipolar line-up consisting of the MAPRST0002 and the PH1214-300M deliver typical gain of 18 dB at 150 μs pulse width and 10% duty cycle. The saturated power output typically exceeds 360 Wpk, and guaranteed collector efficiency for each device is 50%, with typical values in the high 50s to low 60s. The line up was designed to support ATC pulsed radar applications in the 1200 MHz to 1400 MHz frequency band.

The silicon bipolars consisting of the MAPRST1214-06UF, MAPRST1214-30UF and MAPRST1214-150UF were designed for ultralong pulse radar applications in the 1200 MHz to 1400 MHz bandwidth. They provide 150 Wpk. This line-up delivers a minimum 24 dB gain with minimum collector efficiencies of 45% for the 150 UF and 30 UF (typical >50%) and 40% for the 6 UF. Devices are rated for operation up to 6 mS pulse width and 25% duty cycle and are assembled in hermetic ceramic/metal packages for ultralow thermal resistance.

M/A-COM
(800) 366-2266
www.macom.com

Microwave Technologies

Band reject filter

Lorch Microwave's 5BRX-2441/X78-SR is a hybrid band reject filter with bidirectional inputs. The filter features a 3 dB bandwidth of 220 MHz. The notch depth is 45 dB from 2402 MHz to 2480 MHz. The VSWR is 2.0:1 from dc to 3500 MHz, excluding the notch area. The physical size is 1.5 x 0.80 x 0.50, excluding SMA female removable connectors.

Lorch Microwave
(800) 780-2169
www.lorch.com

Publications

GSM ciphering

Tektronix is offering an electronic technical brief that highlights the principles of GSM protection and the evolution to UMTS security.

In a digital mobile network, the subscriber is exposed to several basic attacks and needs to be protected against them—eavesdropping, unauthorized identification, unauthorized usage of services, offending the data integrity and observation. The brief contains details of the UMTS security architecture, followed by a short abstract about protocol testing when ciphering is active.

Tektronix
(800) 833-9200
www.tektronix.com

Interconnect catalog

Aries Electronics Inc. has published an eighth edition shortform catalog covering a range of interconnection and packaging products.

The 12-page catalog includes the first side-stackable BGA socket available on the market. Designated the pin-ball socket, this device can be soldered side by side, directly to the existing footprint of a PC board, improving packaging density. The socket incorporates Aries' spring probe technology.

Also detailed are Aries' Correct-A-Chip technology and products that enable designers to convert virtually any package type or footprint to any other. Typical Correct-A-Chip products include DIP-to-PLCC adapters, standard DIP adapters, DIP-to-SOIC adapters, SMD-to-DIP adapters, PGA adapters, and countless other "from-to" configurations while enabling designers to upgrade without board redesign or rework.

Also included in the catalog are data and product information on Aries' high-frequency RF test sockets, which use the company's patented Microstrip Contact System. Aries' line of BGA products for chip scale packaging is also covered in the catalog, as are LGA sockets, test and burn-in sockets, display sockets, cable jumper assemblies, DIP/SIP sockets and headers, programming devices and other socket packages.

Aries Electronics Inc.
(908) 996-6841
www.arieselec.com

Test and Measurement

VXI carriers

Acqiris has introduced two intelligent VXI carriers that provide a transparent interface between the PXI/CompactPCI digitizers and VXIbus via an onboard PowerPC processor with firmware. The single-width, C-size IX200 and IX202 intelligent VXI carriers allow the full range of Acqiris PXI and CompactPCI modules, previously used only in PXI and CompactPCI systems, to be directly inserted into a VXI system, a well-accepted platform in automated test equipment (ATE) and defense/aerospace functional test applications.

The ability to replace discontinued VXI waveform analyzer and oscilloscope modules in existing ATE systems by interfacing PXI/CompactPCI components to VXI provides users with an increased return on investment as well as a significantly improved life cycle for high-speed acquisition and mixed signal test application systems. The IX200, which accepts one 6U PXI/CompactPCI module, can be used with any of Acqiris' three new V-Class high-speed digitizers, the DC271A, DC241A, and DC211A, which now offer switchable 50 Ω/1 MΩ input impedance. The DC271A features four channels, each of which can synchronously acquire signals at rates of up to 1 GS/s. The DC241A offers two channels, each with up to 2 GS/s sampling, and the single-channel DC211A provides 4 GS/S sampling. Using channel interleaving, the DC271A and DC241A achieve the same 4 GS/s single-channel performance offered by the DC211A. The modules combine their sampling rates with a 1 GHz bandwidth at 50 Ω, and 300 MHz at 1 MΩ input impedance. The DC271A, DC241A, and DC211A include 128 kpoints, 256 kpoints, and 512 kpoints of acquisition memory respectively, and are optionally upgradable to up to 8 Mpoints, 16 Mpoints, and 32 Mpoints. The IX202 has two adaptor

0.5 to 2000MHz MIXERS

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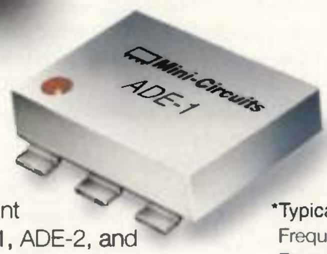

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actual size

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*Typical Specifications:	ADE-1	ADE-2	ADE-11X
Frequency LO/RF (MHz)	0.5-500	5-1000	10-2000
Frequency LO/IF (MHz)	DC-500	DC-1000	5-1000
LO Level (dBm)	7	7	7
IP3 (dBm)	15	20	9
Conv. Loss (dB)	5.0	6.67	7.1
L-R Isolation (dB)	55	47	36
L-I Isolation (dB)	40	45	37
Price $ea. (Qty. 25)	*2.49*	*2.49*	*2.49*
Dimensions: L.310"xW.220"xH	.162"	.112"	.112"

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slots that accept 3U PXI/CompactPCI modules. The lower slot is dedicated to an Acqiris product such as the DC140 dual-channel 1 GHz high-speed PXI digitizer, acquiring data at up to 2 GSps.

Pricing for the IX200 and IX202 intelligent PXI/CompactPCI carriers starts at $4990. Delivery is 10 weeks ARO. Pricing for the DC271A, DC241A and DC211A V-Class high-speed digitizers starts at $9990. Delivery is six weeks ARO.

Acqiris
(845) 782-6544
www.acqiris.com

Time and Frequency

GaAs voltage-controlled oscillator

Mimix Broadband Inc. has introduced a gallium arsenide (GaAs) hetero-bipolar transistor (HBT) monolithic microwave integrated circuit (MMIC) voltage-controlled feedback oscillator (VCO), which uses an on-chip filter to provide the necessary oscillation conditions. The circuit consists of a linear Lange-coupled phase-shifter, a Lange-coupled quadrature generator, a differential amplifier, a four-quadrant I/Q modulator, and an output buffer differential amplifier. This device also contains a frequency divider (divide-by-four) for phase-locking and an output buffer amplifier. From 5.5 GHz to 8.4 GHz, this VCO achieves +4 dBm fundamental output power and +1 dBm divide-by-four output power.

This VCO, identified as 9OSC0315, is suited for wireless communications applications such as millimeter-wave point-to-point radio, local multipoint distribution services (LMDS), and SATCOM. This VCO technology has been issued a patent in the United States, Europe and Japan.

Mimix performs 100% on-wafer dc and output power testing on the 9OSC0315, as well as 100% visual inspection to MIL-STD-883 method 2010. The chip also has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process.

Engineering samples are available from stock, and production quantities are available six to eight weeks ARO.

Mimix Broadband Inc.
(281) 988-4600
www.mimixbroadband.com

5 GHz VCOs

Crystek Crystals Corporation has expanded its line of high-performance voltage-controlled oscillators (VCOs) with a new 5 GHz model in a 0.5 inch x 0.5 inch standard SMD package. The CVCO55BH-5256-5356 VCO generates a frequency range of 5256

MHz to 5356 MHz with a tuning voltage range of 1 VDC to 4 VDC.

The VCO has a low phase noise performance of -86 dBc/Hz at 10 kHz offset typical and excellent linearity throughout its tuning range. The model CVCO55BH-5256-5356 exhibits an output power of 0±2.0 dBm into a 50 Ω load with a supply of +5 Vdc and a typical current consumption of 25 mA. Pushing and pulling are minimized to 5 MHz/V and 4 MHz, respectively. Second harmonic suppression is -10 dBc typical.

Crystek Crystals Corp.
(800) 237-3061
www.crystek.com

Digitally tuned VCXOs

Cardinal Components Inc. has introduced a digitally tuned VCXO (CDVP). The CDVP offers higher available frequencies (1 MHz to 200 MHz), greatly reduced sample and production lead-times and a device that can aid in system tolerancing.

The digitally tuned CDVP series is available in a 9.6 mm x 11.4 mm surface-mount package and operates from a 3.3 V power supply. Available with factory-programmed center frequencies from 1 MHz to 200 MHz, it can be tuned over a -70 ppm to +120 ppm range. The CDVP maintains a ±50 ppm stability over an operating temperature of -40° C to +85° C. Frequency tuning changes are accomplished via a single write over the devices I2C interface. The CDVP allows the user to implement PLL systems 100% digitally, eliminating the need for analog and interface circuitry.

Cardinal Components
(973) 785-1333
www.cardinalxtal.com

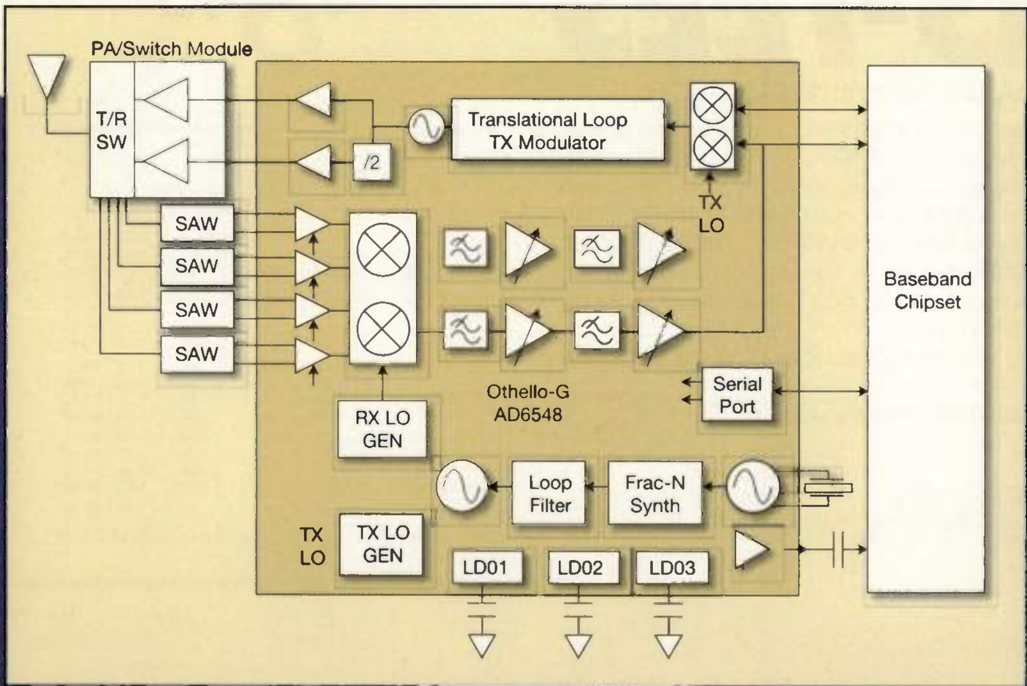
Single transceiver chip supports full quad-band operation

Prompted by growth in the wireless marketplace, **Analog Devices** has unveiled a transceiver chip that shrinks the radio size in cellular telephones to as little as 1.5 square centimeters. The AD6548, the latest addition to its Othello family of direct-conversion transceivers for GSM/GPRS handsets, enables a complete quad-band radio that is 30% smaller than anything available on the market, according to ADI. Also called Othello-G radio, it supports full quad-band operation and integrates virtually all the necessary components, such as voltage-controlled oscillators (VCOs) and the associated tank circuits, phase-locked loop (PLL) filters, and power management circuits, for a complete cost-effective, ultracompact cellular handset radio design. The only external components required for a complete radio design are the receive surface acoustic wave (SAW) filters, power amplifier, transmit/receive switch, and a few passives. Othello-G features four fully integrated programmable gain differential low-noise amplifiers (LNAs) for full quad-band (GSM850/900/1800/1900) support. The AD6548 uses a single integrated local oscillator (LO) VCO for receive and transmit circuits. The LO is generated with a fast-locking fractional-N PLL synthesizer with integrated loop filters, Tx and Rx VCOs and tank circuits (see the figure). The synthesizer lock times are optimized for GPRS applications up to and including class 12.

To dramatically reduce the radio bill of material (BOM) cost, the synthesizer integrates a loop filter and incorporates a complete reference crystal calibration system. The translation-loop transmitter architecture eliminates the need for external filtering between the transceiver and power amplifier. In addition, the AD6548 includes on-chip voltage regulators with independent power-down controls, enabling direct-to-battery connection, minimizing power consumption, and eliminating the need for external regulator components. In fact, according to the maker, the Othello-G radio chip enables a fully functional reference design with approximately 75% fewer components than its previous version.

Implemented in 0.35 micron BiCMOS process, the AD6548 offers sensitivity in the -109 dBm to -110 dBm range for 2.4% bit error rate. Other key specs include 77 dB of gain control range, 26 MHz crystal frequency and 10 microamperes maximum power-down current (battery voltage present, regulators in shutdown mode, registers kept alive). Operating voltage range for the radio chip is 2.9 V to 5.5 V. The specified temperature range for the device is -20° C to +85° C. Sampling now, the AD6548 comes in a 32-lead LFCSP package and is priced at $3, in 10k units.

Analog Devices Inc.
(781) 937-1428
www.analog.com



Log-amp performs advanced RF controls

By Ken Yang

The logarithmic amplifier (log-amp) is often used as an RF power-sensing device. Because of its low cost and wide dynamic range, it is commonly employed as a demodulator in ASK and FSK radio receivers. Today, the log-amp has expanded its role to include automatic gain and power-control loops.

The basic purpose of a log-amp is to convert an RF input signal to an output voltage proportional to the log of RF power. Modern log-amps accomplish this task with exceptional dynamic range, and their operation is simple. Inputs are single-ended or differential, and the detector outputs connect to the non-inverting terminal of an internal op-amp or transconductance amplifier. The integrated op-amp allows a user-adjustable slope and an easily implemented closed-loop operation for power-control applications. Output voltage is proportional to the log of the input power. Thus, the RF input power is calculated as follows:

$$P_{RFIN} = \frac{V_{OUT}}{SLOPE} + P_{INT} \qquad \text{Eq. 1}$$

$$V_{OUT} = SLOPE(P_{RFIN} - P_{INT}) \qquad \text{Eq. 2}$$

where P_{RFIN} is the RF input power in dBm, P_{INT} is the zero-volt intercept point in dBm, and SLOPE is the detector slope in mV/dB.

RF transmitter applications should maintain constant output power regardless of part-to-part variations or changes in supply voltage and temperature. That capability is important for power amplifiers operating near the saturation region (P1 dB compression point), where the gain drops as output power increases.

An automatic gain- or power-control loop employs a log-amp as shown in Figure 1, where a directional coupler connects the power-amplifier output to the log-amp input. The log-amp then monitors the output power and provides a dc voltage output to the error amplifier, which compares against a reference level. The error-amplifier output drives the power amplifier's gain input until the dc voltage derived from the output power equals the reference voltage applied at SET. Operating in a closed loop, the power amplifier maintains a constant output power that is independent of external variations. Output power is easily changed, however, by changing the reference voltage at SET.

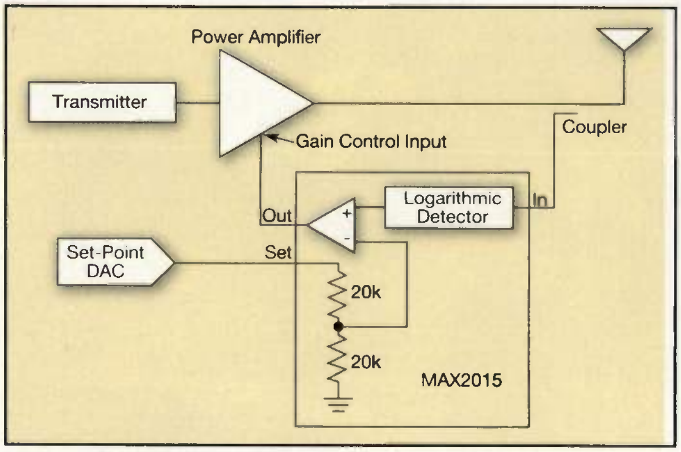


Figure 1. Operating in a closed loop, the power amplifier output is maintained constant by the MAX2015 even while operating near the compression point.

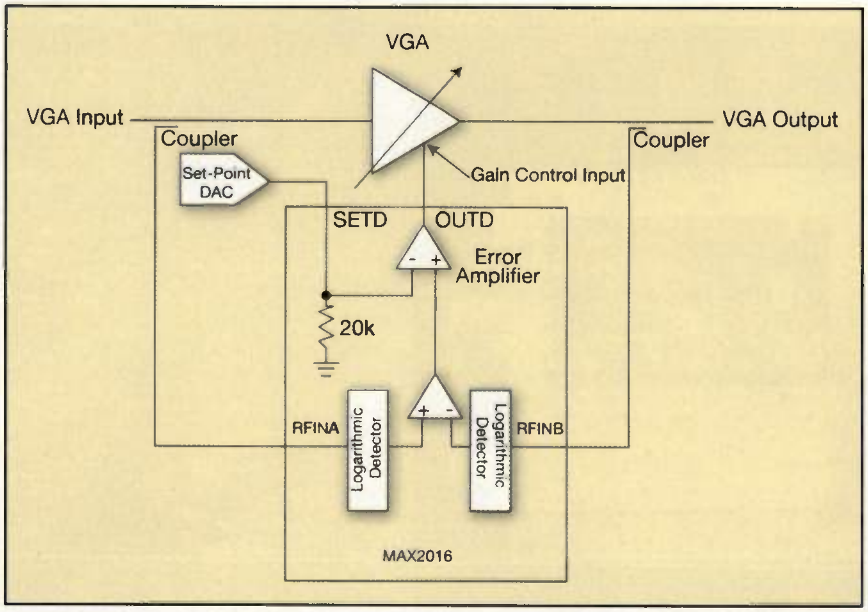


Figure 2. This dual log-amp regulates the variable-gain amplifier (VGA) to maintain a constant gain.

For applications that must regulate gain instead of power, the Figure 2 circuit maintains constant gain in the face of changes in supply voltage, temperature and output power. By monitoring the input and output power using two log-amps, you achieve gain regulation. Internal to the MAX2016 is a difference amplifier that produces a voltage proportional to the power difference or gain, and that voltage is fed to the error amplifier for comparison. The error-amplifier output then drives the AGC input of the power amplifier to maintain constant gain.

Steady advances in integrated circuit technology have enabled log-amps to expand their role beyond that of simple power detection and demodulation. They now perform advanced RF controls such as power-control loops and gain-control loops. Such RF control systems ensure that a system is operating with peak performance. RFD

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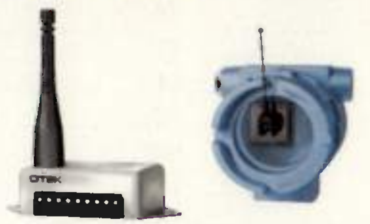

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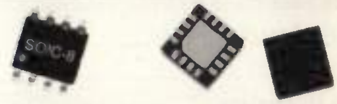

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