

INSTRUCTION MANUAL
FOR
SYNCHRONOUS PATTERN DISTORTION
GENERATOR, MODEL DT-120

PART II

THEORY AND MAINTENANCE

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Chapter 1

INTRODUCTION

1-1. Scope:

a. This instruction manual describes the Synchronous Pattern Distortion Generator Model DT-120. It is provided in two parts: Part 1 - Operation, and Part 2 - Theory and Maintenance. One copy of Part 1 is mounted inside the cover of the portable case.

b. Hereafter the Synchronous Pattern Distortion Generator, Model DT-120 will be referred to as the DT-120.

1-2. Purpose and Use:

a. The DT-120 is a portable test instrument designed to supply synchronous test patterns for testing data systems and equipment.

1-3. Description:

a. Refer to figures 1, 2 and 3. The DT-120 is a portable instrument fitting into a case measuring 7 inches high by 9 inches wide by 15 inches deep and weighs approximately 16 pounds. Removal of the case cover reveals a front panel with all the operating controls and a cut out compartment on the bottom for storage of the line cord. Part 1 of the instruction manual is located inside the case cover. The unit is held in the case by four (4) front panel screws.

The DT-120 is constructed of a main chassis into which six circuit Modules are plugged. Five of the Modules fit into the rear of the unit and a sixth (the pattern matrix) is plugged in behind the front panel. The five rear Modules are each held secure by means of a 6-32 x $\frac{1}{4}$ " screw from the top of the chassis into the module frame. The matrix module is secured by a combination of spring clips located next to the connector and a cover over the top of the main unit.

1-4. Technical Description:

a. The DT-120 is completely self contained in its own portable case. The circuit design is completely solid state.

Its pattern may be selected for 33-35-36, or 40 bits in length, covering all codes with characters of twelve bits or less. The pattern itself is programmed by means of plug-in diode holders into a matrix board. The arrangement provides a semi-permanent pattern with the flexibility of being able to easily change to another pattern.

The DT-120 also generates a Steady Mark, Steady Space, 1:1 Reversals, and 2:2 Reversals. Marking and Spacing Bias distortion may be introduced in 5% steps from 0 to 45%.

The timing is controlled from a crystal controlled oscillator with an accuracy and stability of 1 part in 10^4 per day to provide operation at 75, 150, 300, 600, 1200, 2400, and 4800 bits per second. Provisions are made for adding four more crystal controlled speeds.

The polar output signal is an isolated \pm 12 volts @ 10 ma. with an impedance of 600 ohms, negative constituting a mark. A zero center 15-15 ma. meter is used to monitor the output.

A polar timing signal operating at twice the output signal rate going negative in the center of each bit of the output signal is provided.

1-5. Technical Characteristics:

Message Selection:

1. Steady mark
2. Steady space
3. Pattern - Selected for 33-35-36 or 40 bits
4. 1:1 Reversals
5. 2:2 Reversals

Forty Bit Pattern:

Bits are selected by means of a plug-in diode holder into a Programming Board. Thirty diodes mounted in individual holders are supplied with storage of excess diodes in extra points of the programming board.

Speeds:

The following speeds in bits/sec are supplied from a crystal controlled oscillator with an accuracy of 1 part in 10^4 and a stability of 1 part in 10^4 per day.

75,150,300,600,1200,2400 and 4800 bits per second. A switch will select the output rate.

Provision is made for four more speeds to be added. This may be accomplished by adding a new crystal and capacitor for each speed and adding jumpers on the speed switch.

Distortion:

Marking or Spacing bias may be introduced in 5 percent steps from 0 to 45 percent to the pattern or reversal signals. The Distortion is produced digitally and is independent of the selected speed of operation.

Accuracy:

To 1% time duration.

Front Panel Test Points:

Test points for measuring power supply voltages are provided on the front panel.

Output:

The output signal is isolated \pm 12 volts at 10 ma. Minus constitutes a mark condition. The output impedance is 600 ohms. A zero center 15-15 ma meter is included in the output leads.

Terminations:

The output signal is terminated on a jack on the front panel of the pattern generator with the signal on the tip of the jack and the common point of plus and minus power supplies on the sleeve. In parallel with the jack are two binding posts to also terminate the signal output.

In addition to the signal output a synchronizing signal is brought to a jack and a binding post on the front panel. The connection is to the tip of the jack providing \pm 12 volts at 10 ma. The signal operates at twice the bit rate, going negative in the center of each bit of the output signal.

Power:

115v \pm 10% 50/60 cps approximately 10 watts.

Operating Temperature Range:

0° to 50°C continuous.

Mechanical:

a. The unit is mounted in a portable metal case approximately 9" wide x 7" high x 15" deep with a handle for carrying and a removable cover. Weighs under 16 pounds.

b. Plug-in modular construction using standard logic sub-modules.

THEORY OF OPERATION2-1. General:

a. Introduction.

The DT-120 uses computer logic circuit techniques to produce a Programmed Pattern with controlled amounts of Bias distortion for use as a standard source of data test signals.

The majority of circuits in the Message Generator are repetitive and fall into two classes, bistables (flip-flops) and gates. A detailed analysis of these circuits is provided here and should be used for reference when consulting the remainder of the theory.

b. Bistables (flip-flops)

A typical flip-flop is shown in figure 4. The circuit is called bistable because it has two stable states. The circuit is in a stable state with Q1 conducting (on) and Q2 non-conducting (off) or vice-versa. Assume Q1 on and Q2 off. The collector of Q2 is clamped through CR4 to -9 volts. This negative voltage causes current to flow through R6 to the base of Q1 to saturate it. Some of the current flows through base resistor R3 to the +15 volts supply, to maintain a negative base to emitter voltage capable of saturating Q1. The saturation current of Q1 causes a voltage drop across R1 which places the collector of Q1 near ground (approx. -.2v). The voltage divider formed by R2 and R7 from ground to positive 15 volts places the base of Q2 positive thereby insuring turn-off. Resistors R3 and R7 absorb collector leakage current I_{cbo} during the off condition to insure that either transistor can be reverse biased up to temperatures of 50° Centigrade. The resulting condition is stable since Q1 - on is forced by Q2 - off to remain that way and Q2 - off is forced by Q1 - on and the positive bias from R7 to remain that way. The circuit operation is identical with Q1 turned off and Q2 turned on.

A change in condition is usually accomplished by triggering the "ON" transistor off. The regenerative action of the circuit then turns the "OFF" transistor on. For example to turn Q1 off a positive pulse is applied to C1 where it is differentiated by C1R4. The resulting positive spike passes through CR1 to the base of Q1 to turn it off. Capacitors C2 and C4 help to speed up the regenerative action which then takes place while C1 is turning off and Q2 is turning on. When the flip-flop is used in a counting function, input capacitors C1 and C3 are tied together. The input pulse is steered to the off transistor by the differentiating resistors R4 and R8. The collector of Q1, the "ON" transistor, is at ground thereby allowing the trigger to go positive at the junction of C1R4 while the collector of Q2 is at -9 volts keeping the trigger at C3R8 at a net negative potential. This system is called collector steering.

When a flip-flop is not used for counting, but rather as a storage element resistors R4 and R8 may be returned either to the collectors or to external steering signals. Several trigger circuits consisting of a capacitor, resistor, and diode combination may be used for each transistor of the flip-flop.

c. Gates

Two types of logical gates are used in this unit, the transistor NOR gate and the diode AND gate. The most frequently used gate is the transistor "NOR" gate shown in figure 5. It consists of a transistor Q1, its collector resistor R1, a base biasing resistor R2 (mainly for operating at elevated temperatures) and a number of input resistors which may range from one to five. The gate operates so that a single negative (-9 volts) input will cause Q1 to saturate and bring its collector to ground. On the other hand all inputs must be positive (ground potential) to cause Q1 to turn off and provide a negative output. Thus the gate will go negative when there is positive coincidence on all inputs, a characteristic which makes it an AND gate, or the gate will go positive when any of the inputs goes negative, a characteristic which makes it an OR gate. The circuit then is used to perform both the AND and the OR logical functions by proper choice of input signals.

Capacitor C1, a small capacitor, is sometimes used to speed up the operation of a gate during the turn-off time.

The diode AND gate shown in figure 5 is another form of the logical AND gate. Unlike the transistor gate described above it does not invert the signal. Any negative (-9 volts) signal on one of the inputs will cause a negative output through a forward biased diode regardless of the signals on the other three. If all the inputs are positive (ground) then the output will go positive.

d. Distortion

The DT-120 produces both marking and spacing bias distortion. Refer to figure 6 for output signal waveforms showing the effects of distortion. Line 1 shows an undistorted signal. Line 2 shows the same signal with 25% marking bias. The mark-to-space (M/S) transitions are used in this discussion as a reference and are therefore shown undistorted. The space-to-mark (S/M) transitions occur early by 25% of a bit time, producing longer than normal length mark pulses and shortened space pulses. Line 3 shows the signal with 25% spacing bias. The S/M occurs late by 25% of a bit time, resulting in shortened mark pulses and lengthened space pulses.

2-2. Block Diagram Theory of Operation:

Refer to figure 7, a Block Diagram of the DT-120.

The heart of the unit is a crystal oscillator operating at a frequency of 192,000 KCPS for the standard speeds of 75,150,300,600,1200, and 4800 Baud. An additional 4 crystal holders are provided in module 1 to allow the unit to be set up for other speeds.

The crystal oscillator output is coupled through an isolating emitter follower to a binary (both in module 1). The binary provides a squared-up standard amplitude signal at 96,000 KCPS to drive the count down chain.

The standard speeds are all related to each other by multiples of 2 so a binary counting chain is used to provide the proper frequency signal for each operating speed. This chain consists of 6 binaries; 2AF, 2BF,

2CF, 2DF, 2EF, and 2FF. Switch section S2A selects the proper frequency signal which passed through gate 2GGQ1 to binary 2HF which divides the frequency by 2. The signal frequency at this point is 20 times the output rate.

Binarys 2IF, 2JF, 2KF, and gate 2GGQ2 form a decade divider which divides the frequency by 10. This signal is further divided by 2 by binary 2LF to produce the desired bit rate timing.

The output signals from each of the binarys in the decade are applied through the Percent Distortion switch S3 to a diode AND circuit to produce a delay pulse. The position of this delay pulse within a bit time is programmed into the wiring of S3. Thus the delay pulse moves in 5% steps as S3 is advanced.

Bit rate timing is supplied to the timing output driver which provides a 12 volt, 600 ohm, polar signal.

Bit rate timing is also supplied to the input of a three stage counter consisting of binarys 3AF, 3BF, and 3CF. The outputs from these binarys are decoded by a group of eight NOR gates to sequentially scan the eight columns of the matrix from A to H.

NOR gate 3DGQ2 detects the sampling of column H and provides a count input to another three stage counter consisting of binarys 4AF, 4BF, and 4CF. This counter is connected with feedback to reduce the normal count cycle of eight down to a count of five. A group of four gates in addition to a signal taken directly from the counter scan the five rows of the matrix.

At each intersection of a row and column on the matrix a diode may be inserted to form an electrical connection between that row and column. At any time one of the five rows is being selected, it has a negative voltage applied. This signal is coupled through the diodes in the selected row to the corresponding columns. The columns provide a fourth input to the column distributing gates and when the column is negative the associated gate is not allowed to go into coincidence.

The output from each of the column distributor gates are combined by an OR circuit into a single signal.

A reset circuit composed of a diode AND circuit and a transistor amplifier is provided to shorten the pattern from its normal 40 bit length to 33, 35, or 36 bits. One input to the AND circuit comes from the fifth row driver. The other input can be strapped to column gate B, column gate D, or column gate E. When the appropriate column gate is scanned by the distributor, coincidence is obtained in the diode AND circuit and the distributor counters for both rows and gates are reset to scan position 1A (row 1 column A). When a 40 bit message is used, the reset circuit is strapped to ground to prevent its operation. When dot cycles are selected as the generator output, switch section S1A grounds the reset circuitry to prevent it from functioning.

Switch section S1C selects one of five inputs to the distortion and output circuits. Distortion is produced by the cooperative actions of the sampling binary 4HF, the delay binary 4IF, and the output binary 4JF.

When zero distortion output is set on switch S3, the distortion circuits are bypassed and the selected output signal is sent directly to the output driver through NOR gate 4GGQ2.

The signal output driver is identical to the timing output driver and provides a 12 volt, 600 ohm, polar signal into a 600 ohm line.

A 15-0-15 milliamp meter is provided to monitor the output current. Red lines on this meter indicate the nominal signaling current of 10 milliamperes.

NOTE: In this theory of operation as well as in Chapter 3 Maintenance and Alignment, submodules, submodule pin numbers, components, and module connectors are referred to by a coding system as described in Chapter 4 Parts List. This system provides a unified means of component location as well as component identification. It is important to become familiar with this system before going on with the detailed theory of operation.

2-3. Module 1 Crystal Oscillator:

Refer to figures 8A and 8B for a schematic and component layout of Module 1.

The basic timing is produced by a transistor Pierce oscillator consisting of transistor Q1 and its associated biasing networks. Any one of five crystals may be switched into the circuit by switch section S2B. Only one crystal (Y1) is supplied as original equipment. Piston capacitors C1B, C2B, C3B, C4B, and C5B are provided to trim out the circuit tolerances and adjust the operating frequency to the exact crystal frequency.

Transistor Q2 acts as an emitter follower to provide load isolation for the oscillator.

Transistors Q3 and Q4 form a binary circuit which divides the crystal frequency in half and produces fast rise time square signals to actuate the count down in Module 2. Note that this binary has in addition to the usual circuit parameters two extra diodes CR5 and CR6 which are shunted across the trigger steering resistors R7 and R14. These diodes provide the trigger capacitors C9 and C10 with a low impedance recharge path and substantially increases the speed capability of the binary.

In addition to the timing circuits, Module 1 also contains the Distortion Delay AND gate. Operation of this gate is explained in paragraph 2-6.

2-4. Module 2 Count Down:

Refer to figure 9A for a Block Diagram of Module 2 and to figures 9B and 9C for wave forms associated with these circuits.

Module 2 contains 11 binary counter stages. The first six stages 2AF, 2BF, 2CF, 2DF, 2EF, and 2FF form a simple binary counter. Outputs from each of these stages as well as the input signal to binary 2AF (see figure 9B) are sent to the speed switch S2 where the proper frequency is selected to operate the unit. Gate 2GGQ1 amplifies the selected signal and drives the remainder of the count down circuits.

Binaries 2HF, 2IF, 2JF, and 2KF form a decade divider. The decade consists essentially of four cascaded binary stages with a feed back loop superimposed to reduce the count from 16 to 10. Line 2 of figure 9C shows the input wave form at 20 times the selected bit rate. This signal causes binary 2HF to reverse its state for each cycle of input signal as shown on line 3 of figure 9C. The input circuits (pins 10 and 19) of 2HF respond only to the positive going transitions of line 2 thus producing at the output (pins 12 and 17) of 2HF a signal whose frequency is one half that of the input.

In a similar manner the second decade stage 2IF is triggered by the output of 2HF. Binary 2IF changes its state each time it receives a positive going transition from 2HF, producing the waveform of line 4. Identical connections are made from binary 2IF to binary 2JF and from binary 2JF to 2KF. Line 1 on figure 9C shows the binary count during each count interval. Note that starting at zero (0000) the count increases in pure binary fashion to eight (0001) requiring nine input cycles to reach this number. At this point the feed back loop operates.

The count would continue to binary fifteen before repeating except for the action of the feed back circuit. The Q2 gate of submodule 2GG has two inputs. One connected to 2HF pin 17 and one connected to 2KF pin 12. Referring to figure 9C note that when the binary count of eight (0001) 2KFQ2 (output pin 17) is negative, 2KFQ1 (output 12) would be positive. Thus both inputs to 2GGQ2 (pins 9 and 11) will go positive when the count of eight (0001) is reached and the gate transistor will turn off causing its output (pin 12) to go negative. This wave form is shown on line 7 of figure 9C.

The output (pin 12) of 2GGQ2 is connected to the set on inputs (pin 21) of 2IF and 2JF. These inputs are sensitive only to positive going transitions so that the negative transition produced when the count of eight is reached has no effect on the decade. When the next count into the decade changes binary 2HFQ2 to its negative state, 2GGQ2 turns back on and its output goes positive resetting binaries 2IF and 2JF. Thus on the tenth count into the decade, the binary count is changed to 15 (1111) not nine (1001) as it would be for a straight binary counter. The decade will cycle from 15 (1111) to zero (0000) on the next count completing the counting cycle. Notice that the output of 2KF (line 6) makes one complete cycle for each ten cycles of the input (line 2) wave form.

The output of binary 2KF is used as the input to binary 2IF which provides square wave signals at the desired bit rate.

2-5. Module 3 Column Distributor:

Refer to figure 10A for a block diagram of Module 3 and to figure 10B for the wave forms associated with this module.

The column distributor consists basically of a three stage binary counter made up of binaries 3AF, 3BF, and 3CF, and the decoding gates 3GG, 3HG, 3IG and 3JG. Ancilliary circuitry for controlling the pattern length plus a gate for triggering the row distributor is on submodule 3DG.

The three binaries are interconnected to form a standard binary counter. Wave forms for the three stages are shown as lines 1,2, and 3 of figure 10B.

The column decoding gates 3GGQ1, 3GGQ2, 3HGQ1, 3HGQ2, 3IGQ1, 3IGQ2, 3JGQ1 and 3 JGQ2 serve to convert the binary coding provided by the 3 stage counter into a "one-hot " code. That is, a code in which one and only one of the eight transistors is cut-off during each hit interval. These AND logic gates use PNP transistors so that a cut-off transistor supplies a negative voltage at its output. Lines 4 through 11 of figure 10B show the sequence of outputs from the decoding gates.

Note that there is a fourth input to each decoding gate. This input is the matrix column. If this input is negative, the transistor will be held in a conducting condition even though the three counter inputs achieve coincidence. Thus the output from each decoding gate is controlled both by the counter to give timing and by its associated matrix column to give the proper pattern of marks and spaces.

The outputs from each of the decoding gates for matrix columns A through D are mixed in a logical OR circuit formed by 3KGQ1. Similarly the outputs from the decoding gates for matrix columns E through H are mixed in a logical OR circuit formed by 3KGQ2. The outputs of these two gates are combined in a logical OR combination by having their collectors tied together. Thus when any of the first four decoding gates shuts off, its output will go negative turning on 3KGQ1 and grounding the pattern output connection to module connector pin 3X. Also when any of the second four decoding gates shuts off, its output will go negative and turn on 3KGQ2 which will also ground the pattern output connection to module connector pin 3X.

Gate 3DGQ2 detects the sampling of matrix column H and provides a signal to activate the row distributor contained in module 4.

When a 40 bit pattern is used, the pattern length strap is placed on a grounded terminal which prevents any action by reset gate 3DGQ1.

When a shorter pattern is desired, the pattern length strap is placed on one of the other terminals. Now a logical AND circuit is formed by diode 3CR4, resistor 3R1 and the diode chosen by the pattern length strap. Let us assume the strap is placed on the terminal for a pattern length of 33 bits.

The input to gate 3DGQ1 (pin 11) will be positive (ground) unless both diode inputs are negative simultaneously. The input to diode 3CR4 comes from matrix row 5 and will be negative when this row is being scanned. The input to diode 3CR1 comes from matrix column B decoding gate. This input will go negative when matrix column B is being scanned. At this time the diode AND circuit will go negative turning gate 3DGQ1 on. The positive transition on the output (pin 12) of gate 3DGQ1 will reset both the row and column distributors so that the matrix scanning sequence jumps back to Row 1, Column A which is the first bit of the pattern.

Note two important details in this resetting process. First, when a 33 bit pattern is desired, the column producing the 34th bit is connected to the reset AND gate. This causes resetting to occur at the end of the 33rd bit. Second there must be no diode pin in the matrix board in the 34th bit position in order that the matrix input to gate 3GGQ2 will be at ground and allow the transistor shut off when scanned by the column distributor counter.

In order to prevent resetting when reversals (1:1 and 2:2) are being transmitted by the DT-120, switch section S1A grounds row 5 of the matrix in these two positions. This prevents the diode AND circuit from going into coincidence and causing a reset.

2-6. Module 4 Row Distributor, Distortion, and Output:

Refer to figure 11A for a block diagram of module 4 and to figures 11B and 11C for wave forms associated with this module. Also refer to figure 18 for a schematic of the output circuits.

The row distributor consists of a three stage counter, with feed-back to reduce the count from the normal binary count of eight to a count of five, and the row decoding gates which produce a "one-hot" code from the binary coded counter outputs.

The counter is made up of binaries 4AF, 4BF, and 4CF. Note that the interconnections between these binaries are normal cascaded binary connections with the addition of a feed back loop from the Q1 output of 4CF (pin 12) to resetting inputs on 4AF and 4BF. Refer to lines 1 through 4 of figure 11B. Line 1 shows the binary number representing the states of each stage of the counter. The distribution cycle starts at binary seven (111) recycles to zero (000) and then proceeds in normal fashion until binary 3 (011) is reached. When the counter advances to binary 4 (100), the Q1 output of 4CF causes binaries 4AF, and 4BF to be reset to ones. This action is accomplished in about 2 microseconds. The end result is a binary 7 (111) in the counter starting a new distributor cycle.

The "one-hot" coded output required to drive the matrix rows is produced by gates 4DGQ1, 4DGQ2, 4EGQ1 and 4EGQ2. Note in line 4 of figure 11B that the output of binary 4CF is in its "one" state for only one interval in the count cycle. Thus it is not necessary to provide a decoding gate for row 1 of the matrix. The outputs of the row 2 through row 5 gates are shown in lines 5 through 8 respectively. Note also that the binary codes for rows 2, 3, and 4 outputs are unique using only counter stages 4AF and 4BF so that only two inputs are provided in decoding gates 4DGQ1, 4DGQ2 and 4EGQ1.

The signal output of the matrix and the reversal signals from binaries 3AF and 3BF undergo timing delays which would affect signal distortion accuracy if used directly. Further, the matrix signal contains holes and spikes due to imperfect commutation in the row and column distributors. In order to prevent these imperfections from reaching the output, a sampling circuit consisting of gate 4GGQ1 and binary 4HF are provided.

All of the output signals as received from the message select switch section S1C are polarized such that a mark is negative (-9v) and a space is positive (gnd). Gate 4GGQ1 provides an inversion of these signals such that a mark is positive (gnd) and a space is negative (-9v). These two signals (normal and inverted) are used to condition the steering circuits of binary 4HF. A sampling pulse from binary 2LF is applied to the trigger capacitors (pins 10 and 19) of 4HF. Each time the sample pulse input goes positive it causes binary 4HF to assume the same state (mark or space) as is being transmitted from message selector switch S1 at that instant. Note in lines 1 and 2 of figure 11C that the sample pulse positive transitions occur in the center of the bit time from the matrix. Thus holes and spikes in the signal do not affect binary 4HF, since these occur only between bits.

Line 3 of figure 11C shows the regenerated signal at the output of 4HF. The matrix signal has been reproduced but the timing errors are removed along with any holes and spikes.

When the Percent Distortion switch S3 is in the zero position and the pattern or reversals are chosen by the Message Select switch S1, the output of binary 4HF is sent to the output driver 4K120S1 through gate 4GGQ2. When S3 is in any other position or when steady mark or steady mark is selected by S1, the output driver 4K120S1 receives its signal from output binary 4JF. This action is controlled by switch sections S3E and S1D. In the zero position, -9 volts is sent to two diodes located on the module harness board 4CR1 and 4CR2. Diode 4CR1 clamps the output of binary 4JF to -9 volts to prevent it from operating. Diode 4CR2 is reversed biased so that the signal from 4HF (pin 17) is allowed to operate gate 4GGQ2.

When the percent bias switch S3 is in any other position (5,10,15,20,25,30,35,40, or 45) a ground signal is sent to diodes 4CR1 and 4CR2. Diode 4CR1 is reversed biased so that binary 4JF is free to operate while diode 4CR2 shorts to ground any signal appearing on pins 18 and 20 of gate 4GGQ2. Resistor 4R1 provides isolation so that the output of 4HF is not grounded.

Marking bias is accomplished as shown in line 7 of figure 11C by delaying the M/S transitions. This is accomplished using binaries 4IF and 4JF. Binary 4IF produces the delayed transition while binary 4JF constructs the distorted signal from delayed M/S transitions and undelayed S/M transitions.

Binary 4IF has two set inputs on transistor Q1. The trigger inputs come from the two outputs (pins 12 and 17) of binary 4HF. Thus either the M/S or S/M transitions may trigger binary 4IF depending upon the steering circuit inputs. Toggle switch S4 provides either -15 volts or ground to these steering circuits (pins 6 and 11). Assuming that marking bias is being generated, submodule pin 11 is negative while pin 6 is at ground. This allows only the M/S transitions to trigger 4IF.

Binary 4IF is triggered back to its initial state by a delay pulse generated in Module 1. Refer to figure 8A. A diode AND circuit is formed by Resistor R15 and diodes CR7, CR8, CR9, and CR10. The inputs to the diodes come from the decade divider in Module 2 through the Percent Distortion switch S3. Switch S3 selects the normal (pin 17) or inverted (pin 12) outputs from each decade stage to be applied to the diode inputs. Since the decade operates at 20 times bit rate, it makes two complete cycles per bit. Thus the diode AND circuit will achieve coincidence twice per bit. Coincidence will occur for 1/20 of a bit time. Wiring of switch S3 on sections A,B,C, and D is such that the diode AND circuit will go into coincidence at times corresponding to 5% distortion, 10% etc. The pulse produced by the diode AND gate is called the delay pulse and is shown in line 4 of figure 11C.

Binary 4IF is triggered by either the M/S transitions for marking bias as shown in line 5 of figure 11C, or by the S/M transitions for spacing bias as shown in line 6. In each case 4IF is returned to its initial state by the next delay pulse to occur. Since these delay pulses occur at 5% distortion times according to the setting of the Percent Distortion switch S3, the return of binary 4IF represents the M/S transition (or S/M transition when generating spacing bias) distorted by the desired amount.

Binary 4JF constructs a distorted signal from the delayed and undelayed transitions sent to it.

The delayed transitions from submodule pin 12 of binary 4IF are sent to input circuits on both transistors Q1 and Q2 of binary 4JF (pins 10 and 19). The Q2 output (pin 17) of binary 4HF is sent to an input on the Q1 side of binary 4JF (pin 8) while the Q1 output of binary 4HF is sent to an input on the Q2 side of 4JF. Thus the output binary 4JF may be set to mark by an undelayed S/M transition (marking bias) or a delayed S/M transition (spacing bias). The binary can be reset to space by a delayed M/S transition (marking bias) or an undelayed M/S transition (spacing bias). The Bias toggle switch S4 controls the combinations to be used by controlling the dc voltage on the four steering circuit resistors inputs (pins 6 and 18 and pins 11 and 23). When sending marking bias, pins 6 and 18 are at ground allowing undelayed S/M transitions to set 4JF to space through pin 19. When sending spacing bias pins 11 and 23 are at ground allowing undelayed M/S transitions to set 4JF to space through pin 21 and delayed S/M transitions to set 4JF to mark through pin 10.

Output signals from binary 4JF and gate 4GGQ2 (whichever has been selected by S10 and S3E) are sent to the input pins (2 and 3) of output submodule 4K120S1.

Refer to figure 18 for a schematic and component layout of submodule type 120-S1. Both the signal output driver and the timing output driver use this submodule type. Transistors Q1 and Q2 act as amplifiers. They also provide a d-c level shift producing a polar signal from the neutral input signal. Transistors Q3 and Q4 provide the 12 volt 10 ma, 600 ohm polar output. Only one of the two transistors conducts at a time. Q3 conducts when the output is on mark with Q4 conducting when the output is on space. Use is made of the complimentary symmetry properties of NPN and PNP transistors to provide the required push-pull action with only a single ended driving signal. When Q2 is conducting, its collector is at +12 volts and causes Q3 (PNP) to be cut off and Q4 (NPN) to saturate. Inversely when Q2 is cut off, its collector is at a negative voltage causing Q3 to saturate and Q4 to cut off. The output passes through the front panel meter indicator and appears on the front panel at binding post 7TB1 and jack 7J1.

A identical submodule in position 4L is used to provide a 12 volt, 600 ohm, polar timing signal at the front panel binding post 7TB2 and jack J2. This signal has no meter indicator. It has the property of making one complete cycle per bit time of output signal. It goes negative in the center of each bit time of the OUTPUT signal.

2-7. Module 5 Power Supply:

Refer to figure 12A for a schematic of module 5 and figure 12B for printed circuit layouts.

AC voltage to the power supply is controlled by switch 7S5 on the front panel. Also on the front panel are the line fuses 7F1 and 7F2, power indicator lamp 7I1 and power transformer 7T1.

The power transformer is provided with two primary windings. These are connected in parallel as shown in figure 12A for 115V AC operation. For special applications the primary may be rewired as shown in detail "A" for 230 V AC operation. Two secondary windings are provided which supply

approximately 20 volts RMS to the rectifiers.

Located in module 5 on etched circuit card PC-111 are two bridge rectifiers which convert the AC power into approximately 23 volts DC to operate the voltage regulators.

Located on etched circuit board PC-110 in module 5 are the voltage regulators which supply constant voltages of -15 volts, -9 volts, and +15 volts.

The regulators are of the series type using zener diodes as voltage references. The -9 volts supply is derived from the -15v. Since the plus and minus voltage regulators are essentially the same a detailed explanation on one will be given.

The plus 15 volt regulator receives the unregulated voltage from the bridge rectifier consisting of CR5, CR6, CR7, and CR8. This voltage is filtered by the 500 microfarad capacitor C6. A fast blow 1/8 ampere fuse F3 protects the regulator in the event of an overload or component failure in the regulator. Transistor Q6 is a power type 2N301 mounted on a heat dissipating metal bracket. This transistor is the series voltage dropping element in the regulator. Control signals are fed to its base by the amplifier transistor Q3. These control signals adjust the voltage drop from the emitter to collector to maintain a fixed 15 volts to ground at the emitter even though the load current or the line AC voltage may vary.

The feed back control signals are generated by comparing the regulator output voltage with the drop across a zener diode. Resistor R11 and zener diode CR10 form a voltage divider across the unregulated voltage. The circuit uses that property of a zener diode wherein it maintains a fixed voltage regardless of the current through it. This voltage is used to set the emitter potential of regulator amplifier Q3. The base of Q3 is set by potentiometer R13 and resistor R14 to cause Q3 to be forward biased on its emitter base junction. This will cause current to flow in its collector junction causing voltage drop in R10, the collector resistor. The voltage at the collector of Q3 is directly coupled to the base of the series regulator Q6.

To illustrate the feed back principle which operates the regulator, assume that the regulator output were to increase, that is go more positive than +15 volts. This would increase the voltage across the output divider R13 and R14 and hence increase the forward bias on Q3 since its emitter voltage is stabilized by zener CR10. The increased base current in Q3 will increase its collector current causing more voltage drop across R10. This will make the base of Q6 closer to its emitter potential and reduce the current flow in this series regulator causing a larger voltage drop from collector to emitter. The gain in this feed back loop is sufficient to provide large changes in the voltage drop across Q6 for very small changes in the output voltage.

Resistor R12 improves the regulation and ripple factor by feeding some of the unregulated voltage to the base of amplifier transistor Q3. Capacitor C3 stabilizes the high frequency response of the system to prevent oscillations.

The construction of the negative 15 volt regulator is identical except that an additional power amplifying stage is provided between the control signal amplifier Q1 and the base of the series passing transistor Q4.

The negative 9 volt supply is obtained from the negative 15 volt supply. Because the 15 volt supply is already regulated, it is not necessary to provide further regulation. Resistor R8 and potentiometer R7 form a voltage divider to obtain -9 volts from the -15 volts. This voltage is used to control the base of Q5 a power transistor type 2N301 in an emitter follower circuit to provide sufficient current gain to drive the load. A 10 MFD capacitor 2C2 is used to reduce the ac impedance of the 9 volt supply.

The positive 12 volts output is obtained from the positive 15 volt supply through the voltage dropping resistor R16. A 12 volt zener diode CR12 regulates this voltage against load variations. Capacitor 7C1 serves to reduce the AC output impedance and therefore smooth out small spikes caused by load variations.

The negative 12 volt supply is similarly obtained from the negative 15 volt supply through R15. Zener diode CR11 regulates this voltage.

2-8. Module 6 Pattern Programming Matrix:

Refer to figure 13 for a schematic diagram of module 6. Also refer to figure 2 in part 1 of this manual.

Module six is a special matrix board in which each matrix cross points may be cross connected by inserting a special plug into the appropriate hole. The plug contains a diode connected as shown in figure 13. Insertion of a diode into one of the 40 positions of the pattern field will produce a "mark" output in the generated pattern.

MAINTENANCE AND ALIGNMENT

3-1. General:

a. Component Replacement

The use of printed circuit boards in this unit requires caution in the replacement of defective components. Printed circuit boards are easily damaged by excessive heat during soldering. Use a small iron (25 watts to 35 watts) and apply the hot iron tip to the lead of the component to be removed. DO NOT APPLY IRON TO FOIL. As soon as the solder melts remove the iron and brush excessive solder away. Straighten leads and, if necessary, reheat and pull the lead out. Do not force or twist the leads to remove them as this may result in damage to the foil.

Never attempt to save the component at the expense of damaging the printed circuit board. Cutting out of the component and subsequent removal of the remaining portion of the leads is the preferred method of component removal.

Before inserting the new component clear all holes of solder. This may be accomplished by briefly heating the area of the hole and, when the solder is soft, tap the board. Mount the component on the p - c board, gently pushing the leads through the holes. Bend the leads close to the foil and clip them to about 1/8" in length. Apply flux to the joints and solder. Remove the iron as soon as the solder flows into the joint. Clean the joint of excess flux with alcohol and the repair is complete.

b. Repair of Printed Circuit Conductor

If the foil conductor is damaged it must be replaced with a physical wire conductor. Remove the defective portion of the conductor. Drill two holes one at each end of the break alongside the foil. Insert either buss wire or insulated wire from the side of the board opposite that of the broken conductor, and bend the ends of the wire across the foil. Apply flux and solder. Check with an ohmmeter for continuity.

3-2. Test Equipment Required:

The following test equipment is required for maintenance, and trouble shooting of the Message Generator:

Oscilloscope - Tektronix Model 535A or Equivalent

Frequency Counter - Hewlett Packard Model 523B or Equivalent

Multimeter - Simpson Model 260 or Equivalent

3-3, Alignment:

a. General

Alignment of the DT-120 is made at the factory and should not require realignment unless components are replaced or when called for in paragraphs 3-4 and 3-5.

There are only two areas of alignment in the unit. They are:

1. Power Supply Voltages
2. Crystal Oscillator Frequency

b. Power Supply Adjustments

All power supply parts except the transformer and dc filter capacitor 7C1 and 7C2 are located in Module 5. Adjustments and fuses are provided there for the +15 volts, -15 volts, and -9 volt supplies while the +12 volt and -12 volt use zener diode regulators without fuses or adjustments.

Use a 20,000 ohm/volt meter (or better) in conjunction with the test points located on the front panel or those at the rear of Module 5. Adjust the variable resistor on the rear of Module 5, located opposite the test point of the voltage being measured.

c. Oscillator

Module 1 contains the crystal oscillator timing source along with one stage of binary divider. The DT-120 is supplied with one crystal in position Y1 with a frequency of 192,000 KC. Piston capacitor 1C1B is used to adjust the frequency of the crystal oscillator to its exact value.

Connect a frequency counter such as the Hewlett Packard Model 523B to test point TP1 on Module 1. Connect the ground lead of the counter to one of the ground points located either on the front panel or at the rear of Module 5. Set the counter to read frequency at a sampling time of 1 second. Adjust capacitor 1C1B for a reading of 96,000 cps. A finer adjustment can then be made by setting the counter to a 10 second sampling time and adjusting to 96,000.0 cps.

NOTE: Adjustment of the piston capacitor 1C1B is best made with a non conducting (fiber) screwdriver. If one is not available, an ordinary screwdriver may be used but will result in added capacity or may even stop the oscillator while it is engaged. No damage will result. The adjustment is made then, by turning the screw and removing the screwdriver before taking a frequency reading. The procedure is repeated until the proper reading is achieved.

3-4. Adding New Speeds:

Provision has been made in the oscillator (Module 1) of the DT-120 for the addition of up to four (4) crystals and associated load capacitors to provide operation at four additional speeds. Crystal frequencies may be selected in the range of 90Kc to 240Kc. The oscillator circuit is designed to use crystals with parallel resonance based on the CR-37/U military type. (Digitech specifies as original equipment a crystal with somewhat better temperature and resistance characteristics than the CR-37/U).

The component reference designations for the frequency determining parts have been marked on the printed circuit board. For example, the crystal supplied with the DT-120 is designated Y1, its load capacitor is designated C1A, and its trimmer capacitor C1B. The following chart provides the relationship between sets of components for a single oscillator frequency and the switch connection which ties the selected crystal to the circuit.

TABLE I

<u>Crystal</u>	<u>Load Capacitor</u>	<u>Trimmer Capacitor</u>	<u>Switch Connection*</u>
Y1	C1A	C1B	7S2B1 through B7
Y2	C2A	C2B	7S2B8
Y3	C3A	C3B	7S2B9
Y4	C4A	C4B	7S2B10
Y5	C5A	C5B	7S2B11

* Switch sections are lettered alphabetically with A being closest to the front panel.

There are three steps required in adding a new speed. They are:

1. Select a crystal frequency
2. Select a load capacitor
3. Make the appropriate jumper connection between sections A and B of speed switch 7S2.

The following tables will be helpful for steps 1 and 3.

TABLE II

BAUD MULTIPLIER AND JUMBER CONNECTIONS

<u>Multiplier</u>	<u>Jumper Connections on 7S2</u>
40	From B8 (9, 10, or 11) to A1
80	From B8 (9, 10, or 11) to A2
160	From B8 (9, 10, or 11) to A3
320	From B8 (9, 10, or 11) to A4
640	From B8 (9, 10, or 11) to A5
1280	From B8 (9, 10, or 11) to A6
2560	From B8 (9, 10, or 11) to A7

TABLE III

SUGGESTED LOAD CAPACITY

<u>Frequency Range</u>	<u>Load Capacity C2A to C5A</u>
90 Kc - 130 Kc	680 mmf
130 Kc - 180 Kc	560 mmf
180 Kc - 210 Kc	470 mmf
210 Kc - 240 Kc	360 mmf

Step 1 - To select a crystal frequency multiply the desired operating speed in bauds or bits per second by the multipliers in Table II until a frequency in the 90Kc to 240Kc range is reached.

Step 2 - Select a load capacity from Table III for the crystal frequency selected and insert it into the designated location on Module 1.

Step 3 - Wire a jumper on speed switch 7S2 located in the upper right corner (facing the unit). The jumper must be wired from section B (B8 for a crystal in position Y2, B9 for Y3, etc.) to the pin on section A designated in Table II opposite the multiplier used to determine the crystal frequency.

An example is given below. The required speed is 750 bauds, and the crystal is to be placed in position Y2.

EXAMPLE

<u>Multiplier</u>	<u>Bauds Desired</u>	<u>Crystal Frequency</u>	<u>C2A</u>	<u>7S2 Jumper</u>
40	750	30Kc		
80	750	60Kc		
60	750	120Kc	680mmf	B8 to A3

The results show a crystal frequency of 120Kc. Table III indicates a recommender C2A of 680 mmf and the jumper is tied from 7S2B8 to 7S2A3, (Table II) The trimmer capacitor is C2B (Table I).

3-5. Trouble Shooting Procedures:

a. General

The first step in servicing a defective generator is to sectionalize the fault to a particular module or other section of the unit. Test points are provided in the rear of the unit on the modules for use in localizing troubles. The signal flow is generally from left of the unit to right when facing the unit from the rear.

When the fault is isolated to a particular module the next step is to turn off the power and remove the defective module. This is done by removing the #6 holding screw on the top of the unit for that module and pulling the module out. Next insert the adapter card into the vacant space before turning the unit on.

Precaution: Always turn power off when inserting or removing modules. After inserting adapter card be sure to check that the connector is properly mated before applying power.

With the defective module extended the third step is to locate the defective component. Since the circuits are constructed in the form of sub-modules containing, with few exceptions, either a complete binary or two transistor gates a trouble shooting procedure for these logic elements will be discussed here. This discussion should be referred to when consulting the trouble shooting chart. See Figures 16 and 17.

b. Trouble Shooting a Binary (flip-flop) Figure 16

There are two types of check which can be made to isolate a defective component in the flip-flop circuit. The first type of check is to determine whether the circuit is dc stable. Ground the base lead of Q1 to turn it off. The collector of Q1 should go negative to -9 volts and the collector of Q2 should go to ground. If Q1 does not turn off, (1) it may have an internal collector to emitter short, or (2) the collector is grounded somewhere in the external circuit. If Q2 does not turn on, going to ground, it may have a base to emitter open or a base to collector open in the transistor. Open circuits between collector of Q1 to base of Q2 are another possible cause. Next, reverse this procedure grounding the base of Q2. The dc check, therefore, will locate faulty transistors, resistors or connections within the flip-flop circuit.

If the flip-flop circuit is dc stable grounding the bases of Q1 and Q2 alternately will cause the circuit to flip back and forth between its two stable states. The second type of check involves the ac trigger circuits each consisting of a capacitor, resistor, diode combination. There is at least one trigger circuit connected to each transistor base in a flip-flop. With a signal on each input check the collectors of Q1 and Q2 to determine which one is at ground and doesn't turn off. The trigger circuit associated with that transistor is suspect. The most probable cause of trouble is a defective diode. This may be checked with the Volt-Ohm meter in the circuit. Forward resistance of a good diode will be under 30 ohms on the RX1 scale, while the reverse resistance will normally be in the range 200 K to 400 K on the RX 10,000 scale. Input trigger diodes are located on sub-modules in position 7, 9, 20, and 22.

c. Gates - PNP (Figure 17)

Transistor gates are rather simple to trouble shoot in that they contain only two component types, transistors and resistors. If a gate is found to be not operating, check the base wave form on the Oscilloscope. For the transistor to saturate the base must be negative about - 0.2 volts with respect to the emitter and to be cut-off the gate must be positive (up to about 3 volts). If either one of these conditions exists steadily then the gate collector will stay at the appropriate voltage (gnd. or -9 volts) without changing and the inputs to the gate should be checked. A base voltage significantly more negative than -0.2 volts with respect to its emitter indicates an open circuit.

To determine whether a transistor which is saturated is defective, short the base to the emitter; this should cut the transistor off, producing a negative voltage at the collector.

If the defect keeps the gate always cut-off, check the forward resistance on the transistor base to emitter and base to collector junctions for an open circuit condition.

d. Gates - NPN (Figure 18)

Transistors Q1 and Q4 of submodule 120-S1 are NPN types. They are characterized by positive collector to emitter voltages. In the conducting state the base is + .2 volts positive with respect to the emitter, while in the off state the base goes negative relative to its emitter. The trouble shooting procedure is the same as for PNP gates except that polarities are reversed and the voltage levels are those of figure 18.

3-6. Trouble Shooting

A logical step by step process of trouble shooting will be outlined in the following paragraphs.

The process will involve the utilization of test points to determine which module or assembly is at fault. If a spare assembly is available it may be then plugged in to restore the unit to service, or if time permits, the indicated checks within the module can be made to locate and replace the defective component.

The trouble shooting discussion will assume no hint of the location of the fault, and will begin with a check of power voltages, oscillator, and timing chain before going into pattern generation and distortion circuits. As more familiarity is gained by the service personnel with the unit, Steps in the process may be omitted to shorten the trouble shooting time. Each Step will reference the appropriate paragraphs and figures dealing with that section of the unit.

Refer to paragraphs 3-1, 3-2, 3-4 for specific information on component replacement, test equipment required, and how to trouble shoot the logical circuits found on individual submodules. Submodule identification and location of components may be found in the Parts List Chapter 4 and the figures associated with each Module.

Before starting to trouble shoot the following checks should be made:

1. Be sure a-c power of 115 volts 60 cps is applied to the unit in the switch is ON.
2. Be sure that all modules are fully inserted and properly seated.

STEP 1: Check all dc voltages with a 20K ohm/volt meter using the test points on the front panel.

The -9v and -12v supplies are derived from the -15v regulated output, while the +12 v supply is derived from the +15 v regulated output. A complete failure of either the -15v or the +15v regulators then will affect other supply voltages as well.

MODULE 5 TROUBLE CHART

<u>Symptom</u>	<u>Probable Cause</u>	<u>Remedy</u>
No - 15 volts	Fuse F1 open ($\frac{1}{2}$ Amp)	Replace F1
No - 9 volts	Fuse F2 blown (1/8 Amp)	Replace F2
No + 15 volts	Fuse F3 blown (1/8 Amp)	Replace F3
-15v reads low about 7 volts and does not change when R5 is adjusted	Q1 has collector to emitter short.	Replace Q1
+15v reads low (7 volts)	Q3 has collector to emitter short.	Replace Q3
-15v and -9v reads high and will not adjust.	Q1, Q2, or Q4 open	Replace
+15v reads high and will not adjust	Q3 or Q6 open	Replace
-9 volts only will not adjust	F2 or Q5 open	Replace
-12 volts reads high and is not regulating	Zener CR11 open	Check zener diode with ohmmeter - Replace if necessary
-12 volts reads 0 volts	1. Zener CR11 shorted 2. External circuit is shorted.	Remove Module from unit and check with ohmmeter - Replace if necessary

The same treatment is advised for the +12 v zener regulator CR12 as outlined above for the -12 v.

References - Paragraph 2-7 and figures 12A, 12B.

When it has been determined that all Power supply voltages are correct go on to:

STEP 2: Check 1TP1 on Module 1 for 96KC timing signal on all active positions of speed switch 7S2. If it is there, go on to STEP 3. If it is not there, use the chart below.

MODULE 1 TROUBLE CHART

A. Oscillator

<u>Symptom</u>	<u>Probable Cause</u>	<u>Remedy</u>
No signal at Collector Q1 or Emitter of Q2	1. Q1 or Q2 defective 2. Crystal not properly seated or is defective 3. Switch 7S2B defective.	1. Replace 2. Remove crystal and reseal or replace. 3. Check for broken wires.
Signal at Q2 6 volts or more peak to peak, but no signal at 1TP1 (Q4)	1. Defective binary made up of Q3 and Q4.	Refer to section 3-4b for trouble shooting procedure
Low signal at Q2 (5 volts or less) - No signal at 1TP1 - Binary checks good.	R1 high C1A high C6 high	Reduce these component one at a time to raise signal level at Q2.

B. Delay Gate

<u>Symptom</u>	<u>Probable Cause</u>	<u>Remedy</u>
Distortion percent does not increase smoothly in 5% steps.	1. Defective Diode 2. Bad switch connections on PerCent Distortion Switch 7S3	1. Check forward resistance of CR7 through CR10 and replace defective unit. 2. Check wires.

References: Paragraph 2-3 , 2-6, Figures 8A, 8B.

When the 96KC timing signal has been established go on with:

STEP 3.

- A. Check 2TP1 for signals on each position of 7S2 (Speed). For the 75 baud speed the binaries in positions A,B,C,D,E, and F are all in action. A 1500 cps signal at 2TP1 on 75 baud, therefore, indicates that all these binaries are functioning. If no signal appears on 75 baud, but a 3KC signal appears on 150 baud then binary 2FF is faulty. Similarly if the first indication of signal appears on 300 baud 2EF is faulty, and so on to 4800 baud indicating that 2AF is faulty.

Confirmation of the cause is made by removing the module, extending it on the adapter card, and using an oscilloscope to view the signal at each submodule.

If a signal appears at 1TP1 but does not appear at 2TP1 at 4800 baud speed, then gate 2GGQ1 is suspect.

- B. Check 2TP2 for proper waveform at 4800 baud (See figure 15). If this signal does not appear, extend the module on the adapter and check for wave forms in figure 9C. If no signal appears on one of the binaries then it is defective. If signals appear on all of the binaries involved, but do not match the wave forms of figure 9C then the reset gate 2GGQ2 and diodes CR22 on 2IF and 2JF are suspect.

- C. As a final check, look for a signal at bit rate at the collector of 2LFQ2 (also on front panel 7TB2).

References: Paragraph 2-2, 2-4 Figures 9A, 9B, 9C. When all signals are correct go to the next step.

- STEP 4. Module 3 generates bit length signals and distributes them to the matrix decoding gates. Check at 3TP1 for the proper signal (See figure 15). If it does not appear or is incorrect, this indicates trouble with binaries 3AF, 3BF or 3CF or gate 3DGQ2. The module should be extended to locate the problem. (See paragraphs 2-2, 2-5, figures 7, 10A, 10B)

With the proper signal at 3TP1 go on to:

- STEP 5. To finish a check of the Timing, observe the signal at 7TP7 (Sync) on the front panel at 4800 baud (See figure 15). A correct signal here indicates that binaries 4AF, 4BF, 4CF are functioning. No signal indicates a failure in one of the binaries, while an incorrect signal indicates a problem in the feed back loop of these binaries (See paragraphs 2-2, 2-6 figures 7, 11A, 11B).

STEP 6. Next check the matrix row driving signals at 4DGQ1, 4DGQ2, 4EGQ1 and 4EGQ2. Use 7TP7 to synchronize the scope and either extend the module or remove the top cover and observe these signals on module 6. Assuming the correct signal at 7TP7, failure to see a similar waveform at these points, displaced in time, would indicate trouble with the particular gate involved. (See paragraphs 2-2, 2-6, figures 7, 11A, 11B)

STEP 7. Check for proper pattern at 3TP2. The signal at this point will depend on the pattern which is programmed into the matrix. Using the front panel sync test point 7TP7, and triggering the scope on the negative portion of this signal a view of the pattern will be seen starting with Row 1 Column A. To determine whether gates 3GG, 3HG, 3IG, 3JG and 3KG are all functioning remove module 6 the pattern matrix and observe a ground signal at 3TP2. If the signal goes negative at some point it indicates that one of these gates is shorted. An open gate, on the other hand, would always produce a space signal in the pattern whenever it was scanned by the bit distributor regardless of the programmed pattern. (See paragraph 2-2, 2-5, figures 10A, 10B)

Beside the gates mentioned above, a pattern error can also be caused by a bad diode or poor connection in Matrix Module 6. In general a single isolated bit error would probably originate in Module 6, while a group of errors spaced eight bits apart would originate in Module 3, and a group of errors eight bits in a row would originate in the row drivers of Module 4.

STEP 8. All that remains to be checked now is the distortion and output circuits in Module 4. (See Figure 11A, 11C, 18)

All selected message types pass through gate 4GGQ1 and are re-generated in binary 4HF. When the Percent Distortion switch is on 0%, the signal passes through 4GGQ2 to the output circuits located on submodule K.

Check the signal at test point 4TP1 to verify that all five types may be selected. Turn the Message Select switch 7S1 to 1:1 for the remainder of the check and look for the signal at 7TB1, the output signal terminal, on the front panel.

If the signal appears on all distortion positions except 0% then 4GGQ2 is at fault. If, on the other hand, the signal appears only on 0% distortion, then some components in binaries 4IF or 4JF are at fault.

If the amount of distortion introduced is incorrect for some positions of the PERCENT DISTORTION switch it indicates a defective diode (1CR7 through 1CR10) in the delay gate located on Module 1, or a broken wire on 7S1.

Check operation on both Marking and Spacing Bias for distortions other than 0%. If the signal does not appear for either type of distortion the problem probably lies with the transistors of these binaries. Operation on Marking Bias only indicates possible open diodes CR7 on 4IF, CR9 and CR22 on 4JK. Operation on Spacing Bias only on 4JF. An ohmmeter check will reveal the defective diode.

STEP 9. Finally, if no signal appears on the output of 7TB1 and a signal can be found at 4GGQ2 (0%) or 4IF (5% up) the trouble lies in the output circuits on 4K-120-S1 (See figure 18). The circuit is made up of an NPN OR gate Q1 followed by a PNP inverter gate Q2 driving a pair of complimentary amplifiers Q3 and Q4. The voltage levels are shown for the collectors of Q1, and Q2 and the emitters of Q3 and Q4 with the output loaded with 600 ohms or unloaded. Starting with Q1, improper voltage levels indicate a defective transistor.

STEP 10. The timing output at 7TP2 is achieved by applying the bit rate timing signal from 2LF to the input of 4L120S1. Trouble shooting this submodule is the same as that outlined above in STEP 9.

SHORT PATTERNS:

Operation on less than a 40 bit pattern involves the use of diodes 3CR1 through 3CR4, gate 3DGQ1 and the reset diodes (CR22) of 3AF, 3BF, 3LF and 4CF. If the unit does not operate properly on 33, 35, or 36 bits use an ohmmeter to check these diodes.

CONCLUSION:

The foregoing STEP process of trouble shooting is based on making sure that all signals covered by one STEP are good before going on to the next step. The whole process can be done in a matter of minutes on a good unit, and therefore, on a defective unit should lead the maintenance man to the localized trouble spot in a short time.

In this section it has been assumed that all trouble will be caused by failure of diodes and transistors rather than resistors and capacitors. This assumption is expected to be valid in the vast majority of cases, but if the trouble cannot be detected to a defective semiconductor, these other component types, associated with the defective circuit, should be investigated.

Chapter 4

PARTS LIST

4-1. General

The DT-120 is constructed of eight main assemblies. These are:

	<u>Part Number</u>
Assembly 1 - Module 1-Oscillator	120-MOD 1
Assembly 2 - Module 2-Count Down	120-MOD 2
Assembly 3 - Module 3-Bit Distributor and Matrix Gates	120-MOD 3
Assembly 4 - Module 4-Distortion & Output	120-MOD 4
Assembly 5 - Module 5-Power Supply	120-MOD 5
Assembly 6 - Module 6-Pattern Programming Matrix	120-MOD 6
Assembly 7 - Main Chassis	120-ASY.7
Assembly 8 - Case	120-ASY.8

Assemblies 2,3, and 4 are made using a submodular construction in which only three standard submodule designs are used. For these modules the parts list catalogs only the submodule type. A schematic diagram, component layout and component descriptions for each submodule design is given in figures 16,17 and 18. Paragraph 4-1 describes the submodule designations and component part numbers.

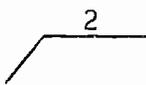
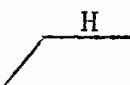
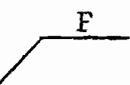
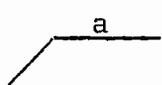
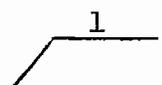
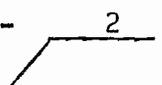
Modules 1 and 5 do not use submodular construction. For these modules the parts list describes all replaceable components.

In some instances, resistors listed as $\frac{1}{4}$ watt will be found to be $\frac{1}{2}$ watt types. This substitution will in no way affect the performance of the DT-120.

4-2. Submodule Designations:

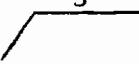
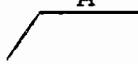
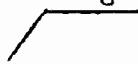
The submodule reference designators are designed to provide both locating and circuit identification information.

Example #1, 2HFa1-2

					
Module Number	Sub- Module Location	Type of Logic	Design Type	Number of Inputs to Q1	Number of Inputs to Q2

Thus 2HFa2 refers to a submodule located in position H of module 2. This submodule is a binary (flip-flop) of the "a" circuit design and has a "set one" input as well as the standard count inputs. Figure 16 provides all information on this submodule type; schematic diagram component layout and Bill of Material. Figure 19 shows submodule location and pin numbers on the harness board.

Example #2, 3AGal-4

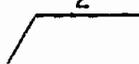
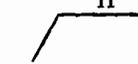
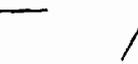
					
3	A	G	a	1	4
Module Number	Sub- Module Location	Type of Logic	Design Type	Number of Inputs to Q1	Number of Inputs to Q2

Thus 3AGal-4 refers to a submodule located in position A of Module3. This submodule is a double gate of the "a" circuit design. One input resistor is provided for the gate whose output is submodule pin 12. Four input resistors are provided for the gate whose output is submodule pin 17. Figure 17 provides all information on this submodule type; schematic diagram, component layout, and bill of material. Refer to Figure 19 for submodule locations and pin numbers.

Part Numbers For Submodule Components

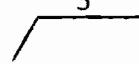
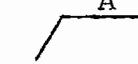
The component part numbers are designed to provide locating as well as circuit parameters.

Example #1, 2HFaR1

					
2	H	F	a	R	1
Module Number	Sub- Module Location	Type of Logic	Design Type	Component Type	Location on Sub- Module

Thus 2HFaR1 refers to a resistor located in position number one of submodule H in module number 2. Refer to Binary (flip-flop) submodule reference drawing figure 16 is shows that the resistor is used as the collector resistor of transistor Q1 and is a $\frac{1}{4}$ watt composition type with a tolerance of $\pm 5\%$. From the chart in figure 16A, the "a" design value of R1 is 3900 ohms.

Example #2, 3AGaQ2

					
3	A	G	a	Q	2
Module Number	Sub- Module Location	Type of Logic	Design Type	Component Type	Location on Sub- Module

Thus 3AGaQ2 refers to a transistor located in mounting clip number two of submodule A in module number 2. Referring to the Double Gate submodule reference drawing figure 17A shows that the transistor is used in the second gate and for the "a" design is a 2N404.

Figures 16B and 17B provide the values for "b" designs, while figure 18 provides the layout and values for the output submodule 120S1.

4-3. List Of Parts:

120-MOD1 - Assembly 1 (MODULE 1)

<u>COMPONENT DESIGNATOR</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
1R1	Resistor, fixed, composition, 43K ohms, $\frac{1}{4}$ W, 5%	120-R1
1R2	Resistor, fixed, composition, 7500 ohms, $\frac{1}{4}$ W, 5%	120-R2
1R3	Resistor, fixed, composition, 4300 ohms, $\frac{1}{4}$ W, 5%	120-R3
1R4	Resistor, fixed, composition, 22 ohms, $\frac{1}{4}$ W, 5%	120-R4
1R5	Resistor, fixed, composition, 1000 ohms, $\frac{1}{4}$ W, 5%	120-R5
1R6	Resistor, fixed, composition, 1000 ohms, $\frac{1}{2}$ W, 5%	120-R5
1R7	Resistor, fixed, composition, 30K ohms, $\frac{1}{4}$ W, 5%	120-R6
1R8	Resistor, fixed, composition, 3900 ohms, $\frac{1}{4}$ W, 5%	120-R7
1R9	Resistor, fixed, composition, 30K ohms, $\frac{1}{4}$ W, 5%	120-R6
1R10	Resistor, fixed, composition, 160K ohms, $\frac{1}{4}$ W, 5%	120-R8
1R11	Resistor, fixed, composition, 30K ohms, $\frac{1}{4}$ W, 5%	120-R6
1R12	Resistor, fixed, composition, 3900 ohms, $\frac{1}{4}$ W, 5%	120-R7
1R13	Resistor, fixed, composition, 160K ohms, $\frac{1}{4}$ W, 5%	120-R8
1R14	Resistor, fixed, composition, 30K ohms, $\frac{1}{4}$ W, 5%	120-R6
1R15	Resistor, fixed, composition, 16K ohms, $\frac{1}{4}$ W, 5%	120-R9
1C1A	Capacitor, Mica, Dipped, 470 mmfd, 500V, 5%	120-C1
1C2A	Not Installed	
1C3A	Not Installed	
1C4A	Not Installed	
1C5A	Not Installed	
1C1B	Capacitor, Piston, .8 to 30 mmfd	120-C2
1C2B	Capacitor, Piston, .8 to 30 mmfd	120-C2
1C3B	Capacitor, Piston, .8 to 30 mmfd	120-C2
1C4B	Capacitor, Piston, .8 to 30 mmfd	120-C2
1C5B	Capacitor, Piston, .8 to 30 mmfd	120-C2
1C6	Capacitor, Mica, Dipped, 2000 mmfd, 500V, 5%	120-C3
1C7	Capacitor, Mica, Dipped, 150 mmfd, 500V, 5%	120-C4
1C8	Capacitor, Mica, Dipped, 150 mmfd, 500V, 5%	120-C4
1C9	Capacitor, Mica, Dipped, 150 mmfd, 500V, 5%	120-C4
1C10	Capacitor, Mica, Dipped, 150 mmfd, 500V, 5%	120-C4
1C11	Capacitor, Ceramic, .47 mfd., 3V., +100% -0%	120-C5
1CR1	Diode, 1N636	120-CR1
1CR2	Diode, 1N636	120-CR1
1CR3	Diode, 1N636	120-CR1
1CR4	Diode, 1N636	120-CR1
1CR5	Diode, 1N636	120-CR1
1CR6	Diode, 1N636	120-CR1
1CR7	Diode, 1N636	120-CR1
1CR8	Diode, 1N636	120-CR1
1CR9	Diode, 1N636	120-CR1
1CR10	Diode, 1N636	120-CR1
1Q1	Transistor, 2N1224	120-Q1
1Q2	Transistor, 2N404	120-Q2
1Q3	Transistor, 2N404	120-Q2
1Q4	Transistor, 2N404	120-Q2
1P1	Plug, 22 Pins	120-P1
1Y1	Crystal 192.000KC	120-Y1

Assembly 2 - 120-MOD2 (MODULE 2)

<u>SUBMODULE POSITION</u>	<u>SUBMODULE TYPE</u>	<u>PART NUMBER</u>	<u>NOTES</u>
A	Fal-1	2AFal-1	
B	Fal-1	2BFal-1	
C	Fal-1	2CFal-1	
D	Fal-1	2DFal-1	
E	Fal-1	2EFal-1	
F	Fal-1	2FFal-1	
G	Ga2-2	2GGa3-2	Capacitor C10=82mmfd added, Diode CR2 added
H	Fb1-1	2HFb1-1	
I	Fb1-2	2IFb1-2	
J	Fb1-2	2JFb1-2	
K	Fb1-1	2KFb1-1	
L	Fal-1	2LFal-1	

THE FOLLOWING COMPONENT ARE LOCATED ON THE HARNESS CARD

<u>COMPONENT DESIGNATOR</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
2P1	Plug, 22 Pin	120-P1

Assembly 3 - 120-MOD3 (MODULE 3)

<u>SUBMODULE POSITION</u>	<u>SUBMODULE TYPE</u>	<u>PART NUMBER</u>	<u>NOTES</u>
A	Fal-2	3AFal-2	
B	Fal-2	3BFal-2	
C	Fal-2	3CFal-2	
D	Ga1-3	3DGa1-3	Diode CR27 added. Capacitor C19, 22 mmfd added.
E	Not Used	-----	-----
F	Not Used	-----	-----
G	Ga4-4	3GGa4-4	
H	Ga4-4	3HGa4-4	
I	Ga4-4	3IGa4-4	
J	Ga4-4	3JGa4-4	
K	Ga4-4	3KGa4-4	No resistor R28
L	Not Used	-----	-----

THE FOLLOWING COMPONENTS ARE LOCATED ON THE HARNESS BOARD

<u>COMPONENT DESIGNATOR</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
3CR1	Diode, 1N636	120-CR1
3CR2	Diode, 1N636	120-CR1
3CR3	Diode, 1N636	120-CR1
3CR4	Diode, 1N636	120-CR1
3R1	Resistor, Fixed, Composition, 16K ohms, $\frac{1}{4}$ W, 5%.	120-R9
3P1	plug, 22 pin	120-P1

Assembly 4 - 120-MOD4 (MODULE 4)

<u>SUBMODULE POSITION</u>	<u>SUBMODULE TYPE</u>	<u>PART NUMBER</u>	<u>NOTES</u>
A	Fal-2	4AFal-2	
B	Fal-2	4BFal-2	
C	Fbl-2	4CFbl-2	
D	Gb2-2	4DGB2-2	
E	Gb2-3	4EGB2-3	
F	Not Used	Not Used	
G	Gal-2	4FGal-2	Diode CR27 Added
H	Fal-1	4GFal-1	
I	Fa2-1	4IFa2-1	
J	Fa2-2	4JFa2-2	
K	120S1	4K120S1	
L	120S1	4L120S1	R2 Not Used

THE FOLLOWING COMPONENTS ARE LOCATED ON THE HARNESS BOARD

<u>COMPONENT DESIGNATOR</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
4R1	Resistor, Fixed, Composition, 16K ohms, $\frac{1}{4}$ W, 5%	120-R9
4CR1	Diode, 1N636	120-CR1
4CR2	Diode, 1N636	120-CR1
4P1	Plug, 22 pin	120-P1

Assembly 5 - 120MOD5 (MODULE 5)

<u>COMPONENT DESIGNATOR</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
5R1	Resistor, fixed, composition, 4700 ohms, $\frac{1}{2}$ W, 5%	120-R10
5R2	Resistor, fixed, composition, 1000 ohms, $\frac{1}{2}$ W, 5%	120-R5
5R3	Resistor, fixed, composition, 120 ohms, $\frac{1}{4}$ W, 5%	120-R11
5R4	Resistor, fixed, composition, 4700 ohms, $\frac{1}{2}$ W, 5%	120-R10
5R5	Resistor, variable, wire wound, 5K ohms, $\frac{1}{2}$ W, 20%	120-R12
5R6	Resistor, fixed, composition, 1000 ohms, $\frac{1}{2}$ W, 5%	120-R5
5R7	Resistor, variable, wire wound, 1000 ohms, $\frac{1}{2}$ W, 20%	120-R13
5R8	Resistor, fixed, composition, 390 ohms, $\frac{1}{2}$ W, 5%	120-R14
5R9	Resistor, fixed, composition, 390 ohms, $\frac{1}{2}$ W, 5%	120-R14
5R10	Resistor, fixed, composition, 1000 ohms, $\frac{1}{2}$ W, 5%	120-R5
5R11	Resistor, fixed, composition, 4700 ohms, $\frac{1}{2}$ W, 5%	120-R10
5R12	Resistor, fixed, composition, 68K ohms, $\frac{1}{2}$ W, 5%	120-R15
5R13	Resistor, variable, wire wound, 5K ohms, $\frac{1}{2}$ W, 20%	120-R12
5R14	Resistor, fixed, composition, 1000 ohms, $\frac{1}{2}$ W, 5%	120-R5
5R15	Resistor, fixed, composition, 100 ohms, 2W, 5%	120-R16
5R16	Resistor, fixed, composition, 100 ohms, 2W, 5%	120-R16
5F1	Fuse, 3AG, $\frac{1}{2}$ Amp, 250 volts	120-F1
5F2	Fuse, 3AG, 1/8Amp, 250 volts	120-F2
5F3	Fuse, 3AG, 1/8Amp, 250 volts	120-F2
5C1	Capacitor, fixed, ceramic, .01 mfd, 50V	120-C6
5C2	Capacitor, fixed, ceramic, .01 mfd, 50V	120-C7
5C3	Capacitor, Mica, Dipped, 390 mmfd, 500V, 5%	120-C8
5C4	Not Used	
5C5	Capacitor, fixed, electrolytic, 500mfd, 50V	120-C9
5C6	Capacitor, fixed, electrolytic, 500mfd, 50V	120-C9

<u>COMPONENT DESIGNATOR</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
5CR1	Diode, 1N2859	120-CR2
5CR2	Diode, 1N2859	120-CR2
5CR3	Diode, 1N2859	120-CR2
5CR4	Diode, 1N2859	120-CR2
5CR5	Diode, 1N2859	120-CR2
5CR6	Diode, 1N2859	120-CR2
5CR7	Diode, 1N2859	120-CR2
5CR8	Diode, 1N2859	120-CR2
5CR9	Diode, 1N754	120-CR3
5CR10	Diode, 1N754	120-CR3
5CR11	Diode, 1N3022B	120-CR4
5CR12	Diode, 1N3022B	120-CR4
5Q1	Transistor, 2N404	120-Q2
5Q2	Transistor, 2N404	120-Q2
5Q3	Transistor, 2N404	120-Q2
5Q4	Transistor, 2N301	120-Q3
5Q5	Transistor, 2N301	120-Q3
5Q6	Transistor, 2N301	120-Q3
5P1	Plug, 22 pin	120-P1

Assembly 6 - 120MOD6 (MODULE 6)

<u>COMPONENT DESIGNATOR</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
6PB	Program Board	120-6PB
6P1	Plug, 15 pins	120-P2
6P2	Diode Holders (including 1N636 Diode)	120-P3

NOTE: A quantity of thirty diode holders are provided in Assembly 6.

Assembly 7 - 120-ASY7 (Main Chassis)

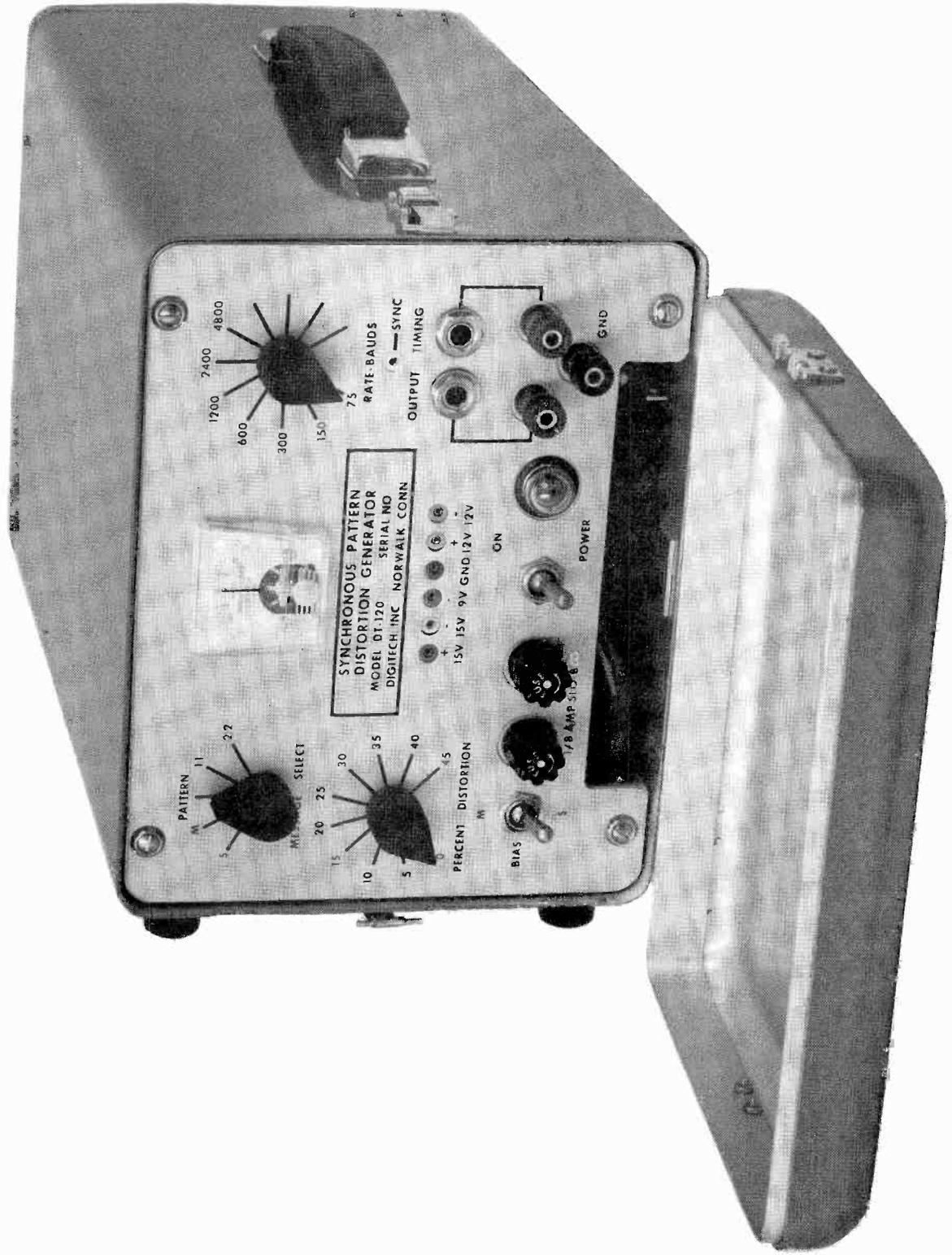
<u>COMPONENT DESIGNATOR</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
7F1	Fuse, 3AG, 1/4Amp, Slo Blo	120-F3
7F2	Fuse, 3AG, 1/4Amp, Slo Blo	120-F3
7M1	Meter, Center Zero, 15-0-15 ma.	120-B1082
7I1	Lamp, Neon - NE51	120-I1
7TB1	Binding Post, 5 way, Red	120-TB1
7TB2	Binding Post, 5 way, Red	120-TB1
7TB3	Binding Post, 5 way, Black	120-TB2
7J1	Jack, Telephone	120-J1
7J2	Jack, Telephone	120-J1
7S1	Switch, Rotary, 3 Pole, 5 pos.	120-S1
7S2	Switch, Rotary, 2 Pole, 11 pos.	120-S2
7S3	Switch, Rotary, 5 Pole, 10 pos.	120-S3
7S4	Switch, Toggle, DPDT	120-S4
7S5	Switch, Toggle, DPST	120-S5

7C1	Capacitor, fixed, electrolytic, 500 mfd, 50V	120-C9
7C2	Capacitor, fixed, electrolytic, 10 mfd, 25V	120-C10
7T1	Transformer, Power, Intermediate	120-B1081
1J1	Socket, 22 pins	120-J2
2J2	Socket, 22 pins	120-J2
3J3	Socket, 22 pins	120-J2
4J4	Socket, 22 pins	120-J2
5J5	Socket, 22 pins	120-J2
6J6	Socket, 15 pins	120-J3

Assembly 8 - 120-ASYS (CASE)

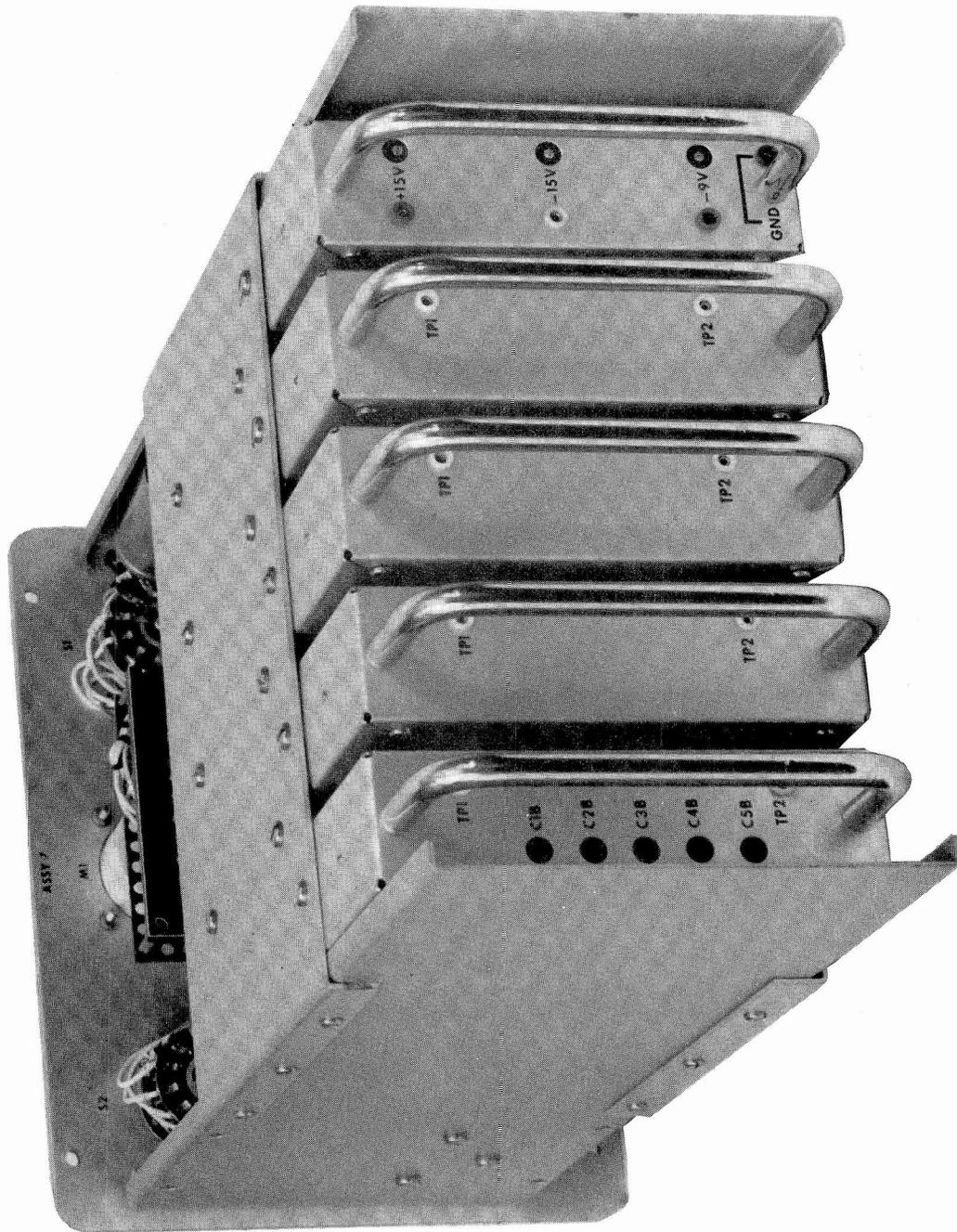
<u>DESCRIPTION</u>	<u>PART NUMBER</u>
Case, with cover and latches	C1104
Feet, Rubber	120-F
Handle	120-H

<u>DESCRIPTION</u>	<u>PART NUMBER</u>
Test Adapter Card for extending Modules 1 to 5	PC-149-3



DT-120 FRONT VIEW

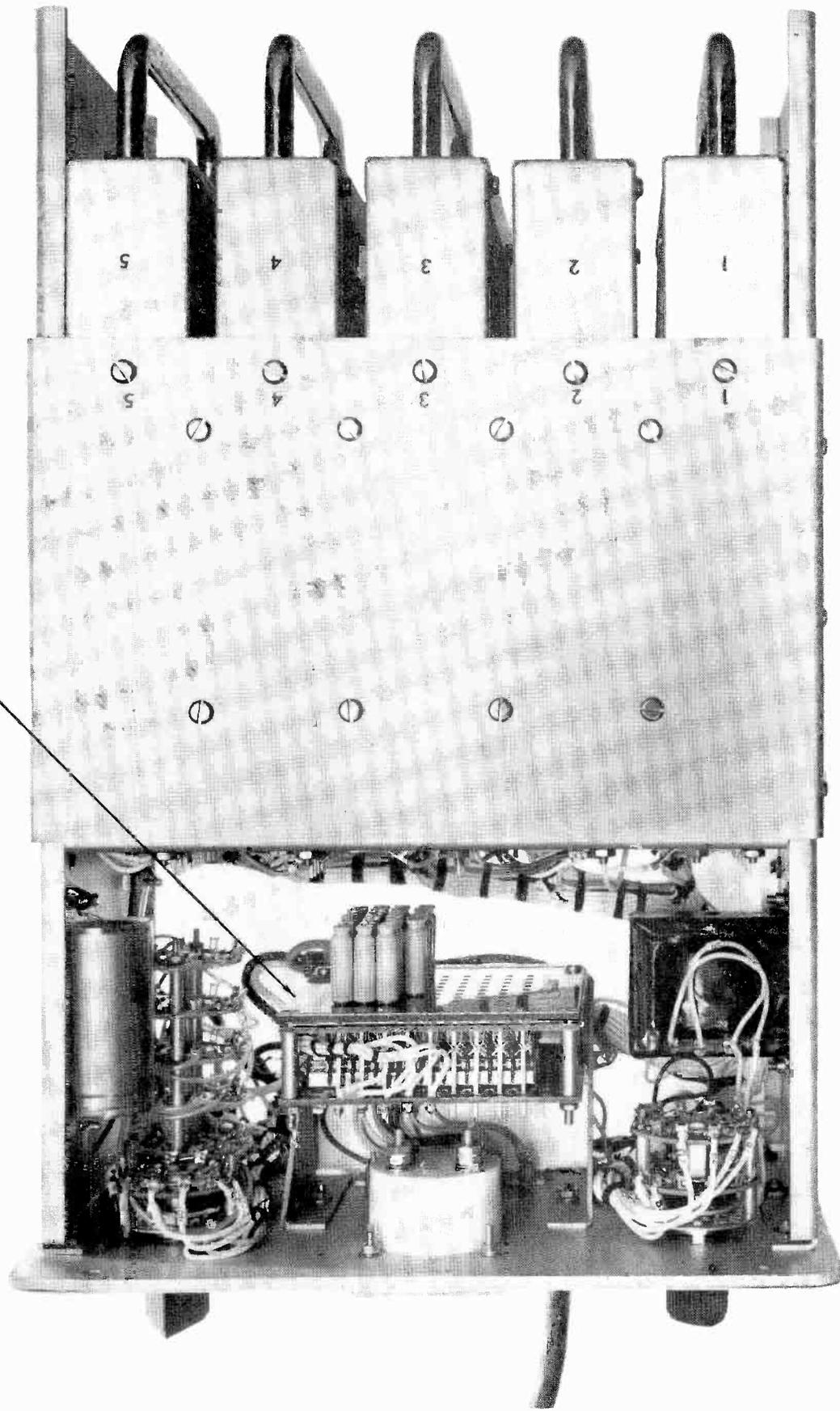
FIGURE 1



DT-120 REAR VIEW

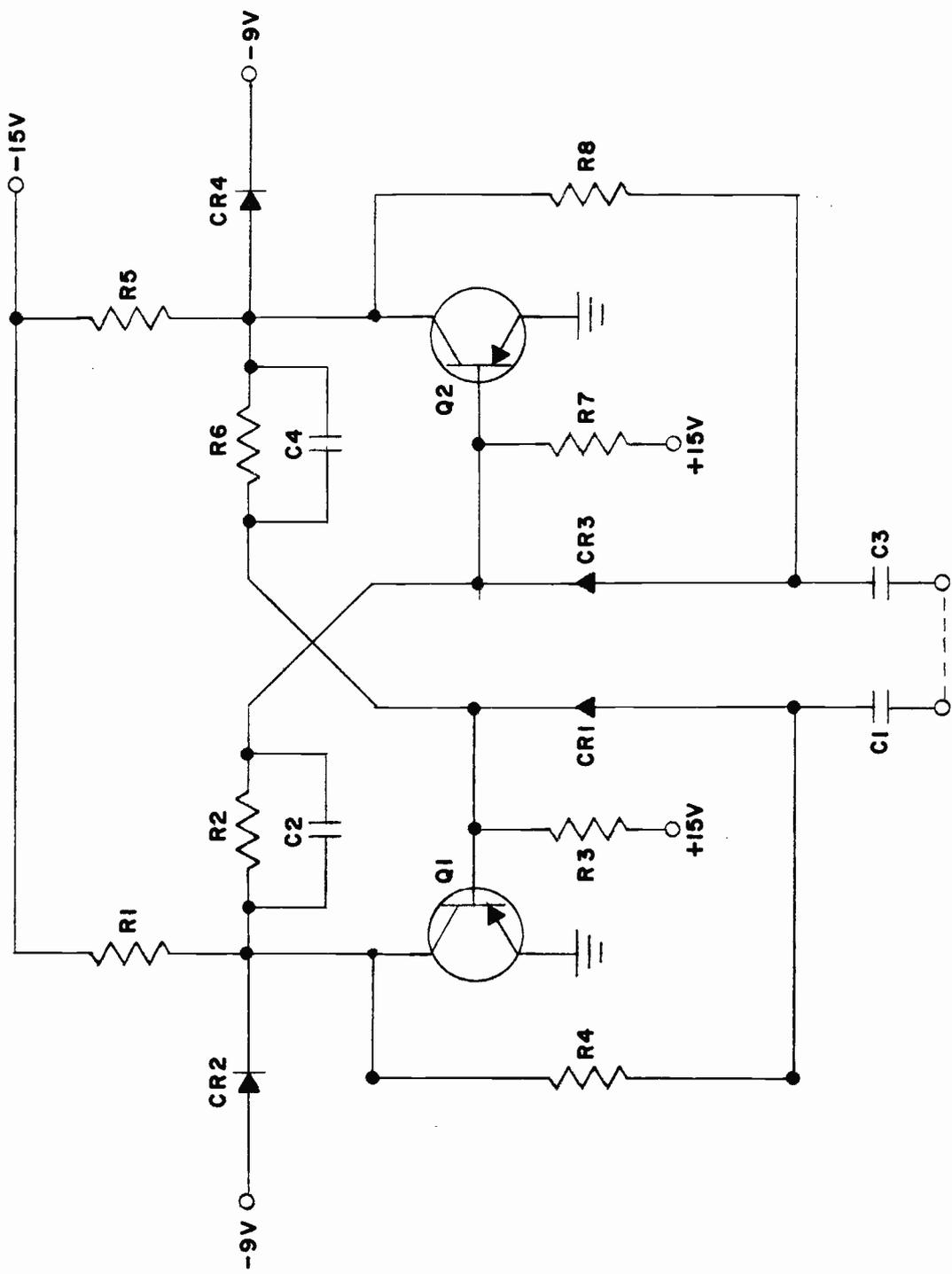
FIGURE 2

MODULE 6

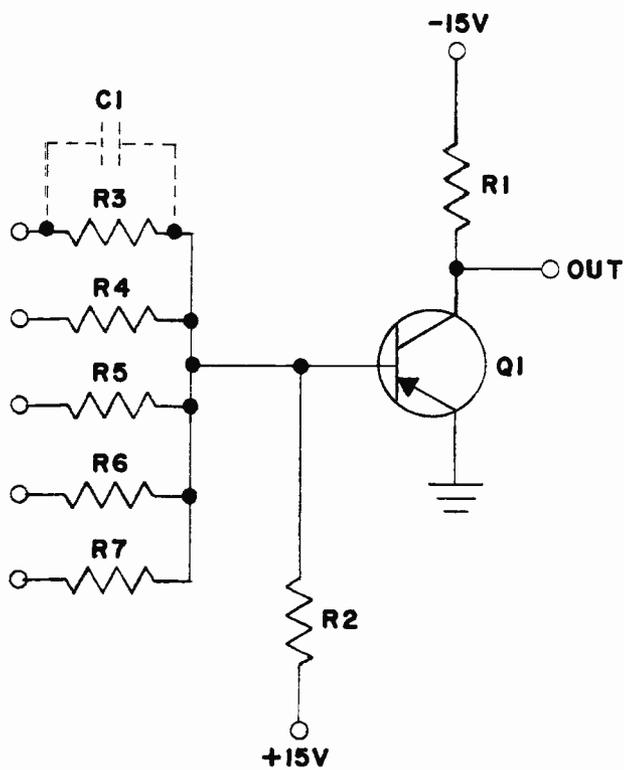


DT-120 TOP VIEW

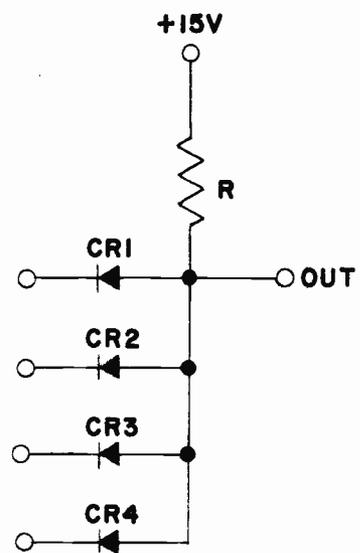
FIGURE 3



BINARY (FLIP-FLOP)

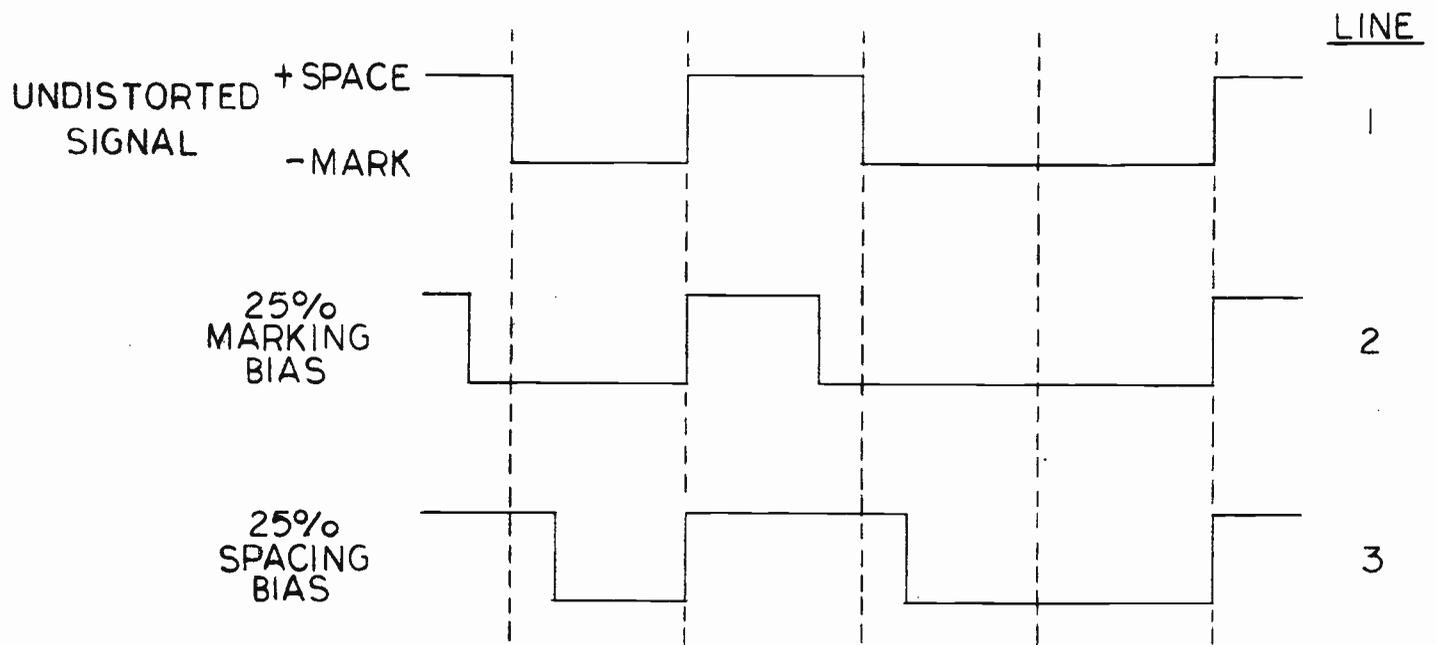


TRANSISTOR "NOR" GATE



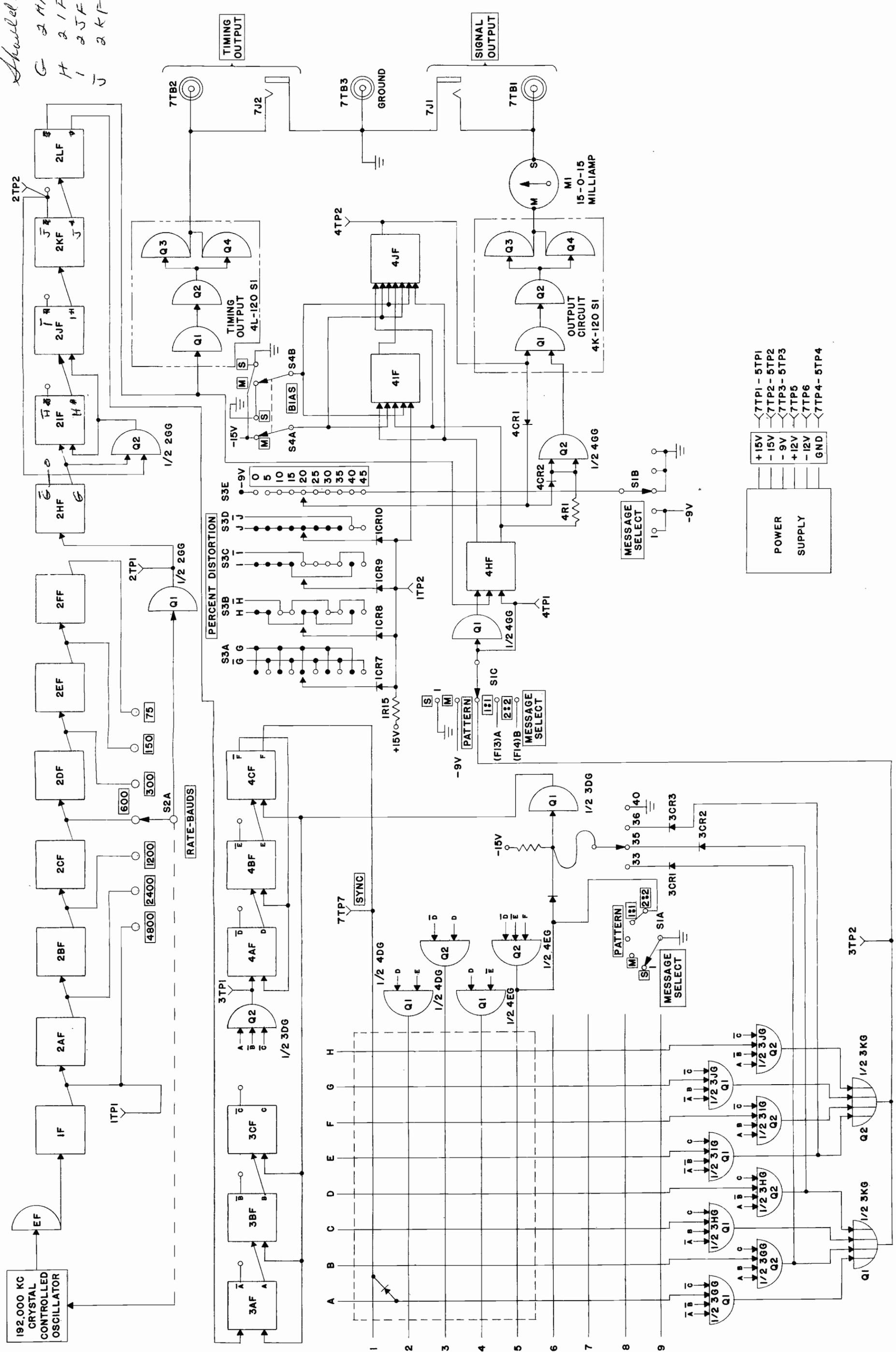
DIODE "AND" GATE

GATE CIRCUITS

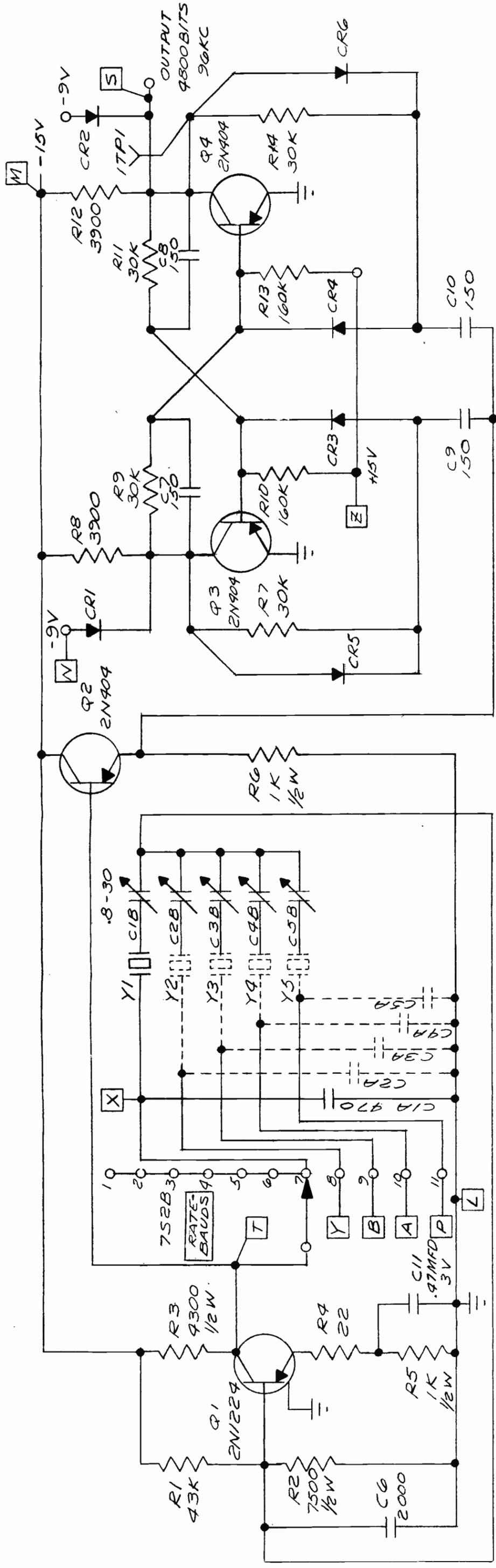


TYPES OF DISTORTION

Should be
 G 2 HF
 H 2 IF
 I 2 JF
 J 2 KF

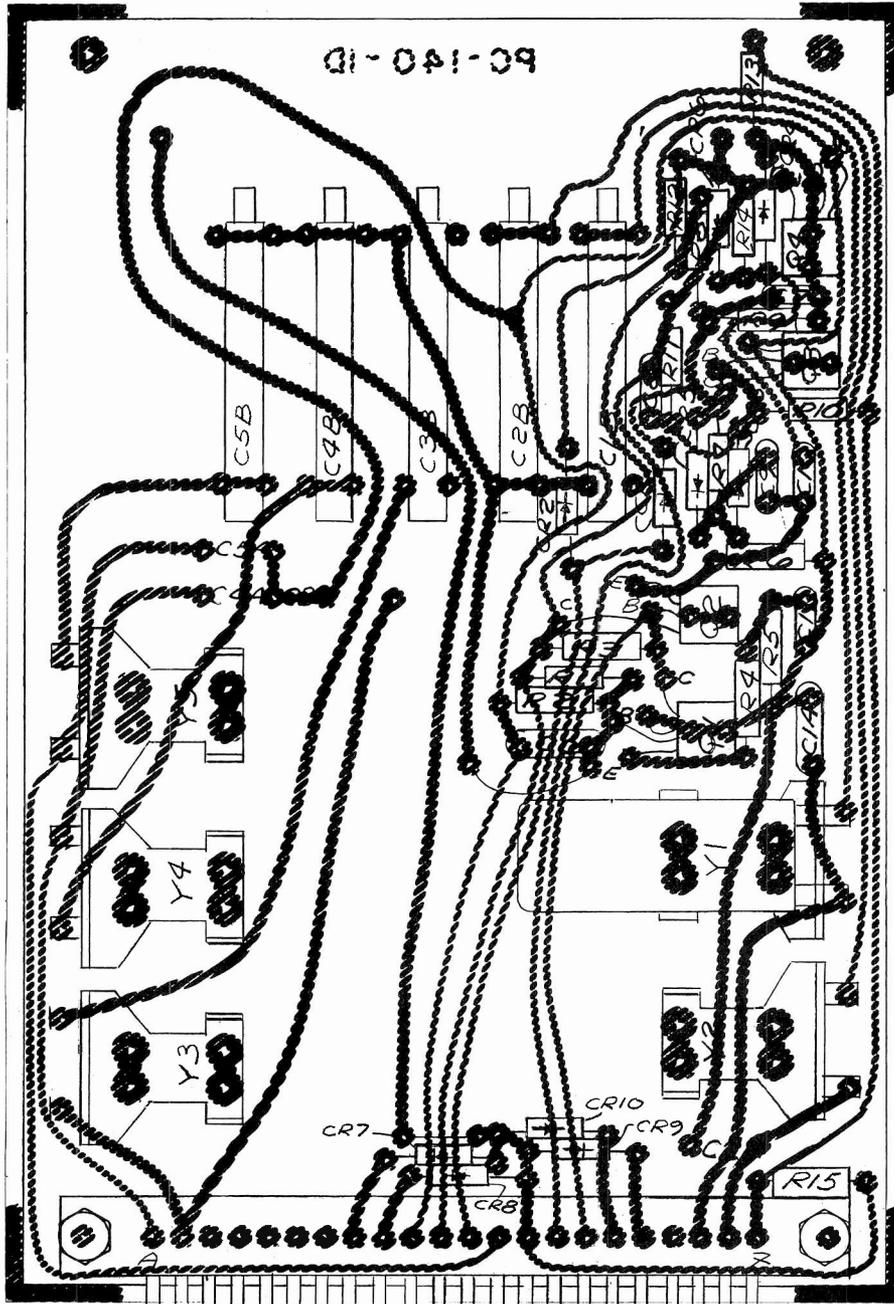


BLOCK DIAGRAM



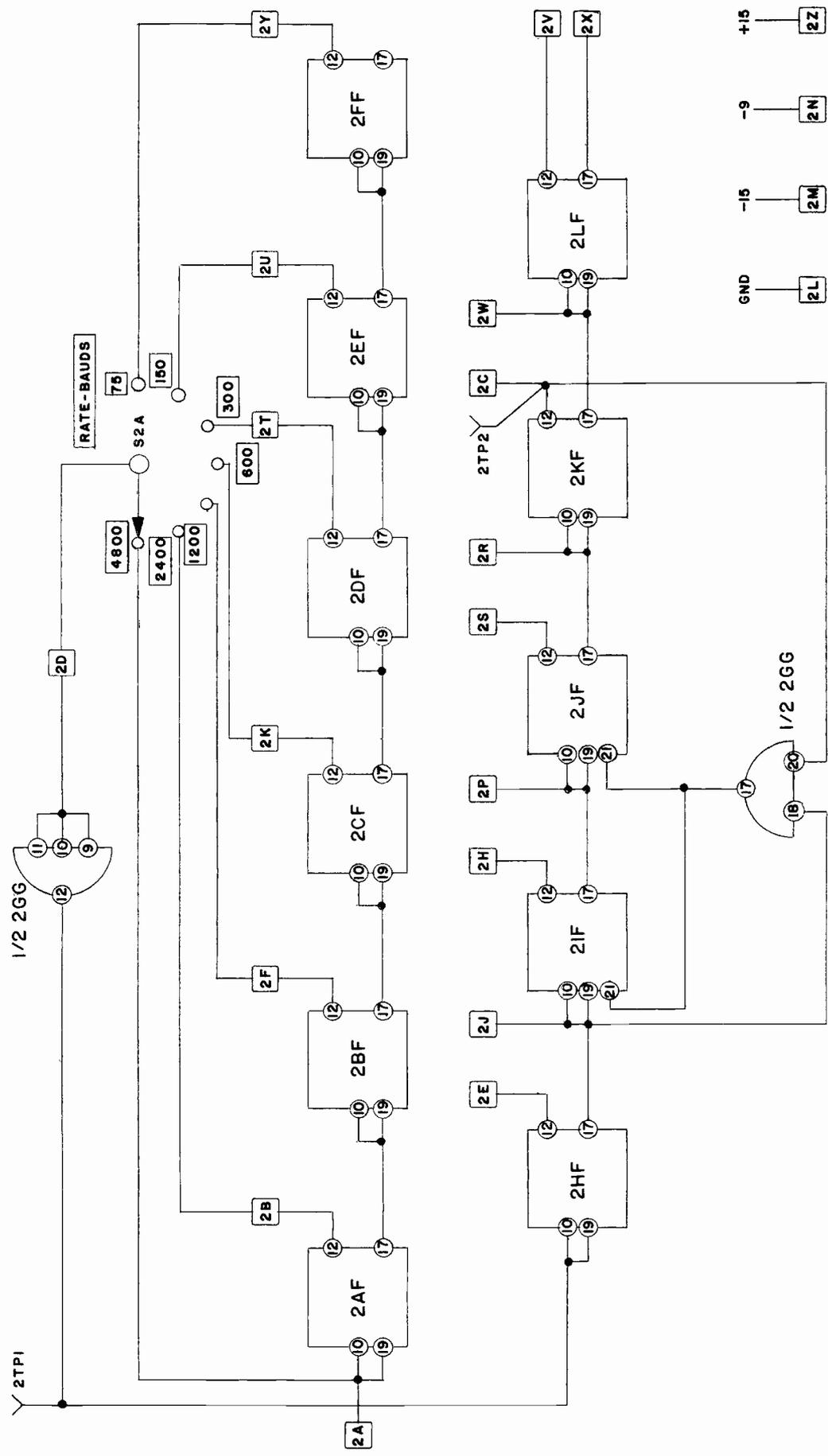
- NOTES:
- 1- CRYSTALS Y2, Y3, Y4, Y5 AND CAPACITORS C2A, C3A, C4A, C5A ARE NOT ORIGINALLY SUPPLIED WITH THE UNIT.
 - 2- UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, 1/8W, ±5% TOLERANCE.
 - 3- UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE 1N MMFD.
 - 4- THE LETTERS ENCLOSED BY A BLOCK REFER TO THE CONNECTOR PIN.

MODULE 1
SCHEMATIC DIAGRAM

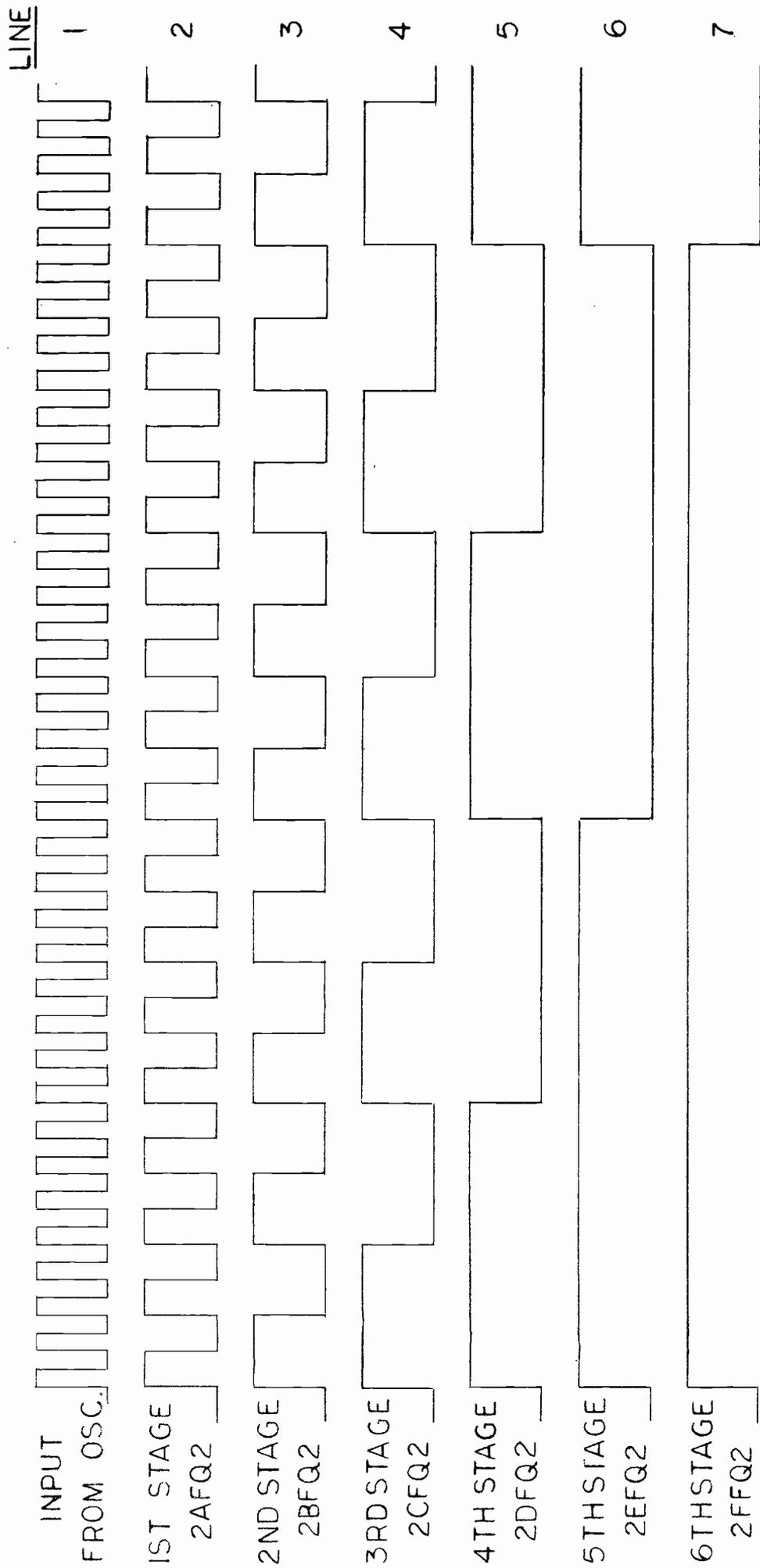


MODULE 1
COMPONENT LAYOUT

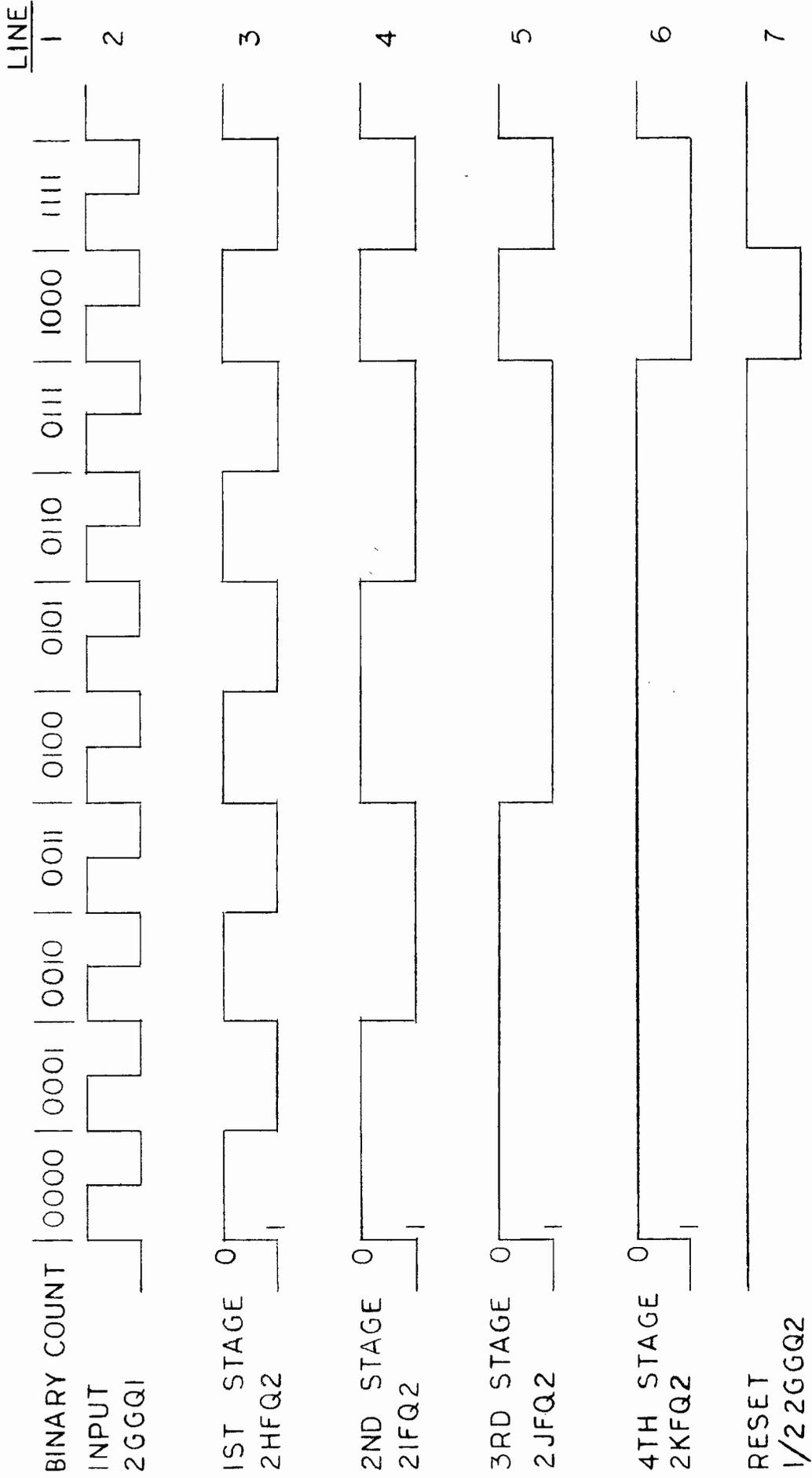
DT-120
FIGURE 8B



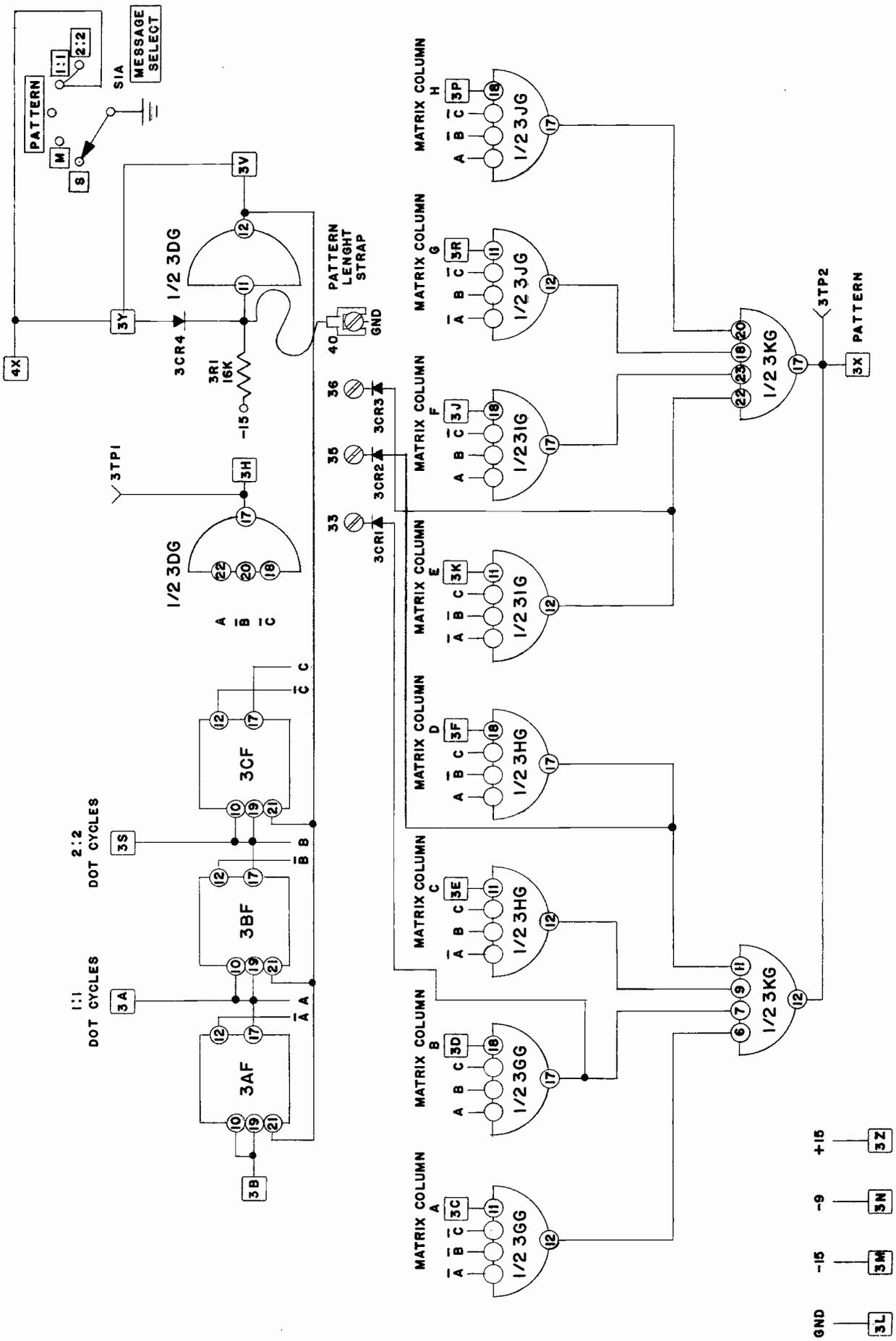
MODULE 2
BLOCK DIAGRAM



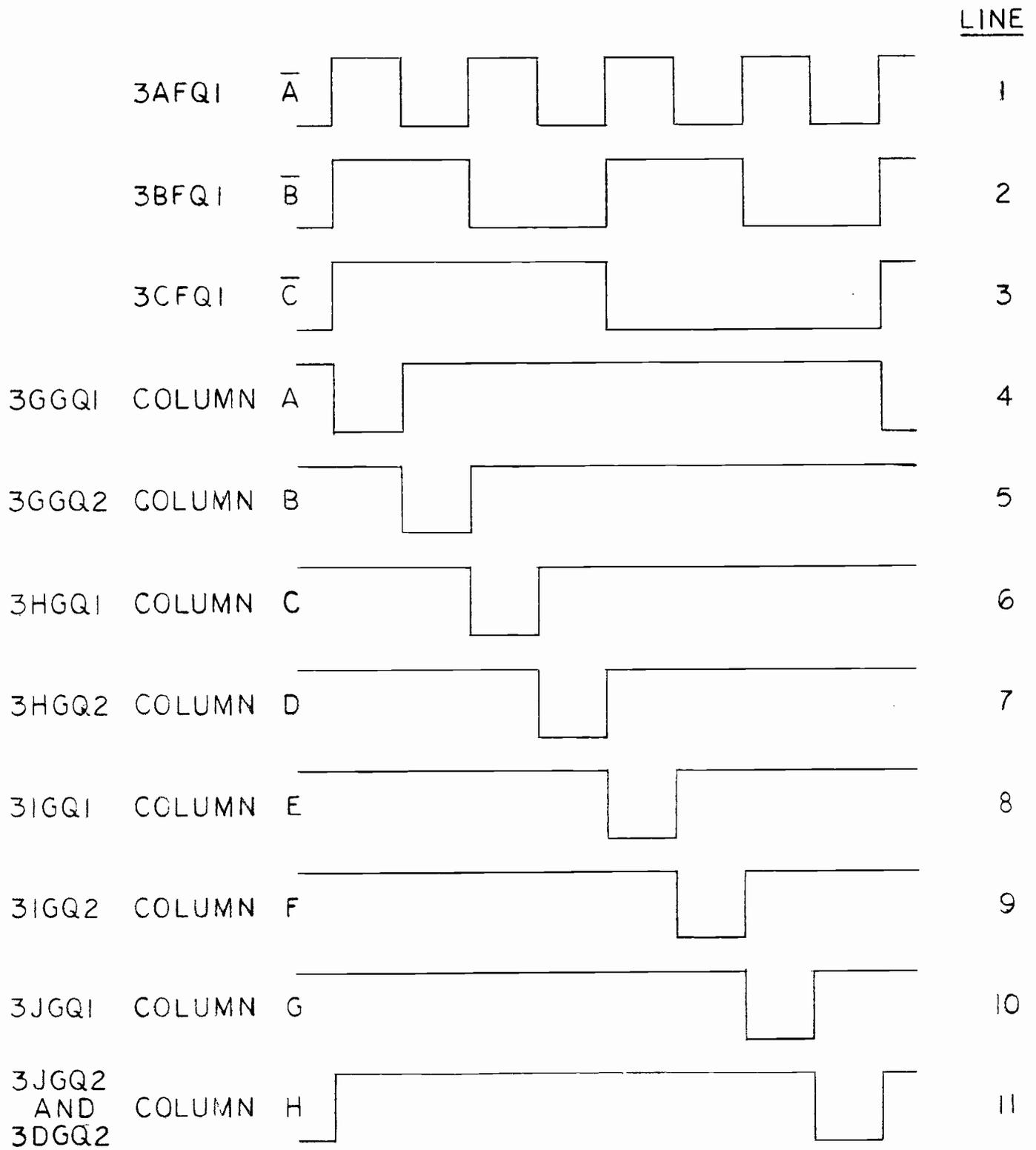
MODULE 2
TIMING COUNTDOWN WAVEFORMS



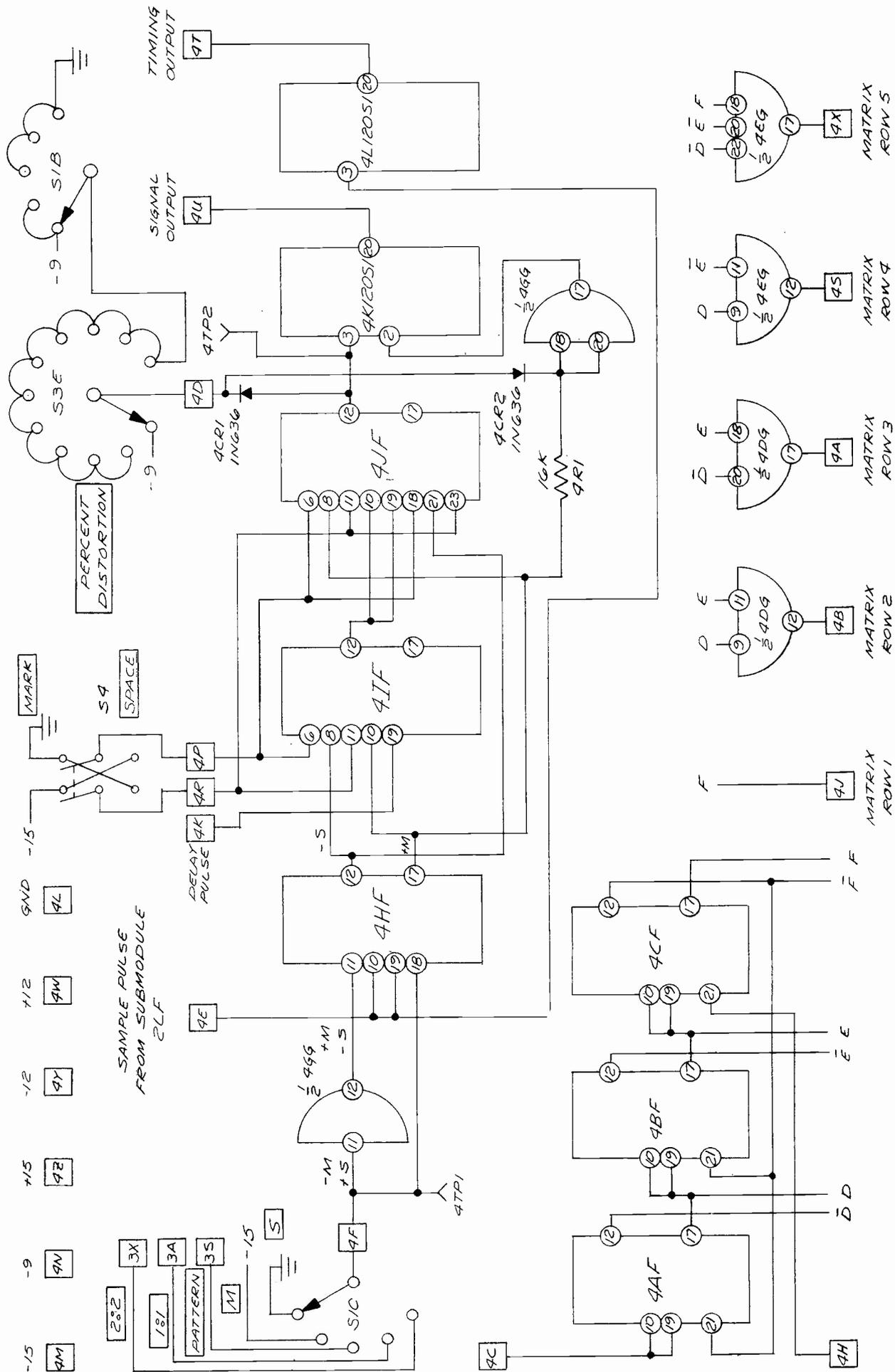
MODULE 2
 DECADE DIVIDER WAVEFORMS



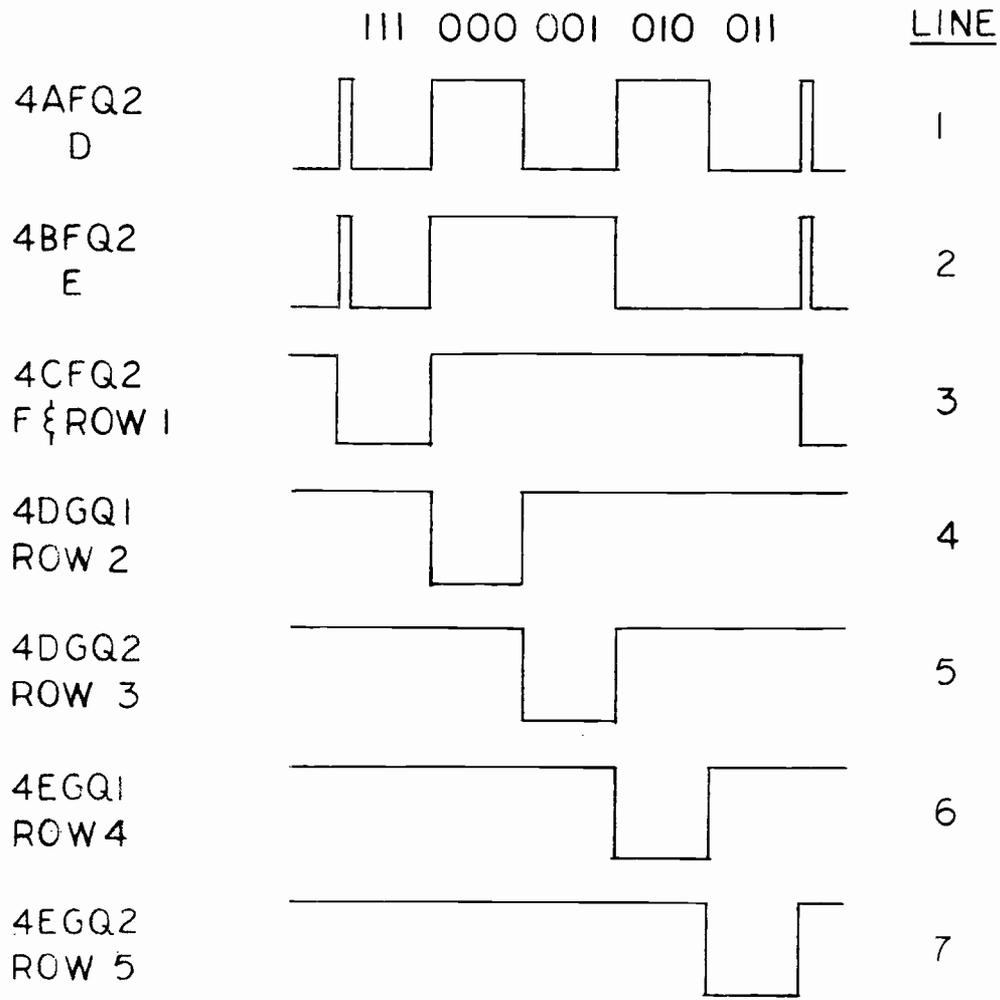
MODULE 3
BLOCK DIAGRAM



MODULE 3
COLUMN DISTRIBUTOR WAVEFORMS

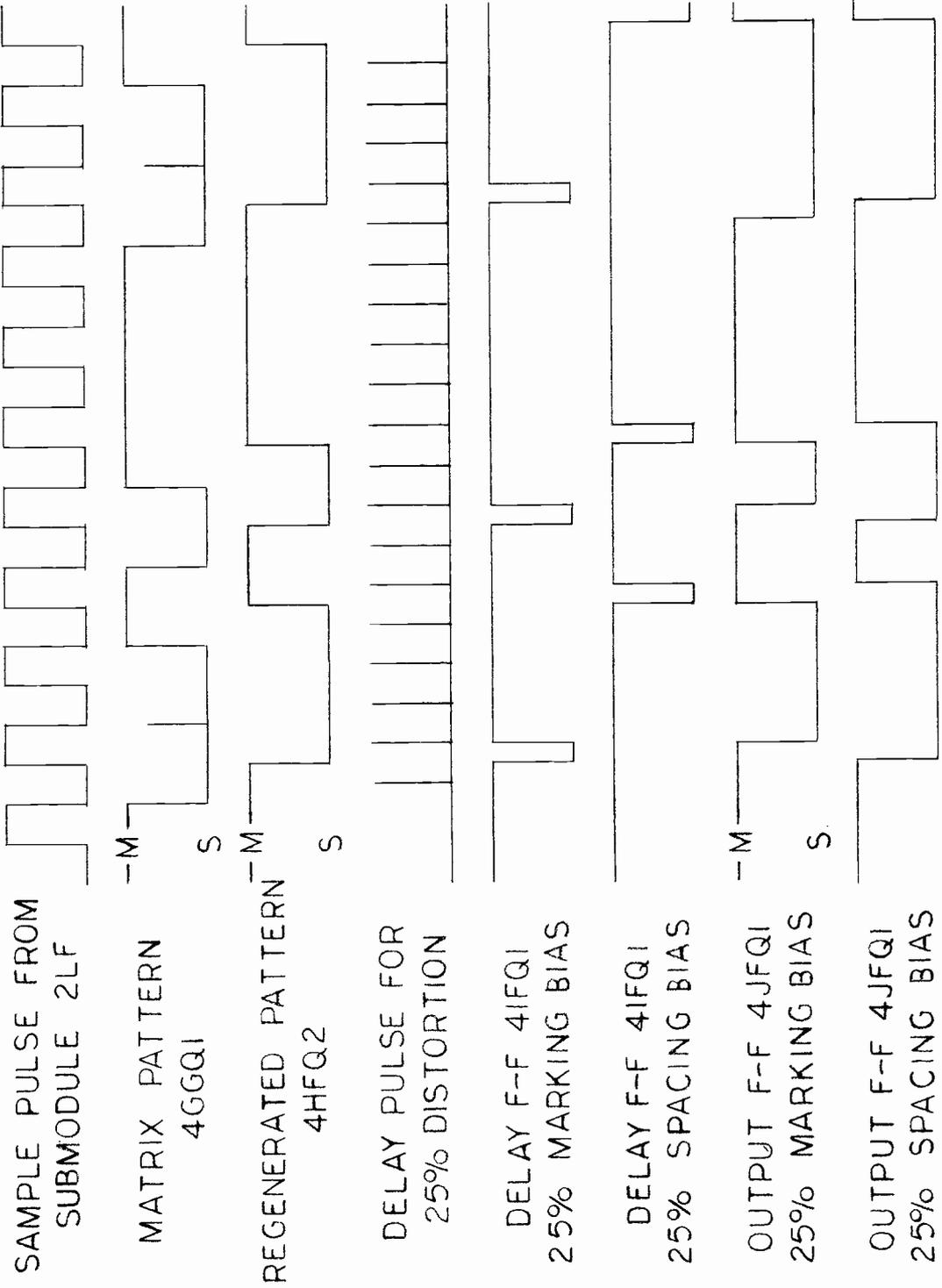


MODULE 9, BLOCK DIAGRAM

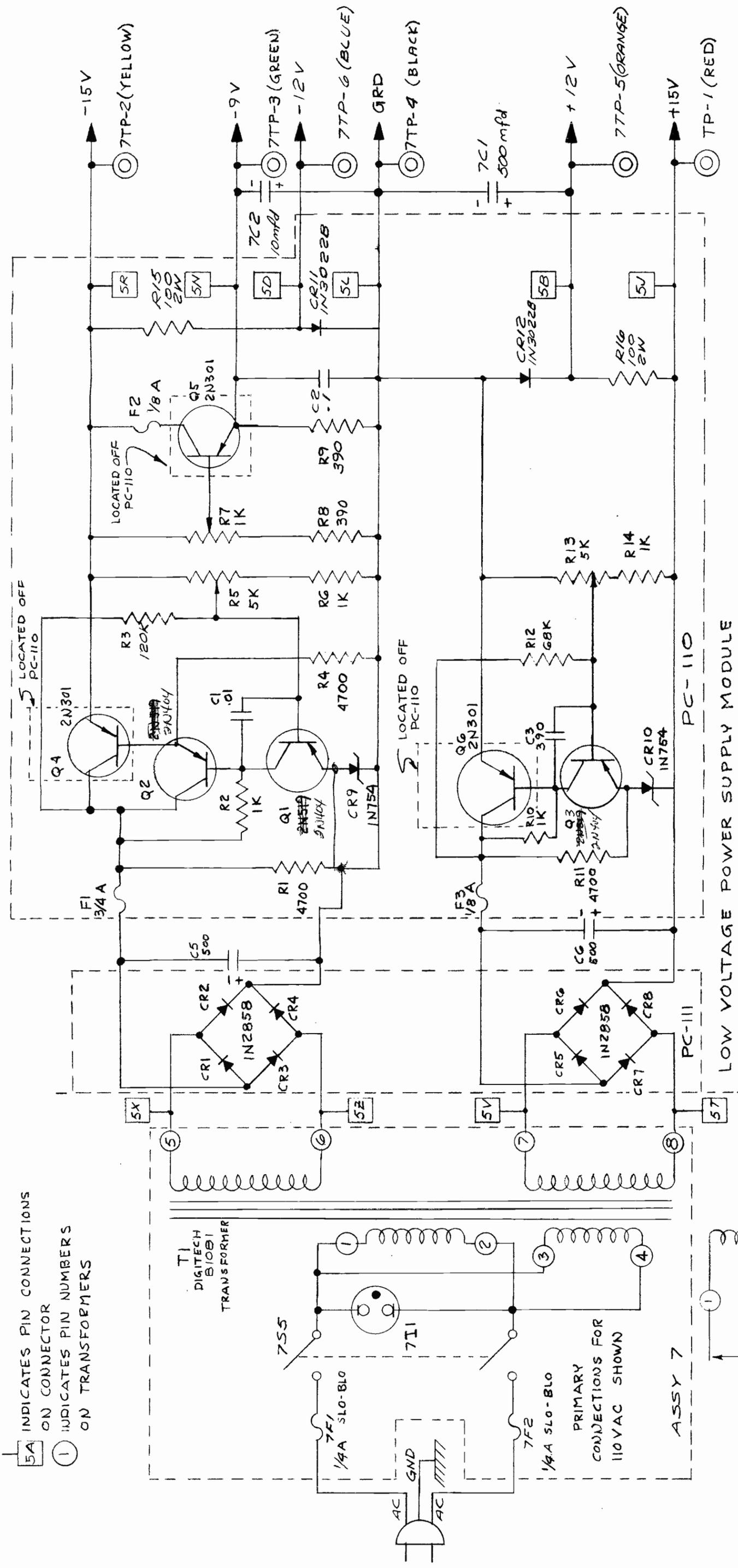


MODULE 4
ROW DISTRIBUTOR WAVEFORMS

LINE



MODULE 4
DISTORTION CIRCUIT WAVEFORMS

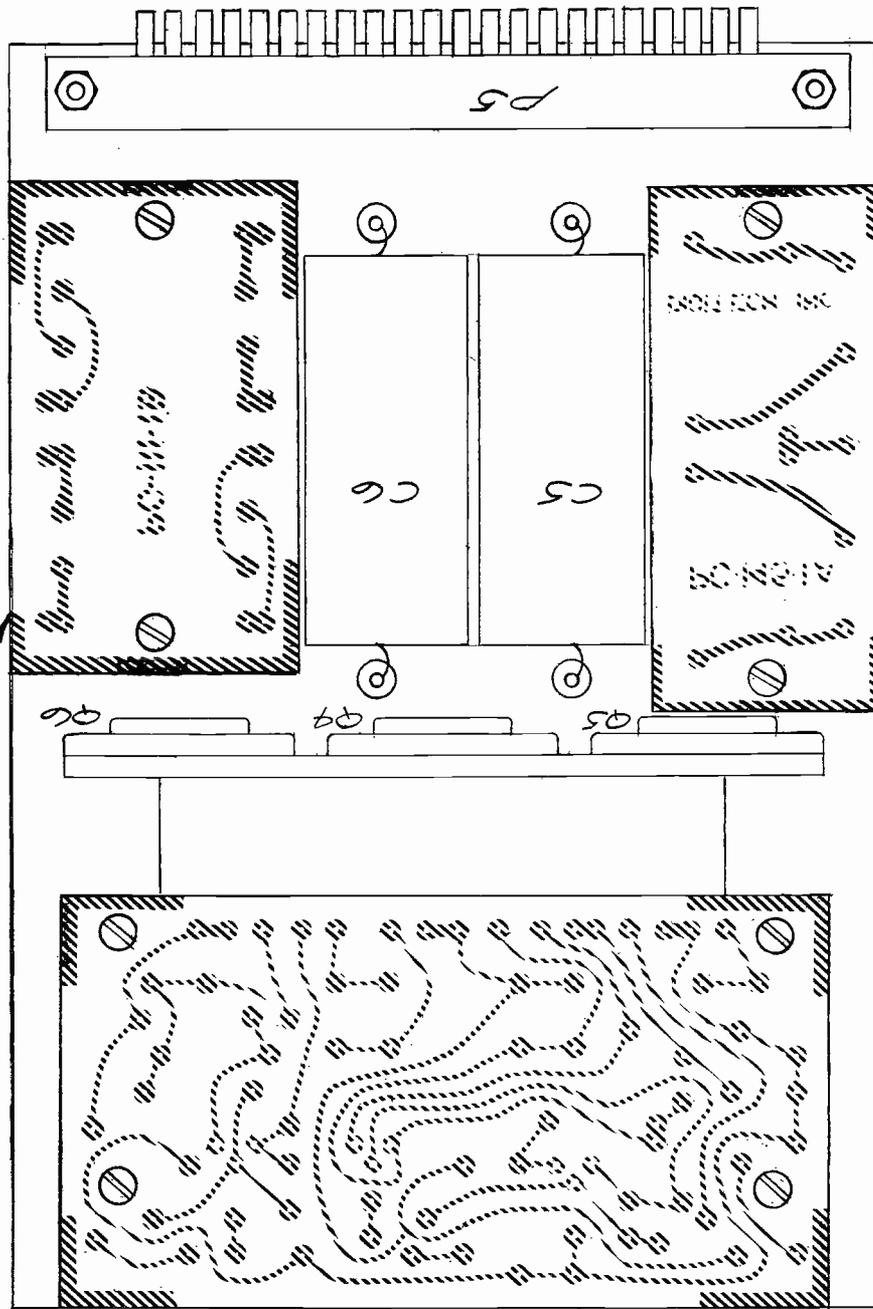


5A INDICATES PIN CONNECTIONS ON CONNECTOR
 1 INDICATES PIN NUMBERS ON TRANSFORMERS

T1 DIGITECH B1081 TRANSFORMER
 T2 DIGITECH B1081 TRANSFORMER
 ASSY 7
 PRIMARY CONNECTIONS FOR 110VAC SHOWN
 230VAC
 DETAIL "A"
 PRIMARY CONNECTIONS FOR 220 VAC.

LOW VOLTAGE POWER SUPPLY MODULE

MODULE 5
SCHEMATIC DIAGRAM



P5

C6

C5

Q6

Q4

Q5

PC-110

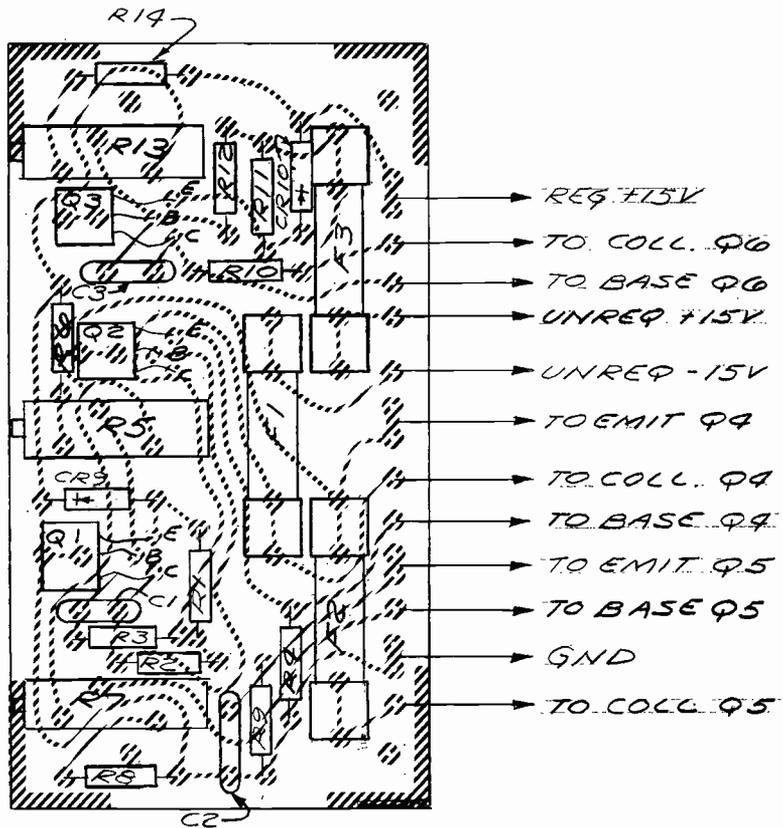
PC-195

PC-111

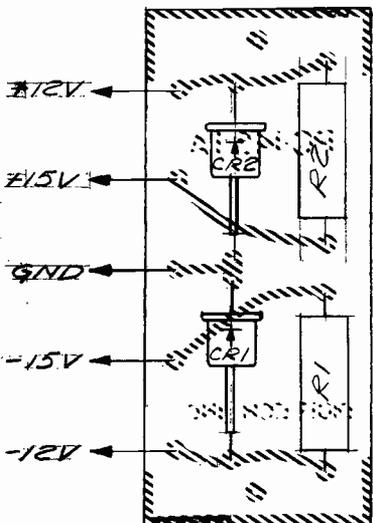
C

C

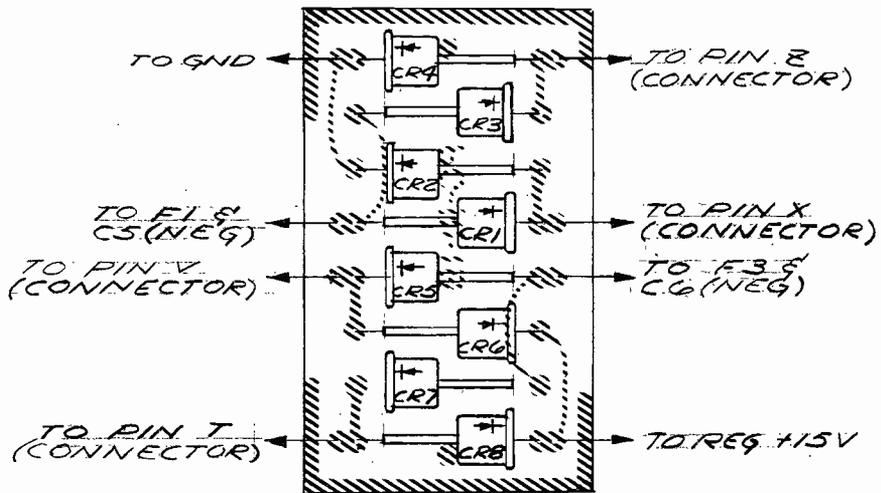
PC-110



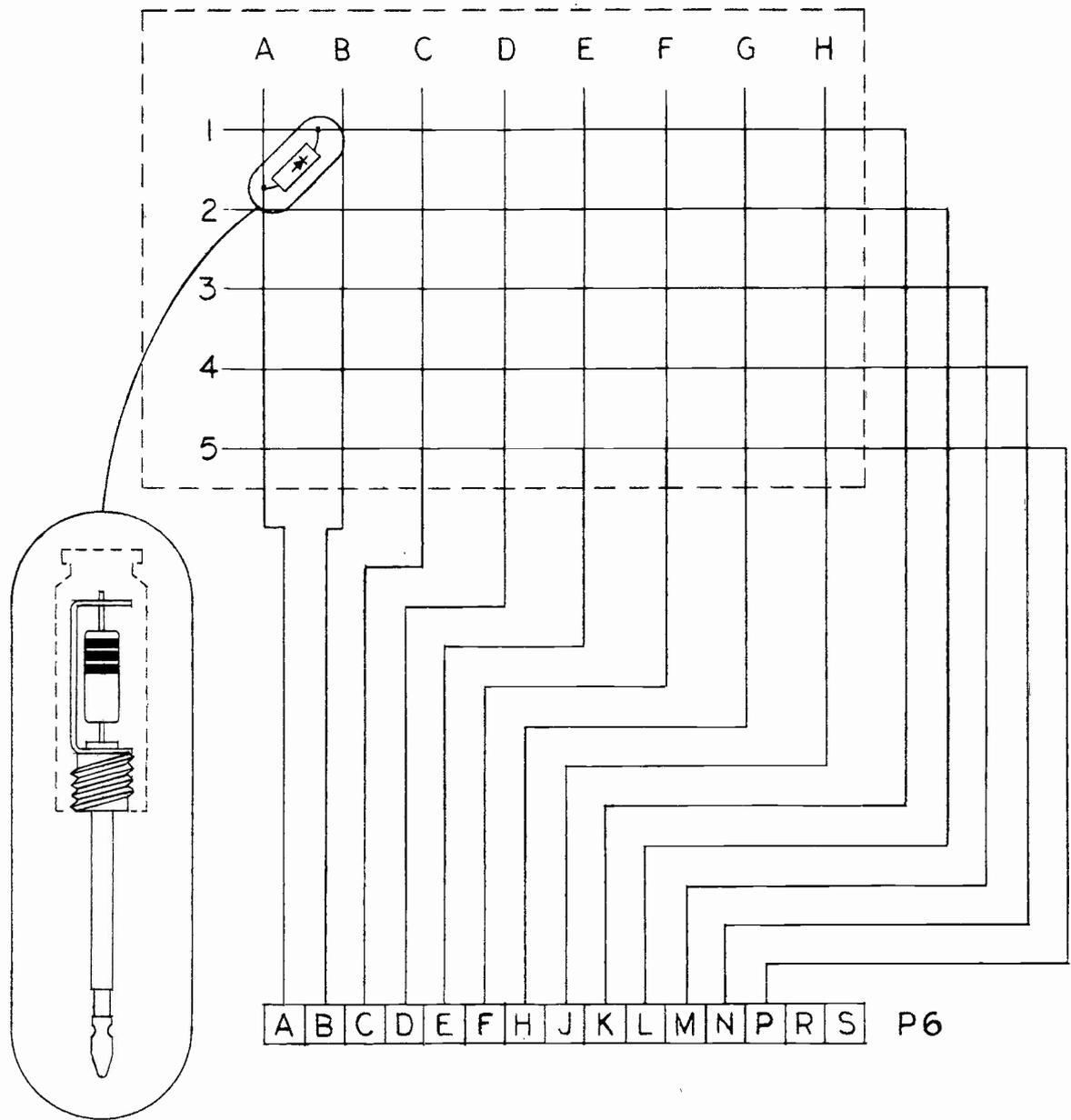
PC-195



PC-111



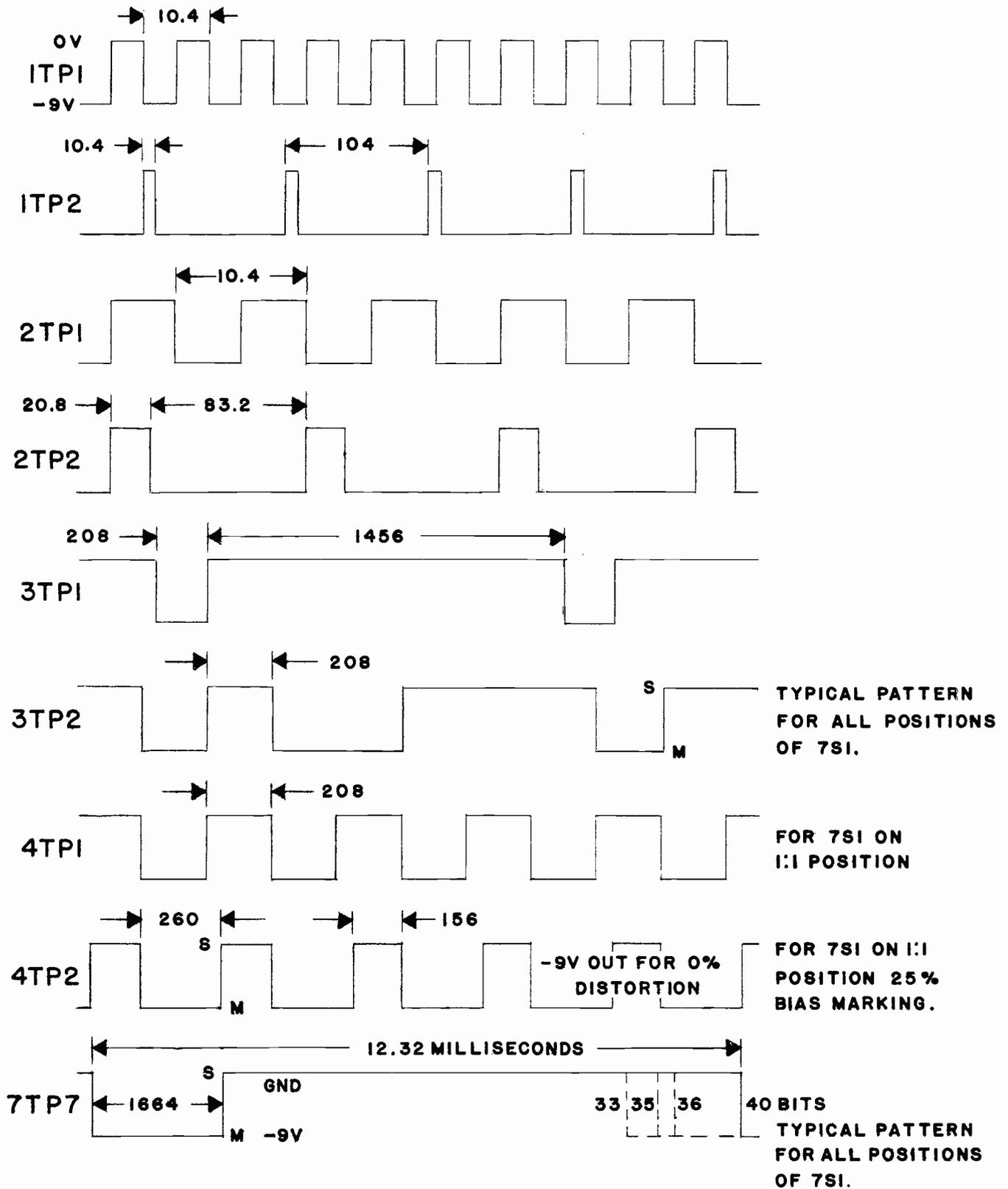
MODULE 5, COMPONENT LAYOUT



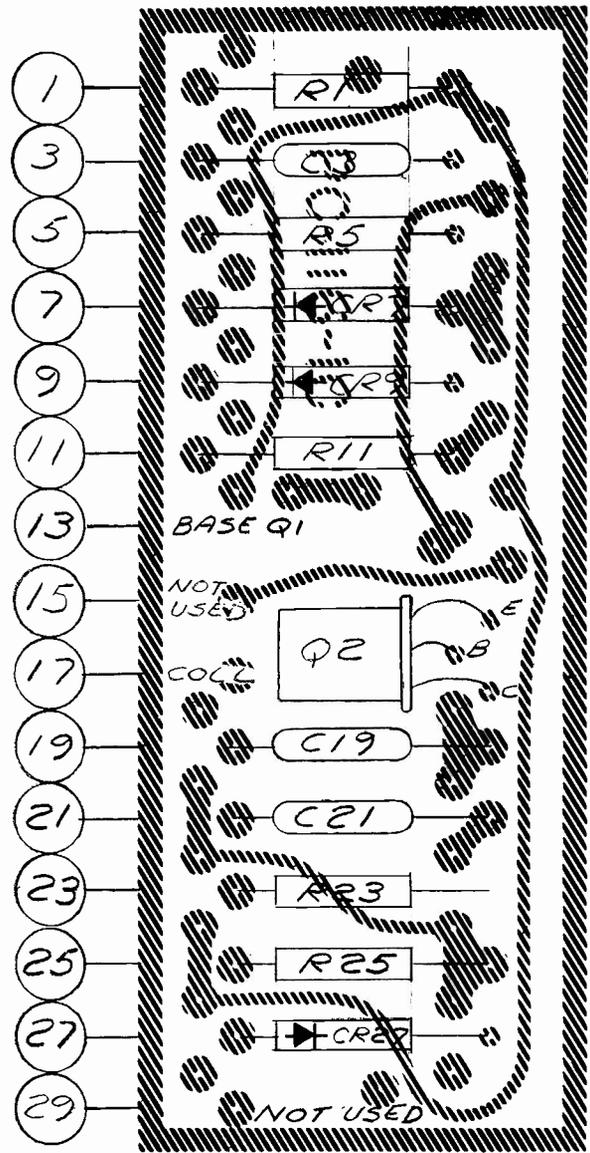
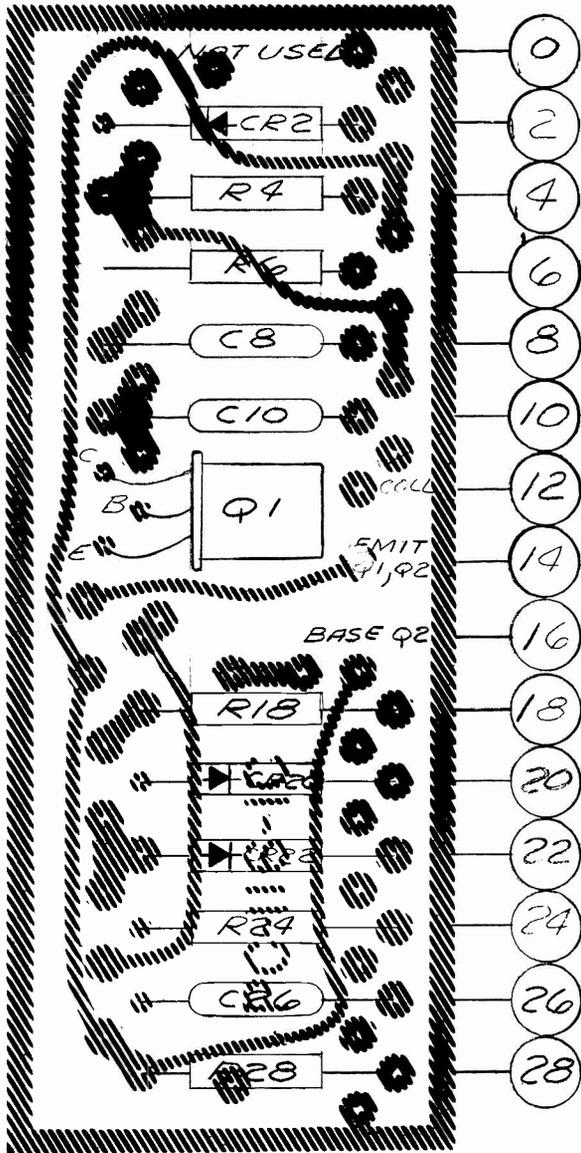
SCHEMATIC, MODULE 6

NOTE:

TIMES ARE IN MICROSECONDS FOR 4800 BAUD OPERATION.



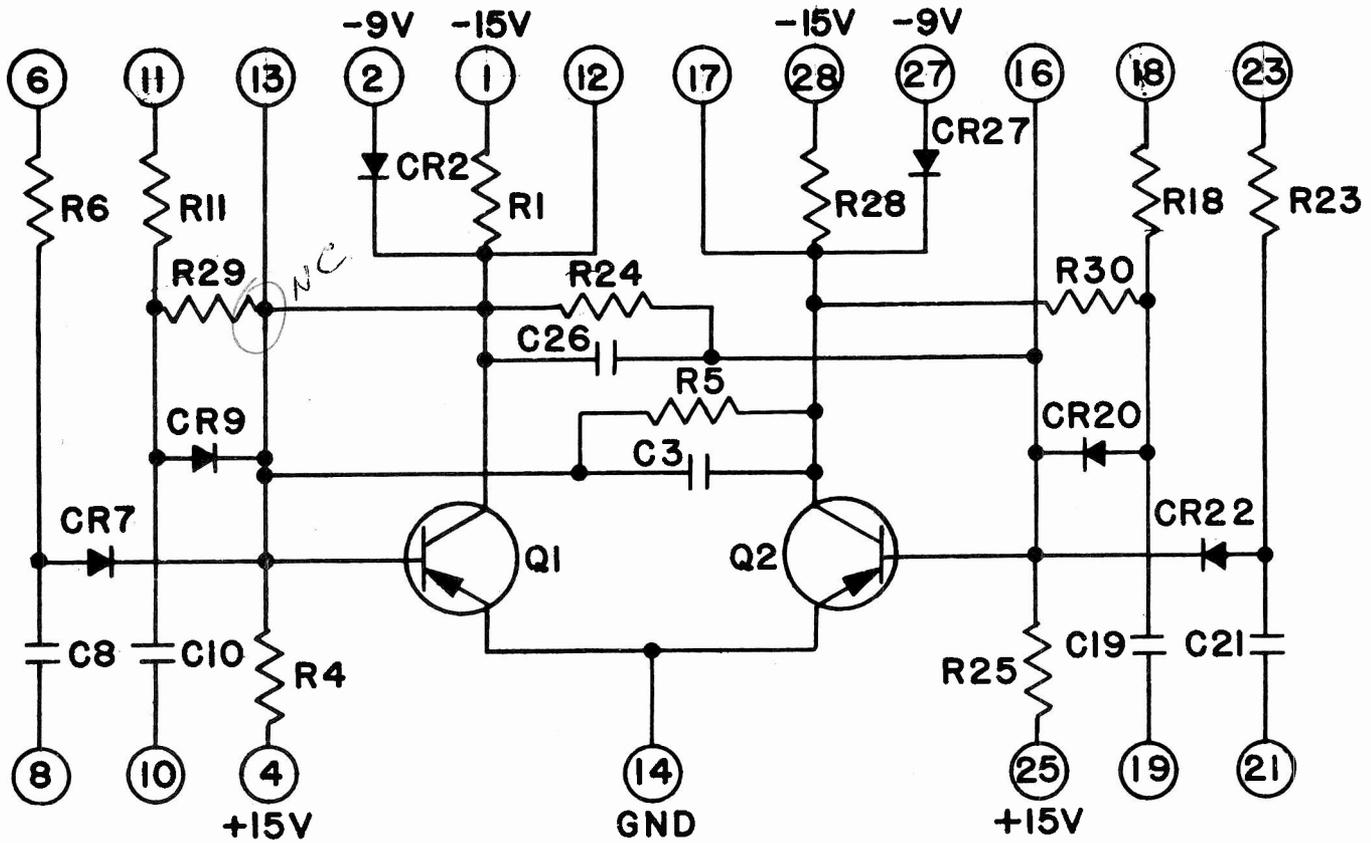
TEST POINT WAVEFORMS



NOTES:

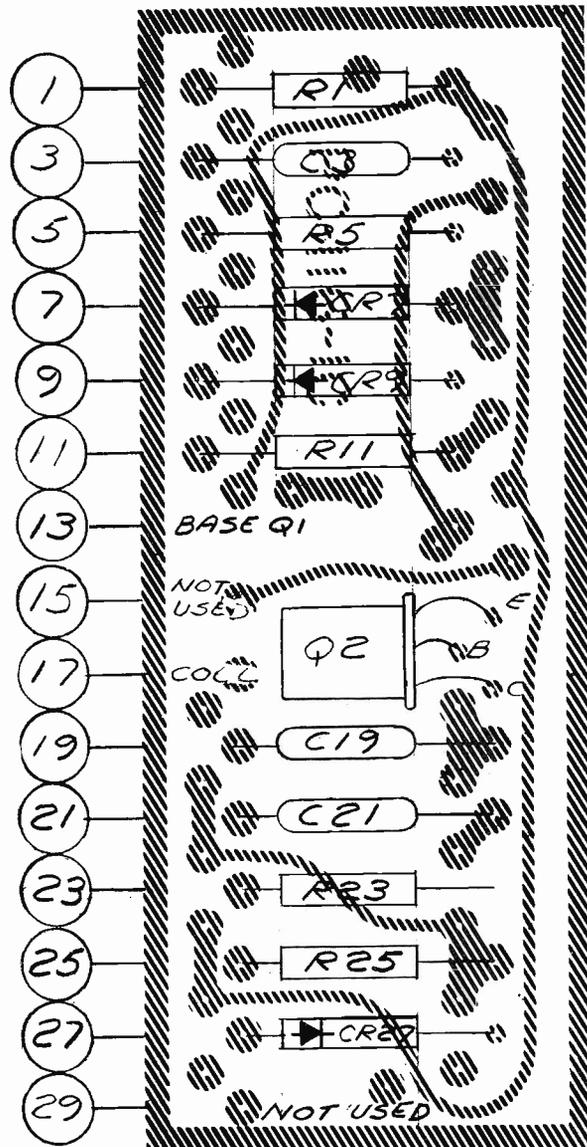
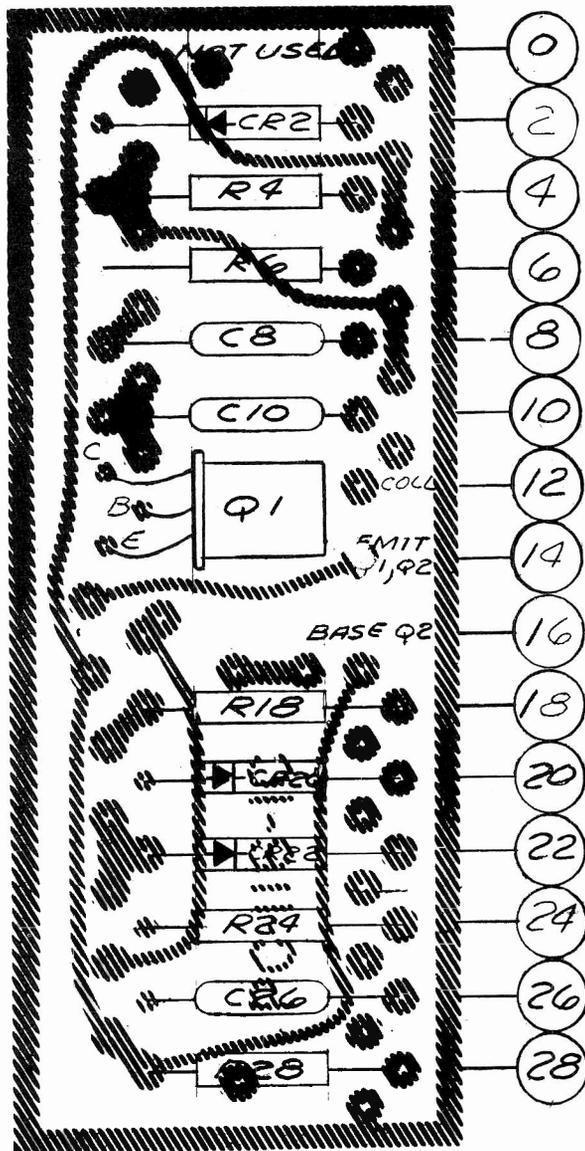
- 1- FOR EXPLANATION OF DESIGN VALUES SEE APPENDIX 1.
- 2- RESISTORS R29 AND R30 ARE NOT NORMALLY USED. SEE CHART OF SUBMODULES OR PARTS LIST FOR LISTING OF SUBMODULES WHICH USE THESE RESISTORS.

SUBMODULE, TYPE Fa
COMPOSITE LAYOUT



DESIGN VALUES

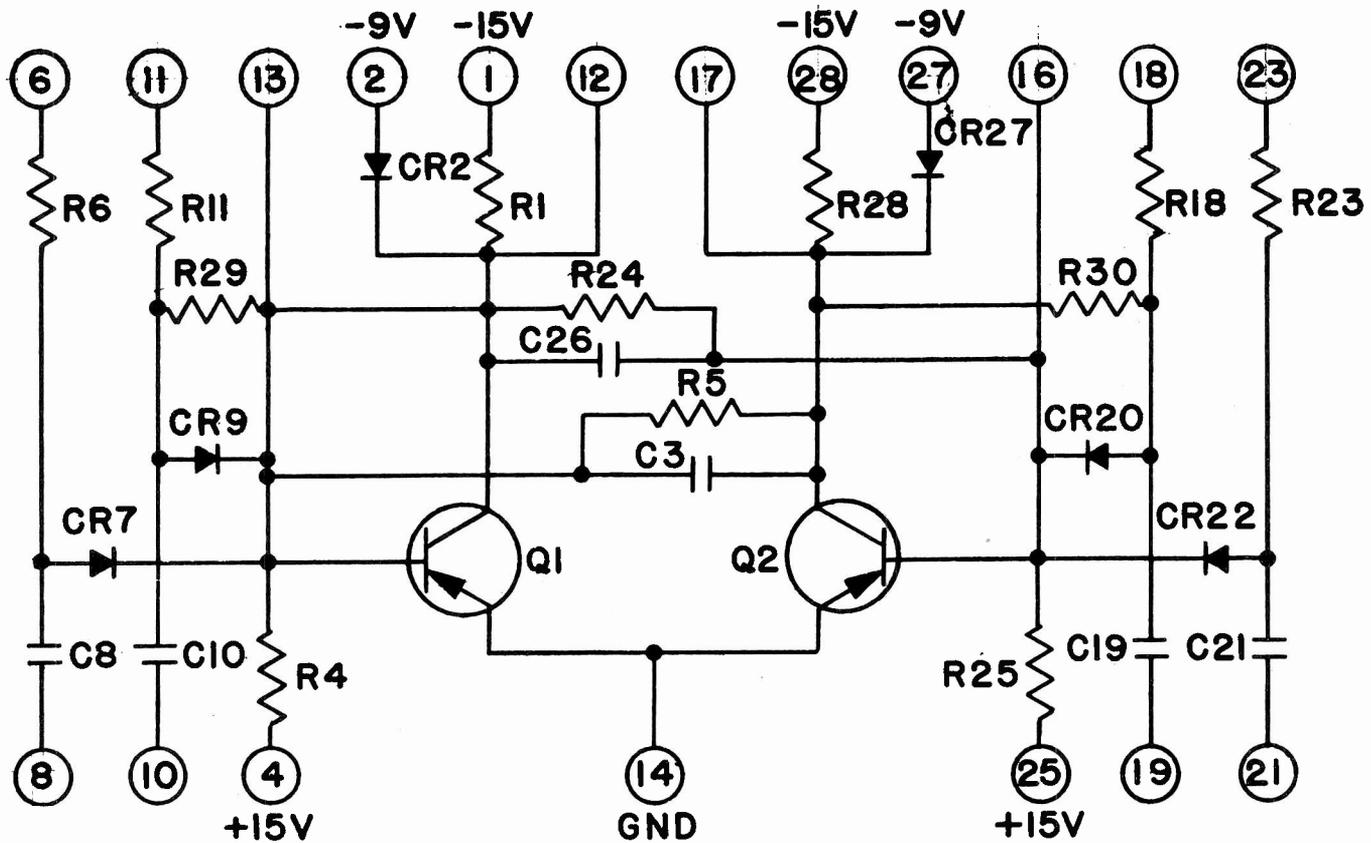
PART NUMBER	DESCRIPTION	1-1	1-2	2-1	2-2
R1	RESISTOR, 1/4W, 5%, CARBON	3900	3900	3900	3900
R4	RESISTOR, 1/4W, 5%, CARBON	160K	160K	160K	160K
R5	RESISTOR, 1/4W, 5%, CARBON	30K	30K	30K	30K
R6	RESISTOR, 1/4W, 5%, CARBON	—	—	30K	30K
R11	RESISTOR, 1/4W, 5%, CARBON	30K	30K	30K	30K
R18	RESISTOR, 1/4W, 5%, CARBON	30K	30K	30K	30K
R23	RESISTOR, 1/4W, 5%, CARBON	—	30K	—	30K
R24	RESISTOR, 1/4W, 5%, CARBON	30K	30K	30K	30K
R25	RESISTOR, 1/4W, 5%, CARBON	160K	160K	160K	160K
R28	RESISTOR, 1/4W, 5%, CARBON	3900	3900	3900	3900
R29	RESISTOR, 1/4W, 5%, CARBON	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2
R30	RESISTOR, 1/4W, 5%, CARBON	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2
C3	CAPACITOR, DIPPED MICA	82 mmf	82 mmf	82 mmf	82 mmf
C8	CAPACITOR, DIPPED MICA	—	—	82 mmf	82 mmf
C10	CAPACITOR, DIPPED MICA	82 mmf	82 mmf	82 mmf	82 mmf
C19	CAPACITOR, DIPPED MICA	82 mmf	82 mmf	82 mmf	82 mmf
C21	CAPACITOR, DIPPED, MICA	—	82 mmf	—	82 mmf
C26	CAPACITOR, DIPPED, MICA	82 mmf	82 mmf	82 mmf	82 mmf
CR2	DIODE	1N636	1N636	1N636	1N636
CR7	DIODE	—	—	1N636	1N636
CR9	DIODE	1N636	1N636	1N636	1N636
CR20	DIODE	1N636	1N636	—	1N636
CR22	DIODE	—	1N636	1N636	1N636
CR27	DIODE	1N636	1N636	1N636	1N636
Q1	TRANSISTOR	2N404	2N404	2N404	2N404
Q2	TRANSISTOR	2N404	2N404	2N404	2N404



NOTES:

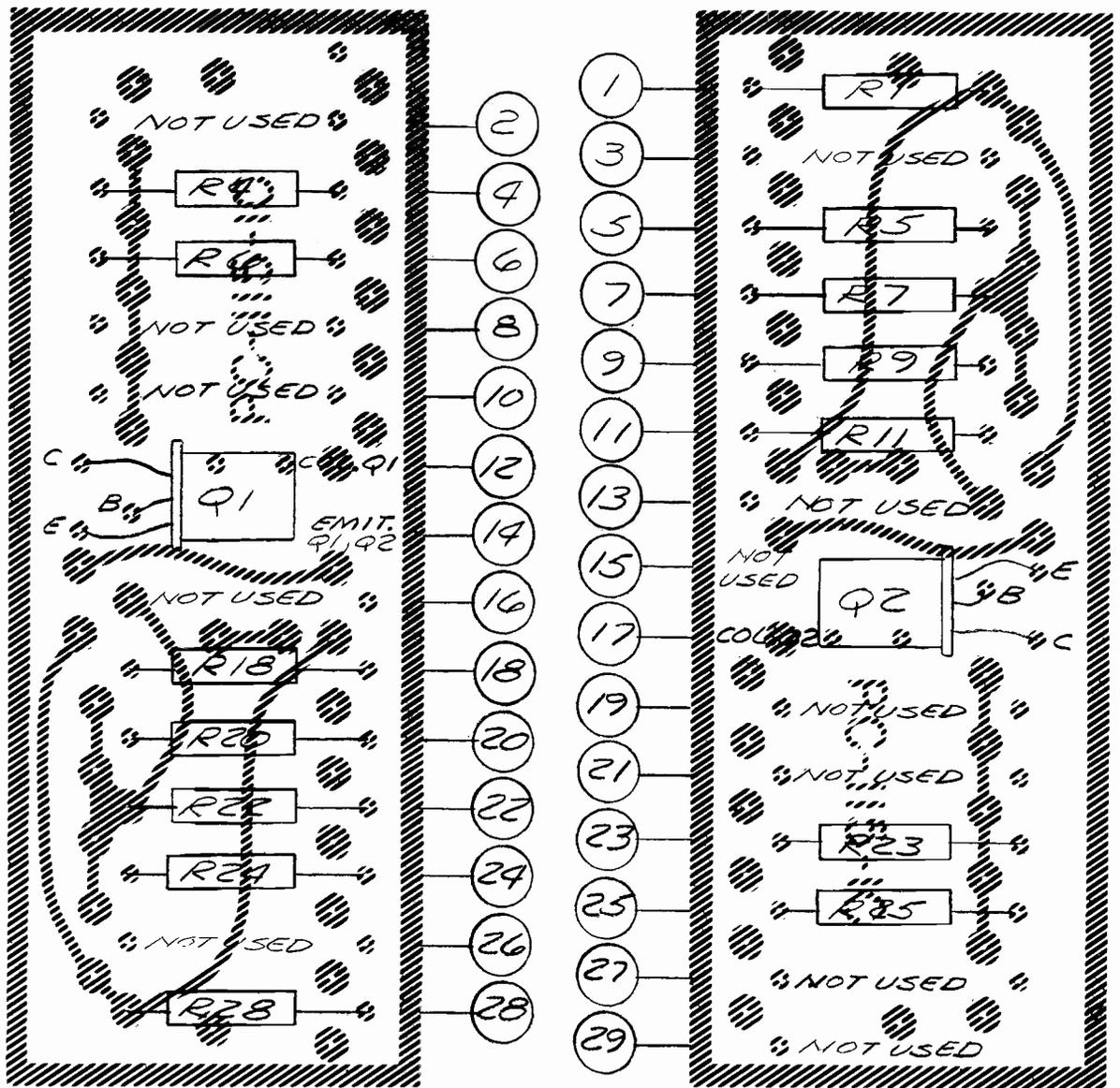
- 1- FOR EXPLANATION OF DESIGN VALUES SEE APPENDIX 1.
- 2- RESISTORS R29 AND R30 ARE NOT NORMALLY USED SEE CHART OF SUBMODULES OR PARTS LIST FOR LISTING OF SUBMODULES WHICH USE THESE RESISTORS

SUBMODULE, TYPE F₆
COMPOSITE LAYOUT



DESIGN VALUES

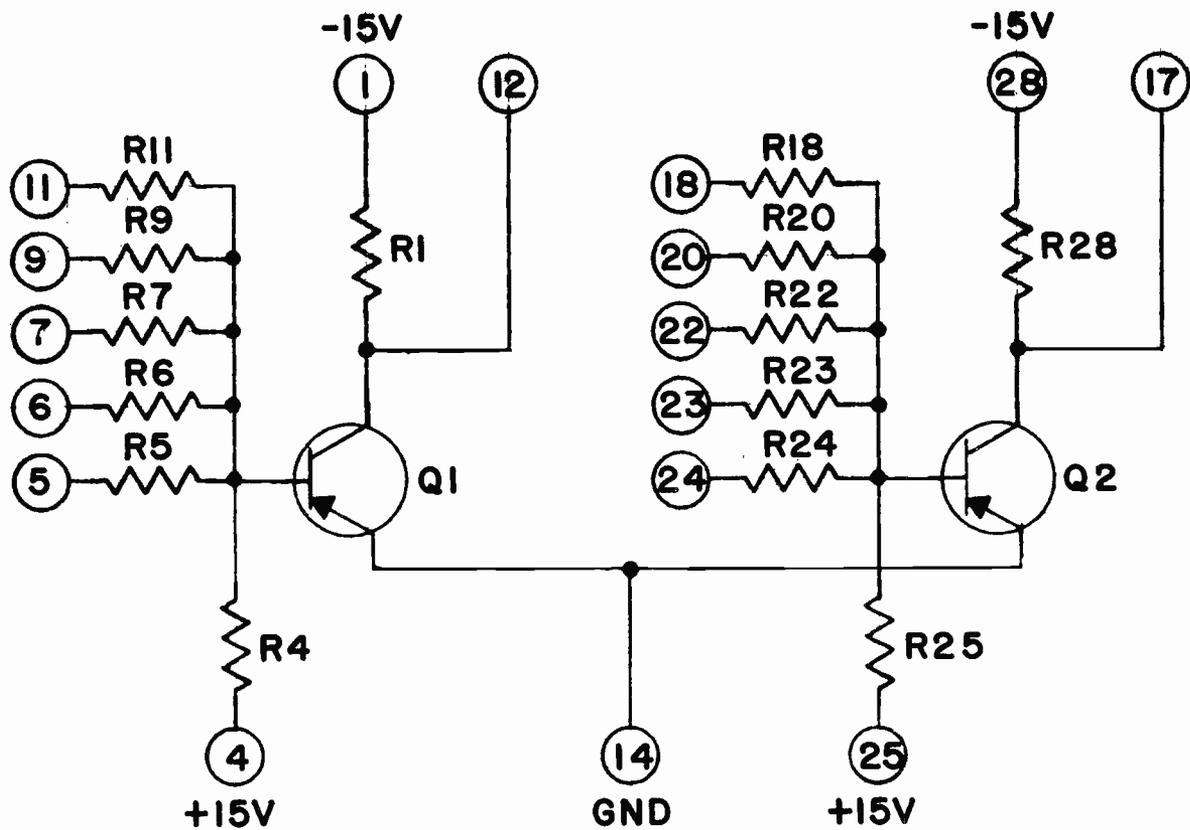
PART NUMBER	DESCRIPTION	1-1	1-2	2-1	2-2
R1	RESISTOR, 1/4W, 5%, CARBON	1800	1800	1800	1800
R4	RESISTOR, 1/4W, 5%, CARBON	120K	120K	120K	120K
R5	RESISTOR, 1/4W, 5%, CARBON	16K	14K	16K	16K
R6	RESISTOR, 1/4W, 5%, CARBON	—	—	30K	30K
R11	RESISTOR, 1/4W, 5%, CARBON	30K	30K	30K	30K
R18	RESISTOR, 1/4W, 5%, CARBON	30K	30K	30K	30K
R23	RESISTOR, 1/4W, 5%, CARBON	—	30K	—	30K
R24	RESISTOR, 1/4W, 5%, CARBON	30K	30K	30K	16K
R25	RESISTOR, 1/4W, 5%, CARBON	120K	120K	120K	120K
R28	RESISTOR, 1/4W, 5%, CARBON	1800	1800	1800	1800
R29	RESISTOR, 1/4W, 5%, CARBON	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2
R30	RESISTOR, 1/4W, 5%, CARBON	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2	SEE NOTE 2
C3	CAPACITOR, DIPPED MICA	82 mmf	82 mmf	82 mmf	82 mmf
C8	CAPACITOR, DIPPED MICA	—	—	150 mmf	150 mmf
C10	CAPACITOR, DIPPED MICA	150 mmf	150 mmf	150 mmf	150 mmf
C19	CAPACITOR, DIPPED MICA	150 mmf	150 mmf	150 mmf	150 mmf
C21	CAPACITOR, DIPPED, MICA	—	150 mmf	—	150 mmf
C26	CAPACITOR, DIPPED, MICA	82 mmf	82 mmf	82 mmf	82 mmf
CR2	DIODE	1N636	1N636	1N636	1N636
CR7	DIODE	—	—	1N636	1N636
CR9	DIODE	1N636	1N636	1N636	1N636
CR20	DIODE	1N636	1N636	—	1N636
CR22	DIODE	—	1N636	1N636	1N636
CR27	DIODE	1N636	1N636	1N636	1N636
Q1	TRANSISTOR	2N404	2N404	2N404	2N404
Q2	TRANSISTOR	2N404	2N404	2N404	2N404



NOTE:

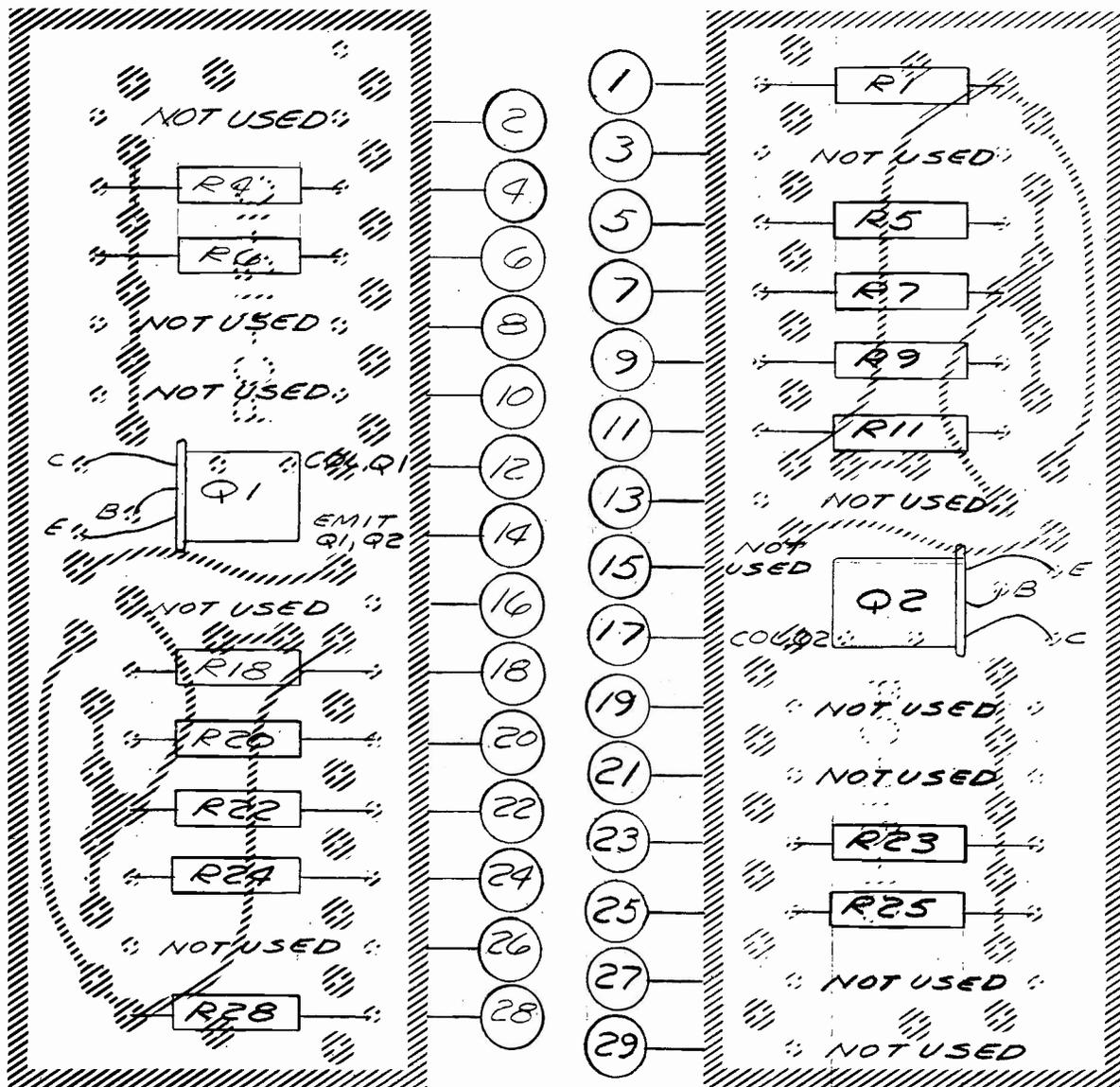
WHEN LESS THAN FIVE INPUTS ARE PROVIDED THE RESISTORS ARE PICKED ACCORDING TO THE FOLLOWING TABLE

NUMBER OF INPUTS	Q1	Q2
1	R11	R18
2	R11, R9	R18, R20
3	R11, R9, R7	R18, R20, R22
4	R11, R9, R7, R6	R18, R20, R22, R23
5	R11, R9, R7, R6, R5	R18, R20, R22, R23, R24



DESIGN VALUES		
PART NUMBER	DESCRIPTION	VALUE
R1	RESISTOR, CARBON, 1/4W, 5%	3900
R4	RESISTOR, CARBON, 1/4W, 5%	160K
R5	RESISTOR, CARBON, 1/4W, 5%	30K
R6	RESISTOR, CARBON, 1/4W, 5%	30K
R7	RESISTOR, CARBON, 1/4W, 5%	30K
R9	RESISTOR, CARBON, 1/4W, 5%	30K
R11	RESISTOR, CARBON, 1/4W, 5%	30K
R18	RESISTOR, CARBON, 1/4W, 5%	30K
R20	RESISTOR, CARBON, 1/4W, 5%	30K
R22	RESISTOR, CARBON, 1/4W, 5%	30K
R23	RESISTOR, CARBON, 1/4W, 5%	30K
R24	RESISTOR, CARBON, 1/4W, 5%	30K
R25	RESISTOR, CARBON, 1/4W, 5%	160K
R28	RESISTOR, CARBON, 1/4W, 5%	3900
Q1	TRANSISTOR	2N404
Q2	TRANSISTOR	2N404

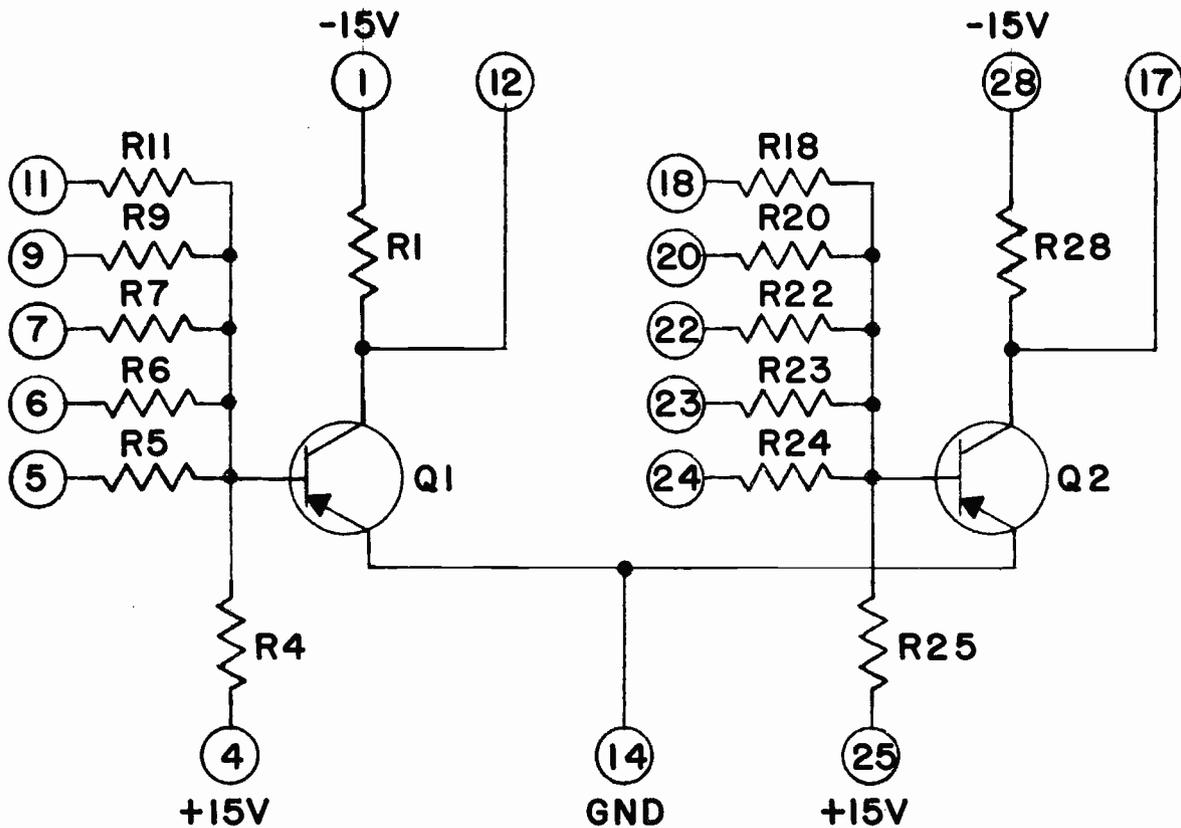
SUBMODULE, TYPE G_a
COMPOSITE LAYOUT



NOTE:

WHEN LESS THAN FIVE INPUTS ARE PROVIDED THE RESISTORS ARE PICKED ACCORDING TO THE FOLLOWING TABLE.

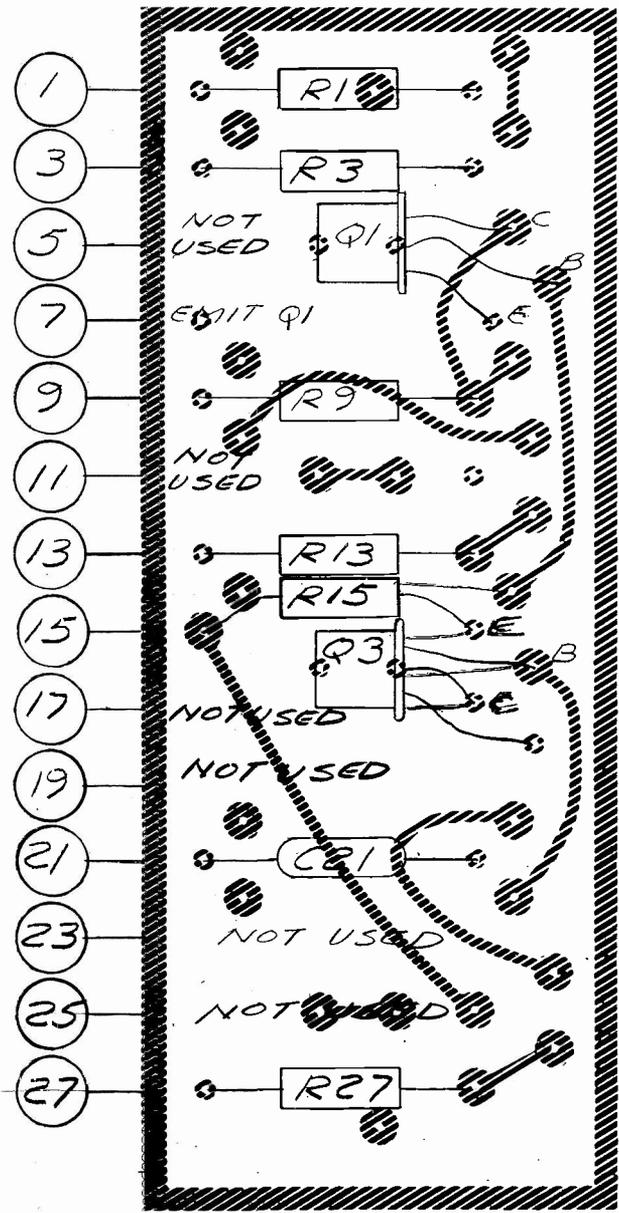
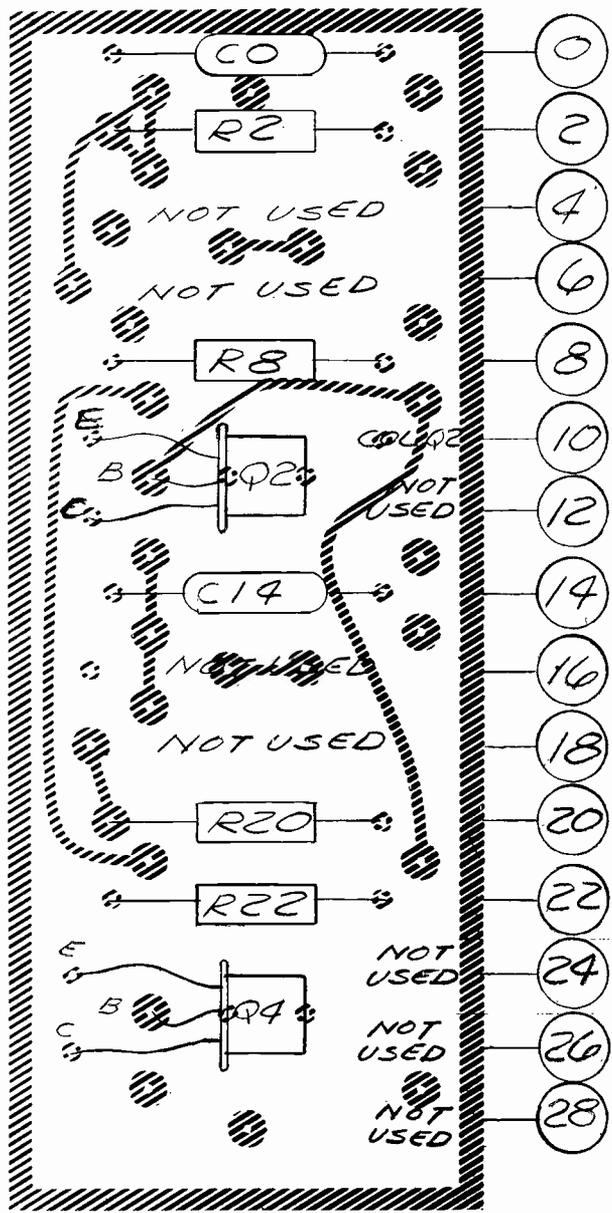
NUMBER OF INPUTS	Q1	Q2
1	R11	R18
2	R11, R9	R18, R20
3	R11, R9, R7	R18, R20, R22
4	R11, R9, R7, R6	R18, R20, R22, R23
5	R11, R9, R7, R6, R5	R18, R20, R22, R23, R24



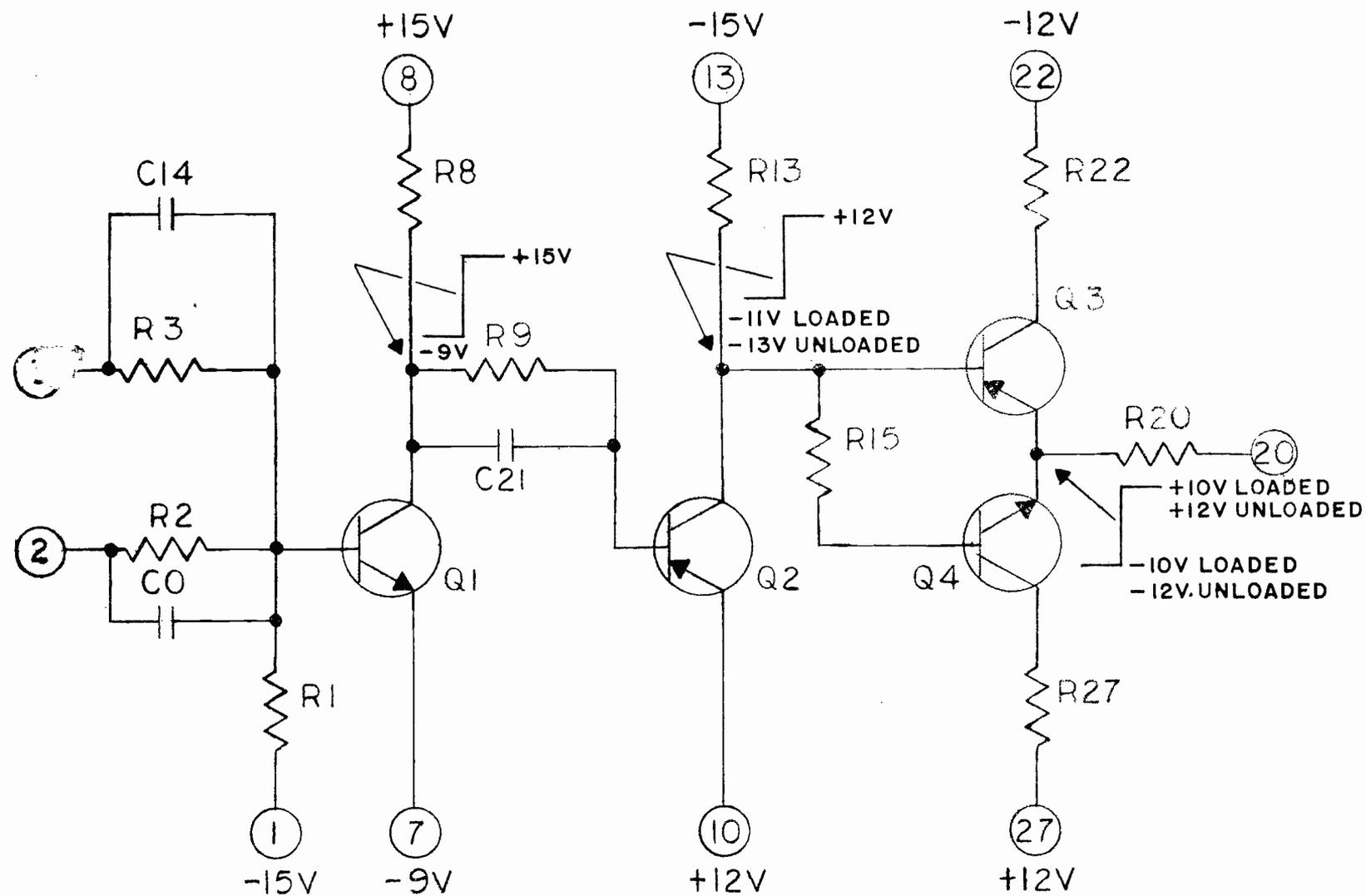
DESIGN VALUES		
PART NUMBER	DESCRIPTION	VALUE
R1	RESISTOR, CARBON, 1/4W, 5%	1800
R9	RESISTOR, CARBON, 1/4W, 5%	120K
R5	RESISTOR, CARBON, 1/4W, 5%	10K
R6	RESISTOR, CARBON, 1/4W, 5%	10K
R7	RESISTOR, CARBON, 1/4W, 5%	10K
R9	RESISTOR, CARBON, 1/4W, 5%	10K
R11	RESISTOR, CARBON, 1/4W, 5%	10K
R18	RESISTOR, CARBON, 1/4W, 5%	10K
R20	RESISTOR, CARBON, 1/4W, 5%	10K
R22	RESISTOR, CARBON, 1/4W, 5%	10K
R23	RESISTOR, CARBON, 1/4W, 5%	10K
R24	RESISTOR, CARBON, 1/4W, 5%	10K
R25	RESISTOR, CARBON, 1/4W, 5%	120K
R28	RESISTOR, CARBON, 1/4W, 5%	1800
Q1	TRANSISTOR	2N404
Q2	TRANSISTOR	2N404

SUBMODULE, TYPE G_b

COMPOSITE LAYOUT

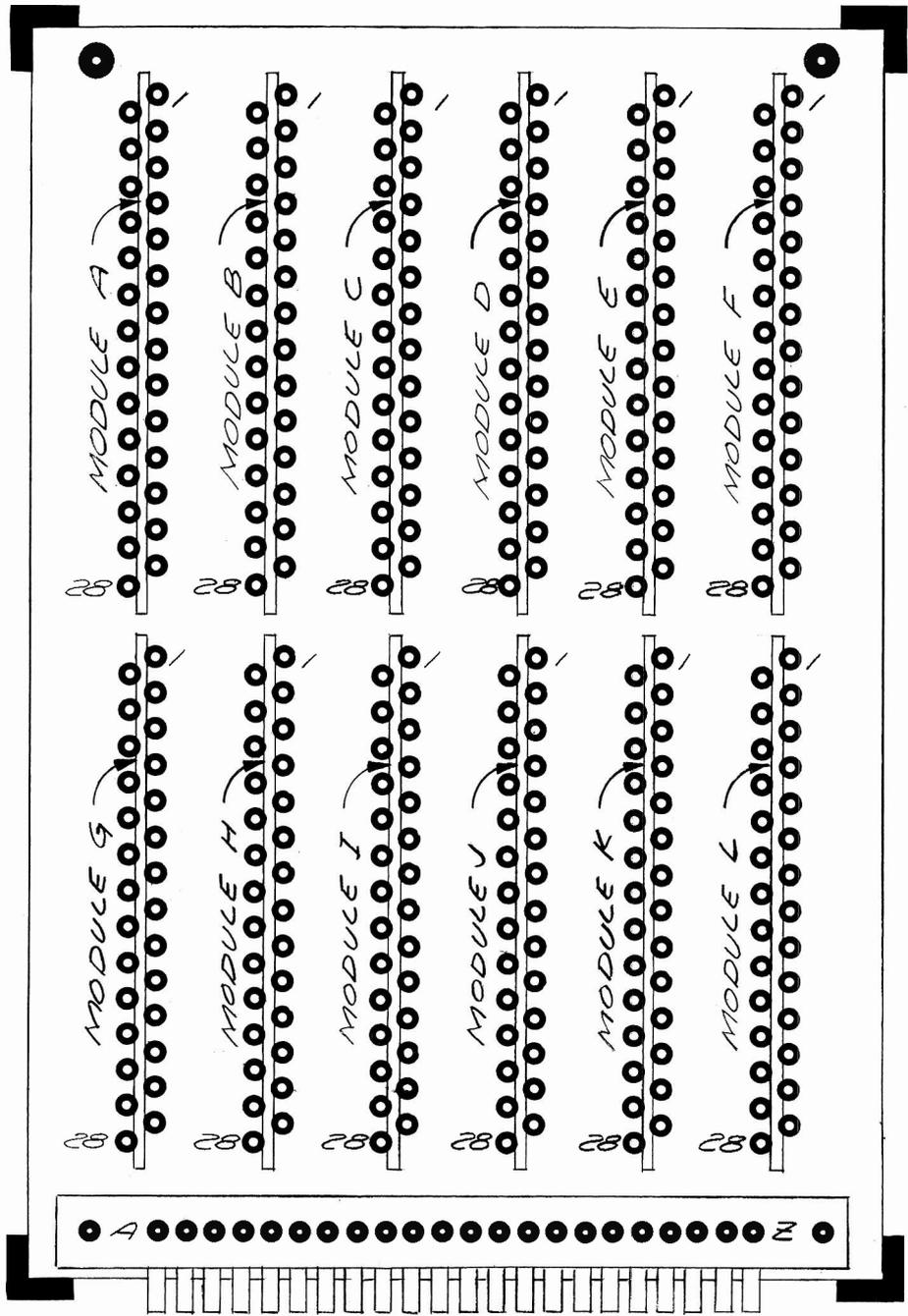


SUBMODULE, TYPE 120-S1
COMPOSITE LAYOUT



DESIGN VALUES		
PART NUMBER	DESCRIPTION	VALUE
R1	RESISTOR, CARBON, 1/4W, 5%	82K
R2	RESISTOR, CARBON, 1/4W, 5%	22K
R3	RESISTOR, CARBON, 1/4W, 5%	22K
R8	RESISTOR, CARBON, 1/4W, 5%	3900
R9	RESISTOR, CARBON, 1/4W, 5%	30K
R13	RESISTOR, CARBON, 1/4W, 5%	3900
R15	RESISTOR, CARBON, 1/4W, 5%	1800
R20	RESISTOR, CARBON, 1/4W, 5%	390
R22	RESISTOR, CARBON, 1/4W, 5%	200
R27	RESISTOR, CARBON, 1/4W, 5%	200
C0	CAPACITOR, DIPPED MICA	150mmf
C14	CAPACITOR, DIPPED MICA	150mmf
C21	CAPACITOR, DIPPED MICA	150mmf
Q1	TRANSISTOR	2N1605
Q2	TRANSISTOR	2N404
Q3	TRANSISTOR	2N404
Q4	TRANSISTOR	2N1605

DT-120
FIGURE 18



SUBMODULE LOCATING DIAGRAM