ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

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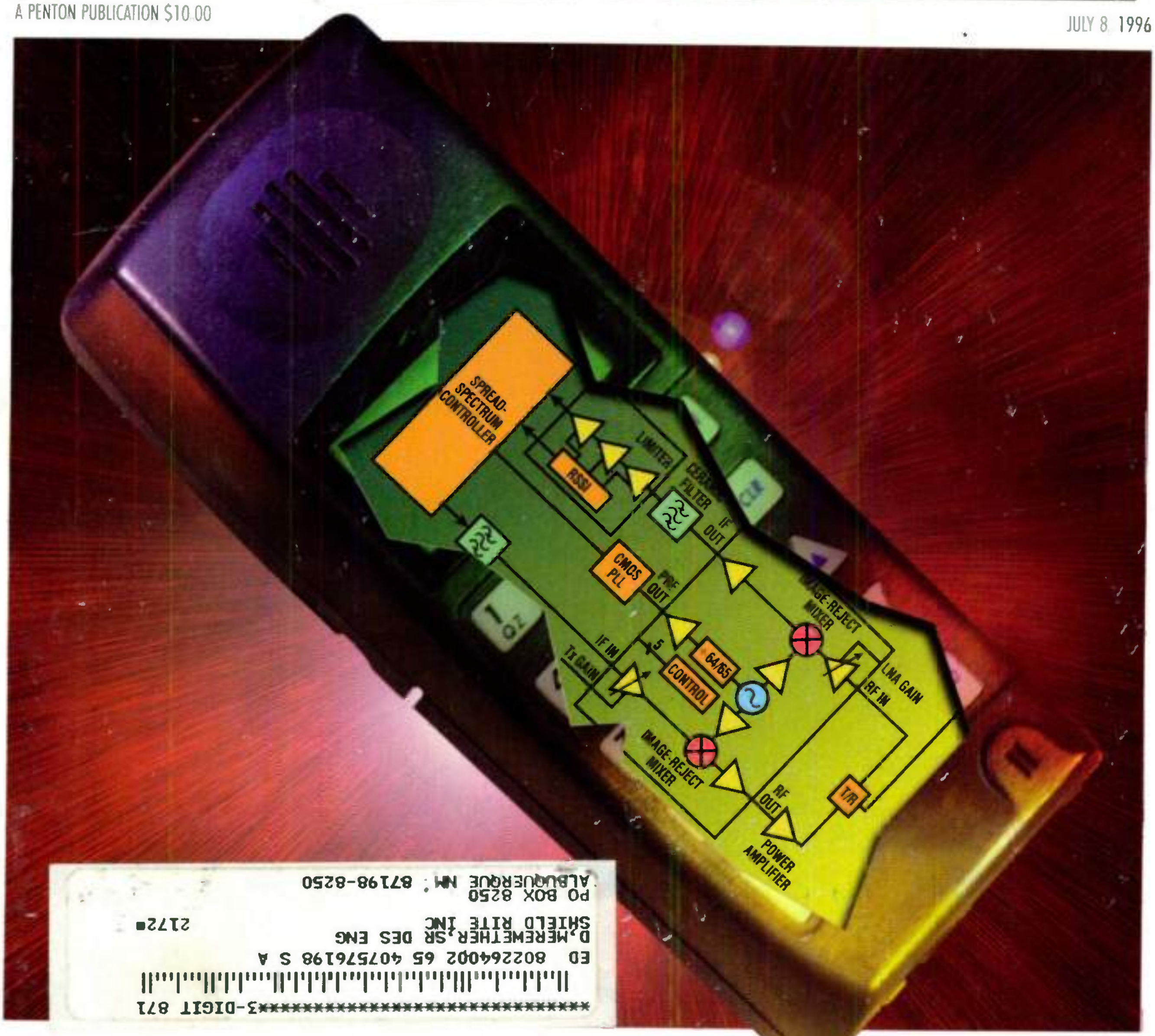
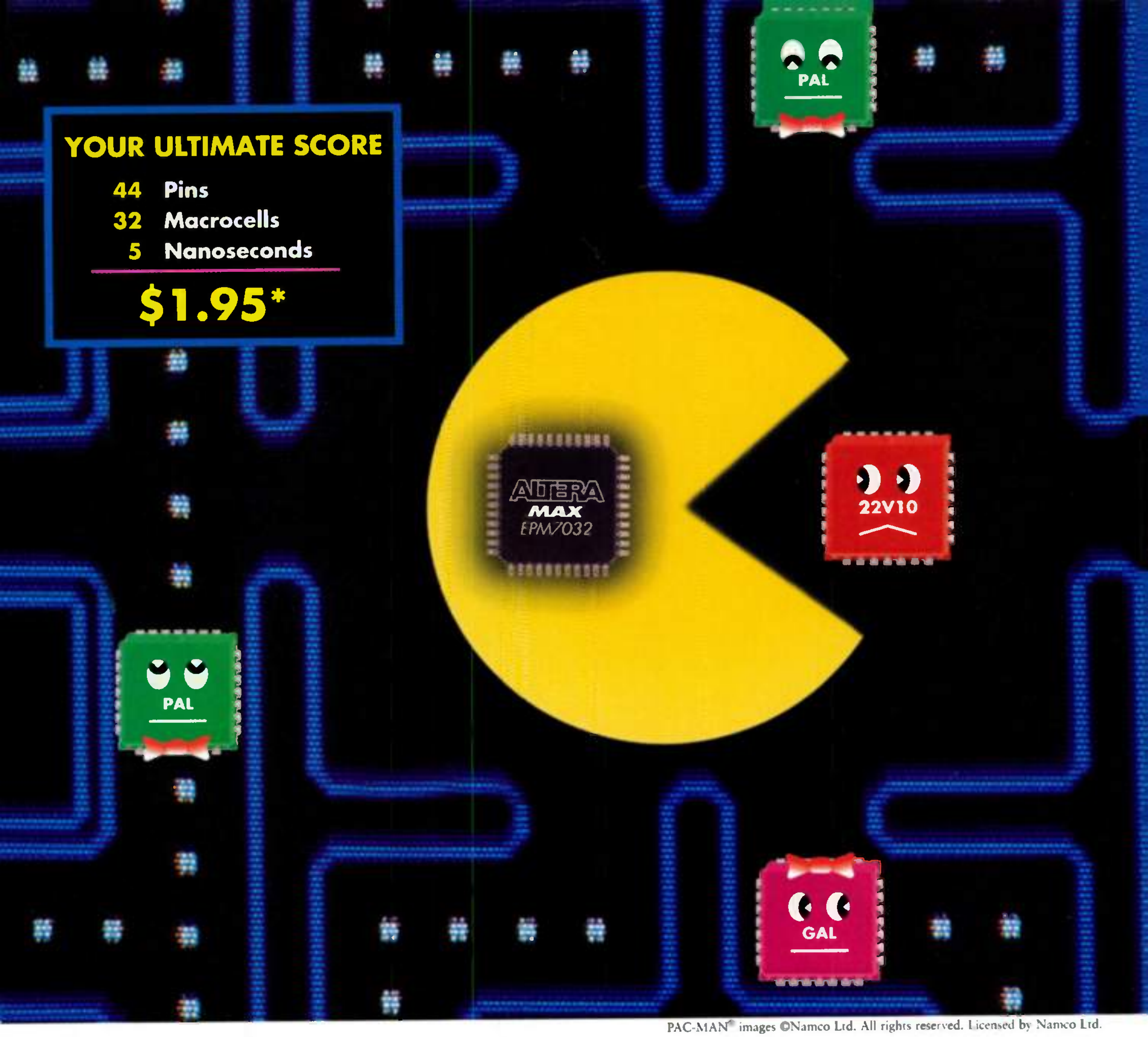


27-GHz Process Produces Low-Power Wireless ICs p. 67



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July 8, 1996 Volume 44, Number 14

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Expanding their technology base by acquisition gives many manufacturers a definite position separation.

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ISA-based board, to be followed by a PCI-based model, simultaneously displays NTSC and SVGA data.

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ELECTRONIC DESIGN

July 8, 1996 Volume 44, Number 14

DEPARTMENTS

Jesse H. Neal Editorial Achievement

Awards: 1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

COVER ART: JOE DRIVAS

ELECTRONIC DESIGN 40 YEARS AGO

Transistors In 1956

Prices have come down. This has meant more and more transistors have been used—3-1/2 million in 1955. Almost 2 million have been sold already in the first quarter of 1956. As transistorized products hit the market, competitors are forced to redesign their equipment, and the demand for transistors rises sharply. Between 10 and 11 million are expected to be sold by transistor manufacturers in 1956, according to industry experts.

From a technical viewpoint, transistors have improved in quality. The current gain of alloy types now holds up for much higher current levels. The spread of characteristics within any one type has been narrowed. Further, several new general classes of transistors based upon application as well as structure have come about. Advances in the art of applied solid state physics such as "grown-diffused" units have been announced but are not yet available commercially.

The work on solid state diffusion and the advances in micro-techniques have been most significant. However, no one technique for producing very high-frequency transistors is ahead as of now. Perhaps this will come in the next year. The most important matter otherwise was the government's antitrust suit resulting in many AT&T patents being made royalty free.

The price of transistors today extends from $0.50 for low-quality units in lots of hundred thousands (for toy use only), through $5 for computer units, and to $50 for new experimental units. The $1 special offered by the jobbers for the amateur is all too often so widespread in its characteristics from one to another as to lead to disgust with transistors. One manufacturer, however, sets and holds reasonable limits and puts them on the specification sheet supplied with the dollar transistor. Most others will probably follow suit this next year.

The long standing demand by radio manufacturers for transistors that approach tubes in cost is being met. Now a radio manufacturer is considering replacing a tube with a transistor on the basis of cost alone. At the beginning of the year some transistorized computer packages were found to be cheaper, all things considered, than the vacuum tube packages that they were replacing.

The current gain of the alloy types has been sustained over longer periods by double emitter doping and other techniques so that power types with a current gain of 60 at 1 to 2 amps are now obtainable. In the smaller deciwatt class, the sustained current gain now gives push-pull class B audio output up to more than 100 mw with less than 5% distortion at any level. In the high frequency p-n-p's the current gain varies as little as between 60 and 80, for example, from tens of microamperes to tens of milliamperes collector current.

A year ago only one manufacturer offered standard units with a maximum current gain spread of as low as 2 to 1. Now it is almost mandatory to keep within that range. The same manufacturer is now offering units with ±20% current gain spread and even some rated at ±10%.

This achievement of closer tolerance units is more superficial rather than real. Production line units are simply divided into groups or types with smaller ranges, though the production spread is always being lowered. The problem is mostly one of designation and stocking of types. *(Electronic Design, July 1, 1956, p. 38)*

This was the lead section of a two-page overview article, written by Norman B. Saunders, Circuit Engineering Consultant, for this issue's annual Transistor Data Chart. The chart itself covered about five pages and listed the basic characteristics of more than 300 transistors from 21 manufacturers, most of whom have long since left the business. How many readers recall such companies as Clevite, Nucleonics Products, Transitron, and National Aircraft Corp. as manufacturers of transistors?—SS


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IEEE Antennas and Propagation Society International Symposium & URSI National Radio Science Meeting, July 21-26. Hyatt Regency, Baltimore, Maryland. Contact Jon A. Moellers, Box 746, MS 55, Baltimore, Maryland 21203; (410) 993-6774; fax (410) 993-7432; e-mail: moellers.i.a@nort.bwi.wec.com.

Sixth USENIX Unix Security Symposium, July 22-25. Fairmont Hotel, San Jose California. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; http://www.usenix.org.

IEEE Power Engineering Society Summer Meeting, July 28-Aug. 1. Radisson Hotel Denver, Denver, CO. Contact Gary Petersen, P.S. Company of Colorado, 5525 E. 38th Ave., Denver, CO 80207; (303) 329-1506.

International Conference on Applications of Photonic Technology Sensing, Signal Processing & Communications (ICAPT 96), July 29-Aug. 1. Montreal, Quebec, Canada. Contact George A. Lampropoulos, A.E.G. Signals Ltd., 1320 Yonge St., Suite 209, Toronto, Ontario M4T 1X2, Canada; (416) 923-4425; fax (415) 923-9129, e-mail: lampro@gpu.utcc.utornonto.ca.

AUGUST

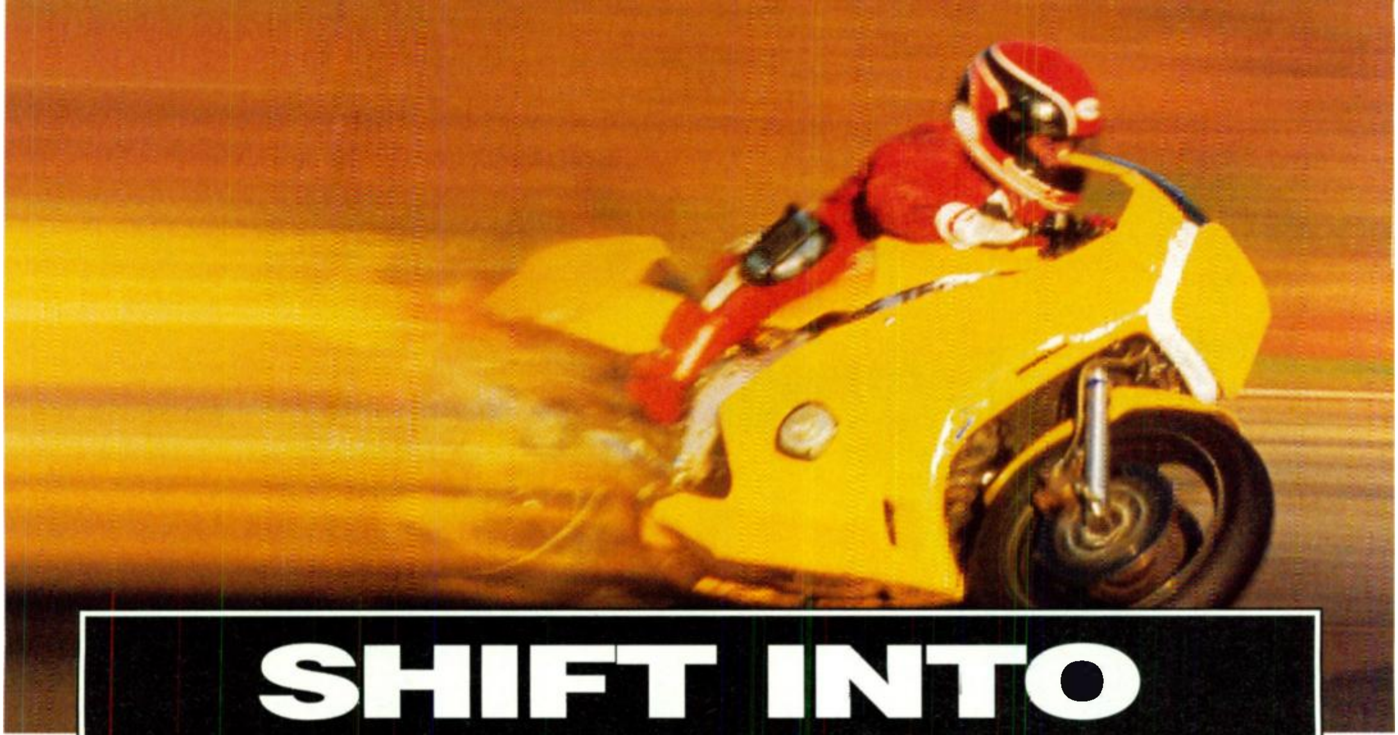
13th International Electronics Industry Testing Equipment & Instrument Exhibition For Asia (EIE Asia 96), Aug. 2-5. Hong Kong Convention & Exhibition Centre. Contact Stephanie Hung, Publicity Officer, (852) 2865 2633 ext. 344; fax (852) 2866 1770/2865 5513.

International Symposium on Low-Power Electronics and Design, Aug. 12-14. Monterey Conference Center, Monterey, CA. Contact Jan Rabaey, Department of EECS, University of California at Berkeley, Cory Hall, Berkeley, CA 94720; (510) 643-8206; e-mail: jan@eecs.berkeley.edu.

IEEE International Workshop on Memory Technology, Design, and Testing, Aug. 13-14. Pan Pacific Hotel, Singapore. Contact IEEE Computer Society Test Technology Technical Committee, 205 Tennyson Ave., Suite C, Altoona, PA 16602.

IEEE International Symposium on Electromagnetic Compatibility (EMC 96), Aug. 19-23. Santa Clara Convention Center, Santa Clara, California. Contact David Hanttula, Silicon Graphics Inc., MS 3U 946, P.O. Box 7311, Mountain View, California 94039; (415) 390-1071; fax (415) 962-9439; e-mail: hanttula@esd.sgi.com.

Eighth IEEE Workshop on Local & Metropolitan Area Networks (LAN/MAN 96), Aug. 25-28. Potsdam, Germany. Contact Daniel Pitt, Hewlett-Packard Labs, 1501 Page Mill Rd., Palo Alto, CA 94304; (415) 857-7096; fax (415) 857-8526; e-mail: pitt@hpl.hp.com.



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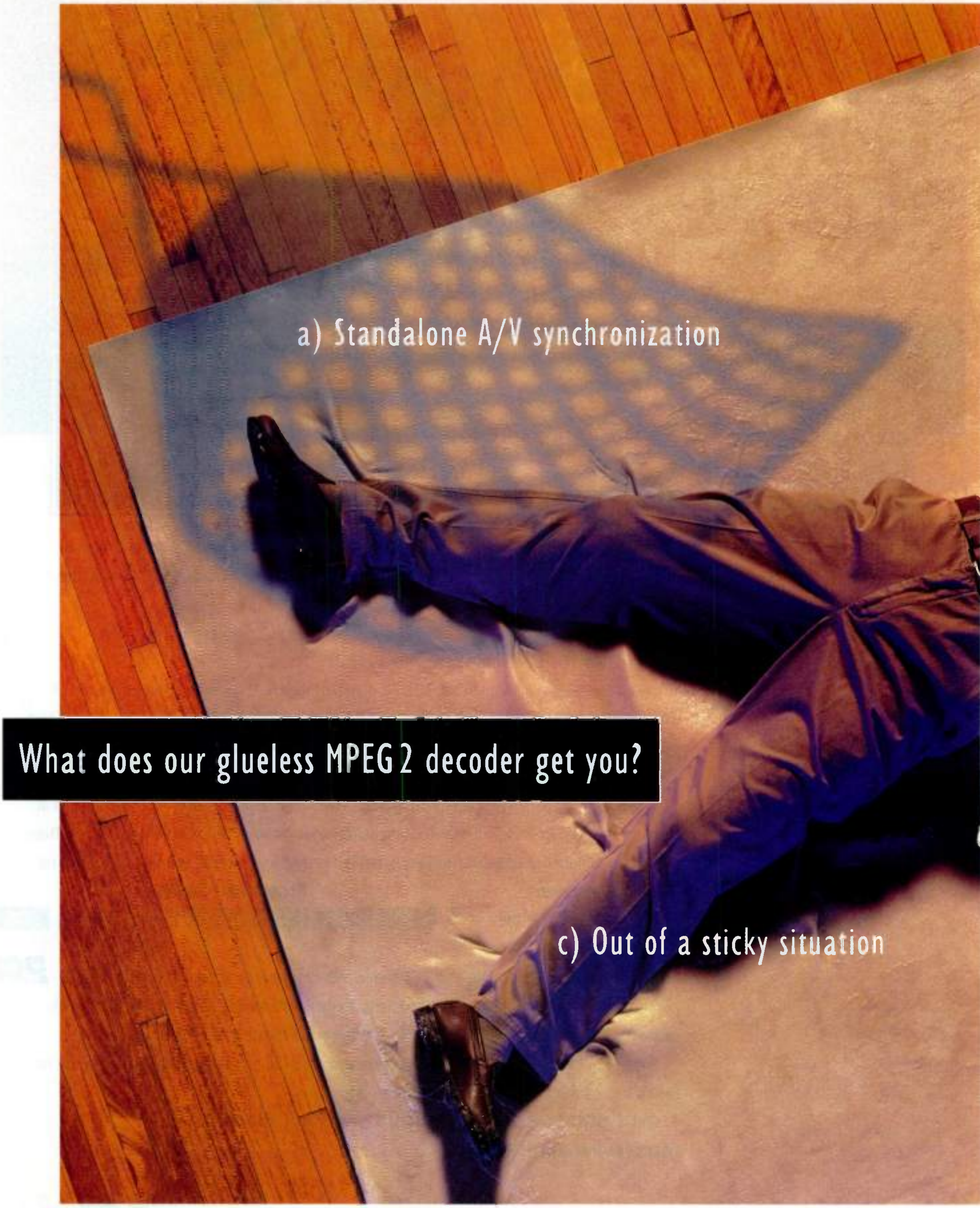
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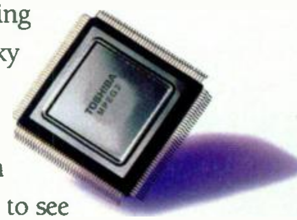

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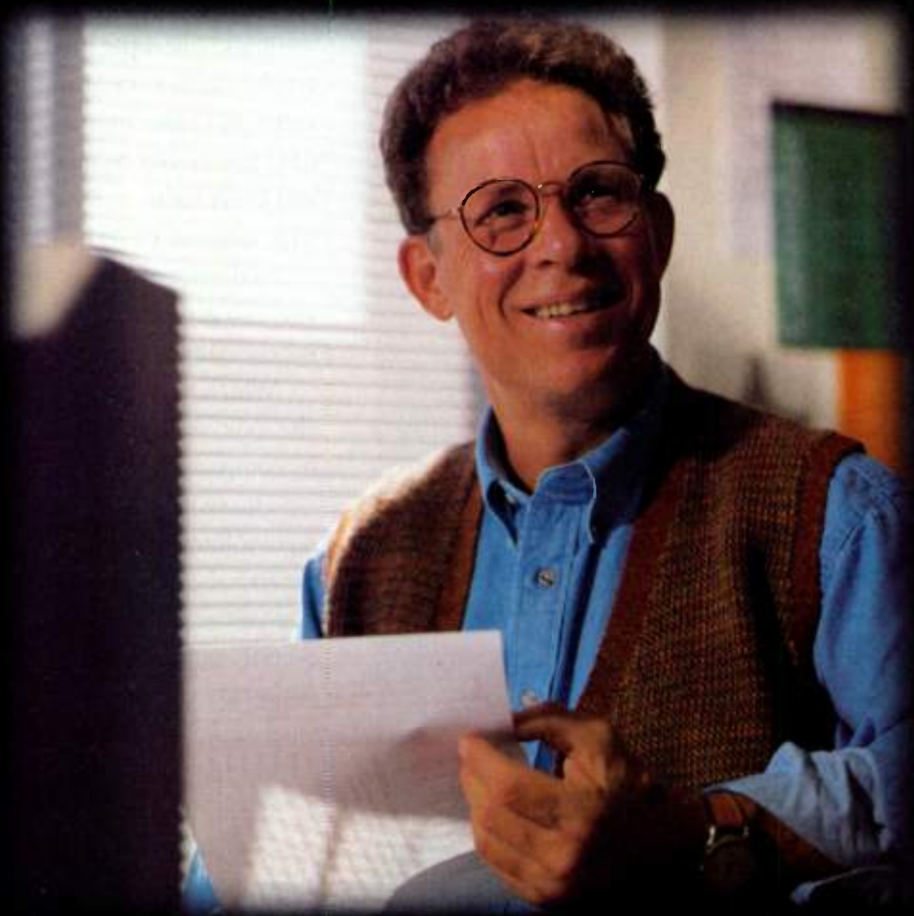

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INSIDE INTEL

Why is Intel Corp. such a great company? There are many reasons, but I have five of my own. The first three are quotes from Co-founder Bob Noyce; Chairman Gordon Moore; and CEO (and personification) Andy Grove.

About 25 years ago, when all of Intel's employees could fit in one room, Bob Noyce said: "Don't be encumbered by past history. Go off and do something wonderful." What soon followed was the first DRAM, the first EPROM, and the first microprocessor (the 4004). Jack Kilby might argue, but I think this could only have happened in California, where technology refugees flourished in a new world of palm trees, endless sun, and unbounded optimism. Noyce had the vision, and they were primed to take him at his word.

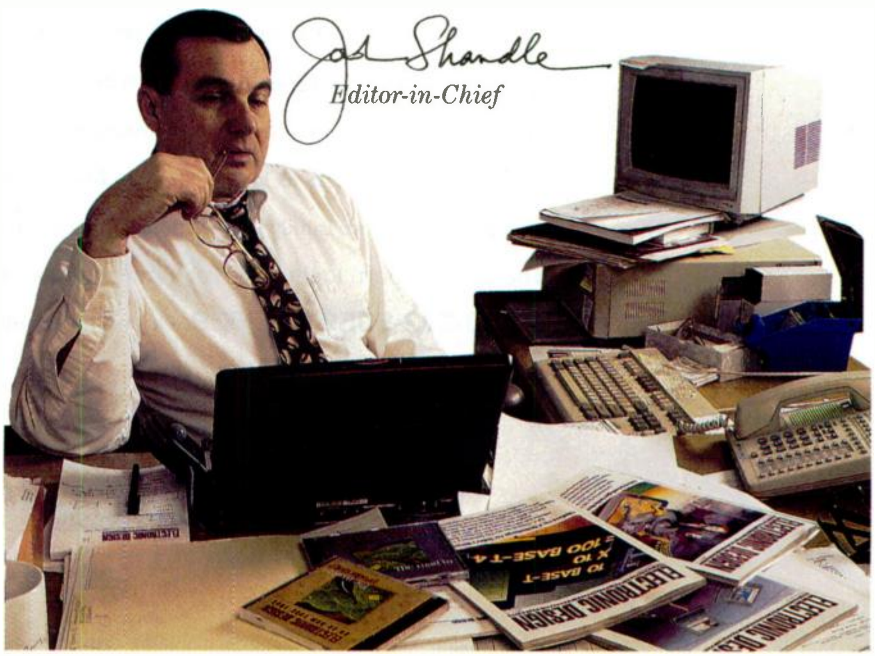
The second quote made Gordon Moore a household name in techno-literate families. "The number of transistors per chip will double every 18 months." There weren't many that believed him. The infant semiconductor industry had no history of sustained growth at that rate. Many "showstoppers" stood in the way. But he was right. Intel is now a $16 billion company and "Moore's Law" is the most elegant verbal expression of a technology road map that I know of.

Andy Grove is famous for: "Only the paranoid survive." I would replace "survive" with "succeed stupendously." (Sorry Andy, *everybody* gets edited at *Electronic Design!*)

Grove's doomsday dogma is the philosophical base for the "Intel Inside" campaign; its move from an LSI company to a microprocessor company in 1981; its transformation into a microcomputer company (PC chip sets, motherboards, etc.); and its next strategic metamorphosis into a communications company of sorts.

Reason #4: They treat their employees well. Intel spent $134 million on training last year; almost $1 billion in profit sharing, bonus and stock options; and a unique sabbatical leave program.

Reason #5: Intel has a powerful propaganda machine. This formidable engine for redefining reality is now focusing on the (admittedly unproven) network-computer concept. Only the paranoid survive, and what would happen to a high-performance microprocessor company if the network really was a computer, and an ARM Ltd. microprocessor was all we needed in our homes? What follows is Intel's quaint (but dangerous) notion of "bandwidth dissonance," which holds that the data pipe into the home will be limited to 28.8 kbits/s for the foreseeable future. More to come on that subject. *jshandle@class.org*



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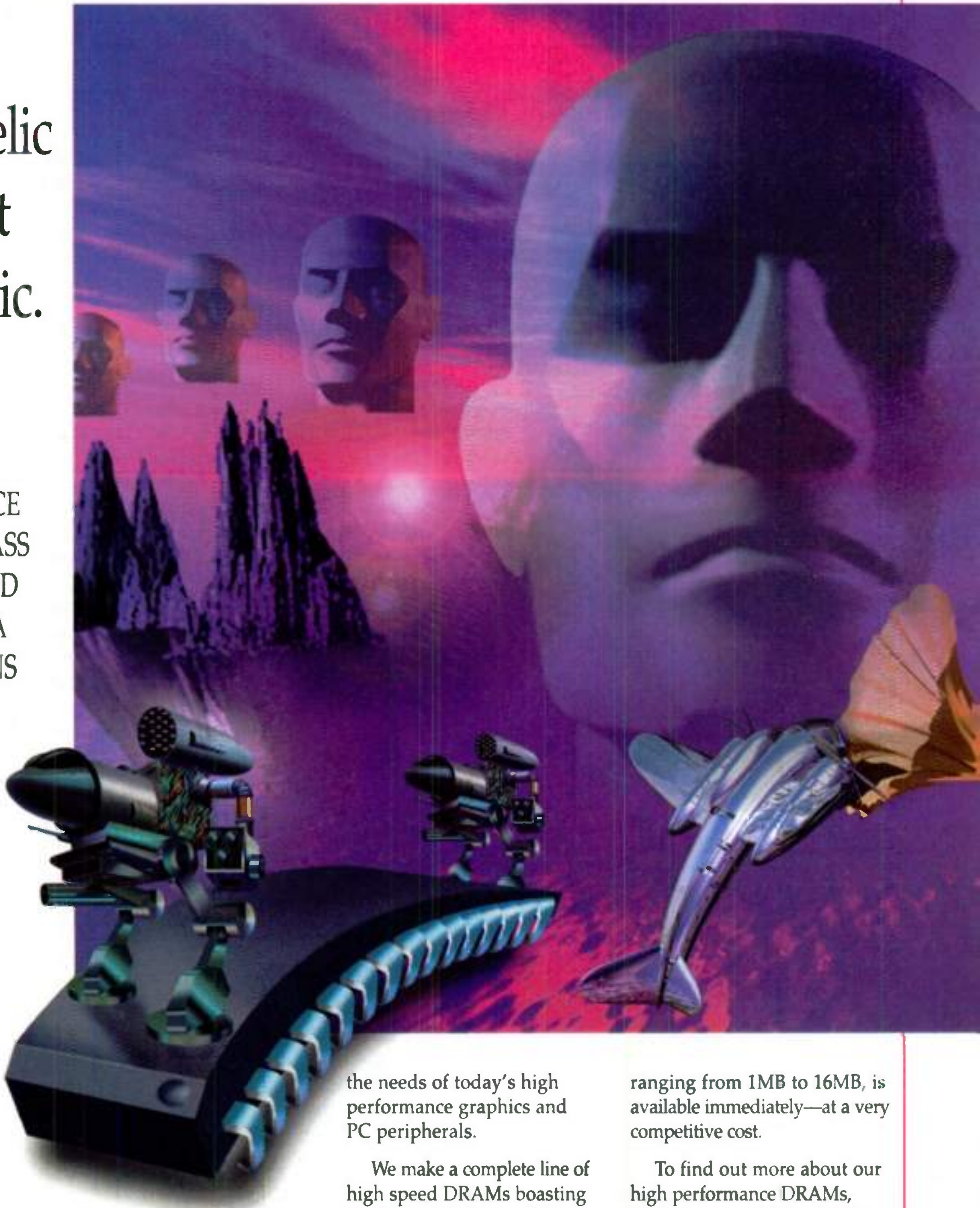

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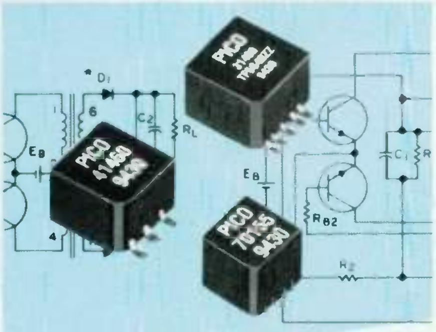

WHO'S RESPONSIBLE?

The semiconductor industry is on the verge of tackling what seems to be an impossible mission. And the acceptance of responsibility is split so many ways that the customer may have nowhere to turn. What's the mission? Basically, it involves providing—on a grand scale—intellectual property in the form of predesigned megacell functions (cores). System designers then could incorporate these cores into ASIC- or FPGA-based designs.

But designers are cautious about incorporating cores they haven't designed themselves because its hard to pinpoint responsibility if the final chips don't perform as expected. If the semiconductor supplier was the lone source of the megacells, it would be relatively easy to blame the supplier should the final circuit not function. However, it's unlikely that one IC manufacturer could provide the wide range of cores needed by designers. That's because that supplier would have to supply a variety of functions to serve such applications as the PCI bus, ATM switching, data communications, and microprocessor-based controllers. A side industry of independent providers of such intellectual property has emerged to fill the void.

DAVE BURSKY
SEMICONDUCTORS

To supplement what the ASIC suppliers deliver, a new class of companies has emerged—small, independent providers of intellectual property that are focusing on delivering complex megacell functions. These functions then are supplied in any of several forms—circuit net lists, HDL description files, full physical circuit designs, and so on. Aside from the issue of guaranteeing the basic functionality of the core, the IP providers must guarantee the performance of the core when it's incorporated into a larger circuit—a huge challenge since the IP providers have little or no control over how their IP will be employed.

However, until recently, these independent IP suppliers—companies such as Logic Innovations, Technical Data Freeway, Virtual Chips, and others, as well as suppliers of synthesis tools like Synopsys and Synplicity, had to compete with the ASIC suppliers to get the customers. Now, the ASIC suppliers, ranging from FPGA manufacturers such as Actel, Altera, and Xilinx to gate-array and ASIC manufacturers like Chip Express, are setting up deals with some of the intellectual-property providers. Through such deals, these suppliers and manufacturers are able to add the core functions to their libraries, thus expanding the range of functions they can offer.

The selection of cores available from these companies is extensive—much more than a single company can create on its own. For example, Virtual Chips offers close to a dozen variants of PCI building blocks, and will shortly have blocks available for the universal serial bus (USB). Technical Data Freeway not only offers PCI blocks, but also provides a vast array of communication and network related functions for applications such as ATM systems and .SONET..

ASIC suppliers have struggled with the issue of intellectual-property rights and responsibilities over the last few years. In fact, until recently, they had opted to simply use their own internally developed cores. But customer demands continue to persist for more variety, as well as the need to get to market quicker by concentrating on value-added expertise rather than on commodity functions. Consequently, this has given ASIC suppliers the incentive to expand their libraries by incorporating third-party-developed cores.

Working with the ASIC/FPGA supplier alleviates some of the questions customers may have regarding who to contact if something doesn't function properly. Rather than go round and round by pointing fingers at the silicon manufacturer, the core provider, or the system designer, the ASIC provider can become the central focal point. This will finally put the designer's mind at ease. Taking responsibility for the total system is the only right thing to do.

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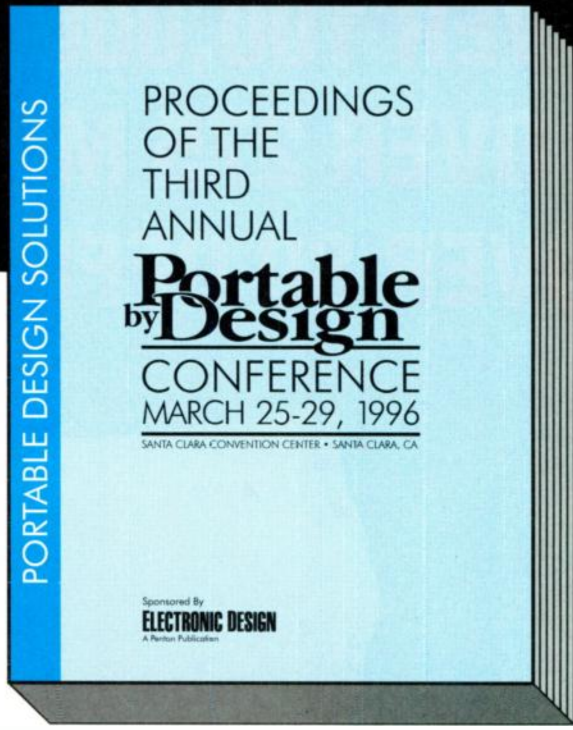

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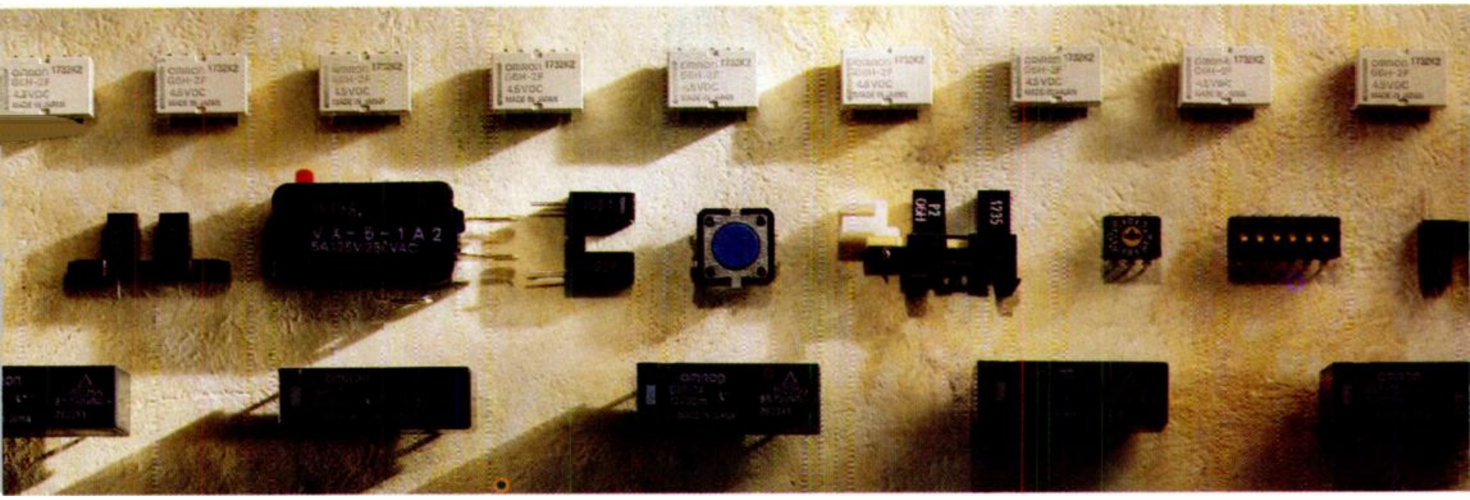

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TECHNOLOGY NEWSLETTER

Capacitance Extractor Uses Nuclear Algorithm

Research done by Dr. Yannick Le Coz at Rensselaer Polytechnic Institute, Troy, N.Y., has resulted in a very fast capacitance extractor used for IC design. The tool implements what are known as floating random walks—an unconventional algorithm that has its origins in the simulation of nuclear-physics interactions. A commercial capacitance extractor called QuickCap, which is based on Dr. Le Coz's theoretical work, is available from Random Logic Corp. QuickCap executes faster and consumes less memory than conventional capacitance extractors. For many IC structures, researchers have observed speed increases of 100 to 1000 times, and memory requirements decreasing by a factor of 30,000. Particularly important is that QuickCap's execution time remains fixed as IC-interconnect complexity increases. QuickCap is also now part of Sematech's Local Interconnect Parasitic Extraction project. For more information, contact Dr. Le Coz at (518) 276-2937 or *ylecoz@cie.unix.rpi.edu*. In addition, Ralph Iverson at Random Logic Corp. is available at (617) 666-1010 or *rbiverson@aol.com*. *LM*

Standard Specifies Generators, Receivers

The Telecommunications Industry Association (TIA), Arlington, Va., has published TIA/EIA-423-B, "Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits," a revision of TIA/EIA-423-A. The standard is meant to specify generators and receivers that can operate at data-signaling rates nominally up to 100 kbits/s. TIA/EIA-423-B designates the electrical characteristics of the unbalanced voltage digital interface circuits, normally implemented in IC technology, that may be employed when specified for the interchange of serial binary signals between Data Terminal Equipment (DTE) and Data-Circuit-Terminating Equipment (DCTE), or in any point-to-point interconnection of serial binary signals between digital equipment. This standard is intended to be referenced by other standards that define the complete DTE/DCTE interface, (i.e., connector, pin assignments, function) for applications where the electrical characteristics of an unbalanced voltage digital interface circuit are required. For a copy of this standard, call Global Engineering Documents at (800) 854-7179. *CM*

Efficiency Improved For Optoelectronics

By tunneling though the energy barriers that prevent the free flow of electrons in semiconductor lasers, researchers at the University of Michigan, Ann Arbor, found a simple way to improve the speed, efficiency, and effectiveness of these devices, which are commonly used in optoelectronic communications systems and industrial applications. The tunneling injection laser developed by a U of M engineering research team improves laser performance by using tunneling to inject electrons through a thin energy barrier directly into the active quantum well.

"Feeding carriers into one of these lasers is like trying to pour water though a narrow funnel," says Pallab K. Bhattacharya, U of M professor of electrical engineering and computer science. "Electrons tend to remain in the wide top of the device where they contribute to adverse effects, instead of falling down into the narrow well where they recombine with holes (positively charged particles) to release their energy as a photon of light." The addition of two thin energy barriers during the growth of the laser crystal creates a tunnel that channels electrons directly into the bottom of the quantum well, making it possible to feed a carrier into the device every 1 or 2 ps—the same time it takes photons to leave the laser.

Because electrons are used more efficiently in the tunneling injection laser, undesirable shifts in wavelengths of light output called "chirps" are reduced. The laser also operates at lower threshold currents, which are less sensitive to ambient temperature, an important feature for industrial applications. Funding for the research was provided by the Advanced Research Projects Agency (ARPA) and the Department of Defense. *CM*

Biological Imaging Developed At Cornell

Investigators of biological systems will now be able to witness fundamental biological processes in living cells—including metabolism, wound healing, behavior of malignant cells, and nerve communication. This breakthrough is the result of microscopy that shows the activity and behavior of living cells under a variety of conditions. Processing of image data from this technique was facilitated by using the IBM SP at the Cornell Theory center, Ithaca, N.Y.

Nonlinear laser microscopy is similar to confocal microscopy in that it has an inherent optical sectioning capability allowing the operator to look at a single plane within a specimen. However, nonlinear laser microscopy has some additional advantages, such as minimal photo damage and a higher signal-to-noise ratio, over nonfocal microscopy.

Walt W. Webb, a Cornell professor of applied physics, notes that the new microscope technology uses pulsed lasers and fluorescent markers to detect and image cellular activity with sensitivity to detect tens of individual molecules in focal volumes on the order of one femtoliter. "We have the ability now to image dynamics of specific molecular distributions and signals in living cells with a sensitivity and diversity that heretofore was unattainable without disruption of life processes," he says. "This gives us a valuable and remarkable tool for a host of biomedical investigations."

Image reconstruction and analysis of a good portion of these optical sections—typically 10 to 50 Mbytes of data—requires a relatively powerful computer system. In collaboration with CTC's Visualization Group, Webb's laboratory has been using the IBM RS/6000 Scalable POWERparallel Systems (SP) and other CTC computers to carry out 3D image reconstruction and quantitative analysis of image data. IBM Visualization Data Explorer software running on an SP node has become their standard system for such work. Two-photon excitation of mitochondrial NADH molecules provides a measure of the metabolic state of cells. Three-photon excitation with red laser light can be used to image the activity of key proteins, particularly those containing the amino acid tryptophan, which usually absorbs only deep ultraviolet light. For more information, call (607) 254-8686 or visit *http://www.tc.cornell.edu/er95/media/* on the World Wide Web. *CM*

OVI Group Evaluates Chip-Scale Reliability

Open Verilog International (OVI) is planning to add analog and mixed-signal extensions to the IEEE Verilog hardware-description-language (HDL) standard. The OVI organization already has a preliminary Verilog-Analog (Verilog-A) standard proposal from a group subcommittee. Verilog-A is important to many high-growth and complex design applications, such as multimedia and wireless communications. It covers the analog semantic extensions for adding analog behavioral descriptions to Verilog. The next release of the proposal, scheduled for December, will be the Verilog-Mixed Signal (Verilog-MS) standard. For more information, contact OVI at (408) 358-9510 or ovi@netcom.com. *LM*

Verilog Standard Will Add Analog Extensions

Cadence recently opened a new design-services organization that will focus exclusively on analog, mixed-signal, and RF design—all key components for the development of communications and multimedia products. The facility, located in Columbia, Md., is part of Cadence's Design Factory network. Its 19-member design team consists of experienced military and aerospace industry veterans with more than 160 total years of experience in analog and mixed-signal design. The operation offers expertise in system design and custom-IC solutions, low-power electronics, and RF electronics. Initially the team will specialize in five critical design areas: telecommunications, networking, wireless, multimedia, and smart power. Already the operation has a contract for a video-graphics-accelerator IC from a major multimedia provider. For more information, call Cadence at (408) 943-1234 or visit their Web page at *http://www.cadence.com*. *LM*

Design Service Group Focuses On Wireless

An extensive research program has been designed to evaluate the reliability of chip-scale packages (CSPs). The program is being conducted by the Swedish Institute of Production Engineering Research, Gothenburg, with assistance from Tessera, San Jose, Calif. The research will focus on the compatibility of CSPs with surface-mount assembly and the field reliability of the finished circuit boards. Until now, there has been a severe lack of available experimental data on the reliability of CSP assemblies. Tessera, which developed and markets the micro ball-grid-array (µBGA) package, will supply test packages, experimental data acquired in its research facilities, and technical assistance. The data Tessera will share with the Institute includes electrical, mechanical, and thermal 3D modeling of the µBGA package, as well as results obtained using finite-element analysis studies. For further information, contact Tessera's Dr. Tom DiStefano at (408) 894-0700 or the Institute's Dr. Bill Brox at 011-46-31-706-6000. Dr. Brox can also be reached via e-mail at *bb@ivf.se*. *DM*

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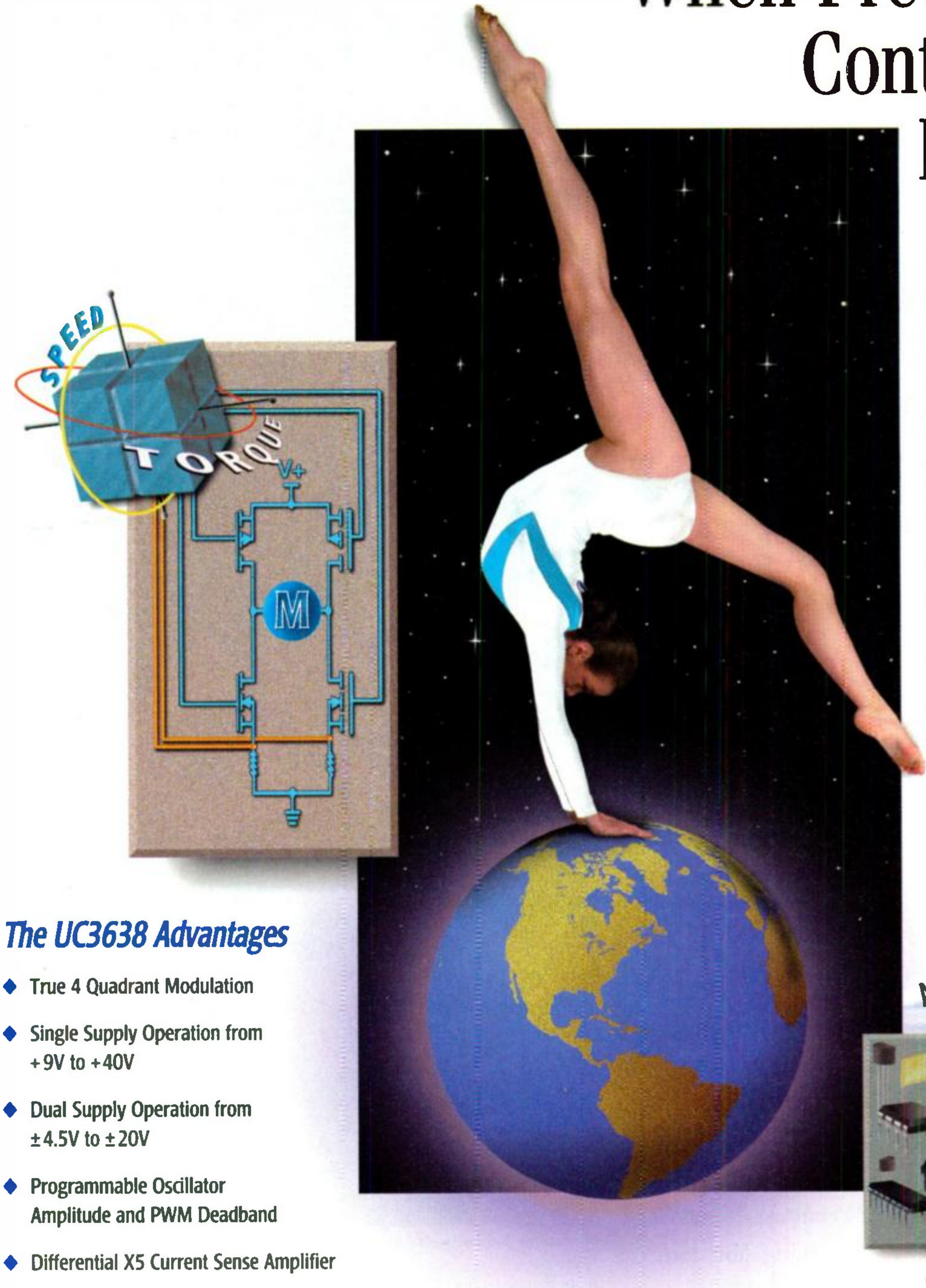

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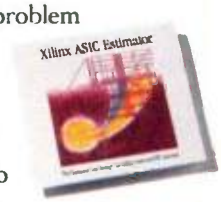

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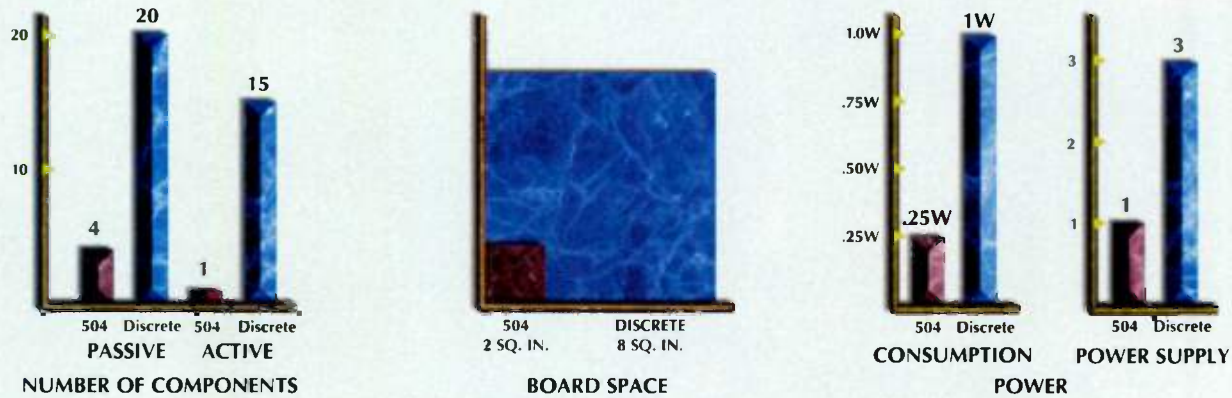

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Simplified Process Is Used To Make Micromachined FET-Like Four-Terminal Microswitches And Microrelays

Silicon micromachining technology has been proposed to make four-terminal microrelay devices, where two of the terminals are used for actuation, while the other two are switched (much like a conventional relay). Such devices are considerably smaller than conventional relays, dissipate much less power, and can be integrated with other devices on the same silicon die. Until now, attempts at producing microelectromechanical relays have fallen short. Devices have had limited lifetimes as well as problems with the quality of the electrical contact.

Researchers at Northeastern University, Boston, Mass., in collaboration with a consortium of automatic test-equipment (ATE) companies spearheaded by Analog Devices, Wilmington, Mass., have now proposed an even smaller and lower-power-dissipating three-terminal microswitch; the micromechanical equivalent of an FET. As a result of their efforts, they have successfully built three- and four-terminal microswitches and microrelays using a simple four/five-mask-set process. Work on the 30-µm-wide by 65-µm-long devices was performed by Northeastern University researchers Sumit Majumder, Greg Jenkins, and Bob McClelland, and professors Paul Zavracky and Nicol McGruer. Analog Devices' Dr. Richard Payne also participated in the project.

The microswitch has been operated for over 10 million cycles before failure. Devices have been successfully switched up to 5 mA. The contact resistance is typically less than 50 mΩ. A breakdown (standoff) voltage of more than 100 V and an off impedance of more than $10^{15}\Omega$ were achieved.

Like a FET, the microswitch consists of a source, gate, and drain, with a beam connected to the source, hanging over the drain *(Fig. 1)*. When a voltage is applied between the gate and source terminals, an electrostatic field is formed between the gate electrode and the beam, pulling the beam toward the gate and substrate and connecting the beam with the drain.

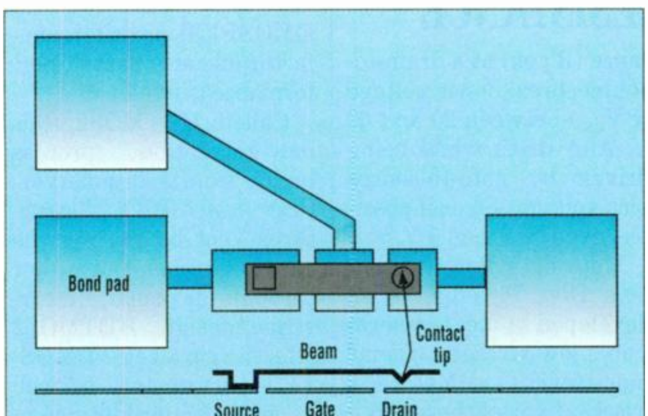

Fig. 1 Three-terminal silicon micromachined microswitch

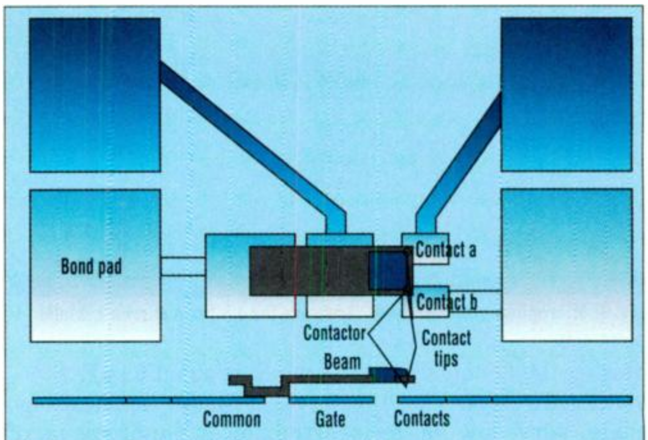

Fig. 2 Four-terminal silicon micromachined microrelay

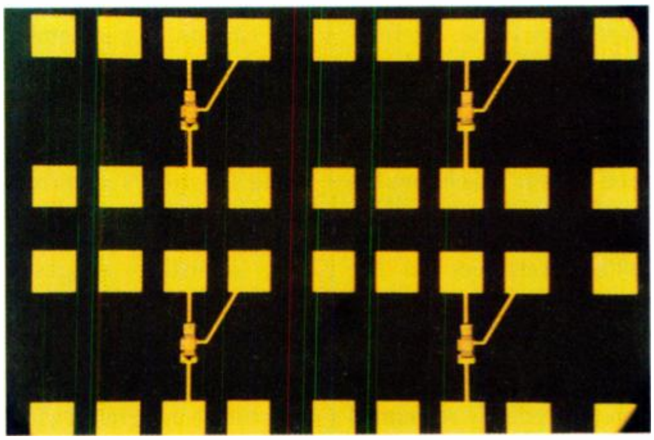

Fig. 3: Microphotograph of silicon die with four 3-terminal micromachined microswitches

A microrelay can be similarly constructed with the exception that the contacting and actuating functions must be isolated. This is achieved by isolating a contacting bar (contactor) from the actuating beam *(Fig. 2)*. When actuated, the contactor shorts two contact electrodes together.

The fact that the microrelay can be fabricated on nearly any insulating substrate makes it ideal for switching microstrip circuits. Different lengths of microstrip can be switched to create a digital phase shifter. And, active or passive elements can be connected for a variety of functions including digital impedance matching. The insertion loss is low because of the microstrip-like configuration and the low contact resistance, and crosstalk is minimized by the low parasitic capacitance of the device.

According to Zavracky, such a device potentially has a much broader operating-temperature range than a conventional silicon FET making it useful for many low- and high-temperature applications. With a sufficiently long lifetime, it can be used for simple electronic logic functions in harsh environments.

Microswitches and microrelays find applications in numerous systems re-

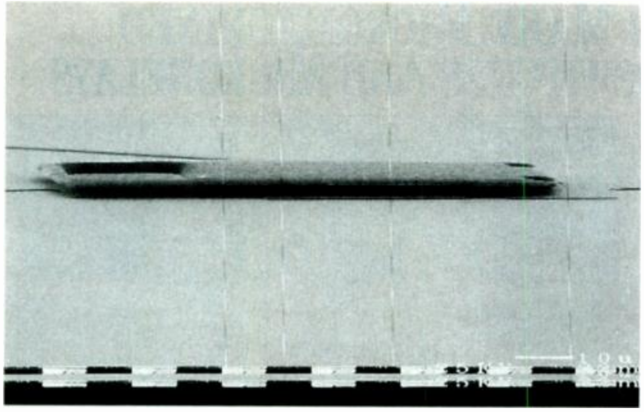

Fig. 4: Microphotograph of beam structure for a silicon micromachined microrelay

quiring the benefits of conventional relays. These include very low on-resistance of less than 50 mΩ and very high off-resistance of more than $10^{15}\Omega$. Microrelays have the obvious advantage of being significantly smaller than conventional devices, including reed relays. This offers the possibility of integrating microrelays with conventional electronics on the same chip.

The devices reported by Northeastern University employ electrostatic actuation. The energy consumed in the process of actuating a microrelay is proportional to the product of the square of the actuation voltage, which is approximately 30 V, and the gate capacitance, which is about 0.1 pF.

For most applications, the power requirements of the relay are insignificant compared to other associated circuits. For example, if the relay were to be operated 1000 times per second, the power consumption would be about 10 µW. While the relays reported by Northeastern University operate at only 150 kHz, modeling suggests that devices operating at up to 10 MHz are possible.

As previously mentioned, semiconductor circuits can be integrated with the microrelay. Microrelays made by Northeastern University occupy an area less than µm on a side. The process used to fabricate the device is compatible with materials used in standard semiconductor processes. Therefore, a wafer with completely processed silicon circuits can be further processed in order to add a microrelay.

Unlike FETs, microrelays do not display charge injection. As a result, voltages can be switched between nodes of a circuit without their values shifting during the switching process. This may provide certain advantages in the creation of analog switching circuits including digital-to-analog and analog-to-digital converters (DACs and ADCs).

In a microrelay, the actuator is isolated from the contactor by an electrical insulator. The only electrical coupling between the two is through the capacitance associated within infringing electric fields. In the devices reported by Northeastern University, the separation between the actuator and the contact is 5 µm, which renders the problem of capacitive coupling insignificant. Measurements of the resistance between the actuator and the contactor were above 10^{12} mΩ at a voltage of 200 V. These characteristics make microrelays a potential replacement for optoisolators.

To make the device, Northeastern University's researchers started by depositing thin layers of chromium on gold on a glass substrate. These layers are photolithographically patterned to form the source, gate, and drain electrodes and the bond-pad interconnections. Next a sacrificial layer is deposited and patterned twice. The first patterning step defines the contact regions. The second step defines the beam base vias. Next, the wafer is patterned to define the beams. These beams are formed from electroplated nickel *(Fig. 3)*.

For the microswitch, the process ends by removing the sacrificial layer and drying the device *(Fig. 4)*. For a microrelay, a fifth mask is needed. An insulating layer is deposited and patterned such that it mechanically connects the contactor to the actuating beam, while at the same time providing electrical isolation.

For further information, contact Paul Zavracky at (617) 373-2919 or Richard Payne at (617) 937-2248.

ROGER ALLAN

PLANAR VERTICAL DMOS PROCESS CUTS POWER-MOSFET SPECIFIC ON-RESISTANCE

Domination is most apropos when describing low-voltage power MOSFETs (vertical DMOSFETs) in today's low-voltage power-control arena. Low-voltage power MOSFETs pervade power-management and switching-regulator applications in both portable and plug-in-the-wall systems, and are finding homes in various battery-charging applications.

Three factors govern power-MOSFET process design: Cost, manufacturability, and the ability to fabricate tiny discrete FETs with the lowest possible on-resistance. That is, the process must be low cost (which implies high-yield manufacturability), and it must use the silicon efficiently.

In addition, the process has to provide inherently a very low specific on-resistance (R_{ds}on) at a drain-to-source breakdown voltage (BV_{dss}) between 20 and 60 V. And that's while being driven by gate-to-source bias voltages of, or if possible, even less than 5 V.

Motorola's Power Products Div., Phoenix, Ariz., developed a next-generation low-voltage planar (non-trench) DMOSFET process to meet these three critical criteria. The new process' prime feature is a lower specific on-resistance, and it's achieved with low-cost processing (if DMOSFETs aren't manufacturable at low cost, performance is irrelevant).

Called HDTMOS2, this new-generation process breaks from traditional vertical MOSFET structures—not by putting the gate in a trench, but rather through a planar, linear-stripe design. HDTMOS2 offers improved DMOSFET performance as well as manufacturability compared with devices coming off today's HDTMOS fabri-

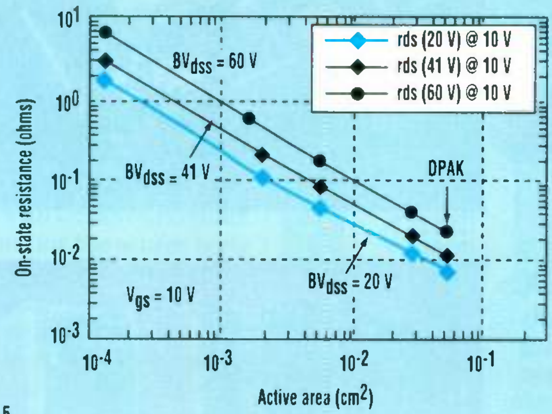

Fig. 5

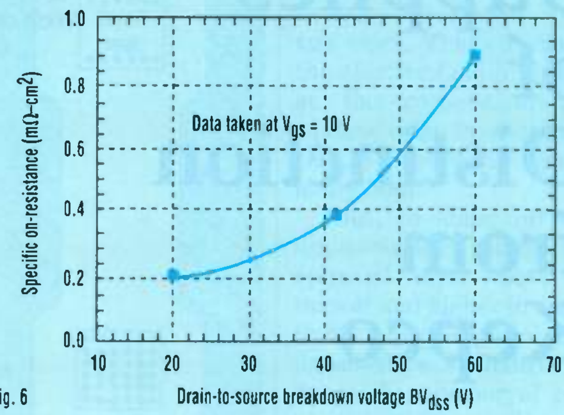

Fig. 6

breakdown or "snap-back." This condition occurs when just one of the MOSFET's million or so cells makes poor contact with the source metal. The source metal heats up and breaks down, and the remainder of the cells catch the disease.

The snap-back issue is improved in the linear-stripe structure because there are multiple contacts to the same p^+ material. Snap-back avoidance is further enhanced because the high-density process produces a greater number of source connections. If one source-contact is poor, one or more nearby contacts handle the job.

A plot of *measured* specific on-resistance versus gate-to-source bias (drive) voltage for a specific FET rated at 41 V illustrates the capability of the new process *(Fig. 3)*. A 10-V drive results in an R_{ds}on of just 0.4 mΩ-cm^2. That's 40% lower than the R_{ds}on of similarly rated FETs from the previous generation of low-R_{ds}on HDTMOS FETs.

The solid line in the figure represents the results of the modeling, which was performed on a computer.

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The modeling also enabled the process designers to determine how the MOSFET structure's different regions contributed to the specific on-resistance *(Fig. 4)*. In this 41-V part, the access region and the drift region (both are parts of the epitaxial region) represent the major portion of the device's on-resistance.

Motorola already characterized several HDTMOS2 devices of varying die sizes and breakdown-voltage ratings *(Fig. 5)*. The on-resistance of three FETs (rated at 20, 41, and 60 V) while operating at a drain-to-source voltage of 10 V is plotted against active chip area on a log-log axis.

Several new HDTMOS2 FETs were packaged and characterized, with the results analyzed and benchmarked against first-generation HDTMOS devices. For instance, the DPAK MTD20N03HDL features a mean breakdown voltage of 43 V and a mean R_{ds}on of 23.5 mΩ at a gate-to-source voltage (V_{gs}) of 10 V and drain current of 10 A. At the same operating points, a similarly rated (41-V) HDTMOS2 FET sports a mean R_{ds}on of a mere 13.5 mΩ. That's just over one-half the on-resistance of present HDTMOS devices.

As is the case with other MOSFETs, users wind up paying dearly for higher breakdown voltages. That's because the on-resistance increases *exponentially* with breakdown voltage *(Fig. 6)*.

To maintain the same on-resistance, therefore, the silicon area also must increase *exponentially* with voltage rating. Increasing the voltage rating of one of these FETs by just 20 V (from 40 to 60 V) doubles the product of R_{ds}on × the silicon area (this characteristic is called the R_{ds}on area product).

The die size is a direct function of the R_{ds}on area product. Thus, as MOSFET voltage ratings climb (for a specific on-resistance and current rating) so does the cost, directly reflecting the required rise in the die size.

Like its predecessor, the HDTMOS2 process is portable (it can be transferred from one fabrication facility to another). It is also CMOS-compatible, further easing fabrication requirements. That is, the new HDTMOS2 FETs can be manufactured on any one of Motorola's many conventional VLSI CMOS fabrication facilities around the world.

Old DRAM fabrication facilities make great power MOS facilities. Moreover, because the HDTMOS2 process and the new device structure are relatively simple, it is easy to add process modules on it (e.g., CMOS) to create higher levels of integration, such as electrostatic-discharge (ESD) protection and/or CMOS control circuitry.

For more information about the Motorola HDTMOS2 process, contact Chris Gass at Motorola's Power Products Div. at (602) 244-4935.

FRANK GOODENOUGH

Innovative Array Architecture Makes Solar Illumination Monitoring Possible

Solar-powered generators, which find use in climate-control equipment among other applications, rely heavily on solar illumination sensors for optimum effectiveness. These sensors are characterized by their ability to measure quantitatively the intensity and direction of an incident light source.

In recent years, these sensor devices have been based on a discrete diode design that allows for the transmission of signals containing location and intensity information.

However, such sensors can't achieve high angular selectivity or measure light intensity independently of the incidence angle. As a result, sensor data must be externally processed to yield the necessary angular and intensity information.

To fill that void, researchers from CSEM SA, Neuchatel, Switzerland, developed a method to eliminate the need for external processing, as well as make it easier to integrate the sensor in a system. CSEM's two-part solution involves a novel analog chip and a dedicated optical front-end. This makes possible the acquisition of azimuth, elevation, and intensity of sunlight as three continuous independent signals.

The analog chip, which is fabricated using a 2-µm, 2-layer metal CMOS process, has a die size of 5.5 by 5.5 mm^2. The chip contains an array of 1365 photosensitive cells, each measuring 95 by 82.5 μm^2.

The cell array is structured as a hexagon, where the cells are interconnected according to a polar reference frame. This frame-of-reference choice makes it possible to reduce a two-dimensional center-of-gravity computation to two one-dimensional center-of-gravity computations, while at the same time maintaining the same coordinate system.

The individual cells in the hexagonal interconnection network are connected to two network lines. One line defines the radial position and the other line defines the angular position.

Each cell is responsible for converting incident light on the photodiode into electrical current, compensating for optical losses and consequently carrying out a series of computations. This occurs when a cell is activated so that its illumination intensity is sufficiently larger than the average illumination intensity received by all the cells at a given instant in time.

As a result, this design requires the presence of a sun spot for the cells to be activated. That's because in its absence, the distribution of illumination on the network matrix would be relatively uniform and no single cell would receive enough illumination to be activated.

Once activated, though, the cell injects a current onto its two position lines, providing data that can be used to compute azimuth, elevation, and illumination intensity.

The second half of the solar-illumination monitoring device is the optical system. This system is composed of a diaphragm that sets the diameter of the sun spot and a hemispherical lens where the spherical part faces the cell array.

The system gives a relatively constant spot diameter, expressed in polar coordinates, for any sun elevation. The position of the light spot on the chip has an angular coordinate that's equal to the azimuth and a radial coordinate that's proportional to sun elevation.

During operation of the solar-illumination monitor, a sun spot is projected onto the cell array from the optical system where it's been concentrated and refracted. When the sun spot hits the optical system, 15 of the 1365 cells are activated.

This number of cells was chosen to ensure that there is a continuous output signal with high precision, since the average effect on more than one cell decreases the sensitivity of the device to mismatch error when compared to that of only one cell.

In addition, if one or more of the cells in the matrix are defective, the output signal won't be impacted significantly.

The current distribution that's generated by the active cells is used to compute the exact position of the sun spot. The intensity of the solar illumination is obtained by summing all of the photocurrents that are produced by the active cells.

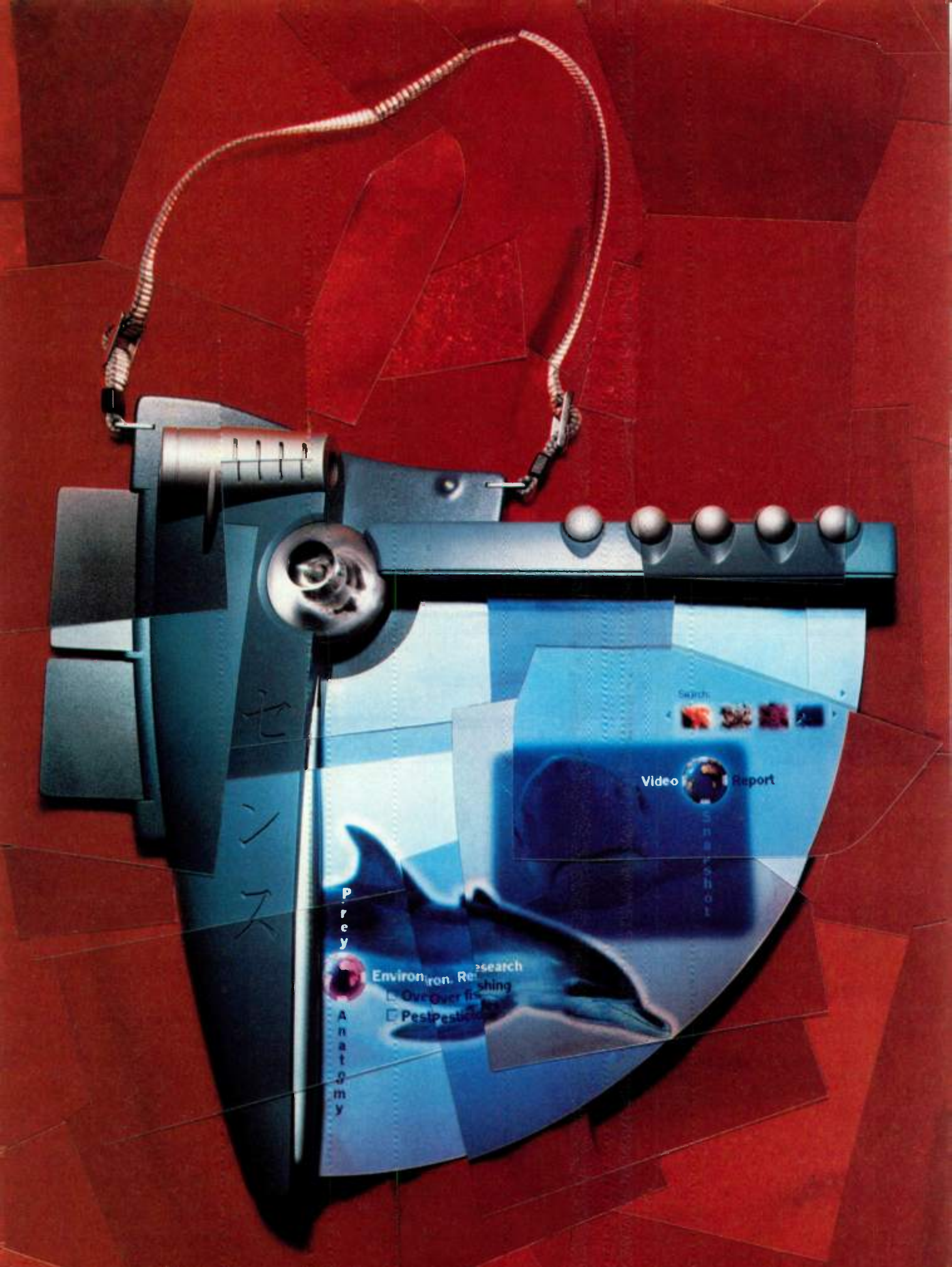
Each individual cell's photocurrent is weighted before summing it with those photocurrents of other cells. The azimuth and elevation then can be deduced from the light-spot's center-of-gravity computations.

One interesting feature of the solar-illumination monitor is its ability to not only detect the presence of a sun spot, but to also point out when the sun isn't visible. This feat is accomplished by checking if the number of active cells and the illumination intensity level are larger than a fixed threshold.

The solar-illumination monitor device operates from a 5-V power supply with a less than 1-ms response time to illumination onset. The system boasts an azimuth range of -120° to $+120^\circ$ and an elevation range of 5° (horizon) to 90° (zenith). Its illumination intensity is 100 to 1300 W/m^2.

For further information about CSEM's solar illumination monitor system, telephone CSEM SA at +41 38 205 111 or fax at +41 38 205 770.

CHERYL AJLUNI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"Compared with a conventional DMOS device, where the gate is formed by a surface deposition of polysilicon, that reduces the current path through the transistor's channel by about one-half," he says. With conventional DMOS structures, there is a significant horizontal component in the conduction path before the gate field takes effect and directs the channel current flow vertically through the silicon bulk material to the drain *(Fig. 2)*. The effect of the trench structure is to eliminate this horizontal conduction component. Hodgskiss estimates that the horizontal and vertical paths in a standard DMOS device are each about 8 µm long.

By eliminating the horizontal path together with increasing the cell density, the specific resistance of the transistor's channel is reduced by about 50%. Hodgskiss adds that another by-product of the structure is that it reduces what he calls the "JFET" effect, which puts a further restriction on current flow through the channel in conventional planar gate transistors.

Hodgskiss points out that simply reducing the physical thickness of the silicon is not an option for transistors that have to withstand applied voltages up to 55 V specified by automobile equipment-makers.

As well as reducing the channel current path, etching of the trench divides the transistor into a series of small cells, each of which generates its own channel through the vertical bulk of the silicon. Since these channels are in parallel, the total resistance is lower than for each individual cell.

Hodgskiss admits that other companies have adopted the cellular approach to keep power transistor on-resistance as low as possible, and he is aware that others are experimenting with the trench process. He claims, however, that Philips has taken a different approach in making the cells in its TrenchMOS process hexagonal rather than square *(Fig. 3)*. That reduces unwanted field effects caused by sharp corners, Hodgskiss asserts. It also allows Philips to get a better ratio of active to non-active silicon area—effectively a greater gross channel cross-section for a given die size.

According to Alun Price, Power MOS product manager, during the present process, TrenchMOS cells can be made down to 11 µm pitches, although he expects this to be reduced to 9 µm by year's end.

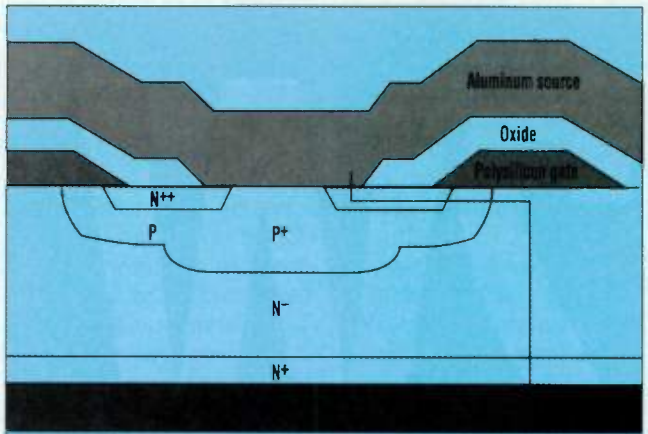

Fig. 2 Conventional DMOS structure

For transistors with a cell pitch of 11 µm, the end result is a drain-to-source on-resistance ($R_{ds}(on)$) of 125 mΩ/mm^2, Price claims. That compares with 270 mΩ/mm^2 for Philips' conventional DMOS process. He adds that moving to a 9-µm cell pitch will reduce $R_{ds}(on)$ still further to around 110 mΩ/mm^2.

One effect of achieving a relatively low specific resistance through the silicon is that it places emphasis on resistance that's external to the bulk silicon—such as the source metallization layer and packaging—which now represents a greater proportion of total device resistance. Hodgskiss says that the resistance of the source metal has been reduced by increasing the thickness of the final aluminum deposition, while packaging resistance has been held low by using thicker bonding wires—350 µm in diameter rather than 250 µm in diameter—and by using three wires instead of two wires. That shaves 1 mΩ off the total. Attention also has been paid to the methods used to attach the die to the drain contact.

The net result is more flexibility in transistor design compared with the older DMOS process. Price says that with TrenchMOS, Philips now has the option of producing transistors with a smaller die size for the same power-handling capability, or reduced power dissipation for a device with the same die size. Price claims that designers can use either approach and gain significant reductions in systems and piece-part costs.

"For example, a lower-power dissipation for the same-sized packaged may mean that a designer may be able to use only one power transistor rather than two in parallel to drive, say an automatic braking system pump,", says Price, "while the second approach, using a smaller die for a given power rating means we can use a package outline suitable for surface mounting and for handling by automatic pick-and-place machines, saving board area and manufacturing costs."

Price adds, "The targets we set for a transistor rated at 55 V and packaged in a standard TO220AB (SOT87) outline include a total on-resistance of 8 mΩ. The best we could get with the DMOS process was 20 mΩ. At 50 A, Ohm's Law says that those 12 mΩ saved

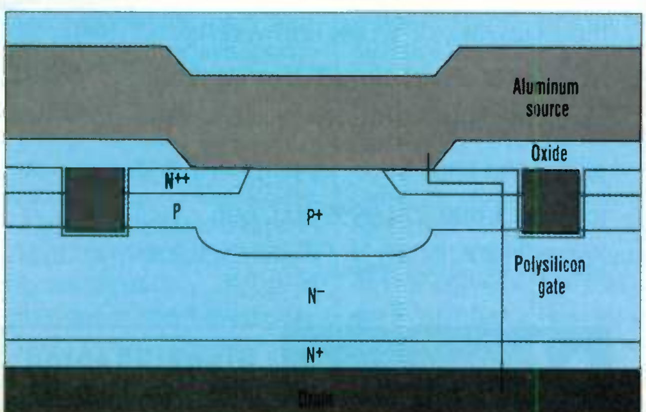

Fig. 1 TrenchMOS cell structure

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LM1972	2-Channel Digitally Controlled Audio Attenuator	4.5V-12V	120dB	.0008%	110dB	Dip (20) SO (20)
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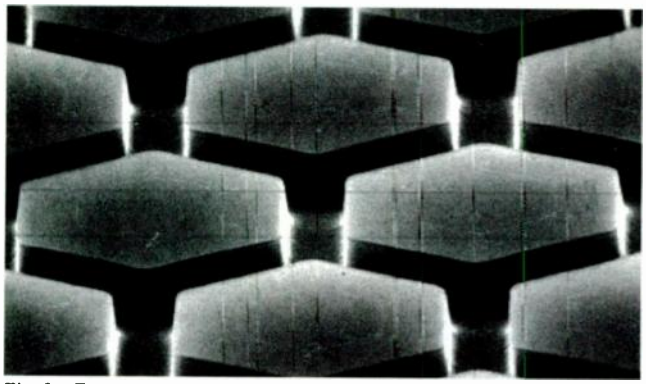

Fig. 3a: Trenches formed in silicon

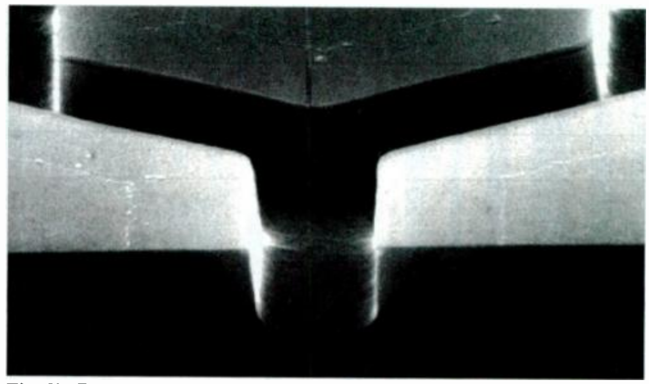

Fig. 3b: Trench before filling with polysilicon

mean 30 W that doesn't have to be dissipated." He adds, "In more representative terms, the TrenchMOS process means that we expect to be able to get a similar performance from a transistor packaged in a SOT223 surface-mount package."

A comparison between a typical standard power MOS transistor from Philips' current catalog and prototype TrenchMOS devices reveals the practical performance gains. Price says that reveals that TO220 transistors with a die size of 20.5 mm^2 showed a typical on-resistance at 25°C of 22 mΩ for the DMOS device and 12 mΩ for the TrenchMOS transistor. That means an increased maximum current rating from 42 to 52 A. In the case of a TrenchMOS transistor with the same on-resistance and maximum current rating, die size can then be reduced to 13.5 mm^2, implying much reduced manufacturing cost.

Space saved by the process also brings another advantage, leaving room for the incorporation of Zener diodes to provide ESD protection for the gate electrode. Price says that ESD gate protection will be incorporated into all devices made with the TrenchMOS process, providing protection against over-voltages of up to 2 kV.

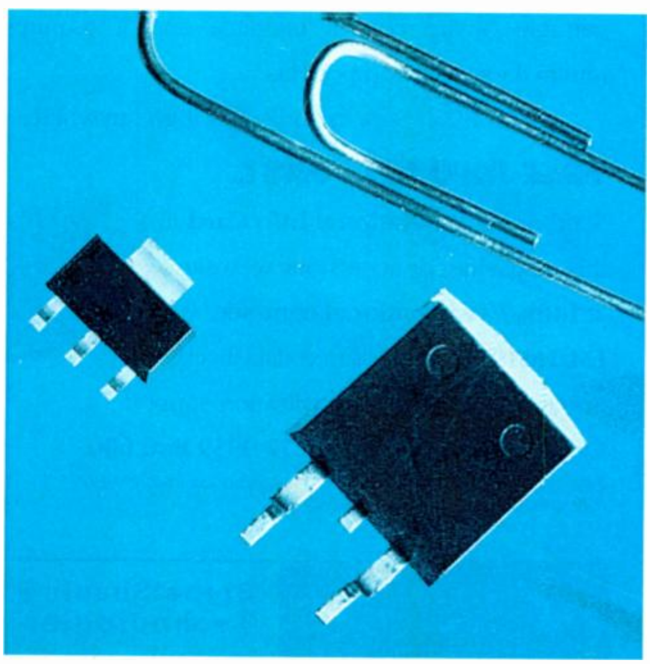

Fig. 4: TrenchMOS power transistor in SOT223 (left) and SOT404 (right)

In the longer term, the new process will impact Philips' range of smart-power devices—Philips brands these "TOP-FETS"—as well as discrete transistors, Price says. He indicates that for a typical TOP-FET device, the chip area is divided roughly equally between logic circuits and the power transistors they control.

"We now plan to shrink the geometries of the logic, using 1- or 0.8-μm processes that we have for the Trench FET process, and use trench to shrink the area of the power device. So overall, we can shrink the size of TOP-FET devices and reduce the cost to a level that the automotive industry is prepared to pay for relay replacement," Price comments.

Transistors made with the TrenchMOS process are scheduled for sampling in the third quarter, with commercial production starting in the fourth quarter. In addition to standard TO220 packages, a new package outline will be introduced for some of the new devices. Price designates this the SOT428, which he describes as a "D-Pack" that in size falls between the SOT223 and the SOT404 surface-mount packages. Philips has already made available in the first quarter of this year the BUK7840-55, a 10-V 40-mΩ transistor in an SOT223 surface-mount package *(Fig. 4, top)*. Philips also plans to launch in the 4th quarter the BUK7608-55, a 10-V 8-mΩ transistor in an SOT404 surface-mount package *(Fig. 4, bottom)*.

Price says that at the outset, a range of 12 55-V-rated transistors will be introduced to the market with on-resistance ranges of 8, 14, and 18 mΩ, with two gate voltage ratings of 10 V (for general-purpose automotive applications) and 5 V (for use in logic circuits), and in two package styles, the TO220AB (SOT78) and the SOT404.

In addition, two devices, one with a 10-V gate voltage and one with a 5-V gate voltage, will be offered in SOT223 subminiature surface-mount packages. These will be rated at 40 mΩ of on-resistance. Prices have yet to be finalized.

For more information, contact Alun Price at Philips Semiconductors Ltd., Bramhall Moor Lane, Hazel Grove, Stockport, Cheshire SK7 5BJ England. Telephone +44 (0) 161 483 0011; Fax +44 (0)161 483 0352.; e-mail ukzajpr@nlevdpsb.snads.philips.nl

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OUTPUT	PushPull	OpenDrain	PushPull	OpenDrain
SUPPLY VOLTAGE	2.7-15V	2.7-15V	2.7-15V	2.7-15V
I_{SUPPLY}	12µA	12µA	7µA	7µA
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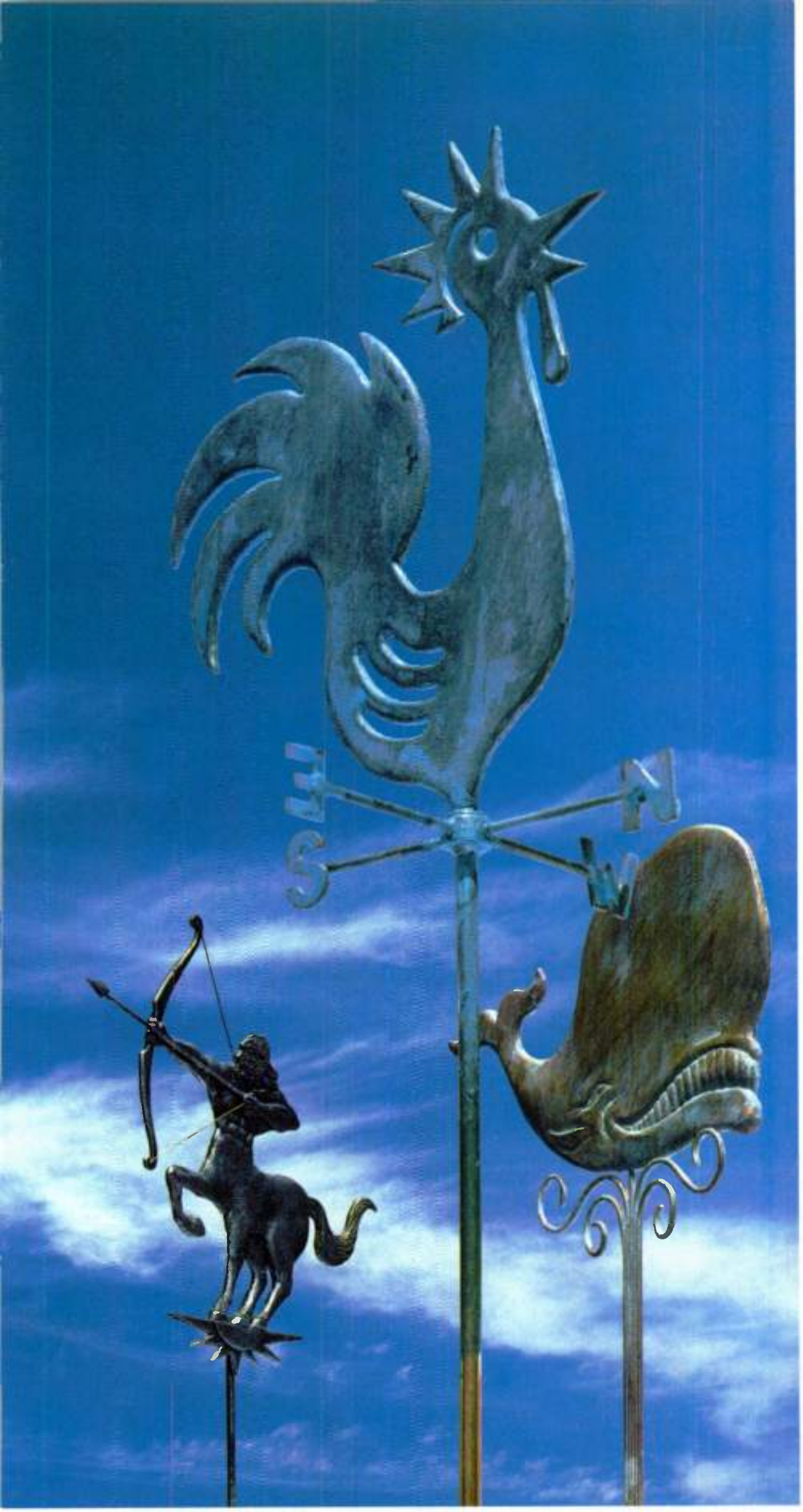

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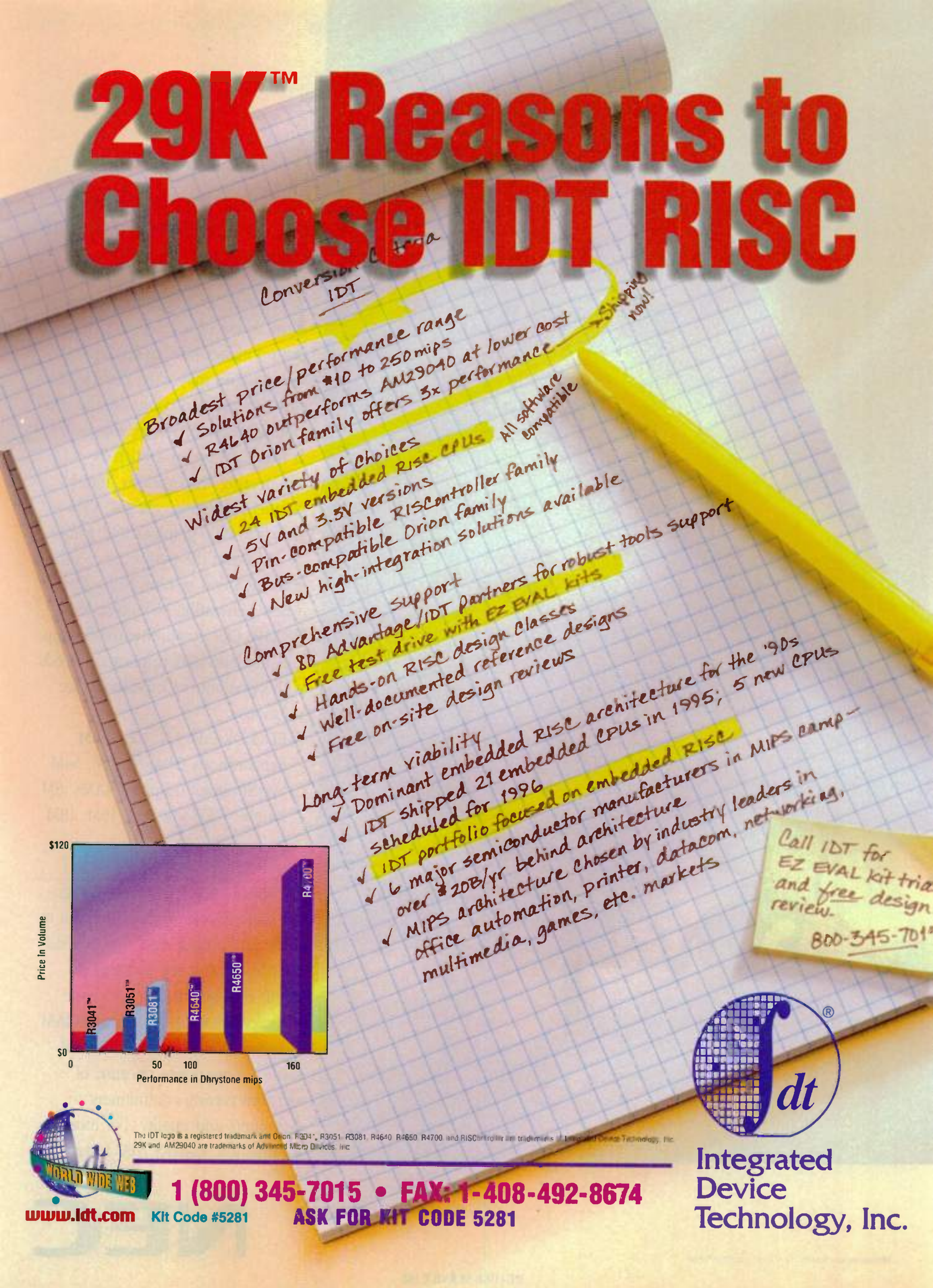

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Machine Vision Moves Into The Mainstream

Higher-Speed, Higher-Resolution, And Advanced Intelligence Join With Performance Standards to Propel Cameras Into The 21st Century.

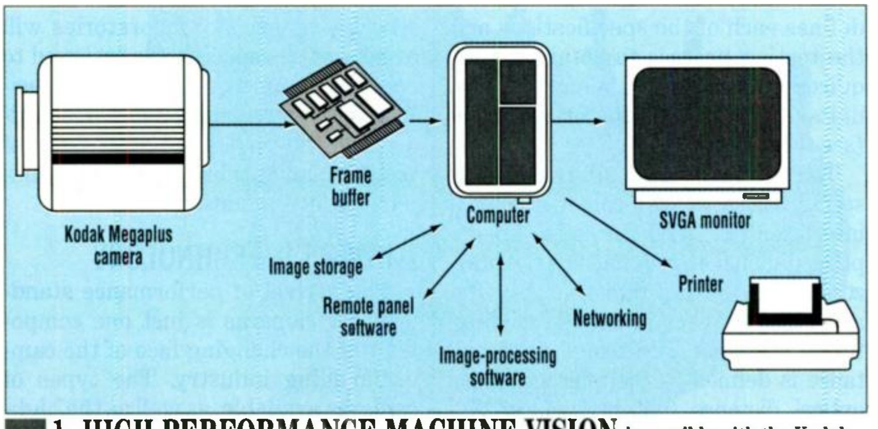
CHERYL AJLUNI

A movement toward standards for video cameras, coupled with performance improvements for cameras, is pushing machine vision into the mainstream. No longer is the camera only an item for consumer use; it also is an indispensable system helping to satisfy a wide variety of imaging needs. Traditionally relegated to the role of a tool, the camera is now evolving to a level of instrument-grade performance. A set of camera performance standards from the American National Standards Institute (ANSI) and the International Standards Organization (ISO) are forthcoming that will define the camera as an imaging device that promises to influence not only the way an engineer collects information, but the quality of that information as well.

In the past, cameras served a singular function as a tool that captures a picture. These devices were readily available and often inexpensive enough that when broken, they could simply be discarded. Yet, as the vision industry changes, so does this stereotype of the camera.

Today, cameras are everywhere. There are different types of cameras at different price levels. They are appealing to consumers and engineers alike, and for some of the same reasons. No longer do end users, especially engineers, want or need a camera that just takes a picture. They're now concerned with getting a quality picture that can be easily manipulated to provide additional information. In effect, the camera is moving toward being used as an actual instrument rather than simply as an enabling tool for capturing an image.

With the growing trend toward higher-speed and higher-resolution devices and the advent of new technologies, the time is right for such a transformation. For example, sensor technology, often employed in cameras, has matured enough to effectively increase camera performance. IC technology has made a previously complicated device cheaper and easier to fabricate.



1. HIGH-PERFORMANCE MACHINE VISION is possible with the Kodak ES 1.0 Megaplus CCD camera system. Its flexibility allows it to be used in a number of applications. The remote-control panel is available from Kodak in a PC version, or in Macintosh or Sun versions from third-party vendors.

PERFORMANCE STANDARDS

Standards have been in place since the dawn of the camera in one form or another. Some were simply company-specific methodologies, while others were borrowed from industry. The broadcast industry, for example, lent its techniques to verify individual characteristics, such as resolution—as reported in the number of TV lines employed. Other characteristics of the camera, such as noise ratio, can be checked by an engineer through the performance of generally accepted up-and-coming camera designs must be radiometrically and spatially accurate devices so they can effectively measure things, instead of just taking a picture. In addition, cameras must exhibit a marked increase in resolution and speed to keep up with the continually more complex applications in which they are used.

In the past, most cameras were used for surveillance and broadcasting type applications, neither of which was dependent on the type of display that was used. These cameras were designed to an RS-170 standard to interface with black-and-white TVs at a fixed speed. This standard, however, has become too inflexible and restrictive to engineers using cameras in machine vision applications. For example, the fixed speed limits the engineer's ability to properly image fast moving objects. Another limitation is a fixed frame rate of 30 frames/s, fixed resolutions of 510 by 492 and 768 by 494 pixels, non-square pixels with an aspect ratio of 4:3, low fill factors which equates to a lower full-well capacity and increased aliasing, small pixels with a low dynamic range, an interlaced frame of two fields of odd and even with a 16-ms delay between fields, and predominantly analog outputs. Most engineers want cameras that produce digital outputs, faster framing, higher resolution, and better image quality to meet the needs of more demanding algorithms.

As a result, a megaresolution CCD camera has been developed by Eastman Kodak that has (at least) a 1-million-pixel sensor array. The Megaplus CCD model ES 1.0 can capture 30 images per second using a specially-developed digital imaging technology, with a spatial frequency of over 1 million pixels *(Fig. 1)*. The technology calls on an electronic imager to digitally capture an image. Designed to be integrated into an image-processing system, the camera allows for precise and convenient computer control of image exposure and capture timing. An accumulation mode significantly reduces the sensors' dark current, making the images ideal for computer enhancement, manipulation, and analysis.

At the heart of the monochrome camera is a CCD interline-transfer-architecture sensor which has an array of 1008 (horizontal) by 1018 (vertical) pixels with a progressive-scan readout system. Each pixel measures 9 μm^2 on

TV CAMERA STANDARDS

Camera performance measurement	Units	Definition
Responsivity	Volts/watt/cm^2/second	Derivative of the GTF with respect to illuminationirradiance (dy/dx of GTF).
Minimum illumination/irradiance Minimum luminous/radiant exposure	Watts/cm^2/second	The illumination or irradiance level required to produce a mean video level output equal to the RMS random noise in complete darkness.
Spectral responsivity	Volts/watt/cm^2/second	A two-dimensional discrete function describing the relationship between a camera's responsivity and the spectral band of irradiance.
Equivalent ISO speed	Lux-seconds or lux with a known exposure time	An adaption of the saturation-based equivalent ISO speed standard. Computed using the measured GTF and responsivity—78/H_{sat}, where H_{sat} equals the focal-plane expsoure for maximum valid camera output.
Dynamic range	dBs	A ratio based on values computed from two select X-axis coordinates on the PTF curve.
Luminous signal/noise ratio	dBs	A ratio based on values computed from the Y- and X-axis values from a select X-axis coordinate on the PTF curve.
Dark-field nonuniformity	%RMS (root-mean-square)	The ratio between the standard deviation of the nonuniformity at a select X-axis coordinate of the PTF and the X-axis value of a second X-axis coordinate. The nonuniformity is an additional measurement result extracted during measurement of the PTF.
Photoresponse nonuniformity	%RMS	The ratio between the standard deviation of the nonuniformity and the X-axis value at a select X-axis coordinate on the PTF. The nonuniformity is an additional measurement result extracted during measurement of the PTF.
Gamma ratio	Ratio	The slope of the best-fit line to a log-transformed GTF for a specified range of X-axis values.
Nonlinearity	%integral	The quantitative measure of departure from the device's theoretical GTF, which may be linear, logarithmic, or other vendor-specified function. %integral equals the ratio between the sum of all Y-axis departures on the transformed GTF and the X-axis value at a select X-axis coordinate.
Limiting resolution	Cycles/mm	A select X-axis coordinate value of the MTF.

GTF (gamma-transfer function)—a two-dimensional discrete function describing the relationship between a camera's mean signal output and the illuminance/irradiance or luminous/radiant energy projected into the camera. MTF (modulation transfer function)—a two-dimensional discrete function describing the relationship between the frequency of a sine-wave pattern projected into the camera and the %modulation of the camera's signal output. PTF (photon transfer function)—a two-dimenstional discrete function describing the relationship between the mean and the variance of the random component of the camera's signal output.

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9-μm centers with a 60% fill factor using a microlens. The camera outputs 8-bit digital images with 256 levels of gray. Integral to the camera's design is the inclusion of internal image-enhancement circuitry which guarantees the uniformity of the captured image.

That feature is important to engineers working on demanding applications with stringent uniformity requirements for data-analysis purposes. The camera includes a built-in electronic shutter, which is vital in assuring its performance level when imaging fast-moving objects, and is characterized by an exposure times as short as 100 μs. A special triggered double-exposure mode is also available, capturing two images separated by a user-controlled delay ranging from 1 to 400 μs. The camera offers single- and continuous-frame modes, giving the engineer greater flexibility in system applications.

Other features include dual 20-MHz channels with proprietary balancing circuitry for output, gain control of 0, 6, and 12 dB, multi-camera synchronization, a spectral response in the visible region (high) and near-infrared (low), and full computer control via serial, RS232 or RS422 connectors. The camera also has digital cabling, a remote-control panel, and an optional clear or infrared filter.

Another example of an intelligent camera is one that EG&G Reticon, Sunnyvale, Calif., developed. Its digital line-scan camera incorporates a number of key features which include an on-board processor, digital architecture and a pinned photodiode detector which has a good blue-light response and can read out at over 40 MHz. The processor, the Intel 80C51, sets all of the required voltages in the camera, monitors its health, sets the user configuration, and communicates with the outside world via an RS-232 port at 9600 baud. Running on its own oscillator, the processor's baud rate is independent of the line rate and the clock rate.

The camera's digital architecture enables it to perform functions which have traditionally been handled in the analog domain, and eliminates many inadequacies associated with earlier analog cameras. For example, channel-to-channel balancing of a multi-tap sensor has always been a challenging problem. But since the digital architecture utilizes the complete signal path in any real-time corrections (by the inclusion of a microprocessor and a digital feedback loop), the problem is virtually eliminated. The microprocessor and feedback path also allow the gain and offset variables to be adjusted in the analog domain, based on actual video data. And, because the algorithms stored in the microprocessor are more advanced than the simple analog loops they replace, the camera offers higher performance.

Integral to the camera's design is a dedicated analog front end which utilizes many of the traditional approaches of a video chain *(Fig. 2)*. During its operation, the two outputs from the sensor are buffered, ac-coupled, and line-clamped to ground to set the dc level. Each of the stable dc-video signals are then fed into separate selectable gain stages. The output from each stage is then passed to the offset control and into a 10-bit analog-to-digital converter (ADC) stage. Digital data from the camera is output via RS-422 drivers in either a two- or single-channel multiplexed, raster-order format. The algorithms in the microprocessor make the gain and offset variable adjustments based on the video data at the output of the camera.

According to Reticon researchers Mark Kelley and Chris Raanes, "The advantage of the processor and RS-232 serial port is the ability to perform noninvasive adjustments to internal settings. Most operating biases are set via digital-to-analog converters (DACs) that can be accessed over the RS-232 control line. Among the accessible variables are a 1x and a 2x analog gain switch, a global-offset level, channel balancing offsets, and an analog gain value per tap. The on-board processor has flash memory to store a user-defined configuration. Once the user has programmed the camera to the desired setting, the RS-232 cable can be permanently disconnected."

Special features of the device include the ability to background subtract in the analog domain, using the RS-232 control to adjust the global offset variable, and the ability to control the operating conditions of the camera based on actual processed camera data. In the latter case, the engineer can override the camera's internal balance algorithms, putting in its place code which has been written on the image processor and fed back into the camera circuitry.

EG&G Reticon's digital line-scan 4096-element LD2040 is the first in a planned family of cameras. Further development of the digital line-scan technology will focus on the achievement of resolutions from 512 pixels to 8000 pixels and higher, and pixel rates to 40 MHz per tap and above.

DALSA Inc., Ontario, Canada, also is developing advanced camera and image capturing technology for the future. The company offers a variable-scan technology format employed in a number of its camera designs that are specifically designed for machine vision and imaging applications. It has square pixels with a 1:1 aspect ratio, sensors with a 100% fill factor, continuous scanning so that no image information is lost, and is flexible over a wide range of speed frame/line rates.

Dalsa believes that cameras that use a variable-scan format can be "ideal" devices that offer increased flexibility of design, and multiple taps for increased throughput. Such cameras would effectively offer a 100% fill factor that reduces aliasing, square pixels with isotropic image transforms, 8-, 10-, and 12-bit digital outputs, higher resolutions, superior noise performance, larger pixels which translate into a higher dynamic range, higher speeds of up to 50-MHz data rates, faster frame rates of 60+ frames/s for 512-by-512-pixel and lower formats and 30+ frames/s for 1024-by-1024-pixel and higher formats, and single outputs for a simpler interface. The aforementioned companies are just a few of the many camera manufacturers working on improving machine-vision technology. Together with improved standards, cameras of the future will evolve from being a basic tool to a workable instrument-grade type device. □

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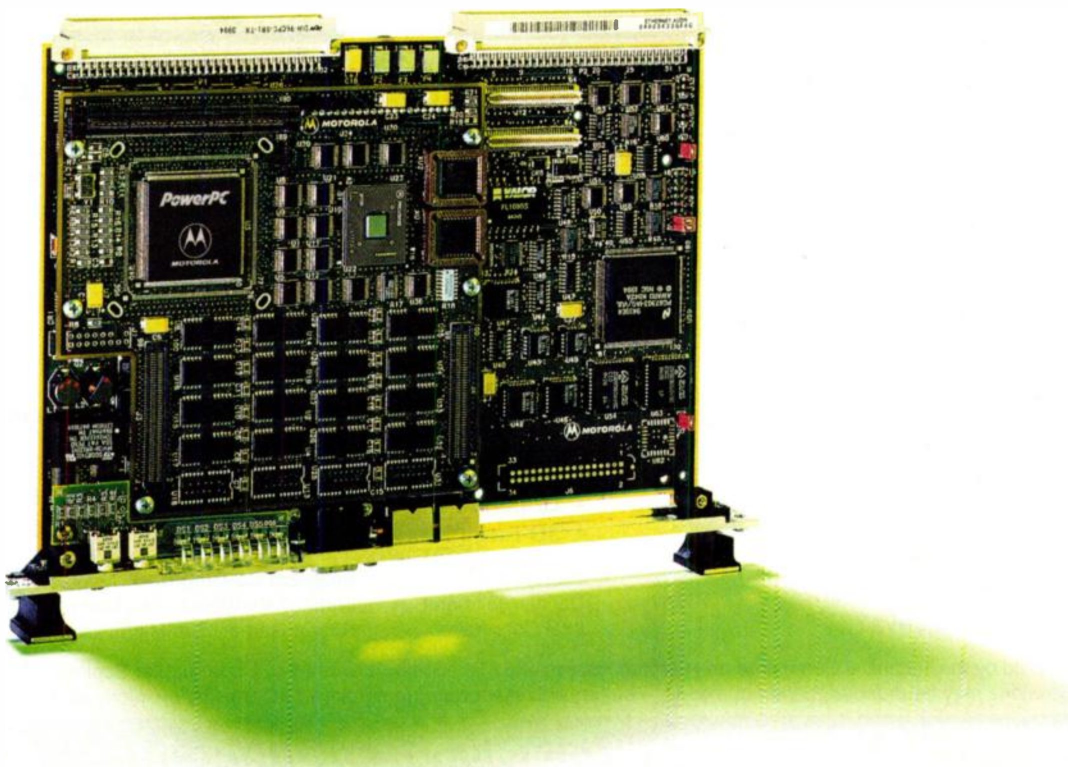
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UPCOMING MEETINGS

SEPTEMBER

Fourth European Congress on Intelligent Techniques & Soft Computing (EUFIT 96), Sept. 2-5. Aachen, Germany. Contact Karl Lieven, Chairman, Organization Committee, EUFIT '96, Promenade 9, 52076 Aachen, Germany; (49) 2408-6969; fax (49) 2408-94582; e-mail: eufit@mitgmbh.de; http://www.mitgmbh.de/elite/eufit.html.

Fifth IEEE International Fuzzy Systems Conference, Sept. 8-11. Hyatt Regency Hotel, New Orleans, Louisiana. Contact Frederick Petry, School of Engineering and Computer Science, 301 Stanley Thomas Hall, Tulane University, New Orleans, Louisiana 70118-5698; (504) 865-5840; fax (504) 862-8247; e-mail: petry@cs.tulane.edu.

Surface-Mount International, Sept. 8-12. San Jose Convention Center, San Jose, CA. Contact Yolanda King, Miller Freeman Inc.; (415) 905-4994; e-mail: yking@mfi.com.

Connector and Interconnection Symposium and Trade Show, Sept. 16-18. Boston, Massachusetts. Call (703) 907-7536.

NESEA Sustainable Transportion & S/EV96 Symposium, September 16-18. Madison Square Garden, New York. Contact Northeast Sustainable Energy Association (NESEA), 50 Miles St., Greenfield, Massachusetts 01306; (413) 774-6051; fax (413) 774-6053.

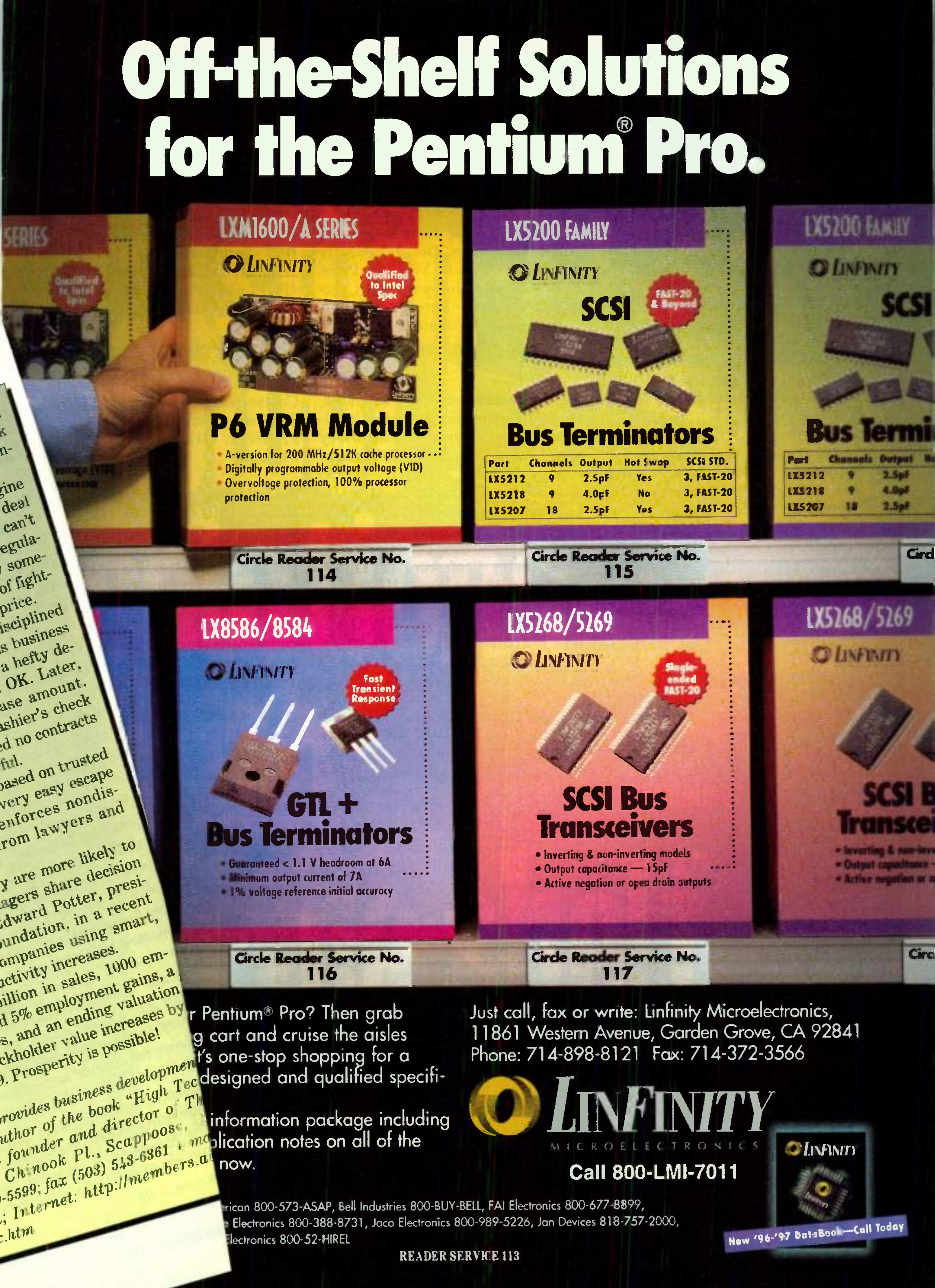
Embedded Systems Conference, Sept. 16-19. San Jose Convention Center, San Jose, California. Contact Natasha Claro, Miller Freeman Inc.; (415) 905-2354.

AUTOTESTCON 96, Sept. 16-19. Dayton Convention Center, Dayton, OH. Contact Jerry Duchene, ASC/ENAS, Bldg. 20, 2450 D. St., Suite 2, WPAFB, OH 45433-7630.; (513) 255-2025; fax (513) 255-3460; e-mail: duchenjl@smtplink.en.wpafb.af.mil.

Third IEEE International Conference on Image Processing (ICIP 96), Sept. 16-19. Swiss Federal Institute of Technology, Lausanne, Switzerland. Contact Murat Kunt, Signal Processing Laboratory, EPFL, CH-1015 Lausanne, Switzerland, (41) 21-693-2626; fax (41) 21-693-2603; e-mail: kunt@ltssun2.epfi.ch.

Interactive Multimedia Association First Annual Expo, Sept. 17-19. Jacob Javits Convention Center, New York. Contact IMA Expo '96, 951 Naruber's Island Blvd., Suite 700, San Mateo, CA; (415) 286-2531; http://www.ima.org.

11th Annual Workshop on Computer Communications (11th CompComm), Sept. 22-25. Reston, VA. Contact Guy Omidayar, 4301 Forbes Boulevard, Lanham, Maryland 20706; (301) 918-1191; fax (301) 731-3380; e-mail: gomidyar@tsmi.iitri.com.



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TRUDEL to form

One of the challenges of the Information Age is discovering truth. Today almost anyone—on just about any side of any issue—claims they represent the side of the angels, including at truth and beauty, and often goodness and mercy. Worse yet, anyone can download a deluge of data to "prove" their case.

The Machine Age was based on the charmingly naive notions of simple rules and black and white issues. That doesn't work anymore. Maybe it never did. Adding more rules, laws, bureaucrats, accountants, and lawyers has made matters worse. Much worse.

Today's world more closely resembles a Star Trek holodeck than a laboratory for repeatable Newtonian bench science. We can create prosperous new realities in a myriad of rich colors, but the era of bosses and workers, linear methodology, and repetitive process industries is drawing to an end. This belief led me to found my consulting practice in 1988.

Many in Western business and government differ. We disagree on the most basic issues. Are present business methods working, or are most firms declining? Is the Dilbert model of clueless management, burned-out workers, and shoddy products valid? Or have U.S. firms finally reached the nirvana of renewed global competitiveness?

I say major change is needed, but Bob Allen of AT&T and many on Wall Street would disagree. They can point to profits, stock prices, and their bonus packages as evidence.

In the end, it all boils down to "Who can you trust?" In a society that tolerates greed and clever crooks with tricky lawyers, trust can only be based on strong rela... tionships.

This is why small teams are the future of busin... How many people can you know well enough to "re...

trust? Experts say perhaps 50, if you are luc... wise. The most successful firms and societi... hard to expand that number. They are ruthle... ishing or banishing violators.

I recently bought a sophisticated, used, aircraft for my business. It could be disas... like that went sour. All the lawyers in ... save you. The courts and the FAA's m... tory bureaucracy are of little or no h... one involved in just such a dispute. ... ing, the legal bills have exceeded th...

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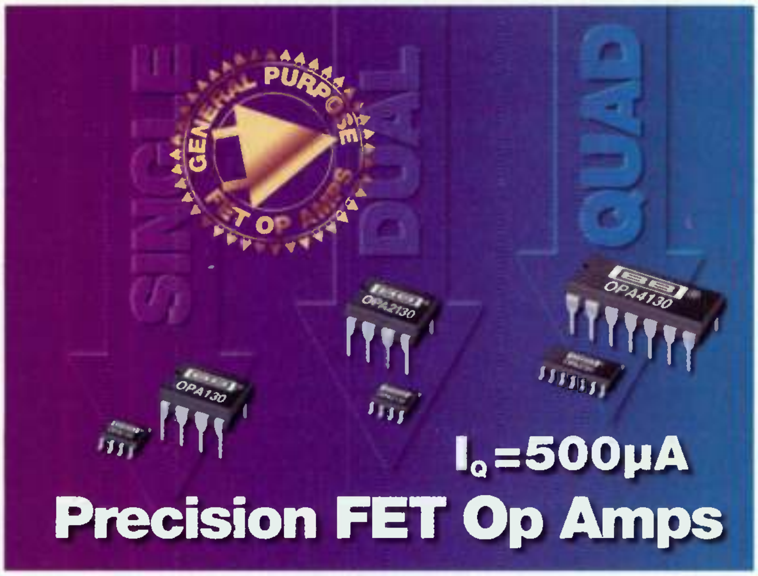

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OPA130 series of single, dual, and quad FET-input op amps are ideal for general-purpose, portable, and battery powered applications. They're easy to use and free from phase inversion and overload problems commonly found in FET-input op amps. Key specs: 500µA/amp low quiescent current, 1mV max offset voltage, 120dB min open loop gain, 20pA max input bias current, 1MHz bandwidth, and ±2.25V to ±18V wide supply range. OPA130 and OPA2130 (dual) are available in 8-pin DIP and SO-8 surface-mount packages. OPA4130 is available in 14-pin DIP and SO-14 surface-mount packages. **OPA130** is priced at **$1.30** in 1000s; **OPA2130** is **$2.10**; **OPA4130** is **$3.40**.

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Operational Amplifiers Brochure

Our new eight page brochure, *Operational Amplifiers*, features over twenty new op amps. It has selection guides on precision and high speed op amps along with complete specifications, and applications information. Four pages of technical info highlight high speed amps, video amps, audio amps, precision amps, current-feedback amps, wide bandwidth amps, single power supply amps, precision FET amps, and switchable-input amps. **FREE** from local sales rep or call **(800) 548-6132**.

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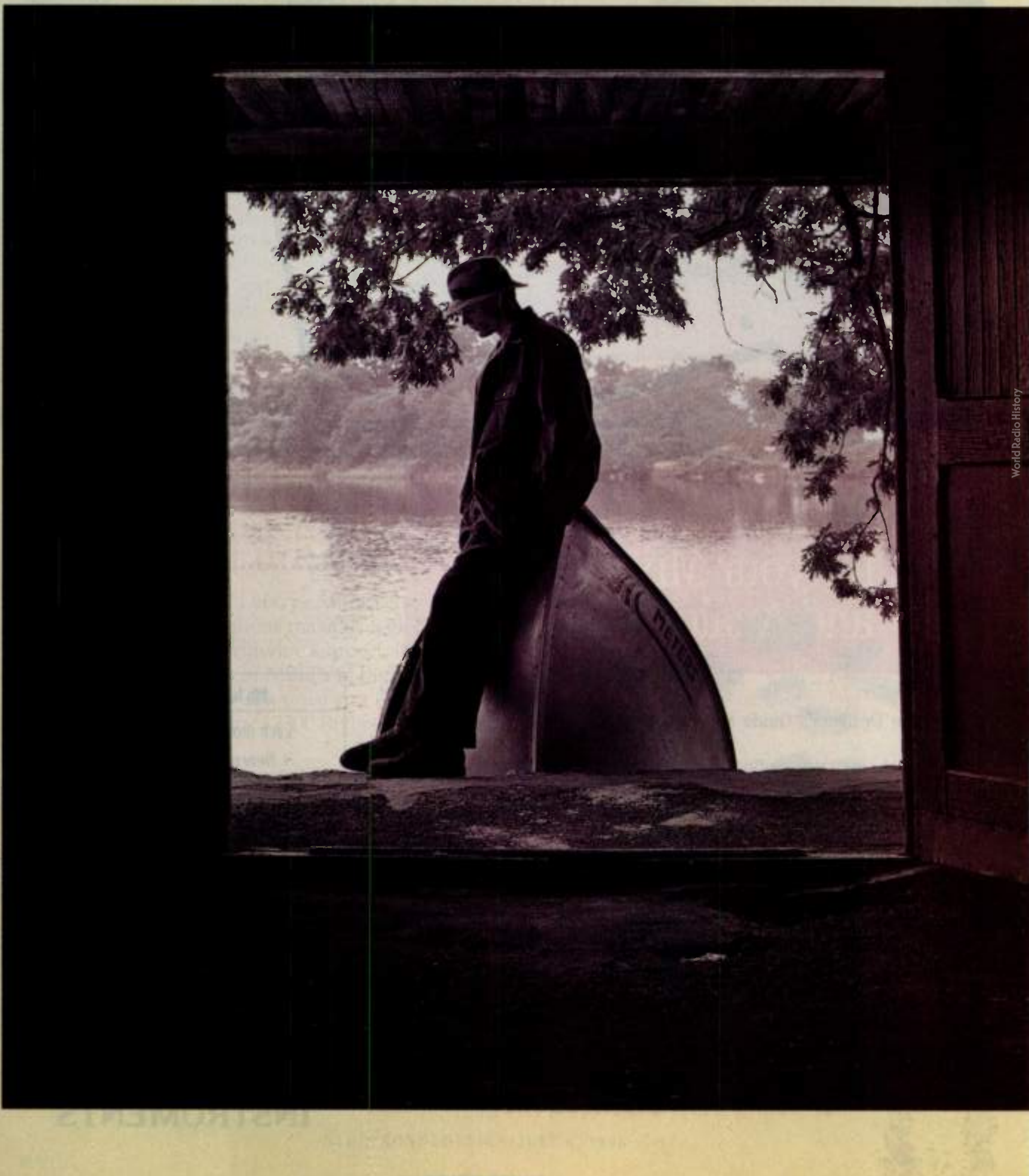

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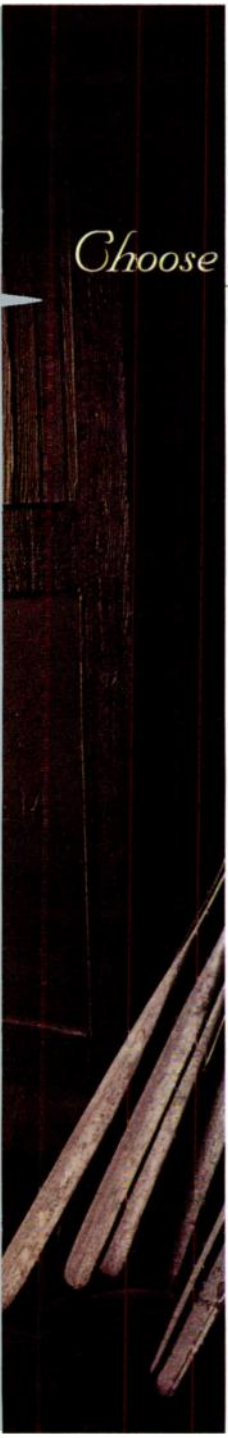

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SPECint92/SPECfp92	80/60	75/85	—	—
SPECint95/SPECfp95	—	—	5.5/5.5	3.29/n/a
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SEPTEMBER

Second International Conference on Satellite Communications (ICSC 96), Sept. 23-27. Moscow, Russia. Contact Henrich Lantsberg, IRE RAS Mokhvaya 11 Moscow 103907 Russia,; (7) 095 2034985; fax (7) 095 8414; e-mail: h.lantsberg@ieee.org.

13th International Conference on Microwave Ferrites, Gyromagnetic Electronics & Electrodynamics, Sept. 23-27. Busteni, Prahova Valley, Romania. Contact Secretariat: AFERRO-SA, 72321 Bucharest, Cales Floreasca 169, P.O. Box 30-30, Romania; (004)-1-212 10 29, fax (004)-1-312 37 46; e-mail: icmf@lmn.pub.ro.

Second International Congress on Molded Interconnect Devices (MID 96), Sept. 25-26. University of Erlangen-Nuremberg, Erlangen, Germany. Contact MID '96 Conference Secretariart, Research Association 3-D MID, Elektronische Baugruppen (3-D MID e.V.), Frank Pohlau, Egerlandstrasse 7, D-91058, Erlangen, Germany; (49) 9131/85-7964; fax (49) 9131/30 25 28.

IEEE ATM Workshop (ATM 96), Sept. 25-27. San Francisco, CA. Contact Guy Copeland, Computer Sciences Corp., MC299, 3001 Centreville Rd. Herndon, VA 22071; (703) 471-3044; fax (703) 471-3145; e-mail: gcopelan@csc.com.

Third IEEE Workshop on Interactive Voice Technology for Telecommunications Applications (IVTTA 96), Sept. 29-Oct 1. Basking Ridge, NJ. Contact Murray F. Spiegel, Bellcore, 445 South St., Room 1C237R, Morristown, NJ 07960; (201) 829-4518; fax (201) 829-5963; e-mail: spiegel@bellcore.com.

Fifth IEEE International Conference on Universal Personal Communications (ICUPC 96), Sept. 29-Oct. 3. Cambridge, MA. Contact Donald M. Steinbrecher, Steinbrecher & Co., 30 North Ave., Burlington, MA 01703-3398; (617) 273-1400; fax (617) 273-4166; e-mail: dsteinbrecher@steinbrecher.com.

OCTOBER

First International Industrial Control Programming Conference (IPC), Oct. 1-2. Centre des Congres de la Villette, Paris, France. Contact Eelco van der Wal, Managing Director, PLCopen, P.O. Box 2077, NL 5300 CB Zaltbommel, Netherlands, (31) 418-541139; fax (31) 418-515115.

First International Embedded Computing Conference, Oct. 1-2. Centre des Congres de la Villetter, Paris, France. Contact Josey van Alem, Active Exhibitions Europe, P.O. Box 2114, NL 5300 CC Zaltbommel, Netherlands, (31) 418-512999; fax (31) 418-515115.

Third International CAN Conference, Oct. 1-2. Centre des Congres de la Villetter, Paris, France. Contact Josey van Alem, Active Exhibitions Europe, P.O. Box 2114, NL 5300 CC Zaltbommel, Netherlands, (31) 418-512999; fax (31) 418-515115.

IEEE International Telecommunications Energy Conference (INTELEC 96), Oct. 6-10. The Westin Hotel, Boston, MA. Contact C.K. McManus, GNB Industrial Battery Co., Woodlake Corporate Park, 829 Parkview Blvd., Lombard, IL 60148-3249; (708) 691-7938; fax (708) 629-2635.

International Conference on Signal Processing Applications and Technology (ICSPAT), Oct 7-10. World Trade Center, Boston, MA. Contact Miller Freeman Inc., (415) 356-3391; fax (415) 905-2220; e-mail: dsp@mfi.com.

Second European Workshop on Mobile & Personal Satcoms (EMPS 96), Oct. 9-11. Rome, Italy. Contact Francesco Vatalaro, Universita di Roma Tor Vergate, DIE, Via Della Ricera Scientifica, 00133 Roma, Italy; (39) 6772599 4464; fax (39) 6 2020519; e-mail: vatalaro@tovvxl.ccd.utovrm.it.

Third International Conference on Electronics, Circuits, and Systems (ICECS 96), Oct. 13-16. Rodos, Greece. Contact ICECS Secretariat, Electrical Engineering Department, University of Patras, 26500, Greece; (30) 61 997 283; fax (30) 61 994 798; Internet: http://www.vlsi.ee.upatras.gr/ICECS96/.

19th IEEE/CPMT International Electronics Manufacturing Technology Symposium, Oct. 14-16. Austin, T[illegible] Contact E. Jan Vardaman, Te[illegible] Search International, 9430 Resea[illegible] Blvd., Bldg. 4, #400, Austin, TX 787[illegible] (512) 343-4508; fax (512) 343-4509[illegible] mail: j.vardaman@ieee.org.

OCTOBER

IPC TechWorks 96, Oct. 19-24. Naples, FL. Contact David Bergman, IPC TechWorks '96; fax (847) 509-9798; e-mail: DavidBergman@ipc.org.

IEEE International Test Conference (ITC 96), Oct. 20-24. Washington Sheraton Hotel, Washington, DC. Contact Doris E. Thomas, ITC, 205 Tennyson Avenue, Suite C, Altoo[illegible], PA 16602; (814) 941-4666; fax (8[illegible] 941-4668.

IEEE Military Communications C[illegible]ference (MILCOM 96), Oct. 2[illegible] Reston, VA. Contact John S. Quilt[illegible] The Mitre Corp., 7525 Colshire Dr., McLean, VA 22102-3481; (703) 883-6071; fax (703) 883-3397.

WESCON 96, Oct. 22-24. Anaheim Convention Center, Anaheim, CA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045-3194; (800) 877-2668; fax (310) 641-5117.

IEEE/AIAA 15th Digital Avionics Systems Conference, Oct. 27-Nov. 1. Sheraton Colony Square Hotel, Atlanta, [illegible] Contact Ellis F. Hitt, Battelle, 505 K[illegible] Ave., Columbus, OH 43201-2693; (6[illegible] 424-6595; fax (614) 424-3962.

Communication Design Engineer[illegible] Conference, Oct. 28-31. Santa Clara Convention Center, Santa Clara, CA. Contact Natasha Claro, Miller Freeman Inc.; (415) 905-2354.

19th Space Simulation Conference, Oct. 28-31. Radisson Plaza Lord Baltimore Hotel, Baltimore, MD. Co[illegible]tact The Institute of Environmen[illegible] Sciences, 940 East Northwest Hw[illegible] Mount Prospect, Illinois 60056; (70[illegible] 255-1561; fax (708) 255-1699.

PCB Design Conference East, Oct. [illegible]31. Tara's Ferncroft Conference R[illegible]sort, Danvers, MA. Contact Yolan[illegible] King, Miller Freeman Inc. (415) 9[illegible] 4994.

ELECTRONIC DESIGN QUICKLOOK

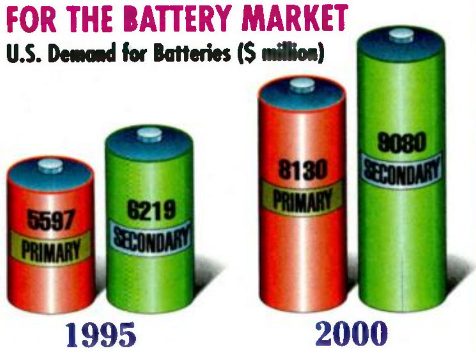
EDITED BY ROGER ENGELKE AND MIKE SCIANNAMEA

MARKET Facts

The **"EVERLASTING"** demand for batteries, primarily those in the more expensive bracket that offer longer life and higher performance, will continue as long as portable devices proliferate. According to research done by The Freedonia Group Inc., Cleveland, Ohio, overall battery sales will increase 7.8% annually to over $17 billion by the year 2000. Within the secondary (rechargeable) batteries market, lead-acid types will maintain their domination. Most lead-acid sales will involve starting-lighting-ignition (SLI) batteries. Added gains also are anticipated in backup power, though, benefiting from the fervent need to provide continuous power for central data-processing systems, aircraft radar-tracking systems, and other equipment in which power failure can't be tolerated. Other rechargeable batteries, such as nickel-cadmium and the more-advanced varieties, are expected to make sizable strides in grabbing a larger chunk of the market. This is due to the increased number of cordless portable devices, such as household appliances, telecommunication devices, and sophisticated electronic products (portable computers, etc.). Another reason for the growth is that recycling problems associated with these batteries (nickel-cadmium, lithium, nickel-metal-hydride, and zinc-air) are finally getting addressed adequately. As for primary (non-rechargeable or disposable) batteries, consumer preference for alkaline batteries over lower-priced zinc-carbon or zinc-chloride types, as well as the previously discussed portable phenomenon, will jump-start this market. To obtain their 293-page study titled "#779, Batteries," contact The Freedonia Group at 3570 Warrensille Center Rd., Ste. 201, Cleveland, Ohio 44122-5226; (216) 921-6800; fax (216) 921-5459; e-mail: tfgi@ix.netcom.com.—*RE*

A "POSITIVE" OUTLOOK FOR THE BATTERY MARKET

U.S. Demand for Batteries ($ million)



Primary: Alkaline and others
Secondary: Lead-acid and non-lead acid
Source: The Freedonia Group

EYE ON ISO 9000

Pressure Systems Inc. (PSI), and its subsidiary, KPSI, have achieved ISO 9001 certification. The company is a manufacturer of pressure scanning instruments for industrial and aerospace applications. Contact PSI, 34 Research Dr., Hampton, VA 23666. CIRCLE 691

Johnson Matthey Electronics' (JME) San Jose, Calif. facility has received ISO 9001 certification. The facility manufactures thermocouples used in precision temperature measurement and assembles components for semiconductor process equipment. Contact JME, E. 15128 Euclid Ave., Spokane, WA 99216; (509) 924-2200. CIRCLE 692

Hoffman Engineering Co. has achieved ISO 9001 registration. The company is a supplier of electrical and electronic enclosures, specializing in products for various industrial environments. Contact Hoffman Engineering Co., 900 Ehlen Dr., Anoka, MN 55303-7504; (800) 355-3560; fax (612) 942-6940. CIRCLE 693

Aavid Thermal Technologies Inc. has received ISO 9001 certification. The company designs, develops, and manufactures thermal-management products that dissipate unwanted heat in electronic and electrical components and systems. Contact Aavid Thermal Technologies Inc., One Kool Path, P.O. Box 400, Laconia, NH 03247-0400; (603) 528-3400; (603) 528-1478. CIRCLE 694

QLP Laminates Inc. has been awarded ISO 9002 certification. The company is a supplier of printed-circuit board laminates and materials. Contact QLP Laminates Inc., 4955 E. Hunter Ave., Anaheim, CA 92807; (714) 970-1471; fax (714) 779-0392. CIRCLE 695

OFFERS YOU CAN'T REFUSE

TRUDEL *to form*

One of the challenges of the Information Age is discovering truth. Today almost anyone—on just about any side of any issue—claims they represent the side of the angels, including at least, truth and beauty, and often goodness and mercy. Worse yet, anyone can download a deluge of data to "prove" their case.

The Machine Age was based on the charmingly naive notions of simple rules and black and white issues. That doesn't work anymore. Maybe it never did. Adding more rules, laws, bureaucrats, accountants, and lawyers has made matters worse. Much worse.

Today's world more closely resembles a Star Trek holodeck than a laboratory for repeatable Newtonian bench science. We can create prosperous new realities in a myriad of rich colors, but the era of bosses and workers, linear methodology, and repetitive process industries is drawing to an end. This belief led me to found my consulting practice in 1988.

Many in Western business and government differ. We disagree on the most basic issues. Are present business methods working, or are most firms declining? Is the Dilbert model of clueless management, burned-out workers, and shoddy products valid? Or have U.S. firms finally reached the nirvana of renewed global competitiveness?

I say major change is needed, but Bob Allen of AT&T and many on Wall Street would disagree. They can point to profits, stock prices, and their bonus packages as evidence.

In the end, it all boils down to "Who can you trust?" In a society that tolerates greed and clever crooks with tricky lawyers, trust can only be based on strong relationships.

This is why small teams are the future of business. How many people can you know well enough to "really" trust? Experts say perhaps 50, if you are lucky and wise. The most successful firms and societies work hard to expand that number. They are ruthless in punishing or banishing violators.

I recently bought a sophisticated, used, multiengine aircraft for my business. It could be disastrous if a deal like that went sour. All the lawyers in the world can't save you. The courts and the FAA's megastate regulatory bureaucracy are of little or no help. I know someone involved in just such a dispute. After years of fighting, the legal bills have exceeded the aircraft's price.

The solution? Expert, trustworthy, multidisciplined teams. I paid a trusted friend to help me. His business is buying and selling aircraft. He put down a hefty deposit to hold the plane based on my verbal OK. Later, sight unseen, I paid him the full purchase amount. When we went to get it, he brought a cashier's check and a mechanic friend he trusted. We used no contracts or lawyers, and the results were wonderful.

My consulting engagements are also based on trusted relationships. My simple contract has very easy escape clauses. It clarifies deliverables, enforces nondisclosure, and protects both sides from lawyers and bureaucrats.

"High salaries in the next century are more likely to come from companies where managers share decision making with employees," said Edward Potter, president of Employment Policy Foundation, in a recent *Wall Street Journal* article. Companies using smart, trusted teams see 18-25% productivity increases.

Assume a firm with $100 million in sales, 1000 employees, 20% productivity, and 5% employment gains, a starting valuation of 2X sales, and an ending valuation of 4X sales. In a decade, stockholder value increases by $582 million and jobs by 629. Prosperity is possible!

John D. Trudel, CMC, provides business development consulting and is the author of the book "High Tech with Low Risk." He is founder and director of The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; phone (503) 640-5599; fax (503) 543-6361; e-mail johntrudel@aol.com; Internet: http://members.aol.com/johntrudel/index.htm

QUICKLOOK

Is Your Company Among The BEST?

Question: Why do some companies put out better products than others? What makes these companies stand out above the rest? According to a recent study on product-development practices, the leaders are much more willing to define their products with suppliers, to intertwine development efforts with strategic goals, and to define various aspects of the product in multiple ways. The study was conducted by Product Development Consulting Inc. (PDC) and the Management Roundtable.

Of the 335 companies that responded to the survey, 81 were defined as best-in-class, based on market share, sales, and qualitative success factors. The surveyed companies represented a broad cross-section of industries, including medical, hardware and software, communication, and instrumentation companies.

The study reveals the kinds of characteristics that set leading companies apart from their competition when it comes to product development. For example, the best-in-class companies (BEST) collaborated with suppliers more frequently and consistently than the rest of survey respondents (REST). To be specific, the BEST companies do things like have a supplier permanently on-site to collaborate on product information; share ideas on strategic and product planning; and solicit suppliers' input on product plans.

There is strong evidence to suggest that when a company coordinates its development efforts with its strategic goals, it is well worth the investment in time, effort, and dollars. In fact, 66% of the BEST use a product line or division strategy, 42% use a product portfolio analysis, and 30% use a technology forecast to develop products, versus 51%, 28%, and 21% of the REST, respectively. Furthermore, 67% of the BEST use competitive analysis and market share estimates to product development planning, compared to 57% of the REST.

BEST companies are more likely to have defined and communicated a number of success factors to their development teams. How companies deal with such issues as project endorsement by upper management, user requirements, product positioning, and strategic alignment significantly influence the chances of product success.

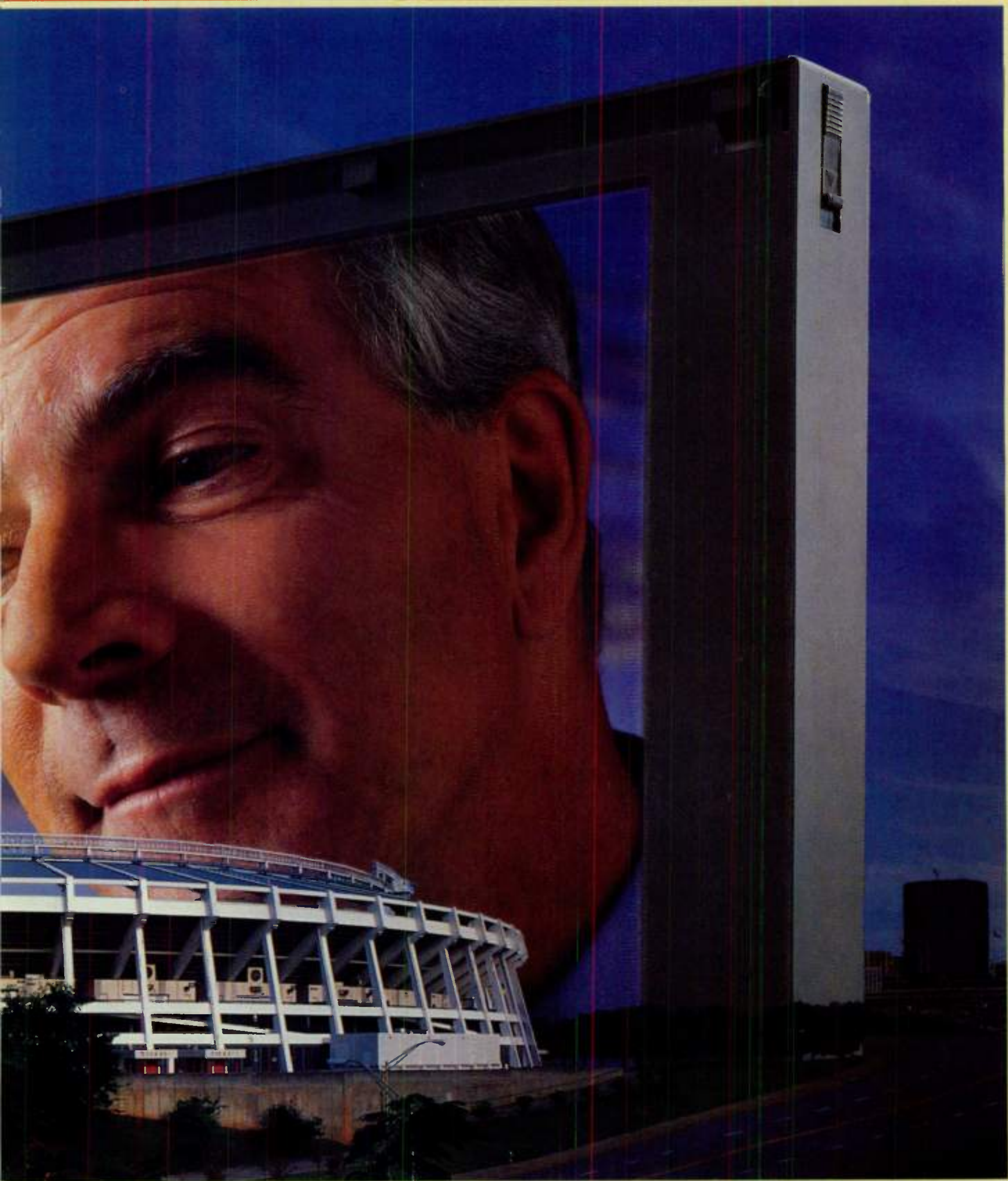
The BEST companies cancel markedly fewer projects in full-scale development—only 10%, compared to an average of 17% among the REST. This can be attributed to a company doing its homework up front. In other words, they ask, and more importantly, they listen. Over one-third of all respondents ranked late discovery of customer requirements as the number one reason for making major changes to projects after full-scale development had already started. Over a fourth of the respondents reported that unanticipated technical difficulties caused them to change features late in the development process. Only 26% of BEST companies reported making changes to their projects (26%) than the REST, which made changes to 39% of their products.

To obtain a copy of this report, contact PDC Inc., 84 State St., Boston, MA 02109; (617) 723-1150; fax (617) 723-3050.—MS

Our LCD's *have grown.*

In the two short years since we entered the market, Samsung has become one of the world's leading TFT LCD manufacturers.

As you may know, we already offer a line of TFTS 20% brighter



and with 30% more color saturation than the closest competitors.

We'll be following up soon with more products that are—well—larger than life. Including a 13.3" XGA notebook panel, and XGA and SXGA panels actually designed for desktop monitors—in a whopping 14" and 15.1".

And hey, with the desktop impending, can the coliseum really be far behind?

Onward and upward, guys.

SAMSUNG

SEMICONDUCTOR

STILL A *Generation* AHEAD.

(MOTOR HEADS? YOU SAID IT, NOT US.)

When Logic Switches *Too Fast*

"We've been shipping the same product for 10 years now, and it worked just fine until last month. I don't know what happened, but that new batch of chips just doesn't seem to work anymore. The darn thing just has a 5-MHz processor and a few logic gates. What could have gone wrong?"

Sound familiar? That's not too surprising. I hear the same story from engineers all over the country. The most common cause of this nagging problem is rise-time shrinkage.

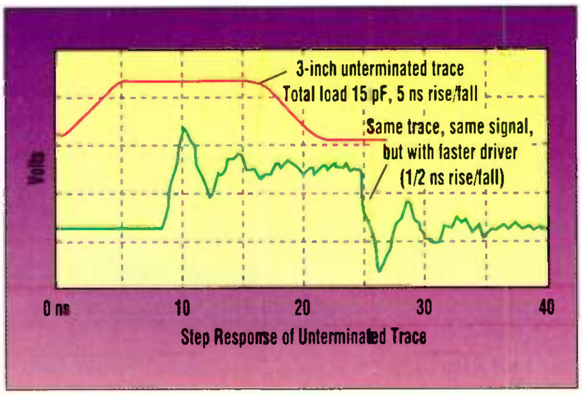
Not long ago, the major TTL logic families all had typical rise and fall times that, by modern standards, were very slow—on the order of 10 ns. Products that use these old chips have few problems with ringing or crosstalk. Today's digital logic operates much faster. Modern vanilla-bean logic families have rise and fall times on the order of 1 ns or less. As chips continue to shrink, and as switching speeds continue to improve by a factor of two every few years, we will soon see rise and fall times slink down into the deep subnanosecond realm, a territory previously reserved for UHF and microwave engineers. This relentless, shrinking trend toward subnanosecond rise times brings us to the crux of the problem: Faster switching exaggerates problems with ringing and crosstalk. Over the years, as logic outputs have continued to switch faster and faster, problems with ringing and crosstalk have gotten progressively worse.

Howard W. Johnson

The two traces in the figure illustrate the nature of the problem. This scenario represents the behavior of an unterminated logic trace which is driven with two different test signals:

(a) Typical 1986 driver output (rise/fall = 5 ns)
(b) Typical 1996 driver output (rise/fall = 1/2 ns)

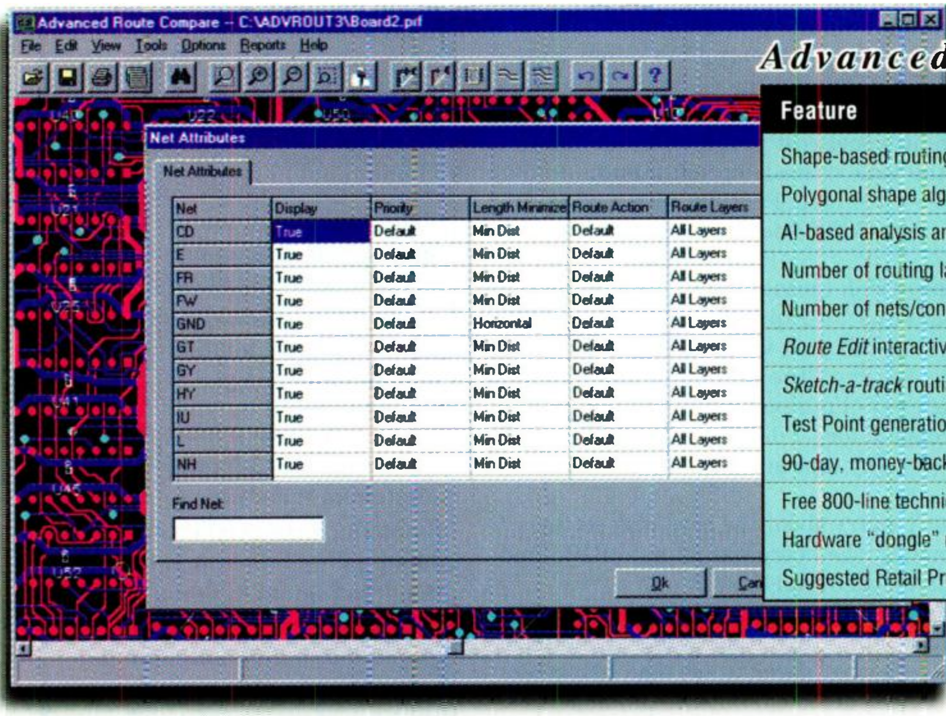
In both cases, the trace is the same length (3 in.) and is driven with the same logic pattern. With the older, slower driver, the signal looks OK. With the newer, faster driver, the signal is almost unrecognizable. There aren't too many of us that would want to depend on such a signal for our processor clock or address-data bus, yet this is precisely the signal found in many digital products (hopefully, not yours). These products were often designed in one era, assuming slow logic, and subsequently assembled using more modern, faster logic. The clock rate in both cases is the same. *Nobody sped up the clock.* The problem is entirely due to an increase in switching speed (faster rise and fall times). Where ringing is concerned, the switching speed matters more than the clock rate.



This example brings home two very important points. First, for a given layout, faster switching makes for uglier signals. This problem is inescapable. It can only be circumvented by improving the layout, reducing the loads, or adding terminators. Second, chip manufacturers are not always doing us a favor when they begin shipping "new and improved" logic circuits. When they are substituted into an older design, the increase in speed may buy you nothing but headaches.

Howard W. Johnson is the president of Olympic Technology Group Inc., a high-technology consulting firm that specializes in solving high-speed digital design problems. Dr. Johnson is the author of "High-Speed Digital Design: A Handbook of Black Magic" (Prentice-Hall, 1993), and reguarly presents technical workshops for digital engineers, including courses for Oxford University. He can be reached at 16541 Redmond Way, Suite 264, Redmond, WA 98052; (206) 556-0800; e-mail: 74720.2333@compuserve.com.

Shaped-based routing from Protel®



Advanced Route3 vs. Specctra®

Feature	Route3	Specctra SP-10
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Polygonal shape algorithms	✔	–
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Number of nets/connections/pins	Unlimited	Unlimited
Route Edit interactive routing	Included	Optional
Sketch-a-track routing option	Included	Optional
Test Point generation/DFM option	Included	Optional
90-day, money-back guarantee	✔	–
Free 800-line technical support	✔	–
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Letters from London

Board Games

PETER FLETCHER

Working as a field-service engineer with what was then Burroughs Machines Ltd. nearly 35 years ago, I got to appreciate very quickly that learning how things work isn't that difficult. Learning how to mend them when they break is another matter altogether, though.

I was starkly reminded of this when I finally got around to replacing the motherboard on my four-year-old PC a few weeks ago. I could have bought a new one, I suppose, but the job seemed simple. I had the machine and its software set up the way I liked it—it just needed a bit more "ooomph." And, of course, it would cost roughly half of what I'd pay for a brand new machine with the same ultimate specifications.

So the motherboard was acquired—a 100-MHz Pentium with modern 70-pin SIMM slots to replace the 25-MHz 486SX board crammed full of old-fashioned 30-pin SIMMs.

It was time to get started. Carefully think through everything that could go wrong, make sure I have backups on tape of everything vital. Preparation paid off and the actual installation went fine. Less than an hour to strip out the old and replace the new. The only delay was recovering a dropped screw from inside the case—I'm never happy to apply power until all loose metallic parts are accounted for—I do miss my spring-headed Burroughs screwdriver. Still, a bit of sticky tape around the cross head will hold the bolts.

Now for the moment of truth. "Don't worry about the hard-disk settings," said the man in the spares department, "the board has an auto BIOS and will detect and adjust for the disk drives all by itself."

Switch on. "Boing" said the machine. "No drives detected—insert System Disk and press F1." Did that. "Floppy fail." Take it all to bits again (have to remove the power supply to get the board); check to see if all connectors and sockets are firmly seated. "No drives detected." Check all jumpers—I discover that it had been set to the wrong clock speed. "Don't worry," said the spare parts man, "we'll set it up and test it before shipping."

Same story: "No drives detected." That's odd, the hard-disk-drive lights (I have two) lit up and stayed lit. At this point, field-service intuition came into play. The Pentium has a dinky little fan that clips on top. Power for that is picked up from a short bundle of wire with a standard PC power connector at either end (one male, the other female), with a couple of pick-up wires to take the feed to the fan. This is inserted in line with the most convenient feed from the power pack. I chose to use the line that fed the master disk.

These connections seemed firm and good, but something dinged in the back of my head. After a little prodding, poking, and wiggling, I concluded that it "didn't feel quite right." Sure enough, one of the male connector's pins was loose. Quick tweak with the fine-nose pliers, put it all back together, and bingo. "Primary master found, primary slave found." We now seem set to live happily ever after.

Except... where did I put that listing of all the IRQ and memory settings I printed from the Windows 95 Device Manager COM 3—a Hayes Enhanced Serial Port. It seems to have decided not to live at peace with the mouse...

Peter Fletcher is Electronic Design's U.K. correspondent. His e-mail address is: panflet@cix.compulink.co.uk.

CONFERENCE CALL

The Neutron Scattering Satellite Meeting to the XVII IUCr Congress will be held Aug. 5-7 at the National Institute of Standards and Technology's (NIST) headquarters in Gaithersburg, Md. The purpose of the conference is to address advances in neutron scattering instrumentation and applications crystallography, materials science, and molecular biology. Topics to be discussed include developments in neutron instrumentation and detecting advances in data analysis techniques, thin films, and neutron sources. For more information, contact Susan Krueger, NIST, E151 Reactor Bldg., Gaithersburg, MD 20899-0001; (301) 975-6734; e-mail krueger@enh.nist.gov.

The sixth annual Surface Mount International Advanced Electronics Manufacturing Technologies conference and exhibition will be held Sept. 8-12 at the San Jose Convention Center, San Jose, Calif. Featured will be a full-day seminar on chip scale packaging, and a special session on reducing solder joint defects. The conference will include classes, tutorials, and workshops, and over 100 companies are expected to exhibit their latest products and services. For more information, contact Miller Freeman Inc., 600 Harrison St., San Francisco, CA 94107; (415) 905-4994; fax (415) 905-2220.

CORRECTION

In the April 1 review of Nihal Kularatina's book "Modern Electronic Test and Measuring Instruments," the incorrect pricing was given. The hardcover version is priced at $89, and the paperback version is $45. The book is available from the IEEE Operations Center, IEE/INSPEC Dept., 445 Hoes Lane, Piscataway, NJ 08855; (908) 981-0060. The editors wish to apologize for the error.

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1601A

Here's to the WINNERS

LINEAR TECHNOLOGY CORP. (LLTC) was recently awarded the 1996 Kachina Award for "Best Financially Managed Company with Manufacturing Facilities" from In-Stat, the electronics market research firm based in Scottsdale, Ariz. Headquarted in Milpitas, Calif., LLTC is an independent manufacturer of high-performance analog integrated circuits. The company previously received the award in 1992.

Companies considered for the award must be publicly traded U.S. corporations recognized as active in the semiconductor market. The award is calculated on the basis of categories such as net income, cost of sales, R&D investment, return on investment, inventory turnover, and net operating profit. This year's award was based on 1995 calendar year financial information.

For more information about LLTC, they may be contacted at 1630 McCarthy Blvd., Milpitas, CA 95035-7417; (408) 432-1900; fax (408) 434-0507. For more information on the Kachina Award, contact In-Stat at (602) 483-4447.

EURO watch

ALFRED VOLLMER

Last year, I told you about the successor of the current CD, which will store audio, video, and computer data–the DVD (digital versatile disk) (*Electronic Design*, Oct. 13, 1995, p. 64R). The first specific hardware elements are now available for setting up a DVD player/writer. Telefunken Microelectronic GmbH (Temic), Heilbronn, Germany, has developed a modular concept for laser drivers/controllers dubbed the U8600B, and will mainly be used in DVD optical disk drives for reading and writing optical disks. In contrast to the currently available magneto-optical (MO) drives, a DVD-RAM drive (drive for reading and writing of DVDs) uses the "phase-change method" to eliminate the process of erasing the disk before rewriting it, which makes DVDs work a lot faster than MO disks.

For the first time ever, all the available functional blocks are now integrated onto one single silicon chip consisting of a broadband servo amplifier, an RF modulator, a pulse-width generator, a digital bus control, and a supervisory unit. The core element of the U8600B is the broadband servo amplifier driving the laser diode with a 100-MHz bandwidth. The dc-current amplification is up to 110 dB and the maximum current is 200 mA with "extremely short rise and fall times," according to a company spokesman. The radio frequency (RF) modulator uses the laser-mode hopping method in order to decrease noise. By using integrated D/A converters, the power values can be varied between the three different operation modes of the laser diode--read, erase, and write. Two pulse-width generators create the write and switch-off impulses. A three-wire bus controls the digital control of the power and pulse width parameters.

The functional blocks can be configured in an ASIC according to the customer's needs. The disk capacity is 2.6 Gbytes with a maximum bit rate of 10.8 Mbit/s, about 20 times faster than current CD technologies. Within a DVD drive, the emitted laser light is controlled by a servo loop consisting of the laser itself, parts of the optical path, a photodiode, and an amplifier. This servo principle is an efficient method for generating the pulse form required for the high write density. The laser power, which is relatively low, is also generated by the controller. For reading the DVD, an additional photo diode sensitive to laser light and an amplifier are used.

DVD, the successor to the current CD, will have a disk diameter of 120 millimeters. This is the same as with the current CD, but the laser wavelength used is 650 nm. The capacity of a single-sided DVD-ROM (read-only) is 4.7 Gbytes. With a capacity of 2.6 Gbytes, a rewritable DVD-RAM is able to store over four times the capacity of an ordinary CD. A high-end version of the DVD-ROM will have a maximum storage capacity of 17 Gbytes.

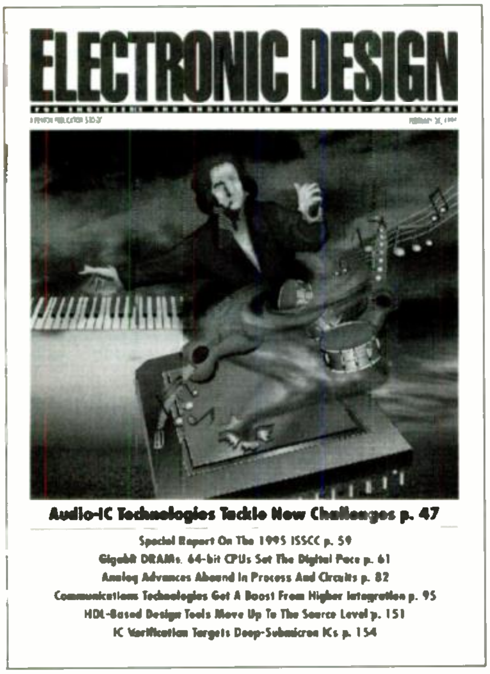
The phase-change principle stresses that GeSbTe layers (Germanium Antimon Tellur) can change their structure from amorphous to monocristalline by warming up the layer to a specific temperature. Depending on the intensity of the laser, it creates the required temperatures. This phase shift changes the transparency of the optical layer for the laser beam. If there is a reflecting layer underneath the thin GeSbTe layer, data can be read with low laser energies and written with maximum laser energy. In contrast to MO disks, there is no need for a magnetic erase procedure before rewriting the disk which saves a lot of time and makes the writing procedure a lot faster.

From today's viewpoint, the modulation technique of the new technology offers a very high write density. Data is written by using a pulse-width modulation that encodes the number of logical zeros following a logical one. By using this method, a write length of 0.25 μm is achieved for every data bit, which means that a data bit is half as long as the wavelength of the used light. The market potential is quite big. Temic predicts that about 60 million DVD-RAM players will be sold by the year 2000. These players will also be able to read today's ordinary CD-ROMs.

Alfred Vollmer is an Electronic Design correspondent based in Munich, Germany. His Compuserve address is 75162,1246.

STRATEGIC PARTNERS WORKING TOGETHER

Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.



A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

Electronic Design is that strategic information partner — a partner who provides the information that helps the systems designer make those critical decisions that stay the course of the technology road map.

Your Strategic Information Partner.

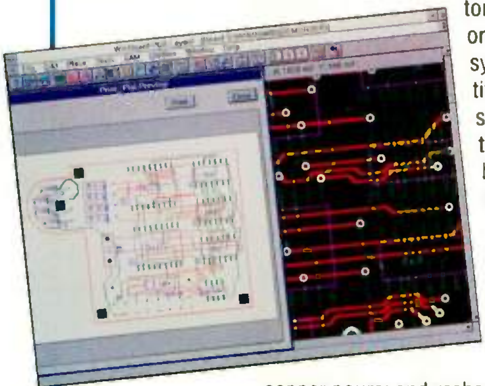
ELECTRONIC DESIGN

A · P E N T O N · P U B L I C A T I O N

QUICKLOOK

HOT PC PRODUCTS

NTE Electronics has released WinDraft schematic design and WinBoard PCB layout, two software programs from IVEX Design International that work with Windows 95 to improve and simplify engineering and design of printed circuit boards. The software also can be used with Windows 3.1, Windows 3.11, and Windows/NT. WinDraft can generate schematic designs within minutes of installation and provides everything needed for wiring, drawing, printing, and finishing the design. It features a full graphical library editor and title block editor; capability to create new component libraries or build upon existing libraries to design custom symbols; and user-definable on-line ERC to identify problem areas in the circuit before final design. The WinBoard PCB layout software delivers the most sophisticated interactive routing capability available for the Windows environment. It has all the power necessary to accommodate complex board designs and the tools to maneuver high speed circuits, analog designs, and dense SMT boards. Also included in Winboard software is a library of over 700 module footprints; on-line editing of pad stacks; quick and easy placement of multiple copper pours; and reshaping of copper zones. Both programs require a 486/DX PC, 8 Mbytes RAM, 10 Mbytes hard disk space, and SVGA. The cost for the software is $29.95 each. Contact NTE Electronics, Inc., 44 Farrand St., Bloomfield, NJ 07003; (201) 748-5089; fax (201) 748-6224.



Tenax Software Engineering has released version 3 of Vortex, the Power Reading Tool, which offers new features such as the ability to read popular word processing files in their native format. These filters will include MS Word, WordPerfect, HTML, and SGML. Additional features include user configurable weighted timing for specific words and punctuation. A new control panel provides VCR-style file access, including fast forward, fast rewind, skip, and word search. Keyboard interfaces for the new control panel support real time variable speed reading. Contact Tenax Software Engineering, 2103 Harrison Ave. NW, Suite 141, Olympia, WA 98502; phone and fax (360) 866-1686; Internet: http://www.halcyon.com/chigh/vortex.html.

INTERNET NEWS

Are Americans risking their funds in on-line banking? Are credit card transactions on the Internet secure? Can our financial privacy be invaded easily in Cyberspace? These are some of the issues being addressed by the Information Infrastructure Standards Panel (IISP), a group of more than 80 companies, organizations, and government agencies working together under the aegis of the American National Standards Institute (ANSI). IISP's objective is to identify the standards needed to facilitate the growth of the information superhighway by determining where new standards development work is needed, and by ensuring that those standards are created in a timely fashion.

Speakers at a recent IISP meeting reviewed varying perspectives of ensuring financial and information security in Cyberspace and focused on the role of standards in developing methods to increase security. The panel also approved nine new application-to-application standards needs added to the 35 standards previously identified as key requirements.

The IISP is working to identify the standards needed for networks—among telecommunications, cable, and broadcast/wireless companies, for example—to interconnect and operate compatibly. Some specific areas of standards requirements being addressed include healthcare informatics, application-to-network issues, nomadicity (facilitating access to services, people and content while "on the move"), entertainment, information security and encryption, and intellectual property rights. Standards needed for global coordination also are being examined.

IISP recently hosted a roundtable of standards organizations that focused on standards that will tie cross-industry networks together. Participants included the Internet Engineering Task Force, Committee T1-Telecommunications, National Cable Television Association, and the Electronic Industries Association.

IISP's members represent sectors—including information technology, telecommunications, cable television, banking, medical, and wireless—that are converging and interconnecting. Panel members include Hewlett-Packard, AT&T, the National Association of Broadcasters, the Federal Communications Commission, and the National Institute of Standards & Technology. ANSI is a private nonprofit organization that coordinates the U.S. voluntary standards system, bringing together interests from the private and public sectors to develop voluntary standards for an array of U.S. industries.

Information on IISP, including membership and meeting schedules, is available on the panel's World Wide Web site (http://www.ansi.org/iisp/iisphome.html) or by contacting R.M. Chick Hayden (212-642-4920; e-mail: chayden@ansi.org) or Peter Lefkin (212-642-4979; e-mail: plefkin@ansi.org). For more information on ANSI, contact them at 11 West 42nd St., New York, NY 10036; (212) 642-4900; fax (212) 398-0023.

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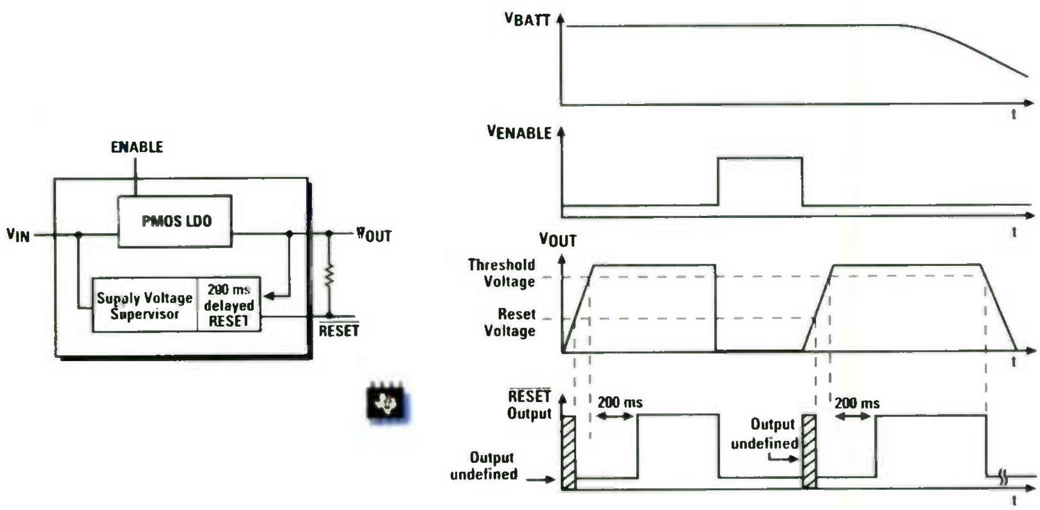

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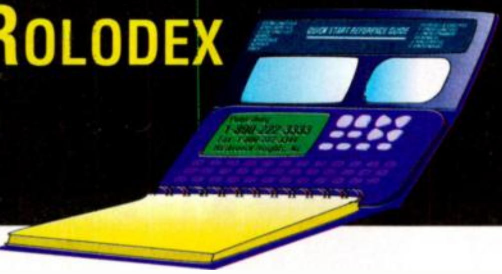


http://www.natinst.com/idnet: Users will be able to learn about National Instruments' entire library of instrument drivers for use with LabVIEW and LabWindows/CVI software at this InstrumentationWeb site. Users can search the network by keyword or phrase and browse all instrument drivers categorized by vendor, by LabVIEW instrument drivers, and by LabWindows/CVI instrument drivers. Extensive information can be downloaded, including the communication interface of the instruments; the operating system with which the driver is compatible; the version of LabVIEW or LabWindows/CVI used to create the driver; the availability and origin of the driver; and whether the driver is VXIplug-and-play-compliant.

http://www.thomasregister/cpi: Surfers will be able to view Computer Power's short-form catalog that features many emergency power systems, including the new Survivor UPS series. This Thomas Register-owned site is dedicated to providing timely information to the industry.

http://www.avxcorp.com: Tap into the latest information on AVX's selection of MLC and tantalum capacitors, power-supply capacitors, resistor chips, arrays and networks, and integrated passive components. Color catalogs can be viewed on the site, as is technical data of thin-film inductors, SMT fuses, transient suppressors, filters, piezoelectric resistors, and timing devices. Also included are current AVX financial summaries and the corporate overview detailing AVX's history.

http://www.cast-inc.com: Designers can see descriptions of CAST Inc. and its latest VHDL simulation and synthesis model library offerings at this web site, and are able to join the private CAST Club for some VHDL fun. CAST Club members can download a free VHDL model every month, and have access to VHDL-themed crossword puzzles and other games. An on-line member roster and forums for exchanging VHDL stories and tips support the growing CAST Club community.

http://www.nmia.com/ergoware: Computer injuries? Yes, this page created by LBI Inc. is geared toward the little-discussed world of computer ergonomics, Carpal Tunnel Syndrome, and other computer-related injuries. It also reviews products designed to help reduce the risk of being injured while working with computers, such as the Ergoware Wrist Supports and Mouse Pads.

http://www.solutions.apple.com/: Information on Apple Computer Inc.'s Apple Internet Server Solution, which is part of its Macintosh Internet Solutions Guide, is available at this site. The Guide contains the latest info on the Solution, Workgroup Servers 7250/120 and 8550/132, and third parties that support the MacOS platform with e-mail services, server software, authoring tools, and so on.

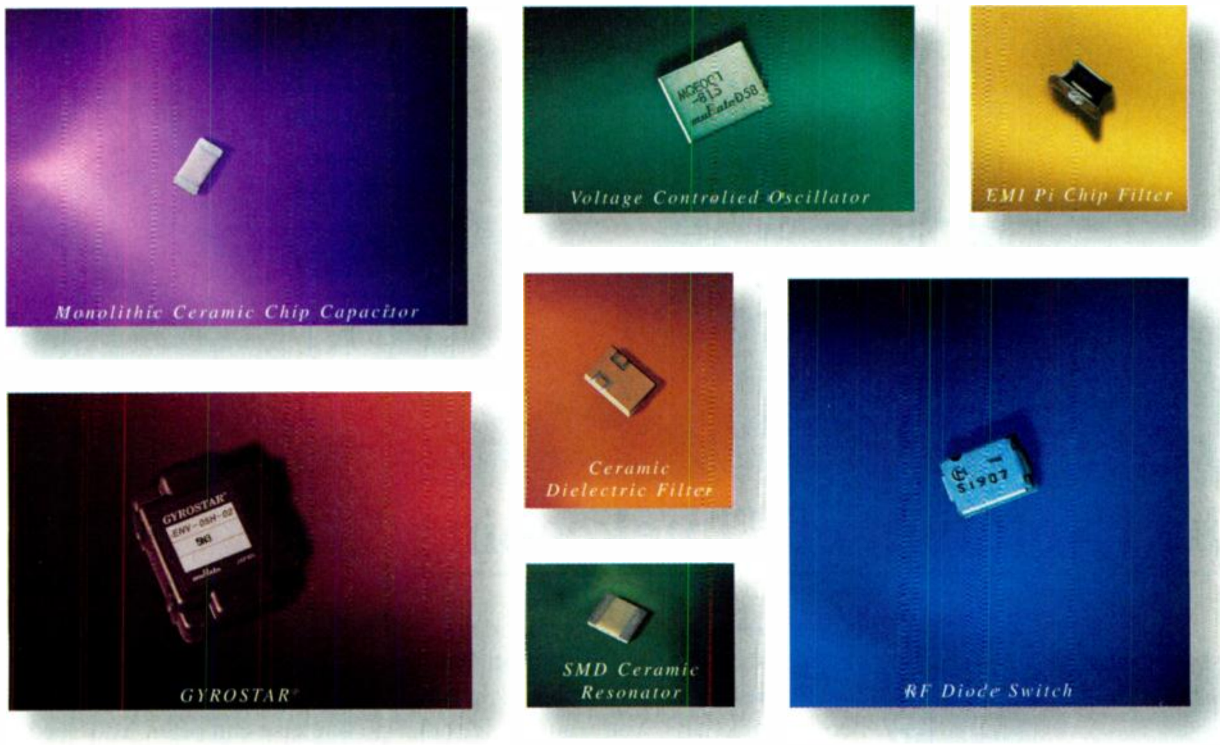
Back To SCHOOL

TECHNOLOGY EXCHANGE Company offers education and training for software developers, engineers, and information technology (IT) professionals. Over 50 courses are offered, including "Network Trouble Shooting," "Object-Oriented Software Engineering," and "Multivendor Networking." Courses are held in various locations around the country, and on-site training is available for companies.

For more information, contact the company at One Jacob Way, Reading, MA 01867; (800) 662-4282; fax (617) 942-3001; Internet: http://www.aw.com/tec.

"Software Testing & Quality Assurance" is a two-day seminar on improving the quality of software, and will show students how to use various tools and strategies to perform stringent software testing based on business requirements. Students also will learn how to correctly document work, and will explore the key features of automated tools that facilitate the testing process. The importance of traceability, walk-throughs and inspections, defect tracking, and other testing procedures will be examined. The seminar will be held in various locations around the country through October.

For more information, contact Data-Tech Institute, P.O. Box 2429, Clifton, NJ 07015; (201) 478-5400; Internet: http://www.datatech.com.



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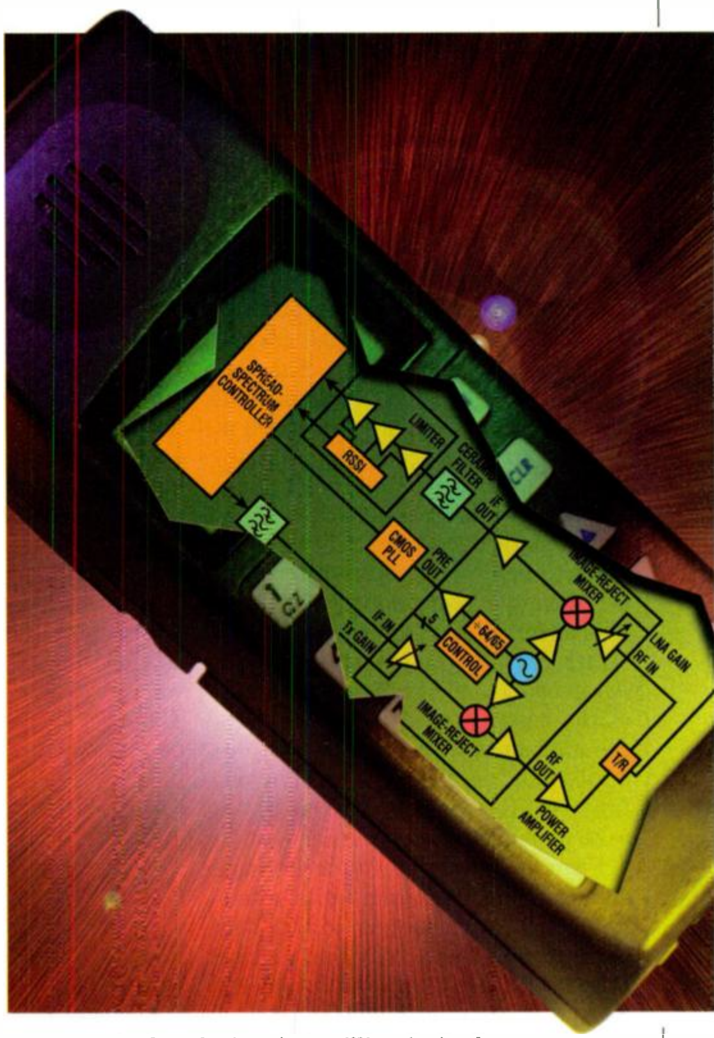
27-GHz Process Makes Unique Parts For RF Transceivers

PAUL MCGOLDRICK

A leading-edge silicon bipolar process, acquired by Maxim Integrated Products from Tektronix, has been developed to produce devices for wireless communications up to 2 GHz with power dissipations of about 100 mW. The process is also capable of producing devices that transmit data over fiber at up to 2.5 Gbits/s, as well as timing circuits for ATE, and high-speed data converters. With a noise corner below 2 kHz, the process is also useful for making phase-locked oscillators.

Textronix's process, GST-2 (Gigaspeed Sampling Technology), is a successor to the earlier GST-1 process successfully used in a line of Gsample/s 8-bit ADCs. GST-2 is a 300% improvement over another in-house process, C-Pi (a recessed oxide-isolated, high-speed complementary bipolar process).

GST-2 is a self-aligned double-polysilicon bipolar process that uses trench isolation. At voltages where wireless products need to operate—around 2 V—the process provides some astounding performance figures. For example, it is capable of an f_t >27 GHz, an f_{max} >28 GHz, BV_{ceo} of 4.7 V, and a B of 200.

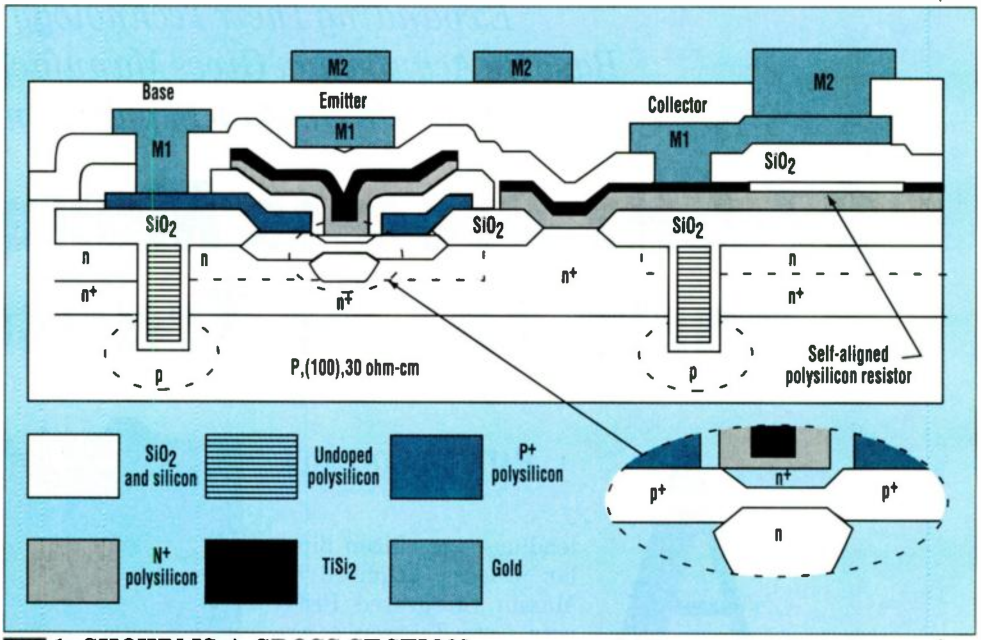


A LOOK BACK

Two years ago, Maxim was looking for ways to increase its fabrication capacity to meet a backlog. The need was for a quick expansion, so they decided to acquire an existing operation. Among other possibilities, Tektronix's in-house fabrication facility was available. Tektronix had been operating the plant as a corporate necessity, producing the specialized ICs and hybrids it needed for its core equipment, but in volumes that it would have been hard-pressed to persuade some other manufacturer to produce. Tektronix also did not want to get into the general semiconductor market and was reported as losing $20 million in its last year of operations.

Maxim not only liked what it saw in terms of the facility, they liked the fact that Tektronix had a process on the back-burner which could quickly get Maxim into the wireless market. The plant (on the main Tektronix campus in Beaverton, Ore.) continues to make the parts that Tektronix needs for its equipment—with new parts to be added—and a joint venture, Maxtek, assembles hybrids for Tektronix equipment. But other changes are dramatic. Instead of handling 4000 wafers per year under Tektronix, the Class-10 fabrication facility now handles 120,000 wafers per year. Apart from duplicating the processes that Maxim has available in its Sunnyvale, Calif. facility, the Beaverton facility also continued the ramp-up of the RF process.

To understand how these performance levels were achieved, it may be wise to focus at how devices are made in the GST-2 process. The cross-section of an npn transistor fabricated with GST-2 shows the substrate to be a p on p^+ epitaxial wafer with a polysilicon film on the backside *(Fig. 1)*. An n-type epitaxial layer is grown on the p^+ and n^+ buried layers, and deep trenches are etched through the n-type epitaxial layer and the n^+ buried layer into the p-type substrate. The trench width is about 0.8 µm and the depth is about 4.0 µm. The bottoms of the trenches are implanted with boron ions and are then filled-in with 0.1 µm of silicon dioxide (SiO_2) film and undoped polysilicon film.



1. SHOWN IS A CROSS-SECTION of an npn transistor made on the Tektronix (now part of Maxim) GST-2 process.

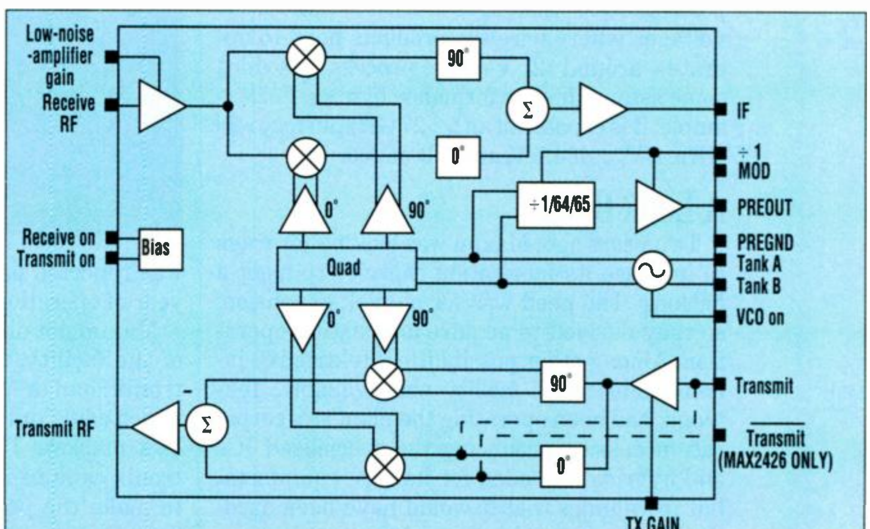
The base island, collector, and substrate contact areas are defined using field-oxidation processes with the collector contact being doped with phosphorus-ion implantation, and the substrate with boron-ion implantation. An amorphous silicon film is deposited as the base electrode and boron ions are implanted with a film of SiO_2 deposited on top. Photolithography defines the base electrode in this layer-cake with a reactive-ion etch.

Firm leakage between the intrinsic and extrinsic base regions is established by the implanting of BF_2 ions through a 0.007-µm oxide film with an acceleration energy of 25 keV. A 0.3-µm SiO_2 layer is deposited and then etched back to form a sidewall oxide spacer.

A selectively implanted pedestal collector layer is implemented by implanting phosphorus ions at 170 keV underneath the intrinsic base region which itself is implanted by BF_2 ions at 25 keV. Then the emitter polysilicon film is deposited after cleaning. This film is dosed to 7 x 10^{15} cm^{-2} with arsenic ions, and a further film of SiO is deposited on top. The arsenic impurities are diffused within the layer at a temperature of 850°C for 30 minutes, then further diffused to form a single-crystal silicon layer using rapid thermal annealing with temperatures between 1025 and 1100°C. This also diffuses the other impurities implanted previously. The rapid thermal annealing process plays an important role in achieving the minimum impurity distributions.

A selective titanium silicide ($TiSi_2$) film is sputtered on top of the emitter and collector polysilicon, but not formed where resistor areas are patterned. This layer forms the self-aligned second polysilicon-layer resistors which are connected directly to the emitter and collector electrodes without the use of contact holes. Using nitrided titanium-tungsten (TiW) as a barrier metal, a 2.4-µm gold interconnect is electroplated on all three terminals. Use of a gold solution provides very high immunity to electromigration.

Tektronix has had extensive experience in the use of gold processes and barrier-metal needs. This is one of the significant differences compared with other technologies, as is the exclusive use of active ions to achieve geometry tightness, the size of the trenches



2. A BLOCK DIAGRAM of the MAX2420 family of transceiver ICs; the MAX2426 transmit-side simplification allows the input of baseband signals to the mixer.

used, the breakdown voltage, and reverse-stress capability, plus the high productivity of the process. Yields, for example, compare well with simpler bipolar technologies.

GST-2 gives the possibility of manufacturing RF ICs, low-noise devices, RF power amplifiers, sheet resistors, Schottky diodes, MOS capacitors and lateral pnp transistors (with f_ts of 80 MHz). The use of trench isolation allows close device spacing and gives high wafer densities.

MAXIM'S GST-2-PROCESS IMAGE-REJECT TRANSCEIVERS

Device	Function	IF (MHz)	Local-oscillator injection
MAX220	Image reject down and up	10.7	High side
MAX2440	Image reject down	10.7	High side
MAX2460	Image reject down and up	10.7	Low side
MAX2421	Image reject down and up	46	High side
MAX2441	Image reject down	46	High side
MAX2422	Image reject down and up	70	High side
MAX2426	Image reject down/BPSK transmit	70	High side
MAX2442	Image reject down	70	High side

Models And Simulation Tools

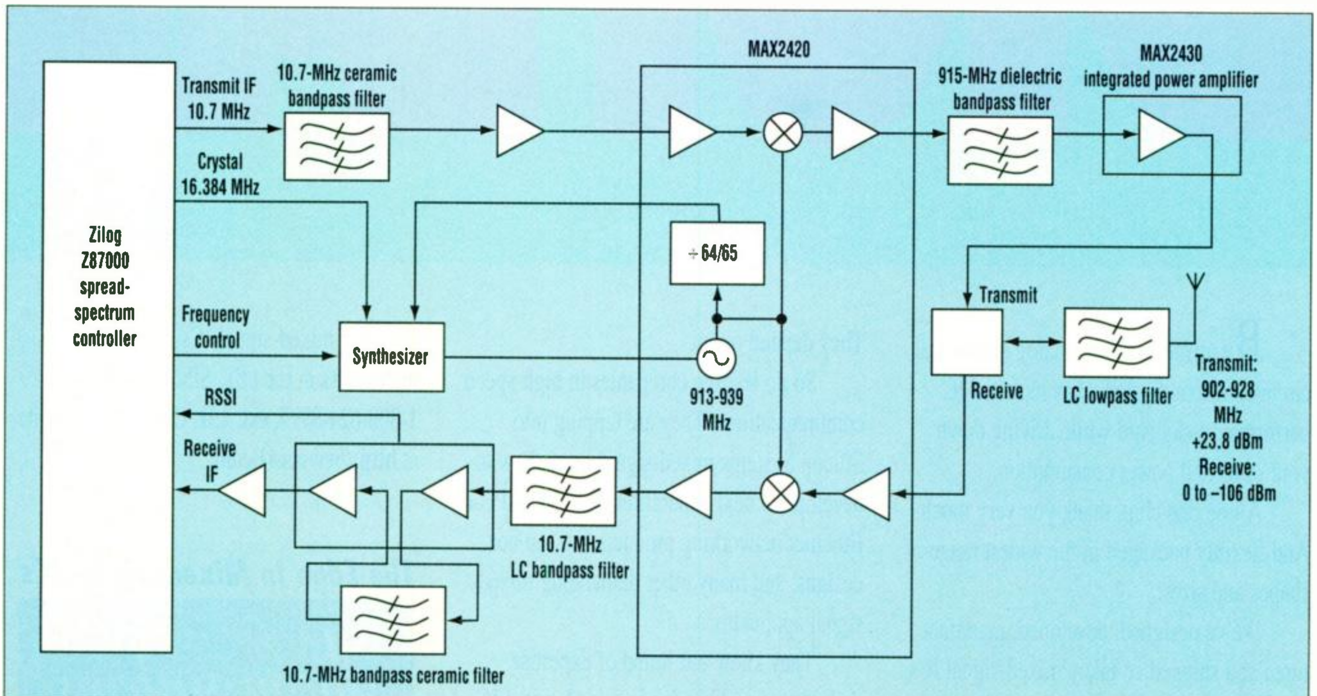
Getting a process to work is only part of the story towards producing useful parts. A significant advantage for the Maxim facility is over fifteen years of Tektronix experience in developing models. TekSpice 2 (compatible with Spice) was developed within the Microelectronics Group and remains part of Tektronix but available to Maxim. TekSpice exhibits an enriched description language and does not suffer the convergence problems commonly associated with Spice. Apart from allowing fast analyses, post-processing and extraction capabilities are included along with Smith-chart and Fourier-transform analyses. A powerful Maxim addition to TekSpice 2 is the electrical rules checker (QuERC) which looks at possible design failures that other simulators ignore. For example, it contains the ability to look at biasing of devices in a region where the model may be inaccurate, points where excessive dissipation in the device or a resistor might cause failure, or errors where ratings are exceeded or not optimized.

In the design process using TekSpice, the intent is to always produce a part that behaves as required—a predictive intention rather than a reflective result; modeling is started early in the design to predict performance and algorithms. All the test patterns are measured and equations are designed from generic models down to the subset levels. There are equations for each application mostly developed by Portland State University professor Paul VanHalen.

The result is a layout system and library that work together to avoid problems in the design of parts that closely match the simulated results. The twenty high-frequency design engineers at Maxim have been empowered by the system, and its browsers, for design guidance, problem solving, and tolerance modeling. For the GST-2 process, the library now contains up to 50 such devices.

The New Family

A new range of ICs, using the GST-2 process, is a family of 900-MHz image-reject transceivers for low-cost radios. Uses will include cordless telephones and base stations, cellular telephones, and wireless data links. The



3. A TYPICAL ARRANGEMENT for the complete transceiver using the MAX2420 and a Zilog spread-spectrum controller.

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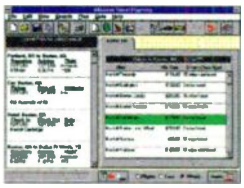

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design intention has been, throughout, to produce parts that absorb into the ICs the most cost-effective solutions for the total product—leaving already low-cost parts outside the chip.

There are vociferous arguments by each manufacturer of these types of products for the inclusion or exclusion of particular features. The Maxim family offers a range to bridge between these different design philosophies. A major requirement of the designs was that the tolerances would be tight enough that no adjustments were necessary.

The result is a range with different IF and local-oscillator (LO) injection choices for conventional and data modulation *(see the table)*. The MAX2420, for example, is an image-reject transceiver with rejection both on the mix up and the mix down from and to the IF of 10.7 MHz. The LO mix on the part is on the high side of the carrier frequency. The same features are on the MAX2460, but there the LO mix is on the low side of carrier. Other versions in the family are for 46- and 70-MHz IFs with simplified up-conversion with no image rejection.

The block diagram for the entire family is similar *(Fig. 2)*. The ICs are designed for 50 Ω at RF and 330 Ω at IF. The receive path consists of amplifier, downconverter, and buffer. The RF signal from the antenna passes to a 900-MHz, variable-gain, low-noise amplifier (LNA), which with logic high on the LNA Gain pin, gives a gain of approximately 16 dB. With logic low, the gain falls to about 3 dB. Intermediate values can also be realized. The LNA has a noise figure of about 1.8 dB at maximum gain.

The downconverter is implemented using an image-reject, double-balanced mixer. An input buffer provides two outputs, each of which is fed to a double-balanced mixer. A quadrature LO drives each mixer. The outputs of the two mixers are passed through RC-phase shifters to produce signals in 90° quadrature which are summed together. The final mathematical relationship is such that the fundamental IF signals are reinforced and the image signals are canceled (see "Image rejection using quadrature cancellation," below). Typical image rejection is about 35 dB. The buffered output appears at the IF pin of the IC. The turn-on/turn-off time of the receiver is a maximum of 1 µs, and the total conversion power gain is typically 22 dB.

The transmitter side of the chip operates in a similar fashion. The IF is applied to the Transmit pin and passes through a buffer amplifier with about 30 dB gain adjustment controlled from the Transmit Gain pin. This is for products where the manufacturer wants to control output power when the transceiver is in close proximity to the base station. The signal is then split through RC-phase shifting to give quadrature signals at the double-balanced mixers that are fed with quadrature LO signals. Again, the mathematics reinforce the fundamental carrier signals and cancel the image signals. The image rejection is about 35 dB while the LO leakage to the output is about –35 dBc. The output is fed through a pre-driver to give a maximum signal level of about +3 dBm. Turn on/turn off time of the transmitter is a maximum of 500 ns.

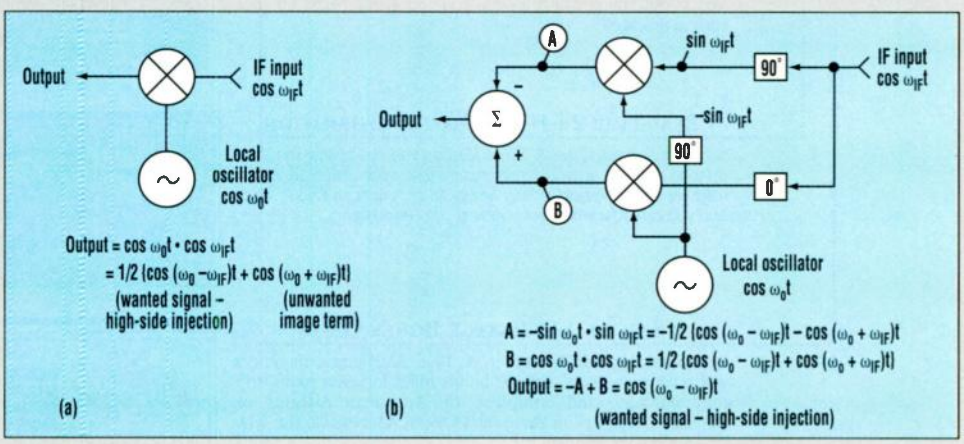
Oscillator Sections

The on-chip LO is formed by an emitter-coupled differential pair. An external LC-resonant tank circuit connected to TANK A and TANK B sets the oscillator frequency *(Fig. 2, again)*. Part of the tank capacitance can be split with back-to-back varactors with the common terminal becoming the dc feed point to create a voltage-controlled oscillator. If needed, the LO can also be overdriven from an external source; in that case a drive level of about –3 dBm from 50 Ω should be ac-coupled to either tank pin.

The on-chip prescaler provides the link for a PLL to the oscillator. There are two different modes controlled by the *Divide-by*1 pin. When this is low, the prescaler is in the dual modulus divide-by-64/65 mode. When it is high, the prescaler is disabled and it becomes an oscillator buffer-amplifier with an output of about –6.5 dBm into 50 Ω. When the prescaler is active, the choice of 64 or 65 as a division ratio is made by the Mod pin being high or low, respectively. The choice allows for an intelligent choice in the locking window of a lower-frequency PLL. A

IMAGE REJECTION USING QUADRATURE CANCELLATION

A simple mixer is the multiplication of the signal and the oscillator applied to it. The resulting output is a combination of the wanted signal and an image term separated by twice the IF. Shown here is the mixer in an upconverter role *(see the figure, a)*. The same upconversion using the system employed in the Maxim MAX2420 family with balanced quadrature modulators, results in two separate mixes with the image terms in each being of opposite polarity. The summation of the two signals results in cancellation of the unwanted image signals *(see the figure, b)*.



number of low-cost synthesizers are available at the approximately 16.4 MHz required for carrier frequencies of 902 to 928 MHz.

The remaining components not on chip for the completion of a transceiver include the IF strip—available at low-cost—and the IF filters (very low cost), the baseband system of choice (such as from Zilog, Cylink or Rockwell), and at the antenna end, the transmit/receive switch (not suitable for design as a CMOS product at low power), and any additional power amplification wanted for the transmitter. A suitable IC is available for this position from Maxim, the MAX2430, which delivers 20 dBm from a 3-V supply. The arrangements of a complete system for a 240-mW (+23.8-dBm) output and a receiver with a sensitivity range of 0 to –106 dBm are for a supply rail of 4.7 V using a Zilog spread-spectrum controller, the Z87000 *(Fig. 3)*.

Power Management

A critical component of any IC designed for portable applications is the device's power management. In the MAX2420 family, the receiver and transmitter have their own enable inputs, $Receive_{on}$ and $Transmit_{on}$, so that the receiver functions can be disabled during transmission and vice versa. As transmit and receive share common LO and IFs, it is recommended that this facility be used in any case to avoid interference across the paths. Parts of the oscillator circuitry can also be shut off if they are not required. In a normal configuration, using the prescaler and oscillator, the receive mode will require about 35 mA from a 3.3-V supply and the transmit mode would be about 36.5 mA. A shutdown mode is available where the current drawn is less than 1 µA. □

Price And Availability

The MAX2420 is supplied in a 28-pin SSOP package with pricing at $4.49 in quantities of 1000. Samples are available immediately.

Contact Hans Dropmann, Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA; (408) 737-7600; fax (408) 737-7194.

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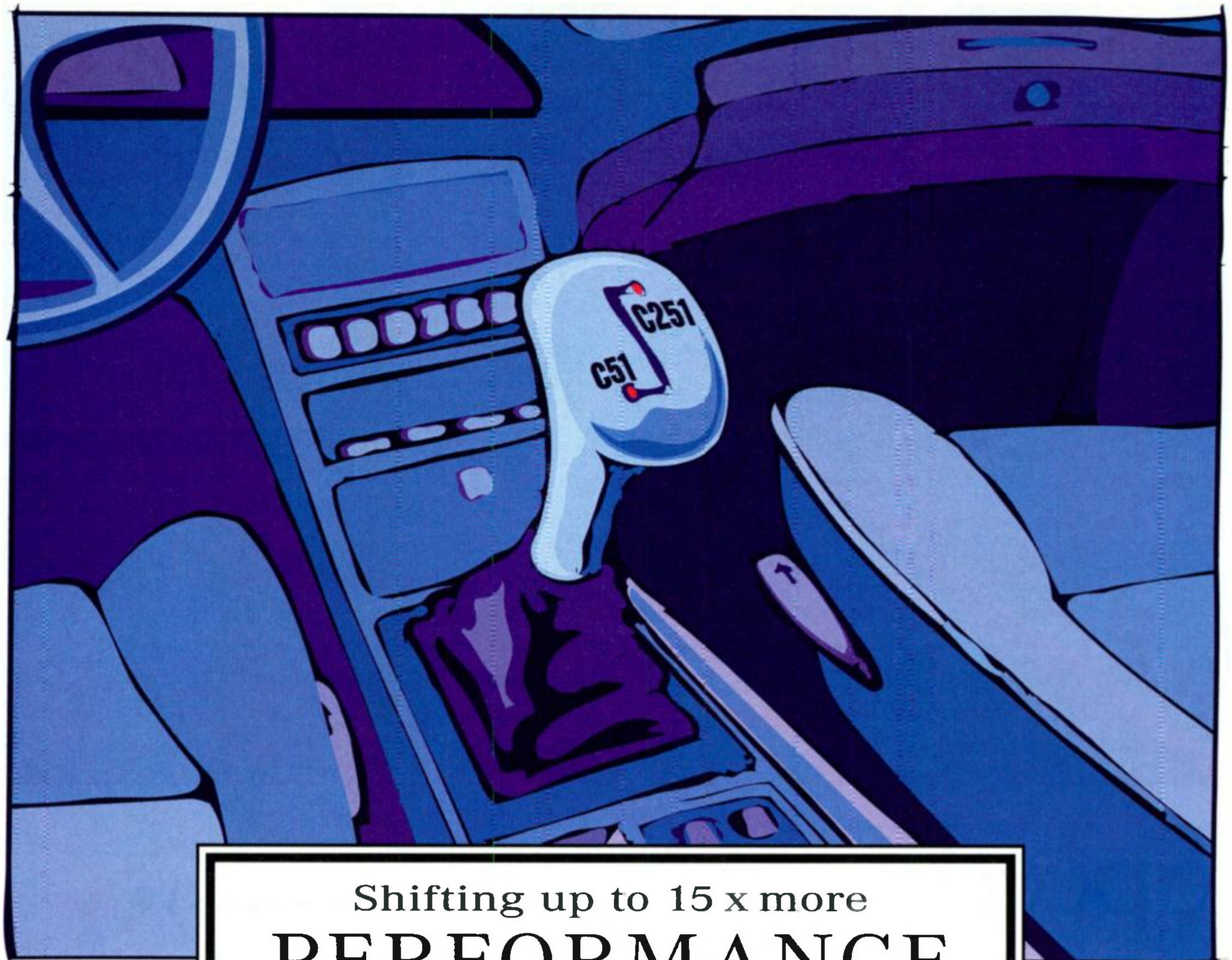

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HIGH-LEVEL DESIGN

EDA Vendors Advance Toward System-Level Design

A Major Factor Driving The Adoption Of System-Level Methodologies Is The Price Of High-Level Errors.

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The following report features contributed articles from three major electronic design automation (EDA) vendors active in the development of tomorrow's system-level design solutions. All three perceive that the number of design starts in telecommunications, multimedia, and digital signal processing (DSP) are dominating today's ASIC landscape. These ASICs are increasingly complex, highly proprietary, and must operate at extreme frequencies. And even though the time to market is continually shortening, design teams are becoming smaller as well. It seems that the pressure on the engineer can only be relieved through next-generation system-level design methods.

A major factor driving the adoption of a system-level design methodology is the high price of errors made during the high-level design phase. When the requirements are being captured, the functional specification is created, and the appropriate architecture is selected. These errors create major problems in meeting the schedule, because they are only detectable during the integration and test phases that occur much later downstream.

Problems with today's methods

The conventional design methodology separates hardware and software design into two fairly independent paths that are not reunited until quite late in the design process at the integration and test phase. If there are problems at this point, the time-to-market pressures often force a last-minute integration solution that's focused on software, even though that type of fix may not be the best solution. The long lead times and high cost of ASIC design turns often indicate that a software fix is the only viable alternative, but the true cost of a software solution may actually be quite high, because it may compromise the final product's functionality and performance.

Next-generation methodology

To enable system-level design, a new generation of hardware/software codesign tools will be required. In these articles, Mentor Graphics calls their approach integrated system design, Cadence promotes the notion of block-based design, and Synopsys focuses on behavioral synthesis. But all three companies are looking at ways to move the design process to a higher level of abstraction and deal with reusable blocks of intellectual property, such as embedded cores.

To fully realize the potential benefits of block-based design, the EDA industry is in need of new design and delivery standards for intellectual property (IP). These standards will facilitate the evaluation of predesigned components and their subsequent integration into formalized design flows and different design-automation environments that extend from system-level design through silicon implementation. End users must be capable of combining blocks from many different providers and standardize on a unified internal design flow. Standards will make it easier for component IP providers to support multiple EDA design flows without requiring separate design kits for each. Standards also are needed for increased levels of intellectual property protection.

Integrated systems design

In integrated systems design, the two separate hardware and software design flows are in constant communication throughout the design cycle, so that the system-level view is continuously observed throughout the design cycle. Mentor Graphics' concept of the integrated system design methodology is divided into two main parts. First is the requirements/specification phase, where the goal is to create a design that is functionally correct. Specification and architectural errors can be quickly detected and remedied before they impact the later stages of design. After this process, the hardware and software can be implemented according to clearly defined parameters.

The second part of integrated system design is the process of continually validating the interaction between the hardware and software design activities. A "virtual prototype" is constructed during this phase and is integrated and tested via simulation and/or system emulation. The virtual prototype reveals any design errors before they are compounded as the project moves forward.

By resolving conflicts early in the hardware/software design phase, engineers can achieve significant productivity gains. But they can realize even more gain if the errors are resolved during the specification and partitioning phase.

Block-based design

Cadence points out that another primary enabler for system-level design is the notion of reusable blocks of intellectual property. With a block-based design methodology, the user performs architectural design by placing the functional blocks. The designer then rapidly evaluates the interaction of a specific block with other blocks in the system and its operating environment. For each IP alternative that meets the system functionality and performance requirements, the user leverages pricing and IP characterization data to rank each piece of IP for cost and power.

As a specification evolves into a chip architecture, floorplanning is performed to meet timing budgets and routing requirements. Floorplanning tools must be closely linked to process-specific layout tools to identify potential routing problems early in the design process. For blocks of custom functionality, partitioning tools are used to break down larger blocks into appropriate types and sizes for lower-level block design.

Libraries of parameterized elements accelerate the time required to produce an efficient, working deep-submicron implementation. Taking advantage of these regular structures saves tremendous time in capture, functional verification, management of critical paths, clock and power distribution, and floorplanning and physical design. In addition to the time savings, these parameterized elements greatly improve the efficiency of implementations.

Behavioral design

Synopsys is making a substantial effort among its user base to raise productivity by elevating the design abstraction from the register-transfer level (RTL) to the behavioral level. Behavioral design enables much faster creation, verification, and modification of complex designs using high-level specifications. It allows designers to quickly create and evaluate multiple architectures by simply changing the high-level constraints. After making high-level trade-offs, a behavioral synthesis tool automatically creates a fully optimized gate-level design.

Behavioral synthesis represents a major shift in methodology for RTL designers. This new process of designing at a higher level of abstraction may be painful and frustrating without the right preparation. But according to its early adopters, behavioral coding is more intuitive, and it facilitates fast design creation and debugging. After investing a short period of time to become proficient at writing behavioral code, a designer can achieve dramatic advances in productivity.

With behavioral synthesis, designers do not need to specify registers because it automatically creates them to accommodate scheduling. Instead, behavioral designers must become familiar with nonblocking (signal) and blocking (variable) assignments. That is, output assignments should be made using signal assignments, and all other operations are handled using variable assignments. A behavioral synthesis tool is free to move designated operations by using variable assignments across clock boundaries in order to optimize for operators and register utilization. Signal assignments, on the other hand, explicitly infer registers in a manner similar to RTL.

New verification methods

Once basic system functionality is established, the designer must verify that all possible interactions between large blocks of IP have been fully tested. Because the vast majority of ASIC errors occur at the interfaces between hardware blocks, and that most system errors occur at the interfaces between hardware and software, interface verification becomes critical as entire systems are put onto a single chip. The problem is the fact that it takes billions of cycles to fully verify this much functionality when using logic simulation.

Therefore, alternative strategies such as modeling at higher levels of abstraction and virtual prototyping must be employed to get around the verification bottleneck. Any valid approach to an integrated systems methodology must bridge the gap between hardware and software simulation environments, and create a bidirectional information flow that benefits the design teams on both sides.

In the conventional scenario, the hardware and software designers each employ simulation tools to exercise and verify their respective functionality and performance. However, both domains are virtually

independent from each other. Software designers have debugging tools that exercise their code, but the portions of the code dealing with hardware I/O are usually represented by primitive routines that return and retrieve only minimal information. The software design can be viewed in terms of the three types of code used in most embedded systems—the application program, the real-time operating system, and the firmware that interacts directly with the target system hardware.

Hardware designers use logic simulators that are strongly oriented toward timing and logic verification, and employ various methods that present a very limited approximation of software's impact on the target system's bus. Hardware logic simulators are capable of dealing with the basic bus cycles presented by microprocessor operations, but can't offer the performance needed to evaluate significant amounts of code execution. The problem is compounded by the immense complexity of full-functional microprocessor models.

For true hardware/software codesign to become a reality, it's necessary to reconcile the performance differences between instruction set simulators and hardware logic simulators, and to provide an orderly exchange of necessary signal information between the two. Clearly, the performance bottleneck is on the hardware simulation side. Even when freed of the burden of microprocessor modeling, hardware simulators are much more limited in their throughput than software simulators.

A potential solution lies in the fact that there are a relatively high ratio of total processor instruction cycles compared to the number of I/O bus cycles on the target hardware. If non-I/O bus transactions can be filtered out of the total number of clock cycles, the number of cycles presented to the hardware simulator can be substantially reduced, and overall simulator throughput can be significantly increased by several orders of magnitude. Once this hardware/software bridge is established, the first major step in the integrated systems design methodology will be achieved.

Then, for the first time, a system-level virtual prototype will exist throughout the hardware/software design flow. Software designers will be able to detect hardware-related bugs early in the design cycle, when they are relatively easy to fix. Hardware designers will get a much truer picture of their design's performance and functionality, and can quickly identify ways to optimize it. Most importantly, both hardware and software errors will be found and repaired before the integration and test stage, and before they become a major obstacle to the product's quality, cost, and schedule.

Verification of complex systems is accelerated by the use of system-level (functional) modeling and simulation techniques. The models written at this stage may not be cycle-accurate with respect to the final implementation of this system, but they can be quickly simulated.

Because the designs are written at a high level of abstraction, they do not reference the low-level implementation details, and they do not refer to as many clock cycles as may exist in the final implementation. Behavioral designs are also much quicker to simulate, because behavioral code consists of only 10 to 20% of the number of lines of code in an RTL design. ☐

Rita Glover is President of EDA Today, a market research firm in Phoenix, Arizona, that provides market analysis and consulting services on electronic design automation issues. A 14-year veteran of the EDA industry, she has worked as a technical communications consultant, technical writer, courseware developer, and instructor of EDA tools. Comments can be e-mailed to ritag@edat.com.

Making the shift toward integrated systems design

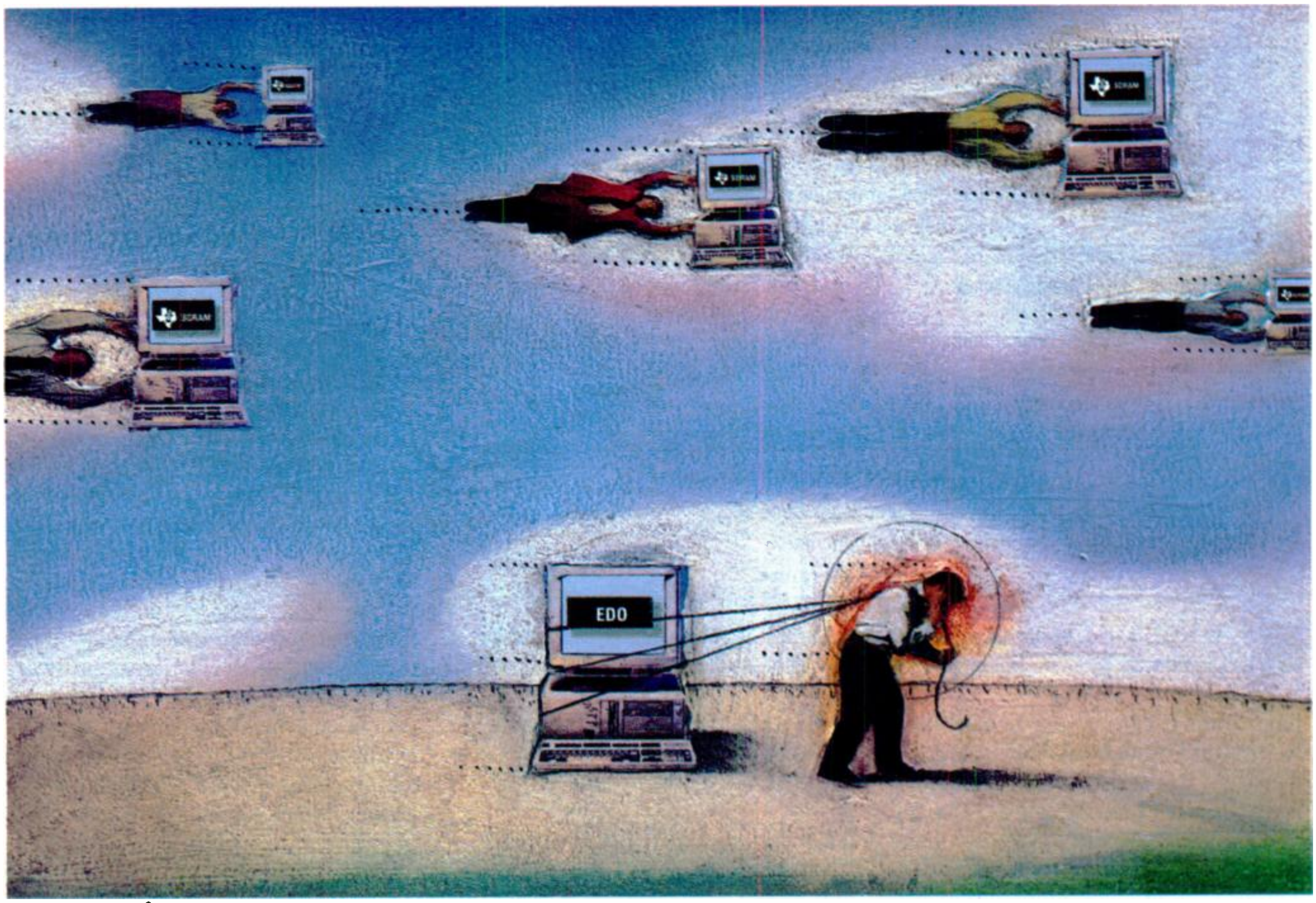
Hardware and software design flows must be in constant communication.

BY BRIAN BAILEY AND SERGE LEEF, Mentor Graphics Corp.

As the size and complexity of electronic systems continue their inexorable climb, many engineering organizations are feeling the wear and tear from conventional design methodology. The conventional methodology separates hardware and software designs into more or less independent paths, and then reunites them at the integration and test phase. An alternative approach is found in integrated systems design, where these two basic design flows are in continuous communication throughout the design cycle. But a new generation of hardware/software codesign tools will be required for this methodology to become reality.

One factor driving the adoption of this new methodology is the high price of design errors made early in the cycle—errors that only surface during the integration and test phases, where they become major obstacles to meeting schedules. Errors of this kind are typically introduced in the system-design phase, when the requirements are being captured, the functional specification are created, and theappropriate architecture selected.

At the beginning of the system-design phase, the design is often specified as a series of functional blocks interconnected in a manner that represents the symbolic dataflow between them. This functional specification is then partitioned into an architecture composed of hardware and software components. During this



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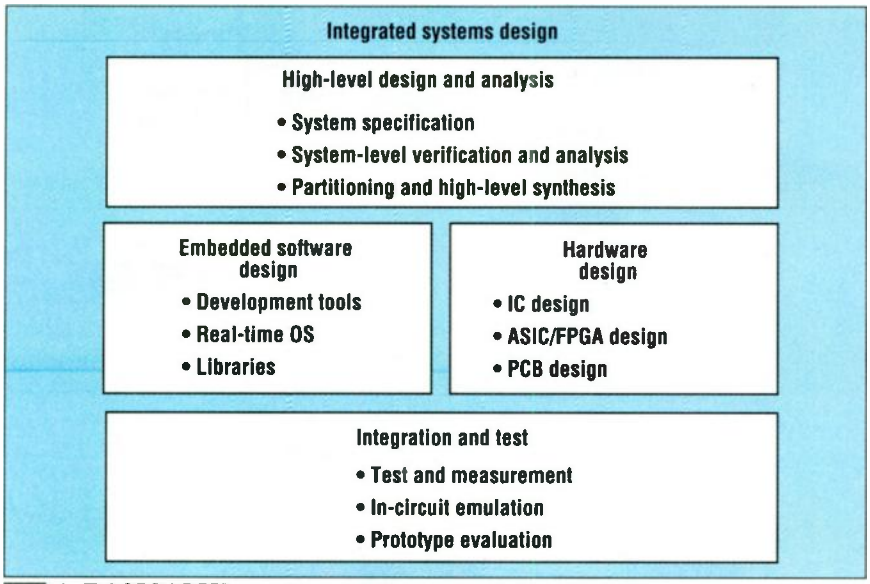

1. BASICALLY, the design cycle tends to fall into four separate phases—system definition and partitioning, hardware implementation, software implementation, and integration and test.

partitioning process, particularly when tools are not available to assist the designer, it often becomes difficult to keep the hardware/software boundary defined in a way that accurately maps back to the functional specification. These system-level ambiguities can cause major problems during the integration and test phase, when the true magnitude of up-front mistakes becomes apparent. For this reason, up to one-third of the typical design cycle is spent in the integration and test phase.

In many instances, the time-to-market pressures force last-minute integration solutions that focus on software, even if it is not the optimum solution. The long lead times and high costs of ASIC design turns make software seem like the obvious choice, even though the true cost of a software solution may be quite high when it is examined closely. For this reason, the bias toward remedial action in software may compromise the functionality and performance of the final product.

This basic problem is only amplified by current trends in the development of electronic products. Many new systems employ custom hardware in the form of ASICs with hundreds of thousands of gates, and software that may include a complete real-time operating system (RTOS), plus over a million lines of C or C++ code. At the same time, the ratio of hardware to software engineers has reversed in the last decade, reinforcing the growing role of software as a significant factor to the value of new products.

Resolving Conflicts

The practice of integrated system design promises to solve these problems by ensuring that the system-level view is continuously observed throughout the design cycle. At the front of the cycle, specification and architectural errors can quickly be detected and remedied before they impact the later stages of design. And once hardware and software designs commence, the interface between them can be continually validated. Studies show that the resolution of conflicts early in the hardware/software design phase yields significant productivity gains. They also show even more gain if the errors can be resolved during the specification and partitioning phase.

Basically, the design cycle tends to fall into four separate phases *(Fig. 1)*. The first phase is system definition, which includes requirements definition, functional specification, system-level validation, and partitioning into hardware and software. Once the partitioning into hardware and software specifications is complete, the actual hardware and software implementations can begin. Subsequently, they proceed on independent paths, sharing no milestones until prototype hardware is built. Finally, during the integration and test phase, the software is executed on the target hardware and ensures that the design works as originally intended.

In the future, the first phase of the design cycle will evolve to the point where designers can create an executable specification that's partitioned into hardware and software descriptions, which are then synthesized using commercially available tools. But in the current time frame, there's little interaction between the specification and the downstream phases. There's also little, if any, interaction between the software and hardware implementation phases. As a result, the bulk of the work done in validating the hardware/software interface is put off until integration and test.

The immediate remedy for this problem is an integrated system design methodology that actively employs hardware/software codesign, so there's a continuous reconciliation of hardware and software throughout the design cycle. In this manner, inherent conflicts within the design are revealed earlier in the process, and the integration and test phase—which currently consumes up to one third of the cycle—is reduced to an absolute minimum.

The integrated system design methodology can be divided into two parts. One is the activity performed in the requirements/specification phase. The goal here is to create a design that is functionally correct, and to implement the hardware and software within a well-defined boundary between them. The second part is the interaction between the hardware and software design phases. This part of the methodology allows the construction of a "virtual prototype," which can be integrated and tested via simulation to reveal design errors before they compound as the project moves forward.

The development of technology to address the requirements/specifications phase is the subject of intense research and development in both the electronic design automation (EDA) industry and academia. But as of now, there are no comprehensive solutions. However, the creation of a virtual hardware/software prototype to support the design phase is much closer to realization, and will consume the balance of this article.

Bridging The Gaps

In the conventional scenario, both the hardware and software domains employ simulation tools to exercise

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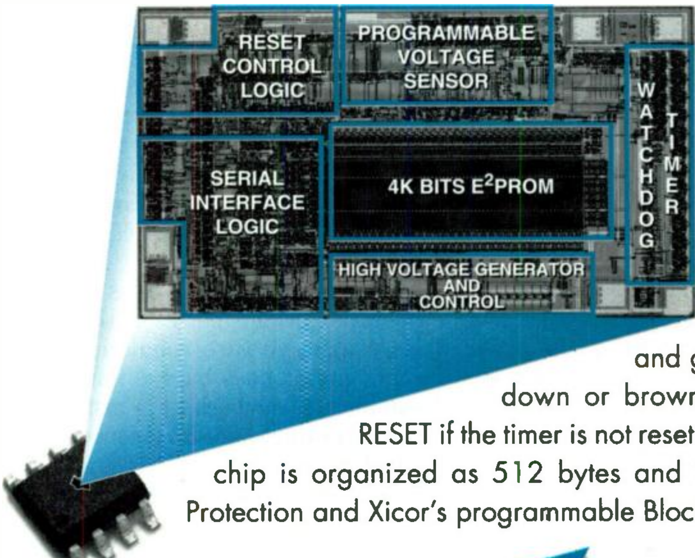
New Product and Applications Information for Design Engineers

8051 μC Supervisory Circuit Combines Reset Controller, Programmable Watchdog Timer and E²PROM



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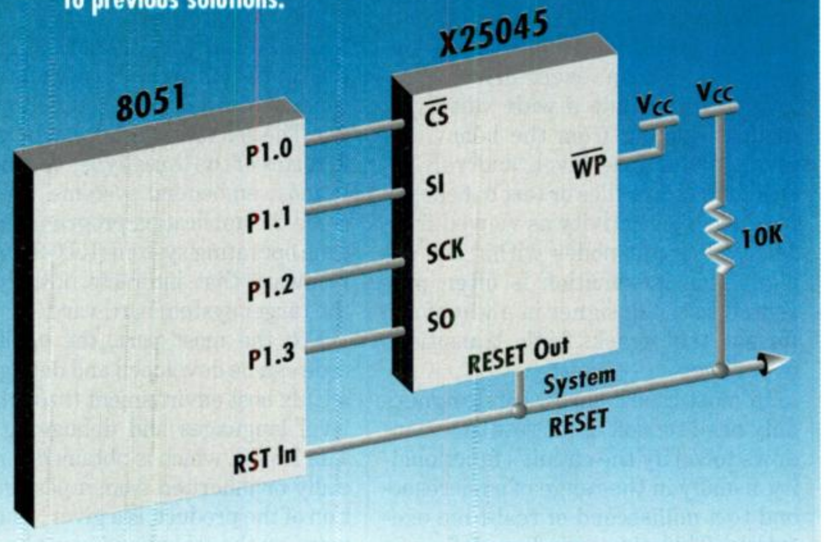

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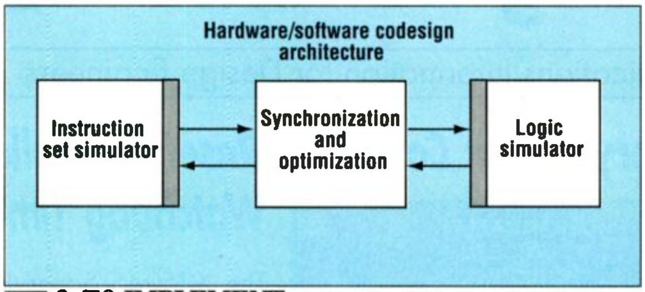


2. TO IMPLEMENT true hardware/software codesign, it's necessary to reconcile the performance differences between instruction-set simulators and hardware logic simulators, and also to provide an orderly exchange of signal information between the two sides.

Obviously, any valid approach to an integrated systems methodology must bridge this gap between hardware and software simulation environments and create a bidirectional information flow that benefits both design teams. To understand the specific requirements of this co-simulation environment, it helps to take a closer look at the specifics of software and hardware simulators.

The capabilities and performance of contemporary hardware logic simulators are well-known and widely understood. These event-driven programs can include a wide variety of models ranging from the behavioral level to the gate level, and rely on stimulus vector files or test benches to produce logic activity as viewed from selected circuit nodes within the design. This information is often presented to the designer in a waveform format that tracks logic transitions over time.

In most cases, hardware designers only need to look at narrow time windows to verify the circuit's functionality, usually in the range of a microsecond to a millisecond of real-time execution. This time window defines a level of hardware simulation performance that's adequate for most tasks, and is approximately seven orders of magnitude less than real time. For example, when simulating a 100-MHz target system, a simulator could evaluate 10 clock cycles/s. At this rate, a millisecond time window would require 2.7 minutes.

At this level of performance, hardware simulators are capable of dealing with the basic bus cycles presented by microprocessor operations, but simply do not offer the performance needed to evaluate significant amounts of code execution. The problem is compounded by the immense complexity of full-functional microprocessor models. In a typical scenario, a logic simulator can evaluate approximately one instruction per second. Even though the boot routine for a typical product might consume several seconds of real-time execution, and may simultaneously produce many millions of instructions, the magnitude of the problem becomes readily apparent.

On the software side of design flow, the simulation and validation process is conducted in a somewhat different manner. The software design can be viewed in terms of the three types of code used in most embedded systems. These include the application program, the real-time operating system (RTOS), and the firmware that interacts directly with the target system hardware.

For the most part, the application code can be developed and debugged in a Unix host environment through high-level languages and debugging tools. The RTOS, which is obtained commercially or inherited from a past generation of the product, is a given. The firmware, on the other hand, must be examined and debugged in terms of actual instruction-set execution on the target microprocessor. This is usually done through instruction-level software simulation, which makes no attempt to fully model the internal circuitry of the target processor or the surrounding hardware.

One approach to this microprocessor-level software simulation method is the compiled-code method, also known as native-code simulation. First, the embedded source code is compiled to the host CPU rather than the target. Then, as it executes on the host, all the I/O operations are trapped and made to exercise a bus-functional model that's integrated in the target system. This I/O activity is converted to the appropriate bus cycles which exercise the target hardware.

While this approach does create a potential bridge between the hardware and software simulation environments, it does have a number of significant drawbacks. For instance, it can only utilize high-level source code, which rules out the use of commercial RTOS and legacy software libraries of target-specific machine code. It also presents a distorted view of real-time software execution as the processor state and timing information are abstracted away, and the host execution rate is often radically different than the target rate.

EXCHANGING SIGNALS

A second approach is instruction set simulation, which models all the major storage elements and instruction-level behaviors of the target processor but abstracts out the internal circuitry. This model provides register-level information about the target processor's internal state. A companion bus-interface model can be used to add bit-level accuracy to represent activity on the processor's interface pins as seen by the target hardware. Some instruction-set simulators are cycle-accurate and will produce the exact bus behavior that will occur in the physical system. This kind of simulator is a tool that can be bridged to the hardware simulation domain so the specific nature of the interaction between hardware and software can be examined.

To implement true hardware/software codesign, however, it is necessary to reconcile the performance differences between instruction-set simulators and hardware logic simulators. It is also necessary to provide an orderly exchange of necessary signal

information between the two sides *(Fig. 2)*. Clearly, the performance bottleneck is on the hardware simulation side. Even when freed of the burden of microprocessor modeling, logic simulators are limited in their throughput capabilities. This compares to upwards of 100,000 instructions/s on the software simulation side.

Note that the high ratio of total processor instruction cycles compared to the number actually devoted to I/O bus cycles affecting the target hardware points toward a potential solution. If one takes the total number of clock cycles and selectively filters out non-I/O bus transactions, the number of cycles presented to the hardware simulator is substantially reduced, and the overall simulator throughput is significantly increased. This includes filtering all activity associated with instruction fetches and memory read/writes to unimportant locations.

With this kind of filtering in place, the hardware simulator would only see bus-level stimulus directly associated with the hardware I/O, and all the intervening bus traffic could be removed from the simulation. The net result is to boost overall simulation performance by several orders of magnitude.

Once this hardware/software bridge has been established, the first major step in the integrated systems design methodology has been achieved. On the hardware side, the functional specification is first expressed as a behavioral model using VHDL or Verilog to construct an executable version of the circuit design. This model can then be used on the software simulation side to represent I/O operations that are associated with the firmware portion of the target software. In the second phase of the design, the hardware is expressed in a more detailed register-transfer-level (RTL) of VHDL. This model can be interfaced with an instruction-level software simulation of the activity on the bus of the target system. In the final phase, the VHDL is synthesized to a gate-level hardware description.

For the first time, a system-level virtual prototype now exists throughout the hardware/software design flow. Software designers can now detect hardware-related bugs early in the design cycle, when these bugs are relatively easy to fix. Hardware designers can obtain a much truer picture of their design's performance and its functionality and can quickly identify ways to optimize it. Most importantly, both hardware errors and software errors are encountered and repaired before the integration and test stage, when they become a major obstacle to keeping a project on schedule. ☐

Brian Bailey and Serge Leef both work in the Codesign Business Unit of Mentor Graphics Corp., Wilsonville, Ore. Bailey, who is chief technologist, can be reached by phone at (503) 685-1371 or by e-mail at brian_bailey@mentorg.com. Leef is the director of research and development. He can be reached at be phone at (503) 685-7000 or by e-mail at serge_leef@mentorg.com.

Block-based design: creating a system on a chip

Traditional methodologies don't meet the needs of building systems on a chip.

BY PHILIP GEORGE, Cadence Design Systems Inc.

Deep-submicron technology delivers access to five million usable gates built with 0.35-µm geometry. Moore's Law indicates that this capacity will continue to double in complexity every 18 months. From the semiconductor vendor's point of view, the maximum dollar/wafer can only be achieved by producing complex systems on chips. In addition, end-product life cycles are shrinking and causing many of these products to reach a commodity pricing phase sooner, thus reducing the profit margin possible. This, in turn, puts greater pressure on the design team to innovate more complex products in less time at lower costs.

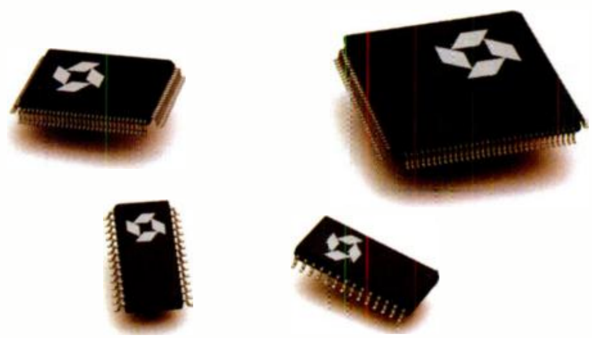
From the system house perspective, the required combination of time to market with competitive price/performance can only be achieved by developing complex systems on chips. So, for the first time in the industry, the business requirements of the semiconductor industry align perfectly with the business requirements of the system houses.

Just as we have seen trends of transistors becoming Boolean gates, adders, and multiplexers, we now see digital-signal-processor and microprocessor cores, sophisticated protocol decoders, and filters becoming available for use in one chip. What was once simply an ASIC of synthesized control logic is now quickly becoming a complete system on a chip. Unfortunately, traditional design methodologies have not kept up with the unique requirements of building systems on a chip. Consequently, virtually every electronics company in the world is struggling to find the right formula for success in this area.

Future system-on-a-chip designers must evolve from traditional top-down or bottom-up design methodologies to block-based design. Block-based design is founded in principle on the mixing of blocks that are represented at multiple levels of abstraction, described in any language (such as C, C++, VHDL, or Verilog). These blocks describe either hardware or embedded software.

Today, block-based design is quite error prone, time consuming, and resource intensive, thereby posing a threat to the growth and profitability of this market. However, the key to success is a formalized method for developing, accessing, and integrating intellectual property *(Fig. 1)*.

Bottleneck.



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New products designed today are generally developed in three distinct phases: System design, hardware/software architectural design, and hardware/software implementation. System design is performed in a variety of ways. One methodology for system design can be a paper specification describing the system algorithms proven through mathematical formulas and black magic. This paper specification is then given to design architects who decide on many of the critical hardware and software elements, usually based on past experiences and instinct. Descriptions usually include the selection of the processor, the memory size, and the refinement of the interface protocol between elements.

The first sign of automation in this paper-spec methodology is found when the implementation team translates the paper specification to a block-diagram schematic, which is then partitioned to the team members. While some engineers begin drawing the schematics for the larger components, others are writing Verilog or VHDL to define the special control functions of the system. Meanwhile, software engineers develop software-dataflow charts, and then write embedded software for the processor or higher-level system software. Of course, they must wait for the hardware to begin testing. This design flow takes a very traditional approach to the high-level design phase, but with no electronic connection to the implementation phase.

A second methodology starts at the highest-level algorithmic design (both hardware and software algorithms), which is accomplished through C programming. System environmental models, design functions, interface protocols, and communication standards are written in a combination of C, C++, and even Fortran (with a C wrapper). An essential part of this step is the design of the stimulus input module and an expected results comparator in order to effectively test the system model (the C program).

This second methodology offers some automation and a fairly rigorous testing process. Once again, a paper specification is given to architectural designers to decide on the hardware and software elements. Some of the C models designed in this phase can be used in software design as well as for development of an accurate IC testbench by hardware engineers.

Finally, a third methodology leverages a formalized design-automation environment to provide the algorithmic designer with a library of application-specific functions (typically coded in C or C++) and a variety of environmental and stimulus-creation building blocks in order to test the system algorithms and architecture. A common example might be the use of pre-packaged library elements to represent the behavior of a set-top box, specifically the audio and video compression functions. The input signals would also be modeled to include realistic effects of noise or distortion.

Once completed, unambiguous specifications of the design and test suites for verification can be extracted, formatted, and generated in standard formats (Verilog, VHDL, print on change for vectors, etc.). With this approach, the implementation team can automatically leverage the work of the high-level systems designers to both improve productivity and reduce design risks.

Need For Change

There are two key aspects of the system-on-a-chip design process that require change in design methodology to successfully overcome the daunting market challenges. The first is the process of formalizing the algorithmic and architectural design phases, so that this information will become a fully-executable specification for the implementation team. Second is the departure from using a traditional register-transfer-level (RTL) synthesis flow to define the entire functionality of an ASIC.

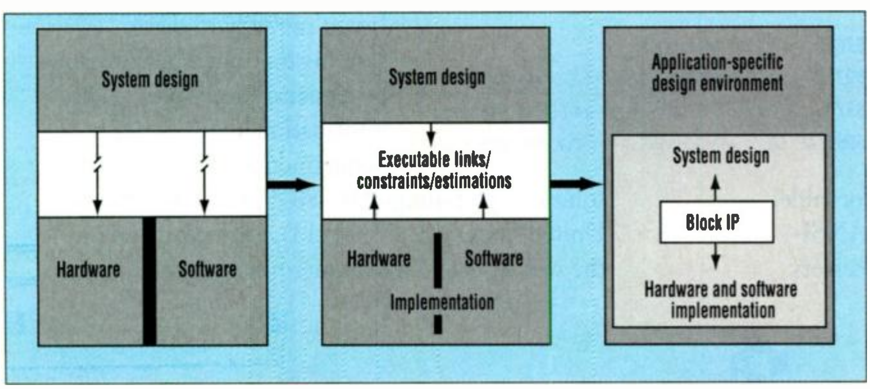
No longer can everything on the silicon be designed through synthesis. This is especially true considering that it's becoming less feasible to produce multimillion-gate designs within the tight schedules demanded by system houses. A multimillion-gate, deep-submicron chip designed using a traditional ASIC approach would take years instead of months to develop. Therefore, a new methodology and supporting infrastructure is needed.

If the next-generation product must be 30% lower in cost to design, 50% smaller to consume less power, have 100% higher performance, and be designed in half the time—then there is a need to design with as many predictable and pre-verified blocks as possible. Design reuse must really mean reuse of nearly complete blocks that can be quickly integrated while being continuously verified at all levels in the context of the system application environment *(Fig. 2)*.

Block-Based Design

Block-based design is the methodology for designing complete systems in silicon with first-time success. It requires access to a wide variety of standard intellectual property (IP) models that can be quickly composed and verified in the context of a system description. IP can be internally developed for design reuse, or provided by ASIC and IC vendors, or by other third-party developers.

Users first place functional blocks in an architectural design and quickly evaluate the functional interaction of a specific block with other blocks in



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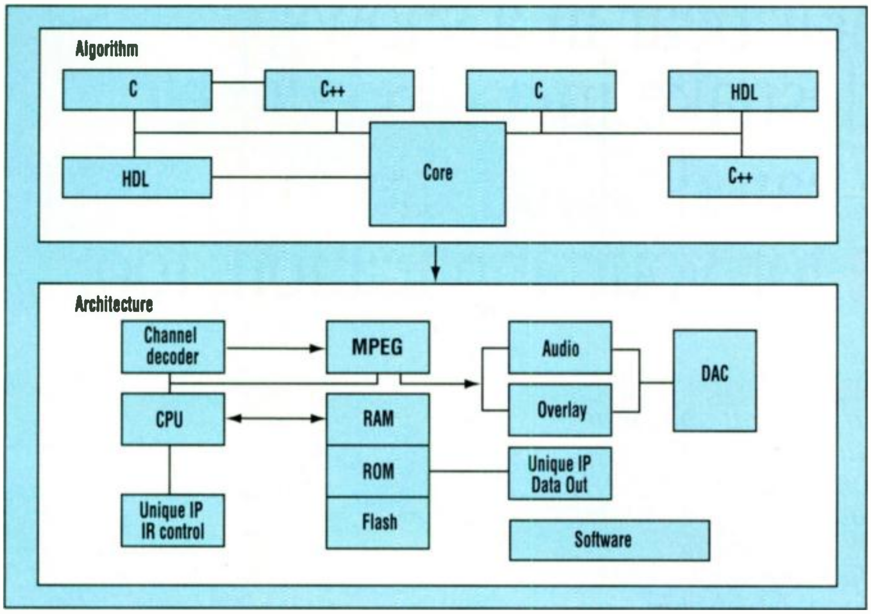

2. A CLOSER TIE BETWEEN the algorithmic, architectural, and implementation design phases is key to speeding the design cycle while providing the much needed verification suites to ensure first-time success.

the system and its operating environment. For each IP alternative that meets system functionality and performance requirements, the user would leverage pricing and IP characterization data to rank each piece of IP for cost and power.

Once the basic system functionality is established and specific IP choices are made, the designer can verify that every possible interaction between large blocks has been fully tested. The vast majority of errors in an ASIC today occur at the hardware-to-hardware interfaces, and the vast majority of errors in the system today occur at the hardware-to-software interfaces. Consequently, interface verification is extremely critical as entire systems are put onto a single chip. As billions of cycles are needed to fully verify functionality, modeling at higher levels of abstraction and rapid prototyping may provide viable alternatives to ensure adequate verification performance.

As the system-on-a-chip specification evolves into a chip architecture, floorplanning is performed to meet timing budgets and routing requirements. The floorplanning tools must have a close link to process-specific layout tools in order to identify potential routing problems early in the design process.

Using a proactive approach (such as a timing-driven design flow) greatly reduces the number of iterations during IC layout. A common tool, such as a basic spreadsheet, can be used to calculate timing and analyze the many interdependencies. If integrated with floorplanning tools, the spreadsheet also can provide designers with immediate feedback on physical implementation decisions. Once the system has been developed at this block level and the initial floorplan is complete, additional partitioning takes place to accommodate the proprietary aspects of the design and an overall design-for-test strategy is created, taking into consideration each unique block.

For those newly-designed functions (custom blocks), partitioning tools are used to break down larger blocks into appropriate types and sizes for lower-level block design. Again, time-to-market requirements require that pre-characterized and verified library elements be leveraged. At this level, the greatest potential for reuse is with datapath and memory elements.

Libraries of parameterized elements greatly speed the time required to produce an efficient deep-submicron implementation that actually works. Taking advantage of regular structures through parameterized libraries saves tremendous time in capture, functional verification, management of critical paths, clock and power distribution, as well as in floorplanning and physical design. In addition to the tremendous time savings, these parameterized elements greatly improve the efficiency of implementations. Recent advances in datapath-generation technology are shown to reduce area by 30% and path lengths up to 50%.

Conventional synthesis is still required for the control portion of custom blocks within the context of a detailed floorplan. And finally, a design-for-test controller and associated logic must be added to ensure test access to each unique block, and the integration of various IP test routines (such as different types of scan, BIST, and boundary scan) into a unified and high-coverage test program.

The emergence of IP-design and -delivery standards will play an important role in allowing companies to fully realize the benefits of block-based design. These standards will facilitate the evaluation of component IPs and their subsequent integration into formalized design flows and design-automation environments that span from system-level design through silicon implementation. Users must have the ability to combine blocks from many different providers and standardize on a unified internal design flow. Standards will make it easier for component IP providers to support multiple electronic-design-automation (EDA) solutions and design flows without requiring separate design kits for each, and should also provide for increased levels of intellectual-property protection.

Every month there are announcements of more silicon capacity; new specialized cores and megafunctions (IP); and new competitors with increasingly complex products, time-to-market advances, and reduced product costs. These factors directly influence the design of a product, and when viewed in the traditional design paradigms, they can create overwhelming challenges. Fortunately, innovative block-based design methodologies are evolving to help designers take advantage of the complex cores provided by ASIC and IC vendors. Block-based design embeds a continuum of design intent and productivity improvements into the product-

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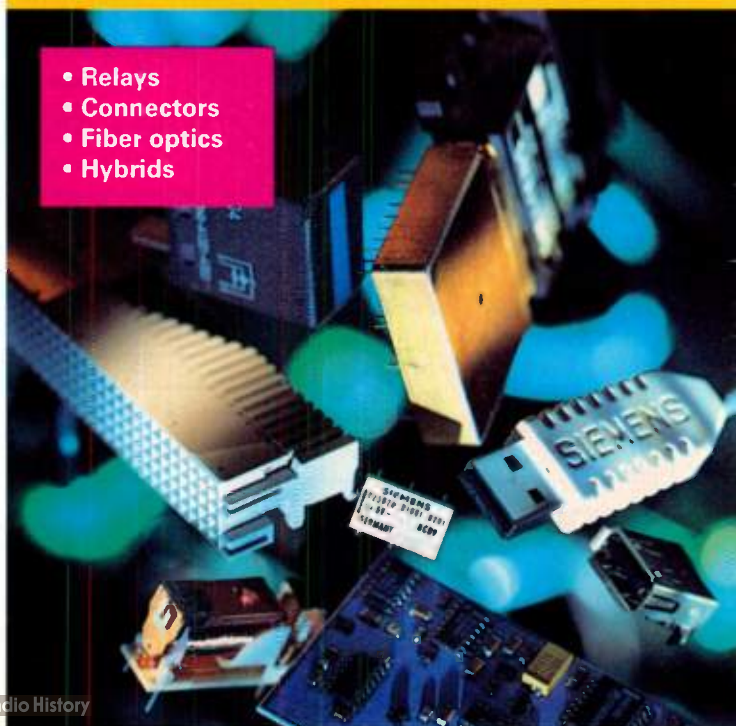

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Philip George is the product marketing manager for the High-Level Design Group at Cadence Design Systems Inc., San Jose, Calif. He can be reached by phone at (408) 894-2317 or by e-mail at pgeorge@cadence.com.

Moving from RTL to behavioral-level design

Behavioral design is a major methodology shift for most engineers.

BY PRADEEP FERNANDES, Synopsys Inc.

Design starts in telecommunications, multimedia, and digital signal processing (DSP) are dominating today's ASIC landscape. These ASICs are increasingly complex, highly proprietary, and operate at high frequencies. At the same time, design teams are becoming smaller while time-to-market continues to shorten.

Each of these fields has its own unique set of challenges. Telecommunications designers, for example, are primarily interested in quickly writing, implementing, and verifying complex specifications. They're also primarily interested in short turnaround loops for modifications due to specification changes, and in performing throughput/latency and RAM-based trade-offs.

DSP designers, on the other hand, are more interested in keeping the specification close to the algorithmic-level of abstraction. And, they're interested in minimal area implementations that meet the required throughput, and in trading off throughput/latency/clock period versus area.

Behavioral design meets all of these needs. It enables much faster creation, verification, and modification through high-level specification. Designers also can create and evaluate multiple architectures quickly, simply by changing high-level constraints. After making high-level trade-offs, behavioral synthesis can automatically create a fully-optimized gate-level design.

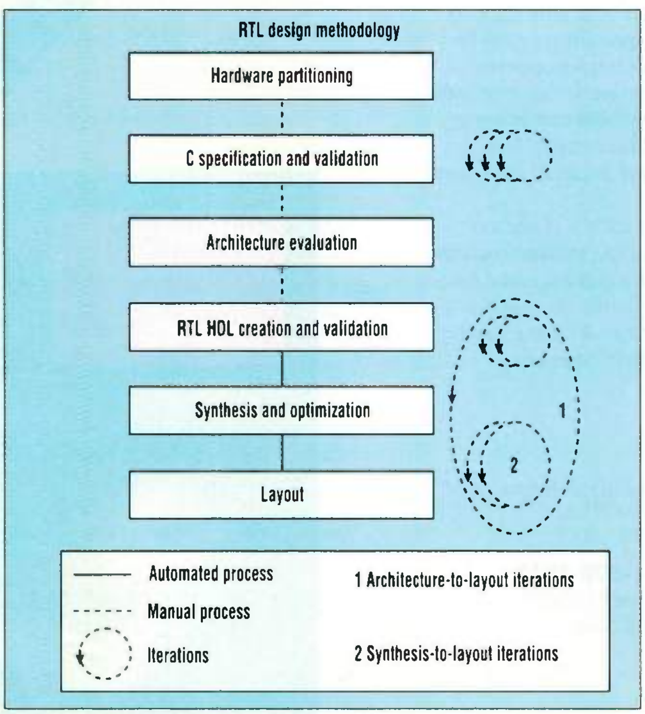
Before proceeding, it makes sense to clarify some terminology:

Latency: the number of cycles for a given functionality to be completed
Throughput: the number of cycles between successive sets of input data
Schedule: assigning functionality to specific clock cycles
I/O: reading from and writing to ports of a design

Making The Move

Behavioral design is a major methodology shift for engineers accustomed to designing at the register-transfer level (RTL). It can be painful and frustrating without the right preparation. Fortunately, a large number of "bleeding-edge" designers have already broken this new ground, making it easier for others to migrate. The rest of this article outlines what it's like to move from RTL to behavioral design. It's based on actual experiences of designers using Synopsys' Behavioral Compiler. The key areas of focus are:

- RTL versus behavioral methodology
- Behavioral coding style
- Design analysis and control strategy
- Verification strategy



1. AFTER high-levelchip partitioning, RTL design begins with architecture specification and validation. Engineers do "back-of-the-envelope" evaluations for various alternative architectures.

RTL Vs. Behavioral

After high-level chip partitioning, RTL design begins with architecture specification and validation. This is typically done in C for quick simulation and debugging. Next, the team does "back-of-the-envelope" evaluations for various alternative architectures. These are largely based on rules-of-thumb and team experience.

Timing and area assumptions are not validated until after simulation and synthesis are complete. By that time, designers will have frozen their underlying architecture because they are unwilling to change the RTL code and go through the resimulation process *(Fig. 1)*.

Design teams are hit hard by timing and area surprises late in the development cy-

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cle. Even worse, their only recourse, gate-level and layout-level iterations through logic synthesis and place-and-route, are often insufficient to get back within specification. The only way out may be last-minute architecture changes that place incredible stress on the entire team and can result in lower-quality designs. Last-minute architecture changes require a time-consuming code rewrite and revalidation, followed by yet another gate-to-layout implementation cycle. Designers need a new methodology that helps them get the right architecture early in the design cycle.

Behavioral design begins with the creation of a behavioral hardware-description-language (HDL) specification *(Fig. 2)*. After quick functional verification, designers use behavioral synthesis to automatically create a number of RTL implementations or architectures.

Moving to the behavioral level would eliminate the manual RTL architecture creation, validation, and evaluation phase. Behavioral HDLs are more abstract, considerably easier to understand, and often simulate more than an order of magnitude faster than RTL code. The behavioral code for one satellite DSP system simulated 23 times faster than the original RTL description. The compact behavioral code also facilitates the processes of code maintenance and modification.

Design at the behavioral level directly addresses a very difficult problem: How do you make accurate architectural trade-offs? Synopsys' Behavioral Compiler maps all operators to technology specific gates, extracts accurate area and delay values, and uses these to evaluate architectural alternatives during scheduling. The tool actually uses bit-level, rather than unit-level, timing to enable sophisticated cascading or chaining of operators. Fast architectural exploration uncovers potential problems very early in the design process, while there is still time to make dramatic trade-offs.

Behavioral Compiler's gate-level timing ensures that it doesn't build more logic between registers than can execute in a clock cycle. Therefore, designers do not spend unnecessary time iterating at the net-list level to meet timing. Advanced capabilities such as register sharing, operator sharing, multicycling, and memory-access scheduling make it considerably easier for designers to create area-efficient, high-performance designs.

BEHAVIORAL CODING

Unlike RTL synthesis, designers using behavioral synthesis do not need to specify registers. Behavioral synthesis automatically creates registers to accommodate scheduling. Instead, designers need to become familiar with nonblocking (signal) and blocking (variable) assignments. Output assignments need nonblocking assignments. All other operations

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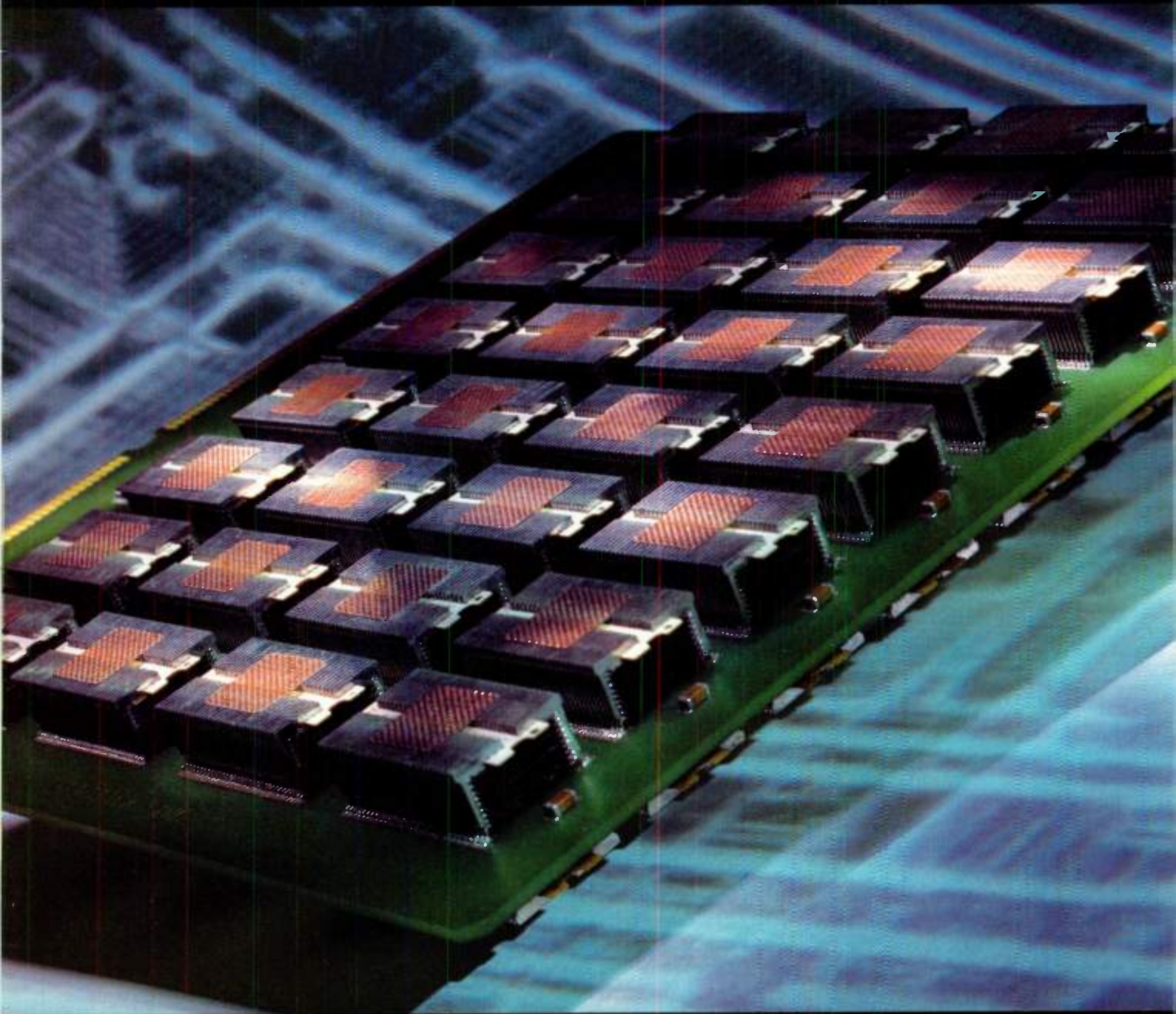

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need blocking assignments. Behavioral synthesis is free to move operations assigned using blocking assignments across clock boundaries so it can optimize for operators and register utilization. Nonblocking assignments, on the other hand, explicitly infer registers in a manner similar to RTL synthesis.

Behavioral synthesis stores all other variables in temporary registers which it can reuse based on variable lifetime analysis. This requires that designers specify "wait until clk'event and clk='1'" or "@(posedge clk)" statements only when performing I/O operations. To analyze register contents, Behavioral Compiler produces register scheduling reports that show the contents of all intermediate registers in different clock cycles. This helps designers understand the internal implementation.

The other primary behavioral coding style change is the use of more intuitive coding constructs to implement functionality. For example, this includes using "infinite" and "while" loops for implementing handshaking, "for" loops for implementing iterative functionality, and array accesses to read/write RAMs without explicitly writing the RAM control signals.

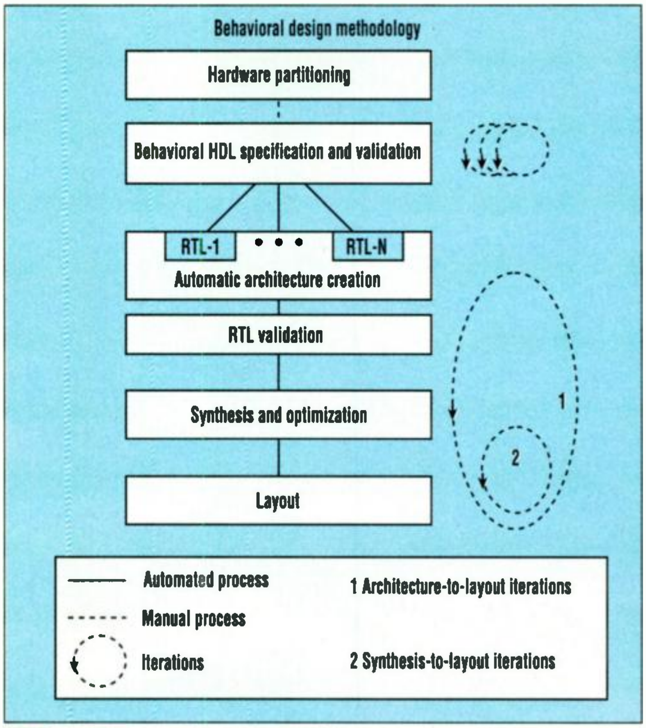
It typically takes a month or two for designers to become proficient at writing behavioral code, but the payback can be immediate. A recent asynchronous transfer mode (ATM) segmentation and reassembly (SAR) design highlights the benefits. The designer worked on the RTL code for over four weeks without getting it to simulate correctly. In less than three weeks, he was able to code the function behaviorally and get the design working with higher-than-expected throughput. According to the designer, behavioral coding was more intuitive, facilitating fast design creation and debug.

Design Analysis

Designers often worry about losing control as they move to behavioral design, because behavioral synthesis automatically creates the architectures. Even when using higher levels of abstraction, designers need direct control over some aspects of the implementation. Behavioral Compiler has an extensive set of controllability commands to fulfill this need. For example, designers can explicitly constrain operations to specific clock cycles, or have specific timing relationships be made relative to each other. They also can encapsulate critical logic using Synopsys' Designware library elements, thereby controlling the underlying implementation.

Library encapsulation is very useful for high-speed designs. Here is how one designer used it to implement a pipelined graphics processor: Behavioral Compiler reported that it was multicycling a multiplier because its delay was longer than the clock cycle. After trying various compile techniques without success, the designer noticed that the multiplication was always followed by saturation logic. The multiplier delay was 1.5 times the clock delay, while the saturation logic was 0.3 times the clock delay. The designer encapsulated the multiplier and saturation logic together and used behavioral retiming to pipeline the result. The pipelined operation had a critical path that was 0.9 times the clock delay. He then used Behavioral Compiler's loop pipelining feature to pipeline the entire graphics module, including the new pipelined saturation multiplier. Behavioral Compiler automatically synthesized a new pipeline controller for the design.

In two days, the designer had produced a gate-level design with reduced area and improved throughput. This process would have taken much longer if designed with RTL methods. He would have had to manually pipeline the multiplier, change the pipeline register assignments to account for the extra delay at different stages, change the entire pipeline controller because the entire pipeline is changed, verify that the changes were correct, and resynthesize.



2. BEHAVIORAL DESIGN begins with the creation of a behavioral hardware-description-language (HDL) specification. After quick functional verification, designers use behavioral synthesis to automatically create a number of RTL implementations or architectures.

To help designers analyze their automatically generated architectures, Behavioral Compiler produces reports on finite state machines (FSMs), registers, and operations, showing exactly when and how all the functionality was implemented. The reports help identify bottlenecks in the source code.

When analyzing these reports, one telecommunications designer noticed that while his RAM was fully-utilized, the rest of the resources were underutilized. Changing the single-port RAM to a dual-port RAM resulted in lower latency by better balancing resource utilization. This type of tradeoff is easy to obtain when using behavioral design.

Verification Strategy

Unlike RTL design, where the inter-cycle and intra-cycle behavior is fixed, behavioral design allows users to change cycle-level behavior based on constraints. Taking advantage of this new power may require a different verification strategy.

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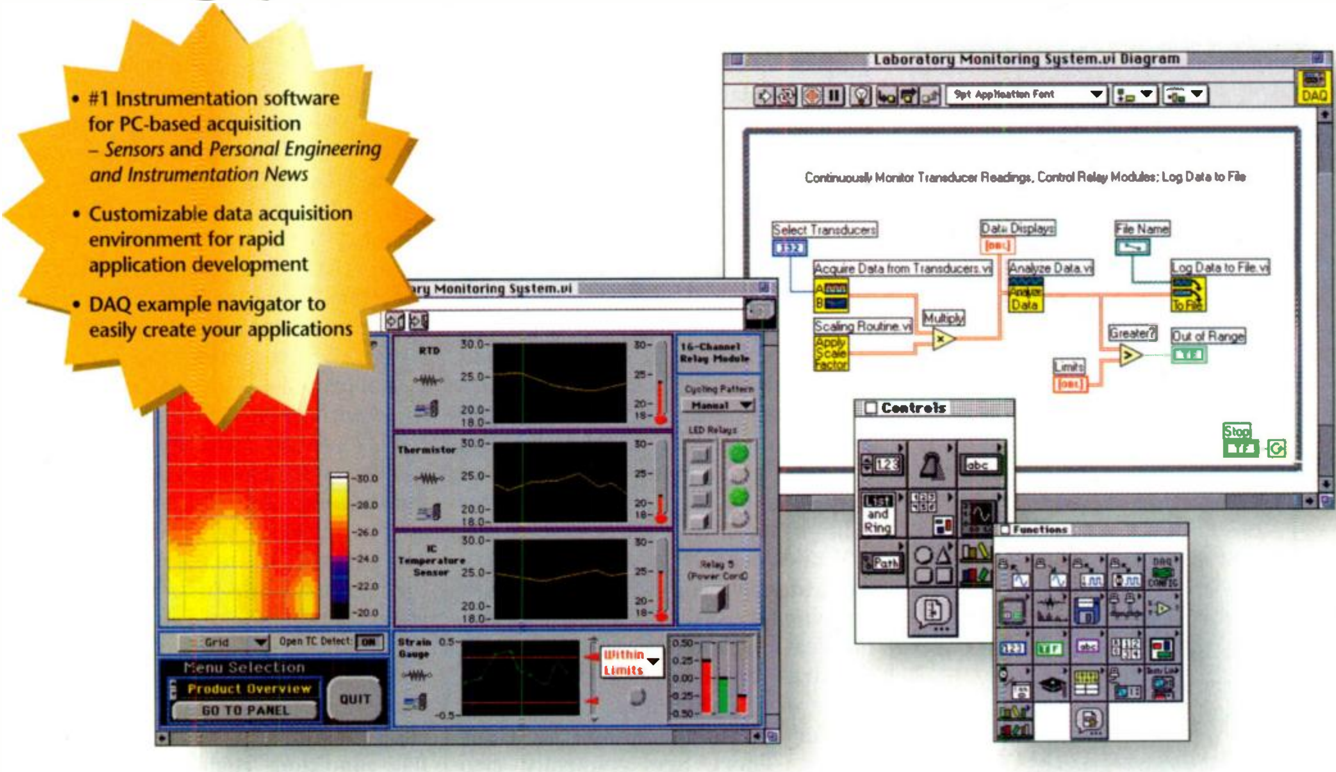

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Verification of complex systems is broken down into several phases. The first phase usually consists of system-level (functional) modeling and simulation. The models written at this stage may not be cycle-accurate with respect to the final implementation of this system. However, models are written at this level because they can be simulated extremely quickly and they are very easy to debug. The models simulate much faster because they are written at a high level of abstraction, they do not refer to low-level implementation details (such as components, control signals, etc.), and do not refer to as many clock edges as may exist in the final implementation phase.

While these descriptions are sufficient to model one process that takes data in and passes data out, the communication between many processes requires them to handshake. In other words, they must receive and ask for data and communicate their status. There are generally two mechanisms for doing this.

Under the first mechanism, the models communicate their status via acknowledge/request signals, and all the processes run independently of each other. For example, when process1 needs data from process2, it requests it. If process2 is ready, it will send it to process1. Otherwise, process1 waits until process2 is ready to communicate.

This first scheme of communication requires clock edges only around these handshake sequences and not anywhere else, thus enabling fast simulation. In addition, this strategy defines an explicit communication strategy between each set of processes, and no assumptions are made about when the communication occurs. This model is used whenever processes don't have deterministic completion times, wherein designers can make latency and throughput trade-offs. Waveforms are identical before and after scheduling. The scheme is accomplished using Behavioral Compiler's superstate-fixed scheduling mode.

The second mechanism is to specify predetermined points in time at which the communicating processes will exchange data. This requires the models to be cycle-accurate at the interface level. For example, suppose that process1 and process2 need to communicate with each other, and the system designer specifies that at a point 20 clock cycles after the two processes start, process1 is to exchange data with process2. This type of model doesn't distribute the functionality between the clocks—it just lumps all the clocks together after the functionality is written. There's no explicit communication protocol between the processes—the communication protocol is implicit and pre-defined with respect to time.

This second strategy can be employed whenever processes have guaranteed and deterministic response times, wherein designers don't need to make latency and throughput trade-offs. The strategy is accomplished using Behavioral Compiler's cycle-fixed scheduling mode. To further aid verification, many behavioral design tools also include static analysis capabilities to flag conditions such as unused variables and unused operations.

EASING THE TRANSITION

For designers who want access to some behavioral optimizations but can't move to a behavioral methodology, behavioral retiming may be the answer for them. While behavioral retiming can't provide them with the full power of architecture design, it can provide them with substantial quality of results improvements.

Behavioral retiming optimizes register placement in gate-level designs without changing cycle-level behavior. Designers don't modify their source code or their testbenches, because the design's functionality doesn't change. Instead, with the push of a button, designers have seen performance improvements of up to 15%. Behavioral retiming is applicable on FSM, datapath, and mixed FSM-datapath designs. Find out more about behavioral design and its applications under the Behavioral Compiler section of Synopsys' web site (http://www.synopsys.com/products/beh_syn). □

Pradeep Fernandes is a senior corporate applications engineer for Synopsys Inc., Mountain View, Calif. He can be reached at (415) 694-4185 or by e-mail at pradeep@synopsys.com.

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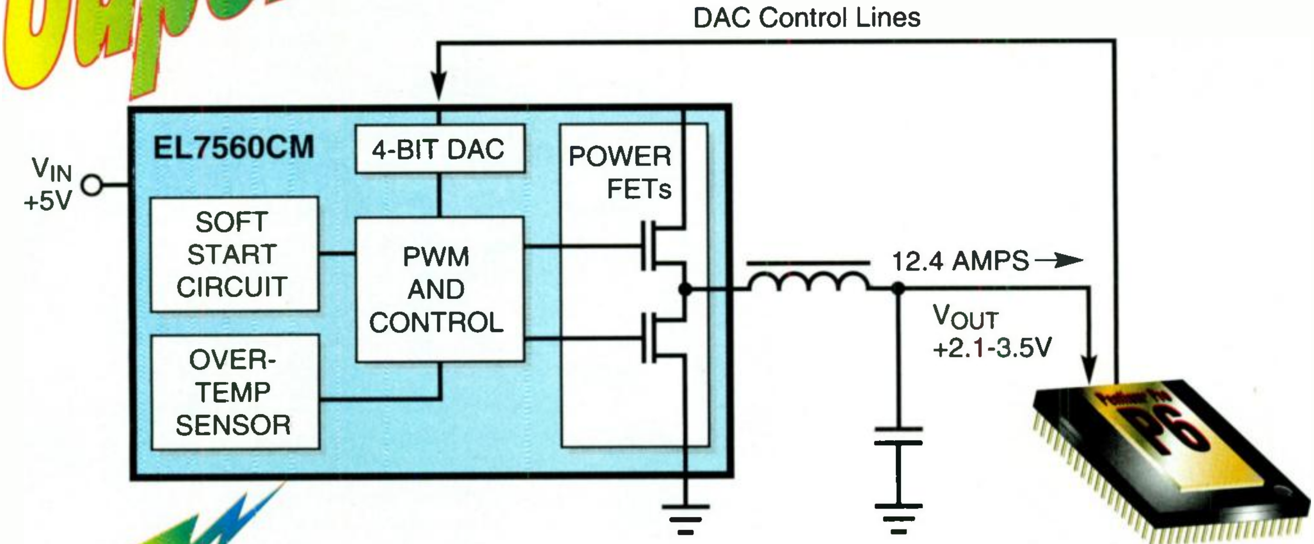

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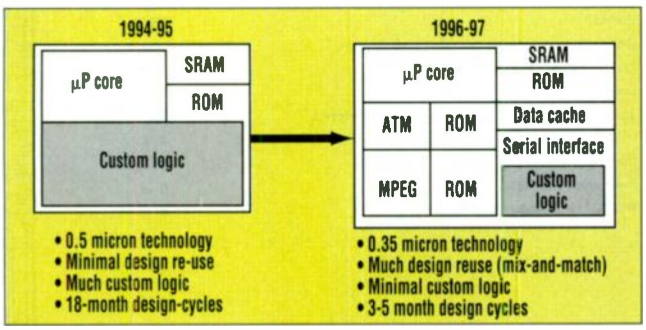
Design Reuse In Today's DSP Design Methodology

Now You Can Really Stop Reinventing The Wheel!

STEVE SVOBODA
Alta Group of Cadence Design Systems
555 N. Mathilda Ave.
Sunnyvale, CA 94086; (408) 733-1595.
e-mail: svoboda@altagroup.com

This is the first installment of a two-part article that demonstrates how design reuse and software-executable models of design elements will play a key role in increasing productivity and reducing time to market.

Picture this: It's 9:30 a.m. and your boss has given you a new assignment. A new modulation-coding technique developed for reducing power consumption in cellular phones, and he wants you to try it out. "This might be the greatest thing since Trellis-Coded Modulation (TCM) was developed in the mid-80s," he says. "One of our DSP gurus has written all the algorithms in C, and we want to see if it can be incorporated into the handset we're rolling out at the end of the quarter, the 'Road Warrior (RW)-2000.' Let's meet tomorrow morning at 9:00 and go over your results."



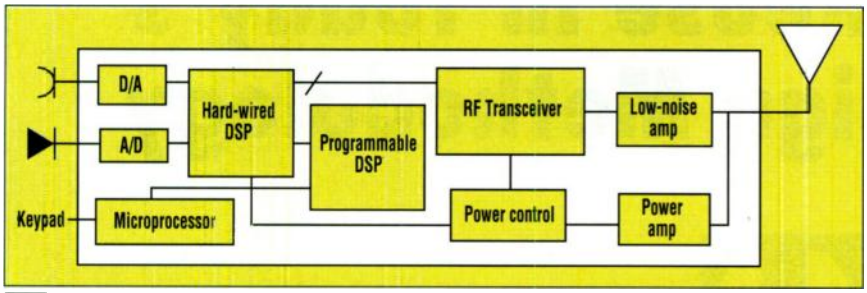
1. THE IC has evolved from noncustomizable cores with extensive custom-logic being used to provide added functionality. Instead, today's IC designers prefer to "mix and match" design building blocks that can be easily attached to an extensible core. This enables a designer to minimize both development time and cost.

After refilling your coffee cup, you go back to your desk and get to work. You bring up an executable-model ("virtual prototype") of the RW-2000 on your workstation, and decide that not only will you have to add new DSP firmware to handle the modulation/coding, you'll also have to swap-out one of the DSP cores in the design since it can't handle the additional processing. Furthermore, you'll have to change some of the firmware running on the microcontroller to accommodate the new device.

Next, you search through the World Wide Web and find "executable-models" of extensible DSP cores available from several vendors. Two of those models look like promising candidates, so you download them to your workstation. After customizing their I/O and memory configurations to fit cleanly within the rest of the design architecture, you remove the original processor-core from the RW-2000 virtual prototype and swap-in the first candidate. You then compile the C code given for that target processor and change the microcontroller code. You're ready to start running simulations to determine the effect on system-level performance when your watch starts beeping—it's time for lunch and your twice-weekly game of volleyball!

After lunch, you provide the RW-2000 virtual prototype with a series of digitized audio inputs that include recorded words, sentences, and hi-fi audio. You listen to the output through a pair of headphones. Analysis tools estimate what the actual power consumption for the system would be for each set of inputs. You repeat the same sequence with the second candidate processor-core to see how well the system works with that one. The simulation results clearly indicate that the second candidate is better.

At this point, you begin "environmental testing." You adjust various "controls" in a simulated "verification environment" to test the effects of noise, co-channel interference, and Rayleigh fading. You also test the performance of the system under various hand-off scenarios. Afterwards, you determine that while there is a barely perceptible degradation in audio performance, the phone's performance would be about 2% less reliable during hand-offs, and the new modulation-coding technique decreases average power consumption by over 40%! A worthwhile trade-off, no doubt. After



2. TODAY'S MOBILE TELEPHONE is a highly integrated design, requiring only a handful of building blocks. Just a few years ago, mobile phones typically contained scores of discrete components. Today, the number of major components is less than ten. Designs are quickly becoming highly standardized, with the main sources of differentiation being the embedded software running on the microcontroller and DSPs.

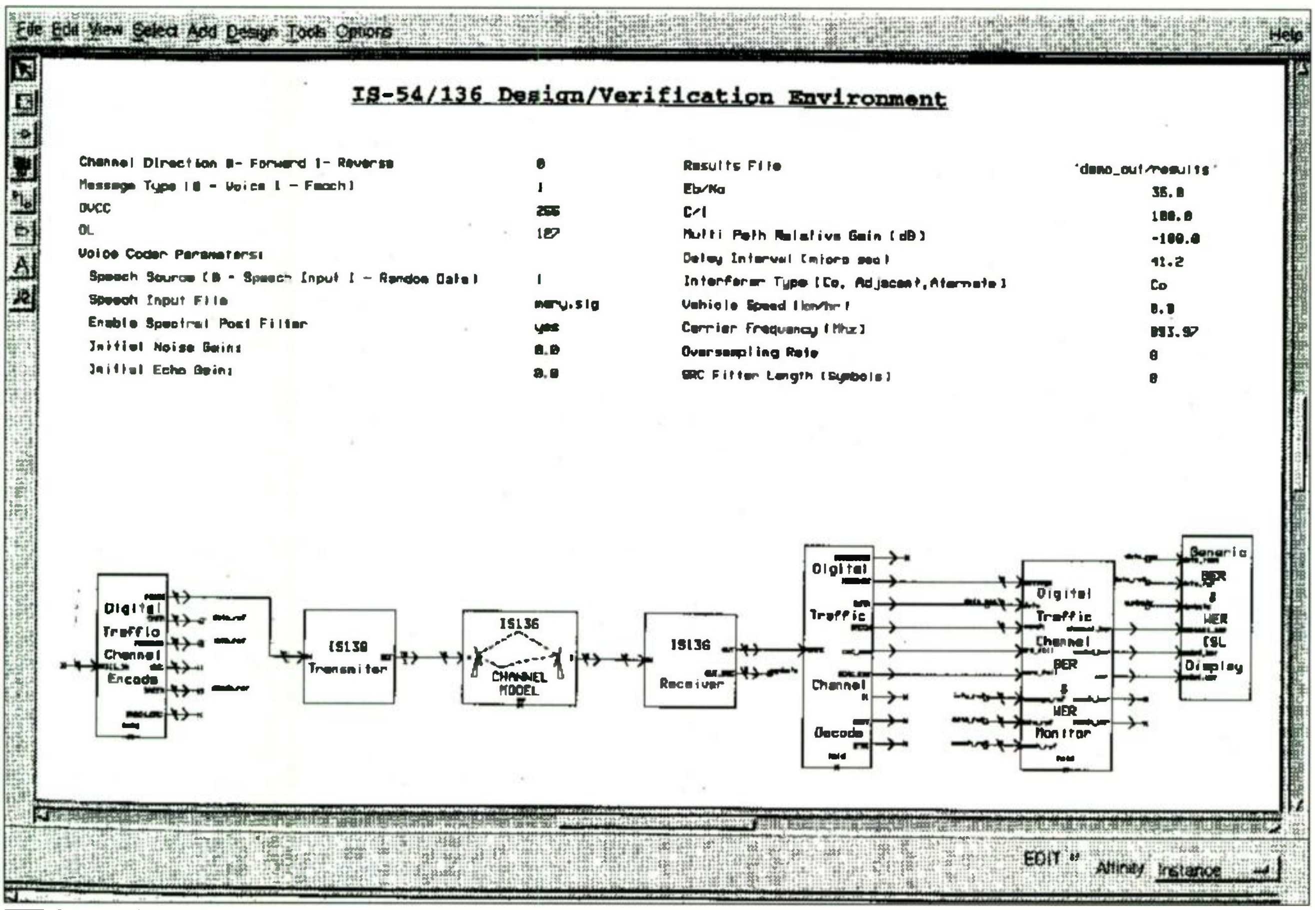
printing all the test results to review with your boss the next morning, you realize that it's 7:00 p.m.—time to go home after a solid day's work!

Think that this scenario sounds far-fetched? Think again.

Current electronic product design is characterized by increasing levels of component integration, customizability, and design reuse, enabling manufacturers to deliver greater functionality within smaller "packages" at lower cost. Recent advances in system-level design tools have played a key role in making this possible. The capabilities of system-level design tools from companies such as Alta Group, as well as the published results from research programs such as Ptolemy at U.C. Berkeley, show that the technology and infrastructure already exists to make scenarios such as the one depicted earlier commonplace.

IC DESIGN

One place where all these changes can be seen at work is in IC design *(Fig. 1)*. The availability of low-cost standard designs and the increasing ability of designers to integrate and customize multiple components (e.g. "megacells" and "cores") is moving them away from building "custom" components and toward designing with "building blocks" instead (ELECTRONIC DESIGN, *Jan. 22, p. 81*). Designers now have a large selection of processor-cores whose architecture (memory, I/O, etc.) can be readily customized. Moreover, semiconductor manufacturers are providing detailed, "executable-models" of these processor-cores so prospective users can test their performance within an overall system. Examples include TI's C5x-



3. THIS IS-54/136 WIRELESS VERIFICATION ENVIRONMENT contains models of the key architectural components of the IS-54/136 cellular telephone standard, and of the cell-phone's transmitter and receiver sections. By allowing them to interact under simulated environmental conditions, an engineer can understand and verify the "real" phone's performance.

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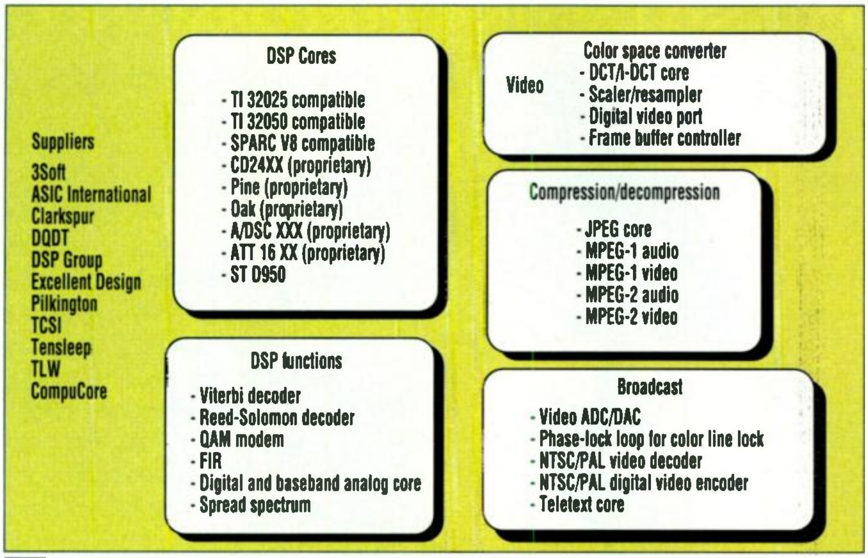

4. A SAMPLING OF CURRENTLY AVAILABLE IP executable cores demonstrates the rapid acceptance of design reuse within the communications industry. For many components, executable-specifications for use within a system-level design environment already exist. As the number of applications for DSP grows, manufacturers are striving to integrate new technologies into their products. This will cause new markets to develop around the development, sale, and transfer of IP. Executable specifications will be the vehicle for this commerce.

series, AT&T's 16XX-series, DSP Group's OAK/PINE cores, Motorola's 56000-series, and SGS-Thomson's D-950 series.

Cellular Phone Design

In similar fashion, the design of complex electronic systems such as cell-phones is also changing. Today's cellular phone is a marvel of modularity and integration. In the late '80s, each of the functional blocks would have comprised dozens of discrete components, custom ICs, and hardware *(Fig. 2)*. Nowadays, the total number of major components in a cell phone is usually less than 10.

Cell-phone designs were also difficult to modify and/or customize. The lack of powerful DSPs and microprocessors limited the use of embedded software, adversely impacting the quality and cost of products and services consumers could obtain. But as DSPs and microprocessors have grown more powerful, manufacturers increasingly rely on embedded software, leading to an explosion in the number of features and brands of cellular phones available. Embedded software, extensible DSP cores, and customizable ICs make it easy for manufacturers to adapt standard designs and deliver new products to market quickly. It used to be that the development cycle for a typical cellphone ranged from 24 to 36 months—it now ranges from 12 to 18 months (for pagers it can be as little as 6 to 8 months).

There is no question that the cellular phone of the future will carry the trend toward increasing integration and customizability to further extremes. As new technologies are incorporated to provide consumers with complex new services and capabilities, verifying product performance, functionality, and ease-of-use will become increasingly important for manufacturers. At the same time, competitive pressures will continue to drive companies to shorten development-cycles, reduce costs, and minimize technical risk. Manufacturers of various electronic products will experience these market dynamics to a significant extent.

Given the situation, one can see why the current methodology for designing electronic products such as cell-phones and ICs is having to evolve rapidly. The purpose of this two-part series of articles is to describe these changes, and their impact. This first article describes the emerging methodology for developing electronic products, which is heavily based upon "system-level" design and maximizing "design reuse." We will show you how by moving up to the system-level (i.e. designing at higher levels of abstraction) and reusing proven designs, you can build more complex products faster and less expensively, and with lower risk.

Part II will focus on the specific challenges you may encounter in trying to put this new methodology into practice. Although system-level design and hardware-synthesis technologies are relatively mature (software-synthesis technology is emerging, but still in its infancy), difficulties can still surface as designers drive their system-level designs toward final implementation. We also will discuss where some of the "technology-gaps" exist and how to work around them.

Current Limitations

If we go back to the design scenario depicted earlier and examine how to perform all the tasks that were described, equipped only with devices such as mathematical analysis tools, C models of DSP functions, DSP cards for breadboarding in the laboratory, and perhaps HDL and logic simulators, we can see several limitations.

To begin with, using these tools to build a complete prototype of the "RW-2000" and its operating environment would be very difficult and expensive, if not impossible. But without such a prototype, how do you go about modifying the design and testing the results? Theoretically, you might simulate the entire system in a logic-level or RT-level simulator, but how practical would this be? With gate-counts for single ICs now exceeding 250K, simulating the performance of complex functions on a logic-level or RT-level simulator takes days, and sometimes weeks. So, how do you go about efficiently making design tradeoffs? Or debugging your design? Or iterating on the design? How do you simulate the system's operation under realistic conditions and measure the effects on overall performance? Solving all these of problems requires a *paradigm-shift*.

Instead, you begin with a virtual prototype of the entire product or system. The virtual prototype contains accurate executable-models of all the

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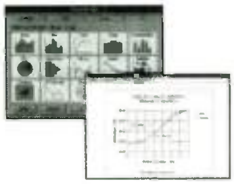

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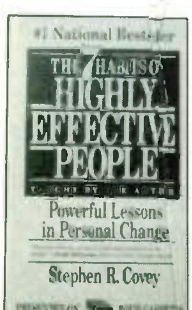

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system components, some that you have designed yourself, and others obtained from multiple sources. Some components (where implementation details are not of concern) are represented as C/C++ algorithms running inside of "blocks." At the inputs/outputs to those blocks, you monitor the data as it is processed by that algorithm one word/data-sample at a time. Other components (where implementation details are of particular interest) are represented as RT-level or logic-level models, running inside other blocks. At the inputs/outputs to those blocks, you monitor what is happening to each bit during each clock-cycle. Models of the system operating environment enable you to continuously verify system performance under realistic conditions. Design changes consist of editing block-diagrams to "mix-and-match" different system components, changing block parameters, and using debugging and visualization tools to monitor the system's operation "on-the-fly."

The ability to mix-and-match system components enables design reuse, which is growing increasingly important in the electronics industry. As "convergence" products embodying multiple technologies become commonplace, and the overall complexity of electronic products increases, not having to "reinvent the wheel" becomes critically important. The information-explosion of the late 20th century and higher levels of technological specialization are making successive technological innovations increasingly expensive. As a result, it is becoming increasingly difficult for a single company to possess all the technological "know-how" it may want to embody into a product.

The most practical solution is for a company to focus on the key technologies it knows best and license the others. Companies typically refer to their proprietary technology and designs as "intellectual property" (IP). In general, IP refers to any knowledge or technology that has market-value. It can be an actual piece of hardware, an executable-model of that piece of hardware, a schematic, or just an algorithm. The newly emerging methodology for electronic product design is essentially to combine hardware and software building-blocks from multiple vendors to build complete systems and products. This is commonly known as *IP-based design*.

Until now, we have been very general, and you may have questions such as:

- How is IP-based design supposed to work?
- What makes IP-based design possible?
- What are some of its limitations?

In the rest of this article, we will explore the first two questions in some depth. The third question will be addressed in the next article (Part II).

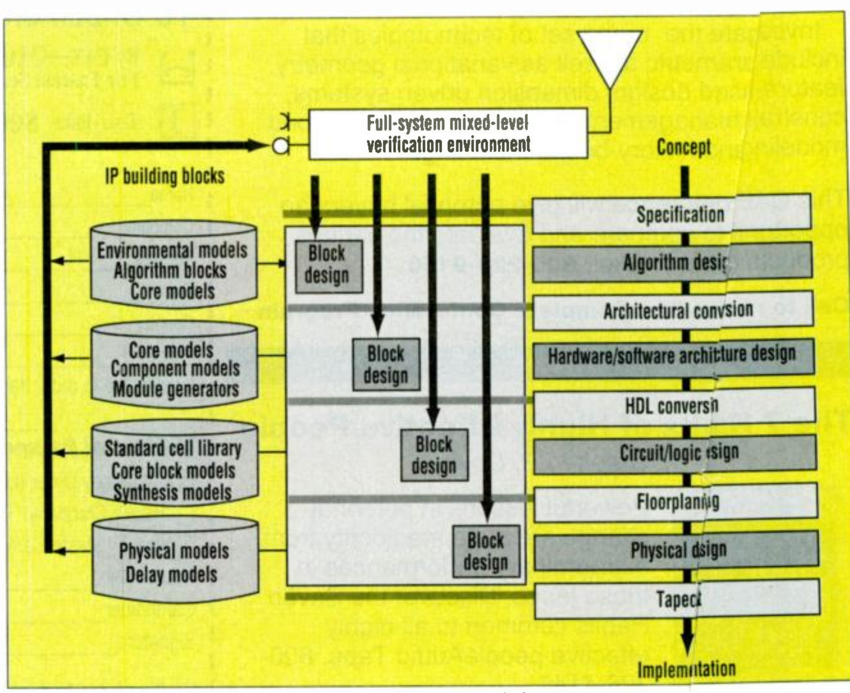
To understand the "how" and "why" of IP-based design, one must first be familiar with several key concepts and definitions in the areas of system design representation and verification. Later on, these concepts and definitions will be tied together to describe how IP-based design works.

Levels Of Abstraction

At different stages in the development process, systems/devices are represented at different levels of abstraction.[1] Using the appropriate level of design-abstraction at each stage lets the designer complete the tasks for that stage as efficiently as possible. This ensures that system functionality is carried reliably from each stage to the next—resulting in faster system integration and fewer design iterations.

When a system/device is represented algorithmically or behaviorally, we describe its functionality in terms of its inputs and outputs. On the other hand, we say nothing about what is inside (i.e. the implementation). For example, within one of Alta Group's Signal Processing WorkSystem (SPW) product libraries, you can find a functional building block called "Fixed-point Viterbi Decoder." The block contains C code that executes the Viterbi algorithm, and has parameters to adjust for register length, code rate, and so on. But the eventual implementation depends upon the particular design steps you wish to follow. For example, that algorithm could be implemented in custom hardware (using any number of different hardware architectures) or as firmware running on a DSP processor.

Alternatively, representing a system/device in terms of a hardware/software architecture means defining it in terms of its hard-



5. IP-BASED DESIGN METHODOLOGY within a mixed-level verification environment will allow manufacturers to develop more complex products within shorter time frames. Thanks to these powerful tools, design reuse and continuous verification are rapidly becoming standard practice within large segments of the industry.

Fig. 1

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Fig. 2

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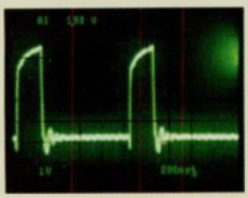

Analog

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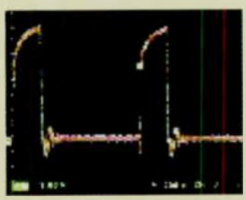

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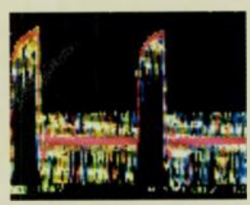

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Max. Record Length	250K	500K	250K	500K	500K
Max. Wfm. Acquisition Rate	100,000 Wfm/s	100,000 Wfm/s	180,000 Wfm/s	400,000 Wfm/s	400,000 Wfm/s
Display	Monochrome	Monochrome	Color	Color	Color

Tektronix

ware/software subcomponents and the interconnections/dependencies between them. In the case of the Viterbi Decoder, a hardware architecture representation includes specifications for items such as the shift-registers, adders, muxes, latches, buses, and clocking. There are two ways of capturing this information: Directly in the form of HDL "code," or in block diagrams where each block maps directly to an HDL code segment.

Several of the more popular hardware architecture development tools use the block-oriented approach. In many cases, designers find it much easier to troubleshoot designs captured in the form of block diagrams (where they can monitor the inputs/outputs to/from each block) than if they are captured in long sequences of HDL code.

Finally, a physical representation of a system/device describes the implementation fully in terms of its subcomponents. Not only do we specify all the individual subcomponents of the design and their connectivity, but we also describe their spatial relationship. For example, in the case of an IC, we would define the dimensions of the logic cells and gate arrays, their physical locations on the silicon, and the physical locations of all the paths connecting them.

EXECUTABLE SPECS

The concept of "executable-specifications" is one of the cornerstones of IP-based design methodology. IP-based design consists essentially of integrating the executable specifications of multiple IP components to develop a complete system design. An executable specification is defined as an abstract object representing (in a machine-readable and machine-executable form) a particular functionality where the level of detail/abstraction can vary, according to the designer's requirements and the design-context in which the executable specification is being used. It can be thought of as a "box" where one defines explicitly all the characteristics such as inputs, parameters, and outputs, and the inner workings are defined to whatever level of implementation-detail is required by the designer.

In the case of the Viterbi Decoder, an executable-specification could be a C/C++ algorithm, or a defined set of hardware resources executing a sequence of logical operations captured in Verilog/VHDL, or potentially a megacell available as "CoreWare" from a company such as LSI Logic. All of these different representations accomplish the same high-level function—a Viterbi Decoder.

Possibly the best example of an executable-specification for a semiconductor device is that of an executable DSP core model which comes in two classes: Instruction-set simulators and cycle-accurate simulators. An instruction-set simulator verifies that

IT IS BECOMING INCREASINGLY DIFFICULT FOR A SINGLE COMPANY TO POSSESS ALL THE TECHNOLOGICAL "KNOW-HOW" IT MAY WANT TO EMBODY INTO A PRODUCT.

the firmware running on the processor performs all the correct functions on the input data. For every sample of input data, the processor executes a set of assembly-instructions and generates samples of output data so one can verify that the relationships between the data at the output to the data at the input are valid, and that the order of the data appearing at the output is also valid.

On the other hand, no timing information is provided—this requires a cycle-accurate simulator. In a cycle-accurate model, the logic-levels of all the processor's inputs and outputs are defined for every clock-cycle. With this capability, one can easily integrate and test a processor's functionality with other clocked-hardware.

Another defining characteristic of an executable specification is that its performance can be monitored on-the-fly. The designer can observe the operation of the executable specification of each building block within a system design, and visualize the way the overall product will work from the earliest stages in the design cycle. As implementation details are added (i.e. as executable specifications containing greater amounts of implementation-level detail get substituted-in), the designer can continue to visualize the overall system's performance and ensure that nothing has been adversely affected.

MIXED-LEVEL VERIFICATION

The other cornerstone of IP-based design methodology is full system mixed-level verification. This is the capability to combine executable specifications to represent an entire system, where each can be at a different level of abstraction. For example, a system model for the cell-phone design consists of executable-specifications for each of the building blocks, where some are represented algorithmically/behaviorally and others are represented architecturally, depending upon the requirements of the designer *(Fig. 2, again)*. "Full system" refers to the capability to simulate end-to-end performance. "Mixed level" refers to the capability to integrate different levels of abstraction within the same model.

The key benefit of full system mixed-level verification is the capability to simulate the performance of an entire system within its operating environment. The operation of a cell-phone can be simulated under various environmental conditions along with its interaction with external systems, such as the cellular base-station. An example of this is depicted by using an IS-54/136 Wireless Verification Environment *(Fig. 3*.

Models of all the key architectural components of the IS-54/136 standard interact with a model of the cell-phone transmitter and receiver within simulated environmental conditions to verify the system's overall performance. Full-system mixed-level verification is a new development in system-level design.

This capability is based upon the pioneering research in "Heterogeneous System Simulation" by Dr. Edward A. Lee et al., University of

California, Berkeley. His team studied methods for combining different simulation paradigms (i.e. "models of computation") such as synchronous dataflow, dynamic dataflow, cycle-based, and discrete-event within a single overall simulation environment.[2]

Different classes of system behavior require different simulation paradigms in order to be described fully. In other words, full system mixed-level verification requires combining all these paradigms within a single environment.

Note that the definitions of "system" and "operating environment" are always relative. In one context, the system can be a cell-phone/base station operating within an urban RF environment, while in another context, the system can be a DSP core or an IC operating within an environment consisting of other ICs, processors, memories and glue-logic. As one proceeds from the algorithmic/behavioral level down to the physical-level in the design process, the nature of the test inputs and outputs of the design-under-test changes; test-bench generation and signal estimation becomes highly important.

Another advantage of full-system mixed-level verification is that it aids, and mostly automates, the process of translating high-level signal inputs into test-vector inputs (i.e. test-bench generation). It also translates test-vector outputs into "signal estimates" (i.e. testbench extraction).

Therefore, full-system mixed-level verification is the key technology that enables a designer to combine the executable specifications of different system components and perform IP-based design.

PUTTING IT ALL TOGETHER

IP-based design fundamentally integrates executable specifications to create complete systems. The key to this method is having the design information you need represented in the form of executable specifications at the appropriate levels of design-abstraction, and having a development environment that enables you to integrate executable specifications together and test their performance *(Figs. 4 and 5)*.

There are a number of advantages to starting the IP-based design process at the highest possible level of abstraction. First, it is much easier to verify functionality. Simulating a system's performance at the highest level of abstraction is rapid and efficient because the amount of detail that is simulated is restricted to the level of detail required in the results. In fact, implementation-level details often impede, rather than aid, the designer in ensuring that a system-model is capturing all the required functionality.

As electronic systems embody additional functionality, their complexity (measured in terms of number of gates, or lines of code) increases by an even greater incremental amount. As a result, verifying functional correct-

DESIGN REUSE TECHNIQUES FOR THE 21ST CENTURY

ness becomes increasingly critical, yet more challenging, to accomplish. Since we are limited in the number of distinct objects and pieces of information that can be tracked simultaneously, the only recourse is to begin a design at the highest possible level of abstraction, gradually working down toward implementation.

Moreover, as design-tools continue to improve and automate the design process at lower levels of implementation, it leaves designers free to focus on the higher levels, where their decisions can have a major impact on product quality and functionality. In effect, the designer's emphasis changes from building the system right to building the right system.

System-level design also facilitates design reuse, whether you are doing new designs or modifying "legacy" designs. System-level design information is easier to understand and to combine with other system-level design information than is physical-level design information.

Interfaces between physical-level components must be designed at the physical level. System-level components, on the other hand, either have standard interfaces, or can have interfaces designed at the algorithmic/behavioral level and taken down to implementation along with the system-level components.

Just as system-level IP-based design makes the design process more efficient, it also leads to more efficient designs. The ability to simulate the operation of different parts of a design in any combination, and measure their exact performance, eliminates the need to "over design." Performance margins for different portions of the design can be made "tighter," and you can then focus on delivering maximum performance only "where it counts." Having a common design environment and methodology that system-level and implementation-level designers can use together also fosters concurrent engineering, and improved capability for design exploration. These capabilities also help you maximize design reuse and more easily upgrade products by adding functionality to legacy designs.

In second part of this series, we will cover how to put IP-based design into practice. Some of the topics to be discussed are:

- Who is developing all the IP? How will it be packaged, delivered, and safeguarded?
- How does one go about integrating IP from multiple sources? What new capabilities must system-level design tools develop to bring about further improvements?
- How can users of IP continue to differentiate their products from their competitors' to succeed in the marketplace?

As system-level design tools progress and IP delivery takes on greater importance, these and other related issues continue to be addressed by system-level design-tool vendors. The good news is that even though some of the answers are incomplete, IP-based design methodology is already far enough along to offer designers ample benefits. □

Steve Svoboda manages development and marketing for Alta Group's Signal Processing WorkSystem (SPW). He holds a bachelor of science degree in electrical engineering and a bachelor of arts degree in economics from Johns Hopkins University, as well as master's degrees in both electrical engineering and engineering management from Stanford University. He has two patents currently pending in the U.S. for inventions in the field of FM co-channel interference cancellation.

References:

1. See Gajski et al., "Specification and Design Of Embedded Systems (Ch. 1)" for a thorough discussion on this topic.
2. Heterogeneous simulation is a complex subject and outside the scope of this article. The interested reader is encouraged to examine the research papers published from the Ptolemy project. Many are available through the WWW.

HOW VALUABLE?	CIRCLE
HIGHLY	534
MODERATELY	535
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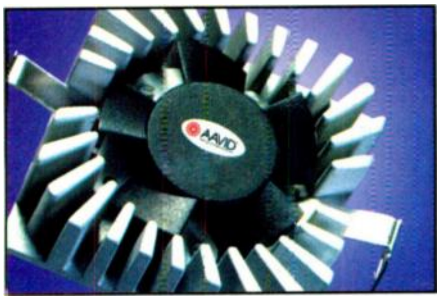

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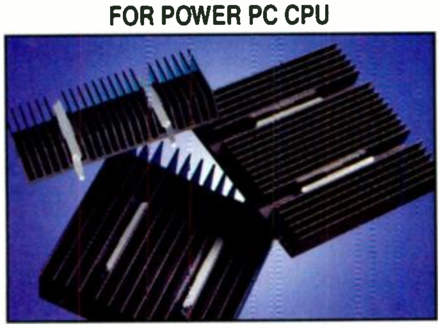

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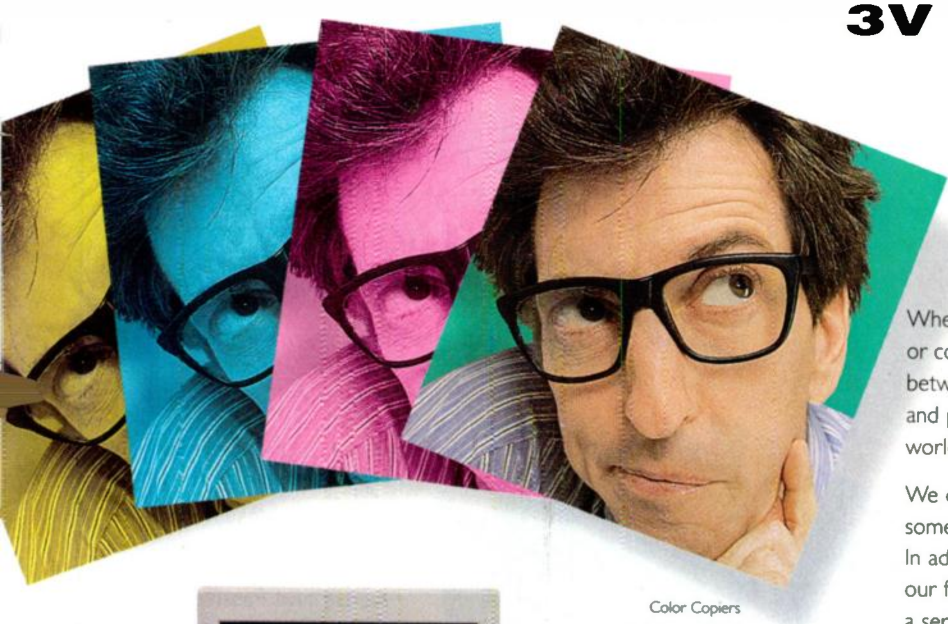

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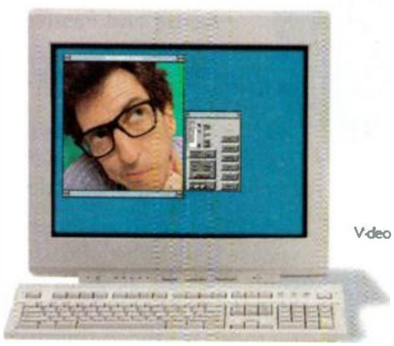

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READER SERVICE 95

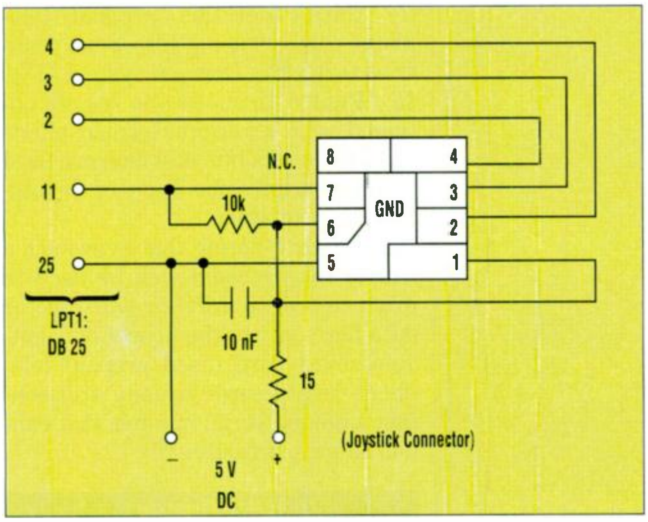
CIRCLE 520

Simple PC Smart Card Reader

PATRICK GUEULLE, B.P. 279, 76055 Le Havre Cedex, France.

ISO 7816-compliant "synchronous" smart cards (such as those used for prepaid telephone cards) are simply secure serial EPROMs or EEPROMs and can be read without the need of intricate hardware or software.

Shown is the simplest possible arrangement, based upon a direct connection of the smart card socket to the parallel printer port of any PC *(Fig. 1)*. Only a spare 5-V power supply is needed, possibly borrowed from an unused "joystick" port. The 15-ohm resistor is needed to avoid any short-circuits when anything but a true smart card is inserted into the connector.



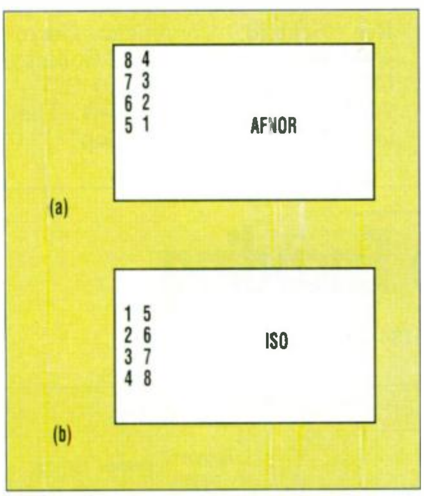
1. THE SIMPLEST APPROACH for synchronous cards uses a direct connection socket to the PC parallel port.

Two layouts can be found for the flat contacts on the card itself. Figure 2a shows the oldest one (AFNOR), mainly used in France, and figure 2b, the internationally approved one (ISO). It should be stressed that on most modern cards with their contacts in the ISO position, contacts #4 and #5 are not used, and are often omitted.

Smart card connectors are usually fitted with a full set of sixteen wipers; eight for the contacts in the AFNOR position, and eight for the contacts in the ISO position. It is a good practice to parallel the wipers with the same number in both sets.

Read operations can be performed by means of very simple software. For example, the short Turbo-Pascal program shown in figure 3a. It uses the LPT1 port to send "micro-instructions" to the smart card, and to sense the bits that the card outputs on its data line (contact #7).

The instruction set used here is the



2. TWO LAYOUTS are attributed for the flat contacts on smart cards. fig. 2a shows AFNOR (the oldest one), and Fig. 2b shows the internationally-approved ISO layout.

(a)

```
uses crt;
var a,e,f,g:integer;
  begin
  clrscr;
  port[888]:=0;
  port[888]:=250;
  port[888]:=248;
  clrscr;
  for f:=1 to 8 do
   begin
   for g:=1 to 32 do
     begin
     port[888]:=249;
     delay(1);
     e:=port[889];
     a:=e and 128;
     if (a=128) then write('0 ') else write('1 ');
     port[888]:=251;
     end;
   writeln;
   end;
end.
```

(b)

```
1 0 1 1 1 0 1 1 0 0 0 0 0 0 1 1 0 1 1 1 0 0 0 1 0 1 0 1 0 0 1 1
1 1 0 0 0 0 1 1 0 1 0 1 0 1 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 1 1 0
1 1 0 0 0 0 1 1 0 1 0 1 1 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 1 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1
```

3. A SHORT TURBO-PASCAL PROGRAM can perform read operations. Fig. 3b's program lists all 256 bits of memory.

```
(a)

uses crt;
var a,e,f,g:integer;
  begin
  clrscr;
  port[888]:=0;
  port[888]:=252;
  port[888]:=254;
  port[888]:=252;
  port[888]:=248;
  clrscr;
  for f:=1 to 16 do
   begin
   for g:=1 to 32 do
     begin
     port[888]:=248;
     delay(1);
     e:=port[889];
     a:=e and 128;
     if (a=128) then write('0 ') else write('1 ');
     port[888]:=250;
     end;
   writeln;
   end;
end.

(b)

1 0 0 0 0 0 0 0 0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 0 1 0
1 1 1 0 1 0 1 0 0 1 0 0 1 0 0 1 0 1 0 0 0 1 1 0 1 1 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

4. FIG. 4a IMPLEMENTS THE INSTRUCTION SET of most smart cards used in Europe. Fig. 4b shows the results obtained with a recent German phonecard.

one for Gemplus GPM256-type cards, 256-bit OTP EPROMs used as token holders in many applications (for example, prepaid telephone cards in France and in most countries of the world). The program lists all 256 bits of the memory *(Fig. 3b)*. The second program listing implements the instruction set of "Eurochip" cards, secure EEPROMs that are widely used for third-generation prepaid telephone cards in some European countries using the German system *(Fig. 4a)*. Figure 4b shows the results obtained with a recent German phone card, the extra bits of which are used to implement some type of cryptographic protection.

It is worth noting that even such a simple reader could well be used to grant access to a PC or software or data files, only to the bearer of a suitable smart card (used prepaid telephone smart cards usually still contain a unique serial number that cannot be forged easily). □

IFD Winner

IFD Winner for February 5, 1996

Rea Schmid, Comlinear Corp, 4800 Wheaton Dr., Fort Collins, CO 80525-9483; tel: (970) 225 - 7421; fax: (970) 226 - 0564. The idea: "Wideband AGC Loop"

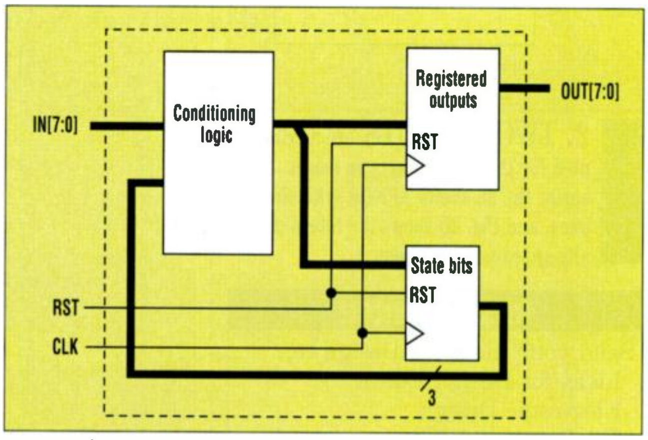
CIRCLE 521

Registered Outputs In State Encoding

CHRIS JONES, Cypress Semiconductor, 3901 N. First St., San Jose, CA 95134-1599.

A critical element in state machine design is the state encoding. A fully encoded scheme that is either sequential or gray uses the least number of flip-flops for holding the state information, while a one-hot-one encoding employs more flip-flops and reduces the next state and output logic. In some cases, however, using registered outputs as part of the state encoding provides a solution that lies between these two alternatives.

Consider the state machine as described in the state table *(see the table)*. (This may be familiar since it is PREP benchmark #3, the small state machine.) The XX entries in the IN[7:0] column indicate a "don't care" input condition. Figure 1 shows the block diagram for this state machine where eight outputs are registered. With eight states, sequential encoding would require three macrocells within a CPLD. The eight



1. THREE STATE BITS are required for fully encoding the state information, and the eight outputs are registered.

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	POS-150	75-150	-103	-23	20	11.95
	POS-200	100-200	-102	-24	20	11.95
	POS-300	150-280	-100	-30	20	13.95
	POS-400	200-380	-98	-28	20	13.95
	POS-535	300-525	-93	-26	20	13.95
	POS-765	485-765	-85	-21	22	14.95
	POS-1025	685-1025	-84	-23	22	16.95
NEW	POS-1060	750-1060	-90	-11	30*	14.95
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NEW	POS-2000	1370-2000	-95	-11	30*	14.95

*Max. Current (mA) @ 8V DC.
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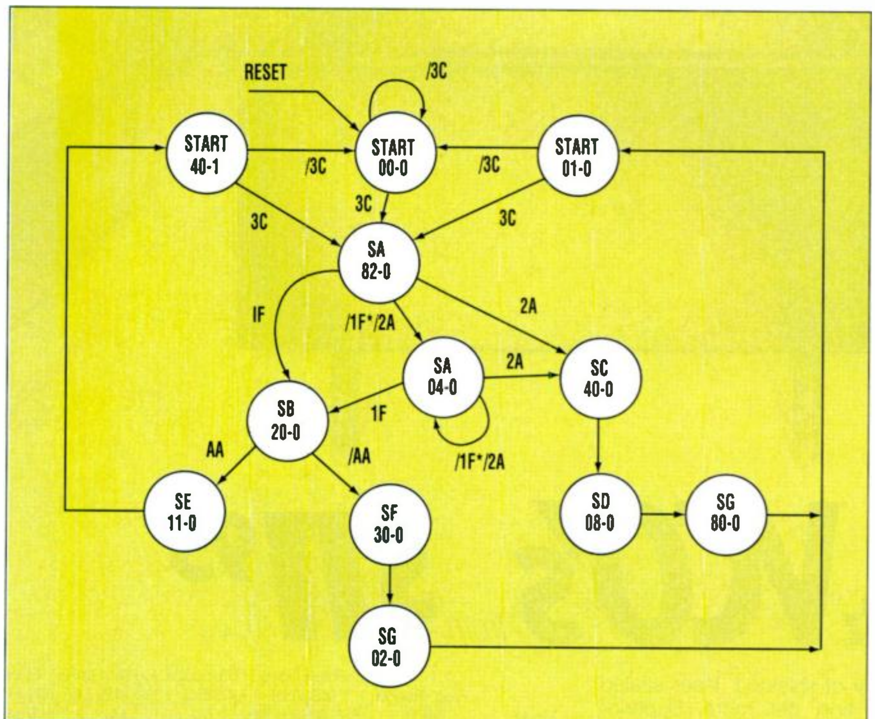
registered outputs require eight more macrocells, bringing the total macrocell requirement to eleven. When this state machine is implemented in a Cypress CY7C371 32-macrocell CPLD, 11 macrocells and 41 product terms are required, with some macrocells utilizing the T flip-flop and others the D flip-flop that is provided.

Since the outputs are registered, they can be utilized to help encode the states. This requires that the OUT[7:0] bus should be an input into the conditioning logic, but there is no adverse impact on performance in a CPLD *(Fig. 1, again)*. If the output vector is unique under every condition, then these registered outputs can also be used as the entire state information. However, referring back to the table, the 8-bit outputs are not unique, since 40 is the output when transitioning either from SA to SC or from SE to START. This then requires one extra state bit to differentiate these two identical outputs in the two different states. If any output vector value occurs in more than two spots, enough additional state bits are required to uniquely identify the different states.

STATE TABLE

Current State	IN[7:0] (hex)	Next State	OUT[7:0] (hex)
START	/3C	START	00
START	3C	SA	82
SA	/1F*/2A	SA	04
SA	1F	SB	20
SA	2A	SC	40
SB	AA	SE	11
SB	/AA	SF	30
SC	XX	SD	08
SD	XX	SG	80
SE	XX	START	40
SF	XX	SG	02
SG	XX	START	01



2. THE 8-BIT OUTPUT VECTOR is used in the state encoding with one additional bit that differentiates state SC from state START when the output is 40.

The equivalent state diagram shows the first two of the three digits in each state are the hexadecimal representation of the 8-bit output vector *(Fig. 2)*. The last digit in each state is the single bit that differentiates the two states that have identical "40" outputs—state SC and state START (arriving from state SE).

The implementation in a CY7C371 now requires 9 macrocells and 44 product terms, so less macrocells are required at the expense of more product terms. The product term expense is quite small, and in part is due to more macrocells using the T flip-flop. The real gain is that three of these state machines will now fit in the 32-macrocell CY7C371, since only 27 macrocells are required for the three instances. ☐

CIRCLE 522

Recovering From Power Fluctuations

ALFREDO CHINGCUANCO, Z-World Engineering, 1724 Picasso Ave., Davis, CA 95616; (916) 757-3737; fax (916) 753-5141.

Embedded systems often employ power-failure-detection circuits like that shown in Figure 1a. A common power-management IC, the 691 (Maxim, Linear Technology, and Analog Devices), monitors a simple voltage divider. The IC generates a nonmaskable interrupt (NMI) to the system microprocessor when the *raw* dc input falls below a certain level (1.3 V for the 691). R1 and R2 are chosen such that the power-management IC generates an NMI before the *unregulated* dc input droops low enough to shut down the system microprocessor.

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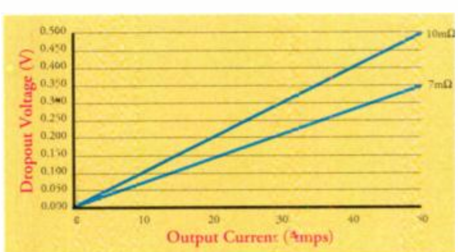

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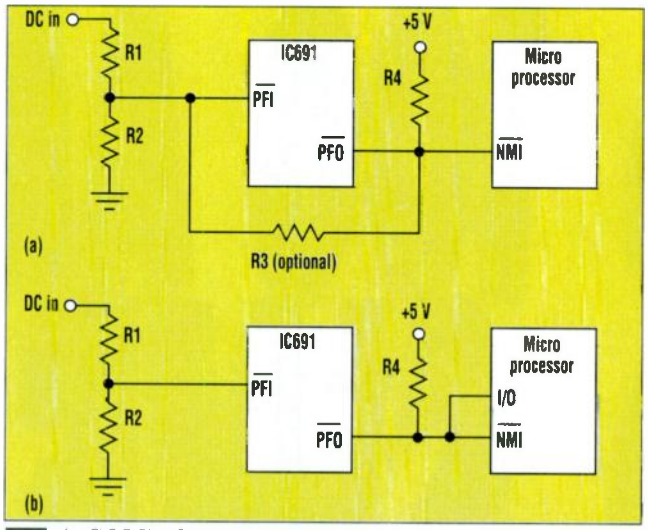
MICREL SEMICONDUCTOR

High Performance Analog Power ICs

READER SERVICE 143

tiple power fluctuations follow each other rapidly—a common occurrence in the real world. Many microprocessors overwrite vital state registers as a part of their nonmaskable-interrupt responses. If a second NMI occurs before the micro processor finishes its power-failure-interrupt routine, the microprocessor can't restore its original, pre-power-failure state. Also, depending on the number of fluctuations of the raw dc input (and, hence, the number of stacked NMIs), the microprocessor's stack could possibly overflow, corrupting your program's code or data.



A COMMON POWER MANAGEMENT IC can fail when multiple power fluctuations follow each other rapidly (a). Allowing the system microprocessor to sample the state of the power-fail signal (PFO) protects the system from errors arising from multiple NMIs during brownouts (b).

Following the manufacturer's recommendations to add an optional hysteresis resistor (R3) around the 691 won't solve the multiple-fluctuation problem if input-power excursions exceed the hysteresis band. The hysteresis voltage is:

$$V_{hysteresis} = V_H - V_L$$

$$V_H = 1.3 \times [1 + R1/R2 + R1/R3]$$

$$V_L = 1.3 \times [1 + R1/R2 - (5\ V - 1.3\ V)R1/1.3\ V(R3 + R4)]$$

where R1 = 51 kΩ; R2 = kΩ; R3 = 300 kΩ; R4 = 10 kΩ; and $V_{hysteresis} \approx 830$ mV.

Having the system microprocessor read the state of the power-management IC's PFO line is the key to handling multiple power fluctuations. Figure 1b shows the PFO connected to an I/O line of the system microprocessor as well as its NMI input. As a result, the microprocessor can determine if the raw dc input either is still in a low-voltage (or "brownout") state or has returned to the normal operating level.

The program *(see the listing)* is for the Zilog Z180 but can be adapted easily to other processors. In response to a power-failure NMI, the Z180 saves its program counter on its processor stack. It copies its maskable interrupt flag (IEF1) to another internal register (IEF2) and zeros IEF1. The Z180 later restores saved state information when it executes a RETN (return from NMI) instruction. To prevent corrupting the system stack, the routine reserves memory for its own stack.

The program assumes that system's watchdog timer (if any) has been enabled. When the 691 detects a brownout and asserts PFO, the system microprocessor begins executing the interrupt-service routine in the program. The routine first takes care of saving the system's vital state data.

While responding to a power-failure interrupt, the interrupt-service routine can save only a finite amount of state information. The amount of code the microprocessor can execute to save the data depends on the decrease rate of regulated dc voltage after the raw dc voltage drops below the power-failure threshold.

The routine then enters a loop, checks the status of the PFO line and resets the watchdog timer. When the power returns, the program exits, either allowing the watchdog timer to reset the system or jumping to a Reset routine, as needed. The routine never returns from the first NMI, eliminating concerns about multiple NMI interrupts. □

```
main() {
   ...
}
...
char dummy[24]            ; temporary stack for interrupt routine
...
#define PFO_BIT 6         ; test bit for checking /PFO's state

#JUMP_VEC NMI_VEC myint         ; declare interrupt vector

#asm
myint::                  ; label for interrupt routine
   ld    sp,dummy+24     ; force stack pointer to top of array dummy
                         ; to prevent overrunning stack

Do whatever service possible here, within allowable execution time.
Then:

loop:
   call hitwd            ; "hit" watchdog to prevent its timing out
                         ; during brownout
   ld    bc,PFO          ; set up for reading /PFO's state
   in    a,(c)           ; read /PFO state
   bit   PFO_BIT, a      ; check state of /PFO
   jr    z,loop          ; wait until the brownout condition clears

timeout:                 ; then...a tight loop to force a watchdog timeout
   jp    timeout         ; This loop will eventually reset the Z180
#endasm

If your watchdog is not enabled or your system lacks one, you can force
the microprocessor to restart execution at 0x0000. Substitute this program
fragment for the ''timeout'' fragment above.

   restart:
      ld    a,0xe2           ; set up Z180 MMU
      out0  (CBAR),a         ;    "     "
      jp    0000h            ; jump to 0x0000
```

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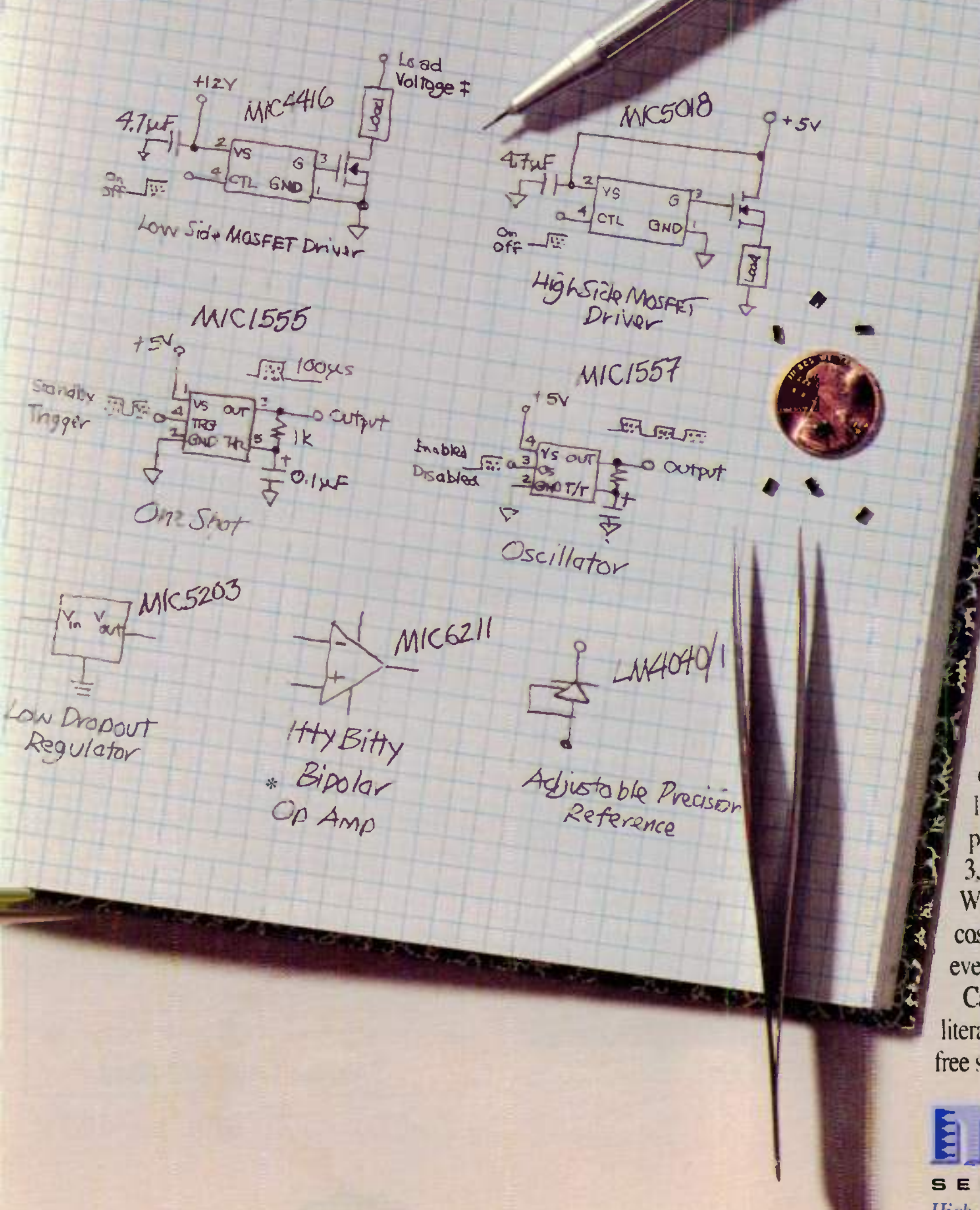

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What's All This Training Stuff, Anyhow?

Over the years, the British Royal Navy always had a good number of ships. In 1796, about 600 ships were in their fleet, including Ships Of The Line, Frigates, and Sloops. All powered by sails. In 1896, there were about 220 ships—all steam-powered. Those numbers are approximate, per my 1894 *Encyclopedia Britannica*.

In those days, every ship needed a navigator. You couldn't go out on the open seas and get where you were going without a good navigator. So every ship in the Royal Navy had a Navigator. Young gentlemen spent five years in the Navy's War college, getting a fine education. After graduation, Navigators were typically assigned to small ships, and after considerable seasoning, became qualified to be the Navigator on a Ship Of The Line.

BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

A Navigator was entrusted with a ship worth hundreds of thousands of pounds, with hundreds of sailors. Everybody respected the Navigator. The enlisted men couldn't just overpower the officers, and mutiny, and kill or cast off the Navigator. Without the Navigator and his five years of education, they would never get home. So, the mystique of the Navigator was one contributor to the stability of life aboard ship.

About 1936, the Royal Navy faced a serious problem. With the winds of war whipping up all around Europe, the Royal Navy had to make plans to expand. The Navy would need hundreds of new ships. And, thus, it would need hundreds of new navigators. Ahem.....

How could the Navy get hundreds of navigators in such a short time? If the lead time is five years, then they would have had to start ~~training~~ educating their navigators two or three years previous to that. What to do?

In the end, pragmatism won out over tradition. Bright young men good at math and science were thrown into a newly-planned crash course in navigation. After six months, some pretty good navigators came out of the Naval College and were assigned to ships. Perhaps these navigators were not quite as well-grounded or well-rounded as the traditional ones, but they received some very good training. They were supplied with good reference books, good tools, sextants, and charts, and with good radio navigational aids. The advent of radar didn't do any harm. So when war came down on Europe in 1938, the Royal Navy had lots of problems, but a shortage of Navigators wasn't a significant one.

John Christensen, one of our Applications Engineers who is an experienced sailor, pointed out that any good Community College can teach you a course in navigation in six or eight weeks, with just one evening of classes per week. Any fairly thoughtful person can, with a small modern calculator, master the art of navigation in a *whole lot* less than 6 months.

In fact, John said he taught his wife Felicity the art of navigation in one morning. However, that's an unfair comparison: She is intelligent, and John was sober (or so he claims).

Here at National Semiconductor, we have some very good training programs. We also have, as I'm sure you'll suspect, some mediocre ones, and a few outright lousy ones (remember "Apples and Oranges"?). Still, our training programs have expanded, and the number of things you can learn cover a wide range from Solid-State Physics to The Path of Dialogue, from Digital Signal Processing (DSP) to Doing Business in India (or China or Japan). We have 8-D Problem Solving, and we have Electronics for Non-Technical People. There are courses in Team Leadership, and in Team Followership. (Heck, if you have a team with "All Chiefs and No Indians," that usually doesn't work well.)

Still, every time I see a catalog of courses from our Training Center, I think about trained bears. And trained monkeys. Yes, training is sometimes suitable for animals. And sometimes it's suitable for people to do certain jobs. But, as you may have noticed by now, I prefer Education. I like to see people think about what they're doing and understand it so when something goes wrong, they can figure out what to do, or call in the right experts. If the guys at Chernobyl were EDUCATED instead of merely *trained*, would they have made less of a botch? Or at Three Mile Island? (Maybe they were educated *just a little*, and we should all be aware that a *little* education is a dangerous thing...)

I was recently invited by our Training Center to help plan the training of technical people in various analog techniques. First, we were told we should make some plans to have an Analog Forum, so that Analog Experts could lecture to Analog people on Analog topics. Some parts of that plan sounded like good ideas, but we really have to make the program open to all NSC employees. People who have never worked with analog circuits or analog systems need to learn about this strange analog world. Okay, I got some approval on that.

Next, I'll have to go discuss with our Training experts, Sharadon Smith and some other people, the idea of offering some Analog *Education*. I can't think of many things I know that I could TRAIN people about Analog. But there are a lot of topics

PEASE PORRIDGE

where I might *educate* people.

Sharadon and I aren't far apart, not in any big disagreement, as we discussed by phone and e-mail. We agree that there's a continuous spectrum of gradations between *training* and *education*, and we're interested in all of these, as appropriate. We agree on the need for *learning*, so that people can apply their knowledge—especially in ambiguous or unexpected situations where you can't expect training to tell you what to do. That sounds like *education* to me.

We also agreed that any such learning is best when you can start using it right away. Education that will only be useful in the far future isn't likely to stick and may be of doubtful value (don't get me started on how I took Fourier Analysis as an MIT freshman, and that it wasn't until a couple of years later when my engineering instructors told us it was supposed to be *useful* for something....)

Don't take what I said the wrong way, though. If kids are learning to drive, they need Driver Training as well as Driver Education. They need to learn situations on when it's correct to slow down and *think* about a problem. They also must learn when thinking or cogitating is WRONG, when they must respond reflexively, and do what they trained themselves to do. If a dog jumps out in front of you on an EMPTY freeway, you do one thing. If a dog jumps out in front of you on a CROWDED freeway, you do something different. If a DEER jumps out in front of you, you do something different yet. You must know in advance what to do in each of these cases.... I wrote about this back in December of 1991, and I'll write about it some more in a few months.

Still, there's a real difference between Training and Education. Think of the difference if your kid comes home from school and says, "We had Sex Education Class today," as compared to "We had Sex Training Class today." *Vive la différence!*

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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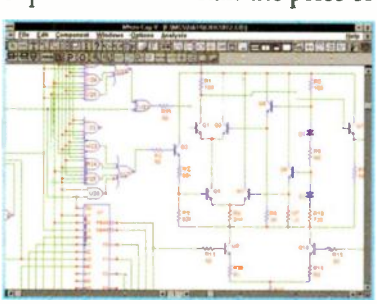

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Configuring An Off-The-Shelf PFC Supply

Here's how to design IEC-compliant compact supplies using readily available components.

BY RICHARD OKADA and STEVE KELLER

RO Associates Inc., 246 Caspian Dr., P.O. Box 61419, Sunnyvale, CA 94088; (408) 744-1450.

Speeding up the design cycle has long been a crucial goal of design engineering, and configuring power supplies with proven, modular components can help. Power-supply design cycles are generally 75% to 85% shorter with modules than with the more traditional approach that uses discrete ICs, transistors, and magnetics. What's more, choosing modular components that already meet UL, CSA, and other agency standards makes certification of the supply as a whole a much quicker process.

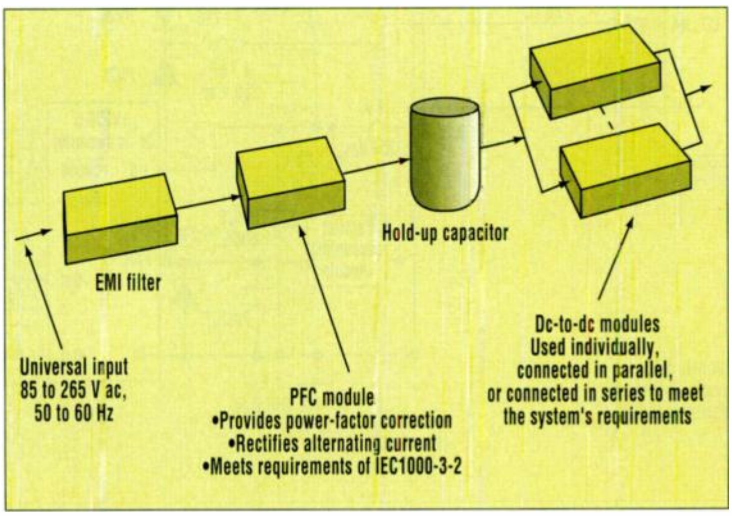
Module-based power supplies offer a number of benefits that ultimately result in lower cost of ownership. For instance, the modules are already debugged, so field reliability is higher. Output-power capability, hot-plug-in capability, redundancy, and other features can be configured to the customer's exact needs *(Fig. 1)*. Serviceability is enhanced and maintenance costs are reduced because modules can be readily replaced. And you can easily keep up with the shifting sands of IC operating voltages by substituting modules with alternate output voltages.

Another factor favoring the modular approach is the arrival of the IEC specifications that took effect last January. They place tight restrictions on the EMI and power-factor performance of power supplies sold in Europe. Many modular power-supply component suppliers, including RO Associates, offer power-factor-correction (PFC) modules and EMI-filter modules that enable designers to quickly meet the latest IEC regulations.

The following configuration suggestions were derived from the design of a 5-V power supply with PFC, N+1 redundancy, and current sharing. We'll begin by examining a schematic that shows one of the redundancy blocks for this supply *(Fig. 2)*. This block is repeated N+1 times to obtain the required output power with redundancy. The design is based entirely on off-the-shelf modules, which are shown in the schematic with heavy outlines. As with most supplies, this design can be divided into two sections—an input stage and an output stage. The input stage converts the ac-input power into high-voltage dc power. The output stage then converts the high voltage dc power into isolated, low voltage output power.

First, we'll look at the input stage in some detail. The PFC module is the main component of the input stage. Its primary function is to convert the ac input power into dc output power. The difficult part of this conversion is meeting the constraint that the input power factor must be near unity. This requires that the instantaneous input current be proportional to the instantaneous input voltage. In other words, the PFC module has to look like a resistive load to the ac power source. Power-factor regulations are set forth in the new IEC specification, IEC 1000-3-2. Most PFC modules contain a diode bridge to convert the bipolar input voltage into a unipolar, half-sine wave. They then convert the rectified voltage to a higher dc output voltage using a boost-topology dc-to-dc converter. A simplified diagram of this approach is shown *(Fig. 3)*.

There are two characteristics of the boost-topology dc-to-dc converter that significantly affect the PFC module's design and application. First, the



1. The modular building-block approach to power-supply design enables designers to configure power supplies that meet the latest international specifications for power-factor correction. By using modules that have already been UL-approved, the design and qualification cycle is dramatically shortened.

output is not isolated from the input. This means that the high-voltage bus is considered to be a "primary circuit" by the safety agencies, and that all of the safety regulations that apply to primary circuits also apply to the outputs and status signals of the PFC module.

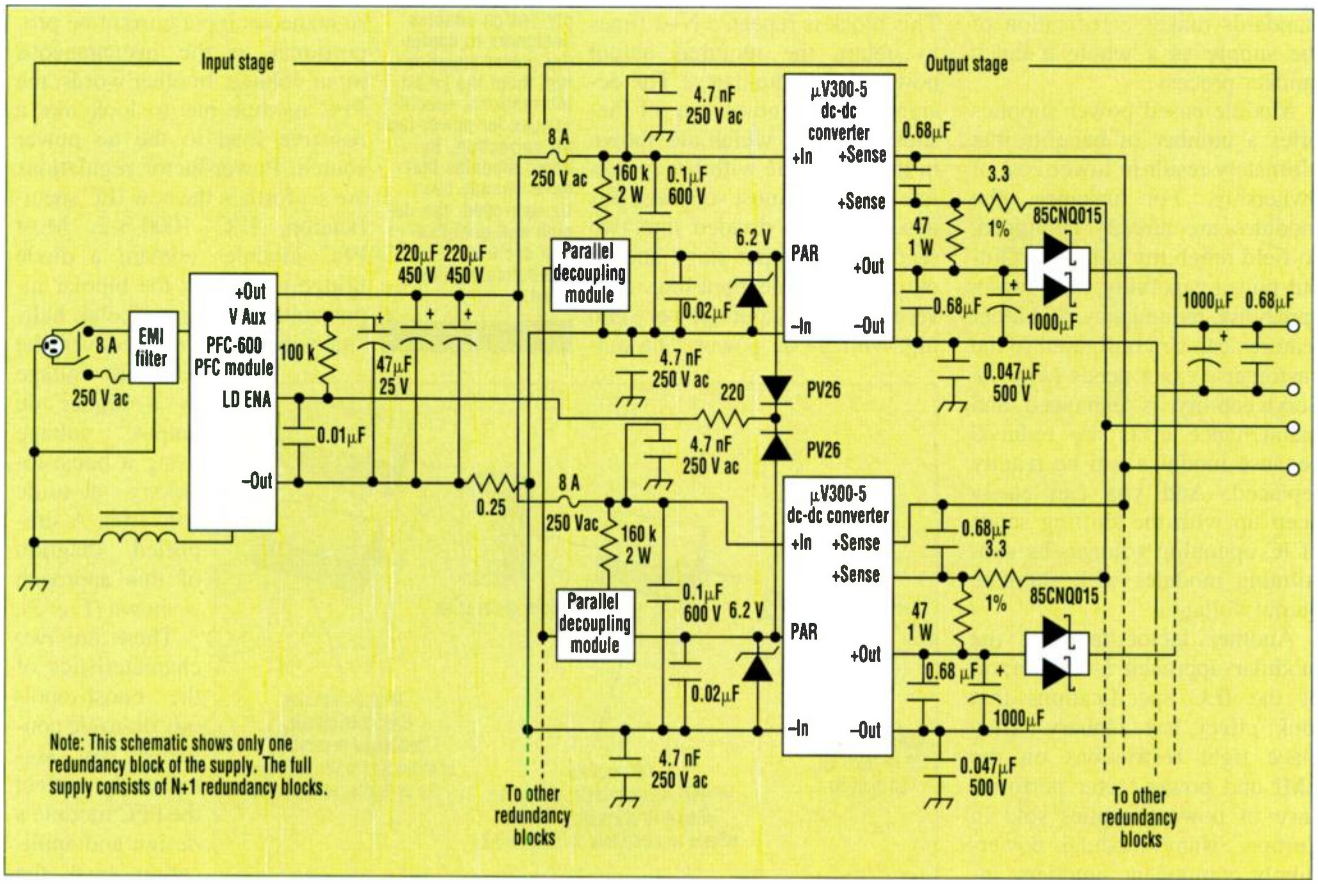
The second characteristic is that the output voltage must always be higher than the input voltage. This characteristic has two consequences in a PFC module: The output voltage must be very high to operate from a utility line, and the converter is not inherently protected against short circuits or current limited. A benefit of the first consequence is that if the output voltage is high enough to operate from the highest utility voltage, the module can then operate from any utility voltage. Currently, the highest utility voltage is 264 V ac, which has a peak voltage of 373 V. Therefore, for a PFC module to have a truly "universal" input range, the regulated output voltage must be higher than 373 V, and is typically set around 380 V. The fact that the boost converter is not short-circuit protected requires the module manufacturer to add a protection circuit. This is typically accomplished by placing a solid-state series switch in the output stage of the PFC module *(Fig. 3, again)*.

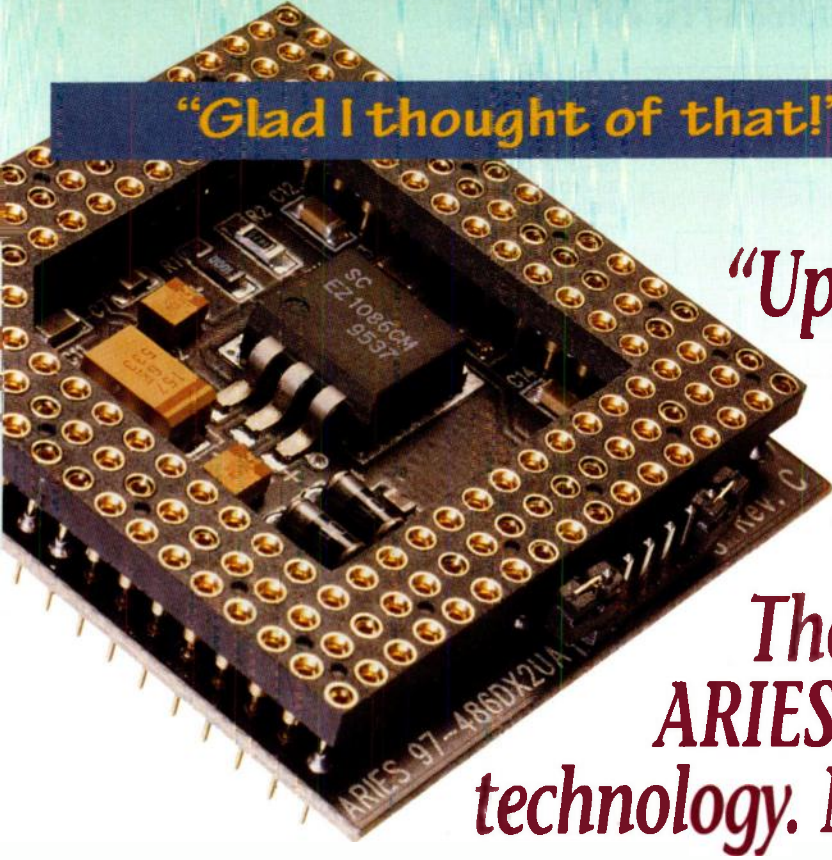
Paralleling PFC modules for higher-power applications must be approached with great care. When PFC modules are paralleled, the internal bridge rectifiers will not share current equally between the modules. In some applications this may be acceptable as long as the total input current for the system doesn't exceed the current rating of one of the PFC rectifier diodes. High-power applications, however, require special techniques to parallel PFC modules.

There's a simple, cost effective way to force the paralleled rectifiers to properly share the return current *(Fig. 4)*. This approach places a resistor (R_S) in series with the return pin of each PFC-module output. The resistor improves the current sharing by reducing the sensitivity of the return current to the voltage drop across the diode-resistor combination. Load sharing between the PFC modules is enhanced in this approach by using parallelable dc-to-dc converters. The approach shown in Figure 4 ensures PFC-module load sharing by connecting the same number of output modules to each PFC module. The fact that the output modules are sharing the load will force the PFC modules to do the same. This approach can even be extended to provide N+1 redundancy. Other approaches to load sharing use PFC modules that have built-in current-sharing provisions. These approaches are similar to those used to parallel dc-to-dc modules, which are discussed later in this article.

2. This modular power supply can be easily expanded to provide more power by adding more redundancy blocks. The parallel decoupling modules (PDMs) instantly decouple a dc-dc module if it should fail, enabling the power supply to continue performing without interruption.

PFC modules require an input-EMI filter for proper operation. The filter performs two functions: It protects the external world from the switching noise generated by the PFC module, and it filters externally generated noise before it can reach and disturb the PFC module. The EMI filter should have one or more





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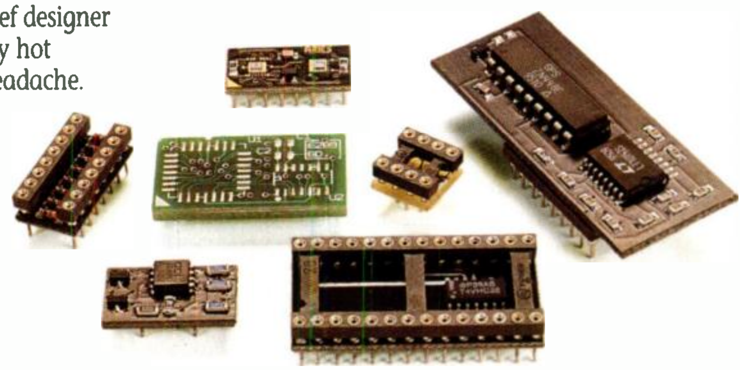

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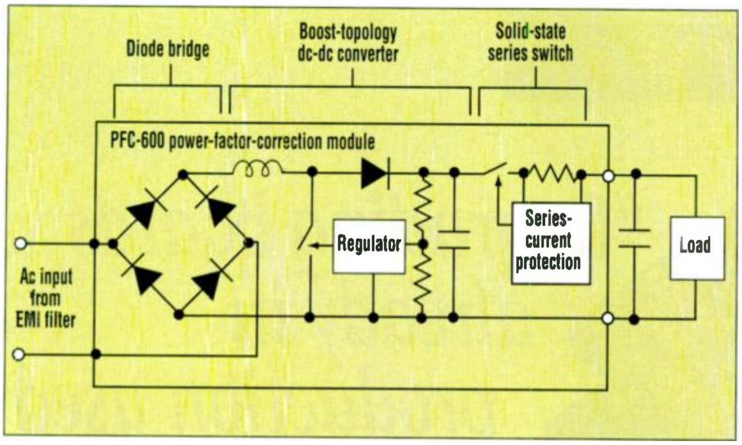


3. This simplified PFC-module diagram shows the basic structure of a PFC converter. Most PFC modules contain a diode bridge to convert the bipolar input voltage into a unipolar, half-sine wave.

capacitors on its output (the PFC-module side) to ensure that it presents a low source impedance to the PFC module at the module's switching frequency. If the EMI filter doesn't have sufficient capacitance, or if the EMI filter is remotely located, an agency-recognized X capacitor[1] should be added across the line at the PFC module's input. Because a PFC module can generate significant amounts of high-frequency noise, it'll require a fairly large EMI filter. As a rough estimate, the volume of the filter will be two to three times the volume of the PFC module.

For proper operation, PFC modules require holdup capacitors in addition to an EMI filter. The amount of holdup capacitance across the PFC module's output is based on the required holdup time. The holdup time is determined by the length of time that the supply must be capable of running without any input power. A typical range of holdup times is 20 ms to 50 ms. The required capacitance is calculated by balancing the energy lost by the capacitor with the energy used by the load (including the dc-to-dc converters) using:

$$C = \frac{2PT_{hold}}{V_1^2 - V_2^2}$$

where C is the required holdup capacitance in farads, P is the load power (including the dc-to-dc converters) in watts, T_{hold} is the holdup time in seconds, V_1 is the output voltage of the PFC in volts, and V_2 is the minimum input voltage of the dc-to-dc converters in volts.

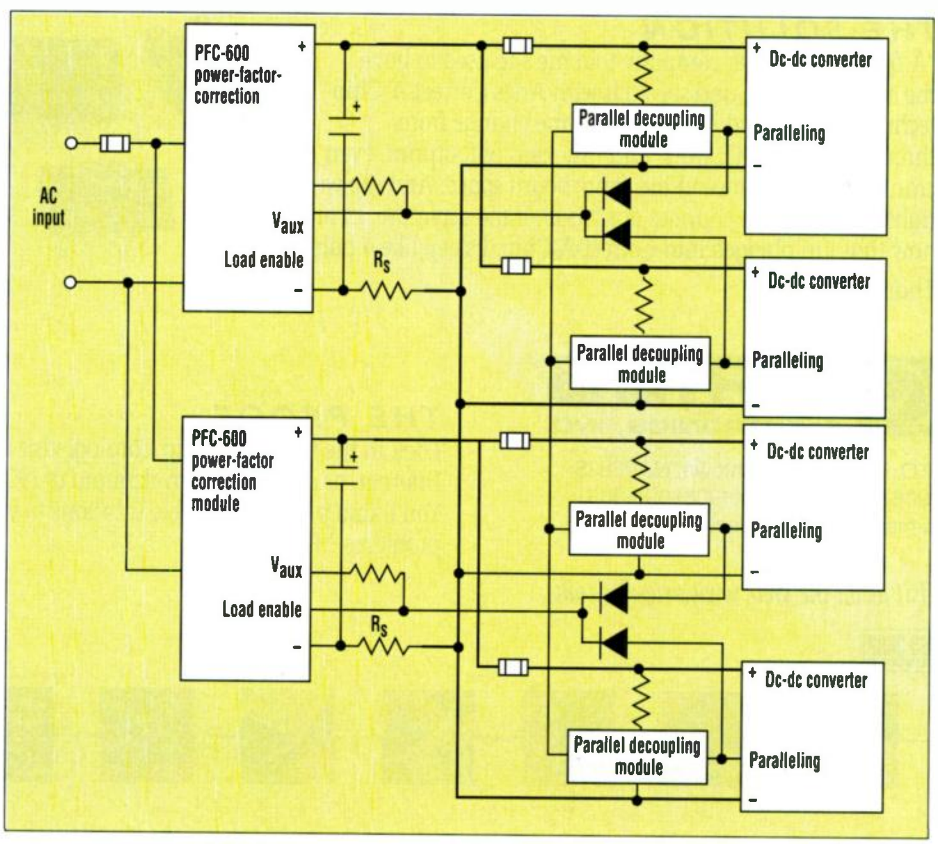
When selecting capacitors to provide the required holdup capacitance, pay attention to the capacitors' voltage and ripple-current ratings and to the minimum capacitance over the operating temperature range of the supply. Capacitors, especially electrolytics, can lose a significant percentage of their capacity at low temperatures.

We'll now turn our attention to the supply's output stage, which is made up of one or more dc-to-dc modules that convert the high voltage from the PFC module into the desired output voltages. The first step in selecting the output modules is to determine the output voltage and current requirements. Once the designer has determined those parameters, the next step is to select the modules that will fulfill them from a supplier's catalog. Dual- and triple-output modules are more cost-effective than multiple single-output modules. The most important features to consider when selecting a module are: Cost, efficiency, footprint, agency approvals, reliability, and power density. Some other module features to consider are: Maximum operating temperature, thermal protection, parallelability, input and output overvoltage protection, short-circuit protection, and available status signals.

High-power systems can benefit from the advantages of modular components by connecting several dc-to-dc modules in parallel. The parallel connection allows a group of modules to achieve higher current levels than are available from a single unit. To ensure that all of the modules share the load current equally, it's necessary to connect a control signal to each module.

Output trimming allows the de-

4. A simple approach for paralleling PFC modules forces the diode bridges to share current by placing a small resistor (R_S) in the return path. Load sharing is enhanced by using current-sharing converters for the load.



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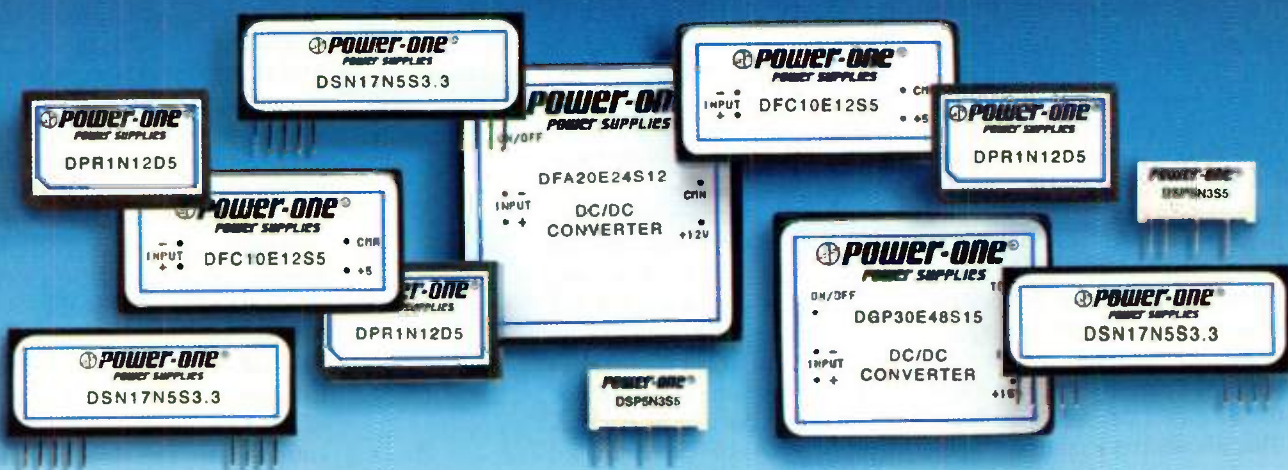

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DFA6	6	9-27, 20-60		•	•		•		•	
DFC6	6	3.5-16		•	•		•		•	
DFC10	10	9-18, 18-36, 36-72	•	•			•		•	
DGP12	12	3.5-16		•			•		•	
DFC15	15	20-60		•			•		•	
DSN17	17	4.5-6, 6.5-15.5	•	•						
DFA20	21	9-18, 18-36, 36-72	•	•			•		•	
DGP30	30	36-72		•			•		•	
Dual Output products provide the indicated Vout as one positive and one negative output										
DSP1	1	4.5-5.5		+/-		+/-	+/-	+/-	+/-	+/-
DFC10	10	9-36, 18-72		+/-			+/-		+/-	
DGP12	12	3.5-16		+/-			+/-		+/-	
DFC15	15	20-72					+/-		+/-	
DFA20	20	9-18, 18-36, 36-72		+/-			+/-		+/-	
Triple Output products provide a main output (•) and two symetrical outputs (+/-)										
DGP20	20	9-18, 18-36, 36-72		•			+/-		+/-	

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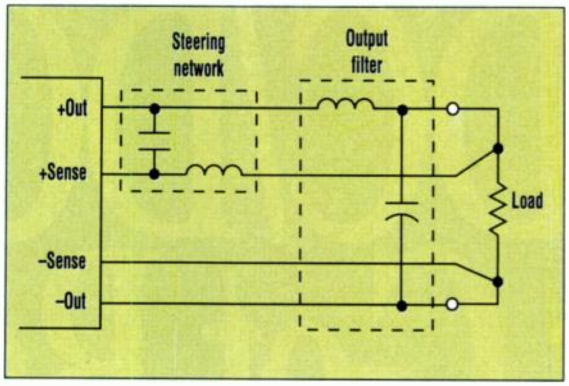
signer to make adjustments in the output voltage. Almost all modules that have an output-trim feature can be trimmed by ±10%. Some modules can be trimmed down by as much as 40%, albeit with slightly reduced output performance. The upper end of the adjustment range is usually limited by the overvoltage-protection circuit in the dc-to-dc module. The most common use of the trim feature is to obtain nonstandard output voltages. This allows designers to achieve nearly any output voltage while stocking only a few standard modules. Other uses include distribution-loss compensation, voltage margining, and remote programming. When designing for an application requiring a trimmed module, the designer must observe both the maximum output power and the maximum output current ratings of the module. For example, a 200-W, 5-V, 40-A module trimmed to 4 V will only be capable of providing 160 W because of its maximum current rating.

Remote sensing moves the point of voltage regulation from the module's output to the load. This allows the module to compensate for voltage drops in the power-distribution system. The voltage drops are generally due to resistive losses in the PCB traces and connectors as well as voltage drops across ORing diodes. Most modules can compensate up to 0.5 V or 10% of the nominal output voltage, whichever is greater. The limiting factor in how much drop can be compensated is the module's overvoltage-protection circuit.

Remote sensing is usually straightforward, but there are a few caveats to observe:

•The sense leads of the module must always be connected. If the design is such that the sense leads can fail open or can be left unplugged, then connect 100-Ω resistors from each sense pin to the corresponding output pin (such as from +SENSE to +OUT).

•Do not sense around a low-frequency output filter. Sensing around an output filter will place the filter in the module's feedback loop and can cause instability. Consider using trimming instead of remote sensing if your application requires an output filter whose corner frequency is near, or below, the loop-crossover frequency of the module. If both remote sensing and a low-frequency output filter are needed, it may be necessary to use a frequency-selective steering network *(Fig. 5)*.



5. If both remote sensing and a low-frequency output filter are required, it may be necessary to use a frequency-selective steering network.

•Protect the sense signals from noise sources by bypassing the sense signal at the load and shielding the sense lines. For best performance, the bypassing should consist of both an electrolytic (or tantalum) capacitor and a ceramic capacitor in parallel. Shielding can be accomplished by using shielded twisted-pair or coax cable, or by burying the sense traces between ground planes in applications where they are routed through a PWB.

Fault tolerance is a power-supply feature that is being required much more often these days. In a fault-tolerant system, the outputs are unaffected by one or more component failures. The best way to achieve fault tolerance is to use N + M redundancy. It's here that the modular approach has the most advantages. In this scheme, N is the number of modules required to provide full power to the load, and M is the number of extra modules used in the system. M typically ranges from 1 to 3. That way, if one of the modules fails, the system still can supply full power to the load until the damaged module can be replaced. For this scheme to work, the failed module(s) must decouple from the input power, the output power, and the current-sharing control busses without any significant effects.

Input-bus protection is accomplished by placing a fuse in series with the +IN pin of each module. The fuse should have a current rating that's higher than required by the dc-to-dc module, but is lower than the output-current rating of the PFC module. This ensures that the fuse will open if the modules fail.

The output bus can be protected by placing an ORing diode in series with each module's output. Therefore, if a module fails with a short on its output, the diode will be back-biased and the output bus will be protected. Choose diodes that exhibit a very low forward-voltage drop such as Schottky diodes. One important thing to note about a diode is that the forward voltage decreases as the diode temperature rises. Therefore, to improve efficiency, it's better to allow the diode to run a little warm under normal operating conditions. A good compromise temperature is 70°C. This allows a low forward-voltage drop without degrading reliability.

Good pc-board layout practices are critical in realizing all of the benefits of using modular components. The three key factors governing the layout of a modular power supply are grounding, noise prevention and abatement, and component mounting and placement. Keeping these factors in mind when creating the layout will speed the overall design and debug cycle.

We recommend using a four-layer board to implement a good grounding strategy. Use the two outer layers for split power and ground planes, and the two inner layers for low-level signals. Where necessary, add extra planes to the inner layers to beef up the high-current paths. The top layer, located closest to the modules and components, should be divided into four sections. The goals in providing all of these sections on the top layer are: (a) to minimize the loop area of any generated noise; (b) to shield the low-level signals from noise emitted by the modules; and (c) to provide a safe place on which to mount the modules and components. The remaining layers

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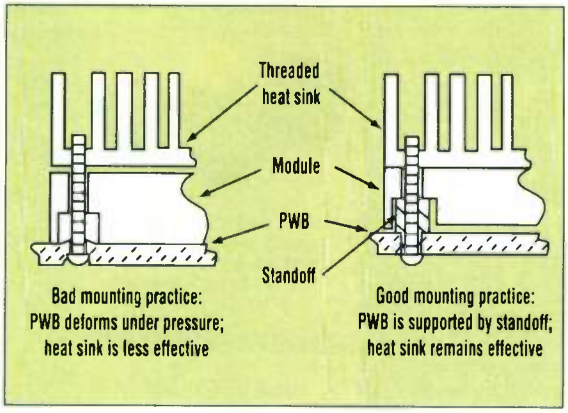
should be designed around the top layer. Note that there shouldn't be any traces or planes crossing the gaps between the sections of the top layer. If there are, then those signals may be quite noisy and could couple noise to other traces.

The four sections of the top layer are: (1) the chassis ground plane; (2) the dc-to-dc-converter input-return plane; (3) the dc-to-dc-converter case ground plane; and (4) the power-supply output-return plane(s). The chassis ground plane provides a ground path to the EMI filter as well as shielding for the PFC module. The PFC module's case should be connected to the chassis ground plane through an inductor or ferrite bead. The dc-to-dc-converter input-return plane shields any input-referenced control signals and provides a safe mounting point for the holdup capacitors.

The case ground plane for the dc-to-dc converters provides a safety ground and shielding for the converters. If all of the converters are from the same series of a given manufacturer, then use a single plane for all of the module cases and connect it to chassis ground. Otherwise, to prevent crosstalk between the modules, you may have to isolate the converter cases from each other with inductors or beads. The output return plane is the most difficult to design. If your grounding design calls for a common return from the load to the power supply, then the output return plane should be connected to it. Otherwise, you must choose the return plane(s) carefully to avoid ground loops. This is especially true if there are output-referenced control signals that are common to all of the modules.

Noise prevention and abatement also are important facets of board design. The most effective noise-prevention strategy is to keep signal traces short. Doing so is facilitated by using SMT components where possible to reduce spacing and lead inductance. Careful planning in the placement of the modules and components can also reduce the trace length, as well as improve the routability of the board. Keep the



6. Proper module mounting is essential to maintain performance over the life of the system.

loop areas of all signals, especially the high-current signals, as small as possible. Large loop areas will increase the magnetic coupling between traces. Magnetic coupling is difficult to counteract because magnetic shielding is usually required instead of copper shielding. Because a pc board only uses copper conductors, the traces and ground planes may be ineffective as shields against magnetic coupling.

Loop areas can be reduced by routing signal traces next to their return paths and by shortening the length of the traces. Loop areas can also be reduced by placing bypass capacitors as close to the noise source as possible. When laying out the pc board, always leave provisions for as many noise-abatement capacitors as possible. Consider this as risk reduction for the debug phase of your design. The most effective noise-abatement capacitors are connected from the input pins to the case and from the output pins to the case. Also effective are capacitors between the sense lines in remote-sense applications and capacitors from the parallel pin to its return pin in paralleling applications.

Proper module mounting and placement is paramount to the reliability and performance of the power supply. Improper mounting techniques can strain the leads of the module or reduce the thermal coupling between the module and its heat sink. The most common mounting method uses screws that pass through the heat sink, module, and board with either the heat sink or the board having built-in threads to secure the screw. When using this mounting method, be careful not to rely on unreinforced pc-board material to maintain the torque on the screw.

While some modules have a flat surface on the side against the board, most have recessed mounting holes or slots to allow for more mounting versatility. Under compression, the board material will cold-flow into the recess, reducing the tension on the screw *(Fig. 6)*. The result will be a loss of thermal coupling between the module and the heat sink, leading to higher module temperatures and lower reliability. To avoid this scenario, a standoff should be placed between the pc board and the module. A swaged standoff is preferred because the barrel passes through the board and contacts the screw head. This completely removes the compression force from the board. Another benefit of using standoffs is that their height can be selected to slightly raise the module off the board for cleaning. ☐

Notes:

1. An X capacitor is a capacitor that is approved by US and foreign safety agencies for use from line to neutral or line to line in non-isolated applications.

Richard Okada has for 22 years been vice-president of marketing at RO Associates. Okada received a B.S. in physics from the University of California, Berkeley, in 1970, and an MBA from the University of California, Los Angeles, in 1972. Before joining RO Associates, Okada worked at Hughes Aircraft as a member of the technical staff.

Steve Keller develops power-supply products and supports customer applications for RO Associates. Keller earned a BSEE from Arizona State University, Tempe, in 1986, and an MSEE from Santa Clara University in 1993. Before joining RO Associates, Keller spent nine years at Kaiser Electronics designing analog and power circuitry for military airborne display systems.

HOW VALUABLE?

HIGHLY	CIRCLE 531
MODERATELY	CIRCLE 532
SLIGHTLY	CIRCLE 533

▼ LOW-PROFILE SWITCHERS OPERATE WORLDWIDE

The PSA-10L Series comprises four 10-W switching power supplies designed for worldwide operation. Input range is from 85 to 264 V ac, 47 to 440 Hz. Four versions are available with dc-output ratings of 5 V at 2 A, 12 V at 0.8 A, 15 V at 0.65 A, and 24 V at 0.4 A. All ratings are at 50°C operation with convection cooling. Overvoltage protection is standard and short-circuit protection is provided on all outputs. Total height for the supplies is 18 mm and board dimensions are 50 by 105 mm (about 2 by 4 in.). The series meets UL standard 1950, CSA 22.2 234, and TUV IEC 950. An on-board EMI filter provides total compliance with FCC Class B, VDE 0871B, and EN 55022B emitted-radiation standards. MTBF is projected at 100,000 hours, depending on the model. Pricing is $22 in lots of 500 with delivery from stock.

Phihong USA
1585 McCandless Dr.
Milpitas, CA 95035
(408) 946-7888
▶ CIRCLE 709

▼ 350-W SWITCHER HAS SMALL STANCE

The Easymod family of modifiable switching power supplies has been joined by the AN 350 model, a 350-W, 60-A peak unit with a footprint of just 9 by 5 in. and height of 2 in. The Easymod supplies offer from one to four outputs and feature IEC-555.2-compliant power-factor correction. All outputs are isolated, adjustable, independently regulated, and capable of high peak currents without lockup for powering high-capacitance loads. With their small size and high power density, the AN Series supplies provide major-agency safety approvals and CISPR EN60065 (CE) filtration on any output combination from ±2 to ±48 V dc. The compact U-channel supplies are offered with a wide choice of options such as a cover and fan assembly, 9-to-380-V dc inputs, and many others. Modificatoins can be performed on as few as 100 pieces with no NRE charges. OEM pricing starts at under $350 with delivery in eight to 10 weeks.

Power Solutions Inc.
4699 N. Federal Hwy.
Pompano Beach, FL 33064
(954) 943-4110
▶ CIRCLE 710

MANUFACTURERS OF OPEN-FRAME SWITCHING POWER SUPPLIES

Manufacturer	Output power (W)	Output voltages (V dc)	Number of outputs	Input range (V ac) (Type?)	EMI shielding available?	Power factor correction available?	Industry-standard footprints?	Cooling options
Absopulse Electronics Carp, Ontario, Canada (613) 836-3511 CIRCLE 630	10 to 5000	12 to 260	One to four	90 to 240 (autoselecting depending on model)	Yes	Yes	Yes	Fans, convection, conduction
Advanced Power Solutions Pleasanton, Calif. (510) 485-1280 http://www.advpower.com e-mail: msaps@aol.com CIRCLE 631	5 to 500	3.3, 5, 12, 15, 28, 36, 48	One to five	100 to 500 W autoselecting; 5 to 100 W universal	Yes	Yes (on supplies from 80 to 500 W)	Yes	Convection or fan
American Reliance Inc. Arcadia, Calif. (818) 303-6688 http://www.amrel.com e-mail: amrel@amrel.com CIRCLE 632	30 to 1050	5 to 250	One to three	115/230 V manual	No	No	Half- and full-rack styles	Fans supplied as standard
Applied Kilovolts Portslade, Sussex, U.K. (44) 1273 439440 CIRCLE 633	5 to 250	1 kV to 60 kV	Two	24 V and 110 V ac	Cover included	No	Yes	Convection or fan
Ascent Power Technologies Concord, Ontario, Canada (905) 660-9814 e-mail: harryt@ascent.com CIRCLE 634	10 W to 4 kW (custom)	1.5 V to 100 kV	Up to 20	85 to 260	Yes	Yes	Yes	Free convection or forced-air conduction
Astec America Inc. Carlsbad, Calif. (619) 757-1880 http://www.astec.com CIRCLE 635	25 to 350	5 to 60	One to four	85 to 264; autoselecting	Yes	Yes	Yes	Convection and fan
Astrodyne Corp. Taunton, Mass. (508) 823-8080 CIRCLE 636	15 to 300	5 to 24	One to four	85 to 264; autoselecting	Yes	No	Yes	Convection or fan
Bertan High Voltage Hicksville, N.Y. (516) 433-3110 http://www.bertan.com e-mail: info@bertan.com CIRCLE 637	1 kW	500 V to 125 kV	Four or more	120/240	Yes	No	No	Air

N.A. = not applicable; N.S. = not specified

▼ OPEN-FRAME SUPPLIES ACHIEVE HIGH DENSITY

Power densities of up to 5.3 W/in.^{3} are offered by two additions to the M Series of Moduflex open-frame switchers. A 250-W model comes with from one to four outputs, while the 425-W unit offers one to five outputs with a 5-V, 50-A main output. All outputs are highly regulated, adjustable, and floating. They're also protected against overload, short circuit, and overvoltage. Based on a modular system concept, each M Series supply consists of a motherboard with 90-to-132-V or 180-to-264-V input and a choice of three output-module types that provide nominal outputs of 75, 150, or 350 W. Other options include an autoranging input. Pricing ranges from $0.55/watt for 425-W units in OEM quantities. Modules with most commonly used voltages and ratings are stocked for two-week delivery. Non-standard types take from six to eight weeks.

Deltron Inc.
290 Wissahickon Ave., Box 1369
North Wales, PA 19454-1369
(215) 699-9261
▶ CIRCLE 711

▼ SWITCHMODE SUPPLIES FEATURE REGULATION

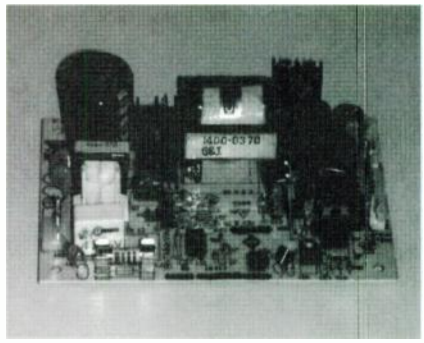
Up to 48 W of regulated dc output streams from the CSL and CSZ Series open-frame switchmode power supplies. The units feature a low-profile design and measure 4.5 by 3.0 by 1.95 in. (CSL) and 6.25 by 3.5 by 2.375 in. (CSZ). Other features include a wide-range input of 90 to 260 V, 47 to

63 Hz with outputs ranging from 5 to 48 V dc. Multiple-output versions are also available. The supplies carry the CE mark and are UL-recognized. Call for pricing and delivery information.

Jerome Industries Corp.
730 Division St.
Elizabeth, NJ 07201
(908) 353-5700
▶ CIRCLE 712

▼ OPEN-FRAME UNITS SPORT UNIVERSAL INPUT

Based on a 3-by-5-in. format, the PPO Series of open-frame switching power supplies features a universal input and outputs of from 20 to 65 W. All configurations are convection cooled



and come in single- as well as multiple-output versions. The series carries UL, CSA, and VDE approvals. Typical 40-W, multiple-output units sell for $20 in OEM quantities. Call for delivery information.

Advanced Power Solutions
1040 Serpentine Lane, #201
Pleasanton, CA 94566
(510) 485-1280
▶ CIRCLE 713

MANUFACTURERS OF OPEN-FRAME SWITCHING POWER SUPPLIES

Manufacturer	Output power (W)	Output voltages (V dc)	Number of outputs	Input range (V ac) (Type?)	EMI shielding available?	Power-factor correction available?	Industry-standard footprints?	Cooling options
CEC Electronics Corp. Hauppauge, N.Y. (516) 582-4422 CIRCLE 638	10 W to 1 kW	3.33 to 48	One to five	110/220, 50/60 Hz; 208, 40 to 400 Hz	Yes	Yes (single- and three-phase active PFC available)	Yes (custom types also available)	Convection and conduction
Celestica Inc. North York, Ontario, Canada (416) 448-4524 CIRCLE 639	300 W to 2 kW	5 to 48	One to eight	90 to 264, autoselecting	Yes	Yes (standard)	Yes	Fans are optional
Computer Products South Boston, Mass. (617) 464-6656 CIRCLE 640	25 W to 1 kW	3.3 to 48	One to five	85 to 264, autoselecting	Yes	Yes	Yes	Optional fan or convection cooling
Condor DC Power Supplies Oxnard, Calif. (805) 486-4565 e-mail: condordc@ condorpower.com CIRCLE 641	20 to 400	3.3, 5, 12, 15, 24, 48	Up to five	85 to 264, universal input	Yes	Yes (on 350-W units)	Yes	Convection or fan
Conversion Equipment Corp. Orange, Calif. (714) 637-2970 CIRCLE 642	85 W to 1 kW	2 to 250	Up to seven	85 to 265, autoselecting or universal inputs available	Yes	Yes	Yes	Convection (no fan), fan-cooled, and conduction
Converter Concepts Inc. Pardeeville, Wisc. (608) 429-3000 CIRCLE 643	10 to 350	5 to 48	One to four standard (more on custom basis)	90 to 264, universal	Yes	Yes (on select models)	Many models have standard footprints	Fans (optional)

N.A. = not applicable; N.S. = not specified

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In today's competitive global marketplace, customers need to bring their supplier's enabling technology in alignment with their own systems requirements. Systems designers want to know, not just where their strategic suppliers are today, but where they are going.

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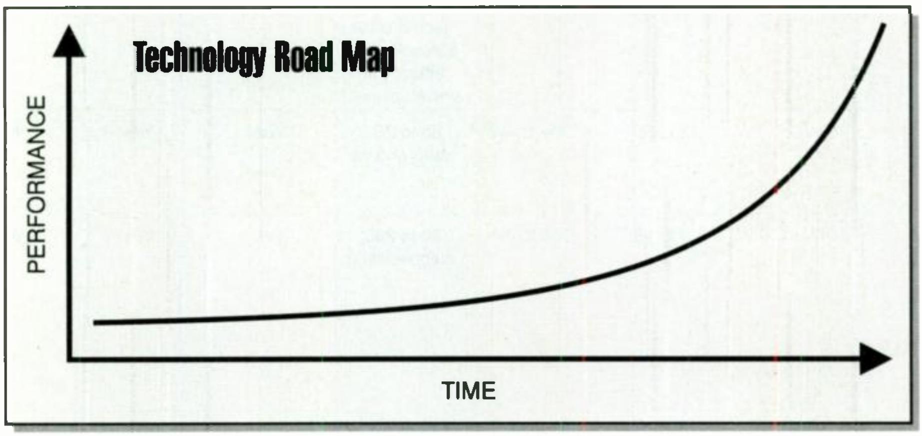

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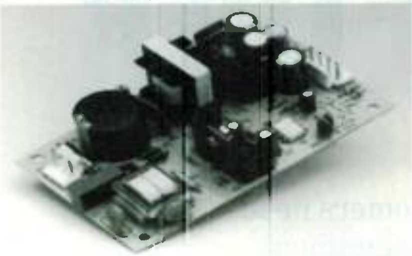
A · P E N T O N · P U B L I C A T I O N

▼ MINIATURE SUPPLIES DELIVER 15-W OUTPUT

The high power densities and low costs demanded for telecom, embedded controls, and instrumentation



power supplies are met by the O Series of miniature open-frame switchers. The 15-W supplies accept a universal input from 85 to 265 V ac and provide voltage outputs of from 5 to 24 V dc in single- and dual-output configurations. Measuring 4.2 in. long by 2.4 in. wide by 1.1 in. high, the miniature supplies are suited for low-to-medium-power applications where space is at a premium. Features include reliable single-board construction and standard Molex-style connectors. Line/load regulation is ±0.3%, ripple and noise is specified at 50 mV p-p, and there's continuous current-limit protection. Typical operating efficiency is 77%. Pricing starts at $15 for lots of 1000 with delivery in six weeks.

Astrodyne
300 Myles Standish Blvd.
Taunton, MA 02780
(508) 823-8080
▶ CIRCLE 714

▼ THREE-OUTPUT SUPPLY SUITS COMPUTER USES

The SW Series of low-cost, industry-standard 3-by-5-in. open-frame power supplies is suited for applications in computers, peripherals, and office-automation equipment. The series comprises ten fully regulated, triple-output models with either universal or auto-selectable ac input for worldwide operation. Available in 30-, 40-, 65-, and 100-W packages, the supplies feature OEM-type input/output connectors for ease of wiring and installation. System-filtering requirements are simplified because the supplies meet VDE 0871, Curve B for EMI. The supplies also offer output surge-current capability, which ensures reliable operation in applications with highly capacitive or inductive loads. Pricing starts at $0.39/watt.

Lambda Electronics Inc.
515 Broad Hollow Rd.
Melville, NY 11747
(516) 694-4200
▶ CIRCLE 715

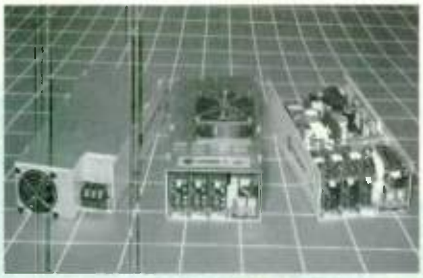
MANUFACTURERS OF OPEN-FRAME SWITCHING POWER SUPPLIES

Manufacturer	Output power (W)	Output voltages (V dc)	Number of outputs	Input range (V ac) (Type?)	EMI shielding available?	Power factor correction available?	Industry-standard footprints?	Cooling options
Custom Power Ronkonkoma, N.Y. (516) 467-5328 http://www.custompower.com e-mail: sales@cps.mhs.compuserve.com CIRCLE 644	Custom	Custom	Custom	24 to 310, autoselect is optional	Yes	Yes	Yes (custom types also available)	Convection, conduction, liquid
Deltron Inc. North Wales, Pa. (215) 699-9261 CIRCLE 645	40 W to 2 kW	5 to 48	One to seven	115/230, optional autoranging from 90 to 264 V	Yes	Yes	Yes	Fan standard/optional
Digital Power Corp. Fremont, Calif. (510) 657-2635 CIRCLE 646	50 to 750	±2 to ±60	One to four	90 to 132 or 180 to 264 (some units autoselecting; others true universal input	Yes	Yes	Yes	Convection and internal or external fan
ETA-USA San Jose, Calif. (800) 382-7697 CIRCLE 647	10 W to 4 kW	2 to 52	One to five	85 to 254, autoranging	Yes	Yes	Yes	Convection or forced air
GlobTek Inc. Northvale, N.J. (201) 784-1000 http://gramercy.ios.com/~globtek e-mail: globtek1@chelsea.ios.com CIRCLE 648	10 W to 1 kW	3 to 48	One to five	90 to 260; autoselecting	Yes	Yes	Yes	Convection and forced air
Integrated Power Designs Wilkes-Barre, Pa. (717) 824-4666 CIRCLE 649	45 to 300	2 to 48	One to five	85 to 264	Yes	Yes	Yes	Convection
International Power Sources Inc. Ashland, Mass. (508) 881-7434 CIRCLE 650	15 to 200	5 to 48	One to four	85 to 264; universal	Yes	No	Yes	Fan or optional cover with fan on unit

N.A. = not applicable; N.S. = not specified

▼ 500-W SWITCHERS OFFER MODULARITY

Thanks to a flexible, modular design, the Z Series of switching power supplies can be quickly assembled at the factory in a large variety of multi-output configurations from three basic auxiliary-output modules. The 2.45-by-5.0-by-10.5-in. supplies feature power density of 3.8 W/in.^{3} as well as

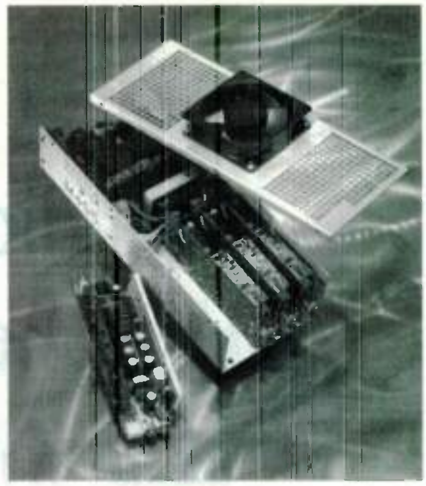


input power-factor correction. The output modules have wide-range, adjustable outputs of 2 to 6 V, 5 to 15 V, and 15 to 26.5 V. They also feature independent overvoltage and overcurrent protection with adjustable OVP. Both single- and multiple-output models are offered with up to four total outputs in either 400- or 500-W versions. Unit prices start at $475 with OEM pricing starting at $309. Samples are available in two weeks and production lots ship in eight weeks from receipt of order.

Unipower Corp.
3900 Coral Ridge Dr.
Coral Springs, FL 33065
(954) 346-2442
▶ CIRCLE 716

▼ MODULAR SUPPLIES HAVE WIDE INPUTS

With its universal input of 90 to 264 V ac, the model M500 open-frame power supply is suitable for all domestic and international electrical power conditions. The modular 500-W supply provides a main output of 5 V dc at 55 A. Up to three auxiliary modules may be used to provide adjustable outputs of 4.5 to 8 V at 10 A, 8 to 16 V at 10 A, and 16 to 28 V at 5 A. In addition, the M500 supply enables the selection of any two of the following fixed voltages: 5, 12, 15, or 24 V at 1 A. Thus, the supply may be configured with any combination of auxiliary modules with up to seven



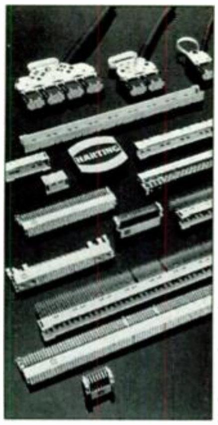
adjustable and fixed outputs. At full load, the supply is rated for operation from zero to 50°C. The supplies are UL-, CSA-, and VDE-listed and are offered with FCC Class B filtering. Pricing is $0.85/watt in OEM quantities. Delivery is in eight to 10 weeks.

Xentek Inc.
1770 La Costa Meadows Dr.
San Marcos, CA 92069
(800) 493-6835
▶ CIRCLE 717

MANUFACTURERS OF OPEN-FRAME SWITCHING POWER SUPPLIES

Manufacturer	Output power (W)	Output voltages (V dc)	Number of outputs	Input range (V ac) (Type?)	EMI shielding available?	Power factor correction available?	Industry-standard footprints?	Cooling options
Jerome Industries Corp. Elizabeth, N.J (908) 353-5700 e-mail: jeromeIND@aol.com CIRCLE 651	Up to 250	5 to 48 (plus multiple outputs)	Up to seven	85 to 264; autoselecting	Yes	Yes	Yes	Convection and fan
Keltron Power Systems Waltham, Mass. (617) 894-8700 e-mail: keltron@tiac.com CIRCLE 652	10 to 600	5 V to 50 kV	One to four	Autoranging ac or dc inputs	Yes	Yes	Yes	Convection or air flow
Kepco Inc. Flushing, N.Y. (718) 461-7000 http://www.kepcopower.com e-mail: hq@kepcopower.com CIRCLE 653	3 to 1500	3 to 48	Up to four	85 to 264, wide range	Yes	Yes	Yes	<300 W: convection; >300 W: forced air
LZR Electronics Gaithersburg, Md. (301) 921-4600 CIRCLE 654	1 to 500	1 to 200	One to four	90 to 265, autoselecting	Yes	Yes	Yes	N.S.
Lambda Electronics Inc. Melville, N.Y. (516) 694-4200 http://www.lambdapower.com CIRCLE 655	10 to 450	2 to 48	One to four	85 to 264, autoselecting	Yes	Yes	Yes	Convection or forced air
Lutze Inc. Charlotte, N.C. (704) 357-8835 e-mail: info@lutze.com CIRCLE 656	0.04 to 50 A	24 V dc	15	24 to 575	Yes	No	Yes	N.S.

N.A. = not applicable; N.S. = not specified



har-pak® 2.5 MM High Density Connector system

Developed for backplane and daughterboard applications in modern rack systems. The 5 row 2.5 mm connector design offers solderless PCB terminations, optimum utilization of space, three dimensional modularity, high contact density, EMI protection, and the ability to double-side sudace mount components on daughter cards without loss of a 15 mm card pitch. The har-pak connector system permits using a three dimensional 2.5 mm grid. With the exceptional capabilities of the connector, only one connector style is required to solve your power, signal, ground, and high data rates; simplifying the design and manufacturing of future systems. The compliant pin technology utilizes the same 1mm plated through hole standard for many DIN 41612 compliant pin technologies. The consistency in design uses the many years of manufacturing and design experience already available. These attributes combined can lead to new advancements in board-level designs: 15 mm card pitch with double-sided suface mounted daughter cards, butterfly or mid-plane techniques, modular design both horizontally and vertically, low number of system components, combination with other standardized packaging systems, and lower applied costs.

READER SERVICE 204

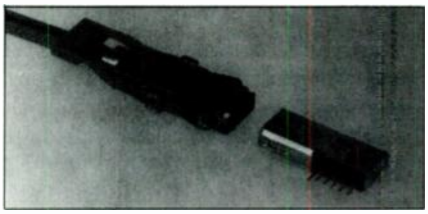
75 Ohm Coaxial Contacts for DIN Connectors

Especially suited for use in telecommunications, medical imaging equipment and/or video receiving/transmission equipment. Can be used with the DIN 41612 Style "M" connectors. This coax contact can handle video signals either on a board-to-board application or a I/O application. Temperature range from -55°C up to +125°C. Working voltage: 250 V eff/50Hz. Maximum contact current: 1.5A (DC). Frequency Range; bisDC up to10 GHz. Most popular configuration to date is the board-to-board arrangement with the Right Angle Female on the PC board and the Straight Male Pin Crimp on the backplane.

READER SERVICE 205

har-link New Modular Metric I/O Connector System

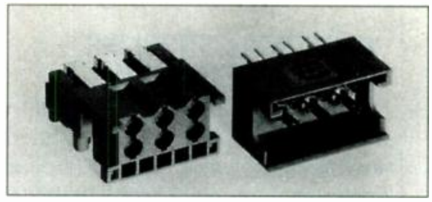
har-link's space saving design offers more than twice the density of many other connector systems. Designed to meet the requirements of high contact density, integrated board fixing, quick efficient locking devices, shielding with ground continuity and reliable wiring techniques, **har-link** also provides a low installed cost. Fully shielded to provide a resistant system against E.M.I. emission or susceptibility. Sequenced mating levels have been included to satisfy requirement for "Hot Swapping." Unique, reli-



able positive latch system has easily operated "push-pull" mechanism that prevents free cable connectors from vibrating loose or being inadvertently unplugged. Simple, but reliable polarization system prevents the mating of connectors in the wrong orientation.

READER SERVICE 206

NEW HIGH DENSITY MICRO-COAXIAL CONTACTS



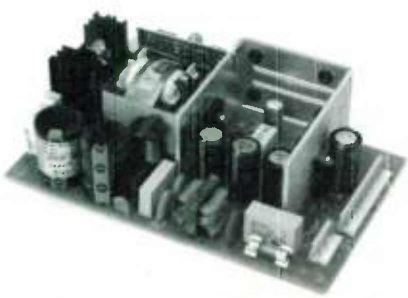
Designed for high speed data transfer rates.Can be used in the iec 1076-4-2 2.5mm High Density connector system, har-pak®. Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without a cable transition.

READER SERVICE 207

READER SERVICE 138

▼ MEDICAL SUPPLIES SPORT ISOLATION

Input-to-output isolation of 4000 V ac is featured in a family of medical switching power supplies. The family includes four series from 40 to 200 W. Each series includes single-output



models (5, 12, 15, and 24 V) as well as several multi-output models with a variety of output combinations. Other key electrical features include low safety leakage current of 50 µA maximum at 1100 V ac and 100 µA maximum at 240 V ac. The supplies also feature a wide universal-input range of 85 to 240 V ac as well as output overvoltage and overcurrent protection. They carry major safety-agency approvals and are built to meet the conducted limits of EN55011 (CISPR11) Level B. Pricing in OEM lots is from $37 (40-W models) to $117 (200-W models). Samples are delivered from stock; production quantities ship in eight to 10 weeks.

International Power Sources Inc.
200 Butterfield Dr.
Ashland, MA 01727
(508) 881-7434
▶ **CIRCLE 718**

▼ 150-W SWITCHERS HAVE LOW PROFILES

An overall height of just 1.38 in. is featured in a series of 150-W, convection-cooled switchers. The FDA150 Series includes nine single- and dual-output models that come in a rugged aluminum U-channel chassis. Users have a choice of quick-disconnect or screw I/O terminals. Single-output models provide tightly regulated outputs of 3.3, 5, 12, 15, 24, or 28 V dc. The 5-V primary of the dual-output models is rated at 25 A maximum with an auxiliary output of 12, 15, or 24 V. The supplies' autoranging input circuit supports operation from 90 to 265 V ac at 47 to 440 Hz. Other features include a built-in EMI-suppression filter that's typically 10 dB better than EN55022/FCC Class B requirements, and 5300-V input-to-output isolation. Pricing is from $96.25 in lots of 1000. OEM orders ship in eight weeks.

Power General
152 Will Dr., Box 189
Canton, MA 02021
(617) 828-6216
▶ **CIRCLE 719**

MANUFACTURERS OF OPEN-FRAME SWITCHING POWER SUPPLIES

Manufacturer	Output power (W)	Output voltages (V dc)	Number of outputs	Input range (V ac (Type?)	EMI shielding available?	Power factor correction available?	Industry-standard footprints?	Cooling options
Modular Devices Inc. Scotts Valley, Calif. (408) 335-3562 e-mail: tommdi@aol.com CIRCLE 657	150 W to 4 kW	1.2 to 400	As required	Autoselecting	Yes	Yes	Yes (select models)	As required
Multicomp Beaverton, Ore. (503) 626-4200 CIRCLE 658	3 to 600	5 to 75	Up to six	90 to 264, autoselecting	Yes	Yes	No	Convection and forced air
Oryx Power Products Mt. Prospect, Ill. (847) 635-6222 CIRCLE 659	30 to 400	±5 to ±24	One, three, or four	90 to 264, N.S.	Yes	Yes	Yes	Convection and forced air
Phihong USA Milpitas, Calif. (408) 946-7888 http://www.phihongusa.com CIRCLE 660	10 to 200	+5 to +24, -15 to -5	Up to four	90 to 264 universal; 90 to132/ 180 to 264 autoranging	No	No	Yes	Convection or 20- or 30-cfm fans
Pico Electronics Power Supply Div. Mt. Vernon, N.Y. (914) 699-5514 e-mail: HLSC73@prodigy.com CIRCLE 661	30 to 200	5 to 24	Up to four	85 to 264, autoranging	No	Yes	Yes	Fan
Power General Canton, Mass. (617) 828-6216 e-mail: powergeneral@ nidecpg.com CIRCLE 662	20 to 250	3.3 to 28	Up to four	85 to 265, universal; 90 to 265, autoranging	Yes	Yes	Yes	Convection and forced air
Power-One Camarillo, Calif. (805) 987-8741 http://www.power-one.com CIRCLE 663	30 W to 4 kW	2 to 120	Up to 21	85 to 264, N.S.	Yes	On some products	Yes	Fan or convection

N.A. = not applicable; N.S. = not specified

This is our power output. If you're waiting for it to waver,

we suggest you order some pizza and find a good place for your sleeping bag.

There's no use looking for a spike, surge, or any imperfection in the output of a Techron power amplifier. We offer the cleanest power available in the industry. As well as frequencies up to 40,000 Hz, and our well-known total reliability, which has made Techron the choice for major MRI manufacturers. For our complete catalog of specs or to discuss custom applications, call 1-800-933-7956.

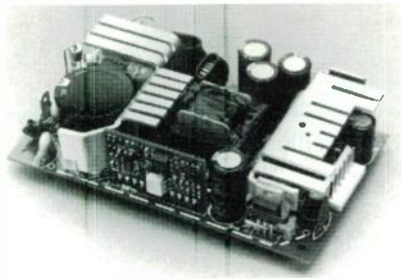
TECHRON.

1718 W. Mishawaka Road, Elkhart, Indiana 46517
(219) 294-8300 • Techron is a division of Crown® International Inc.

READER SERVICE 185

▼ 65-W POWER SUPPLY FIXES POWER FACTOR

Models with or without power-factor correction can be had with the NLP65 line of 65-W switching power supplies. The high-density units offer a



standard 3-by-5-in. footprint and maximum height of 1.4 in. The low profile enables the supplies to be used in 1U rack designs. They accept universal inputs over the range of 90 to 264 V ac and are offered in single-, dual-, and triple-output models. Compliance with UL, CSA, VDE, BABT, and CE Mark safety standards is featured, as is adherence to EMI, FCC, and CISPR 22 Limit B specs. The supplies also offer overload and short-circuit protection. Call for pricing and delivery information.

Computer Products
Power Conversion America
7 Elkins St.
South Boston, MA 02127
(800) 733-9288
▶ **CIRCLE 720**

▼ 1-kW SWITCHER PACKS MANY FEATURES

Power-factor correction, current sharing on all outputs, and N+1 redundancy are among the many features designed into the NMX 1000 Series of 1000-W switchers. The supplies offer third-wire forced current sharing on main outputs and precision regulation or slope programming on auxiliary outputs. They have no minimum load requirements, are self-cooled, and offer high efficiency and MTBF. When used with external ORing diodes, the NMX 1000 supplies are readily configured as a multiple-output, redundant system.

Todd Products Corp.
50 Emjay Blvd.
Brentwood, NY 11717
(516) 231-3366
▶ **CIRCLE 721**

▼ SEMI-CUSTOM SUPPLIES OFFER MODULARITY

A line of semi-custom modular power systems is fabricated using standard modules and custom packaging. Noise and heat loss have been characterized and controlled at the module level, resulting in fast prototyping. Models can be specified from 200 W to 2 kW in custom form factors. Some custom features include cooling, special logic, margining, and more. The high-density units sport high reliability with MTBF specifications of 3 million hours being typical. Flexible inputs can be single-phase universal ac, three-phase, ac, or dc. Other features include power-factor correction to IEC specifications, EMI filtering, active current sharing/parallel operation, cascaded boost/half-bridge topology, zero-current and zero-voltage switching, and soft-start characteristics. Prototypes are delivered in four to six weeks after ordering.

Celestica Power Systems
844 Don Mills Rd.
North York, Ontario M3C 1V7
(800) 461-2913
▶ **CIRCLE 722**

MANUFACTURERS OF OPEN-FRAME SWITCHING POWER SUPPLIES

Manufacturer	Output power (W)	Output voltages (V dc)	Number of outputs	Input range (V ac) (Type?)	EMI shielding available?	Power-factor correction available?	Industry-standard footprints?	Cooling options
Power Solutions Inc. Pompano Beach, Fla. (954) 943-4110 CIRCLE 664	15 to 350	±2 to ±60	One to four	85 to 264, universal	Yes	350-W models only	Yes	Fan optional on most models
Power Switch Corp. Lodi, N.J. (201) 478-0800 e-mail: pwrswitch@aol.com CIRCLE 665	10 to 400	3.3 to 48	One to five	85 to 264, N.S.	Custom	Yes	Yes	Convection and forced air
Rantec Microwave & Electronics Inc. Power Systems Div. Los Osos, Calif. (805) 528-5858 CIRCLE 666	10 W to 1 kW	5 to 28	Multiple on custom models; three on standard products	85 to 270	Yes (on HDM high-density modules)	Yes	Yes	Baseplate cooling
Shindengen America Rolling Meadows, Ill. (708) 593-8585 CIRCLE 667	5 to 130	5 to 48	One to four	85 to 264, N.S.	Yes	Yes	Yes	Convection
Sierra West Power Systems Las Cruces, N.M. (505) 522-9928 CIRCLE 668	5 W to 3 kW	2 to 300	One to five	90 to 135, 180 to 270, autoselecting	Yes	Yes	Yes	Conduction or convection
Switching Power Inc. Ronkonkoma, N.Y. (516) 981-7231 http://www.switchpwr.com e-mail: sales@switchpwr.com CIRCLE 669	100 to 800	2 to 48	Five	90 to 264, selectable or autoselecting	Yes	Yes	Yes	Side fan, top fan, or customer cooling options

N.A. = not applicable; N.S. = not specified

▼ COMPACT SUPPLIES SUIT AUTOMATION TASKS

Clean, stable dc power for industrial-automation applications is provided by a line of compact power supplies. Several versions are available, including single- and three-phase types; filtered and non-filtered units; series-regulated types; short-circuit and under- and over-voltage protected units; and secondary-switched supplies. Output power ranges up to 1200 W with output currents of up to 50 A and supply voltages to 500 V. The units' compact packaging conserves space on crowded control panels. Supplies of up to 60 W can be snap-mounted on DIN rails. Absolute isolation between primary and secondary circuits is featured as standard, and separately mounted terminal screws eliminate the possibility of supply voltages reaching the circuit board. All supplies come with status-indication lights. Call for pricing and delivery information.

Lutze Inc.
1911-A Associates Ln.
Charlotte, NC 28217
(800) 447-2371
▶ CIRCLE 723

▼ QUAD-OUTPUT SUPPLY DELIVERS 500 W

The 170 Series of 500-W, multi-output power supplies offers outputs of 5 V at 50 A, 12 or 15 V at 8 A, –12 or –15

V at 8 A, and either 2.1 or 3.3 V at 3 A. The supplies feature an autoranging input from 90 to 264 V ac, 47 to 63 Hz, and the unit holds regulation down to 85 V or 170 V ac. They're designed for N+1 redundant operation with the 5-V and 2.1- or 3.3-V outputs current sharing with like outputs on similar models. Operating at a fixed frequency of 80 kHz, the supply has a built-in cooling fan and dc-power-good indication as standard equipment. Size is 11 in. long by 5 in. wide by 2.5 in deep. Pricing is from $289 in lots of 1000 with delivery in six to eight weeks.

Conversion Equipment Corp.
330 W. Taft Ave.
Orange, CA 92665
(714) 637-2970
▶ CIRCLE 724

▼ HOT-SWAP SUPPLY HAS BROAD INPUT

The latest in a series of hot-swappable power supplies is the 250 HP series. The units offer universal inputs with built-in ORing diodes for N+1 redundancy. They can be delivered with from one to four outputs and with built-in current sharing and status indicators. Their hot-swap DIN connector plugs easily into any system backplane. Standard four-output units are configured with outputs of 5 V at 30 A, 12 V at 12 A, –12 V at 12 A, and –5 V at 2 A. These standard outputs can also be customized to meet specific requirements. Pricing is $329 for lots of 500.

Switching Power Inc.
3601 Veterans Hwy.
Ronkonkoma, NY 11779
(516) 981-7231
▶ CIRCLE 725

MANUFACTURERS OF OPEN-FRAME SWITCHING POWER SUPPLIES

Manufacturer	Output power (W)	Output voltages (V dc)	Number of outputs	Input range (V ac) (Type?)	EMI shielding available?	Power-factor correction available?	Industry-standard footprints?	Cooling options
Tamura Corp. Temecula, Calif. (909) 694-8350 CIRCLE 670	10 to 500	3.2 to 48	One to four	85 to 264, N.S.	No	Yes	Yes	Convection, forced air
Tectrol Inc. Downsview, Ontario, Canada (416) 630-8108 CIRCLE 671	5 W to 4 kW	2 to 400	One to 15	85 to 265, autoselecting	Yes	Yes	Yes	Natural convection and fan cooling
Technology Dynamics Bergenfield, N.J. (201) 385-0500 CIRCLE 672	25 to 600	3 to 500	Four	90 to 264, autoselecting	Yes	No	Yes (on select models)	Forced air, hard mounting
Tektris Electro Corp. La Mesa, Calif. (619) 593-5000 http://www.tektris.com CIRCLE 673	5 to 600	2 to 300	One to five	85 to 265, autoselecting	Yes	Yes	Yes	Convection, fans
Todd Products Corp. Brentwood, N.Y. (516) 231-3366 CIRCLE 674	150 to 1500	2 to 60	Up to four	90 to 264, universal	Yes	Yes	Yes	Self or external
Transistor Devices Inc. Cedar Knolls, N.J. (201) 267-1900 http://www.transdev.com e-mail: info@mailer.transdev.com CIRCLE 675	500 and up	2 to 56	One to five	85 to 265, autoselecting	Yes	Yes	N.S.	Free air or fan

N.A. = not applicable; N.S. = not specified

▼ DIP ZIF SOCKETS SPEED DEVICE TESTS

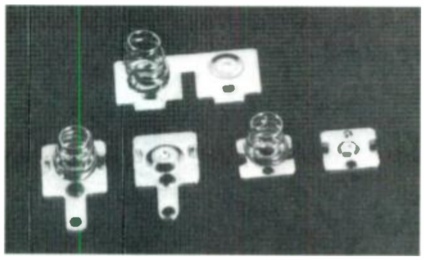
A line of quick-release, zero-insertion-force DIP test sockets speeds production-test applications. The Series X57X test sockets feature a spring-actuated release handle that remains in the off

position until manually depressed. In operation, the handle is pushed down and the IC device inserted and tested. Then, by releasing the handle, it springs back to the off position so that the device may be moved. The quick-release handle, which is offered in short, long, or loop configurations, can be mounted on either side of the test socket. The sockets accept devices on pitches of 0.300 through 0.600 in. centers with 24 through 48 pins. A 40-pin socket with tin-plated contacts goes for $8.30 in lots of 500. Delivery is in two to four weeks.

Aries Electronics Inc.
P.O. Box 130
Frenchtown, NJ 08825
(908) 996-6841
▶ CIRCLE 726

▼ BATTERY CONTACTS SUIT MOLDED CASES

Designed with spring-tension capabilities, a line of battery contacts and springs offers a self-adjusting feature to accommodate a variety of battery lengths. The contacts and springs are made for use with molded cases



and/or portable products with molded-in battery compartments. They're offered in AA, AAA, and N sizes. Furnished with or without solder tabs for pc-board or wire-lead mounting, the devices include base plates made of steel with a nickel finish. The spring contacts incorporate steel-coil springs with nickel finishes for a low contact resistance. Delivery is from distributor stock. Call for pricing information.

Keystone Electronics Corp.
31-07 20th Rd.
Astoria, NY 11105-2017
(800) 221-5510
▶ CIRCLE 727

▼ SPRING CONTACT PROBES OFFER LONG WORKING LIFE

A myriad of uses is possible for a line of spring-loaded contact probes including simulated connectors, battery contactors, and custom contactors. The spring-loaded contacts replace solid, stationary pins or stamped metal in cable-connector, battery-contact, or custom-contactor designs, increasing the life cycle of both the connector itself and the mating connector. The low insertion force of each individual spring-loaded contact and the contact's travel along the Z axis only assure that very little torque is exerted at the mating interface. The probes offer gentle but consistent force at interface boundaries. The probes can be designed with a radius, spear, cup, crown, flat, or other-shaped tip, while stamped metal provides only a radius tip.

Synergetix
310 S. 51st St.
Kansas City, KS 66106
(913) 342-0404
▶ CIRCLE 728

MANUFACTURERS OF OPEN-FRAME SWITCHING POWER SUPPLIES

Manufacturer	Output power (W)	Output voltages (V dc)	Number of outputs	Input range (V ac) (Type?)	EMI shielding available?	Power-factor correction available?	Industry-standard footprints?	Cooling options
Tri-Mag Inc. Visalia, Calif. (209) 651-2222 CIRCLE 676	10 to 350	2.7 to 350	One to six	85 to 265, autoselecting or universal	Yes	Yes	Yes	Convection or forced air
Tri Source Inc. Shelton, Conn. (203) 924-7030 CIRCLE 677	50 W to 1 kW	3.3 V to 4 kV	Five	90 to 130, 180 to 264, autoselecting	Yes	Yes	Yes	Convection or internal fan
Unipower Corp. Coral Springs, Fla. (954) 346-2442 CIRCLE 678	150 to 500	2 to 48	One to five	90 to 132, 180 to 264, jumper or autoselecting; also 90 to 264, universal	Yes (cover includes fan)	Yes (to 0.99)	No	Open frame with forced air or cover with fan
Wilmore Electronics Co. Hillsborough, N.C. (919) 732-9351 CIRCLE 679	5 to 700	5 to 130	One to five	86 to 264, wide range	Yes (offer both open-frame and enclosed units)	Yes	Standard and custom	Convection
Xentek Power Systems San Marcos, Calif. (619) 471-4001 CIRCLE 680	Up to 500	5; 4.5 to 8; 8 to 16; 16 to 28; 5, 12, 15, or 24	Up to seven	90 to 264, autoselecting	Yes	No	Yes	Fan

N.A. = not applicable; N.S. = not specified

▼ MALE POWER TERMINAL CUTS JOINT FATIGUE

A quick-disconnect, 0.250-in. male blade power terminal sports a built-in stabilizing feature. The Rigitab terminal ensures that stresses placed on the blade are safely dissipated without damage to pc boards or solder joints. Conventional male blades typically create direct stress on the solder joint. Often, service personnel rock power terminals to disengage them, and built-up oxidation can make disconnection difficult. These stresses can cause intermittent faults or opens, which may be difficult and costly to detect. The Rigitab terminal overcomes this problem by safely dissipating these forces, reducing rework and repair frequency.As a result, the Rigitab blade provides extended pc-board life and increased reliability Call for pricing and delivery information.

Autosplice Inc.
10121 Barnes Canyon Rd.
San Diego, CA 92121
(619) 535-0077
▶ **CIRCLE 729**

▼ HARD-DRIVE CONNECTOR SUITS SCSI UNITS

A three-in-one integrated connector simplifies the manufacture of hard-disk drives by incorporating power, SCSI, and user-control lines in one unit. The connectors come in straddle-mount, SMT, or through-hole styles for pc-board thicknesses of from 0.036 to 0.067 in. Their high-temperature resin construction makes them well suited for use in high-volume IR-reflow processing. Connector contacts are rated at 1 A for data lines and 3 A for power lines. Contacts are made of phosphor bronze, copper alloy, or brass. The mating contact areas are plated with a gold flash over 50µin. of palladium nickel. The solder-connection areas are plated with a minimum of 100 µin. of tin-lead solder over nickel. Power-line contacts are located on 0.200-in. centers. Data-line contacts for 50-pin SCSI and 6-pin user interfaces are located on 0.100-in. centers. In lots of 200,000, the connectors sell for about $0.01/contact, according to configuration. Delivery is in two weeks for existing connector configurations.

Ranoda Electronics Inc.
2315 N.W. 107th Ave.
Miami, FL 33172
(305) 593-0129
▶ **CIRCLE 730**

▼ POWER RESISTORS ARE NON-INDUCTIVE

Constructed of a ceramic substrate with an embedded thick-film cermet resistive element, the Power-Ω non-inductive planar power resistors are intended for applications like inrush-current limiters, power-supply preloads, telecommunication T-1 cards, and snubbers in switching supplies and UPSs. The 0.1-in.-thick, 1-in. tall resistors mount vertically on pc boards, dissipating power upwards and preventing heat from propagating to other components or into the pc board. Dissipation is as high as 40 W/in.^{2}. Not only are the planar resistors able to handle instantaneous current surges up to 20 times their nominal ratings, they react well in high-frequency applications. Standard parts range from 1 kΩ to 200 kΩ with tolerances from 1% to 10%. Call for price and delivery.

Spectrol Electronics Corp.
4051 Greystone Dr.
Ontario, CA 91761
(909) 923-3313
▶ CIRCLE 731

▼ SURFACE-MOUNT LEDs WITHSTAND PROCESSING

The high temperatures of SMT soldering won't faze the AND4XX family of surface-mount LEDs. The family comprises four different colors of ultra-miniature LEDs. Measuring just 2.0 by 1.25 by 1.1 mm, the AND4RA (red), AND4OA (orange), AND4YA (yellow), and AND4GA (green) LEDs all require about 20 mA of forward current. The devices are said to be very bright for their size and emit light at a wide 150° viewing angle. The red LED has a luminous intensity of 40 mcd. The orange and yellow types are typically rated at 60 mcd, and the green device is rated at 15 mcd. Target applications include keyboard lights on cellular and cordless phones, automotive panel lighting, camera in-viewer indication, and others. Prices range from $0.36 to $0.59 each in lots of 10,000. Delivery is from stock.

Purdy Electronics Corp.
720 Palomar Ave.
Sunnyvale, CA 94086
(408) 523-8210
▶ CIRCLE 732

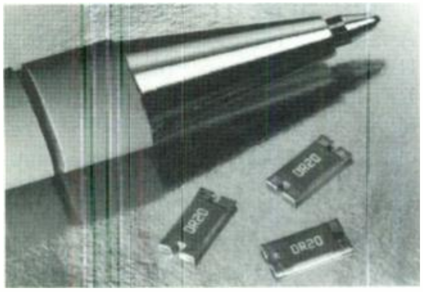
▼ INTEGRATED NETWORKS MELD PASSIVES, ACTIVES

Thin-film passive components such as resistors and capacitors can be combined with active devices such as diodes, charge pumps, voltage references, op amps, analog multiplexers, mixed-signal elements, and logic circuits on a single silicon chip, thanks to CMD's integrated passive network (P/Active) technology. Rather than using traditional ceramic materials for substrates, CMD's process uses semiconductor-manufacturing technology. These devices save pc-board space and costs in SCSI terminators, where precision termination networks must be combined with active switching circuitry while providing a voltage source. Operating up to 3 GHz, the networks are designed specifically for use in Pentium, Pentium Pro, and RISC-based processor environments. Call for pricing and delivery.

California Micro Devices
215 Topaz St.
Milpitas, CA 95035
(408) 263-3214
▶ CIRCLE 733

▼ CHIP RESISTORS OFFER LOW VALUES

Two series of true full-Kelvin, four-terminal, low-value chip resistors are suitable for current-sensing applications. The S2512FK Series measures 0.250 by



0.125 by 0.030 in. and is rated at 2 W. The S2010FK series measures 0.200 by 0.100 by 0.030 in. and is rated at 1 W. Both series offer resistance values from 0.10 to 1.0 Ω and feature tolerances as tight as 0.001 Ω. Standard features include marking of resistance value and current/sense terminals as well as wrap-around nickel barrier terminations. Options include high-reliability screening and epoxy-bondable terminations. Pricing for the S2010FK Series is $0.82 in lots of 10,000. Call for delivery.

State of the Art Inc.
2470 Fox Hill Rd.
State College, PA 16803-1797
(800) 458-3401
▶ CIRCLE 734

▼ ULTRA-BRIGHT LEDs COME IN THREE COLORS

The DDP 200T Series of LEDs comes in amber, orange, and red and feature upwards of 8000 mcd luminous intensity at 20 mA. Packaged in the model PMR200 panel light housing, the lamps' 8° viewing angle is significantly enhanced for maximum visibility in high ambient-light conditions. Besides panel-mount configurations, the lamps come in a wide variety of styles for replacement of incandescent bulbs of any voltage. They provide reliable 100,000-hour lifespans in applications requiring ultra-bright illumination of switches, lenses, and legends. Pricing is $3.50 for the PMR200T-XXK style in lots of 1000. Delivery is in six to eight weeks.

Data Display Products
445 S. Douglas St.
El Segundo, CA 90245-4630
(310) 640-0442
▶ CIRCLE 735

▼ CERAMIC TRIM CAPS TAKE LITTLE ROOM

At 0.196 in. in diameter and 0.080 in. in height, the Vari-Thin Series 513 ceramic trimmer capacitors take little pc-board space and are suited for use in avionics, telecommunications, crystal filters, or any application requiring miniaturized capacitance trimming. The devices operate from –55 to +85°C at 100 WV dc and are offered in three basic terminal configurations. The devices' ceramic base seats directly on module substrates or pc boards with no mechanical or metal protrusions beneath the base plane. Tusonix offers a full line of ceramic trimmers with a capacitance range of from 1 to 3 pF to 15 to 60 pF. Call for pricing and delivery.

Tusonix Inc.
P.O. Box 37144
Tucson, AZ 85740-7144
(520) 744-0400
▶ CIRCLE 736

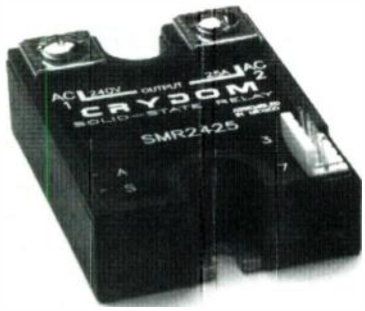
▼ TINY AC RELAYS HANDLE HIGH CURRENTS

Large amounts of power can be controlled with a low-level dc logic input signal by the DRD Series ac solid-state relays. The 600-V, 10-A devices fill the need for higher current and voltage dual relays that are surface-mountable in a small 2.5-by-0.75-by-0.2-in. package. They incorporate a triac design to provide full-wave control and high-current capability with high dv/dt capacity. Featured is zero-crossing circuitry that switches on at zero voltage and off at zero current for superior switching of inductive loads. Also offered is non-zero-crossing drive circuitry, which allows for phase-control capability as well as on-off control. An optocoupler provides the interface to the logic-level dc input signal and electrical I/O isolation. Call for pricing and delivery information.

Gentron Corp.
7345 E. Acoma, Suite 101
Scottsdale, AZ 85260
(800) 436-8766
▶ **CIRCLE 737**

▼ SOLID-STATE RELAYS MONITOR SYSTEMS

Built-in system monitoring in a single compact package is offered by the Series SMR solid-state relays. They provide visual and audible fault-detection



alarms for loss of voltage, open-circuit load, damaged relay output, and loss of dc-supply current. Designed for applications where immediate fault detection is required, they come in three models with maximum load currents of 25, 50, and 90 A. Operating-voltage range is 48 to 280 V rms with dc supply and control-voltage range of 8 to 32 V dc. Call for pricing and delivery.

Crydom
411 N. Central Ave.
Glendale, CA 91203-2020
(818) 956-3900
▶ **CIRCLE 738**

▼ HIGH-FREQUENCY RELAYS ARE SENSITIVE TYPES

A family of relays that switch up to 4 GHz is available under the NAiS brand. RK, RM, and RP relays offer excellent high-sensitivity characteristics required in telecommunications equipment. They have isolation magnitudes up to 60 dB, insertion losses as low as 0.3 dB, and a VSWR as low as 1.3:1. Maximum switching is rated1.5 GHz for the RK, 1.8 GHz for the RP, and 4 GHz for the RM. Applications include information-superhighway equipment, digital communications, multiplex radio and broadcast satellites, marine-communication equipment, and T&M equipment. Call for pricing and delivery.

Aromat Corp.
629 Central Ave.
New Providence, NJ 07934
(800) 276-6289
▶ **CIRCLE 739**

▼ POWER ROCKER SWITCH MOUNTS ON PC BOARDS

The newest addition to the DF Series of power rocker switches is a DPST model with right-angle pc-board terminals. Also included in the line are panel-mounted rockers with quick-connect terminals. The right-angle unit features a European-style actuator with positive detent and good tactile feedback. In addition, the UL- and CSA-approved switch offers contact ratings of 16 A at 125/250 V ac, 1/4 hp at 125 V ac, and 1/2 hp at 250 V ac. Computer-related and power applications are targeted, especially those requiring pc terminations and attractive appearance. Electrical life is 10,000 make-and-break cycles at full load with a minimum mechanical life of 100,000 cycles. Pricing is $1.75 in lots of 1000 with delivery in four to six weeks.

C&K Components Inc.
Clayton/Unimax Div.
8182 U.S. Hwy. 70 W.
Clayton, NC 27520
(800) 334-7729
▶ CIRCLE 740

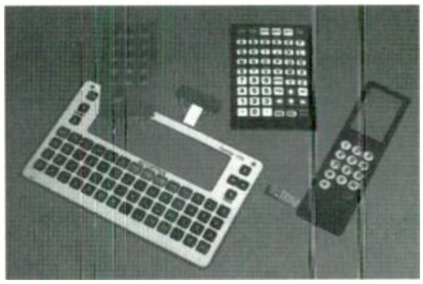
▼ SELECTOR SWITCH SPORTS SPRING RETURN

The C1 spring-return switch features a return that breaks contact when released by the user. Originally designed as a guidance device for flight simulators, the switch has applications in test and measurement, audio, avionics, and industrial applications. The device also features compact size (0.8 in.^{2}), three selector positions, and a life cycle of up to 25,000 operations. Three versions are offered: solder lug, vertical, and rear pc board. Switch variations include shaft and bushing lengths, value-added components, and shorting and non-shorting versions. The unit is indexed at 30, 60, and 90°. Typical pricing ranges from $5.25 to $6.50 in lots of 5000 to 25,000. Delivery is from stock to three weeks for OEM lots; samples are delivered within one week.

Electroswitch
2010 Yonkers Rd.
Raleigh, NC 27604
(919) 833-0707
▶ CIRCLE 741

▼ KEYPAD DOME SWITCHES OFFER TACTILE FEEL

A proprietary manufacturing process yields a line of polytactile dome switches that provide a keypad with strong, uni-



form tactile feel and high-temperature performance. Additional domes can be added on a given part at no extra cost. The polyester is reshaped into the geometry of the dome in the forming process, so the "memory" of the plastic sheet is in the shape of the dome. Call for pricing and delivery information.

Xymox Technologies Inc.
9099 W. Dean Rd.
Milwaukee, WI 53224
(800) 869-9669
▶ CIRCLE 742

▼ EPOXY ADHESIVE BONDS MOST RUBBERS

A two-component, flexible epoxy adhesive is available for bonding most rubbers without surface preparation. Most rubber compounds are extremely difficult to bond and require time-consuming and potentially hazardous corrosive agents to chemically etch the surfaces to achieve good adhesion. The EP21TDC-7 adhesive makes superior bonding possible without etching. It offers excellent performance with neoprene, nitrile, and SBR rubber compounds as well as with metals and most plastics. The adhesive cures at room temperature or more quickly at elevated temperatures. After curing, it exhibits a high T-peel strength of 40 pli and an elongation of over 300%. No solvents or other volatile substances are released during the curing process. Call for pricing and delivery information.

Master Bond Inc.
154 Hobart St.
Hackensack, NJ 07601
(201) 343-8983
▶ CIRCLE 743

▼ HEAT-SHRINK TUBING BONDS TO PVC

The only adhesive known to bond to PVC substrates lines Alpha Wire's FIT-110 and irradiated FIT-115 heat-shrinkable tubing. The adhesive-lined (dual-wall) tubing is used in cable as-

semblies and connectorization applications. Until now, an adhesive version that would bond to PVC cables and connectors had been unavailable, the company claims. When heated, the meltable liner creates a waterproof seal for indoor and outdoor uses, cable connections, insulation repairs, and splices. Both types are available in black and in six sizes ranging from 3/16-in. to 1-in.-minimum diameters. Standard put-up spools are 100 ft. Call for pricing and delivery information.

Alpha Wire Corp.
711 Lidgerwood Ave.
Elizabeth, NJ 07207-0711
(800) 522-5742
▶ CIRCLE 744

▼ STAMPED HEAT SINKS BROADEN THEIR APPEAL

Over 80 standard models have been added to Wakefield Engineering's line of board-level stamped heat sinks. Various mechanical configurations are offered for TO-220, TO-202, and 15-lead multiwatt components having power-dissipation levels of up to 10 W (natural convection). Designs include straight-fin, folded-fin, stag-

gered-fin, and twisted-fin technology and are offered in a variety of heights and mounting configurations. Emphasis is placed on thermal performance, ease of component-to-heat-sink assembly, and wave-solderable tab options. Most of the new additions feature labor-saving clips integral to the heat sink, or clips which can quickly fasten the component to the heat sink. These clips eliminate the need for hardware or installation tools and provide stress-free, reliable surface contact. Typical pricing is $0.27 in lots of 500 with delivery from stock to eight weeks.

Wakefield Engineering Inc.
60 Audubon Rd.
Wakefield, MA 01880
(617) 245-5900
▶ CIRCLE 745

▼ PLASTIC BGA PACKAGE RESISTS MOISTURE

A line of plastic and enhanced ball-grid-array (BGA) packages exceeds the Level 2 moisture resistance requirements as defined by Jedec JESD22-A112, rev. A. The enhanced plastic BGA consists of a multilayer substrate with up to four to six layers of copper, which drastically improves the packages' thermal and electrical performance. Standard plastic BGAs typically comprise two layers of copper. There are six levels used to rate a package's moisture sensitivity. A Level 1 package is not considered moisture-sensitive. Levels 2 through 6 define various levels of sensitivity relative to the amount of time a package can remain in a standard room environment without risking package "popcorning" during the assembly process. Level 2 ratings ensure that product integrity will be maintained when the package is stored in environmental conditions up to 30°C and 60% relative humidity for 8760 hours or 1 year. A range of ball counts and package dimensions is available. Call for pricing and delivery.

Hana Technologies Inc.
2099 Gateway Pl., Suite 340
San Jose, CA 95110
(408) 452-7474
▶ CIRCLE 746

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next wireless design without it...

Wireless circuit and system designers face an uphill climb. They must create innovative designs quickly but at the same time cost effectively, to compete in today's competitive wireless markets. Where do these engineers turn when they need design help? *Wireless Systems Design*.

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MPEG-2 Decompression Board Puts Real-Time Video On The PC

ISA-Based Board, To Be Followed By A PCI-Based Model, Simultaneously Displays NTSC And SVGA Data.

RICHARD NASS

Computer users have become exposed to MPEG-1 and MPEG-2 digital video standards in the last few years. While information about these standards, and what they mean to end users, has come directly from the PC manufacturers, it's the title developers who are actually pushing the standards. This group includes game developers and the Hollywood studios that are putting movies into an MPEG-2 format. While these groups are doing their best to develop titles that can be run on PCs, there's a similar push from IC and add-in board makers to come up with the hardware necessary to run these titles. Such is the case with the Zantares card from Paragon Technology Inc., State College, Pa. *(Fig. 1)*. The board runs MPEG-2-based video over the ISA bus.

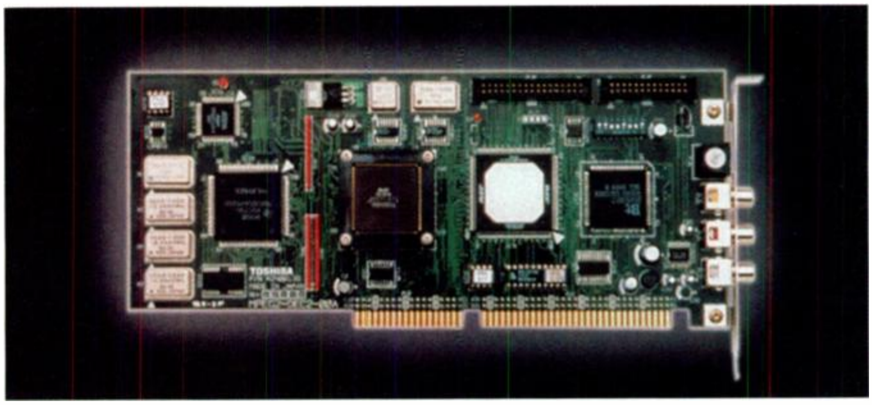
By compressing data at a rate of up to 200 to 1, MPEG-1 has a typical playback rate of about 1.5 Mbits/s. Because it is compressed with a lossy algorithm—meaning that some data is lossed during the compression process—images are not as clear as the original. When the image is viewed at a resolution of 640 by 480 pixels (VGA) or larger, the blockiness and jagged edges become more prevalent. Some decompression-product designers have developed methods such as mathematical interpolation to correct this situation. The native resolution for MPEG-1 video is set at 352 by 240 pixels.

MPEG-1 compression systems range in cost from about $3000 to $30,000. The higher-priced systems provide more control over the compression parameters.

MPEG-2 differs from MPEG-1 in terms of resolution, compressed data rates, and file size. Typical data rates range from 4 to 8 Mbits/s. MPEG-2 also uses a lossy technique. Hence, the higher the compression ratio, the more information that's lost, resulting in a lower-quality decompressed image. But the native resolution of MPEG-2 is higher than MPEG-1 at 720 by 480 pixels.

MPEG-2 typically carries a lower compression rate than MPEG-1. While this results in a higher-quality image for the viewer, it also means that the compressed file is larger. With a 6-Mbit/s data rate, one minute of MPEG-2 video will require about 45 Mbytes of hard-disk space. Hence, a conventional CD-ROM can store about 15 minutes of MPEG-2 video. By reducing the data rate (and thus reducing the video quality), the storage requirement can be reduced.

The Zantares board is based on the VxP505 video processor from AuraVision Corp., Fremont, Calif., and the TC81200F video decoder from Toshiba America Electronic Components Inc., San Jose, Calif. *(Fig. 2)*. The MPEG-1 audio capability that's built into the board is handled by a TI TMS320AV110 processor, coupled to a small block of DRAM. The board can simultaneously output data to an NTSC (or PAL) moni-



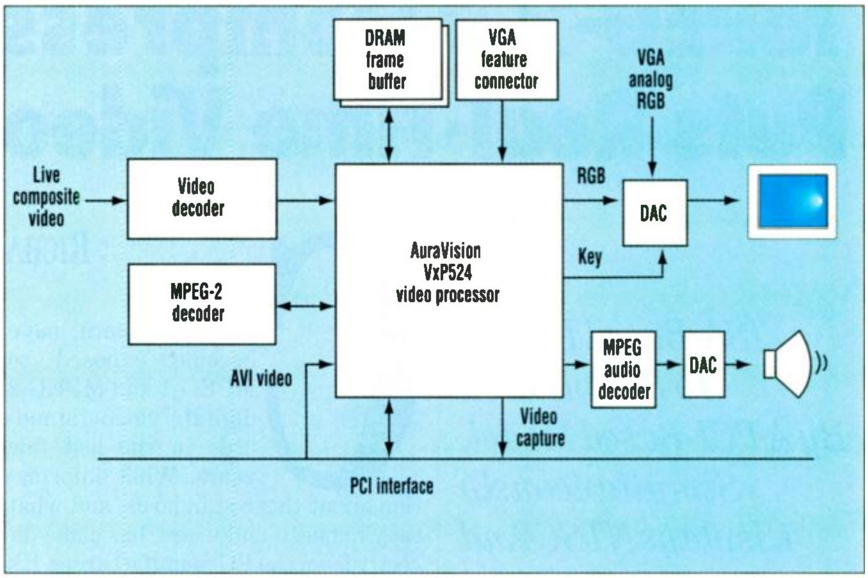
1. THE ZANTARES BOARD, designed by Paragon Technology, runs MPEG-2-based video in real time. The ISA-bus-based board can simultaneously output data to an NTSC/PAL monitor at full-screen resolution and an SVGA display, in a continuously variable window.

tor (full screen) and an SVGA display in a continuously variable window. It ships with drivers for Windows 3.1 and Windows 95.

The AuraVision part, used as a windowing controller, handles the decompressed video, or video that comes from a camera or other source. It then places that video stream into a video window, using a bilinear video-scaling technique.

The controller has a 24-bit internal resolution and a 24-bit external resolution that's dithered to 18 bits. It also offers on-chip color- and chroma-keying for video and graphic overlays. The video typically runs in less than a full screen, with the Windows graphics filling in around the outside to create the full screen. Because the VxP505 has a direct interface to the ISA bus, it can actually pull in the graphics information from the bus, and then place the video in its proper window.

The TC81200F chip is a real-time video decoder that decompresses MPEG-2 video bit streams. It has built-in scaling filters, so it can scale down the video inside the chip without any help from the windowing controller. It also includes a DRAM control unit.



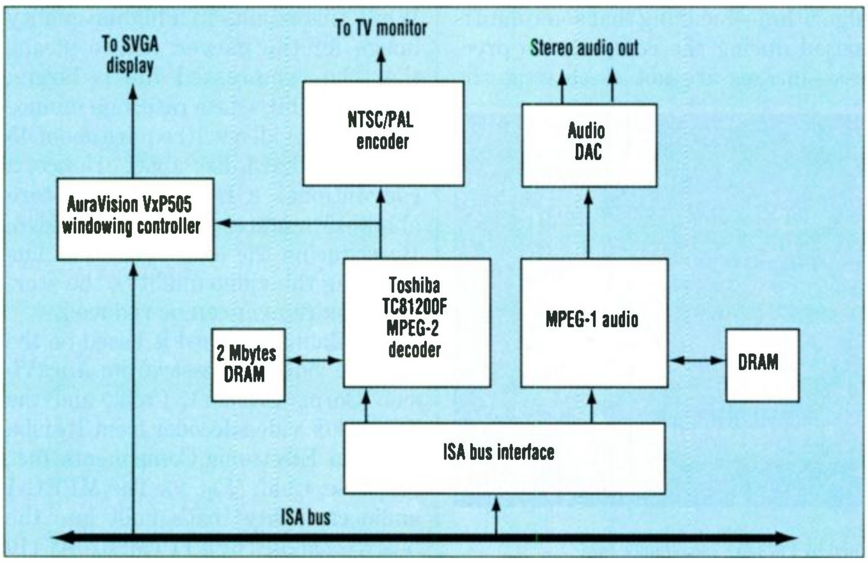
3. PARAGON TECHNOLOGY'S next-generation board, based on the PCI bus, will be built with AuraVision's VxP524, a true-color video-capture and playback processor. The 24-bit part can operate in either a master or slave mode on the PCI bus. It also offers a dual-buffer mode and 2D interpolated scaling, cropping, and time scaling.

WHAT'S NEXT?

Paragon's next-generation board, which is already in the works, will be based on the PCI bus and will have AC3 audio support. Otherwise, the two are functionally the same. Toshiba's TC8121F decodes the MPEG-2 video on the next board. This is because that part can also do MPEG-1 audio decoding. All the audio and video decoding is done on-chip and all the synchronization between the audio and video is handled without any intervention from the host CPU. By integrating the audio and video decoders, some memory (and cost) can be eliminated because the audio and video operate from the same DRAM buffer. Anywhere from 512 kbytes to 4 Mbytes of DRAM are supported by the chip.

The next-generation board will be built with AuraVision's VxP524, a true-color video-capture and playback processor, which just happens to supply a direct link to the PCI bus *(Fig. 3)*. The 24-bit part offers a dual-buffer mode and 2D interpolated scaling, cropping, and time scaling. It can operate in either a master or slave mode on the PCI bus.

The next-generation board may also contain a VGA subsystem, giving the board ultimate control on the quality and speed of the graphics subsystem. This also eliminates the need for a separate card to do the graphics. Another possibility is to include a SCSI or IDE interface on the card, so the data can be pulled in directly from the disk drive. ☐



2. THE GUTS OF THE ZANTARES BOARD come from the VxP505 video processor and the TC81200F video decoder. The MPEG-1 audio capability is handled by the TMS320AV110 processor, coupled to a small block of DRAM.

PRICE AND AVAILABILITY

The Zantares MPEG-2 ISA-based decompression card is available now for $1500. The PCI-based counterpart will be available in August for under $1000.

Paragon Technology Inc., Suite A1, 3006 Research Dr., State College, PA 16801; (814) 234-3335. **CIRCLE 500**

HOW VALUABLE?	CIRCLE
HIGHLY	525
MODERATELY	526
SLIGHTLY	527

PRODUCTS NEWSLETTER

14-Bit IC DAC Clocks At 100 MHz

By surpassing cellular base-station manufacturers' most stringent intermodulation (IM) distortion requirements, the industry's first 14-bit, 100-MHz, IC DAC makes possible a factor-of-20 increase in the voice-channel capacity per baseband-to-intermediate frequency (IF) chain before time or code-division multiplexing. The DAC from Harris Semiconductor, Melbourne, Fla., is based on three patent-pending circuits. One of these reduces the glitch in current-steered DACs and is vital to the chip's ac performance. The HI5741 provides IM distortion components as low as those found in $7000 discrete-component-based, rack-mounted DACs. The IC DAC runs less than $50 in relatively small quantities. Like most high-precision, high-resolution DACs today, the HI5741 combines an R/2R network with a segmented structure. It uses the R/2R network for the 10 LSBs and the 15 equal segmented current sources for the 4 MSBs. The current sources are driven by a thermometer code decoder. Call (800) 442-2747, ext. 7566. *FG* **CIRCLE 626**

High-Performance Emulators Go Portable

Embedded-systems design engineers now can get their hardware and software to market faster with a high-performance in-circuit emulator that offers real-time execution in a portable package. The first microprocessors supported by SuperTAP emulators from Applied Microsystems Corp., Redmond, Wash., are Intel Corp.'s i386EX and the recently introduced 40-MHz Am186ES and Am186EM-series from Advanced Micro Devices. The small form factor makes the emulators easy to use on a desktop, more accessible than conventional laboratory bench instruments, and less expensive than their benchtop counterparts. Available now, prices range from under $10,000 to $14,000 depending on the processor supported. Features include 40-MHz operation, 64-kbyte trace capability, and a debugger and linker/locator. Contact Applied Microsystems at (206) 882-2000; e-mail: *info@amc.com. JS* **CIRCLE 627**

Communications Controller Weds RISC And DSP

By combining DSP and 32-bit RISC capabilities and integrating peripheral functions for digital-cellular communications all on one chip, a new controller from Temic Semiconductors, Santa Clara, Calif., aims at applications such as GSM, DECT, and DSC1800-based transcoding stations, switching systems, bridges, routers, and ISDN adapters. The TSC701 is the first in a series of products based on the company's SPARClet core, a derivative of Sun Microsystems' SPARC V8eR1 architecture. The TSC701's primary advantage is that it offers a single programming environment for both DSP and RISC functions. In addition to DSP library, the chip has an applications library that can be used to implement a communications coprocessor with 128 HDLC channels. Software development tools include a compiler, assembler, architecture simulator, debug, and a real-time operating system. Samples are available now and production quantities are projected for the fourth quarter of 1996, priced at $70 each in 10,000-unit quantities. Call (408) 988-8000; fax (408) 970-3950. *JS* **CIRCLE 628**

375-MHz Buffers Boast Fast Slew Rates

A family of single and quad closed-loop buffers from Maxim Integrated Products, Sunnyvale, Calif., are targeted for applications requiring fast slew rates, such as component or composite video, medical imaging, RF, and telecom. The buffer output stages guarantee a 70-mA output current, an output swing greater than ±2.5 V over temperature into 50 Ω, and can drive capacitive loads greater than 70 pF without oscillations. Supply current is 8 mA per channel, differential phase is 0.01°, and differential gain is 0.01%. Input offset voltage is 0.5 mV and input-referred voltage noise is 5.6 nV/√Hz. The MAX4178 (single) and MAX496 (quad) buffers have fixed gains of +1 (0 dB), a slew rate exceeding 1400 V/µs, and provide bandwidths of 375 MHz, –3 dB and 80 MHz, 0.1 dB, respectively. The MAX4278 (single) and MAX497 (quad) buffers have a fixed gain of +2 (6 dB), a slew rate exceeding 1500 V/µs, and provide bandwidths of 275 MHz, –3 dB and 120 MHz, 0.1 dB, respectively. No external feedback resistors are required for driving back-terminated 50- or 75-Ω coaxial cables. Available in the extended-industrial and military temperature ranges, the single MAX4178 and MAX4278 come in 8-pin µMAX , SO, and plastic DIP packages. For the commercial temperature range, the quad MAX496 and MAX497 come in a 16-pin narrow SO package. Call (408) 737-7600, ext. 6087. *FG* **CIRCLE 629**

Edited by Clifford Meth

Miniature rotary switch

The miniature rotary switch 07R with a volume of about one cubic centimeter is equipped with a solid stainless steel spindle. It is not effected by rapidly changing environmental influences, such as temperature, humidity, and vibration. The stable solder tags in 2.54-mm grid are tinned, while the contacts are plated with a gold layer of 2-μm thickness. The 07R switch is built for a service life of 10,000 switching cycles and is available with a maximum of 4 switching positions in four basic versions: for horizontal and vertical fitting with steel spindle or screwdriver operation. The switch in a thermoplastic package is also available with an optional water-tight threaded bush. AV

Elma Electronic AG, *Hofstrasse 93, 8620 Wetzikon, Switzerland.*
CIRCLE 696

Low-loss regulator ICs

The Sanken SI-300IN Series of low-loss IC regulators are ideally suited to power-supply applications in televisions, video recorders, and office-automation equipment. The devices are supplied in a TO-220 fully molded package, which requires no insulating plate. Built-in protection is provided against overcurrent, excessive input voltage, and overheating. The SI-300IN Series is particularly suited to applications where a constant output voltage is required without on/off control. Input/output difference voltage is IV, and power dissipation is 1.5 W under stand-alone conditions with no heatsink. CM

Allegro Micro Systems, *Balfour House, Churchfield Rd., Walton-on-Thames, Surrey, KT12 2TD, England.*
CIRCLE 697

MPEG video playback evaluatation kit

The DPC7131 evaluation kit from Philips Semiconductors uses a standard ISA slot on a PC and takes MPEG-1 data from a hard disk or CD-ROM, decodes it using the new SAA7131A IC, and outputs either RGB for a PC or a variety of TV standards, (i.e. PAL, SECAM, NTSC, CVBS, or S-Video). Data can also be input from an external video source, such as a camera or VCR via the SAA7110 multi-standard decoder. The board enables either source to be processed or the two combined into one composite image. A complete suite of driver software for Windows MCI and DOS OMI is supplied with the board. The SAA7131A is a versatile full MPEG-1 video and audio decoder that requires only 4 Mbytes of DRAM to decompress MPEG-1 video at data rates up to 5 Mbit/s, coupled with full decoding and synchronisation of MPEG audio data. Full-screen standard VGA mode of 640 by 480 is possible using its line-repeat mechanism, and there is real-time horizontal pixel interpolation with 1-2-1 filter or pixel repeat function.

The SAA7131A's on-chip 16-bit ISA-bus interface requires no additional glue logic, and is used to feed the decoder with control commands, MPEG bitstreams, and PCM audio data. In addition to handling MPEG single bitstreams and ISO11172 MPEG system bitstreams, from which any one of 16 video channels can be selected, it can also accept bitstreams conforming to the Video-CD 1.1/2.0 specification, allowing it to be used in set-top video-disk players and in multimedia PCs. For Video-CD applications, the SAA7131 also supports decoding of high-resolution (704 x 480 pixel) still pictures.

To achieve the real-time synchronisation and frame rate conversion required for sophisticated multimedia systems, the video and audio information extracted from MPEG bitstreams is temporarily stored in external buffer memories before and after decoding. All these buffers are implemented with one 4-Mbit DRAM, which is accessed and refreshed via the SAA7131A's on-chip memory controller. This contrasts with other MPEG decoders which, because they require an external DRAM controller and separate FIFO and frame buffers, result in increased component cost and PC board real estate. PF

Philips Semiconductors *, 5600 MD Eindhoven, The Netherlands.* **CIRCLE 698**

Modem chipset supports DSVD

Both digital simultaneous voice and data (DSVD) protocols, as well as other mainstream business audio applications (from telephone answering machines to speakerphones) are supported by the V.34 28.8-kbit/s modem chipset. The combination of DSVD and hands-free speakerphone operation makes the Catamaran chipset ideal for collaborative computing. DSVD allows users to send simultaneous voice and data messages over one telephone line. The speakerphone enables users to manipulate the mouse and keyboard without trying to juggle a handset. Besides convenience and ease of use, the Catamaran chipset cuts the overall cost of collaborative computing by eliminating the need for a second telephone line. The chipset is compatible with the Intel-led DSVD Protocol Specification for DSP Group's open TrueSpeech 8.5 kbit/s, Multi-Tech's Talk Anytime protocol, and virtually all data-sharing software applications. The chipset also supports V.34 (28.8 kbit/s), V.32bis, V.22bis, V.21, Bell212A, and Bell103 for data, V.17 (14.4 kbit/s), V.29, V.27ter, and V.21 for fax, speakerphone, telephone answering machine, and business audio. CM

AT&T, *Hilary Ln., Marketpoint Europe Ltd., Osprey House, Berkeley Business Park, Finchampstead, Berks, RG11 4YJ, England.* **CIRCLE 699**

COMPUTER BOARDS

BOARD EMPLOYS DUAL CPUs TO ACCELERATE 3D GRAPHICS

The Fire GL board fits the 3D criteria. It's based on a dual-processor design, with up to 20 Mbytes of on-board memory. The board combines the GLiNT 300SX processor from 3Dlabs with the Vision 968 graphics engine from S3 to handle the 3D and 2D graphics acceleration, respectively. In a single-slot PCI configuration, the Fire GL is suited for such applications as CAD, 3D animation, and virtual reality under Windows NT and OpenGL.

The accelerator board can render 300,000 gouraud-shaded polygons/s. Additional 3D capabilities include Z-buffering and support for double buffering at resolutions up to 1280 by 1024 pixels. The memory is partitioned so that up to 12 Mbytes of DRAM are used for the Z-buffering, and 8 Mbytes of VRAM is used for the high-resolution display and double buffering.

The Z-buffering helps speed the removal of hidden surfaces and is needed for accurate renderings required in animation sequences. Double buffering allows for the real-time display and rotation of 3D models and increases user interactivity by providing faster switching among different 3D views.

With 16 Mbytes of memory (8 Mbytes DRAM and 8 Mbytes of VRAM), the Fire GL sells for $2995. The 4-Mbyte DRAM upgrade costs $160.

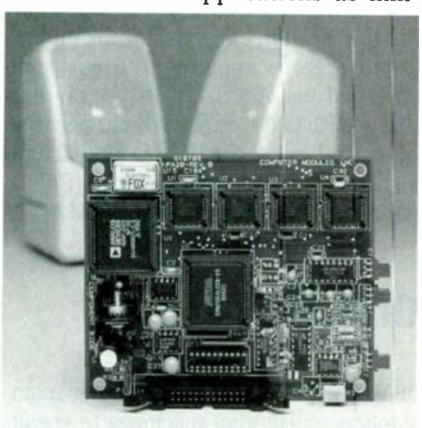
Diamond Multimedia Systems Inc., *2880 Junction Ave., San Jose, CA 95134; (408) 325-7000.*

CIRCLE 800

■ RICHARD NASS

BOARD STORES 4 MINS. OF AUDIO

With the ability to store and reproduce more than four minutes of high-quality audio, the AudioPro board is suited for such applications as mili-



tary simulators, danger announcements, voice feedback systems. The board can be mounted directly onto or inside a piece of machinery or instrument. It works with either an ac or dc adapter. The audio is stored in nonvolatile memory at an 8-kHz sampling rate with 8-bit resolution. The audio can be divided into a maximum of 512 phrases, selected through on-board switches or by computer control. The AudioPro board sells for $420. An upgraded version is available, with 16-bit resolution and a 44-kHz sampling rate. RN

Computer Modules, *2350 Walsh Ave., Santa Clara, CA 95051; (408) 496-1881.* CIRCLE 801

FLAT-PANEL DISPLAY SYSTEM OFFERS BRIGHT COLORS

A high level of brightness is one of the key features of the Ultra-HiBrite line of flat-panel display systems. Displays are available in a 10.4-in. form factor, showing Super VGA or VGA resolution, or 8.4- or 6.4-in. form factor, showing VGA resolution. The systems include a PC/104- or ISA-expandable flat-panel computer (with a 486 or Pentium processor) and a plug-in monitor. The panels are rated are rated at up to 900 nit. The panels themselves operate as CRT replacements and can be directly plugged into any standard VGA output. The 10.4-in. Ultra-HiBrite VGA model sells for $4325. RN

Computer Dynamics, *7640 Pelham Rd., Greenville, SC 29615; (864) 627-8800.* CIRCLE 802

GRAPHICS ACCELERATOR COMES WITH 128 BITS

Designed for PCI-based Power Macintosh computers, the Twin Turbo-128M graphics accelerator is based on a 128-bit architecture. With its 128-bit wide memory bus and 32-bit PCI interface, the card is suited for such graphics-intensive applications as Photoshop, Quark Express, and Word. The board runs Release 2.0 of IMS's software acceleration code, which was recently released. Registered Twin Turbo-128M users can get the enhanced software from the company free of charge. RN

Integrated Micro Solutions, *2085 Hamilton Ave., Third Floor, San Jose, CA 95125; (408) 369-8282.*

CIRCLE 803

PASSIVE-BACKPLANE BOARDS HOLD ALPHA CPUs

A pair of PCI-based single-board computers are driven by Alpha microprocessors. The Alpha PCI 64 and Alpha PCI 164 boards are suited for data-acquisition, data-interpretation, and raster image-processing applications. The difference between the two boards is in the CPU—the Alpha PCI 64 holds a 266-MHz 21064, while the Alpha PCI 164 is built with the 300-MHz 21164. Prices for the single-board computers start at $2995. Both are available immediately. A complete passive-backplane system is also available, in two configurations—commercial quality desktop and tower enclosures—and a rack-mount enclosure. The products all adhere to the PICMG standard. RN

Digital Equipment Corp., *2 Results Way, Marlboro, MA 01752; (508) 264-7723.* CIRCLE 804

PC CARD DOES DATA, FAX, ETHERNET, VOICE MAIL

Users can employ Ethernet or modem capabilities with the NovaLAN 288 Modem, a Type II PC Card, which provides remote access to a LAN, and comes bundled with a Windows-based voice-data-fax system and direct-connect cellular capabilities. The LAN portion combines a burst mode with memory-sharing techniques to get high-speed operation on either a 10BaseT or 10Base2 Ethernet network. The card operates with Netware, Windows 95, Windows for Workgroups, Banyan Vines, Lantastic, and other systems. The V.34/V.42 bis modem sends and receives data at 28.8 kbits/s and faxes at 14.4 kbits/s. Available now, the NovaLAN 288 Modem sells for $399. RN

NovaLink Technologies Inc., *48511 Warm Springs Blvd., Suite 208, Fremont, CA 94539; (800) 668-2546, or (510) 249-9777.* CIRCLE 805

EMBEDDED I/O MODULE TRANSFERS 160 MBYTES/S

With a peak rate of 160 Mbytes/s, Sky Computers claims that the SkyBurst 160 parallel I/O interface is the industry's fastest implementation of the Front Panel Data Port (FPDP) 32-bit parallel I/O standard. The high rate is achievable because the daughtercard connects to the SkyBolt II motherboard through a 320-Mbyte/s SkyChannel packet-bus interface. This connection ensures that no bottleneck will occur.

The SkyBurst 160 implements the full FPDP specification, including full use of the SYNC signal, variable-length data transfers, and support for both TTL and PECL clocks. The card can act as both a transmitter and a receiver, all under software control. Available now, the SkyBurst 160 embedded I/O module sells for under $2000 in large quantities. RN

***Sky Computers Inc.**, 27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920.* **CIRCLE 806**

SBC'S MODULAR CPU PERMITS UPGRADES

While the V254 single-board computer is built with one or two Pentium processors, it can be upgraded to either a faster Pentium, a PowerPC, or an Alpha CPU later. The board is designed in two sections. The processor comprises one section in a modular form, and the I/O subsystem sits on a baseboard. The processor module holds 256 Mbytes of memory, in user-installable SIMMs. It also contains dual PMC slots, allowing users to customize the board. The module connects to the baseboard through a PCI interface. Features of the baseboard include fast and wide UltraSCSI (40 Mbytes/s), Ethernet, 64-bit graphics, VME64, IDE, and floppy, parallel and serial ports. With one Pentium processor, the V254 single-board computer starts at $3995. Prices for the dual-Pentium start at $4595. OEM discounts apply. RN

***General Micro Systems**, 8358 Maple Pl., Rancho Cucamonga, CA 91730; (909) 980-4863.* **CIRCLE 807**

PCI SBC HOLDS DUAL PENTIUMS

One or two Pentiums can drive the PIP10, a PIGMG-compliant single-board computer that connects through the PCI bus. It operates with CPUs running at 100, 133, 166, or 200 MHz, suiting it for machine control, telecommunications, and other graphic-intensive environments. The PIP10's dual-processor configuration supplies a platform suitable for symmetrical processing under Windows NT or OS/2 for compute-intensive applications. Use of Intel's Triton II chip set results in IDE hard-disk drive support that includes Modes 0 through 4 operation (up to 16 Mbytes/s), and concurrent PCI-ISA operations. The board has room for 256 Mbytes of system RAM, 512 kbytes of cache memory, 256 kbytes of shadow RAM for the system and video BIOS, and a flash BIOS for field reprogramming and customization. It starts at $1895. RN

***Pro-Log Corp.**, 12 Upper Ragsdale Dr., Monterey, CA 93940; (800) 252-3279 or (408) 646-3649.* **CIRCLE 808**

COMPUTER BOARDS

CONTROLLER ACCELERATES USB DESIGNS

Connecting to the Universal Serial Bus (USB) just got easier, thanks to the 82930A controller. The part is compatible with USB specification version 1.0, jointly developed by Compaq, Digital Equipment, IBM, Intel, Microsoft, NEC, and Northern Telecom. Using the chip, OEMs can develop telephony and peripheral products with the plug-and-play and hot-swap capabilities defined by the bus.

The 12-MHz, 8-bit device offers ample memory and addressing space, low power and noise, and efficient high-level-language support. It is feature and instruction-set compatible with the MCS251 microcontroller family with instruction-set enhancements for compliance with USB. The chip supports isochronous and nonisochronous data transfers and includes a serial-bus interface engine with USB packet decoding and generation. It also features four transmit FIFOs and four receive FIFOs.

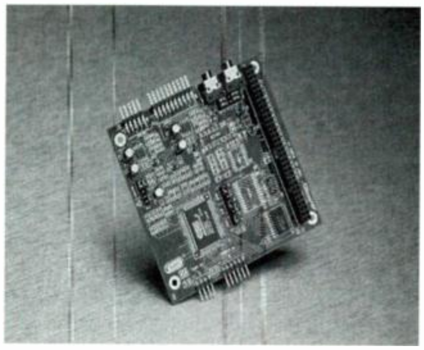
Available now, the 82930A USB controller is housed in a 68-lead PLCC. In lots of 10,000, the parts sells for $6 each. To help facilitate designs, an 82930A controller starter kit is available which contains an evaluation board, schematics, and documentation. A second kit, the Peripheral Development Kit, adds a PC motherboard with on-board host USB-compliant firmware. RN

***Intel Corp.**, P.O. Box 7641, Mt. Prospect, IL 60056; (800) 628-8686.* **CIRCLE 809**

MODULE ADDS SOUND TO EMBEDDED SYSTEMS

Many embedded systems have a need for high-quality audio. The Embedded Sound Module (ESM) offers just that in a PC/104 form factor. It offers full-frequency record and playback for applications such as alarms and status messages, and other announcement-oriented environments.

The ESM includes a 16-bit analog-to-digital converter that samples at software-selectable rates ranging from 5 to 44.1 kHz, and a Yamaha OPL3-compatible 20-voice FM synthesizer. It can compress and decompress .WAV files to minimize the storage requirements. Both 8- and 16-bit record and playback modes are avail-



able. An on-board six-channel mixer can control all the inputs, which can be a stereo line in, a stereo CD in, a mono microphone in, and a mono PC speaker in.

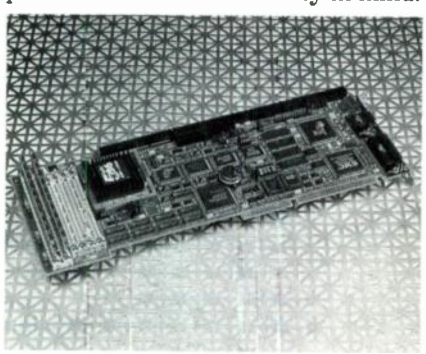
Outouts includes stereo line out, amplified stereo out, and analog PC speaker out. Speakers can be driven directly by the ESM's 0.5-W stereo audio amplifier. Volume can be controlled through software or by adding an external control. Drivers are bundled for Windows 3.1, Windows 95, and Windows NT.

Available now, the ESM is priced at $189 each in lots of 100. A development kit, which eases system integration, includes the ESM, software utilities, and manuals. The kit costs $275. RN

***Ampro Computers Inc.**, 990 Almanor Ave., Sunnyvale, CA 94086; (408) 522-2100.* **CIRCLE 810**

SBC OFFERS EASY UPGRADE PATH

The TEK-AT4LVG single-board computer is built with flexibility in mind.



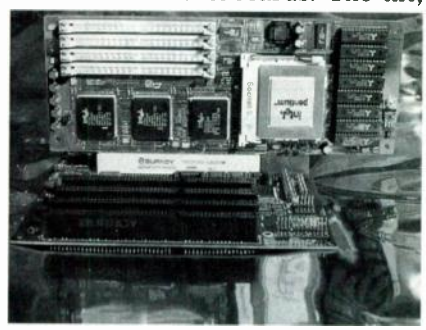
As a result, specifiers can customize the board to their liking. Aimed at high-speed industrial applications, such as telecommunications, medical, and industrial, the board is based on the Intel 486DX processor, with a clear upgrade path to a Pentium Overdrive, Cyrix 5x86, or AMD 486-class microprocessor.

On-board features include up to 4 Mbytes of flash EPROM, 512 kbytes of cache memory, fast SCSI-2, Super VGA video, serial and parallel ports, and local-bus IDE. Up to 64 Mbytes of DRAM is supported, and they connect using either 30- or 72-pin SIMMs. The video subsystem can be configured with up to 2 Mbytes of EDO DRAM. An entry-level unit, with a 66-MHz 486DX2 CPU, 1 Mbyte of video DRAM, and 256 kbytes of cache memory (and no system memory) sells for $1019 in single quantities. Large-volume discounts apply. RN

***Teknor Industrial Computers Inc.**, 7900 Glades Rd., Boca Raton, FL 33434; (800) 387-4222 or (407) 883-6191.* **CIRCLE 811**

MOTHERBOARD HOLDS MOST POPULAR CPUS

The Platform 2000 kit makes it possible for designers to build custom feature-set motherboards. The kit,



which is essentially a base motherboard, contains a 64-bit PCI interface that is capable of 266-Mbit/s transfers. The CPU card is plugged into the PCI bus.

CPU designs are available for a 233- or 300-MHz Alpha 21066 (with 256-kbyte cache), a 486DX, a 486DX/2, a 486SL, a Cyrix 486DX, a Pentium, and a 100-MHz PowerPC 601. New processors will be added as they become available. The board offers three PCI slots and four ISA slots.

Other features include an on-board fast SCSI-2 controller, a parallel and two serial ports, and a floppy-disk-drive interface. The base motherboard is priced at $199. Systems can run most popular operating systems. RN

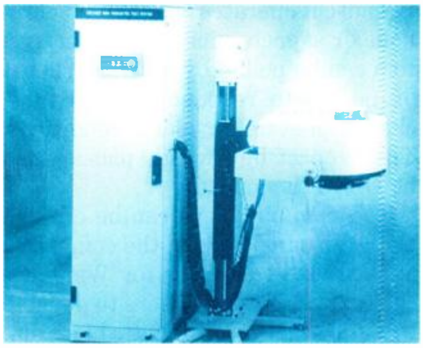
***Shannon Computers Inc.**, P.O. Box 149, 389 Merrymeeting Rd., New Durham, NH 03855 (603) 875-3800.* **CIRCLE 812**

INSTRUMENTS

SYSTEM SPEEDS PARAMETRIC TESTING OF DEEP SUB-MICRON CMOS DEVICES

Designed for dc parametric testing of deep sub-micron CMOS processes, the S600 extends production device characterization to sub-picoamp levels. Depending on the test suite content and measurement levels, users can expect to see throughputs two to 10 times better than those currently available from parametric testers. Measurements below 10 pA, for example, are accomplished in less than one-tenth the time.

The system's test head has active electronics for each of the probing pins. Test head amplifiers are close to the device under test and each pin can be driven by its own voltage supply. This reduces capacitive loading on the circuit node being measured. Source-measurement instrumentation is accessed through a fast, long-life solid-state switching matrix. The result is faster settling times on low-current measurements and more accuracy in gate oxide and interlayer dielectric capacitance measurements below 1 pF. The system delivers 1-pA settling to within 5% in less than 100 ms with 0.1 V applied, and 1% repeatability at 1 pF within 50 ms. A modular design offers flexibility while simplifying test configurations. The system can include up to eight source-measure units. A 100-MHz, 50-Ω switching matrix ensures impedance-matched, low-loss access to probe pins. Advanced system diagnostics continually check the system.



S600 software is built around the Keithley Test Environment (KTE), a data-oriented programming interface that allows users at any level to create test plans and document results. The latest Unix release of KTE has enhanced capabilities for developing new measurement algorithms and for customizing and integrating the test floor by modifying a test sequencer or adding user subroutines. Call the company for price and availability information.

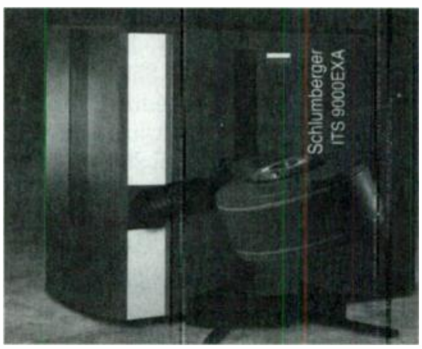
***Keithley Instruments Inc.**, 28774 Aurora Rd., Cleveland, OH 44139-1891; (800) 552-1115 or (216) 248-0400.*

CIRCLE 813

■ JOHN NOVELLINO

MIXED-SIGNAL TESTER HANDLES HIGH-PERFORMANCE ANALOG, DIGITAL

Targeting today's increasingly complex mixed-signal devices, the ITS 9000EXA aims to supply Big D-Big A performance—that is, high-performance digital and analog features rather than the traditional compromise of one or the other. The system is thus well-suited for testing sophisticated audio and video multimedia devices. The ITS 9000EXA delivers a 100/200-MHz data rate, edge-placement accuracy of 275 ps, local memory depth to 32 Mvectors, and looping and complex subroutines. With up to 448 I/O channels, the system can test the largest mixed-signal devices or can test smaller devices in parallel. An optional at-speed, hardware algorithmic pattern generator, with 16X-by-16Y addressing and 64 data lines, is available. Thus the system can test the embedded memory used, for example, for real-time error correction for digital video disk technology and decompression of MPEG data streams.



On the other side, the ITS 9000EXA supplies full synchronization (both synchronous and asynchronous) between the digital and analog subsystems. This allows the system to fully test NTSC/PAL encoders/decoders, RAMDACs with 200-MHz clocks, and devices that support conferencing functions such as H.324 and H.320 multimedia protocol standards. The tester has a low noise floor and a dynamic range of 110 dB. An audio test option enables full performance testing of 16- or 18-bit digital-to-analog or analog-to-digital converters.

The system's Advanced Synbolic ATE Programming object-oriented graphical programming environment simplifies test programming for devices with complex timing and linear requirements. The result is faster time-to-market. ITS 9000EXA prices start at about $1.4 million for a system configured for video test capability. Delivery is typically within 90 days.

***Schlumberger ATE**, 1601 Technology Dr., San Jose, CA 95110-1397; (408) 437-5091.*

CIRCLE 814

■ JOHN NOVELLINO

BOARDS CONVERT PCS TO POWER-SUPPLY TESTERS

The ELTEST Power Supply Tester product family allows users to configure a low-cost, Windows- and PC-based test system with plug-in boards and virtual instrument software. The PC-467 power supply measurement board ($1999) employs a 14-bit, 1-Msample/s analog-to-digital converter. The PC-465 electronic load controller board ($1895) supplies 12-bit current and voltage measurement as well as control over load amplitude, offset, period, and slew rate. The three models in the PC-EL series of 400-W loads ($999 each) offer loading to 500 V and 25 A. The PC-EL2 ($249) is a 100-W serial-input electronic load. The system is controlled by the Powerwin virtual instrument software ($1495), which offers a large library of industry-standard test functions and real-time graphic presentation of captured waveforms. JN

***ELTEST**, 26 Oxford Rd., Mansfield, MA 02048-1127; (508) 339-8120.*

CIRCLE 815

Data-Acquisition System Communicates Over Ethernet

The EDAS family of data-acquisition and control products uses a 10Base-T interface and built-in TCP/IP to communicate over any Ethernet LAN, so that data from remote locations can be shared with other networked resources. Each EDA unit acts as an application server, supplying data-acquisition and control functions to clients on the network.

The first member of the family is the EDAS-1001E-1 digital I/O Ethernet data-acquisition system. It provides 32 channels of TTL digital I/O capability, programmable as inputs or outputs in four 8-bit ports. All inputs can be configured for state detection, counting, or latching. Eight of the digital output channels can be individually configured for predetermined output states at power-up.

The unit's two high-speed 16-bit counter channels can perform frequency measurements and general-purpose event counting up to 250 kHz. Because it operates in either synchronous or asynchronous mode, the system can be polled by network clients or be set to respond only to time, change-of-state, or alarm conditions. The compact, lightweight package can be DIN-rail mounted.

EDAS applications can be created using Visual Designer, the company's applications-generator for Windows. The software allows users to develop the application by drawing a block diagram rather than by writing code. Also available are Net Link software libraries for Unix, Windows, and DOS. These libraries include drivers and extensive documentation for programmers who want to develop applications in C and C++.

The U.S. list price for the EDAS-1001E-1 is $749.

***Intelligent Instrumentation Inc.**, 6550 Bay Colony Dr., MS130, Tucson, AZ 85706; (800) 685-9911 or (520) 573-0887.*

CIRCLE 816

■ JOHN NOVELLINO

Synthesis Software Creates BIST For Memory Arrays

A built-in self-test (BIST) synthesis product for testing of memory arrays in systems-on-silicon designs automatically inserts BIST logic into the design and verifies correct operation. The software, MBISTArchitect, uses proprietary BIST technology from Digital Equipment Corp. and operates as a point tool in Mentor Graphics' top-down design or a third-party environment. MBISTArchitect generates register transfer level Verilog or VHDL descriptions of memory test logic interconnected to multiple arrays, along with a hardware description language test bench. The designer can use the test bench to verify and synthesize the design using any industry-standard Verilog or VHDL simulator or synthesis tool.

The software supports multiple algorithms that ensure comprehensive test coverage of manufacturing defects, including March C and March C+. The ability to use multiple algorithms allows the designer the flexibility to analyze tradeoffs between test application time and quality of test before choosing the appropriate algorithm. The product also supports parallel application of test patterns, which reduces test time, especially for deep memories. A floating license for MBISTArchitect costs $55,000. Production shipping is scheduled for the third quarter. The software is available for HP-PA, IBM RS6000, DEC Alpha, and Sun SPARC workstations.

***Mentor Graphics Corp.**, 8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777; (503) 685-7000.*

CIRCLE 817

■ JOHN NOVELLINO

PCMCIA Data Cards Feature High Resolution

Three PCMCIA cards offer high-performance data-acquisition capability to users of notebook computers running Windows 3.1 or Windows 95. The DAQCard-AI-16E-4 ($995) supplies 12-bit resolution and 250-ksample/s sampling. The DAQCard-AI-16XE-50 ($895) features 16-bit resolution and up to 200-ksample/s sampling on one channel (20 ksamples/s on multiple channels). Both have 16 single-ended (eight differential) analog inputs, eight TTL I/O lines, and two 24-bit counter-timers. The 16E-4 also has analog trigger capability and incorporates the company's NI-PGIA instrumentation amplifier so that the card can accurately measure input signals regardless of the input gain. The DAQCard-516 ($495) delivers 16-bit resolution at 50 ksamples/s on eight single-ended (four differential) channels. It has eight TTL I/O lines and two 16-bit counter-timers. The cards come with the company's NI-DAQ driver software. JN

***National Instruments Corp.**, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100; info@natinst.com; http://www.natinst.com.* CIRCLE 818

Data-Acquisition Boards Include On-Board DSP

The RTI-2100 family of ISA-bus data-acquisition boards features an integrated hardware/software solution that includes on-board sample and hold, digital signal processing (DSP), and programmable gain on each channel. The series offers sampling speeds from 500 kHz to 1 MHz at 12-bit resolution, accommodating inputs from the millivolt range to ±5 V. Also available are 12- and 16-bit digital-to-analog channels and 24-bit I/O lines. The boards use the company's ADSP-2101 DSP to control channel and gain switching and data movement and packing. Two-thirds of the IC's capacity remains and can be programmed for functions like signal filtering and averaging. The boards come with an array of software for DOS, Windows 3.1, and Windows 95, including RTI-STAT, an advanced data-acquisition program with graphical pull-down menus and context-sensitive help. Also included are a variety of third-party drivers. RTI-2100 series prices start at $1260. Delivery is from stock. JN

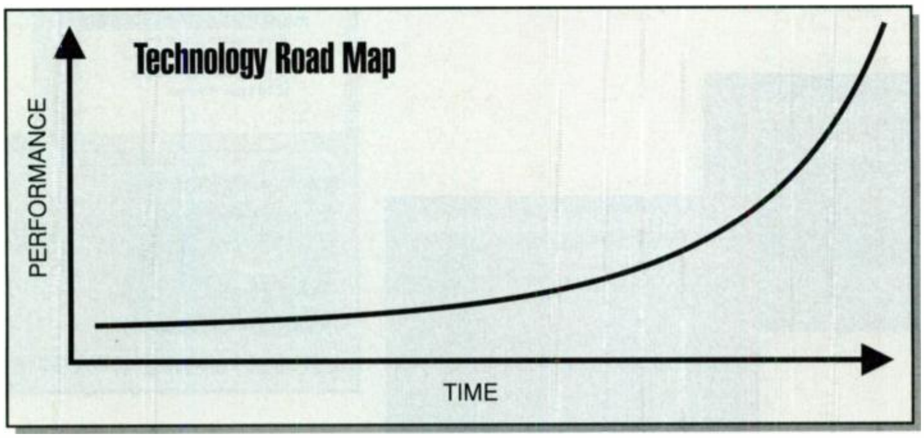
***Analog Devices Inc.**, 3 Technology Way., Norwood, MA 02062; (800) 262-5643; fax (617) 326-8703.* CIRCLE 819

STRATEGIC PARTNERS WORKING TOGETHER

In today's competitive global marketplace, customers need to bring their supplier's enabling technology in alignment with their own systems requirements. Systems designers want to know, not just where their strategic suppliers are today, but where they are going.

But systems designers have another working-together partner, an objective strategic information partner who not only reports on what's available today, but who is constantly scanning the technology horizon to help engineers and engineering managers plan for their next designs; helping them figure out which technologies will be useful and which will end up on the scrap heap.

Electronic Design is that strategic information partner. By providing the information that helps the system designer walk the line between leading edge and bleeding edge, *Electronic Design* helps the engineer get a more competitive product to market, faster.



Your Strategic Information Partner.

ELECTRONIC DESIGN

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TINY GPS ENGINE ADDS NAV TO LAPTOPS, HANDHELDS

Measuring a mere 3.25 by 1.25 in., The Lassen GPS engine may well be the smallest navigation receiver of its kind. It is intended for OEM applications, ranging from vehicle navigation and data collection, to mobile computing and asset tracking.

Drawing only 0.8 W of 5-V power, the compact, unit boasts an 8-channel, DSP-based receiver that provides rapid, accurate, robust location fixes. A "hot start" feature allows the receiver to gain its first fix within 20 s. of power-up under most conditions. If extreme accuracy is desired, the Lassen's auxiliary serial port can be used to support differential GPS operation, allowing location to within 2 meters.

Because the receiver's 32-bit microcontroller spends only a portion of its time managing the GPS functions, it can easily be programmed to support custom applications. The Lassen is available now as either a raw OEM board, or as a fully assembled Type II PC card. The OEM board costs $300 in sample quantities, with substantial discounts for higher volumes.

A complete raw chipset will be available to manufacturers beginning in the third quarter of this year. Pricing for the chipset is still to be determined. LG

Trimble Tracking and Communication, *645 N. Mary Ave., Sunnyvale, CA 94088; (408) 481-8000, email: oeminfo@trimble.com.* **CIRCLE 820**

CELLULAR BASEBAND CHIPS HANDLE CDPD AND AMPS

A baseband chipset is able to provide combined voice and data communications using the AMPS and CDPD (cellular digital packet data) protocols. DSP Communications D5101 chipset can be used for a wide variety of products, including CDPD-only modems, AMPS cellular phones with built-in CDPD capability, and combined circuit-switched CDPD modems. It complies with releases 1.0 and 1.1 of the CDPD specification.

The D5101 chipset consists of a function-specific DSP and a mixed-signal ASIC. The ASIC is designed so that its output can be directly interfaced to the IF stage of a standard cellular radio. In CDPD mode, it provides all necessary physical and MAC-layer processing. In AMPS mode, it supports all the AMPS audio SAT, and wideband data processing. Software that supports the complete CDPD protocol stack and AMPS call processing is available, along with software development assistance for specialized applications. The chipset can operate on supply voltages ranging from 3 to 5.5 V. It draws only 38 mA in when operating, and 1.5 mA in standby mode. Housed in 44 and 100-pin TQFPs, the D5101 is currently sampling. Pricing is available upon request. LG

DSP Corp., *20300 Stevens Creek Blvd., Cupertino, CA 95014; attn: Kelly Birmingham, (408) 777-2700; fax -2770.* **CIRCLE 821**

3V DOWNCONVERTER/LNA FOR CDMA/AMPS CELLULAR APPS

The TQ9223 is optimized for use as a dual-mode (TDMA/AMPS) RF receiver front-end. It integrates a low-noise amplifier (LNA) with a low/high gain selector, and an RF mixer to provide a complete downconverter function. Capable of operating at frequencies between 500 and 1600 MHz, the LNA and mixer provide a gain of 20 dB and a 2.5 dB system noise figure, plus a third-order intercept point of -10 dBm. The device operates on a single 3-to-5-V supply, drawing only 10 mA.

The TQ9223 is housed in a SO-14 plastic package and is available from stock now. Pricing is $1.50, in quantities of 100,000 per year. LG

TriQuint Semiconductor Inc., *3625A SW Murray Blvd., Beaverton, OR 97005 ; (503) 644-00335359, fax (503) 644-3198.* **CIRCLE 822**

LOW-POWER QUADRATURE MOD-DEMOD RUNS ON 3 V

The MAX2450 combines a monolithic quadrature modulator and demodulator with a supporting oscillator and a divide-by-8 prescaler. Suitable for use in cordless and GSM and North American cellular applications, wireless LANs, and 2-way pagers, it operates from a single +3 V supply and draws only 5.8 mA. The demodulator accepts an amplified and filtered IF signal in the 35 to 80 MHz range, and demodulates it into the I and Q baseband signals with 51 dB of voltage conversion gain. The IF input is terminated with a 400-ohm thin-film resistor for matching to an external IF filter. The baseband outputs are fully differential and have 1.2 V p-p signal swings. The modulator accepts differential I and Q baseband signals with amplitudes of up to 1.35 V p-p, and bandwidths up to 15 MHz, and produces a differential IF signal in the 35-to-80 MHz range. An evaluation kit is also available for the MAX2450, to assist with evaluation and prototyping tasks. Packaged in 20-pin SOIC or SSOP, the MAX2450 is shipping now. Pricing is $3.99 in lots of 1000. LG

Maxim Integrated Products, *120 San Gabriel Drive, Sunnyvale, CA 94806; (800) 998-8800, (408) 737-7600, fax (408) 737-7600.* **CIRCLE 823**

VSAT RECEIVER CAN BE PROGRAMMED FOR MULTI-RATES

A two-chip solution can now be used as the core of a variety of very small aperture terminal (VSAT) satellite receiver applications. Its programmable multi-rate digital demodulation enables manufacturers to employ a single design for front end systems that operate at different data rates of up to 2.5 Mbits/s.

The chip set consists of the HSP50110 digital quadrature tuner and the HSP50210 digital Costas loop. The HSP50110 can support 10-bit real or complex in-phase (I) and quadrature (Q) inputs at rates of up to 53 Msamples per second. It converts the IF or baseband signal obtained from an inexpensive A/D converter with up to 10-bit resolution to a quadrature baseband signal. It tunes, filters, and passes this data to the HSP50210 digital Costas loop, while providing AGC functions to the receiver. The HSP50210 performs filtering, carrier tracking, and symbol tracking functions to recover BPSK or QPSK digital data from the signals received from the HSP50110.

The HSP50110 and HSP50210 both cost $23.97 each, in 1000-piece lots, with the price dropping to $9.25 each for orders of 500,000 pieces. An evaluation board (HSP50110/210EVAL) is also available at a cost of $285. LG

Harris Semiconductor, *P.O. Box 883, Melbourne, FL 32902-0883; (800) 9488-HARRIS, ext. 7547.*

CIRCLE 824

G.729 VOICE-COMPRESSION CODE FOR TMS320C5x DSPs

A complete implementation of the ITU G.729 voice compression algorithm is now available for TMS320C5x DSPs. The G.729 algorithm is the latest compression scheme approved by the ITU and uses the CS-ACELP (Conjugate-Structure Algebraic Code Excited Linear Prediction) to compress standard 64-kbit/s pulse code modulated (PCM) voice data to an 8-kbit/s stream while maintaining toll-line voice quality. Suitable for GSM cellular and several PCS standards, the encoder and decoder are able to operate under a real-time task switching kernel. The software suite is designed to support full duplex operation using a single TMS320C5x DSP. The code has a high-level C-callable interface. It is also fully re-entrant, and can be used for multi-channel operation. The decoder and encoder are fully independent which permits a DSP device to support as many combinations of full and half-duplex channels as its processing speed allows. Sample software and licensing fee information are available upon request. LG

Castelton Network Systems Corp., 4260 Still Creek Drive, Suite 320, Burnaby, B.C., V5C 6C6, Canada, attn: Greg Celmainis ; (604) 293-0039, fax (604) 293-0047, email gregc@castleton.com. CIRCLE 825

DIRECT-CONVERT FSK RCVR FOR BETTER, CHEAPER PAGERS

The SL6609 direct-conversion paging receiver incorporates on-chip automatic frequency control (AFC) to enhance a pager's performance while reducing its cost and size. Able to operate at frequencies of up to 900 Mhz, the chip also features programmable post-detection filters which enable designers to optimize circuit performance for a range of different data rates.

The SL6691 delivers a typical sensitivity figure of -128 dBm at 450 Mhz with its AGC loop closed. The direct-conversion architecture employs only one mixing stage, thus reducing component count and design time. Since filtering is implemented on-chip, external passives are not required and noise problems due to routing signals off the chip are eliminated. The SL1669 is housed in a 32-led plastic quad flatpack and is available from stock now. Pricing is $9.77, in quantaties of 10,000. LG

GEC Plessey Semiconductors, 1500 Green Hills Road, Scotts Valley, CA 95067, attn: Brent Wilkins; (408) 438-2900, fax (408) 438-6231. CIRCLE 826

FOUR-CHIP DBS RECEIVER FOR 900 Mhz - 2.15 Ghz APPS

A four-chip DBS receiver circuit is designed to replace the bulky, expensive discrete solutions found in most satellite receivers today. The receiver consists of four devices; the UPC2782GR RF downconverter, the UPC2766GR I/Q demodulator, the UPC 2708T RF amplifier, and the UPC1505GR 3 GHz prescaler. The UPC2782GR RF downconverter combines a Gilbert cell mixer, two stages of LO buffering, a low phase noise oscillator, a high output gain control amplifier, and temperature compensation circuitry. Its wide dynamic range and +3 dBm third-order intercept point combined with an 11 dB noise figure allow it to deliver outstanding performance across its 900 MHz to 2.5 GHz operating range.

The UPC2766GR I/Q demodulator features a bandwidth of DC to 100 MHz and an onboard input gain control. This permits it to accept a wider dynamic range of signal strengths which helps to optimize the receiver's bit error rate to allow the use of smaller dishes, lower signal strength, or a combination of both. The UPC 2708T RF amplifier is a MMIC that delivers a low noise output with flat gain characteristics. When combined with an AGC signal, this device sets the noise figure and signal level for signal processing in the downconverter. Finally, the UPC 1505GR is a 3-GHz divide -by-64/128/256 prescaler. Its high divide ratios allow the use of lower cost low-frequency PLLs. The UPC2784, 2766, and 2781 are all availible in SSOP 20-pin packages. The UPC2708T LNA is housed in a 6-pin miniature TO6 package. Pricing for the parts in lots of 100,000 is as follows; UPC2766 I/Q demodulator - $2.70, the UPC 2708 RF amplifier - $0.80, and the UPC1505 3 Ghz prescaler - $1.50, and the UPC2782 downconverter - $1.45. LG

California Eastern Labs, 4590 Patrick Henry Drive, P.O. Box 54964, Santa Clara, CA 950541817; (408) 988-,3500 fax (408) 988-0279. CIRCLE 827

DUAL-MODE SAT-NAV RCVR CAN USE GPS AND GLONASS

The GG24 navigation receiver is the world's first single-board receiver to tightly integrate the U.S. Global Positioning Satellite (GPS) system and the Russian GLObal NAvigation System (GLONASS) navigation technologies in a practical OEM module. The GG24's ability to receive and use signals from not only the 24 GPS satellite, but also from the 24 GLONASS satellites, ensures its rapid integration into a wide variety of high-precision land, sea and air-based applications.

Signal acquisition times and reception in areas with large obstructions is greatly improved, thanks to having twice as many possible "targets" available in the sky at any given moment. Because it is able to receive the unscrambled GLONASS signals, the GG24 is able to immediately deliver the 7-to-10 meter accuracy promised by GPS at the turn of the century, when the selective access (SA) signal degradation is removed from its broadcast. Also included on the receiver board is a Receiver Autonomous Integrity Monitoring (RAIM) system which is used to verify the integrity of its navigation information.

The GG24 has external inputs to permit the use of differential data for precision navigation and other positioning tasks. The unit's differential performance is enhanced by the combination of GPS ad GLONASS, thanks again to having more satellites to work with.

Sample units of the GG24 are available now, with production volume orders for for the units fulfilled within 60 days of order placement. The GG24 will be offered in different mechanical formats for easy integration into OEM applications. A Eurocard format OEM board is available at $5995, while a PCMCIA-based unit with a ruggedized external sensor package and power supply costs $9995. Substantial discounts are available for customers purchasing the units in production-level volumes. LG

Ashtech Inc., 1170 Kifer Road, Sunnyvale, CA 94086; (408) 524-1400, fax (408) 524-1500, email www. ashtek.com. CIRCLE 828

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SMALL PRINTERS

Star Micronics America Inc., OEM Division, Piscataway, N.J., has released its small printers catalog. The 32-page, four-color guide details the company's full line of dot-matrix and thermal printer products from POS solutions to kiosk printers. The brochure describes the features of all of Star's printers, printer mechanisms, control boards, and accessories. Information on applications, print speed, reliability, print method, and dimensions is also provided. In addition, specification charts, print samples, diagrams, and photographs of the products are included. To receive a free copy of the catalog, call the company at (800) 772-7636. MS **CIRCLE 700**

STANDARD POWER SUPPLIES AND DC-DC CONVERTERS

A 192-page full-line power-supply catalog is available free from Lambda Electronics Inc., Melville, N.Y. The catalog contains detailed specifications, mechanical drawings, and prices of over 1000 power supplies, dc-dc converters, power systems, and accessories. Also listed are over 200 new products, including 1.5 W to 6 W converters, and high-density distributed power front ends for 24 V and 48-V dc converters. For a copy, call (516) 694-4200. MS **CIRCLE 701**

FIBER-OPTIC COMPONENTS CATALOG

Lasertron, Burlington, Mass., has released its "1996/97 Short Form Catalog." This 12-page catalog includes the company's product offering of fiber-optic components for use in communication and instrumentation systems. Sections include detailed descriptions of pinFET receivers, light-emitting diodes, and package specifications. Photographs and technical drawings of the products are featured. Also included is a list of Lasertron's U.S. and international offices and their representatives. To receive a copy of the catalog, contact the company at (617) 272-6462. MS **CIRCLE 702**

APPLICATION NOTE DETAILS AVIONICS DATABUS

ILC Data Device Corp., Bohemia, N.Y., has an application note, AN/A-4, entitled "Avionics Databus Basics." The six-page fold-out discusses ARINC-429, ARINC-629, and Mil-Std-1553 fundamentals and comparative attributes. AN/A-4 describes the three popular avionics buses, their relative signal formats, and protocols. It also includes a comparison table highlighting architecture, encoding, transmission mode, media, and coupling, data and effective bit rates, subscribers and relative cost, weight, and reliability. As such, it is an ideal primer for design engineers and nonspecific as to product implementations. The note explores how each bus works and compares in capability. For more information, call (516) 567-5600, ext. 7405. CM **CIRCLE 703**

SERVO POSITIONING SYSTEM PRODUCT BROCHURE

A full-color, eight-page brochure describing servo-positioning systems is available from CMX Systems Inc., Wallingford, Conn. The brochure offers descriptions of the three systems currently available from the company, along with a discussion of their applications and an explanation of fringe counting interferometry—the core technology behind these products. Complimentary copies of the brochure are available by contacting the company at (800) 269-8922. MS **CIRCLE 704**

DATA SHEET FOR MODULATION ANALYZER

A two-page data sheet on the Model 8201 modulation analyzer is available from Boonton Electronics Corp., Parsippany, N.J. The literature contains charts that describe the Model 8201, including its carrier-frequency range, level measurement capability, and GPIB programmability. Also outlined in the data sheet are the product's applications, including mobile radio production testing and ATE applications. For a free copy of the data sheet, contact Boonton Electronics at (201) 386-9696. MS **CIRCLE 705**

OMS-100 OPTICAL TEST SET

A four-page brochure on the OMS-100, an economical, future-oriented solution for measuring optical systems and devices used in telecommunications and data communications applications, is available from Wandel & Goltermann, Morrisville, N.C. The full-color brochure explains all the pertinent features, specifications, functions, and applications of the OMS-100, including its ability to make SDH/SONET measurements, and perform PON/PDN Tests (FITL) and LAN tests, as well as calibration and device tests. The brochure illustrates each explanation with easy-to-read charts and diagrams. For more information, call (800) 924-3773 or fax (800) 280-6294. CM **CIRCLE 706**

200 METERS AND INSTRUMENTS

A 100-page data book produced by a team of panel meter experts is available from Datel Inc., Mansfield, Mass. The "Digital Panel Meter Data Book and Applications Guide" contains information on numerous 3.5- and 4.5-digit LCDs, LED displays, and miniature digital voltmeters. The book also gives details on a number of new products, including self-powered ac and dc voltage monitors, and ultra low-power LED display DPMs. All products include data sheets with specifications and dimensional drawings. The book also contains sixteen fully illustrated application notes that describe in detail such panel meter applications as dc ammeters, resistor scaling networks, and tachometers. The book is available free of charge directly from DATEL or any of its authorized sales representatives. For more information, call the company at (508) 339-3000 or fax 339-6356. MS **CIRCLE 707**

COMMUNICATIONS ICs

A communication products data book from Crystal Semiconductor, Austin, Texas, includes product and applications information on the company's complete range of datacom and telecommunication ICs. The 878-page data book uses detailed product descriptions and operations discussions to provide a comprehensive overview of Crystal's communications product family. Full data sheets for over 30 products, including complete information on new products, are provided. The catalog divides the product line into four major categories: Ethernet Local Area Network (LAN) products; other datacom products, including a new infrared IrDA-compatible transceiver IC; telecommunications products, including T1/E1 products; and signal-processing components, such as echo cancelers and modem/audio analog front ends. CM **CIRCLE 708**

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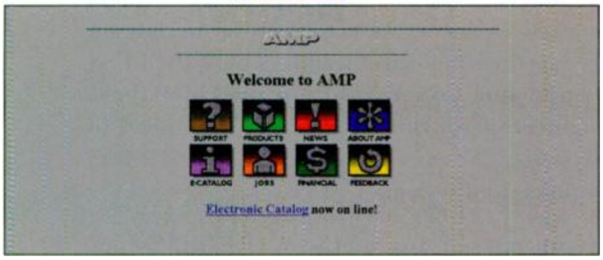

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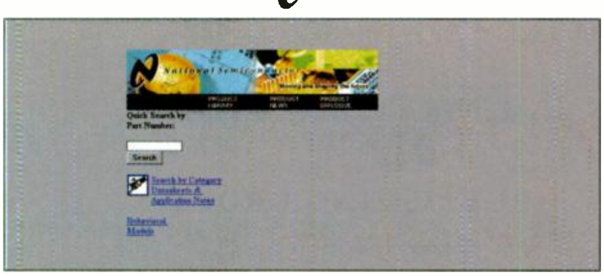

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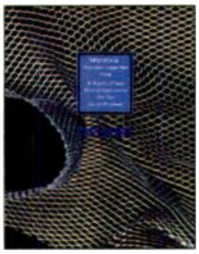


CIRCLE 250

DELKER CORPORATION

THE LOW COST MEMORY SOLUTION

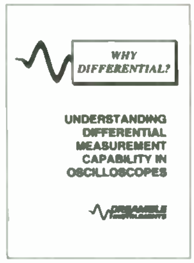
EXEL's SPI Lite product line provides a cost savings relative to existing SPI and SIOP compatible E2PROMs. These products are being introduced in response to a market demand for a lower cost solution to interfacing nonvolatile memory with the Motorola family of microcontrollers. The first two devices in this family currently available are the XL25026 and XL25046. Additional product offerings, willll be available in the near future.

CIRCLE 251

EXEL MICROELECTRONICS

DIFFERENTIAL MEASUREMENTS

A discussion of single-ended and differential scope measurements on ground referenced and floating signals. Differential amplifier characteristics such as common mode rejection ratio and common mode range are covered. 1-800-376-7007



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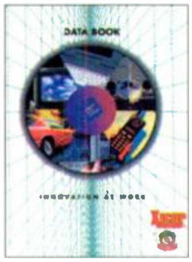


CIRCLE 254

XICOR

HIGH-VOLTAGE POWER SUPPLIES

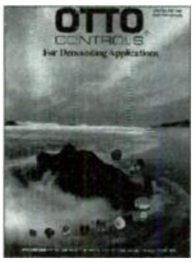
Universal Voltronics MT.KISCO. New York is offering literature covering its BRC line of high-voltage power supplies, which are used in Medical/Industrial lasers, Capacitor charging, X-ray and Electrostatic paint deposition.

CIRCLE 255

UNIVERSAL VOLTRONICS

SNAP-ACTION SWITCHES

All new Catalog 105 has 72 pages featuring the new sealed rocker K Series and detailing an in-depth line of precision snap-action push-button, toggle, rocker, limit and basic switches. All feaure OTTO's unique design assuring low contact resistance, high contact pressure and long cycle life. Quality made in the U.S.A.



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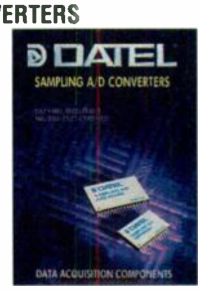
OTTO CONTROLS

SAMPLING A/D CONVERTERS

DATEL announces new 348-page catalog! Sampling A/D Converters (10-16 bits to 20MHz), Flash Converters, CDS Circuits, S/H Amps, D/A Converters, Mux's, Op Amps, Active Filters, Ap notes. MIL-STD-883 screening. Phone: (508) 339-3000, (800) 233-2765, Fax: (508)339-6356

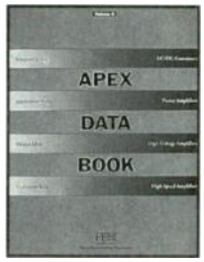


CIRCLE 257

DATEL, INC.

POWER AMPLIFIERS

Apex Microtechnology's 6th edition DC/DC Converters, Power & HV Amplifiers Data Book & Application Notes contains product data sheets on the company's high power and high voltage POAs, hi-rel hybrid dc/dc converters. These application notes provide valuable technical assistance for circuit design. The data book also provides insight on obtaining optimum performance out of these types of devices.

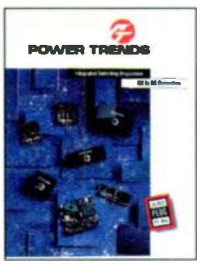


CIRCLE 258

APEX MICROTECHNOLOGY CORP.

NEW SWITCHING REGULATORS

Power Trends Inc., has released a new 72 page full line catalog for its Integrated Switching Regulators (ISRs) and DC to DC Converters. The catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product, along with mechanical configuration options and ordering information.

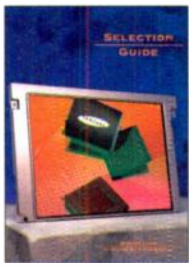


CIRCLE 259

POWER TRENDS INC.

SAMSUNG PRODUCT SELECTION GUIDE

The latest catalog is available on request by calling 1-800-446-2760. It contains product and ordering information on Memory, Micro, TFT-LCD, ASIC and RF/Microwave products offered by Samsung Semiconductor, the world's leader in memory products.



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NEW TEST & MEASUREMENT CATALOG

Keithley Instruments offers a 264 page catalog of electronic test and measurement instruments. An introduction to each product line includes technical data, applications, and a comprehensive selector guide allowing for efficient equipment evaluation. Keithley's complete line of measurement instrumentation includes digital multimeters, electrometers, sources, picoammeters,and more.

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KEITHLEY INSTRUMENTS

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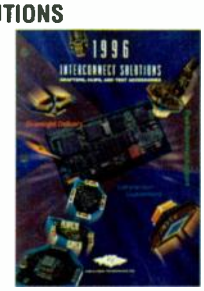

CIRCLE 264

EMULATION TECHNOLOGY

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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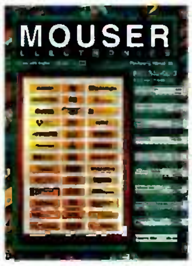

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MOUSER ELECTRONICS

IN CIRCUIT EMULATORS

Nohau Corporation is a manufacturer of In-Circuit Emulators for the 8051 family, the MCS(251 family, the P51XATM family, the 80C196 family, the 68HC16 family, the 683XX family, and the 68HC16 family. Web Site http://www.nohau.com/nohau
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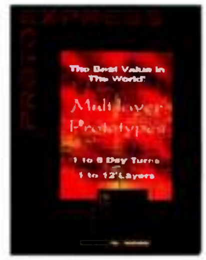

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The Relex Reliability Software for Microsoft Windows and the Mac provides Reliability Predictions per MIL-HDBK-217, Bellcore, Mechanical, and CNET standards, as well as FMEA/FMECA analysis and Maintainability Predictions. The new four color 20-page catalog describes the flexible CAD Interface, extensive parts libraries, and stunning graphics.

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NEW TRIMMER CATALOG

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CIRCLE 274

C&K COMPONENTS, INC.

80186, 80196,8051 EMULATION

Signum Systems has released its 1996 catalog of in-circuit emulators. This full line catalog includes Intel processors, Texas Instruments DSP'sZilog controllers, and National Semiconductor HPC family. Call (800) 838-8012 for information. Internet address: ww.signum.com

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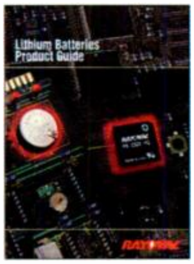
Z-WORLD ENGINEERING

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

Lithium Batteries Product Guide

Demand for high performance, small footprint, reliable and cost effective electronic devices require a good match between the battery and the technology. The Rayovac Lithium Batteries and Product Guide details: electrical characteristics, application goals, packaging and environmental effects of Rayovac Lithium batteries.



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CIRCLE 282

GRAYHILL, INC

BIVAR'S NEW 96/97 CATALOG

The new catalog lists LED assemblies, holders, mounts and mounting products for virtually all configurations. Assemblies include all standards, as well as all popular variations and options for customer-specific orders. Assembly versatility and reduced inventory are assured by molded or extruded LED hardware for vertical, dual, tri-level and quad-level LED mounts. Phone: (714)951-8808, Fax: (714) 951-3974

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BIVAR, INC.

PENTEK 1996 PRODUCT CATALOG

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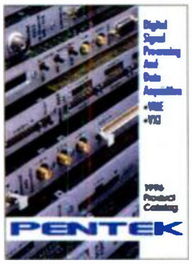

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CIRCLE 285

CHRONOLOGY

CRYSTAL OSCILLATOR CATALOG

A new product catalog and selection guide from Champion Technologies features their full line of crystal oscillators. Technical information, specifications and mechanicals are featured in this catalog for over 60 of Champion's VXCOs, TCXOs, VCTCXOs, data clocks and related products. Frequency ranges up to 155.52 MHz for general purpose to high frequency or tight stability applications.
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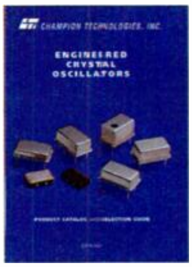

CIRCLE 286

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CIRCLE 289

ROLYN OPTICS CO.

1966 SRAM Data Book

In a continuing effort to provide advantages to its customers, Micron Technology, Inc. , Boise, ID, recently published its 1996 SRAM Data Book. The updated edition includes pipelined and flow-through sections for Micron's SyncBurst SRAMs, a Synchronous SRAM Modules section, and several new technical notes and data sheets. Contact: Susan L. Littleton (208) 368-3850

CIRCLE 292

MICRON TECHNOLOGY, INC

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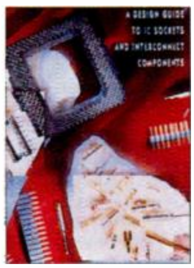

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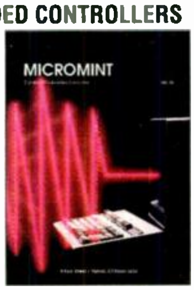

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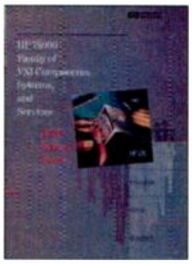

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PRECISION INTERCONNECT

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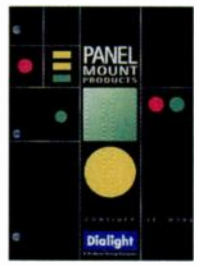

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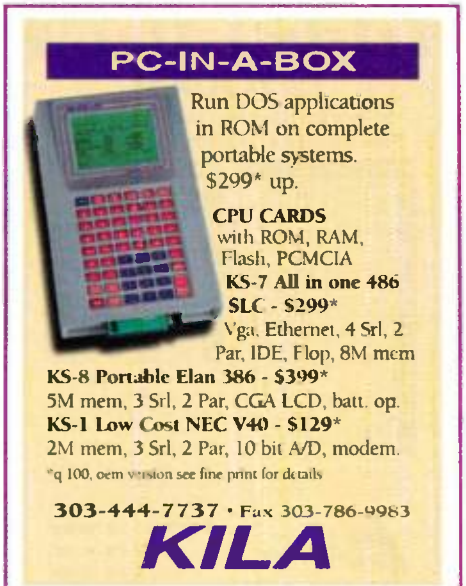

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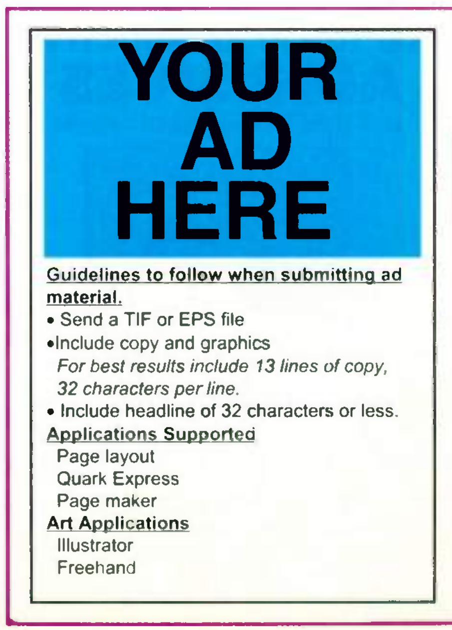

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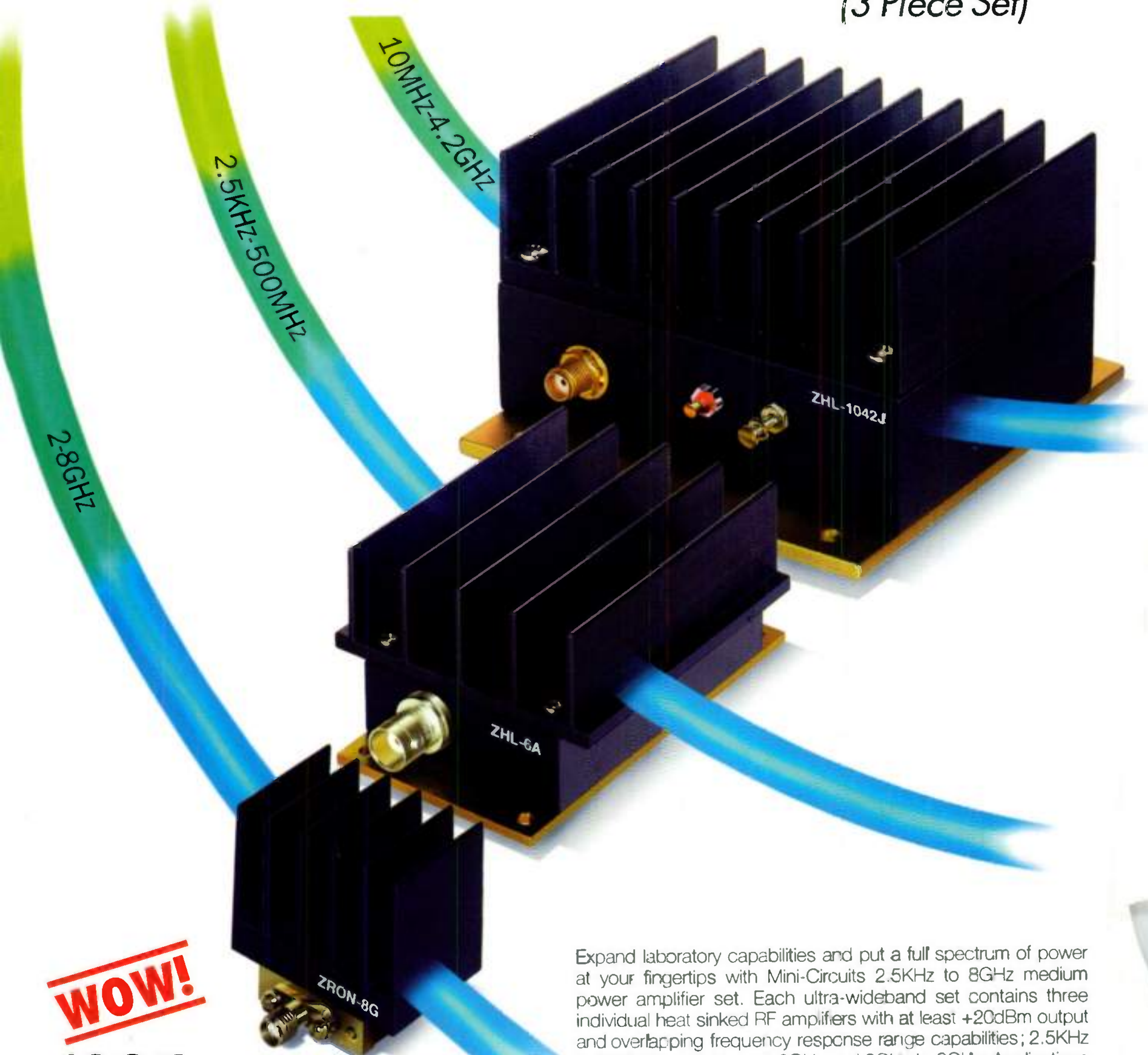

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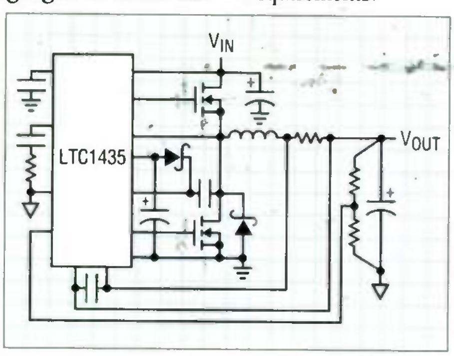

The LTC1435 operates with efficiencies as high as 95% over a 3.5V to 36V input voltage range. The 99% duty cycle capability allows inputs to drop very close to output voltages while still regulating. This means the LTC1435 can handle a variety of power sources, from lithium-ion, nickel-metal-hydride and nickel-cadmium rechargeable batteries to 30V wall adapters. The 1.19V ± 1% reference ensures compatibility with the latest CPU core voltage requirements.

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