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INTRODUCTION

Since its inception, the Ideas for Design section has always been one of the bestread sections of Electronic Design. In recent years, it has consistently vied with Pease Porridge for the top spot in our periodic readership surveys. Perhaps it's the unpredictability of each section that draws readers—In the IFD section, as it's known here in the office, you never know when you're going to find that circuit you've been looking for to solve a particular design problem; And, in Pease Porridge, the creative unpredictability of Bob Pease is becoming legendary in the industry.

A little history: Ideas for Design as we know it today began in Electronic Design in March 1961, although the section title itself dates back to 1954, when it was used to designate a single, particularly useful article. In 1961, probably with more ideas coming in from readers than could ever be published one to an issue, the editors decided to publish several ideas in each issue and allow readers to vote for the one idea that they considered the most useful. At that time, no other electronics trade publication had a similar section.

Since then, we've probably published more than 4000 ideas (it's difficult to estimate, but we could figure on about 125 ideas a year for 35 years). We have often been asked why we haven't collected the ideas into a book. Actually, we have done so in the past—I have on my bookshelf right now the office copies of Volumes 3 and 4 of "400 Ideas for Design" published by Hayden Book Co. in 1976 and 1980, respectively. Volume 1 was published in 1964, and Volume 2 in 1971 (our office copies of those earlier volumes took a walk a long time ago.) Today, we have our CD-ROMs covering the complete contents of Electronic Design from 1989 through 1994, and we now are working on getting complete copies up on the Internet.

In this supplement, we have collected many of the ideas that were voted "Best of Issue" by our readers in Electronic Design from early 1995 through early 1996. We hope you enjoy reading it and, more importantly, find it useful. We'd like to hear from you, because we plan to publish another, similar supplement in 1997, containing the Ideas for Design voted Best of Issue for a corresponding time frame.

One final note: In several places throughout this supplement, you'll notice small boxes calling for readers to contribute articles to the Ideas for Design section. The fact is that we rely on our readers to supply the brief articles that make up Ideas for Design. We encourage all readers to participate in the IFD program, and share their innovative ideas with other readers.

> STEPHEN E. SCRUPSKI Editorial Director

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Charge Pump Generates Gate Drive

CHESTER SIMPSON, 3360 Tracy Dr., Santa Clara, CA 95051; (408) 296-1925.

any products that are loaded with logic hardware use 5 V as the main power source. The management, distribution, and conversion of this main 5-V rail often requires power FET devices. These devices are used as "switches" either in a dc mode (to connect or remove power to specific circuits) or in an ac mode (where the FET is driven at high frequency to provide dc-dc conversion).

In most cases, an n-FET makes a much better switch than a p-FET because of drastically lower cost, much lower on-resistance, and greater selection and availability of product. The only drawback of using an n-FET is that it requires "highside drive" for the gate, which means a voltage source must be available that's higher than the 5-V rail. This "gate-drive voltage" needn't be well regulated, because it's simply used to pull the gate up high enough to turn the FET fully on.

The amount of voltage required for gate drive to assure the FET is fully turned on is typically about 5 V higher than the drain. Consequently, in 5V systems, the available drive must be at least 10 V. Of course, more voltage is better, since it results in reduced on-resistance for the FET and, correspondingly, less power dissipation.

The amount of current that the gate-drive source must provide depends on the application: If the gate drive is only for FETs used as dc switches, then a few hundred microamperes is sufficient (the amount of dc current that flows into the gate is negligible). However, if the gate-drive source is used to provide bias voltage to a high-frequency converter, it may require 30 to 40 mA of average current. That's because the 2000 to 3000 pF of gate capacitance present on a typical power FET must be charged up and down at 100 kHz or more, and that takes a lot of current.

This Idea for Design presents a charge-pump circuit that's well suited for generating a gate-drive rail for either application, showing how to optimize selected components to address the "high current" or "low current" requirements that were stated previously.

The "high current" version will address applications requiring up to 40 mA, while the "low current" version is a lower-cost alternative providing up to 1 mA.

A charge pump is usually preferable to a typical switching converter for applications in which load current is < 50 mA. That's because it can be built with inexpensive, off-theshelf components, it requires no transformer or inductor, and it produces zero EMI interference. Charge-pump (voltage-doubler) ICs are on the market, but they won't work in this case due to the fact that they only generate about 8 V from a 5-V input (two doublers could be used, but the cost is prohibitive).

The design shown is a voltage tripler, which provides the right amount of voltage needed for gate drive in a 5-V system (about 10 to 14 V) (*Fig. 1*). The circuit boosts the 5-V input by charging capacitors C1, C2, and C3 so that the voltage across C1 approximately equals $3 \times (V_{in}-V_{diode})$. Resistors R5 and R6, as well as capacitors C4 and C5 are



1. A CHARGE PUMP built as a voltage tripler can provide just the right amount of voltage needed for gate drive in a 5-V system.

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used to set up the LM555 (U1) as an astable (free-running) oscillator that produces a 40-kHz square wave of 50% duty cycle at pin 3 (any typical ceramic capacitors can be used for C4 and C5).

On each complete cycle, C3 is charged up to about 4.3 V through CR3 when pin 3 of U1 pulls down to ground. When pin 3 is driven high (up



2. THE CURVES indicate the output voltage delivered by the high-current and low-current versions of the voltage tripler as a function of load.

to about 4 V), Q2 is turned on pulling the negative side of C2 to ground, and C3 charges C2 up to about 8 V through CR2. When pin 3 of U1 again goes low, Q1 turns on and pulls the negative side of C2 up to 5 V, which means its positive side swings up to about 13 V. This charges C1 up to about 12 V through diode CR1. As the charge pump operates, this cycle repeats continuously to keep delivering current to C1, which flows into the load connected to the VG point. The voltage seen at VG depends on load.

Obviously, optimizing the components used makes a better design. Therefore, if higher current (up to 40 mA) is needed, CR1-CR3 must be Schottky diodes similar to 1N5818. Also, C1-C3 must be 10- μ F aluminum electrolytic capacitors. For a low-curent version, if 1 mA of load current is sufficient for the gatedrive source, 1N4148-type diodes are best for CR1-CR3, and 0.022- μ F ceramic capacitors can be used for C1-C3 to save on cost and size.

The curves show the output voltage delivered by both versions of the circuit (using the components called out in the schematic diagram) as a function of load current (*Fig.* 2).

Voted "Best of Issue," Electronic Design, September 18, 1995

Sine Waves With Crystal Accuracy

RONALD MANCINI. Harris Semiconductor, P.O. Box 883, M/S 58-096, Melbourne, FL 32902-0883.

any test and design functions require a sine-wave signal source with excellent frequency accuracy. Although signal generators are used for accurate sine-wave signal sources in the initial design stages, they're too costly to dedicate to manufacturing test functions. One option is to design a sine-wave crystal oscillator, but it can be costly because the design task is difficult and risky.

Another option (*see the figure*) can replace signal generators in fixed frequency applications. The HA7210 crystal oscillator, which is typically used as a square-wave generator, functions as the basic oscillator circuit because it solves a myriad of design problems, such as startup, wide frequency range, and cost. The circuit topology is a Pierce oscillator that has a crystal- π circuit in its feedback network. The crystal- π network also functions as an excellent crystal filter, delivering a pure sine wave of the selected frequency at its output.

In this application, the HA7210 is configured as a 1-MHz oscillator with the other functions, such as enable, not being used. The frequency can be modified by changing the crystal and digital code on the frequency-select input pins. Notice that the sine-wave oscillator input is taken from pin 2 of the HA7210 (a node that's recommended for the crystal connection) rather than the square-wave output.

The node, which is the output of the crystal- π feedback network, is very sensitive to loading and stray capacitance, so the circuitry buffering the sine-wave source must not load down this point. If the feedback node can be buffered without affecting the oscillator's stability or sine-wave purity, the problem is solved. The CA3130 is selected as the buffer because it has a 14-MHz bandwidth, and its extremely high input impedance minimizes loading on the oscillator: C1 and R1 couple the sine wave from the oscillator to the CA3130

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buffer. The buffer input impedance is 1.5 T Ω in parallel with 4.3 pF. If C1 is selected as 3 pF, the overall loading capacitance seen by the oscillator is 1.77 pF, which has no adverse effect on the oscillator. R1 is selected as 40 M Ω to provide a path for the buffer input bias current (it can be as large as 50 pA). This component selection yields a clean sine wave with an offset voltage of approximately 2 mV and a 2.5-V p-p amplitude.

The buffer's sine wave output leads the digital output of the oscillator by approximately 54. Both outputs are low impedance and available for simultaneous use as signal sources.

Voted "Best of Issue,"

Electronic Design, September 5, 1995



A CRYSTAL OSCILLATOR, when used in this type of configuration, produces frequency-accurate sine waves, and thus can be used as a replacement for the costly signal generator.

Broadband Amplifier/Balanced Mixer

DON SCHENDEL, 6234 E. Aster Dr., Scottsdale, AZ 85254-4429; (602) 948-6880.



arious CMOS digital functions are usable in many analog applications. For

instance, a single CMOS package (MC74AC00) makes possible a low-power, low-noise, broadband amplifier and balanced mixer (see the figure).

NAND gates 1 and 2 are configured in a self-biased, push-pull amplifier. The 470-k, 1/4-W resistor allows the gate outputs (pins 3 and 6) to establish equilibrium with the gate inputs (pins 1 and 5) for a nominal bias potential of +2.5 V. ($V_{CC}/2$). Pins 2 and 4, when connected together, allow for an external "enable" control of the amplifier. The amplifier is enabled when the control line is in the "high state" (V_{CC}). Both ends of the bias resistor are ac-bypassed at the center points of transformers T1 and T2 by 0.01- μ F capacitors. Transformers T1, T2, and T3 are twisted-wire (transmission-line) types on small ferrite core toroids. Bandwidth and performance of the transformers are a function of the



A LOW-POWER, LOW-NOISE broadband amplifier and balanced mixer can be built using a single quad 2/input NAND gate CMOS package (the MC74AC00).

number and size of the wire turns on the type of toroids chosen for use. The upper frequency-response limit for this circuit is 60 MHz.

The balanced mixer is configured with the two remaining gates (3 and 4). Input pins 9 and 12 are connected to the secondary windings of transformer T2. Pins 10 and 13 also can be used as an "enable" control. The local oscillator (LO) potential is applied to point A (see the figure, again). The IF is realized at the secondary output of transformer T3. If point A is connected to point B (the 330-k, 1/4-W resistor and 0.01-µF capacitor node), a bias of +2.5 V is applied to pins 9 and 12 of gates 3 and 4 of the mixer. In this configuration, pins 10 and 13 become the drive points for the LO potential. This lowers the drive power required of the LO source and reduces LO power common-mode, inverse feedback through the amplifier stage.

Transformer T3 can be replaced by a small audio transformer, such as a 1-k ct : 8 Ω for direct conversion of either AM or SSB signals. The broadband amplifier exhibits power gains of 12 dB and greater with a noise factor 4.5 dB or less from 3 to 30 MHz. The balanced mixer offers 10 dB or greater conversion gain at a



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relatively low noise factor. The quad 2/input NOR gate, MC74AC02, also can be used for this function with similar performance.

However, the package pin configuration of this circuit must be changed accordingly. Other CMOS varieties, such as the 74HCxx family, may be used in this application.

Voted "Best of Issue," Electronic Design, October 2, 1995

Acquire Watt-Hour Data With RS-232

W. STEPHEN WOODWARD. Venable Hall. CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet:woodward@uncvx1.oit.unc.edu



ong-term measurement and recording of power consumption is useful when

assessing energy efficiency of electrical appliances and apparatus. For meaningful readings of "real" (nonreactive) power, the wattmeter must be insensitive to both load reactance and nonlinearity.

This circuit utilizes a symmetrical pair of transistor multipliers to directly compute the four-quadrant product of real current and line voltage (*see the figure*). The result is averaged and converted to a variable-frequency, optically isolated, RS-232-compatible pulse output suitable for direct connection to the comm port of a standard PC. PC comm port hardware interprets each pulse as the "start bit" of a valid (although meaningless) character. Simple software running in the PC then can monitor the frequency of character reception as an accurate measure of power consumption.

Looking at one perspective of the circuit, consider positive half-cycles of the ac line voltage. These cause current proportional to the instantaneous line voltage to flow through R_v and forward-bias Q4 and Q5. If the instantaneous load current through R_i is zero, then the Rv current will divide equally between Q4 and Q5 due to the inherent matching of these elements from the CA3096A array.

The current entering Q4 is inverted by A2 and summed with Q5's current at integrator A1, at which point the currents will cancel, thus reflecting the zero-power condition. However, if the current is nonzero, the resulting voltage developed across R_i will cause a mismatch in the Q4/Q5 currents. Because we're dealing with positive half-cycles, if the load current is in phase with the line voltage, every ampere of load current will make the Q5 end of R; 1.0 mV more positive than the $Q\bar{4}$ end. Each millivolt of Ri voltage causes 0.8% of mismatch in the Q4/Q5 currents, with Q4 passing more than Q5. Consequently, the currents summed by A1 will no



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longer cancel and A1 will accumulate 3.2 nA for every watt drawn by the load. The transistor multiplier's negative temperature coefficient is largely compensated by the positive temperature coefficient of the copper current-sensing resistor R1.

A1's output controls the currentto-frequency converter, which consists of A3 and Sa, Sb, and Sc. The idle state of the converter sets A3's output high. This connects C1 to A1's output and charges C2 to the 8V reference voltage developed by Q1. When A1's output voltage charges C1 enough to pull A3's inverting input higher than its noninverting input, A3's output goes low. This event initiates the discharge cycle of C1, the duration of which determines the length of the RS-232 output pulse generated by Sb through isolator O1.

Meanwhile, Sa resets the chargepump capacitor C2. This action provides frequency-proportional current feedback that, at equilibrium, accurately balances the difference between the Q4/Q5 currents, making the output frequency of the converter equal to 1 Hz for every watt of average load power. Full-scale output is 1200 Hz. For negative line half-cycles, Q4/Q5 turn off and Q2/Q3 take over power computation duties.

Voted "Best of Issue," Electronic Design, April 3, 1995

"Beeper" Finds Circuit Shorts

JIM WOOD. Inovonics Inc., 1305 Fair Ave., Santa Cruz, CA 95060; (408) 458-0552.

his design offers a way to trace resistance in the milliohm range, right to a short between bridged traces beneath a solder mask (see the figure). It simply translates resistance into an audible tone, which increases in pitch as the measured value approaches zero.

In the classic op-amp multivibrator (shown in the inset), oscillation frequency is determined not only by the R1C1 time constant, but also by the hysteresis set by the R2/R3 resistor ratio. A1 in the main figure, with current boosters Q1 and Q2, is this same configuration.

Assuming a virtual ground at the output of A2, free-run frequency is about 1 kHz-quite audible through a tiny 8- Ω speaker. Q1 and Q2 deliver a ± 10 -V squarewave to R4, dumping a ± 100 mA through a short circuit placed across the probe tips. R5 ensure than open circuit voltage never exceeds ± 0.1 V.

A2 monitors the voltage between the probes. The differential input must have its own separate path to the probe tips to eliminate test lead resistance from the measurement. Miniature "zip-cord" sold as loudspeaker wire makes a tidy two-conductor test lead.

When the probes are open, A2's gain equals the R4/R5 divider loss, and the output of both amplifiers is identical. This has two effects: First, hysteresis is greatly increased and frequency falls to a low growl, and secondly, the loudspeaker that



RESISTANCE BETWEEN BRIDGED TRACES can be translated into an audible tone with this circuit. The tone increases in pitch as the measured value approaches zero. The inset at the lower right shows a classic op-amp multivibrator.

bridges the two in-phase outputs is effectively silenced.

A dead short across the probe tips will return nothing to A2 and the circuit will squeal at its nominal 1-kHz rate. Anything less than a perfect short produces some output from A2, increasing multivibrator hysteresis and lowering the pitch. The circuit has so much "leverage," and the ear is so sensitive to pitch changes in this range, that it's easy to resolve minute resistance differences.

Any general-purpose op amp will

suffice in this circuit-a couple of 741s or an equivalent dual. Again, two wires must be taken to each probe tip and soldered securely. Also, probes must make low-resistance contact with the circuit under test. The H.H. Smith #317 probe is ideal here. Its tip is a replaceable, oldfashioned steel phonograph needle that can pierce insulating layers and dig into oxidized solder joints.

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A Miniature Broadband Antenna

M.J. SALVATI, Flushing Communications, 150-46 35th Ave., Flushing, NY 11354; (718) 358-0932.

n electrically short dipole retains its figure-eight polar pattern (with characteristically sharp nulls) at all frequencies below its half-wave resonant frequency. However, the output impedance of an electrically short dipole is so high that it can't develop sufficient power to drive the usual receiver.

Using the impedance converter shown (*see the figure*) solves this problem by providing a huge current gain so that the voltage appearing at the dipole's output can eventually drive a 75- Ω load. Combining a short (3-to-6-ft.) dipole antenna and the converter results in a broadband (3 to 30 MHz) receiving antenna that can be rotated to null out an interfering signal. Because the dipole is short and the converter's differential voltage gain is only 4 dB, the signal level will be lower than with the usual receiving antenna. But, the salient feature of this



A SHORT DIPOLE ANTENNA and impedance converter combined together can be rotated to null out an interfering signal. The converter supplies a tremendous current gain so that the voltage appearing at the dipole's output can eventually drive a 75-V load.

antenna system is its ability to reject an unwanted signal, not its gain.

The 2N5911 dual FET is configured as a pair of source followers to present a very high impedance load to the antenna, as well as power gain to drive the differential amplifier. It's extremely important to minimize the input capacitance of the source follower through proper device selection and construction technique. A high-frequency FET with low interelectrode capacitances, such as the 2N59111 or any of the Siliconix U440 family, is an excellent choice. Similarly, miniature (1/8 W) carbon-film resistors and minimal board footprints should be used for the gate connections.

The CA3028 is connected in its differential mode to combine the signals from the dipole halves into a single, ground-referenced signal. A 75- Ω collector load resistor also provides back-matching for the connecting cable. A multiplexing network, comprised of the capacitor, resistor, and RF choke connected to the output jack, allows the connecting cable to carry both the output signal and the operating current. A similar network at the power supply separates the two, so that the output signal can be applied to the receiver's 75- Ω input. The CA3028's biasing can be adjusted for equal signalpeak clipping at maximum output through the 20-k trimpot in the FET's gate-biasing circuit.

The dipole was created by colinearly joining two telescoping antennas (spaced about 0.5-in. apart) with a plastic rod jammed into their bases. This produces a dipole adjustable from 36 to 74 in. This adjustability is used only to fit the amount of space available in the reception area. There are no frequency-related adjustments because the dipole is always nonresonant at the antenna's operating frequencies (3 to 30 MHz).

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Output Voltage V

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10.5

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0/5

Example below: VKP60MT512 Vout1 = 5Vdc Vout2 = 12Vdc Vout3 = 12Vdc

1.2/0.5 2.4/1 3.6/1.5 4.8/2 6/2.5 lout₁/(lout₂ + lout₃)(A)

12.0

6/2.5

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equation $T_{\rm pw} = -R_{\rm d} \ C_2 \ ln \Bigg[\frac{V_{\rm ltp} - 1V}{V_{\rm utp} - 1V} \Bigg] + P_{\rm dly}$ $= -(1K) (330 \text{pF}) \ln \left[\frac{0.667 \text{V}}{2.333 \text{V}} \right] + 75 \text{ ns}$ = 488 ns

To approximate frequency:

$$\begin{split} F(v_{in}) = & \left(\frac{R_5 \ C_2 \ (V_{utp} - V_{ltp})}{v_{in} - 0.5 V} + T_{pv}\right)^{-1} \\ = & \left(\frac{(2.7 K)(330 pF)(3.333 - 1.667)}{v_{in} - 0.5 V} + 1.188 \ ns\right)^{-1} \end{split}$$

 $= \left(\frac{1.486 \times 10^{-6} \text{ Vs}}{\text{v}_{\rm m} - 0.5 \text{ V}} + 488 \text{ ns}\right)^{-1}$

Upon observation, the prototype circuit linearity was approximately 2% over the tested range. Also, up to 6-MHz operation was possible using the MAX942 by carefully selecting C2 and the hysteresis resistors.

On the low side, discrete transistors can be used instead of the Motorola MPQ2N2222 monolithic quad package. This may cause some instability at low frequencies. The transistors should be located in close thermal proximity. On the high side, a good matched transistor pair can be used. Analog Devices' MAT-01 is a good choice. Other high-speed comparators are available. The Spice program uses an LT1016 device from Texas Instruments (see the listing).

Voted "Best of Issue," Electronic Design, November 20, 1995

1.

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+ RC=.119 XTB=1.5 CJE=35.5P CJC=12.2P TF=500P TR=85N)

* Metorgla 30 Volt .2 Amp 300 MHz SiNEN Transistor 04-11-1991

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.SUBCHT L11016T 1 2 1 4 5 6 21
F1 3 7 V1 1

IEE 7 4 DC 100.0E-6

EVO 20 0 POLY(1) 3 0 -1.

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R 20 5 33
                                                               -1.4 1
 ADDED PULL-UP RESISTOR
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         9 2 7 QIN
8 7 QIN
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  MODEL OIN NEW (IS=800.3E-18 BF=10)
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 VI 10 5 3
VI 10 11 DC 0
  25 5 ): 6 QOC
MODEL QUE NPN(IS=800.02-18 BF=53.30E3 CJC LE-15 TF=154.3E-15 TR=4.192E-9)

        DP
        4
        3
        DX

        RP
        3
        4
        2.041E3

        RP1
        3
        6
        67

  ADDED POWER RESISTOR
  MODEL DX D IS=800.0E-18)
  ENDS
 .ENDS
.TRAN 258-9 4GE-6 20E-6
*INCLUDE FEVICE.LIB
.MODEL DN4148 D(RS=.8 CJO=4PF IS=7E-09 N=2 VJ=.6V
* TT=6E-09 M=.45 BV=100V)
+ TT=6E-09 M=.45 BV=100V)

*ALIAS V(5)=FOUT

PRINT TRAN V(5)

R2 1 9 1CK

V3 3 0 DC 1V

C2 1 4 330PF

OlB 4 6 5 QN2222

R3 9 5 10K

X1 9 4 1 0 5 0 xx LT1016T

OlC 6 6 5 QN2222
 R5 3 5 2.7K
R1 9 0 10K
        8 5 1 F
 D1 8 4 DN.4148
V1 1 0 DC +5V
  . END
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ide-bandwidth systems often need a dc-to-highfrequency automatic

gain control (AGC) circuit to amplify various signal types. Even though there are many high-speed AGC parts available, they tend to work at extremely high bandwidths and at prices that aren't cost-effective for applications today. The idea presented here takes advantage of the technology of dc variable gain amplifiers to implement an AGC circuit with an external loop.

Automatic leveling loops or gaincontrol loops are difficult to implement without affecting bandwidth when changing gain. However, highspeed monolithic variable-gain amplifiers and high-speed voltagefeedback amplifiers can be used to implement a high-performance fastsettling loop function for continuous-waveform signals (see the figure). At the same time, the loop maintains a gain bandwidth that's independent of changes in gain.

The circuit uses a variable gain amplifier (U1) in the forward path to amplify the continuous-time-domain signals occurring at Vin. U1 has two input pins with high-input impedance that provide both noninverting (pin 3) and inverting (pin 6) functions. Once one has selected the inverting or noninverting configuration, the common-mode input voltage range is set by the designer with resistor R_g . The maximum peak input voltage on pin 6 and the current through R_g is used to calculate the resistor value using the following equation:

 $R_g = Vin(peak)/I_R$

IR is the current through the resistor, which is 1.8 mA typically. The maximum common-mode range is ± 2.2 V for a ± 5 -V supply operation. The minimum usable signal level is determined by the input RMS noise.

Once the maximum required gain is determined, Rf is selected by the formula shown below, while setting



HIGH-SPEED MONOLITHIC variable gain amplifiers and highspeed voltage-feedback amplifiers are used to implement a high-performance fast settling AGC loop function.

$$V_{g}$$
 to +1 V:

$$A_{\rm V} = 1.85 ({\rm R_f}/{\rm R_g}) (({\rm V_g}+1)/2)$$

 V_g is the gain-control voltage and has a linear voltage range of -1 to +1V with a gain linearity of 0.04% for Vout of ± 2.0 V. The CLC522 attenuates the signal internally from this maximum level. Therefore, the input noise floor and the output voltage range determine the lower and upper signal limits for the part. The output voltage range is ± 4.0 V with an output current of ± 70 mA.

The maximum bandwidth is a function of the internal current-feedback amplifier and the selection of Rf. U2 has a usable selectable-gain range from 2 (6 dB) to 100 (40 dB). At a gain of 2 with V_{out} of 2 V p-p, a 330 MHz bandwidth is achieved. For gains of 20 to 100, -3-dB bandwidths of 165 MHz and 45 MHz can be expected. Adding capacitance in parallel with R_g will extend the -3dB bandwidth for gains of 10 to 220 MHz.

The low-noise dual voltage-feedback amplifiers (U2) extend the dynamic range by placing the Schottky diodes or other low capacitive diodes in the feedback path. R1 and Ry set the gain of the rectifier. The adjustable resistor (R_{adj}) sets the desired output voltage level and ensures that the initial conditions at pin 2 of U2 are +1 V with no input signal. When the rms current of the signal is greater than the negative current from R_{adj} , the integrator decreases the gain of U1. Conversely, when the signal drops below the R_{adj} current, the gain of U1 is increased. The acquisition time and hold time are set by R_x , R_y , and C.

For larger gains and smaller bandwidths, the CLC428 meets the performance bandwidth requirements. When smaller gain ranges and larger bandwidths are required, a higher unity-gain-bandwidth CLC420 or CLC440 amplifier should be substituted for U2.

Voted "Best of Issue," Electronic Design, February 5, 1996

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Low-Cost Precision Thermometry

W. STEPHEN WOODWARD. U. of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvx1.oit.unc.edu.

mong the wide variety of temperature-sensing components available, the least expensive and most available is the diode-connected transistor. Circuits exploiting the approximate -2.2-mV/degree temperature dependence of the base-emitter junction forward voltage are common and work well. They all suffer, however, from unpredictability of the characteristics of the individual transistors. Consequently, they must be recalibrated whenever the sensing transistor is replaced.

A method does exist, though, that uses the humble transistor as a precalibrated temperature sensor (see Jim Williams' article "AN45," in the *Linear Applications Handbook, Vol. II*, published by Linear Technology Inc.). This "delta-V_{be}" technique exploits the proportionality of dynamic impedance of transistors to absolute temperature. At 298K, for example, delta V_{be} is about 60 mV/decade. This number is independent of transistor device-to-device and even type-to-type variation. It can, therefore, be used to fashion precision thermometers that need no transistor-dependent calibration. However, the reference cited recommends a number of premium components that increase the cost and thus loses the advantage of using inexpensive transistors in the first place.

The circuit described here, by contrast, combines the delta- V_{be} effect with inexpensive generic parts to achieve two channels of truly lowcost "no calibrate" transistor thermometry (*see the figure*). CMOS switch S1 modulates the bias current applied to temperature sensors Q1 and Q2 over a 10:1 ratio. Only this ratio, rather than the exact current, matters in this case. The resulting square waves at the input of A1 and A2 have amplitudes directly propor-

tional to the absolute temperature of Q1 and Q2. A1/A2 scale their respective ac inputs to 10 mV/degree, yielding 2.98-V p-p square waves at 298K. Despite the fact that fairly high gain is required (34 dB), the accoupled signal path ignores offsets and permits use of inexpensive (LM324) op amps. The dc component of these signals is blocked by C3/C4 and the ac is synchronously rectified by S2/S3. This produces stable, lowimpedance (about 500 Ω) dc outputs. Multivibrator A3 produces a 400-Hz square wave for modulation and synchronous-rectification timing.

The two thermometer channels have unadjusted accuracies of better than 1 degree. Trimmer P1 allows matching of the tracking of the two to <0.1 degree. This is ideal for applications like wet-bulb/dry-bulb hygrometry and thermal-management analysis. The circuit's power consumption is less than 2 mA at 8 to

15 V, which is ideal for battery operation. P o w e r - s u p p l y feedthrough is about 0.1 degree/V = -60 dB.

Voted "Best of Issue," Electronic Design, August 21, 1995

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TWO CHANNELS of low-cost "no calibrate" transistor thermometry can be achieved with this circuit, which combines the delta-V_{be} effect with inexpensive generic parts.

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Generate FIR Filter Coefficients

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he calc_coeffs() function can calculate FIR filter coefficients h(i) for low-pass, highpass, bandpass, and band-reject filter types (*see the listing*). For an odd-valued filter length N, coefficient values having even-symmetry about the h[(N - 1)/2] coefficient (i.e., h(i) = h(N - 1 i) will exhibit linear phase. This makes the filter's time delay (Td) independent of frequency. Td = (N - 1)/2fs, where fs is the sampling frequency in hertz. The first half of the coefficients, 0 through (N - 1)/2, are stored in the filter_coeffs (MAX) array.

To reduce stopband ripple, a Hamming window (window_type = SNGL) is applied as weighted factors to the filter coefficients. By applying the window a second time (window_type = DUAL), the stopband attenuation substantially improved at the price of broadening the transition region (see the figure).

All filter types and filter lengths above 15 exhibit excellent passband ripple of less than 0.1 dB with respect to unity gain. The low-pass characteristics illustrate both the broadening of the transition region and deep stopband attenuation (*see the table*).

The FIR filter gain H(f) can be calculated as follows:

$$H(f) = h[(N-1)/2] + 2\sum_{i=0}^{\frac{N-3}{2}} h(i) \cos \left[2\pi \left(\frac{N-1}{2} - i\right)f\right]$$

for f = 0 to 0.5 Hz The f1 and f2 definitions (normal-



THE CURVES show the FIR filter bandpass characteristic when applying a single Hamming window and a dual window. When the window was applied a second time, stopband attenuation improved substantially.

Filter length	f2/fs	
(N)	f2 + 0.05 Hz	f2 + 0.1 Hz
31	-11 dB (-6)	-59 dB (-23)
41	-19 dB (-10)	-57 dB (-52)
61	-56 dB (-23)	-57 dB (-96)
81	-59 dB (-54)	-59 dB (-88)
101	-58 dB (-82)	-61 dB (-88)
127	-62 dB (-81)	-69 dB (-90)
() = dual windowed		

ized) are:

 $f_{low} f = f_{high}$

Low-pass filter: f1 = 0; f2 = cut-off frequency

High-pass filter: f1 = pass frequency; f2 = 0.5Bandpass/band-reject filter: f1 = At the pass frequencies, the gain is down 6 dB. A frequency offset (plus or minus) should be applied for other values of gain.

Voted "Best of Issue," Electronic Design, June 26, 1995

```
#include <math.h> // FIR FILTER COEFFICIENTS PROGRAM
                                                                                                                                 (i = 0; i <= (filter_len-1)/2;i++ ) {
                                                                                                                         for (1 = 0; 4
double arg;
arg = 2.0 * PI/(filter_len = 1);
ham_coeffs[i] = 0.54 - 0.46 * cos(arg * i);
if(window_type == DUAL ) ham_coeffs[i] *= ham_coeffs[i];
#define MAXLEN 127 //Maximum filter length
#define MAX (MAXLEN+ 1)/2)
#define PI (4.0*atan(1.0)) //Define pi constant
#define LPF 1 //Enumerate filter types
#define UPP 2
                                                                                                                        / Calculate filter coeffficients and pass through window
f(filter_type == BRF ) ( Fl = 0.0; F2 = fl;)
lse(F1=f1;F2=f2;)
#define HPF
#define BPF
#define BPF 3
#define BRF 4
#define SNGL 1 //Hamming window
#define DUAL 2 //Hamming window squared
                                                                                                                             if((filter_type == BRF) && (!flag)) { flag= 1; F1 = f2; F2 = 0.5;}
   int i, flag = 0
double ham_coeffs[MAX], A,B,C,F1,F2;
                                                                                                                          else break:
                                                                                                                       // Calculate DC component value of coefficients
if( filter_type == LPF) filter_coeffs(i) = 2.0 * f2;
if( filter_type == HPF) filter_coeffs(i) = 2.0 * (0.5 - f1);
if( filter_type == BFF) filter_coeffs(i) = 2.0 * (f2 - f1);
if( filter_type == BFF) filter_coeffs(i] = 1.0 - 2.C * (f2 - f1);
   //Clear filter_coeffs array
for(i = 0; i < MAX;i++ ) filter_coeffs[i]=0.0;</pre>
   // Calculate Hamming Window Coefficients
```

World Radio History

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World Radio History

Save Energy In Snubber Network

FERNANDO GARCIA. General Instrument Co., 1330 Capital Pkwy., Carrollton, TX 75006.

eakage inductance, always a nuisance in switch-mode power supplies, is the main instigator of voltage overshoots. These voltage spikes may damage the power-switching devices unless they are tamed by a snubber network.

Though snubber networks perform the required task of protecting costly devices, it comes at the expense of efficiency. The efficiency penalty is usually regarded as nominal, but in the face of ever increasing requirements, additional techniques must be found.

One idea along that route would be to return the wasted snubber energy to an auxiliary output, such as, for instance, on flyback regulators. A flyback regulator offers the advantage of providing multiple output voltages with a single magnetic structure, and is therefore very compact and cost-effective (*Fig. 1*).

This particular circuit has a main +5-V output, as well as a +12.5-V



2. THE MODIFIED snubber network's operation at pin 4 of U1 is shown in this waveform (vertical scale: 10 V/div; horizontal: 2 ms/div).

auxiliary output. The device being driven also required a "bias" voltage of +27 V with a few milliamperes of current.

Originally, the voltage was going to be provided with a charge-pump technique, but closer inspection showed that the voltage could be obtained without any additional setup.





The heart of the regulator is formed by a National Semiconductor LM2577-ADJ "simple switcher" controller IC. The main and auxiliary voltage configurations came straight from the company's application literature, with resistors R1 and R2 providing the feedback for the main +5-V output. The auxiliary +12.5-V output is regulated by the intrinsic tight coupling of a discontinuous-mode flyback topology. R3 and C1 are compensation devices.

Whereas another winding could have been used in the transformer to provide the +27-V bias output, a "free" output may be realized from the voltage spikes in the primary winding being transferred via diode D3 to a reservoir capacitor (C4). The charge in the capacitor is drawn by the current of both the bias load and the shunt Zener regulator D4. Enough charge is depleted from the capacitor to allow the next voltage spike to almost fully dump its energy in the next cycle.

In a sense, this is a modified snubber network where the energy is being put to good use instead of wasting it as heat on a resistor. Figure 2 shows the network's operation.

Further efficiency points may be gained by returning the shunt Zener current to the +5-V supply. The Zener current contribution is small enough to only negligibly effect the voltage regulation.

Because the capacitor doesn't discharge completely to 0 V due to the Zener's voltage, this modified snubber isn't as effective as the traditional "lossy" snubber.

However, for applications that do not require extreme operating conditions, the circuit offers a useful cost reduction and efficiency improvement.

Voted "Best of Issue," Electronic Design, May 1, 1995
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ZOS-75	37.5-75	-110	0.016	-26
ZOS-100	50-100	-111	0.026	-29
ZOS-150	75-150	-107	0.017	-26
ZOS-200	100-200	-106	0.015	-25
ZOS-300	150-280	-103	0.017	-27
ZOS-400	200-380	-10€	0.021	-24
ZOS-535	300-525	-96	0.018	-27
ZOS-765	485-765	-96	0.033	-27
ZOS-1025	685-1025	-92	0.051	-25

Notes: Tuning voltage 1 to 16V required to cover freq, range. Power output +9dBm Typ. (Main). Power 12V DC, +130mA (MAX.). Operating temperature range: 55°C to +85°C.





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Battery Charger Made More Efficient

HERB SEIDENBERG. Toshiba America Information Systems, 2 Musick St., Irvine, CA 92718; (714) 587-6930.

he project at hand was to build a small, efficient, inexpensive, full-function battery charger that could charge 2 to 10 NiCd or NiMH cells. Choosing the charging controller, the Maxim MAX712/713, was simple because it was the only one that was pin programmable and didn't require software development. For reasons of efficiency, a switching regulator instead of the standard pass regulator had to be added. But, the MAX713's application notes suggested non-standard, non-state-ofthe-art switching regulators as well as complex feedback loops.

Instead, a switching regulator that could be set up as a constant current source was needed. This would bypass the current sensing of the MAX713 and eliminate its relatively larger current-sense resistor. Connecting the negative end of the battery directly to ground provides more voltage and reduces IR losses.

Linear Technology's LTC1148HV synchronous step-down switching regulator seemed to fill this role because it's more than 90% efficient, it features two current sense inputs (Sense+ and Sense-), and a current control pin (I_{th}) that has a dc input linearly related to the maximum coil current (*Fig. 1*).





For example, with a low, commonly available 0.1 Ω sense resistor and I_{th} connected to the 2-V reference

output of the MAX713, the peak coil current is set to 1.55 A. The average current will still vary with output



1. THE LTC1148HV SYNCHRONOUS STEP-DOWN switching regulator was found to be the best fit as a constant current source for the MAX713 charging controller.

BEST IDEAS FOR DESIGN Ideas voted "Best Of Issue" by the readers of Electronic Design

voltage, but this can be compensated for by feeding back some of the output voltage to $I_{\rm th}$. A spreadsheet can help calculate the values of resistors R5, R6, and R8 for the desired current level and linearity.

The constant-voltage regulation loop of the LTC1148 is disabled once the voltage divider (R2 and R7) for VFB is set above the highest voltage that the battery is going to reach during charge.

With the battery above the constant voltage regulation point, the switching regulator will supply no current.

If a trickle-charge current is desired, a switch (U5A) and a resistor (R14) can be added that supply the desired current directly from the primary dc source (V_{in})—a simple wall cube—when the MAX713 controller terminates fast charge or

during battery undervoltage condition at startup.

Some other important aspects of the MAX713 that should be kept in mind (*Fig. 2*):

•The NC switch in J2 detects if no battery is plugged in and disables the switching regulator through the shutdown input.

•Diode D2 indicates if power is applied, while D3 signals if the charger is in the fast mode.

•Connecting PGM0 and PGM1 to the proper voltage selects the number of cells to be charged; PGM2 and PGM3 select the maximum charge time.

•Upon timeout or dV/dT detection, FASTCHG goes inactive, which disables the switching regulator through the Shutdown pin, turns the green LED off, and turns the tricklecharge switch on. •Thermistor voltage dividers can be added to the TEMP, THI, and TLO pins of the MAX713 to provide temperature trip points.

•The maximum number of cells (10) is limited by the maximum V_{in} of the MAX713 and the LTC1148, which is 20 V. With a larger number of cells, ripple voltage on V_{in} becomes a limiting factor.

•To make L1 as small as possible, the switching frequency of the LTC1148 can be set as high as 250 kHz.

The circuit is optimized for charging six cells at 400 mA. It has a timeout of 4.4 hours, a trickle charge of 24 mA, an open-circuit voltage of 11.5 V, a supply voltage of 12 V, and a switching frequency of 125 kHz.

Voted "Best of Issue," Electronic Design, May 15, 1995

Measure Picoamperes With DVM

MARSHALL J. BELL. B.I. Instruments, 221 Kingslynn Rd., Stoughton, WI 53589; (608) 873-6449.

any times, the need arises to measure current below 1 μ A. The circuit shown helps along those lines, as it turns any voltmeter into a picoammeter with scales of 1 nA/V and 1 μ A/V (see the figure).

By using a 3-1/2 digit voltmeter with a resolution of 1 mV, the readout will be in picoamperes or nanoamperes. In addition, it can be attached to an oscilloscope. The frequency response is about 1 kHz for the 1 μ A/V setting and 150 Hz for 1 nA/V.

Looking at the circuit, U1B forms a transimpedance amplifier. With S1 in the position shown, the transimpedance is 1 M Ω . In the other position, a gain of 1000 is added to make the total transimpedance 1 G Ω .

R1, C1, D1, and D2 protect the input from high voltages, and R5 isolates the op amp's output from any



THIS PICOAMPERE PRECONDITIONER allows a digital voltmeter to evaluate photdiodes and the shutdown current of ICs.

load capacitance.

The op amp's input current and voltage offset must be low for this circuit to work. In this case, a Linear Technology LT1047 was used. It has a nominal input bias current of ± 5 pA and a VOS of $\pm 3 \mu$ V at room temperature.

Five units were tried and they produced an output of less than 1 mV in the 1 G Ω range, so the manufacturer's ratings are conservative.

U1A is used to split the 9-V battery into positive and negative supplies. The LT1047 is overkill for this purpose, but it made the task easier. The total current is essentially the supply current of the op amps.

For the prototype, the total current measured for the LT1047s was $< 100 \mu$ A, so a standard 9-V battery should last six months if you forget to turn it off.

The entire circuit fits into a box small enough to hang off the input of a voltmeter or oscilloscope.

Voted "Best of Issue," Electronic Design, December 16, 1995

World Radio History

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Feedback Improves Notch Filter Q

ERIC KUSHNICK. LTX Corp., LTX Park at University Ave., Westwood MA 02090-2306; (617) 461-1000.

n Electronic Design's February 20, 1995 Ideas for Design section, a high Q bandpass/band-reject filter is described (see "Tunable Filters Cover Wide Range," p. 110). The filter does indeed have a very high Q as a bandpass filter, but as a notch filter, the Q is about 1/5 (Q = F_{notch}/(BW at -3 dB)). However, the notch filter Q can be increased to almost any desired value by adding a little positive feedback.

The schematic illustrates a 60-Hz notch filter with positive feedback (Fig. 1). If the optional buffer is connected between points A and B instead of the short circuit, then the resistors determining the positive feedback (R4 and R5) are completely independent of the resistors determining the notch frequency and notch depth (R1, R2, and R3). In this case (with the buffer), the exact equations and F notch apply, Ŧ $1/(2\pi C \times (3 \times R1 \times R2)^{1/2})$, where R1 = R1A + R1B and C1 = C2 = C3 = C.

R3 determines the depth of the notch, and for the buffered case, the maximum notch depth occurs when R3 = 6(R1 + R2). The Q may be independently adjusted by varying the



2. THE NOTCH FILTER'S RESPONSE, with K=0.96, shows a Q of about 5.

factor K, the ratio of R5 to (R4 + R5). The Q is approximately equal to $(1/5) \times (1/(1 - K))$. In actual practice, however, the value of R4 often is much less than the values of R1, R2, and R3. In this case, the optional buffer can be



1. BY ADDING POSITIVE FEEDBACK, a notch filter's Q can be increased to almost any desired value.

replaced with the short circuit between points A and B. The equations for F_{notch} , Q, and R3 now are no longer exact, but a little tweaking of the values on a simulator can bring back the desired response. The values shown were optimized for the "no buffer" case in a short period of time.

The response of the bufferless circuit in Figure 1 is shown with K equal to approximately 0.96, and with K = 0 (to get K = 0, disconnect the top of R4 from the op amp and ground it) (*Fig.* 2). With K = 0.96, the Q of the notch filter is about 5.

By making R1 less than R2, small changes in R1 can affect the notch frequency much more than the notch depth, because the notch frequency depends on the product of R1 and R2, while the notch depth depends on the sum of R1 and R2. This allows the filter frequency to be easily adjusted for production variations in the values of the three capacitors, C1, C2, and C3, which helps reduce the effect of production variations and makes the filter easy to produce.

Voted "Best of Issue," Electronic Design, Februay 19, 1996

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Transformer-Less DC-DC Converter

V. LAKSHMINARAYANAN. Centre for Development of Telematics, Sneha Complex, 71/1 Miller Rd., Bangalore-560 052, India.

his configuration should prove handy in situations in which dual-polarity supplies are needed for a few devices on a board that has only one +5-V supply. The circuit doesn't use any dc-dc converter ICs, nor does it require any transformers or inductors. Three Schmitt-trigger inverters, such as the 7414, form the heart of the circuit (see the figure). One inverter is configured as a high-frequency astable multivibrator emplo-ying a single resistor and a capacitor. For the RC values shown, the frequency of the astable output is around 100 kHz. The oscillation frequency is given by f = 1/T, where:

 $T = R1C1 \ln[(1 - V_{CC}/V_{LT})/(1 - V_{CC}/V_{UT})]$

where $\bar{R}I$ and C1 are the timing components of the astable, V_{CC} is the supply voltage, and V_{LT} and V_{UT} are the lower trip point and upper trip point of the Schmitt trigger (in this circuit, $V_{LT} = 0.9$ V, $V_{UT} = 1.7$ V, and $V_{CC} = 5$ V, because standard TTL is used).

The astable's output drives a pair of inverters that, in turn, drive a pair of diode-capacitor voltage-doubler circuits. The outputs of the



WHEN SEVERAL DEVICES on a pc board require dual-polarity supplies and there's only a single +5-V supply, this circuit may be useful. It has no dc-dc converter chips, no transformers, nor any inductors.

diode-capacitor circuits are around 8.5 V with the polarities shown. Diodes D1-D4 should be fastswitching types like the 1N914 or 1N4148. As a result, the circuit can generate ± 8.5 V from a single ± 5 -V supply, making it useful in many applications. Because the device doesn't have any coils or transformers, it saves pc-board space and reduces cost.

Voted "Best of Issue," Electronic Design, October 13, 1995

Portable Airspeed Measurement

W. STEPHEN WOODWARD, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvxl.oit.unc.edu.

omputer-compatible airflow instruments are widely available but are usually expensive, bulky, and mechanically fragile. This anemometer continuously converts airspeed in the range of zero to tens of meters per second into an RS-232-compatible data stream while overcoming those drawbacks. It's battery-powered and, when combined with a laptop or notebook PC, consists of a fully portable airspeed measurement system.

The anemometer's principle of

operation is that of the familiar constant temperature hot-wire anemometer. In this case, the relationship between electrical resistance and the temperature of tungsten wire is used to monitor and regulate the temperature of a heated filament exposed to the airflow. The power needed to maintain a constant difference between ambient and filament temperatures then can be used to directly calculate airspeed via "King's Law." The law states that the rate of heat loss is proportional to the temperature differential

between air and filament, multiplied by the square root of airspeed.

In this version (see the figure), comparator U1 monitors the ratio of the resistance of filament F1 (a denuded Radio Shack #272-1141 incandescent lamp) to reference R3. Whenever Rw < R3/R10, U1 triggers timer U2 to apply heating pulses from battery V1 to F1 via Q1. The result is to maintain a constant filament temperature of approximately 250°C.

The average power dissipated in the filament is given by: $F_p \times T_h \times V_w^2/Rw$, where F_p = pulse frequen-

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THIS ANEMOMETER continuously converts airspeed, ranging from zero to tens of meters per second, into an RS-232-compatible data stream.

cy, T_h = heat pulse duration, V_w = pulse amplitude at the filament, and Rw = filament resistance. Th is generated by a linear timing ramp produced by Q2's collector current as it charges C2 to U2's threshold voltage. Because Q2's collector current is made proportional to V_w^2 and to ambient temperature, T_h is inversely proportional to these factors. This feature compensates the quantum of heat delivered by each pulse against variations in battery voltage and air temperature, and keeps F_p proportional to the square root of airspeed. Maximum F_p (corresponding to 20 \pm meters/s) is 1370 Hz.

Each filament heating pulse causes Q3 to transmit an RS-232 start bit to the COM port (formatted for 9600 baud, 1 start, 1 stop, 5 data, and no parity bits) of the connected computer. A simple software routine tallies these pulses and averages their frequency. Subtraction of an empirically derived zero offset from the average, squaring, and normalizing it with a suitable scaling constant produces the final airflow measurement.

Battery life is extended by applying filament power only when the

COM port is "Open" and by the wide range of battery voltage (4.6 to 6 V) compatible with the accurate anemometer operation. As the battery finally does reach end of life and V_w drops below 4.5 V, T_h becomes longer than 677 mus (the longest start bit compatible with COM-port framing requirements). The resulting "framing error" provides a reliable "low battery" warning.

Voted "Best of Issue," Electronic Design, January 22, 1996

Optically Isolated Precision Rectifier

W. STEPHEN WOODWARD. Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvxl.oit.une.edu

solation amplifiers and precision rectifiers are widely available functions. With this circuit, both functions can be combined in one topology (see the figure). It achieves excellent rectification symmetry and zero stability, and Therefore, the voltage developed

good linearity (better than 1%) and frequency response (>10 kHz), with a minimum of precision components.

Al acts as a voltage-to-current converter by servoing the current through the D1-D4 bridge and L1.

across R1 equals the instantaneous input voltage. The diode bridge's fullwave rectification causes L1 to be forward-biased regardless of the polarity of the input voltage. The magnitude of the bias controls the intensity of optical coupling between **Designers** set standards for excellence in our most critical industries. Often, lives and livelihoods depend on the circuits you design. Your goal: design better circuits faster. Since our inception, MicroSim has been setting the standards for desktop EDA systems that enable you to do just that. Try our evaluation software. See how MicroSim can help you set tomorrow's standards.





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L1 and Q1, and, thereby, the magnitude of Q1's collector current.

A2 servos the current through L2 and R2 so that the current passed by Q2 balances that passed by Q1. Because of the good tracking of elements of the PS2501-2 dual optoisolator, a constant ratio exists between L1 and L2 currents. Consequently, R2 can be adjusted so that the output voltage across R2 is equal to the rectifier's isolated input voltage.

R3 and C1 provide frequency compensation for the L2-Q2 feedback loop. D5 prevents potentially destructive reverse bias of L2.

If the input voltage range is very large compared with the forward drops of D1-D5 and L1, such as when the 120 V ac mains must be monitored, A1 can be eliminated and the input voltage simply applied directly to the bridge, optoisolator, and suitable R1. All the while, good accuracy is maintained. Moreover, in this instance, the need for isolated dc power supplies for the isolated op amp would also disappear.

Voted "Best of Issue," Electronic Design, June 12, 1995



AN ISOLATION AMPLIFIER and precision rectifier can be combined in one topology, as demonstrated here. Only a handful of precision components are required to attain its zero stability, better than 1% linearity, and excellent rectification symmetry.

Linear DAC Has Nonlinear Output

CHARLES G. BAGG. 17 Drake Rd., Fitchburg, MA 01420; (508) 342-7603.



hen controlling a nonlinear device such as an incandescent lamp, it is

desirable to have fine resolution at the high end, where a small change in current may cause a large change in brightness. At the low end, where the filament is not even glowing, coarser resolution is quite adequate. Log DACs are available, but they have their fine resolution at the wrong end.

Using the simple circuit shown (Fig. 1), any desired compression can be produced using just about any multiplying DAC. A negative 10-V reference is fed through R1 to inverting amplifier A1, which has



1. WHEN CONTROLLING A NONLINEAR device, this circuit can produce any desired compression using just about any multiplying digital-to-analog converter.

an initial gain set to unity by R2. A1's output supplies a positive variable reference to the DAC.

The DAC output provides additional feedback through R3, reducing the amplifier's gain as the DAC data increases. (You can also think of A1 as a fixed-gain summing amplifier in which the DAC output is subtracted from the 10-V reference input). Either way, the variable reference is gradually reduced so that each step is progressively smaller than the one before.

With the values shown, as the DAC data approaches full scale, the reference approaches 1/4 of its original value. This gives the output four times as much resolution at the high end as at the low end. By decreasing the value of R3, greater compression and higher resolution can be achieved. The

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variable-reference output also may be useful in some applications.

The math is surprisingly simple. Since the DAC feeds back a fraction of the variable reference voltage to R3, it multiplies the effective value of R3 proportionally. Therefore, the equivalent resistance, R_E, equals R3 times (DAC resolution/DAC data). The parallel resistance of R2 combined with R_E equals (R2R_E) / (R2 + R_E), which we'll call R_P The gain of A1 now is simply R_P/R1.

For a quick approximation, remember that when the data is zero, resistor R3 is out of the circuit. When the data is all ones, the DAC is practically a straight piece of wire, so that R_E is approximately equal to R3. The step size is always the variable reference divided by the DAC resolution.

It's easy to set up a spreadsheet



2. BY MIXING AND MATCHING the resistor values for the DAC and the reference voltage in a spreadsheet and plotting the results, the proper amount of compression can be obtained. Here, an 8-bit DAC was used.

with a series of values for the DAC data and plot the results (Fig. 2). Then the resistor values and reference voltage can be adjusted to get the desired compression.

Voted "Best of Issue," Electronic Design, April 17, 1995

Single Comparator Window Detector

JOSEPH V. D'AIRO, 424 Higbie Ln., West Islip, NY 11795; (516) 661-1694.

imply by adding two steering diodes, a window detector can be built using only a single comparator. The detector performs well for windows of about 1 V or greater, but it isn't suitable where extreme precision is required because the forward drops of the diodes vary.

In the basic circuit (Fig. 1), two resistive dividers set threshold voltage levels at both the inverting and noninverting inputs of the comparator by dividing the reference voltage. The input voltage is steered to the appropriate comparator input by diodes CR1 and CR2.

When the input voltage is within the window, neither diode conducts, and the comparator is biased for a High output. When the input goes above the window, CR2 conducts and pulls the inverting input high, causing the comparator output to go Low. When the input voltage goes below the window, CR1 conducts, pulling the noninverting input low, again causing the comparator output to go Low. The source resistance of V_{in} must be low compared to the equivalent parallel resistance of each divider. That's because the conducting diode must "pull" its divider until its voltage level crosses the threshold set by the opposite divider.

The diode forward drops must be considered when setting the threshold voltages. The lowerlimit threshold voltage, VA, is set one diode drop above the required lower limit, while the upper-limit threshold, V_B, is set one diode drop below the upper limit. In this example, the reference voltage is 6.0 V and the window is selected to extend from 1 to 4 V. At low current levels, the diode about 0.5 V, so the thresholds are set to 1.5 and 3.5 V, respectively.

One typical application for the detector involves monitoring a leadacid battery (*Fig. 2a*). It indicates a fault when the battery voltage is out-





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2. ONE APPLICATION for the window detector is as a lead-acid battery monitor (a). It indicates when the battery voltage is outside an 11-to-14-V window. LEDs can be used if an op amp such as the LM324 is the comparator (b).he

side an 11-to-14-V window. Because the circuit is powered by the battey, the input and reference were switched to keep the comparator inputs within its common-mode range.

The circuit's reference is 5.0 V. The resistor values in divider R1/R2 were selected to produce 5.5 V at the inverting input when the battery voltage is 14.0 V. Divider R3/R4 is set to produce 4.5 V at the noninverting input when the battery voltage is equal to 11.0 V.

When the battery voltage is within the window, the noninverting input is more positive than the inverting input and the output LED is off. When the battery voltage falls below 11 V, the inverting input is clamped at 4.5 V by CR2, the noninverting input continues below that, the comparator output goes Low, and the LED turns on. When the battery voltage rises above 14 V, the noninverting input is clamped at 5.5 V by CR1, the inverting input continues above that, the comparator output again goes Low, and the LED turns on. Resistors R5 and R6 show that hysteresis may be added to this circuit in a conventional manner.

If an op amp like an LM324 is used as the comparator, two LEDs can be implemented (*Fig. 2b*). The green LED will turn on when the battery voltage is within the window, and the red LED turns on when the battery voltage is outside the window.

Voted "Best of Issue," Electronic Design, January 23, 1995

Single-Supply Summing Amplifier

ALEX BELOUSOV. Standard Motor Products Inc., 37-18 Northern Blvd., Long Island City, NY 11101; (718) 392-0200.

his circuit produces an output that is the absolute value of the sum of two analog input signals, V1 and V2. The circuit (*see the figure*, *a*) consists of two amplifer stages, shown within the dashed boxes, which are included in the rail-to-rail dual op amp TLC2272, used in a single-supply mode. (Other rail-to-rail op amps also can be used.)

The output of summing amplifier U1A, at terminal 3, is a high-impedance output, while the optional output amplifier, U1B, offers a lowimpedance output at terminal 4.

The equivalent circuit is shown in part b of the figure. With the assumption R1 = R2 = r, the two basic equations are:

(1) For
$$(V_1 + V_2) \ge 0$$
, the output voltage, V_{out} , is:

 $v_{out} = (v_1 + v_2)R4/(r + 2R3 + 2R4)$

(2) For
$$(V_1 + V_2) < 0$$
, then:
 $V_{out} = -(V_1 + V_2)R3/r$

$$= -(V_1 + \hat{V}_2) K$$

where $\hat{K} = R\bar{3}/r$ (the expression for standard inverting amplifier gain.)

To provide the symmetry of transfer function for both input polarities, the right-hand parts of both equations must be equal:

K = R3/r = R4/(r + 2R3 + 2R4).After simple mathematical manipulation, the equations become:

R4 = R3(1 + 2K)/(1 - 2K).

The last expression, taken with the previous assumption that

(R1=R2=r=R3/K), defines the main relationship between resistors R1 to R4, needed to assure proper operation of the summing amplifier.

Note that if K = 1/4, the resistor ratio will be as shown in the figure, part a. If we define a basic resistance as R, then the relationships between the resistors are:

R3=R; R1=R2 =4R; R4 =3R.

It is important to note that the absolute values of the resistors do not matter; the values need only be "ratio-matched." Thus, any standard low-cost resistive network will be applicable.

The output terminal 3 may be connected directly to a digital multimeter or analog-to-digital converter with high input impedance. For bet-

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MAX962	2	0.5	CMOS	No	+2.7 to +8	8	7
MAX963*	2	0.5	CMOS	Yes	+2.7 to +8	11	7
MAX964*	4	0.5	CMOS	No	+2.7 to +8	8	7

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THE ABSOLUTE VALUE of the sum of the two input voltages is developed by the first stage of this circuit (a). The second-stage amplifier provides impedance matching and additional gain. The equivalent circuits (b) are used to analyze the overall circuit.

ter impedance matching, the additional noninverting output amplifier is recommended.

The optional amplifier provides impedance matching and produces an additional gain of (1+R5/R6). If R5 is set equal to 3R6, unity gain of the whole amplifier is obtained. Consequently, the circuit returns the absolute value of the sum V_1+V_2 of the input voltages. However, all practical op amps introduce errors. In this application, the most critical dc error source is the parasitic positive voltage on pin 1 of op amp U1A when V_1+V_2 is greater than 0. In an ac mode, the input capacitance of U1 defines the frequency bandwidth.

When the values of resistors are as is shown (*see the figure*, *a*, *again*), the frequency range measured at the -3-dB points spans from dc to 20 kHz. To obtain a wider frequency range, lower resistances for R1 to R4 must be used. Also be aware of the possible nonlinear distortion, which could result from variations in the input capacitance of op amp U1 with changes in input voltage.

Voted "Best of Issue," Electronic Design, January 23, 1995

Eliminate Periodic Noise

W. STEPHEN WOODWARD, Venable Hall, CB3290, Univ. of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvxl.oit.unc.edu

he intrusion of periodic noise (for example, 60-Hz "hum") into electronic circuits seems inevitable, particularly when high-impedance, low-level signals are involved. The dominant mode of noise induction in such situations is capacitive. Because capacitive induction emphasizes high frequency noise components, 60-Hzrelated noise is likely to be heavy in harmonic content and extremely nonsinusoidal. For this reason, purely analog "notch" filters are limited

when cleaning up corrupted signals.

This analog/digital synchronousaverager circuit (*see the figure*) implements a robust "comb" filter that (theoretically) infinitely attenuates all 60-Hz harmonics. It does this independently of precision component tolerances and with a transient response ideal for use with analog/digital converters. Signal components with frequencies below 20 Hz are passed virtually undisturbed.

In the circuit, A1 continuously inte-

grates and inverts the sum of the input signal and the output of buffer amplifier A2. Depending on the state of FF2, either switches S1A and S1B (FF2 = 0) or S1C and S1D (FF2 = 1) will conduct. In the former case, the A2 buffer's input comes from the voltage stored on capacitor C3, while C2 tracks A1. In the latter case, the roles of C2/C3 are reversed.

Because flip-flop FF2 toggles once each 60-Hz cycle, A1 always integrates the difference between the instantaneous input voltage and the

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integral of the input taken over the preceding cycle.

The transfer function of such a piecewise integration is well known. It's characterized by a series of impulses that occur at f (the fundamental frequency of the integration cycle) and at all integer multiples of the frequency f.

This extreme attenuation (greater than 10,000:1 in the prototype) of harmonic noise is not limited by component tolerances.

The filter's settling time for an input step, however, does depend upon the trimming of potentiometer P1. If P1 is properly adjusted, the filter's transient response to an input step will settle to better than 1% within one or two line cycles following the input step. Otherwise, a minor overshoot or undershoot may be observed. However, even then, the filter's transient response will be supe-

ble complexity.

Optional unity-gain inverter A3 undoes the signal inversion performed by A1 and incorporates trimmer pots P2 and P3 for precise



rior, for most purposes, to that of THE "COMB" FILTER IMPLEMENTED IN THIS synchronous a linear analog filter of compara- averager infinitely attenuates all 60-Hz harmonics.

> adjustment of overall filter gain and zero offset. The signal-processing function that results is de accurate. noninverting, and virtually blind to

60-Hz related noise.

Voted "Best of Issue," Electronic Design, July 10, 1995

Low-Cost Step-Down Regulator

EUGENE E. MAYLE, R.L. Drake Co., 230 Industrial Dr., Franklin, OH 45005; (513) 746-4556.



n inexpensive and efficient discrete step-down volt-

age regulator can be built using a complementary transistor arrangement that uses both positive and negative feedback and is referenced to a Zener diode. A flyback conduction diode and a few passive components complete the circuit.

A general-purpose pnp audio output-stage transistor is chosen for Q1 (see the figure). In a common-emitter configuration, Q1 acts a "switch transistor" under the control of Q2, the "com-

Input = 18.0 V, output taken at C3							
		Rip					
Output (V)	Load (ohms)	(mV p-p)	(kHz)	Efficiency (%)			
12.54	1k	50	4	67			
12.5.2	90.9	25	112	86.5			
12.49	47.6	40	58	88.9			
12.45	24.4	70	31	91.8			
Input = 18.0	V, output taker	n at C4					
		Rip					
Output (V)	Load (ohms)	(mV p-p)	(kHz)	Efficiency (%)			
12.53	1 k	58	0.8	67			
12.46	90.9	1.5		86.5			
12.37	47.6	1.5		88.4			
12.20	24.4	1.5		90.4			
Output taken at C3, load = 24.4 ohms							
		Rip					
Input (V)	Output (V)	(mV p-p)	(kHz)	Efficiency (%)			
15.0	12.35	73	17.8	93.4			
18.0	12.45	70	31.0	91.8			
21.0	12.53	75	43.3	90.8			

parator transistor." The value of R2 is chosen low enough to quickly discharge the parasitics of Q1 during turn-off, ensuring fast switching. R5 is a precautionary element included as base current-limiting a mechanism for Q1. Q2, a general-purpose npn transistor, operates as a common-emitter in its positivefeedback mode and as a common-base amp in its negative-feedback mode. After initialization of power, bias resistor R1 provides base current to turn on Q2, which turns on Q1. This results in additional bias current flow

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through network R3, R4, and C2. Thus, a positivefeedback loop is formed. Q1 and Q2 output currents ramp the voltage across C3. Zener diode CR2 eventually clamps the voltage at Q2's base while its emitter voltage at C3 continues to rise. Once Q2's Vbe drop becomes sufficiently small, Q2 turns off Q1, completing the negative-feedback loop.

The back EMF generated by L1 forces Q1's collector negative, at which point it's clamped by Schottky diode CR1. The polarity of network R3, R4, and C2 becomes reversed and shunts current away from Regulation involves charging C3 through L1, and the



Q2's base, enhancing the THIS inexpensive and efficient discrete step-down turn-off. A regulated bias regulator is based on a complementary transistor point now is established at arrangement that employs both positive and negative $Q2\ensuremath{\text{'s}}$ emitter and across C3. feedback and is referenced to a Zener diode.

there's insufficient current draw

decay of C3 through the load. If | put to stabilize at about 0.7 V high. At light loads, charging time is from the load, R3 will cause the out- almost load independent while

decay is directly dependent. Overshoot can occur fixed due to circuitresponse delays and ripple frequency will be low.

At higher loads, the charge-to-decay-time ratio approaches 1:1, the ripple voltage approaches a minimum, and the oscillation frequency peaks. Still heavier loads require that L1 supply load current while charging C3, which increases the entire cycle--ripple frequency goes down and ripple voltage goes up.

Inductor L1 is selected to maintain the switching frequency above the audible range for the intended operating load. The output filter L2 and C4 reduces ripple to less than 10 mV p-p over a large range of loads, with only a slight decrease in efficiency.

Voted "Best of Issue," Electronic Design, February 6, 1995

Positive Feedback Terminates Cables

JERRY STEELE. National Semiconductor Corp., Tucson Design Center, 940 Finance Center Dr., Suite 120, Tucson, AZ 85710; (602) 751-2380.

ositive feedback along with a series output resistor can provide a controlled output impedance from an op-amp circuit, with lower losses than would result from using an actual resistor. The circuit is useful occur when driving coaxial cables that must be terminated at each end in their characteristic impedance, which is often 50 Ω . Adding a 50- Ω series resistor on the op amp's output obviously reduces the available signal swing.

As can be seen in Figure 1, the circuit is an adaptation of the Improved Howland Current Pump, which is usually designed to maximize output impedance. It uses the positive feedback to provide a multiplication of the current sense resistor's value. For example, with R1 = R2 = R3 = 1 Ω , and R4 = 1.2 Ω s, the circuit supplies a 50- Ω output impedance with only 5 Ω of real resistance to lose voltage swing through.



1. COUPLING positive feedback with a series output resistor provides a controlled output impedance from an op-amp circuit, reducing losses that would otherwise occur with an actual resistor. The circuit is an adaptation of the Improved Howland Current Pump.

Adding positive feedback has the effect of multiplying circuit gain by the same ratio as it multiplies the sensing resistor (the example values given had a gain of about 10). Keep in mind that loading will cause the output voltage to drop to half (that's proof of the concept), so the loaded gain is half the unloaded gain. Available voltage swing remains essentially unimpaired. This can be a valuable feature, especially in lowvoltage circuits like those used with National Semiconductor's LM7131. This part can provide 4-V pulses into a 150- Ω cable on 5-V supplies, but back termination would typically halve that. This technique maintains the full 4-V capability.

The circuit tolerates capacitive loads well, better than just the op amp alone. The inductive portion of any load is what could cause stability



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problems. Note that coax cable is a transmission line and isn't considered purely inductive or capacitive. Load inductance will manifest itself as overshoot in pulse response, if the overshoot is less than 40% of the total peak-to-peak amplitude of the pulse then the circuit has adequate phase margin.

Setting the desired gain involves pegging the values of the negative feedback resistors. Remember that the gain will ultimately be multiplied by an amount equal to what the series output resistor R5 is being multiplied. For convenience, the input leg of the positive feedback (R3) can be set equal to R1. The following equations solves for R4:

$$R_4 = \frac{\left(\frac{A_{ol}}{1 + A_{ol}[R1/(R1 + R2)]}\right) \cdot R_3}{1 - \frac{R_5}{Z}}$$

where Z is the desired output



2. THE VALUE OF THE TECHNIQUE demonstrated in Figure 1 is shown in this application, which uses National Semiconductor's LM7131 in a battery-operated piece of portable equipment operating at 3 V.

impedance. A_{ol} is the open-loop gain of the op amp.

An example demonstrates the value of this technique (*Fig. 2*). A1 is National's LM7131 in a batteryoperated portable device operating at 3 V. At the 3-V supply, the LM7131 is specified for a maximum swing of 2 V. Using positive feed-

back for back termination makes this entire voltage swing available. At the receiving end, another LM7131 provides gain to present a 0-to-4-V input to a high-speed 12-bit ADC.

Voted "Best of Issue," Electronic Design, March 6, 1995



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Charger Built With Few Parts

JOSEPH J. DENGEL, U.S. Merchant Marine Academy, Engineering Dept., Kings Point, NY 11204.

battery charger for small NiCd batteries, which can be constructed using just four components, comes in handy as a lightweight and compact travel charger or in "floating" simple battery-backed projects. The circuit sacrifices isolation from the power line for a compact design. This lack of isolation requires the user to exercise prudence in the circuit's use, heed the notes mentioned below and ensure that circuit operation and the potential shock hazards are understood. As a travel charger for AA, C, or 9-V batteries, the circuit will usually fit inside a 35-mm film canister. A short ac plug comes out of one end and two small clip-leads from the other.

In the circuit (see the figure), the capacitor is ac rated at 120 V ac with a value determined from the equation below. The fuse is selected to match the designed charging current/line voltage, and should not be above 0.25 A. The diode D1 rectifies the line voltage and diode D2 provides a discharge path for the capacitor, which bypasses the battery. D2 is a Zener diode that limits the opencircuit voltage between the two charging leads when there's no load present.

Battery charging is based on average current flow. After selecting a desired charging current in amperes, the value of the capacitor



BUILT WITH JUST FOUR COMPONENTS, this charger for small NiCd batteries is useful as a compact travel charger or in "floating" simple battery-backed projects. It's small enough to fit in a 35-mm film canister.

(in farads) is computed from the equation:

C = $(I_{avg} \times 0.0167)/340$ (1) For example, AA NiCd batteries usually have a 0.5 amp-hr rating and an overnight charge rate of 10% as a rule of thumb. Charging current of 0.05 A results in a 2.5- μ F capacitor.

Some other notes about the circuit: 1. The negative charging lead should be connected to the neutral conductor (wide blade on a polarized plug). Hotel wiring often is incorrect, so keep both charging leads, the batteries, the appliance, and yourself clear from external ground paths.

2. The charging leads may be shortcircuited without damage and any reasonable number of batteries can

```
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1.7MEG; EFFECTIVE LOSS COMPONENT FOR CAPACITOR
VAC
         1.0
R1
         1,2
         2,3
RC1
                  DIN5245; VOLTAGE-LIMITING DIODE, 15V, 0.5 WATTS
DIN4007; BLOCKING DIODE
.25;INTERNAL RESISTANCE OF BATTERY, "AA" CELL
DC 1.2 AC 0.0 ; SINGLE CELL BATTERY
         0,3
D1
D2
R2
         4,5
V1
          5.0
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*R3
         4.0
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Tt=5.7u)
. PROBE
END
```

be charged in series without affecting the average charging current. When not in use, the circuit should be unplugged.

3. The Zener-diode voltage rating should be set slightly above the highest voltage for the battery array. Its wattage rating can be approximated by:

 $P_d = I_{avg} \times V_z$ (2)

4.The Zener diode is the only component that may dissipate any power; it should be liberally sized, especially if the final circuit will be completely enclosed.

5.Batteries may be charged while still installed in the tape player or radio (convenient because a separate battery holder isn't required). Use caution to prevent an open circuit in the battery path, or else the charging voltage will pulse at a value determined by the Zener. This may not be beneficial for the appliance if it's turned on or is in an "idle mode."

6.A four-diode, full-bridge rectifier may be used in place of diode D1. This reduces capacitor size by onehalf for any given charging current. The zener diode will dissipate twice the calculated power and should be placed at the output of the bridge.

Voted "Best of Issue," Electronic Design, December 4, 1995

Measure Temp Through Printer Port

YONGPING XIA, 23008 Arlington Ave., Torrance, CA 90501; (310) 784-1442.



single-chip digital thermometer IC developed by Dallas Semiconductor,

Dallas, Texas—the DS1620—can measure temperature from -55 to +125°C in 0.5°C increments.

The circuit shown uses a PC's printer port to communicate with a DS1620 (see the figure).

The C program (see the listing) will set the printer port to power the IC, send control commands to and read measured data from the IC, convert the data to temperature, and display it on screen.

Voted "Best of Issue," Electronic Design, March 18, 1996



TEMPERATURE CAN BE

measured and displayed on a PC screen using this circuit. It utilizes a PC's printer port to communicate with a single-chip digital thermometer IC (DS1620).

<pre>#include <stdlib.h> #include <stdio.h> #include <conio.h> #include <dos.h></dos.h></conio.h></stdio.h></stdlib.h></pre>	
<pre>#define POWER_ON #define POWER_OFF #define CLK_ON #define CLK_OFF #define RESET_ON #define RESET_OFF #define OUT_HIGH #define OUT_LOW</pre>	0x01 0xfe 0x20 0xdf 0xbf 0x40 0x80 0x7f
<pre>typedef unsigned int int i, data, out_po char msg[80];</pre>	<pre>WORD; rt, in_port, out=0;</pre>
<pre>/* find printer port void find_port(void) { out_port=*(WORD fa: in_port=out_port+1 out !=POWER_ON; outportb (out_port delay(1000); }</pre>	<pre>address */ r *)MK_FP(0x0040,8); ; , out); /* power on *</pre>
<pre>/* send control commu void ssend_control(ir { int control; control=control_dat for (i=0; i<8; i++</pre>	and to DS1620 */ nt control_data) :a;)
out&=CLK_OFF; outportb(out_po	rt, out);

delay(5); out 1 =RESET_OFF; outportb(out_port, out); delay(5);

/* read data from DS1620 */
int read_chip(void)
{
 int in, temp;

```
rst();
send_control(0x0c);
send_control(0x03);
rst();
send_control(0xee);
send_control(0x00);
rst();
send_control(0xaa);
out (=OUT_HIGH;
outportb(out_port, out);
```

```
for (i=0; i<9; i++)
{
    out&=CLK_OFF;
    outportb(out_port, out);
    delay(5);
    temp=inportb(in_port);
    in=in+(((temp/64)&0x01)<<i);
    out |=CLK_ON;
    outportb(out_port, out);
    delay(5);
}</pre>
```

return(in);

main()

in=0.

```
int temp1;
float tempC;
clrscr();
gotoxy(50,24);
printf("Hit any key to quit");
find_port();
do {
    temp1=read_chip();
    if (temp1..256)
    temp1==512;
    tempC=((float)temp1/2);
    gotoxy(1,1);
    gotoxy(1,1);
    delay(1000);
    } while (!kbhit()); /* quit if any key *
```



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s Window	CALC.EP	J - CALC.SCH					-
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imple RS-232 Tester

RIAN-NICOLAE ION, Noesis-Domaine Technologique de Saclay, Bat. Ariane 4, rue Rene Razel, 91892 Orsay Cedex, France.

ne problem in transferring data using the RS-232 standard is whether the TxD and RxD cables should be cross-coupled. It's easy to determine this when a DMM is available, but it might be difficult to do in the field when there's no meter at hand.

A simple solution handles this task easily, in a small package that could be carried in a pocket (*Fig.* 1). The tester is basically a window comrator, in which the Low and High

vels are set at +3.0 V and -3.0 V, spectively, by resistors R2, R3, d R4. Resistor R1, when not drin by an RS-232 output, will have a low voltage across it (approximately 0 V), and the LED D1 at the output of the comparators is turned off.

If the unknown wire of the cable that's tested is an RS-232 output, then it will drive the In point to either a voltage between +3 and +12V or between -3 and -12 V. In both cases, one of the two comparators' outputs will be driven low. This turns the LED on, indicating the presence of a wire connected to an RS-232 output. The comparator should be an LM339 type or equivalent (with an open-collector output).

The disadvantage of this scheme is that the thresholds are very sensitive to the supply variations. To eliminate that, the thresholds at the inputs of the comparators can be created using the normal forward drop on a simple diode (a Zener with such a low voltage would be more expensive and difficult to find), and then be brought to the necessary levels by IC1 (+3 V at its output) and IC2 (a simple inverter) (*Fig. 2*).

To minimize parts count, a quad op amp could be used for IC1-4, one that can assure a V_{OH} level high enough to turn off LED D2.

Voted "Best of Issue," Electronic Design, Februay 19, 1996



1. THIS PEN-SIZED device can easily handle the task of determining whether TxD and RxD cables should be cross-coupled when transferring data using the RS-232 standard.



2. THRESHOLDS often are sensitive to supply variations. In this setup, thresholds are created using a diode's forward drop and then brought to the necessary levels by IC1 and IC2.

Build An Accurate Log Amp

MOSHE GERSTENHABER and Frank J. CIARLONE, Analog Devices Inc. Two Technology Way, Norwood, MA 02602; (617) 329-1241.

ogarithmic amplifiers are used in application in which the input possesses wide dynamic range, and there's a ed to resolve signal throughout its ge.

conventional logarithmic amplifi-(Fig. 1a) consists of an amplifer and nonlinear element in its feedback, a reference circuit, and one specialized component to remove

CALCULATED, ACTUAL AND ERROR OF THE LOGARITHMIC AMPLIFIER						
VIN	Vout (Calculated)	V OUT (Measured)	Error/FS			
+10 V	1.985	1.990 V	0.05%			
+1 V	0 V	.0030 V	0.03%			
+100 mV	-1.985	-1.99 V	0.05%			
+10 mV	-3.97	-3.97 V	0%			
+1 mV	-5.954	–5.93 V	0.24%			
+100 muV	-7.94	-7.96	0.20%			

BEST IDEAS FOR DESIGN Ideas voted "Best Of Issue" by the readers of Electronic Design

temperature effects. Although such circuits are rather common, they have some limitations. For example, the input must be referenced to ground because common-mode signals will generate errors in the "logging" device, and the input signal's source impedance must be small so that there's no interaction with the input resistance of the logarithmic amp. Moreover, the system bandwidth changes as the signal changes because the nonlinear device alters the loop bandwidth as the current through it is varied.

By modifying the logarithmicamplifier circuit, it can reject common-mode voltages and only measure differential signals. Its bandwidth is independent of the input voltage andits input impedance is very high. The log circuit consists of an instrumentation amp, and an op amp together with a diode-connected transistor that produces a voltage proportional to the logarithm of the current.

A circuit consisting of a voltage reference, an instrumentation amp, and an op amp together with a diode-connected transistor act as a reference circuit. A thermometer IC, a fixed-gain instru-



circuit. A ther- 2. THIS CROSS PLOT of Vout versus Vin mometer IC, a demonstrates the circuit transfer function. The horizonta fixed-gain instru- scale = Vin 2V/div; Vertical = Vo 1V/div.



1. UNLIKE THE CONVENTIONAL LOGARITHMIC amplifier (a), a more accurate amp can be built to reject common-mode voltages (b). The modified amp consists of an instrumentation amp and an op amp configured as a voltage-to-frequiency converter.

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mentation amp, and a divider circuit provide the necessary temperature compensation and scaling for a transfer function:

 $V_{out} = 1.985 \log 10(V_{in}/1 \text{ V})$ V_{REF} must be set to 1.000 V and,

with Vin = V_{REF} , the grain adjust has to be set so that Vo = 0 V. Calibration at low input voltage is done by changing buffer A4's offset voltage. The table illustrates the calculated, actual, and error of the loga-

rithmic amp in Fig. 1b. Figure 2 shows a cross plot demonstrating the circuit transfer function.

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Creating a Good, Stable Sine Wave

ARTHUR D. DELAGRANGE. 437 W. Watersville Rd., Mt. Airy, MD 21771; (301) 829-2430.

classic problem in electronics is the generation of a good, stable sine wave. There are a thousand ways to do it; none of which are perfect. So here's number 1001, which offers some advantages...

Semi-digital circuits (e.g., crystal oscillators and dividers) can create square waves of very stable amplitude and frequency. Although a square wave often is considered as a sine wave having 100% distortion,

this is far from true. The "error" consists entirely of odd-frequency harmonics if the duty cycle is exactly 50% (this can be guaranteed by generating twice the desired frequency and dividing by two).

Removing the odd harmonics is a reasonable task for a filter. The obvious solution, a narrowband filter, isn't acceptable because analog types are notorious for poor stability. Digital and semi-digital (e.g., switched capacitor) are better in this respect, but they add their own noise and harmonics.

Such a task can be accomplished using the filter shown in Fig. 1. Without R1 and R2, it's an active version of a 5-pole passive lowpass L-C ladder. This type has excellent amplitude stability in the passband, 30dB/octave slope outside the passband, low component sensitivity, and a capacitor to ground at the output, which ensures continuous high-frequency roll-off and minimizes stray noise pickup. The rejection would be inadequate at the third and fifth harmonics, but notches at these frequencies can be created with just two more resistors, R1 and R2. This turns the device into an elliptic-like filter (this isn't a true elliptic, because when the zeros are assigned arbitrarily, the humps in the reject band won't be equal).

At first glance, the filter appears complicated, but a closer inspection shows that it can be built with as



to ground at the output, **1. USING AN ELLIPTIC-LIKE FILTER**, which ensures continuous this circuit can remove odd harmonics from a square

which ensures continuous this circuit can remove odd harmonics from a square high-frequency roll-off and wave, creating a stable sine wave. The seemingly comminimizes stray noise pick- plex filter actually can be built with as few as six parts.

few as six components. How so? The op amps can be a quad DIP. RA can be two RB resistors in parallel. RC can be equal to RB. R3 can be leftover RB resistors in series. Consequently, all of the resistors other than R1 and R2 can be in two DIPs.

Performance results are shown in Figs. 2 and 3. Fig. 2 shows the filter frequency response, and Fig. 3 illustrates the output spectrum when using a 1-kHz square-wave input.

Note that all harmonics are in excess of 80 dB down (this performance was achieved using 1% film capacitors; a DIP of matched ceramics, which are more lossy, yields 70 dB rejection of harmonics).

Some notes on the filter: No 1% tolerances are necessary if matched components are used and R1 and R2 are tweaked to adjust the notch frequencies (this is easily done by adjusting R1 for minimum signal out at the third and R2 for the fifth). Because the filter is passive-derived, it must be lightly loaded. However, if the load provides dc continuity to ground, R3 may be eliminated.

Similarly, if the driving impedance isn't small compared to the resistors in the filter, its impedance may be subtracted from the filter input resistor to compensate. The op amps are part of tuned circuits and should have a gainbandwidth product of at least 100 times the notch frequency (when the filter

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was changed for a 10-kHz input by reducing the the capacitor values to 1000 pF, harmonic rejection dropped to 66 dB). At much higher frequencies, the passive version might be better.

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2.FREQUENCY-RESPONSE RESULTS FOR THE filter in Fig. 1 are illustrated. The filter is essentially flat within the passband and rolls

off at about 30 dB/octave. Note the notches at the third and fifth harmonics.



3. THE FILTER'S OUTPUT SPECTRUM, using a 1-kHz squarewave input, shows that all harmonics are in excess of 80 dB down.

Convert Pulse Width To Analog

W. STEPHEN WOODWARD. Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvxl.oit.unc.edu.

nstruments possessing an internal digital architecture are sometimes required to produce an analog output. Often, these requirements are introduced very late in the product-development cycle (thanks a lot, marketing!), when it may be difficult to provide board space and addressing logic for a conventional DAC.

The circuit shown arose from just such a scenario, which involved a small microprocessor-based (Z-80) product that needed a greater than 15-bit resolution 0-to-5-V analog output grafted on.

The product had few assets free for the control of even a serial-input DAC. What was available, however, was much idle processor time unneeded for the 500-ms measurement cycle, exactly one uncommitted output bit, and some unoccupied capacity in the system ROM.

It was, therefore, apparent that design modifications could be introduced. Such alterations would generate, twice per second as part of the measurement cycle, a softwareloop-timed pulse with duration ranging from 3 to 363 ms that would be proportional to the measured quantity. Pulse duration would be $7.26 \mu s$ or one part in 50,000.

This circuit (see the figure) converts these pulses to a monotonic analog 0-to-5-V output with $100-\mu V$ resolution that settles to better than 1% only 1 cycle after a change in



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SOFTWARE-LOOP-TIMED PULSES ARE converted to a 0-to-5-V analog output that settles to better than 1% only one cycle after a change in pulse duration. The pulses have a duration ranging from 3 to 363 ms.

pulse duration.

During the interval between output pulses, the CD4053B CMOS Lswitches are in the state illustrated. S1 is closed, S2 is holding C1 reset, and S3 connects C2 to A2's summing point. At the start of an output pulse, switch S1 releases one end of R2. This causes the noninverting input of A1 to drop about 4 mV negative. The exact amplitude of this step is adjusted by potentiometer P1 so that a pulse width of the minimum 3 ms produces a zero output.

While this is happening, switch S2 begins the charge of capacitor C1 through R1. The rate of this charging is adjusted so that a pulse with the maximum duration of 363 ms produces a 5-V output.

Simultaneously, S3 connects the right-hand end of C2 to A2's output. As a result, at the end of the integration cycle, the left-hand terminal of C2 will be at A2's output voltage. The minimum input pulse duration is set to 3 ms, rather than zero, so that C2 always has sufficient time to equilibrate to this differential.

Therefore, at the end of the integration cycle, when switch S3 returns to the idle state and connects C2 to A2's summing point, a charge equal to C2 times the voltage difference between A1 and A2's outputs will be delivered to C3. This charge transfer occurs as S2 returns to the idle state and resets C1, pulling the left-hand terminal of C2 back to the idling voltage.

The result is that if C2 = C3, A2's output will slew exactly by the difference between the output value from the previous measurement cycle to the one appropriate for the new cycle. If this equality isn't exact, one or two cycles may be required for precise settling.

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Programmable Noise Generator

FRANK N. VITALJIC. 514-13th St., Bellingham, WA 98225.

he noise voltage (en) generator shown is able to generate uniform or Gaussian noise (see the figure). The noise is multiplied by (K), resulting in a noise power of $K^2\sigma_n^2$ volts² at the filter's input. This power is available at the filter's output by setting the bandwidth fully open (i.e., FL = 0, FH = 0.5 Hz).

The 127-tap linear phase filter passes frequencies between F1 and F2, thus bandlimiting the filter output noise (e_{out}). The output is sampled at a rate of Fs Hz, and stored as 500 samples in the *noise_data* array (*see listing for noise_generator() program*). The output noise power is approximately:

 $\sigma_{out} \ge 2 \approx 2 [(F2 - F1)/Fs] K^2 \sigma_n^2 volts^2$

The statistics of the output data (mean, variance, min, max) are stored in the *stats* array. The output noise power can be set as desired by adjusting (K) accordingly.



THIS PROGRAMMABLE

noise voltage generator is capable of producing uniform, or Gaussian, noise. The output noise power can be set as desired by adjusting (K).

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```
#include<stdlib.h> //PROGRAMMABLE BAND-LIMITED DIGITAL
 #include<math.h>
                                                                              NOISE GENERATOR PROGRAM
 void noise_generator(int noise_type,
                                                                                                                              //O=uniform, 1=Gaussian
                                                                          int seed, //Seed for srand()function
double FL, //Low band-edge | normalized
double FH, //High band-edge | F/Fs $ 0.5
double noise_mul, //Noise multiplier
double*noise_data, //500 data points
double*stats) //Array of mean, variance
//min, max noise data,
                                                                                                                                                                                               variance,
 resp
//Generates 500 data points of user programmable band-limited noise //Requires the function calc_coeffs()published in ELECTRONIC DESIGN, June 26, 1995, p. 104.
        double filter_coeffs[MAXLEN],*data_ptr,*coef_ptr,*p, *q;
double data_in[626],*out_ptr, gaus[2], acum;
        int i. i:
 //Calculate noise filter coefficients
    calc_coeffs(BPF, MAXLEN, DUAL, FL, FH, filter_coeffs);
 //Duplicate symmetrical coefficients in upper-half of array
                     p = filter_coeffs; q = &filter_coeffs[126];
for(i = 0; i < 63; i++)*q- = *p++;</pre>
 //Generate broad-band noise data for filter input
srand(seed); //Initialize rand()function sequence
       share of the state of the 
                               gaussian(gaus);
*p++ = noise_mul * gaus[0]; *p++ = noise_mul * gaus[1];
       3
   /Input broad-band noise to filter and store band-limited noise
      /Input broad-band noise to filter and store band-limited no
/in array noise_data, 500 points.
out_ptr = noise_data;
for(i = MAXLEN-1; i < 626; i++) {
    data_ptr = &data_ir[i];
    coef_ptr = filter_coeffs;
    acum = (*coef_ptr++) * (*data_ptr-);
    for(j = 1; j < MAXLEN; j++) acum += (*coef_ptr++) *
/data_ptr_b;
 *data_ptr-);
*out_ptr++ = acum;
//Calculate min/max noise data
stats[2] = stats[3] = noise_data[0];
for(i = 1; i < 500; i++) {
    if(noise_data[i] < stats[2]) stats[2] = noise_data[i]; //min
    if(noise_data[i] > stats[3]) stats[3] = noise_data[i]; //max
 //Calculate mean/variance noise data
      stats[0] = stats[0] / 500.0; //mean
stats[1] = stats[1] / 500.0 - stats[0] * stats[0]; //variance
    //end noise_generator()
double uniform(void)
//Generate zero mean uniform random number, -0.5 to 0.5
{ return ((double)(rand() & RAND_MAX)/RAND_MAX - 0.5);
void gaussian(double *gp)
 //Generate zero mean unit variance Gaussian random number pair
        double x,
     Generate pair of random numbers, Box-Muller Transform
       do (
                       x = 2.0 * uniform(); y = 2.0 * uniform();
/ A = 2.0 = unit(); y = 2.0 = unit();
r x*x + y*y;
} while((r > 1.0) || (r == 0.0));
//Map x and y to gaussian random number pair
a = sqrt(-2.0 * log(r) / r);
*gp++ = x * a; *gp = y * a;
  3
```
Active Filter Uses Equal Value Parts

MICHAEL A. WYATT, Honeywell Inc., 13350 U.S. Hwy. 19, Clearwater, FL 34624; (813) 539-5653; fax (813) 539-2558.

qual-value components can be quite an advantage in filter designs when considering the total costs associated with the procurement, stocking, and assembly of the filter.

For instance, the Butterworth active third-order low-pass filter (*Fig. 1a, middle*) uses equal value resistors and capacitors. This feature normalizes the filter's 3-dB corner frequency to 1/RC (in radians) for both low-pass and high-pass designs (*Fig. 2a*).

The two additional op amps for the normalized filter may cost less than the unequal value components in the traditional Sallen-Key filter (quad op amps don't cost much more than single op amps), especially if the application calls for precision components (see Fig. 1a, again)

PSpice's (MicroSim Corp., Irvine, Calif.) behavioral modeling capability allows for the comparison of the normalized and Sallen-Key thirdorder filters to an ideal filter.

The Laplace behavioral voltagecontrolled voltage source ``EIdeal'' (*Fig. 1a, top*) is configured as an ideal Butterworth low-pass filter with a 1-kHz bandwidth ($\omega_c =$ 6283.19 radians/s).

The Laplace transfer function (entered as symbol attribute of Eldeal) for the third-order Butterworth low-pass filter is as follows:

$$\text{'I'(s)} = \frac{1}{\left[(s^3 / \omega_c^3) + 2 (s^2 / \omega_c^2) + 2 (s / \omega_c) + 1 \right] }$$

The graphs in Fig. 1b are plots of the ideal, normalized, and Sallen-Key low-pass filter frequencydomain magnitude and error responses.

Note how both the normalized and Sallen-Key filters follow the ideal response well into the stopband. The error plots were created by plotting the difference between the responses of the real filter and the ideal filter.

The plots indicate that the nor-

malized filter achieves performance results that are equal to those of the Sallen-Key low-pass filter.

Interchanging the resistors and capacitors transforms the normalized low-pass filter into a high-pass filter with the same corner frequency (*Fig. 2a*).

This concept is illustrated with an

ideal Butterworth high-pass filter transfer function (EIdeal):

$$T(s) = \frac{s^2 / \omega_c^2}{\left[(s^2 / \omega_c^2) + 2 (s^2 / \omega_c^2) + 2 (s / \omega_c) + 1\right]}$$

Notice that the Sallen-Key filter must be modified according to impedance levels at each node. This yields a filter with equal-value



1. USING EQUAL-VALUE components in a third-order Butterworth lowpass filter design (a), will lead to lower total costs when procuring, stocking, and assembling the filters. Plots of the ideal, normalized, and Sallen-Key lowpass filter amplitude and error responses show that the normalized and Sallen-Key filters follow the ideal response well into the stopband (b).

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capacitors and unequal-value resistors, an improvement over the traditional low-pass design of equalvalue resistors and unequal-value capacitors.

The graphs in Fig. 2b indicate that the normalized high-pass filter com-

pares favorably with the Sallen-Key filter in high-pass applications, much like the previously mentioned low-pass case.

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2. A HIGH-PASS THIRD-ORDER Butterworth filter with equal-value components can also be built (a). The normalized filter once again compares favorably with the Sallen-Key in high-pass applications (b).

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