SUPPLEMENT TO

ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

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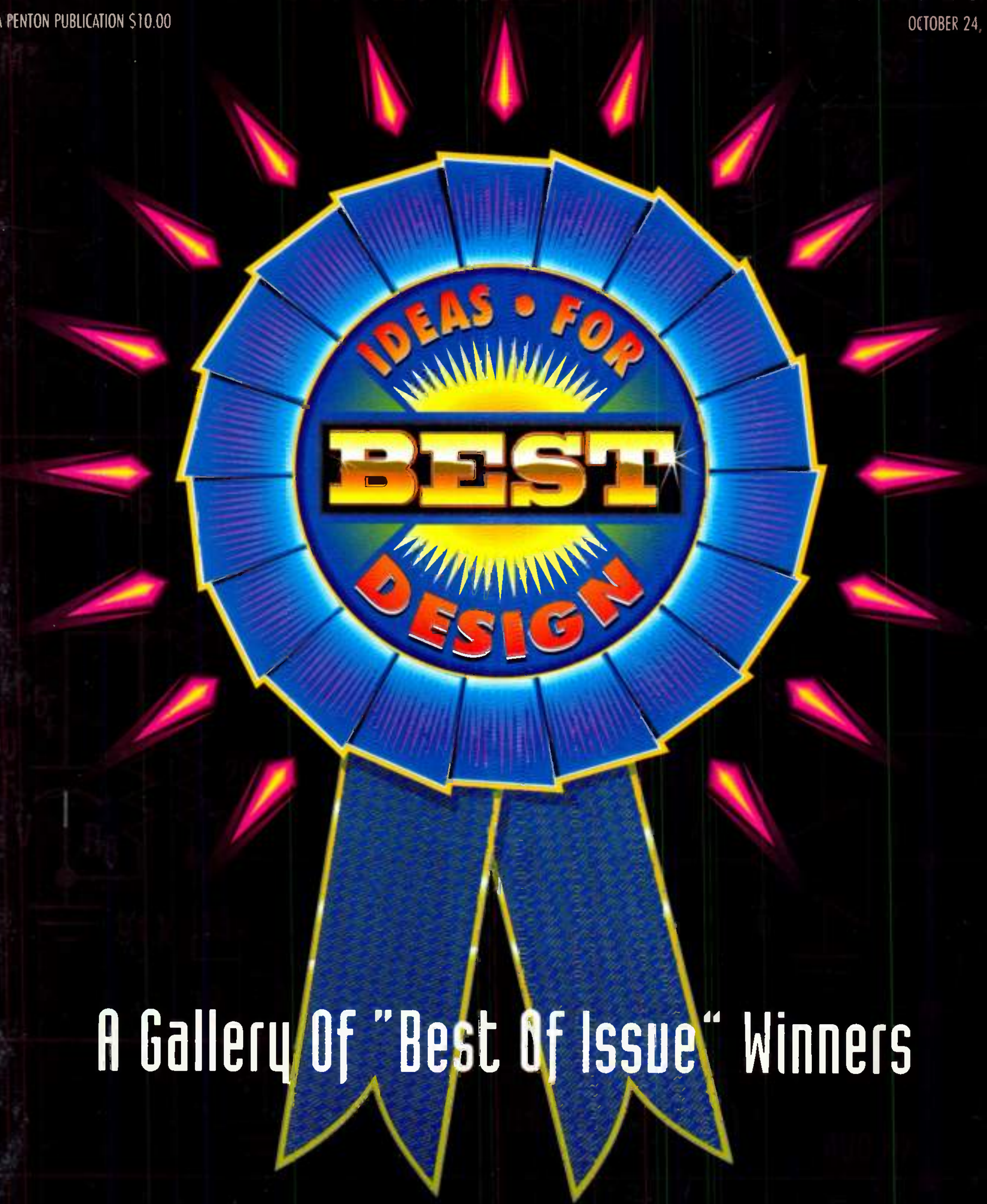

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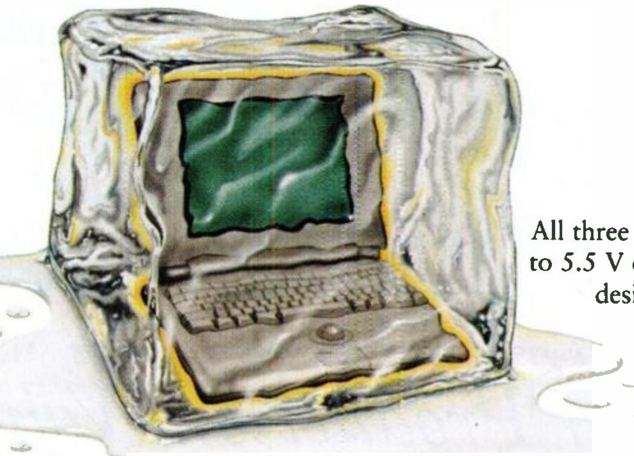

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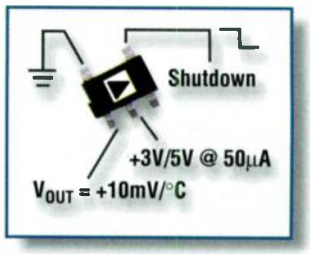

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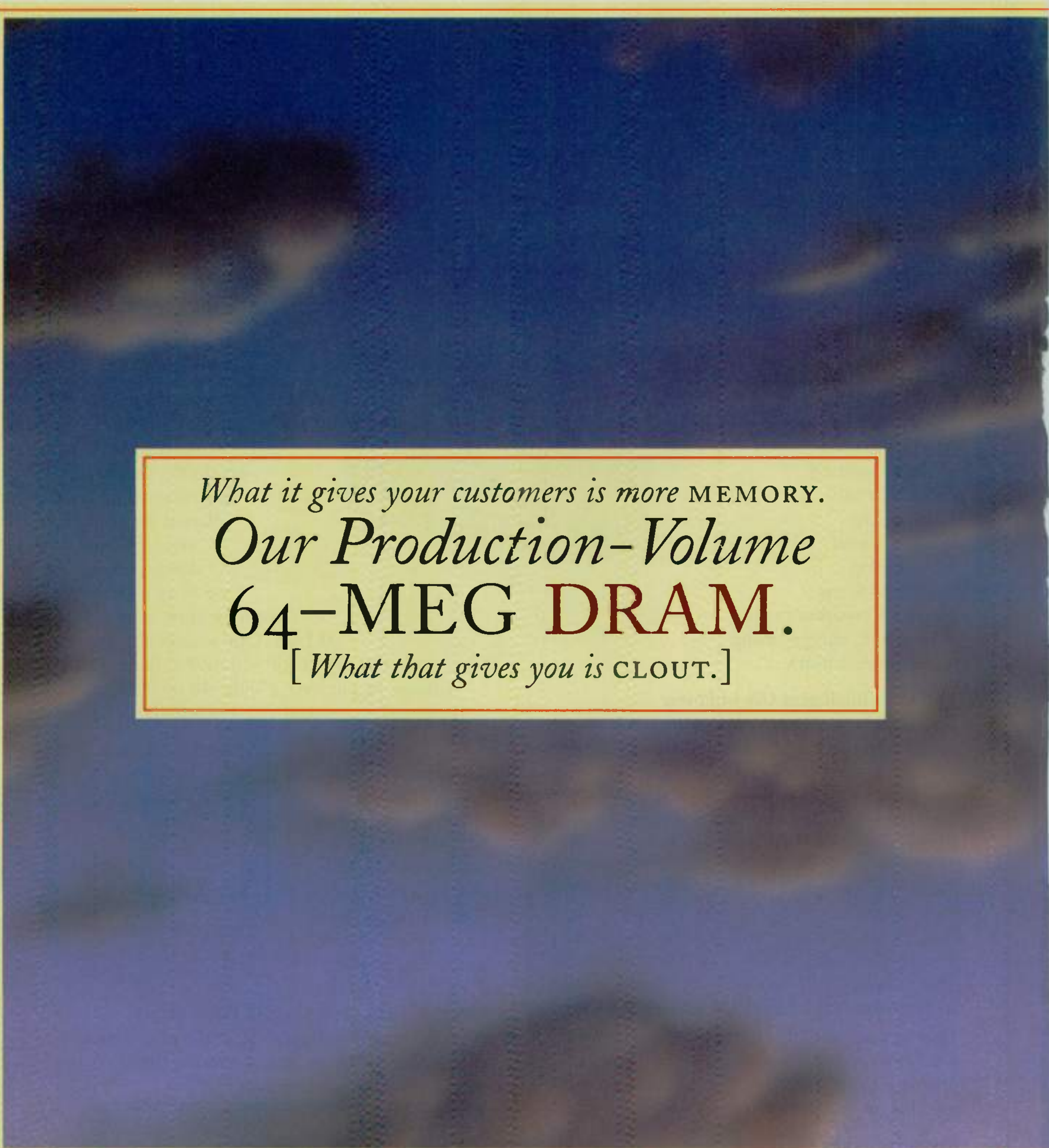

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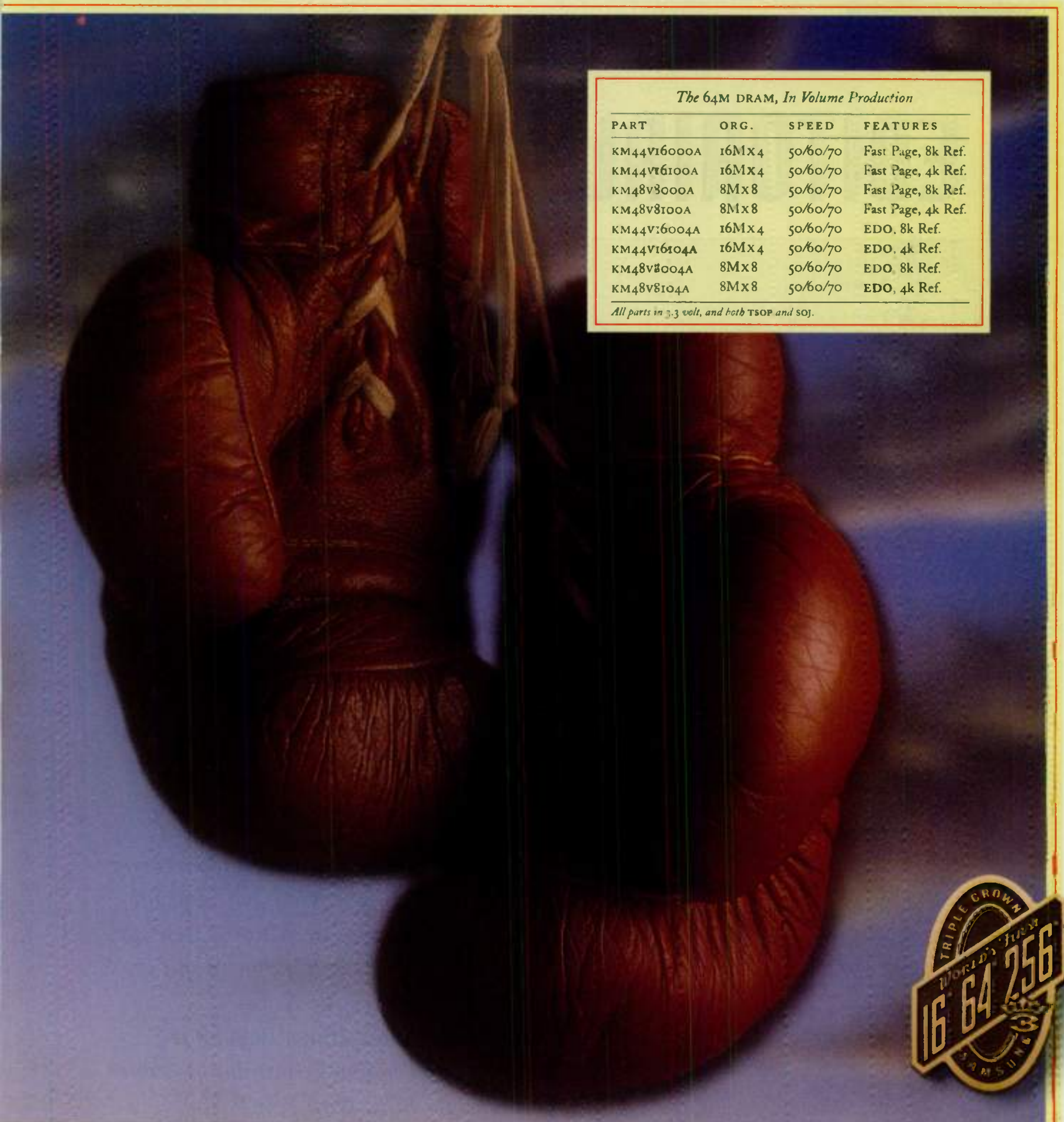

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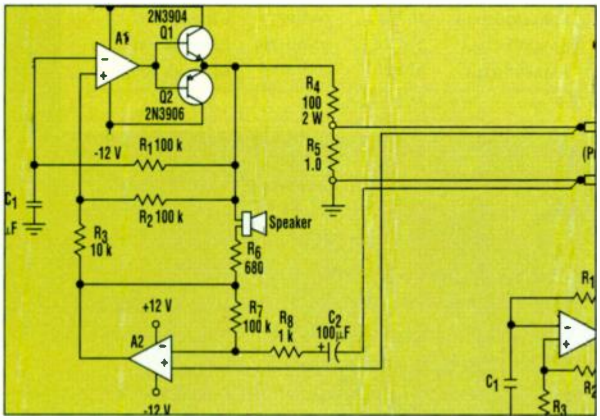

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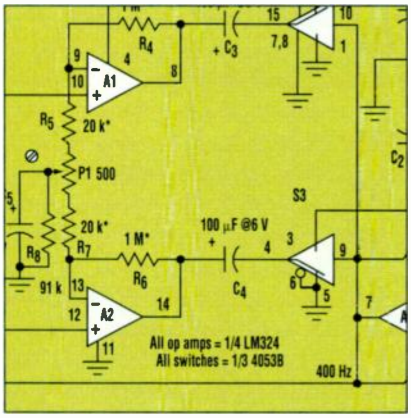

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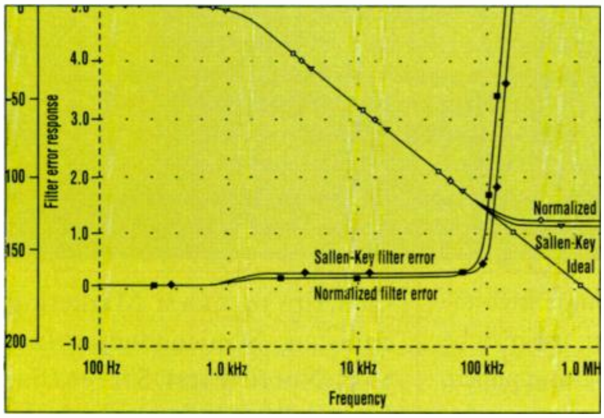

71

Think Analog Arrays

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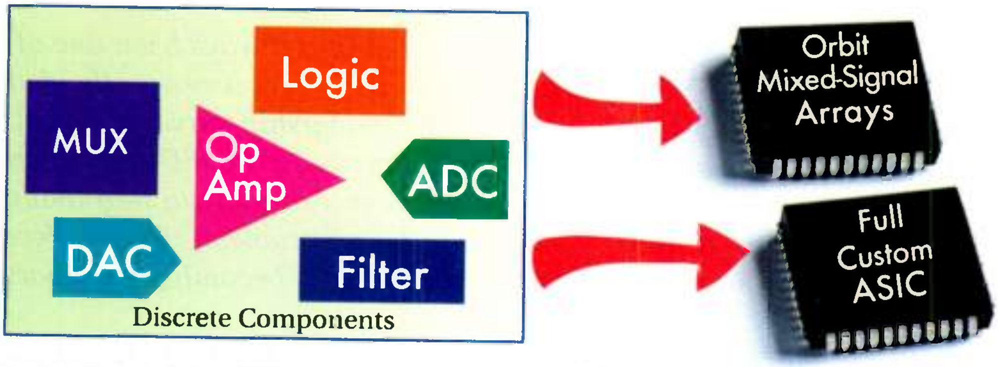

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INTRODUCTION

Since its inception, the Ideas for Design section has always been one of the best-read sections of Electronic Design. In recent years, it has consistently vied with Pease Porridge for the top spot in our periodic readership surveys. Perhaps it's the unpredictability of each section that draws readers—In the IFD section, as it's known here in the office, you never know when you're going to find that circuit you've been looking for to solve a particular design problem; And, in Pease Porridge, the creative unpredictability of Bob Pease is becoming legendary in the industry.

A little history: Ideas for Design as we know it today began in Electronic Design in March 1961, although the section title itself dates back to 1954, when it was used to designate a single, particularly useful article. In 1961, probably with more ideas coming in from readers than could ever be published one to an issue, the editors decided to publish several ideas in each issue and allow readers to vote for the one idea that they considered the most useful. At that time, no other electronics trade publication had a similar section.

Since then, we've probably published more than 4000 ideas (it's difficult to estimate, but we could figure on about 125 ideas a year for 35 years). We have often been asked why we haven't collected the ideas into a book. Actually, we have done so in the past—I have on my bookshelf right now the office copies of Volumes 3 and 4 of "400 Ideas for Design" published by Hayden Book Co. in 1976 and 1980, respectively. Volume 1 was published in 1964, and Volume 2 in 1971 (our office copies of those earlier volumes took a walk a long time ago.) Today, we have our CD-ROMs covering the complete contents of Electronic Design from 1989 through 1994, and we now are working on getting complete copies up on the Internet.

In this supplement, we have collected many of the ideas that were voted "Best of Issue" by our readers in Electronic Design from early 1995 through early 1996. We hope you enjoy reading it and, more importantly, find it useful. We'd like to hear from you, because we plan to publish another, similar supplement in 1997, containing the Ideas for Design voted Best of Issue for a corresponding time frame.

One final note: In several places throughout this supplement, you'll notice small boxes calling for readers to contribute articles to the Ideas for Design section. The fact is that we rely on our readers to supply the brief articles that make up Ideas for Design. We encourage all readers to participate in the IFD program, and share their innovative ideas with other readers.

STEPHEN E. SCRUPSKI
Editorial Director

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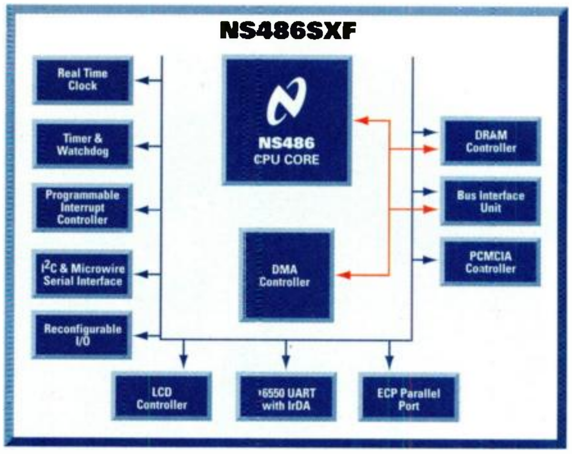

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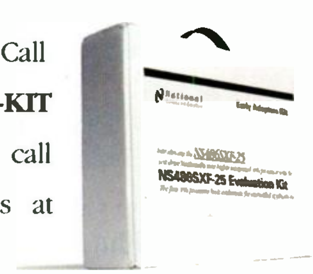

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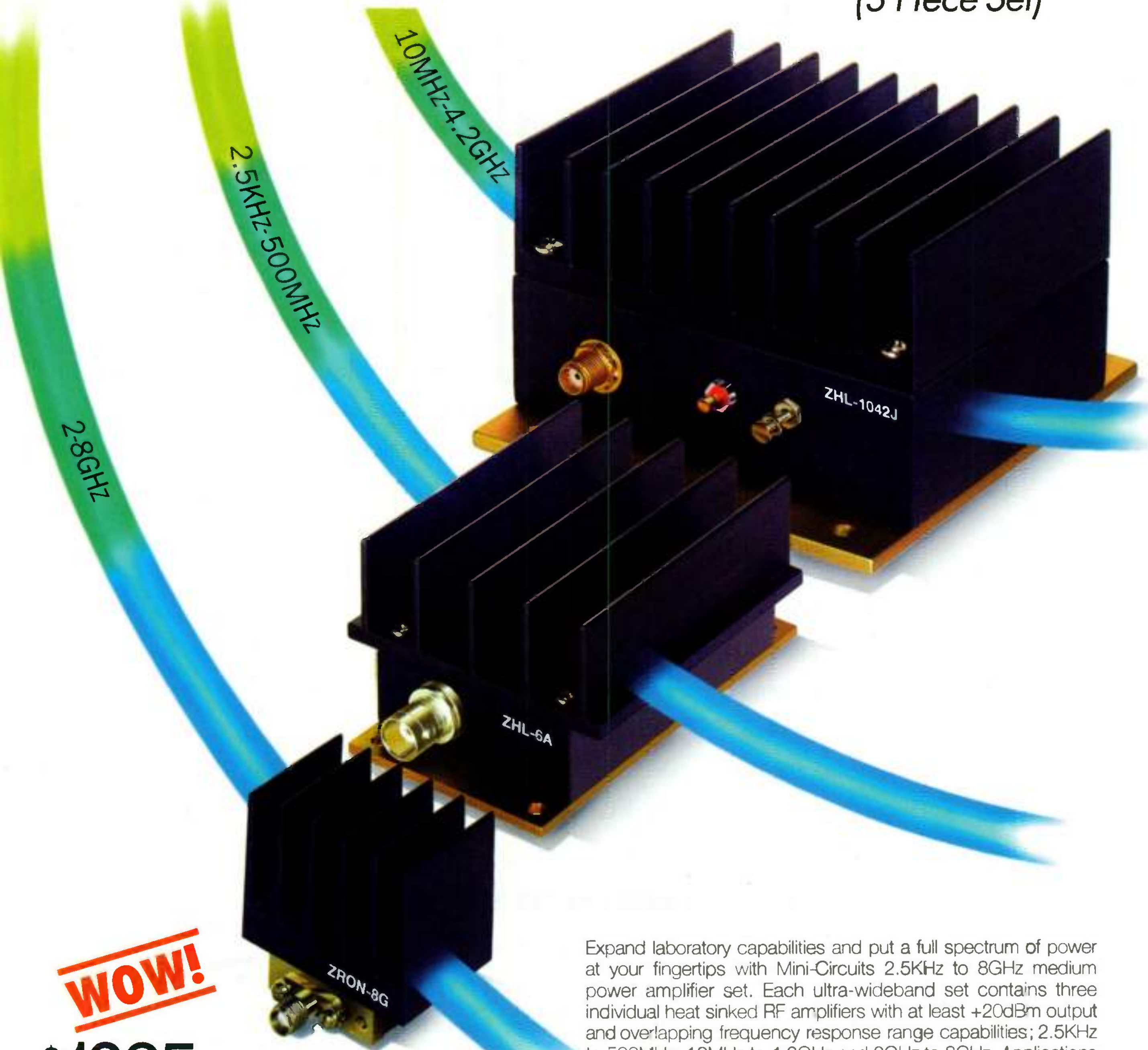

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Charge Pump Generates Gate Drive

CHESTER SIMPSON, 3360 Tracy Dr., Santa Clara, CA 95051; (408) 296-1925.

Many products that are loaded with logic hardware use 5 V as the main power source. The management, distribution, and conversion of this main 5-V rail often requires power FET devices. These devices are used as "switches" either in a dc mode (to connect or remove power to specific circuits) or in an ac mode (where the FET is driven at high frequency to provide dc-dc conversion).

In most cases, an n-FET makes a much better switch than a p-FET because of drastically lower cost, much lower on-resistance, and greater selection and availability of product. The only drawback of using an n-FET is that it requires "high-side drive" for the gate, which means a voltage source must be available that's higher than the 5-V rail. This "gate-drive voltage" needn't be well regulated, because it's simply used to pull the gate up high enough to turn the FET fully on.

The amount of voltage required for gate drive to assure the FET is fully turned on is typically about 5 V higher than the drain. Consequently, in 5-V systems, the available drive must be at least 10 V. Of course, more voltage is better, since it results in reduced on-resistance for the FET and, correspondingly, less power dissipation.

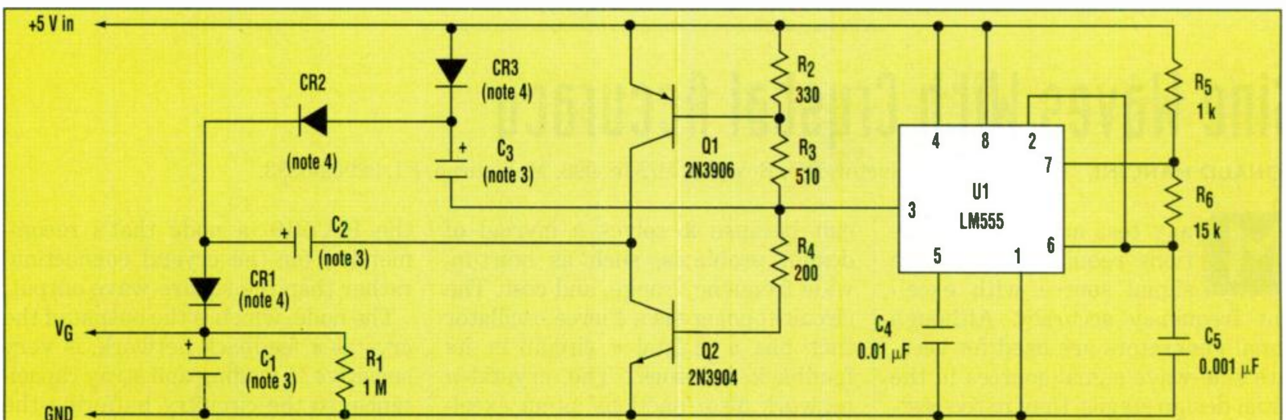
The amount of current that the gate-drive source must provide depends on the application: If the gate drive is only for FETs used as dc switches, then a few hundred microamperes is sufficient (the amount of dc current that flows into the gate is negligible). However, if the gate-drive source is used to provide bias voltage to a high-frequency converter, it may require 30 to 40 mA of average current. That's because the 2000 to 3000 pF of gate capacitance present on a typical power FET must be charged up and down at 100 kHz or more, and that takes a lot of current.

This Idea for Design presents a charge-pump circuit that's well suited for generating a gate-drive rail for either application, showing how to optimize selected components to address the "high current" or "low current" requirements that were stated previously.

The "high current" version will address applications requiring up to 40 mA, while the "low current" version is a lower-cost alternative providing up to 1 mA.

A charge pump is usually preferable to a typical switching converter for applications in which load current is < 50 mA. That's because it can be built with inexpensive, off-the-shelf components, it requires no transformer or inductor, and it produces zero EMI interference. Charge-pump (voltage-doubler) ICs are on the market, but they won't work in this case due to the fact that they only generate about 8 V from a 5-V input (two doublers could be used, but the cost is prohibitive).

The design shown is a voltage tripler, which provides the right amount of voltage needed for gate drive in a 5-V system (about 10 to 14 V) (*Fig. 1*). The circuit boosts the 5-V input by charging capacitors C1, C2, and C3 so that the voltage across C1 approximately equals 3 × (V_{in}–V_{diode}). Resistors R5 and R6, as well as capacitors C4 and C5 are



Notes:
1. Resistor tolerance is 5%.
2. All capacitors are ceramic, except as specified in Note 3
3. Values of C_1, C, and C depends on desired load current:
For the "low current" version, use 0.022-µF ceramic (Panasonic ECU-S1J223MEA or similar).
For the "high current" version, use 10-µF/25-V aluminum electrolytic (Panasonic ECE-A1EGE100 or similar) observing polarity shown.
4. Diode type used at CR1, CR2, and CR3 depends on load current:
For "low current" version, use 1N4148 or similar.
For "high current" version, use a small Schottky diode such as 1N5158 or similar.

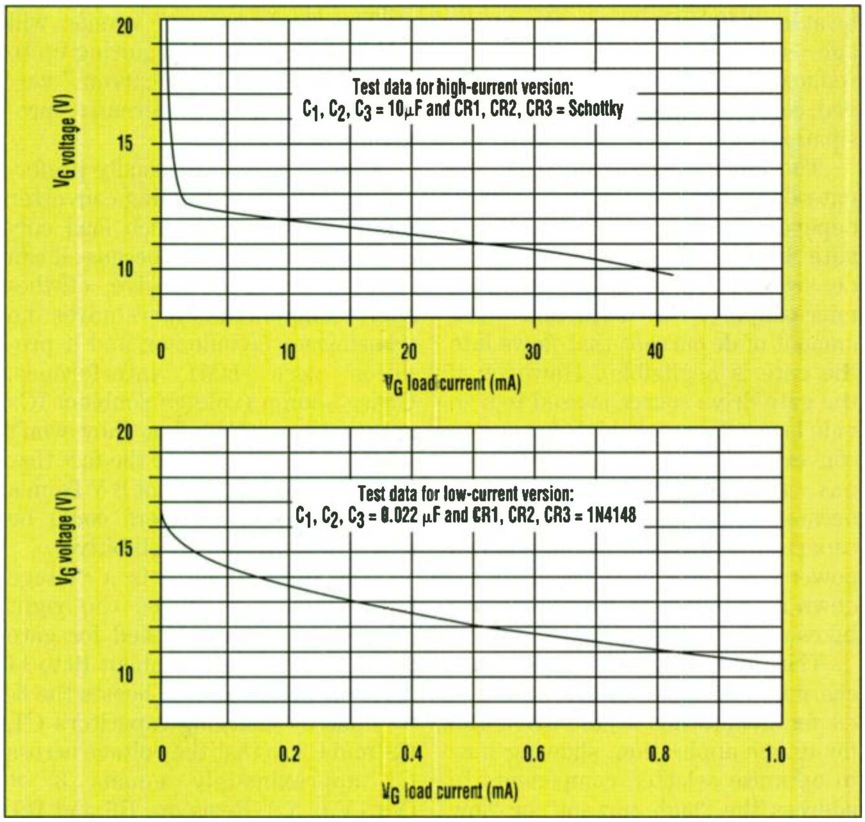
1. A CHARGE PUMP built as a voltage tripler can provide just the right amount of voltage needed for gate drive in a 5-V system.

used to set up the LM555 (U1) as an astable (free-running) oscillator that produces a 40-kHz square wave of 50% duty cycle at pin 3 (any typical ceramic capacitors can be used for C4 and C5).

On each complete cycle, C3 is charged up to about 4.3 V through CR3 when pin 3 of U1 pulls down to ground. When pin 3 is driven high (up to about 4 V), Q2 is turned on pulling the negative side of C2 to ground, and C3 charges C2 up to about 8 V through CR2. When pin 3 of U1 again goes low, Q1 turns on and pulls the negative side of C2 up to 5 V, which means its positive side swings up to about 13 V. This charges C1 up to about 12 V through diode CR1. As the charge pump operates, this cycle repeats continuously to keep delivering current to C1, which flows into the load connected to the VG point. The voltage seen at VG depends on load.

Obviously, optimizing the components used makes a better design. Therefore, if higher current (up to 40 mA) is needed, CR1-CR3 must be Schottky diodes similar to 1N5818. Also, C1-C3 must be 10-μF aluminum electrolytic capacitors. For a low-curent version, if 1 mA of load current is sufficient for the gate-drive source, 1N4148-type diodes are best for CR1-CR3, and 0.022-μF ceramic capacitors can be used for C1-C3 to save on cost and size.

The curves show the output voltage delivered by both versions of the circuit (using the components called out in the schematic diagram) as a function of load current (*Fig. 2*).



2. THE CURVES indicate the output voltage delivered by the high-current and low-current versions of the voltage tripler as a function of load.

Voted "Best of Issue," Electronic Design, September 18, 1995

Sine Waves With Crystal Accuracy

RONALD MANCINI, Harris Semiconductor, P.O. Box 883, M/S 58-096, Melbourne, FL 32902-0883.

Many test and design functions require a sine-wave signal source with excellent frequency accuracy. Although signal generators are used for accurate sine-wave signal sources in the initial design stages, they're too costly to dedicate to manufacturing test functions. One option is to design a sine-wave crystal oscillator, but it can be costly because the design task is difficult and risky.

Another option (*see the figure*) can replace signal generators in fixed frequency applications. The HA7210 crystal oscillator, which is typically used as a square-wave generator, functions as the basic oscillator circuit because it solves a myriad of design problems, such as startup, wide frequency range, and cost. The circuit topology is a Pierce oscillator that has a crystal-π circuit in its feedback network. The crystal-π network also functions as an excellent crystal filter, delivering a pure sine wave of the selected frequency at its output.

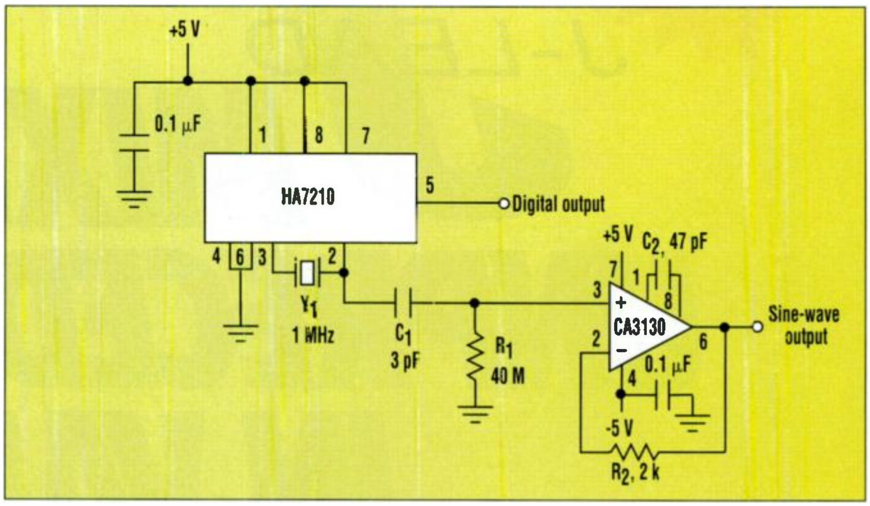
In this application, the HA7210 is configured as a 1-MHz oscillator with the other functions, such as enable, not being used. The frequency can be modified by changing the crystal and digital code on the frequency-select input pins. Notice that the sine-wave oscillator input is taken from pin 2 of the HA7210 (a node that's recommended for the crystal connection) rather than the square-wave output.

The node, which is the output of the crystal-π feedback network, is very sensitive to loading and stray capacitance, so the circuitry buffering the sine-wave source must not load down this point. If the feedback node can be buffered without affecting the oscillator's stability or sine-wave purity, the problem is solved. The CA3130 is selected as the buffer because it has a 14-MHz bandwidth, and its extremely high input impedance minimizes loading on the oscillator: C1 and R1 couple the sine wave from the oscillator to the CA3130

buffer. The buffer input impedance is 1.5 TΩ in parallel with 4.3 pF. If C1 is selected as 3 pF, the overall loading capacitance seen by the oscillator is 1.77 pF, which has no adverse effect on the oscillator. R1 is selected as 40 MΩ to provide a path for the buffer input bias current (it can be as large as 50 pA). This component selection yields a clean sine wave with an offset voltage of approximately 2 mV and a 2.5-V p-p amplitude.

The buffer's sine wave output leads the digital output of the oscillator by approximately 54. Both outputs are low impedance and available for simultaneous use as signal sources.

Voted "Best of Issue," Electronic Design, September 5, 1995



A CRYSTAL OSCILLATOR, when used in this type of configuration, produces frequency-accurate sine waves, and thus can be used as a replacement for the costly signal generator.

Broadband Amplifier/Balanced Mixer

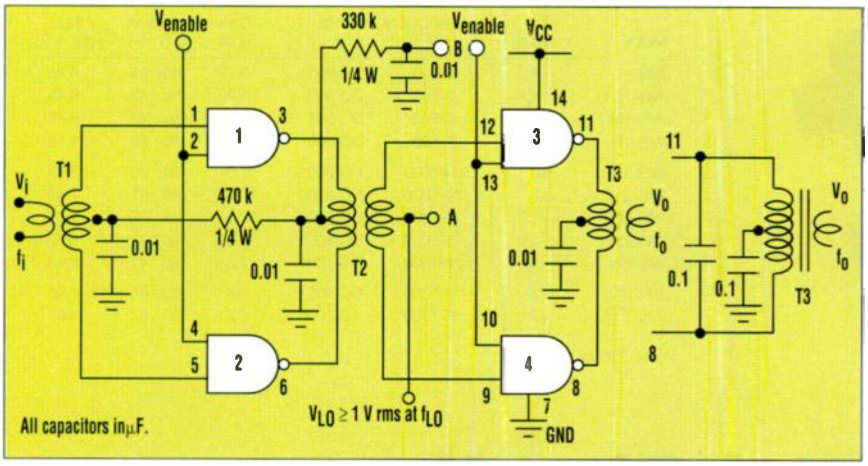
DON SCHENDEL, 6234 E. Aster Dr., Scottsdale, AZ 85254-4429; (602) 948-6880.

Various CMOS digital functions are usable in many analog applications. For instance, a single CMOS package (MC74AC00) makes possible a low-power, low-noise, broadband amplifier and balanced mixer (see the figure).

NAND gates 1 and 2 are configured in a self-biased, push-pull amplifier. The 470-k, 1/4-W resistor allows the gate outputs (pins 3 and 6) to establish equilibrium with the gate inputs (pins 1 and 5) for a nominal bias potential of +2.5 V. ($V_{CC}/2$). Pins 2 and 4, when connected together, allow for an external "enable" control of the amplifier. The amplifier is enabled when the control line is in the "high state" (V_{CC}). Both ends of the bias resistor are ac-bypassed at the center points of transformers T1 and T2 by 0.01-µF capacitors. Transformers T1, T2, and T3 are twisted-wire (transmission-line) types on small ferrite core toroids. Bandwidth and performance of the transformers are a function of the number and size of the wire turns on the type of toroids chosen for use. The upper frequency-response limit for this circuit is 60 MHz.

The balanced mixer is configured with the two remaining gates (3 and 4). Input pins 9 and 12 are connected to the secondary windings of transformer T2. Pins 10 and 13 also can be used as an "enable" control. The local oscillator (LO) potential is applied to point A (*see the figure, again*). The IF is realized at the secondary output of transformer T3. If point A is connected to point B (the 330-k, 1/4-W resistor and 0.01-µF capacitor node), a bias of +2.5 V is applied to pins 9 and 12 of gates 3 and 4 of the mixer. In this configuration, pins 10 and 13 become the drive points for the LO potential. This lowers the drive power required of the LO source and reduces LO power common-mode, inverse feedback through the amplifier stage.

Transformer T3 can be replaced by a small audio transformer, such as a 1-k ct : 8 Ω for direct conversion of either AM or SSB signals. The broadband amplifier exhibits power gains of 12 dB and greater with a noise factor 4.5 dB or less from 3 to 30 MHz. The balanced mixer offers 10 dB or greater conversion gain at a



A LOW-POWER, LOW-NOISE broadband amplifier and balanced mixer can be built using a single quad 2/input NAND gate CMOS package (the MC74AC00).

relatively low noise factor. The quad 2/input NOR gate, MC74AC02, also can be used for this function with similar performance.

However, the package pin configuration of this circuit must be changed accordingly. Other CMOS varieties, such as the 74HCxx family, may be used in this application.

Voted "Best of Issue," Electronic Design, October 2, 1995

Acquire Watt-Hour Data With RS-232

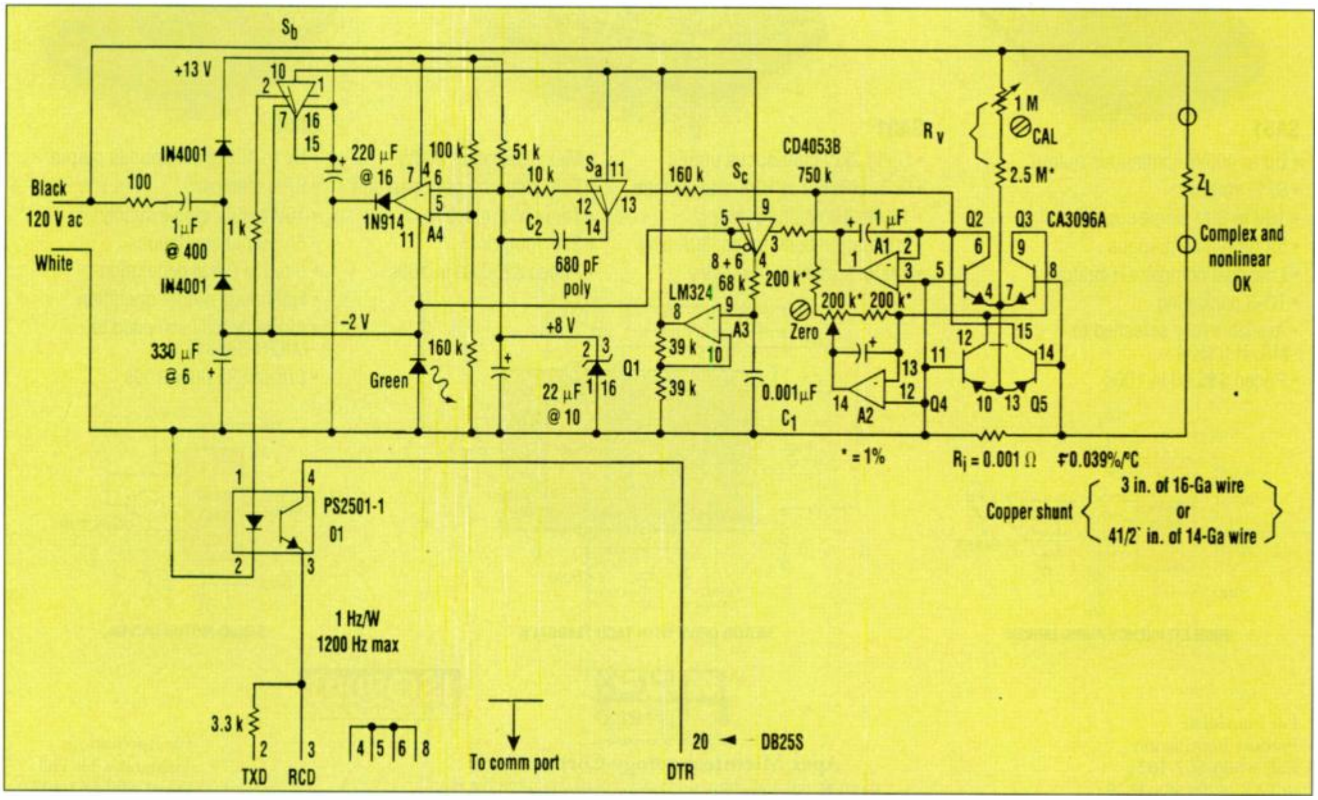
W. STEPHEN WOODWARD, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet:woodward@uncvx1.oit.unc.edu

Long-term measurement and recording of power consumption is useful when assessing energy efficiency of electrical appliances and apparatus. For meaningful readings of "real" (non-reactive) power, the wattmeter must be insensitive to both load reactance and nonlinearity.

This circuit utilizes a symmetrical pair of transistor multipliers to directly compute the four-quadrant product of real current and line voltage (*see the figure*). The result is averaged and converted to a variable-frequency, optically isolated, RS-232-compatible pulse output suitable for direct connection to the comm port of a standard PC. PC comm port hardware interprets each pulse as the "start bit" of a valid (although meaningless) character. Simple software running in the PC then can monitor the frequency of character reception as an accurate measure of power consumption.

Looking at one perspective of the circuit, consider positive half-cycles of the ac line voltage. These cause current proportional to the instantaneous line voltage to flow through R_V and forward-bias Q4 and Q5. If the instantaneous load current through R_i is zero, then the Rv current will divide equally between Q4 and Q5 due to the inherent matching of these elements from the CA3096A array.

The current entering Q4 is inverted by A2 and summed with Q5's current at integrator A1, at which point the currents will cancel, thus reflecting the zero-power condition. However, if the current is nonzero, the resulting voltage developed across R_i will cause a mismatch in the Q4/Q5 currents. Because we're dealing with positive half-cycles, if the load current is in phase with the line voltage, every ampere of load current will make the Q5 end of R_i 1.0 mV more positive than the Q4 end. Each millivolt of R_i voltage causes 0.8% of mismatch in the Q4/Q5 currents, with Q4 passing more than Q5. Consequently, the currents summed by A1 will no



THIS OPTICALLY ISOLATED AC POWER-TO-FREQUENCY converter produces an RS-232-compatible output suitable for direct input to a PC communications port.

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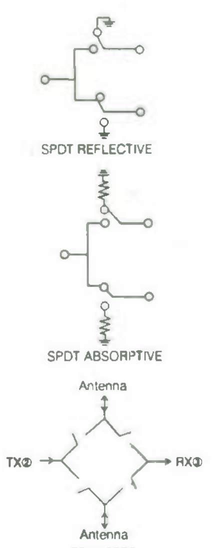

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longer cancel and A1 will accumulate 3.2 nA for every watt drawn by the load. The transistor multiplier's negative temperature coefficient is largely compensated by the positive temperature coefficient of the copper current-sensing resistor R1.

A1's output controls the current-to-frequency converter, which consists of A3 and Sa, Sb, and Sc. The idle state of the converter sets A3's output high. This connects C1 to A1's output and charges C2 to the 8-V reference voltage developed by Q1. When A1's output voltage charges C1 enough to pull A3's inverting input higher than its noninverting input, A3's output goes low. This event initiates the discharge cycle of C1, the duration of which determines the length of the RS-232 output pulse generated by Sb through isolator O1.

Meanwhile, Sa resets the charge-pump capacitor C2. This action provides frequency-proportional current feedback that, at equilibrium, accurately balances the difference between the Q4/Q5 currents, making the output frequency of the converter equal to 1 Hz for every watt of average load power. Full-scale output is 1200 Hz. For negative line half-cycles, Q4/Q5 turn off and Q2/Q3 take over power computation duties.

Voted "Best of Issue," Electronic Design, April 3, 1995

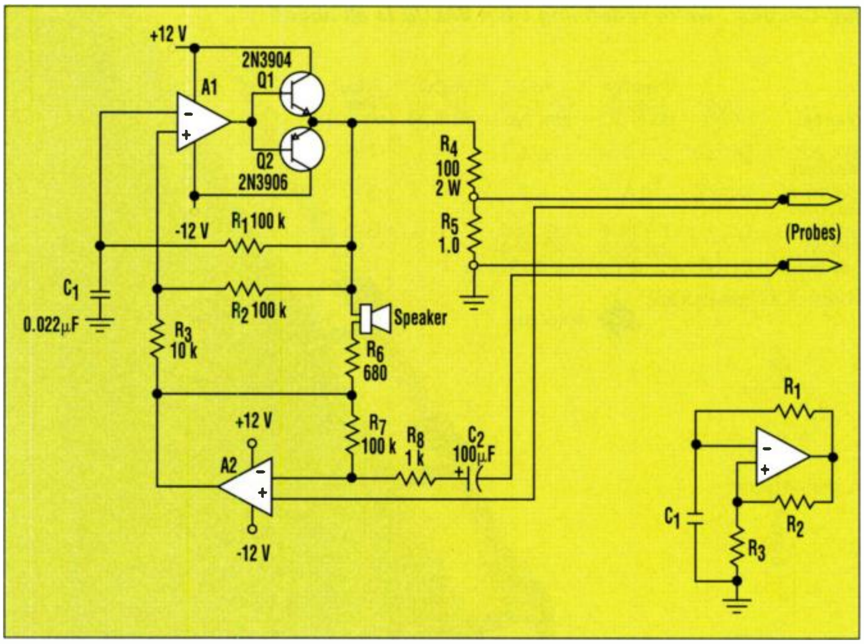
"Beeper" Finds Circuit Shorts

JIM WOOD. Inovonics Inc., 1305 Fair Ave., Santa Cruz, CA 95060; (408) 458-0552.

This design offers a way to trace resistance in the milliohm range, right to a short between bridged traces beneath a solder mask (see the figure). It simply translates resistance into an audible tone, which increases in pitch as the measured value approaches zero.

In the classic op-amp multivibrator (shown in the inset), oscillation frequency is determined not only by the R1C1 time constant, but also by the hysteresis set by the R2/R3 resistor ratio. A1 in the main figure, with current boosters Q1 and Q2, is this same configuration.

Assuming a virtual ground at the output of A2, free-run frequency is about 1 kHz–quite audible through a tiny 8-Ω speaker. Q1 and Q2 deliver a ±10-V squarewave to R4, dumping a ±100 mA through a short circuit placed across the probe tips. R5 ensure than open circuit voltage never exceeds ±0.1 V.



RESISTANCE BETWEEN BRIDGED TRACES can be translated into an audible tone with this circuit. The tone increases in pitch as the measured value approaches zero. The inset at the lower right shows a classic op-amp multivibrator.

A2 monitors the voltage between the probes. The differential input must have its own separate path to the probe tips to eliminate test lead resistance from the measurement. Miniature "zip-cord" sold as loudspeaker wire makes a tidy two-conductor test lead.

When the probes are open, A2's gain equals the R4/R5 divider loss, and the output of both amplifiers is identical. This has two effects: First, hysteresis is greatly increased and frequency falls to a low growl, and secondly, the loudspeaker that bridges the two in-phase outputs is effectively silenced.

A dead short across the probe tips will return nothing to A2 and the circuit will squeal at its nominal 1-kHz rate. Anything less than a perfect short produces some output from A2, increasing multivibrator hysteresis and lowering the pitch. The circuit has so much "leverage," and the ear is so sensitive to pitch changes in this range, that it's easy to resolve minute resistance differences.

Any general-purpose op amp will suffice in this circuit–a couple of 741s or an equivalent dual. Again, two wires must be taken to each probe tip and soldered securely. Also, probes must make low-resistance contact with the circuit under test. The H.H. Smith #317 probe is ideal here. Its tip is a replaceable, old-fashioned steel phonograph needle that can pierce insulating layers and dig into oxidized solder joints.

Voted "Best of Issue," Electronic Design, April 3, 1995

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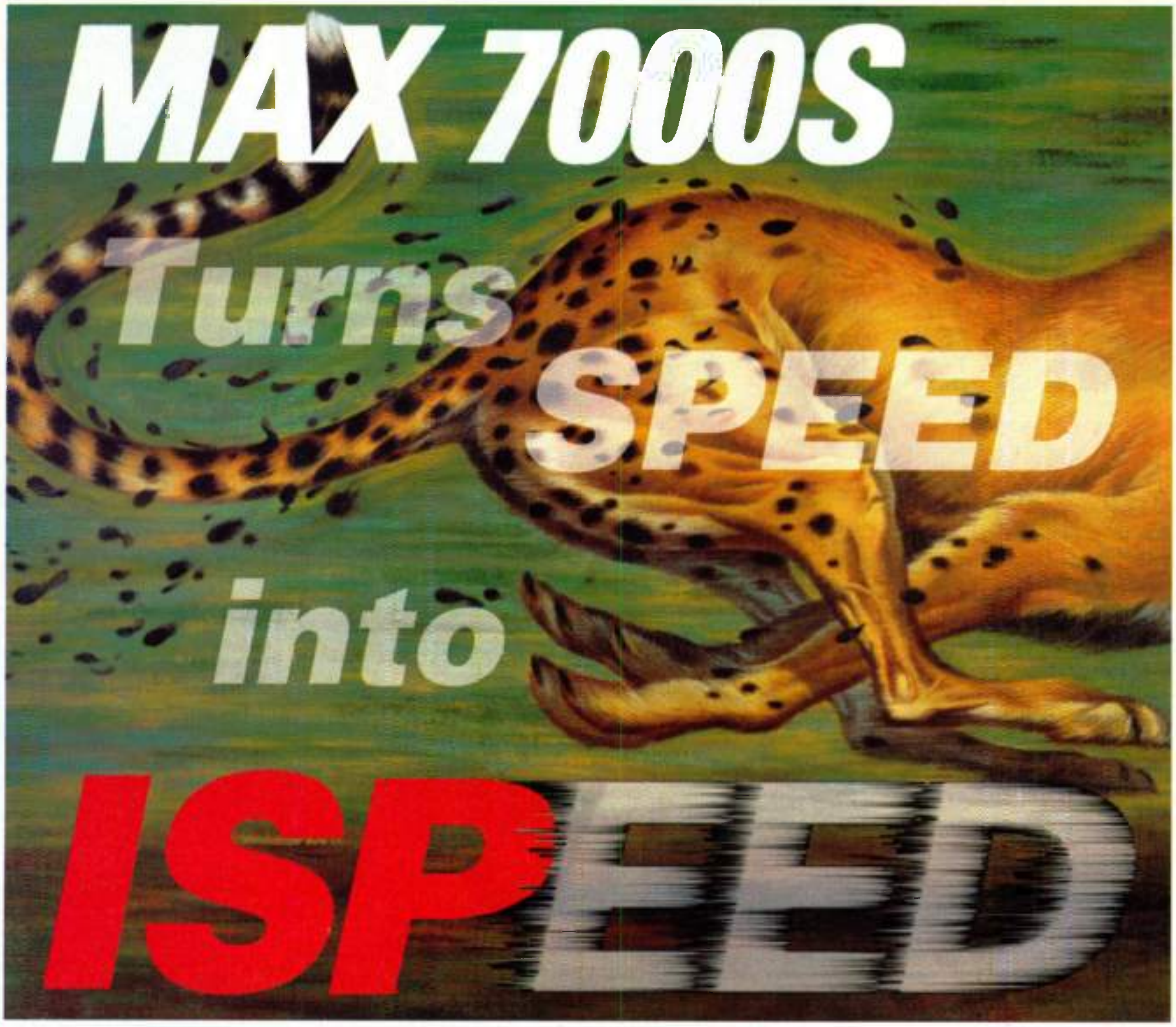

Device	ISP	Speed (t_{PD})
EPM7256S	Yes	7.5
EPM7192S	Yes	7.5
EPM7160S	Yes	7.5
EPM7128S	Yes	7.5
EPM7096S	Yes	7.5
EPM7064S	Yes	5
EPM7032S	Yes	5

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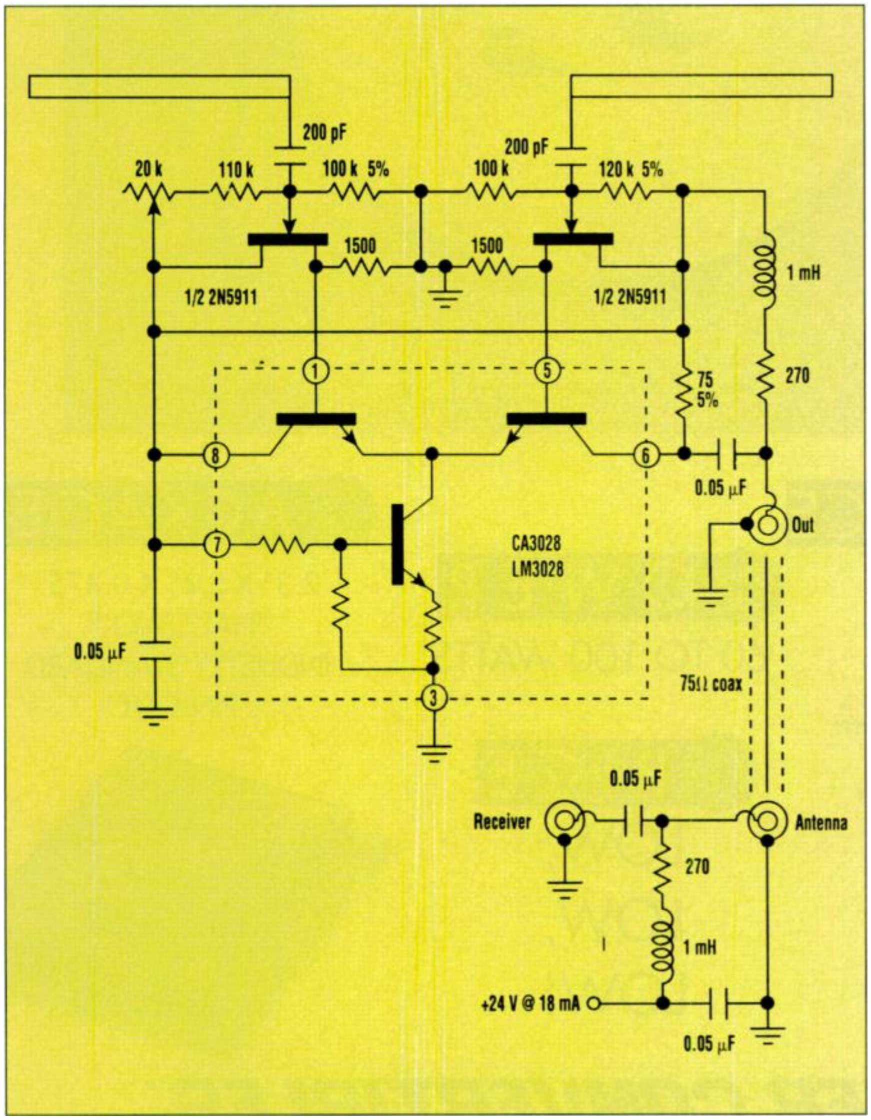
A Miniature Broadband Antenna

M.J. SALVATI, Flushing Communications, 150-46 35th Ave., Flushing, NY 11354; (718) 358-0932.

An electrically short dipole retains its figure-eight polar pattern (with characteristically sharp nulls) at all frequencies below its half-wave resonant frequency. However, the output impedance of an electrically short dipole is so high that it can't develop sufficient power to drive the usual receiver.

Using the impedance converter shown (*see the figure*) solves this problem by providing a huge current gain so that the voltage appearing at the dipole's output can eventually drive a 75-Ω load. Combining a short (3-to-6-ft.) dipole antenna and the converter results in a broadband (3 to 30 MHz) receiving antenna that can be rotated to null out an interfering signal. Because the dipole is short and the converter's differential voltage gain is only 4 dB, the signal level will be lower than with the usual receiving antenna. But, the salient feature of this antenna system is its ability to reject an unwanted signal, not its gain.



A SHORT DIPOLE ANTENNA and impedance converter combined together can be rotated to null out an interfering signal. The converter supplies a tremendous current gain so that the voltage appearing at the dipole's output can eventually drive a 75-V load.

The 2N5911 dual FET is configured as a pair of source followers to present a very high impedance load to the antenna, as well as power gain to drive the differential amplifier. It's extremely important to minimize the input capacitance of the source follower through proper device selection and construction technique. A high-frequency FET with low interelectrode capacitances, such as the 2N59111 or any of the Siliconix U440 family, is an excellent choice. Similarly, miniature (1/8 W) carbon-film resistors and minimal board footprints should be used for the gate connections.

The CA3028 is connected in its differential mode to combine the signals from the dipole halves into a single, ground-referenced signal. A 75-Ω collector load resistor also provides back-matching for the connecting cable. A multiplexing network, comprised of the capacitor, resistor, and RF choke connected to the output jack, allows the connecting cable to carry both the output signal and the operating current. A similar network at the power supply separates the two, so that the output signal can be applied to the receiver's 75-Ω input. The CA3028's biasing can be adjusted for equal signal-peak clipping at maximum output through the 20-k trimpot in the FET's gate-biasing circuit.

The dipole was created by colinearly joining two telescoping antennas (spaced about 0.5-in. apart) with a plastic rod jammed into their bases. This produces a dipole adjustable from 36 to 74 in. This adjustability is used only to fit the amount of space available in the reception area. There are no frequency-related adjustments because the dipole is always nonresonant at the antenna's operating frequencies (3 to 30 MHz).

Voted "Best of Issue,"
Electronic Design, February 20, 1995

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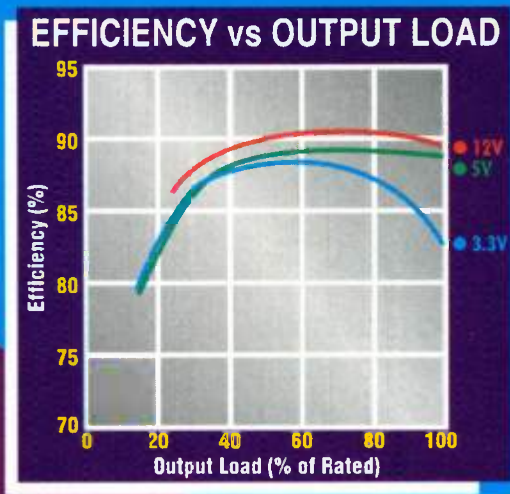

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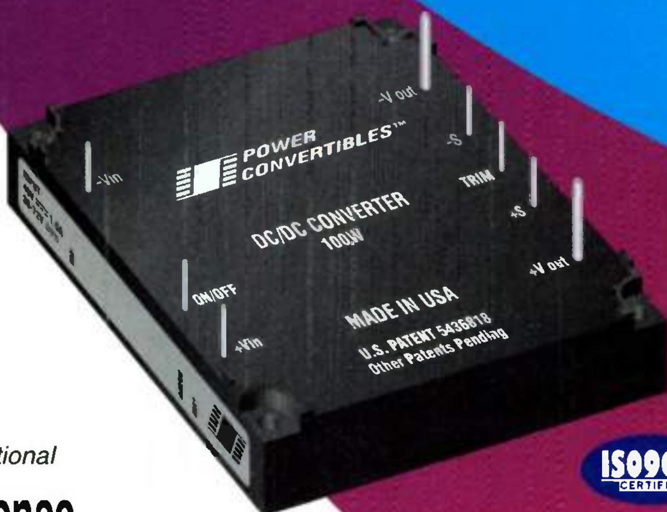

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equation

$$T_{pw} = -R_4 C_2 \ln\left[\frac{V_{ltp} - 1V}{V_{utp} - 1V}\right] + P_{dly}$$

$$= -(1K)(330pF)\ln\left[\frac{0.667V}{2.333V}\right] + 75 \text{ ns}$$

$$= 488 \text{ ns}$$

To approximate frequency:

$$F(v_{in}) = \left(\frac{R_5 C_2 (V_{utp} - V_{ltp})}{v_{in} - 0.5V} + T_{pw}\right)^{-1}$$

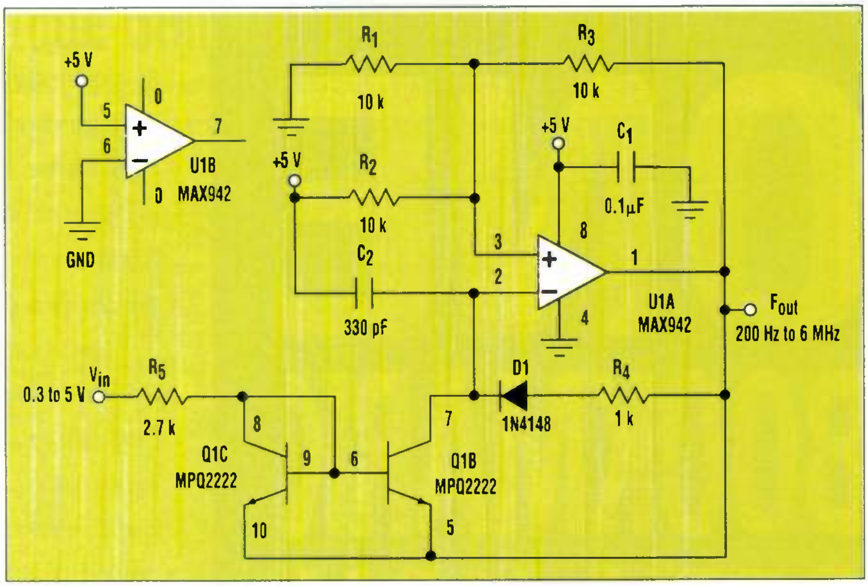
$$= \left(\frac{(2.7K)(330pF)(3.333 - 1.667)}{v_{in} - 0.5V} + 488 \text{ ns}\right)^{-1}$$

$$= \left(\frac{1.486 \times 10^{-6} \text{ Vs}}{v_{in} - 0.5 \text{ V}} + 488 \text{ ns}\right)^{-1}$$

Upon observation, the prototype circuit linearity was approximately 2% over the tested range. Also, up to 6-MHz operation was possible using the MAX942 by carefully selecting C2 and the hysteresis resistors.

On the low side, discrete transistors can be used instead of the Motorola MPQ2N2222 monolithic quad package. This may cause some instability at low frequencies. The transistors should be located in close thermal proximity. On the high side, a good matched transistor pair can be used. Analog Devices' MAT-01 is a good choice. Other high-speed comparators are available. The Spice program uses an LT1016 device from Texas Instruments (*see the listing*).

Voted "Best of Issue," Electronic Design, November 20, 1995



THIS WIDE-BANDWIDTH voltage-to-frequency converter, which is a variation of a relaxation oscillator, is rather inexpensive to produce.

```
*SPICE_NET
*INCLUDE BJTN.LIB
.MODEL QN2222 NPN (IS=15.2F NF=1 BF=105 VAF=98.5 IKF=.5
+ ISE=8.2P NE=2 BR=4 NR=1 VAR=20 IKR=.225 RE=.373 RB=1.49
+ RC=.149 XTB=1.5 CJE=35.5P CJC=12.2P TF=500P TR=85N)
*   Motorola 30 Volt  .8 Amp 300 MHz SiNPN Transistor 04-11-1991
*INCLUDE TICOMP.LIB
.SUBCKT LT1016T   1 2 3 4 5 6 21
*
F1     3  9  V1  1
IEE    7  4  DC  100.0E-6
EVO 20  0 POLY(1) 3 0 -1.4 1
*ADDED OUTPUT SUPPLY
R1 20 5 33
*ADDED PULL-UP RESISTOR
R2 21 0 1MEG
*ADDED RESISTOR
EOUT 21 0 POLY(1) 20 5 .2 1
*ADDED COMPLEMENTARY OUTPUT
Q1     9  2  7 QIN
Q2     8  1  7 QIN
Q3     9  8  3 QMO
Q4     8  8  3 QMI
.MODEL QIN NPN(IS=800.0E-18 BF=10)
.MODEL QMI PNP(IS=800.0E-18 BF=1002)
.MODEL QMO PNP(IS=800.0E-18 BF=1000 CJC=1E-15 TR=6.211E-9)
E1    10  6  3  9  1
V1    10 11 DC 0
Q5     5 11  6 QOC
.MODEL QOC NPN(IS=800.0E-18 BF=53.30E3 CJC 1E-15 TF=154.3E-15 TR=4.192E-9)
DP     4  3 DX
RP     3  4 2.041E3
RP1 3  6 .67
*ADDED POWER RESISTOR
.MODEL DX D(IS=800.0E-18)
*
.ENDS
.TRAN 25E-9 40E-6 20E-6
*INCLUDE DEVICE.LIB
.MODEL DN4148 D(RS=.8 CJO=4PF IS=7E-09 N=2 VJ=.6V
+ TT=6E-09 M=.45 BV=100V)
*ALIAS  V(5)=FOUT
.PRINT TRAN  V(5)
R2 1 9 10K
V3 3 0 DC 1V
C2 1 4 330PF
Q1B 4 6 5 QN2222
R3 9 5 10K
X1 9 4 1 0 5 0 xx LT1016T
Q1C 6 6 5 QN2222
R5 3 6 2.7K
R1 9 0 10K
R4 8 5 1K
D1 8 4 DN4148
V1 1 0 DC +5V
.END
```

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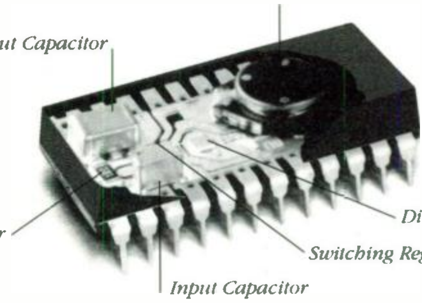

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Wideband AGC Loop

REA SCHMID, Comlinear Corp., 4800 Wheaton Drive, Fort Collins, CO 80525-9483; (970) 225-7421; fax: (970) 226-0564.

Wide-bandwidth systems often need a dc-to-high-frequency automatic gain control (AGC) circuit to amplify various signal types. Even though there are many high-speed AGC parts available, they tend to work at extremely high bandwidths and at prices that aren't cost-effective for applications today. The idea presented here takes advantage of the technology of dc variable gain amplifiers to implement an AGC circuit with an external loop.

Automatic leveling loops or gain-control loops are difficult to implement without affecting bandwidth when changing gain. However, high-speed monolithic variable-gain amplifiers and high-speed voltage-feedback amplifiers can be used to implement a high-performance fast-settling loop function for continuous-waveform signals (*see the figure*). At the same time, the loop maintains a gain bandwidth that's independent of changes in gain.

The circuit uses a variable gain amplifier (U1) in the forward path to amplify the continuous-time-domain signals occurring at Vin. U1 has two input pins with high-input impedance that provide both noninverting (pin 3) and inverting (pin 6) functions. Once one has selected the inverting or noninverting configuration, the common-mode input voltage range is set by the designer with resistor R_g. The maximum peak input voltage on pin 6 and the current through R_g is used to calculate the resistor value using the following equation:

$$R_g = Vin(peak)/I_R$$

IR is the current through the resistor, which is 1.8 mA typically. The maximum common-mode range is ±2.2 V for a ±5-V supply operation. The minimum usable signal level is determined by the input RMS noise.

Once the maximum required gain is determined, Rf is selected by the formula shown below, while setting V_g to +1 V:

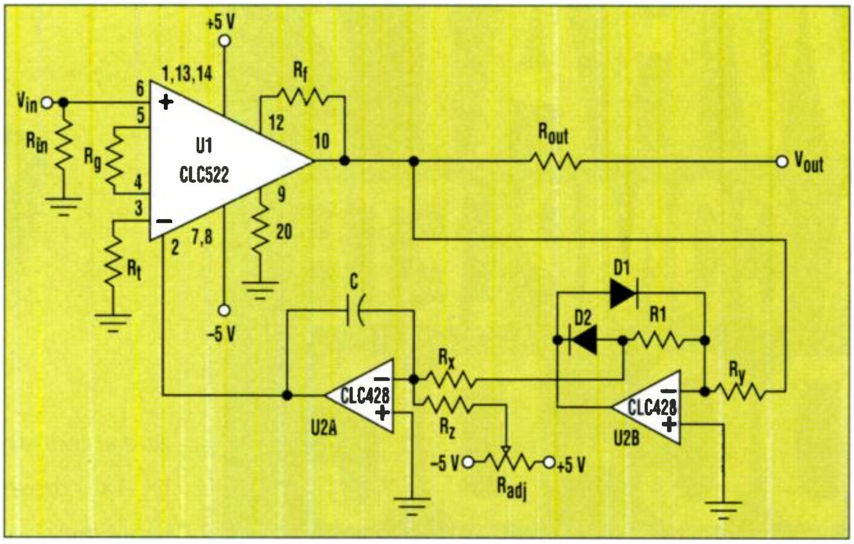
$$A_V = 1.85(R_f/R_g)((V_g + 1)/2)$$

V_g is the gain-control voltage and has a linear voltage range of –1 to +1 V with a gain linearity of 0.04% for Vout of ±2.0 V. The CLC522 attenuates the signal internally from this maximum level. Therefore, the input noise floor and the output voltage range determine the lower and upper signal limits for the part. The output voltage range is ±4.0 V with an output current of ±70mA.

The maximum bandwidth is a function of the internal current-feedback amplifier and the selection of Rf. U2 has a usable selectable-gain range from 2 (6 dB) to 100 (40 dB). At a gain of 2 with V_{out} of 2 V p-p, a 330 MHz bandwidth is achieved. For gains of 20 to 100, –3-dB bandwidths of 165 MHz and 45 MHz can be expected. Adding capacitance in parallel with R_g will extend the –3-dB bandwidth for gains of 10 to 220 MHz.

The low-noise dual voltage-feedback amplifiers (U2) extend the dynamic range by placing the Schottky diodes or other low capacitive diodes in the feedback path. R1 and Ry set the gain of the rectifier. The adjustable resistor (R_{adj}) sets the desired output voltage level and ensures that the initial conditions at pin 2 of U2 are +1 V with no input signal. When the rms current of the signal is greater than the negative current from R_{adj}, the integrator decreases the gain of U1. Conversely, when the signal drops below the R_{adj} current, the gain of U1 is increased. The acquisition time and hold time are set by R_x, R_y, and C.

For larger gains and smaller bandwidths, the CLC428 meets the performance bandwidth requirements. When smaller gain ranges and larger bandwidths are required, a higher unity-gain-bandwidth CLC420 or CLC440 amplifier should be substituted for U2.



HIGH-SPEED MONOLITHIC variable gain amplifiers and high-speed voltage-feedback amplifiers are used to implement a high-performance fast settling AGC loop function.

Voted "Best of Issue," Electronic Design, February 5, 1996

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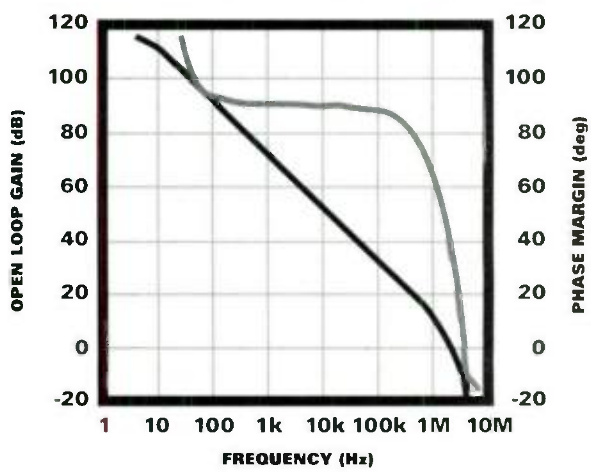

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Low-Cost Precision Thermometry

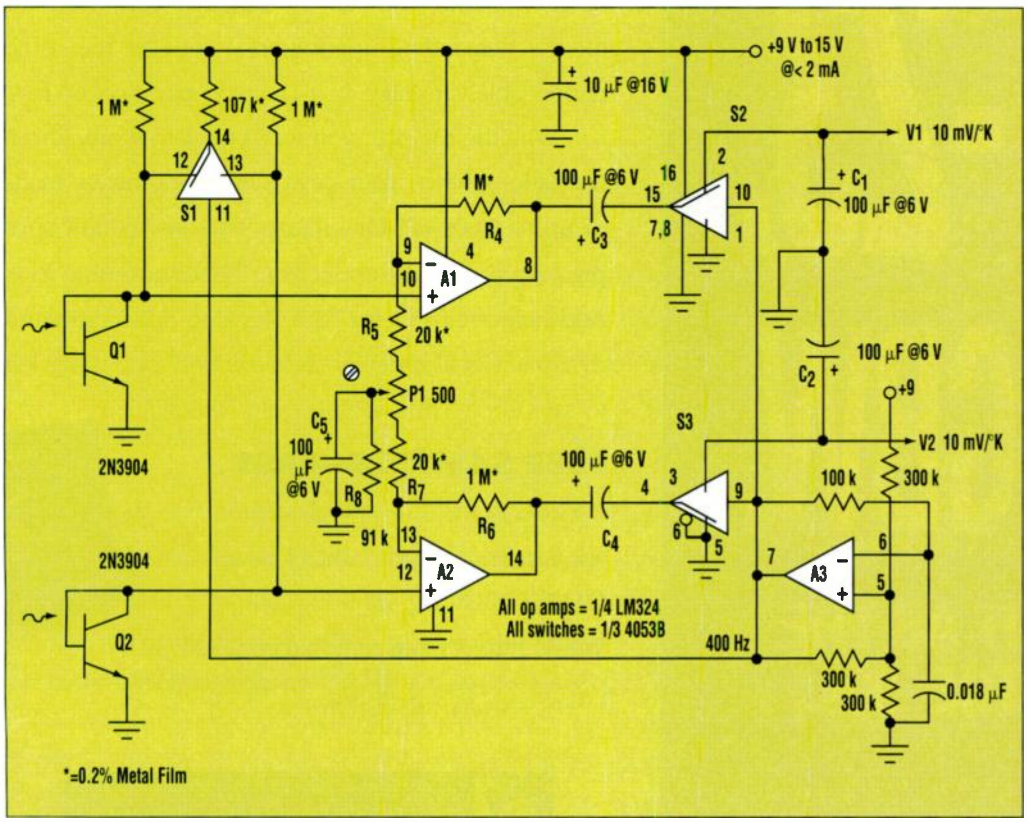
W. STEPHEN WOODWARD. U. of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvx1.oit.unc.edu.

Among the wide variety of temperature-sensing components available, the least expensive and most available is the diode-connected transistor. Circuits exploiting the approximate –2.2-mV/degree temperature dependence of the base-emitter junction forward voltage are common and work well. They all suffer, however, from unpredictability of the characteristics of the individual transistors. Consequently, they must be recalibrated whenever the sensing transistor is replaced.

A method does exist, though, that uses the humble transistor as a precalibrated temperature sensor (see Jim Williams' article "AN45," in the *Linear Applications Handbook, Vol. II*, published by Linear Technology Inc.). This "delta-V_{be}" technique exploits the proportionality of dynamic impedance of transistors to absolute temperature. At 298K, for example, delta V_{be} is about 60 mV/decade. This number is independent of transistor device-to-device and even type-to-type variation. It can, therefore, be used to fashion precision thermometers that need no transistor-dependent calibration. However, the reference cited recommends a number of premium components that increase the cost and thus loses the advantage of using inexpensive transistors in the first place.

The circuit described here, by contrast, combines the delta-V_{be} effect with inexpensive generic parts to achieve two channels of truly low-cost "no calibrate" transistor thermometry (*see the figure*). CMOS switch S1 modulates the bias current applied to temperature sensors Q1 and Q2 over a 10:1 ratio. Only this ratio, rather than the exact current, matters in this case. The resulting square waves at the input of A1 and A2 have amplitudes directly proportional to the absolute temperature of Q1 and Q2. A1/A2 scale their respective ac inputs to 10 mV/degree, yielding 2.98-V p-p square waves at 298K. Despite the fact that fairly high gain is required (34 dB), the ac-coupled signal path ignores offsets and permits use of inexpensive (LM324) op amps. The dc component of these signals is blocked by C3/C4 and the ac is synchronously rectified by S2/S3. This produces stable, low-impedance (about 500 Ω) dc outputs. Multivibrator A3 produces a 400-Hz square wave for modulation and synchronous-rectification timing.

The two thermometer channels have unadjusted accuracies of better than 1 degree. Trimmer P1 allows matching of the tracking of the two to <0.1 degree. This is ideal for applications like wet-bulb/dry-bulb hygrometry and thermal-management analysis. The circuit's power consumption is less than 2 mA at 8 to 15 V, which is ideal for battery operation. Power-supply feedthrough is about 0.1 degree/V = –60 dB.



TWO CHANNELS of low-cost "no calibrate" transistor thermometry can be achieved with this circuit, which combines the delta-V_{be} effect with inexpensive generic parts.

Voted "Best of Issue," Electronic Design, August 21, 1995

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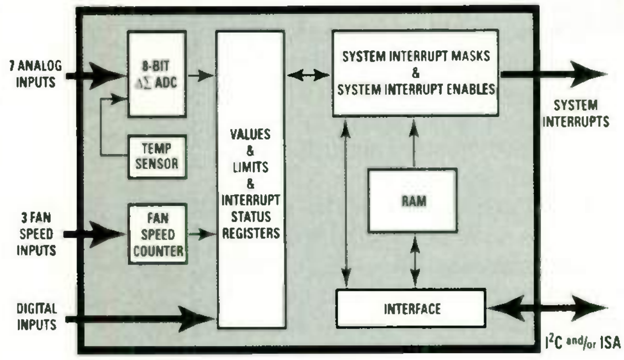

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Generate FIR Filter Coefficients

FRANK N. VITALJIC, 514 13th St., Bellingham, WA 98225.

The calc_coeffs() function can calculate FIR filter coefficients h(i) for low-pass, high-pass, bandpass, and band-reject filter types (*see the listing*). For an odd-valued filter length N, coefficient values having even-symmetry about the h[(N – 1)/2] coefficient (i.e., h(i) = h(N – 1 – i) will exhibit linear phase. This makes the filter's time delay (Td) independent of frequency. Td = (N – 1)/2fs, where fs is the sampling frequency in hertz. The first half of the coefficients, 0 through (N – 1)/2, are stored in the filter_coeffs (MAX) array.

To reduce stopband ripple, a Hamming window (window_type = SNGL) is applied as weighted factors to the filter coefficients. By applying the window a second time (window_type = DUAL), the stopband attenuation substantially improved at the price of broadening the transition region (see the figure).

All filter types and filter lengths above 15 exhibit excellent passband ripple of less than 0.1 dB with respect to unity gain. The low-pass characteristics illustrate both the broadening of the transition region and deep stopband attenuation (*see the table*).

The FIR filter gain H(f) can be calculated as follows:

$$H(f) = h[(N-1)/2] + 2\sum_{i=0}^{\frac{N-3}{2}} h(i)\cos\left[2\pi\left(\frac{N-1}{2} - i\right)f\right]$$

for f = 0 to 0.5 Hz

The f1 and f2 definitions (normalized) are:

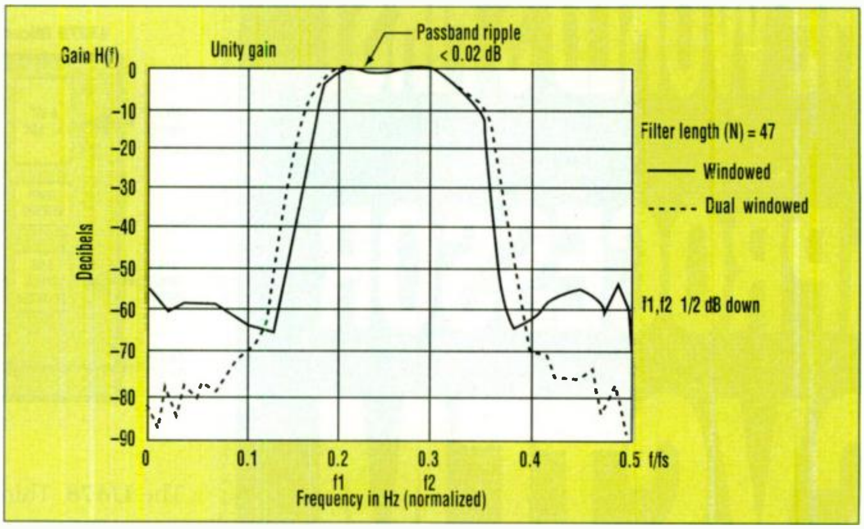
Low-pass filter: f1 = 0; f2 = cut-off frequency

High-pass filter: f1 = pass frequency; f2 = 0.5

Bandpass/band-reject filter: f1 = f_{low} f2 = f_{high}

At the pass frequencies, the gain is down 6 dB. A frequency offset (plus or minus) should be applied for other values of gain.

Voted "Best of Issue," Electronic Design, June 26, 1995



THE CURVES show the FIR filter bandpass characteristic when applying a single Hamming window and a dual window. When the window was applied a second time, stopband attenuation improved substantially.

Filter length (N)	f2/fs	
	f2 + 0.05 Hz	f2 + 0.1 Hz
31	–11 dB (–6)	–59 dB (–23)
41	**–19 dB (–10)**	**–57 dB (–52)**
61	–56 dB (–23)	–57 dB (–96)
81	**–59 dB (–54)**	**–59 dB (–88)**
101	–58 dB (–82)	–61 dB (–88)
127	**–62 dB (–81)**	**–69 dB (–90)**
( ) = dual windowed		

```
#include  <math.h> // FIR FILTER COEFFICIENTS PROGRAM

#define MAXLEN 127    //Maximum filter length
#define MAX  ((MAXLEN+ 1)/2)
#define PI  (4.0*atan(1.0)) //Define pi constant
#define LPF  1     //Enumerate filter types
#define HPF  2
#define BPF  3
#define BRF  4
#define SNGL  1     //Hamming window
#define DUAL  2     //Hamming window squared

void calc_coeffs( int filter_type,int filter_len,int window_type
                  doublef1,doublef2,double *filter_coeffs)
//Calculates FIR filter coefficients for the four filter types:
//Low Pass LPF, High Pass HPF, Band Pass BPF, and Band Reject BRF.
// The coefficients are stored in the filter_coeffs array.
{
  int i, flag = 0
  double ham_coeffs[MAX], A,B,C,F1,F2;

  //Clear filter_coeffs array
   for(i = 0; i < MAX;i++ ) filter_coeffs[i]=0.0;

  // Calculate Hamming Window Coefficients
  for (i = 0; i <= (filter_len-1)/2;i++ ) {
  double arg;
  arg = 2.0 * PI/(filter_len - 1);
  ham_coeffs[i] = 0.54 - 0.46 * cos(arg * i);
  if(window_type == DUAL ) ham_coeffs[i] *= ham_coeffs[i];
 }
 // Calculate filter coefffieients and pass through window
 if(filter_type == BRF ) { F1 = 0.0; F2 = f1;}
 else{F1=f1;F2=f2;}
 for (;;) {
  for(i = 0; i < (filter_len-1)/2; i++ ){
    A = sin(2.0 * PI * ((filter_len-1)/2 - i) * F1);
    B = sin(2.0 * PI * ((filter_len-1)/2 - i) * F2);
    C = PI * ((filter_len-1)/2 - i);
    filter_coeffs[i] += ((B - A)/C) * ham_coeffs[i];
  }
  if((filter_type == BRF) && (!flag)) { flag= 1; F1 = f2; F2 = 0.5;}
  else break;
 }
 // Calculate DC component value of coefficients
 if( filter_type == LPF) filter_coeffs[i] = 2.0 * f2;
 if( filter_type == HPF) filter_coeffs[i] = 2.0 * (0.5 - f1);
 if( filter_type == BPF) filter_coeffs[i] = 2.0 * (f2 - f1);
 if( filter_type == BRF) filter_coeffs[i] = 1.0 - 2.0 * (f2 - f1);
 }
```

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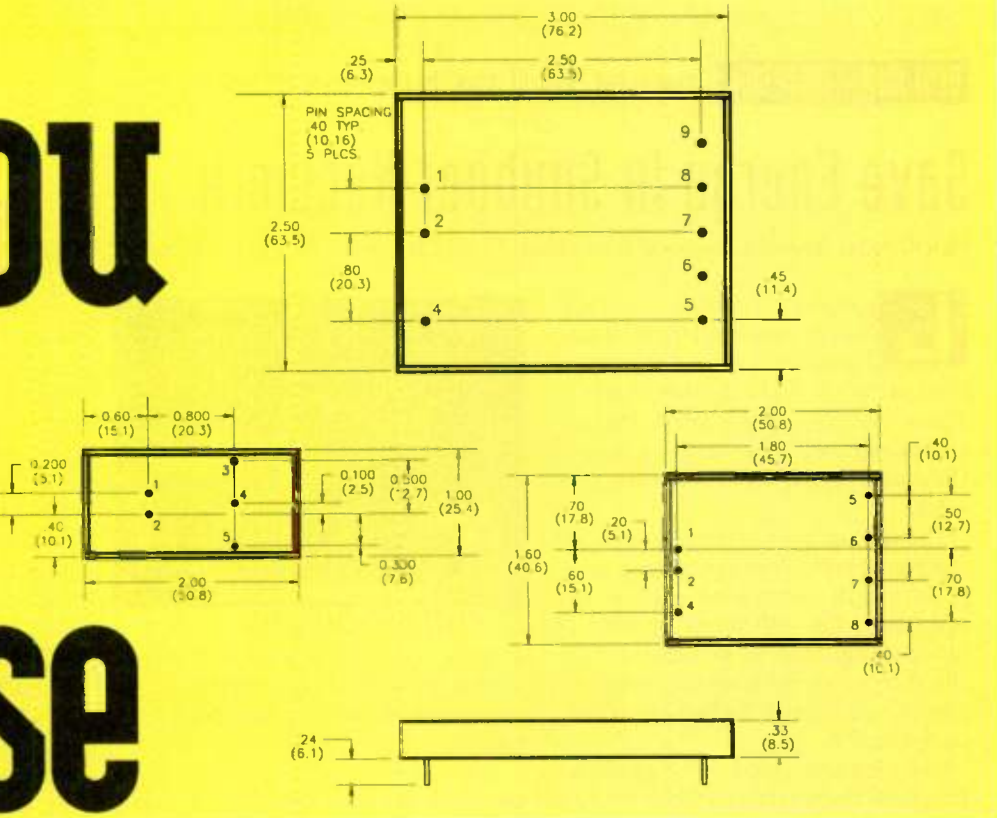

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READER SERVICE 177

Save Energy In Snubber Network

FERNANDO GARCIA, General Instrument Co., 1330 Capital Pkwy., Carrollton, TX 75006.

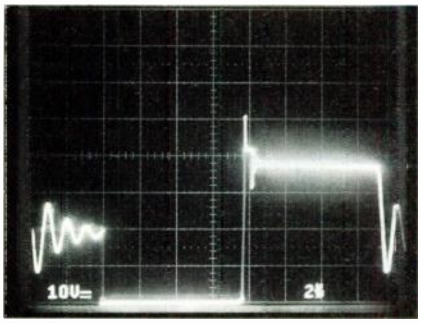
Leakage inductance, always a nuisance in switch-mode power supplies, is the main instigator of voltage overshoots. These voltage spikes may damage the power-switching devices unless they are tamed by a snubber network.

Though snubber networks perform the required task of protecting costly devices, it comes at the expense of efficiency. The efficiency penalty is usually regarded as nominal, but in the face of ever increasing requirements, additional techniques must be found.

One idea along that route would be to return the wasted snubber energy to an auxiliary output, such as, for instance, on flyback regulators. A flyback regulator offers the advantage of providing multiple output voltages with a single magnetic structure, and is therefore very compact and cost-effective (*Fig. 1*).

This particular circuit has a main +5-V output, as well as a +12.5-V auxiliary output. The device being driven also required a "bias" voltage of +27 V with a few milliamperes of current.

Originally, the voltage was going to be provided with a charge-pump technique, but closer inspection showed that the voltage could be obtained without any additional setup.



2. THE MODIFIED snubber network's operation at pin 4 of U1 is shown in this waveform (vertical scale: 10 V/div; horizontal: 2 ms/div).

The heart of the regulator is formed by a National Semiconductor LM2577-ADJ "simple switcher" controller IC. The main and auxiliary voltage configurations came straight from the company's application literature, with resistors R1 and R2 providing the feedback for the main +5-V output. The auxiliary +12.5-V output is regulated by the intrinsic tight coupling of a discontinuous-mode flyback topology. R3 and C1 are compensation devices.

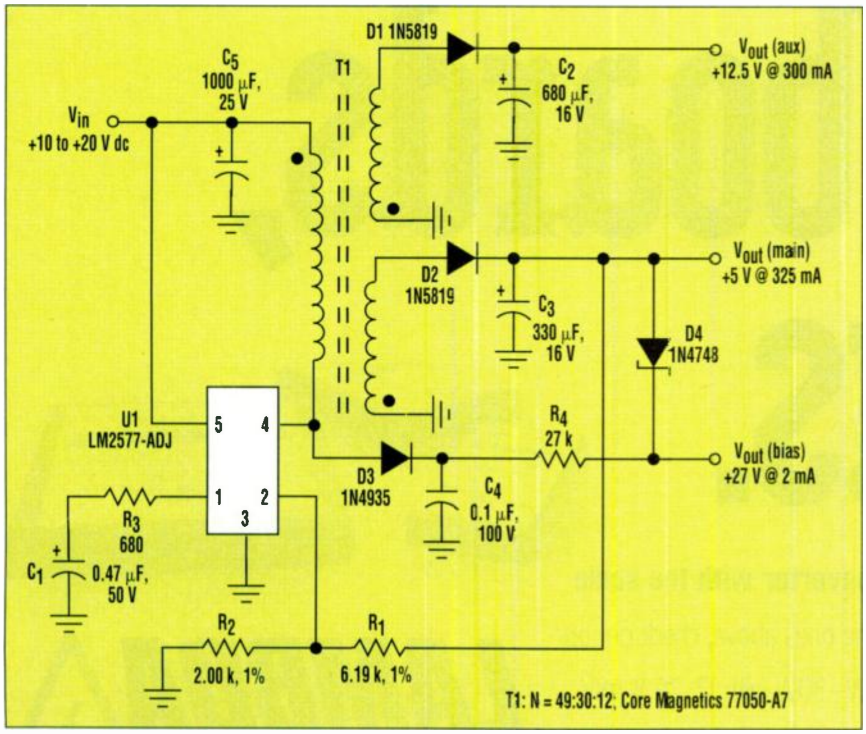
Whereas another winding could have been used in the transformer to provide the +27-V bias output, a "free" output may be realized from the voltage spikes in the primary winding being transferred via diode D3 to a reservoir capacitor (C4). The charge in the capacitor is drawn by the current of both the bias load and the shunt Zener regulator D4. Enough charge is depleted from the capacitor to allow the next voltage spike to almost fully dump its energy in the next cycle.

In a sense, this is a modified snubber network where the energy is being put to good use instead of wasting it as heat on a resistor. Figure 2 shows the network's operation.

Further efficiency points may be gained by returning the shunt Zener current to the +5-V supply. The Zener current contribution is small enough to only negligibly effect the voltage regulation.

Because the capacitor doesn't discharge completely to 0 V due to the Zener's voltage, this modified snubber isn't as effective as the traditional "lossy" snubber.

However, for applications that do not require extreme operating conditions, the circuit offers a useful cost reduction and efficiency improvement.



1. A FLYBACK regulator is a good application for implementing an energy-efficient snubber network. The network saves what would otherwise be wasted snubber energy by returning it to an auxiliary output.

Voted "Best of Issue," Electronic Design, May 1, 1995

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ZOS-75	37.5-75	-110	0.016	-26
ZOS-100	50-100	-111	0.026	-29
ZOS-150	75-150	-107	0.017	-26
ZOS-200	100-200	-106	0.015	-25
ZOS-300	150-280	-103	0.017	-27
ZOS-400	200-380	-100	0.021	-24
ZOS-535	300-525	-96	0.018	-27
ZOS-765	485-765	-96	0.033	-27
ZOS-1025	685-1025	-92	0.051	-25

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The QMS 2425 printer with NEC's V$_R$4300 processor received the PC Magazine Editors' Choice award.

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READER SERVICE 111

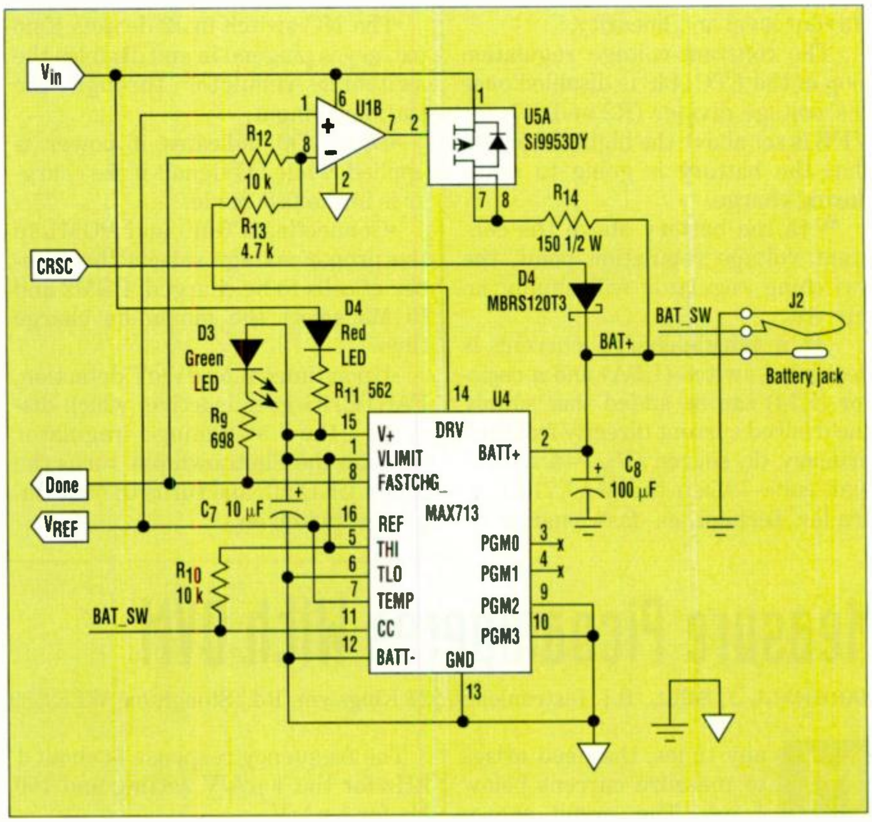
Battery Charger Made More Efficient

HERB SEIDENBERG, Toshiba America Information Systems, 2 Musick St., Irvine, CA 92718; (714) 587-6930.

The project at hand was to build a small, efficient, inexpensive, full-function battery charger that could charge 2 to 10 NiCd or NiMH cells. Choosing the charging controller, the Maxim MAX712/713, was simple because it was the only one that was pin programmable and didn't require software development. For reasons of efficiency, a switching regulator instead of the standard pass regulator had to be added. But, the MAX713's application notes suggested non-standard, non-state-of-the-art switching regulators as well as complex feedback loops.

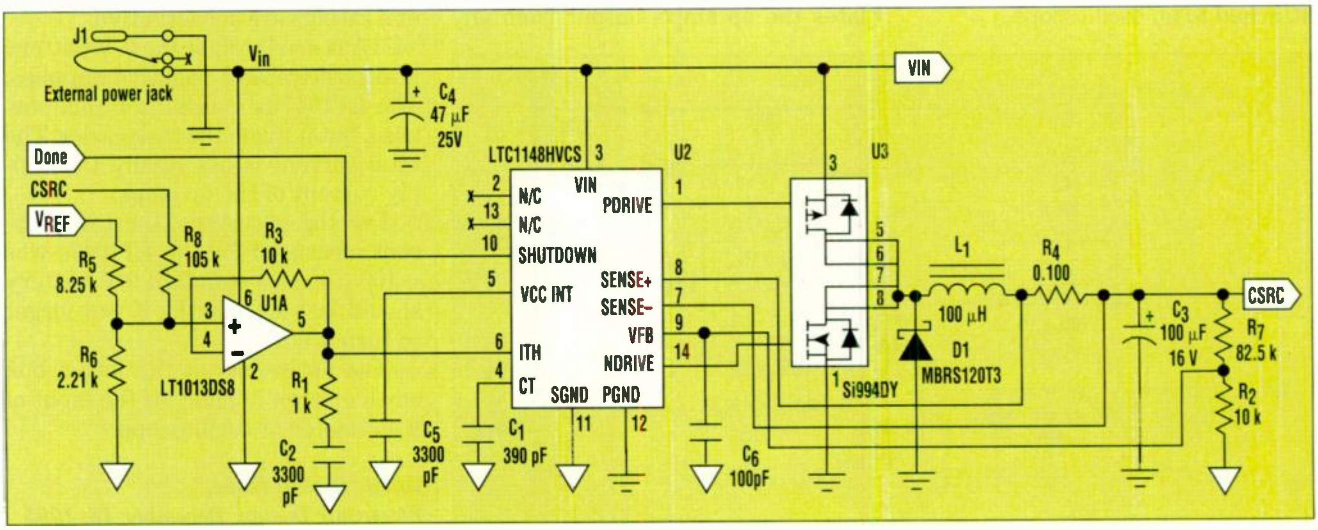
Instead, a switching regulator that could be set up as a constant current source was needed. This would bypass the current sensing of the MAX713 and eliminate its relatively larger current-sense resistor. Connecting the negative end of the battery directly to ground provides more voltage and reduces IR losses.

Linear Technology's LTC1148HV synchronous step-down switching regulator seemed to fill this role because it's more than 90% efficient, it features two current sense inputs (Sense+ and Sense–), and a current control pin (I_{th}) that has a dc input linearly related to the maximum coil current (*Fig. 1*).



2. BECAUSE IT'S pin programmable and doesn't require software development, the MAX713 charging controller was used in the development of small, efficient battery chargers that could charge 2 to 10 NiCd or NiMH cells.

For example, with a low, commonly available 0.1 Ω sense resistor and I_{th} connected to the 2-V reference output of the MAX713, the peak coil current is set to 1.55 A. The average current will still vary with output



1. THE LTC1148HV SYNCHRONOUS STEP-DOWN switching regulator was found to be the best fit as a constant current source for the MAX713 charging controller.

voltage, but this can be compensated for by feeding back some of the output voltage to I_{th}. A spreadsheet can help calculate the values of resistors R5, R6, and R8 for the desired current level and linearity.

The constant-voltage regulation loop of the LTC1148 is disabled once the voltage divider (R2 and R7) for VFB is set above the highest voltage that the battery is going to reach during charge.

With the battery above the constant voltage regulation point, the switching regulator will supply no current.

If a trickle-charge current is desired, a switch (U5A) and a resistor (R14) can be added that supply the desired current directly from the primary dc source (V_{in})—a simple wall cube—when the MAX713 controller terminates fast charge or during battery undervoltage condition at startup.

Some other important aspects of the MAX713 that should be kept in mind (*Fig. 2*):

- The NC switch in J2 detects if no battery is plugged in and disables the switching regulator through the shutdown input.
- Diode D2 indicates if power is applied, while D3 signals if the charger is in the fast mode.
- Connecting PGM0 and PGM1 to the proper voltage selects the number of cells to be charged; PGM2 and PGM3 select the maximum charge time.
- Upon timeout or dV/dT detection, FASTCHG goes inactive, which disables the switching regulator through the Shutdown pin, turns the green LED off, and turns the trickle-charge switch on.
- Thermistor voltage dividers can be added to the TEMP, THI, and TLO pins of the MAX713 to provide temperature trip points.
- The maximum number of cells (10) is limited by the maximum V_{in} of the MAX713 and the LTC1148, which is 20 V. With a larger number of cells, ripple voltage on V_{in} becomes a limiting factor.
- To make L1 as small as possible, the switching frequency of the LTC1148 can be set as high as 250 kHz.

The circuit is optimized for charging six cells at 400 mA. It has a timeout of 4.4 hours, a trickle charge of 24 mA, an open-circuit voltage of 11.5 V, a supply voltage of 12 V, and a switching frequency of 125 kHz.

Voted "Best of Issue,"
Electronic Design, May 15, 1995

Measure Picoamperes With DVM

MARSHALL J. BELL, B.I. Instruments, 221 Kingslynn Rd., Stoughton, WI 53589; (608) 873-6449.

Many times, the need arises to measure current below 1 µA. The circuit shown helps along those lines, as it turns any voltmeter into a picoammeter with scales of 1 nA/V and 1 µA/V (*see the figure*).

By using a 3-1/2 digit voltmeter with a resolution of 1 mV, the readout will be in picoamperes or nanoamperes. In addition, it can be attached to an oscilloscope.

The frequency response is about 1 kHz for the 1 µA/V setting and 150 Hz for 1 nA/V.

Looking at the circuit, U1B forms a transimpedance amplifier. With S1 in the position shown, the transimpedance is 1 MΩ. In the other position, a gain of 1000 is added to make the total transimpedance 1 GΩ.

R1, C1, D1, and D2 protect the input from high voltages, and R5 isolates the op amp's output from any load capacitance.

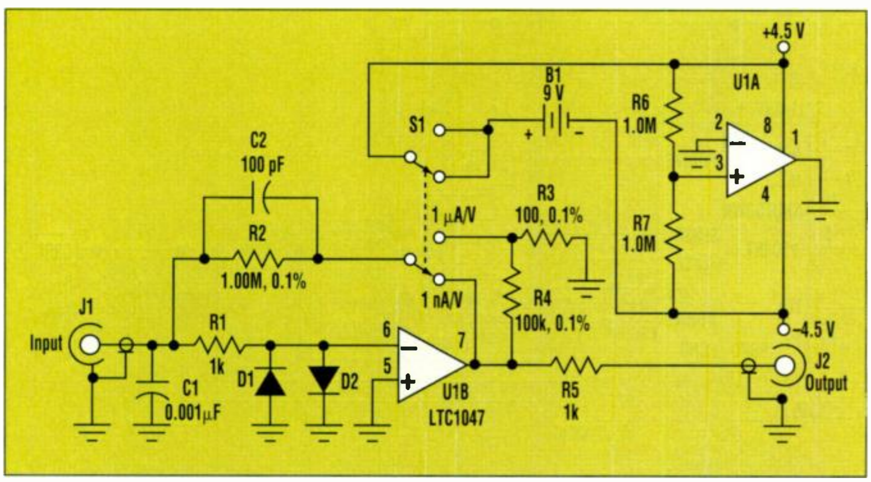
The op amp's input current and voltage offset must be low for this circuit to work. In this case, a Linear Technology LT1047 was used. It has a nominal input bias current of ±5 pA and a VOS of ±3 µV at room temperature.

Five units were tried and they produced an output of less than 1 mV in the 1 GΩ range, so the manufacturer's ratings are conservative.

U1A is used to split the 9-V battery into positive and negative supplies. The LT1047 is overkill for this purpose, but it made the task easier. The total current is essentially the supply current of the op amps.

For the prototype, the total current measured for the LT1047s was < 100 µA, so a standard 9-V battery should last six months if you forget to turn it off.

The entire circuit fits into a box small enough to hang off the input of a voltmeter or oscilloscope.



THIS PICOAMPERE PRECONDITIONER allows a digital voltmeter to evaluate photdiodes and the shutdown current of ICs.

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Feedback Improves Notch Filter Q

ERIC KUSHNICK, LTX Corp., LTX Park at University Ave., Westwood MA 02090-2306; (617) 461-1000.

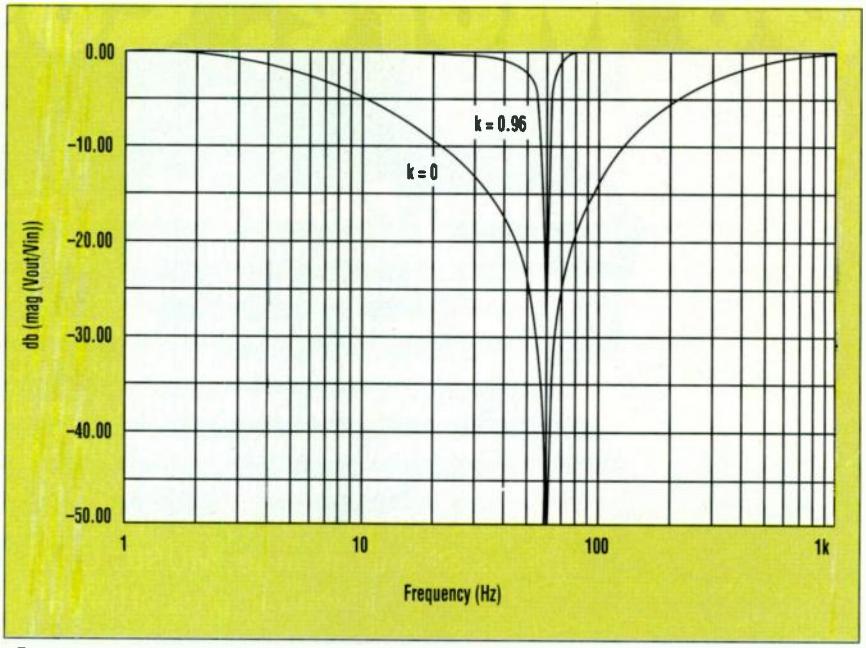
In Electronic Design's February 20, 1995 Ideas for Design section, a high Q bandpass/band-reject filter is described (see *"Tunable Filters Cover Wide Range,"* p. 110). The filter does indeed have a very high Q as a bandpass filter, but as a notch filter, the Q is about 1/5 ($Q = F_{notch}/(BW \text{ at } -3 \text{ dB})$). However, the notch filter Q can be increased to almost any desired value by adding a little positive feedback.

The schematic illustrates a 60-Hz notch filter with positive feedback (*Fig. 1*). If the optional buffer is connected between points A and B instead of the short circuit, then the resistors determining the positive feedback (R4 and R5) are completely independent of the resistors determining the notch frequency and notch depth (R1, R2, and R3). In this case (with the buffer), the exact equations apply, and $F_{notch} = 1/(2\pi C\times(3\times R1\times R2)^{1/2})$, where R1 = R1A + R1B and C1 = C2 = C3 = C.

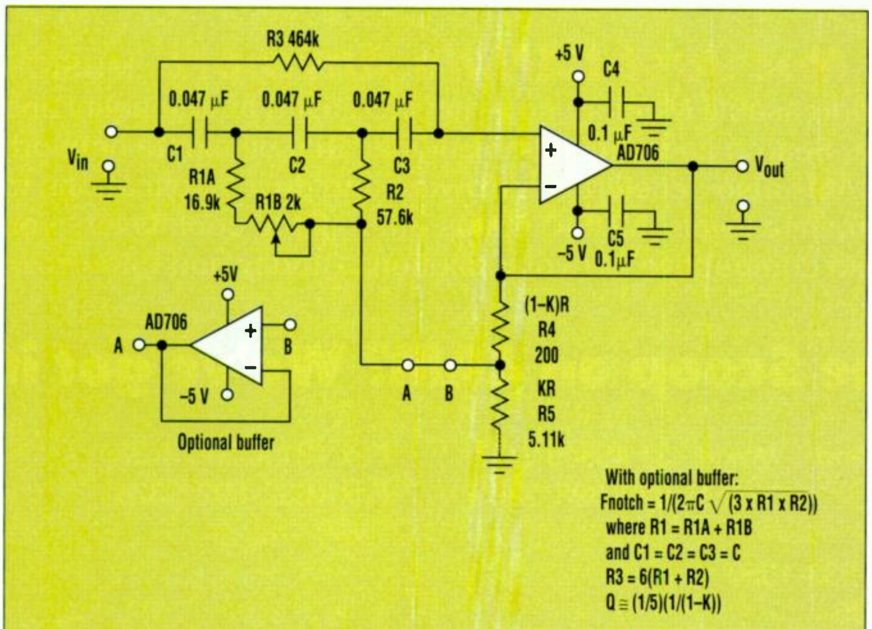
R3 determines the depth of the notch, and for the buffered case, the maximum notch depth occurs when R3 = 6(R1 + R2). The Q may be independently adjusted by varying the factor K, the ratio of R5 to (R4 + R5). The Q is approximately equal to (1/5) × (1/(1 - K)). In actual practice, however, the value of R4 often is much less than the values of R1, R2, and R3. In this case, the optional buffer can be replaced with the short circuit between points A and B. The equations for F_{notch}, Q, and R3 now are no longer exact, but a little tweaking of the values on a simulator can bring back the desired response. The values shown were optimized for the "no buffer" case in a short period of time.

The response of the bufferless circuit in Figure 1 is shown with K equal to approximately 0.96, and with K = 0 (to get K = 0, disconnect the top of R4 from the op amp and ground it) (*Fig. 2*). With K = 0.96, the Q of the notch filter is about 5.

By making R1 less than R2, small changes in R1 can affect the notch frequency much more than the notch depth, because the notch frequency depends on the product of R1 and R2, while the notch depth depends on the sum of R1 and R2. This allows the filter frequency to be easily adjusted for production variations in the values of the three capacitors, C1, C2, and C3, which helps reduce the effect of production variations and makes the filter easy to produce.



2. THE NOTCH FILTER'S RESPONSE, with K=0.96, shows a Q of about 5.



1. BY ADDING POSITIVE FEEDBACK, a notch filter's Q can be increased to almost any desired value.

Voted "Best of Issue," Electronic Design, Februay 19, 1996

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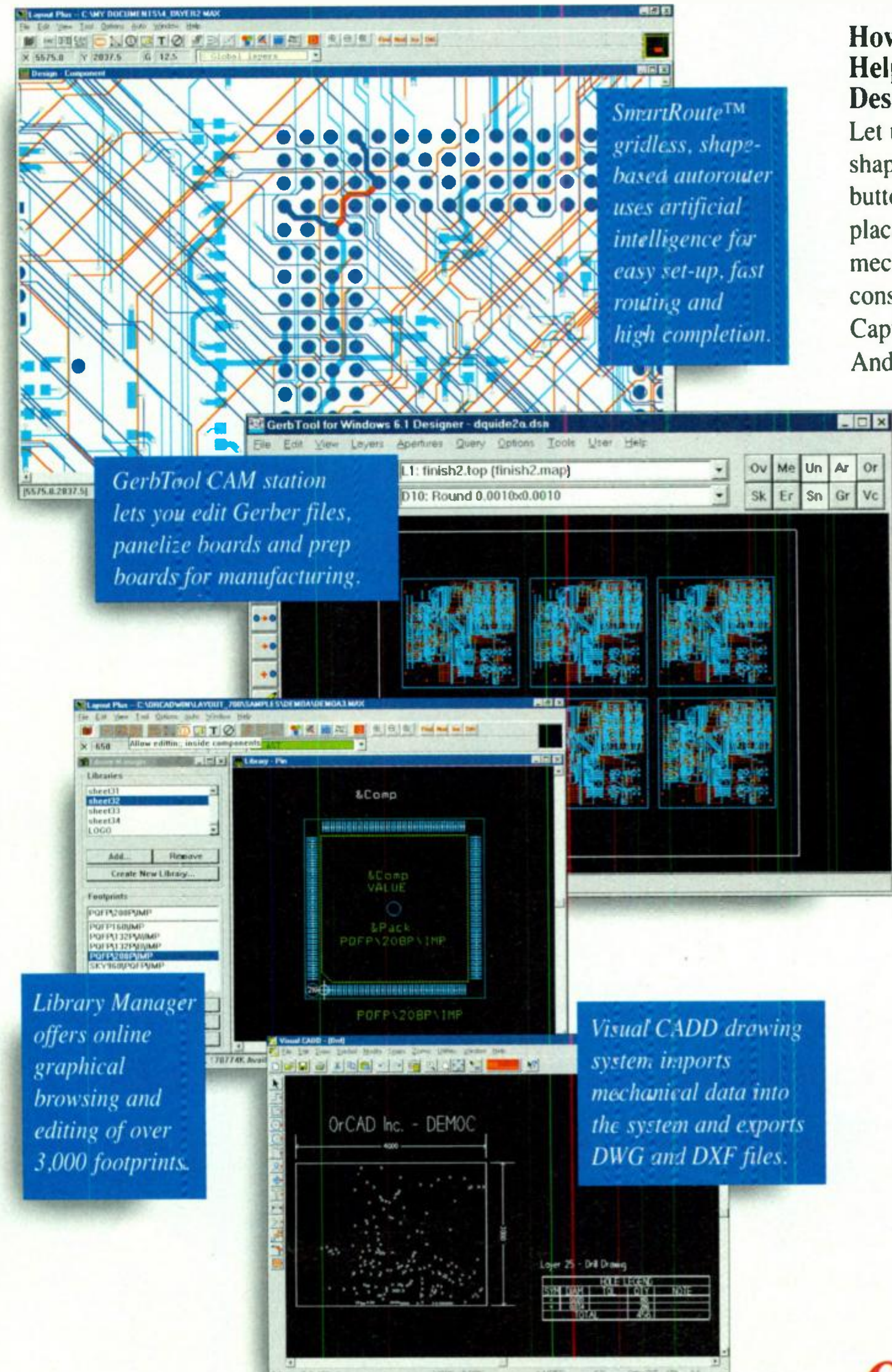

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Transformer-Less DC-DC Converter

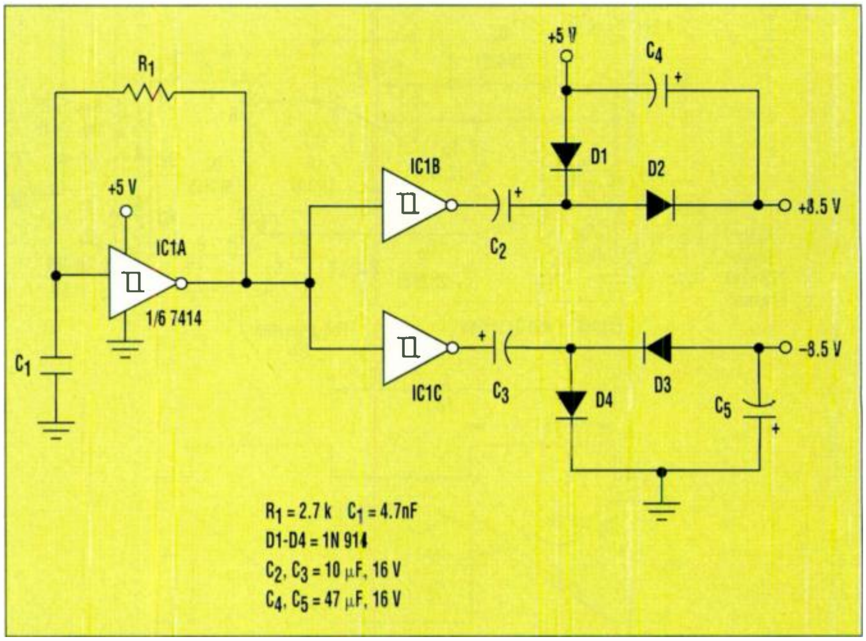
V. LAKSHMINARAYANAN, Centre for Development of Telematics, Sneha Complex, 71/1 Miller Rd.,Bangalore-560 052, India.

This configuration should prove handy in situations in which dual- polarity supplies are needed for a few devices on a board that has only one +5-V supply. The circuit doesn't use any dc-dc converter ICs, nor does it require any transformers or inductors. Three Schmitt-trigger inverters, such as the 7414, form the heart of the circuit (see the figure). One inverter is configured as a high-frequency astable multivibrator emplo-ying a single resistor and a capacitor. For the RC values shown, the frequency of the astable output is around 100 kHz. The oscillation frequency is given by f = 1/T, where:

$T = R1C1 \ln[(1 - V_{CC}/V_{LT})/(1 - V_{CC}/V_{UT})]$

where R1 and C1 are the timing components of the astable, V_{CC} is the supply voltage, and V_{LT} and V_{UT} are the lower trip point and upper trip point of the Schmitt trigger (in this circuit, V_{LT} = 0.9 V, V_{UT} = 1.7 V, and V_{CC} = 5 V, because standard TTL is used).

The astable's output drives a pair of inverters that, in turn, drive a pair of diode-capacitor voltage-doubler circuits. The outputs of the diode-capacitor circuits are around 8.5 V with the polarities shown. Diodes D1-D4 should be fast-switching types like the 1N914 or 1N4148. As a result, the circuit can generate ±8.5 V from a single +5-V supply, making it useful in many applications. Because the device doesn't have any coils or transformers, it saves pc-board space and reduces cost.



WHEN SEVERAL DEVICES on a pc board require dual-polarity supplies and there's only a single +5-V supply, this circuit may be useful. It has no dc-dc converter chips, no transformers, nor any inductors.

Voted "Best of Issue,"
Electronic Design, October 13, 1995

Portable Airspeed Measurement

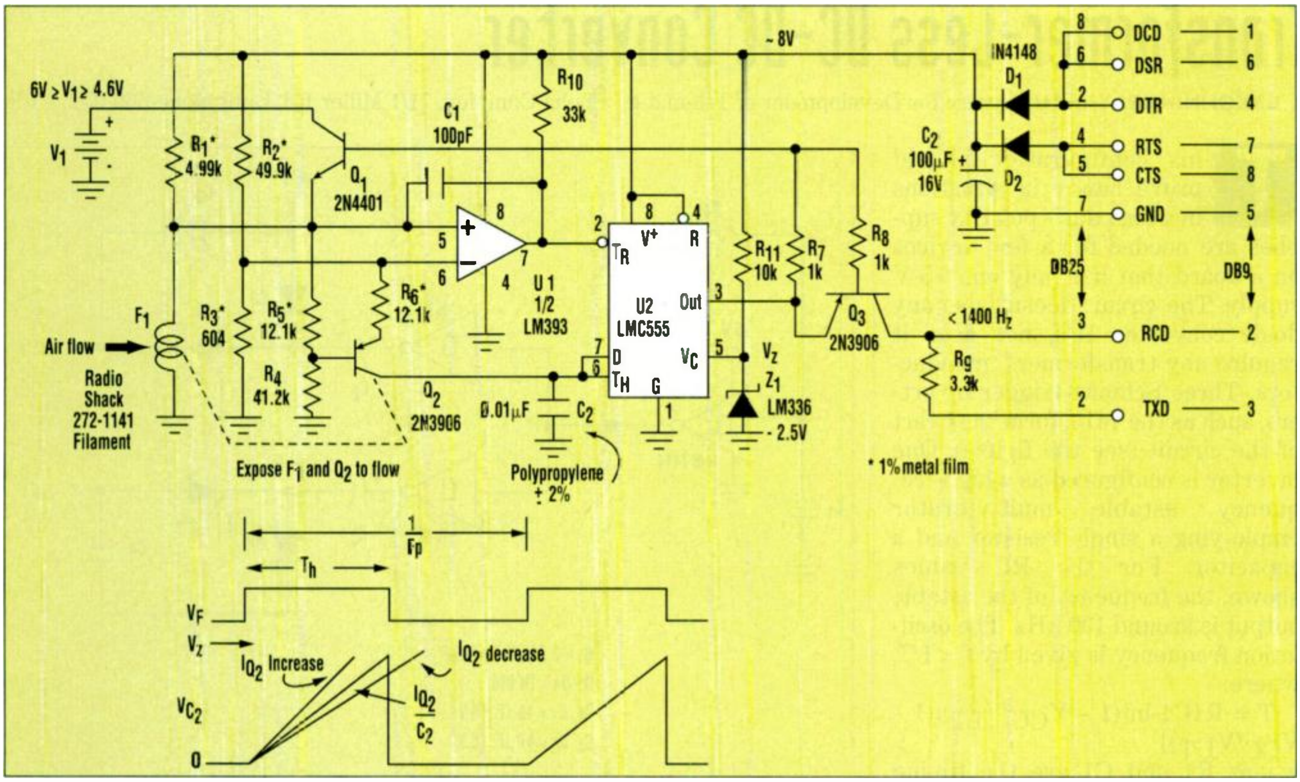
W. STEPHEN WOODWARD, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvxl.oit.unc.edu.

Computer-compatible airflow instruments are widely available but are usually expensive, bulky, and mechanically fragile. This anemometer continuously converts airspeed in the range of zero to tens of meters per second into an RS-232-compatible data stream while overcoming those drawbacks. It's battery-powered and, when combined with a laptop or notebook PC, consists of a fully portable airspeed measurement system.

The anemometer's principle of operation is that of the familiar constant temperature hot-wire anemometer. In this case, the relationship between electrical resistance and the temperature of tungsten wire is used to monitor and regulate the temperature of a heated filament exposed to the airflow. The power needed to maintain a constant difference between ambient and filament temperatures then can be used to directly calculate airspeed via "King's Law." The law states that the rate of heat loss is proportional to the temperature differential between air and filament, multiplied by the square root of airspeed.

In this version (*see the figure*), comparator U1 monitors the ratio of the resistance of filament F1 (a denuded Radio Shack #272-1141 incandescent lamp) to reference R3. Whenever Rw < R3/R10, U1 triggers timer U2 to apply heating pulses from battery V1 to F1 via Q1. The result is to maintain a constant filament temperature of approximately 250°C.

The average power dissipated in the filament is given by: $F_p \times T_h \times V_w^2/Rw$, where F_p = pulse frequen-



THIS ANEMOMETER continuously converts airspeed, ranging from zero to tens of meters per second, into an RS-232-compatible data stream.

cy, T_h = heat pulse duration, V_W = pulse amplitude at the filament, and Rw = filament resistance. Th is generated by a linear timing ramp produced by Q2's collector current as it charges C2 to U2's threshold voltage. Because Q2's collector current is made proportional to V_W^2 and to ambient temperature, T_h is inversely proportional to these factors. This feature compensates the quantum of heat delivered by each pulse against variations in battery voltage and air temperature, and keeps F_p proportional to the square root of airspeed. Maximum F_p (corresponding to 20 meters/s) is 1370 Hz.

Each filament heating pulse causes Q3 to transmit an RS-232 start bit to the COM port (formatted for 9600 baud, 1 start, 1 stop, 5 data, and no parity bits) of the connected computer. A simple software routine tallies these pulses and averages their frequency. Subtraction of an empirically derived zero offset from the average, squaring, and normalizing it with a suitable scaling constant produces the final airflow measurement.

Battery life is extended by applying filament power only when the COM port is "Open" and by the wide range of battery voltage (4.6 to 6 V) compatible with the accurate anemometer operation. As the battery finally does reach end of life and V_W drops below 4.5 V, T_h becomes longer than 677 mus (the longest start bit compatible with COM-port framing requirements). The resulting "framing error" provides a reliable "low battery" warning.

Voted "Best of Issue," Electronic Design, January 22, 1996

Optically Isolated Precision Rectifier

W. STEPHEN WOODWARD, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvxl.oit.unc.edu

Isolation amplifiers and precision rectifiers are widely available functions. With this circuit, both functions can be combined in one topology (*see the figure*). It achieves excellent rectification symmetry and zero stability, and good linearity (better than 1%) and frequency response (>10 kHz), with a minimum of precision components.

A1 acts as a voltage-to-current converter by servoing the current through the D1-D4 bridge and L1. Therefore, the voltage developed across R1 equals the instantaneous input voltage. The diode bridge's full-wave rectification causes L1 to be forward-biased regardless of the polarity of the input voltage. The magnitude of the bias controls the intensity of optical coupling between

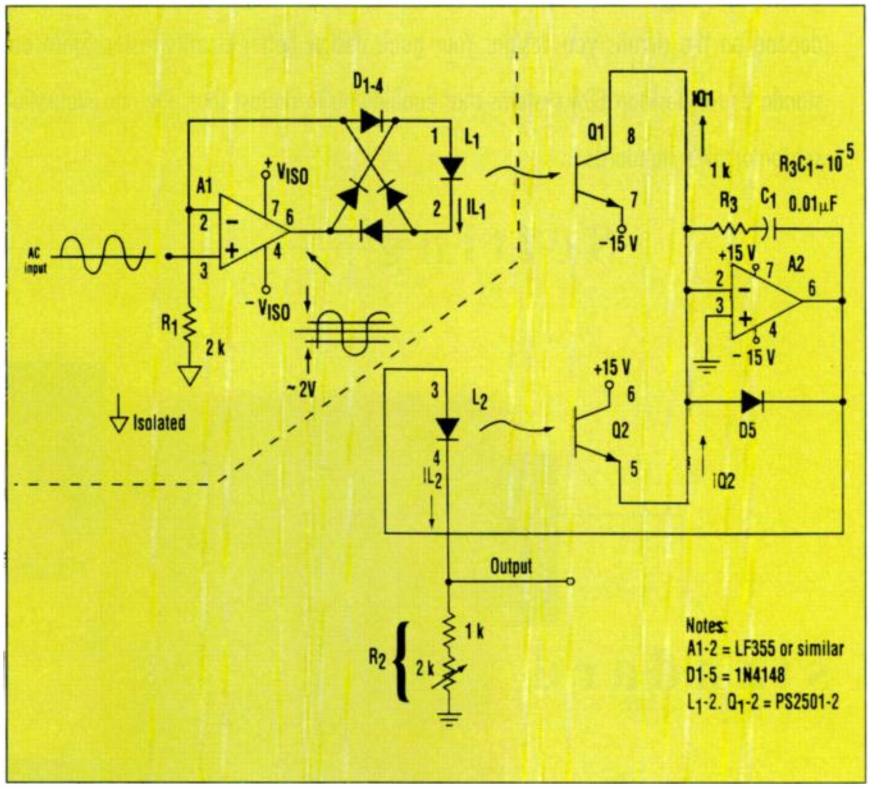
L1 and Q1, and, thereby, the magnitude of Q1's collector current.

A2 servos the current through L2 and R2 so that the current passed by Q2 balances that passed by Q1. Because of the good tracking of elements of the PS2501-2 dual optoisolator, a constant ratio exists between L1 and L2 currents. Consequently, R2 can be adjusted so that the output voltage across R2 is equal to the rectifier's isolated input voltage.

R3 and C1 provide frequency compensation for the L2-Q2 feedback loop. D5 prevents potentially destructive reverse bias of L2.

If the input voltage range is very large compared with the forward drops of D1-D5 and L1, such as when the 120 V ac mains must be monitored, A1 can be eliminated and the input voltage simply applied directly to the bridge, optoisolator, and suitable R1. All the while, good accuracy is maintained. Moreover, in this instance, the need for isolated dc power supplies for the isolated op amp would also disappear.

Voted "Best of Issue," Electronic Design, June 12, 1995



AN ISOLATION AMPLIFIER and precision rectifier can be combined in one topology, as demonstrated here. Only a handful of precision components are required to attain its zero stability, better than 1% linearity, and excellent rectification symmetry.

Linear DAC Has Nonlinear Output

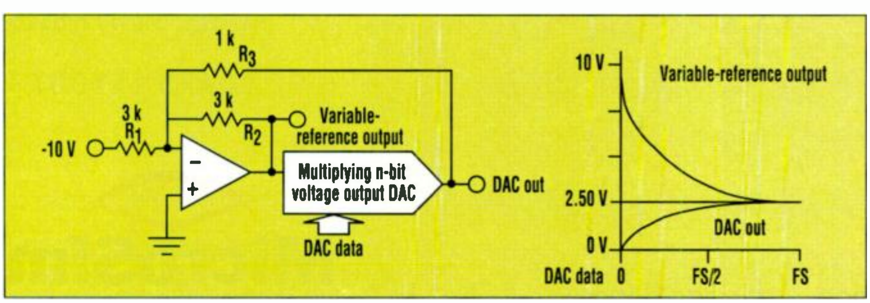
CHARLES G. BAGG, 17 Drake Rd., Fitchburg, MA 01420; (508) 342-7603.

When controlling a nonlinear device such as an incandescent lamp, it is desirable to have fine resolution at the high end, where a small change in current may cause a large change in brightness. At the low end, where the filament is not even glowing, coarser resolution is quite adequate. Log DACs are available, but they have their fine resolution at the wrong end.

Using the simple circuit shown (*Fig. 1*), any desired compression can be produced using just about any multiplying DAC. A negative 10-V reference is fed through R1 to inverting amplifier A1, which has an initial gain set to unity by R2. A1's output supplies a positive variable reference to the DAC.

The DAC output provides additional feedback through R3, reducing the amplifier's gain as the DAC data increases. (You can also think of A1 as a fixed-gain summing amplifier in which the DAC output is subtracted from the 10-V reference input). Either way, the variable reference is gradually reduced so that each step is progressively smaller than the one before.

With the values shown, as the DAC data approaches full scale, the reference approaches 1/4 of its original value. This gives the output four times as much resolution at the high end as at the low end. By decreasing the value of R3, greater compression and higher resolution can be achieved. The



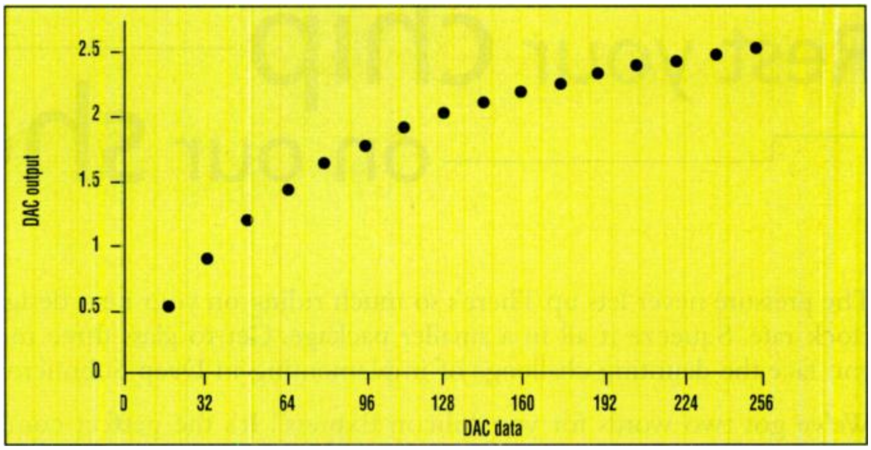
1. WHEN CONTROLLING A NONLINEAR device, this circuit can produce any desired compression using just about any multiplying digital-to-analog converter.

variable-reference output also may be useful in some applications.

The math is surprisingly simple. Since the DAC feeds back a fraction of the variable reference voltage to R3, it multiplies the effective value of R3 proportionally. Therefore, the equivalent resistance, R_E, equals R3 times (DAC resolution/DAC data). The parallel resistance of R2 combined with R_E equals ($R2R_E$) / (R2 + R_E), which we'll call R_P. The gain of A1 now is simply R_P/R1.

For a quick approximation, remember that when the data is zero, resistor R3 is out of the circuit. When the data is all ones, the DAC is practically a straight piece of wire, so that R_E is approximately equal to R3. The step size is always the variable reference divided by the DAC resolution.

It's easy to set up a spreadsheet with a series of values for the DAC data and plot the results (Fig. 2). Then the resistor values and reference voltage can be adjusted to get the desired compression.



2. BY MIXING AND MATCHING the resistor values for the DAC and the reference voltage in a spreadsheet and plotting the results, the proper amount of compression can be obtained. Here, an 8-bit DAC was used.

Voted "Best of Issue," Electronic Design, April 17, 1995

Single Comparator Window Detector

JOSEPH V. D'AIRO, 424 Higbie Ln., West Islip, NY 11795; (516) 661-1694.

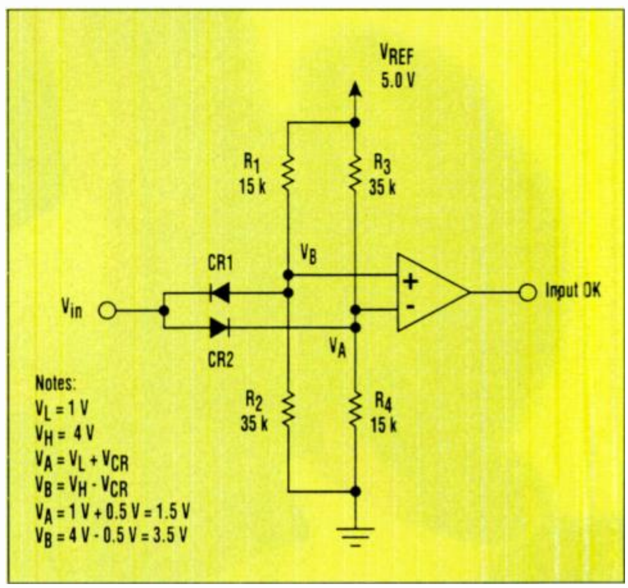
Simply by adding two steering diodes, a window detector can be built using only a single comparator. The detector performs well for windows of about 1 V or greater, but it isn't suitable where extreme precision is required because the forward drops of the diodes vary.

In the basic circuit (Fig. 1), two resistive dividers set threshold voltage levels at both the inverting and noninverting inputs of the comparator by dividing the reference voltage. The input voltage is steered to the appropriate comparator input by diodes CR1 and CR2.

When the input voltage is within the window, neither diode conducts, and the comparator is biased for a High output. When the input goes above the window, CR2 conducts and pulls the inverting input high, causing the comparator output to go Low. When the input voltage goes below the window, CR1 conducts, pulling the noninverting input low, again causing the comparator output to go Low. The source resistance of V_{in} must be low compared to the equivalent parallel resistance of each divider. That's because the conducting diode must "pull" its divider until its voltage level crosses the threshold set by the opposite divider.

The diode forward drops must be considered when setting the threshold voltages. The lower-limit threshold voltage, V_A, is set one diode drop above the required lower limit, while the upper-limit threshold, V_B, is set one diode drop below the upper limit. In this example, the reference voltage is 6.0 V and the window is selected to extend from 1 to 4 V. At low current levels, the diode forward drops are about 0.5 V, so the thresholds are set to 1.5 and 3.5 V, respectively.

One typical application for the detector involves monitoring a lead-acid battery (*Fig. 2a*). It indicates a fault when the battery voltage is out-



1. A WINDOW DETECTOR that uses only a single comparator can be constructed if two steering diodes are added. Due to varying forward drops of the diodes, it's best to use the circuit in aplications with windows of about 1 V or greater.

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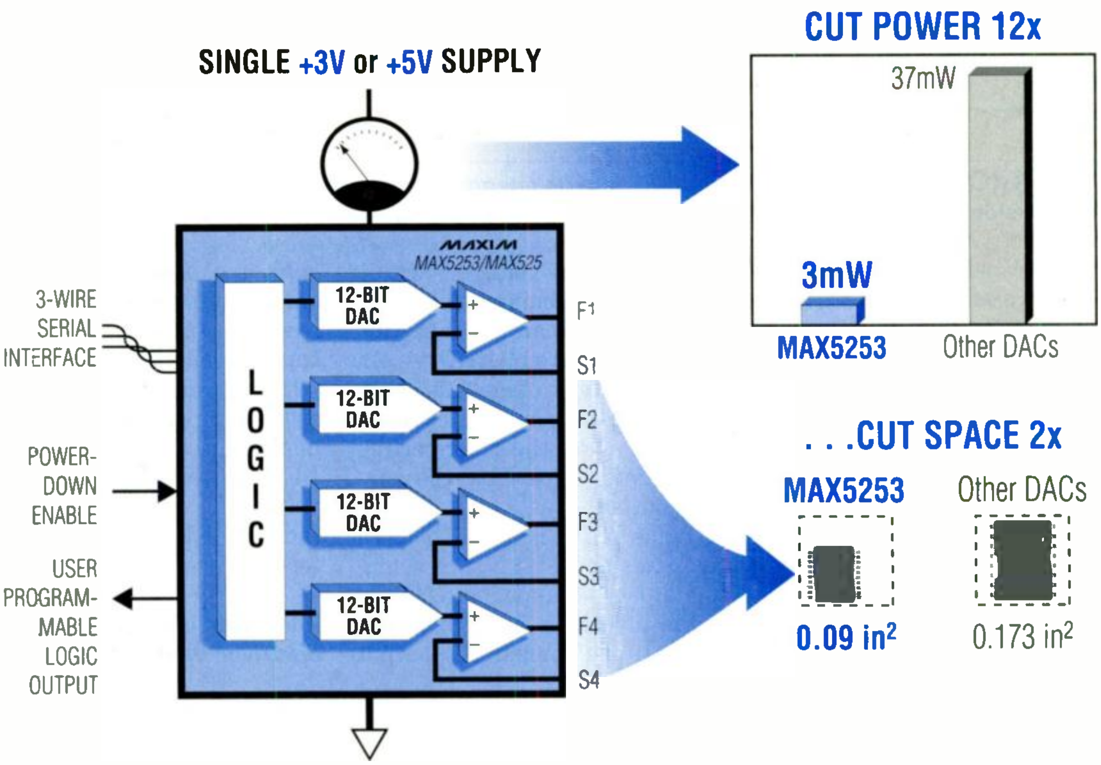

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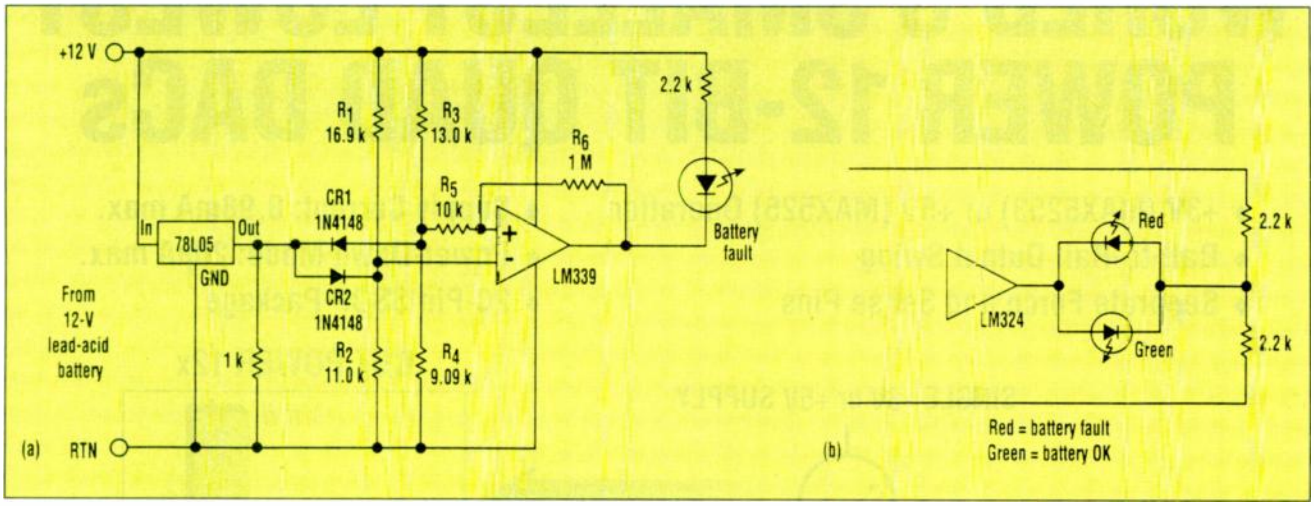

2. ONE APPLICATION for the window detector is as a lead-acid battery monitor (a). It indicates when the battery voltage is outside an 11-to-14-V window. LEDs can be used if an op amp such as the LM324 is the comparator (b).he

side an 11-to-14-V window. Because the circuit is powered by the battey, the input and reference were switched to keep the comparator inputs within its common-mode range.

The circuit's reference is 5.0 V. The resistor values in divider R1/R2 were selected to produce 5.5 V at the inverting input when the battery voltage is 14.0 V. Divider R3/R4 is set to produce 4.5 V at the noninverting input when the battery voltage is equal to 11.0 V.

When the battery voltage is within the window, the noninverting input is more positive than the inverting input and the output LED is off. When the battery voltage falls below 11 V, the inverting input is clamped at 4.5 V by CR2, the noninverting input continues below that, the comparator output goes Low, and the LED turns on. When the battery voltage rises above 14 V, the noninverting input is clamped at 5.5 V by CR1, the inverting input continues above that, the comparator output again goes Low, and the LED turns on. Resistors R5 and R6 show that hysteresis may be added to this circuit in a conventional manner.

If an op amp like an LM324 is used as the comparator, two LEDs can be implemented *(Fig. 2b)*. The green LED will turn on when the battery voltage is within the window, and the red LED turns on when the battery voltage is outside the window.

Voted "Best of Issue," Electronic Design, January 23, 1995

Single-Supply Summing Amplifier

ALEX BELOUSOV, Standard Motor Products Inc., 37-18 Northern Blvd., Long Island City, NY 11101; (718) 392-0200.

This circuit produces an output that is the absolute value of the sum of two analog input signals, V1 and V2. The circuit *(see the figure, a)* consists of two amplifer stages, shown within the dashed boxes, which are included in the rail-to-rail dual op amp TLC2272, used in a single-supply mode. (Other rail-to-rail op amps also can be used.)

The output of summing amplifier U1A, at terminal 3, is a high-impedance output, while the optional output amplifier, U1B, offers a low-impedance output at terminal 4.

The equivalent circuit is shown in part b of the figure. With the assumption R1 = R2 = r, the two basic equations are:

(1) For $(V_1 + V_2) \geq 0$, the output voltage, V_{out}, is:

$V_{out} = (V_1 + V_2)R4/(r + 2R3 + 2R4)$

(2) For $(V_1 + V_2) < 0$, then:

$V_{out} = -(V_1 + V_2)R3/r$

$= -(V_1 + V_2)K$

where $K = R3/r$ (the expression for standard inverting amplifier gain.)

To provide the symmetry of transfer function for both input polarities, the right-hand parts of both equations must be equal:

$K = R3/r = R4/(r + 2R3 + 2R4)$.

After simple mathematical manipulation, the equations become:

$R4 = R3(1 + 2K)/(1 - 2K)$.

The last expression, taken with the previous assumption that (R1=R2=r=R3/K), defines the main relationship between resistors R1 to R4, needed to assure proper operation of the summing amplifier.

Note that if K = 1/4, the resistor ratio will be as shown in the figure, part a. If we define a basic resistance as R, then the relationships between the resistors are:

R3=R; R1=R2 =4R; R4 =3R.

It is important to note that the absolute values of the resistors do not matter; the values need only be "ratio-matched." Thus, any standard low-cost resistive network will be applicable.

The output terminal 3 may be connected directly to a digital multimeter or analog-to-digital converter with high input impedance. For bet-

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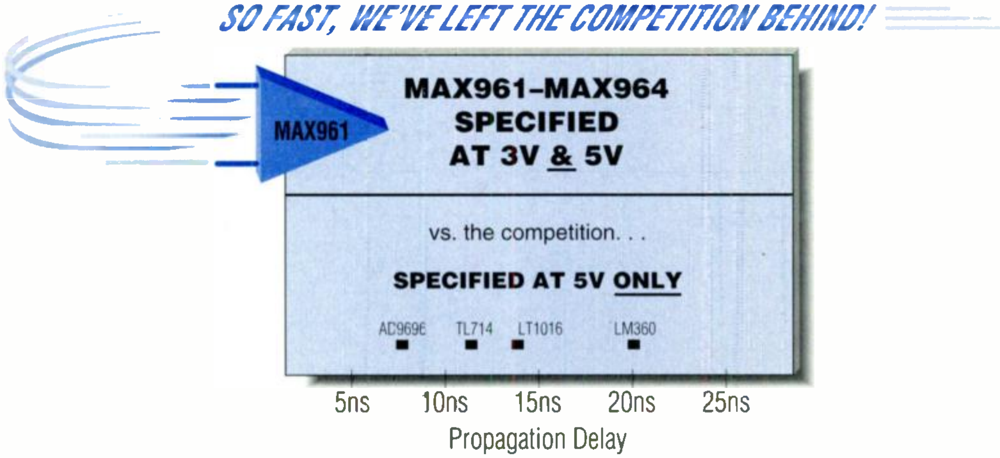

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MAX962	2	0.5	CMOS	No	+2.7 to +8	8	7
MAX963*	2	0.5	CMOS	Yes	+2.7 to +8	11	7
MAX964*	4	0.5	CMOS	No	+2.7 to +8	8	7

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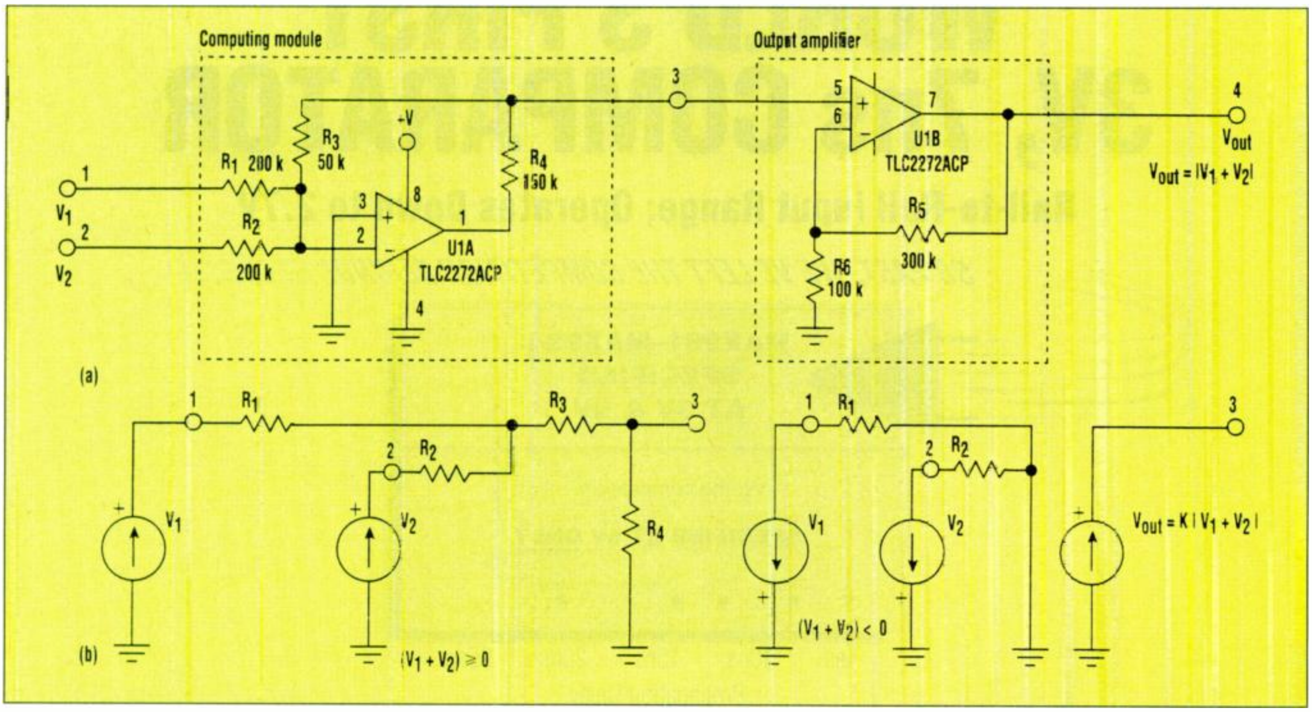

THE ABSOLUTE VALUE of the sum of the two input voltages is developed by the first stage of this circuit (a). The second-stage amplifier provides impedance matching and additional gain. The equivalent circuits (b) are used to analyze the overall circuit.

ter impedance matching, the additional noninverting output amplifier is recommended.

The optional amplifier provides impedance matching and produces an additional gain of (1+R5/R6). If R5 is set equal to 3R6, unity gain of the whole amplifier is obtained. Consequently, the circuit returns the absolute value of the sum V_1+V_2 of the input voltages.

However, all practical op amps introduce errors. In this application, the most critical dc error source is the parasitic positive voltage on pin 1 of op amp U1A when V_1+V_2 is greater than 0. In an ac mode, the input capacitance of U1 defines the frequency bandwidth.

When the values of resistors are as is shown (*see the figure, a, again*), the frequency range measured at the -3-dB points spans from dc to 20 kHz. To obtain a wider frequency range, lower resistances for R1 to R4 must be used. Also be aware of the possible nonlinear distortion, which could result from variations in the input capacitance of op amp U1 with changes in input voltage.

Voted "Best of Issue," Electronic Design, January 23, 1995

Eliminate Periodic Noise

W. STEPHEN WOODWARD, Venable Hall, CB3290, Univ. of North Carolina, Chapel Hill, NC 27599-3290;
Internet: woodward@uncvxl.oit.unc.edu

The intrusion of periodic noise (for example, 60-Hz "hum") into electronic circuits seems inevitable, particularly when high-impedance, low-level signals are involved. The dominant mode of noise induction in such situations is capacitive. Because capacitive induction emphasizes high frequency noise components, 60-Hz-related noise is likely to be heavy in harmonic content and extremely nonsinusoidal. For this reason, purely analog "notch" filters are limited when cleaning up corrupted signals.

This analog/digital synchronous-averager circuit (*see the figure*) implements a robust "comb" filter that (theoretically) infinitely attenuates all 60-Hz harmonics. It does this independently of precision component tolerances and with a transient response ideal for use with analog/digital converters. Signal components with frequencies below 20 Hz are passed virtually undisturbed.

In the circuit, A1 continuously integrates and inverts the sum of the input signal and the output of buffer amplifier A2. Depending on the state of FF2, either switches S1A and S1B (FF2 = 0) or S1C and S1D (FF2 = 1) will conduct. In the former case, the A2 buffer's input comes from the voltage stored on capacitor C3, while C2 tracks A1. In the latter case, the roles of C2/C3 are reversed.

Because flip-flop FF2 toggles once each 60-Hz cycle, A1 always integrates the difference between the instantaneous input voltage and the

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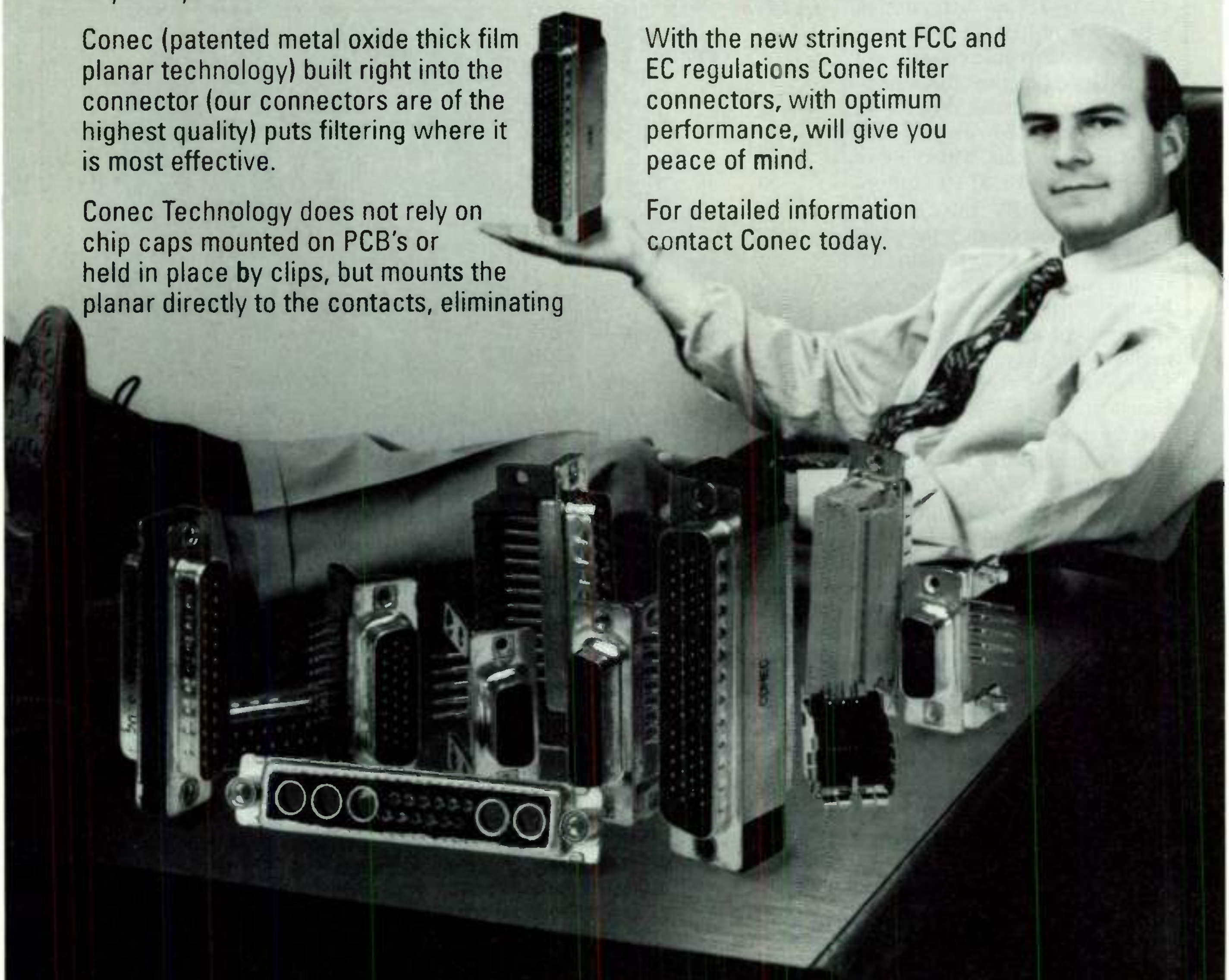

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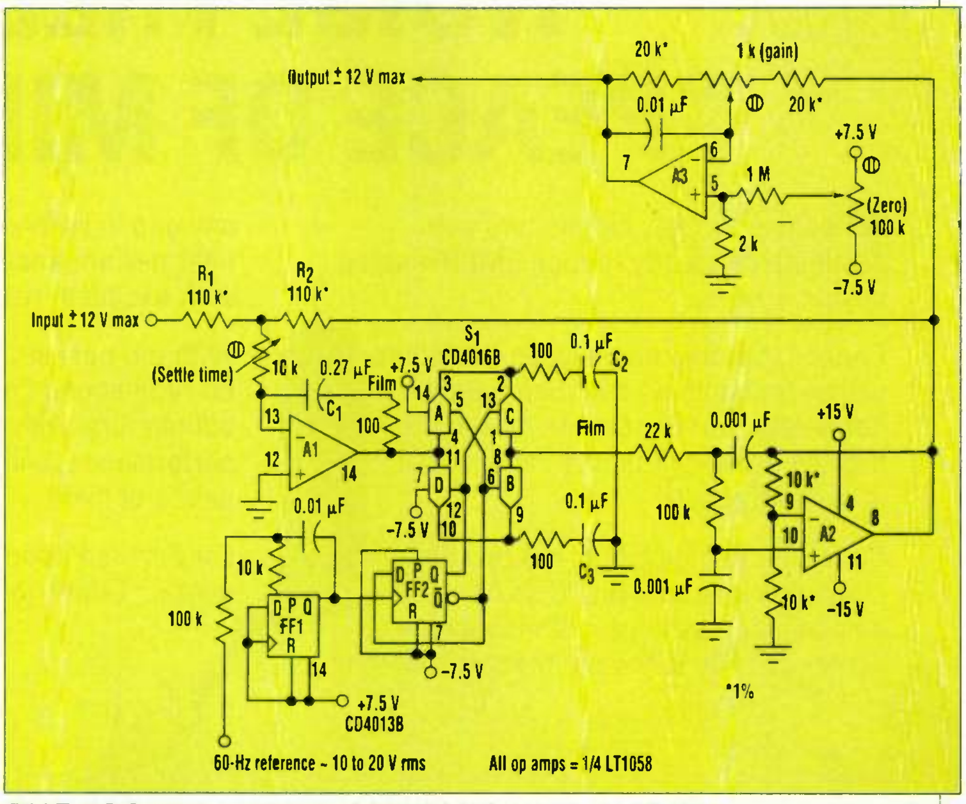
integral of the input taken over the preceding cycle.

The transfer function of such a piecewise integration is well known. It's characterized by a series of impulses that occur at f (the fundamental frequency of the integration cycle) and at all integer multiples of the frequency f.

This extreme attenuation (greater than 10,000:1 in the prototype) of harmonic noise is *not* limited by component tolerances.

The filter's settling time for an input step, however, does depend upon the trimming of potentiometer P1. If P1 is properly adjusted, the filter's transient response to an input step will settle to better than 1% within one or two line cycles following the input step. Otherwise, a minor overshoot or undershoot may be observed. However, even then, the filter's transient response will be superior, for most purposes, to that of a linear analog filter of comparable complexity.



THE "COMB" FILTER IMPLEMENTED IN THIS synchronous averager infinitely attenuates all 60-Hz harmonics.

Optional unity-gain inverter A3 undoes the signal inversion performed by A1 and incorporates trimmer pots P2 and P3 for precise adjustment of overall filter gain and zero offset. The signal-processing function that results is dc accurate, noninverting, and virtually blind to 60-Hz related noise.

Voted "Best of Issue," Electronic Design, July 10, 1995

Low-Cost Step-Down Regulator

EUGENE E. MAYLE, R.L. Drake Co., 230 Industrial Dr., Franklin, OH 45005; (513) 746-4556.

An inexpensive and efficient discrete step-down voltage regulator can be built using a complementary transistor arrangement that uses both positive and negative feedback and is referenced to a Zener diode. A flyback conduction diode and a few passive components complete the circuit.

A general-purpose pnp audio output-stage transistor is chosen for Q1 (*see the figure*). In a common-emitter configuration, Q1 acts a "switch transistor" under the control of Q2, the "comparator transistor." The value of R2 is chosen low enough to quickly discharge the parasitics of Q1 during turn-off, ensuring fast switching. R5 is a precautionary element included as a base current-limiting mechanism for Q1. Q2, a general-purpose npn transistor, operates as a common-emitter in its positive-feedback mode and as a common-base amp in its negative-feedback mode. After initialization of power, bias resistor R1 provides base current to turn on Q2, which turns on Q1. This results in additional bias current flow

Input = 18.0 V, output taken at C3				
Output (V)	Load (ohms)	Ripple (mV p-p)	Ripple (kHz)	Efficiency (%)
12.54	1k	50	4	67
12.52	90.9	25	112	86.5
12.49	47.6	40	58	88.9
12.45	24.4	70	31	91.8
Input = 18.0 V, output taken at C4				
Output (V)	Load (ohms)	Ripple (mV p-p)	Ripple (kHz)	Efficiency (%)
12.53	1 k	58	0.8	67
12.46	90.9	1.5	--	86.5
12.37	47.6	1.5	--	88.4
12.20	24.4	1.5	--	90.4
Output taken at C3, load = 24.4 ohms				
Input (V)	Output (V)	Ripple (mV p-p)	Ripple (kHz)	Efficiency (%)
15.0	12.35	73	17.8	93.4
18.0	12.45	70	31.0	91.8
21.0	12.53	75	43.3	90.8

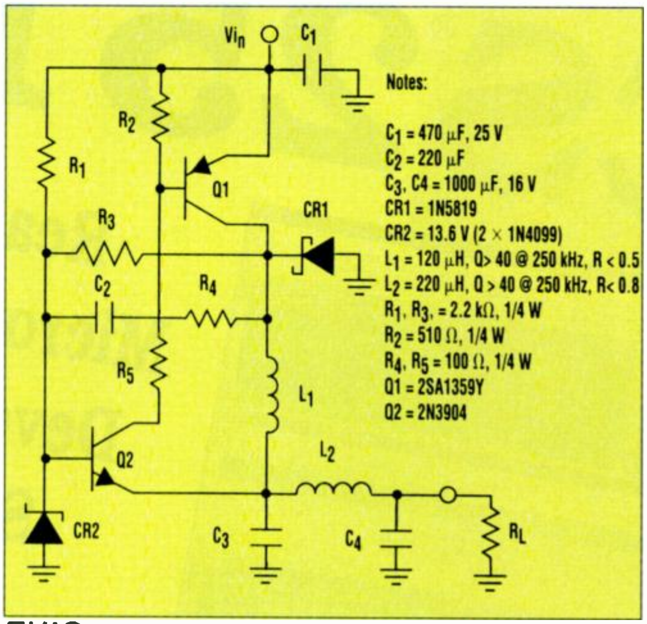
World Radio History

through network R3, R4, and C2. Thus, a positive-feedback loop is formed. Q1 and Q2 output currents ramp the voltage across C3. Zener diode CR2 eventually clamps the voltage at Q2's base while its emitter voltage at C3 continues to rise. Once Q2's V_{be} drop becomes sufficiently small, Q2 turns off Q1, completing the negative-feedback loop.

The back EMF generated by L1 forces Q1's collector negative, at which point it's clamped by Schottky diode CR1. The polarity of network R3, R4, and C2 becomes reversed and shunts current away from Q2's base, enhancing the turn-off. A regulated bias point now is established at Q2's emitter and across C3. Regulation involves charging C3 through L1, and the decay of C3 through the load. If there's insufficient current draw from the load, R3 will cause the output to stabilize at about 0.7 V high. At light loads, charging time is almost load independent while decay is directly dependent. Overshoot can occur due to fixed circuit-response delays and ripple frequency will be low.

At higher loads, the charge-to-decay-time ratio approaches 1:1, the ripple voltage approaches a minimum, and the oscillation frequency peaks. Still heavier loads require that L1 supply load current while charging C3, which increases the entire cycle--ripple frequency goes down and ripple voltage goes up.

Inductor L1 is selected to maintain the switching frequency above the audible range for the intended operating load. The output filter L2 and C4 reduces ripple to less than 10 mV p-p over a large range of loads, with only a slight decrease in efficiency.



THIS inexpensive and efficient discrete step-down regulator is based on a complementary transistor arrangement that employs both positive and negative feedback and is referenced to a Zener diode.

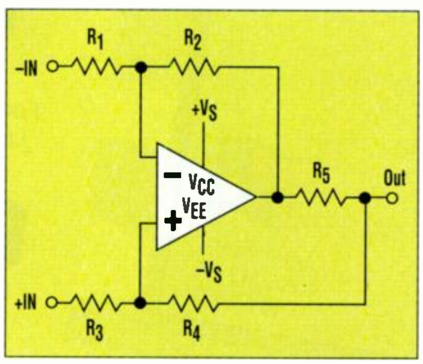
Voted "Best of Issue," Electronic Design, February 6, 1995

Positive Feedback Terminates Cables

JERRY STEELE, National Semiconductor Corp., Tucson Design Center, 940 Finance Center Dr., Suite 120, Tucson, AZ 85710; (602) 751-2380.

Positive feedback along with a series output resistor can provide a controlled output impedance from an op-amp circuit, with lower losses than would result from using an actual resistor. The circuit is useful occur when driving coaxial cables that must be terminated at each end in their characteristic impedance, which is often 50 Ω. Adding a 50-Ω series resistor on the op amp's output obviously reduces the available signal swing.

As can be seen in Figure 1, the circuit is an adaptation of the Improved Howland Current Pump, which is usually designed to maximize output impedance. It uses the positive feedback to provide a multiplication of the current sense resistor's value. For example, with R1 = R2 = R3 = 1 Ω, and R4 = 1.2 Ωs, the circuit supplies a 50-Ω output impedance with only 5 Ω of real resistance to lose voltage swing through.



1. **COUPLING** positive feedback with a series output resistor provides a controlled output impedance from an op-amp circuit, reducing losses that would otherwise occur with an actual resistor. The circuit is an adaptation of the Improved Howland Current Pump.

Adding positive feedback has the effect of multiplying circuit gain by the same ratio as it multiplies the sensing resistor (the example values given had a gain of about 10). Keep in mind that loading will cause the output voltage to drop to half (that's proof of the concept), so the loaded gain is half the unloaded gain. Available voltage swing remains essentially unimpaired. This can be a valuable feature, especially in low-voltage circuits like those used with National Semiconductor's LM7131. This part can provide 4-V pulses into a 150-Ω cable on 5-V supplies, but back termination would typically halve that. This technique maintains the full 4-V capability.

The circuit tolerates capacitive loads well, better than just the op amp alone. The inductive portion of any load is what could cause stability

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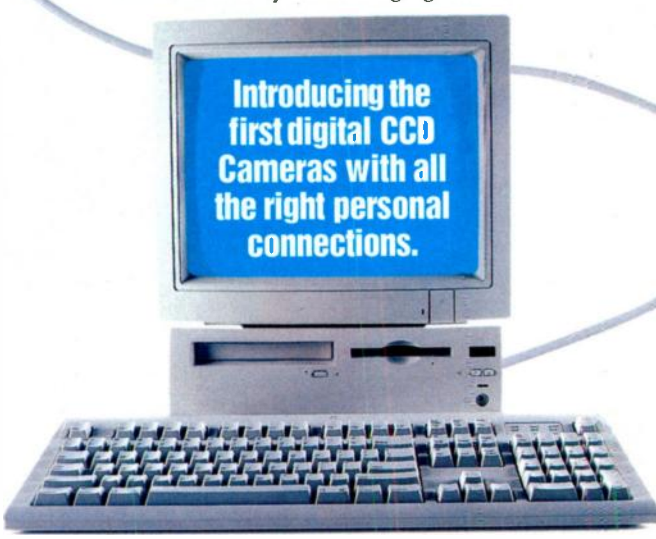

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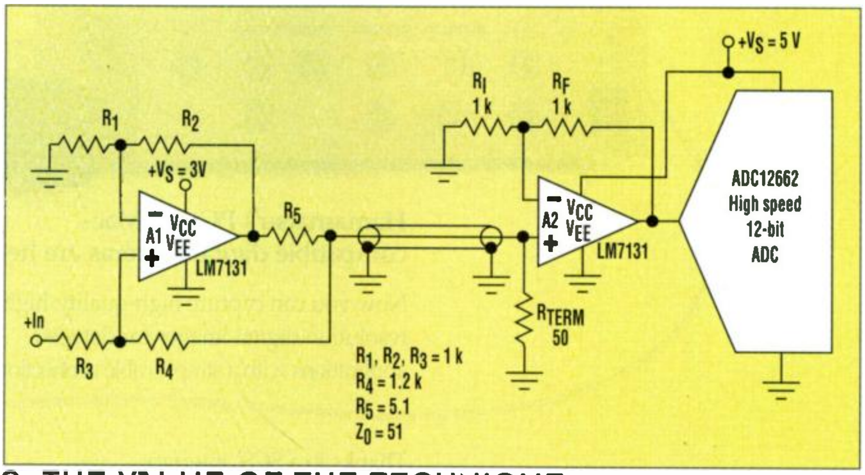
problems. Note that coax cable is a transmission line and isn't considered purely inductive or capacitive. Load inductance will manifest itself as overshoot in pulse response, if the overshoot is less than 40% of the total peak-to-peak amplitude of the pulse then the circuit has adequate phase margin.

Setting the desired gain involves pegging the values of the negative feedback resistors. Remember that the gain will ultimately be multiplied by an amount equal to what the series output resistor R5 is being multiplied. For convenience, the input leg of the positive feedback (R3) can be set equal to R1. The following equations solves for R4:

$$R_4 = \frac{\left(\frac{A_{ol}}{1 + A_{ol}[R1/(R1+R2)]}\right) . R_3}{1 - \frac{R_5}{Z}}$$

where Z is the desired output impedance. A_{ol} is the open-loop gain of the op amp.



2. THE VALUE OF THE TECHNIQUE demonstrated in Figure 1 is shown in this application, which uses National Semiconductor's LM7131 in a battery-operated piece of portable equipment operating at 3 V.

An example demonstrates the value of this technique (*Fig. 2*). A1 is National's LM7131 in a battery-operated portable device operating at 3 V. At the 3-V supply, the LM7131 is specified for a maximum swing of 2 V. Using positive feedback for back termination makes this entire voltage swing available. At the receiving end, another LM7131 provides gain to present a 0-to-4-V input to a high-speed 12-bit ADC.

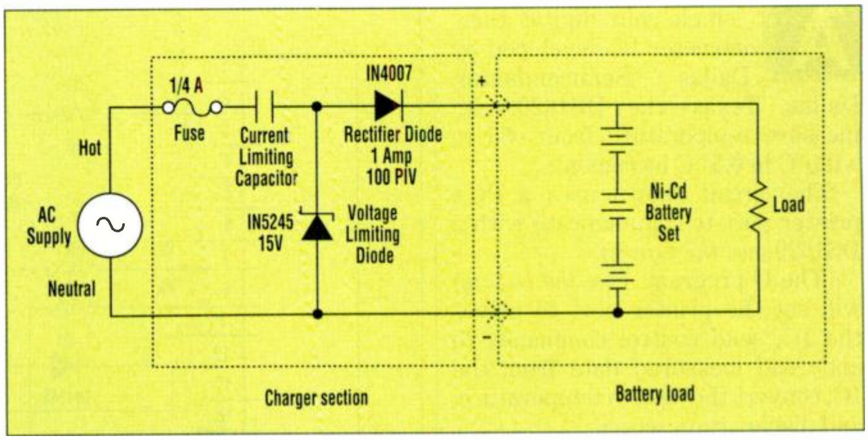
Voted "Best of Issue," Electronic Design, March 6, 1995

Charger Built With Few Parts

JOSEPH J. DENGEL, U.S. Merchant Marine Academy, Engineering Dept., Kings Point, NY 11204.

A battery charger for small NiCd batteries, which can be constructed using just four components, comes in handy as a lightweight and compact travel charger or in "floating" simple battery-backed projects. The circuit sacrifices isolation from the power line for a compact design. This lack of isolation requires the user to exercise prudence in the circuit's use. heed the notes mentioned below and ensure that circuit operation and the potential shock hazards are understood. As a travel charger for AA, C, or 9-V batteries, the circuit will usually fit inside a 35-mm film canister. A short ac plug comes out of one end and two small clip-leads from the other.

In the circuit *(see the figure)*, the capacitor is ac rated at 120 V ac with a value determined from the equation below. The fuse is selected to match the designed charging current/line voltage, and should not be above 0.25 A. The diode D1 rectifies the line voltage and diode D2 provides a discharge path for the capacitor, which bypasses the battery. D2 is a Zener diode that limits the open-circuit voltage between the two charging leads when there's no load present.



BUILT WITH JUST FOUR COMPONENTS, this charger for small NiCd batteries is useful as a compact travel charger or in "floating" simple battery-backed projects. It's small enough to fit in a 35-mm film canister.

Battery charging is based on average current flow. After selecting a desired charging current in amperes, the value of the capacitor (in farads) is computed from the equation:

$$C = (I_{avg} \times 0.0167)/340 \quad (1)$$

For example, AA NiCd batteries usually have a 0.5 amp-hr rating and an overnight charge rate of 10% as a rule of thumb. Charging current of 0.05 A results in a 2.5-µF capacitor.

Some other notes about the circuit:

1.The negative charging lead should be connected to the neutral conductor (wide blade on a polarized plug). Hotel wiring often is incorrect, so keep both charging leads, the batteries, the appliance, and yourself clear from external ground paths.

2.The charging leads may be short-circuited without damage and any reasonable number of batteries can be charged in series without affecting the average charging current. When not in use, the circuit should be unplugged.

3.The Zener-diode voltage rating should be set slightly above the highest voltage for the battery array. Its wattage rating can be approximated by:

$$P_d = I_{avg} \times V_z \quad (2)$$

4.The Zener diode is the only component that may dissipate any power; it should be liberally sized, especially if the final circuit will be completely enclosed.

5.Batteries may be charged while still installed in the tape player or radio (convenient because a separate battery holder isn't required). Use caution to prevent an open circuit in the battery path, or else the charging voltage will pulse at a value determined by the Zener. This may not be beneficial for the appliance if it's turned on or is in an "idle mode."

6.A four-diode, full-bridge rectifier may be used in place of diode D1. This reduces capacitor size by one-half for any given charging current. The zener diode will dissipate twice the calculated power and should be placed at the output of the bridge.

```
.OPTIONS EXPAND LIBRARY LIST NODE
.TRAN   .001   0.03   0   50U
;
VAC   1,0   AC 169 0   SIN(0, 169, 60, 0, 0, 0); 120VAC RMS
R1    1,2   5.2 ; EQUIVALENT FUSE RESISTANCE, 1/4-AMP, 250V S.B.
C1    2,3   1.5U; CURRENT LIMITING SERIES CAPACITOR
RC1   2,3   1.7MEG; EFFECTIVE LOSS COMPONENT FOR CAPACITOR
D1    0,3   D1N5245; VOLTAGE-LIMITING DIODE, 15V, 0.5 WATTS
D2    3,4   D1N4007; BLOCKING DIODE
R2    4,5   .25;INTERNAL RESISTANCE OF BATTERY, "AA" CELL
V1    5,0   DC 1.2  AC 0.0 ; SINGLE CELL BATTERY
*R3   4,0   500; LOAD RESISTANCE
;
.model D1N5245 D(Is=3.142f Rs=3.536 Ikf=0 N=1 Xti=3 Eg=1.11
Cjo=80.5p M=.4186
+               Vj=.75 Fc=.5 Isr=1.527n Nr=2 Bv=15 Ibv=24.573m
Nbv=1.0932
+               Ibvl=7.1249u Nbvl=.65646 Tbvl=833.33u)
.model D1N4007 D(Is=14.11n N=1.984 Rs=33.89m Ikf=94.81 Xti=3 Eg=1.11
+               Cjo=25.89p M=.44 Vj=.3245 Fc=.5 Bv=1500 Ibv=10u
Tt=5.7u)
.PROBE
.END
```

Voted "Best of Issue," Electronic Design, December 4, 1995

Measure Temp Through Printer Port

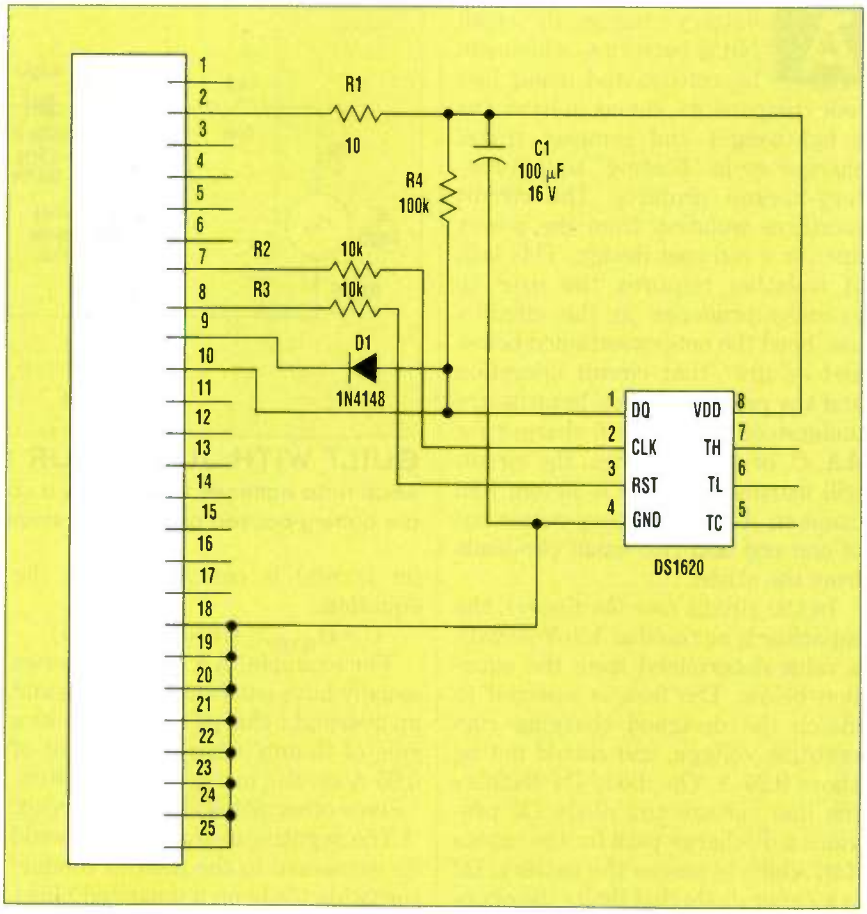
YONGPING XIA, 23008 Arlington Ave., Torrance, CA 90501; (310) 784-1442.

A single-chip digital thermometer IC developed by Dallas Semiconductor, Dallas, Texas—the DS1620—can measure temperature from –55 to +125°C in 0.5° C increments.

The circuit shown uses a PC's printer port to communicate with a DS1620 (*see the figure*).

The C program (*see the listing*) will set the printer port to power the IC, send control commands to and read measured data from the IC, convert the data to temperature, and display it on screen.

Voted "Best of Issue," Electronic Design, March 18, 1996



TEMPERATURE CAN BE measured and displayed on a PC screen using this circuit. It utilizes a PC's printer port to communicate with a single-chip digital thermometer IC (DS1620).

```
#include <stdlib.h>
#include <stdio.h>
#include <conio.h>
#include <dos.h>

#define POWER_ON        0x01
#define POWER_OFF       Cxfe
#define CLK_ON          0x20
#define CLK_OFF         Jxdf
#define RESET_ON        0xbf
#define RESET_OFF       0x40
#define OUT_HIGH        0x80
#define OUT_LOW         0x7f

typedef unsigned int WORD;

int  i, data, out_port, in_port, out=0;
char msg[80];

/* find printer port address */
void find_port(void)
{
  out_port=*(WORD far *)MK_FP(0x0040,8);
  in_port=out_port+1;
  out |=POWER_ON;
  outportb (out_port, out); /* power on */
  delay(1000);
}

/* send control command to DS1620 */
void ssend_control(int control_data)
{
  int control;
  control=control_data;
  for (i=0; i<8; i++)
   {
     out&=CLK_OFF;
     outportb(out_port, out);
     if (control/2*2==control)
       out&=OUT_LOW;
     else
       out |=OUT_HIGH
     control/=2;
     outportb(out_port, out);
     delay(5);
     out |=CLK_ON;
     outportb(out_port, out);
     delay(5);
   }
}

/* reset DS1620 */
void rst(void)
{
  out&=RESET_ON;
  outportb(out_port, out);
  delay(5);
  out |=RESET_OFF;
  outportb(out_port, out);
  delay(5);
}

/* read data from DS1620 */
int read_chip(void)
{
  int in, temp;
  rst();
  send_control(0x0c);
  send_control(0x03);
  rst();
  send_control(0xee);
  send_control(0x00);
  rst();
  send_control(0xaa);
  out |=OUT_HIGH;
  outportb(out_port, out);
  in=0;
  for (i=0; i<9; i++)
   {
     out&=CLK_OFF;
     outportb(out_port, out);
     delay(5);
     temp=inportb(in_port);
     in=in+(((temp/64)&0x01)<<i);
     out |=CLK_ON;
     outportb(out_port, out);
     delay(5);
   }
  return(in);
}

main()
{
  int temp1;
  float tempC;
  clrscr();
  gotoxy(50,24);
  printf("Hit any key to quit");
  find_port();
  do {
     temp1=read_chip();
     if (temp1..256)
     temp1-=512;
     tempC=((float)temp1/2);
     gotoxy(1,1);
     printf("Temperature: %.1f deg C ",tempC);
     gotoxy(1,1);
     delay(1000);
   } while (!kbhit());   /* quit if any key  */
}
```

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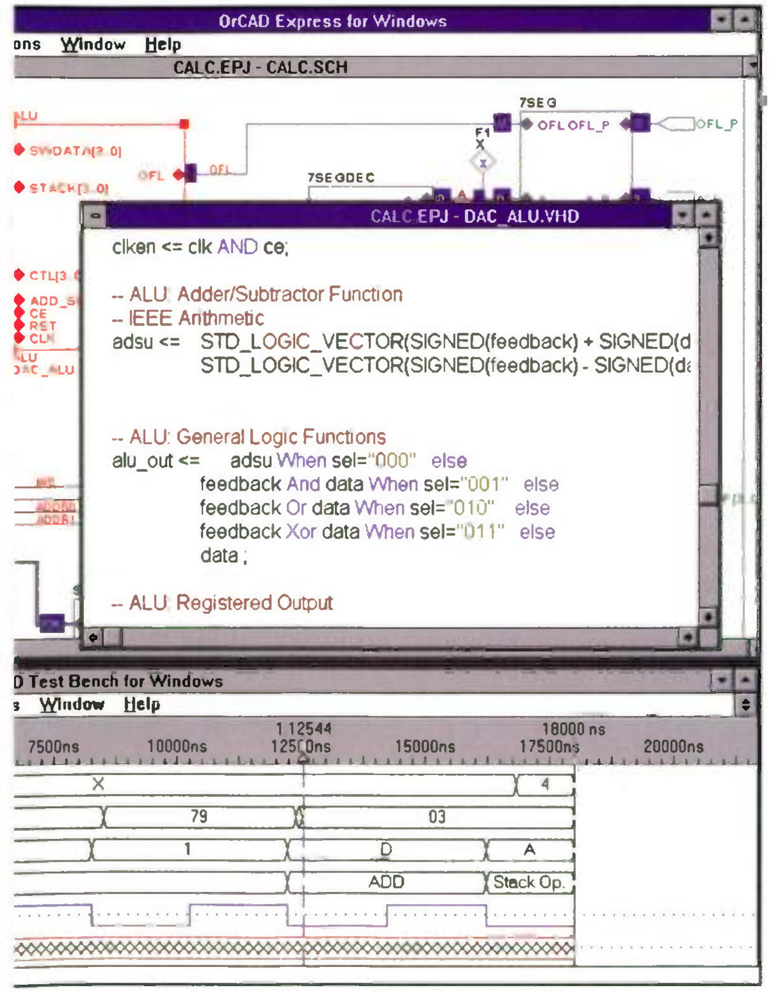

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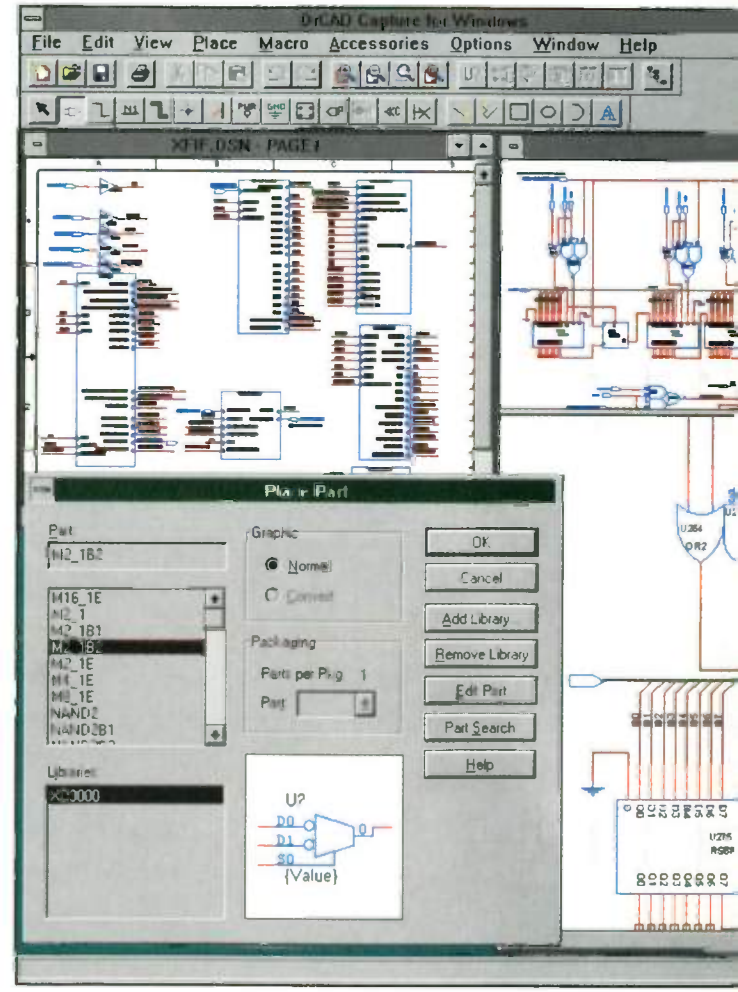


imple RS-232 Tester

RIAN-NICOLAE ION, Noesis-Domaine Technologique de Saclay,Bat. Ariane 4, rue Rene Razel, 91892 Orsay Cedex, France.

One problem in transferring data using the RS-232 standard is whether the TxD and RxD cables should be cross-coupled. It's easy to determine this when a DMM is available, but it might be difficult to do in the field when there's no meter at hand.

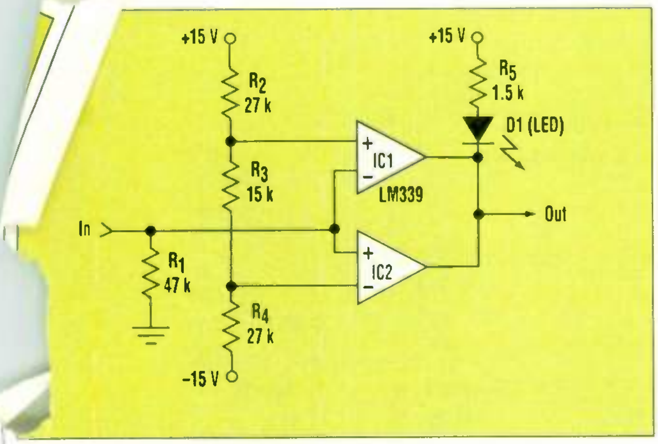
A simple solution handles this task easily, in a small package that could be carried in a pocket (*Fig. 1*). The tester is basically a window comparator, in which the Low and High levels are set at +3.0 V and –3.0 V, respectively, by resistors R2, R3, and R4. Resistor R1, when not driven by an RS-232 output, will have a low voltage across it (approximately 0 V), and the LED D1 at the output of the comparators is turned off.

If the unknown wire of the cable that's tested is an RS-232 output, then it will drive the In point to either a voltage between +3 and +12 V or between –3 and –12 V. In both cases, one of the two comparators' outputs will be driven low. This turns the LED on, indicating the presence of a wire connected to an RS-232 output. The comparator should be an LM339 type or equivalent (with an open-collector output).

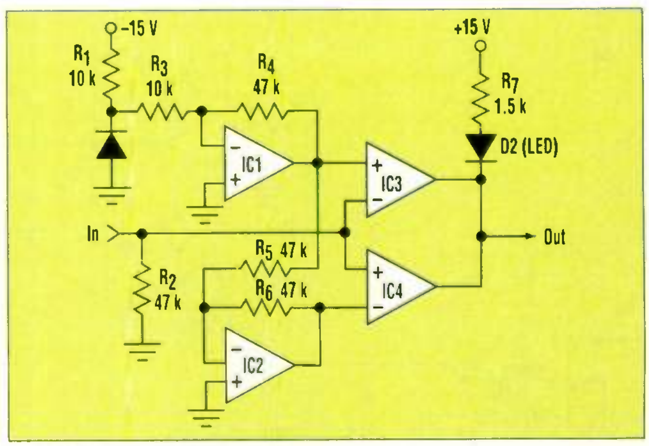
The disadvantage of this scheme is that the thresholds are very sensitive to the supply variations. To eliminate that, the thresholds at the inputs of the comparators can be created using the normal forward drop on a simple diode (a Zener with such a low voltage would be more expensive and difficult to find), and then be brought to the necessary levels by IC1 (+3 V at its output) and IC2 (a simple inverter) (*Fig. 2*).

To minimize parts count, a quad op amp could be used for IC1-4, one that can assure a V_{OH} level high enough to turn off LED D2.

Voted "Best of Issue," Electronic Design, Februay 19, 1996



1. THIS PEN-SIZED device can easily handle the task of determining whether TxD and RxD cables should be cross-coupled when transferring data using the RS-232 standard. .



2. THRESHOLDS often are sensitive to supply variations. In this setup, thresholds are created using a diode's forward drop and then brought to the necessary levels by IC1 and IC2.

Build An Accurate Log Amp

MOSHE GERSTENHABER and Frank J. CIARLONE, Analog Devices Inc. Two Technology Way, Norwood, MA 02602; (617) 329-1241.

Logarithmic amplifiers are used in application in which the input possesses wide dynamic range, and there's a need to resolve signal throughout its range.

conventional logarithmic amplifi (Fig. 1a) consists of an amplifer and nonlinear element in its feedback, a reference circuit, and one specialized component to remove

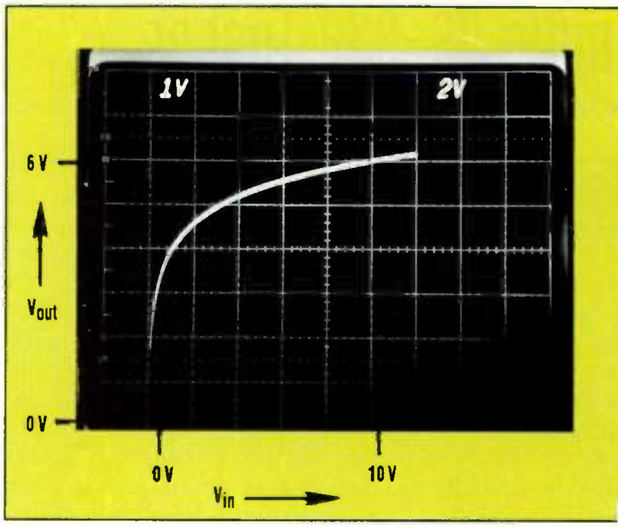
CALCULATED, ACTUAL AND ERROR OF THE LOGARITHMIC AMPLIFIER

VIN	VOUT (Calculated)	V OUT (Measured)	Error/FS
+10 V	1.985	1.990 V	0.05%
+1 V	0 V	.0030 V	0.03%
+100 mV	–1.985	–1.99 V	0.05%
+10 mV	–3.97	–3.97 V	0%
+1 mV	–5.954	–5.93 V	0.24%
+100 muV	–7.94	–7.96	0.20%

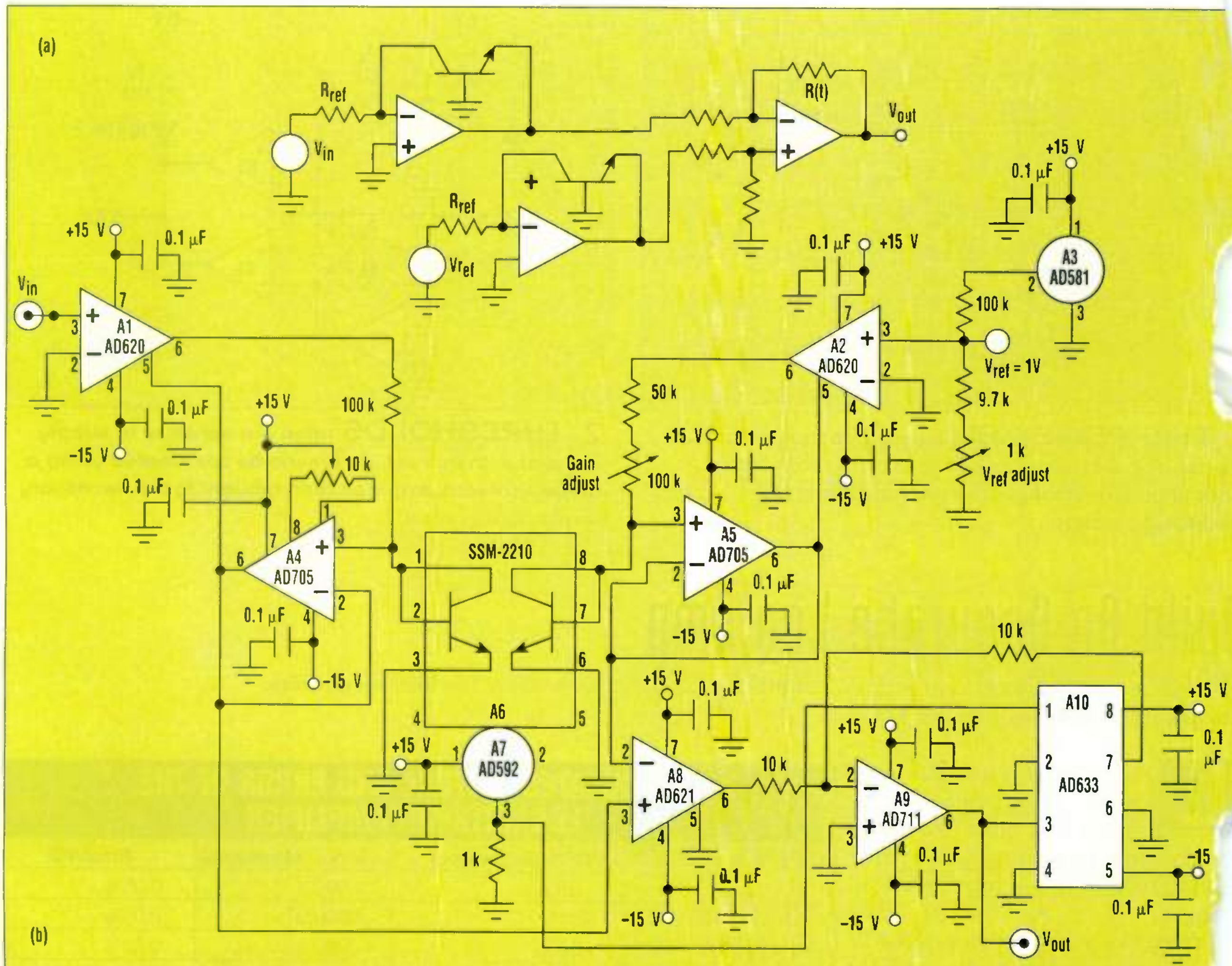
temperature effects. Although such circuits are rather common, they have some limitations. For example, the input must be referenced to ground because common-mode signals will generate errors in the "logging" device, and the input signal's source impedance must be small so that there's no interaction with the input resistance of the logarithmic amp. Moreover, the system bandwidth changes as the signal changes because the nonlinear device alters the loop bandwidth as the current through it is varied.

By modifying the logarithmic-amplifier circuit, it can reject common-mode voltages and only measure differential signals. Its bandwidth is independent of the input voltage andits input impedance is very high. The log circuit consists of an instrumentation amp, and an op amp together with a diode-connected transistor that produces a voltage proportional to the logarithm of the current.

A circuit consisting of a voltage reference, an instrumentation amp, and an op amp together with a diode-connected transistor act as a reference circuit. A thermometer IC, a fixed-gain instru-



2. THIS CROSS PLOT of Vout versus Vin demonstrates the circuit transfer function. The horizonta scale = Vin 2V/div; Vertical = Vo 1V/div.



1. UNLIKE THE CONVENTIONAL LOGARITHMIC amplifier (a), a more accurate amp can be built to reject common-mode voltages (b). The modified amp consists of an instrumentation amp and an op amp configured as a voltage-to-frequiency converter.

mentation amp, and a divider circuit provide the necessary temperature compensation and scaling for a transfer function:

$V_{out} = 1.985\log10(V_{in}/1\ V)$

V_{REF} must be set to 1.000 V and, with Vin = V_{REF}, the grain adjust has to be set so that Vo = 0 V. Calibration at low input voltage is done by changing buffer A4's offset voltage. The table illustrates the calculated, actual, and error of the logarithmic amp in Fig. 1b. Figure 2 shows a cross plot demonstrating the circuit transfer function.

Voted "Best of Issue," Electronic Design, November 6, 1995

Creating a Good, Stable Sine Wave

ARTHUR D. DELAGRANGE, 437 W. Watersville Rd., Mt. Airy, MD 21771; (301) 829-2430.

A classic problem in electronics is the generation of a good, stable sine wave. There are a thousand ways to do it; none of which are perfect. So here's number 1001, which offers some advantages...

Semi-digital circuits (e.g., crystal oscillators and dividers) can create square waves of very stable amplitude and frequency. Although a square wave often is considered as a sine wave having 100% distortion, this is far from true. The "error" consists entirely of odd-frequency harmonics if the duty cycle is exactly 50% (this can be guaranteed by generating twice the desired frequency and dividing by two).

Removing the odd harmonics is a reasonable task for a filter. The obvious solution, a narrowband filter, isn't acceptable because analog types are notorious for poor stability. Digital and semi-digital (e.g., switched capacitor) are better in this respect, but they add their own noise and harmonics.

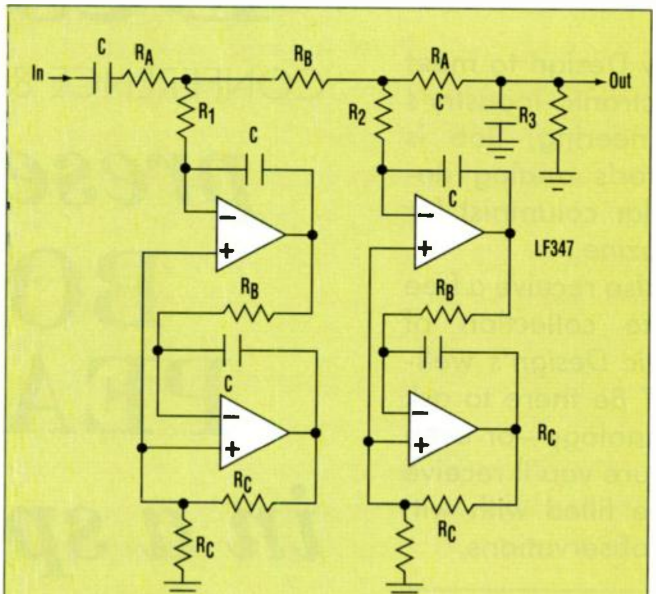
Such a task can be accomplished using the filter shown in Fig. 1. Without R1 and R2, it's an active version of a 5-pole passive low-pass L-C ladder. This type has excellent amplitude stability in the passband, 30-dB/octave slope outside the passband, low component sensitivity, and a capacitor to ground at the output, which ensures continuous high-frequency roll-off and minimizes stray noise pick-up. The rejection would be inadequate at the third and fifth harmonics, but notches at these frequencies can be created with just two more resistors, R1 and R2. This turns the device into an elliptic-like filter (this isn't a true elliptic, because when the zeros are assigned arbitrarily, the humps in the reject band won't be equal).

At first glance, the filter appears complicated, but a closer inspection shows that it can be built with as few as six components. How so? The op amps can be a quad DIP. RA can be two RB resistors in parallel. RC can be equal to RB. R3 can be left-over RB resistors in series. Consequently, all of the resistors other than R1 and R2 can be in two DIPs.

Performance results are shown in Figs. 2 and 3. Fig. 2 shows the filter frequency response, and Fig. 3 illustrates the output spectrum when using a 1-kHz square-wave input. Note that all harmonics are in excess of 80 dB down (this performance was achieved using 1% film capacitors; a DIP of matched ceramics, which are more lossy, yields 70 dB rejection of harmonics).

Some notes on the filter: No 1% tolerances are necessary if matched components are used and R1 and R2 are tweaked to adjust the notch frequencies (this is easily done by adjusting R1 for minimum signal out at the third and R2 for the fifth). Because the filter is passive-derived, it must be lightly loaded. However, if the load provides dc continuity to ground, R3 may be eliminated.

Similarly, if the driving impedance isn't small compared to the resistors in the filter, its impedance may be subtracted from the filter input resistor to compensate. The op amps are part of tuned circuits and should have a gain-bandwidth product of at least 100 times the notch frequency (when the filter

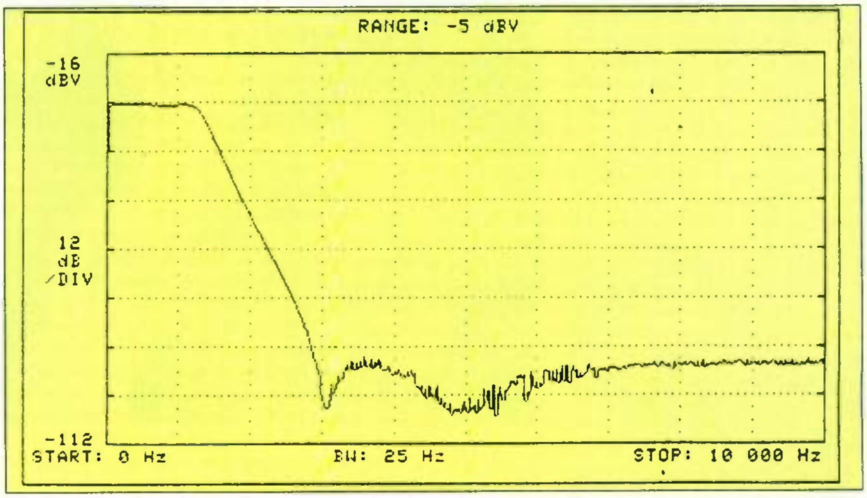


Notes: Values for 1-kHz signal
C = 0.01 µF, 1%*
R_A = 10 k, 1%*
R_B = 20 k, 1%
R_C = 20 k nominal; matched required
R_1 = 1.407 k calculated; 1.40 k, 1% used
R_2 = 506.6 Ω calculated; 511 Ω, 1% used
R_3 = 100 k nominal; for dc bias
*Looser tolerance with matching is okay if R_1 and R_2 are adjusted.

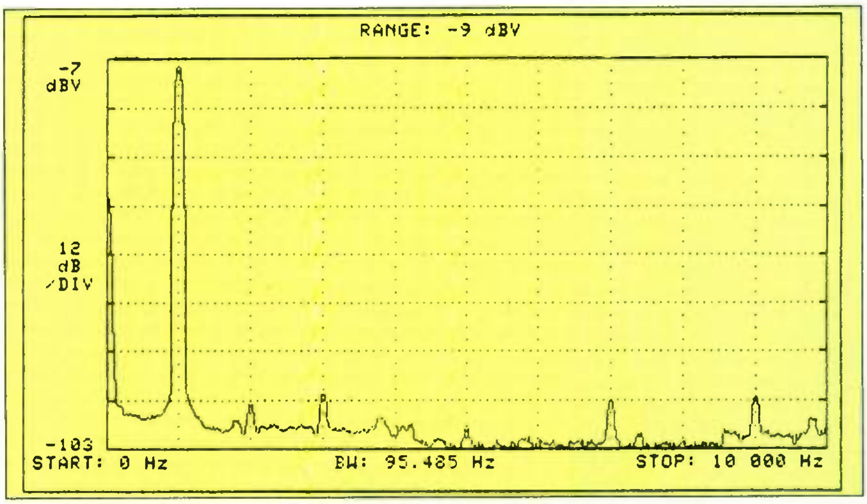
1. USING AN ELLIPTIC-LIKE FILTER. this circuit can remove odd harmonics from a square wave, creating a stable sine wave. The seemingly complex filter actually can be built with as few as six parts.

was changed for a 10-kHz input by reducing the the capacitor values to 1000 pF, harmonic rejection dropped to 66 dB). At much higher frequencies, the passive version might be better.

Voted "Best of Issue," Electronic Design, November 6, 1995



2. FREQUENCY-RESPONSE RESULTS FOR THE filter in Fig. 1 are illustrated. The filter is essentially flat within the passband and rolls off at about 30 dB/octave. Note the notches at the third and fifth harmonics.



3. THE FILTER'S OUTPUT SPECTRUM, using a 1-kHz square-wave input, shows that all harmonics are in excess of 80 dB down.

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Convert Pulse Width To Analog

W. STEPHEN WOODWARD, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@uncvxl.oit.unc.edu.

Instruments possessing an internal digital architecture are sometimes required to produce an analog output. Often, these requirements are introduced very late in the product-development cycle (thanks a lot, marketing!), when it may be difficult to provide board space and addressing logic for a conventional DAC.

The circuit shown arose from just such a scenario, which involved a small microprocessor-based (Z-80) product that needed a greater than 15-bit resolution 0-to-5-V analog output grafted on.

The product had few assets free for the control of even a serial-input DAC. What was available, however, was much idle processor time unneeded for the 500-ms measurement cycle, exactly one uncommitted output bit, and some unoccupied capacity in the system ROM.

It was, therefore, apparent that design modifications could be introduced. Such alterations would generate, twice per second as part of the measurement cycle, a software-loop-timed pulse with duration ranging from 3 to 363 ms that would be proportional to the measured quantity. Pulse duration would be 7.26 µs or one part in 50,000.

This circuit (*see the figure*) converts these pulses to a monotonic analog 0-to-5-V output with 100-µV resolution that settles to better than 1% only 1 cycle after a change in

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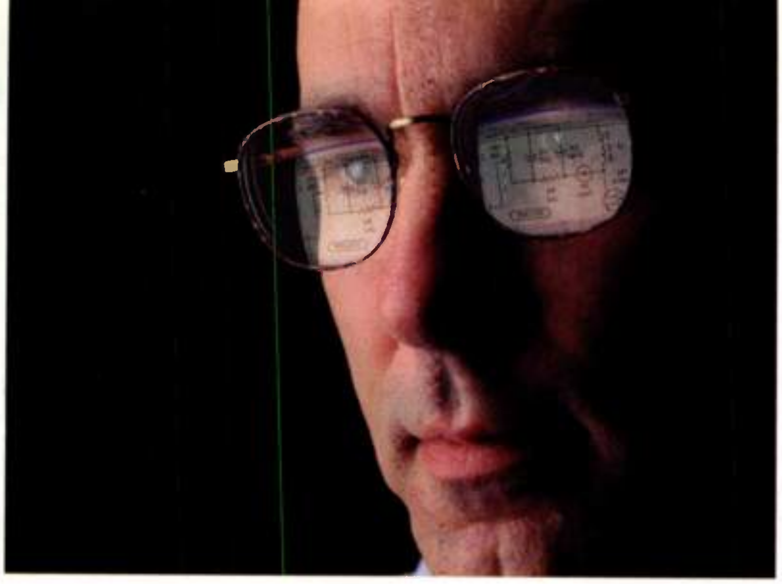

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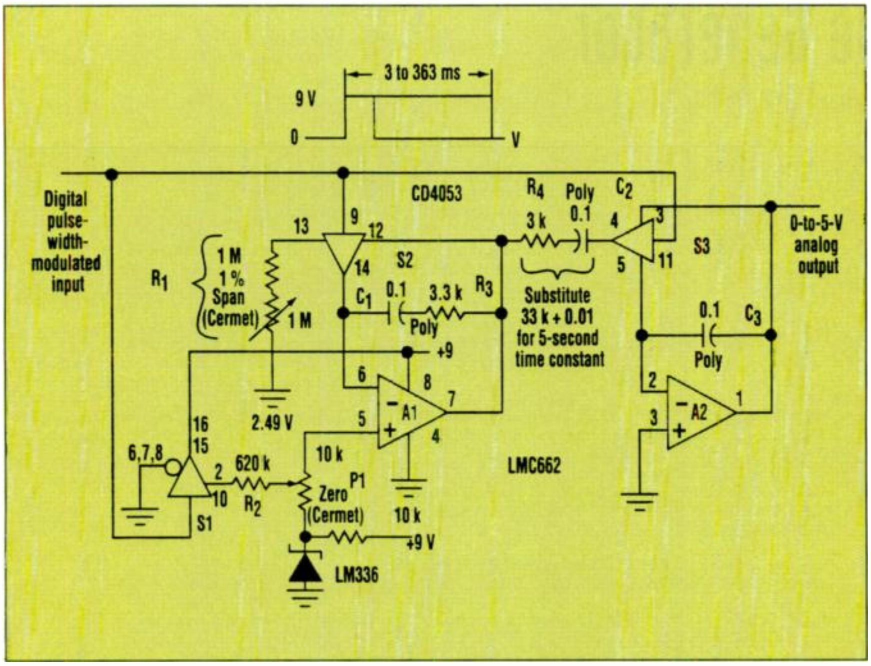

SOFTWARE-LOOP-TIMED PULSES ARE converted to a 0-to-5-V analog output that settles to better than 1% only one cycle after a change in pulse duration. The pulses have a duration ranging from 3 to 363 ms.

pulse duration.

During the interval between output pulses, the CD4053B CMOS Lswitches are in the state illustrated. S1 is closed, S2 is holding C1 reset, and S3 connects C2 to A2's summing point. At the start of an output pulse, switch S1 releases one end of R2. This causes the noninverting input of A1 to drop about 4 mV negative. The exact amplitude of this step is adjusted by potentiometer P1 so that a pulse width of the minimum 3 ms produces a zero output.

While this is happening, switch S2 begins the charge of capacitor C1 through R1. The rate of this charging is adjusted so that a pulse with the maximum duration of 363 ms produces a 5-V output.

Simultaneously, S3 connects the right-hand end of C2 to A2's output. As a result, at the end of the integration cycle, the left-hand terminal of C2 will be at A2's output voltage. The minimum input pulse duration is set to 3 ms, rather than zero, so that C2 always has sufficient time to equilibrate to this differential.

Therefore, at the end of the integration cycle, when switch S3 returns to the idle state and connects C2 to A2's summing point, a charge equal to C2 times the voltage difference between A1 and A2's outputs will be delivered to C3. This charge transfer occurs as S2 returns to the idle state and resets C1, pulling the left-hand terminal of C2 back to the idling voltage.

The result is that if C2 = C3, A2's output will slew exactly by the difference between the output value from the previous measurement cycle to the one appropriate for the new cycle. If this equality isn't exact, one or two cycles may be required for precise settling.

Voted "Best of Issue," Electronic Design, November 6, 1995

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Programmable Noise Generator

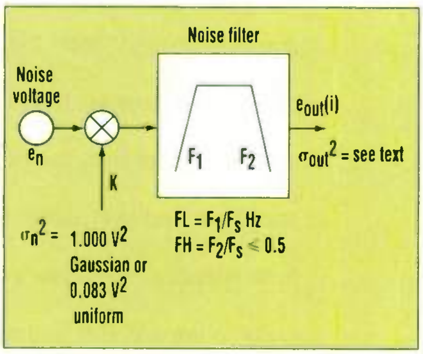
FRANK N. VITALJIC, 514-13th St., Bellingham, WA 98225.

The noise voltage (en) generator shown is able to generate uniform or Gaussian noise (*see the figure*). The noise is multiplied by (K), resulting in a noise power of $K^2\sigma_n^2$volts^2 at the filter's input. This power is available at the filter's output by setting the bandwidth fully open (i.e., FL = 0, FH = 0.5 Hz).

The 127-tap linear phase filter passes frequencies between F1 and F2, thus bandlimiting the filter output noise (e_{out}). The output is sampled at a rate of Fs Hz, and stored as 500 samples in the *noise_data* array (*see listing for noise_generator() program*). The output noise power is approximately:

$$\sigma_{out}{}^2 \approx 2[(F2 - F1)/Fs]K^2\sigma_n{}^2\text{volts}^2$$

The statistics of the output data (mean, variance, min, max) are stored in the *stats* array. The output noise power can be set as desired by adjusting (K) accordingly.



THIS PROGRAMMABLE noise voltage generator is capable of producing uniform, or Gaussian, noise. The output noise power can be set as desired by adjusting (K).

Voted "Best of Issue," Electronic Design, January 8, 1996

```
#include<stdlib.h>  //PROGRAMMABLE BAND-LIMITED DIGITAL
#include<math.h>    //   NOISE GENERATOR PROGRAM

void noise_generator(int noise_type,    //0=uniform, 1=Gaussian
                     int seed,          //Seed for srand()function
                     double FL,        //Low band-edge | normalized
                     double FH,        //High band-edge | F/Fs $ 0.5
                     double noise_mul,    //Noise multiplier
                     double*noise_data,   //500 data points
                     double*stats)        //Array of mean, variance,
                                          //min, max noise data,
resp.
//Generates 500 data points of user programmable band-limited noise
//Requires the function calc_coeffs()published in ELECTRONIC DESIGN,
June 26, 1995, p. 104.
{
  double filter_coeffs[MAXLEN],*data_ptr,*coef_ptr,*p, *q;
  double data_in[626],*out_ptr, gaus[2], acum;
  int i, j;

//Calculate noise filter coefficients
  calc_coeffs(BPF, MAXLEN, DUAL, FL, FH, filter_coeffs);

//Duplicate symmetrical coefficients in upper-half of array
      p = filter_coeffs; q = &filter_coeffs[126];
      for(i = 0; i < 63; i++)*q- = *p++;

//Generate broad-band noise data for filter input
  srand(seed); //Initialize rand()function sequence
  p = data_in;
  if(noise_type == 0)
        for(i = 0; i < 626; i++) *p++ = noise_mul * uniform();
  else for(i = 0; i < 313; i++) {
         gaussian(gaus);
         *p++ = noise_mul * gaus[0]; *p++ = noise_mul * gaus[1];
  }

//Input broad-band noise to filter and store band-limited noise
//in array noise_data, 500 points.
  out_ptr = noise_data;
  for(i = MAXLEN-1; i < 626; i++) {
        data_ptr = &data_in[i];
        coef_ptr = filter_coeffs;
        acum = (*coef_ptr++) * (*data_ptr-);
        for(j = 1; j < MAXLEN; j++) acum += (*coef_ptr++) *
(*data_ptr-);
        *out_ptr++ = acum;
  }

//Calculate min/max noise data
  stats[2] = stats[3] = noise_data[0];
  for(i = 1; i < 500; i++) {
        if(noise_data[i] < stats[2]) stats[2] = noise_data[i]; //min
        if(noise_data[i] > stats[3]) stats[3] = noise_data[i]; //max
  }

//Calculate mean/variance noise data
  stats[0] = stats[1] = 0.0;
  for(i = 0; i < 500; i++) {
         stats[0] += noise_data[i];
         stats[1] += noise_data[i] * noise_data[i];
  }
  stats[0] = stats[0] / 500.0; //mean
  stats[1] = stats[1] / 500.0 - stats[0] * stats[0]; //variance
} //end noise_generator()

double uniform(void)
//Generate zero mean uniform random number, -0.5 to 0.5
 { return ((double)(rand() & RAND_MAX)/RAND_MAX - 0.5); }

void gaussian(double *gp)
//Generate zero mean unit variance Gaussian random number pair
 { double x, y, r, a;
//Generate pair of random numbers, Box-Muller Transform
  do {
       x = 2.0 * uniform(); y = 2.0 * uniform();
       r  x*x + y*y;
  } while((r > 1.0) || (r == 0.0));
//Map x and y to gaussian random number pair
  a = sqrt(-2.0 * log(r) / r);
  *gp++ = x * a; *gp = y * a;
 }
```

Active Filter Uses Equal Value Parts

MICHAEL A. WYATT, Honeywell Inc., 13350 U.S. Hwy. 19, Clearwater, FL 34624; (813) 539-5653; fax (813) 539-2558.

Equal-value components can be quite an advantage in filter designs when considering the total costs associated with the procurement, stocking, and assembly of the filter.

For instance, the Butterworth active third-order low-pass filter (*Fig. 1a, middle*) uses equal value resistors and capacitors. This feature normalizes the filter's 3-dB corner frequency to 1/RC (in radians) for both low-pass and high-pass designs (*Fig. 2a*).

The two additional op amps for the normalized filter may cost less than the unequal value components in the traditional Sallen-Key filter (quad op amps don't cost much more than single op amps), especially if the application calls for precision components (*see Fig. 1a, again)*

PSpice's (MicroSim Corp., Irvine, Calif.) behavioral modeling capability allows for the comparison of the normalized and Sallen-Key third-order filters to an ideal filter.

The Laplace behavioral voltage-controlled voltage source "EIdeal" (*Fig. 1a, top*) is configured as an ideal Butterworth low-pass filter with a 1-kHz bandwidth (ω_c = 6283.19 radians/s).

The Laplace transfer function (entered as symbol attribute of EIdeal) for the third-order Butterworth low-pass filter is as follows:

$$T(s) = \frac{1}{\left[(s^3/\omega_c^3) + 2\,(s^2/\omega_c^2) + 2\,(s/\omega_c) + 1\right]}$$

The graphs in Fig. 1b are plots of the ideal, normalized, and Sallen-Key low-pass filter frequency-domain magnitude and error responses.

Note how both the normalized and Sallen-Key filters follow the ideal response well into the stopband. The error plots were created by plotting the difference between the responses of the real filter and the ideal filter.

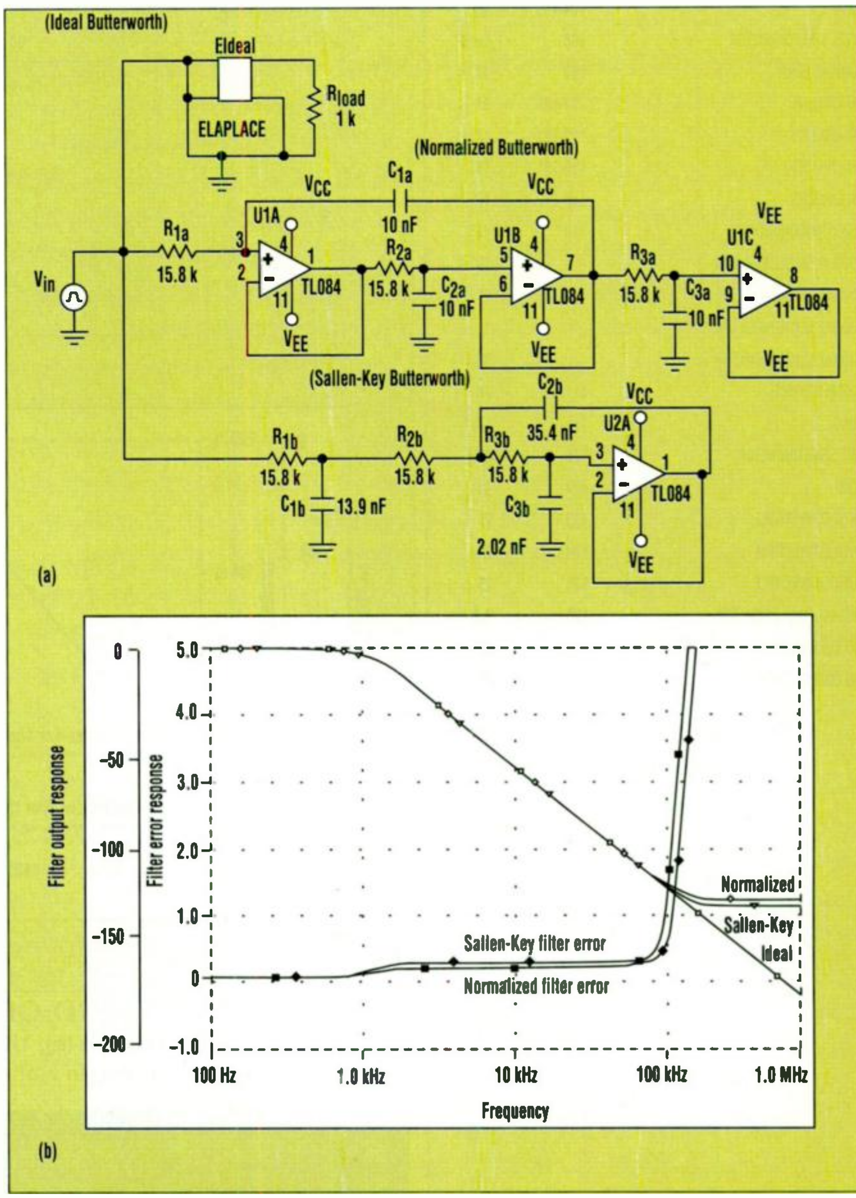
The plots indicate that the normalized filter achieves performance results that are equal to those of the Sallen-Key low-pass filter.

Interchanging the resistors and capacitors transforms the normalized low-pass filter into a high-pass filter with the same corner frequency (*Fig. 2a*).

This concept is illustrated with an ideal Butterworth high-pass filter transfer function (EIdeal):

$$T(s) = \frac{s^3/\omega_c^3}{\left[(s^3/\omega_c^3) + 2\,(s^2/\omega_c^2) + 2\,(s/\omega_c) + 1\right]}$$

Notice that the Sallen-Key filter must be modified according to impedance levels at each node. This yields a filter with equal-value



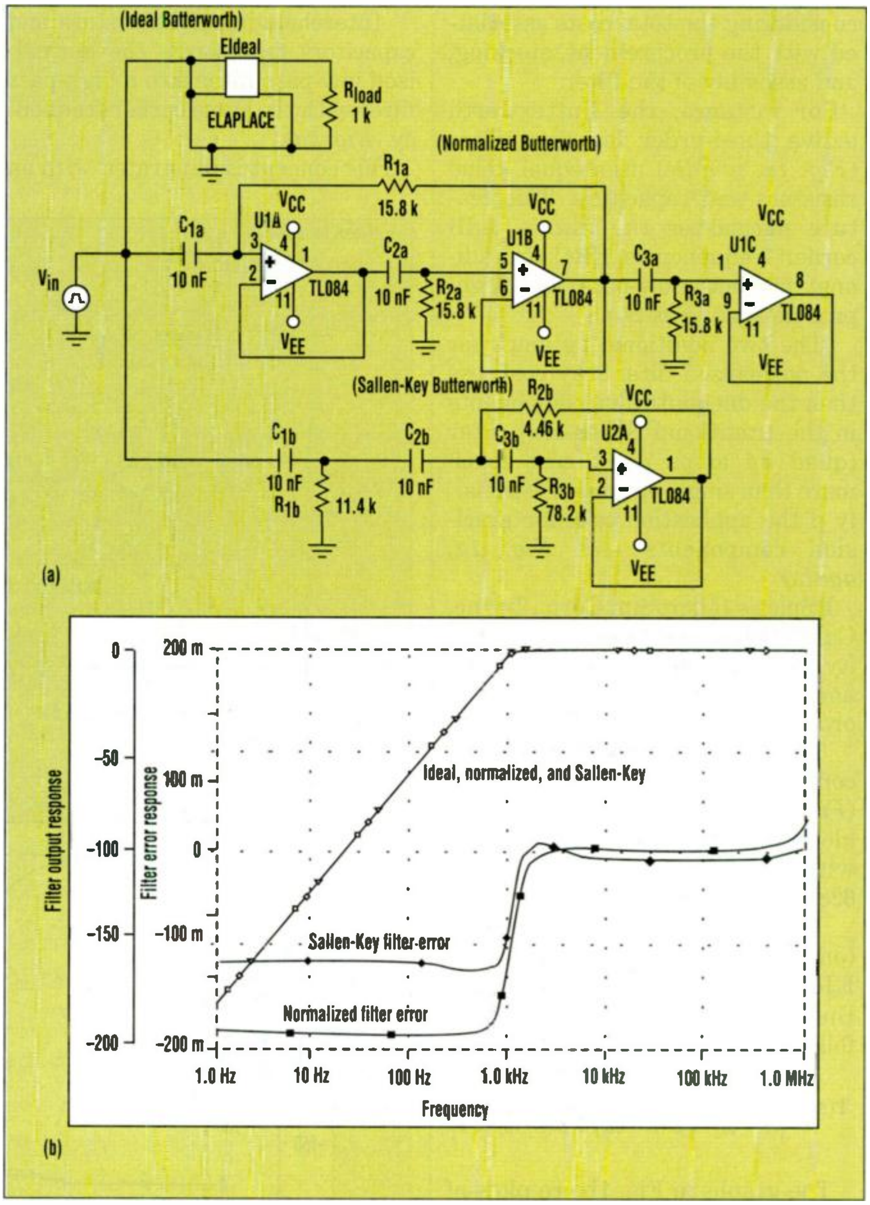
1. USING EQUAL-VALUE components in a third-order Butterworth low-pass filter design (a), will lead to lower total costs when procuring, stocking, and assembling the filters. Plots of the ideal, normalized, and Sallen-Key low-pass filter amplitude and error responses show that the normalized and Sallen-Key filters follow the ideal response well into the stopband (b).

INDEX OF ADVERTISERS

capacitors and unequal-value resistors, an improvement over the traditional low-pass design of equal-value resistors and unequal-value capacitors.

The graphs in Fig. 2b indicate that the normalized high-pass filter compares favorably with the Sallen-Key filter in high-pass applications, much like the previously mentioned low-pass case.

Voted "Best of Issue," Electronic Design, August 8, 1995



2. A HIGH-PASS THIRD-ORDER Butterworth filter with equal-value components can also be built (a). The normalized filter once again compares favorably with the Sallen-Key in high-pass applications (b).

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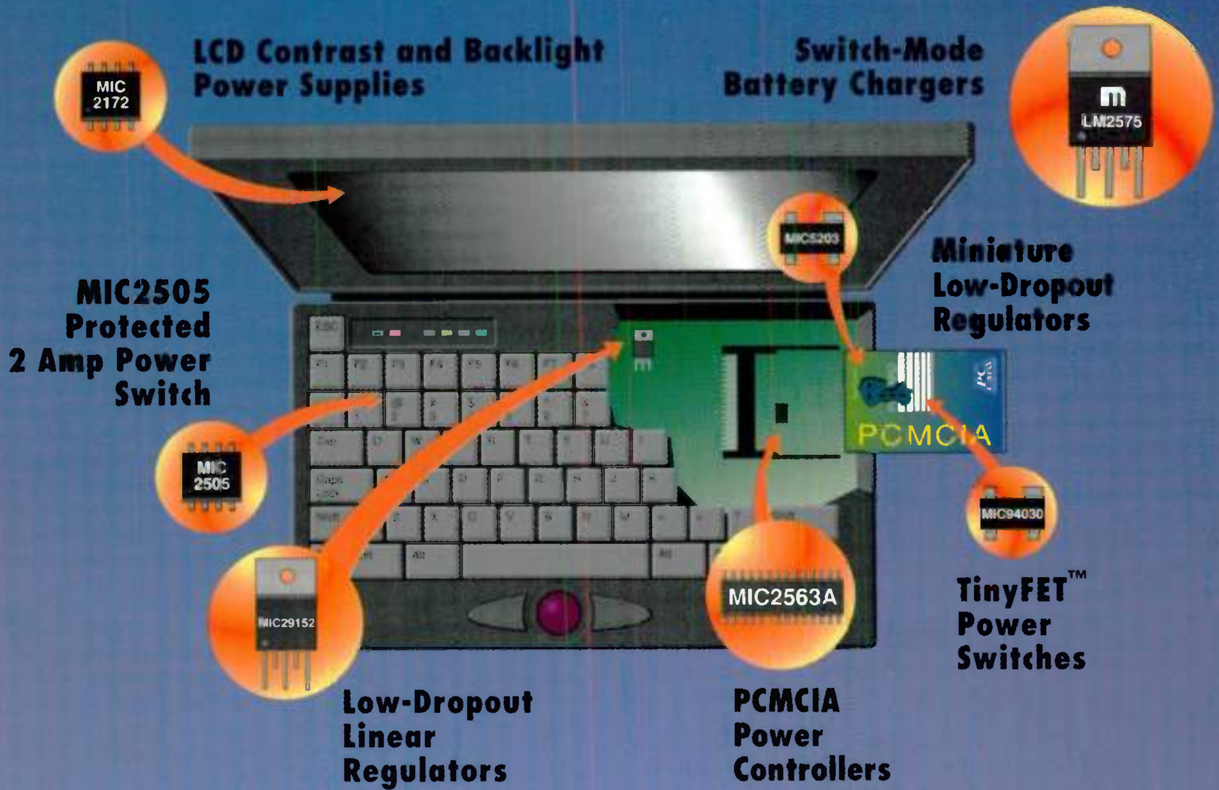

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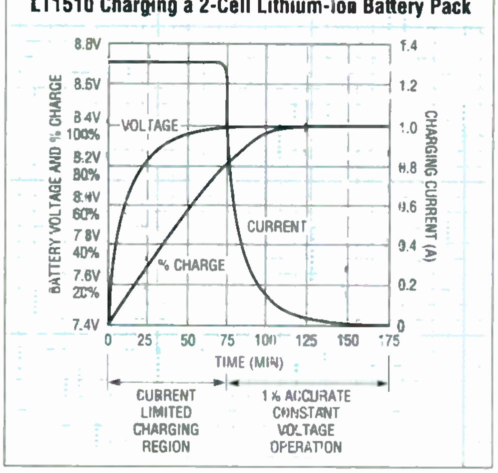

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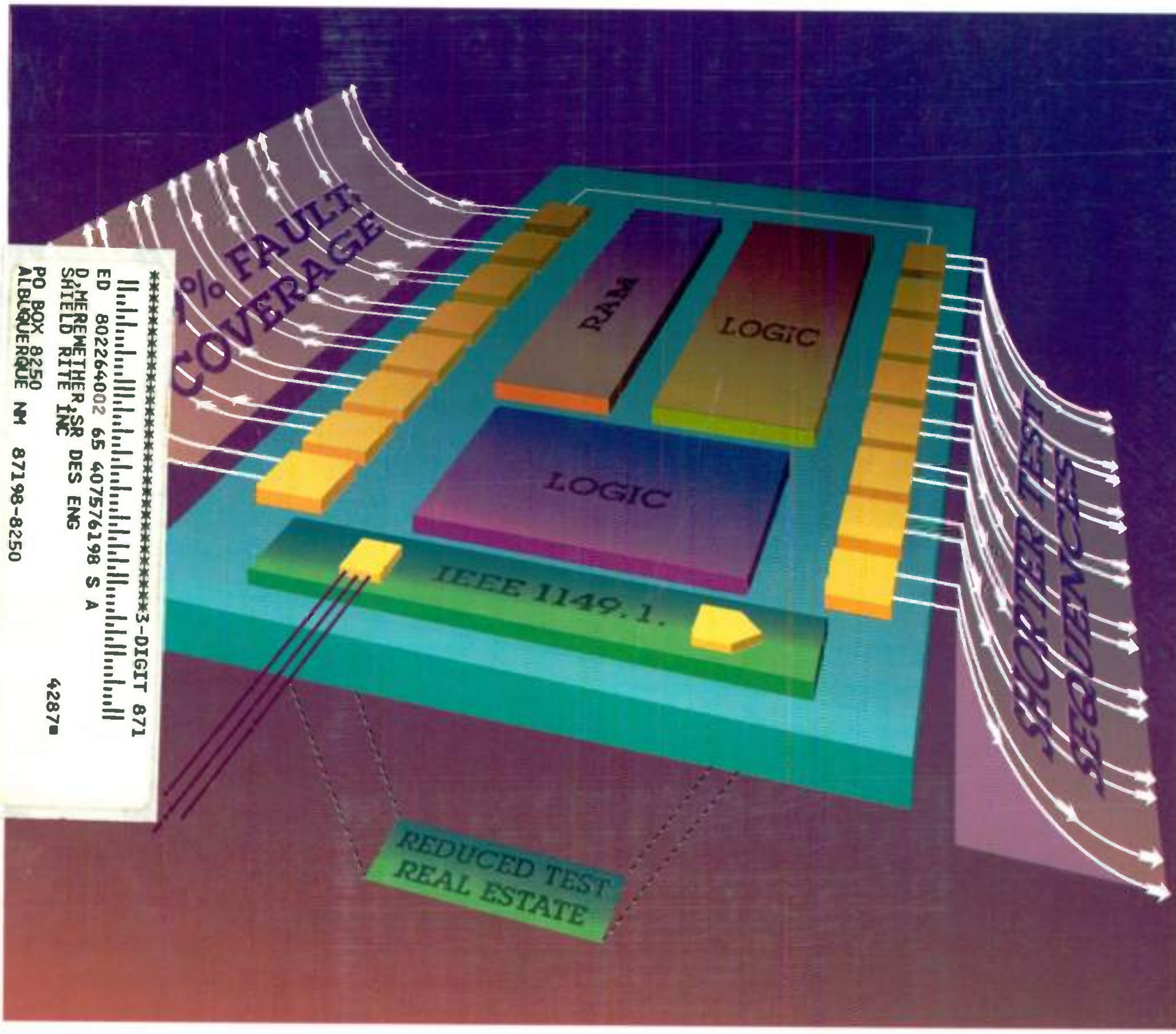

High Coverage, Low Overhead Come To Logic BIST p. 53

DREAM TEAM

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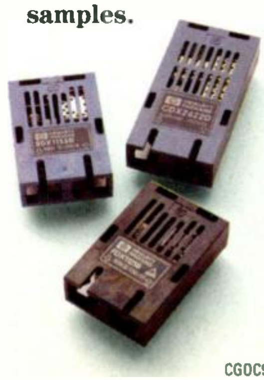

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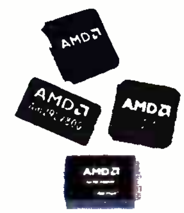

Half of the silicon we make this year will include linecard ICs, Ethernet controllers and repeaters, programmable logic devices, flash and EPROM memory, and embedded processors.

Magic Packet® technology gives the new HP Vectra XM the power to lower network administration and maintenance costs. Now a network manager can remotely wake-up a PC in sleep mode and remotely power-up a PC that has been powered down.

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Model	*Freq (MHz)	Gain (dB)	Max. Power Out (dBm, @ 1dB Comp)	Dynamic Range NF(dB)	Dynamic Range IP3(dBm)	①Price $ ea. (10 Qty.)
ERA-1	DC-8000	11.6	13.0	7.0	26	1.80
ERA-1SM	DC-8000	11.0	13.0	7.0	26	1.85
ERA-2	DC-6000	14.9	14.0	6.0	27	1.95
ERA-2SM	DC-6000	13.1	13.0	6.0	27	2.00
ERA-3	DC-3000	20.2	11.0	4.5	23	2.10
ERA-3SM	DC-3000	19.4	11.0	4.5	23	2.15
ERA-4	DC-4000	13.9	▲19.1	5.2	▲36	4.15
ERA-4SM	DC-4000	13.9	▲19.1	5.2	▲36	4.20
ERA-5	DC-4000	19.0	▲19.6	4.0	▲36	4.15
ERA-5SM	DC-4000	19.0	▲19.4	4.0	▲36	4.20

Note: Specs typical at 2GHz, 25°C

▲ Typ. numbers tested at 1GHz. At 2GHz, Max. Pwr. Out may decrease by 0.4dB & IP3 by 3 to 4dB.

* Low frequency cutoff determined by external coupling capacitors.

① Price (ea.) Qty 1000: ERA-1 $1.19, -2 $1.33, -3 $1.48, -4 or -5 $2.95. SM option same price.

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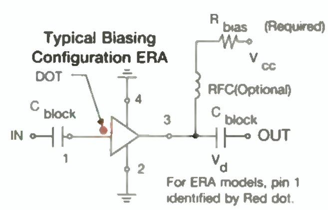
Chip Coupling Capacitors at 12¢ each (50 min.)

Size (mils)	Value
80x50	10, 22, 47, 68, 100, 220, 470, 680, 1000, 2200, 4700, 6800, 10,000 pf
120x60	.002, .047, .068, .1 µf

ACTUAL SIZE

Typical Biasing Configuration ERA



For ERA models, pin 1 identified by Red dot.

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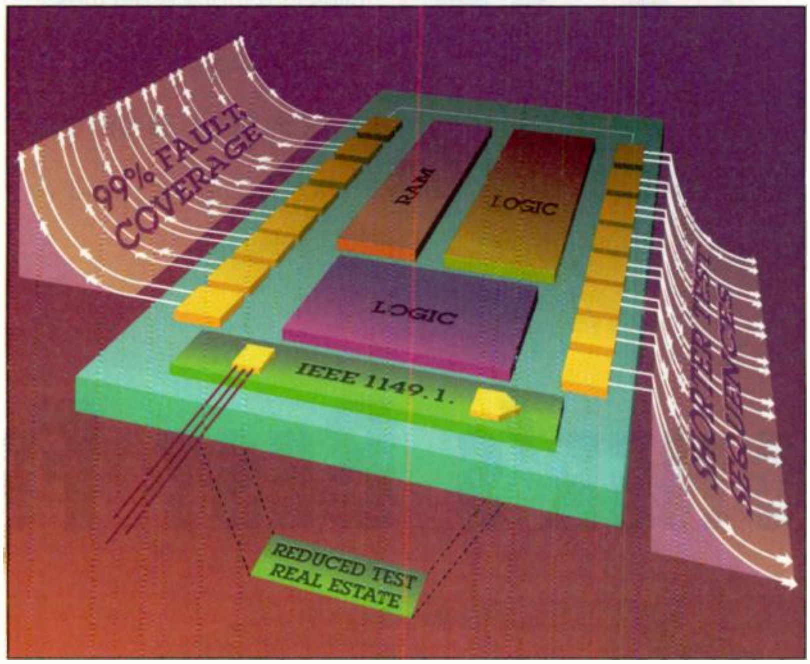
ELECTRONIC DESIGN

October 24, 1996 Volume 44, Number 22

COVER STORY



Higher Coverage, Lower Overhead Enhance Logic BIST p. 53

A design-for-test tool automatically inserts built-in self-test structures into ICs, and does a better job of it.

FEATURES

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published twice monthly except for 3 issues in May and 3 issues in October by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $105 U.S., $185 Canada, $210, $255 International. Periodicals Postage Paid at Cleveland, OH and at additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S Patent Office.

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ELECTRONIC DESIGN

October 24, 1996 Volume 44, Number 22

DEPARTMENTS

COVER ART: MARGARET ENDRES

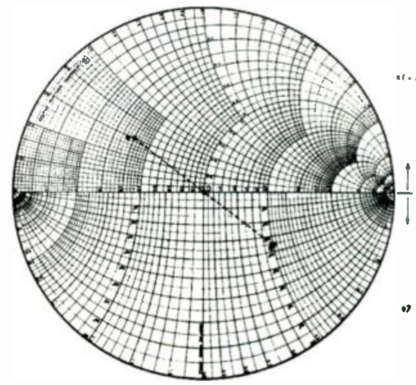
Jesse H. Neal Editorial Achievement

Awards: 1967 First Place Award
1968 First Place Award
1972 Certificate of Merit
1975 Two Certificates of Merit
1976 Certificate of Merit
1978 Certificate of Merit
1980 Certificate of Merit
1986 First Place Award
1989 Certificate of Merit
1992 Certificate of Merit

ELECTRONIC DESIGN 40 YEARS AGO

Polar to Rectangular Conversion Chart, H. E. Schrank, Bendix Radio Div., Bendix Aviation Corp., Towson, Md.

Designed to aid in calculations which involve converting complex numbers from rectangular to polar form, this chart is particularly suited for circuit and transmission line problems involving impedances or admittances. The chart consists of a simple combination of the Smith impedance chart and its alternate "Z-θ" form, known as the Carter chart. Both charts are normalized to unity impedance at the center, and the halves corresponding to positive reactance components were chosen in making this conversion chart. Negative reactances can, of course, be handled simply by reading theta as a negative angle.



Using the chart is simply a matter of locating the rectangular components of an impedance (r + jx) in the lower half of the chart, and then reading its polar components (z/θ in the upper half of the diagram).

Although the accuracy of this chart is not as good as slide-rule computations, it is a useful time-saver for rough estimating and checking. Its best accuracy is obtained by scaling the r, x, and z components to avoid the regions of the chart where the respective contours are crowded. For example in converting z = 10/53 to rectangular form, it is advisable to use a scaling factor of say 10, in order to work near the middle of the cart; thus, the chart is entered with z' = z/10 = 1.0/53, and the rectangular components r' = 0.6, x' = 0.8 are found as indicated in the example. The angle θ is, of course, not scaled. The final results are r = 10, r' = 6.0; x = 10, x' = 8.0; i.e., z = 6.0 + j8.0.*(Electronic Design, October 15, 1956, p. 44)*

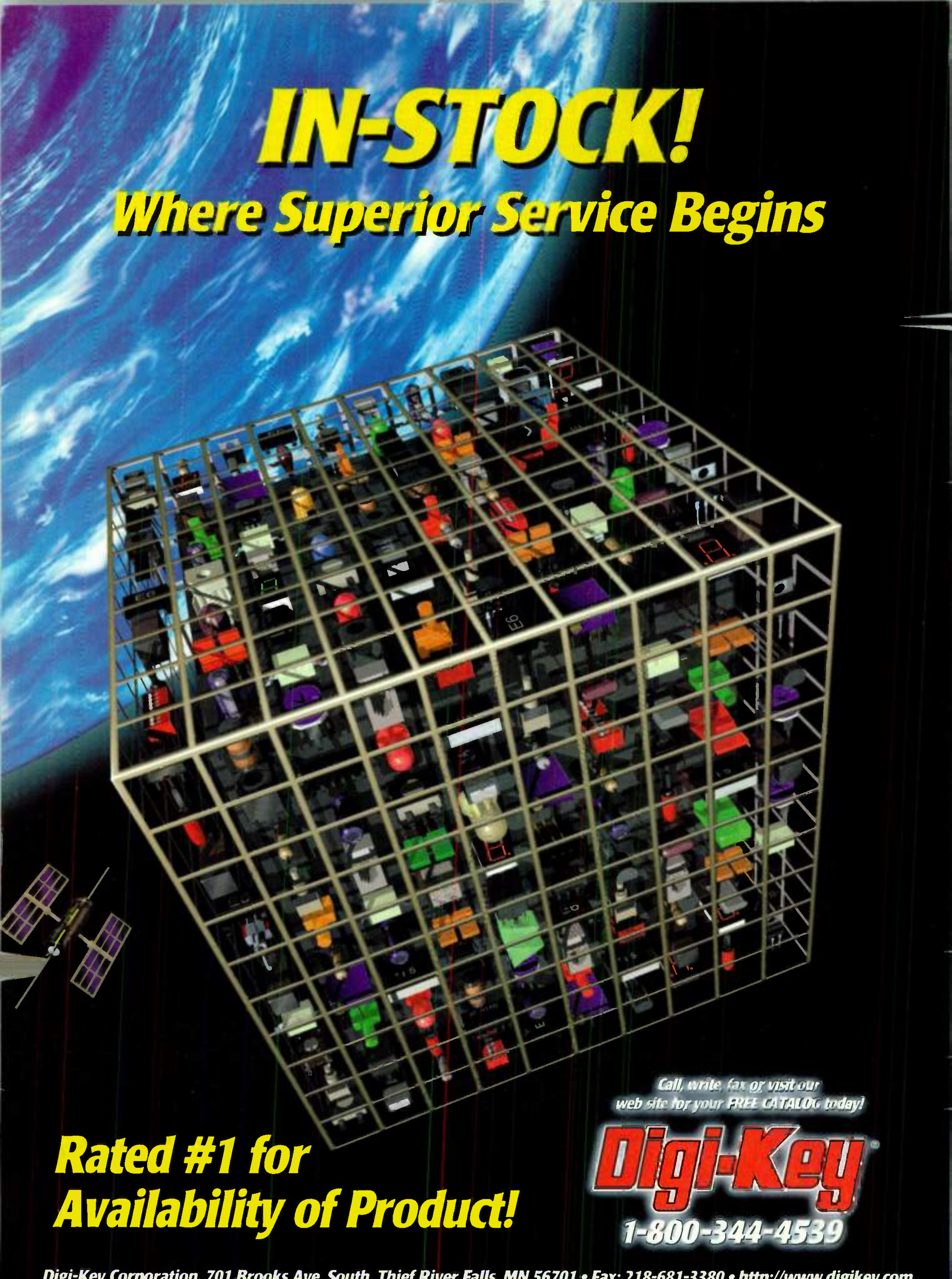
This is another example of the type of pencil-and-paper graphical tools that were used by engineers to solve complex problems before the arrival of the calculator and personal computer.—SS

Electronic Industry Growth

Dr. W.R.G. Baker, president of RETMA and GE VP, Syracuse, predicts that a major portion of the electronics business 10 years hence will come from products not now in production. Electronics, 4th largest American industry, now employs 75 per cent of its more than 1-3/4 million employees on jobs which didn't even exist 10 years ago.

He indicates that to "...assume its responsibilities toward society...industry must: See that new products are not put on the market until the product is ready for market, and vice versa; Never fail to fulfill responsibilities for research, development, production and delivery of military products; Work increasingly to provide a fair return on investments; Take a genuine interest in employee welfare by providing good pay, pleasant working conditions and steady jobs; Recognize that industry and the community have interrelated responsibilities which must be met if both are to prosper; Help provide for our increasing technology by assisting the field of education wherever possible; Assure efficient use of one of our great natural resources, the radio spectrum, by thoroughly studying the problem of whether uhf can be made reasonably comparable to vhf TV service."*(Electronic Design, October 1, 1956, p. 5)*

It looks like Dr. Baker was right on with every one of his points—he could probably make almost the same speech today. His mention of uhf tv, however, raises an interesting point: did over-the-air uhf tv ever really make it, even with every television set equipped with a uhf tuner? Reception here in the Northeast was never that great for uhf broadcasts, and it seems that it wasn't until cable tv came along that uhf stations drew much of an audience.—SS



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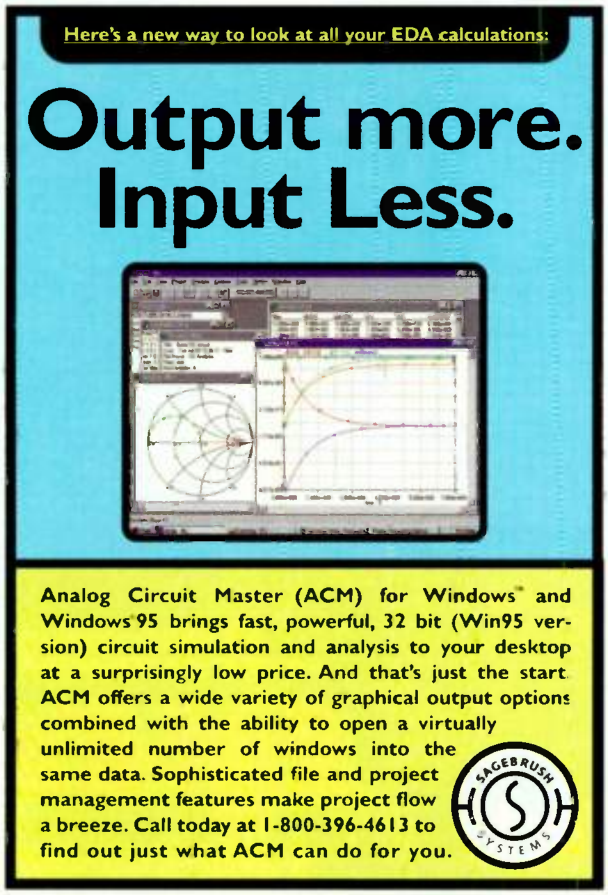

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UPCOMING MEETINGS

NOVEMBER

Miniature Card Implementers Forum Info Workshop, Nov. 1. Boston, MA. Contact Kevin Randolph, (800) 462-1042 or (619) 673-0870; fax (619) 673-1432; e-mail: mcif@annabooks.com; http://www.annabooks.com.

IEEE Ultrasonics Symposium, Nov. 2-7. Hyatt Regency Hotel, San Antonio, TX. Contact Jeff Schoenwald, Rockwell Science Center, 1049 Camino Dos Rios, Thousand Oaks, CA 91360; (805) 373-4236; fax (805) 373-4158; e-mail: jsschoen@scimail.remnet.rockwell.com.

IEEE Nuclear Science Symposium (NNS 96), Nov. 2-9. Anaheim Marriott, Anaheim, CA. Contact Jessica Quiroz, Health Sciences Research, Imaging Center, COM, University of California, Irvine, CA 92717-5026; (714) 824-6001; fax (714) 824-3481; e-mail: jquiroz@uci.edu.

GaAs REL Workshop, Nov. 3. Peabody Hotel, Orlando, FL. Contact Anthony A. Immorlica, EIA/JEDEC, JC-50 Workshop, 2500 Wilson Blvd., Arlington, VA 22201-3834; (315) 456-3514

GaAs IC Symposium, Nov. 3-6. Peabody Hotel, Orlando, FL. Contact Philip Wallace, 35 Technology Dr., Warren, NJ 07059-5197; (908) 412-5987; fax (908) 412-5985; e-mail: wallacepw@aol.com.

Northcon, Nov. 4-6. Washington State Convention and Trade Center, Seattle, WA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668 or (310) 215-3976; fax (310) 641-5117; e-mail: northcon@ieee.org; http://www.northcon.org.

IEEE/RJS International Conference on Intelligent Robots & Systems (IROS 96), November 4-8. Senri Life Science Center, Osaka, Japan. Contact Minoru Asada, Dept. of Mechanical Engineering for Computer Controlled Machinery, Osaka University, Suita, Osaka 565 Japan; (81) 6 879 7347; fax (81) 6 879 7348; e-mail: asada@robotics.com.eng-osada-u.ac.jp.

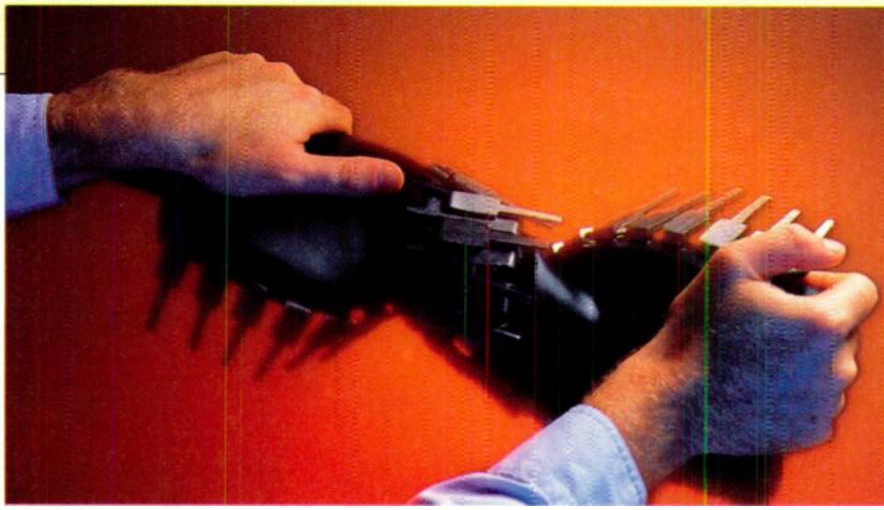
JEMIMA T&M 96, Nov. 5-7. Tokyo Ryutsu Center, 1-1-6 Heiwajima, Ohta-ku, Tokyo 143, Japan. Contact Nobuo Kishino, Director, JEMIMA, 0081-3-3502-0601; (fax) 0081-3-3502-0600.

Ninth International Symposium on Systems Synthesis, Nov. 6-8. Sheraton Grand, La Jolla, CA. Contact Frank Vahid, Dept. of Computer Science, University of California, Riverside, CA 92521-0304; (909) 787-4710; e-mail: vahid@cs.ucr.edu.

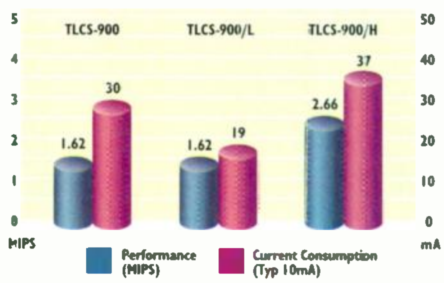
IEEE Frontiers in Education Conference (FIE 96), Nov. 6-9. Marriott Hotel, Salt Lake City, UT. Contact Magdy F. Iskander, Electrical Engineering Dept., University of Utah, Salt Lake City, UT 84112; (801) 581-6944; fax (801) 581-5281; e-mail: iskander@ee.utah.edu.

Toshiba TLCS-900 16-bit Microcontroller Family

When you've squeezed your current micro for all it's worth.



You've milked it for every last drop of functionality. Now it's time to take a look at Toshiba's new 16-bit family of microcontrollers, which will give you the perfect combination of performance and integrated peripherals.



The TLCS-900 increases performance four times over a typical 8-bit MCU, while the higher-performance TLCS-900/H is eight times faster. The low-power TLCS-900/L rounds out the family. All are highly integrated, featuring on-chip peripherals that include A/D and D/A converters, DRAM controllers, serial interfaces, real-time clocks, and ROM, RAM or Flash memory. This degree of integration yields a lower parts count, reduced system costs and increased reliability.

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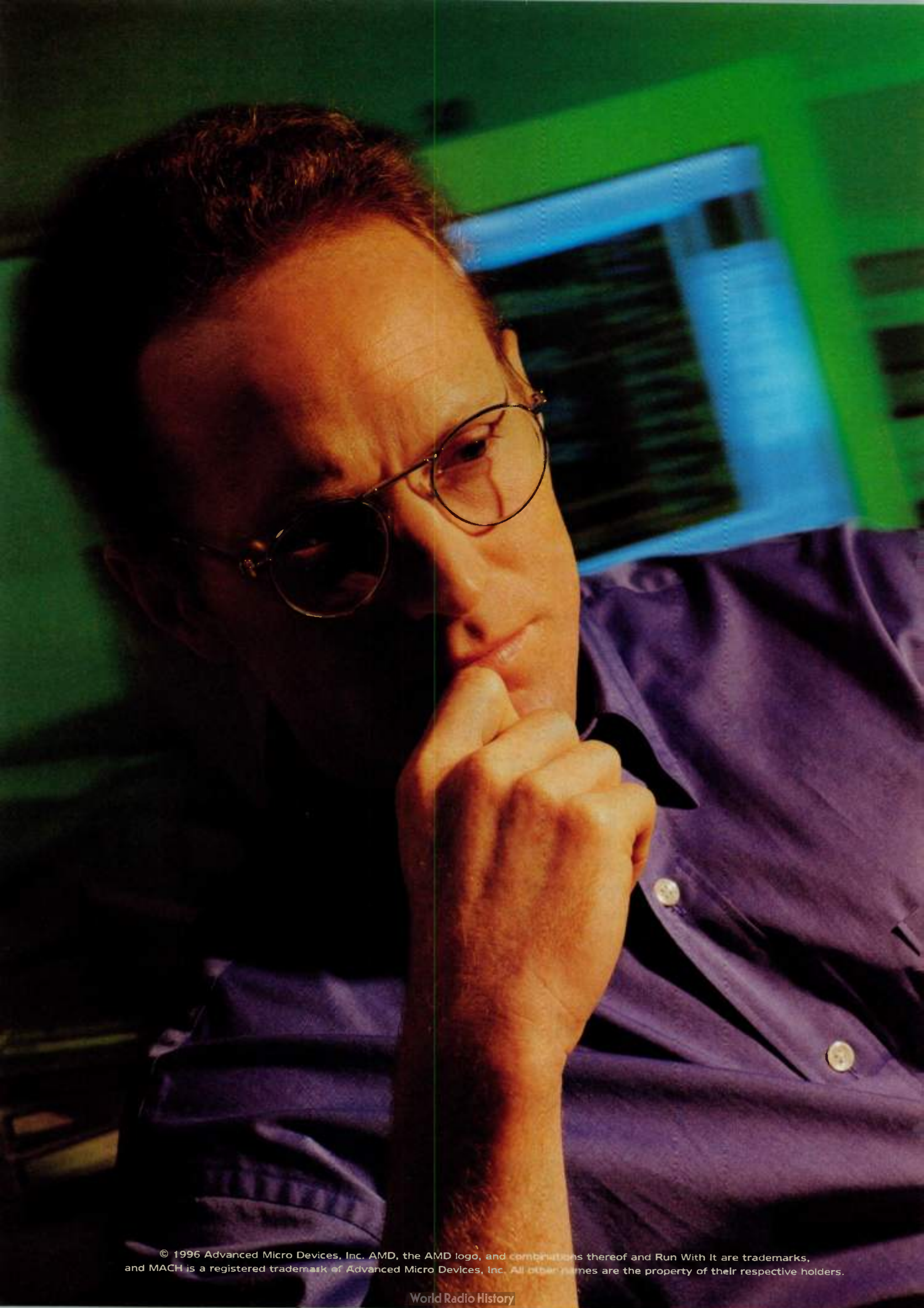

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IEEE International Conference on Computer Aided Design (ICCAD), Nov. 10-14. Red Lion Hotel, San Jose, CA. Contact Robert A. Rutenbar, Dept. of ECE, HH #3105, Carnegie-Mellon Univ., 5000 Forbes Ave. Pittsburgh, PA 15213; (412) 268-3334; fax (412) 268-2859; e-mail: rutenbar@ece.cmu.edu.

Miniature Card Implementers Forum Info Workshop, November 11, 1996. Tokyo, Japan. Contact Kevin Randolph, (800) 462-1042 or (619) 673-0870; fax (619) 673-1432; e-mail: mcif@annabooks.com; http://www.annabooks.com.

AUTOFACT 96 Conference & Exposition, Nov. 12-14. Cobo Center, Detroit, MI. Contact Society of Manufacturing Engineers, (800) 733-4763.

IEEE/EMI Advanced Semiconductor Manufacturing Conference & Workshop (ASMC), Nov. 12-14. Hyatt Regency Cambridge, MA. Contact Margaret Kindling, SEMI, 805 15th St. #810, Washington, DC 20005; (202) 289-0440; fax (202) 289-0441; e-mail: mkindling@semi.org.

Electronica 96, 17th International Trade Fair for Components & Assemblies in Electronics, Nov. 12-15. Munich, Germany. Contact Messe Munchen GmbH, Messegelande, D-80325 Munchen; (49) (89) 5107-229; fax (49) (89) 5107-174.

ACM/IEEE Supercomputing 96, Nov. 17-22. Lawrence Convention Center, Pittsburgh, PA. Contact Beverly Clayton, Pittsburgh Supercomputing Center, 4400 Fifth Ave., Pittsburgh, PA 15213; (412) 268-4960; e-mail: clayton@psc.edu.

LEOS 96, Nov. 17-22. The Westin Hotel, Boston, MA. Contact Melissa K. Estrin, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331; Piscataway, NJ 08855-1331; (908) 562-3896; fax (908) 562-8434; e-mail: m.estrin@ieee.org.

Surface Mount Technology Associations Third Technology in the Park Symposium, Nov. 18-21. Sheraton Imperial Hotel, Research Triangle Park, NC. Contact Sue Rectenwal, SMTA Headquarters, (612) 920-7682; smta@smta.org.

Asia Pacific Conference on Circuits & Systems (APCCAS 96), Nov. 18-21. The Swiss Grand Hotel, Seoul, Korea. Contact Jae Ho Chung, Inha University 253, Yonghyun-dong, Nam-ku Incheon, Kyunggi-do, 402-701 Korea: (82) 32 860 7420; fax (82) 32 866 7776.

IEEE Global Telecommunications Conference (GlobeCom 96), Nov. 18-22. QEII Conference Centre, Westminster, London, U.K. Contact Bob G. Blake, British Telecom Laboratories, Martlesham Heath, Ipswich, Suffolk 1P5 7RE; 44 473 644855; fax 44 473 647438; e-mail: blake_r_g@bt-web.bt.co.uk.

IEEE TENCON 96, Digital Signal Processing Applications, Nov. 26-29. Perth, Western Australia. Contact Australia Promotions Pty. Ltd., P.O. Box 1025, Bentley Delivery Centre, WA, 6983, Australia; (61) 9-470-2552; fax (61) 9-470-2556.

DECEMBER

DB/EXPO 96, Dec. 2-6. Jacob K. Javits Convention Center, NY. Contact Dave Codd or Karl Foster, Blenheim NDN, 1975 W. El Camino Real, Suite 307; Mountain View, CA 94040: (800) 2DB-EXPO; fax (415) 966-8934; e-mail: DBEXPONY@blen-usn.mhs.com puserve.com.

IEEE International Electron Devices Meeting (IEDM), Dec. 8-11. San Francisco Hilton & Towers, San Francisco, CA. Contact Melissa Widerkehr, Widerkehr & Assoc., 101 Lakeforest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: widerkehr@aol.com.

Winter Simulation Conference (WSC 96), December 8-11. Hotel Del Coronado, Coronado, California. Contact James J. Swain, Dept. IDE, University of Alabama, Huntsville, Alabama 35899; (205) 890-6749; fax (205) 890-6608.

35th IEEE Conference on Decision & Control, Dec. 11-13. International Conference Center Kobe & Portopia Hotel, Kobe, Japan. Contact Hidenori Kimura, Faculty of Engineering, Osaka University, Suita, Osaka 565, Japan; (810) 6 877 5111, ext. 5121.

Miniature Card Implementers Forum Info Workshop, Dec. 12. Austin, TX. Contact Kevin Randolph, (800) 462-1042 or (619) 673-0870; fax (619) 673-1432; e-mail: mcif@annabooks.com; http://www.annabooks.com.

JANUARY 1997

USELINUX: Linux Applications Development & Deployment Conference, Jan. 6-10. Marriott Hotel, Anaheim, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; http://www.usenix.org.

USENIX Technical Conference, Jan. 6-10. Marriott Hotel, Anaheim, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; http://www.usenix.org.

Annual Reliability & Maintainability Symposium (RAMS), Jan. 20-23. Philadelphia Marriott, Philadelphia, PA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

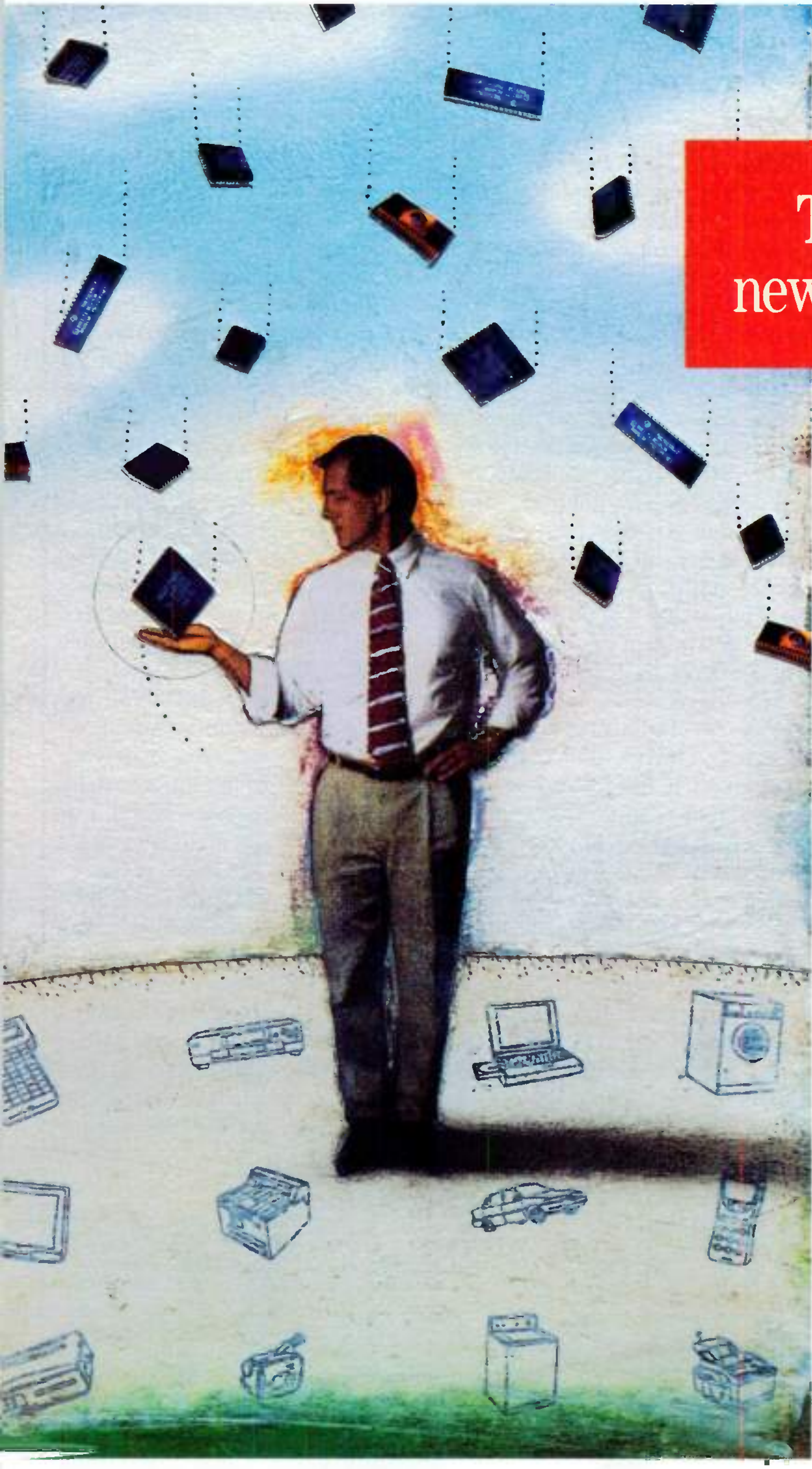
Second Annual Pan Pacific Microelectronics Symposium, Jan. 29-31. Sheraton Maui Resort, Maui, HI. Contact JoAnn Stromberg, Pan Pacific Symposium, 5200 Wilson Rd., Suite 215, Edina, MN 55424; fax (612) 929-1819.

FEBRUARY

IEEE Aerospace Conference, Feb. 1-8. Snowmass at Aspen, Colorado. Contact Stephen Franklin, Deputy Program Chair, 4800 Oak Grove Drive, Pasadena, California 91109; (818) 393-0814; fax (818) 393-0530; e-mail: stephen.f.franklin@jpl.nasa.gov.; http://chirp.plk.af.mil:1050/ieee/index.html.

IEEE Power Engineering Society Winter Meeting, Feb. 2-6. New York Hilton & Towers, NY. Contact Frank E. Schink, 14 Middlebury Ln., Cranford, New Jersey 07016-1622; (908) 276-8847; fax (908) 276-8847.

Second International Conference on Chip-scale Packaging, Feb. 20-21. Sunnyvale Hilton Inn, Sunnyvale, CA. Contact Subash Khadpe; (610) 799-0419; fax (610) 799-0519; e-mail: skhadpe@semitech.com.



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VIRTUAL SOCKETS

Something big is shaping up for the creative side of the electronics industry. The engineers who design ASICs may be getting a break that will diminish the drudgery of their jobs and release their pent-up creative energy now stymied by inadequate design tools on one hand and proprietary IC processes and cell libraries on the other. It's called the Virtual Sockets Interface (VSI), and it started with the tacit admission that the million-transistor ASIC designs that we have been hearing about for the past few years were not going to happen in any significant number. Unless, of course, the industry sets some standard way of assembling intellectual property such as cores and reusing customer-designed logic blocks from previous designs.

In essence, ASIC designers will have an environment analogous to the environment board designers have enjoyed for years. In a board design, pin-compatible chips from different IC houses can always be expected to work together. The big difference is that instead of plugging chips onto boards, ASIC designers will be plugging intellectual property into silicon. This is possible because of virtual sockets and standard buses that will be defined across the industry for the first time. If a piece of intellectual property conforms to the standard interface, it will be reusable again and again. It can be mixed and matched with other VSI-defined IP.

Once VSI's significant implementation problems are solved, we will undoubtedly see a revolution in the design industry. Companies such as Advanced RISC Machines (ARM) Ltd., Cambridge, U.K., will become a major driving force. Although ARM has just a few hundred employees around the world, its impact is much more significant because of its leveraged business model. For every engineer on the ARM payroll, you can count up to 20 engineers in its partner companies that also are working on enhancing ARM's RISC cores.

Since much is at stake in the VSI initiative, we can expect that there will be attempts to derail it. One argument that will be raised is "commoditization." If all this IP is out there for anybody to use, the argument goes, how will companies achieve product differentiation? The answer is simple. The creativity of the chip architects will make the difference. But even if one accepts the commoditization argument, there is a bright side. Putting the ability to design of million-gate ASICs into the hands of hundreds (perhaps thousands) of design teams will result in a proliferation of affordable products of all types. In other words, the market for electronics will grow, and that's good news for everybody. *jshandle@class.org*


Editor-in-Chief

How Do We Get To Lower-Power ICs?

I recently returned from the 1996 International Symposium on Low Power Electronics and Design. It was a conference dominated by papers from academia and the R&D labs of large systems houses such as Lucent Technologies and IBM. It provided an interesting window on a rather vital pin (or pins) of every IC package. That is: To what minimum and maximum voltages will the V_{DD} pin be required to connect? No concern is given as to whether it will be available. That is assumed.

The majority of the papers also assumed the SIA road map was "real" and would be followed to the end without regard to economic practicality. But that's another story. The papers that were presented assumed that power-supply voltages would drop *below* 2 V. Unlike last year's conference, there was no talk of logic running off 100-mV supply voltages while immersed in liquid nitrogen. Many papers were divided between process techniques, and circuit or system design techniques, that might further cut the power required by digital ICs. Some papers described mixed-signal systems working off low voltages, and others described sophisticated software designed to simplify logic-circuit redundancy. Although most of the papers described analog solutions to so-called digital problems, others described pure analog circuit problems such as cutting the power devoted to clocks, phase-locked loops, line drivers, and even a few data converters.


FRANK GOODENOUGH
ANALOG & POWER

There was talk of "triple-tub CMOS," as well as adiabatic logic and other techniques aimed at beating the CV^2 dissipation problem. As supply voltages drop, to maintain performance gains provided by moving to sub-submicron CMOS, MOSFET threshold voltages must be lowered—a tricky business. Triple-tub CMOS gives logic designers flexibility. Two tubs contain n-channel FETs (one holds a FET with a conventional threshold voltage, the second sports a FET with a lower threshold voltage), and the third holds the p-channel FET.

An evening panel discussed the relative importance of circuit/system design tied to special low-power synthesis software versus innovative, ultra-low-power process technology. There was little controversy. The panel members agreed that the processes came first and then low-power designs based on them.

Adiabatic logic and similar energy-recycling schemes involving pre-, pulse-, or slow-charging of capacitors at first seem like black magic, anti-gravity, or perpetual motion, but their proponents claim they work. In fact, a logic family called "domino logic" was developed to implement it. (I'll believe it works when I see it described someday in an *Electronic Design* cover story.)

A paper by researchers at Stanford University described a digital switching power-supply controller for variable-frequency and voltage circuits. They put a ring oscillator and a PWM synchronous buck-regulator controller on a digital chip. The inductor, capacitors, and power MOSFETs were off-chip. The oscillator determined the minimum supply voltage required to operate at a clock frequency that maximizes energy efficiency. The output of the supply was slaved to this voltage. As the CV^2 load on the supply changed, both its PWM frequency and its output voltage changed.

I wonder if a similar approach can be used to optimize the supply voltage of a power supply for ultra-fast advanced microprocessors instead of cherry-picking it at the factory and creating a 4- or 5-bit code on processor pins to set the regulator's output. The ring oscillator adjusts the supply voltage so that it oscillates at a maximum frequency, or at minimum power dissipation at some desired clock frequency.

Copies of the Digest of Technical Papers (IEEE Catalog #96TH8211) are available from the IEEE Service Center, 44 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; or by using ACM Order #477964 at (800) 342-6626; Europe: +44-1-865-382338.

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HEARING-IMPAIRED PLACE CALLS IN SIGN LANGUAGE

A three-month trial underway in Texas enables people who are hard of hearing, speech-impaired, and/or deaf to communicate electronically in American Sign Language. Until now, hearing-impaired subscribers relied on inexpensive telephone text terminals (TDDs) to pass messages to each other. Specially equipped operators, known as relays, currently provide text-to-speech/speech-to-text services, allowing the hard of hearing to use operator assistance or directory services, as well as communicate with telephone users. Recently, some hearing-impaired individuals have been using computer videoconferencing technology, which permits them to communicate in their native sign language. Unfortunately, they must still rely on TDDs to access operator services and "talk" with hearing people. The experimental service, jointly developed by Sprint Communications and the Texas Public Utility Commission, will demonstrate the feasibility of providing the same relay services using videoconferencing technology.

Known as Relay Texas Video, the three month trial will provide traditional relay services for the deaf using videoconferencing technology. A Sprint interpreter viewing the live video relays the conversation in voice or sign language with the person being called. Individuals anywhere in the state can participate, providing they're rigged with the proper equipment. Basic requirements are an ISDN line and a desktop computer equipped with an H.320-compatible videoconferencing system. For individuals who don't have the hardware at home, public facilities were installed in Austin, Big Springs, Dallas, El Paso, Fort Worth, Pharr, and Corpus Christi, with others to possibly follow. The service will be available until November 30, 1996 from 8 A.M. through 8 P.M. A video relay operator can be reached by calling 888-VRI-TEST. For further information about the project, call James Fisher at (202) 828-7406. *LG*

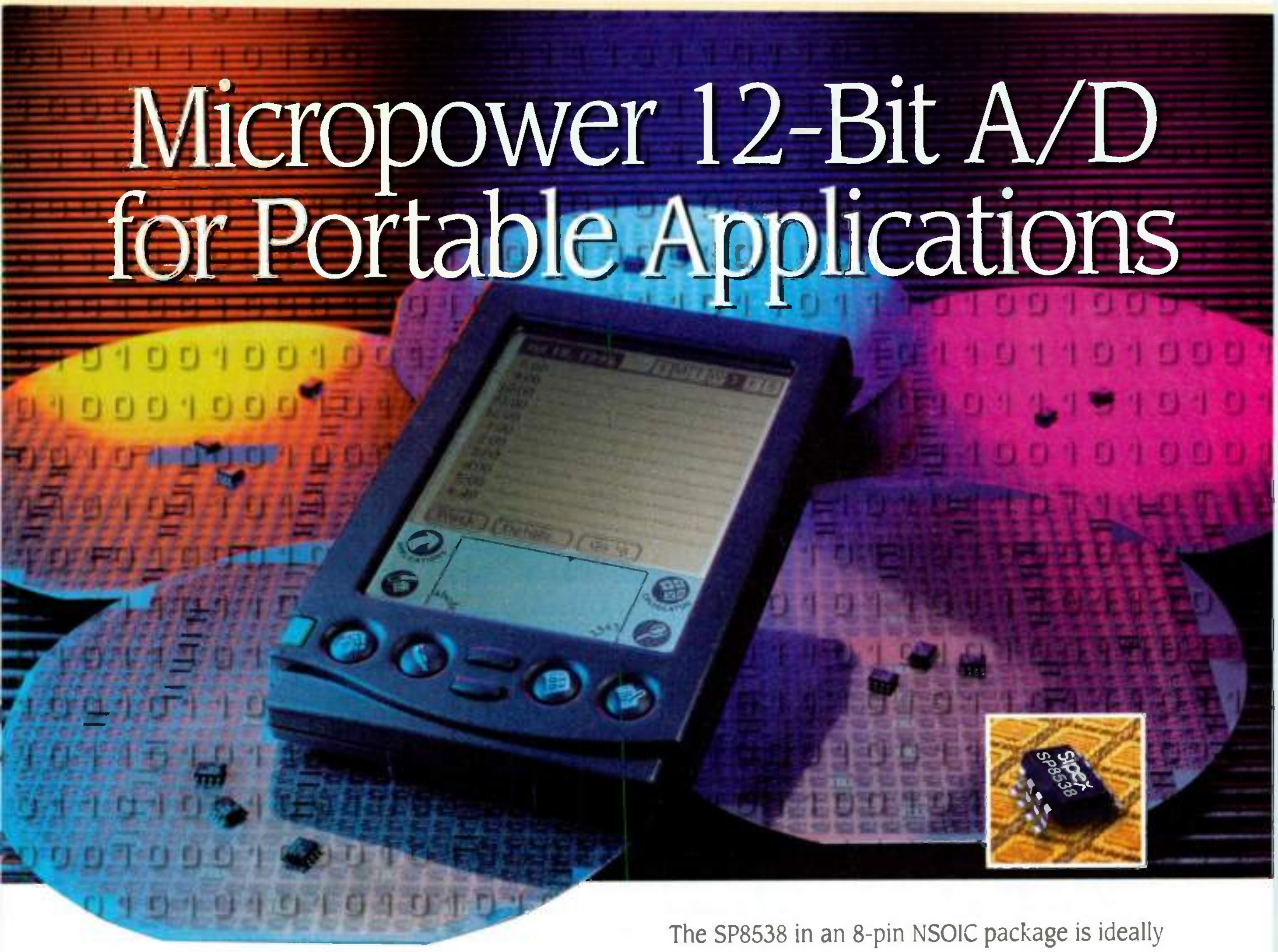
VIRTUAL SCREENING USED TO DETECT COLON CANCER

Biomedical engineers are using virtual-reality imaging to develop a colon cancer screening test that's more comfortable, convenient, and less expensive than the standard exam. David Vining, M.D., assistant professor of radiology at the Bowman Gray School of Medicine, Rosslyn, Va., has developed a method of using a spiral CT scan to build a three-dimensional image of the entire colon. The scan itself takes about 50 seconds. The patient lies on a table, which moves through a rotating X-ray beam. Minutes later, the patient can go home. The X-ray data then is processed into a computer image that's color-enhanced—the brightly colored areas indicate the location of the polyps. Another major advantage of the virtual exam is cost. A colonoscopy typically costs from $900 to $1500, while the virtual exam using spiral CT might cost $450 to $650, says Vining.

A preliminary study in 30 patients showed the test to be as accurate as a colonoscopy. However, the image processing takes too long for routine clinical use. Vining's group is working to reduce the image-processing time and improve clarity. Plans are to screen 200 volunteers to assess improvements in the system and compare results with those of a colonoscopy. For further information, contact Frank Blanchard at (703) 528-2430; e-mail: fb@whitaker.org, Web: http://bme.www.ecn.purdue.edu/bme. *RE*

POROUS SiC EXPECTED TO YIELD INNOVATIVE DEVICES

It's expected that porous silicon carbide (SiC), like porous silicon (which has been extensively researched), will produce novel semiconductor devices. By suitable choice of the macrostructure, microstructures, and compositions of the porous regions, it can produce ultraviolet light-emitting diodes, ultraviolet lasers, blue electroluminescent devices and chemical-sensor filters. One method that's already been developed involves electrochemical etching on an SiC wafer. The wafer is mounted on a carrier with a nickel contact, and covered completely with a black wax barrier except for the region to be made porous. The etching fluid in the vessel is 2.5% hydrofluoric acid and the reference electrode is a saturated calomel, with a platinum wire counter-electrode. A bias is applied to the contact on the wafer with respect to the calomel electrode. Where needed, SiC can be oxidized to insulating silicon dioxide at a much faster rate when it's made porous by this method. The electrochemical etching can be repeated as is necessary and the process can be accelerated with ultraviolet light. For more information, contact Joseph Shor or Anthony Kurtz, NASA-Lewis Research Center, Cleveland, Ohio, at (216) 433-4000. *PMcG*



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VIDEO DISPLAY TECHNOLOGY ENABLES TRANSPARENT 3D COLOR IMAGES INSIDE CLEAR FLUORESCENT GLASS

A graduate student at Stanford University, Stanford, Calif., Elizabeth Downing, has developed a novel 3D video display technology that not only utilizes a new method of producing three-dimensional images, but provides significant advantages over available 3D technologies. Manufactured through funding from a $350,000 grant from the U. S. Navy in 1993, as well as support from the U. S. Defense Advanced Research Projects Agency (DARPA), the display effectively marries a number of key components including semiconductor lasers, fluorescent glasses, and scanners. In conjunction with these governmental agencies, the project was also assisted by researchers from SDL Corp., San Jose, Calif., who provided the required diode lasers and other associated electronics, and Robert Macfarlane, an expert in upconversion, IBM, San Jose, Calif., who helped identify the proper glasses needed to create the display's three different colors. While at the moment only a prototype, the display device, roughly one square foot in size, is able to produce 3D color images inside a sugar-cube sized solid fluorescent glass cube.

The concept of displaying 3D objects in fluorescent glass dates back to the mid 1960s. It was not until recently, however, that the technology had advanced enough to make such a concept plausible.

In fact, the difficulties that can arise from working with fluorescent glass have only now been solved. For example, finding the appropriate glass mixtures to use for the 3D video display would have been virtually impossible 20 years ago, because the variety of fluorescent glass materials available today simply didn't exist.

As opposed to some of the more conventional 3D technologies, the 3D video display technology creates an image that doesn't just appear to be three dimensional. Rather, it is actually drawn in three dimensions. Consequently, more than one person can view the image at the same time. Reminiscent of a limitation that affects holographic or stereo pairs (techniques for producing 3D images), the 3D video display produces emissive, as opposed to reflective images. The advantage of this feature is that the images can be easily seen in ordinary room light.

At the heart of the 3D fluorescent glass display is a scientific principle known as "upconversion." According to this principle, when certain atoms from the rare-earth family are struck in rapid succession by two infrared laser beams of light of slightly different wavelengths, visible light is emitted. To translate this fact into a working display, small amounts of these atoms are doped into a cube of fluorescent glass as impurities. Then, two infrared laser beams are directed through the glass. At their point of intersection, a point of visible light is created. Then, the two laser beams are scanned vertically, horizontally, backward, and forward through the volume of the cube. Through strict control of the points where the two beams intersect, visible images are produced. To date, this method has successfully produced 3D wire figures, surfaces, and simple solid shapes.

To generate color images, the fluorescent glass display utilizes another well-known technique whereby impurities that create red, green, and blue colors are mixed into the fluorescent glass in separate layers. Next, these layers are placed very close together. Then, as the laser beams enter the glass, adjacent color layers are stimulated at approximately the same time, causing the different colors to fuse into a single colored dot.

In the current prototype model of the display, three thick layers of glass, each doped with the impurities that create red, green, and blue, are employed. Consequently when looking at the image, a pink object appears in front of a green object that appears in front of a blue object. In an actual display, however, 3D objects of any color could easily be created by utilizing thousands of groupings of red, green, and blue doped glass layers.

The display, while still in development, has two foreseeable drawbacks. Primarily, since the surface images formed are transparent, unlike most 3D technologies which are opaque, a certain number of applications, such as television or desktop computer displays, would be virtually impossible. Other applications, such as medical imaging and scientific simulation, would see this as an advantage since transparent images accurately show all the features of an object.

Another disadvantage of the display technology is that it takes roughly 500 times as much data to construct a 3D object as it does to draw the same object in only two dimensions. To overcome this limitation, holographic storage technology is being investigated. With its high-speed data-transfer capability, it is conceivable that this technology could effectively be used to drive the fluorescent glass display in the future.

Of all the potential applications for which the display could be used, the one that holds the most promise is medical imaging. Currently, the technology in use for MRI, CAT-scan, and ultrasound imaging requires a series of two-dimensional flat pictures on different planes to be stacked on top of one another. Images produced by this technology are opaque, potentially hiding some of the features of a surface being examined—a distinct disadvantage. On the other hand, the new 3D video technology can produce more accurate images leading to more accurate diagnosis. With the current projected cost of a 10-in. fluorescent glass display at roughly $80,000, this improvement in clinical diagnosis is expected to more than justify the cost.

Further investigations relating to the 3D video technology include appropriate storage technologies, methods for sizing up the display, and avenues of commercialization.

For more information, contact the Stanford University News Service at (415) 723-2558, email: info@news-service.stanford.edu, or the www at: http://www.stanford.edu/news/.

CHERYL AJLUNI

ADVANCED PROCESSORS AND GRAPHICS/MULTIMEDIA CHIPS MAKE THEIR DEBUT AT THE MICROPROCESSOR FORUM

Providing a glimpse into the near future, presentations at this week's Microprocessor Forum, the Fairmont Hotel, San Jose, Calif., whetted designers' appetites for high-performance, feature-rich processors. Boasts of CPUs with new highs in floating-point performance, instruction sets enhanced for processing video, new features to streamline memory use, as well as other enhancements dominated many of the sessions.

Additional presentations covering graphics and multimedia showed off the efforts of many companies to develop dedicated and programmable processors for all aspects of multimedia.

In a session dedicated to advances in the X86 architecture, Intel Corp., Santa Clara, Calif., detailed the multimedia extensions that it has embedded in the microarchitecture of the forthcoming enhanced Pentium processor, the P55C (ELECTRONIC DESIGN, *May 13, p. 44*). And countering the MMX efforts that Intel has put forth, designers from Cyrix Corp., Richardson, Texas, unveiled the details of the M2 processor, a 6x86-class CPU with MMX-like instructions, a larger cache and additional enhancements. In addition, Advanced Micro Devices Inc. (AMD), Austin, Texas, gave designers a peak at the K6, its next-generation CPU that includes multimedia enabling features and a new microarchitecture that provides a significant performance boost over the company's previous chip, the K5. The K6 will be performance-competitive with the Intel Pentium Pro processors.

The Cyrix M2 will include a superscalar X86-compatible core with optimizations for both 16- and 32-bit code, and the ability to operate at clock rates from 180 to 225 MHz (initial releases). The chip will be able to drop into a 6x86 socket and packs about 6 million transistors into a chip area of less than 200 mm^2 thanks to a 0.35-µm, 5-layer metal process. A total of 57 new instructions have been added to the X86 instruction set that will provide full MMX compatibility.

On the processor chip, Cyrix's designers spent more than half their transistor budget on the 64-kbyte unified cache and other smaller translation buffers, line caches, branch history table, branch target cache, and return stack. Enhancements to the data path and floating-point unit allow them to handle new data types as well—packed byte, word, double-word, and quad-word formats and eight new media registers support the multimedia operations. Like the Intel MMX operating mode, the Cyrix extensions do not require a new processor state; they use existing floating-point context switch mechanisms, thus providing compatibility with existing operating-system and application software.

The rising importance of multimedia in home as well as business applications has started to make its impact on the world of CPU design. Over the last few years, Hewlett-Packard Co. (H-P), Cupertino, Calif., and Sun Microsystems Computer Co., Mountain View, Calif., have both modified their CPU data paths and added instructions to better manipulate video data and execute MPEG algorithms. Now, Intel, Cyrix, and AMD have done the same, and more companies also are following suit.

For example, Digital Equipment Corp. (DEC), Hudson, Mass., has extended the Alpha instruction-set architecture to reduce the overheads in processing motion video, and the MIPS Technologies Division of Silicon Graphics Inc., Mountain View, Calif., also detailed extensions to the MIPS architecture and instruction set that will accelerate the computations needed to process multimedia data streams.

Peter Bannon, a processor architect at DEC, detailed the motion-video instruction enhancements to the Alpha, which will allow host-based MPEG-2 video encoding for future Alpha-based desktop systems—the first CPU chip to do real-time encoding without hardware assist. The commands support single-instruction/multiple-data (SIMD) operations and provide Pack and Unpack instructions for pixel merge and de-merge parallel operations. The extensions also provide clamping instructions for saturation control

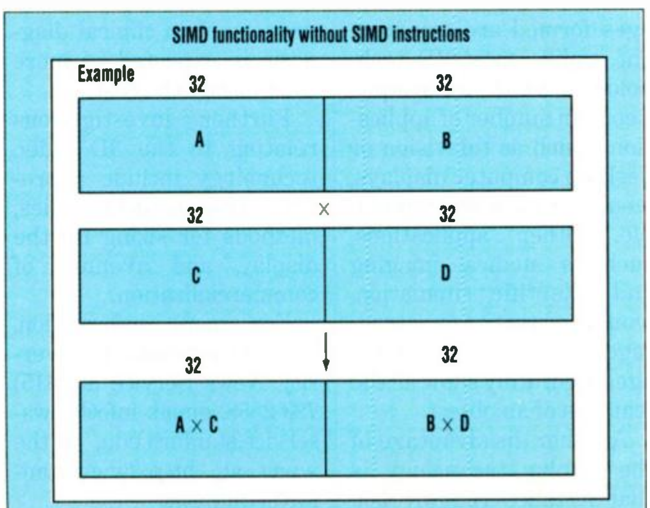

Fig. 1

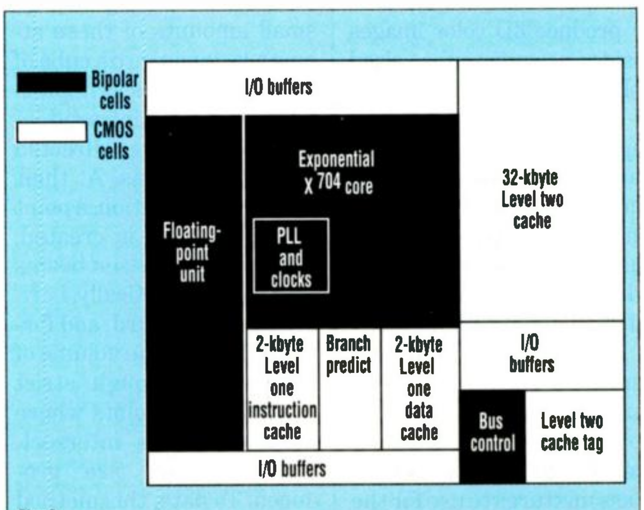

Fig. 2

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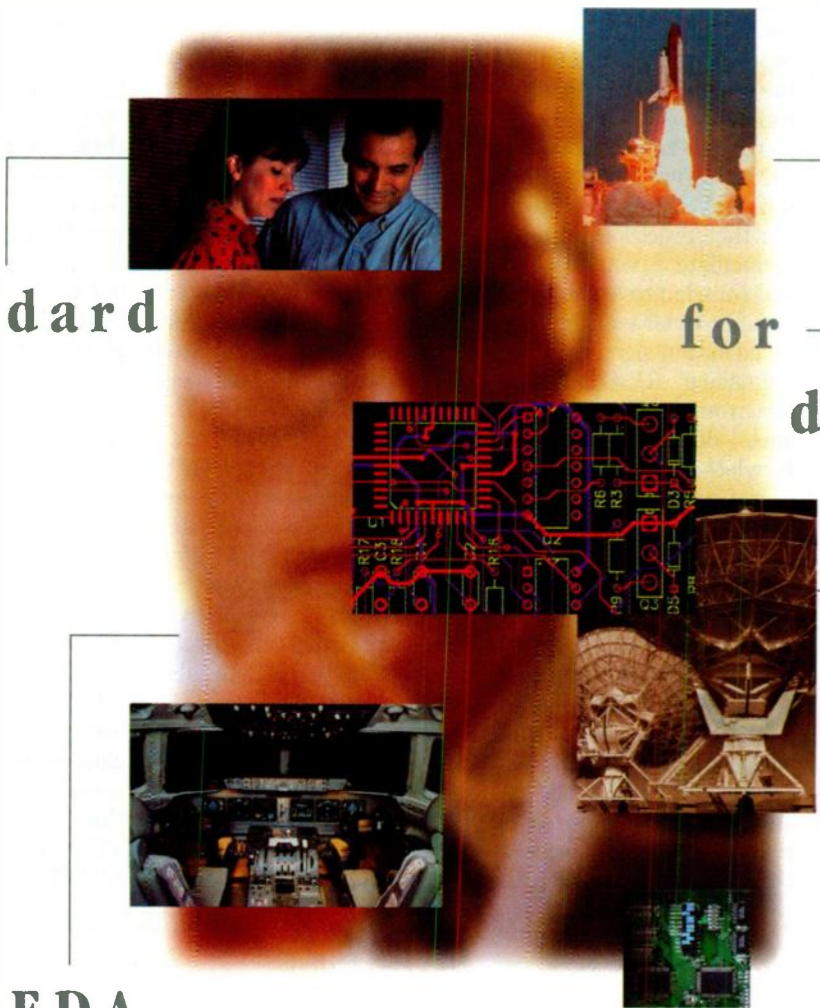

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on pixel operations. Another key addition to the instruction set is a pixel-error instruction—this command replaces a sequence of about ten instructions that would be needed when executing motion-estimation algorithms. This instruction reduces the CPU overhead on motion estimation from 61% to only 15%, thus freeing up considerable CPU resources for other tasks.

Designers at MIPS have made similar observations about the benefits of optimizing the instruction set for multimedia and have thus created the MIPS V instruction set architecture, which was unveiled at this week's conference. Part of the enhanced architecture is a split 64-bit data path that allows for what the company calls paired single data types—SIMD functionality without SIMD instructions. Basically, the 64-bit-long data word is divided into two 32-bit subwords, which are treated as independent values but synchronized to the flow through the data path *(Fig. 1)*. In the case of a floating-point multiplication, the first two numbers are loaded into a 64-bit register that is split into two 32-bit registers, C and D. Then the next two numbers are loaded into another 64-bit register that is also split into two sections, A and B.

When the multiplication occurs, A is multiplied with C, and the 32-bit product is saved in a third register (half of a 64-bit register). Similarly, the product of B times D is saved in the other half of the third 64-bit register. Consequently, two results are produced every instruction cycle. That lets the processor to deliver twice the floating-point throughput of previous versions—ideal for many 3D graphics algorithms.

The enhancements included in the MIPS V architecture, the MDMX instruction extensions, consist of many new instructions for signal processing. One new feature is the ability to split the data path into as many as eight subsections that can operate in SIMD fashion, executing up to eight identical operations in parallel and providing up to an eight-fold reduction in algorithm execution time. Unlike other processors that accumulate the results in their 64-bit accumulator, MIPS' designers increased the accumulator to 192 bits. That allows each of the eight computations to retain their precision during intermediate computations and thus improve the visual or audio quality of the processed output signals.

Pushing RISC architectures to even higher performance, designers at DEC, Hewlett-Packard Co., IBM Corp., Austin, Texas, Quantum Effect Designs Inc., Santa Clara, Calif., and Exponential Technology Inc., San Jose, Calif., presented details of their next-generation processors. With about double the throughput of almost every other processor now shipping, the 21264, a superscalar version of the DEC Alpha processor, gets much of that performance increase through the use of an aggressive out-of-order execution scheme and clock speeds that exceed 500 MHz.

Tackling extensions to well-established product lines, designers at Quantum Effects Designs detailed an extension to the MIPS IV architecture targeted at low-cost workstations and high-end embedded markets. Targeted for operation at an internal clock frequency of 300 MHz, the RISCMark 7000 will be fabricated in a 0.25-µ CMOS process that yields a chip area of just 80 mm^2. That will result in an estimated performance of more than 10 SPECint95 and also greater than 10 SPECfp95.

The chip employs a two-way superscalar architecture with large, integrated level-1 and level-2 nonblocking write-back caches. The level-1 instruction and data caches are 16 kbytes each, and both have 4-way set associativity and a 32-byte line size. The L2 cache is 256 kbytes and is also 4-way set associative and has a 32-byte line size. An off-chip level 3 cache of up to 8 Mbytes also can be added.

The system interface allows for two simultaneous outstanding read operations, and a mode bit is included to allow the chip to be setup in a backwards-compatible operating mode for the R4600 and R5000 CPUs. And for debugging support, the chip includes two watch registers with mask fields that can be configured to watch for data or instruction activity. Also included on the chip are performance counters and JTAG boundary-scan test logic.

In addition, H-P disclosed details on the PA-8200, a follow-on to the PA-RISC 8000 that will eliminate some of the system bottlenecks H-P designers encountered with their first 8000-family member. Aiming for the highest floating-point throughput of any IBM microprocessor to date, designers from IBM detailed the P2SC Power2 Super Chip, a single-chip implementation of the Power architecture.

Unannounced but included in the program at the conference are the first details of the biCMOS implementation of the PowerPC architecture by Exponential Technology. The X704 CPU is a bus-compatible extension of the PowerPC60x architecture that can operate at internal clock speeds of 466, 500, or 533 MHz. Such high clock rates and a superscalar architecture that issues up to three instructions each cycle allow the chip to deliver a SPECint95 rating of be-

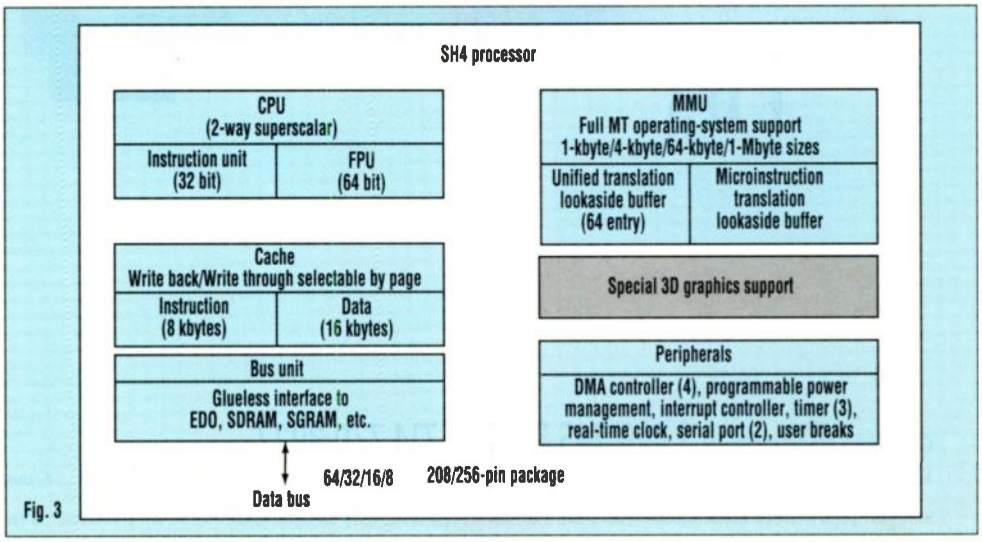

Fig. 3

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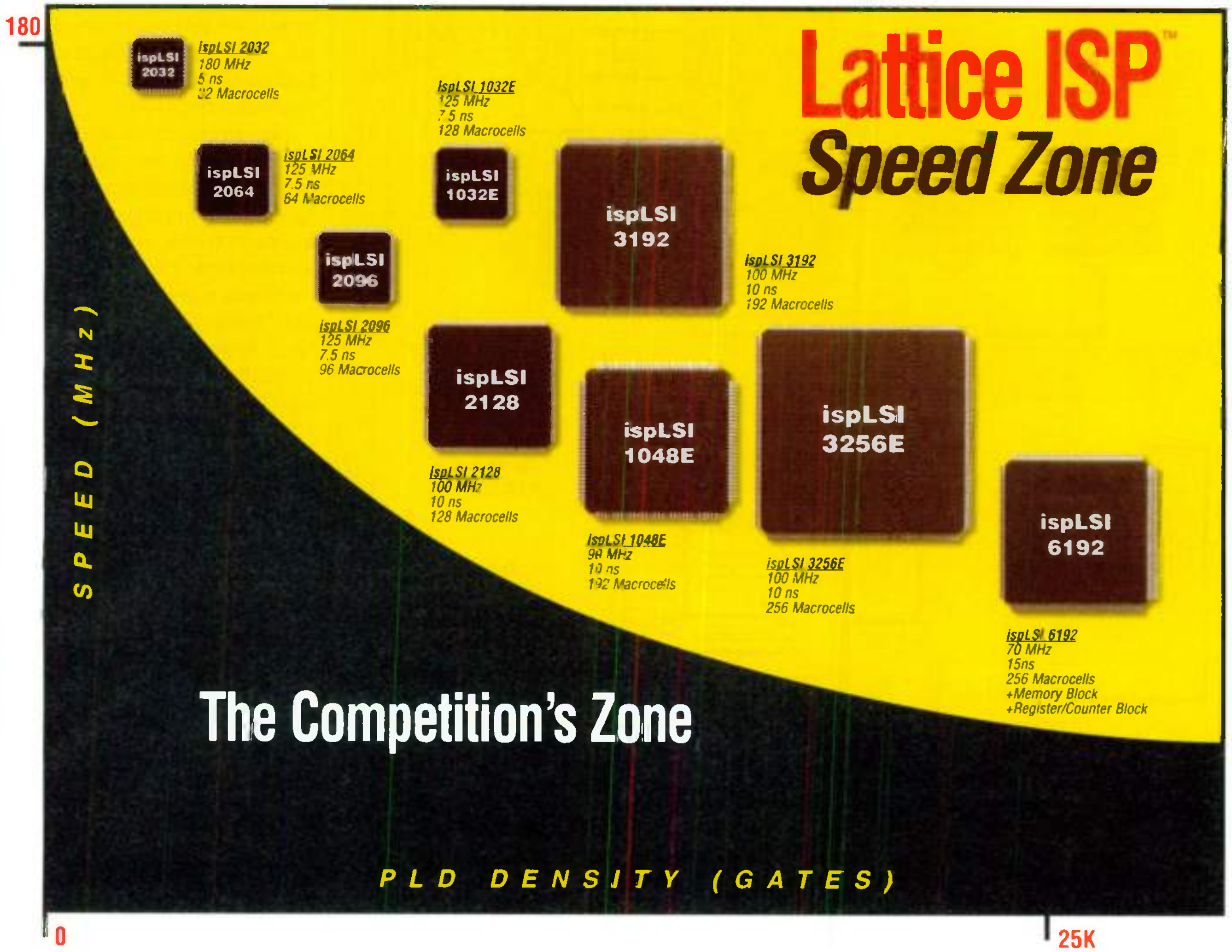

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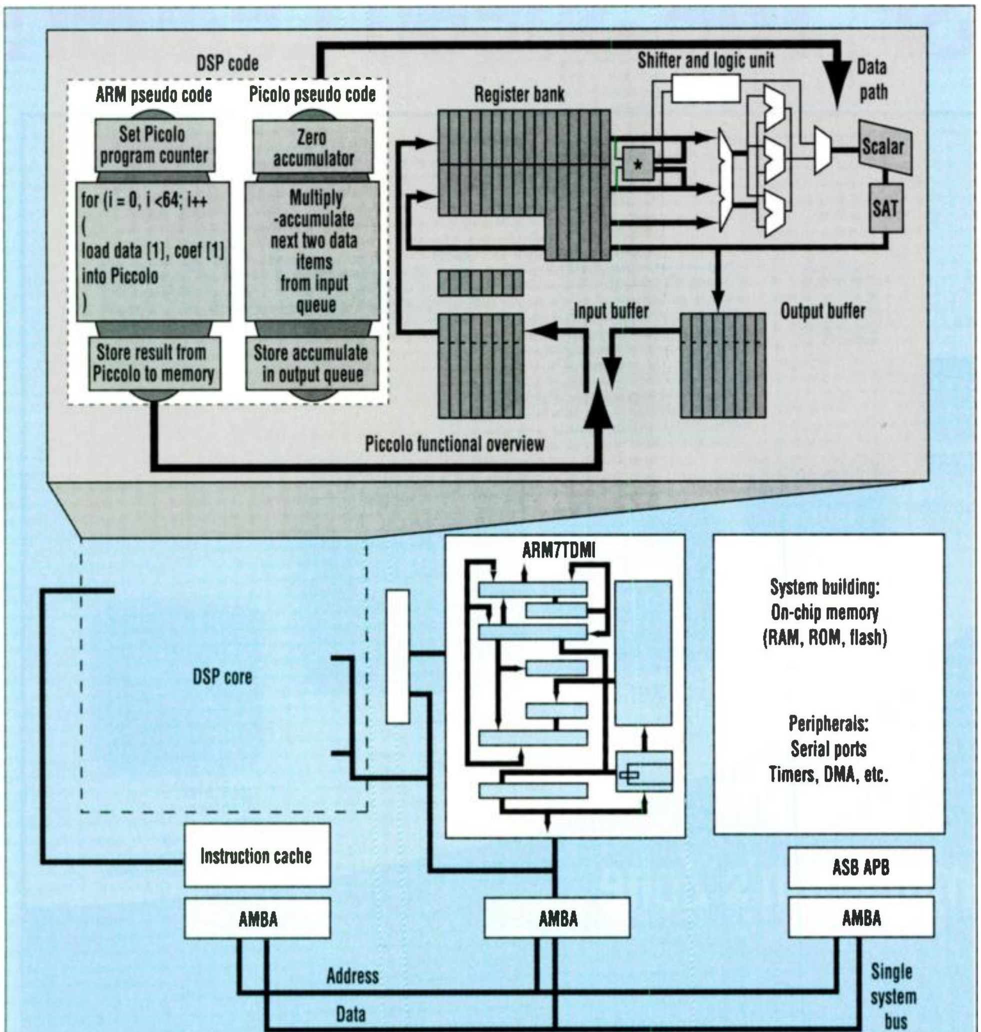


Fig. 4 ARM signal-processing architecture

tween 11 and 13. And since the chip is bus-compatible with the 604, it can work with existing PowerPC chip sets such as those from Apple Computer Inc., Cupertino, Calif., or the Firepower processor (now part of Motorola).

Implemented in a 0.5-µm biCMOS process, the chip combines high-speed bipolar logic with dense low-power CMOS cache memory *(Fig. 2)*. Thus, the chip occupies less than 150 mm^2 and will be housed in a 356-lead BGA package that has a built-in heat spreader to help deal with the expected 75-85 W of power the chip will dissipate. A unique on-chip Blast-Cache interface between the dual internal Level 1 instruction and data caches (2 kbytes each) and a unified 32-kbyte Level 2 cache provides an 8-Gbyte/s peak transfer bandwidth between the two levels over two independent 64-bit data paths. The dual on-chip caches and the fast updates improve the cache hit ratio and CPU throughput.

The x704 architecture allows up to three instructions to be issued every cycle and employs superscalar extensions, a six-stage internal pipeline, and strong branch prediction (and fast recovery from mispredicted branches) to minimize program execution overheads. Up to five unresolved branches can be handled, and just three cycles are needed to recover from a mispredicted branch.

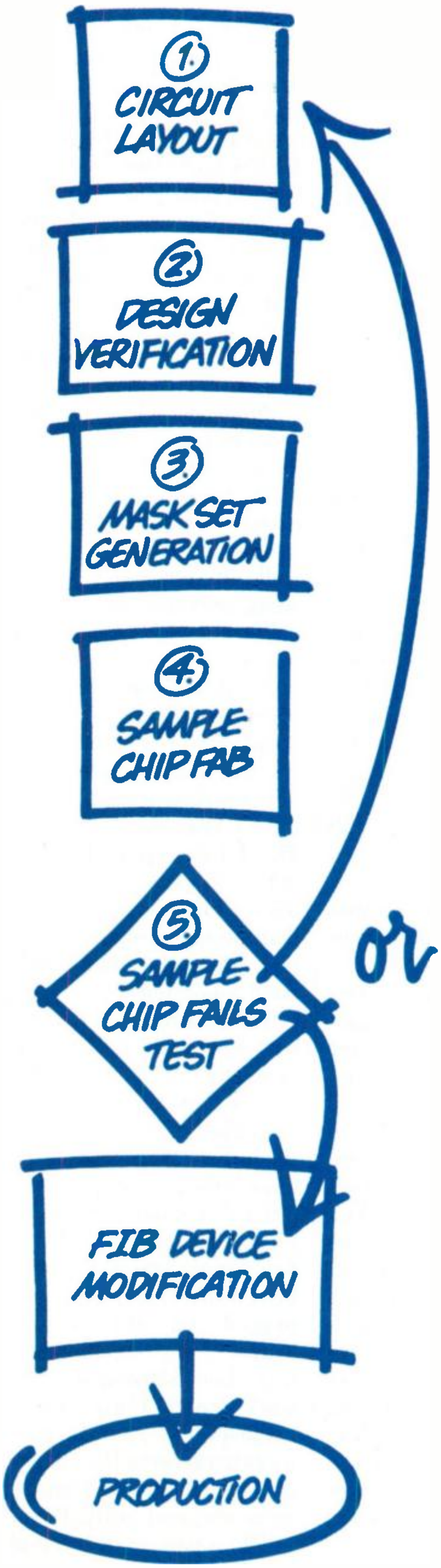
RISC-based embedded processors also will benefit from architectural and process improvements. The first superscalar implementation of the SH architecture was divulged by Hitachi America Ltd., the SH-4, while Sun Microsystems detailed the core architecture of the picoJava processor, including a description of the special hardware support integrated on the chip to support the Java byte-code instruction set.

Three additional MIPS-compatible processors were also unveiled, one for low-end desktops and high-end embedded systems developed by Quantum Effect Design, another by LSI Logic Corp., Milpitas, Calif., targeted at cost-sensitive applications, and a new member from the ARM camp, the Piccolo, with an architecture that merges DSP and microcontroller functions.

Like previous members of the SH family, the superscalar SH4 processor developed by Hitachi employs a 16-bit instruction set and is upward-compatible with all members except for the SH-DSP version. Employing a 2-way superscalar architecture, the chip can deliver a top throughput of 360 MIPS when clocked at 200 MHz. Yet it consumes just 1.8 W *(Fig. 3)*. With first silicon expected in the first quarter of next year, Hitachi plans to initially fabricate it with a 0.35-µm, four-level metal CMOS process. But by mid-1998, it will shift to a 0.25-µm rule set that should yield a chip area of just 6.5 by 6.5 mm. The low-power design techniques used—such as pass-transistor logic—also allow the company to offer a lower-power version that consumes just 100 mW when clocked at 100 MHz.

Targeted at graphics, the chip includes a special 128-bit processing block that handles 3D graphics geometry computations in conjunction with the on-chip 64-bit floating-point unit. The combination achieves a peak throughput of 1.4 GFLOPS when running at 200 MHz.

Internally, the main data path of the SH4 includes a 32-bit integer unit, a 64-bit floating-point unit, a cache subsystem that contains 8 kbytes of instruction cache and 16 kbytes of data cache, and a bus interface that provides a glueless interface to extended-data-output (EDO) DRAMs, SDRAMs, SGRAMs, and other memories. Also included on the chip is a memory-management



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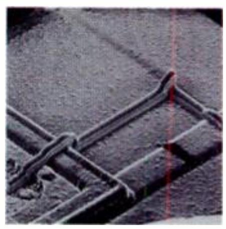
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unit (MMU) with a unified 64-entry translation look-aside buffer (TLB) and a 4-entry microinstruction TLB, the graphics processor, and peripherals—a DMA controller, three timers, real-time clock, dual serial ports, an interrupt controller, and programmable power management.

First details of the picoJava core architecture were also disclosed by Robert Garner, director of Java Media Processors at Sun Microelectronics. The processor is aimed at providing fast, native execution of Java byte codes with no code-size expansion. To do that, its designers defined the picoJava I CPU to include a simple RISC-style four-stage pipeline with a 64-entry hardware stack with a background spill and fill algorithm. The algorithm ensures data in the stack is kept current—when the stack overflows, the algorithm writes the oldest data back into the cache, and when the stack empties, the algorithm reloads the stack with the latest data. And to improve the performance of the stack, the picoJava-I executes the extra load operations associated with the stach architecture simultaneously with the compute instructions, thus hiding about 60% of the load operations.

The architecture can switch tasks quickly, provides a low interrupt latency, includes hooks for in-circuit emulation support, handles big- and little-endian data formats, and allows for instruction breakpoint and address watchpoint traps to ease software debugging. Some simple benchmarks for the picoJava-I include javac and raytracer that can be run on Intel Pentium processors using just-in-time compilation or an interpreter. In those two cases, and normalizing the Pentium performance to 1 (at 100 MHz), the interpreted code for javac and raytracer, respectively, executes at 0.46X and 0.37X that of the Pentium. On the other hand, the same benchmarks execute at 5.2X and 5X that of the JIT compilation (for the picoJava-I simulated for a clock speed of 100 MHz).

The Java instruction set consists of about 200 op codes that are divided into five categories—arithmetic, shift, and logical, constants, conversions, and stack operations in the first category; load/store from local variables and object fields in the second; control transfer and compare in the third; method invocation and return in the fourth; and lastly, array, object, monitor, exception, and several other commands in the fifth group. Most instructions will execute in one to three instruction cycles, with the underlying mechanism for instruction ranging from hardwired for the fastest-executing operations, state-machine and microcode-driven operations for more complex, not as time-critical commands, and trap and emulate mechanism for the most-complex infrequent operations.

Moving from the high to the low end, the TinyRISC from LSI Logic uses a similar strategy as put forth by Hitachi—it has 16-bit instructions to minimize code space. The initial version will be the TR4101, a 2-mm^2 core that can be used in ASIC designs. The 32-bit CPU consumes 1 mW/MHz when operating from 3.3V. Lower-power and higher-performance versions are in development.

Based on the recently-released MIPS16 architecture, the TinyRISC employs a new instruction set that allows mixed-mode operation with both 16- and 32-bit commands. The CPU uses a true subset of the MIPS I and II architecture and employs a three-stage pipeline with a unified instruction/data path. Most of the 32-bit instructions can be translated into a 16-bit format and internally decompressed on-the-fly into a 32-bit format.

The TinyRISC core can operate at a maximum clock frequency of about 70 MHz, delivering a throughput of about 60 Drystone MIPS. Verilog and VHDL models are available for designers to use in their ASIC designs. A hardware evaluation chip also will be available.

Many of today's applications are demanding both control capabilities and the ability to process signals (everything from servo loops to audio). To do that, designers at Advanced RISC Machines Ltd. (ARM) developed a merged CPU/DSP architecture dubbed Piccolo that was described at this week's conference. The chip consists of an ARM 7TDMI processor core (the Thumb core) and a high-performance DSP block (120 MIPS and a 32-bit instruction set), as well as on-chip caches and peripherals *(Fig. 4)*.

In the combined architecture, the Piccolo DSP block has its own program counter and instruction set, and fetches all of its instructions from a private buffer. On the other hand, the ARM core generates all data addresses for the Piccolo and all data transfers take place across the internal coprocessor interface. The chip can then execute functions such as a 16-tap finite-impulse-response (FIR) filter in just 815 clock cycles, and a 256-point in-place FFT in 6617 cycles.

Dedicated chips for multimedia applications show what can be done with a more targeted architecture. Chromatic Research Inc., Sunnyvale, Calif., for instance, is showing off its second-generation Mpact processor, which went through major internal enhancements to achieve a many-fold improvement in 3D performance and a higher level of integration. Targeting MPEG and other multimedia applications, Fujitsu Ltd., Kawasaki, Japan, Samsung Corp., San Jose, Calif., and Oak Technology and MicroUnity, both in Sunnyvale, Calif., all detailed high-performance multimedia support chips.

Based on a RISC core, the Oak processor is targeted at digital versatile disk (DVD) applications that include the execution of decoding algorithms for MPEG-2 and AC-3 audio. It combines a vector signal processor block for signal processing (audio, video, telecom, and graphics data) and an ARM7 core for control operations. Trying a long-instruction word approach, the Fujitsu MMA was initially developed as a coprocessor for SPARC-based systems. The chip has a peak throughput of 1 Goperation/s. Lastly, MicroUnity detailed a MediaProcessor designed for cable modems and other broadband applications.

The conference also played host to several key invited presentations. For openers, Gordon Moore, chief executive officer of Intel, discussed the history of the microprocessor in this, its 25th year. Additional perspectives were presented by Bernard Pueto, founder of Concord Consulting, Portola Valley, Calif., who focused on the lessons learned from computer history; Len Shustek of Network General Corp., also in Portola Valley, who examined ways to preserve the history of the computer and microprocessor; and lastly, David Liddle, a partner at Interval Research, who examined microprocessor applications in the next 25 years.

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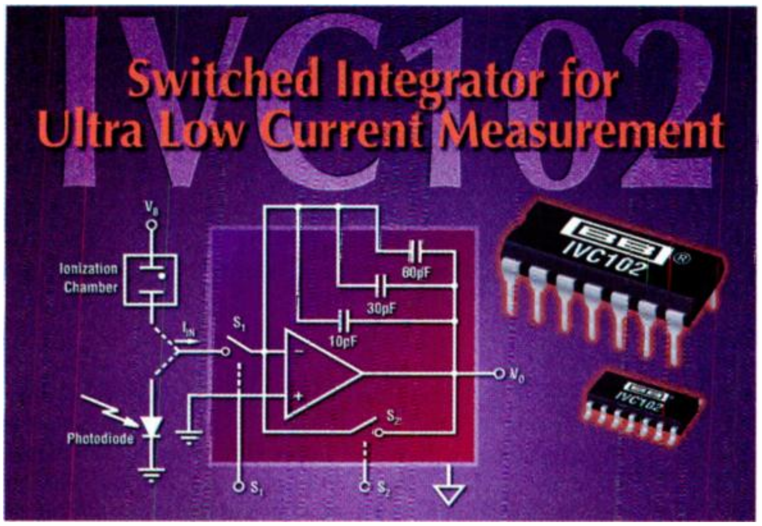
New Product Update



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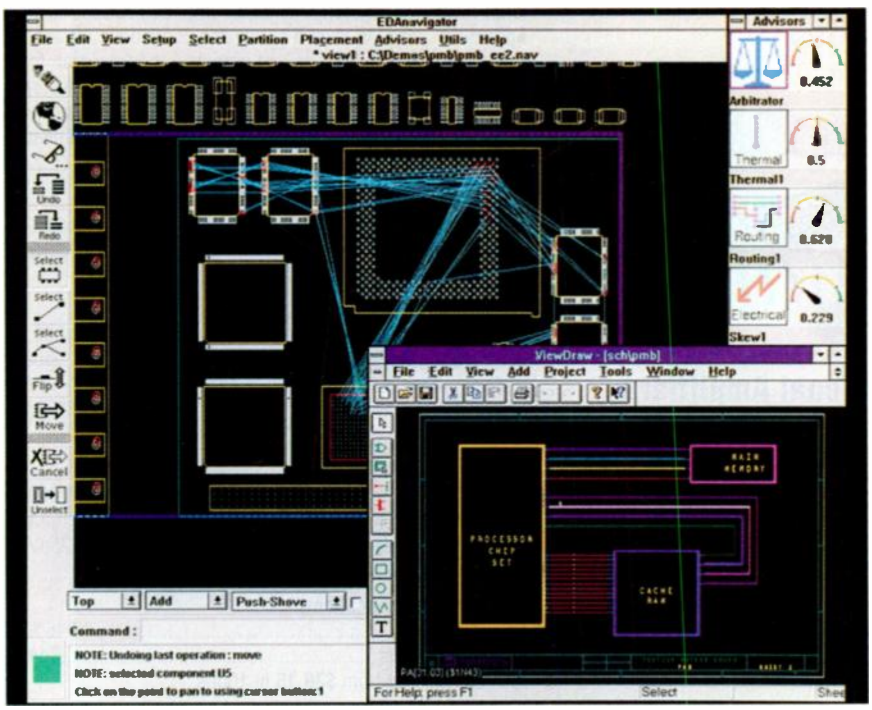
Analysis Tools Target Pc-Board Design-Cycle Front End

Utilizing Pc Board Analysis Tools Decreases Design Iterations, Cost, And Time To Market.

CHERYL AJLUNI

The rising speed and complexity of high-performance components have raised substantial physical issues that can result in design malfunctions if they are ignored during the functional design process or, if they are addressed in a sequential fashion. Until now, board-level designs were driven by layer minimization and manufacturability. Current designs are being driven by such constraints as massive siliconization, interconnect delays at the deep submicron and board levels, faster on- and off-chip board clock speeds, and signal paths that span across a number of multiple- packaging hierarchies.

These malfunctions can lead to a string of costly iterations, and are becoming more difficult to fix after the fact. What's needed is a new approach: An innovative design paradigm that will enable better management of the functional and physical design relationships, as well as simultaneous optimization of a board across multiple performance domains. Whether referred to as performance engineering, correct by design, correct by construction, or top-down design, it all boils down to the same thing—a dramatic decrease in design iterations, cost, and time to market. The way to get there, according to many in industry, is by bringing back-end physical design processes as far up front in the design cycle as possible. In other words, the design tools must play a preventive role rather than a reactive one.



1. EDANAVIGATOR FOR WINDOWS COMPLEMENTS traditional CAE/CAD tools for both engineers and layout designers. It provides easy-to-use hierarchical floorplanning, partitioning, interactive and automatic placement, constraint management and multiconstraint trade-off optimization. The screen capture depicts some of this functionality through its depiction of thermal, routability, and electrical advisors guiding interactive placement with multiconstraint trade-off analysis.

In the past, it was not uncommon for a design engineer to sketch out a design and then simply "throw it over the wall" to the layout engineer. But the complex nature of today's designs have made this method almost impossible. Analysis tools currently on the market have offered some help, but they are typically used in the back-end where it is too late to fix some of the more costly mistakes. And, because most tools are based on a sequential use model, only one engineering constraint can be dealt with at any given time. Yet, increasing design complexity also increases the probability that a design solution that satisfies one constraint will violate

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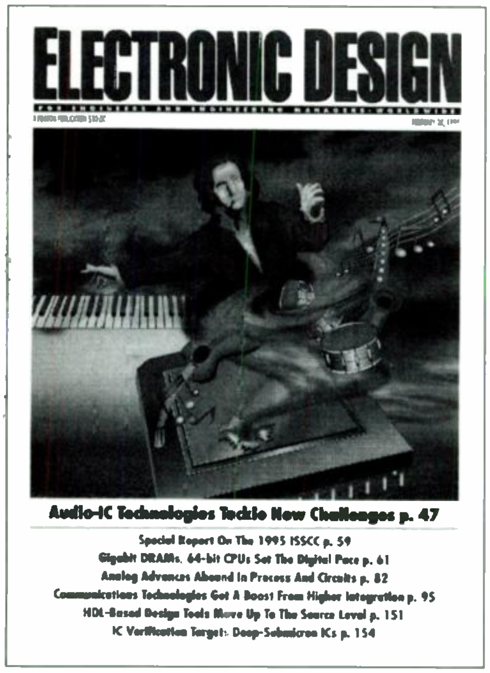
Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.



A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

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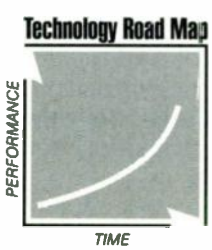

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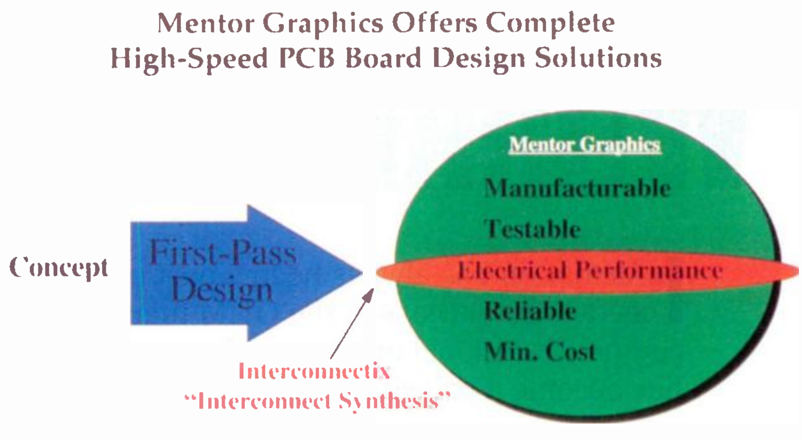
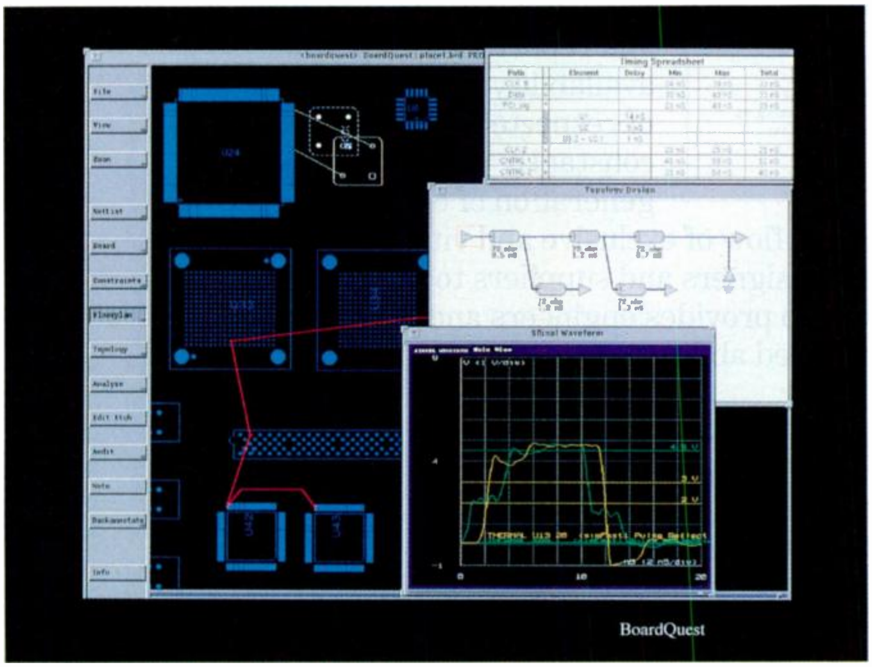
several others. For example, while placing components close together may minimize silicon real estate and help meet timing constraints, it may also cause unacceptable thermal effects or manufacturing problems. Without the available tools to handle more than one constraint at a time, numerous design iterations and several prototyping turns are inevitable.

Another factor instigating a change in the flow of pc-board design tools is siliconization. This technology has provided designers with a number of complex silicon building blocks, and consequently, the ability to design boards with radically different functions next to one another. Having this new-found flexibility means that planning a design, positioning components, and fashioning interconnect tends to be more critical than ever. Ultimately, electrical behavior, timing, EMI, thermal, and noise constraints play a much more crucial role than physical rules in determining the nature of a design.

High-speed boards also have contributed to the need for a more modern design approach. With board speeds passing 50 MHz, layout has become a critical issue in overall system performance. The design of complex interconnects guided solely by design constraints passed down from engineering is no longer viable. Engineers left to their own wits to define and resolve conflicting high-speed engineering constraints, while ensuring the performance of literally hundreds of critical signals within individual boards and across entire system configurations, are fighting a losing battle. These challenges are compounded by the fact that product life cycles are continuing to shorten. Using traditional methods of pc-board layout and having to spend weeks debugging and fixing the problems just doesn't cut it anymore. According to Harris EDA, Fishers, New York, building and testing multiple prototypes is no longer a viable method of ensuring that a complex design will work as specified and that it will be successfully manufactured. If you haven't done system-level analysis by the time you get to the pc-board layout stage, it's already too late.



3. MENTOR GRAPHICS WILL LEVERAGE the interconnect technology from Interconnectix within the electrical performance portion of its current pc-board tool design cycle. This will help designers attain single-pass design success.



2. CADENCE'S BOARDQUEST OFFERS ENGINEERS an intuitive environment to explore net topologies and characterize design performance prior to physical implementation. Using a combination of logical and physical design abstractions, design engineers can proactively perform constraint trade-offs, timing-guided placement, termination synthesis, and form-factor analysis. Boardquest provides access to analysis tools via a smooth integration, eliminating the need for special library or database translators.

THE BENEFITS ARE...

Moving the back-end physical design processes as far up front as possible in the design cycle sounds simple enough, but in reality, it requires a highly-intuitive tool set. For example, engineers should have the ability to conduct prelayout exploration and sketch possible net implementation schemes to make important design trade-offs. Although this method of design means that a great deal of time is invested in the design before it is laid out, many in industry would agree that it's nothing compared to the time it would take to go through multiple iterations.

As an example, thermal analysis is typically done after a board is laid out,

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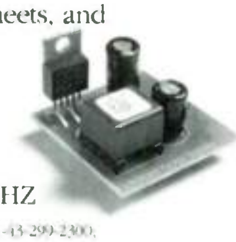

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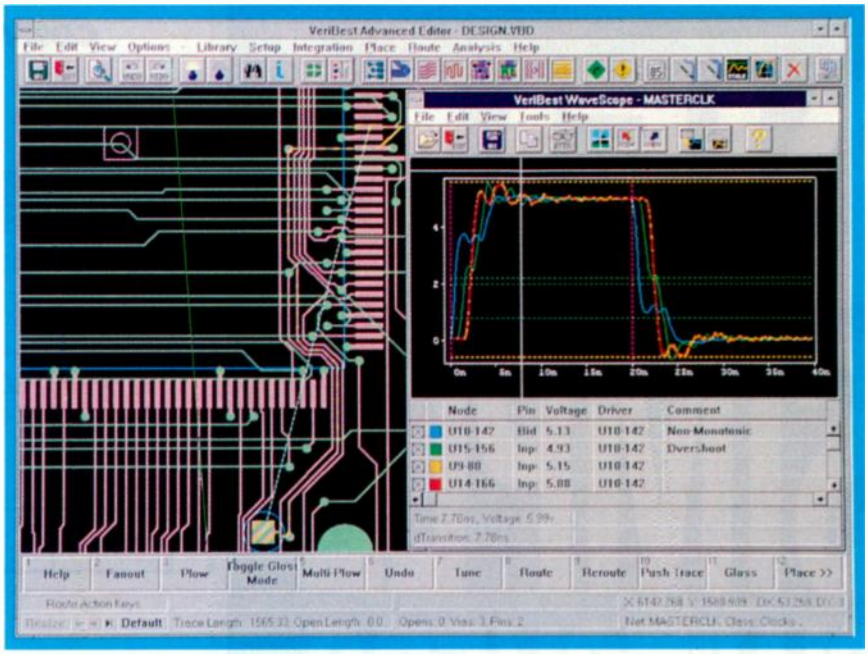
in order to check for hot spots which could cause a board failure. If a hot spot is located, the designer must go back and fix the problem. However, by bringing thermal analysis up front, the problem could be detected and prevented before the board is ever laid out. Signal integrity is another analysis technique that could prove more useful if used early on in a design cycle. By checking the signal integrity well before a design schematic even exists, architectural decisions, such as partitioning, can be made in an informed manner based on solid, accurate information.

Since the use of analysis tools up front allows for a fair amount of exploration and enables design trade-offs, the designer is better able to understand the implications of issues related to the physical aspect of the design, such as thermal integrity, timing performance, electromagnetic interference, and reliability. This knowledge empowers the designer to make more educated decisions in the design process, thereby eliminating many costly design changes down the line. In addition, by fully addressing these issues as they pertain to a specific pc-board design, the designer can achieve a more optimized, higher-performance design.

As high-speed board design continues to evolve, designers are being forced to play a more interactive, hands-on role in the design process. Eying this change, pc-board tool vendors are scrambling to be the first to find the "Holy Grail" of the EDA industry, a pc-board design solution that enables first-pass design success. While some may look to point tools for the answer, many believe that the only possible way to attain this goal will be through the development of a highly integrated tool suite that emphasizes flexibility yet, affords its users the benefit of an open environment.



4. THE WAVEFORM display tool, Wavescope, emulates a virtual oscilloscope during physical design, a function not previously offered in pc-board design-tool packages.

THE SOLUTIONS

Recognizing the limitations of the traditional pc-board design-layout tools, many pc-tool vendors are now offering tools that bring analysis as far up front in the design cycle as possible. For some vendors, this is not a recent move. Harris EDA, for example, has had one prime focus since its management buyout in 1993—to bring analysis to the front end. In May 1994, that goal was met with the introduction of EDAnavigator. Based on a client-server architecture that streamlines the flow of the design data, it plugs into existing design environments to compliment traditional CAE and CAD tools *(Fig. 1)*. Bridging the gap between logical and physical domains, it maintains data consistency and allows for both automatic and interactive trade-offs between key analog parasitics. The EDAnavigator also has the capability to read existing shape libraries from a variety of different sources.

Designers using this tool can explore floorplanning and partitioning options based on form factor, quickly place designs using timing and manufacturing constraints, and then further analyze and optimize designs for routability, electrical performance, thermal effects, and other critical physical metrics. User-defined net classes and constraints allow the designer to specify timing rules on critical nets.

One of the benefits of EDAnavigator is its automatic and interactive post-layout analysis. This feature provides the designer access to fully explore any number of design alternatives, enabling design optimization much earlier in the design cycle. Because EDAnavigator it relies on a proprietary simulated evolution algorithm, user-guided automatic realization of fully placed pc boards is possible in minutes rather than days.

EDAnavigator is complemented by Design Explorer, a powerful set of interactive floorplanning, hierarchical physical partitioning and placement functions, and Design Advisors for predictive analysis across multiple domains. The Advisor Backplane and Arbitrator also are available to manage multidomain performance tradeoffs. According to Laurence S. Liebson, president and chief executive officer of Harris EDA, "Both engineers and layout designers are using EDAnavigator to reduce overall design time by 25% or more and eliminate multiple, costly prototype spins." EDAnavigator software is available on Unix, and on Windows NT, 95, and 3.11 platforms.

ISIS, offered by Viewlogic Systems, Marlboro, Mass., consists of point tools that include ISIS PreVUE, ISIS Analyzer, and ISIS Designer. They are all integrated into one environment known as Constraints Management System (CMS). With ISIS, engineers can conduct a series of trade-offs, provide fast critical circuit optimization, and model in-

terconnect on a net-by-net basis. The combination of logical and physical design parameters during analysis provides a comprehensive approach to overall design optimization.

ISIS PreVUE, which can be utilized at any stage of the design cycle, provides a conceptual prototyping scratch-pad environment, along with spreadsheets to evaluate and analyze transmission lines. In this environment, signal performance and integrity can be optimized by performing what-if trade-offs. Information from these trade-offs can then be used as the electrical constraints for the design-in question. Physical parameters such as board stack and conductor dimensions also can be evaluated and optimized. In addition, the tool provides a means of matching device logic and the corresponding termination and net topology strategies prior to completion of the schematic. Wizards also are available to help graphically model signals and net topology strategies. The wizards ensure quick access into the impact of various approaches.

ISIS Analyzer enables circuit optimization through dynamic floorplanning and analysis. The tool works by performing a signal integrity analysis, using actual physical design data on components as they're placed. A graphical interpretation of the results is displayed, allowing the designer to make educated decisions regarding the choice of components. An intelligent checking feature, based on proven shape-based technology from Cooper and Chyan Technology, Cupertino, Calif., compares signal threshold constraints with actual simulation or analysis results. The feature also provides designers with results that match the needs and constraints of the downstream CAD layout environment. These results are then transported to a CMS spreadsheet and back-annotated to MOTIVE for static timing analysis. Information from the signal integrity and timing analysis can be utilized to automatically create constraints via the automatic constraint synthesis (ACS). ACS also can decide which paths are the most critical, in order to specify the net priority for the purposes of placement and routing.

According to Omniview Inc. Pittsburgh, Pa., part of the solution for decreasing cost, design iterations, and time-to-market involves addressing many of the critical questions (Will bus contention be a problem? Are 32 processors really overkill?) early in the design cycle. To accomplish this task, the company developed the performance modeling workbench (PMW). By bringing together the speed and power of VHDL, graphical architecture entry, automatic model generation, and advanced graphical analysis, PMW can not only answer those questions, but can rapidly create a number of alternate hardware and software architectures. These models can then be simulated and analyzed for performance metrics of such things as latency and throughput. The PMW tool suite includes a hot spot analyzer that utilizes a color scale to show the variance over time of selected performance parameters in the hardware architecture diagram, histograms, activity time lines (which display a performance parameter for a given hardware element of software task versus time), and an analysis control panel (enables playback of the simulation transcript). If more elaborate tools are required, the performance data generated in PMW can be easily exported to most spreadsheets, such as Mentor Graphics' DSS.

The PMW offers a number of benefits not previously possible. Primarily because it models software and hardware separately, comparisons of the performance of alternate hardware/software architectures can be easily made. It also allows for simple identification of bottlenecks and overdesigns, as well as exploration of trade-offs between single- and multithreaded implementations. Because PMW is based on a generic parametrized VHDL model library, the designer can write custom performance models that can be reused in future designs. Currently, most performance models are proprietary and must be thrown away when the designer proceeds to the next design step.

The PMW fully supports a VHDL top-down design methodology. Its output directly feeds into the input of Fidelity, another product offering from Omniview that specifically focuses on providing a smooth transition between the conception and the realization of a hardware design. With this tool, the engineer simply inputs a high-level description of the intended design, in either a block diagram or VHDL format, along with requirements and constraints into Fidelity. In a matter of minutes a synthesized component-level layout-ready schematic is created. According to the company, it transforms conceptual designs to rapidly create and evaluate alternative hardware architectures, and handle the tedious, time-consuming, and error-prone tasks of component selection, timing analysis, and detailed electrical design. Basically, it removes the grunt work of board-level design so the designer can spend more time on the what-ifs.

Using add-in advisors, Fidelity also allows for the concurrent management of a variety of other non-electrical factors that can affect the design. These factors include dependability, testability, manufacturability, partitioning, and specialized packaging. Intelligent trade-offs between conflicting requirements also can be made without having to be an expert in each domain. Other features include archive specifications and preferences for retrieval and reuse, simplification of new-part entry, and automatic timing-equation generation. Fidelity has no language requirement or behavioral code to write.

An object-oriented design archive captures the entire design environment including architecture, requirements, and constraints. Subsequently, designs can be retrieved later, and quickly re-run to access the impact of key technology insertion, or to reengineer spares for older systems. Fidelity version 1.2 is currently available on Sun SPARCstations using SunOS version 4.1.2 operating system or later, or Solaris version 1.X and 2.3 operating system or later. It's also available on HP9000 platforms using the HP-UX A.9 version operating system or later.

Cadence, San Jose, Calif., is another company with solutions for the design of high-speed complex components. Cadence's solution, known as performance engineering, differs from other pc-board tools in the design methodology by focusing on the en-

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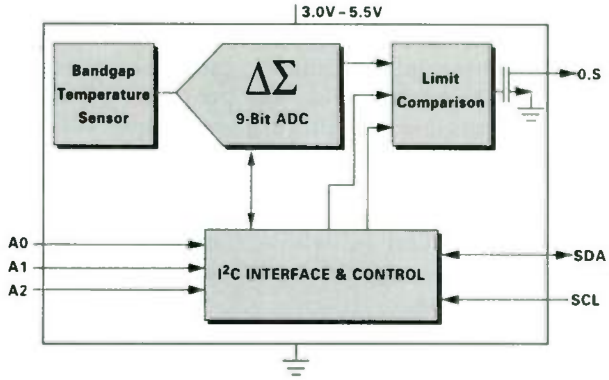

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tire design process to ensure the integrity of the design intent throughout the exploration, design, and implementation of high-speed systems. It embeds an automated-constraint continuum into the front-to-back process and provides an engineering function-oriented—rather than tool-driven—environment for trade-offs and deriving the optimum set of design-specific rules and guidelines. This set-up resolves negotiable technology constraints.

Cadence's pc-board design tool, Boardquest, defines and uses high-speed engineering constraints to ensure the performance of critical signals within individual boards and across entire system configurations *(Fig. 2)*. It does this by providing a dynamic engineering planning environment for single-board designs that include form-factor analysis, package-conscious performance tradeoffs, termination synthesis, and on-line post-layout verification of target constraints. It also allows for simultaneous performance optimization across multiple domains such as timing, signal integrity, EMI, thermal, reliability, and manufacturability. This capability enables designers to proactively characterize and continuously refine design performance as partitioning decisions across an entire multiboard system are made. Using Boardquests SigXplorer, designers can perform what-if interconnect topology explorations as early in the design cycle process as they like.

The Boardquest tool utilizes a unique synthesis technique to automatically create terminators across single- and multiple-board configurations based on interconnect performance criteria. The synthesis employs a proprietary algorithm to accurately predict when terminators are required, and to determine the proper termination schemes within the context of a specific design.

Using the Boardquest tool, a designer can accurately constrain physical packaging based on timing, signal integrity, EMI, and thermal performance constraints derived during earlier exploration stages. Any design-specific engineering rules that result from this process, such as net topology, pin ordering, or min/max crosstalk values, can then be used to drive the detailed physical implementations of the design without requiring further designer intervention.

Another Boardquest feature is the ability to store pre-defined topology templates. Designers can use these templates for application to nets during the system design and board floorplanning stages for quick verification of design performance. The topology can then be automatically implemented by Allegro's correct-by-design layout tools.

Boardquest is fully integrated with Cadence's front-to-back board-design solution, including Concept and Composer design entry, and the Design for Analysis tools of SigNoise, EMControl, Thermax and Viable, and the Allegro correct-by-design layout system. Available in targeted product design environments (PDE), Boardquest configurations starting at $19,000 include system design planning, timing-guided board floorplanning, form-factor analysis, and automatic constraint management. It's available on Unix workstations and servers from Sun Microsystems, IBM, and Hewlett-Packard.

Mentor Graphics, Wilsonville, Ore., has recently acquired Interconnectix, Beaverton, Ore. Interconnectix brings its interconnect-synthesis technology, which actively addresses the interconnect model through the use of high-level electrical abstractions of interconnect (in terms of timing and signal-purity specifications), to drive the creation of physical interconnect structures. By adding this technology to its Board Station and Board Station 500 family of products, Mentor Graphics hopes to develop a complete pc-board design solution that combines electrically driven interconnects with high-speed design for manufacturability *(Fig. 3)*.

Board Station and Board Station 500 are based on an integrated system design methodology that fully integrates the entire design flow from system-level design through final manufacturing output. Board Station is specifically designed for pc-board design and layout. Integrated with the company's other EDA tools, it shares a common database that encompasses schematic capture, simulation, electronic packaging, physical layout, manufacturability, testing and documentation. A user interface enables coordination of shared information between engineers defining pc-board logic, and those working at the device level.

Board Station 500, an integrated high-speed design system, provides users with the comprehensive functionality needed for designing high-speed pc boards. It includes timing and constraint-driven place-and-route algorithms, as well as high-speed analysis to control and analyze physical effects, and to maintain signal integrity.

This past July, Cooper & Chyan Technology (CCT) Inc., Cupertino, Calif., announced an agreement to acquire UniCAD, Inc., Ottawa, Ontario, Canada, a company specializing in pc-board electrical integrity, analysis, and optimization tools. CCT, known for its fast circuit interconnection software for pc boards, multichip modules (MCMs), and ICs, intends to leverage the tools offered by UniCAD to provide an integrated next-generation solution. According to Jack Harding, CCT's president and chief executive officer, "Beyond clock speeds of 66 MHz, the high-speed pc-board interconnect problem requires a tight coupling between place-and-route software and analysis tools. While the acquisition of Interconnectix provides us with more products to sell, we are primarily interested in its future potential to offer an integrated solution built from customer-proven point tools." CCT's next-generation system would allow the router to embed the analysis tool, resulting in correct-by-construction routed and placed pc boards, and accelerated design times.

Synario Design Automation, Redmond, Wash., traditionally a key player in Windows-based EDA tools for CPLD/FPGA design, also has plans to address both logical and physical design constraints via analysis prior to pc-board layout. An announcement is expected later this year about a comprehensive Windows-based EDA solution that will allow designers to maintain their design flows from IC through system design. The solution will provide entry, simulation, and pc-board layout interfaces, as well as incorporate a

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top-down methodology for the design of systems and boards.

An interesting development out of VeriBest Inc., Boulder, Colo., is a signal integrity analysis tool for high-speed pc-board designs. Known as the VeriBest PCB Signal Analyzer, it supplements the VeriBest PCB design and Design Capture package offering *(Fig. 4)*. The software package includes tools for layout, analysis, and manufacture of high-complexity pc boards that specifically address the critical timing issues designers must contend with as they move to higher clock speeds and densities. VeriBest PCB and Design Capture are linked through InterTool Communication (ITC) to help ensure that their databases are always in sync, notifying the designer of any changes. This connection significantly reduces the risk of schematic and pc-board mismatch. Offering true IBIS compatibility, VeriBest PCB allows for analysis and simulation in the same environment, as opposed to other tools that require some form of translation from the design to the simulation tool to be able to work with the schematic. It also provides its own virtual oscilloscope, Wavescope, that allows verification of wires and displays simulated results.

The VeriBest PCB Signal Analyzer is significant because it, in conjunction with the VeriBest interactive router, enables designers to quickly analyze and tune nets, ensuring board-level timing requirements are met and hazards are eliminated. Also included in the tool are a placement analysis tool, waveform rules checker that offers autorouting capability, and transmission-line simulation including crosstalk analysis. By moving these analysis functions forward in the design process, the VeriBest PCB Signal Analyzer improves time to manufacturing through the elimination of the time-consuming, repetitive process of post-layout analysis. Available for use on Windows NT, the VeriBest PCB Signal Analyzer costs $10,000. □

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DS1667	2	Volatile	256-Lin	10K, 50K, 100K	5V, ±5V	3-Wire Serial
DS1669	1	Nonvolatile	64-Lin	10K, 50K, 100K	4.5V to 8.0V	Pushbutton
DS1800	2	Volatile	128-Log	50K	2.7V to 5.5V	3-Wire Serial/PB
DS1801	2	Volatile	64-Log	45K	2.7V to 5.5V	3-Wire Serial
DS1802	2	Volatile	64-Log	45K	2.7V to 5.5V	3-Wire Serial/PB
DS1803	2	Volatile	256-Lin	10K, 50K, 100K	2.7V to 5.5V	2-Wire Addressable
DS1804	1	Nonvolatile	100-Lin	10K, 50K, 100K	2.7V to 5.5V	Increment/Decrement
DS1806	6	Volatile	64-Lin	10K, 50K, 100K	2.7V to 5.5V	3-Wire Addressable
DS1807	2	Volatile	64-Log	45K	2.7V to 5.5V	2-Wire Addressable
DS1866	1	Volatile	8-Log	10K	2.7V to 5.5V	3-Input Parallel
DS1867	2	Nonvolatile	256-Lin	10K, 50K, 100K	5V, ±5V	3-Wire Serial
DS1868	2	Volatile	256-Lin	10K, 50K, 100K	5V, ±3V	3-Wire Serial
DS1869	1	Nonvolatile	64-Lin	10K, 50K, 100K	3.0V to 8.0V	Pushbutton

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A Design-For-Test Tool Automatically Inserts Built-In Self-Test Structures Into ICs, And Does A Better Job Of It.

Higher Coverage, Lower Overhead Enhance Logic BIST

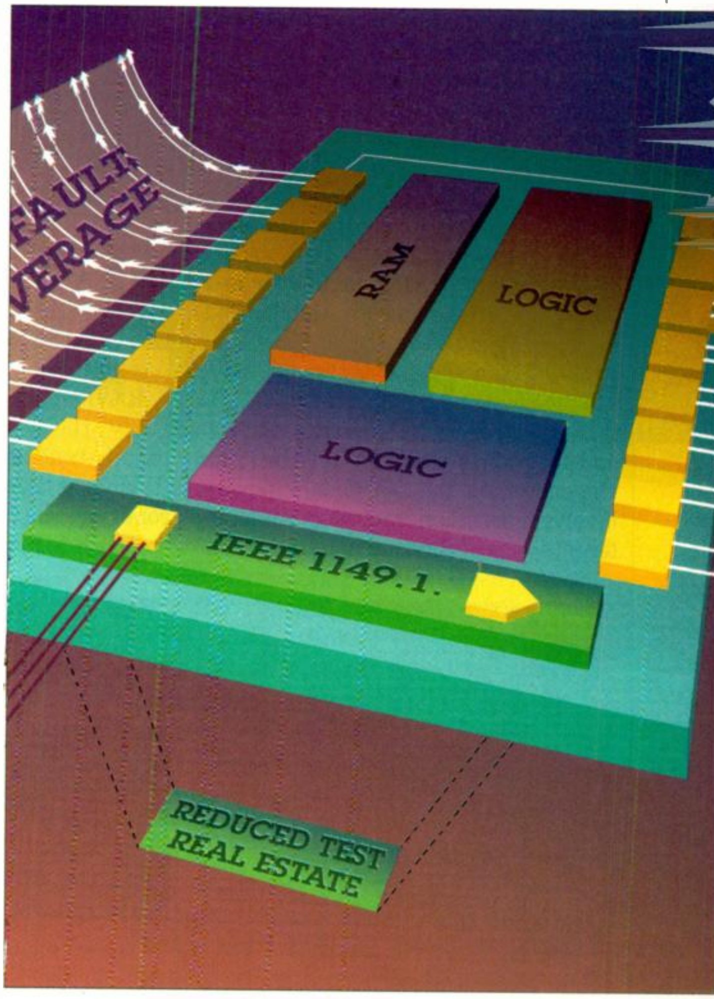
JOHN NOVELLINO

Built-in self-test (BIST) offers designers several advantages that are becoming more widely recognized as ICs become larger and more complex. On-chip test circuitry eliminates test-point accessibility problems, reduces pattern counts, and facilitates at-speed testing. It also protects intellectual property in core-based ICs. But, in the case of random-logic, BIST use has been limited by a reluctance to accept higher area overhead, lower test coverage, and longer test sequences.

Now, those problems associated with logic BIST are addressed by a design tool called LBISTArchitect, which automatically inserts BIST structures into ASICs, ICs, and core designs. The software offers designers the flexibility to make trade-offs and meet design goals while supplying at-speed fault coverage equivalent to that of leading-edge automatic test-pattern-generation (ATPG) tools. LBISTArchitect was developed jointly by Mentor Graphics Corp., Wilsonville, Ore., Texas Instruments Systems Group, Dallas, Texas, and McGill University, Montreal, Canada.

With LBISTArchitect, designers can self-test random-logic circuitry using up to 40% fewer test points than previously needed. Leveraged with the company's other DFT tools, the new software offers 100% coverage of testable faults. Additionally, designers can perform trade-off analyses for test coverage, run time, and area overhead in order to find the optimum combination for their applications.

The new tool is based on FastScan, the company's scan-based ATPG software *(Fig. 1)*. LBISTArchitect generates a complete Verilog or VHDL description of the BIST controller, pattern generator, and data compressor. It creates a register transfer level (RTL) description of the BIST logic, which enhances design portability by simplifying reuse across different technologies. The BIST controller works in



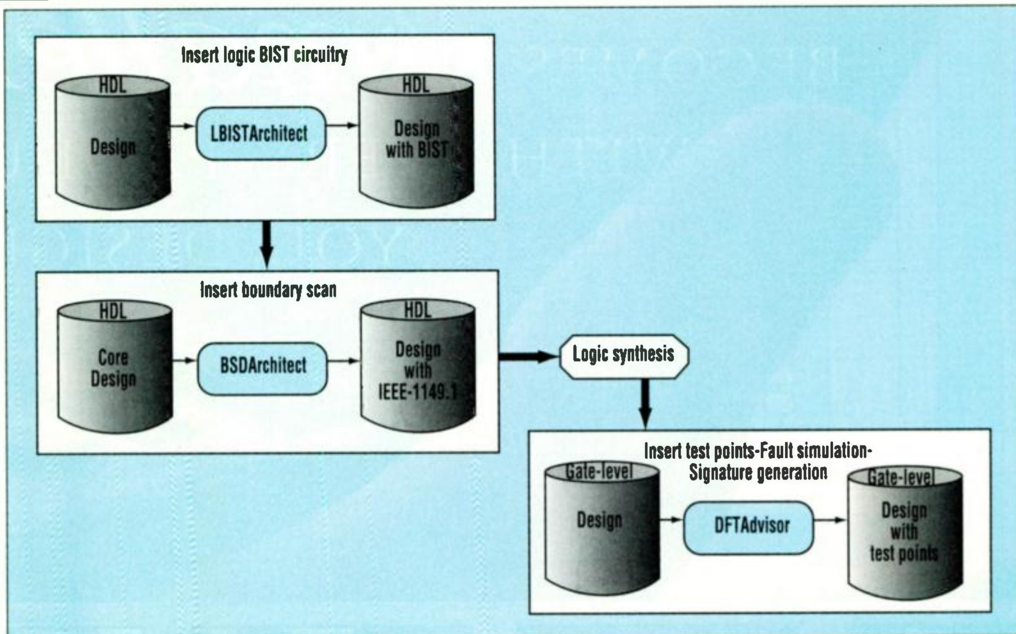
conjunction with the IC's IEEE-1149.1 boundary-scan controller *(Fig. 2)*.

The RTL code can be simulated and synthesized with any industry-standard tool, including QuickHDL and Autologic II from Mentor Graphics, Design Compiler from Synopsys, and Verilog-XL from Cadence. The software also integrates with Mentor's DFTAdvisor to provide design rule checking, deterministic fault simulation, and calculation of multiple-input shift register (MISR) signatures.

LBISTArchitect's generation of RTL code

with logic BIST, LBISTArchitect uses some innovative technologies. One, a proprietary technique called multiphase test-point insertion (MTPI), allows complete test coverage by increasing controllability and observability, but with less overhead. It also optimizes test-point combinations.

Another innovation is pseudo-random-deterministic (PRD) pattern generation, which uses a standard linear-feedback shift register (LFSR) to generate the on-chip test vectors but overcomes the functional circuitry's random-pattern resistance. In effect, the technology offers the benefits of both pseudo-random power generation and deterministic pattern generation.



3. THE BIST DESIGN FLOW, when using LBISTArchitect, crosses different levels of abstraction, starting out at a high level with register transfer level code and finishing with gate-level descriptions.

PRD pattern generation employs a combination of new techniques. It starts with pseudo-random pattern generation, then deterministically calculates test cubes to detect the most difficult random-pattern-resistant faults, like stuck-at and delay faults. It proceeds by calculating new seeds and reloading the LFSR. An extended polynomial allows seeds of variable length. All of the patterns can be applied on-chip, unlike typical deterministic ATPG patterns that must be applied through expensive automatic test equipment.

Texas Instruments (TI) was a natural partner for Mentor Graphics in this kind of project, according to Mark Olen, product line manager in Mentor Graphics' DFT Group. Over the years, TI accumulated in-house expertise by using DFT and BIST in its own products.

TI worked closely with Mentor Graphics from the earliest stages of the LBISTArchitect program, supplying the CAE experts with a systems designers' point of view. The collaboration was initiated by Andy Halliday, a DFT engineer in TI's Systems Group, during various interactions with Mentor Graphics' technical staffers at conferences.

"We worked with them quite a bit in specifying the requirements, from the user's perspective, of what this tool had to have," says Don Sterba, test automation manager in TI's Systems Group. His group's participation started with the project planning and continues through beta testing. "We worked closely through the specification phase, and then looked at the prototype version as they [Mentor Graphics] went along, giving them feedback on that and some of the advanced architecture that we needed," says Sterba.

He notes that TI had worked for years developing VHDL-based approaches to BIST and using them from one project to another. But, as the technology evolved, cost and long-term support issues made it desirable to work with Mentor Graphics on a commercially available solution.

Greg Young, who, along with Halliday, helped develop those in-house BIST implementations, says that the work on LBISTArchitect was part of an effort to come up with a number of DFT approaches to fit different applications. "From our point of view, we are looking for strategic DFT methodologies that will cover a number of different areas, not just the ASIC level, but through the system level," says Young, a member of the Systems Group's technical staff.

TI has received a copy of the latest version of LBISTArchitect and has begun using it, but it's too early for a full report on the tool. However, the MTPI capability resulted in a significant reduction in the number of gates and test points required, compared to previous projects, says Young.

A disadvantage of the in-house tool is that it takes an expert to run it, as well as an expert to maintain it, says Sterba. As a result, one of the goals of the collaboration with Mentor Graphics is to formulate a tool that could be run by a wide range of designers.

TI is actively evaluating that issue as part of the LBISTArchitect validation process. "We have Greg and Andy, who have quite a bit of experience, here as the experts," says Sterba. "But we also have a junior-level person working with them to make sure that the tool is usable. With some fairly limited training, he's been able to take the product, pick it up, and start running with it." □

PRICE AND AVAILABILITY

A floating license for LBISTArchitect costs $75,000. The price includes a license for DFTAdvisor. The software is available for HP-PA, IBM RS6000, and Sun SPARC industry-standard workstations. Beta testing started in the third quarter, with production software scheduled for delivery in mid-December.

Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777; Contact Ian Burgess, product manager, (503) 685-1329. **CIRCLE 501**

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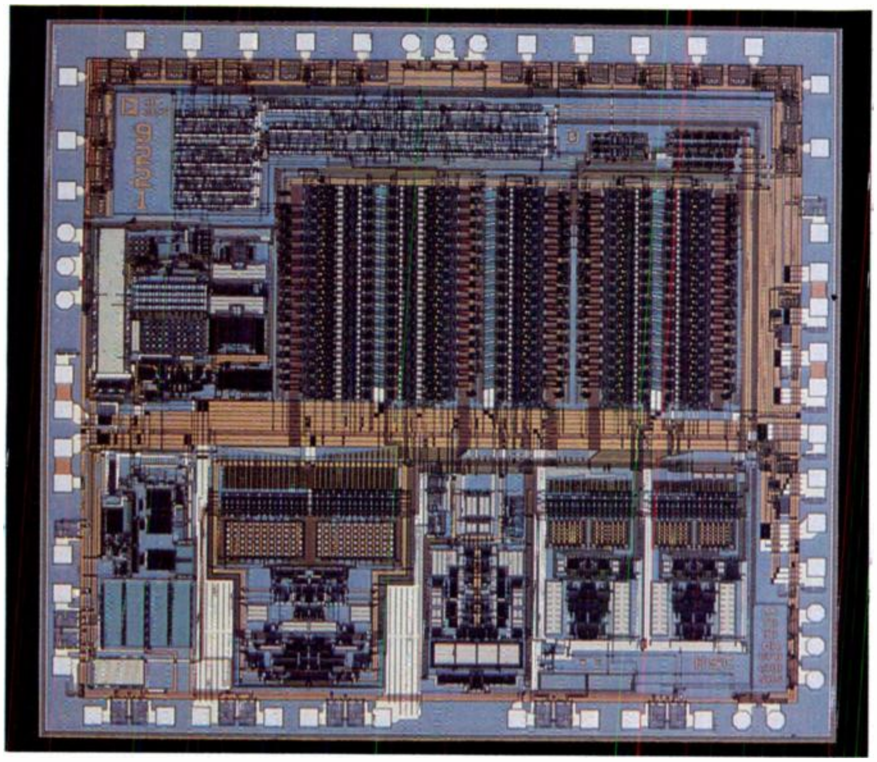

COURTESY: ANALOG DEVICES

12-Bit IC ADCs Becoming Commodity Components

FRANK GOODENOUGH

12-Bit Sampling, Low-Power, High-Speed ADCs Offer Designers Affordability And Reliability.

Who could have imagined when Peter Halloway's AD574 hit the streets in 1978 that 12-bit IC ADCs (analog-to-digital converters) with equal or superior performance would now be commodity devices priced at under $15 each in 1000-unit quantities *(see the table)*? At least one way to ensure a successful ADC-based analog/mixed-signal system design has not changed since the advent of the AD574 is to read the data sheet carefully when selecting an ADC *(see "ADCs With Multiplexers Are Shaping Up In Designs," p.67)*. While most data sheets are generally excellent sources of information, designers still may have questions about a device's specifications.

For the record, and in contrast with today's denizens of the "commodity" ADC arena, the AD574 was the first 12-bit IC ADC. A 2-chip, non-sampling ceramic-packaged hybrid (a 28-pin, double-width DIP), it sported a successive-approximation-register (SAR) architecture based on a thin-film, laser-trimmed, R2R DAC (digital-to-analog converter). Its throughput rate ran about 40 kHz. At the time, it was priced at about $40 each, and it was hardly a commodity item. But it was a lot cheaper and a lot smaller than that day's hybrids or modules.

The AD574 ADC, and the families of general-purpose IC ADCs that it spawned, soon eliminated most of the then-current hybrid and module ADCs from all but the most critical high-speed, high-resolution and military/space applications. Today, those applications, particularly if they are demanding guaranteed ac specifications, are dominated by costly (some go for over $1000 each) hybrids, modules, and board-level ADCs from companies such as Datel, Mansfield, Mass., Analogic, Wakefield, Mass., and Edge Technology, Lynnfield, Mass.

In fact, Edge Technology recently announced a 16-bit ADC (the ET2665) that samples its input at 5 MHz. It's packaged in a small metal-can module, measuring 3 by 1.5-in., and is 0.375-in. thick. It is priced at $642 each in OEM quantities.

But today, not only is the arena dominated by pure-CMOS devices, but almost all new IC ADCs run off a single 5-V rail, with 3.3-V (and lower) ADCs on the horizon. In fact, so widespread is CMOS and its favorite architecture, the switched-capacitor SAR, that regardless of the technology, it's difficult to find the process or architecture mentioned on a data sheet. Moreover, analog system designers are being forced to give up split ±15-V supply rails if they want low power, low cost, and serial I/O. But for some applications, the 12-bit CMOS SAR ADC is being challenged by high-resolution CMOS delta-sigma ADCs, and for other applications, by high-speed pipeline designs that may be on a bipolar or a biCMOS process.

How Far We've Come

The IC ADCs of today, like the microprocessors, microcontrollers, and DSPs to which they feed real-world data, have seen many changes since 1978. Like their digital kin, with each change, features and performance grew. Speed increased at the outset, albeit slowly, but as faster processes and architectures arrived, speed climbed significantly.

There was a time when a 12-bit, 1-MHz-sampling-rate IC ADC was the key component of analog IC design. One company had three separate developments underway at the same time. And low-cost devices with that kind of performance, such as Linear Technology's LTC1410 and National Semiconductor's ADC12762, are just becoming readily available today *(see the table, again)*.

Whether it was because IC designers discovered they could do it easily, or customers who wanted superior ac specifications demanded it, sampling ADCs arrived about ten years ago. Soon after sampling, with the advent of all-CMOS analog ICs, came switched-capacitor SAR ADCs (which usually provide inherent sampling) and with them, calibration (first on chip, then at the factory). The switched-capacitor SAR ADCs soon dominated the low-cost ADC arena.

The wide use of CMOS also brought about ADCs with analog multiplexers on the front end. Earlier, multichip sampling hybrids and modules often avoided multiplexers on the front end because in most instances, the under-$10 multiplexer failed when it was exposed to an unexpected off-chip voltage, thereby destroying an expensive device.

Lost But Not Forgotten

With the move to CMOS, prices have plummeted in the last few years. With the lower prices have come truly useful "bells and whistles" features such as differential inputs, very low power through a variety of unique approaches to power management, and ADCs in tiny 8-pin SOICs and even smaller packages with serial outputs. In many cases, however, ease-of-use in the form of "completeness" was sacrificed. That is, many of the newest CMOS ADCs lack an internal clock or a reference. And most new ADCs, particularly those in 8-pin packages with their serial I/O, including one or more bipolar (inputs capable of handling both plus and minus voltages) inputs, are specified for a single positive full-scale input voltage instead of two or more.

There was a time, even after the advent of the AD574 (which had both a clock and a reference), that completeness was the key feature of most IC ADCs. But with completeness becoming less of a factor, what significance does it now have to the system designer?

To begin with, though parasitic bipolar transistors are available on most CMOS processes, the technology is still not known for its precision, low-drift, bandgap references. And if the chip runs off a 5-V rail, even if a good bipolar device is available, it's still impossible to run a 6-V buried Zener reference off a 5-V rail. However, to handle the task, low-cost bipolar-transistor bandgap references that can do the job are becoming available in tiny packages like the SOT 23.

Why no clocks? Because eliminating the clock saves power. And high-speed precision clocks are not that simple to build. Like the reference, they take up die area. In addition, most systems sport a clock somewhere in the design. By synchronizing the ADC with the system clock, it usually is possible to cut the effects of digital noise by making sure the ADC's critical comparisons do not occur simultaneously with a clock pulse.

Why the limited number of full-scale input voltages? With only 8 pins, none are available as extra voltage inputs or for pin strapping to create new voltages. In addition, many of the CMOS processes do not have the thin-film resistors required to trim multiple full-scale voltage ranges to 12-bit accuracy. In this case, the system designer, in addition to giving up split ±15-V rails and TTL, must search diligently for an ADC with multiple full-scale ranges, an internal clock, and a reference on the chip, or design unique signal conditioning around them.

Many of the new CMOS ADCs specify an input voltage range from 0 to the reference voltage (even if they have an internal reference) and a few specify an input range of plus and/or minus the reference voltage. While some of these internal references are actually the 5-V rail, several ADCs derive a convenient 4.096-V reference from the 5-V rail. Other CMOS ADCs have two reference inputs. Ordinarily, the so-called negative reference input is connected to ground. However, a negative voltage can be applied to it in order to handle bipolar signals. In most instances, by applying a positive voltage to the minus input that is lower than the plus reference, the resolution can be changed. Alternatively, some of these ADCs provide a differential input to which a negative offset can be applied in order to handle a negative voltage input.

Dynamic Specifications

While most of these ADCs are used to digitize dc or very slowly changing voltages, some may find homes handling ac input signals. And since they are all sampling ADCs, they are equipped to do it. And while sampling ADCs have dominated this arena for some time, some suppliers have frustrated potential users. Their data sheets specify a sampling rate and provide a set of dynamic (ac) specifications based on it.

But the so-called ac specifications of these ADCs call out an input signal whose frequency is close to dc rather than close to the Nyquist frequency, or at least near one-tenth the Nyquist frequency. For example, the sampling rate may be 100 kHz, but the ac data is taken and presented with an input frequency of 1 kHz. If these specifications are to have any practical value to the system designer who must sam-

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with no noise penalty

From the same company that created FACT™ and FAST® logic technologies, National's Fairchild Logic Group delivers the next answer to HC logic. . . National's VHC. It offers up to twice the output drive and increased speeds up to three times faster than typical HC. **These benefits come with no loss in noise performance!** There are further benefits to National's VHC over HC like reduced static power requirements, 3v characterized specs and 5v input protection.

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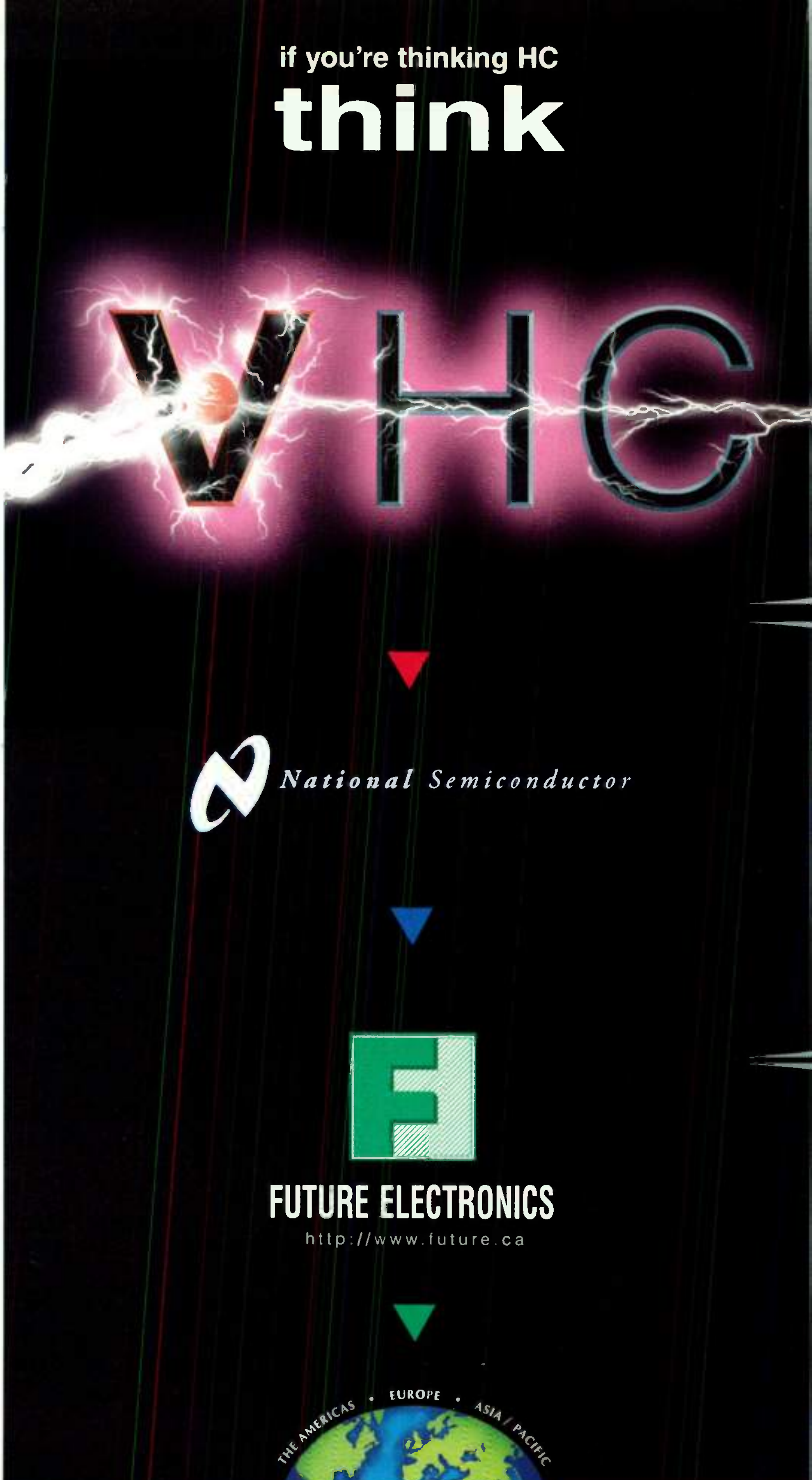

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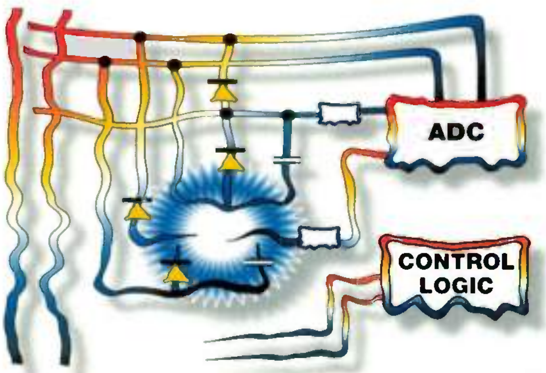
REPRESENTATIVE 12-BIT SAMPLING-TYPE "COMMODITY" ADCs

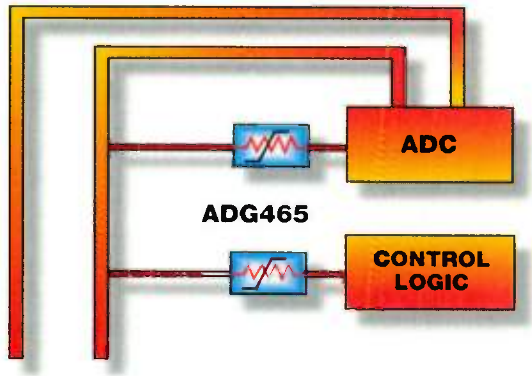
			Ac specifications			Operating power					On-chip features			
Company	Model	Sampling rate (kHz)	f_{in}/f_s (kHz)	THD (dB)	SNR/ SINAD (dB)	mW/mA	Supply voltage (V)	Power down (μA/μW)	I/O (S/P)	8-pin package	Clock	Reference	Price (in 1000s)	Architecture/ features
Analog Devices (800) 262-5643	AD7896	100	10/100	80	/70	11/5	2.7-5.5	5/	S	Yes	Yes	Yes	$6.75	1
	AD7883	50	1/50	80	69/	11/3	3.3	/1500	P	No	No	No	$6.75	1
	AD7853	200	10/200	78	/70	33/5.5	3-5.5	5/18	S	No	No	Yes	$8.95	1,2
	AD7853L	100	10/100	78	/70	10.5/1.9	3-5.5	5/18	S	No	No	Yes	$6.50	1,2
	AD7854	200	10/200	78	/70	20/5.5	3-5.5	5/18	P	No	No	Yes	$10.00	1,2
	AD7854L	100	10/100	78	/70	6.5/1.8	3-5.5	5/18	P	No	No	Yes	$7.25	1,2
	AD7721	469	210/469	78	/74	150/29	5	/100	S/P	No	No	No	$10.00	2,3
Burr-Brown (800) 548-6132	ADS820	20 MHz	10 MHz/20 MHz	NA	58/58	235/55	5	None	P	No	No	Yes	$7.45	4
	ADS7820	100	45/100	80	70/70	100/16.3	5	None	P	No	Yes	Yes	$10.25	1
	ADS7804	100	45/100	80	70/70	100/16.3	5	None	P	No	Yes	Yes	$10.25	1
	ADS7806	40	1/40	80	70/70	35/5.6 (typ)	5	None	P	No	Yes	Yes	$9.25	1
Comlinear (800) 272-9959	CLC949	5-30 MHz	2.4 MHz/5 MHz	SFDR = 64 dB	68/68	65/	5	None	P	No	No	Yes	$48.00	4
Harris Semiconductor (800) 4HARRIS	HI7191	2	0.5/2	81	NA	30/6	±5	/5(typ)	S	No	Yes	No	$6.98	2.5
	HI5812	750	1/750	77	/70	NA	NA	None	P	No	Yes	Yes	$4.64	1
	HI574A	NA	NA	NA	NA	1 W	æ15	None	P	No	Yes	Yes	$9.94	6
Linear Technology (408) 432-1900	LTC1274	100	100/100	76	/70	20/4	5 or ±5	5/50	P	No	Yes	Yes	$7.60	1,7,8
	LTC1277	100	100/100	76	/70	20/4	5 or ±5	5/50	P	No	Yes	Yes	$7.60	1,7,8,9
	LTC1400	400	100/400	76	/70	160/30	5 or ±5	20/125	S	Yes	Yes	Yes	$10.00	1,8
	LTC1410	1.25 MHz	600/ 1250	74	/68	160/	±5	10/	P	No	Yes	Yes	$28.00	1,8
	LTC1285	7.5	1/7.5	80 (t)	/67 (t)	/100	2.7-5.5	0.002/	S	Yes	No	No	$6.35	1,11
	LTC1286	7.5	1/7.5	80 (t)	/67 (t)	/100	5	0.002/	S	Yes	No	No	$5.20	1,11
Maxim (408) 737-7600	MAX120	500	100/500	77	/70	/315	5, -10	None	P	No	No	Yes	$11.50	1
	MAX1241	70	10/70	80	/70	/4	2.7-5.5	10/	S	Yes	No	No	$5.80	1
	MAX187	75	10/75	80	/70	/2.5	5	10/	S	Yes	No	Yes	$6.45	1
	MAX189	75	10/75	80	/70	/2	5	10/	S	Yes	No	No	$5.95	1
	MAX191	100	1/100	80	/70	/5	±5	20 (t)/	S/P	No	Yes	Yes	$9.60	1
	MAX122	333	50/333	77	/69	/315	5, -10	None	S/P	No	No	Yes	$8.25	1
	MAX176	250	50/250	80	/70	/172	5, -12	None	P	No	No	Yes	$9.85	1
Micro Linear (408 433-5200	ML2221	44	8/44	80 (t)	NA	/50	±5	None	S	No	No	No	$13.75	12,13
	ML2223	44	8/44	80 (t)	NA	/50	±5	None	S	No	No	No	$11.00	12,14
National Semiconductor (800) 272-9959	ADC 12041	222	80/215	70 (t)	71 (t)/ 67 (t)	33/6.6	5	15/75	P	No	No	No	$5.50	1,2,13
	ADC 12762	1.4 MHz	100/1.4 MHz	70	67/67	300/35	5	/250 (t)	P	No	No	No	$12.00	10,15
Philips (800) 234-7381	TDA8767	30 MHz	4.4 MHz/30 MHz	64 (t)	61/	335 (t) /60 (t)	5	None	P	No	No	No	$11.00	4
Sipex 508-667-8700	SP8538	25	9.5/20	80	74/73	0.5 (t) /0.15	3.3	2/10	S	Yes	Yes	Yes	$4.20	1

1 = successive approximation register (SAR); 2 = calibrated; 3 = 16-bit delta-sigma; 4 = pipelined; 5 = 23-bit delta-sigma; 6 = SAR (classic); 7 = can undersample; 8 = sleep and nap modes; 9 = single-ended input; 10 = single-and differential inputs; 11 = auto sleep mode; 12 = algorithmic; 13 = 12-bit + sign; 14 = RS-232 out; 15 = 1 and 2 channels.

f_{in} = input frequency; f_s = sampling frequency; I/O = input/output; NA = not available; P = parallel; S = serial; SINAD = signal-to-(noise + distortion); SNR = signal-to-noise ratio; THD = total harmonic distortion. All values are minimum or maximum, unless labeled typical (t), at 25°C and at minimum rated supply voltage.

Protect Your Circuits For As Little As 30¢ Per Channel.



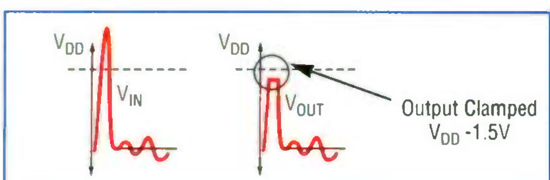


New Single-, Triple- and Octal-Channel Protectors Prevent Overvoltage and Fault Conditions

Now you can maintain structural integrity in your designs and your budget. The ADG465 (single), ADG466 (triple) and ADG467 (octal) are the new, affordable industry standards for around-the-clock system safety.

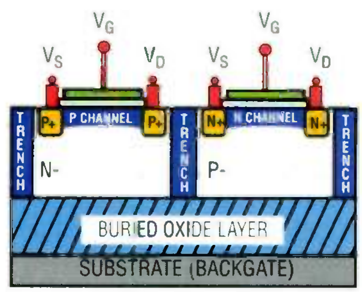
Maximum Protection, Minimum Power

When you fortify your designs with channel protection, any time input voltages exceed the user-selectable rails, an internal switch opens automatically. There's no need for logic drivers. And you can use channel protectors in data acquisition systems with all the advantages of fast response time and trench isolation, preventing latch-up. In multiples, it's possible to secure each channel independently. So whether power supplies are "on" or "off", your designs are always shielded from voltage transients to ±35 V. That's maximum circuit protection at low power (30 μW at 15 V) – even under fault conditions.



Operation of Clamping Function

Fundamental Design Practice



Size, power and price are non-issues. No matter what your application, you can design in an SOT-23 or microSOIC package for unbeatable circuit security starting at just 30¢ per channel*. Simply call the appropriate numbers below for samples and data sheets of the ADG465/66/67. It's a line of defense that leaves no excuse for blowing another design.

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ple some audio or some machine vibrations, the input frequency should have been at least 10 kHz and close to the Nyquist frequency (50 kHz) to truly indicate performance. In contrast, many suppliers of commodity ADCs actually provide ac specifications at input frequencies greater than the Nyquist frequency, thus recommending them for undersampling applications *(see the table, again)*.

There are several explanations for this disparity. First, the supplier lacks either the laboratory or the production test equipment required for running the needed FFTs. Or, to keep down production costs, tests are not performed. In this case, the supplier often provides detailed typical ac data on the data sheet. It's called out as measured with close to the Nyquist frequency input signals.

Note that the ac specifications include the signal-to-noise ratio (SNR), the signal-to-noise + distortion ratio (SINAD), the total harmonic distortion (THD), and the spurious-free dynamic range (SFDR). Suppliers sometimes include the characteristics of the sampling circuit itself—for example, the sample-and-hold amplifier, especially if a standalone sampling-and-hold amplifier is used ahead of the switched-capacitor SAR in order to achieve optimum sampling. Most suppliers include SNR and/or SINAD along with THD. Some add SFDR, and a few provide two-tone intermodulation distortion (IM) figures and/or full-power bandwidth.

Sleep Mode

A couple of years ago, system designers were hit by a pair of virtually inseparable mandates: Cut power and run off a 3.3-V rail. And designers using ADCs were not exempt from these mandates. They have come up with devices able to run off a single 3.3-V rail as well. In fact, most ADCs meeting this challenge run off a supply rail between 2.7 and 5 V.

One of the most intriguing ways to cut power, particularly in a mixed-signal system, is by use of a process called "power management." Simply put, it means turning off the circuit when it's not being used (called by various suppliers the "sleep" mode, the "standby" mode, the "shut down" mode, and/or the "power down" mode). That sounds easy if the IC designer has lots of cheap CMOS switches around, as they do in these ADCs. But what happens to the reference? Whereas the rest of the ADC turns on quickly, the reference may take a number of milliseconds to reach its final value, based on the value of the capacitor hanging on the reference pin.

One approach to this problem used by Linear Technology is to make available to the designer two modes of power down known as "sleep" and "nap" modes. During the sleep mode, everything is asleep. But in the nap mode, the reference, and in some devices the digital logic, is powered up. In the nap mode, the ADC is ready to go in under 1 µs. The functions are available in the speedier LTC1410 and in the slower LTC1274 and LTC1400 *(see the table, again)*. Although most of these ADCs provide a sleep mode, it is not specified whether the ADC's reference is off in the sleep mode. Moreover, if it is turned off, they do not specify how long it takes to wake up.

Why use high-speed ADCs to measure dc voltages? For starters, they offer a novel way to save power. While they use significantly more power than slower devices if on all the time, in some applications they can be powered down most of the time, whereas a slower device might have to be running all the time. Therefore, the average power causing potential battery drain may be less for the high-speed power hog. Not only might a fast ADC save power, but it might be the cheapest way to go. For example, the Harris HI5812, which samples at 750 kHz, costs less than $4.64 each in 1000-unit quantities.

Sleepy Time Chips

Analog Devices' AD7896 and several Linear Technology ADCs, including the LTC1285 and LTC1288, offer a feature called known as "automatic power down." The AD7896 goes into the sleep mode when a conversion is complete. After a conversion command, it is allowed 6 µs to wake up at which time, its sample-and-hold amplifier goes into the "hold" mode and the SAR starts to work. Less than 10 µs later, the conversion is complete, and if running in the automatic power-down mode shuts down. At that time, a read operation is performed on this serial-I/O ADC in its 8-pin SOIC or DIP.

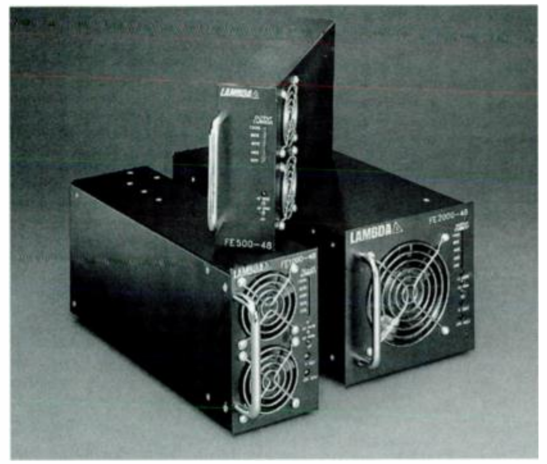
The Sipex serial-I/O SP8538 also features auto shutdown and two inputs. It can be programmed to operate either with a single differential input or with two single-ended inputs. It runs off supply rails between 3 and 5.5 V from which it draws just 150 µA. However, it still achieves a SINAD of 70 dB while sampling a 9.5-kHz signal at the Nyquist frequency. It is priced at $4.20 each in 1000-unit quantities.

National Semiconductor's new high-speed (1.4-MHz sampling rate) ADC, the ADC12762, while not a micropower ADC like the SP8538, employs a somewhat similar one- or two-channel front end. It contains a 2-channel multiplexer whose common lead is brought out to a pin that must be connected to the chip's sample-and-hold amplifier. Gain can be applied off-chip, between the multiplexer and the sample-and-hold amplifier, alternatively a single signal can be applied directly to the sample-and-hold amplifier. The converter is aimed at both 1- and 2-channel applications and at $5.50 each—for a 1.4-MHz ADC—is priced accordingly.

All of the power-down data in the table is for ADCs in the sleep mode *(see the table, again)*. In most cases, if an ADC needs an off-chip reference, it's up to the system designer to come up with a way to put the reference to sleep and to determine just how long it takes to wake up.

The Micro Linear ML2221 and 2223 are two devices that have a lot of potential uses. They both can be considered "power hogs" (they take 50 mA from a 5-V rail and 30 mA from a –5-V rail), but both are 13-bit (12-bit plus sign) serial-I/O ADCs built on an ancient CMOS process. The ML2221 has been around a long time; at least 10 years, but it never caught on. The ML2223 adds a UART to the circuit and provides an RS-232 output. The ADC employs an algorithmic architecture that uses the same circuits over and over again. Yet while sampling an 8-kHz sine wave at 44 kHz, they achieve a THD of –80 dB. One could speculate the kind of perforn ance that could be achieved when using this architecture on a 0.6-µm

Lambda's FE Series



High density, Bellcore compliant distributed power front ends.

Lambda's FE Series modular front ends are the ideal foundation for fault-tolerant distributed power architectures. Designed specifically for telecommunications and high-end computer applications, the FE Series is available from stock in 24 or 48 VDC output modules. Delivering from 500W to 6kW of scaleable power, all models are Bellcore and ETSI compliant, and meet FCC Class B EMI emissions standards. In addition,the FE Series takes up 35% less space than the nearest competitor, and features remote diagnostics, overvoltage and overtemperature protection for remote site use. Hot pluggable and N+N redundant, Lambda's FE Series and FE Series Racking System are the most reliable, cost efficient system solutions. They make designing, building and qualifying your system easier, quicker, and much less expensive.

FE Series Models and Complete Racking Systems

FE0500-48-NA

Module Output Power
0500 – 500W
1000 – 1000W
1500 – 1500W
2000 – 2000W

Nominal Output Voltage
48 – 48VDC
24 – 24VDC

N – without diodes
R – with diodes

A – Analog Control
C – Computer Option

POWER (WATTS)	MAX OUTPUT CURRENT (AMPS)	Vout (VDC)	UNIT PRICE PER DELIVERED QUANTITY 1	10	100	MODEL
24V OUTPUT						
500	21.0	20.0-29.0	$ –	$630	$567	**FE0500-24-NA**
500	21.0	20.0-29.0	715	640	576	**FE0500-24-RA**[1]
1000	42.0	20.0-29.0	–	896	806	**FE1000-24-NA**
1000	42.0	20.0-29.0	1015	911	820	**FE1000-24-RA**[1]
1500	63.0	20.0-29.0	–	1148	1033	**FE1500-24-NA**
1500	63.0	20.0-29.0	1305	1173	1056	**FE1500-24-RA**[1]
2000	84.0	20.0-29.0	–	1350	1215	**FE2000-24-NA**
2000	84.0	20.0-29.0	1550	1395	1256	**FE2000-24-RA**[1]
48V OUTPUT						
500	11.0	40.0-58.0	$ –	$630	$567	**FE0500-48-NA**
500	11.0	40.0-58.0	715	640	576	**FE0500-48-RA**[1]
1000	21.0	40.0-58.0	–	896	806	**FE1000-48-NA**
1000	21.0	40.0-58.0	1015	911	820	**FE1000-48-RA**[1]
1500	32.0	40.0-58.0	–	1148	1033	**FE1500-48-NA**
1500	32.0	40.0-58.0	1305	1173	1056	**FE1500-48-RA**[1]
2000	42.0	40.0-58.0	–	1350	1215	**FE2000-48-NA**
2000	42.0	40.0-58.0	1550	1395	1256	**FE2000-48-RA**[1]

Note: 1. Redundant, or -ing diodes are included in model.

FE5K-N E

Module Type
4K – FE0500
5K – FE1000
6K – FE1500/2000

Input Type
N – Class B EMI and Circuit Breakers.
X – Class A EMI

Mounting Style
N – NEBS/Telcom
E – EIA

MODEL	MODULE CAPACITY 500	1000	1500/2000	19" MOUNTING STYLE	UNIT PRICE PER DELIVERED QUANTITY 1-9
Racking Systems					
FE4K-N-E	7			EIA	**$1195**
FE4K-X-E	8			EIA	**899**
FE4K-N-N	7			NEBS	**1295**
FE4K-X-N	8			NEBS	**999**
FE5K-N-E		4		EIA	**1195**
FE5K-X-E		5		EIA	**799**
FE5K-N-N		4		NEBS	**1295**
FE5K-X-N		5		NEBS	**899**
FE6K-N-E			3[2]	EIA	**1195**
FE6K-X-E			3[2]	EIA	**799**
FE6K-N-N			3[2]	NEBS	**1295**
FE6K-X-N			3[2]	NEBS	**899**

Note: 2. FCC Class B EMI filtering is internal to the FE1500 and FE2000 modules.

Note: 3. EIA Mounting Flanges are located at the front of the Rack. Telecom mounting flanges are center mounted per Bellcore NEBS requirements.

FE Series Specifications

AC Input
line ....85-265VAC, 47-63Hz for FE0500, FE1000, FE1500.
170-265VAC, 47-63Hz for FE2000.

Efficiency
82% typical for 50-100% minimum without isolation diodes.

Power Factor/Harmonic Correction
0.95 minimum at full load. Compliant to IEC-1000-3-2.

Hold-up Time
Output will be maintained above lower limit of output voltage range for 16ms upon loss/disconnect of AC input.

Surge Immunity
IEC-1000-4-5 Level 3 for FE0500. Level 4 for FE1000, FE1500, FE2000.

Regulated Voltage
line and load
regulation ....1.0% from no load to full load. 85VAC-265VAC max.
ripple and noise..........250mV pk-pk max on 24V models. 500mV pk-pk on 48V model. EIAJ RC-9002A procedure (20Mhz bandwidth limit).

Overcurrent Protection
The power module limits the output current to less than 110% of the full power rating. The current limit characteristic has constant power down to V_o min. The converter withstands an indefinite short circuit without damage and is self-recovering.

Output Current Share
±10% of max unit load from 10% to 100% load with single or multiple A/B rail inputs. Current sharing is accomplished via a single wire connection. The power module operates in parallel without any derating of its maximum full load output current, with and without Or-ing diode option. The current sharing bus is not a single point failure mechanism. Current sharing is not required for parallel operation.

Temperature Drift
±2% over the entire temperature range and life.

Overvoltage Protection
Adjustable non-latching unit shutdown.

Overtemperature Protection
Internal circuitry prevents damage by turning off the converter in the event of reduced airflow or excessive ambient operating temperature. The output spontaneously returns when the overtemperature condition is cleared.

Hot Maintenance
Unit is capable of being inserted and extracted with all operational voltages present, with or without Or-ing diode option. Overshoot recovery and inrush current is the same as for turn-on.

Remote On/Off Signal
Standard. Contact closure to turn on. Contacts open to turn off.

AC Fail Signal
Open collector type signal under fault condition, 20V breakdown. During nominal operation, the AC Fail signal conducts up to 5mA maximum. There is a minimum of 16mSec hold-up time in the event of an AC failure or AC disconnect after the AC fail is activated.

Output/Inverter Good Signal
Open collector type signal under fault condition, 20V breakdown. During nominal operation, the Output/Inverter Good Signal conducts up to 5mA maximum. This signal will not alarm when the unit is in a parallel configuration with other units, batteries or at no load.

Auxiliary Bias Supply
12VDC at 50mA.

Front Panel Indicators
An AC present LED indicates that input power is applied to the unit. An output/inverter good LED indicates that DC output voltage is present and the inverter is operational. Operation is the same as output/inverter good signal. An overtemperature shutdown LED indicates that thermal shutdown has occurred. An output current meter LED ladder shows the approximate percentage of output current.

Operating Temperature Range
–40°C to +70°C ambient. From 55°C to +70°C, consult the factory for derating.

Storage Temperature Range
–40°C to +85°C.

Operating Humidity
0% to 95% (non-condensing).

Shock and Vibration
The FE Series is compliant with GR-63-CORE, Zone 4 Upper Level standards assembled in a NEBS-type FE Racking System.

Transportation
The FE Series is tested to MIL-STD-810E requirements.

Isolation Rating
Input/Chassis: 2.5k VAC
Input/Output: 3.0k VAC
Output/Chassis: 500VDC

Conducted Battery Noise
FE Series power modules comply with GR-1089-CORE and prETS300132-2 psophometric noise requirements.

Conducted EMI
FE0500 and FE1000 modules comply with FCC-CFR Part 15, Subpart J, Class A standards with 6dB of margin and with CISPR 22, Class A standards with 6dB of margin. When assembled into an FE-N standard racking system, the system is compliant with Class B standards.
FE1500 and FE2000 modules comply with FCC-CFR part 15, Subpart J, Class B standards with 6dB of margin and with CISPR 22, Class B standards with 6dB of margin.

Radiated Emissions
Class A specifications on modules and racks. FCC Part 15, Subpart J, EN55022.

Conducted Susceptibility (Output)
FE Series power modules comply with Bellcore GR-1089-CORE, 3A/meter and IEC-1000-4-6.

Radiated Susceptibility
All models comply with Bellcore GR-1089-CORE, 10V/meter and IEC-1000-4-3.

ESD
FE power modules comply with Bellcore GR-1089-CORE and IEC-1000-4-2.

Electrical Fast Transient
FE power modules comply with IEC-1000-4-4.

Lightning Surge
FE power modules comply with IEC-1000-4-5.

Physical Data

Model	Weight Lbs. Net	Lbs. Ship.	Dimensions (inches)
FE0500	6.0	7.0	11.97 x 5 x 2.0
FE1000	7.0	8.0	11.97 x 5 x 3.3
FE1500/2000	9.0	10.0	11.97 x 5 x 5.5
FE4K	15.0	18.0	12 x 5.25 x 17.75
FE5K	15.0	18.0	12 x 5.25 x 17.75
FE6K	15.0	18.0	12 x 5.25 x 17.75

Safety Agency Approvals
The FE Series meets safety agency approvals per UL 1950, EN60950, CSA22.2-234. All models are CE marked (Low Voltage Directive).

High Density	Lambda's new FE Series provides up to 6W/in³. In addition, a 3U height 19" rack can provide up to 6kW of power.
Low Cost	Less than 70¢/W for all models in OEM quantities — making the FE Series the lowest cost standard front end on the market today.
Modular and Scalable	Power modules can be added as your system scales. 4 power module sizes allow the system to be scaled in 500W, 1000W and 2000W increments.
Hot Plug N+1 Redundancy	Lambda's FE Series is specifically designed for hot plug N+1 operation to give your system 100% uptime and on-line upgradeability.
Integral Diagnostics	All models contain built-in diagnostics, metering and front panel status display, for remote or local monitoring for system diagnostics.
Automatic Fault Reset	Should an overvoltage, overcurrent or overtemperature condition occur in the system, the FE Series will automatically recover for remote site applications — without service personnel intervention.
Wide Range Input & Power Factor Correction	Full 85-265VAC, 50/60Hz operation ensures worldwide use. Power factor and harmonic correction per IEC-1000-3-2 with reduced input current.
Battery Plant Compliant	The FE Series is designed to drive float battery plants directly with low psophometric noise and constant current operation.
Worldwide Telecom and Safety Approvals	The FE Series is designed to meet Bellcore NEBS and ETSI standards, as well as UL, CSA and VDE requirements. All models carry the CE mark (Low Voltage Directive) for European compliance.
Standard Racking System	The FE Series is available in two racking systems, providing a high level of system versatility. The -N system features internal filtering to FCC Class B emissions standards, as well as front panel circuit breakers. The -X rack allows for increased power density. Both systems feature multiple input rails which enhance system fault tolerance.

The FE Series.

The first truly complete line of standard distributed power front ends can provide anywhere from 500W to 6kW in a 3U rack space.

To order, or for more information on the FE Series, call **1-800-LAMBDA-4/5**, 8am to 8pm, east coast time.

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The new FE Series.

LAMBDA Electronics Inc.

CMOS process.

The ADC12041 from National Semiconductor, while typical of most of the latest low-power CMOS ADCs, also is a 12-bit plus sign converter (maximum full-scale input voltage is ±5 V). Like many ADCs, it provides a pair of differential inputs and a pair of differential reference inputs. It also provides on-chip auto calibration and auto-zeroing on request by a host. With a parallel output, it comes in both a 28-pin SSOP, as well as a 28-pin PLCC. Unlike many of today's ADCs, it specifies a typical total unadjusted dc error (TUE) that comes to a maximum of ±1 LSB. TUE includes differential and integral linearity (DNL and INL) error plus offset, gain and common-mode error. All are specified as "after calibration."

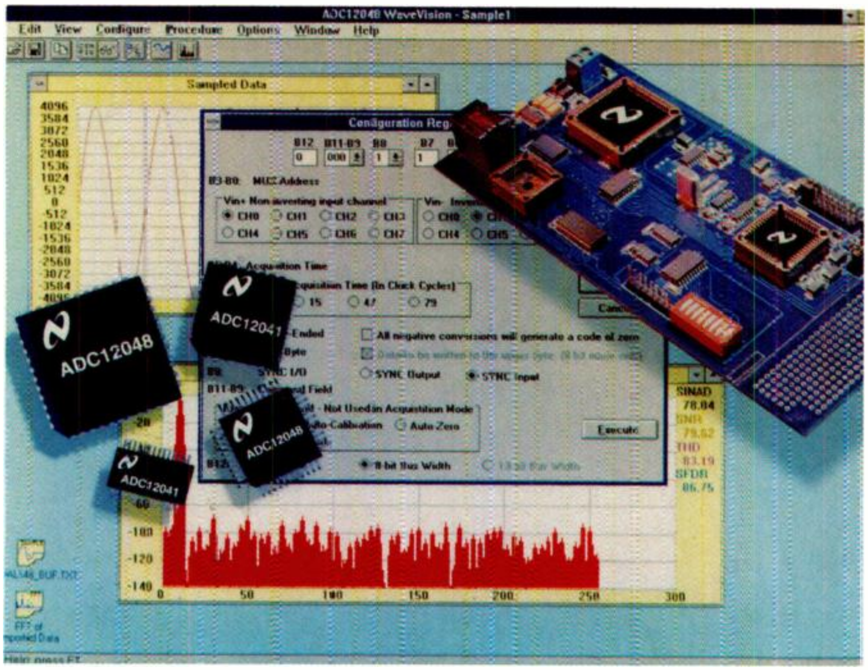
Another way to cut power is to reduce supply voltage; digital IC designers frequently do this. Some of these ICs will run on voltages as low as 2.7 V. Maxim's MAX1245 runs on just 2.375 V. Their MAX1241 provides 0.5 LSB INL running off 2.7 V while sampling at 70 kHz.

If a system designer needs a high-speed sampling converter, Philips' TDA8767 seems to be the way to go. This 30-MHz-sampling-rate ADC costs just $11 each. While its SNR runs 61 dB sampling 4.4 MHz at 30 MHz, its DNL runs ±1 LSB at dc.

A few years ago, delta-sigma (or sigma-delta) ADCs appeared on the scene and today, they dominate the arena above 16 bits. Now, 23-to-34-bit delta-sigma devices are available. And some of them are inexpensive. For example, the 23-bit Harris HI7191 goes for $6.98 each. And it's 12-bit accurate at dc and up to a few hundred hertz. Depending on the application, and with ADCs like the TDA8767 and the HI7191 in mind, general-purpose system designers should look closely at high-speed and high-resolution ADCs not usually aimed at their applications. □

Frank Goodenough may be contacted by fax at (617) 227-4426.

How Valuable?	Circle
Highly	525
Moderately	526
Slightly	527



COURTESY: NATIONAL SEMICONDUCTOR

ADCs With Multiplexers Are Shaping Up In Designs

PAUL MCGOLDRICK

Reading The Data Sheet Is Good Advice For ADCs; With Multiplexer Parts, It Is Critical In Buying The Right Part For Your Design.

Faster, lower-power, cheaper, smaller packaging. All the things happening with single-input ADCs (analog-to-digital converters) also are taking place with the multiplexed input parts. Some of the design results are more logical for the multiplexed ADCs. However, there are even more pitfalls for the unwary when working from a data sheet.

As pointed out in the previous report appearing in this issue, the use of analog multiplexers did not really catch on until system designers made CMOS parts relatively easy to design and implement *(see "12-Bit IC ADCs Becoming Commodity Components," p. 59)*. It also is the case that the means to make intelligent switching of the multiplexer needed a higher adoption level of microcontrol. Those two developments were more or less coincident.

Thinking of multiplexer parts as "commodity" items may be a strange way of expressing it, but it's a fact. The lowest-price 8-input ADC available is National Semiconductor's ADC12138. In 1000-unit lots, it costs $3.38 (that's 42.25 cents per channel; which can certainly be considered commodity pricing). The most-expensive 8-channel part available is Linear Technology's LTC1289, priced at $18.15 apiece in 1000-unit lots. That's $2.28 per channel. Are there differences between the parts? Sure, but enough for the enormous difference in price?

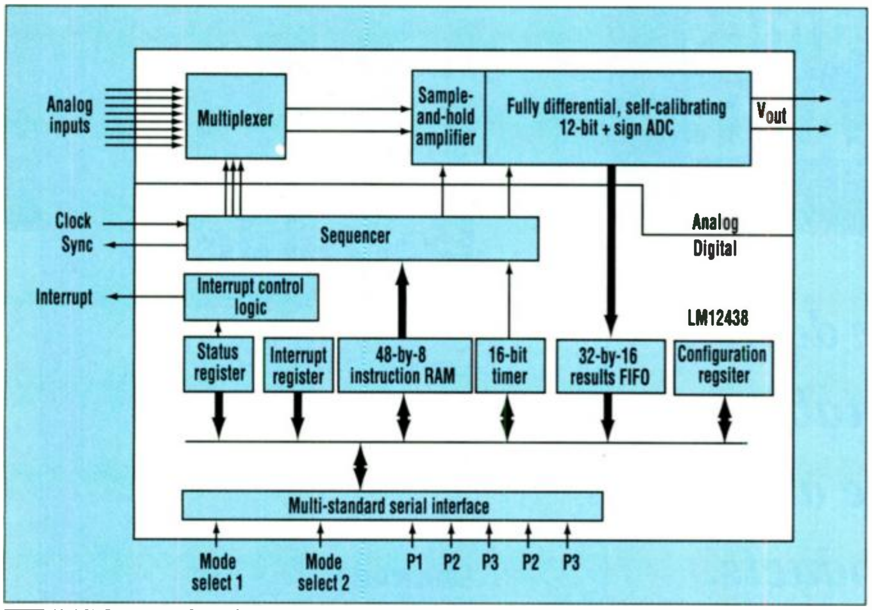
As is the case with the single-input parts, virtually all the multiplexed ADCs operate from single, 5-V rails—with a smattering working from 2.7 and 3.0 V, and one as low as 2.375 V. The majority have no internal references, most are switched-capacitor successive-approximation (SAR) types, and have the same power-down/sleep functionality. In addition, input levels are usually allowable to the reference voltage or higher (the design stories behind this for the 2.7-V parts is a special report in itself.) The vast majority of ADCs have serial I/Os, while those with parallel I/Os are among the fastest parts.

Why 12 bits? Are the ICs being used to take advantage of the resolution? In general, the answer is no. The majority of 12-bit devices are being used to take advantage of the dynamic range, simplifying or even avoiding the needs of scaling at the input. With multiple inputs, there is a large savings in external components when scaling is no longer a necessity in getting the required resolution. In other words, the majority of parts are being used to rather less than their full capability, but successfully. But there are "take-care situations" as well.

A COMPARISON OF LOW-COST 12-BIT ADCs WITH INTERNAL MULTIPLEXERS

Company	Model	Multiplexer inputs	Sampling rate (symbols/s)	Digital output	Price (1000-unit lots)	Comments
Analog Devices Call 1-800ANALOGD or (617) 329-4700	AD7862	2 x 2	250k	Parallel	$12.00	Dual-channel simultaneous sampling.
	AD7864	2 x 4	147k	Parallel	$15.00	4 sample-and-hold amplifiers and 1 ADC.
	AD7858	8	200k	Serial	$9.95	Both are available with 100-ksample/s rates at $6.95 and $7.60 each, respectively.
	AD7859	8	200k	Parallel	$11.75	
Burr-Brown Call 1-800 548-6132 or (520) 746-1111	ADS7824	4	40k	Parallel and serial	$12.30	
Linear Technology Call 1-8004-LINEAR or (408) 432-1900	LTC1288	2	6.6k	Serial	$6.35	Auto-shutdown 3-V operation.
	LTC1289	8	25k	Serial	$18.15	Auto-shutdown 2.7-V operation. Note 1.
	LTC1290	8	50k	Serial	$6.60	Note 1.
	LTC1291	2	54k	Serial	$9.40	
	LTC1293	6	46k	Serial	$9.40	
	LTC1294	8	46k	Serial	$9.40	
	LTC1296	8	46k	Serial	$8.35	
	LTC1298	2	11.1k	Serial	$8.15	
	LTC1594	4	16.8k	Serial	$6.15	Auto-shutdown operation. Note 2.
	LTC1594L	4	10.5k	Serial	$6.25	Auto-shutdown 3-V operation. Note 3.
	LTC1598	8	16.8k	Serial	$6.15	Auto-shutdown operation. Note 2.
	LTC1598L	8	10.5k	Serial	--	Auto-shutdown 3-V operation. Notes 3 and 4.
Maxim Call (408) 737-7600	MAX147	8	133k	Serial	$5.95	2.7 to 5.25-V operation.
	MAX186	8	133k	Serial	$6.95	
	MAX188	8	133k	Serial	$6.25	
	MAX196	6	100k	Parallel	$9.90	
	MAX197	8	100k	Parallel	$9.90	
	MAX198	6	100k	Parallel	$9.90	
	MAX199	8	100k	Parallel	$9.90	
	MAX1245	8	100k	Serial	$6.25	Note 8.
	MAX1247	4	133k	Serial	$5.80	Note 9.
National Semiconductor Call 1-800 272-9959 ext. 659 (Note 5)	ADC12030	2	70k	Serial	44.40	Note 6.
	ADC12032	2	70k	Serial	$4.40	Notes 6 and 7.
	ADC12034	4	70k	Serial	$4.60	Notes 6 and 7.
	ADC12038	8	70k	Serial	$4.80	Notes 6 and 7.
	ADC12048	8	222k	Parallel	$5.95	Note 7.
	ADC12062	2	1.0M	Parallel	$15.00	Note 7.
	ADC12130	2	70k	Serial	$3.09	
	ADC12132	2	70k	Serial	$3.20	Note 7.
	ADC12138	8	70k	Serial	$3.38	Note 7.
	LM12434	4	140k	Serial	$12.50	Note 7.
	LM12438	8	140k	Serial	$12.50	Note 6.
	LM12454	4	88k	Parallel	$12.50	Notes 6 and 7.
	LM12458	8	88k	Parallel	$12.50	Note 6.
	ADC12662	2	1.5M	Parallel	$20.00	Note 7.
	ADC12762	2	1.4M	Parallel	$12.00	Note 7. Not released at press time.
Sipex Call (508) 667-8700	SP8538	2	25k	Serial	$4.20	
Texas Instruments Call 1-800 477-8924	TLC2543	11	66k	Serial	$4.90	
	TLV2543	11	66k	Serial	$5.60	Note 10.

Notes: 1 = Full-duplex I/O; 2 = Part should be released by issue date; 3 = Part release date not known; 4 = Part not priced by press time; 5 = Most parts are self-calibrating; 6 = H versions (e.g. ADC12H030) are available, tested at an 8-MHz clock (instead of a 5-MHz clock). Price premium ranges from 50 to 90 cents more. L versions operate at 3.3 V. No price premiums on most parts; 7 = Multiplexer outputs and ADC inputs are available at part pinout. 8 = 2.375 to 3.6-V operation; 9 = 2.7 to 5.25-V operation; 10 = 3-V operation.



THIS FUNCTIONAL SCHEMATIC **of the National Semiconductor LM12438 ADC shows the extensive digital control that is available.**

The sample rate of the ADC will be effectively divided between the number of inputs being sampled. The sample rates, in general, of the multiplexed parts, are on the "low" side, so the effective sample rates may be extremely low.

All of this indicates that manufacturers expect the parts will be used on dc/near-dc sources and sensors. Indeed, designers may find it difficult with most data sheets to even find any kind of small-signal ac performance detailed. But then, some data sheets seem to be getting more obscure than they used to be—sample rates aren't even quoted on some of them. The applications information from the manufacturers becomes even more critical because of this. For review purposes, dual-input ADCs are included where they use a multiplexer *(see the table)*. In most cases, the inputs can be configured for a differential feed, but they're included for completeness.

As previously mentioned, even if an ADC is being used in near-dc sampling applications, it can be preferable in portable applications to use the higher sampling part when the IC can shutdown between samples. Such programmability is but one function that many of the devices allow. National's LM12438 8-input, serial-I/O ADC for example, epitomizes the company's stated commitment to "systems" with a slew of digital functions: 8 different conversion setups (from the 48-by-8 instruction RAM), a 16-bit timer, and on-chip storage of results with a 32-by-16 FIFO, all without any I/O intervention from the host microprocessor *(see the figure)*. The same functionality also is available on the LM12458, which has a parallel I/O. Manufacturers whose product lines are not restricted to analog will hopefully be able to develop such multiprogramming.

That is, indeed, the case with Texas Instruments' parts—the TLC2543 (5 V) and the TLV2543 (3.3 V)—where a seamless interface can be made with TI's DSP ICs such as the TMS320C25. Software is available for the interface as well. With 11 analog inputs, these ADCs also are the ones with the most multiplexed channels (actually 14 because the part also has three self-test channels) while consuming only 1 mA.

Offerings from Linear Technology are extremely varied. All are serial-I/O parts, while a number have auto-shutdown. The latest ADCs (1594 and 1598) have the multiplexer output available at a pin with the converter input available adjacent to it. This allows for the use of a single device, like a filter, to be applied equally to all inputs. The same capability is on a number of National parts. One 3-V device was available as of this writing, while a second, the LTC1594L, was expected to be available at this time. A third, the LTC1598L, is on an unknown schedule. The LTC1289 is a 2.7-V IC.

Maxim has both serial- and parallel-I/O chips, with the latter seemingly carrying a price premium. The MAX147 and MAX1247 are both 2.7-to-5.25-V parts, while the MAX1245 has the lowest operating voltage of all the multiplexed ADCs: 2.375 V. This allows it to run off the raw output of two cells (NiCd, NMH, or Li-Ion) right through most of the discharge cycle (typically 90%). The MAX197/7/8/9 family (the parallel I/O ones) have programmable input sensitivity. Four different input ranges can be set. In some instances, this internal scaling may give an apparent extension of the resolution. The Maxim parts also are particularly well protected from overvoltage, being tolerant to 16.5 V on the 5-V devices. In addition, an error or fault condition on one of the input channels should not affect the others. For the future, the MAX146 and MAX1246 will be 8- and 4-channel devices, respectively, used on 2.7-V supplies. Both will have a serial I/O with 113 ksamples/s and an on-board 2.5-V reference. The MAX1244 also will extend the range of 2.375-V devices.

National's range includes the fastest sampling parts in the survey with 1.5 Msymbols/s on an ADC12662. Most of National's parts have the multiplexer output at a pin—to allow a fixed process to be applied to all inputs—and higher-clock (8 MHz) and lower-voltage (3.3 V) versions are available on many parts.

The award for the most unusual architecture might go to Analog Devices for two ICs being released next month. The AD7862 is a four-input ADC, however, there are two completely separate 12-bit conversion paths, so two channels can be simultaneously sampled. The AD7864, which might logically be expected to be an 8-channel version of the above, is another surprise. It uses only one converter, and the four input channels each have their own sample-and-hold circuit before the multiplexer.

An interesting range of products. The next steps will, of course, will be to see the commodity label move upwards to higher-resolution devices. Many of the 12-bit ADCs are, in fact, 12-bit plus sign ADCs. Next? □

Paul McGoldrick's e-mail address is: 102447.346@compuserve.com.

How Valuable?	**Circle**
Highly	537
Moderately	538
Slightly	539

The Fundamentals Of Simultaneous Voice And Data

SVD Modems Are The "Talk" Of The Town This Fall. Here Is A Brief Introduction To A Number Of Voice/Data Technologies.

KARL NORDLING and RAPHAEL MEHRBAINS
Cirrus Logic Inc.,
3100 West Warren, Bldg. 1,
Fremont, CA 94538.

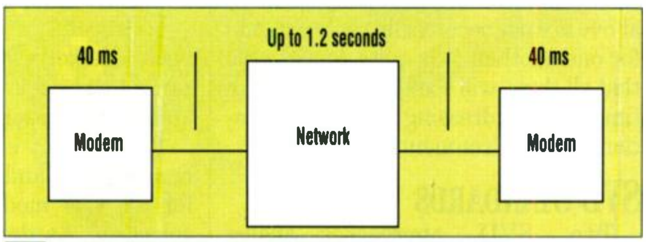
As modems have evolved to provide higher data rates and multimedia transmission capabilities, they have enabled PCs to evolve into multimedia communications devices. They now provide users with the ability to communicate via voice, text, or pictures over the same telephone connection at many levels of performance and functionality.

Even at the bandwidths of today's analog modems, applications such as electronic commerce, customer support, white-board conferencing, and limited videoconferencing are being developed, marketed, and used. Alternate voice/data (AVD), simultaneous voice/data (SVD), and H.324 videoconferencing are just some of the increasingly complex technologies that modem developers have created to address these applications.

General Considerations

Communications channels connecting two PCs (through modems or other devices like LAN or ISDN adapters) can be considered as pipes with no differentiation for the type of data transported. Various data types, however, have specific characteristics and limitations that must be closely considered and designed for in the communications device.

Two major issues that must be considered for specific data types are:



1. FACTORS AFFECTING LATENCY in a voice/data connection are illustrated here. At worst (two satellite hops plus maximum switching latency), the PSTN can contribute 1.2 seconds of delay. Typical figures run in the 50-to-100-ms range.

- The real-time nature of voice and video—latency issues.
- Error recovery issues.

Latency

Latencies, which are essentially the same as propagation delay, are created throughout a telephone connection. An accompanying illustration shows how an end-to-end connection can be modeled at the highest level as two modems, with the telephone network in between *(Fig. 1)*. The maximum latency through the public network is always less than 1.2 seconds, which corresponds to the round-trip delay of a connection involving two satellite hops with the delay caused by each hop estimated at 600 ms. This is a worst-case scenario which does not happen often, even during international calls. Typical delays for calls made within the U.S. is less than 50 to 100 ms for terrestrial connections and 600 ms for satellite connections. The 80-to-100-ms round-trip delay through the modems then becomes significant, especially when one considers the fact that latencies of over 200 to 250 ms start to become annoying to the user.

High levels of latency can be tolerated in data-mode applications. Once initial connection has been established, end users will not perceive any effects due to existing latency in the system. Latency in multimedia applications such as voice or videoconferencing, however, can be very annoying.

The effects of latency are commonly observed in videoconferencing situations. Most readers have probably experienced the effects of latency during international voice calls, such as when two users begin talking simultaneously. Another example of an environment where latency may cause drastic degradation of the end-user experience is the emerging but significant telegaming application. When playing games over a telephone line, it's critical to assure minimum delay so that each player's movements

DESIGN APPLICATIONS

UNDERSTANDING V.70 SIMULTANEOUS VOICE-DATA

Voice and data multiplexing

The third element of the DSVD solution is the multiplexer. ITU standards refer to this function as the V.gmux specification. As defined by the V.70 standard, multiple data streams have to be transmitted and received over a single communications channel. V.gmux describes a standardized procedure between peer stations for multiplexing/demultiplexing multiple streams of information at the same time. The V.gmux standard is based on the V.42 LAPM protocol using HDLC framing procedure. All error-recovery and detection protocols such as frame-check sequences (FCS) also are defined in this specification and include 8-, 16-, and 32-bit frame-check sequences.

In DSVD solutions, digitized voice streams are interleaved with data streams for transmission. Each frame header identifies the frame as a data or voice stream. As mentioned earlier, frames are resynchronized every 10 ms to facilitate error recovery.

SVD ARCHITECTURES

Implementation of multimedia functionality such as video, audio, and data communications requires special attention to the architectural partitioning of a personal computer.

Concurrency is always an important consideration for multifunctional applications. Many video, audio, and data communication functions require significant processing that could be implemented on a host processor, a dedicated accelerator, or a programmable accelerator. Optimum use of the alternatives outlined above depend on cost and concurrency goals and tradeoffs for a target application.

The telegaming application mentioned earlier happens to be one of the worst-case scenarios in MIPS requirements, and therefore warrants a closer look. In a telegaming application, the following communications functions are required to operate concurrently *(see the table)*.

Of course, communications is only a portion of the total MIPS requirement for telegaming. The most important aspects of the game are probably the 3D graphics and 3D audio, and they can easily consume all of the CPU bandwidth on their own. It is evident that each one of these functions can easily be implemented on the host. In order to take advantage of all of these functions for a telegaming application, however, significant acceleration is required.

On the other hand, host implementation of all or some of the features discussed above may be a reasonable trade-off for some applications. Host implementation of features is not only less costly, but it also provides a level of flexibility that cannot be achieved otherwise.

A final architectural issue that needs consideration is the use of resources by various subsystems in a PC. Audio and telephony functionality, and the necessary connection between the two, is one such case. Speakerphones have become a common resource available on several PC models. Audio and communications subsystems of a given PC require connection to the speakerphone. A hardwired connection between audio and modem subsystems is required in most current solutions.

The best system-level approach, however, is to provide a virtual connection in software between the two subsystems. In this type of implementation, the speakerphone acoustic echo-cancellation code can be implemented as part of the modem device, the audio device, or on the host. Both audio and modem systems can take advantage of the speakerphone hardware through a virtual (software connection). ☐

Karl Nordling joined Cirrus Logic in 1992, and is currently vice-president of DSP engineering at Cirrus's RSA subsidiary. Prior to that, he was the president and founder of Data Pump International, and Kinex. He has been active in the field of DSP since 1977.

Raphael Mehrbains received his BSEE in 1981, and his MSEE in 1983, both from the University of Michigan, Ann Arbor. He joined National Semiconductor in 1983 as a circuit design engineer, and joined Cirrus Logic in 1985, where he has held several engineering and marketing positions with graphics and communications groups.

HOW VALUABLE?	CIRCLE
HIGHLY	534
MODERATELY	535
SLIGHTLY	536

PERFECT BALANCE

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On a scale of one to ten, it's a 12. The 68HC12.

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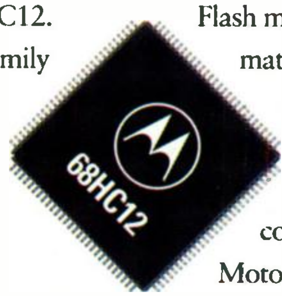

A perfect score. The 68HC12 is a highly integrated 16-bit architecture that is completely source-code compatible with Motorola's industry-standard 8-bit 68HC11 microcontrollers. Customers who need increased performance can now migrate designs directly up to the 68HC12 without sacrificing valuable investments in software.

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UPCOMING MEETINGS

JUNE 1997

International Solid-State Sensors and Actuators Conference (Transducers 97), June 15-19. Hyatt Regency Hotel, Chicago, IL. Contact Kensal D. Wise, 1246 EECS Building, University of Michigan, 1301 Beal Ave., Ann Arbor, MI 48109-2122; (313) 764-3346; fax (313) 747-1781.

Digital Cross Connect Systems Workshop (DCS 97), June 16-19. Banff, Alberta, Canada. Contact Richard Hamley, Stentor Resource Centre Inc., Room 500, 160 Elgin St., Ottawa, Ontario KIG 3J4, Canada, (613) 763-4591; fax (613) 781-2023; e-mail: hamleyrd@stentor.ca.

IEEE Sixth International Fuzzy Systems Conference, June 20-25. Barcelona, Spain. Contact Ramon Lopez De Mantaras, IIIA-CSIC Campus U.A.B., 08193 Cerdanyola del Valles, Spain; (34) 3-580-95-70.

IEEE Power Electronics Specialist Conference (PESC 97), June 22-27. St. Louis, MO. Contact Philip T. Krein, University of Illinois, 1406 W. Green St., Urbana, IL 61801; (217) 333-4732.

International Symposium on Information Theory, June 29-July 4. Ulm, Germany. Contact Han Vinck, Institue of Experimental Mathematics, University of Essen, Ellernstr. 29, 45326 Essen, Germany; (49) 201 3206458; fax (49) 201 3206425.

SEPTEMBER

AUTOTESTCON 97, Sept. 22-25. Disneyland Hotel, Anaheim, CA. Contact Bob Rassa, Hughes Aircraft Co., 2200 E. Imperial Hwy., Los Angeles, CA 90009-2426; (310) 334-4922; fax (310) 334-2578

OCTOBER

IEEE Ultrasonics Symposium, Oct. 7-10. Marriott Hotel, Toronto, Canada. Contact Stuart Foster, Dept. of Medical Biophysics, Room S-658, Sunnybrook Health Science Ctr., 2075 Bayview Ave., Toronto, Ontario, M4N 3M5, Canada; e-mail: stuart@owl.sunnybrook.utoronto.ca.

Sixth IEEE International Conference on Universal Personal Communications (ICUPC 97), Oct. 13-15. Contact Tony Acampora, MC 0409, Bldg EBU1, UCSD, 9500 Gilman Dr., La Jolla, CA 92093-0409; (619) 534-2486; e-mail: acampora@ece.ucsd.edu.

IEEE Holm Conference on Electrical Contacts, Oct. 18-22. Wyndham Franklyn Plaza, Philadelphia, PA. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

IEEE Telecommunications Energy Conference (INTELEC 97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan, Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; (61) 3 634 6216; fax (61) 3 632 3607

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 30-Nov. 2. Chicago Marriott Downtown, Chicago, IL. Contact Meeting Management, 2603 Main St., Suite 690, Irvine, California 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; http://www.eecs.uic.edu/-embs97.

NOVEMBER

IEEE Global Telecommunications Conference (GLOBECOM 97), Nov. 2-7. Phoenix, AZ. Contact Paul Narula, AG Communications Systems, Information Line, (602) 581-4297.

WESCON 97, November 4-6. Santa Clara and San Jose Convention Centers. Contact Electronic Conventions Management, 8110 Airport Boulevard, Los Angeles, California 90045-3194; (800) 877-2668; fax (310) 641-5117.

JANUARY 1998

Annual Reliability & Maintainability Symposium (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, Florida. Contact Jim Howard, Tampa Electric Co., Post Office Box 111, Tampa, Florida 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

MAY 1998

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP' 98), May 12-15. Seattle Convention Center, Seattle, Washington. Contact Les. E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, Washington 98195, (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

JUNE

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, Maryland. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, Maryland 21203; (410) 765-7348; fax (410) 993-7747.

JULY

IEEE Power Engineering Society Summer Meeting, July 11-17. Sheraton Hotel, San Diego, California. Contact Terry Snow, San Diego Gas & Electric, Post Office Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096.

ELECTRONIC DESIGN QUICKLOOK

EDITED BY MIKE SCIANNAMEA AND DEBRA SCHIFF

MARKET *Facts*

To paraphrase the singer Joe Jackson, "Why go out when the T.V.'s on?" Even better, why go to the movies at all, when you have your own personal theater in your living room? According to a recent Consumer Electronics Manufacturers Association (CEMA) study, at the end of 1995, nearly 11 million American households were entertained by their own home-theater systems. In its queries of 750 American households, CEMA found that 6% of respondents owned a mini-dish satellite system, with another 5% planning to purchase a satellite system within a year. The study watched factory sales of home theater products (the category includes: direct-view color T.V.'s 25 inches and larger, laserdisc players, projection T.V.s, hi-fi stereo VCRs, surround sound processors, amps and receivers, subwoofers, center channel speakers, and satellite surround speakers sold as separate units or as multispeaker packages) to learn that they rose 8% in the second quarter, with sales of $1.68 billion, compared to $1.56 billion one year ago. The six-month mark saw a 7% rise to $3.4 billion.

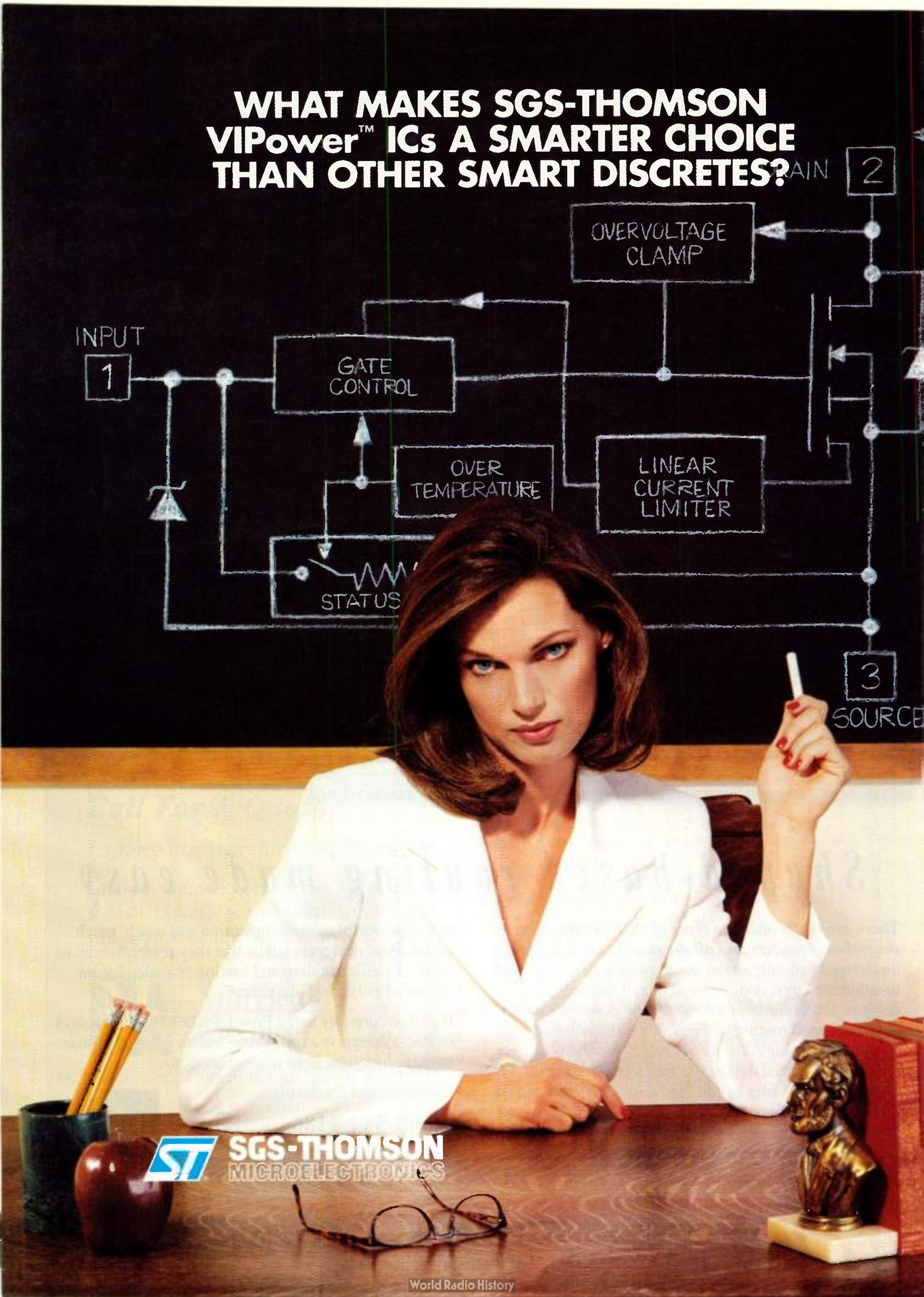
HOME THEATER FACTORY SALES*

IN MILLIONS OF DOLLARS

	2nd Quarter 1996	2nd Quarter 1995	% change
25" & Over Direct View T.V.	905	877	3%
Projection T.V.	241	236	2%
Laserdisc players	15	27	–46%
Hi-Fi VCRs	323	251	29%
Total video	1484	1390	7%
A/V Receivers, amps, & separates	107	106	1%
Speaker separates & packages**	85	60	42%
Total audio	192	166	16%
Total home theater	1676	1557	8%

*Totals may not add due to rounding. **Includes home-theater-in-box packages. Source: CEMA

Also posting a 7% gain in the second quarter was the home theater video market, thanks to large-screen T.V. and stereo VCR demand. Hi-fi VCR sales rose 29% to $323 million in the second quarter, with sales of $587 in the first half of the year. Dealers bought 3% more direct-view televisions that were 25 inches or larger in the second quarter than the first. The home-theater audio market gained 16% in the second quarter, with A/V receiver and amp sales up 1%. Speaker sales, on the other hand, including home theater-in-a-box packages, were up 42% in the quarter. In the blank media category, audio and video tape experienced a 3% drop in unit shipments, in the second quarter, but the first six months of 1996 found sales 2% ahead of the same period in 1995. The drop appeared after three consecutive quarterly gains. This may be attributed to the baby boom unit shipments of compact tapes (camcorder and 8-mm VCR media) that rose to over 12 million for the third time in the last four quarters. That figure is up 10% from the same time last year. VHS-C tapes had sales of 6 million units in the quarter, increasing 13%, while 8-mm standard tapes rose 18% to hit unit sales of 4 million. The old stand-by, standard VHS tapes, continued to rise in unit shipments, 10% to 81.3 million in the quarter, and in dollar sales, 6% to $132 million, with a nod to the Olympics. Blank audio tapes sank 6% in the first half of 1996, with unit shipments down for the third straight quarter. For more information on the study, contact Lisa Fasold at CEMA, 2500 Wilson Blvd, Arlington, VA 22201-3834, (703) 970-7669 or fax (703) 907-7690, e-mail lfasold@eia.org, or see the CEMA World Wide Web site at http://www.eia.org/cema. *DS*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OVERVOLTAGE CLAMP
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LINEAR CURRENT LIMITER
STATUS
2
3
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Service and Technology

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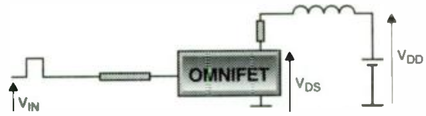


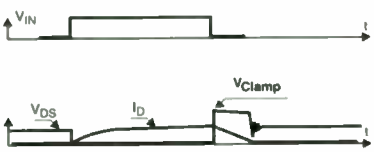
OVERVOLTAGE CLAMP

FEATURES

>Unrivaled energy handling
>Clamp internally set from 42V to 70V

BENEFITS

>No damage due to overvoltage spikes



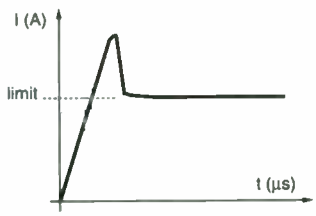
LINEAR CURRENT LIMITER

FEATURES

>Linear current limitation
>Fast step response

BENEFITS

>Load protection
>Adjustable current limit by changing the metal mask



GATE CONTROL

FEATURES

>Analog driving due to direct access to the gate of the Power MOSFET
>Logic-Level operation from a TTL/CMOS driver circuit

BENEFITS

>Pin to pin compatibility with standard MOSFET

OVER TEMPERATURE

FEATURES

>Short circuit protection
>Overtemperature protection
>Automatically restarts at 135°C

BENEFITS

>High safety in all environmental conditions

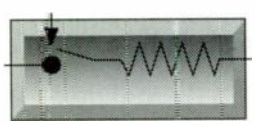
STATUS

FEATURES

>Overtemperature feed back through input pin

BENEFITS

>Real time monitoring



OMNIFETs - AUTOPROTECTED POWER MOSFETs

Type	V_{Clamp} (V)	$R_{DS(on)}$ (mΩ)	Package
VNW100N04	42	12	TO-247
VNW50N04	42	12	TO-247
VNP49N04	42	20	TO-220
VNP49N04FI	42	20	ISOWATT220
VNV49N04	42	20	PowerSO-10
VNB49N04	42	20	D2PAK
VNP35N07	70	28	TO-220
VNP35N07FI	70	28	ISOWATT220
VNV35N07	70	28	PowerSO-10
VNB35N07	70	28	D2PAK
VNP28N04	42	35	TO-220
VNP28N04FI	42	35	ISOWATT220
VNV28N04	42	35	PowerSO-10
VNB28N04	42	35	D2PAK
VNP20N07	70	50	TO-220
VNP20N07FI	70	50	ISOWATT220
VNV20N07	70	50	PowerSO-10
VNB20N07	70	50	D2PAK
VNP14N04	42	70	TO-220
VNP14N04FI	42	70	ISOWATT220
VNV14N04	42	70	PowerSO-10
VNB14N04	42	70	D2PAK
VNK14N04FM	42	70	SOT-82FM
VNP10N07	70	100	TO-220
VNP10N07FI	70	100	ISOWATT220
VNV10N07	70	100	PowerSO-10
VNB10N07	70	100	D2PAK
VNK10N07FM	70	100	SOT-82FM
VNP10N06	60	300*	TO-220
VNP10N06FI	60	300*	ISOWATT220
VNK10N06FM	60	300*	SOT-82FM
VND10N06	60	300*	DPAK
VND10N06-1	60	300*	IPAK
VNP7N04	42	140	TO-220
VNP7N04FI	42	140	ISOWATT220
VND7N04	42	140	DPAK
VND7N04-1	42	140	IPAK
VNK7N04FM	42	140	SOT-82FM
VNP5N07	70	200	TO-220
VNP5N07FI	70	200	ISOWATT220
VND5N07	70	200	DPAK
VND5N07-1	70	200	IPAK
VNK5N07FM	70	200	SOT-82FM

*V_{IN}=7V

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READER SERVICE 142

Edison Site On Most Endangered List

INVENTION FACTORY NEEDS FUNDING FOR REINVENTION

Throwing a wrench into the works of every bad joke aimed at New Jersey, the West Orange, N.J. invention factory of Thomas A. Edison served as the model for laboratories developed by General Electric, Westinghouse, and Bell.

Now, over a century since its opening, the Thomas A. Edison National Historic Site is on the list of the nation's most endangered landmarks. The West Orange research facility was the place where Edison perfected the alkaline storage battery, phonograph, and motion picture camera. The lab itself is one of his greatest triumphs, leading the field in team-based research and development.

According to the National Park Service, which operates the landmark, many of the five million documents and 390,000 objects stored throughout the 10 buildings remain uncatalogued and are in danger of being lost forever due to deteriorating conditions. In its heyday, the three-story main lab contained machine shops, an engine room, stock room, glass blowing and pumping rooms, a department dedicated to photography, experimental rooms, and a 10,000-volume library. Four smaller labs were stocked with the latest machinery and finest instruments for electrical, chemical, and metallurgical experiments. Any and all materials required by scientists and engineers in the course of their research also were stocked in the labs.

Edison opened his West Orange facility in 1887 and directed the lab until his death in 1931. Supporters of the facility are hoping that the renovations will include a multimillion dollar modernization project. It begins with Square D Company's electrical equipment donation and installation. Square D's self-proclaimed obligation to the landmark stems from its presence, in the form of products, in the lab for nearly 90 years.

If you're interested in contributing to the Thomas A. Edison National Historic Site, checks or money orders should be payable to: National Park Foundation/Edison Site, 1101 17th St., NW, Suite 1102, Washington, DC 20036. *DS*

INTERNET NEWS

CYGNUS SUPPORT has released IDK (Internet Development Kit), an Intranet enabling technology. IDK is an Intra/Internet middleware solution used to create World Wide Web front ends to existing company data while providing a web site production plug-and-play environment.

The package allows turn-key Intranet creation and Internet presence by providing highly optimized and stable development conditions. Cygnus has simplified and optimized the best versions of public-domain software for this offering, including: Perl 5 (programming language); Tcl (programming/extension language); Tk (Tcl-based windowing system); Expect (Tcl-based I/O event-driven state machine language); and the Apache HTTP Server package, the world's leading Internet server.

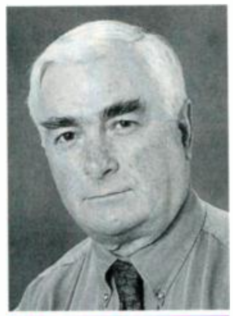
Users can download IDK from the Cygnus FTP site at no cost, or receive it on CD-ROM when they purchase a support contract. Information on how to download the package can be found at http://www.cygnus.com/product/inet/idk.

IDK is the first offering by Cygnus Support's new I*Net product line, focusing on the demand for Intra/Internet consulting, technology, and support. The line aims to broaden the Cygnus emphasis on strategic technical consulting, shared software, unique applications development, and customized levels of support.

For more information, contact Cygnus Support, 1937 Landings Dr., Mountain View, CA 94043; (415) 903-1400; (415) 903-0122; Internet: http://www.cygnus.com.

Letters from London

Going Dutch



PETER FLETCHER

It looks as though Philips Electronics of The Netherlands has taken one more positive step into the future. Back in the summer, the company mounted an exhibition of a number of "concept" products thought through by members of its corporate design department. They represented Philips' carefully crafted "Vision of the Future" (*Electronic Design*, Sept. 3, p. 64P), and were based on a whole raft of technologies. They ranged from micromotors to high-density solid-state memory that are due out of the research and development laboratories in time to be put to practical use in consumer, telecommunications and professional electronics products that may hit the market anytime between 2001 and 2006. (Instinct told me to refer to these years as 2k1 and 2k6, but common sense—and a Microsoft spelling checker— got the better of me).

One of the technologies that was featured in a high proportion of these "VoF" products—68 of them in fact—was the idea of a flat, flexible wide-area light-emitting display. According to the conceivers, this would be based on light-emitting polymer.

At the time, it occurred to me to wonder whether the company that holds the basic patents on this type of display had been consulted. It turns out that at the time that Philips had its vision, it hadn't. But that has now been corrected and Philips has signed a patent licensing deal with the inventors at Cambridge Display Technology Ltd., Cambridge, England.

The Dutch really had little option. A quick look at the list of patents that the Cambridge company holds title to around the world shows it has the plastic light-emitting business pretty well wrapped up. And any company that wants to make plastic displays will have to follow the same route. The list of 24 patent titles owned by CDT is impressive.

It covers virtually every aspect of the manufacture and application of light-emitting plastic from manufacture of organic LED's; nitrile polymers; organic light-emitting diode color display; organic light-emitting diode display (EL device); patterning; photoresponsive materials; polymers in photodetectors; and polymer protection for electrochromic displays; electrooptic modulators; fabrication of organic LED's (composite LED's); stacked EL devices; and tuning co-polymers.

The upshot is that Philips Components has paid a multimillion dollar sum upfront and is committed to shelling out for royalties for the right to use the patents. So far, the Dutch company has not revealed exactly what it intends for the technology, or to reveal more details of its new license, except to confirm that "there will be no transfer of technology from CDT." However, visitors to Philips' web site at http://www-eu.philips.com/design/vof/ can make some pretty shrewd guesses at where any light-emitting plastic components might find their niche.

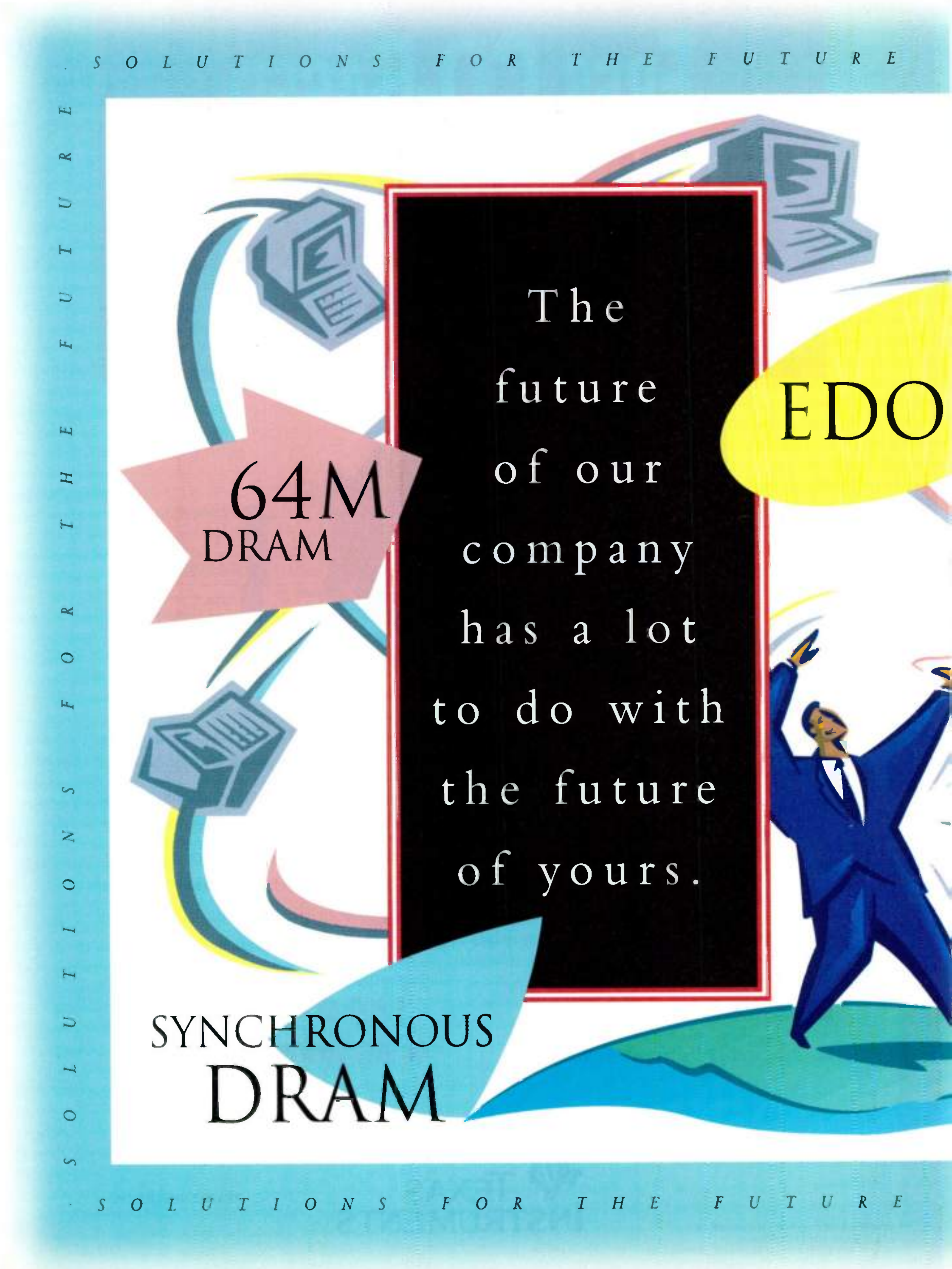
In the meantime, CDT is busy negotiating with the next company in the line. At present, Mark Gostick, CDT's marketing director, won't say who that might be. But he did tell me that it will be aimed at ensuring a ready supply of the right type of polymer raw materials that mass producers such as Philips will need to get LEP production lines rolling. You could always ask Mark directly—his e-mail address is: mgostick@cdtltd.co.uk. Those interested in the physics and chemistry of these devices will find a visit to http://www//cdtltd/co.uk rewarding.

Peter Fletcher is Electronic Design's U.K. correspondent. His e-mail address is: panflet@cix.compulink.co.uk.

OFFERS YOU CAN'T REFUSE

Software that measures the speed of parallel port transfer is available free of charge from Shuttle Technology. The PPTool software allows users to compare the rate of parallel port transfer to that of other interfaces, like SCSI and ATAPI. Users install the software and receive a full assessment of speeds achieved when transferring files. The next version of the software will enable users to compare data transfer speeds using various peripherals such as CD-ROMs, printers, and backup devices. The software can be downloaded from Shuttle's web site at http://www@shuttletech.com. Contact Shuttle Technology Inc., 43116 Christy St., Fremont, CA 94538; (510) 656-0180; fax (510) 656-0390.

Aldec is offering a complimentary copy of its State Machine and HDL editor tools, which are part of the ACTIVE-CAD Development Series, via the World Wide Web. The copy has no limitations and supports ABEL, Verilog, and VHDL. It includes all interfaces to PC-based synthesis tools along with a very comprehensive tutorial. The Graphical State Machine Editor and HDL Editor, complete with Language Assistant and HDL Design Wizards, is provided in an attempt to help educate schematic centric design engineers about HDL design tools. The State Machine Editor is a graphical design entry tool that uses the familiar concept of finite state machines to design complex control diagrams. The editor handles both Mealey and Moore designs and allows for the graphical entry of hierarchical and concurrent state machine designs. The complimentary copy of the State Editor and HDL Editor is available for a limited time at http://www.aldec.com. Contact Aldec Inc., Three Sunset Way, Suite F, Henderson, NV 89014; (702) 456-1222; fax (702) 456-1310.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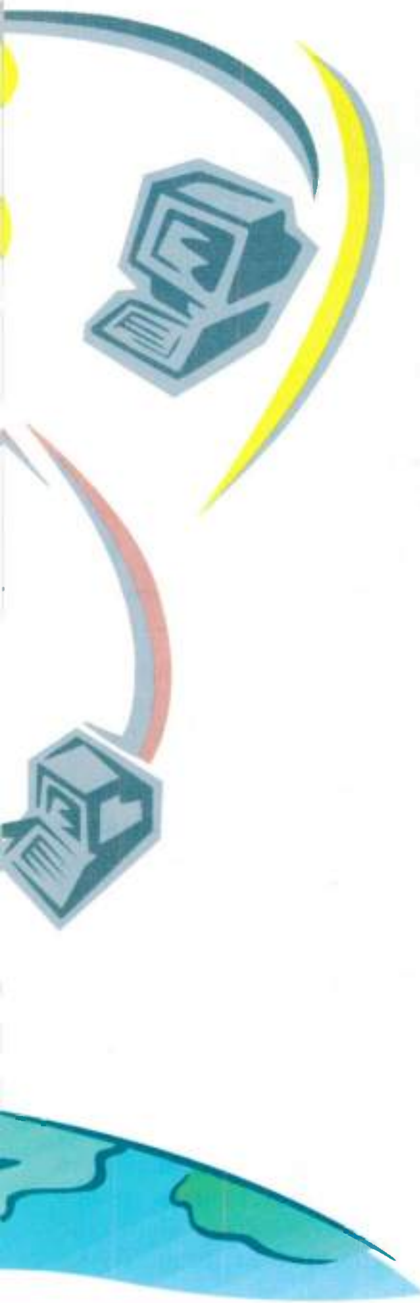

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S O L U T I O N S   F O R   T H E   F U T U R E

HOT PC PRODUCTS

WideNote is a wide-screen format notebook computer designed to allow users to view their spreadsheets without a lot of horizontal scrolling. According to Sharp Electronics, WideNote's manufacturer, the 9.625 in.-by-5.625 in. screen is 50% brighter than ordinary notebooks. It accommodates two World Wide Web pages or two windows applications on screen simultaneously. WideNote comes with a built-in 28,8kbytes/s voice/data/fax modem, in addition to 16-bit stereo sound and speakers. The notebooks run $2999 to $3499. Contact Sharp Electronics Corp., Sharp Plaza, Mahwah, NJ 07430; (201) 529-8737; fax (201) 529-9597; Internet: http://www.sharp-usa.com.

OPEN/stor 2.0 is hierarchical storage management software for Windows NT 3.51 and 4.0. Based on a three-tiered migration strategy, Wang's new software moves inactive files from the server's hard disk to a separate disk storage unit, then on to optical and tape libraries for long-term storage. OPEN/stor's features include disaster prevention by writing to disk and tape simultaneously, and recalling files from storage back to clients. The software is priced from $2995. For more information, contact Wang Software Storage Management Group, Wang Laboratories Inc., 600 Technology Park Drive, Billerica, MA 01821-4130; (508) 967-5000; Internet: http//www.wang.com.

Epson has introduced the LQ-2070, a letter-quality dot matrix printer designed for large and small business applications. The 24-pin wide-carriage forms printer offers faster output and eight built-in barcode fonts, including two UPC codes and Postnet. The LQ-2070 prints at 300 characters per second at 10 characters per inch in high-speed draft mode. The new carriage design prevents ribbon wear by four times as

much as the LQ-1070, its predecessor. The printer is plug-and-play ready and comes with a driver disk that features software for programming defaults, rather than front panel or DIP switching methods. Contact Epson at 20770 Madrona Ave., Torrance CA 90503; (800)-GO-EPSON; Internet: http//www.epson.com.

BOOK REVIEW

Need to design a chip with a hardware description language (HDL)? If so, do yourself a favor and get Douglas Smith's new book, *"HDL Chip Design."* It offers a tutorial approach to using HDLs that's basic, practical, and easy-to-read. The book is intended for both the experienced and novice engineer. A broad range of topics makes it suitable as a teaching aid for beginners, and also as a reference book for accomplished designers.

The 464-page book, priced at $65, is printed in an easy-to-see 8.5- by 11-in. format. It starts with the basics by describing ASICs and FPGAs, the similarities and differences of VHDL and Verilog, and electronic-design-automation (EDA) tools for chip design. The second chapter discusses synthesis constraints and optimization. And there's one whole chapter devoted to practical design and modeling, recommendations, issues, and techniques. The book finishes with practical modeling examples. For instance, it shows six ways to model the same decoder in VHDL, three ways in Verilog, and discusses the merits of each. A comprehensive glossary explains all the terms used in the book. There are two appendices: one for VHDL and one for Verilog. And an index makes finding topics easy.

Both the VHDL and Verilog languages are covered equally throughout the book in an unbiased manner, with VHDL and Verilog models shown side-by-side. In fact, the book contains over 160 modeled examples. Synthesized circuits from either the VHDL or Verilog model are included. In addition, simulated waveforms are shown with the models where appropriate. An added bonus is that a disk containing all the examples in the book is available for an extra $15.

Also keep in mind that there's no risk in buying this book—satisfaction is guaranteed. Customers can get their money back within 15 days if they don't like what they see. Information about the book can be found on the Web at: http://fly.hiwaay.net/~asmith.

Douglas J. Smith can be contacted at Doone Publications, 7950 Hwy. 72W #G106, Madison, AL 35758; (205) 837-0580; e-mail asmith@hiwaay.net.

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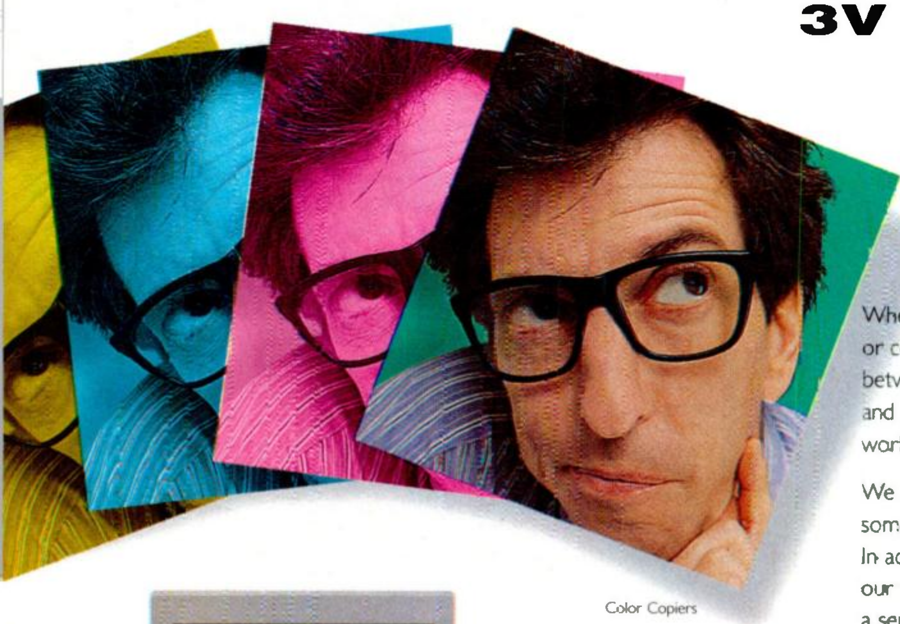
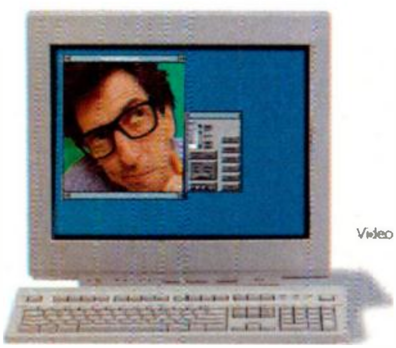


Color Copiers



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XRD87L94	12 bits	1 MSPS	3V	40mW	$17.44

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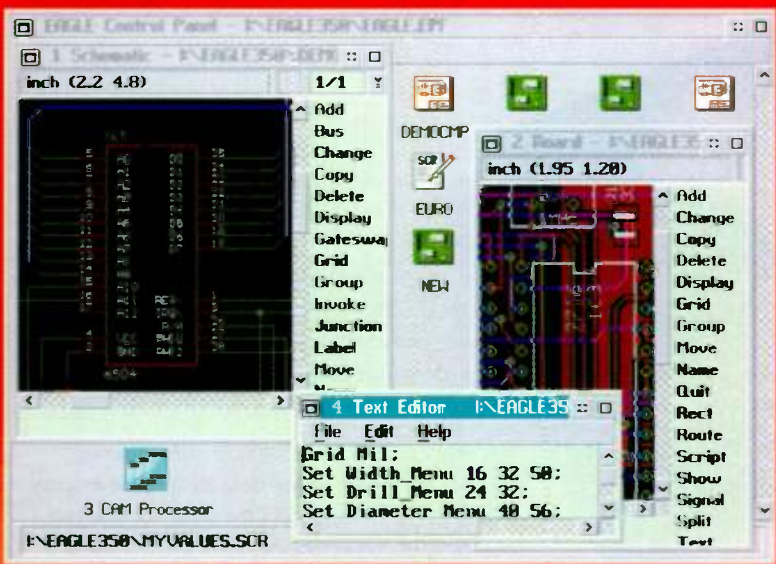

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CIRCLE 520

Digital Variable-Gain Amplifier

CARL E. DICKEY, National Semiconductor Corp., Comlinear Div., 4800 Wheaton Dr., Fort Collins, CO 80525-9483; (970) 226-0500; fax: (970) 226-0564; e-mail: carl.dickey@cc.com.

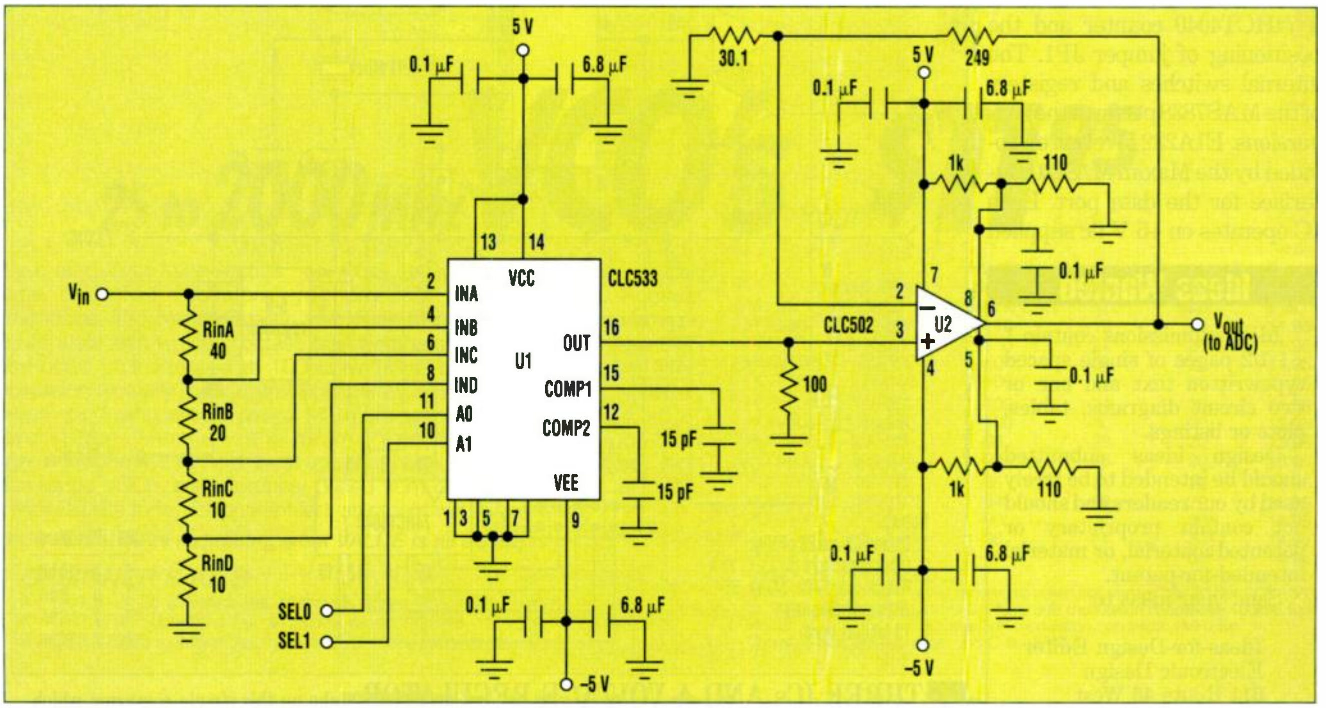
Digital receivers and digital back-channel modems employ a high-speed, analog-to-digital converter (ADC) to extract baseband information from a carrier signal. To increase the dynamic input range of these receivers and modems, an automatic-gain-control (AGC) circuit is often placed upstream of the ADC. Traditionally, these AGC circuits include a variable-gain amplifier (VGA) with an analog feedback circuit to generate the necessary gain and attenuation control signal. However, many of these applications currently employ at least one digital signal processor (DSP) to channelize, filter, and discriminate the baseband information.

These days, it's common practice to employ the DSP to supervise the AGC process through a VGA placed upstream of the ADC. To provide the analog gain-control signal that most high-performance VGA's currently require, the DSP is usually interfaced to the VGA through a digital-to-analog converter (DAC). A digital variable-gain amplifier (DVGA) can be controlled directly by the DSP, eliminating the analog gain-control signal and the associated DAC *(see the figure)*.

The CLC533 is a high-speed 4:1 analog multiplexer. It's controlled with TTL, CMOS, or ECL logic applied to A0 and A1. As the analog multiplexer is switched between inputs A-D, the voltage divider formed by R_{in}(A-D) is selected to provide attenuation in 6-dB steps. The multiplexer's output is attached to the noninverting input of a CLC502 clamping amplifier. The input resistor values can be recalculated if different attenuation steps are required. However, the input resistors should be kept low in value to minimize offset effects caused by the multiplexer's input bias current. In addition, some applications may need a characteristic terminating resistance for best transmission. The required input conditions, step sizes, and part availability are formed into a set of constraining equations that are solved simultaneously to obtain the input resistor magnitudes.

The clamp levels are set by the voltage dividers attached to pin 5 and 8 on U2. Because most ADCs have an input range of 1-2 V p-p, the clamping feature ensures that the ADC is never overdriven. The clamping amplifier must have very fast overdrive recovery so that data conversion can be quickly reestablished once the signal returns to acceptable levels. The clamping amplifier used in this design recovers in 8 ns from a 2X overdrive. Higher recovery speeds can be achieved with a CLC501, which typically recovers in 1 ns from a 32X overdrive.

This circuit is well-suited to drive complex loads such as those presented by flash converters. The output will typically settle to 12 bits in approximately 35 ns and to 14 bits in approximately 60 ns when driving a 500-Ω load. When driving a 100-Ω load, it may be necessary to add a small 5 to 10-Ω resistor in series with the power supply traces. Very fast



THIS DIGITAL VARIABLE GAIN AMPLIFIER (DVGA) provides a dynamic input range of approximately 80 dB at frequencies up to 45 MHz.

PEASE PORRIDGE

several thousand dollars. But if the guy next door is able to buy a 1987 Cadillac for $1000 because a guy in California (or New Jersey or Connecticut) had to get rid of it—then your car is NOT worth nearly as much as you thought it was.

The guys who sell cars are going to love this. They think *you* will cheerfully buy a new car to replace that 10-year-old lemon that nobody can get through smog. Well, if I just had to sell off a perfectly good, reliable, comfortable old 1986 car for $1000 because nobody—not even the Agency—could get it to pass smog, then I am surely not going to cheerfully buy a new car. I may not be able to afford one....

Will the lines at the Official State Repair Stations get any better? I doubt it. Maybe if they let you get your own car repaired, that will help. But for the next 1.6 years, there will be a LOT of cars every month that are introduced to tough tests. Only after all cars have been through the new system once will the repair mess get better.

Will it be true that some cars are more valuable, because it IS possible to keep them well tuned up, and in spec? I guess so. What kind will that be? I don't know. But obviously, my old Beetle seems to be doing OK. If you know a mechanic who can get your Beetle through the test by twisting a screw in the right way—that sounds good to me. What are the test limits for a 1968 VW?

1968 VW TEST LIMITS

Hydrocarbons LIMIT		CO LIMIT	
@IDLE	700 ppm	@IDLE	5.50%
My results	34 ppm	My results	0.34%
@2500 rpm	600 ppm	@2500 rpm	4.50%
My results	16 ppm	My results	0.21%

—So—don't just tell me that all old cars are dirty and fouling and polluting. A well-maintained old car can be both fairly clean and economical.

Anyhow, while this story is copyrighted, please feel free to pass it around to your friends as a public service. There is entirely TOO MUCH misinformation, disinformation, and ignorance on this subject. And if anybody learns stuff, let me know. I KNOW that I don't know the whole story, but I know enough to be of some help.

I wish the bureaucrats and legislators would level with us. I wish they did not try to argue that a car that is 4% less than the Spec is GREAT, but a car that is 4% over spec is a GROSS POLLUTER. I wish they did not try to pretend that when the DMV tries to order you off the road until their 2-month-backlogged repair station can look at your car, that is not a form of CONFISCATION. Even if you could get your car fixed, they won't let you. And they will not tell you what you need to know. That is the WORST kind of bureaucracy.

I wish the Smog Fearmongers did not exaggerate so much. They bend the truth, and tell partially-true stories, almost as badly as the bureaucrats do. I wish not so much Bullbleep was going on....

Latest developments: In Sacramento, 46 legislators said they want to put these regulations on hold until they can rewrite them. The bureaucrats just say, No Way. I think I'll go chew on *my* representative's ankles.

Also, one guy pointed out that some lawyers are putting together class-action suits. They are zeroing in on the administrative errors of depriving people of their property, WITHOUT due process, AND with no right of judicial review, because of the insufficient repair facilities. Hmmmm.... They also are working on the aspect of discrimination based on unequal treatment of property based on age. Why are some of the Gross Polluter limits set arbitrarily high—or low?? Such a mess!

And as Anatole France said, "The law, in its majestic equality forbids the rich as well as the poor to sleep under bridges...." It sure is strange when we find ourselves pulling for the lawyers!

I'm in favor of clean air and low pollution as much as anybody. But let's be fair about how we do it.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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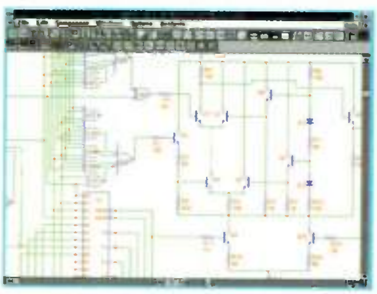

Micro-Cap V gives you a sketch and simulate environment that's easier to learn, easier to use. Aided by familiar SPICE models and extensions, a multi-page hierarchical schematic editor and a massive device library with models for over 7500 parts, you work quickly and smoothly—one keystroke, for example, initiates on-line simulation.

Further, this triumph comes at a very acceptable cost—$3495—less than half the price of would-be contenders.

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We could go on, but our free brochure and demonstration disk can give you all the details. Ask for them. And begin reaping the rewards of total victory.

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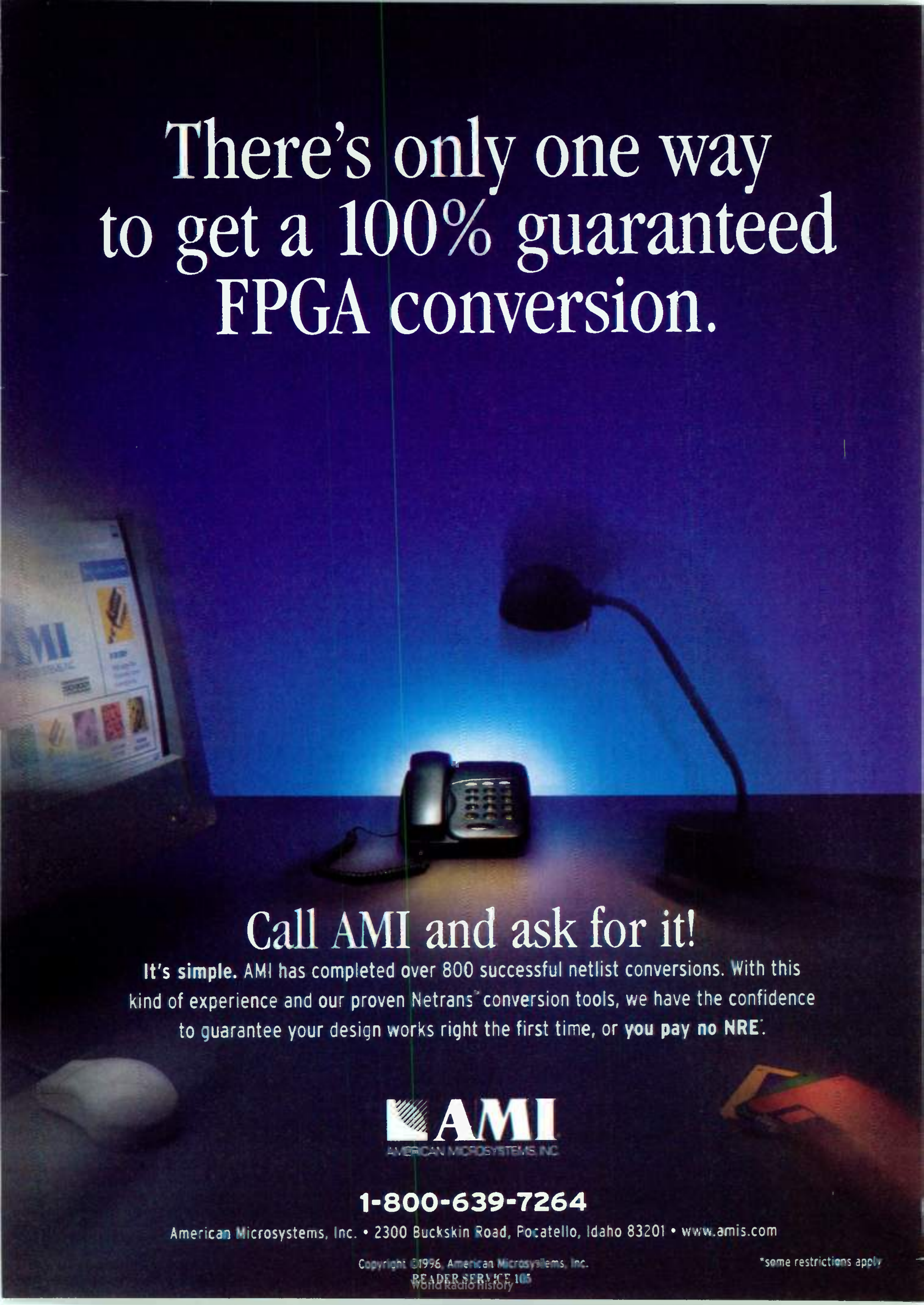
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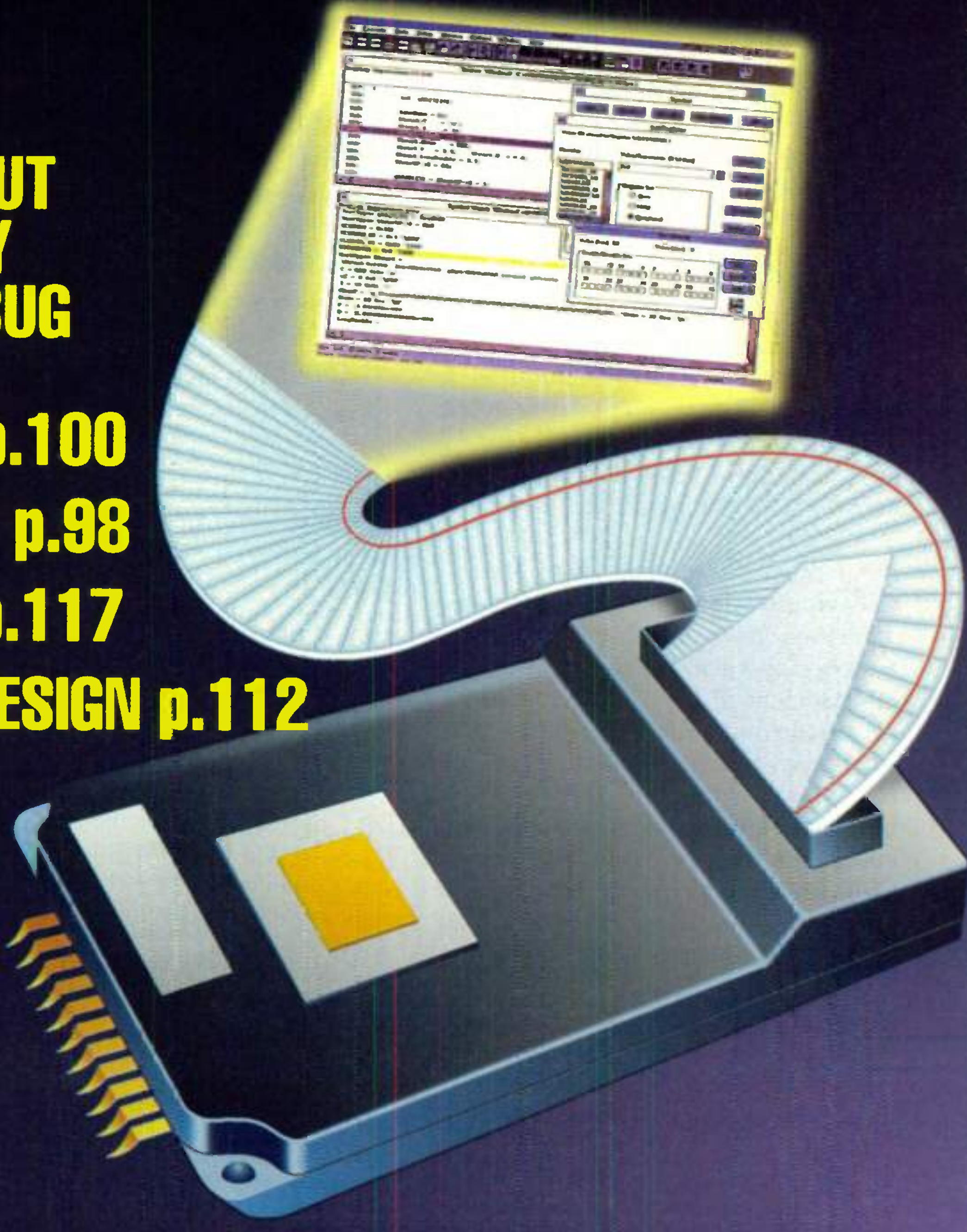
ENGINEERING SOFTWARE

FOR SOFTWARE DESIGN ENGINEERS



TOOL Talk

Carnegie Mellon University's Andrew Consortium has released the first C++ version of its Andrew User Interface System (Andrew 7.4). It is an integrated suite of compound document applications with which Unix users can create documents containing combinations of text, pictures, graphs, figures, spreadsheets, and other embedded objects. Available free of charge, the software has been released in binary form, and can be found on the World Wide Web at http://www.cs.cmu/~AUIS. Contact the university at (412) 268-2900.

Sun Microsystems Inc. has selected Aspect Development Inc.'s Explore CSM system and VIP component reference databases to support its new, enterprise-wide CAD Component Library Management Program, as well as Sun's preferred part and supplier programs. The new system provides Sun's designers with desktop access within their standard design tools to internal Sun preferred data and on-line reference data for all other parts available on the market. Contact Aspect Development at (415) 428-2700; fax (415) 968-4335.

Six private and government-sector Chinese telecommunications manufacturers have adopted Integrated Systems Inc.'s (ISI) pSOSystem for the development of their next generation of telecommunications products. This establishes pSOS as a standard kernel for China's ongoing initiative to become a global telecommunications equipment leader, while decreasing China's reliance on imports for domestic infrastructure requirements. Contact ISI at (408) 542-1500; fax (408) 542-1950.

MediaPhonics and Analog Devices have jointly agreed to market and develop the MediaPhonics Galileo platform. Galileo is an architecture that provides true integration of telephony into PCs, whereby the telephone becomes an actual computer peripheral. The architecture has been designed to run on an Analog Devices chip set, in full compliance with Microsoft Windows 95 TAPI. It will allow manufacturers to design PC cards with the most powerful features currently available for telephony-voice-modem and audio on the same card. Contact Mediaphonics at +33 1 69 47 44 20 or Analog Devices at +33 1 46 74 45 08.

American Megatrends Inc. (AMI) announced a technology agreement with SGS-Thomson Microelectronics to provide firmware support for its ST486 dedicated microprocessor family. AMI will provide firmware and OEM support for SGS-Thomson's new semi-custom ST486 microprocessor to be used on low-cost, PC-based entertainment systems. Contact AMI at (800) 828-9264; Internet: http://www.megatrends.com.

TRENDS TO WATCH

Two research contracts from the U.S. Department of the Navy have been awarded to Software Productivity Solutions Inc (SPS). The two contracts are six-month studies where SPS will conduct extensive leading edge research and development to develop solutions for highly challenging problems in software engineering. The first contract, "Tempus: A Real-Time Measurement Project," predicts the performance of a real-time system early in its development. Based on fundamental measurement theory and practical aspects of software operation, a scientific approach is needed to build on existing technology to specifically target critical timing issues related to real-time software development. The second contract, "Rapid Application Prototyping and Development (RAPAD)," applies a model-based architecture-directed approach to support rapid prototyping. It addresses the needs of reducing development costs, improving overall system quality, and meeting performance objectives. Contact SPS at (407) 984-3370; fax (407) 728-3957.

Established in 1992, the Telecommunication Information Networking Architecture Consortium (TINA-C) attempts to define and validate open architectures for telecommunications service provisions, with focus on broadband and multimedia systems. A specification known as the Distributed Processing Environment (DPE) outlines an architecture for implementing services based on distributed computing and object orientation. One of TINA-C's newest members is IONA Technologies, who pledges to contribute to the DPE architecture with functionality already available in COBRA and Orbix. Contact IONA Technologies at (617) 679-0900; fax (617) 679-0910; Internet: http://www.iona.com.

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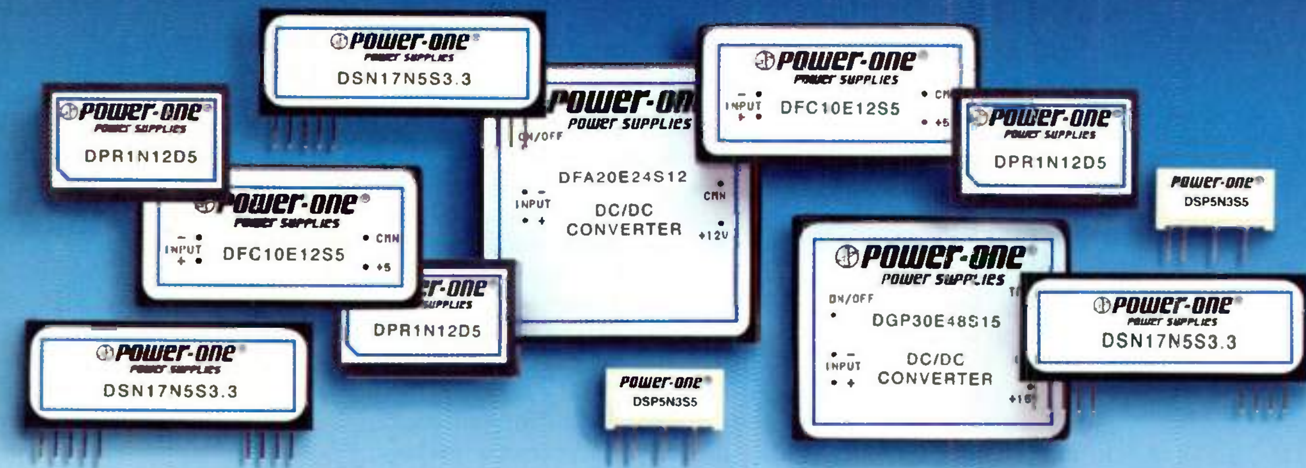

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DFA6	6	9-27, 20-60		•	•		•		•	
DFC6	6	3.5-16		•	•		•		•	
DFC10	10	9-18, 18-36, 36-72	•	•			•		•	
DGP12	12	3.5-16		•			•		•	
DFC15	15	20-60		•			•		•	
DSN17	17	4.5-6, 6.5-15.5	•	•						
DFA20	21	9-18, 18-36, 36-72	•	•			•		•	
DGP30	30	36-72		•			•		•	
Dual Output products provide the indicated Vout as one positive and one negative output										
DSP1	1	4.5-5.5		+/-		+/-	+/-	+/-	+/-	+/-
DFC10	10	9-36, 18-72		+/-			+/-		+/-	
DGP12	12	3.5-16		+/-			+/-		+/-	
DFC15	15	20-72					+/-		+/-	
DFA20	20	9-18, 18-36, 36-72		+/-			+/-		+/-	
Triple Output products provide a main output (•) and two symetrical outputs (+/-)										
DGP20	20	9-18, 18-36, 36-72		•			+/-		+/-	

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READER SERVICE 167

Bond-Out Technology Helps Debug Real-Time Problems

Gerd Lammers
KONTRON ELEKTRONIK

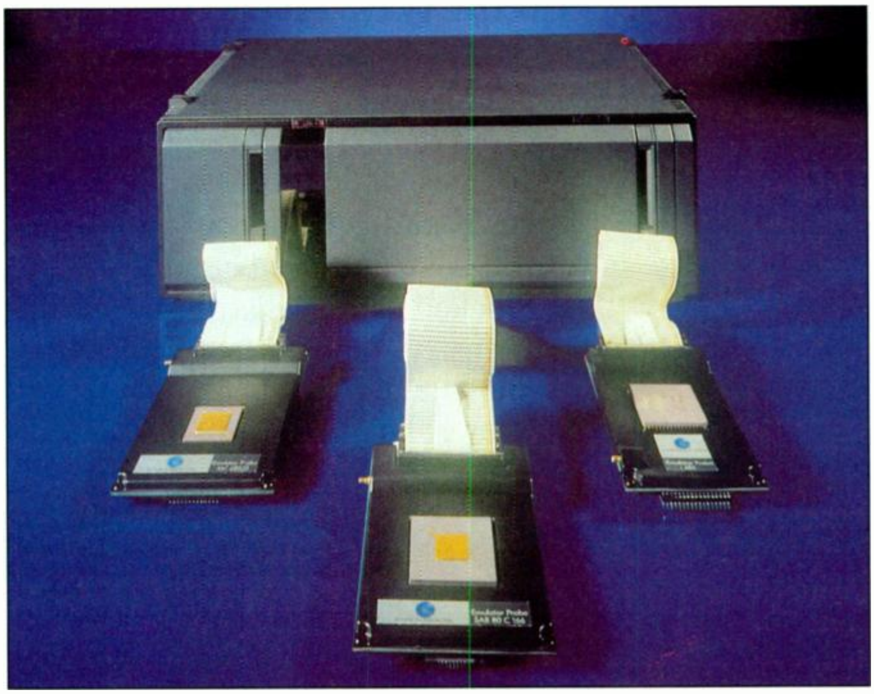
There was a time when embedded firmware was written by hardware designers who focused on assembly-language programming. In those days, the job of an in-circuit emulator was much simpler than it is now. Today, developing software for real-time embedded systems often entails high-level programming. As a result, today's emulators must decode C++ and Ada, keep track of symbols and the locations of stored data, and be aware of how code is optimized.

At the same time, the CPUs executing the software also have grown faster and more complex. In fact, the conventional signal pins on the processor may be inadequate for an emulator to acquire details about how a real-time program is executing. As a result, to widen the window that an emulator has into a CPU, some processor manufacturers, working closely with emulator manufacturers, have begun offering special "bond-out" versions of their CPUs to be used by the emulator as the target processor *(Fig. 1)*. Bond-out chips have wires bonded to the processor's normally unconnected package pins. On the die side, these wires give added access to the processor's internal signals. In this way, they allow an emulator to monitor and control internal states that would otherwise not be accessible.

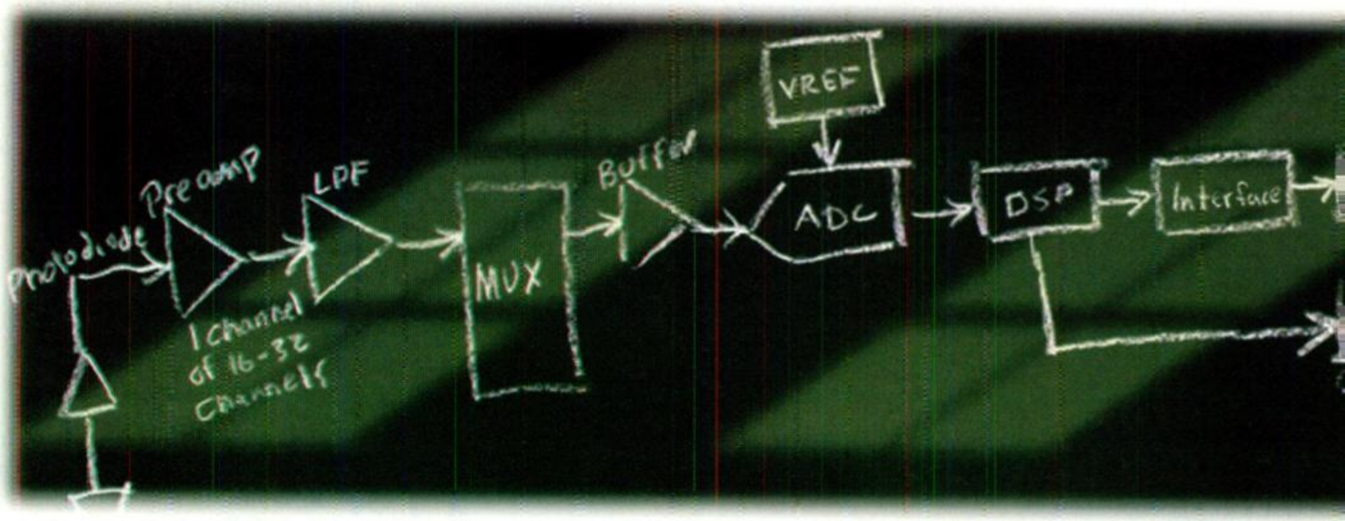
The development of bond-out technology requires close cooperation between both chip and emulator manufacturers, as well as with compiler vendors that provide the symbolic information needed to perform high-level language debugging using the emulator *(Fig. 2)*. A number of companies supply emulators using i386 EX bond-out technology, including Applied Microsystems, Microtek International, Emulation Tools, and Kontron Elektronik. In particular, systems from Kontron Elektronik emulate Intel's i486 family and its derivatives, including the SL Enhanced i486 and other ultra-low-power architectures.

To understand how bond-out wires help a designer better wield an emulator, consider the basic requirements for debugging real-time, embedded software. For the most part, a designer codes the logic of the application on a workstation and cross-compiles it to the binary form used by the target CPU. The point where embedded real-time development differs radically from general software development is when it comes to mating the code to the target hardware.

In integrating real-time software with the target system, several factors become apparent. First is the interaction of the code with the CPU's RAM and ROM, as well as its on-board peripherals, such as UARTs. The other critical aspect is timing; making sure that what happens within



1. THE KONTRON ELEKTRONIK *5SE5 places buffer memory at the probe head therby reduceing signal delays to less than 1 ns.*



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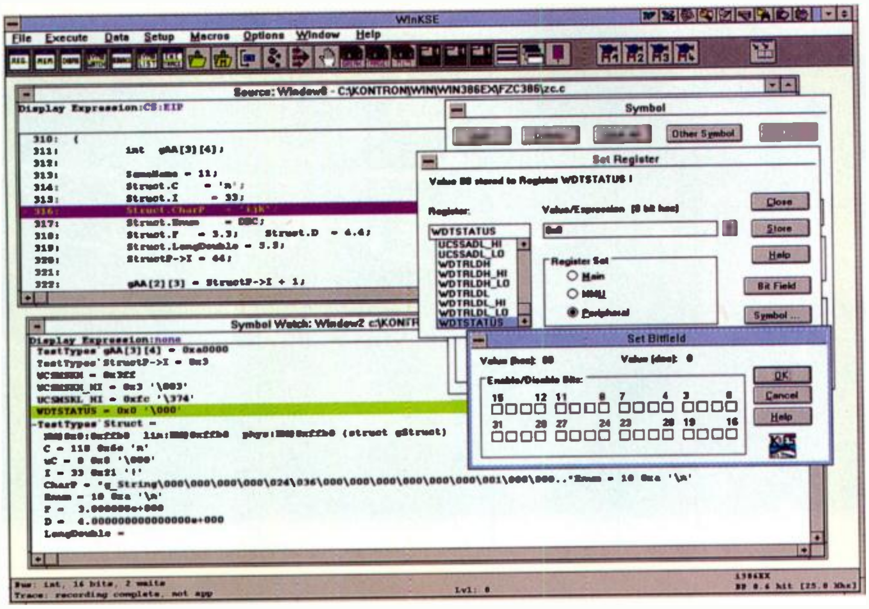


2. BOND-OUT TECHNOLOGY *maximizes an emulator's visibility into and control of the target CPU. Among the features of a modern emulator are a source level debugger and the ability to view and modify main, peripheral and MMU registers.*

the CPU has the right time relationship with the execution flow and with events in other parts of the target system.

Normally, an in-circuit emulator is the tool used to reveal exactly what is happening in the CPU to make sure the real-time requirements are met. In contrast, a software simulator is less likely to be used to debug real-time applications, since it does not operate in real time and would be hard-pressed to discern the critical timing relations.

Ideally, a designer wants to look inside the exact same processor that will power the production system and see it precisely the same way it will run in the production system. Another requirement is to be able to start and stop execution, and possibly change the contents of the CPU's internal registers if needed, without introducing any unwanted effects. The facts of quantum physics notwithstanding, whatever the designer does to observe the processor should not have any influence on the action being observed.

Unfortunately, the complexity of today's embedded CPUs precludes access to all internal activity from the chip's standard package pins. For example, registers, pipelines, and cache memory within the chip are not directly accessible through a processor's normal package pins.

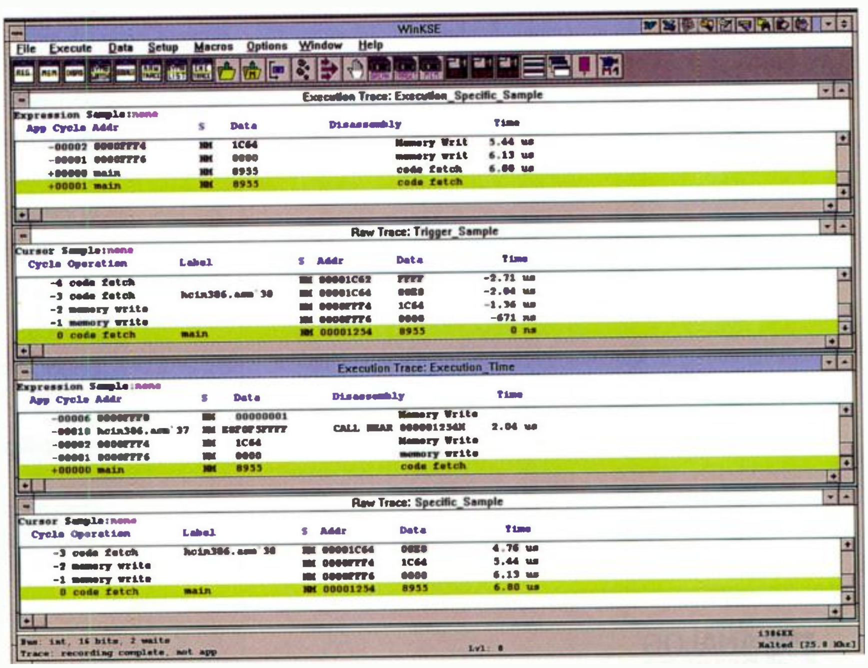
By using a CPU with bond-out technology, however, an emulator can asynchronously trap the processor contents at any time, and can do this whether the processor is operating in real, protected, or virtual modes. But using any emulator that wields bond-out technology is not enough. For real-time development, an emulator that takes advantage of bond-out technology must pass two key tests: First, it must use no system resources, such as memory or interrupts. Secondly, it must not affect the real-time behavior of the system. (Unfortunately, one CPU function that bond-out technology cannot reveal as it occurs is in the on-chip cache. Cache operations happen too quickly to extract a real-time, high-level language trace of their execution. Instead, these operations must be reconstructed after the fact.)

To avoid skewed measurements, the power supply and signal loading characteristics must duplicate that of the final system. To meet the requirements for real-time development, many emulators have a probe that plugs directly into the socket on the target system and draws only the power needed for the emulation chip. In contrast, some emulators will draw their full power from the target system, subtly changing the target system's characteristics.

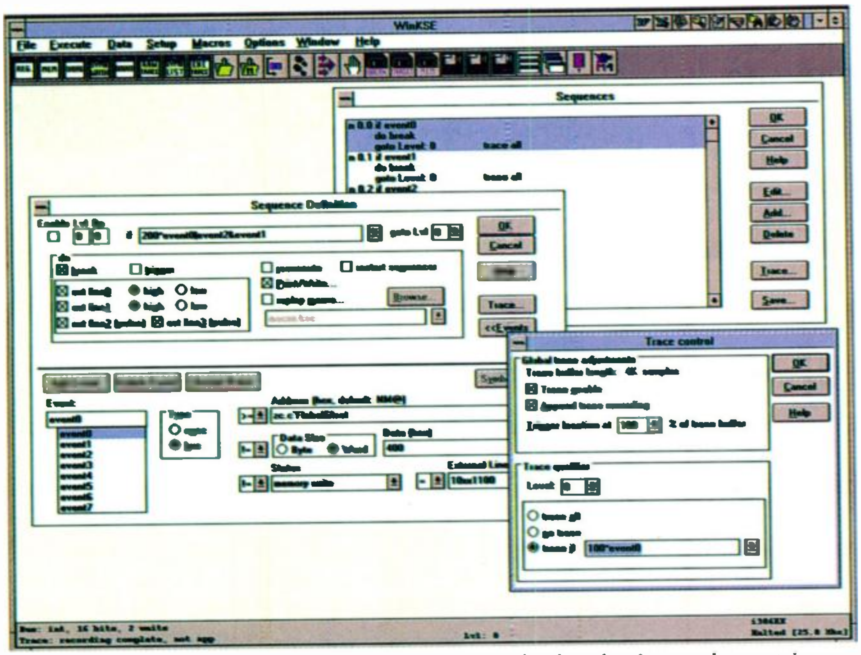
Other measures for closely emulating an actual target CPU include having the emulation probe plug directly into the CPU's socket, and putting the emulator's trace and overlay buffer memory directly on the probe head. These steps minimize the signal delays introduced by the emulator. In cases where the CPU is soldered to a board, an adapter can clip onto the CPU and put the chip's signal pins into a high-impedance state. But because of the extra distance that signals must travel through the clip-on adapter, this approach can add unwanted signal delays.

NO LOADING

To examine program status during emulation, it is often necessary to alter normal execution by using breakpoints, single-stepping through program execution, or issuing a user command to halt execution. A number of emulators halt execution by using the processor's nonmaskable interrupt



3. IN CPUs WITH PREFETCH *pipelines, it is important to trigger on, time-stamp and view trace buffers in both bus cycle ("raw") and execution formats.*



4. AN EMULATOR SHOULD *be able to set complex breakpoints and trace triggers according to events within the processor and the target system as a whole, as well as with sequence counters and counter timers.*

(NMI). When that happens in the real mode, the CPU pushes some of its registers onto the stack, reads the interrupt vector's corresponding jump address, and then jumps to the NMI service routine.

But this relatively simple process uses a CPU interrupt that becomes unavailable to the target system during development. By drawing on the processor's resources, in this case the NMI and whatever memory is allocated for the service routine, the emulator can introduce problems when running a real-time application. For example, a real-time application that calls on the NMI to initiate a procedure can crash if it is preempted by the emulator's own use of the interrupt.

In addition, the memory used by the emulator to store the NMI routine could be inadvertently activated by some normal read or write operation, such as when the application program performs a memory test. Consequently, this simple scenario appropriates resources from the CPU (the interrupt) and from the target system (a portion of its memory).

Things get more complicated in the protected mode. There, an NMI vector access can go to any physical address in memory. These memory areas are kept track of in the interrupt descriptor table (IDT). The emulator has to know the base address of the IDT, and if that address changes, the designer can easily become confused. That's the danger in the protected mode, where the IDT base addresses can be different for each protected mode session. In this case, the emulator uses system resources in a way that cannot be easily detected without deeper insight into the processor's internal states.

For that reason, some processors have a built-in emulation mode. In the emulation mode provided for Intel's X86 processors, for example, program execution can be halted at any point in real, protected, or virtual 8086 mode, even during a transition from one mode to another. This ability to halt execution makes the designer aware of changes to global descriptor table (GDT) base addresses. Coupled with bond-out technology, a high level of control becomes available without using any interrupt resources; resources that remain available to the target system.

Bond-out technology also lets an emulator directly read the contents of any protected mode registers. In this way, it eliminates the need to search through reserved area of memory to locate the registers, an operation that would disrupt the target system's normal program flow. Even the registers needed to calculate those elusive protected mode addresses, including the hidden segment descriptor register, are directly visible. In fact, bond-out technology offers yet another advantage when working with the I486: It lets a designer single-step through the user program, even when the portions of interest are entirely contained in the on-chip cache.

REAL-TIME BEHAVIOR

It is important to understand that a bond-out chip is effectively the same piece of silicon as the standard commercial product. The bond-out chip is built using the same base silicon as that for the production system. It has extra wires bonded to pins, giving access to internal states and control of execution.

This is especially important when dealing with timing issues. To detect and characterize timing problems, the designer can't just freeze execution and look at the internal states. He or she must trigger on selected conditions and record trace data. It does not suffice to set a breakpoint and then single-step through the program. Instead, events must be set that can trigger a trace without altering the timing relationships of execution. Bond-out technology provides the connections that can tell the emulator to assert a hardware breakpoint and trigger a trace.

In fact, real-time development demands two types of hardware events—bus events and execution events *(Fig. 3)*. For bus events, the normal external pins will suffice. The emulator monitors address, data, and status pins and detects the respective event defined in the emulation session. In addition to monitoring the microprocessor itself, the emulator also should have provisions (extra test leads) for monitoring other target system signals *(Fig. 4)*. In processors with a prefetch pipeline, a fetched instruction will appear on the bus that will be captured by a bus event detector. But something may occur that prevents that instruction from actually being executed. To determine that case requires the emulator to offer execution event detection. Triggering a trace solely on an instruction fetch could cause the emulator to record a branch of execution that was not intended if something preempted that instruction. It's also important that event detection not violate real-time behavior. Without bond-out technology, debug registers and interrupt sevice routines must be used, as is the case with monitor debuggers. This violates normal program flow and also prevents detecting the nth occurrence of an event.

The combined ability to emulate the target processor without loading its resources and to accurately reproduce the target system's real-time behavior becomes especially important for interrupt-driven systems. If a system has many interrupts to juggle, there may be no easy way for the emulator to borrow one during development. As for memory, cost alone is one reason to avoid its use for emulation. ▪

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Bond-out technology helps to meet these goals. The program flow of interrupt-drive systems is almost impossible to predict, so a full picture of external activity, internal states, and changes to program flow is essential. In some cases, the designer may need to trigger a halt to execution based on one of those internal conditions, making the access granted by bond-out technology indispensable.

Unlike some bond-out processors, bond-out versions of the i486 processor give access to the on-chip cache so that the designer can single-step program execution while monitoring all the other internal states of the CPU. Moreover, derivatives of the SL Enhanced i486 include a system management mode (SMM) that simplifies the design of power conservation measures in portable systems. By using SMM, the processor can deactivate and reactivate peripherals, including monitors and disk drives, as well as place itself into a sleep mode that consumes about 1/20th of normal power.

Devising the optimal strategy for taking advantage of the SMM is an important aspect of development, especially for portable and hand-held systems, as well as for other embedded designs. SMM is accessed via a system management interrupt and provides bond-out technology to support emulation of SMM. Any emulator used for developing systems where power consumption is critical must be able to work with SMM and during phases where power consumption is set at a minimum.

As microprocessors grow more complex, there will be an increasing need for vendors of chips, compilers, and development tools to work more closely. Eventuall, a time will come when a part of the emulator technology will have to migrate from the instrument onto the processor itself. This will be made necessary by the same imperatives driving emulation today: A designer must know what's going on within the processor in terms of both states and time. When parts of an emulator indeed move onto the chip, bond-out technology will give way to what might then be called "bond-in" technology. ES

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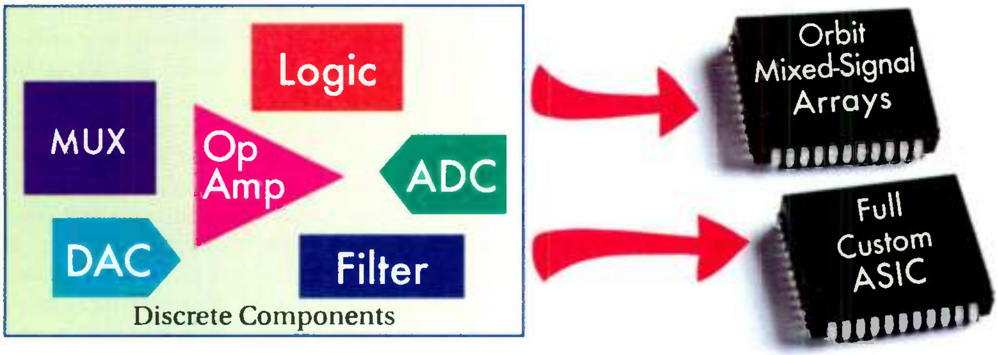

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Navin Govind

System Simulators Can Speed Time-To-Market

DESIGN PROTOTYPES CAN BE AN IMPORTANT AID TO DESIGN ENGINEERS IN MEETING THEIR TIME-TO-MARKET GOALS. IN PARTICULAR, PROTOTYPES CAN BE OF GREAT USE IN GENERATING OPTIMIZED REAL-TIME APPLICATION code with the shortest development cycle. But in the early stages of design and development, physical prototypes are usually not available. In such instances, software simulation of the prototype model early in the design cycle can make the difference in meeting time-to-market goals. System simulation using high-level languages opens the door to system emulation and the selection of the rest of the tools within the tool chain, including a real-time operating system, compilers, assemblers, and debuggers for various projects.

While the concept of using a system or architectural simulator has been around a few years, system designers have not taken full advantage of it as a design resource, particularly when compared to the widespread use of logic or circuit simulation. A key to successful system simulation are the accurate high-level, bus-functional models now available for co-development environments. These models are device models with complete timing accuracy. Tying the bus model interface to a system simulator facilitates software/hardware co-simulation and system validation. A system development environment is shown at a block diagram level *(Fig. 1)*. The system architecture is defined at a hierarchical level, beginning with the bus-functional model to the final system integration.

MODELING

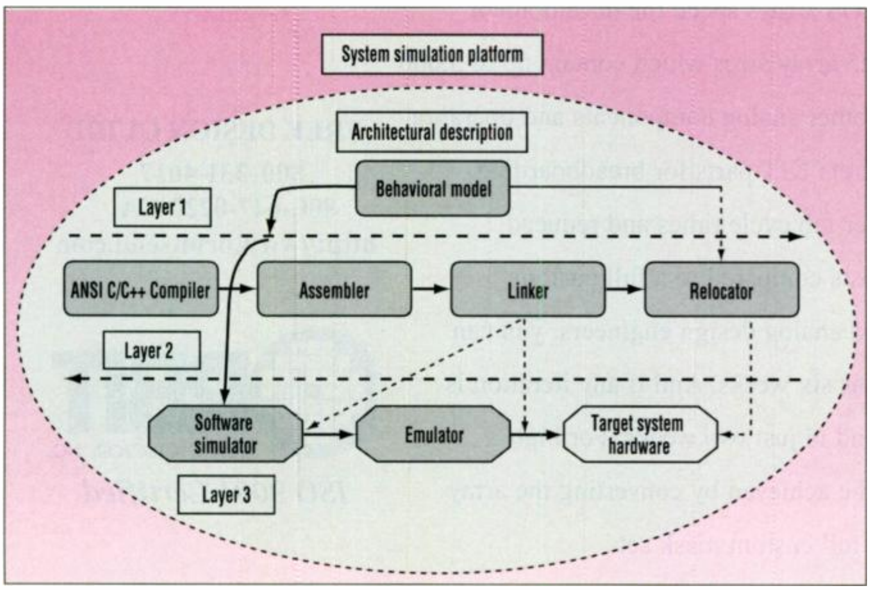
Behavioral modeling can be implemented at a high level to validate the design. When using a behavioral model, results are monitored through interactive graphical user interface (GUI) tools such as debuggers that allow the editing of variables, terms, and rule blocks for fine tuning. Model simulation directly affects the design and development time, as well as verification of a system. For example, complex systems can be analyzed for variable critical margins and system thresholds that would render a system unstable or unrealizable in the final stages of the development cycle. In a simulation environment, blocks in a GUI editor are visually displayed and edited in a well-defined format. Using graphical interface editors, the input and outputs of a system can be manipulated for defining function types, and output shapes are then outputted to the simulation block for validation.

Despite its advantages, modeling suffered from serious shortcomings. First, it required a time-consuming and complex process of identifying system parameters and dynamics. And as most designers know, real-life embedded systems can interact with more complex systems. In these cases, generic floating point-based behavioral modeling, although useful for algorithm validation, are rarely sufficient. But due to its complexity, hardware and software simulation have been insufficient. So it's not surprising that a demand for effective and sophisticated commercial modeling tools emerged. These tools are becoming popular worldwide, even though most designs are still hand-stitched, and problems are discovered during integration, with the only option being a redesign.

The designer's ability to use off-the-shelf real-time operating systems has been particularly problematic. Significant advances have been made in the area of real-time kernels, with a variety of architecture-specific, highly optimized, user-configurable kernels available. Some come integrated with feature-rich native development environments, GUI interfaces, configuration control, network management and Internet access facilities, all tuned to make the software development and system debugging easier and more efficient. Unfortunately, many major developers in the embedded world still do not use these integrated development tools because they believe they do not deliver accurate modeling, simulation, automatic code generation, and hardware/software emulation of systems running such microkernels.

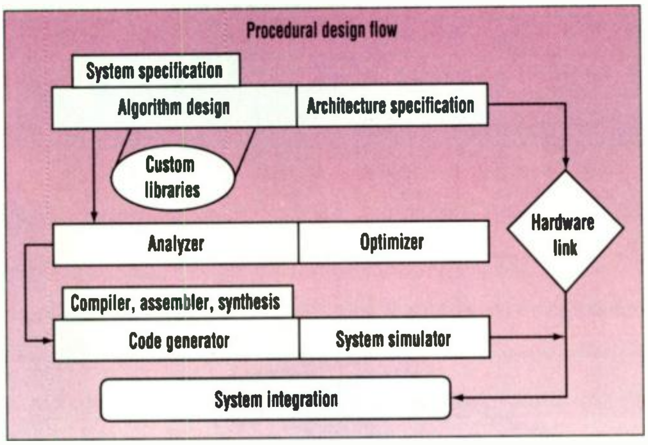
SYSTEM SIMULATORS

For a simple design such as an adaptive PID controller, time-to-market pressures can be eased if the system software integration is 90% complete before the hardware is targeted. This can be accomplished with a system simulator that allows system-level inte-



1. THIS BLOCK DIAGRAM *illustrates a typical system development environment. The architecture is defined at a hierarchical level beginning with the bus-functional model and ends at the final system integration.*

gration to be handled over the entire design cycle rather than just the back end. Desirable features in a system simulator include a completely or partially reconfigurable GUI that supports symbolic disassembly with multiple breakpoint and single-step execution. Support for a source-level, high-level language debugger such as C/C++ also is needed to complete the integration of various levels within the model being described. A usable system simulator also offers features such as easily understood design flow, performance, integrity, specification within industry standards, and support.



2. THIS TYPICAL SYSTEM SIMULATION MODEL *describes a procedural design flow. The choice of tools and the complexity of the system under consideration play a key role in the possible trading off of cost versus accuracy.*

System simulation depends on an accurate, complete system-level description that also requires that software, firmware, microcode, and hardware partitions be determined. For example, in the case of a closed-loop controller, the algorithm for error compensation can be simulated independently and its effect on the system response observed. The algorithm variables can then be individually tweaked for optimization. During debugging, a variable edit option can be used to specify the range, names, and data type of the variable within the simulation tool in floating-point or integer-type resolution.

While implementing a complex control system, a limitation in defining the variables is the degree of scalability the tool supports during code conversions. Standard practice usually dictates that variables be set to a limit within 10% by observation and are defined as integers that can be represented between 0 to 255 for computation. Values of coefficients and variables are chosen so that excessive undershoot and overshoot due to control are minimized. Values can be chosen by observing the change in the control surface plot and designing for a required system gain and zero overshoot.

CODE GENERATION

In the simulator environment, ANSI C code for computation and I/O handling is generated with 16-bit resolution using a GUI tool. Assembly-language code generation using the GUI is an option if the code is required to be compact and fast. In the optimization stage, off-line optimization allows system performance analysis using model simulation, while on-line optimization allows process hardware to be connected to the host system and optimization of the controller performance during run time. When simulation of a control loop is initialized, the simulation fills in input values to the system, invokes the computation of the output values, and outputs the result of the inference simulation. Single control cycles are executed and the changes in inputs and outputs can be observed, which helps to define a real-world control strategy.

Changes in the simulation environment and determination of the controller response through observation and redundancy allows for fine tuning of the controller. Simulations tend to be approximations of actual system behavior. Appropriate optimization of the embedded system is done on-line, taking feedback into consideration. On-line optimization can be realized in real-time mode and enables a system to be visualized and modified in real time while the process is running. The generated code from the GUI tools are recompiled without the on-line option, and integrated into the C196 hardware system in either ANSI C or assembly. The recompiled code compacts the code, since optimization features are enabled during recompilation. Superior simulator performance is attributed to the higher level of abstraction in describing the model and using accurate and procedural modeling techniques.

Since some controllers are prone to immunity from noise and system parameter variations, simulation tends to be ignored during the design and implementation stages. Simulation speed often is a topic of debate. While logic and circuit simulators tend to be time-consuming, a C/C++ language-based simulator will run faster than EDA-based simulators. This means that a fast PC could run a simulation model quickly and effectively.

When rigid design methods are followed, repeated simulation runs must be observed to accurately predict the performance pattern. Problems occurring due to pure time delay can be reduced by including a model that predicts the future output of the system in general. Repeated simulation runs predict the performance and behavior patterns of the system under development and establish observable parameters for stability analysis.

A generic simulator can be used for simulations for similar designs. The compatibility of the tools and the design being implemented must be verified before the tool can be reused. The flexibility of using one set of tools for compatible multiple designs ensures maintaining previous designs, and also speeds up the design cycle.

SYSTEM EMULATION

The next step after system simulation is system emulation to verify software and hardware co-design. This allows system verification long before the hardware is ready for implementation. Software emulation of a target system helps system designers to select the right algorithm for optimization and fine tuning as well as in choosing the right set of tools. The idea of reuse lies within the design and simulation environment. Once the system model is created and verified, it would be possible in most cases to eliminate compatibility issues and a similar simulation platform used on derivative projects.

A visual description of procedural design flow for a system simulation model is shown *(Fig. 2)*. Cost-versus-accuracy trade-offs depend on the choice of tools and the complexity of the system. For a design based on derivatives, the trade-offs are minimal. Debugging at the system level provides a process for discovering and correcting design and integration problems early and accelerates time-to-market by weeks or months. Simulation and model verification should be a necessity rather than an option. The parameter selection and code generation process using the right set of tools determines the robustness and efficiency of the controller-based design. By using a complete ensemble of visual graphical tools, a successful embedded system can be implemented and verified in a short design time-frame.

The advanced concepts of system modeling, simulation, automated design and validation are all well understood. Translating them into practical tools, however, has been difficult. But it has been changing recently. An example of the new approach is the joint effort of Intel Corp., Chandler, Ariz., and Integrated Systems Inc., Sunnyvale, Calif. They have ported ISI's MatrixX tool chain to Intel's MCS(R) microcontrollers. MATRIXs is a full-featured environment for system modeling and visualization, automatic code generation (ANSI C and Ada), virtual and real-time hardware simulation, and automatic documentation. The growing system complexity and availability of tools such as real-time microkernels, combined with the trend toward expensive, long turnaround, custom components, is tipping the scales in favor of automated modeling, design and simulation tools. ES

Navin Govind is a Senior Engineer in the Semiconductor Products Group Division at Intel Corp., Chandler, Ariz. He has participated in the design and development of the MCS 96 architecture and technical marketing of next generation high-performance microcontrollers. He is currently involved in the definition and support of embedded development tools for the MCS 96 families. He has written and presented papers on fuzzy logic in embedded control and simulation techniques, digital signal processing, and system model simulation.

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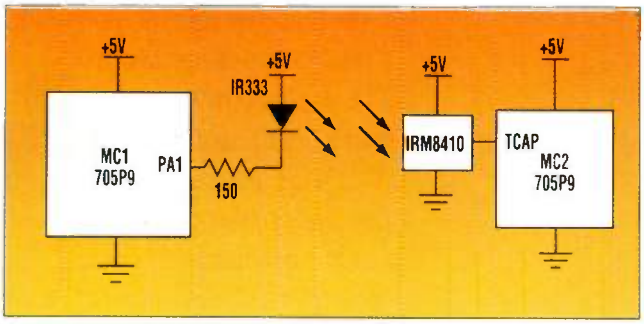
Microcontroller Interface With Infrared

ABEL RAYNUS / *Armatron, 2 Main St., Melrose, MA 02176.*

The circuit diagram shows the IR link for wireless data transmission between two 68HC705P9 microcontrollers (MC1 to MC2). To implement asynchronous communication, MC1 generates three types of output AM signals: start burst, logic0 burst, and logic1 burst. Each type is distinguished by its width, and each burst is separated by a small delay.



TWO MICROCONTROLLERS *can communicate via an IR link with the transmitter and receiver software shown here.*

These signals activate an IR Emitting Diode (IR333), whose bursts of IR light are transformed by the receiver module (IRM8410) into pulses at the TCAP input of MC2. After getting the start pulse, the MC2 software begins logic0 and logic1 pulse-width recognition and the receiver word register begins to fill up. The most important and interesting part of the idea is the communication software.

A software fragment for the transmitter to send an 8-bit word is shown in Listing 1, below. The word of data to be sent is kept in register "reg."

The program starts by sending a "start burst." After that, the program looks through each bit of "reg," starting from the LSB, and generates log1 or log0 bursts, if the bit is a 1 or a 0.

The receiver software fragment is shown in Listing 2. The easiest way to measure the pulse width is to use the input-capture function of the microcontroller timer. Both High and Low bytes of the input capture register are used for more

```
* LISTING 1 ( TRANSMITTER))

*  REGISTERS and VARIABLES:
prtA   equ    $00
ddrA   equ    $04
REG    equ    $81
num    equ    $82     ;output signal register
s      equ    $83     ;bit test number
* INITIALIZATION:
       lda    $ff     :prtA as output
       sta    ddrA
............................................
* WORD GENERATING SUBROUTINE
............................................
word   lda    #$33    ;start burst
       sta    s
       jsr    burst
..................
       lda    #$01
       sta    num
w1     lda    REG
       and    num
       beq    w2
..................
       lda    #$48    ;log1 burst
       sta    s
       jsr    burst
..................
w3     clc            ;0 ->C-carry bit
       lsl    num     ;go to next bit
       bcc    w1      ;is it NOT a last bit?
       bra    w4
..................
w2     lda    #$1f    ;log0 burst
       sta    s
       jsr    burst
       bra    w3
..................
w4     rts            ;return from word
................................
burst  bset   l,prtA  ;40 kHz AM pulse
       dec    s
       dec    s
       inc    s
       inc    s
       bclr   1,prtA
       dec    s
       dec    s
       inc    s
       nop
       bne    burst
..........................
       lda    #S7f    ;Delay 0.64ms
rep    decA
       nop
       nop
       bne    rep
       nop
       rts            ;return from Burst
..................................

*   LISTING 2  (RECEIVER)

* VARIABLES
tlH    equ    $80
tlL    equ    $81
t2H    equ    $82
t2L    equ    $83
tH     equ    $84
tL     equ    $85
num    equ    $86     ;register to form word
reg    equ    $87     ;temporary word register.
word   equ    $88     ;final received word register.
flag   equ    $89     ;0=WF (word flag)
mem    equ    $8a     ;temprorary memory register
* REGISTERS
tcr    equ    $12
tsr    equ    $13
icpH   equ    $14
icpL   equ    $15
* INITIALIZATION
       org    $100
init   bset   1,tcr   ;set positive edge TCAP
       clrx           ;clear memory locations
m0     clr    $80,x   ;from $80 to $8a
       incx
       cpx    #$0b
       blo    m0
..................
WORD FORMING PROGRAM
..................
start  brclr  7,tsr,start
       brset  1,tcr,i1   ;IEDG=1?
       lda    icpH
       sta    t2H
       lda    icpL
       sta    t2L
       bset   1,tcr   ;1 ->IEDG
..........
       lda    t2L
       sub    t1L
       sta    tL
       lda    t2H
       sbc    t1H
       sta    tH
..................
       brclr  0,flag,i2  ;WF=0?
       lda    tH
       cmp    #1      ;tH=1?
       beq    bit0
       cmp    #3      ;tH=3?
       beq    bit1
       bclr   0,flag  ;0-> WF
ires   lda    tsr     ;ICF reset
       lda    icpL
       jmp    start
..................................
i1     lda    icpH
       sta    t1H
       lda    icpL
       sta    t1L
       bclr   1,tcr   ; 0 -> IEDG
       bra    ires
..................................
i2     lda    tH
       cmp    #2      ;tH=2?
       bne    ires
..................................
       bset   0,flag  ;1 -> WF
       lda    #$fe    ;0 -> 0-bit num
       sta    num
       jmp    ires
..................................
bit0   lda    reg     ;put 0 into given reg. bit
       and    num     ;  while saving all
       sta    reg     ;  of the rest bits
       bra    i3
..................................
bit1   lda    num     ;put 1 into given reg. bit
       sta    mem     ; saving all of the
       and    reg     ;  rest of reg. bits
       com    mem
       eor    mem
       sta    reg
..................................
i3     sec            ;1 -> Carry bit
       rol    num     ;go to the next bit
       bcs    ires    ;is it NOT the last bit?
       bclr   0,flag  ;0 -> WF
       lda    reg
       sta    word    ;word is completed!
..................................
```

precise measurement. The starting pulse activates the program and sets the flag (WF=1). After that either logic "1" or "0" will be written one by one into register "reg," beginning from the LSB, depending on the corresponding pulse width.

Only when all 8 bits are completed does the flag drop off (WF=0); the contents of the "reg" is then finally rewritten into the register "Word."

This idea is applicable to any type of microcontroller and needs only one MC1 output pin and one MC2 input pin.

With the external IR components shown in the figure, the distance of reliable communication is about 20 ft.

To vote for this item as the "Best of Issue" in Software Ideas for Design, circle 621.

Program Code Splitting

ALEX EISEN / *State University of New York, Department of Physics, 239 Fronczak Hall, Buffalo, NY 14260.*

The object code created by an assembler for a 16-bit microprocessor consists of a sequence of 16-bit numbers, represented by four ASCII-coded hexadecimal digits, which are transmitted to an EPROM programmer through the serial port. In many cases, however, the code must be downloaded through a single-chip 8-bit programmer. For Motorola S1-9 format, each line of code starts with a header, following with a string length, an address, the body of the object code itself, and finally a checksum to verify the correctness of data transmission.

The purpose of the following program, written in C, is to split the original machine code file into two files—"even-" and "odd-"byte sequences—for downloading into two separate 8-bit EPROM chips.

This program recognizes the S1-9 Motorola format, breaks each line of the original object code into two by separating even and odd bytes and sending them to two different files—"evenwr" and "oddwr"—and calculates and appends a new checksum for each line.

The program thus allows the designer to overcome the limitations of the programmer.

The *hexasc( )* subroutine converts hex digits into an ASCII string, following with a EOS—end of string—while the *aschex( )* subroutine performs conversion of an ASCII string into hex digits, and *chksum( )* calculates the new checksum value.

```
 SPLIT . C
 #include <stdio.h>
 #include <stdlib.h>
 #include <string.h>
 #define EOS '\0'
 char start[40], number[30], addr[20], even[20],
odd[20]:
 char *s, *n, *a, *e, *o;
 char *hexasc(int x, int n)
 {
     char a[10];
     int i,z;
     for(i-n; i>=0;i--){ z=x&0xf;
if((z<=9)&&(z>=0))
     a[i]=z+48; else a[i] =z+55; x>>=4;}
a[n+l]=EOS;
     return(a);
 }
 aschex(char *q )
 {
     char temp[2], *t;
     int n=0;
     t=temp;
     do{ if (*q>='A') *t=*q-55; else *t=*q-48;
         n=n*10+(*t); q++; t++;} while(*q);
     return(n);
 }
 chksum (char *q)
 {
     int i,sum=0;
     char v[2];
     do{ for(i=0;i<2;i++){v[i]=*q; q++;} v[2]=EOS;
       sum=sum+aschex(v);} while(*q) sum=(-
sum&0xff);
     return(sum);
 }
 main ( int argc, char *argv [])
 {
     char buf [80], *b, *q;
     int num, k, l=0, numread=0
     FILE *fp, *fe, *fo;
     if(argc!=2){printf("usage: split filename\n-
");exit(1);}
     if((fp=fopen(argv[1], "rb" )) ==NULL)
         printf("cannot open file\n";exit(1);}
     s=start; b=buf; a=addr; n=number; e=even;
o=odd;
     do{ fseek(fp,numread,SEEK_SET);
         fgets(buf,sizeof(buf),fp);
         *s=*b; *(s+1) =*(b+1); *(s+2)=EOS;
         if(*s!='S') { printf("not Motorola code\n"):
break;}
         if !strcmp(s,"S8") | | !strcmp(s,"S9") | |
!strcmp(s,"S7"))
         { k=10-aschex(s+1);} else
k=aschex(s+1);
         *n=*(b+2); *(n+l)=*(b+3); *(n+2)=EOS;
         for (i=0; i<2; i++) { * (a+i)=*(b+4+i);}
         num=aschex(n)-k-2;
         for(i=0; i<num; i++) { if(! (i%2)) {
             *(e+i)=*(b+2*(k+3)+4*(i/2));
             *(o+i)=*(b+2*(k+4)+4*(i/2)); } else {,
             *(e+i)=*(b+2*(k+3)=4*(i/2) +1);
             *(o+i)=*(b+2* (k+4) +4*(i/2 + 1);}}
         e[num]=EOS; o[num]=EOS;
num=num/2+k+2;
         q=hexasc(num,1); strcpy(n,q);
         q=hexasc (aschex (a)/2,(2* ( k+ 1) - 1));
strcpy(a,q);
         strcat(n,a); strcat(n,e); num=chksum(n);
         q=hexasc(num,1); strcat(n,q); strcat(s,n);
         fe=fopen("evenwr","a"); fprintf(fe,"%s\n",
s);
  fclose(fe);
         *s=*b; *(s+1)=*(b+1); *(s+2)=EOS;
         *n=*(b+2); *(n+1)=*(b+3); *(n+2)=EOS;
         for(i=0;i<2*(k+1); i++) {*(a+i)=*(b+4+i);}
         *(a+2*(k+1))=EOS; num=aschex(n)-k-2;
num=num/2+k+2;
         q=hexasc(num,1); strcpy(n,q):
         q=hexasc(aschex(a)/2,(2*(k+1)-1));
         strcpy(a,q); strcat(n,a); strcat(n,o);
         num=chksum(n); q=hexasc(num,1)
         strcat(n,q); strcat(s,n);
         fo=fopen("oddwr","a");
fprintf(fo,"%s\n",s); fclose(fo);
         numread=numread+strlen(buf); }
while(!feof(fp));
  }
```

To vote for this item as the "Best of Issue" in Software Ideas for Design, circle 622.

Enhanced Numeric Value Conversion

JOSEPH D'AIRO / *424 Higbie Lane, West Islip, NY 11795.*

Accepting numeric input can be troublesome in languages such as Qbasic and related dialects because their input routines require strict compliance with formatting requirements.

For example, numbers such as "1,000" and "$125" will be misinterpreted because of the illegal comma and the dollar sign.

This will be a problem not only when a user forgets the formatting rules, but also when data is read in from a preexisting file such as a database.

There are two steps to overcoming this problem. The first step is to accept the input as a string—and not as a number. The string input routines will allow the non-numeric characters to be *from the* **root of your ideas towering** *products* **grow**

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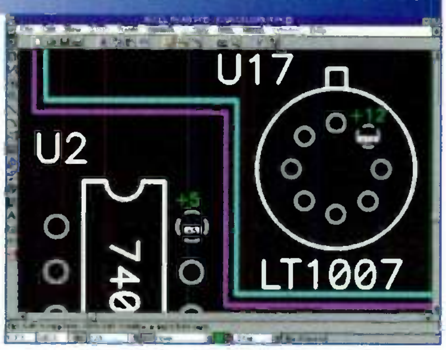

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```
LISTING 1:
THE XVAL() FUNCTION AND DECLARATION IN MAIN ROUTINE

DECLARE FUNCTION xval# (numstr$)

'
'The main routine goes here
'
END

FUNCTION xval# (numstr$)

'Removes all characters that do not appear in
'the list of valid characters
      'Step through the input string
FOR i = 1 TO LEN(numstr$)

      'If the individual character appears in the
      'list, copy it to the end of the output string

IF INSTR("0123456789.-", MIDS (numstrS, i, 1)) THEN
      a$ = a$ + MID$(numstrS, i, 1)

END IF
NEXT i

      'Convert the output string to a number,
      'and return it as the value of the function.
xval# = VAL(a$)
END FUNCTION
```

```
LISTING 2:
DEMO OF THE XVAL() FUNCTION

DECLARE FUNCTION xval# (numstr$)

'
'DEMO ROUTINE
'

CLS

DO

      'Input numbers as strings
PRINT
LINE INPUT "Enter a number (type 'end' to quit) ";b$

      'Quit when 'end' is typed instead of a number
IF b$ = "end" THEN EXIT DO

      'Compare the results of the functions
PRINT  "The VAL function returns: "; VAL(b$)
PRINT  "THE xval function returns: "; xval#(b$)

LOOP

END
```

entered. The second step is to convert the string to a number for further use in the program. There is a built-in function in most BASICs named VAL () which will convert numeric strings into numbers.

Unfortunately, the built-in function will only convert a string until it encounters an illegal character, so "1,000" will convert to 1 and the comma and anything past that point will be ignored. Similarly, "$125" will convert to zero, since the first character, the dollar sign, is illegal and it will be ignored along with all of the remaining characters.

The solution to this problem is a function which will strip out the illegal characters, and then convert the remaining numeric characters to a number. Since this function is an extended version of VAL(), it has been named XVAL().

Listing 1, shown above, shows the XVAL () function. The first statement names the function and lists its parameter, a string variable, as required by the Qbasic interpreter. The function name ends with a "#" to declare it as double-precision.

A FOR loop is set up to step through the numeric input string *numstr$*. The index, *i*, is incremented from 1 to the length of *numstr$* as determined by the LEN () function, so each character is examined in turn.

The INSTR() function compares two strings and returns a non-zero value if the second string appears in the first. In this case, the first string is a reference string of valid characters, composed of the digits 0 through 9, the decimal point, and the minus sign. The second string is one character extracted from *numstr$* at the index point via the MID$ () function.

If the indexed character appears in the reference string, the INSTR() function returns a non-zero value to the IF statement, which is interpreted as TRUE, causing the THEN clause to be executed.

The THEN clause is an assignment statement which adds the indexed character to the end of string *a$*. Conversely, if the indexed character does not appear in the reference string, it is not added to *a$*. In this way, only the valid characters appearing in *numstr$* are copied to *a$*.

Once all the characters appearing in *numstr$* have been processed through the FOR loop, string *a$* contains a copy of *numstr$* less any invalid characters.

The VAL() function is used to convert the valid numeric string representation in *a$* into a number and the result is assigned to XVAL# to be returned as the result of the function.

A program to demonstrate the difference in action between VAL() and XVAL() is shown in Listing 2.

An on-screen prompt asks for a number to be input, then both the VAL() and XMAL() results are printed. Try entries such as "1,234.45", "U101", and "$123" to see the difference.

The LINE INPUT command is used to read the keyboard since it will accept all characters up to a carriage return, while the INPUT command would be confused by commas. Try changing this to see what happens.

Note that the reference string used does not include the BASIC characters for exponential or hexadecimal notation, so those characters will be stripped from the input. They can be included by adding "eEdD" and "&hH" to the reference string, respectively.

To vote for this item as the "Best of Issue" in Software Ideas for Design, circle 623.

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TOOL CREATES 3D MULTIMEDIA TITLES

Hyperwire from the Kinetix division of Autodesk, Inc., is a visual authoring tool for creating 2D and 3D World Wide Web titles in Sun Microsystems' Java environment. The tool allows Web content authors to build multimedia titles that can include works created with Kinetix's 3-D Studio MAX and other VRML-compliant tools. Applications developed with Hyperwire can enhance the Web by augmenting real-world titles with 3-D capabilities. Hyperwire creates applications in Java, the popular programming language for the Internet, and supports the VRML (virtual reality modeling language) 3D Web standard. Titles can be played on platforms running Microsoft Windows 95 and NT, Apple Macintosh, and Unix operating systems. The extensible Hyperwire architecture accepts third-party plug-in applications for expanded features and capabilities. Using Hyperwire, designers and programmers can create richer web sites with interactive games, financial analysis applications, sales demos, advertising, and interactive learning. A free preview version of Hyperwire is available on the Kinetix web site at http://www.ktx.com. Shipping and pricing information will be available later this year.

Reccommended development configurations include a Pentium class PC or compatible system running Microsoft Windows or Windows NT, 16 Mbytes of memory, 20 Mbytes of free disk space, and an 8-bit, 640-by-480-pixel resolution color display.

***Kinetix**, 111 McInnis Pkwy., San Rafael, CA 94903; (415) 507-5000.*

CIRCLE 560

AUTOMATED SOFTWARE TESTING, MANAGEMENT

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***CenterLine Software, Inc.**, 10 Fawcett St., Cambridge, MA 02138-1110; (617) 498-3000; fax: (617) 868-6655; web site: http://www.centerline.com.*

CIRCLE 561

STATISTICS TOOLBOX AIDS ENGINEERS

Tightly integrated within the MATLAB technical computing environment of The MathWorks, Inc., the MATLAB Statistics Toolbox 2.0 is a set of tools for statistical algorithm development, analysis and modeling. Users involved in data analysis, modeling, and simulation can access over 200 statistics functions, including statistical methods for probability distributions, parameter estimation, multivariate statistics, linear and nonlinear modeling, statistical plotting, statistical process control, design of experiments, nonlinear regression, and principal components analysis. In addition, the toolbox provides custom statistical plots and a set of interactive graphical displays for point-and-click analysis, modeling and on-the-job learning of statistical concepts.

The MATLAB compiler and C math library can be used to automatically convert custom-developed statistics routines into C code. GUI tools help users understand and analyze system characteristics through illustrated statistical concepts. These interactive dis-

(continued on next page)

plays provide graphical and textual information that give insight into the characteristics of a specific process or dataset by visually showing the effect of changes. Each Statistics Toolbox function can be applied as is to solve specific problems, or can be used to design custom statistical algorithms. Also, users can integrate a statistical function with any program built using other MATLAB toolboxes, such as Neural Networks, Signal Processing, Image Processing, NAG, and Optimization toolboxes.

The Statistics Toolbox is available for leading desktop engineering platforms supporting MATLAB, including PCs, Macintosh, Unix, and VMS workstations. Pricing for PC and Macintosh computers start at $395. The product runs on MATLAB 4.2 or higher.

***The MathWorks, Inc.**, 24 Prime Park Way, Natick, MA 01760-1500; (508) 647-7000; fax: (508) 647-7001; e-mail: info@mathworks.com.; web site: http://www.mathworks.com.*

CIRCLE 562

ENHANCED TOOLS FOR RF/MICROWAVE DESIGN

MMICAD Version 2 is a set of Windows-based RF/microwave linear simulation software for the PC. The package operates with the Windows 95 and NT 32-bit multitasking operating systems as well as 16-bit Windows 3.1 and 3.11 versions. For MMICAD Version 2, new models have been added to the MMICAD library, including coplanar waveguide, microstrip, suspended substrate, stripline, ideal elements, and noise elements. Version 2 also offers expanded design aids covering capacitor, matching circuit, transmission element, resonator and filter designs.

The package comes with a CD implementation, on-line manuals, and application notes. The software can also be supplied in disk format. Version 2 works with any version of Windows on a 386 or later PC equipped with 8 Mbytes of memory.

The MMICAD Version 2 Suite supports schematic capture using either Protel Advanced Schematic 3 or OrCAD Schematic Capture. An integrated layout capability allows MMICAD to simulate the effect of changes on circuit performance. The layout module works with a variety of graphical file formats, including Gerber photoplot, Calma GDS II, Excellon NC drill, HPGL, DXF, postscript and others. The Version 2 Suite also has programs that offer nonlinear amplifier gain-compression measurements and small-signal modeling of MESFETs and HEMTs. The recommended platform for the Version 2 Suite is a 486 or later PC with 16 Mbytes of memory. Schematic capture, layout, filter synthesis and CAT modules are available separately or integrated with MMICAD in the Version 2 Suite.

***Optotek Ltd.**, 62 Steacie Dr., Kanata, Ontario, Canada K2K 2A9; (613) 591-0336 or 800-361-2911; fax: (613) 591-0584; e-mail: mmicad@optotek.com; web site; www.optotek.com.*

CIRCLE 563

MODULE PROCESSES DIGITAL AUDIO

Digital audio analysis, display, and processing is now available through a menu-driven environment provided by DADiSP/WAV, an add-on module to DADiSP from DSP Development Corp. Integrated with the DADiSP graphical spreadsheet for scientific and engineering data analysis, DADiSP/WAV allows digital audio data to be read, written and edited via pop-up menus or one-line functions. The module supports the standard PCM WAV file format for 8- and 16-bit mono, or stereo data. DADiSP/WAV lets the user call any Windows-compatible WAV player device and play WAV data on any WAV-compatible sound card. All source code is written in the DADiSP programming language (SPL), and variable definitions, and menus are supplied in ASCII text format so they can be customized by the user. DADiSP provides an intuitive icon- and menu-driven environment for data management and display, allowing users to work with data series of any length. The spreadsheet combines hundreds of built-in functions to perform graphical data analysis, mathematical and statistical analysis, data management, and FFT analysis. WAV files are typically digital audio files that conform to the Microsoft Windows WAV file format standard. A WAV file is a binary file consisting of a 44-byte header and its corresponding sound data.

The DADiSP/WAV module is priced at $495.00 each and is used with the DADiSP 4.0 Windows version ($1895.00).

***DSP Development Corp.**, One Kendall Square, Cambridge, MA 02139; (617)577-1133.*

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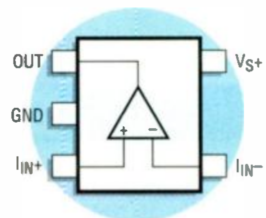

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READER SERVICE 111

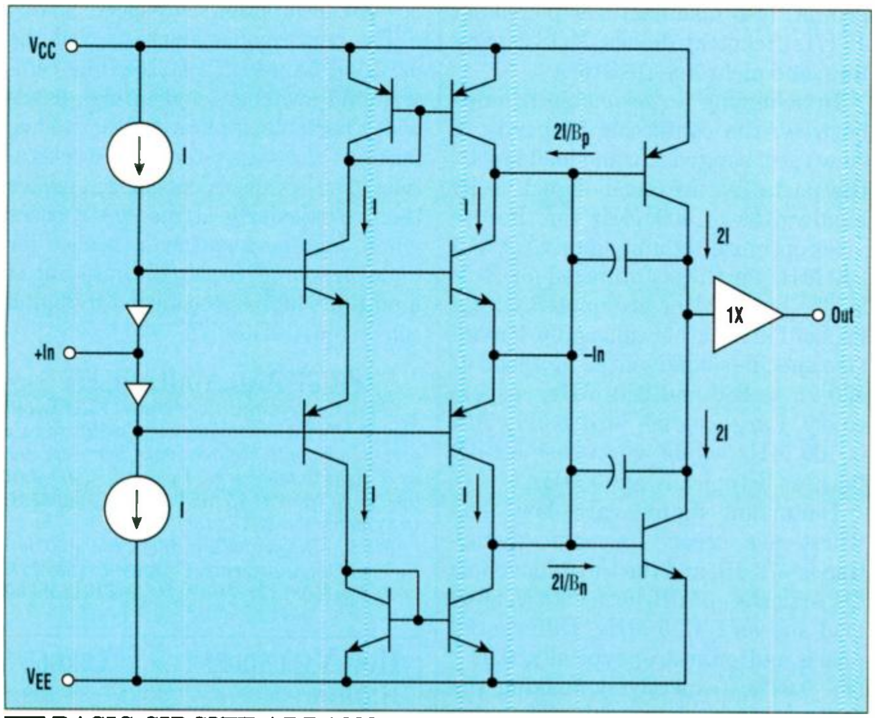
Amplifiers Attain 400-MHz Bandwidths

Current Savings For 1-mA Current-Feedback Amplifiers Could Be Extremely Significant For Multichannel Systems.

PAUL MCGOLDRICK

Using the next stage in the development of one of the fabrication processes acquired from their purchase of the Tektronix semiconductor operation (Beaverton, OR), Maxim has introduced a range of 1-mA current-feedback amplifiers that produce exemplary frequency responses. The MAX418X amplifiers are two-stage systems with biasing arrangements that avoid the problems of feedback systems. The differential-input and -output amplifiers are available in single, dual, and quad arrangements *(see the table)*. Each version has parts that are optimized for a gain (A_V) of either 1 or 2. The single amplifiers are available in the tiny, 6-pin SOT-23 or the 8-pin SO-8, while the duals are available in 8-pin µMAX/SO, or, if equipped with an auto-shutdown feature, 14-pin TSSOPs. The quads also are available in 14-pin TSSOPs.

The architecture of the amplifiers is such that the two stages are bias-related *(see the figure)*. The second stage is an open-loop stage, avoiding the bandwidth limitations and the inherent, potential instability of feedback at some frequencies. The added noise consequences associated with feedback also are eliminated. In order to control the bias of the second stage, a "replica" stage precedes it where the current loops of the second stage are adjusted to balance out impedances, base currents, and matching effects. The current drawn by the second stage is always twice that of the input. A patent is pending for the bias technology.



BASIC CIRCUIT ARRANGEMENT of the Maxim MAX418X series of 1-mA current-feedback amplifiers, with two stages, and a novel replica stage for biasing.

The high-frequency response of the process, together with high β values of 2400 to 2500, allows for very little peaking, or boost, on the output stage. The process used by Maxim is a derivation of the C-Pi process developed by Tektronix, and was acquired by Maxim with the purchase of the Tektronix foundry facilities in late 1993. Improvements in the CB-2 process are particularly noticeable in the pnp devices.

The CB-2 process is a single poly-emitter, recessed-oxide-isolated, high-speed complementary bipolar process. It features a 40-Ω-cm p-type substrate with buried layers (p-type in the pnp, n-type in the npn) and a silicon-dioxide trench between the collector and base. An active base is used under the emitter, and heavy gold metallization techniques are used. CB-2 is optimized for low-voltage applications up to 12 V, but higher-voltage layouts (up to 20 V) also are pos-

1-mA CURRENT-FEEDBACK AMPLIFIERS

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Part number	Number of amplifiers	Optimized for gain (A_V) of	3-dB small-signal bandwidth (MHz)*	Auto-shutdown mode	Package types
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MAX4181	1	1	400	No	SOT-23-6 or SO-8
MAX4182	2	2	340	No	NMAX180 (8-pin)
MAX4183	2	2	340	Yes	TSSOP (14-pin)
MAX4184	2	1	400	No	NMAX180 (8-pin)
MAX4185	2	1	400	Yes	TSSOP (14-pin)
MAX4186	4	2	340	No	TSSOP (14-pin)
MAX4187	4	1	400	No	TSSOP (14-pin)

* = R_L of 1 kΩ and a supply voltage of ±5 V.

sible. The process' LV_{ceo} is over 10.5V for the npn transistor, and greater than 8.0 V for the pnp transistor.

The CB-2's high-frequency performance is not as impressive as the Maxim's flagship GST-2 process, but is high enough for an enormous range of potential products, including this series (the MAX418X series) of products. The f_T for the npn transistor is 8.7 GHz at V_{ce} = 4 V, and 6.4 GHz for the pnp transistor. The maximum frequency (f_{max}) is 9.4 GHz for the npn transistor and 7.0 GHz for the pnp transistor. Betas are high and the process also manufactures p-channel JFETs, Schottky diodes, MOS capacitors, and nichrome resistors.

In achieving a reasonable balance between the conflicting demands of slew rate, bandwidth, and load levels, the parts feature small-signal, 3-dB bandwidths of 400 MHz for the devices optimized at unity gain (A_V), and 340 MHz for those optimized for A_V = 2. The bandwidths are quoted with a load of 1 kΩ. Rather unusually, Maxim also specifies bandwidths at a load of 150 Ω, as 280 and 240 MHz, respectively. Large-signal 3-dB bandwidth is 100 MHz, while worst-case 0.1-dB flatness is typically at 60 MHz.

Distortion figures are low. The worst-case second-harmonic distortion is –72 dB, and the third-harmonic distortion is –54 dB, both with a 150-Ω load and an f_c of 5 MHz. Differential phase and gain are, typically, 0.02° and 0.04%, respectively, making the parts eminently suitable for video work, while the noise-voltage density at the input is 2 nV/√Hz.

Rail voltages for the parts are normally ±5 V, but they can be operated with a single +5-V rail, with the bias set at mid-point to the rail. Because quiescent current drops with a single rail, there's about a 20% reduction in small-signal bandwidth. Some distortion figures worsen while others improve.

Headroom in the devices comes within 1 V of the supply rail(s), input capacitance is about 2 pF, while the typical output current that can be driven is ±30 mA. A 1200-V/µs slew rate and a settling time of 16 ns to within 0.1% completes the picture of these low-power-consumption high-speed parts.

The performance suggests that the parts will be used in portable video cameras and switchers and in high-bandwidth portable applications, as well as for CCD imaging systems and workstations. The low quiescent current makes them particularly attractive in cases where high performance is needed for multiple sources (e.g. in the buffering of inputs into high-speed analog-to-digital converters (ADCs). □

PRICE AND AVAILABILITY

The single-amplifier parts (MAX4180 and MAX4181) are available now. The duals and quads will become available over the next eight to ten weeks. Prices, in 1000-unit lots, vary from $1.75 for the MAX4180/4181, to $4.50 for the MAX4186/4187.

Maxim Integrated Products, Inc., 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600, fax (408) 737-7104. CIRCLE 500

HOW VALUABLE?	CIRCLE
HIGHLY	528
MODERATELY	529
SLIGHTLY	530

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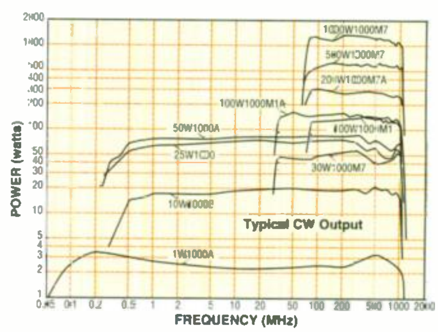

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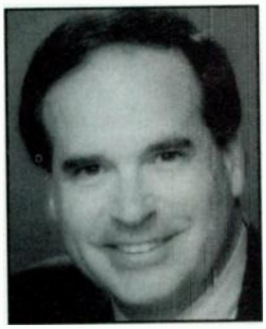

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Communications Solution Comes To Mass Storage

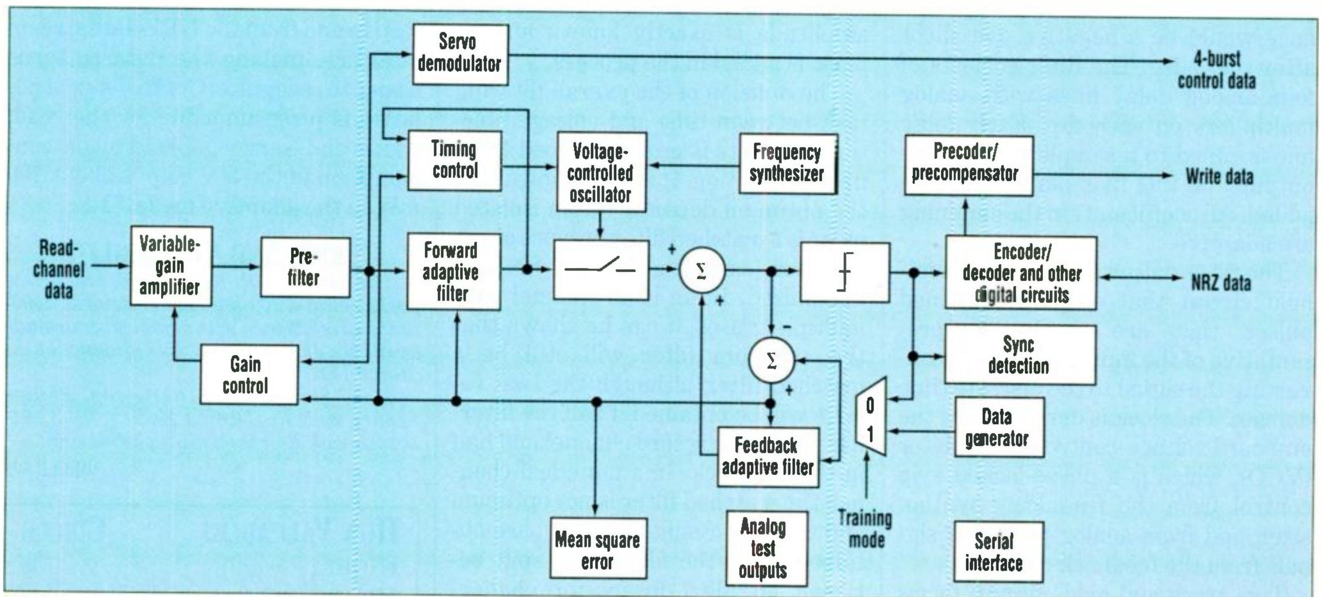
Decision-Feedback Equalization Increases Disk-Drive Capacity At The Same Signal-To-Noise Ratio.

PAUL MCGOLDRICK

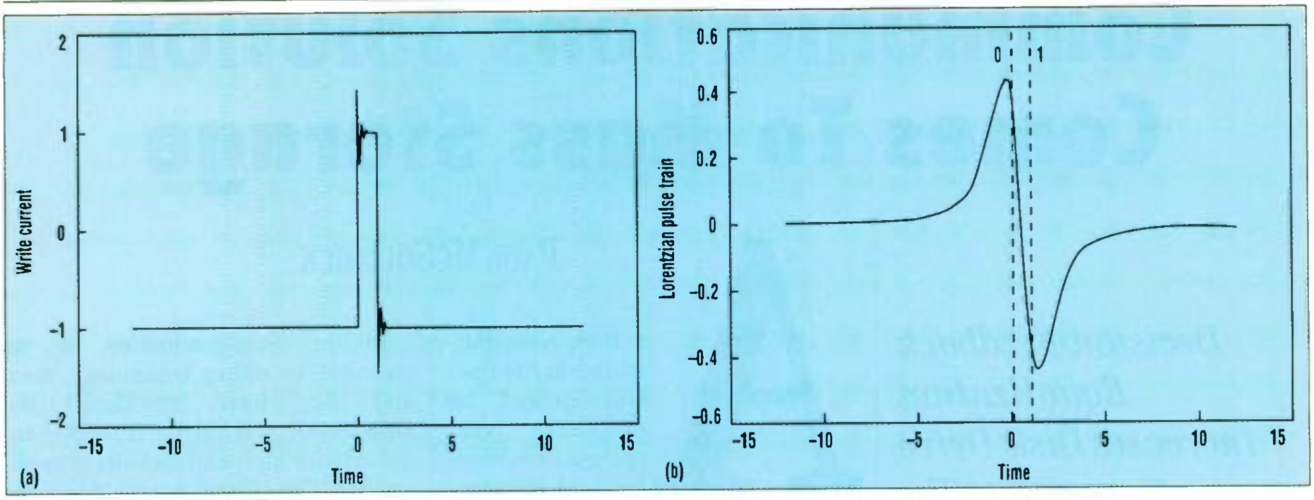
As Rich Nass intimated in his Special Report on disk-drive technology, decision-forward equalization (DFE) has the potential to become a dominant tool in the ability to increase the capacity of high-end disk drives over existing techniques (ELECTRONIC DESIGN, *Aug. 5, p.69*). It is expected to vie with extended partial-response, maximum likelihood (EPRML) techniques, and the figures being quoted range from a 15 to 30% increase in areal density over existing PRML channels with the same signal-to-noise ratio (SNR). Competition for solutions to get to market is intense, and it is almost inevitable that the most robust solutions will come from those that have both mass-storage technology and the company synergy to draw on the communications side of their business. Why? Because DFE implementation is a communications engineering solution to a data stream.

Philips Semiconductors is no stranger to either technology area, and they have introduced the DFE9955R, a RAM-DFE read-channel chip for high-end disk-drive applications. The IC will handle 64 to 240 Mbit/s data rates. It has a fully adaptive RAM-DFE core with an 8-cell analog RAM-based hybrid feedback filter and an analog delay line-based forward filter, both of which are based fully on continuously adaptive least-mean-square (LMS) algorithms. The purpose of the DFE channel is to reproduce the write-channel current waveform with its correct transitions at t = 0 and t = 1 as they are recorded *(Fig. 1a)*. This worst-case transition of a current reversal within the minimum time spacing is known as a "dibit." The reproduced signal on the read channel shows a voltage pulse wider than the write pulse and with considerable interference *(Fig. 1b)*.

DFE is a process for removing inter-symbol interference (ISI) from a signal to recover the original encoded



1. THE WRITE CURRENT and the resulting read voltages from a typical disk drive. The Lorentzian output is broader than the original and shows considerable interference.



2. BLOCK DIAGRAM OF the Philips DFE9955R decision-feedback equalizer aimed at high-end disk-drive applications.

data. The off-disk data (generically known as RDX and RDY), which are amplified by an embedded IC in the disk drive, are ac-coupled to the DFE chip. An analog variable-gain amplifier is controlled by two decision levels, one from the output of the pre-filter, and the second from the later feedback circuitry *(Fig. 2)*. The pre-filter removes obviously out-of-band signals.

The defining parts of a DFE system are the two sets of filters, forward and feedback, and their adaption algorithms. The forward filter is used for pulse shaping and phase minimization. The ISI before t = 0 is moved to after the digital event being recovered—that is, precursor ISI moves to become post-cursor ISI. If a single pulse was to be isolated, the appearance would be a negative overshoot after the pulse. The filter consists of four analog delay lines with analog multipliers on each tap. Each delay line is tuned to a sample period. The outputs of the five multipliers are added. All coefficients in the summing are adaptive.

The filter output feeds a track-and-hold circuit that outputs conjoined pulses that are amplitude-representative of the input, effectively converting the signal to the discrete time domain. The clock is derived from the on-board voltage-controlled oscillator (VCO), which is a phase-locked loop control from the frequency synthesizer, and from analog-produced signals from the feedback circuits.

The track-and-hold circuit forms one input to a summing junction (whose output is the fully corrected signal). The second input is from the feedback adaptive filter. The latter consists of a loop with slicer, shift register, and multipliers. The slicer is a threshold comparator and the input is subtracted from the output to provide the equalizer-error signal to the AGC loop. That signal also drives the time recovery/control circuit and, most importantly, drives the adaptation on the two filter-equalizers. The update process is driven by the mean square error and the coefficients are driven up to the point at which the signal-to-noise ratio is maximized.

As past decisions are clocked through the filter at the sampling rate, the filter output is used to cancel, in the summing junction, the ISI overshoot. Cancellation is precise since the amplitude is exactly known and no noise is added in the process.

The division of the overall filtering task between time and voltage function elements is crucial to good DFE implementation. It is well known that the optimum detector for an isolated pulse is a matched filter because at the detector, sampling instant SNR is maximized. In an ideal channel with multiple pulses, it can be shown that the optimum filter will still be a matched filter, although the best results will be obtained if half the filtering was in the record channel and half in the playback. In a non-ideal channel, the matched filter is not optimum and the best results, as here, are obtained when the filtering is spilt between an ideal filter—for channel noise—and a linear equalizer for minimizing ISI. The design of a linear equalizer for this purpose is usually a compromise unless there is a large SNR margin to work with.

The standard DFE is enhanced in the Philips process by adding non-linear cancellation of the ISI. This consists of an analog RAM (data generator) which will independently compensate for both positive- and negative-going pulses detected by the DFE. The coefficients for the multipliers are picked from a lookup table identified by the first three decisions. This facility improves the potential yield of single-stripe magnetoresistive (SSMR) heads that have large amounts of nonlinearity.

Additional features are the 4-burst servo demodulator and a 16- to 17-bit translation in the encoder-decoder feed to and from the NRZ data stream interface, making the data patterns easier to recognize. Control-signal polarity is programmable for the read, write and servo gates. Power consumption of the 5-V chip is about 700 mW in the adaptive mode. □

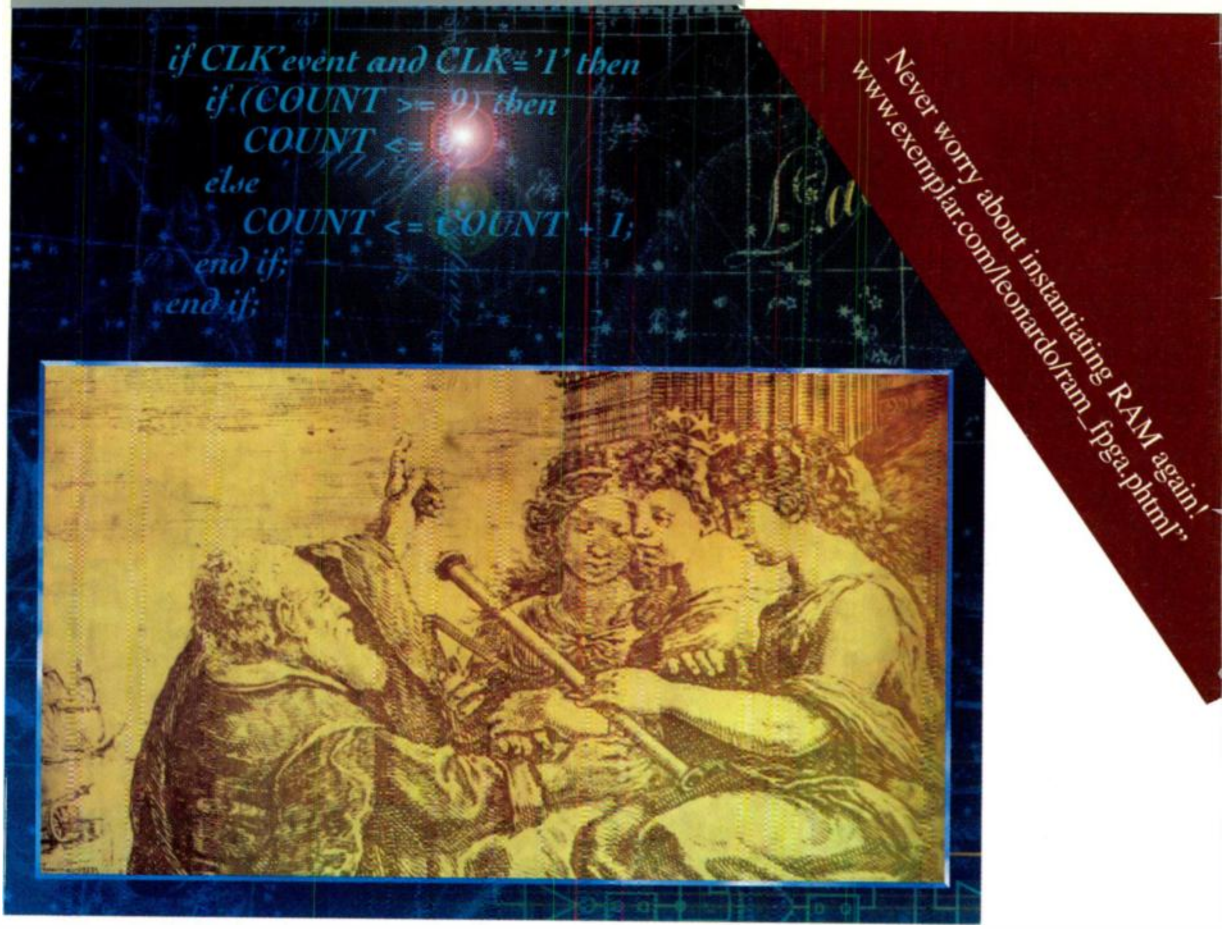
PRICE AND AVAILABILITY

The DFE9955R RAM-DFE product is packaged in a 100-pin LQFP. Price in 1000-unit lots is $25 each with samples being made available January 1997 and production in March 1997.

Mass Storage Products Group, Philips Semiconductors, Dennis Medley, (408) 991-4022; e-mail dmedley@SCS.philips.com.

CIRCLE 502

HOW VALUABLE?	CIRCLE
HIGHLY	546
MODERATELY	547
SLIGHTLY	548



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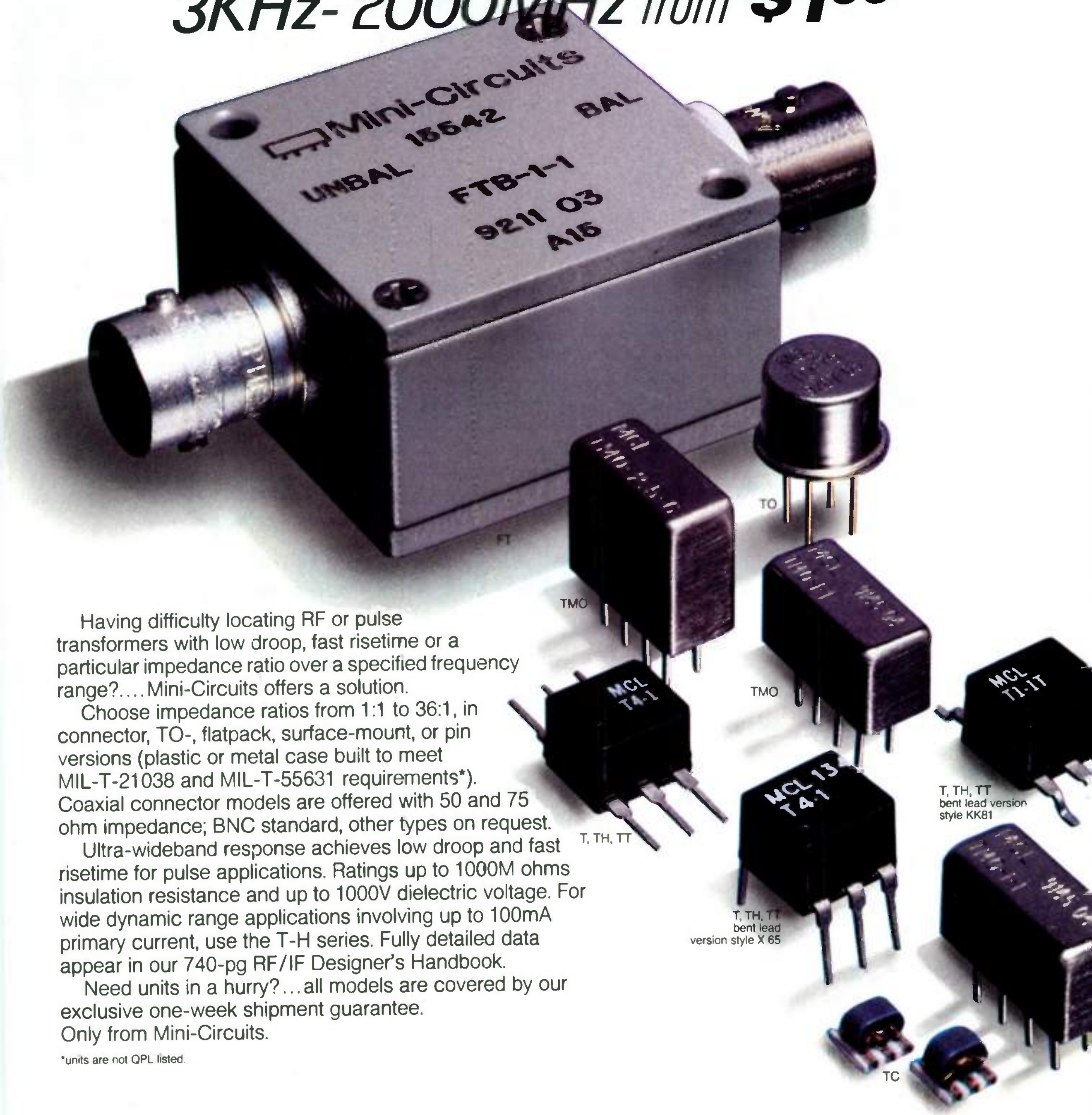

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PRODUCTS NEWSLETTER

Pay-As-You-Go Cellular Phone Is Launched

Those concerned about entering the wireless world because of cost reasons may want to look into the "pay-as-you-go" cellular kit. Developed by Cellular One, Schaumburg, Ill., Cellular One•2•3 includes a cellular phone, a battery, and charger. It also comes with the AccessCard, which is filled with a predetermined amount of local air time. As a result, there's no long-term contract, no credit check, no monthly bill, and no activation fee. Basically, customers choose exactly how much they want to spend on cellular service. Both local and long-distance calls can be made and received, with all charges deducted directly from the customer's account. When the allotted time is nearing its expiration, customers are notified of the number of available minutes remaining. When the initial 60 minutes of air time on the AccessCard expires, users can "refill" their card with the amount of air time they want by making a phone call or taking the card to any participating Cellular One location. Call Gina Macchitelli at (847) 762-2528, or Melissa Vadman at (312) 751-8878. *RE* **CIRCLE 590**

Data-Acquisition Interface Board Expands Capabilities

The recently unveiled AIB-PCx interface board is targeted for instrument data acquisition and control. The general-purpose IBM PC ISA board, designed by Sunset Laboratory Inc., Forest Grove, Ore., features a wide range of sensing capabilities, including measurement of voltage, current, resistance, temperature, sound, light intensity, pressure, acceleration, magnetic field strength, and so on. It features eight software selectable inputs and a 12-bit analog-to-digital converter with a built-in track-and-hold amplifier offering 1.4-µs conversion time (up to 200-kHz data input rates). Six software-selectable input ranges are available—bipolar: –10 V to +10 V, –3 V to +3 V, and –0.5 V to +0.5 V; unipolar: 0 to +10 V, 0 to +3 V, and 0 to +0.5 V. Using an ISA Bus, the board is compatible with all IBM PCs and compatibles from the XT through the 386, 486, Pentium, and Pentium Pro. The AIB-PCx goes for $240; volume pricing is available. For more information, contact Robert A. Cary at (503) 357-5151; fax (503) 357-3168; e-mail: r.cary@sunlab.com. *RE* **CIRCLE 591**

Monochrome Camera Features Progressive-Scanning CCD

The KP-F1 black and white camera developed by Hitachi Denshi America Ltd.'s Industrial Video Systems Div. comes with a full frame shutter and a 1/2-in. progressive-scan-type CCD. Because it uses the progressive-scan technology instead of interlace scanning, the 44 mm by 44 mm by 67 mm camera provides video at 60 frames/s—twice the speed of a standard video camera. The enhanced scanning speed increases the amount of information displayed, improving the image's vertical resolution. Designed specifically for machine-vision applications, it can potentially speed up assembly line operation. For instance, the camera may be focused on bottles of pills to check to ensure that the labels are on correctly all of the pills inside the bottle are where they should be, says Phil Gant, v.p. of the company. The output of the camera travels to a computer which processes the signal and changes the manufacturing process, if necessary. Therefore, the higher the frame rate of the camera, the faster the assembly line can operate. Call (516) 921-7200. **CIRCLE 592**

JTAG Technology Eases Pc-Board Testing

Two newly developed devices from Quality Semiconductor can provide JTAG access to a data bus while being virtually transparent to a system during normal, non-JTAG operation. By combining the "like-a-wire" characteristics of the company's QuickSwitch devices with a JTAG boundary-scan access port, the QS3J245 and QS3J309 are able to reduce pc-board debug time, cut test-program development time, and minimize the need for costly test fixtures. The 8-bit J245 and 9-bit J309 are universal JTAG access-port devices with output enable. It offers scan coverage for system functional blocks without imposing cost and performance penalties of individual scan components. When not in boundary-scan mode, the QuickSwitch devices are turned on, allowing for transparent, bidirectional data propagation. When in boundary-scan mode, scan data can be captured from, or loaded onto, the data bus. The J245 comes packages in a 150-mil, 24-pin QSOP, while the J309 comes in a 150-mil, 28-pin QSOP. In 10,000 units, the price is about $3.47 apiece. Production quantities are available. Call Deepak Savadatti at (408) 450-8016; e-mail: deepal@savadattiqualitysemi.com; or Dan Anderson at (408) 450-8060; e-mail: dan_andersen@qualitysemi.com. *RE* **CIRCLE 593**

INSTRUMENTS

ULTRA-SMALL MODULES MAKE LAB-GRADE MEASUREMENTS IN THE FIELD

The Intelligent Link family of network measurement modules allows laboratory-grade measurements to be made in factory and field environments. The modules are small enough (1 by 1.25 by 6.5 in.) whereby they can be located very close to demanding signals and sensors to reduce lead-length errors and induced noise.

Users can store or display the results locally for monitoring and debug purposes, or transmit them over more than a dozen types of communications networks for remote use. Among the protocols supported are Ethernet, RS-232C, RS-422, RS-485, Centronics, and IEEE-488. On-board intelligence allows the module to apply complex algorithms to the input signals, which eliminates the need for the host computer to provide signal processing.

Each module handles a specific class of analog inputs and has a specific type of network interface at the output. Seven models are currently available. Sensors and signals accommodated include strain, force, weight, RTDs, thermistors, pressure transducers, temperature, humidity, calculated dew point, torque, RPM, horsepower, ohms, and dc volts. Digital inputs and outputs also are available. Other modules planned for the near future will handle low currents, thermocouples, motion sensors, frequency, and counter-timer functions.

Keithley Instruments Inc., *28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115 or (216) 248-0400; e-mail: product_info@keithley.com; Web: http://www.keithley.com.*

CIRCLE 660

■ JOHN NOVELLINO

EMULATORS OFFER REAL-WORLD TESTING FOR WIRELESS COMMUNICATION SYSTEMS

A pair of emulation instruments ensure thorough, repeatable testing of wireless communications equipment. The TAS 4600 is an integrated, one-box unit that emulates the noise and interference found on most wireless communications channels. The TAS 4500 FLEX4 accurately emulates channel characteristics like multipath or terrain-induced fading, delay spread, and path loss. Both instruments employ a modular architecture that can be easily upgraded as a user's needs change or as standards are revised. The TAS 4600 has attenuation capability and includes two channels.

Features offered by the TAS 4600 include an instrument-grade power meter for precise carrier and noise measurements, and calibration constants stored in nonvolatile memory for enhanced accuracy. The system meets or exceeds testing standards for both the cellular and PCS bands, as well as recently introduced CDMA equipment test specifications like IS-97A and IS-98A.

Users can operate the TAS 4600 using front-panel controls or through a host PC using TASKIT for Windows, the company's standard control software. A high-level remote-control command set simplifies test automation. IEEE-488 and RS-232 interfaces are standard.

The TAS 4500 FLEX4 offers a choice of standard or wide-bandwidth signal-processing modules. The two-channel instrument's wide-bandwidth emulation delivers 1-ns resolution for indoor applications. Propagation delays of up to 1.6 ms are available. Users can apply multiple modulations within the same channel. Twelve paths are available, and dynamic range is 114 dB.

With its ability to change fading models and sequence length, the unit allows users to create a wider range of realistic propagation scenarios. For advanced applications, the FLEX4 can expand a four-branch diversity system with full correlation control to test space diversity receivers.

TAS 4600 prices start at $38,950, while the TAS 4500 FLEX4 starts at $34,950. Both instruments are available immediately.

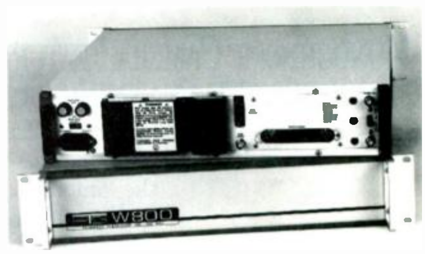
Telecom Analysis Systems Inc., *P.O. Box 497, 34 Industrial Way, Eatontown, NY 07724; (908) 544-8700; fax (908) 544-8347; 76546.2353@compuserve.com.*

CIRCLE 661

■ JOHN NOVELLINO

SYNTHESIZER SPECIALIZES IN WIRELESS COMM TEST

With a range of 800 to 960 MHz, the PTS W800 frequency synthesizer is designed specifically for wireless communications applications. A companion instrument scheduled for introduction shortly, the PTS W1850, covers the 1800-to-1900-MHz wireless bands. Both instruments feature frequency switching of 20 µs, phase noise of "-"110 dBc at a 1-kHz offset, frequency resolution of 0.1 Hz, and spurious outputs of "-"65 dBc. A vector modulator option allows user input of I and Q data for up-conversion to wireless frequencies. The units are designed for rack-mount or benchtop use. Versions are available with manual front-panel controls for engineering and prototype development ($5100) or with remote-control capability only for OEM use ($4800). Delivery is in 8 to 12 weeks. JN



Programmed Test Sources Inc., *9 Beaver Brook Rd., P.O. Box 517, Littleton, MA 01460; (508) 486-3008; fax (508) 486-4495.* CIRCLE 662

SOFTWARE

C/C++ SOFTWARE TARGETS POWERPC, MAC OS

Version 3.0 of the Motorola C/C++ Software Development Kit (SDK) is available for the Mac OS. Besides offering a complete set of development tools for Apple's Macintosh Programmers' Workshop (MPW) environment, including the Kuck & Associates Preprocessor (KAP), the new version of the Motorola SDK includes "plug-in" versions of the C/C++ compilers that can be used directly by licensees of the Metrowerks CodeWarrior and Symantec Project Manager development environments.

The kit also includes versions of the highly optimized "libmoto" libraries, which are compatible with the Apple, Metrowerks, and Symantec environments. The development tools aim to enhance applications such as interactive entertainment and computer games. Tests have shown that code generated by the Motorola compiler is 18% to 29% faster than code generated by other industry-standard compilers for a broad series of standard benchmarks, including Nullstone, Dhrystone, Whetstone, Linpack and the BYTE benchmarks.

As the first development kit to support Apple's MPW, Metrowerks CodeWarrior, and Symantec Project Manager development environments, the C and C++ compilers enable developers to optimize code simultaneously for members of the PowerPC family of microprocessors, including the 601, 603, 604, and 620, while maintaining code compatibility across all PowerPC family members. The Motorola C/C++ kits, which list at $299, comprise a complete MPW development environment (including the MPW shell, debugger, linker, and libraries). A "plug-in" kit consisting of only the Motorola C/C++ compilers, assemblers and "libmoto" libraries for the CodeWarrior and Symantec Project Manager environments also is available for an initial list price of U.S. $99. Additional information is available on Motorola's development tools on its PowerPC Web server, which is located at *http://www.mot.com/PowerPC/*. SVT

***Motorola, RISC Software**, 6501 William Cannon Dr. W, MS OE-112, Austin, TX 78735; (800) 347-8384; ppcinfo@risc.sps.mot.com or motosoftware@applelink.apple.com* CIRCLE 663

SOFTWARE MANAGES DOCUMENTS AND DRAWINGS

Version 4 of the AutoEDMS for Windows is a document, drawing, and image-management system designed for workgroups and multisite enterprises. New features and functions include viewing support for AutoCAD R.13, MicroStation, CALS IV, and HPGL/2. Document management is implemented through user-designed screens containing textual database information and graphical views of managed files. Among the document-management functions are check-in/check-out, revision control, automatic file naming, and file activity audit trails. In addition to documents, users can automatically manage and view drawings, spreadsheets, scanned images, and faxes. All supported file types can be viewed, printed and copied to the Windows clipboard without using native applications. Network operating systems supported include Novell NetWare, NT Server, DEC Pathworks, LAN Manager/LAN Server, Banyan Vines, and Windows for Workgroups. An upgrade from AutoEDMS for Windows Version 3.1 to version 4 is $79 per seat. Upgrade pricing for DOS users is $279 per seat. New product pricing is $895 for the Starter Kit (two users) and $395 per Expansion Kit. An optional CAD Viewing Module is $195 per seat and Document Viewing Modules are $150 per seat. ML

***ACS Software Inc.**, 25825 Eschelman Ave., Lomita, CA 90717-3220; (310) 325-3055. ML* CIRCLE 664

EMULATORLESS DEBUGGING FOR POWERPC 604

Combining the Single-Step On-Chip Debugger from SDS and the Hewlett-Packard Processor Probe for the embedded PowerPC 604 provides real-time debugging performance without the need for in-circuit emulators. The PowerPC 604 is a superscalar, multiprocessor-enabled chip that issues up to four instructions in parallel every clock cycle to six execution units. Its 3-stage, double-precision, floating-point unit allows the use of highly graphics-oriented software packages. At 100 MHz, the PowerPC 604 has an estimated SPECint92 rating of 160 and an estimated SPECfp92 rating of 165. The new PowerPC 604e at 200 MHz provides an increase of approximately 400% in desktop computing power over the original PowerPC 601. Single-Step for the HP Processor Probe is designed to benefit companies developing around a real-time operating system. Single-Step for the HP Processor Probe starts at $8400 under Unix and $6500 under Windows (including the HP Processor Probe hardware). ML

***Software Development Systems Inc.**, 815 Commerce Dr., Suite 250, Oak Brook, IL 60521; (798) 368-0400 or (800) 448-7733.* CIRCLE 665

ADD-ON MODULE PROCESSES DIGITAL AUDIO

Digital audio analysis, display, and processing now is available through a menu-driven environment provided by DADiSP/WAV, and add-on module to DADiSP developed by DSP Development Corp. Integrated with the DADiSP graphical spreadsheet for scientific and engineering data analysis, DADiSP/WAV allows digital audio data to be read, written, and edited via pop-up menus or on-line functions. The module supports the standard PCM WAV file format for 8- and 16-bit mono or stereo data. DADiSP/WAV lets users call any Windows-compatible WAV player device and play WAV data on any WAV-compatible sound card. All source code is written in the DADiSP programming language (SPL), and variable definitions and menus are supplied in ASCII text format so they can be customized by the user.

DADiSP provides an intuitive icon- and menu-driven environment for data management and display, allowing users to work with data series of any length. The spreadsheet combines hundreds of built-in functions so that it's able to perform graphical data analysis, data management, and FFT analysis.

WAV files are typically digital audio files that conform to the Microsoft Windows WAV file format standard. A WAV file is a binary file that consists of a 44-byte header as well as its corresponding sound data. The DADiSP/WAV module, which is priced at $495, is employed with the DADiSP 4.0 Windows version ($1895). ML

***DSP Development Corp.**, One Kendall Square, Cambridge, MA 02139; (617) 577-1133.* CIRCLE 666

DC-DC Converters Have High Isolation

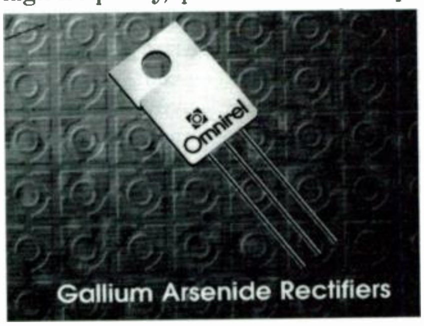
The NMV range of pc-mounted dc-dc converters have an input-to-output isolation and power-handling capability rated at 3 kV and 1 W, respectively. Standard devices operate from 5-, 12-, 24-, and 48-V supplies, and feature outputs of 5, 9, 12, and 15 V. Single- and dual-output versions also are available, which allow loading to be split in any proportion between the outputs.

All devices in the NMV range operate at a power density of 0.89 W/cm^3, have a typical efficiency of 80% at full load, and come in low-profile DIP or SIP package styles. The devices operate to 125°C. Pricing is $10.89. PM

***Newport Technology Inc.,** 6321 Angus Dr., Raleigh, NC 27613; (919) 571-9405.* CIRCLE 667

GaAs Rectifiers Have High Reliability

The IN675x series of GaAs Schottky rectifiers, which is rated at 180 to 250 V and 9 and 10 A, targets high-reliability, high-frequency, power-conversion ap-

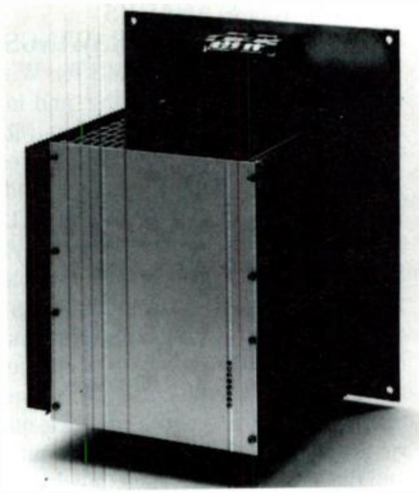


plications. The devices come in a TO-257 metal package and are available with or without isolation (to 700 V), as well as in both single- and center-tap configurations. Features include a reverse recovery time of 12 or 13 ns, a non-repetitive peak surge current of up to 20 A, and an operating temperature range of –55 to 175°C. Pricing ranges from $92.70 to $130 each in lots of 100 to 499, with samples from stock and production quantities available in 8 to 14 weeks. PM

***Omnirel Corp.,** 205 Crawford St., Leominster, MA 01453; (508) 534-5776.* CIRCLE 668

DC Power Converters Are VME-Compatible

The C3600 Series of 1700-W dc-dc and ac-dc converters are 6U VMEbus-



compatible and come in seven standard dc input voltage ranges, from 18 to 36 up to 450 to 900 V. The ac input ranges are 185 to 264 and 93 to 138/185 to 264 (switchable) V ac. A variety of single outputs are available, ranging from 4.5 to 5.5 V dc up to 200 to 250 V dc. Outputs are adjustable and fully regulated to 0.2% or better (load) and 0.1% (line). All units have remote sensing, overvoltage protection, and current-limit protection on the output. Efficiencies run up to 90% and the operating temperature range is –40 to 75°C. Cost is from $1946 each per 100, delivery is five to eight weeks. PM

***Schaefer Inc.,** 200 Butterfield Dr., Ashland, MA 01721; (508) 881-7330.* CIRCLE 669

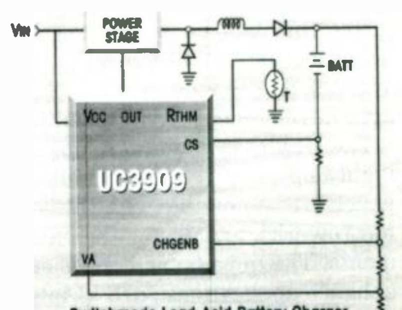
High-Power Switching Supplies Are Rugged

The FE Series of rugged ac and dc switching power supplies have a universal ac input front end with power-factor correction. They're available in pc-board or chassis-mount versions with output power levels of 30, 50, or 100 W. The modules have an operating temperature range of –25 to 85°C (baseplate), fixed frequency operation (100 kHz typical), and 3750-V ac I/O isolation. Measuring from 3.5 by 2.5 by 0.84 in. for the 30-W versions up to 4.8 by 3.8 by 1.0 in. for the 100-W unit, the supplies have triple output protection comprising overvoltage crowbar, thermal shutdown, and continuous short circuit. Line regulation and ripple are ±0.5% and 1% of V_{out} (or 50 mV, whichever is greater), respectively. Agency approvals are pending. Pricing is $97.90 each per 1000 for the 100-W version and delivery is stock to 14 weeks. PM

***Wall Industries Inc.,** 5 Watson Brook Rd., Exeter, NH 03833; (603) 778-2300.* CIRCLE 670

Switchmode Chip Charges Batteries Efficiently

Combining charge-state logic with average-current PWM control circuitry, the UC3909 family boosts the charge



Switchmode Lead-Acid Battery Charger Optimizes Efficient Control

efficiency in lead-acid batteries. The UC3909 includes a thermistor that tracks battery requirements over temperature, thus providing precise control of the rate that matches the battery's ability to accept charge. Four status bits report the state of charging at all times. Also contained is a differential current-sense amplifier, a voltage reference, a thermistor-linearization circuit, voltage and current error amplifiers, a PWM oscillator, a comparator and latch, and a 100-mA open-collector output driver. Undervoltage lockout circuitry also is provided. VB

***Unitrode Corp.,** 7 Continental Blvd., Merrimack, NH 03054-4334.* CIRCLE 671

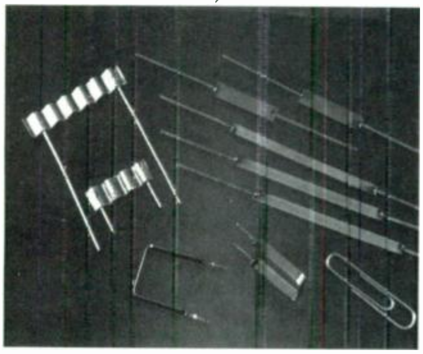
Voltage Regulator Modules Serve Pentiums

A line of voltage regulator modules from C-MAC have been derived from Intel specifications to address the power needs of both the Pentium (P54) and Pentium Pro (P6) processors. These deliver from 2.5 to 13 V at up to 13 A, and offer a high-efficiency solution to providing high-current sources in proximity to the associated processor. Initial samples are available now. VB

***C-MAC Microcircuits Ltd.,** South Denes, Great Yarmouth, Norfolk, NR30 3PX, U.K. (+44) 1493 858536.* CIRCLE 672

WELDED SENSING RESISTORS PERFORM LIKE WIREWOUNDS

Utilizing a three-piece welded element construction, the Series 60 of



Lo-Ohm current-sensing resistors offers the performance of wirewound resistors at low cost. With resistance values as low as 0.005 Ω, the Series 60 is offered in power ratings from 0.1 to 5 W in axial-lead, radial-lead, and corrugated wire radial-lead versions. Price is as low as $0.15 in large quantities. VB

Ohmite, 3601 Howard St., Skokie, IL 60076; (847) 675-2600. CIRCLE 673

VCXO GUARANTEES ±25-PPM ERROR

Models M2031, -2 and -3, available for center frequencies from 1 to 175 MHz, are tested and individually guaranteed to have less than 25 ppm frequency error (deviation) at a control

voltage of 2.5 V. Typical jitter is less than 40 ps p-p, and control-voltage bandwidth extends to 75 kHz. Oscillator startup time is less than 5 ms. Frequency capture ranges of 50, 100, and 150 ppm, respectively, are guaranteed from 0°C through +70°C. They provide full-scale capture with a 0.5 to 4.5 V control voltage, and draw from 30 to 60 mA, depending upon logic family and operating frequency. The VCXOs are available in ECL and HCMOS logic families, and are supplied in dual-in-line packages. VB

MF Electronics, 10 Commerce Dr., New Rochelle, NY 10801; (914) 576-6570. CIRCLE 674

REGULATOR FOR RS-232 IS HIGHLY ACCURATE

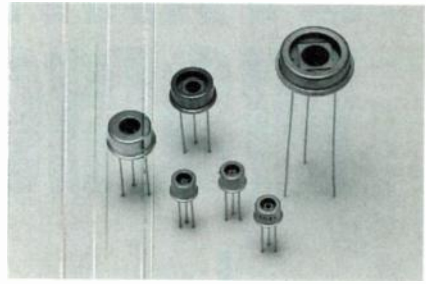
The MicroPR-RS232 pressure regulator for process control applications delivers a high accuracy (within ±0.25%) pressure output in response to a serial input signal. It can control the output pressure of an inert gas from 0 up to

100 psig. Included in the regulator are a Fluistor microvalve chip, a silicon micromachined pressure sensor, and electronic feedback circuitry. It has standard NPT pneumatic connections. Standard pressure ranges of 0 to 5, 30, and 100 psig are available. It has a response time of 2 seconds. Power requirements are 15 V at 100 mA continuous, 250 mA peak. It thus consumes less than 2 W during normal operation over the 0 to +55°C range. The MicroPR-RS232 can be controlled with an analog signal (0.5-4.5 V) or digital (RS-232) control interface. VB

Redwood Microsystems, 959 Hamilton Ave., Menlo Park, CA 94025; (415) 462-5812. CIRCLE 675

AVALANCHE PHOTODIODE IMPROVES MEASURMENTS

Having a low temperature coefficient of breakdown (0.4 V/°C) over a wide temperature range (–40 to +85°C), the silicon S6045 series serves well in applications requiring temperature-stable, distance-related measurements, such as in laser radars. Six models are available, all suited for low-level light detection in the near-infrared spec-



trum. Peak sensitivity occurs at 800 nm. Cutoff frequencies are as follows: S6045-01, 1 GHz at 800 nm; -02, 900 MHz; -03, 600 MHz; -04, 350 MHz; -05, 80 MHz; and -06, 35 MHz. Maximum dark-current ratings range from 0.5 nA for the -01 model to 30 nA for the -06 model. The photodiodes have a typical voltage rating of 200 V. They achieve a quantum efficiency of 75%, with an excess noise figure of 0.3 at 800 nm. They're available in TO-5, -8, and -18 packages with borosilicate-glass windows. VB

Hamamatsu Corp., 360 Foothill Rd., P.O. Box 6910, Bridgewater, NJ 08807-0910; (908) 231-0960. CIRCLE 676

ALUMINUM CAPS GIVE HIGH VALUES FOR SMT BOARDS

Opening the door to ever-greater high-capacitance values in surface-mount applications, the CLB 136, 165, and 048 Elcap Series of aluminum capacitors place as much as 680 µF on board. The CLB 136 is characterized by very low ESR and high ripple-current capability per unit volume, principally for filtering in SMPS circuits. It's available in capacitances from 10 to 470 µF. The CLB 165 Series, with a maximum operating temperature of 125°C, is particularly suited to the engine compartment of motor vehicles. It's available in capacitances from 10 to 330 µF. The CLB 048 Series offers an extended range of capacitances from 10 to 680 µF with voltage ratings from 10 to 100 V. It's particularly well suited to energy storage and telecom applications. The three series are surface-mount equivalents to the company's RVI 136, RHT 165, and RML 048 Series, respectively. They come in a nominal case size of 10 by 10 by 14 mm and are supplied in blister tape-on-reel applications. VB

Philips Components, Building BAE-I, 5600 MD, Eindhoven, The Netherlands. Contact Cor Vreven at (+31) 40 272 2790. CIRCLE 677

EMBEDDED DRAM LETS ASICS DELIVER SYSTEM SOLUTIONS

A family of high-integration system ASICs that contain large blocks of customer-configurable DRAM provide designers with a potential single-chip solution for many memory-intensive systems. Fabricated with 0.5-µm design rules (0.46-µm effective channel lengths), the EDL60 series gate arrays combine 60 to 400 kgates of random logic and from 1 to 16 Mbits of embedded DRAM on one chip.

The first member of the family, the EDL60, will pack 60 kgates and 1 Mbit of user-configurable DRAM. Another chip, slated for release by mid-1997 will pack 100 kgates and 4 Mbits of DRAM. From there, the company will move to a 0.35-µm process, which will allow them to offer a new family member that packs 400 kgates and 16 Mbits of embedded DRAM. Such a chip contains a transistor count equivalent to three Intel P6 microprocessors at 5.5 million transistors each. Additional plans call for process improvements that will transition the technology to a 0.25-µm process in 1998 and a 0.19-µm process in 1999.

The arrays are designed for operation from a 3.3-V supply and have I/O lines that can be powered by the same 3.3-V supply or from a separate 5-V supply for interfacing to 5-V systems. The logic process can support such functions as high-performance phase-locked loops and various I/O interfaces, including PCI, LVDS, and ATA. Individual gates consume just 1.6 µW/MHz with an average load, which keeps the power in the logic array to reasonable levels.

To ease the crosstalk analysis at the system level, the company also provides Spice models for the high-performance I/O blocks. For comprehensive chip testing, the design tools support internal scan ATPG, IEEE 1149.1 JTAG, RAMBIST, and IDDQ test schemes.

Aimed at high-integration applications such as set-top boxes, digital-versatile-disk (DVD) systems, interactive video games, Ethernet/ATM switches, graphics/MPEG frame buffers, and on-chip cache for CPU subsystems, these embedded-memory arrays bring the system RAM on-chip. This makes possible true "system-on-a-chip" implementations.

By bringing the system RAM on-chip, the system benefits because there are fewer chips—it can be made smaller and will consume less power. As a result, it will offer higher reliability and potentially higher performance. Since the signals between the RAM and logic don't have to travel off-chip, less power is needed to drive the signals. Wider buses can be used to transfer data, improving system performance even further. Moreover, user configurability allows designers to select the chip with the memory size that best matches their system requirements, thus optimizing the system cost.

Designs are supported by "open" EDA design tools from vendors such as Cadence, Mentor, Synopsys, and Viewlogic. Customers also can enhance their toolsets with value-added Samsung tools that include dynamic and static power analysis, delay prediction, and clock routing. As gate densities evolve through 1997, customers will be able to integrate a wide variety of processor cores, such as the ARM7 RISC, 80C52, and the Pine and Oak DSPs, as well as a wide range of complex building blocks from the company's macrocell library.

Prices for the embedded arrays depend on many factors, therefore individual quotes are required.

Samsung Semiconductor Corp., *3655 N. First St., San Jose, CA 95134; Farzad Zarrinfar, (408) 954-7228.*

CIRCLE 678

■ DAVE BURSKY

TRIO OF MINIRISC 32-BIT CORES SET THEIR SIGHTS ON HIGH-END TASKS

LSI Logic has added a trio of 32-bit user-definable MIPS R4000-compatible microprocessor cores to its MiniRISC family of CoreWare cells. The cores target such applications as digital-versatile-disk (DVD) systems, set-top box control, direct satellite broadcast receivers, digital cameras, routers, multifunction peripherals, cellular phones, and many other applications.

The first two cores take aim at cost-sensitive applications. They include the CW4002 and 4003 MiniRISC processors, which employ three-stage pipelines to minimize chip area. The third core, the CW4011, is meant for high-performance applications and employs a superscalar architecture with a dual five-stage pipeline.

Fabricated with 0.45-µm design rules, the CW4002 can operate at clock frequencies of up to 40 MHz and deliver a throughput of about 33 MIPS while consuming about 2 mW/MHz. Upping the ante, the CW4003 employs 0.25-µm design rules and can operate at clock rates to 85 MHz as well as deliver a throughput of 75 MIPS. Yet it consumes just half the power of the CW4002—just 1 mW/MHz.

The high-end core, the CW4011, also employs 0.25-µm design rules. But, thanks to its superscalar architecture, the chip can deliver a throughput of 150 MIPS when clocked at 100 MHz. The more-complex architecture does require more power, though—the core consumes about 3.5 mW/MHz. This core also contains DSP-like functionality to support the computational requirements in applications such as multimedia and image processing (MPEG-2 encoding/decoding, 3D graphics, etc.).

All three cores support caches of up to 16 kbytes and include the company's FlexLink interface and ScanICE test debug support. The FlexLink interface allows the standard MIPS-II instruction set to be easily extended and tailored to a particular application by providing a direct connection into the processor's pipeline.

The cost to use the cores is part of the overall ASIC development fee structure and depends on volume, engineering costs, and other factors.

LSI Logic Corp., *1551 McCarthy Blvd., Milpitas, CA 95035; Jim Panfil, (408) 433-8000.*

CIRCLE 679

■ DAVE BURSKY

SYNTHESIS-OPTIMIZED CELL LIBRARY DELIVERS 5MGATES

A high-density ASIC cell library developed by Hitachi includes synthesis-optimized cores and pad cells. The HG73C libraries include four selectable drive strengths, and a patented noise-isolation scheme to reduce power and ground pin count. They also feature fully integrated analog phase-locked loops that can be used to reduce system clock-skew problems; and handcrafted, low-profile cells for simplified routing and minimal chip area.

The libraries are implemented in the company's 0.35-µm CMOS process, which employs a tight, 1.4-µm metal pitch with three levels of metal interconnections. That combination allows for gate counts of up to 5 million gates. By adding two more metal layers, the same silicon could support up to 6 million gates. I/O options include GTL and LV-TTL interfaces, as well as PCI and SCSI blocks.

The GTL and SCSI blocks can drive loads as high as 48 mA, while all other output pads can drive loads of up to 20 mA. When deployed with the Hitachi design kit, the HG73C libraries enable complete design flows and sign-off simulation at the end user's premises. Pre- and post-layout timing correlates to within 5% of Spice simulations.

The same technology also is part of an alternate sourcing arrangement with VLSI Technology Inc., San Jose, Calif. That setup offers the same capabilities in its High Density Initiative libraries. DB

***Hitachi America Ltd.**, 2000 Sierra Point Pkwy., Brisbane, CA 94005-1819; Jim Smith, (800) 285-1601 (U.S.), (415) 589-8300 (outside U.S.).* CIRCLE 680

CAM MEGACELL EASES NET HARDWARE DESIGN

A content-addressable memory, available as a megacell building block, provides designers with a flexible element that can be used in many custom chips targeted at networking applications, such as bridge and router designs, asynchronous-transfer-mode support systems, local-area-network switches, hard-disk drives, and so on. The CAM block, which can be configured for data widths ranging from 32 to 128 bits (selectable on a bit-by-bit basis), allows for bit-by-bit masks for searches with a speed of just 40 ns. By using the CAM generator software, a custom-sized CAM of up to 128 kbits can be created and embedded on the same chip with up to an additional 300 kgates of logic.

The cell is available as part of the ASIC library and design system offered by Kawasaki LSI U.S.A., and is implemented in the company's 0.5-µm ASIC process. Both Verilog and VHDL models are supported for high-level design, and the cell-library is supported on most popular design platforms—Cadence, Mentor, Viewlogic, and others. DB

***Kawasaki LSI U.S.A.**, 4655 Old Ironsides Dr., Ste. 265, Santa Clara, CA 95054; Keith Kawana, (408) 654-0180.* CIRCLE 681

SPEEDY ARM MEGACELL NOW IN 0.35-µm LIBRARY

Shrinking the core area for the ARM Thumb core (ARM7TDMI) to just 2.2 mm^2 by moving the design rules down to 0.35 µm, VLSI Technology brought the megacell into synchronization with its 0.35-µm cell library. Thanks to these small features, the Thumb core is able to operate at clock speeds reaching upwards of 90 MHz. This translates into a CPU throughput of about 80 MIPS—all while operating from a 3-V supply.

The core, which is available as part of the Functional System Block library, will actually be able to operate over a 2.5-to-3.6-V power-supply range. At 2.5 V, the core can operate at 53 MHz. When accessing 16-bit-wide memory, the ARM7TDMI core can deliver a top throughput of 0.75 MIPS/MHz. When interfaced to 32-bit-wide memories, the Thumb core delivers 0.9 MIPS/MHz.

HDL models of the core are available for use with design-automation tools from Compass Design Automation, Quick VHDL, Synopsys, Verilog, and Zycad. Designers can employ the company's VYC86C07-903 evaluation chip in breadboards. The VYF86C07-903FSB building block, now part of the library, can be used to implement new designs. DB

***VLSI Technology Inc.**, 1109 McKay Dr., San Jose, CA 95131; (408) 434-3000.* CIRCLE 682

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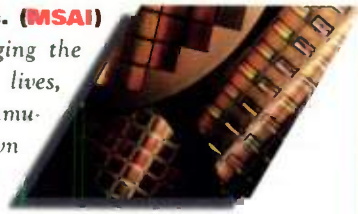

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2
COMPANY
3
DIVISION/DEPARTME
4
MAILING ADDRESS
5
CITY
6
POSTAL/ZIP CODE
7
HOMEADDRESS
8
CITY
9
POSTAL/ZIP CODE
10

1. Your Project Re
2. Your principal j
   1. ☐ Design & Devel
   2. ☐ Design & Devel
   3. ☐ General Corpo
   ☐ Other (please de
3. ☐ Your princi
   07. Design & Develop
   12. Design & Develop
   11. Executive & Oper
   01. Corporate & Oper
   03. Manufacturing & I
4. ☐ What is the
   21. Mainframe, Mini/S
   22. PCs, Workstation
   23. Laptops, Noteboo computers
   24. Other Computer/C
   02. Computer periphe plotter
   03. CAE/CAD/CAM s
   04. Software manufa
   05. Computer system
5. Do you buy thro
6. Do you design v
7. Do you design h
8. Do you have or
9. Do you subscrit
10. Products you sp

A Digital ICs
01 ☐ Microprocessor
02 ☐ 4/8/16 bit uPs/u
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16 ☐ Memory - ROM, EEPROM, Flash
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B Analog/Mixed-Signa
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04 ☐ Linear ICs & Mo
08 ☐ Communication
16 ☐ Audio Processin
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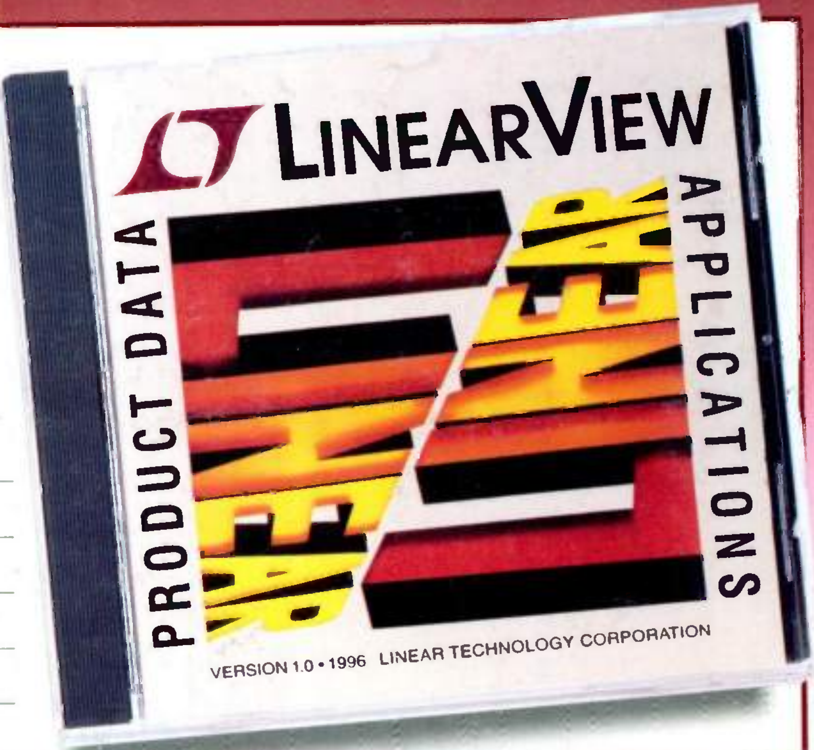

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