ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

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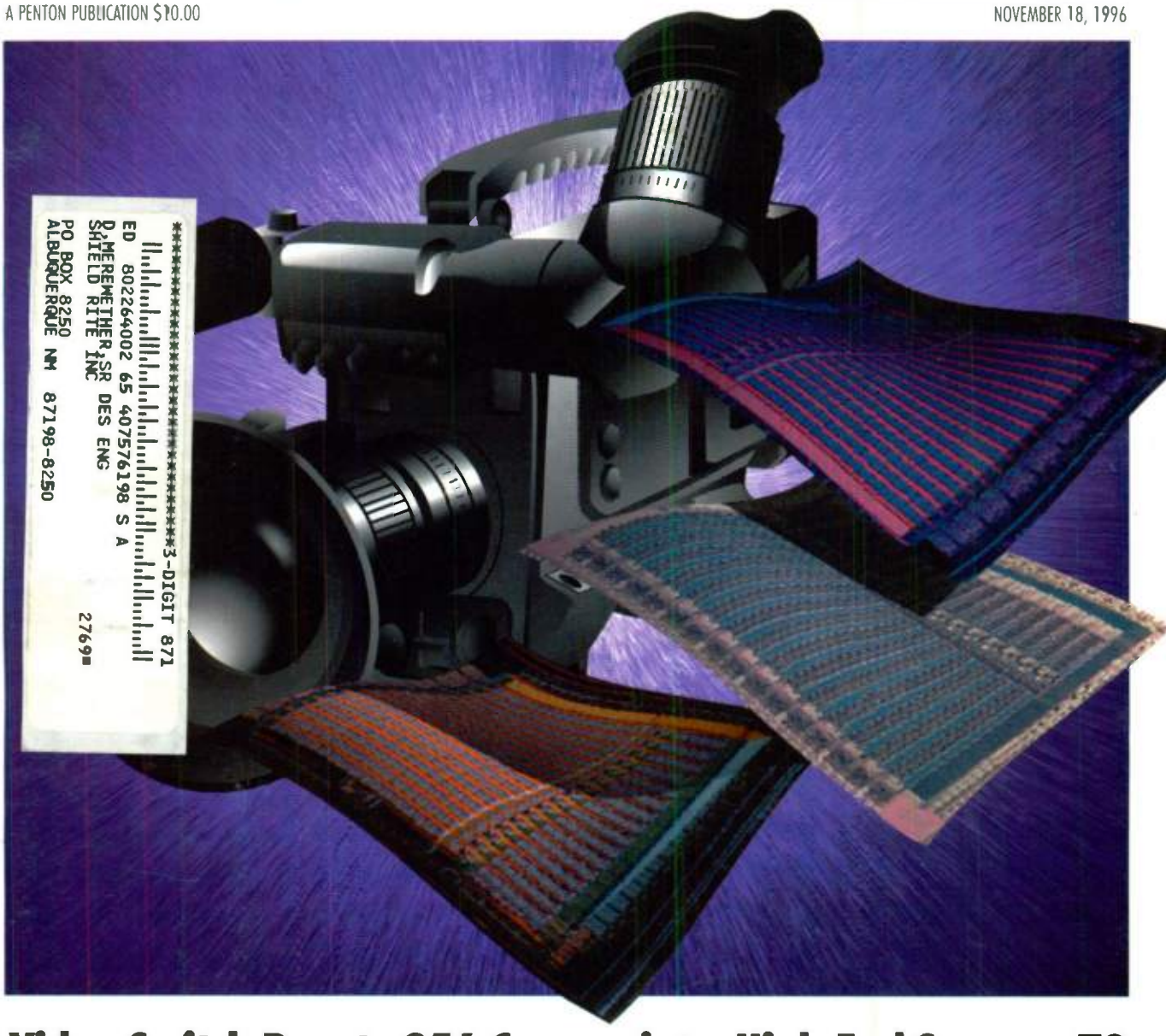
NOVEMBER 18, 1996



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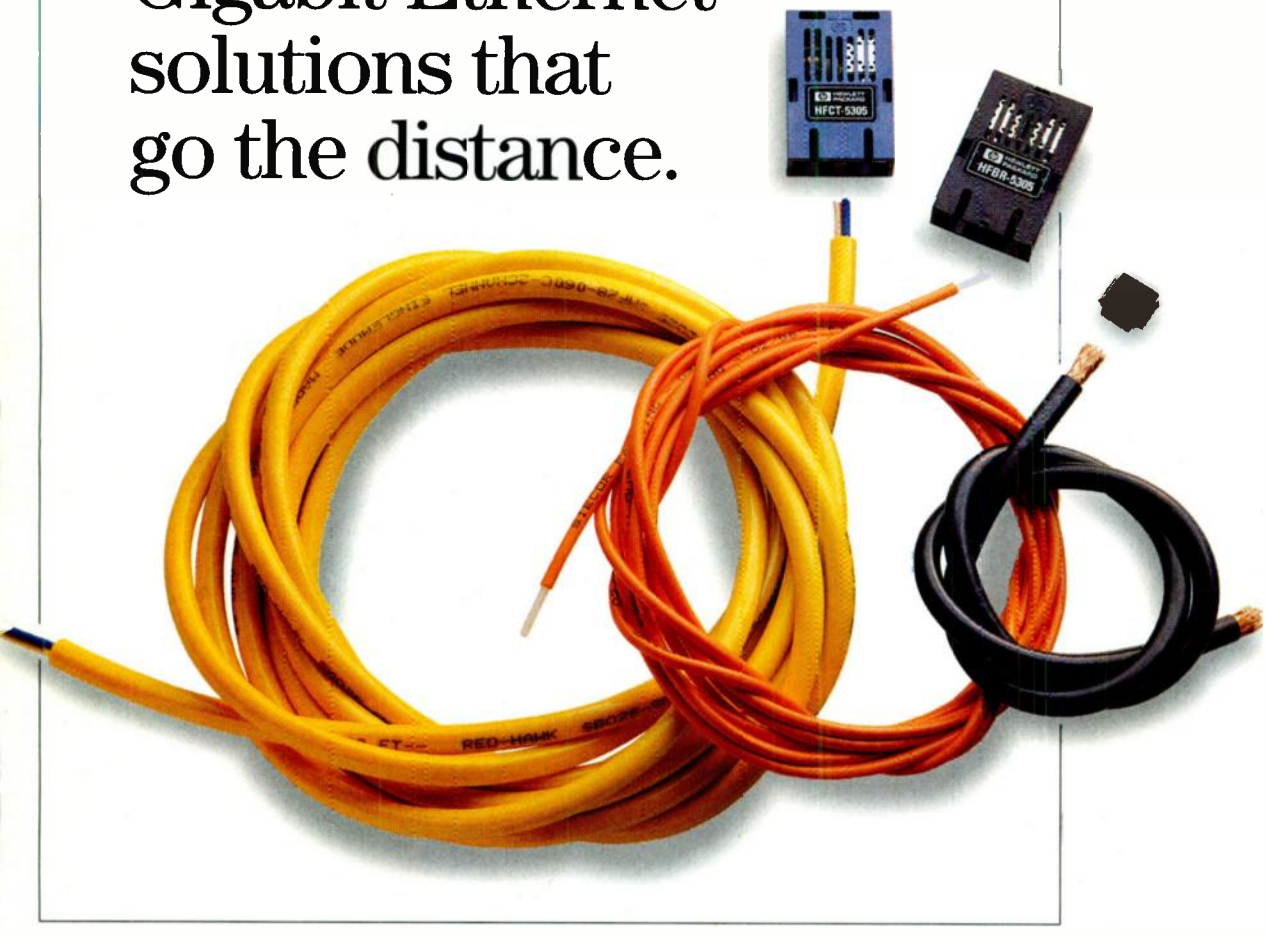

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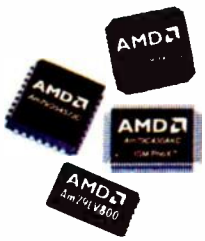

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ERA-3SM	DC-3000	19.4	11.0	4.5	23	2.15
ERA-4	DC-4000	13.9	▲19.1	5.2	▲36	4.15
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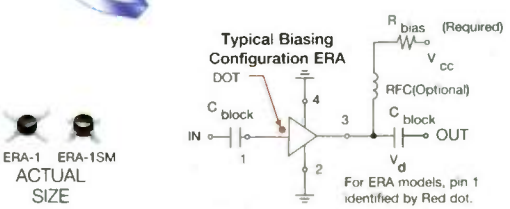

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ELECTRONIC DESIGN

November 18, 1996 Volume 44, Number 24

COVER STORY

256 Video Crosspoints In A TQFP Confound The Critics p. 73

Exceptional frequency response and low distortion change the conventional video switcher future.

FEATURES

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published twice monthly except for 3 issues in May and 3 issues in October by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $105 U.S., $185 Canada, $210, $255 International. Periodicals Postage Paid at Cleveland, OH and at additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.

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ELECTRONIC DESIGN

November 18, 1996 Volume 44, Number 24

DEPARTMENTS

Jesse H. Neal Editorial Achievement

Awards: 1967 First Place Award
1968 First Place Award
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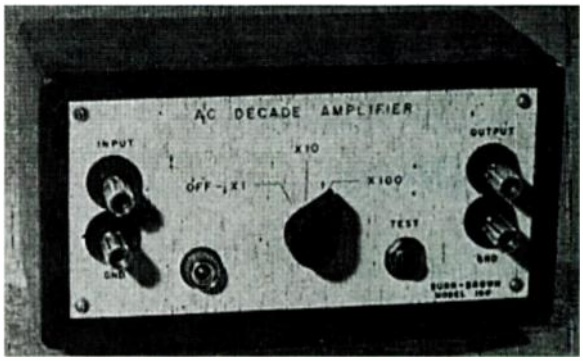
1975 Two Certificates of Merit
1976 Certificate of Merit
1978 Certificate of Merit
1980 Certificate of Merit
1986 First Place Award
1989 Certificate of Merit
1992 Certificate of Merit

COVER ART: B. J. JOHNSON

AC Decade Amplifier

No power cord but long battery life, small size, transistor reliability, and broad band pass add up to make this AC Decade Amplifier a neat laboratory tool. No polarity need be observed in connecting it to measuring equipment. Designed and manufactured by Burr-Brown Research Corp., Route 4, Box 139, Tucson, Arizona, the amplifier is powered by nine type-"C" flashlight cells with an approximate life of 1000 hours. Battery replacement is no problem since fresh standard type-C flashlight cells are easily obtained. The instrument is decaded in gains of X10 and X100 and is accurate to plus or minus 0.2 db at 1 kc. Gain change on both ranges is less than 0.3 db throughout battery life. It has a frequency response of from 1 cps to 800 kc. The low B voltages needed for transistors make possible dc coupling which results in good low frequency response.



The equivalent short-circuit noise resistance on both ranges is approximately 1500 ohms. The equivalent rms input short circuit noise voltage in various bandwidths is therefore approximately as follows: 20-kc bandwidth, 0.7 μv noise; 200-kc bandwidth, 2.2 μv noise; and 800-kc bandwidth, 4.5 μv noise.

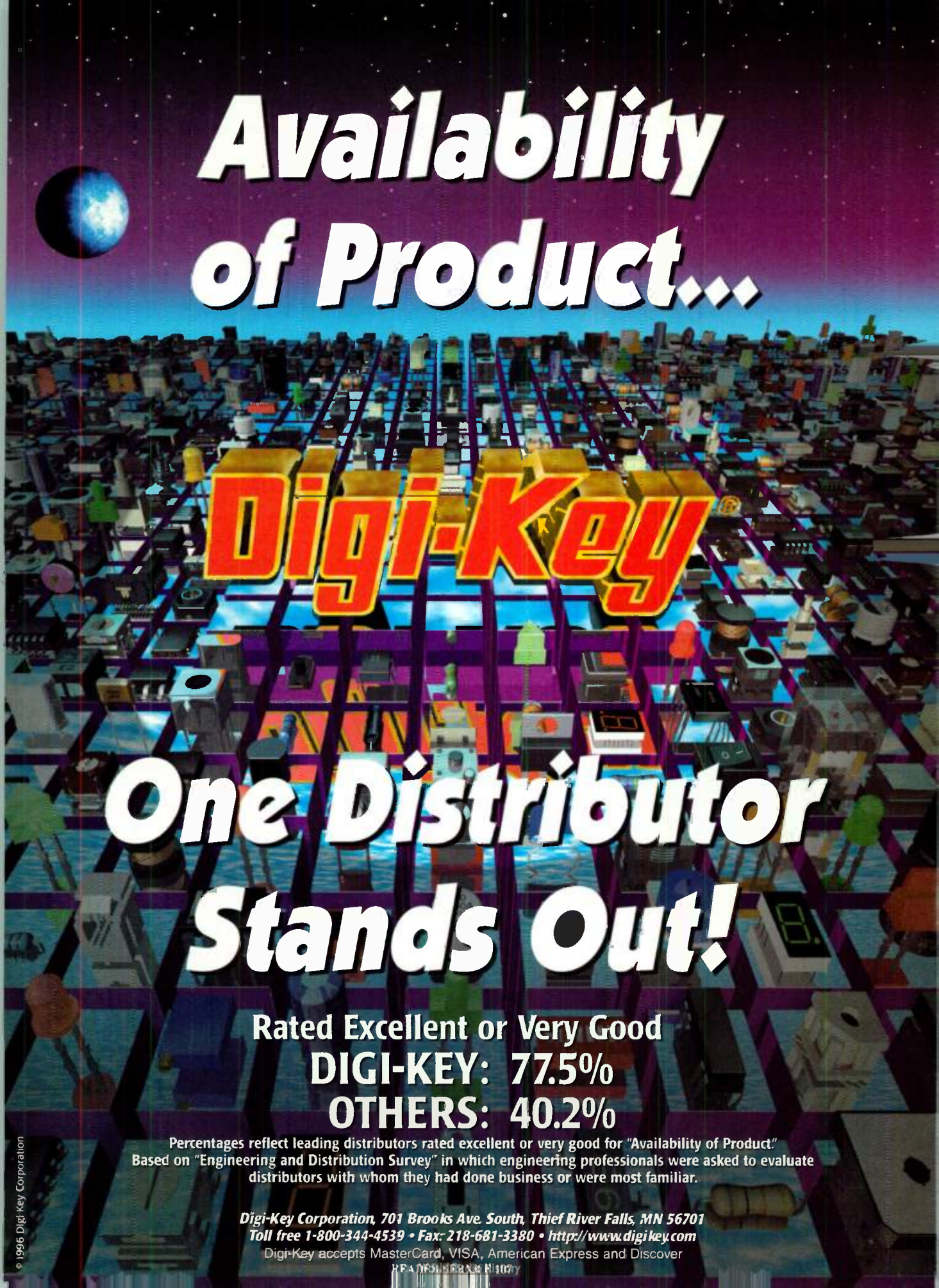
For input signal generator impedances in excess of 1000 ohms the noise figure may be taken as 6 db or less. Input impedance for the amplifier is approximately 100,000 ohms shunted by 35 μμf for both gain ranges. The maximum dc voltage which may be impressed across the input terminals is 150 v. The maximum open-circuit output voltage is 1.2 v rms. Weight of the amplifier is 2-1/2 lbs including batteries. Its dimensions are 7-9/16 in. x 3-7/8in. x 3-9/16 in. This is the first of a series of transistorized lab instruments. Also available now is a square wave generator.*(Electronic Design, November 15, 1956, p. 48)*

Burr-Brown co-founder Tom Brown looks back at the significance of this amplifier, one of the most important devices in the company's history: "This was a case of serendipity finding us. When we were designing this amplifier, without realizing it, we actually were designing the first commercial solid-state op amp. We originally went to dc coupling to get rid of the large capacitors, and it was our customers who recognized this amplfifier as an excellent op amp. From then on, we were in the op amp business."—SS

Electronic Control For Typewriters

In an effort to further simplify the typist's job, International Business Machines Corporation has introduced electronic sensing and control equipment in their standard electric typewriterer. Incorporating an electronic-tube switching circuit which operates a relay hooked up to the tabulator, the unit makes tabulation entirely automatic. Conductive ink is used on the billing or accounting forms which, according to IBM spokesmen, costs only a little more than ordinary ink. Contact for "tab sensing" is made by a conducting brush as it passes over the ink line, thus operating the relay and stopping the carriage in a prescribed number of spaces beyond the line. The electronic unit, although employing a tube, measures only approximately 3 by 6 inches in size. It is mounted beneath the keyboard. One of the problems in "electronifying" the typewriter is the small space available for the electronic unit. Transistors can be expected to play an important part in this development.*(Electronic Design, November 1, 1956, p. 5)*

It's interesting that this scheme is based on special treatment of the paper—the addition of conductive ink—rather than any intelligence built into the electronics, which essentially operates as a relay.—SS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UPCOMING MEETINGS

NOVEMBER

IEEE TENCON 96, Digital Signal Processing Applications, Nov. 26-29. Perth, Western Australia. Contact Australia Promotions Pty. Ltd., P.O. Box 1025, Bentley Delivery Centre, WA, 6983, Australia; (61) 9-470-2552; fax (61) 9-470-2556.

DECEMBER

DB/EXPO 96, Dec. 2-6. Jacob K. Javits Convention Center, New York. Contact Dave Codd or Karl Foster, Blenheim NDN, 1975 W. El Camino Real, Suite 307; Mountain View, California 94040: (800) 2DB-EXPO; fax (415) 966-8934; e-mail: DBEXPONY@blen-usn.mhs.compuserve.com.

Pacific Design 96, Dec. 4-5. Anaheim Convention Center, Anaheim, California. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

IEEE International Electron Devices Meeting (IEDM), December 8-11. San Francisco Hilton & Towers, San Francisco, California. Contact Melissa Widerkehr, Widerkehr & Assoc., 101 Lakeforest Blvd., Suite 270, Gaithersburg, Maryland 20877; (301) 527-0900; fax (301) 527-0994; e-mail: widerkehr@aol.com.

Winter Simulation Conference (WSC 96), December 8-11. Hotel Del Coronado, Coronado, California. Contact James J. Swain, Deptartment IDE, University of Alabama, Huntsville, Alabama 35899; (205) 890-6749; fax (205) 890-6608.

35th IEEE Conference on Decision & Control, December 11-13. International Conference Center Kobe and Portopia Hotel, Kobe, Japan. Contact Hidenori Kimura, Faculty of Engineering, Osaka University, Suita, Osaka 565, Japan; (810) 6 877 5111, ext. 5121.

Miniature Card Implementers Forum Info Workshop, Dec. 12. Austin, TX. Contact Kevin Randolph, (800) 462-1042 or (619) 673-0870; fax (619) 673-1432; e-mail: mcif@annabooks.com; Internet: http://www.annabooks.com.

JANUARY 1997

USELINUX: Linux Applications Development and Deployment Conference, January 6-10. Marriott Hotel, Anaheim, California. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

USENIX Technical Conference, January 6-10. Marriott Hotel, Anaheim, California. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

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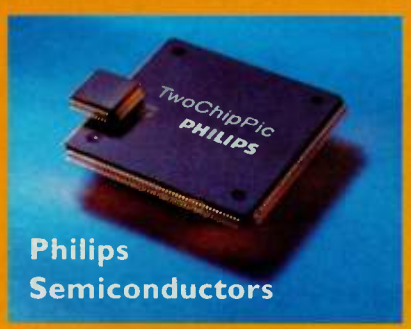

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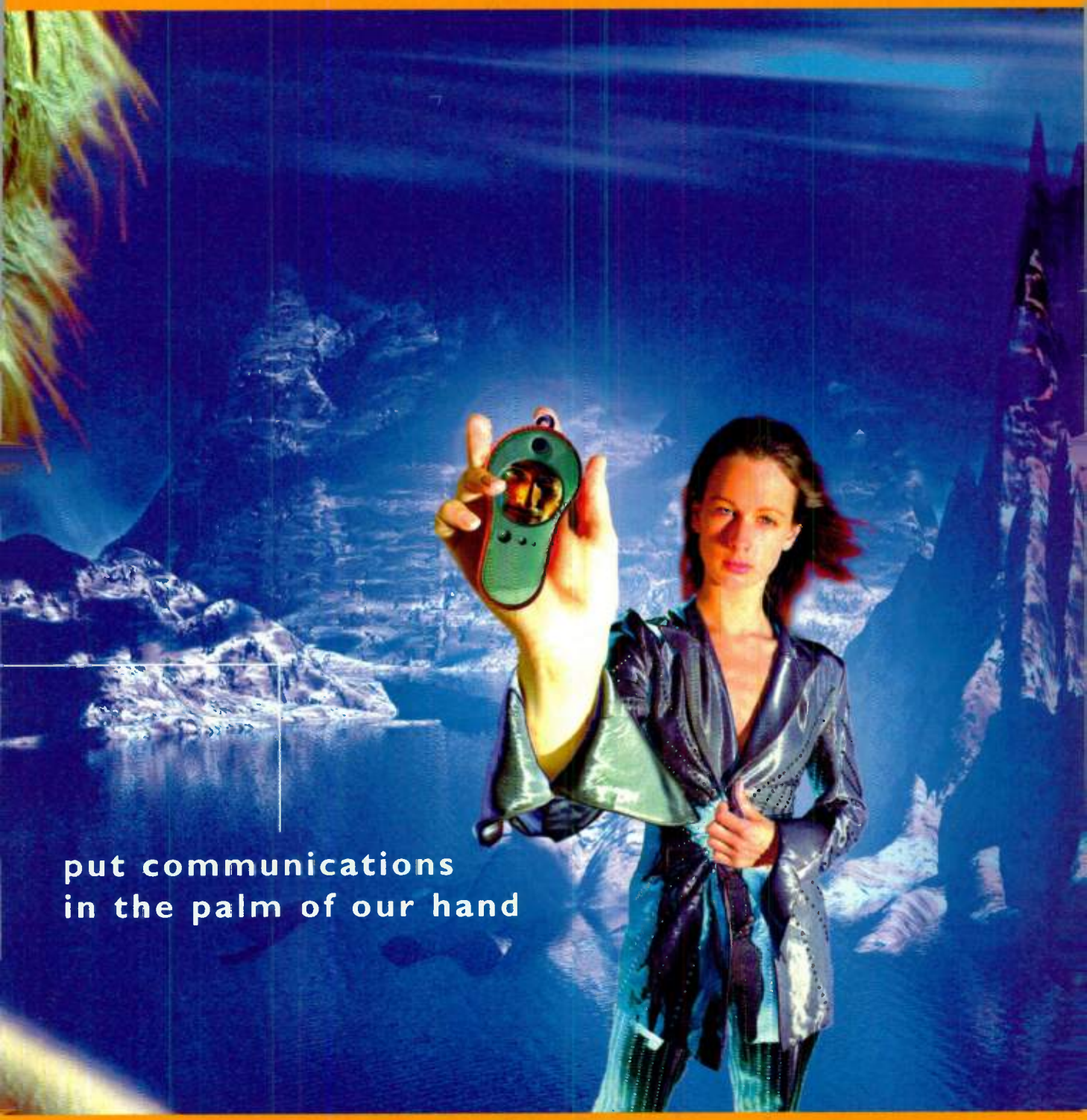

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UPCOMING MEETINGS

JANUARY

Annual Reliability & Maintainability Symposium (RAMS), Jan. 20-23. Philadelphia Marriott, Philadelphia, PA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Asia & South Pacific Design Automation Conference with EDA Technofair (ASP-DAC 97), Jan. 28-31. International Conference Hall, Chiba, Japan. Contact Yoko Nishikawa, ASP-DAC '97 Secretariat, CONVEX Inc., Ichijoji Bldg. 2-3-22 Azabudai, Minato-ku, Tokyo 106 Japan; (81) 3 3589 3355; fax (81) 3 3589 3974.

Second Annual Pan Pacific Microelectronics Symposium, Jan. 29-31. Sheraton Maui Resort, Maui, HI. Contact JoAnn Stromberg, Pan Pacific Symposium, 5200 Wilson Rd., Suite 215, Edina, MN 55424; fax (612) 929-1819.

FEBRUARY

IEEE Aerospace Conference, Feb. 1-8. Snowmass at Aspen, Colorado Contact Stephen Franklin, Deputy Program Chair, 4800 Oak Grove Dr., Pasadena, CA 91109; (818) 393-0814; fax (818) 393-0530; e-mail: stephen.f.franklin@jpl.nasa.gov.; Internet: http://chirp.plk.af.mil:1050/ieee/index.html.

IEEE Power Engineering Society Winter Meeting, Feb. 2-6. New York Hilton & Towers, NY. Contact Frank E. Schink, 14 Middlebury Ln., Cranford, NJ 07016-1622; (908) 276-8847; fax (908) 276-8847.

IEEE International Solid-State Circuits Conference (ISSCC 97), Feb. 6-8. San Francisco Marriott Hotel, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Suite 300, Washington, D.C. 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@mcimail.com.

Second International Conference on Chip-Scale Packaging, Feb. 20-21. Sunnyvale Hilton Inn, Sunnyvale, CA. Contact Subash Khadpe; (610) 799-0419; fax (610) 799-0519; e-mail: skhadpe@semitech.com.

IEEE Applied Power Electronics Conference and Exposition (APEC 97), Feb. 23-27. Westin Peachtree Plaza Hotel, Atlanta, GA. Contact Pam Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 347-5900; fax (202) 347-6109.

SOUTHCON 97, Feb. 25-27. Greater Ft. Lauderdale/Broward County Convention Center, Fort Lauderdale, Florida. Contact Joan Carlisle, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668 ext. 243; fax (310) 641-5117.

MARCH

IPC Printed Circuits Expo 97 & 40th Annual Meeting, Mar. 9-13. San Jose Convention Center, San Jose, CA. Contact JoAnn Galluzzi (847) 509-9700; Internet: http://www.ipc.org.

European Design & Test Conference (ED&TC 97), Mar. 17-20. CNIT Conference & Exhibition Centre, Paris-La Defense, France. Contact ED&TC Conference Secretariat, CEP Consultants Ltd., 43 Manor Pl., Edinburgh, EH3 7EB, UK; (44) 131-300 3300; fax (44) 131-300 3400; e-mail: edtc@cep.u-net.com.

Communication Design Engineering Conference, Mar. 24-26. Washington, DC. Convention Center, Washington, DC. Contact Denise Chan, Miller-Freeman Inc., (415) 278-5231.

Sixth International Verilog Conference, Mar. 31-Apr. 2. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: ivcinfo@ivc-conf.com.

APRIL

INTERMAG 97, Apr. 1-4. Hyatt Regency Hotel, New Orleans, Louisiana. Contact John Nyenhuis, School of Electrical Engineering, Purdue University, West Lafayette, IN 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: nyenhuis@ecn.purdue.edu.

IEEE International Reliability Physics Symposium, April 7-10. Adams Mark Hotel, Denver, Colorado. Contact IRPS Publishing Services, P.O. Box 308, Westmoreland, New York 13490; (315) 339-3971; fax (315) 336-9134; e-mail: 103227.2074@compuserve.com.

IEEE Conference on Computer Communications (INFOCOM 97, Apr. 7-11. Kobe, Japan. Contact Tatsuya Suda, Dept. of Information & Computer Science, University of California, Irvine, CA 92717-3425; (714) 856-5474; fax (714) 856-4056; e-mail: suda@ics.uci.edu; Internet: http://www.ics.uci.edu/infocom/ (North America); http://arpeggio.ics.es.osaka-u.ac.jp/infocom.html (Japan).

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 97), Apr. 21-24. Gasteig Cultural and Convention Center, Munich, Germany. Contact Bernd Girod, Lehrst.f.Nachrichtentechnik, Univ. of Erlangen Nuremberg, Cauerstr. 7, D-91058 Erlangen, Germany; (49) 91-3185-7101; fax (49) 91-3131-30840; e-mail: b.girod@ieee.org.

IEEE International Conference on Robotics and Automation, Apr. 21-27. Albuquerque Convention Center, Albuquerque, NM. Contact Jerry Stauffer, Intelligent Systems and Robotics Center, Program Office, MS0949, Sandia National Laboratories, Albuquerque, NM 87185-0949; (505) 845-8966; fax (505) 844-6161; e-mail: jdstauf@isrc.sandia.gov.

First Convergence Technology & IC Expo, Apr. 22-24. InfoMart, Dallas, Texas. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, California 90045; (800) 877-2668, ext. 243; fax (310) 641-5117.

15th IEEE VLSI Test Symposium, Apr. 27-30. Hyatt Regency Monterey, Monterey, CA. Contact Yervant Zorian, General Chair, Lucent Bell Laboratories, P.O. Box 900, Princeton, NJ 08542-0900; (609) 639-3176; fax (609) 639-3197; e-mail: zorian@lucent.com.

MAY

IEEE Vehicular Technology Conference (VTC), May 5-7. Hyatt Regency at Civic Plaza, Phoenix, Arizona. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, Post Office. Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

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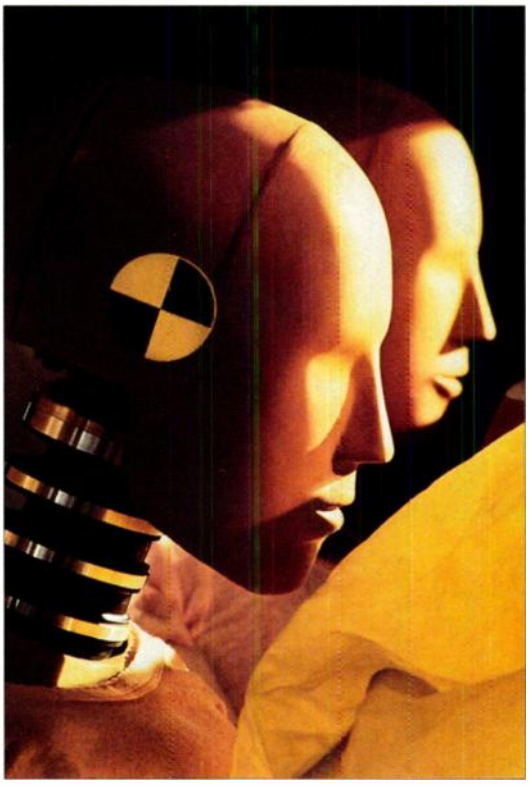

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RESEARCH BASICS

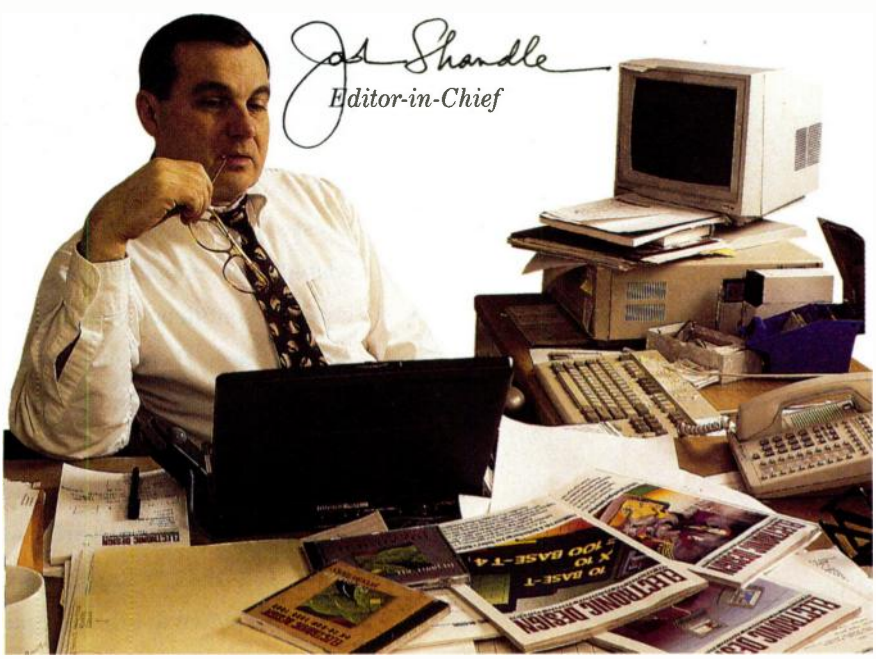
The latest report on research spending in the U.S. confirms the trend we have seen through the 1990s: Less spending overall, and a significant decrease in research and development spending by corporations when measured as a percentage of gross domestic product (GDP). Research has stagnated at the $175 billion range since the decade began, according to the National Science Foundation. Corporate-sponsored research is down. In 1996, it is expected to drop below 1.5% of GDP, which is where we were in 1991.

U.S. spending on basic research has taken a nosedive. Corporation after corporation has said simply that it cannot support basic research and remain competitive. In many circles, this flight from basic research will be taken as an indication of dire times ahead for the U.S. technology industry. Research of the type performed at the former AT&T Bell Labs for more than three-quarters of a century is supposedly the secret sauce that provided the scientific foundation for the explosion in innovative and market-leading technologies and products that spawned a global information revolution. Another significant factor was the programs sponsored by the government through a system of national laboratories and grants from the Defense Advanced Research Agency (DARPA).

Since the economic and legislative factors that play a big role in the decision of how much will be spent on research are unlikely to change, I guess we will just have to wait to see what happens. There is, after all, another side to the argument. While it might be wonderful for Bell Labs to build receiving dishes to listen for signs of intelligence in outer space, for example, did AT&T have the moral right to spend ratepayers' dollars on such a project? Probably not, and AT&T would have not been able to afford such projects, except that it had been granted monopoly power, which is tantamount to the power to tax.

According to this view, universities are the proper venue for basic research. I agree, but there are difficulties there as well. Government funding has been cut back and academic research often depends on graduate students for manpower, and they come and go in a couple of years. In other words, the programs can lack continuity. So there is no easy answer. One thing that would help, though, is a well-defined technology leadership policy with bilateral support in the Congress. *jshandle@class.org*

Jd Shandle
Editor-in-Chief



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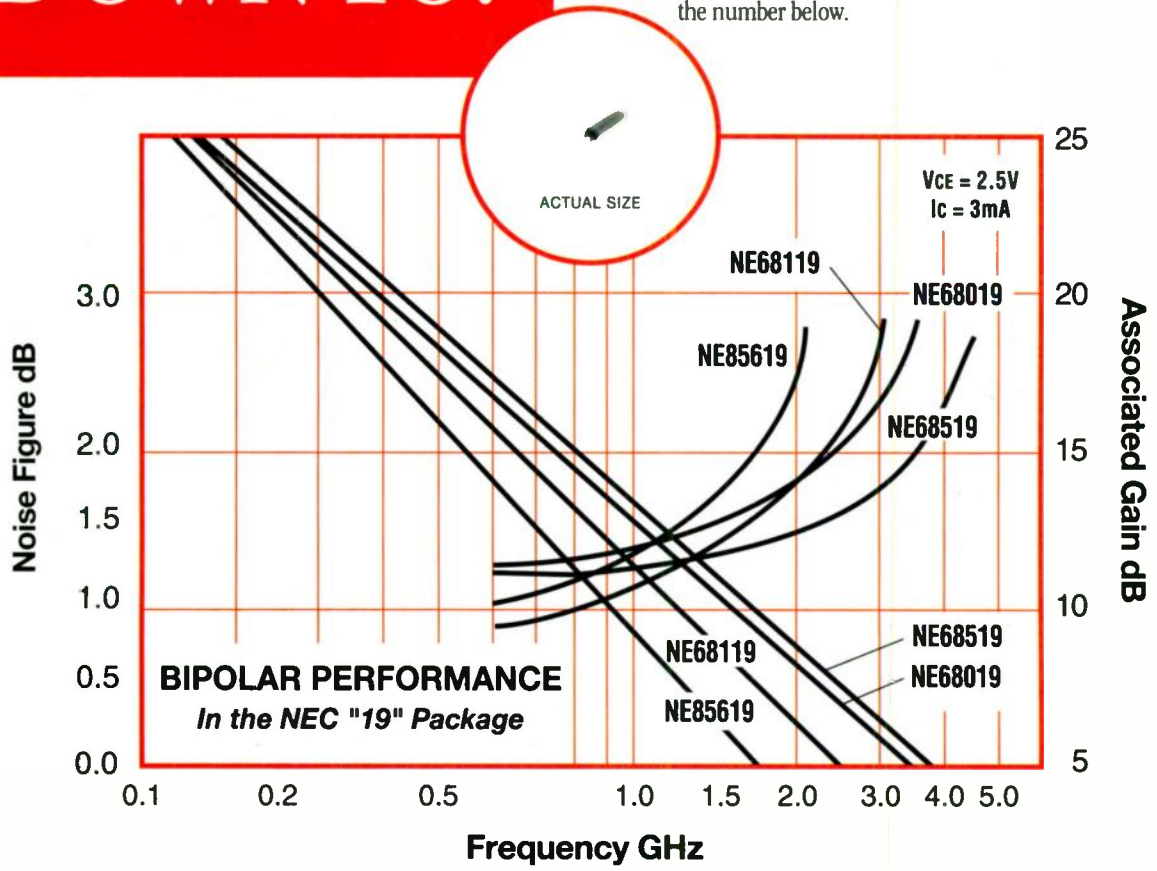

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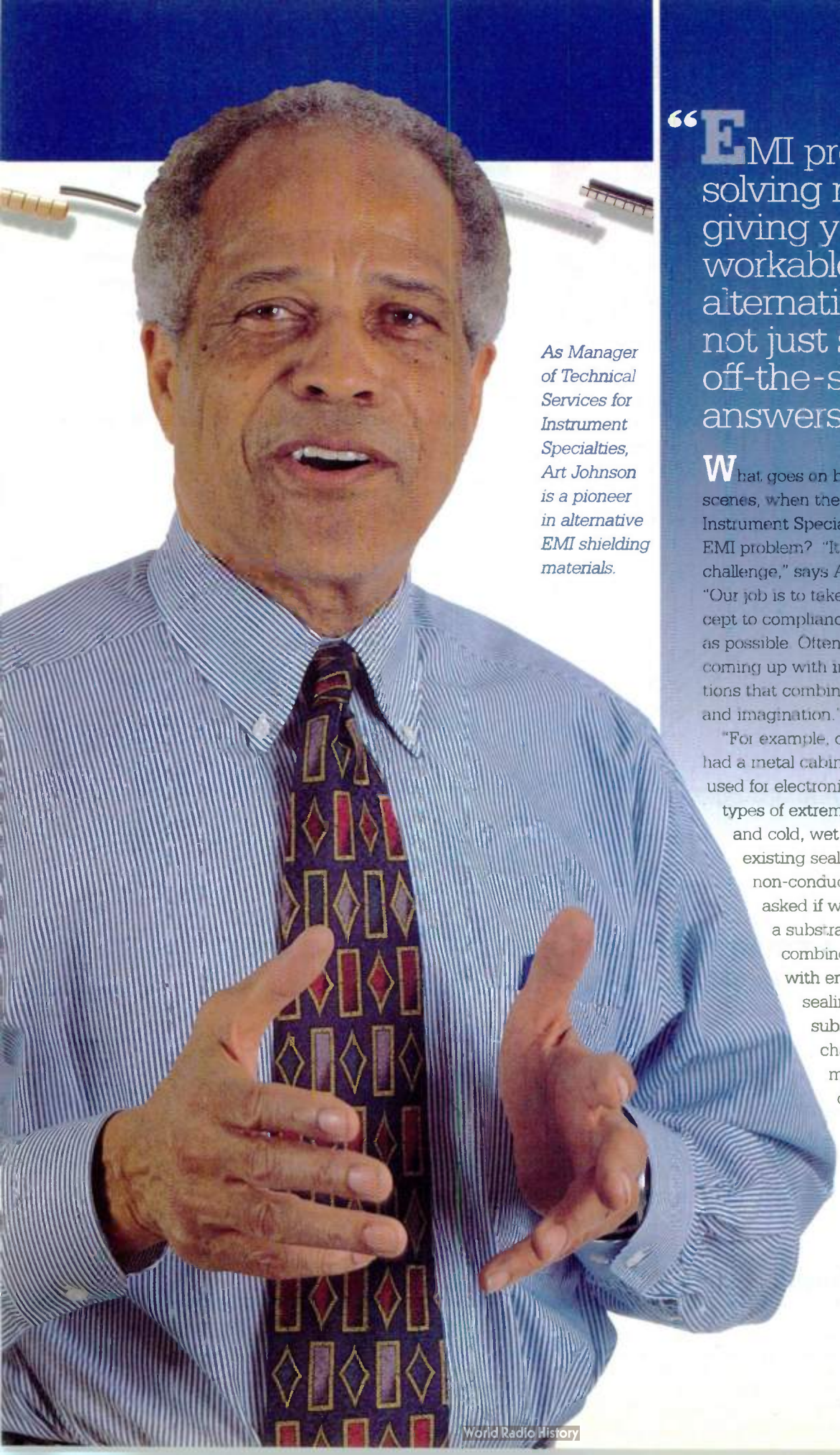
READER SERVICE 139



As Manager of Technical Services for Instrument Specialties, Art Johnson is a pioneer in alternative EMI shielding materials.

"EMI problem solving means giving you workable alternatives, not just some off-the-shelf answers."

What goes on behind the scenes, when the people of Instrument Specialties solve your EMI problem? "It all starts with a challenge," says Art Johnson. "Our job is to take you from concept to compliance as efficiently as possible. Often that means coming up with innovative solutions that combine practicality and imagination."

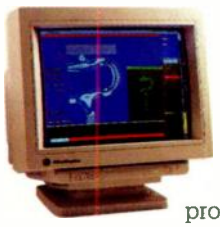
"For example, one customer had a metal cabinet enclosure, used for electronic circuitry in all types of extreme climates, hot and cold, wet and dry. The existing seal was a clip-on, non-conductive type. They asked if we could develop a substrate gasket that combined EMI shielding with environmental sealing — without substantially changing the mechanical design."

LEADING THE WAY IN SHIELDING SOLUTIONS

Customer Response Team goes into action.

Instrument Specialties' Ed Stevens, Linda Hickey, and Gary Meixell — one of our many Customer Response Teams — saw this as an excellent application for an extruded conductive elastomer gasket, anchored by a thin, stamped and formed metal clip-on component.

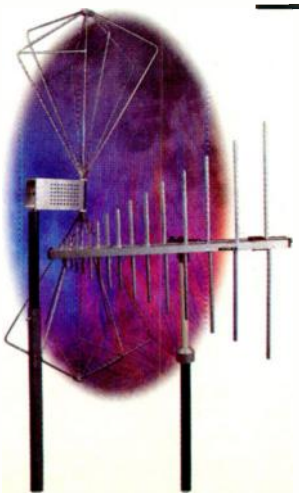
They gave a concept sketch to Bill Stickney and Dan Retz, our Finite Element Analysis (FEA) Team, who turned it into a computer model. "We wanted to know the profile characteristics when the seal was deflated to 50% of its free height," Stickney explains.



From model to prototype.

The FEA Team's model helped us develop a profile with the right spring properties to retain the completed assembly, while staying flexible enough to bend around a 2" radius corner.

This information was then downloaded to the Instrument Specialties Tool Design Group,



where extrusion and stamping dies were created. Once the tooling was finished, a prototype was made and submitted to the customer. They evaluated it for environmental protection, while Instrument Specialties looked at the shielding and compression force characteristics.

Passing the tests.

At our state-of-the-art EMC Compliance Center, Instrument Specialties simulated in-use conditions of the clip-on shield with the help of special fixtures fabricated by our tool shop.

"We performed EMI tests from 30 MHz to 1 GHz," says Ed Stevens, Project Engineer. The results? "We showed 86 dB at 800 MHz average shielding effectiveness, and a 50% deflection force of 8 lbs. per linear foot. The product also withstood a 70-mph rain drip test when it was installed in an enclosure." Mission accomplished!

We can do the same for you.

This is just a single example of a problem solved by one of our many Instrument Specialties teams. With over 550 people, more than 50 years of experience, the industry's widest range of products and services, plus our worldwide support capabilities, we can offer you the same expertise.

Whether you need analysis, design, fabrication, or testing — or a complete concept-to-compliance program — call Instrument Specialties. For a free guide to our EMI/RFI products, please call, write, or fax us today.

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READER SERVICE 130

More Power!

In her first eight weeks on the planet, Anwyn, our new daughter, has transformed the lives of all the people she has touched. Her gentle smile has turned my normally isolated family into a close-knit clan, our friends into attentive aunts and uncles, and both of our moms into raging grandmothers. Anwyn also has worked her magic on her parents, transforming us from hard-working, hard-playing, busy professionals into sleep-deprived morons who spend the little energy we have left at the end of a day cheerfully babbling and cooing over our daughter, or gloating to each other about how cleverly she drools. We're so numb and tired that we consider watching "Home Improvement" on the television an intellectual challenge.

So, there we were, watching Tim and Al turbocharge a food processor, when I nudged Catherine and complained about the ridiculous male stereotypes that the show was foisting upon the American public. "Actually," she said, "I think they're quite accurate." I began to protest, but she continued. "It seems like most of the guys I've ever known have this powerful urge to take something that works perfectly well and 'improve' it to the point of uselessness." She had me there. I suddenly had this image of Bill Gates in a plaid shirt, hunched over his computer, hooting, "MORE POWER!"

LEE GOLDBERG
COMMUNICATIONS

Pressing the point further, she asked "What about that intelligent vehicle highway system you're so excited about?" Intimidated, I used the standard defense: "Honey, IVHS is a very sophisticated system that will revolutionize transportation in America." "Sure," she said. "A multibillion dollar initiative to computerize highways for cars that run on a rapidly disappearing fossil fuel! Isn't that a bit like polishing the fire extinguishers on the Hindenburg? What if we invested the same amount of funding into developing alternate fuels, hybrid electric vehicles, and public transportation? Besides who the heck actually benefits from all this stuff?"

I had to think. It certainly doesn't look like John or Jane Q. Public will benefit much from smart highways. Seems to me that we'll become even more dependent on increasingly expensive cars that will continue to dump crud into the air and consume our dwindling petroleum reserves. Real smart, huh? I figure that the folks who will really benefit from smart highways are the mega-corporations that will build and use them. It's not surprising that the prime backers of the IVHS program are automobile manufacturers, but if you look in the fine print you'll also find TRW, Lockheed Martin, Texas Instruments, Hughes, Westinghouse, and other aerospace manufacturers—the same folks who brought you $600 toilet seats and weapons systems that never worked.

If I didn't know any better, I'd say that the entire IVHS program is a gigantic handout to the defense industry to make up for the downturn in weapons sales. Whoa! Wait a minute! Isn't the country taking a hard line on welfare reform? What about reforming corporate welfare too? It costs us much more than social welfare and doesn't even feed or educate children.

I've seen my tax dollars at play and it's appalling. In my own backyard, Lockheed-Martin is getting over $1.6 billion in government subsidies to close down the spacecraft plant where I used to work in Hightstown, New Jersey. Somehow, the wizards in the boardroom have figured out how to use our tax dollars to subsidize the layoffs of over 2500 people while they move the entire operation to their less-profitable facility in California!

Wouldn't these funds be better invested in our future by having those 2500 engineers tackle some of the challenges we'll be facing in the next century? *But nooo!* Instead, we have Norm Augustine, Jack Welch, Dan Tellep, and the other corporate vampires in their plaid shirts hooting "MORE POWER!" It makes me sick. I'd do something about it, but I'm too exhausted taking care of Anwyn. Besides, "Home Improvement" is on in five minutes. I gotta go. *leeg@class.org*

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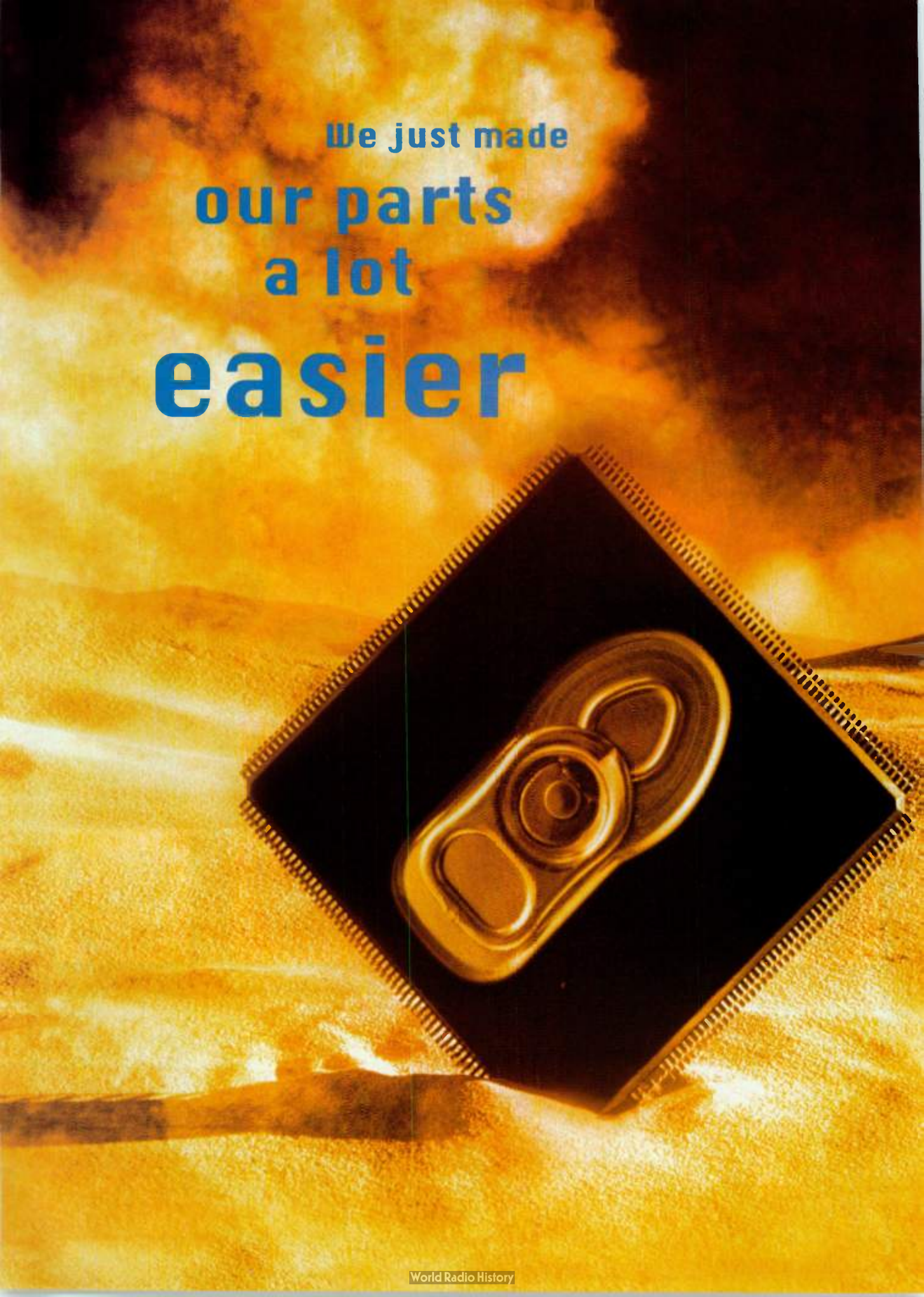

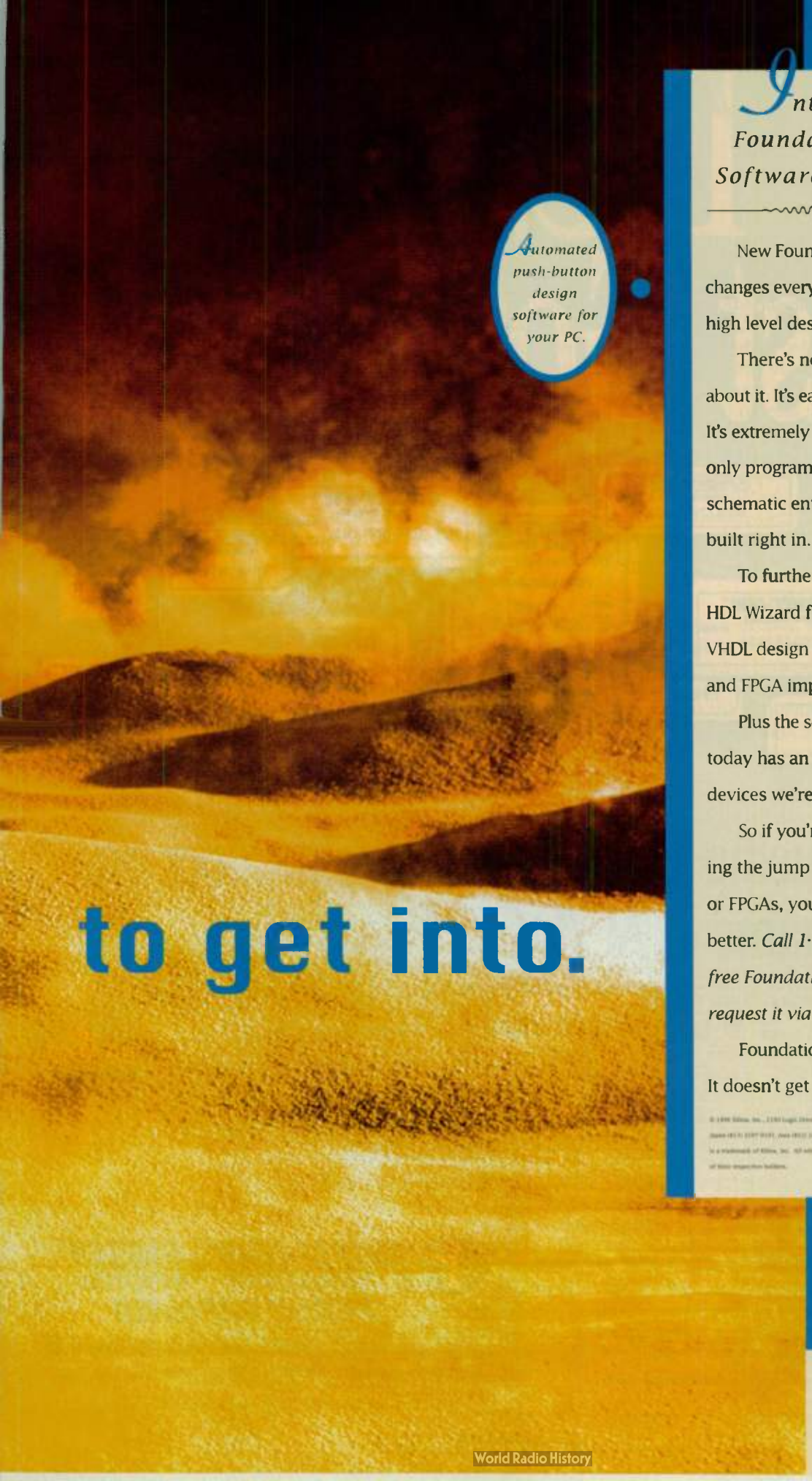

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READER SERVICE 132

ION-BEAM SYSTEM CUTS THIN-FILM DEFECTS 300K-FOLD

An advance in ion-beam deposition technology has brought about a 300,000-fold reduction in defects in multilayer thin films for next-generation semiconductors and thin-film magnetic heads that require defect-free, particle-free environments. The breakthrough was achieved by the IBD-350, a new ion-beam sputter deposition system created by Veeco Instruments Inc. in association with the Lawrence Livermore National Laboratory during its advanced extreme-ultraviolet (EUV) lithography joint development project. Current methods to make EUV multilayer masks employ a technique called magnetron sputtering, which produces about 10,000 defects in a square centimeter. The IBD-350 yields only three defects in 100 square centimeters, thus the 300,000-fold improvement. Ultimately, for the hard-disk drive market, the system will enable the production of next-generation thin-film magnetic heads with greatly increased areal density. As for the semiconductor market, chip manufacturers may be able to build ICs with feature sizes of 0.1 μm and below that are 10 times faster and have 1000 times more memory than comparable chips. For more information, contact Veeco Instruments Inc., Terminal Dr., Plainview, NY 11803; (516) 349-8300; fax (516) 349-8321. *RE*

CABLE MODEM SUPPLIERS SEEK COMMON SPECIFICATION

Five cable modem manufacturers have provided system submissions to the cable television's data-interface specifications process to try to ensure the delivery of an interoperability standard by the end of 1997. Cable Television Laboratories Inc. (CableLabs) is heading up a collaborative effort by many of the nation's major cable operators to generate an open, non-proprietary specification for cable modems ahead of the IEEE's slower-moving effort to deliver the 802.14 standard. The industry specification is anticipated to be published by year's end, with rollout and testing of the first interoperable products targeted for 1997. The suppliers with which the initiative will work include, but aren't limited to, Com21, General Instrument, Hewlett-Packard, LANcity, and Motorola. After the completed specifications are published, modem suppliers are expected to transition their manufacturing to systems that adhere to the new specifications by the end of 1997. For further information, contact CableLabs, 400 Centennial Pkwy., Louisville, CO 80027-1266; (303) 661-9100; fax (303) 661-9199; Internet: www.cablelabs.org. *LG*

SOFTWARE SENDS IMAGES OVER WEB 2 TO 4X FASTER

Congestion on the Internet creates on-line traffic jams that cause fragments of images to be lost in transit. Missing pieces then are retransmitted until the image is complete, resulting in eroded efficiency due to considerable transmission delays. Researchers at Dartmouth College, Hanover, N.H., have come up with a system that speeds up Internet image transmission by a factor of 2 to 4 over the current TCP method while maintaining images of similar overall quality. Dartmouth's system uses "forward error correction," a technique that allows the recipient of an image to reconstruct fragments lost during transmission. Forward error correction is added to an image while it's being compressed, thereby it concentrates on the portions of the image that have the greatest visual impact. Image fragments lost during transmission have little noticeable effect, and no time is wasted on retransmitting lost fragments. Contact Alla Kan, Associate Director, Technology Transfer Office, Dartmouth College, 6210 Raven House, Hanover, NH 03755; (603) 646-3027; fax (603) 646-3670; Web: http://www.cs.dartmouth.edu/jmd/decs/. *RE*

IVA ADOPTS MINIATURE CARD SPECIFICATION

The Miniature Card specification added another to its growing list of supporters. The International Voice Association (IVA), established by Grundig AG, Olympus Optical Co., and Philips Speech Processing, jointly developed a digital speech standard based on the Miniature Card spec to make sure that digital audio recording devices are fully compatible with one another. The speech standard also ensures that they can use the same transportable media for all products. Overall, the Miniature Card specification describes a card that can be used to store and exchange image, text, and voice data. Among its attributes are: a flexible design that can accommodate up to 64 Mbytes of flash, ROM, or DRAM memory; a rugged, pinless connector well-suited for consumer use; and a form factor measuring 38 by 33 by 3.5 mm for minimized card footprint. According to Alan Hanson, chairman of the Miniature Card Implementers Forum (MCIF), "Adoption by a major industry organization like IVA establishes the Miniature Card as the standard for the digital audio recording industry and opens the door to a host of new possibilities." For more information, contact MCIF at (916) 356-7060; or on the Web at http://www.mcif.org. *RE*

Edited by Roger Engelke

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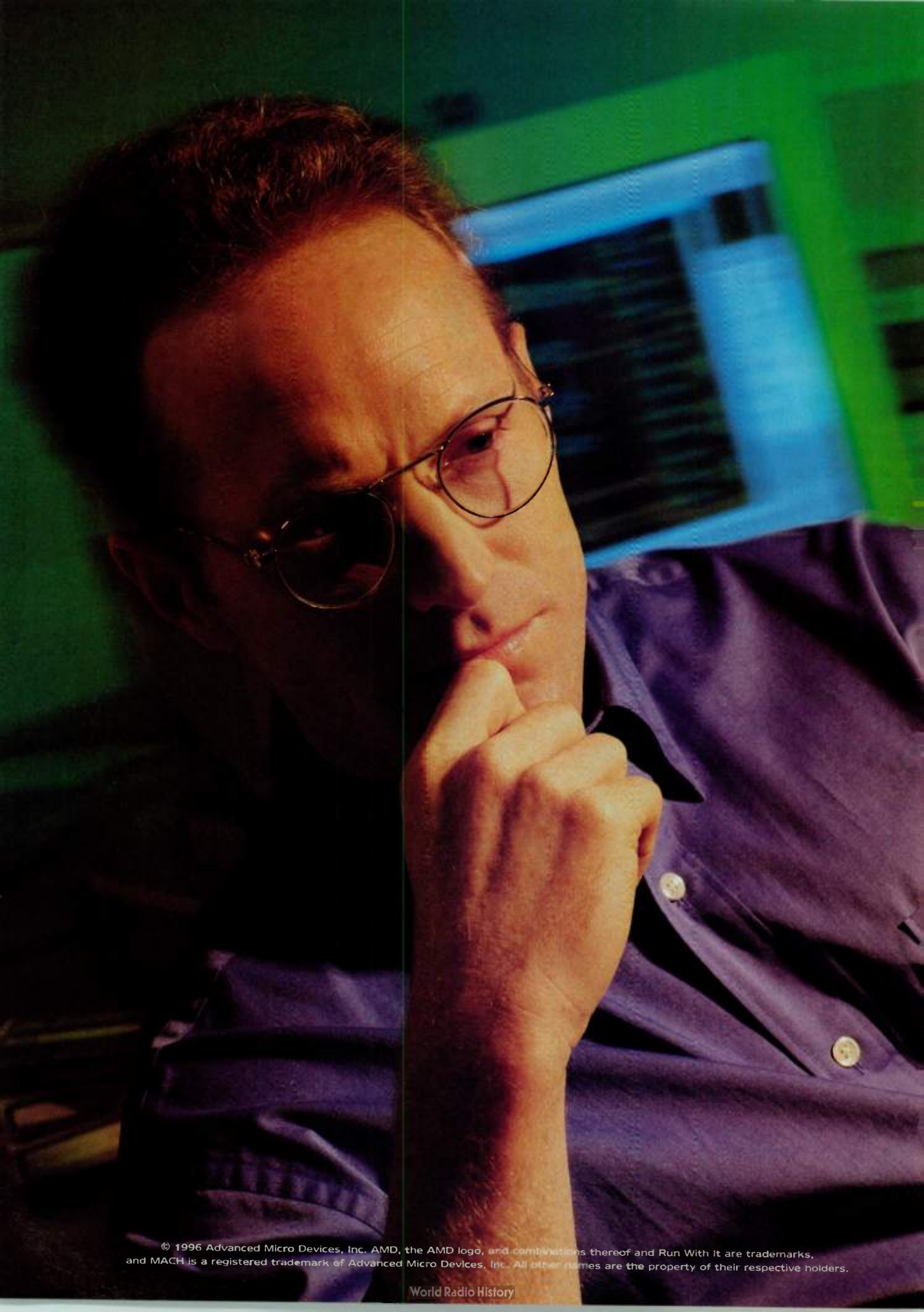

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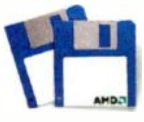

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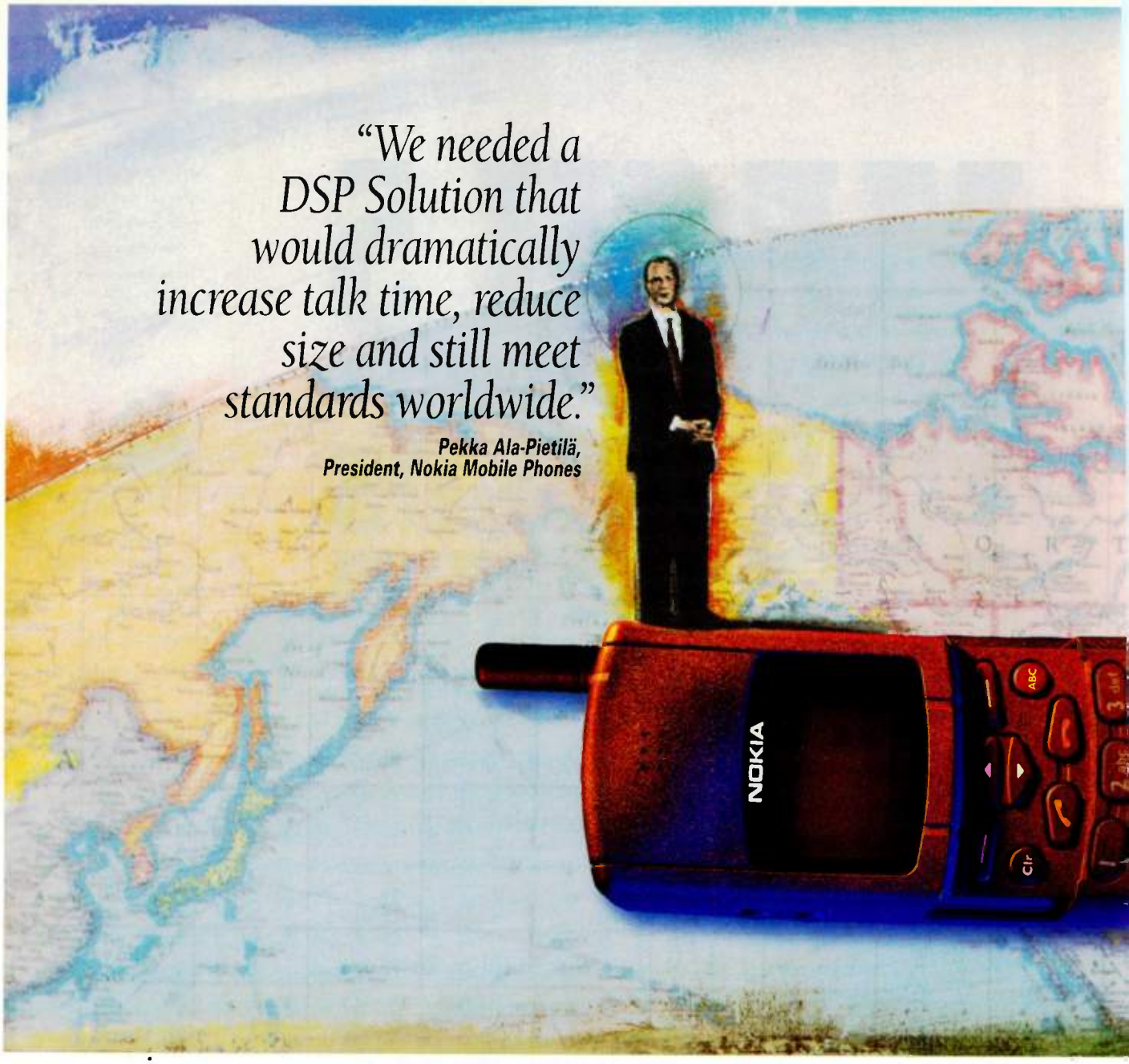

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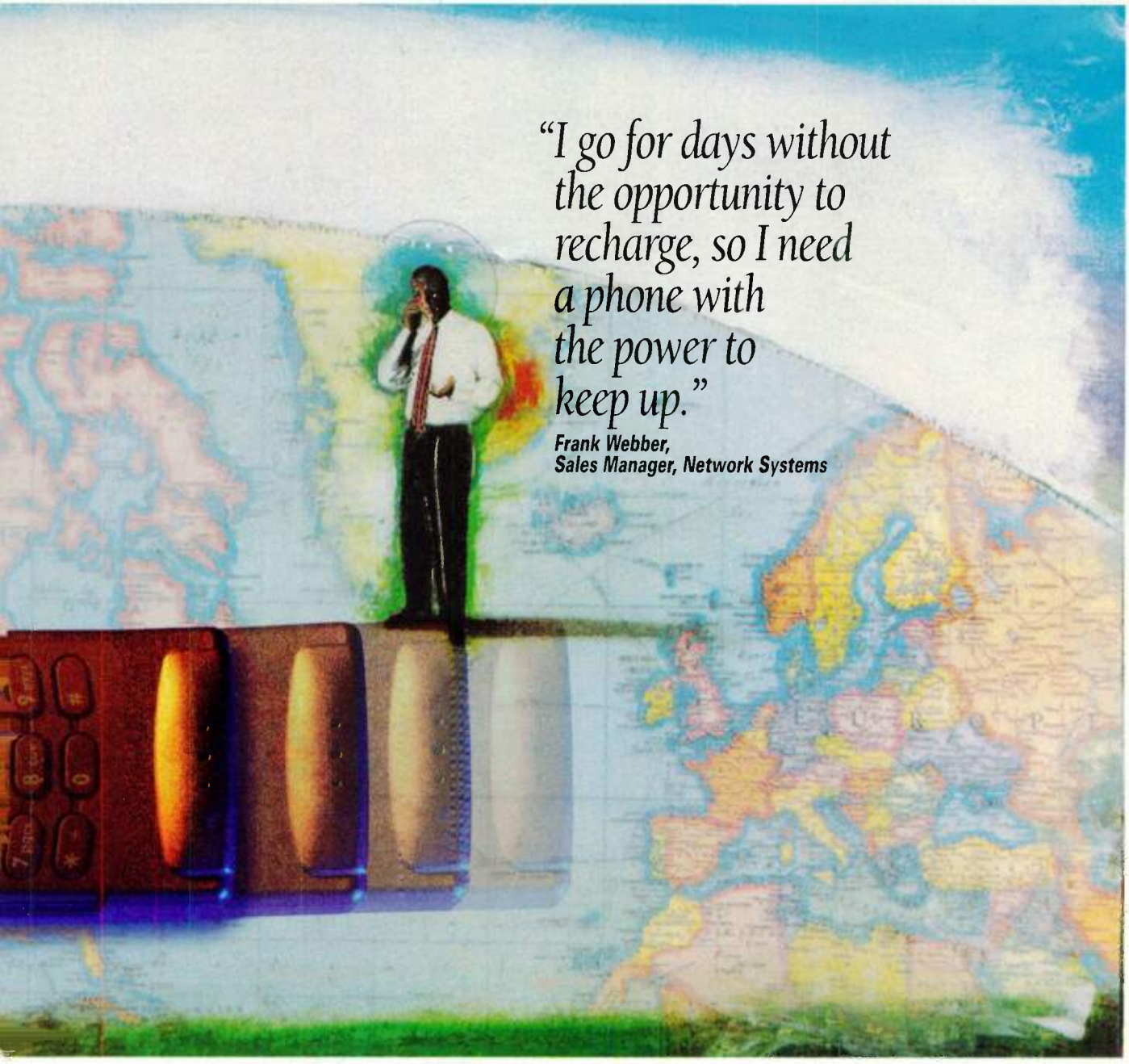

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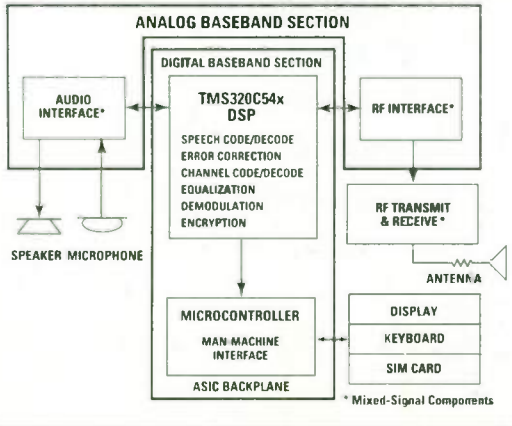

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FIELD-PROGRAMMABLE ANALOG IC ALLOWS EASY DESIGN OF COMPLEX ANALOG SIGNAL PROCESSORS

Designing analog circuits is becoming a lost art, according to David L. Grundy, a visiting professor at two British universities, Huddersfield University and The University of Manchester Institute of Science and Technology, where he lectures on linear circuit design. He reckons that the number of engineers around the world that can design large-scale integrated analog circuits can be counted in the hundreds rather than the thousands. Yet, Grundy declares, analog signal processing offers a number of advantages over digital techniques.

"Analog signal processors are faster because there is no analog to digital conversion, sampling, and digital to analog conversion. They will consume less power because fewer transistors are required. And, they will be lower in cost because the silicon chips are smaller," he claims. The big disadvantage though, is that in using traditional methods, it may take more time and skill to design an analog signal processor. That, he says, is because there are very few design tools that allow a top-down approach to linear circuit design. Grundy says that as a result, most linear circuits are designed from the component level up. This is especially the case for signal-processing systems requiring the implementation of multiplication and division functions.

"While there are traditional analog circuit techniques which can provide high-performance multipliers, they rely very much on component-level behavior, such as the variation of transistor transconductance with operating current," he adds.

Now, Grundy, in collaboration with Zetex plc., Oldham, England, has set out to change that. The company has cast Professor Grundy's theories into silicon, and produced what it calls a field-programmable analog device (FPAD). According to Grundy, the FPAD will become the linear equivalent of FPGAs familiar to logic designers. Moreover, Zetex has developed a software tool that runs on a personal computer under Microsoft Windows, and allows the design of complex analog signal processors in a matter of minutes.

Designated the TRAC 020 (TRAC stands for Totally Reconfigurable Analog Circuit), the FPAD made its first public appearance early this month at the Electronica Exhibition in Munich, Germany. It is slated to enter production in early 1997.

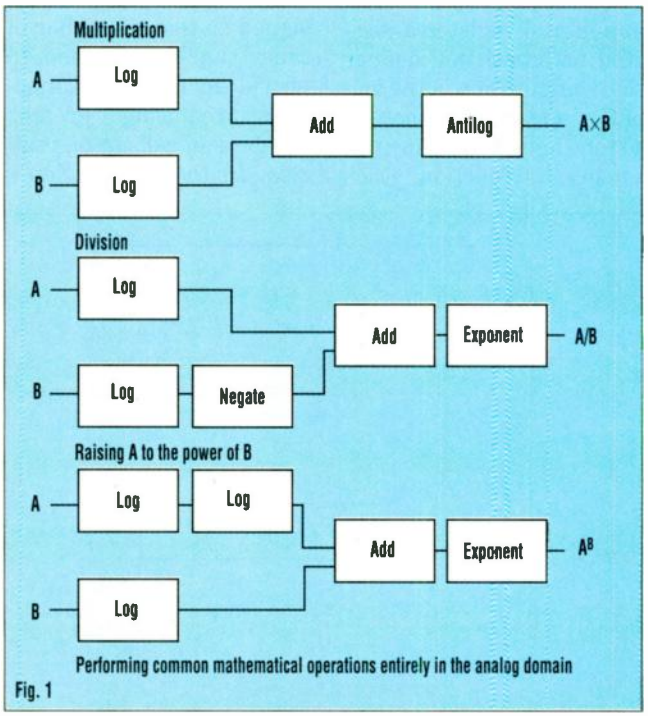
In essence, the device is an uncommitted array of 20 linear cells, each of which can be programmed to perform one of eight predefined functions. It's a biCMOS device, using bipolar circuits for the analog logic functions and digital memory to hold programming data for each of the cells. But, the digital part of the circuit is relatively very small, occupying just 20% of the total silicon area.

Grundy explains that each analog cell requires just three bits to define its function and its interconnection with other cells on the chip for a total of 60 bits. He asserts that the functions required to process signals entirely in the analog domain can be reduced to a set of five mathematical operations—addition, negation, log, antilog, and integration or differentiation with respect to time. He points out that while one of the most common mathematical operations in signal processing is multiplication, it can be readily achieved by logarithmic addition. Similarly, division can be realized by the subtraction of logarithms. Raising a number to a power can be achieved by multiplying a logarithmic value by the required exponent *(Fig. 1)*.

Log and antilog functions can be implemented with relatively simple circuit techniques, Grundy asserts, because of the extraordinarily accurate relationship between voltage and current for a semiconductor junction. He cites the diode equation:

$$I = I_0\{\exp(qv/kT)-1\}$$

where:
I is junction saturation current
q is electron charge
v is the voltage
k is Boltzman's constant



Performing common mathematical operations entirely in the analog domain

Fig. 1

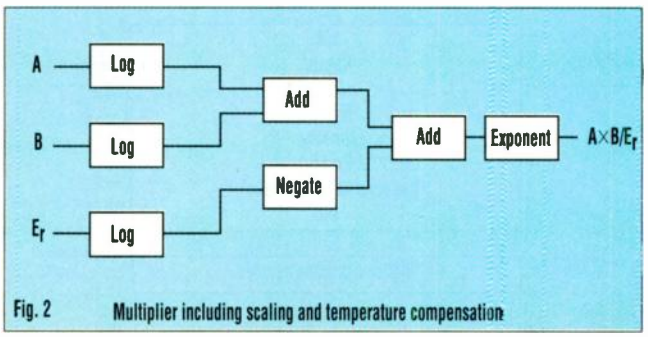


Fig. 2 Multiplier including scaling and temperature compensation

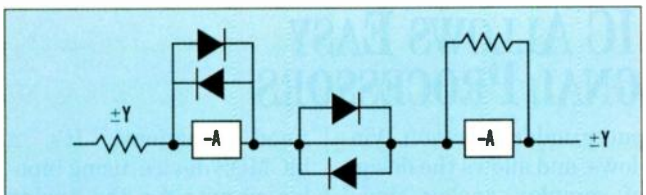


Fig. 3 Log/antilog operation gives output replica of input

and T is the absolute temperature.

This relationship holds over nine decades of current and provides an extremely accurate logarithmic function within the silicon itself. Using the diode junction, however, does require strict control of temperature variations. However, Grundy says that log and antilog functions are complementary and compensate for temperature drift, provided care is taken to ensure that the cells providing these two functions in a given processor layout are located physically close to each other on the silicon array.

Scaling is another problem. "It's not simply a matter of adding voltages across two silicon junctions," Grundy says, "since this could result in excessive currents." To avoid this problem, a portion of the voltage is subtracted in a controlled manner from the logarithmic form of the signal. A practical multiplier configuration is possible using this technique *(Fig. 2)*. A reference voltage, E_r, is introduced, whose logarithm is taken by a silicon junction. This voltage provides both I_o temperature compensation and scaling. Where the diode equation tends to fail is in it's limitation of only accommodating signals of one polarity. However, it is possible to use back-to-back junctions to overcome this limitation, Grundy says.

Such an arrangement is possible where log and antilog functions are performed in succession, ensuring that the output is a temperature-independent replica of the original bipolar input signal *(Fig. 3)*. The end result is a basic analog cell design similar to that shown in *(Fig. 4)*. This design uses both silicon junctions for the logarithmic functions and resistors for voltage-to-current conversion.

Grundy says that as refined for use in the TRAC 020 device, each cell can be represented as an op amp with a small number of components associated with it. The 3-bit binary value held in a digital register associated with each cell defines the configuration of the amplifier and its external resistors and diodes, in turn setting its function. Each cell is, therefore, a self-contained, programmable analog processor *(Fig. 5)*.

In addition to the five basic math functions, the cells can be set to provide precision rectification—by taking the log of a signal and using one-half its antilog—to provide a short-circuit noninverting path, or to turn off. Each cell also can be set in an auxiliary mode, to allow connection with external components such as resistors and capacitors.

On the TRAC 020, the 20 cells are organized in two serial strings of ten. These two strings are initially independent of each other, but cross-connections between cells can be programmed. Grundy says that the TRAC 020 is designed so that a number of them can be cascaded to provide more complex functions requiring greater numbers of cells to be realized. In the future, Zetex plans to make devices with up to 80 cells.

The electrical performance of the device is such that it provides a unity gain bandwidth of 4 MHz with a dynamic range of 80 dB. Noise voltage is 38 nV/$\sqrt{\text{Hz}}$, while total harmonic distortion is 0.02% at 100 mV pk-pk, and 0.08% at 1.0 V pk-pk. Intermodulation distortion is less than 0.1%, and power-supply rejection is 60 dB. Cell-to-cell crosstalk is greater than 60 dB. The input common-mode range is −1.0 to +1.5 V, with an output swing of −1.5 to +0.5 V. Current consumption with all cells on is 30 mA. Temperature drift of the basic cells is 2 μV/°C over an operating-temperature range of 0 to +70C°. The operating-voltage range is ±2.5 V. Packaging is either in a 36-lead SSOP or a 40-lead plastic DIP. The digital part of the circuit can be clocked at up to 10 MHz, which allows the array to be reconfigured in 6 μs.

Software designed by Zetex allows a user to design and simulate the analog application in graphic form, and then send data to the TRAC hardware to facilitate electrical evaluation of the design. Applications for the chip include filters, multipliers, oscillators, voltage-controlled oscillators, phase-locked loops, and arbitrary waveform generators.

Prices have yet to be set, although Zetex says that the part will be priced at a "few dollars." A development kit including software and an evaluation board will be available for a "few hundred dollars."

For more information, contact Zetex plc., Fields New Rd., Chadderton, Oldham, OL9 8NP, U.K.; +44 (0)161 627 5015; fax +44 (0)161 627 5467.

PETER FLETCHER

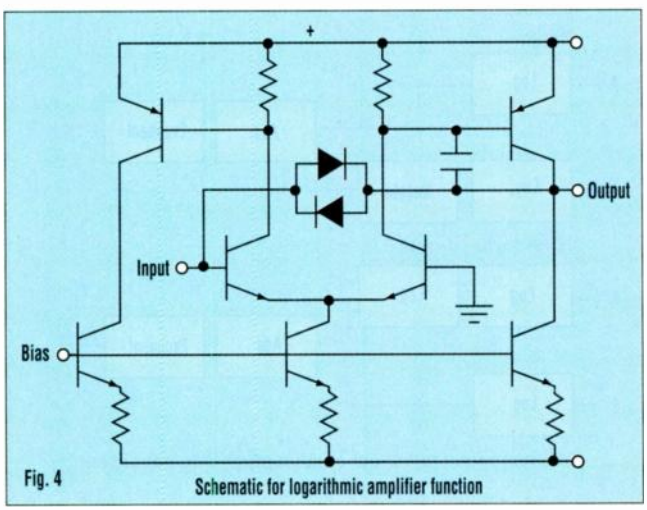


Fig. 4 Schematic for logarithmic amplifier function

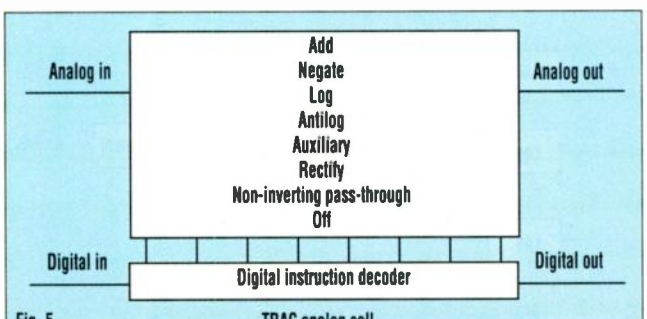


Fig. 5 TRAC analog cell

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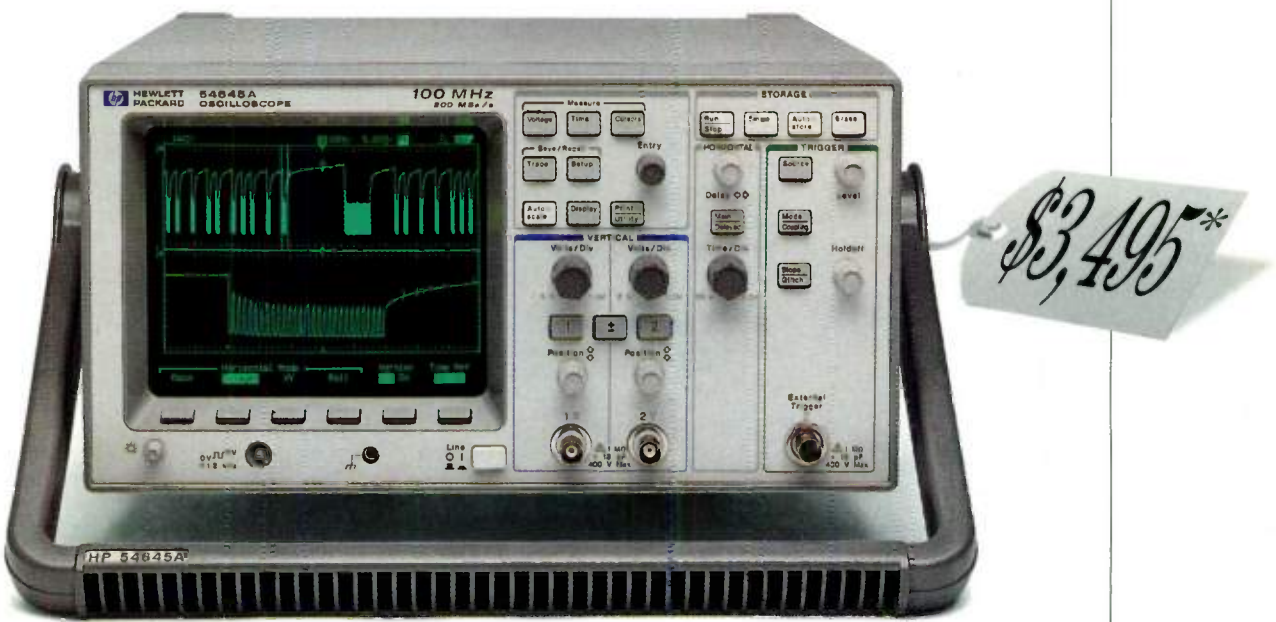

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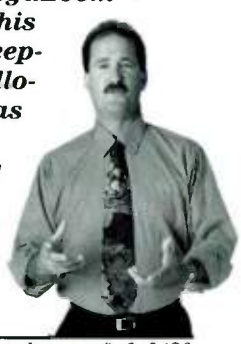

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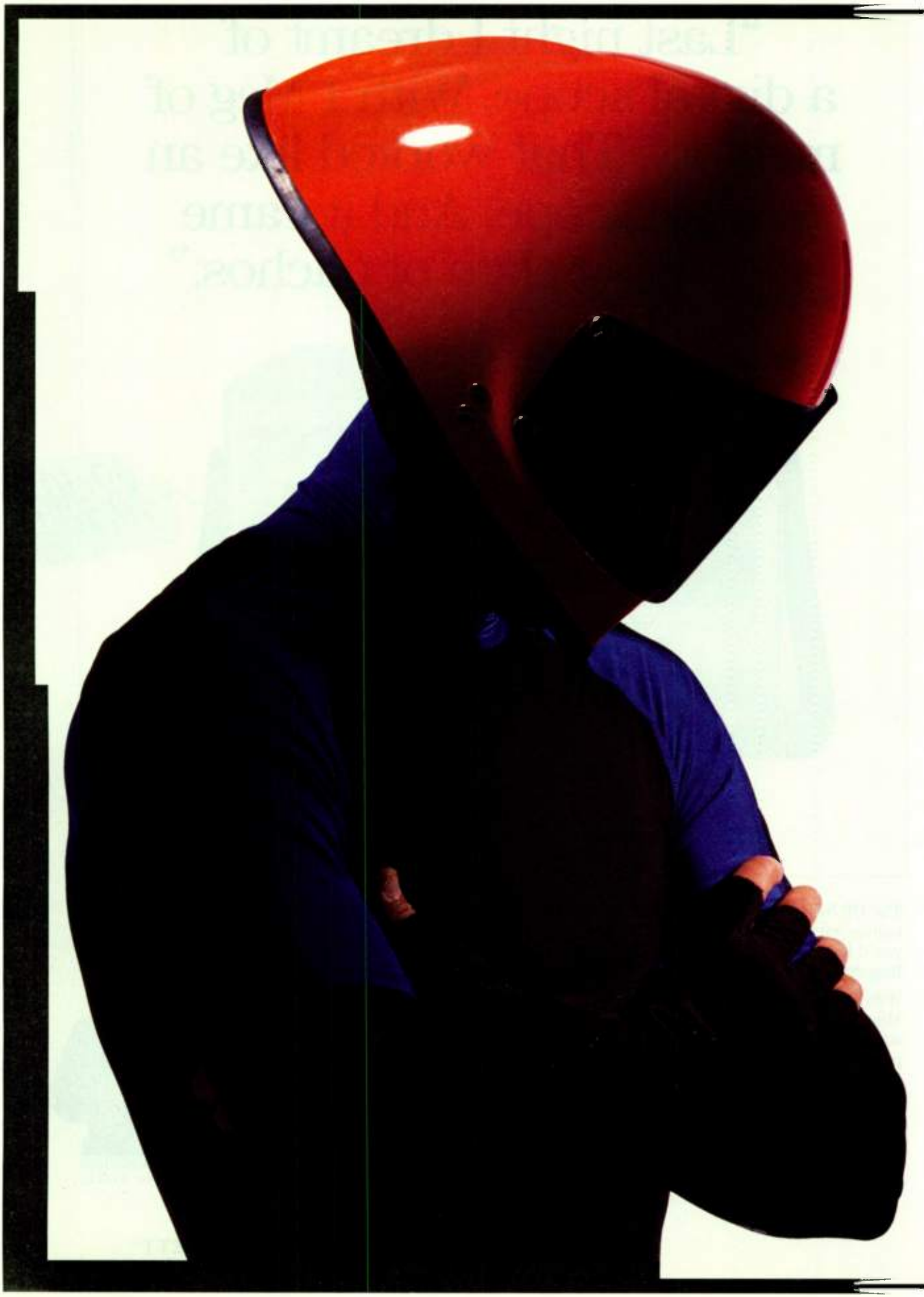

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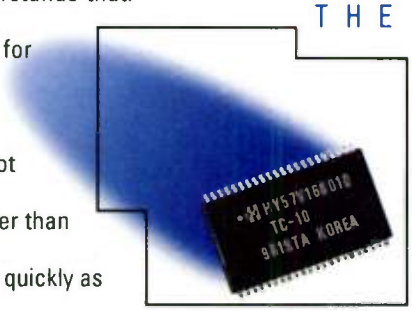

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READER SERVICE 129

AUTOMATIC VERIFICATION AND TEST SYSTEM KEEPS DESIGN PROCESS ON TRACK

Continuously monitoring a product's adherence to design specifications from initial requirements through final implementation can greatly reduce the headaches of final integration and shorten time-to-market. The question is how to do this when a design has been partitioned into hardware and software modules that have been assigned to different teams. Teams tend to focus on the minute problems of their own assignment. Sometimes their workarounds can lead them astray from the overall design specification.

To keep the overall design effort on track, B-Tree Verification Systems, Minneapolis, Minn., has developed an automatic design verification and testing environment. The B-Tree system starts with system requirements that can be used to build functional simulations of software and hardware components. These simulated components can be exercised to verify that they satisfy the functional requirements. Later, as the actual components are developed, they can be substituted for the simulated components and tested.

The B-Tree Verification environment consists of a Windows-based host PC, a simulation-stimulation processor called the "SP box," and a monitoring and capture subsystem to collect system and event data. At the heart of the system is the real-time SP box that initially runs the behavioral modules that define system functionality *(see the figure)*. These modules are derived from target visualization applications that represent different types of peripheral devices and operations. These include keypads, LCDs, port read/write functions, internal data flow, switches and other peripheral functions. Test scripts for the functional models are developed using a scripting language to define the inputs and to compare the actual outputs with the expected outputs.

In addition to its own scripting language, B-Tree has developed a relationship with iLogix that allows iLogix' StateMate functional requirements tool to output test scripts for the B-Tree system. Having a behavioral simulation and the test scripts to fully verify it allows the design to proceed with a functional standard against which to measure progress and compliance with the overall specifications. As hardware is developed, the SP box gradually turns from a simulation processor to a stimulation processor. The SP box has a variety of I/O ports including two RS232 serial ports, an AT and DIN keyboard port, a mouse, rotary knobs, and a touch screen. In addition, there are optional connections for discrete signals including TTL and 8- or 12-bit analog.

As hardware is developed, it can be stimulated in a real-time closed loop under control of a test sequence running on the host PC. As peripheral devices such as keypads or sensors are developed, they can be substituted for their simulation models in the SP box and used in the pass-through mode to directly stimulate the target hardware. It also is possible to set up a mix of target stimulation via actual peripherals and simulated ones. For example, an instrument under development might receive an input from a real keypad attached to the SP box, as well as a sensor input from a simulated sensor. As the design progresses, the SP is increasingly devoted to stimulating the target.

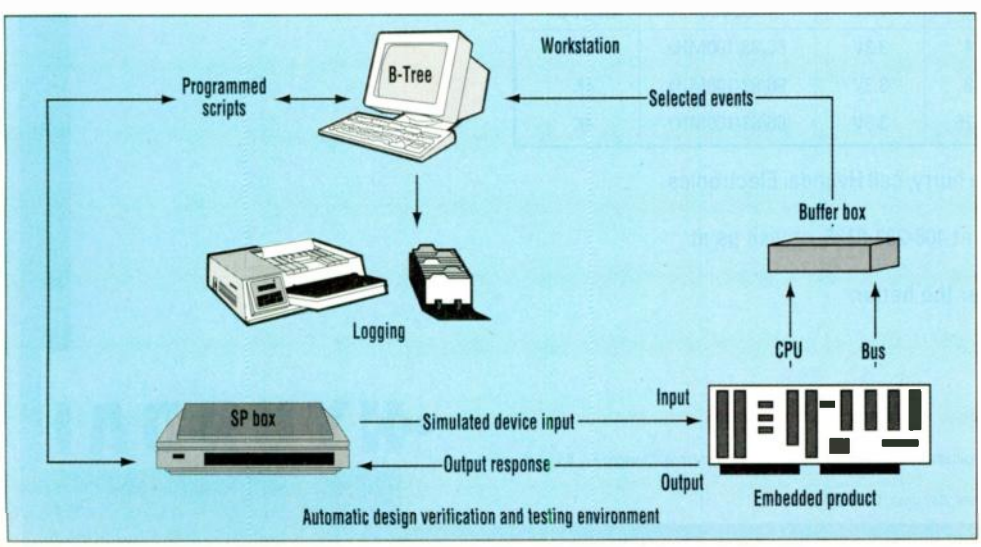
Typically, the main application software is downloaded to the target. Debugging the target during the verification and test process is aided by the monitoring and capture subsystem, also known as the "buffer box." The buffer box captures either the microprocessor signals or the bus signals, or it can be set up to monitor other selected signals on the target system, much like a logic analyzer. To avoid data overload, utilities on the host PC can be used to filter the captured data to display those events of interest.

Tools on the host PC monitor the I/O event stream between target and SP box and the system-level data stream between target and buffer box. The B-Tree environment synchronizes the clocks of the SP box, buffer box and target system, and also timestamps events to a resolution of 1 μs.

If the designer needs a deeper insight into the system's workings, traditional instruments, such as in-circuit emulators and logic analyzers, can be employed. A logic analyzer, for example, can be programmed to trigger on a given event. Comparing the trigger event with time-stamped data from the capture subsystem would enable the designer to correlate the data captures.

For more information, contact B-Tree Verification Systems, 5929 Baker Rd., Suite 475, Minneapolis, MN 55345; (612) 936-7887.

TOM WILLIAMS



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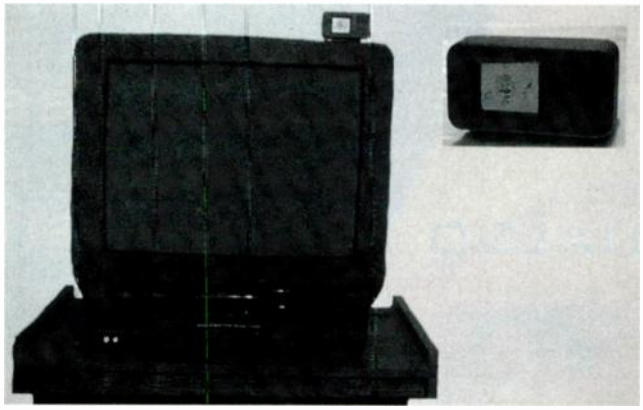
STATIC ELIMINATION TECHNOLOGY RIDS COMPUTER SCREENS AND TELEVISION SETS OF STATIC ELECTRIC FIELDS

Contrary to popular belief, engineers and couch potatoes do have one thing in common: Eye strain caused by staring at a screen that has been charged with static electricity. In fact, anyone who sits in front of a screen for any length of time can attest to the fact that static is more than just bothersome. Recent studies suggest that static electricity can wreak havoc in a number of ways. For example, airborne dust particles attach themselves to a screen and cause a myriad of health risks ranging from eye strain and fatigue to respiratory problems due to allergic reactions to the dust particles.

But this is only the beginning. The same types of dust particles that are attracted to the screen also are attracted to the electronics behind the screen, which, for example, may have an impact on the lifespan of a computer or television, as well as the brightness of the color images they produce.

According to Kevin Cooter, chief executive officer of UltraStat Inc., Colorado City, Colo., "The same static fields being generated from the screen also attract millions of dust particles into the internal circuitry of the TV (or computer). This dust can cause it to break down much earlier than if the static had not been there."

Until now, there had been no way to completely eliminate the static electricity. Conventional solutions had been reactive, as opposed to preventative. Past solutions have, for example, involved occasionally wiping a screen clear of dust instead of finding a way to inhibit its collection from ever occurring.



UltraStat believes it has a solution to the problem. It has developed a system consisting of a black box with an LCD. The system uses a patented static elimination technology that virtually eliminates static from both computer and television screens, and at a cost that makes it accessible to just about everyone. It does this by effectively eliminating the static field between the viewer and the television. With this force removed, airborne dust particles and other contaminants are no longer attracted to the television or the viewer.

Key to the system's operation is a conducting film that contacts the screen's surface along with the black box/LCD module. The module houses a series of resistors and associated electronics. Together, the two components form a pathway that transports the static charge from the screen on the television set to ground.

During operation, the black box is located on top of the television. A velcro strap is affixed to the television and connected to the black box/LCD module by a wire. The conductive film is applied to the screen on the television via a static-conducting spray that is sprayed directly onto the screen's surface. When the television is turned on, the film "encourages" the charge to migrate toward designated pick-up points located at the velcro strap. The electronics in the black box/LCD module then pulls the static electricity in through the connecting wire and subsequently through the series of resistors to ground. When the static electricity and radiation have been eliminated from the television set, the LCD lights up to alert the viewer that the product is working properly.

Static electricity is not only eliminated in a seemingly quick and effortless manner, but there are other significant benefits. Most apparent is the system's ability to prevent dust-particle (PM10 particle) collection and the alleviation of the health risks associated with exposure to static electricity. The lifespan of the television also is increased, and there is a noticeable improvement to the brightness of the pictures displayed on the screen. This benefit is possible because the static elimination technology helps to stabilize the color guns inside the set, allowing for brighter colors on the screen.

Furthermore, because the trajectories of the PM10 dust particles are influenced by the electric fields between a television and the viewer, the same buildup of dust found on the television screen also can occur on a viewer's face. But since the static elimination technology effectively cuts off this field, there is no chance of the particles building up on the viewer's face.

UltraStat sells two products that employ static elimination technology. The first, ClearView, specifically targeted for use with televisions, can be easily installed on any set regardless of brand or size *(see the figure)*. Because it's a passive device, it does not require any batteries or an external power supply.

A similar device, the UltraStat FST, is specifically designed for use with computers. It operates the same way as ClearView with one major exception: A small wire comes out of the device and loops around to actually contact the computer screen. In ClearView, the device simply rests on top of the television. Both devices are currently available at a number of retail outlets nationwide.

ClearView, the most recently released of the two products, has an estimated street price of $29.95. For further information, contact the company at (800) 460-STAT.

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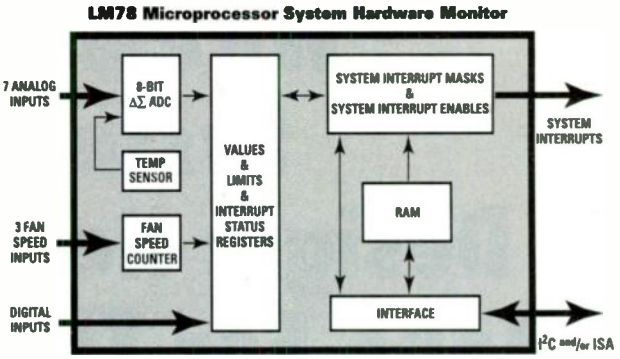

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Wireless System Design: New Hope For The RF-Challenged

Recent Developments In Advanced Design Tools, Techniques, And Components, Are Making RF System Design Easier.

LEE GOLDBERG

The rapid infiltration of wireless technology into everyday life has caught many engineers by surprise. For many of us, RF design has remained an unknown territory, shrouded in mystery, with the murky equations found only in senior-level engineering courses. Until recently, most of us contented ourselves with reveling in the mysteries of 1s and 0s or low-frequency analog design, leaving RF systems to the elite few who didn't sleep through Fourier, LaPlace, Maxwell, and Gauss back in college.

The bad news is that the exploding demand for communications-oriented products means that the "RF-Challenged", will be finding themselves working with one sort of wireless technology or another. The good news is that the cavalry is on the way. It's coming in the form of easier-to-use integrated RF building blocks and more powerful RF-oriented design software. Novice RF engineers also will discover that standards-based systems, innovative architectures, and new design methodologies are making their lives less angst-ridden and more productive.

A DIFFERENT WORLD

The world of RF designers is different from the one occupied by those folks designing digital, or even low-frequency analog systems. One major difference is that many effects that are dealt with by using rough approximation, or even ignored at low frequencies, start playing increasingly dominant roles in the RF spectrum.

Impedance matching between components becomes a challenge at higher frequencies. The impedance of different devices can change significantly. It also can change in a non-linear fashion over each device's operating band, forcing engineers to resort to sophisticated matching networks. Even the circuit traces on the pc board take on a life of their own, forming inductors and capacitors. They add complex networks that keep a circuit from behaving anywhere near where your calculations expected it to be.

Dr. H. S. El-Ghoroury, president of ComQuest Technologies, Encinitas, Calif., explains, "At RF frequencies, the actual circuit elements may change their value depending on what surrounds them. Circuits can display an inconsistent susceptibility to other signals in their vicinity. This susceptibility can be a nonlinear function of frequency, temperature, voltage, humidity, etc." El-Ghoroury continues, "RF circuits emit energy as well, causing additional problems. These parasitic effects are difficult to model since there are so many contributing factors which most modeling tools do not yet address. Parasitic interactions often force designers to "tweak" their circuits' values, grounding and shielding schemes, and, in some cases, adjusting the entire architectures and associated circuit designs. This is especially true when RF designs are integrated with other circuitry." He also cites imperfect circuit operation (leakage from local oscillators, reverse isolation in amplifiers, and capacitor equivalent series resistance) as sources of unanticipated problems in first-pass designs.

The issues involved with RF design are complex enough

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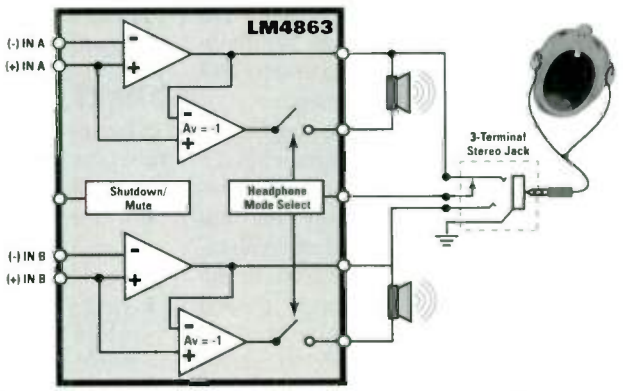
KABOOM.

(Including headphone driver)

INTRODUCING THE LM4863 BOOMER® 1.5W STEREO AUDIO AMP (THE MOST BOOM YOU CAN GET FROM A 5V SUPPLY).



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Introducing the **LM4863.** It's a bridged stereo audio power amplifier that delivers a booming 1.5W per channel to stereo speakers and 75mW per channel to stereo headphones from a 5V supply.

Like every other Boomer, the LM4863 gives you big sound, but very little of the things you don't want. For instance, unique turn on transient suppression circuitry virtually eliminates pops and clicks. It operates on supplies as low as 2.7V. And it consumes as little as 11.5mA, or 0.7µA in shutdown mode. What's more, it costs about half of the next best solution.

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that it usually takes 10 to 15 years to get up the steep side of the learning curve. Happily, the RF market has suddenly become a gold mine for vendors of products that will make life easier for people who are suddenly confronting the wild world of wireless for the first time since college.

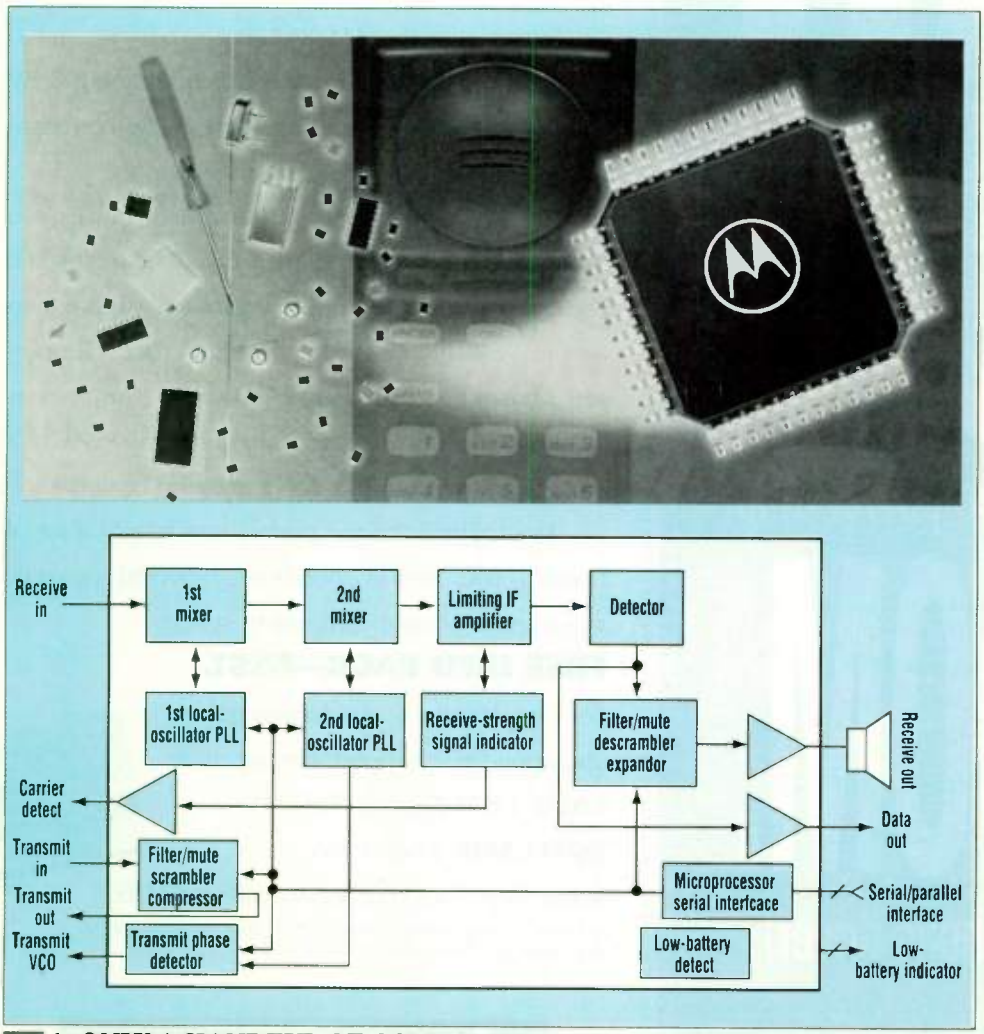
For the many otherwise-competent engineers who are "RF-challenged," it's nice to discover that today's products are beginning to show the high levels of integration and specialization that eliminate at least some of the most punishing low-level design work. This feeling is akin to how we rarely worry about individual transistors when designing large arrays of digital logic. RF design tools are evolving fairly quickly, for both integrated and printed circuits. Finally, RF design practices are changing rapidly—a result of digital signal processing becoming increasingly common, standards-based products streamlining the design process, and reference designs being used on a regular basis.

SMART COMPONENTS

Two of the most important developments in RF components are the drive toward higher levels of integration in high-frequency devices, and the migration of digital technology toward the antenna. Digitization has been playing a major role in many of today's wireless designs already, since the technology is required to support the complex protocols accompanying a portion of today's wireless standards. For example, microcontrollers have been used to control the user and network interfaces in analog cellular telephones for the past decade. But, the new generation of digital PCS and cellular handsets uses digital signal processing for speech compression/decompression, encryption, and baseband I/Q modulation as well.

This high degree of integration is especially useful in the manufacture of high-volume products. Items such as cellular and cordless telephones, and wireless LAN equipment benefit from the technology because their product development costs can be spread over hundreds of thousands of units. For instance, Texas Instrument's TMS320C54x line of DSP ICs have an architecture that has been optimized specifically for use in the baseband sections of wireless terminals and base stations. These low-power (35-100 mW) DSP ICs feature 50 MIPS of processing power. Some also have a hard-wired Viterbi decoding accelerator that reduces a Viterbi "butterfly update" to only four instruction cycles. This addition greatly simplifies channel decoding for applications like GSM handsets and base stations.

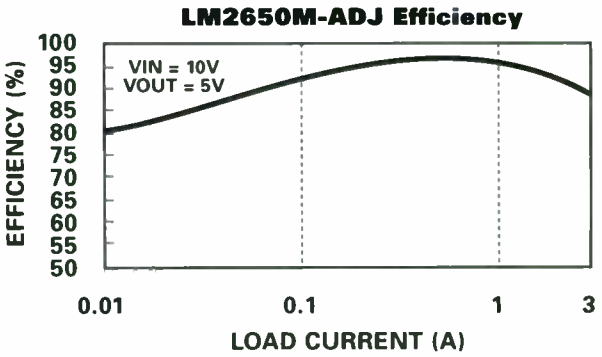
Wireless data also is moving into the mainstream, allowing many manufacturers to offer highly integrated solutions. One good example is the SX045 spread-spectrum transceiver, which is offered by American Microsystems Inc., Pocatello, Idaho. Intended for use in wireless LANs which follow the IEEE 802.11 specification, the SX045 contains all the baseband circuitry required for direct sequence spread-spectrum (DSSS) radio. In addition, it performs all radio-control and data-transfer functions of the physical-layer convergence procedure and handles the handshake logic to the physical layer transceiver. A low-cost microcontroller to run the media-access control protocol, a relatively straight-forward modulator/demodulator, and transmitter section are all that's required for a complete



1. ONLY A HANDFUL OF COMPONENTS IS REQUIRED to implement a cordless telephone using Motorola's MC13110 (a). The chip integrates many of the major digital, analog, and RF functions, reducing both component count and the cost of assembly (b). Significant savings in time-consuming tuning adjustments also are greatly diminished.

>96% EFFICIENT 3A BATTERY SWITCHER.

A SINGLE-CHIP SOLUTION WITH NO EXTERNAL FETs. ANOTHER INDUSTRY MILESTONE FROM NATIONAL.



For the first time, there's a 3A step-down battery switcher that can deliver over 96% efficiency—at substantial cost-savings. It's National's new **LM2650.**

Thanks to its synchronous architecture, this DC-to-DC converter can decrease power consumption and increase battery life in portable applications. Since the LM2650 has integrated FETs on a single chip, it can also save valuable board space. And its automatic sleep mode enables it to retain its high efficiency in light load conditions.

To meet a variety of portable applications, the LM2650 has a wide input voltage range, from 4 to 18V. Its built-in protection features include thermal shutdown and current limit. And it's from National, so it will never be in short supply.

Check out the LM2650. And get high 3A converter efficiency—without a high 3A converter price.

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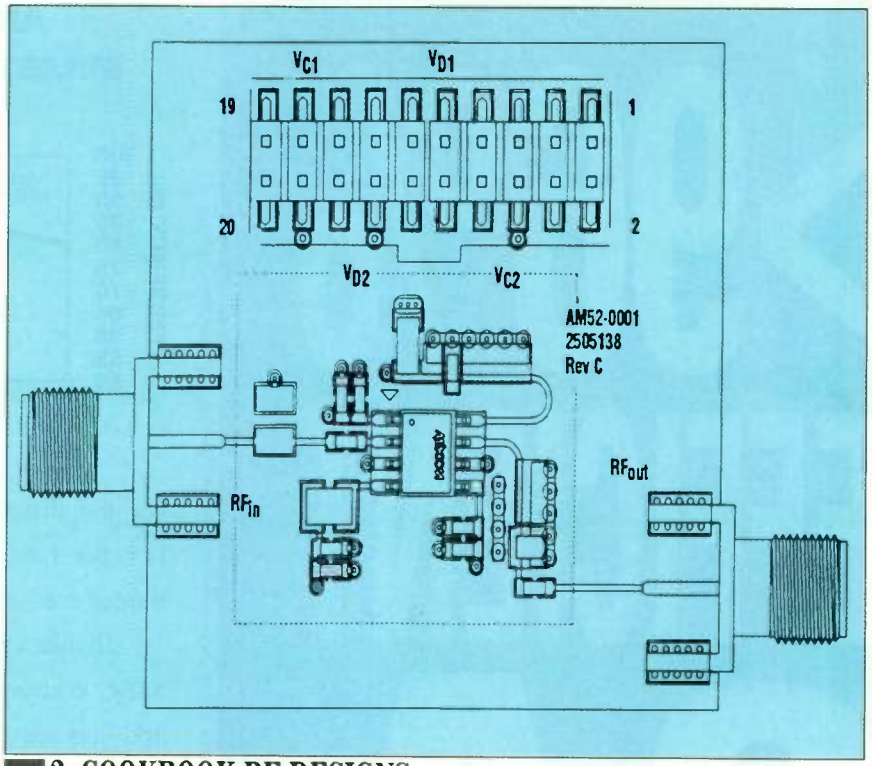
DSSS system.

Above baseband, the move toward integration has been slower, but making substantial advances in the past few years. Achieving integrated RF is not simply a matter of sticking a bunch of fast transistors on a single chip. Some means of matching the impedance between internal elements must still be used. On-chip parasitic effects must be minimized, lest they provide unwanted coupling between different portions of a circuit.

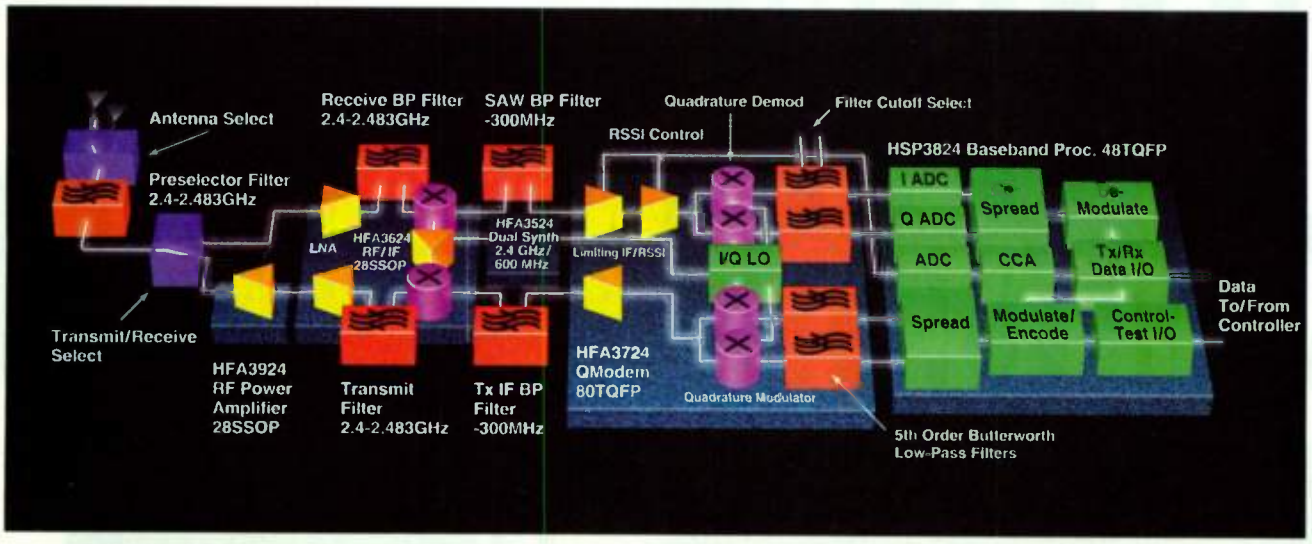
Trench isolation of transistors and careful use of multiple metal layers are only two of the many techniques used to keep crosstalk-induced noise from ruining a chip's RF performance. Additionally, on-chip passive components are becoming increasingly common on both silicon and GaAs devices. These tiny inductors, capacitors, and resistors are used both for coupling internal devices and for compensating for packaging-induced parasitics on the chip's inputs and outputs. The same input and output matching networks also are used to raise the RF devices' impedance to about 50 Ω, making them less tricky to use.

Integration has done much more than cut the parts count in RF devices. Wireless products using RF ICs often enjoy greatly reduced design times, require much less "tweaking" during unit assembly and testing, and have fewer manufacturing tolerance-induced quality control problems. Both the TQ9143, an integrated 1.4-W, AMPS/TDMA power amplifier from TriQuint Semiconductor, Beaverton, Ore., and the AWT0904, a 35-dBm, GSM/AMPS cellular-band amplifier from Anadigics, Warren, N.J., employ these advanced fabrication techniques. Their on-chip bias and matching networks, and voltage converters significantly reduce the production costs and engineering effort required to produce wireless designs (*see* Electronic Design, June 24, 1996, p. 87.

Other high-volume applications have led to the development of mixed-signal chips with high levels of digital and analog integration. Functions



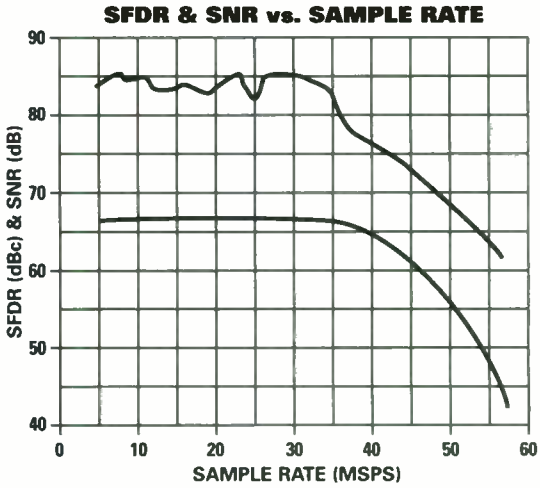
2. COOKBOOK RF DESIGNS are reducing engineering costs and time to market. In this example, the AM52-0001 RF power amplifier from M/A-COM comes with a reference design, including a 4-layer pc-board layout, application notes, and a complete parts list. An optional evaluation kit gives engineers a working prototype and other development tools.



3. THE HARRIS "PRISIM" WIRELESS LAN CHIP SET offers a 5-chip implementation of the IEEE 802.11 standard. Both a reference design and an evaluation kit are available to assist engineers in their development efforts.

12-BIT 41MSPS ADC. SMALL PRICE ($34) TINY SPACE (28-PIN SSOP).

THE COMLINEAR MONOLITHIC CLC952 ADC BEATS THE COMPETITION WITH A 45% SMALLER PACKAGE AND 40% LOWER COST.



In high-speed 12-bit ADCs, you've had few choices. On the one hand prices are too high. On the other performance is too low.

Now, the new 41MSPS Comlinear **CLC952** gives you the best of both worlds with top-level performance at the lowest price. And, with a 28-pin SSOP package, it takes much less space than competitive parts.

Check the specs: 76dBc SFDR, 65dB SNR, >60dB Power Supply Rejection Ratio, and a 250MHz T/H input BW. Top performance... lower price... smaller package. It's ideal for cellular basestations. There's simply no competition.

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such as divider networks and control logic can be fabricated on the same chip as voltage-controlled oscillator (VCOs), PLLs, mixers, and even amplifiers. This technique is somewhat easier in the lower-frequency ranges, such as the 49-MHz band used for CB radios, remote-control toys, and cordless telephones.

Motorola Semiconductor, Phoenix, Ariz., is one of the leaders in this area, producing extremely cost-effective chip sets for the very competitive cordless telephone market. One of their latest entries is the MC13110 RF combo IC, a chip that integrates several of the major functions of a cordless telephone into a single IC *(Fig. 1)*. Included on the chip are a dual-conversion receiver, a compander, a dual universal PLL, a supply voltage monitor, and a frequency inversion voice scrambler/descrambler security circuit.

Thanks to recent developments, digital technology is no longer limited to baseband applications. Faster analog-to-digital and digital-to-analog converters (ADCs and DACs) are making direct digital synthesis (DDS) of RF signals a possibility for lower-frequency (Â-MHz) RF applications. Most converters running above 400 Msamples/s are too bulky and power-hungry for portable applications today, but rapid advances in circuit fabrication will probably see commercially available digital radios passing the GHz threshold before the turn of the century.

These advancements are leading the way for the "software radio," an all-digital architecture which can be programmed to accommodate any modulation scheme or protocol within its frequency capability. While microphone-to-antenna software radios are not quite a reality today, DSPs are finding their way to the heart of many wireless applications.

While extreme levels of integration can be used for many wireless applications, it is often too costly to implement for all but the commercial products with the highest production volumes.

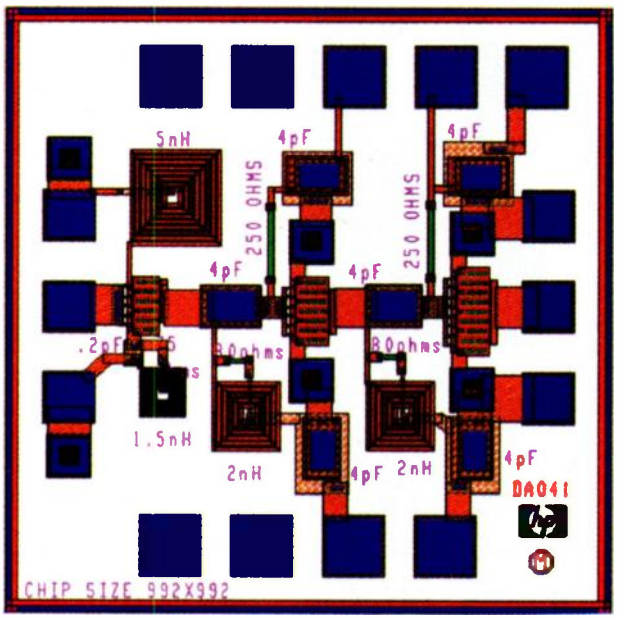
RF Building Blocks

The building-block approach developed by Fujitsu Microelectronics USA, San Jose, Calif., can be used to simplify designs and reduce production costs. Fujitsu has focused on offering its Super Analog component family, a line of smaller, less application-specific integrated "RF building blocks" that can be used in a variety of situations. Currently, their lineup includes the MB5401 integrated low-noise amplifier/mixer, the MB5402 dual low-noise amplifier, and the MB5403 two-stage medium-power amplifier. With a maximum operating frequency of 1.1 GHz, they can simplify both cellular and wireless data applications.

Although current technology does not allow us to apply true functional block-oriented ASIC design techniques to RF circuits yet, Fujitsu does offer a unique "RF Macrocell" technology for speeding up the design process. Known as the Versi-TILE process, it allows designers to work with preengineered bipolar or biCMOS "frames". The frames contain arrays of transistors, capacitors, and resistors that can be placed on a chip and connected to each other or other frames via two or three metalization layers. There also is a library of predesigned "tiles" which include prescalers, VCOs, buffer amplifiers, and PLLs.

Using the building-block approach, designers can go from supplying a preliminary block diagram to receiving working silicon in eight to twelve weeks. In addition to offering rapid turnaround, Versi-TILE has demonstrated a better than 90% first-pass success rate, based on over 100 designs. If a transition to higher-volume production is desired, the Versi-TILE circuit can be turned into an optimized full-custom design in under six months.

Although these sophisticated chip-level solutions make life much easier, they still can be tricky to use. While component count is sharply reduced, the selection and placement of passives, as well as pc-board layout, are all quite critical. To save designers the task of reinventing the wheel, many RF circuit manufacturers now are offering preengineered reference designs which can be used, at no cost, that can form the heart of a wireless product. In many cases, software for both DSPs



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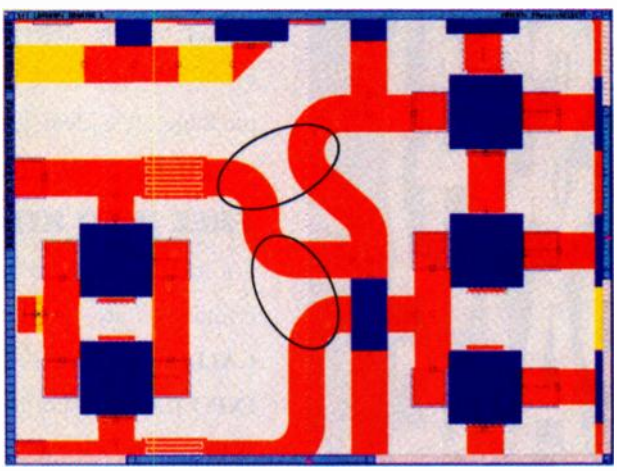

B

4. MULTI-LAYER CIRCUIT simulation and analysis begins at the system definition level and continues through the design of individual devices. Here, HP EEsof's circuit design and analysis package permits designers to accurately simulate the effects of physical layout on circuit performance (a). At this level, designers can examine undesired coupling effects between devices and circuit traces (b).

Pack More DSP Performance Into Your Low-Cost Designs Without Paying For It.

- *Single-cycle instruction execution*
- *512 words Program RAM, 256 words Data RAM*
- *Automatic program booting circuitry*
- *2 programmable serial ports with DMA*

- *2 general-purpose address generators*
- *Zero-overhead circular addressing hardware*
- *Zero-overhead looping hardware*
- *Automatically maintains nested loops*

Now, for just $4.50*, you can design in a DSP that's bursting with performance. Compared to other low-cost DSPs and microcontrollers, the ADSP-2104 from Analog Devices is easier to program, has more on-chip memory and gives you more processor and peripheral features.

DSP	MIPS	PROGRAM RAM	DATA RAM	PACKAGE
ADSP-2104	20	512 Words	256 Words	68-Pin PLCC
ADSP-2105	20	1 K Words	512 Words	68-Pin PLCC
ADSP-2109	20	4 K Words ROM	256 Words	68-Pin PLCC
ADSP-2115	25	1 K Words	512 Words	68-Pin PLCC
ADSP-2101	25	2 K Words	1 K Words	68-Pin PLCC

ADI offers a range of low-cost DSPs

Pin- And Code-Compatible Growth Path
With the ADSP-2104, you have over 100 code-compatible upgrade options. The 68-pin PLCC package is common to over 15 ADSP-21xx DSPs, so you can upgrade without any hardware or software changes.

Boost Your Speed With Single-Cycle Execution
The ADSP-2104 is the only DSP in its price range that can execute all instructions in a single cycle. That's due in part to Analog Devices' superior core architecture, which enables our 20 MIPS DSP to process algorithms faster than DSPs with twice the MIPS. Cycles aren't wasted supporting interrupts, serial port transfers, looped instruction coding, data addressing or arithmetic operations.

The overall result is a performance boost that allows you to design more features and functions into your product. Find out just how much you can expand your low-cost designs by calling for your ADSP-21xx EZ-Kit Lite today.

To order your ADSP-21xx EZ Kit Lite, call your local distributor listed below. The $89 Kit includes evaluation board, assembler, linker, simulator and more. For data sheets dial AnalogFax™ at 1-800-446-6212, Faxcode 2050. Or visit us on the World Wide Web.

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and microcontrollers is also supplied. This advantage makes product design a matter of providing packaging, power supply, and custom features that allow for product differentiation.

At its simplest, a reference design includes a components list, schematic, and in the case of an RF device, the all-important pc-board layout artwork. M/A-COM Inc., Lowell, Mass., makes it easy to design its AM52-0001 power amplifier by putting together an evaluation kit containing application notes, a finished 4-layer pc board, all recommended surface-mount passives, RF connectors, and a dc multipin connector. Also included in the designers kit is a floppy disk with device performance data and a DXF pc-board layout file *(Fig. 2)*.

In extremely high-volume markets, chip manufacturers will go to great lengths to make their product easy to use. Analog Devices Inc., Norwood, Mass., has gone so far as to offer a completely certified design for its AD20msp410 GSM cellular telephone chip set. The three-chip solution includes a complete software package that performs all Layer-1 GSM functions. There's optional software to implement Layers 2 and 3, as well as an application-layer tool kit for developing user interfaces and additional product features. Although it does not sell assembled units itself, Analog Devices went to the trouble of developing a complete cellular telephone design. The design has ETSI type approval, EMI/RFI, and spectral content. Using the preapproved design allows manufacturers bring their products to market in the shortest time possible by eliminating months of compliance testing.

In another case, National Semiconductor, Santa Clara, Calif., is helping electronics manufacturers compete in the highly lucrative market of DECT 1.9-GHz digital cordless telephones by offering a fully developed, type-approved reference design for a full-featured handset and base station. The CompleteDECT solution boasts an advanced RF section with high sensitivity, built-in antenna diversity, ten dialing memories, a 500-m range, a paging function, a 70+ hour standby time, and a 7-hour talk time. Along with a working evaluation unit, the solution

PAST AND FUTURE: THE NEW WORLD OF RF DESIGN

After years of niche status, RF design is enjoying a considerable renaissance. Until very recently, "RF" for most people invoked images of either advanced warfare equipment or amateur radio. However, driven by the dramatic growth in consumer wireless markets, and the relatively small number of new engineering graduates knowledgeable in the area, RF expertise has suddenly become one of the most sought after skills in all of electronic design.

As semiconductor and systems companies rush to build RF design departments and expertise, it's easy to overlook the fact that more is changing than just the design capacity needed. The nature of RF design itself is fundamentally in transition. Companies that try to apply the traditional design approaches to the new problems may find themselves in a losing position.

Much of this difference is driven by changing business dynamics. Most traditional RF customer requirements, especially in government markets, focus on performance and reliability. In consumer wireless design, however, "low cost" and "getting more features to market faster" usually take precedence. This shift has spawned some widespread trends which are already influencing what RF will look like in the future:

RF DESIGN ISSUES FOR CONSUMER MARKETS

Design issue	Traditional RF design	Consumer RF design
Technology	Discrete	IC/ASIC
Design objectives	Performance reliability	Performance, features, low cost
Component count	10-20	300+
Annual production volume	Dozens to hundreds	Might be millions
Product life cycle	Several years	6-18 months
Cost of project delay	Penalty for late delivery	Might miss entire market window

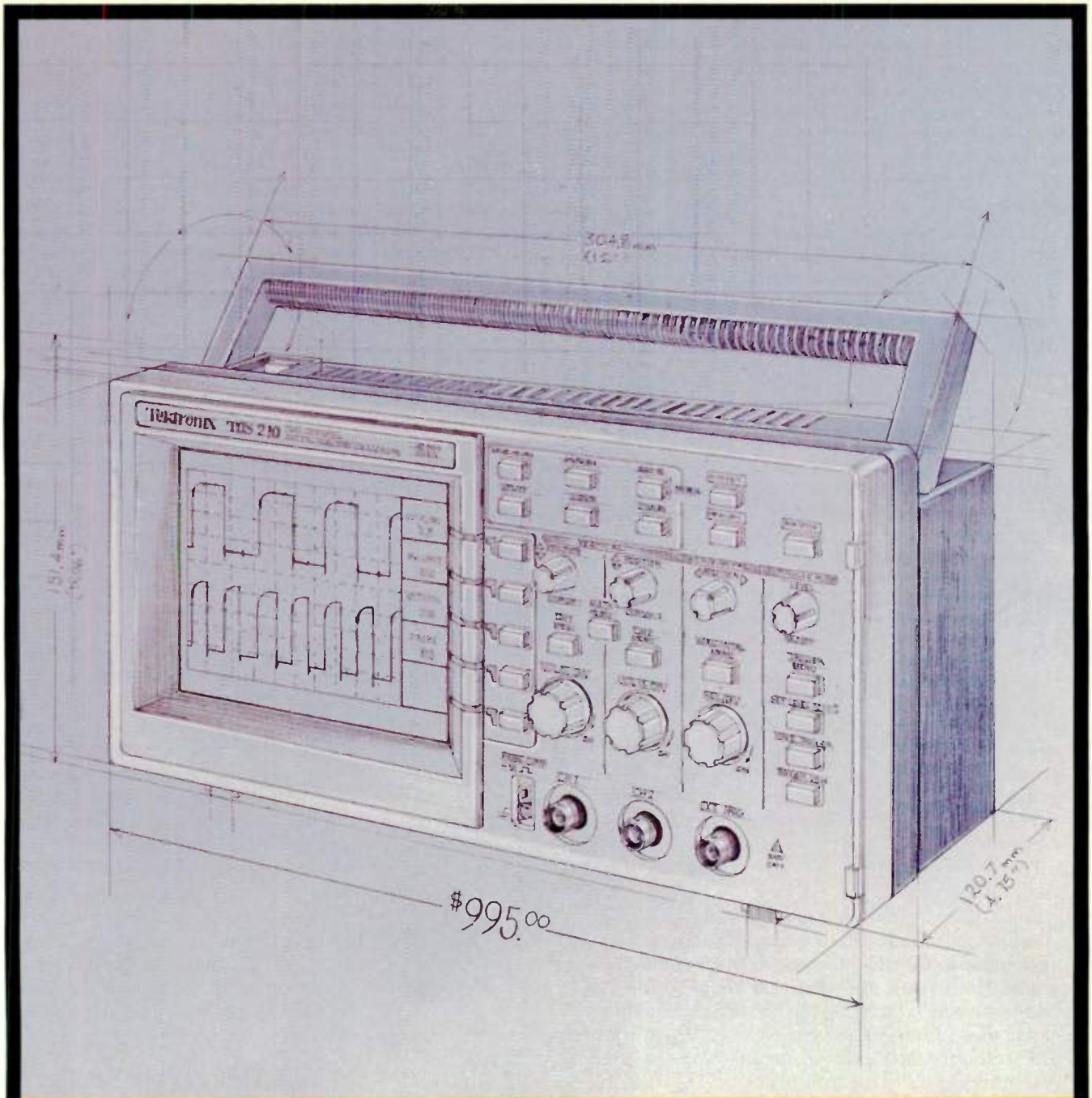
Siliconization of RF systems: to meet cost targets, most RF engineers in consumer business units are looking at silicon ICs as their preferred implementation choice. Although exceptions abound, unit production costs generally decrease with silicon integration. For example, the cost of an IC containing both a cellular transmitter and receiver functional blocks typically is only 20-30% more than that of an IC with only one of the two functions. In companies where production volumes may run in the millions, this can make a significant difference in their product line profitability.

RF engineers also choose IC implementations in order to reduce power consumption. At many consumer frequencies, the interconnect on a chip is short enough to reduce the stringency needed for terminations and impedance control. This technology makes it practical to design much higher impedance systems than the common 50 Ω, reducing power dissipation.

Top-down design: somewhat paradoxically, silicon RF implementations tend to be more complex in terms of component count than hybrid or pc-board implementations. One reason is that analog IC engineers tend to "throw transistors" at design problems. Another reason is that at board level, many of those components can be hidden within well-characterized blocks. The design engineer can work as though he or she were dealing with 10 or 20 blocks, instead of 250 transistors. A chip designer, however, needs to deal with all those devices.

To manage this kind of complexity, analog LSI designers are turning to AHDL based (Analog Hardware Description Language) top-down design practices. AHDL

(contined on page 54)



This digital scope is a major breakthrough no matter how you measure it.

It's never been easier to pick up a Tektronix digital scope. Just $995 will get you the 60 MHz TDS 210, while $1695 will get you its 100 MHz big brother, the TDS 220. Both come loaded with dozens of great features like triggering and automatic setup. They'll even store or recall your measurements at the push of a button. Yet despite all that, the actual scopes are as diminutive as their price tags. Making them easy to pick up in more ways than one. For more information, please contact your Tektronix distributor or call 1-800-479-4490, Action Code 318. Or, visit us at www.tek.com.

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includes schematics, parts-lists, pc-board specifications (including Gerber files), shielding specifications, timing diagrams, memory maps, plus test and tuning procedures.

DECT's simpler cousin, the North American 49-MHz/900-MHz cordless telephone is another market where both cost and time-to-market are critical issues. Recognizing this, Zilog Inc., Campbell, Calif., has developed the ZPhone reference design, a turnkey solution for digital spread-spectrum cordless telephones. Based on its Z87000 and Z87010 baseband chips, and an RF section designed by L.S. Research, Ceadarburg, Wis., the ZPhone design allows manufacturers to produce a product with extended range and high voice quality. The ZPhone is expected to retail for under $140. Both reference designs and complete evaluation kits are available from Zilog.

Harris Semiconductor, Melbourne, Fla., has applied the same formula to its PRISM wireless LAN product line. Recognizing that the IEEE 802.11 wireless LAN standard is a complex, moving target to design products around, Harris has made its 2.4-GHz, 2-Mbit/s, DSSS wireless data system as easy as possible to implement *(Fig. 3)*. In addition to a complete reference design, the PRISM chipset's designers also offer an evaluation kit for prototyping and product development. It consists of two preassembled open-frame PCMCIA transceiver evaluation cards, the PRISM chipset, an industry-standard media-access controller (MAC), RF connectors, PCMCIA extender cards, single-user firmware licenses, diagnostics software, and documentation. If 802.11 compliance is not required, the PRISM system can serve as a platform for the development of customized radios with wider spreading codes and faster data rates which can go as high as 4 Mbits/s.

For one-of-a-kind or low-volume designs, it often pays to completely eliminate all RF engineering by purchasing a complete radio subsystem from another manufacturer, and embedding it in the product. For example, Proxim Inc., Mountain View, Calif., produces the WaveLAN2 product line which allows engineers to integrate a complete wireless LAN subsystem within their products, with a minimum of space, power, or design-time impacts. The unit's type II PCMCIA card-sized radio data unit is self-contained, requiring only a PCMCIA interface and an antenna connection. RangeLAN cards can be connected conventionally, through an external PCMCIA slot, or embedded within the bowels of its host system. The card's microminiature coaxial connector, located on its edge, permits an antenna to be attached directly or run to a remote mounting point via a connecting cable. Power consumption (300 mA during transmit) is one of the lowest in the industry, a plus for battery-powered portable applications.

SMARTER DESIGN SOFTWARE

RF design software has existed for nearly as long as computers, but it hasn't matured at the same rate as its digital cousin. Some of the lag time is due to the lower demand for wireless systems, but the lion's share belongs to the richer set of problems faced by the RF engineer.

Traditionally, Spice and various flavors of harmonic-balance analysis were used to analyze circuit designs. Spice-type programs can be very accurate for single-frequency operation, but become cumbersome when attempting to model transient behaviors. Additionally, Spice tends to choke on the non-linear noise response in components such as mixers, amplifiers, and downconverters.

PAST AND FUTURE: THE NEW WORLD OF RF DESIGN

(continued from page 52)

helps ensure the product will work as a system before actually committing time and effort to designing the individual circuits. Verilog-A, the first real AHDL standard, supports RF-relevant constructions such as frequency domain and noise.

New design practices: the venerable superheterodyne architecture, well understood and reliable, has been the foundation for many generations of RF receiver designs. However, it has some characteristics at odds with the ultimate goal of integrating complex RF LSI into CMOS. One example is that it generally requires multiple off-chip filters. As a result, many design teams are experimenting with alternate RF architectures, such as zero-IF, low-IF, and undersampling techniques.

There's relatively little production experience with most of these architectures, so more analysis is needed (either via test chips, computer simulation, or both). However, the discontinuity associated with new RF circuit techniques, the move to silicon, and intense consumer demand, all suggest that there are substantial rewards are available for the first teams that solve the problem.

In general, the highest impact on the functionality, performance, and cost of a wireless system is to be made at the system architecture level. Optimal partitioning between RF, baseband mixed-signal, DSP, and software will ultimately differentiate one wireless system from another. However, most companies historically didn't organize their efforts in this way. Instead, they had a DSP design group, an RF design group, a software design group, etc., which all worked with each other via loose collaboration and "toss it over the wall" specifications.

A newer trend replaces the functional organization with a project-based one. This new structure has an RF engineer, a DSP designer, and a system architect all being a part of "the PCS group." The design practices now can focus on trade-off analysis between the RF circuits and the overall system.

The ultimate vision of the entire wireless system, optimally architected and integrated on a single fast-turn ASIC, is still years away. However, the road map for consumer RF design leads very clearly in that direction.

Eric Filseth is the marketing director of mixed-signal products at Cadence Design Systems Inc., Chelmsford, Mass. He may be reached at (508) 262-6104.

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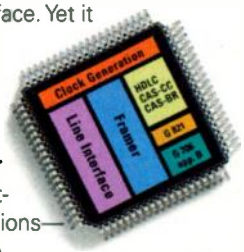
Integrated clock, framer, controller and more.

In addition to its on-board line interface, the FALC54 also integrates a clock for enhanced reliability, a framer, an HDLC controller, deep Tx/Rx FIFOs (64Bytes in each direction), and a 16-bit CPU interface. Yet it comes in an 80 MQFP package.



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Harmonic-balance software also has been used for highly accurate modeling of RF systems. One drawback with the software is that the simulation load grows exponentially with the number of components or frequencies involved. The result is that modeling non-linear components (which produce lots of harmonics), or circuits with much more than 20 devices, can tax even the most powerful workstation.

While these simple tools can be used to design today's complex RF systems, it resembles constructing a small computer using stone knives and bear skins. Since design and analysis tools have lagged behind, engineers have relied on brassboard prototypes and other trial-and-error techniques. Of course, this meant at least two or three (and often more) passes were needed to get a design sufficiently debugged for production. It can be time consuming and costly enough for board-level designs, but the 12 to 15 months and three to five spins required for moderately complex RF ICs is nearly intolerable for the development of commercial wireless products.

Over the past few years, RF design software has finally begun to mature, and RF design practices have begun to change with it. Modern RF system design practice typically begins with using system-level behavior modeling tools. These tools are used to model a proposed circuit's general characteristics, and permit engineers to analyze architectural choices. They could include different schemes for segmenting digital and analog functions. They also could look at the effect of various coding and error-correction algorithms upon the circuit's overall noise and power characteristics.

A Layered Approach

Once the overall architecture is nailed down, individual portions of the circuit can be designed using software which works at the device level. After a circuit has been captured, it can be run through a new generation of circuit simulators that operate in the frequency domain. This process makes the analysis of a circuit's response to complex modulation schemes a much less difficult task. Additionally, new advances in EM simulation allow modeling of the physical characteristics of a circuit, such as package-induced parasitics and the complex impedance generated by circuit board or chip-level interconnect traces *(Fig. 4)*.

This three-level approach offers many advantages. It permits engineers to make better system-level decisions by quickly exploring more design options before committing to a particular architecture. After detailed design begins, accurate circuit simulation helps reduce the amount of costly and time-consuming trial and error required to debug the design once its actually built *(see "Past and future: The new world of RF design," p, 52)*.

There are several commercially available RF design software packages which can be tailored to suit many different types of products. The Cadence/Alta group, Sunnyvale, Calif., offers a suite of RF design tools that support both system-level and device-level design and simulation. The software from Alta is used primarily for high-level system definition and analysis, while the Cadence package is focused towards detailed, device- and board-level circuit design and analysis.

At the system level, Alta's EnWave package is a complete solution, created to specifically address the needs of designers working with wireless communications systems. Some of these systems include PCS, wireless LANs, advanced messaging, satellite communications, and digital cellular standards such as IS-95, IS-136, and GSM. Based on Alta's core simulation technology, the EnWave package includes application-tuned libraries containing hundreds of algorithmic elements that simulate filters, codecs, amplifiers, modulators, mixers, and all the other elements of wireless systems. The package's RF library allows designers to model distortions and nonlinearities in systems, to permit rapid trade-off analysis.

Alta's recently introduced Spectre package also adds the capability to perform whole-chip simulations, including non-linear components. This advance is expected to help cut the number of chip-spins required to produce a working product.

Once a first-cut design is complete, it can be transferred for more detailed fine-tuning within the Cadence environment. While files are not directly transferable between the two systems today, work is underway to develop a seamless interface between the macro and micro design packages.

One of the other major players in the field is HP EEsof. They offer a well-integrated array of RF design tools which include simulation software, element libraries, and device modeling systems. Recently, a new suite of RFIC design tools were released with the intent of shortening the design cycle for RF subsystems. It uses multiple simulation technologies combined with highly accurate device models and efficient optimization algorithms. Even the mechanical properties of the semiconductor chips can be modeled to provide analysis of every aspect of a product's design.

HP EEsof's basic suite of RF design tools includes a linear simulator, a non-linear simulator, transient and convolution simulators, a statistical design package, a custom element development kit, and a Spice netlist translator able to import Berkley 2G6, PSPICE, and HSPICE netlists. Linkages to HP's mechanical design packages and electromagnetic simulation software are available to perform accurate chip- or board-level design and analysis.

Conclusions

We can expect that wireless applications will be a rapidly expanding market well into the 21st century, and that the demand for engineers with RF familiarity will continue to be high. Fortunately, today's design tools and products are making it easier than any time since the discovery of the spark gap transmitter to add wireless capability to your next product. While reference design-based RF subsystems take some of the "fun" out of product development, they give the overworked engineer an opportunity to add value to a product by adding functions and features in more visible locations. □

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Scan-Based Testing Hits The Mainstream

The advent of larger devices that are harder to test makes scan-based design-for-test techniques a priority.

JOHN NOVELLINO

With the average ASIC hitting 50,000 gates, and devices with several hundred thousand (or even a million) gates becoming increasingly common, many designers must now consider adding testability features to their circuits. Design-for-test (DFT) techniques that were fairly recently considered the domain of designers of high-end, high-performance circuits are now becoming mainstream.

One of the most frequently employed DFT strategies involves scan-based testing. Scan-based testing is actually a family of techniques. Although scan testing has been around for some time, there is still disagreement over which methodology is best for which application, and how to define various implementations of scan. But, there is general agreement that scan-based testing will continue to be used in the future. In fact, new tools are still being introduced for implementing scan testing.

One very frequently employed form of scan testing is boundary scan, which was developed as a way to check out interconnects on printed circuit boards that are too densely packed to use a bed-of-nails fixture. Boundary scan was officially codified by the IEEE-1149.1 standard in 1990, but is still often referred to as JTAG, after the Joint Test Action Group, which started the standard's process in Europe.

Designers have found two key elements of the standard, the test access port

COMMON FULL-SCAN DESIGN RULE VIOLATIONS

Violation	Effect on scanability of design	Effect on sequential ATPG	Effect on sign-off simulator
Gated clocks	Design-specific	***	**
Internal clock generators/one-shots	Not scannable	Cannot use	***
Use of positive- and negative-edge flip-flops	Design-specific	Okay	*
Uncontrolled sets/resets	Design-specific	*	*
Flip-flop drives clock and D of next flip-flop	Not scannable	* (may cause race)	**
Asynchronous (unclocked) feedback loops	Okay	**	**
Mixed flip-flops and latches	Okay	*	Okay
Nonscan flip-flops present	Okay	*	*

* = Adds some difficulty
** = Adds more difficulty
*** = Extremely difficult without special DFT techniques

Source: Viewlogic/Sunrise

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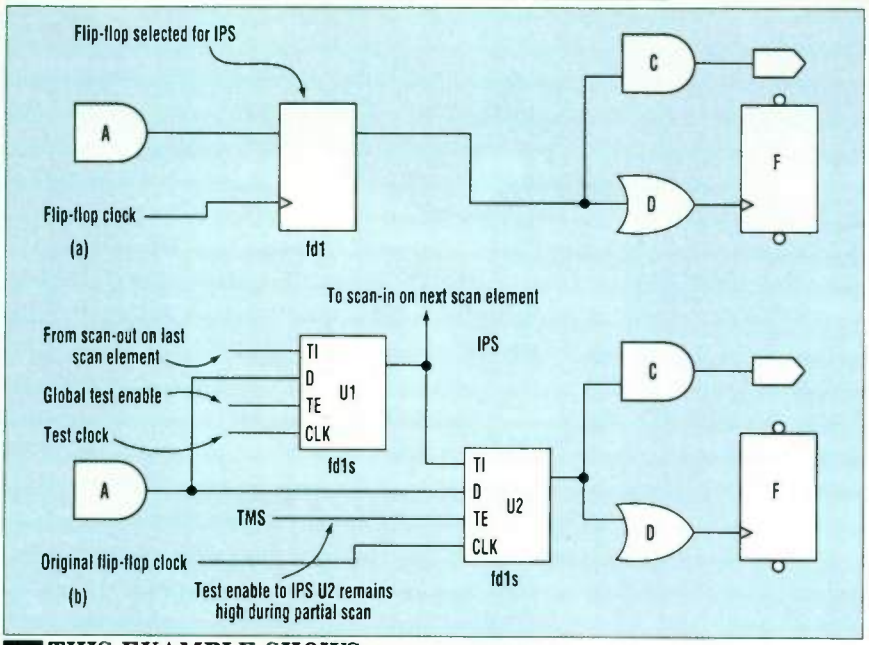


THIS EXAMPLE SHOWS the additional ciruitry needed to replace a non-scan flip-flop (a) with a scannable flip-flop (b) using the Isolated Partial Scan technique.

and the test controller, to be very useful for uses other than their original purposes. As a result, JTAG has become a way to access circuitry that's too densely packed to test with conventional fixturing. It's even being used to program FPGAs.

Internal scan is the general term for a DFT technique that allows designers test the functionality of an IC. Designers add latches to functional storage cells so that they can be scanned to determine the internal state of the device. As is usually the case, tradeoffs must be made. Consequently, two basic versions exist, full scan and partial scan. But, full scan doesn't necessarily mean 100% of the IC is scannable and partial scan can cover a wide range, from 30% to 90%. There's also a lot of room for discussion about the value of each version for specific applications.

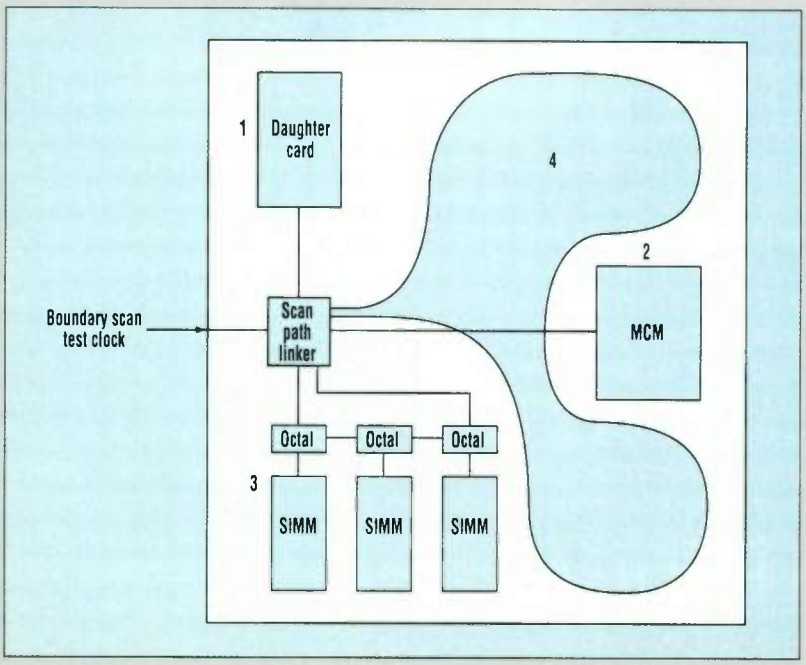
Historically, designers used scan as a way to debug systems, notes Steve Smith, director of marketing at Viewlogic Inc.'s Sunrise Test Business Unit, Freemont, Calif. It started at mainframe computer makers like IBM and worked it's way into workstation companies like Hewlett-Packard, Silicon Graphics, and Sun Microsystems, where it's used not only for IC debug, but also system debug and diagnosis, Smith said.

But, things are changing. "In recent years, probably the last two or three

TESTING HIERARCHICAL AND RECONFIGURABLE SYSTEMS

The hallmark of most IEEE-1149.1 boundary-scan applications has been the physical access that the standard provides in systems too densely packed to use a bed-of-nails fixture. But, sometimes that issue takes a back seat to other problems, such as how to handle the testing of hierarchical or reconfigurable systems.

One example is a satellite communications system developed by an aerospace company. The design team faced a test dilemma because the system's circuit board had several hierarchical levels of subassemblies. It included a daughtercard, a multichip module (MCM), and several single in-line memory modules (SIMMs). Consequently, they could not use their standard in-circuit test methods because an in-circuit fixture cannot test the interconnection of subassemblies to the base circuit board.



The team decided to use boundary scan for interconnect testing, employing a boundary-scan development system to simplify test creation and to physically and logically partition the system. Special control devices called scan path linkers (SPLs) were used at the module level to allow physical partitioning. The result was four scan paths that separately handled the daughter card, the MCM, the SIMMs, and

(continued page 62)

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TESTING HIERARCHICAL AND RECONFIGURABLE SYSTEMS

(continued from page 90)
the remaining logic on the board *(Fig. A)*. The team created a logical partition for the MCM to allow more flexibility in test creation and fault isolation. Logically partitioning the system minimized the number of test sets needed for the entire system. Standalone test sets were developed for each logical and physical partition. The boundary-scan test environment made it easy to take these lower-level tests and re-use them to test the upper levels of the system's hierarchy.

Another example involves a medical imaging company that employed boundary scan to solve a manufacturing test problem. One of the company's product lines uses a base design as a foundation for the different models within the product family. The final configuration can contain a daughter card or MCM, depending on the customer's needs.

The company wanted to be able to test any of the possible configurations within the same manufacturing workflow. Separate test bays or distinct test areas for each model would have slowed the manufacturing process unacceptably.

The test development team decided to implement a boundary-scan environment that would let them easily generate a dynamic software model of the system. With this model, a generic test procedure for the base design could be developed, along with modules needed to test the daughter card and MCM *(Fig. B)*. The boundary-scan test development environment automatically selects the correct test set for the appropriate configuration. This allows the test vectors to be applied quickly on the manufacturing floor.

The system software model allows dynamic and automatic reconfiguration of the scan chain. An easy-to-write standard programming language and a library of ready-made test objects shortened the development time of the test suite.

Glenn Woppman, president and CEO, ASSET InterTech Inc., 2201 N. Central Expwy., Suite 105, Richardson, Texas 75080-2718; (214) 437-2800.

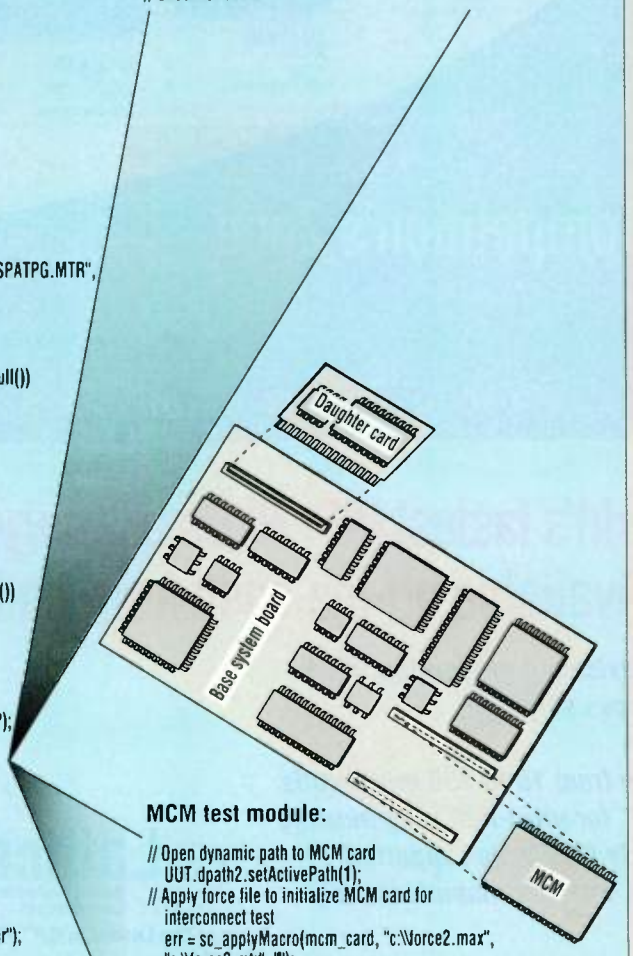
Base system test code:

```
include <stl.h>
include <basesys.h>
include <dcard.h>
include <mcm.h>
BASE_SYSTEM  UUT;
DAUGHTER_CARD d_card;
MCM_CARD     mcm_card;
int ASSETMain (int argc, char *argv[])
{
SC_ERROR err;
// Connect to ASSET
   err = sc_connect(0);
// Check for connection error
...
// Open Base System data base
   if (sc_open(UUT, "BASE_SYSTEM").isNull())
{
// exit and report error
...
}
// Re-set UUT
   sc_reset();
// Verify scan path on Base system
   err = sc_applyMacro("c:\\SPATPG.MAX", "c:\\SPATPG.MTR",
   "");
// Check for macro apply error and test status
...
// Open Daughter card data base
   if (sc_open(d_card, "DAUGHTER_CARD").isNull())
{
// exit and report error
...
}
// Connect Daughter card to Base system
   err = UUT.J2.connectExternal(d_card.TAP);
// Check for errors
...
// Open MCM card data base
   if (sc_open(mcm_card, "MCM_CARD").isNull())
{
// exit and report error
...
}
// Connect MCM card to Base system
   err = UUT.J3.connectExternal(mcm_card.TAP);
// Check for errors
...

// Apply force file to initialize Base system
   err = sc_applyMacro(UUT, "c:\\force3.max",
   "c:\\force3.mtr", "");
// Check for errors
...
// Apply interconnect test to Base system
   err = sc_apply(UUT, "c:\\wit3.sbs", "c:\\wit3.sbr");
// Check for errors
...
// Close ASSET data base files
   sc_close();
// Disconnect from ASSET
   sc_disconnect();
}
```

Daughter card test module:

```
// Open dynamic path to Daughter card
   UUT.dpath1.setActivePath(1);
// Apply force file to initialize Daughter card for
   interconnect test
   err = sc_applyMacro(d_card, "c:\\force1.max",
   "c:\\force1.mtr", "");
// Check for errors
...
// Apply interconnect test to Daughter card
   err = sc_apply(d_card, "c:\\wit1.sbs", "c:\\wit1.sbr");
// Check for errors
```



MCM test module:

```
// Open dynamic path to MCM card
   UUT.dpath2.setActivePath(1);
// Apply force file to initialize MCM card for
   interconnect test
   err = sc_applyMacro(mcm_card, "c:\\force2.max",
   "c:\\force2.mtr", "");
// Check for errors
...
// Apply interconnect test to MCM card
   err = sc_apply(mcm_card, "c:\\wit2.sbs", "c:\\wit2.sbr");
// Check for errors
...
```

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years really, we've seen a radical change and shift in the use of scan technology—more towards what I call a mainstream market," says Smith. The main areas involved are consumer, communication, and high-volume computer products, such as PCs. The reason is that competitive pressures are forcing designers to add functionality, (another way of saying complexity) while bringing new products to market faster. So, companies are looking for ways to automate their testing.

Full Scan Preferred

Most designers would like to use a full-scan approach, because it provides fault coverage and predictability. Due to the design rules imposed by full scan, however, many projects cannot employ it. Instead, many teams are using "almost full scan," according to Smith. "Because the circuits in these market segments have some complex clocking, or embedded memories, or other areas where you cannot use scan, they have to work within some constraints," he says. "So, they're using a full-scan methodology, but in reality it's almost full scan."

In addition to the problem with design rules, once a designer goes to partial scan, sequential automatic test pattern generation (ATPG) algorithms must be used, says Smith *(see the table)*. These algorithms are an order of magnitude more complex than combinational ATPG tools, he says.

Here's where fuzzy definitions come into play again. Partial scan can mean anything up to about 75% scan, according to Smith. "Anything above that and you can actually work within a full-scan environment to some degree. But, you do need to have some of the benefits of sequential ATPG to boost up your fault coverage," says Smith.

Sunrise's answer to the designer's full-scan/partial-scan dilemma is a "structured sequential" technique that combines a structured DFT methodology with sequential ATPG and some enhanced tools. Structured sequential allows designers to back off of 100% scan, and thus some of the burdensome design rules. "There is still a trade-off in terms of run time, fault coverage, and test vector length, but it will be closer to full-scan benefits," says Smith. If the design team completely ignores the design rules, the sequential ATPG tools will still work, but the run time will be very long. "We're trying to get the benefits of both worlds," says Smith.

Scan is indeed being very widely adopted as a DFT methodology, and among its many flavors, full scan is winning the broadest acceptance, according to Najmi Jarwala, chief technologist at LogicVision Inc., San Jose, Calif. Jarwala feels that there are two reasons why some designers want to use partial scan. One is that by not adding the scan circuitry to every flip-flop some area overhead is eliminated. The other involves the performance penalty that may be introduced by adding scan to flip-flops in a critical path that maybe extremely time sensitive. Designers can overcome both those problems, says Jarwala, who is the chairman of the 1149.1 working group.

"My feeling is that the complexity that partial scan introduces is usually not worth the trade-off in terms of the area saving," says Jarwala. "Silicon is getting cheaper, and we are able to put a lot more transistors on a chip. The critical thing now is time-to-market, making sure that you shorten the design cycle, making sure that you can verify and test your logic thoroughly."

Timing considerations normally should not be a problem either if full scan becomes the fundamental criterion. "It's usually possible to allocate your timing budget so that you can work around that," Jarwala says. "The problem that usually occurs is you just do a design without considering DFT, and then you kind of overlay test on top of it. Then you run into these kinds of problems where you can't run a system clock into the flip-flop."

If DFT is a concern up front, designers can even work around the small performance penalty incurred by adding scan to the flip-flops, says Jarwala. It's a matter of properly allocating performance specifications from the product level down to the chip level, and deciding that the product is to have the improved quality that DFT brings to the table. According to Jarwala, "If you keep DFT in mind, you are almost always able to achieve a full-scan methodology, which usually results in a tremendous savings in terms of design time, and just makes the whole project go a lot easier than a partial-scan methodology."

In fact, the term "full scan" may be something of a misnomer, applying more to a methodology than to an actual result. "There's no such thing as a full-scan design," says Doug Wright, product marketing manager at Mentor Graphics Corp.'s DFT Group., Wilsonville, Ore. "Very rarely do you see a full-scan design that has every single flip flop included in the scan chain." That's true despite the fact that the design may be classified as full scan, he says. The design team may use a full-scan methodology, but sections of the circuit may not comply with the clocking rules. There also may be critical paths that the team purposely leaves out of the scan chain.

Speed Versus Die Size

Fault coverage then becomes more difficult. The team will be using combinatorial test-generation tools so that certain sequential parts of the design will not get tested. As a result, the tests may have to be augmented with functional patterns, or maybe even further tests created with sequential tools, notes Wright.

That being the case, is it better to start out with a partial-scan technique? "It really depends on what your overall design goals are," says Wright. "The reason there are two methodologies is that people have different goals in mind. If they want a pushed solution, something that they can get out the door as quickly as possible with the highest fault coverage, full scan is a good methodology. But if you're in a very competitive market where you may be doing a high-volume design, and trying to get the die size as small as possible, the extra time that partial scan takes may pay off in the long run with a decrease in cost per part."

Full scan is the method most people would prefer to use because it has higher, more predictable fault coverage. It fits in well as a back-end process, and as long as you follow the design rules, things should go pretty smoothly, says Susheel Chandra, marketing manager at Mentor's DFT Group. Partial scan is more difficult. "You have to design for partial scan, so to speak, and make sure that you don't use certain types of structures that will make it more difficult for a test pattern generator to

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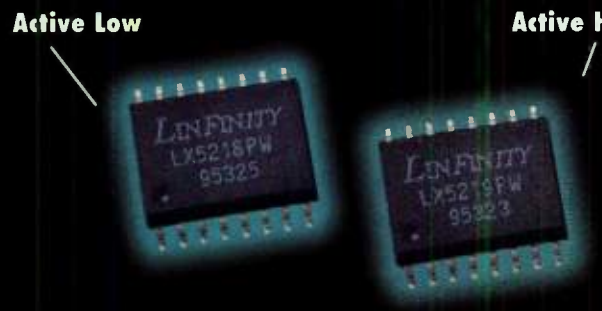

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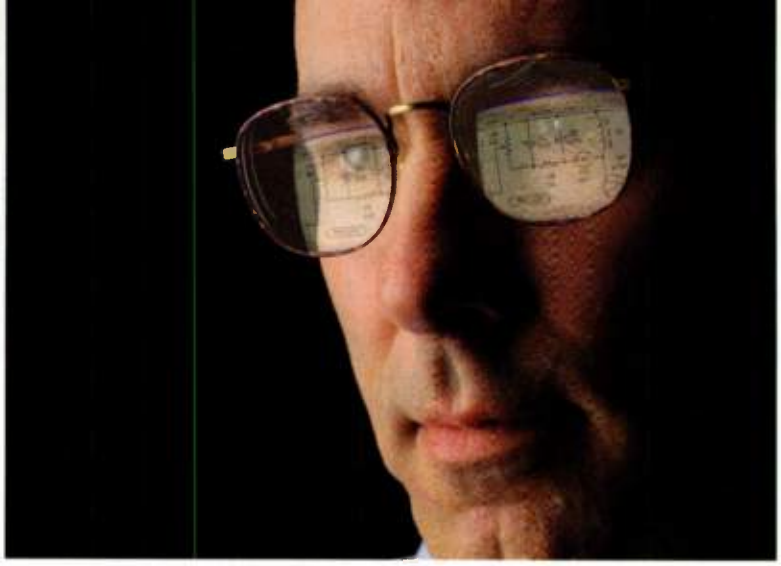

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create the patterns," says Chandra.

To simplify the process, Mentor came up with a technique called Partition Scan, which is a partial scan method that offers most of the benefits of full scan, according to Chandra. Although a team could design a block of circuitry for a certain level of partial scan and get reasonable test coverage, when that block is embedded to the overall circuitry, the controllability and observability are lost. Partition scan was designed to allow designers to do partial scan on a block-by-block basis and still provide predictable test coverage when the blocks are integrated into the chip.

According to comments heard at the last Design Automation Conference and in customer contacts since then, scan users fall into two basic categories, says Ralph Marlett, president of ATG Technology Inc., Ramsey, N.J. Those who have rigorously enforced the scan design rules are very pleased with the overall results, he says. In the other camp are people who like what full scan promises, but feel they just can't live with the rules. "It gets down to the gated clocks, the derived clocks, the derived sets and resets," says Marlett, "that's what kills them."

Power Is Also An Issue

The need for high performance may not be the problem. For example, the desire to reduce power consumption may be the deal breaker. Marlett notes that because CMOS consumes power on the clock transitions, a designer can save power by shutting off clocks to parts of a chip that aren't being used at the moment. To do so requires logic in the clock distribution system to disable the clocks at the appropriate times. That arrangement violates full-scan rules.

"If the clock to some flip-flop is not the system clock, but rather some signal derived from the system clock, then while you're clocking the scan chain you may not be clocking that particular flip-flop," notes Marlett. "Its clock may be, at that moment, disabled. Therefore, you think you're scanning through the whole chain, but you're not."

Mainframe and processor designers can handle such constraints and their designs are primarily full scan, says Marlett. But, the chips for peripheral are a different story. "The disk controllers and the I/O controllers, the communications, these are places where there's communications between basically free-running systems that cannot be on a common clock," he notes. The telecommunications field has a similar problem.

ATG's solution to the design rules problem is a technique called Isolated Partial Scan (IPS) that is incorporated within the Intellect test-generation tool. IPS differs from conventional partial scan because it ensures by construction that the state of non-scan sequential devices is not changed during scan operation. Additionally, no disabling logic to the clocks or asynchronous logic feeding the non-scan devices is required. The technique adds little delay and area overhead, and requires no extra design rules.

What is required is that the scan element output not change during scan operation, the scan clock be distinct from any system clocks, and the test enable pin is available to switch between scan and normal functions. ATG says this can be done with, at most, four additional pins, and that by multiplexing system pins, no pins need be added. IPS also can be configured as a user data register, allowing it to employ existing JTAG pins and test access port controls.

For example, the output gate of device A is captured by the test clock to U1 *(see the figure)*. In this case, the next scan will shift out captured values and shift in new values intended for the D input of the original flip-flop. Because the scan chain logic is shifted by a separate clock and connects to the original circuit at system data input pins, the state of sequential devices in the original circuit is guaranteed to not change during the scan operation.

A complete scan in will result in the new values on the output of U1. These values will be loaded into U2 only if a rising edge is produced by the system logic feeding the original flip-flop clock. □

John Novellino's e-mail address is: jnovelli@class.org.

How Valuable?	Circle
Highly	549
Moderately	550
Slightly	551

Flexible Circuits Use Different Technologies For Manufacture

Circuit Design Engineers Probably Don't Look To Flexibles Often Enough For Solutions To Tricky Packaging Problems.

PAUL MCGOLDRICK

The use of flexible circuits has been somewhat of a design secret. Such circuits are well-known in the hard-disk drive marketplace, but for the average designer, there are enormous stumbling blocks in thinking about flexible circuits for other logical, problem situations. Three obvious considerations are motion, small size, and shape. Much of the reticence among designers about the use of flexible circuits is probably due to a lack of information about what can be done.

Although this article principally addresses the solutions of one company working in the field, there are other companies with similar, but not identical, techniques. Smartflex Systems, Tustin, Calif., had an initial mission of developing and manufacturing flexible circuit assemblies in order to place the preamplifiers in close proximity to the playback head in a disk drive. Another goal of the company was to provide flexible connectivity to the drive electronics. Such uses are still important, but the technologies available to designers open up other uses in the medical, automotive, robotics, and PCMCIA markets.

Surface-mount technology (SMT) on flex and chip on flex (COF) are both in volume-quantity production at multiple sites. The technologies are well understood and reliable, with COF being chosen most often over SMT in applications in which size and thickness are important. SMT uses one to three fine-pitch,

A COMPARISON OF THREE FLEX TECHNOLOGIES

Characteristic	Surface-mount technology (SMT)	Chip on flex (COF) technology	Flex chip on flex (FCOF) technology
Footprint	Large	Medium	Small
IC pad pitch (in.)	0.006	0.006	0.005
Cost factor	1.0	1.1	0.8-2.8
Pretestable	Yes	No	No
Added wafer process	No	No	Yes
Θ_jA	61°C/W	46°C/W	74°C/W
Inductance (nH)	1.0-3.0	1.0-2.0	0.1-0.2
Capacitance (pF)	0.21	0.21	0.3
Additional advantages	• Readily available • High reliability • Easy rework • Good infrastructure	• Small footprint • Good electrical performance • Compatible with most ICs • Excellent thermal resistance	• Uses standard ICs • Good electrical performance • Lowest high-volume cost • No post-cleaning for flux
Added disadvantages	• Lowest electrical performance • High processing temperatures • Requires flux cleaning • Largest outline	• Lower yields • Not pretested • No rework after glob top	• Poor thermal performance on flex • Wafer bumping required • Not pretestable

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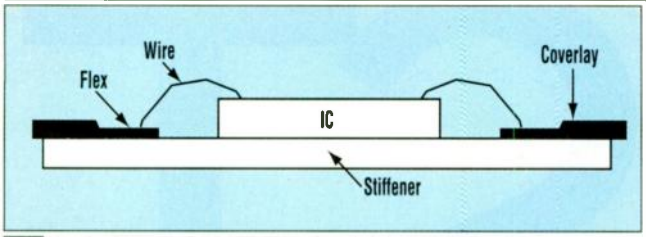
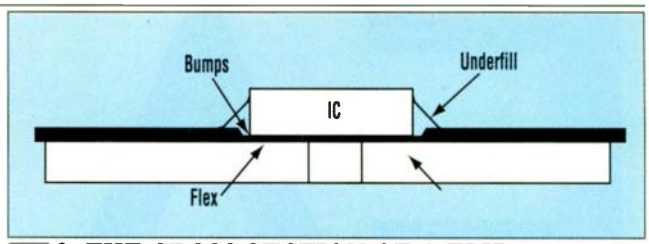


1. A CHIP-ON-FLEX CROSS-SECTION shows the IC mounted to an aluminum stiffener, improving heat transfer. The stiffener is laminated to the backside of the flex.



2. THE CROSS-SECTION OF A FLIP chip on flex (FCOF) arrangement shows its smaller footprint and the ability to route circuits beneath the mounted IC.

surface-mount ICs, and three to twenty discrete components using eutectic tin-lead solder. Direct chip attachment is used in COF with aluminum-wire bonding. Flip chip on flex (FCOF) is the latest generation in flex technology. It is smaller, lighter, thinner, faster, and cheaper. However, it is often the case that mixing the technologies provides a more elegant solution.

A number of other technologies also are starting to come into prominence to meet the needs for smaller footprints and higher levels of reliability. These techniques use pretested packages which are about the same sizes as ICs and go by names like Micro SMT and Micro Ball, among others. Another is *C4* (Controlled Collapse Chip Connection), which is widely used as a direct chip connection system in high-speed computers and vehicles.

A Joint Effort

Generally, the design of the flex circuit is a joint effort of the customer and the assembler. To be cost-effective, the ICs used in an assembly are standard surface-mount discretes in standard plastic packaging, and the circuit must accommodate various interconnecting techniques. Part of the assembler's task is to procure the components, complete the fabrication, and then perform any additional bending, laminating, and bracket attachment required.

SURFACE-MOUNT TECHNOLOGY (SMT) ON FLEX AND CHIP ON FLEX (COF) ARE BOTH IN VOLUME-QUANTITY PRODUCTION AT MULTIPLE SITES.

Each of the technologies has advantages and disadvantages. The packaging methods will be mixed with SMT and through-hole components based on available areas/volumes, performance needs, and cost limitations *(see the table)*.

In each case that "poor thermal performance on flex" is listed, the situation can be addressed with heat sinks and substrate changes. If such a fix is contemplated, the possible costs and layout limitations need to be carefully considered in the circuit design.

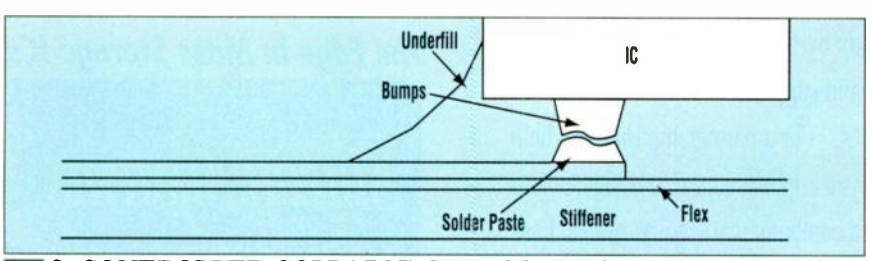
The "footprint" is a definition of working area. COF is is listed as "medium," for example, because the IC is mounted to an aluminum stiffener *(Fig. 1)* that is laminated to the backside of the flex, opposite a cavity. The thermal performance, as noted, is good but there is no way that traces can be routed under the IC. The area between the coverlay edges is dedicated to the COF attachment.

The attachment area is smaller for FCOF, and the area under the chip is available for routing *(Fig. 2)*. Conversely, the area for *C4* is smaller, but because the space under the IC is used for bump lands, it is not available for routing *(Fig. 3)*. The pitch of most micro-packages (the *C4* IC), which is limited by the ability to stencil print solder paste on the substrate, currently measures about 0.012-in. centers.

The *C4* bumps are formed by sputtering 95/5 lead/tin solder through a mask. The solder's melting point at 308°C is considerably higher than the 183°C of the eutectic solder (60/40 tin/lead). The solder does not reflow during the attachment process of the IC, simply "wetting" to the IC's bumps. There is lower stress with the standoff of the IC with its bumps, and this stress is further relaxed by the space being available to be under-filled.

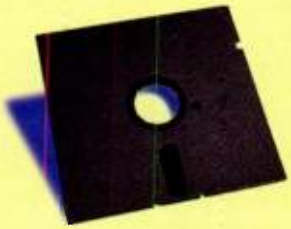
Further work is underway to improve heat sinking, reduce size, lower costs, and improve yield and reliability. Smartflex is located at 14312 Franklin Ave., Tustin, CA 92680; (714) 838-8737; fax (714) 573-6918. □

Paul McGoldrick's e-mail address is: 102447,346@compuserve.com.



3. CONTROLLED COLLAPSE CHIP CONNECTION (C4) has non-reflowed solder bumps keeping the IC off the flex and allowing for circuit routing.

How Valuable?	Circle
Highly	540
Moderately	541
Slightly	542



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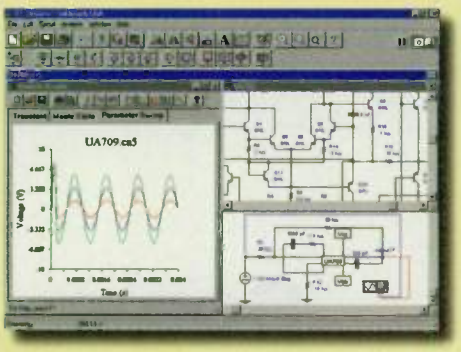

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Exceptional Frequency Response And Low Distortion Change The Conventional Video Switcher Future.

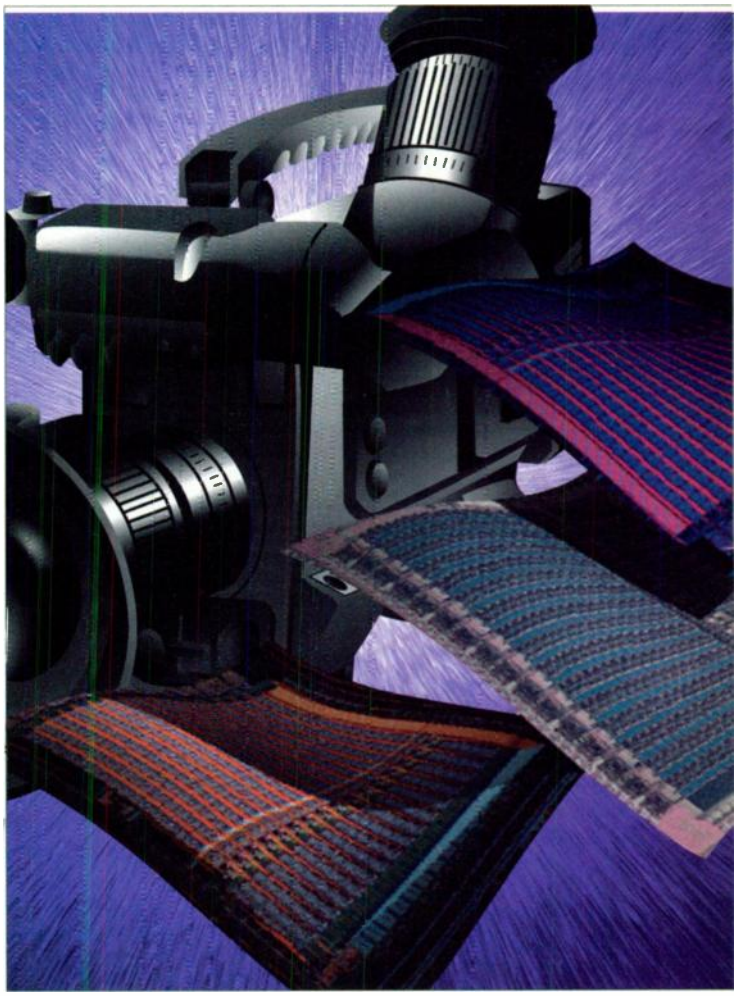
256 Video Crosspoints In A TQFP Confound The Critics

PAUL MCGOLDRICK

One sure thing in life is that when someone says something can't be done, there always will be someone else stubborn enough to try it. One example is the case of video crosspoint components. The conventional size of video crosspoint components has been 8 by 8. Getting to 16 by 16 represents a fourfold increase in the crosspoints, and a different style of practical implementation of the end products. A new IC from Analog Devices combines that functionality with low-power consumption, great video specifications, and full expandability. It comes in a package only 5/8 by 5/8 in., changing the problem of finding space for the circuit to fitting all the BNC connectors *(Fig. 1)*.

The AD8116 is a high-speed, 16-by-16 video-crosspoint switch matrix with a 3-dB bandwidth greater than 200 MHz, and channel switching times faster than 30 ns with 0.1% settling. Unity gain is maintained within 0.1 dB out to 40 MHz. Crosstalk, in all-hostile conditions, is better than –80 dB up to 10 MHz, while differential gain and phase are better than 0.01% and 0.01°, respectively. The input impedance is typically 10 MΩ with 2 pF of capacitance. A major difference between this chip and previous offerings is the 16-by-16 structure with its high level of on-chip integration and the built-in output buffers.

The core of the AD8116 is an array of 256 transconductance (g_m) stages organized as sixteen separate 16:1 input multiplexers, with a common 16-line analog input bus *(Fig. 2)*. Each multiplexer is, basically, a folded-cascode, high-speed, voltage-feedback amplifier with sixteen input stages. The input stages are npn differential pairs with combination taking place at the output stage. Within the output stage there is the high-gain node, compensation, and complementary emitter-follower output buffer. The overall amplifier gain for any signal traveling across the IC is set to unity, and the output is capable of directly driving a back-terminated video load of 150 Ω, with low distortion.



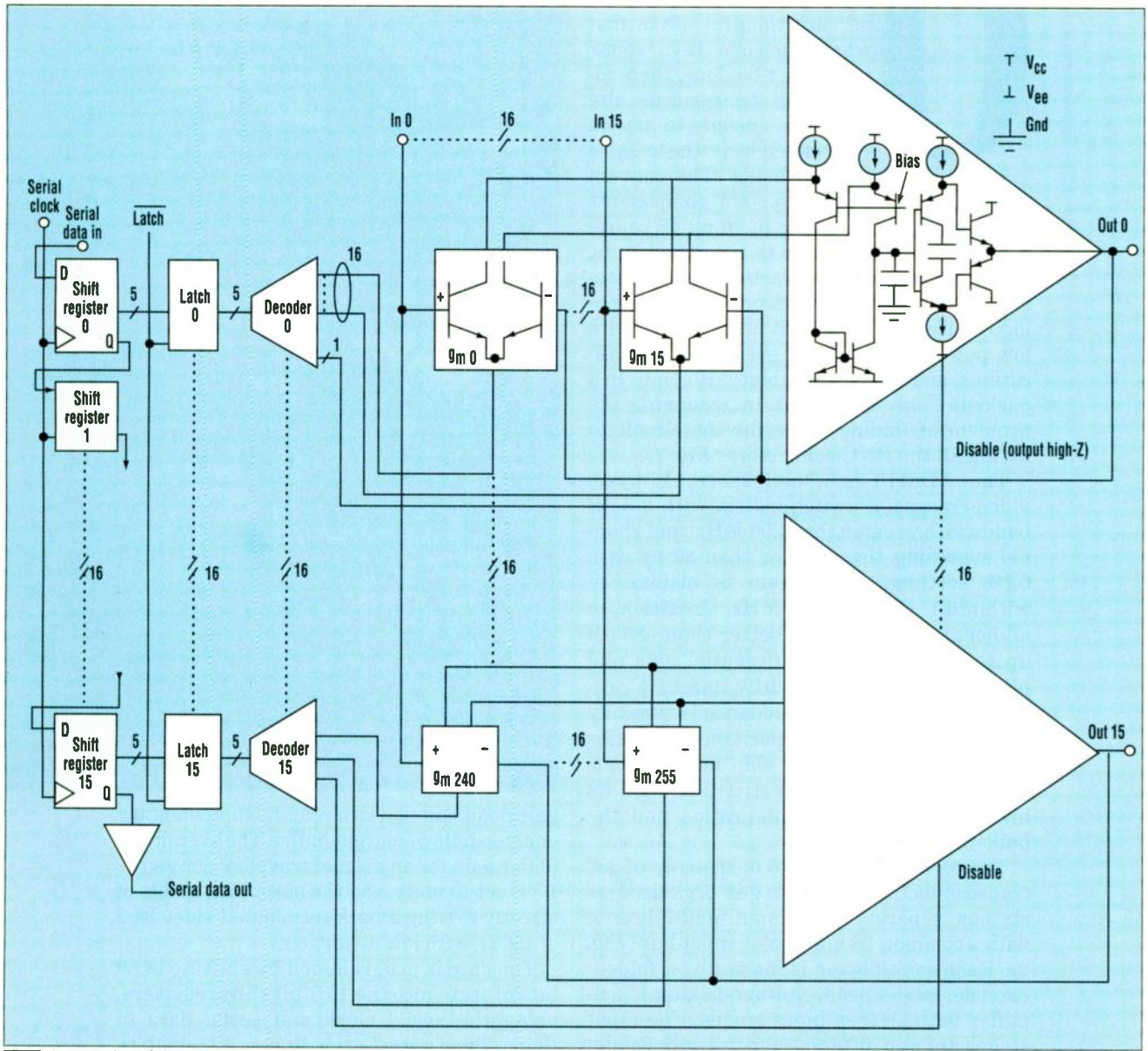
The chip is programmed by shifting in 80 bits of state into the 16 5-bit shift registers, using the serial clock and serial data in lines. Then the Latch line is strobed to change the switch matrix configuration. Reconfiguration time is typically 60 ns

from the falling edge of the $\overline{\text{Latch}}$ signal to the 90% point of output settling. The last bit from the shift registers is brought out at TTL level, as part of the array expansion procedure. A Chip Enable line also is daisy-chained through the IC to offer gating of the serial clock, serial data in, and $\overline{\text{Latch}}$ lines. This technology is used to share the lines among multiple chips, and to select which device to program. A reset line is also provided to disable all the outputs. A power-limitation capacitor can be connected to this pin to minimize possible excessive current drain by competing outputs at power-up. An internal pull-up resistor of 20 kΩ determines, with the capacitor, the enabling time of power-up of the output stages.

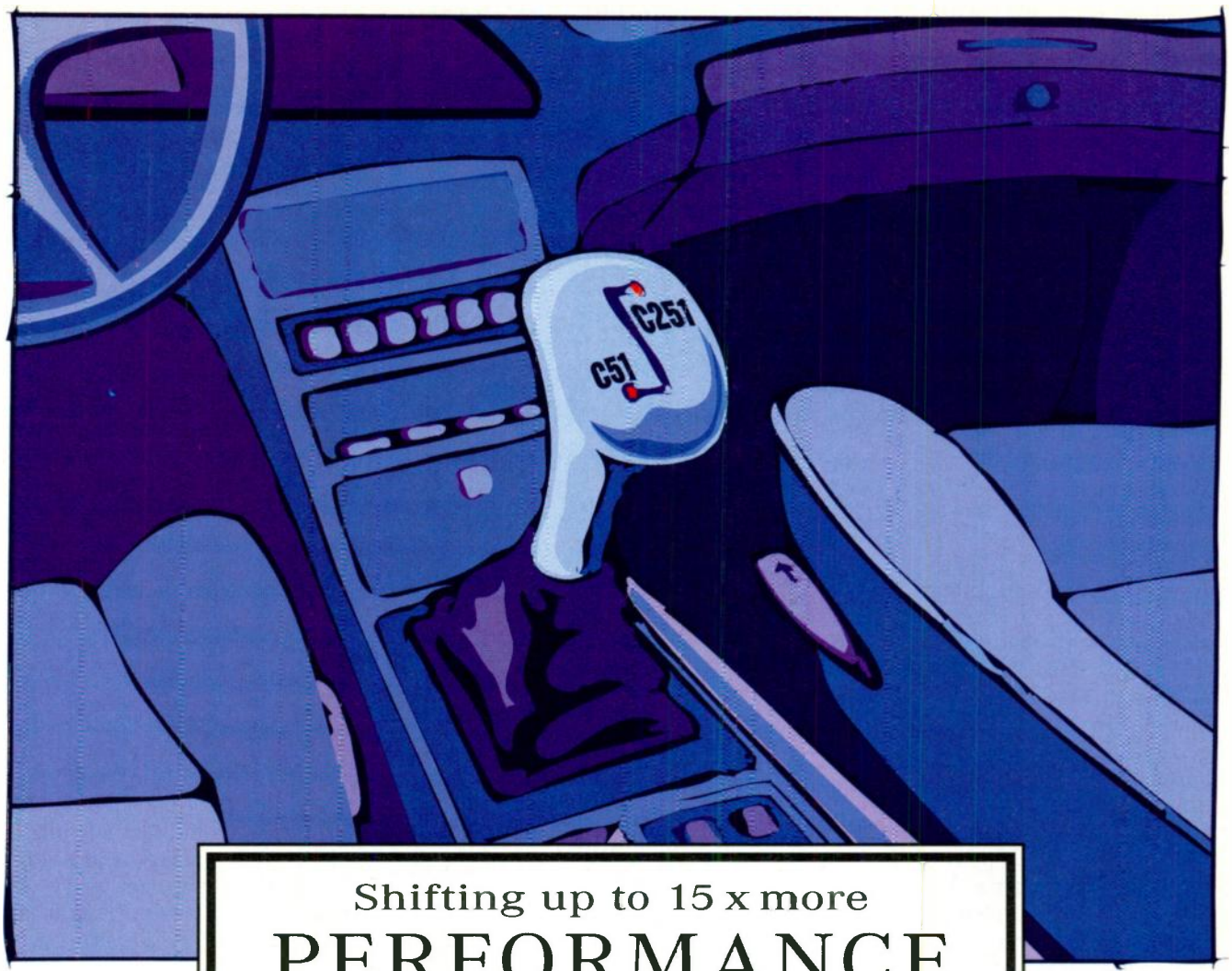
A 5-bit control word feeds 16 output decoders from each of the sixteen latches. The four least-significant bits (LSBs) determine which input is selected by turning on the appropriate stage. A zero in the most-significant bit (MSB) of the control word—fed to the output stage—disables all the input stages and turns the output into a high-impedance state. This action is necessary for coupling larger arrays. The output impedance in this state goes up to 5 MΩ compared to 0.02 Ω when it is enabled. It is expected that the tactile controls associated with the switching would familiar to most of the IC's users.

The AD8116 video crosspoint IC can take inputs up to ±3 V typical, and can output the same. Supply voltage is a nominal ±5 V with an idle current of 90 mA. So, the chip is about a 1-W device. The outputs can supply a typical 40-mA current.

For the majority of users of a crosspoint switcher, the two major specifications are crosstalk and gain matching. As noted, the crosstalk is



1. IN A 128-LEAD TQFP package of only 5/8 by 5/8 in., the AD8116 crams in 256 crosspoints for a video switch with extremely low power consumption per crosspoint.



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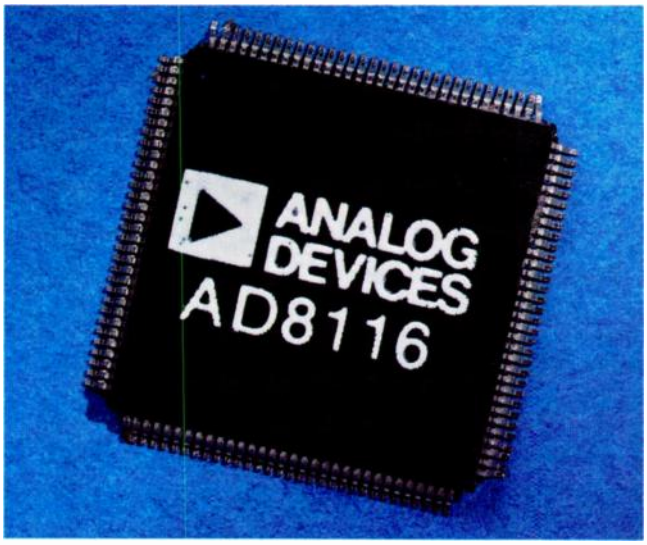
better than 80 dB up to 10 MHz, while the gain matching is better than 0.1% from channel-to-channel with no load, and better than 0.5% with 1-kΩ loading.

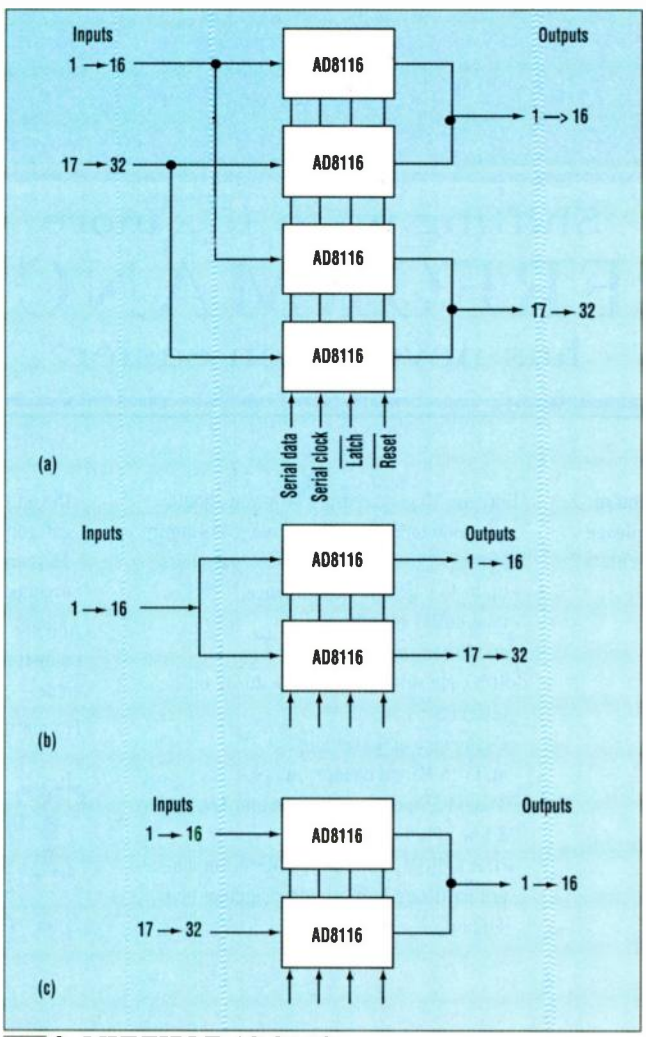
It should always be noted that crosstalk will be dependent on layout. Analog Devices will be making available an evaluation board with Windows software emulation control. There will be lengthy discussions about layout on the data sheet. Considerable assistance has been provided in the way the pin-out of the IC has been chosen. Inputs and outputs are on opposite sides of the device. Pins 1 through 32 form the input side, with every odd-numbered pin being analog ground. Every even-numbered pin is an input connection from pin 2's input 0 up to pin 32's input 15. The outputs are directly opposite the inputs with output 0 on pin 95 and output 15 on pin 65. The even-numbered pins in between output-signal pads alternate between analog V_{CC} and analog V_{EE}.

The side contacts on the package (pins 33 through 64, and 97 through 128) are mostly empty or repeats. The control group is located there, with the daisy-chain connections on both sides. This arrangement allows for the ease of having serial data in and serial data out on opposite sides, or the same side of the IC. Separate digital grounds, digital V_{CC}, and digital V_{EE} pads are provided.

The IC is being specified for a 10-MHz clock rate, but has been tested at higher speeds. The serial data is not I^2C-compatible, but the logic will cope with the inputs being set up with eight differential inputs and outputs. About 25% of the sampled users to date have been designing the chip into component video systems. Since there is no on-board clamping, the IC is suitable for signals with or without syncs. The frequency response also makes it suitable for video systems where the bandwidth is wider than conventional NTSC or PAL interfaces. Applications include high-speed component systems, computer monitors, radar systems, and hotel entertainment systems.



2. THE CORE of the AD8116 crosspoint switch is an array of 256 transconductance (g_m) stages organized as sixteen separate 16:1 input multiplexers with a common 16-line analog input bus.



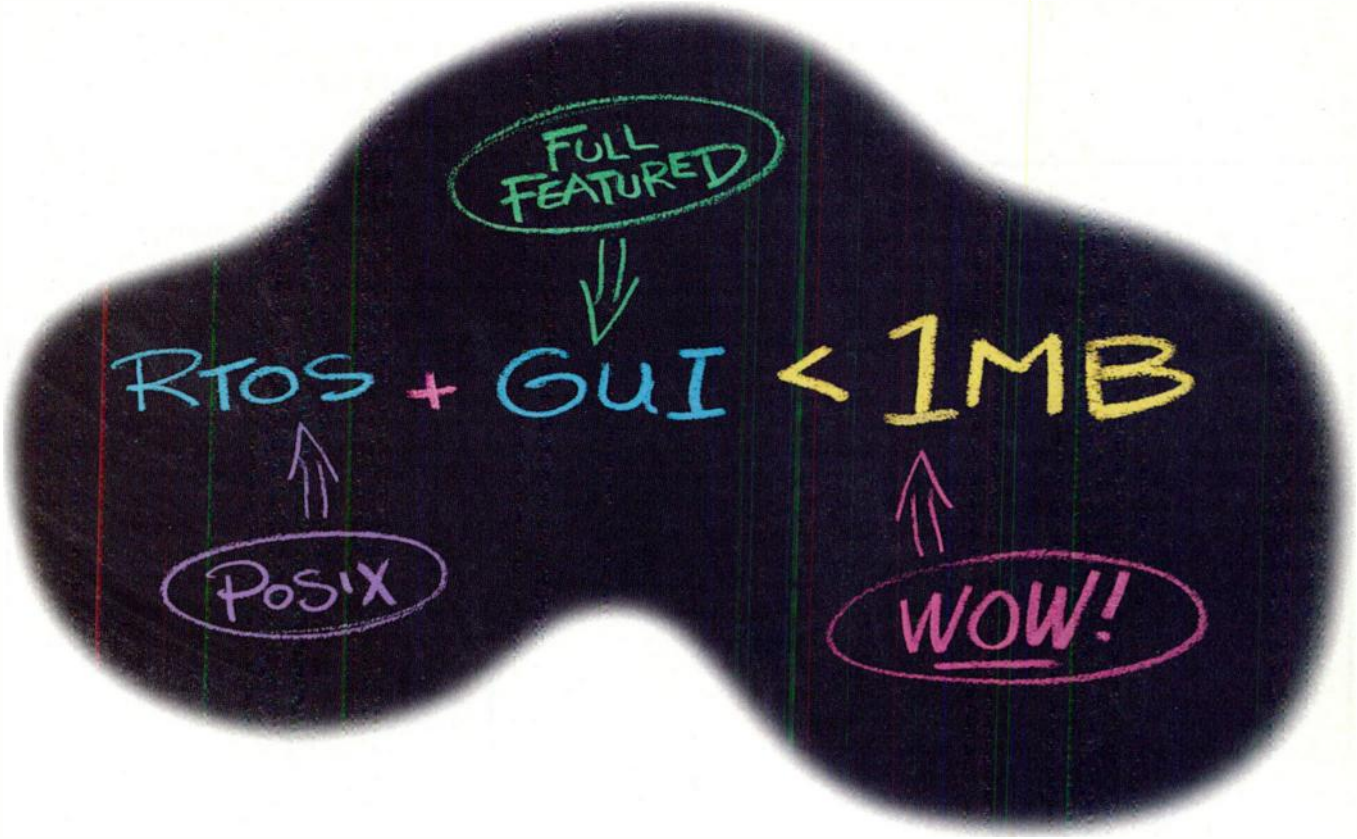
3. MULTIPLE AD8116s can be arrayed to form square or rectangular switches (a). Four ICs can make a 32-by-32 array (b). Two ICs can make a 16-by-32 array, or a 32-by-16 array (c).

The expected markets for the crosspoint will be in the broadcast and near-broadcast markets. The crosspoint also is expected to be used in video-on-demand systems, in-flight entertainment systems, security systems, and video routing for educational areas. In addition, the industrial (internal-defect detection) and medical ultrasound markets are targeted. The majority of these markets represent routing, but the AD8116 is equally suited for production and post-production switchers. It eliminates the on-resistance problems of some systems, and will replace some FET devices. Some interest also has been expressed about the chip's audio applications. In tests, performance has been measured with total harmonic distortion plus noise (THD+N) down at about 100 dB.

In pricing terms, the lowest known alternative cost for a 16-by-16 array is about $160 (about 80% higher than before), while power consumption of the AD8116 is a factor of 7 lower; frequency response of the alternatives is considerably poorer.

MULTIPLE ARRAYS

A 512-by-512 array of AD8116s is already being built. That's 16 32 by 32 devices. Analog Devices feels



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256-CROSSPOINT VIDEO SWITCH

that 1024 by 1024 is perfectly viable. Arrays can be symmetrical or otherwise; in other words, they do not need to be square. A 32-by-32 array would consist of four parts—the serial data, clock, $\overline{\text{Latch}}$, and $\overline{\text{reset}}$ daisy-chained through each *(Fig. 3a)*. Inputs 1 through 16 would be connected to the first and third parts, with inputs 17 through 32 connected to the second and fourth parts. The high-impedance inputs allow for this multiple coupling. Outputs 1 through 16 are taken from the first and second ICs, with the high-impedance disable function allowing outputs to be part of an OR function. The same coupling applies to outputs 17 through 32 from the third and fourth ICs.

A 16-by-32 array would use two parts with the inputs connected to both *(Fig. 3b)*. The outputs are discretely taken from the two ICs while control continues to be daisy-chained between the two. In the opposite rectangle of 32 by 16, the two parts have inputs discretely fed to the two, while the outputs are again OR'd to provide 1 through 16 *(Fig. 3c)*.

The AD8116 is manufactured in Analog Devices' XFCB process (XF is for *Extra Fast*). The XFCB consists of a 1-µm silicon-on-insulator complementary technology, with high packing densities using trench-type isolation. The process exhibits extremely low parasitics, and f_ts higher than 2 GHz. It has proven to be a reliable process since its debut in 1993. It's currently running on 6-in. wafers to produce communications and power-management products. The AD8116 will be the first of a number of crosspoint products, and is particularly distinguished by the fact that it took only 16 weeks from terminal to silicon. □

PRICE AND AVAILABILITY

The AD8116 is available in a 128-lead TQFP and is priced at $90.00 each in 1000-unit lots. Availability is immediate.

Analog Devices Inc., One Technology Way, Norwood, MA 02062; (800) ANALOGD (262-5643) or (617) 461-3392; Internet: http://www.analog.com. **CIRCLE 500**

HOW VALUABLE?	CIRCLE
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MODERATELY	529
SLIGHTLY	530

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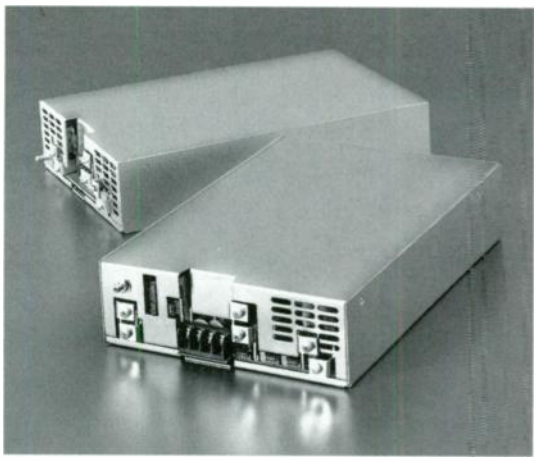
Lambda's PFD Series



Standard 48VDC Input Power Supplies Designed to Meet Bellcore and ETSI Specifications.

Lambda's new PFD Series is designed specifically for telecommunications equipment. They provide multiple output configurations with the industry's widest operating input range (36 - 75VDC), ensuring worldwide operation through worst case input power sags and surges.

The PFD Series is designed with standard features such as current sharing, fan fail detection and input/output signals to provide enhanced system flexibility, reliability and fault tolerant operation. Lambda's PFD Series is available in 32 750W and 1000W packages with a variety of output combinations. And if you don't find the exact output combination that meets your needs, simply call 1-800-LAMBDA-4 for more information on Lambda's UltraFlex™ Series.

The PFD Series is also available in an AC input version in the same package size, which gives system designers the ability to design a single mechanical platform for applications requiring both AC and DC input power.

Lambda introduces standard power supplies that meet Bellcore/ETSI specifications.

The PFD Series for telecom.

36 - 75VDC input range.

750 & 1000W packages.

Multiple outputs.

AC input version available.

LAMBDA Electronics Inc.

PFD Series Standard Full Featured Quad Outputs

MAX POWER	OUTPUT 1 (±10% Adj.)	OUTPUT 2 (±10% Adj.)	OUTPUT 3 (±10% Adj.)	OUTPUT 4 (±10% Adj.)	UNIT PRICE PER DELIVERED QUANTITY 1	10	25	50	MODEL
750W	3.3V @120A	12V @18A	-12V @7A	5V @20A	$1190	$985	$900	$782	**PFD0753-4BH-T**
750W	3.3V @120A	12V @18A	-12V @7A	12V @10A	1190	985	900	782	**PFD0753-4CH-T**
750W	3.3V @120A	12V @18A	-12V @7A	24V @5A	1190	985	900	782	**PFD0753-4DH-T**
750W	3.3V @120A	12V @18A	-12V @7A	48V @3A	1190	985	900	782	**PFD0753-4EH-T**
750W	5V @120A	12V @18A	-12V @7A	5V @20A	1190	985	900	782	**PFD0755-4BH-T**
750W	5V @120A	12V @18A	-12V @7A	12V @10A	1190	985	900	782	**PFD0755-4CH-T**
750W	5V @120A	12V @18A	-12V @7A	24V @5A	1190	985	900	782	**PFD0755-4DH-T**
750W	5V @120A	12V @18A	-12V @7A	48V @3A	1190	985	900	782	**PFD0755-4EH-T**
1000W	3.3V @160A	12V @24A	-12V @10A	5V @20A	1450	1185	1025	919	**PFD1003-4BH-T**
1000W	3.3V @160A	12V @24A	-12V @10A	12V @12A	1450	1185	1025	919	**PFD1003-4CH-T**
1000W	3.3V @160A	12V @24A	-12V @10A	24V @6A	1450	1185	1025	919	**PFD1003-4DH-T**
1000W	3.3V @160A	12V @24A	-12V @10A	48V @3A	1450	1185	1025	919	**PFD1003-4EH-T**
1000W	5V @160A	12V @24A	-12V @10A	5V @20A	1450	1185	1025	919	**PFD1005-4BH-T**
1000W	5V @160A	12V @24A	-12V @10A	12V @12A	1450	1185	1025	919	**PFD1005-4CH-T**
1000W	5V @160A	12V @24A	-12V @10A	24V @6A	1450	1185	1025	919	**PFD1005-4DH-T**
1000W	5V @160A	12V @24A	-12V @10A	48V @3A	1450	1185	1025	919	**PFD1005-4EH-T**

PFD Series Standard Quad Outputs

MAX POWER	OUTPUT 1 (±10% Adj.)	OUTPUT 2 (±2% Fixed)	OUTPUT 3 (±2% Fixed)	OUTPUT 4 (±2% Fixed)	UNIT PRICE PER DELIVERED QUANTITY 1	10	25	50	MODEL
750W	3.3V @120A	12V @18A	-12V @7A	5V @20A	$1090	$900	$810	$730	**PFD0753-4BH-Z**
750W	3.3V @120A	12V @18A	-12V @7A	12V @10A	1090	900	810	730	**PFD0753-4CH-Z**
750W	3.3V @120A	12V @18A	-12V @7A	24V @5A	1090	900	810	730	**PFD0753-4DH-Z**
750W	3.3V @120A	12V @18A	-12V @7A	48V @3A	1090	900	810	730	**PFD7503-4EH-Z**
750W	5V @120A	12V @18A	-12V @7A	5V @20A	1090	900	810	730	**PFD0755-4BH-Z**
750W	5V @120A	12V @18A	-12V @7A	12V @10A	1090	900	810	730	**PFD0755-4CH-Z**
750W	5V @120A	12V @18A	-12V @7A	24V @5A	1090	900	810	730	**PFD0755-4DH-Z**
750W	5V @120A	12V @18A	-12V @7A	48V @3A	1090	900	810	730	**PFD0755-4EH-Z**
1000W	3.3V @160A	12V @24A	-12V @10A	5V @20A	1350	1100	970	866	**PFD1003-4BH-Z**
1000W	3.3V @160A	12V @24A	-12V @10A	12V @12A	1350	1100	970	866	**PFD1003-4CH-Z**
1000W	3.3V @160A	12V @24A	-12V @10A	24V @6A	1350	1100	970	866	**PFD1003-4DH-Z**
1000W	3.3V @160A	12V @24A	-12V @10A	48V @3A	1350	1100	970	866	**PFD1003-4EH-Z**
1000W	5V @160A	12V @24A	-12V @10A	5V @20A	1350	1100	970	866	**PFD1005-4BH-Z**
1000W	5V @160A	12V @24A	-12V @10A	12V @12A	1350	1100	970	866	**PFD1005-4CH-Z**
1000W	5V @160A	12V @24A	-12V @10A	24V @6A	1350	1100	970	866	**PFD1005-4DH-T**
1000W	5V @160A	12V @24A	-12V @10A	48V @3A	1350	1100	970	866	**PFD1005-4EH-T**

Note: 1. Output 4 Option B (5V) is ±10% Adj. Options C, D and E on output 4 are ±2% fixed.
2. For other output voltage combinations, call the factory at 1-800-LAMBDA-4 for more information on Lambda's UltraFlex Series.

Simplify your design.

Lambda's new 48VDC PFD Series is available with the same footprint and input/output connections as the 85 to 265 VAC PFC Series — A single system mechanical design satisfies both AC and DC input power.

To order, or for more information on the PFD Series, call **1-800-LAMBDA-4/5**, 8am to 8pm, east coast time.

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Monterrey
Canadian Co.
TEL: 52-83-882000

Mexico City
Motrek, S.A.
TEL: 52-5-57--9929

Venezuela, Caracas
Vexsing, C.A.
TEL: 58-2-241-0011

Worldwide Website
http://www.lambdapower.com

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L-57A 7/96

LAMBDA Electronics Inc.

515 Broad Hollow Road, Melville, NY 11747-3700
Tel: 516-694-4200 Fax: 516-293-0519

DC Input
36-75VDC.

EMI
Conducted and radiated EMI conforms to EN55022, Curve A; FCC Docket 20780 Part 15 Subpart B, Class A; ETS300 386-1 Part 7.2; Bellcore TR-NWT-001089.

Input Transient Protection
IEC1000/IEC801-4 (Level 5), -5 (Level 3).

Inrush Current

PFD075X	80A
PFD100X	80A

Meets ETS300 386-1 (ETSI)

Input DC Good Signal
Conductance signal from uncommitted opto coupler indicates DC input is above 40.8VDC.

DC Outputs
Voltage ranges are shown in tables.

DC Output Good Signal
Conductance signal from uncommitted opto coupler indicates DC output 1 is within 90% of Vout nominal.

Efficiency
75% typical at V_o nominal, full load, 48VDC$_{in}$.

Regulated Voltage

line regulation	1.0% for line variations from 36 to 75VDC.
load regulation	1.0% for load variations from 10% load to full load and from full load to 10% load on output 1. 5.0% for outputs 2, 3 and 4. 10% pre-load required on output 2 for regulation of all outputs.
ripple and noise (typical)	1.0% of Vout peak to peak.
temperature coefficient	0.03%/°C.
remote programming resistance	1000Ω/volt on output 1, 2 and 4. Output 3 tracks output 2.
remote programming voltage	Volt per volt on output 1, 2 and 4. Output 3 tracks output 2.

Thermal Protection
Internal circuitry protects the power supply against fan failure or excessive ambient temperature.

Overcurrent Protection
Internal circuitry limits all output currents to a safe preset level in the event of an overload or short circuit condition. Upon removal of short or overload condition, normal operation resumes automatically.

Fan Good Signal
Conductance signal from uncommitted opto coupler indicates fan operation.

Output Surge Current
Output 2 can provide a surge current capability equal to three times the rated output current for up to one second, then derating exponentially to steady state value after 10 seconds. The maximum total output power must not be exceeded.

Remote Sensing
Internal sensing allows for remote sensing on output 1 and output 4 (5V option B). Remote sensing allows for 0.625V line drop on +V and 0.125V line drop on -V.

Remote On/Off
Contact closure from remote terminal to -S on output 1 shuts down all outputs of the power supply. Open contact or TTL high signal on remote terminal enables unit.

Redundant Operation
Redundant operation is achieved through external diodes on all outputs.

Cooling
All models are forced air cooled via integral fans.

Operating Temperature Range
0°C to +50°C continuous operation. Derate output power linearly to 50% up to 70°C operation.

Storage Temperature Range
–40°C to +85°C.

DC Output Controls
Multi-turn potentiometers are provided for adjustment over the entire voltage range.

Isolation Rating

Input to Output:	1500VDC
Input to Chassis:	1000VDC
Output to Chassis:	500VDC

Physical Data

Package Model	Lbs. Net.	Lbs. Ship.	Dimensions (Inches)
PFD075x	10.8	12.8	12.0 x 2.65 x 8.0
PFD100x	11.0	13.0	12.0 x 2.65 x 8.0

Options
Consult the factory for additional information on the following options:

Options	Description
N	VME Option
T	Fully Featured Option
PFC	85-265VAC with Power Factor Correction

Please note that on Option T, Current Share, Fan Good Signal, DC Output Good (on all outputs) and Adjustment Capability (on all outputs) are provided.

Option N provides DC Good Signals, Reset and System Reset Signals per IEC1014 and VME specifications.

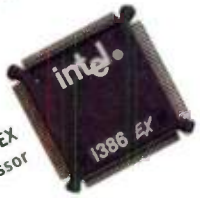
Safety Agency Approvals
The PFD Series is approved for UL1950, CSA 234M90, IEC 950, EN60950 and carries the CE mark (Low Voltage Directive).

Guarantee
One year guarantee includes parts as well as labor. Guarantee applies to operation within the published specifications and recommended application data at the end of one year.

ETSI and Bellcore Compliant	The PFD Series meets the telecommunication specifications for central office equipment, thereby reducing the time and costs associated with obtaining system approvals.
36 to 75VDC Input Range	Wide range input voltage ensures continuous operation through worst case input power sags and surges without the need for external filtering or transient protection circuitry — ideal for global telecom applications
Common Package for AC or DC Input	Both AC and DC input versions have identical footprints, I/O interfaces and mounting holes. Using a single mechanical design platform reduces system design time and cost.
Meets Worldwide Telecom EMI Specifications	The PFD Series meets EN55022 Curve A and FCC Docket 20780 Part 15, Subpart B for conducted and radiated emissions, thereby enhancing system performance and reliability.
Fan Good Signal	Fan Fail Detection combined with internal ambient sensing circuits provides complete system warning, which is critical for fault tolerant applications.
Meets Worldwide Agency Requirements	Safety agency approvals to UL1950, CSA234M90, EN60950, and the CE mark (Low Voltage Directive), simplify the system approval process and accelerate the end products' time to market.
Low Profile	2.65" height provides optimal space allocation.
Remote On/Off	The PFD Series can be activated remotely providing the system designers with flexibility in controlling the power supply.
Input and Output DC Good Signals	Housekeeping circuitry and alarm signals are included as standard features ensuring fail safe system operation.
3.3V Outputs	These standard solutions address the increasing demand for 3.3V logic.
Output Surge Current Capability	Provides high peak current capability on +12V output, ensuring reliable operation for applications using Disk Drives, or highly capacitive or inductive loads.
Remote Sensing	To offset voltage drops in outputs caused by either isolation diodes or load lead losses, all high current outputs have remote sensing capability to ensure load voltage regulates at the required level.

radical technology embedded

New 33MHz Intel386™ EX embedded processor



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Intel's EXPLR2 makes your design work easy. All the hardware you need is fully integrated, so you can start prototyping right away. Better yet, the design-capture files come included. Just cut and paste to create your custom system.

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The EXPLR2 comes with something else. Commitment. With their long-term commitment to embedded applications, Intel, RadiSys, and QNX Software Systems are the right companies to give your designs a real future. **Radical!**

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(to order a board, contact your Intel distributor)

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UPCOMING MEETINGS

MAY

IEEE Custom Integrated Circuits Conference (CICC 97), May 5-8. Santa Clara, CA. Contact Melis Widerkehr, Widerkehr & Assoc., Suite 270, 101 Lakeforest Blvd, Gaithersburg, MD 20877; (301) 527-0902; fax (301) 527-0994.

ELECTRO 97, May 6-8. World Trade Center, Boston, MA. Contact Kathy Lott-Smith, Hickory International, 595 Gilman St., Bridgeport, CT 06605; (203) 334-1397; fax (203) 334-1397.

Electronics Industries Forum of New England, May 6-8. World Trade & Exhibition Center, Boston, MA. Contact Linda Hanson, (914) 779-0696

IEEE Power Industry Computer Applications Conference (PICA), May 11-16. Contact T.C. Wong, American Electric Power, 1 Riverside Plaza, Columbus, OH 43215; (614) 223-2235; fax (614) 223-2205; e-mail: t.wong@ieee.org.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 12-15. Wynham Hotel, Philadelphia, PA. Contact Barry Hornberger, Philadelphia Electric Co., 2301 Market St., Bldg N3-1, Philadelphia, PA 19101; (215) 841-4619.

Fifth IFIP/IEEE International Symposium Integrated Network Management (ISINM 97), May 12-16. San Diego, CA. Contact Ann Marie Lambert, BBN Systems & Technologies, 10 Moulton St., Cambridge, Massachusetts 02138; (617) 873-3819; fax (617) 873-37776; e-mail: isinm97@bbn.com.

IEEE Particle Accelerator Conference, May 12-16. Vancouver, BC, Canada. Contact M.K. Craddock, TRIUMF, 4004 Wesbrook Mall, Vancouver, BC V6T 2A3 Canada; (604) 222-7341; fax (604) 222-7309; e-mail: craddock@triumf.ca.

IEEE Radar Conference, May 13-15. Sheraton University Hotel & Conference Center, Syracuse, New York. Contact Michael Wicks, Rome Laboratory, 26 Electronics Pkwy., Rome, New York 13441; (315) 330-4437; fax (315) 330-2528; e-mail: wicksm@rl.af.mil.

47th Electronic Components & Technology Conference, May 18-21. The Fairmont Hotel, San Jose, CA. Contact Jim Bruorton, Electronic Industries Association, 2500 Wilson Blvd., Arlington, VA 22201-3834; (864) 963-6621.

IEEE Instrumentation & Measurement Technology Conference (MTC 97), May 20-22. Chateau Laurier, Ottawa, Ontario, Canada. Contact Robert Myers, Conference Coordinator, 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OEMed Midwest, May 21-22. Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

OEM Electronics Midwest, May 21-22. Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

Canadian Conference on Electrical & Computer Engineering, May 25-28. Delta Hotel, Newfoundland, Canada. Contact David Collett, Newfoundland & Labrador Hydro, Post Office Box 12400, St. Johns, NF, A1A 4K7, Canada; (709) 737-1372; fax (709) 737-1782; e-mail: t.d.collett@ieee.org.

Fifth IEEE International Conference on Properties & Applications of Dielectric Materials (ICPADM), May 25-30. Sheraton Walker Hill, Convention Center, Seoul, Korea. Contact Joon-Ung Lee, Dept. of Electrical Engineering, Kwangwoon University, 447-1 Wolgye-Dong, Nowon-Ku, Seoul, 139-701, Korea; (82)-2-910-5144; fax (82)-2-942-0107.

JUNE

IEEE International Conference on Neural Networks, June 1-5. Houston, TX. Contact Nicolaos B. Karayiannis, Dept. of Electrical & Computer Engineering, University of Houston, Houston, TX; 77204-4793 (713) 743-4436; fax (713) 743-4444.

IEEE International Conference on Communications (ICC 97), June 8-12. Montreal, Canada. Contact Celia Desmond, Stentor, Fl. 6b, 33 City Center Dr., Mississauga, Ontario L5B 2N5, Canada; (905) 615-6507; fax (905) 615-8421; e-mail: celia.desmond@tc.resonet.com.

IEEE/MTT-S International Microwave Symposium (MTT 97), June 8-13. Convention Center, Denver, CO. Contact John Dunn, Dept. of Electrical & Computer Engineering, University of Colorado, Campus Box 425 Boulder, CO 80309; (303) 492-5920; fax (303) 492-5323; e-mail: dunn@boulder.colorado.edu.

IEEE International Symposium on Circuits & Systems (ISCAS 97), June 9-12. Hong Kong Convention & Exhibition Centre, Hong Kong. Contact ISCAS '97 Secretariat, Department of Electrical & Electronic Engineering, University of Hong Kong, Pokfalam Rd., Hong Kong; (852) 28592710; fax (852) 25598738; e-mail: iscas97@hkueee.hku.hk.

34th Design Automation Conference (DAC 97), June 9-13. Anaheim Convention Center, Anaheim, CA; Contact MP Associates Inc., 5305 Spin Rd., Suite A, Boulder, CO 80301; (303) 530-4333; fax (303) 530-4334.

IEEE International Conference on Consumer Electronics (ICCE), June 11-13. The Westin Hotel O'Hare, Rosemont, IL. Contact Diane D. Williams, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397.

International Solid-State Sensors and Actuators Conference (Transducers 97), June 15-19. Hyatt Regency Hotel, Chicago, IL. Contact Kensal D. Wise, 1246 EECS Building, University of Michigan, 1301 Beal Ave., Ann Arbor, MI 48109-2122; (313) 764-3346; fax (313) 747-1781.

IEEE Digital Cross Connect Systems Workshop VII (DCS 97), June 16-19. Banff Park Lodge, Banff, Alberta, Canada. Contact James H. Simester, Lucent Technologies, P.O. Box 3030, Room 4J-526, 101 Crawfords Corner Rd., Holmdel, NJ 07733-3030; (908) 949-7336; fax (908) 949-2724; e-mail: sims@bostare.ho.att.com.

ELECTRONIC DESIGN
QUICK LOOK
EDITED BY MIKE SCIANNAMEA AND DEBRA SCHIFF

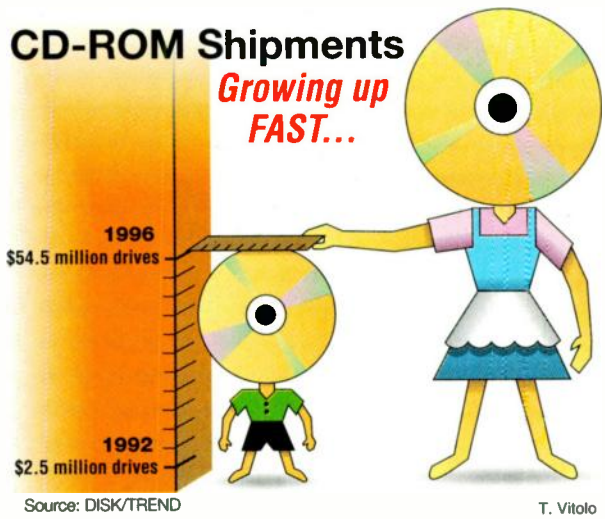
MARKET Facts

Talk about a growth spurt...

Jumping from 2.5 million in 1992 to 54.5 million in 1996, worldwide CD-ROM drive shipments have experienced quite a growth spurt. According to the 1996 DISK/TREND Optical Disk-Drive Report, read-only drives make up 94.6% of all optical disk-drive shipments in 1996, while writable drives provide 3.6% of the worldwide total of 57.6 million drives.

DISK/TREND's projections say that although shipments of DVD-ROM drives will start at the end of 1996, they are not expected to surpass CD-ROM drive shipments until 1999.

CD-ROM drives are expected to have short life cycles as manufacturers scramble to saturate the market with faster drives. In 1995, quad-speed drives drove the market taking 74.5% of CD-ROM drive shipments. This year, 6X and 8X drives will be 78% of the shipment market. Projections estimate that by 1998, CD-ROM shipments will be dominated by 10X and 12X drives. But, by 1998, overall CD-ROM drive shipments will decrease as DVD-ROM drives make their market impact.



Writable drive shipments topped 0.5 million in 1995. It is expected that the count for 1999 will be over 4 million drives shipped, but with a great change in the market makeup. CD-R write-once drives are expected to account for 41.8% of writables in 1996. PD drives, using rewritable or read-only disks, are projected to take 57% of the 1996 writable count. Rewritable DVD drives are expected to eat up one-third of the writable market in 1999.

DISK/TREND separates their optical disk drives with read/write capability into two product groups: above and below 2 Gbytes in drive capacity. In 1995, rewritable 3.5 in. drives with less than 2 Gbytes of space hit 0.5 million units shipped, and in 1999, shipments are expected to rise to nearly 1.3 million. Through 1999, 5.25-in. drives under 2 Gbytes are expected to be shipped at a declining rate, while their 2 Gbytes plus counterparts will be experiencing rapid growth.

CD format disk libraries are becoming more of a presence, seeing shipments of 337,000 in 1995. Forecasts are pegging disk libraries at 1.5 million shipments in 1999. Those libraries designed for conventional optical disks are projected to grow, with the models featuring 1-39 disk capacity leading the pack.

Priced at $1990, the 1996 DISK/TREND Report on optical disk drives is available via their website: http://www.disktrend.com or by contacting DISK/TREND, 1925 Landings Dr., Mountain View, CA 94043; (415) 961-6209; fax (415) 969-2560.—*DS*

WOW! Looking For A Job On The 'Net

Employment opportunities are opening up in many areas of technology, especially in the wireless industry. According to industry sources, over a thousand new employees are hired each month in the wireless arena. But where, besides the Sunday papers, do you look to find these jobs? In fact, there is a new source on the Internet for prospective employers and employees to find each other, and WOW, it may just the ticket to a new opportunity.!

The World of Wireless Communications (WOW-COM) is one of the most comprehensive sites on the Internet for the wireless industry (http://www.wow-com.com). Its newest addition is the Career Center, designed to help fill the industry's need for applicants in all job categories. Some of the companies that are currently advertising in the center are Bell Atlantic NYNEX Mobile, Ericsson, Motorola, QUALCOMM, and Sprint PCS.

The Career Center is a forum that showcases companies and the best applicants. Each job listing includes complete information regarding job title, location, job description, qualifications, salary and benefits packages, and contact information. WOW-COM is a project of CTIA, an association serving the wireless telecommunications industry.

For more information, contact WOW-COM at 1250 Connecticut Ave., NW, Suite 200, Washington, DC 20036; (202) 736-2993; fax (202) 785-0721; e-mail Wccareer@ctia.org.—*MS*

QUICKLOOK

QUICK NEWS

Obit—On October 6, the computer industry lost a legend. Seymour Cray, father of the supercomputer, died as a result of injuries sustained in a car accident. Cray was 71.

Born to a civil engineer in Chippewa Falls, Wis., in 1925, Cray showed an affinity for electrical devices at an early age. He enlisted in the Army after graduating from high school, just in time for the Battle of the Bulge.

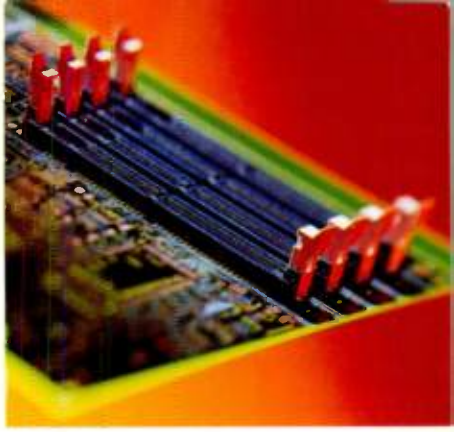
Once home, Cray studied electronics at the University of Minnesota, earning a bachelor's degree in electrical engineering and a master's in mathematics. After graduation in 1951, Cray stayed in Minnesota, joining the team at Engineering Research Associates (ERA). ERA also was home to computer legend John Von Neumann, father of the modern computer. ERA saw the development of Cray's Reduced Instruction Set Computing (RISC). IBM has been identified as the inventor of RISC, despite evidence that Cray's computers were designed with the technique during his tenure at ERA.

After ERA had been acquired by Sperry Rand, Cray left to join ERA's founder in his new concern, Control Data. Supporting his legendary solitary-engineer working technique, he designed the CDC 1640—the first transistor-based computer. He eventually moved his Control Data lab back to Chippewa Falls to remove himself from the corporate structure and develop the CDC 6600. This computer functioned at three million ips, surpassing IBM's 7094 model. Before taking his team from Control Data to begin his Cray Research Company, he designed the CDC 7600 and the unreleased 8600.

Cray Research is best known for creating the Cray 1 supercomputer which was later used in military applications. The Cray 1 quickly became the benchmark for competing developers. In the mid-1980's, both the Cray 2 and the Cray X-MP (designed by Steve Chen) were released to the market.

By the end of the 1980's Cray's Cray 3 project, based on gallium arsenide chips, had cost Cray Research over $120 million. Cray left the company in 1989, taking the Cray 3 and a 10% investment in the project from Cray Research, and moved to Colorado Springs, Colo. to found Cray Computer Corporation. In the 1990's, however, the new company began a rapid decline. With the advent of the cheap microprocessor chip and the end of the cold war, Cray's huge systems became pieces of history. In March, 1995, Cray Computer filed Chapter 11.

There are many sites featured on the World Wide Web that provide detailed information about Cray, ranging from interviews with the Smithsonian to in-depth discussions about the Cray 1 and its progeny. But, mostly Internet users will find constant credit being given to Cray as one of the most influential people in computer history.



Once it's locked into place, your memory modules aren't going anywhere. That's because our DIMM sockets are uniquely designed with dual ejector latches that lock in memory modules, eliminating macro- and micro-motion. For more information on Molex's DIMM sockets, call 1-800-78MOLEX

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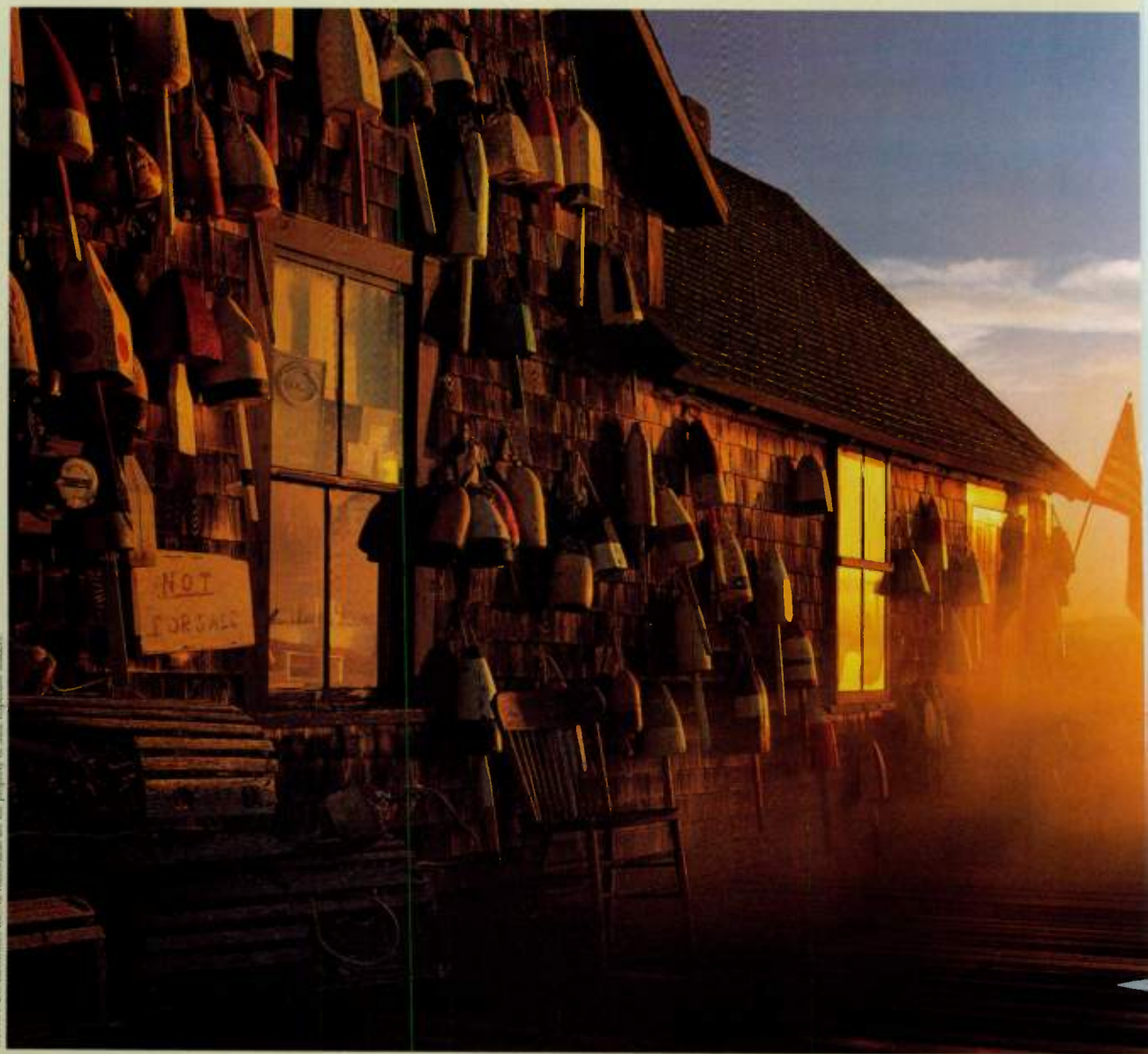
Visit our web site at http://www.molex.com

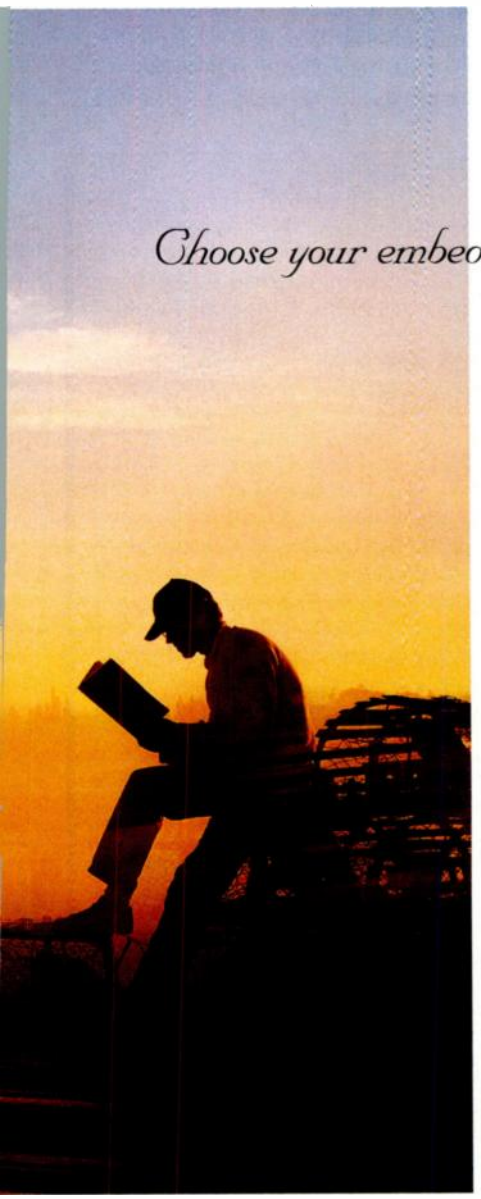
IN EVERY PRODUCT
YOU LEAVE A



	VR4300	PPC603	VR5000	PPC604
Frequency	133MHz	80MHz	200MHz	100MHz
Bus Interface	32-bit	32/64-bit	64-bit	64-bit
I-Cache Size D-Cache Size	16KB 8KB	8KB 8KB	32KB 32KB	16KB 16KB
Pin Count/Package	120 PQFP	240 CQFP 256 BGA	272 BGA 223 CPGA	304 CQFP 256 BGA
SPECint92/SPECfp92	80/60	75/85	---	---
SPECint95/SPECfp95	---	---	5.5/5.5	3.29/n/a
Price in 1,000 Qty *	$45	$195	$300	$549

*PowerPC prices from PowerPC FAQ, 12/17/95. Prices subject to change.

YOU design PIECE OF YOURSELF.



Choose your embedded processor wisely.

What is it about you?

You, who are engaged in a struggle between the clock and the design and yourself. You. The one who will never yield. Is it because you are always searching for a better way? Or is it the idea of this intimate part of yourself empowering others? Could that be the thing that pushes you?

Whatever the reason, one thing is certain. Only the best will make it into your design. So we ask that you consider NEC's V_R4300™ and V_R5000™. Two outstanding embedded processors. Each one providing far better MIPS per dollar than the PowerPC™ 603 or 604.

Frankly, there's no slowing the momentum behind NEC's 64-bit V_R Series.™ In fact, the V_R4300 and V_R5000 have been selected by leading printer, internetworking and video game companies.

A very persuasive fact. But there are others. For example, our programs for companion chipsets. If getting your product to market is a big concern, NEC's V_R4300 and V_R5000 will get you there fast. Because NEC will give you a comprehensive solution, including support for PCI Bus interface and laser printer control peripherals. We've even assembled the third-party tools. So you'll be able to realize your design faster than you ever dreamed possible.

There's something else you can expect from NEC: Scalability. The V_R Series uses a common code library, enabling "forward compatibility." Which makes it easy to upgrade to the latest generation of processor. An important fact when you consider just how many new processors are being developed in the V_R Series. Not to mention the incredible investment you have in developing code.

Call us for more information about the V_R Series at *1-800-366-9782*. Ask for Info Pack 195.

Because we know it's not just a design you're working on. It's personal.

V_R5000. Paramount performance, incredibly affordable. This is the ultimate embedded processor for advanced applications like internetworking.

V_R4300. A high level of performance at an extremely low price. Ideal for office automation products, video games and X-terminals.

NEC

READER SERVICE 123

Offers You Can't Refuse

HEURIKON CORP. has released a white paper that provides an overview of the trends and technologies affecting the telephony market. Entitled "A Vision for the Advanced Intelligent Network," the paper examines business trends of the Advanced Intelligent Network (AIN), including the future of billing, the affect of cable modems, and the shift of ownership of AIN components. Also featured is a look at open systems, including upgrading the SS-7 network and the evolving telephony infrastructure. For a free copy of the white paper, contact Heurikon Corp., 8310 Excelsior Dr., Madison, WI 53717; (608) 831-5000; fax (608) 831-4249; Internet: http://www.heurikon.com.

WARNER ELECTRIC is now offering drive designers a software package that guides users through a step-by-step selection process that produces a drive solution based on the use of off-the-shelf components. "Sizing and Selecting Software for SECO AC/DC Drives" consists of three 3.5-in. diskettes that allow the designer to determine the optimal drive based on products, specifications, or application. The software includes Help screens that provide details on specific products, a glossary of terms, and application engineering information. To obtain a free copy of the software, it can be dowloaded directly from the WeCell BBS or by contacting the Warner Electric Advertising Dept., 449 Gardner St., South Beloit, IL 61080; (815) 389-3771; fax (815) 389-2582; WeCell BBS: (815) 389-6440; Internet: http://www.industry.net.warner.electric.

TRUDEL *to form*

We have been discussing the consequences of two disparate business strategies. Most of the world is into "faster, cheaper." I called this group "the Dilbert firms." These are doomed. They decline into the "nerd-in-Hell" behavior that Jim Adams pokes fun at in his popular comic strip.

The leaders reject that approach. They prefer strategies that "add value and expand the market." This group includes names like Intel, Microsoft, and Hewlett-Packard.

Remember rule #1: The only factor that adds value is knowledge. Peter Drucker said it well: "Knowledge has become the key economic resource and the dominant, if not the only, source of competitive advantage."

Unfortunately, the Western concept of knowledge is very shallow. "I took a class, therefore I know the subject." What nonsense! Our educational system is a national disgrace.

About half of our workforce is illiterate. Our high-school graduates have test scores below those from countries like Spain and Ireland. Even graduate school students are sometimes pushed through with automatic Bs. Unfortunately, neither political party is apparently up to the challenge or pain of fixing these problems.

The knowledge that Drucker and I speak of is deeper. It comes from classes, books, experience, soft science, technology, relationships, and intuition. The Japanese aggressively move their promising people across functional roles. They don't do this because it is fun or cheap; they do it to build mastery.

Masters learn to perceive things that can't be seen, and to quickly grasp and intuitively react to complex changing environments in real time. Few Western MBAs—under-sciencied, and trained in financial abstractions—learn true mastery of technology based business.

"How should we compete with those that pay third-world wages?" My core answer is, "Don't compete where you can't win." I recommend reading Stephen Covey's book, "7 Habits of Highly Effective People," and I endorse his concept of "win/win or no deal."

Did I hear, "Easy for you to say, Trudel?" No, it isn't easy. But it is worthwhile, and it has integrity.

A large firm needed to sort out an emerging market based on new technology. Instead of retaining me, they paid someone who "knew the market" (which had not happened yet, I note) to fill out a form with the numbers that corporate wanted, to do the project that engineering wanted. It "saved" them $30,000, but launched a misguided project that cost over $2 million before it was shut down.

For a product example, consider the garment industry. How can Western firms win in markets where children sew garments for pennies a day? They use knowledge. In this case they use HDTV, CAD systems, and automatic laser cutters to get new fashions on the rack in a week. By the time the sweatshops have copied these, they are on to the next fashion.

Cost matters, of course. If you cannot eventually become the low cost, high quality supplier, your entire market is at risk. Still, the core job of management, marketing, and design teams should be to get out of the zone of commodity competition. If you cannot add some unique value for your customers, you should seriously question why you are in business.

Most important, capitalism can't work without property ownership. You can't make money if other firms are free to steal your knowledge, designs, and intellectual property. That is why the patent wars should matter to you.

John D. Trudel, CMC, provides business development consulting and is the author of the book "High Tech with Low Risk." He is founder and director of The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; phone (503) 640-5599; fax (503) 543-6361; e-mail johntrudel@aol.com; Internet: http://members.aol.com/johntrudel/index.htm.

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When it comes to OTP microcontrollers, narrow your choice and go with the best. Mitsubishi offers the widest range of 8- and 16-bit, low-power, high-performance OTP (One-Time-Programmable) MCUs. We help you save costs and enable powerful embedded solutions with unique combinations of on-chip features – a rich array of functions you won't find anywhere else.

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Model Number	On-Chip ROM/RAM	Series Features
M37471	8~16KB / 128~384B	Small package, battery operation, A-D converter, Serial I/O
M38002	4~32KB / 192B~1KB	High integration, low power
M38063/67	4~48KB / 192B~1KB	A-D/D-A converter, UARTs
M38203/207	4~32KB / 192B~1KB	On-chip LCD driver, battery operation
16-bit OTP Microcontrollers		
M37702	16~32KB / 512B~1KB	Easy upgrade path from 8-bit performance, very low power, 3 volt operation, A-D converter, UARTs, 8 timers, 16 MByte of memory space & more

All our OTP MCUs are fully software compatible, providing an easy migration path between hundreds of Mitsubishi MCU products. Mitsubishi OTPs are supported by a complete line of third-party development tools, low-cost designer kits and qualified programming houses. And now there's a totally new channel for customer service and support – Covenant Electronics, Inc. (CEI) – to give you faster delivery from on-hand stock. For OTP MCU solutions that put you in control of your destiny, narrow your choice. Call (888) 428-9234.

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READER SERVICE 151

CRISIS AT 2000

End of Century Spells Potential Disaster

Ok, I'll concede that it's exciting to be alive near the turn of the century, but discovering that my bank account's status could be threatened (even more than usual) because 90% of all computer applications will be affected by the Year 2000 (Y2K) date change is having a negative affect.

The problem throwing corporations worldwide (not to mention programmers, analysts, and hip consumers) into a tailspin is the date field defining the chronological year. Twenty years ago, due to memory and storage space constraints, many of today's legacy systems were fashioned with a two-digit century value within the date field. The two-digit system does not distinguish between the 20th and 21st centuries, which means that in the current date field, computers are going to read 1900 for what should actually be 2000 information.

Businesses that do not correct this situation are going to see many of their computerized operations either aborted or severely erroneous. But, since many of the decision makers are generally not the same individuals who use the systems on a daily basis, they're greatly underestimating the impact of the date change. Perhaps the business leaders ought to be informed of potential litigation that could arise—there's even talk that the entire financial community could collapse if a solution is not found in time.

There are estimates of hundreds of billions of dollars dedicated to addressing the Y2K date change. For example, at the going rate of $1.00 per line of code, a healthy IT structure could be facing upwards of $75 million worth of conversion costs. That's not even taking into account the upgrades for applications, operating systems, and software.

There are many World Wide Web sites littered with Y2K FAQs. Several of them have links to seminar pages, so if it's in the budget, there are places to go and products to see while there's still time. One site in particular offered a resident program for DOS and Windows that corrects the date change flaw of the CMOS RTC in AT-class PCs and PS/2s, 286 through Pentium and clones. But, the program, Year2000.EXE, does not address Award v4.50 series BIOS (which means my pre-November 1995 Pentium system is just plain out of luck). Year2000.EXE is a component of RighTime, a system clock manager that addresses AT-class PCs' Y2K problems. Year200.EXE can be downloaded for free (for personal useage only, businesses must buy the licensed version) at http://rampages.onramp.net~~-gt-becker.

One of the many groups involved in helping companies survive the date change dilemma is Computer Technology Research Corp. (CTR), Charleston, South Carolina. CTR has recently released a 230-page report, "The Year 2000 Crisis: Developing a Successful Plan for Information Systems," that gives some history of the problem, potential business consequences, compliance information, and proposed solutions. The report is priced at $290 and can be ordered via CTR's site at: http://www.ctrcorp.com or by contacting Computer Technology Research Corp., 6 North Atlantic Wharf, Charleston, SC 29401-2115; (803) 853-6460; fax (803) 853-7210. -

DS

OFF THE SHELF

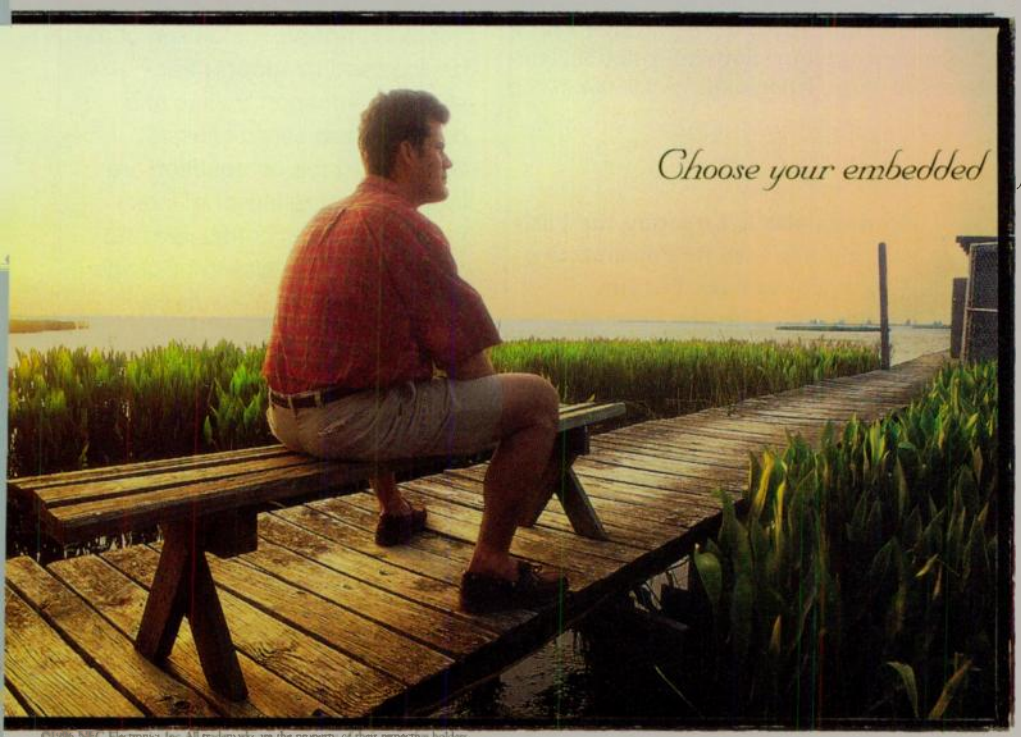
"The Handbook of Walkthroughs, Inspections, and Technical Reviews" shows readers how to implement reviews for a wide range of product and software development. The book outlines procedures to conduct walkthroughs (or peer-group reviews), inspections, and technical reviews, with extensive checklists for each type of material reviewed, including specification, design, and code reviews. The 464-page book is priced at $54.70. Contact Dorset House Publishing, 353 W. 12th St., New York, NY 10014; (800) 342-6657; fax (212) 727-1044; e-mail 71702.1415@compuserve.com.

"The Windows NT Security Handbook" approaches security from the Windows NT operating system, and addresses issues such as protective features within Windows NT, as well as potential security holes. Readers will also learn how to develop security strategies on Windows NT networks, and how to keep an eye on illicit activity that may indicate the presence of hackers. Other topics that are discussed include encryption techniques, constructing firewalls, and discovering viruses. The 512-page book is priced at $29.95. Contact Osborne/McGraw-Hill, 2600 Tenth St., Berkeley, CA 94710; (800) 227-0900; fax (510) 549-6603; Internet: http://www.osborne.com.

"YOU GET TO THAT POINT IN THE PROJECT AND IT HITS YOU.

YOU HAVE THE POWER TO *change* SOMEONE'S LIFE."

ROGER BRINGMANN, Ph.D., *Executive Director of Research*, QMS



"Sounds pretty noble, doesn't it," Roger Bringmann said. "But that's the motivation."

processor wisely.

"In typical QMS™ fashion, we set the goals high for our new printers: make our customer's job easier, help them do it faster, or in the case of a network administrator, painlessly. To get there, we needed twice the performance of the fastest controller card. But it absolutely had to be cost effective.

It all came down to one processor: NEC's 64-bit VR4300.™ Don't think we handed it to them on a silver platter. We went through an extensive evaluation process. And after rigorous testing of three processors--on real world applications--it became clear that NEC would blow the market apart. None of the other processors came close to NEC's price delta and performance. Not Intel™ or PowerPC.™ In fact, the VR4300's 64-bit architecture with the 32-bit interface not only reduced our system costs, it also allowed us to use existing 32-bit code.

The other thing that impressed us was the great things we saw coming down the road for the VR4300. For the entire VR Series,™ in fact. But let me tell you, there are innovative ideas running throughout that entire organization.

Which is why we're putting our brains together--QMS and NEC. Creating new ways to make someone's job a little better."

Call for more information about the VR Series at *1-800-366-9782.* Ask for Info Pack 195.

The QMS 2425 printer with NEC's VR4300 processor received the PC Magazine Editors' Choice award.

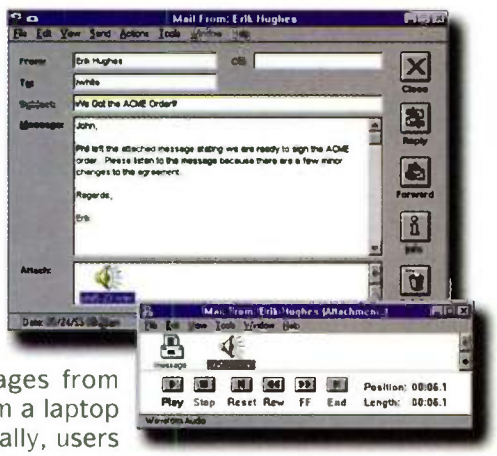
NEC

READER SERVICE 172

HOT PC PRODUCTS

THE INTERNET EXPLORER ADMINISTRATION KIT 3.0 is a tool kit for customizing Microsoft's World Wide Web browser. Currently, the kit is available in English and Japanese formats, with Chinese, French, German, Italian, and Korean versions to follow. Using the Administration Kit, Internet service providers and businesses alike can add their company names or logos to the browser. Users also can create a single-click installation package of Internet Explorer 3.0's components. Additionally, the kit allows users to manage browser settings from a central server. The Administration Kit supports Internet Explorer 3.0 for Windows 95 and Windows NT, as well as Internet Explorer 2.1 for Windows 3.1. There also will be a version to support Internet Explorer 2.1 for Macintosh. Except for shipping and handling fees, the Administration Kit is free via Microsoft's Internet site: http://www.microsoft.com/ie/ieak/. For more information, contact Microsoft Corporation, One Microsoft Way, Redmond, WA 98052-6399; (800) 457-9530

StarMax is the result of Motorola's teaming with Apple Computer. The new Mac clone is based on the PowerPC microprocessor, which Motorola and Apple developed with IBM. The StarMax computers range from $1600 to $3600, with keyboard and mouse, but no monitor. The package does include a five-year warranty. In addition to the StarMax line, Motorola also is targeting the business market with its PowerStack PC line. PowerStack PCs run Windows NT with the PowerPC microprocessor. These units will range from $2500 to $5000, also carrying the five-year warranty. For more information, contact Motorola Computer Group, 2900 S. Diablo Way, Tempe, AZ 85282; (602) 438-3000.



CALLWARE 5.2 AND CALLWARE VIEWPOINT 5.2 are software products that allow voice-mail messages to be attached to e-mail messages. A LAN-based solution, CallWare allows voice-mail servers to link up to the Internet. The Visual Messaging system lets users view and access their messages from the desktop PC as well as from a laptop in a remote location. Additionally, users can play their messages over the phone or through a multimedia device (complete with Play, Record, Rewind, Fast-Forward, and Pause commands). Volume and speed can be adjusted via the Play Dialog Box. Text-to-speech functionality is now an option since CallWare Technologies has integrated its Intranet Telephony Suite with Berkeley Speech Technologies' text-to-speech software, BeSTspeech TTS/Soft. BeSTspeech creates computer-generated synthetic speech on demand from ASCII text to read typed information. For more information, contact CallWare Technologies, 2323 Foothill Dr., Salt Lake City, UT 84109; (801) 486-9922; Internet: http://www.callware.com.

Back To SCHOOL

A full college scholarship will be awarded to the high school student who designs the best design solution to a real-world engineering problem in the first National Engineering Design Scholarship Competition (NEDSC).

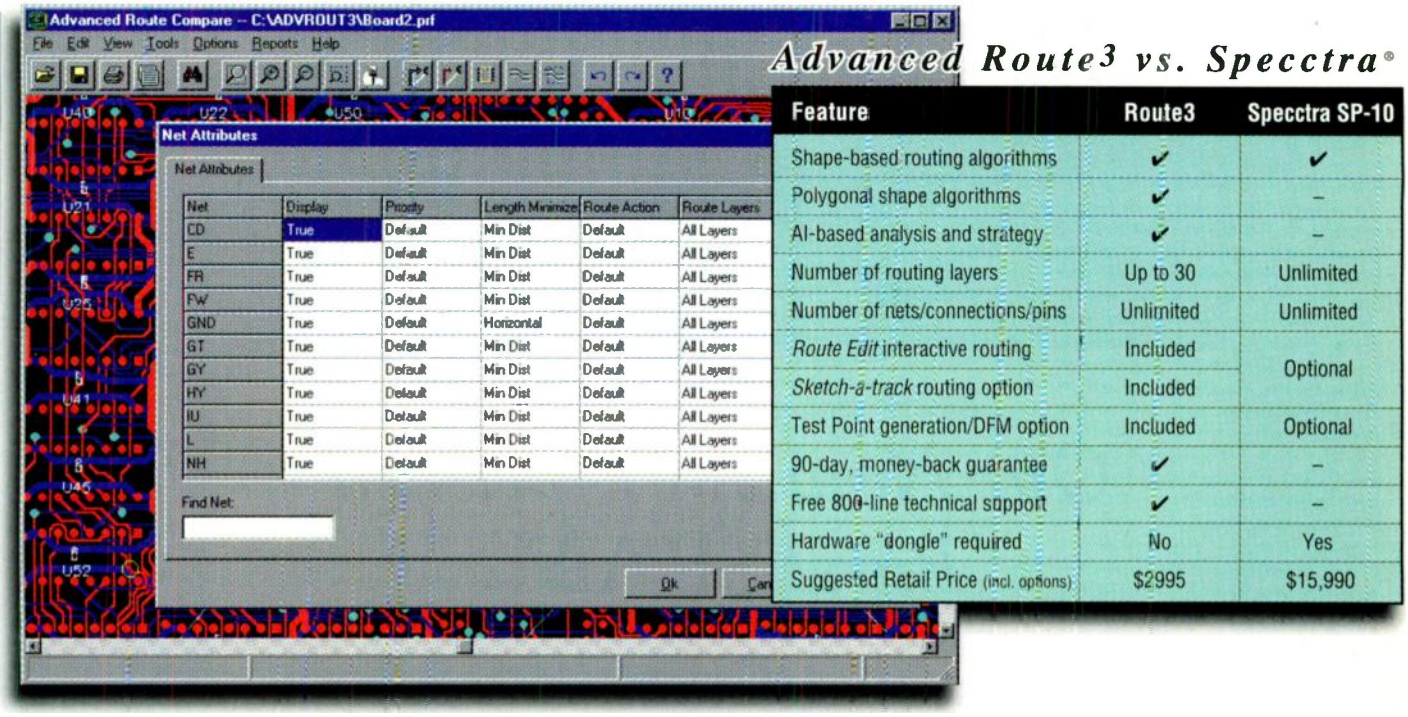
The competition challenges students to improve the design of a device used to support free-standing transport trailers and containerized cargo chassis. Sponsoring the competition are Interpool Inc., a lessor of intermodal dry cargo containers and chassis, and the Newark College of Engineering at New Jersey Institute of Technology (NJIT).

Top prize is a four-year, full-tuition scholarship to NJIT's Newark College of Engineering (valued at $43,500 out-of-state and $24,500 in-state). Second prize is one four-year half-tuition scholarship, and four third prizes of $250 in cash also will be awarded.

Student must be U.S. citizens or permanent residents of the United States and currently attending high school. Enrollment in the Newark College of Engineering is required before scholarship prizes are awarded. A teacher must sign an affidavit that the student's work was unassisted. Registration deadline is December 9, 1996, and all work must be postmarked before February 17, 1997.

For more information, contact the Competition Coordinator, Newark College of Engineering, NJIT, University Heights, Newark, NJ 07102-1982; (201) 596-3434; fax (201) 596-2326; Internet: http://www.njit.edu.

Shaped-based routing from Protel®



Advanced Route3 vs. Specctra®

Feature	Route3	Specctra SP-10
Shape-based routing algorithms	✔	✔
Polygonal shape algorithms	✔	–
AI-based analysis and strategy	✔	–
Number of routing layers	Up to 30	Unlimited
Number of nets/connections/pins	Unlimited	Unlimited
Route Edit interactive routing	Included	Optional
Sketch-a-track routing option	Included	
Test Point generation/DFM option	Included	Optional
90-day, money-back guarantee	✔	–
Free 800-line technical support	✔	–
Hardware "dongle" required	No	Yes
Suggested Retail Price (incl. options)	$2995	$15,990

Shaped-based routing made easy

There are really only two types of PCB autorouters: shape-based routers and all the rest. Today's designers understand that only shape-based routing has the power to automate large, complex and mixed technology designs. Protel *Advanced Route 3* brings you the power of shape-based routing without all the shape-based complexity. Using *Advanced Route 3,* routing is as easy as loading a placed design file and pressing the *Run* button - no "do" files to edit, no "cost" decisions and no problems. Our shape-based router takes over, analyzes the layout, chooses the appropriate routing strategy and races to 100% completion for most designs. It's faster, just as powerful as the competition and much, much easier. Plus, designers tell us that they prefer *Advanced Route 3*'s efficient diagonal routing provided by our advanced polygonal algorithms.

If you're currently using Protel, PADS, Pcad, Massteck or Racal design systems, Protel has an affordable shape-based solution for your routing needs too.

Contact Protel for details.

1-800-544-4186
www.protel.com

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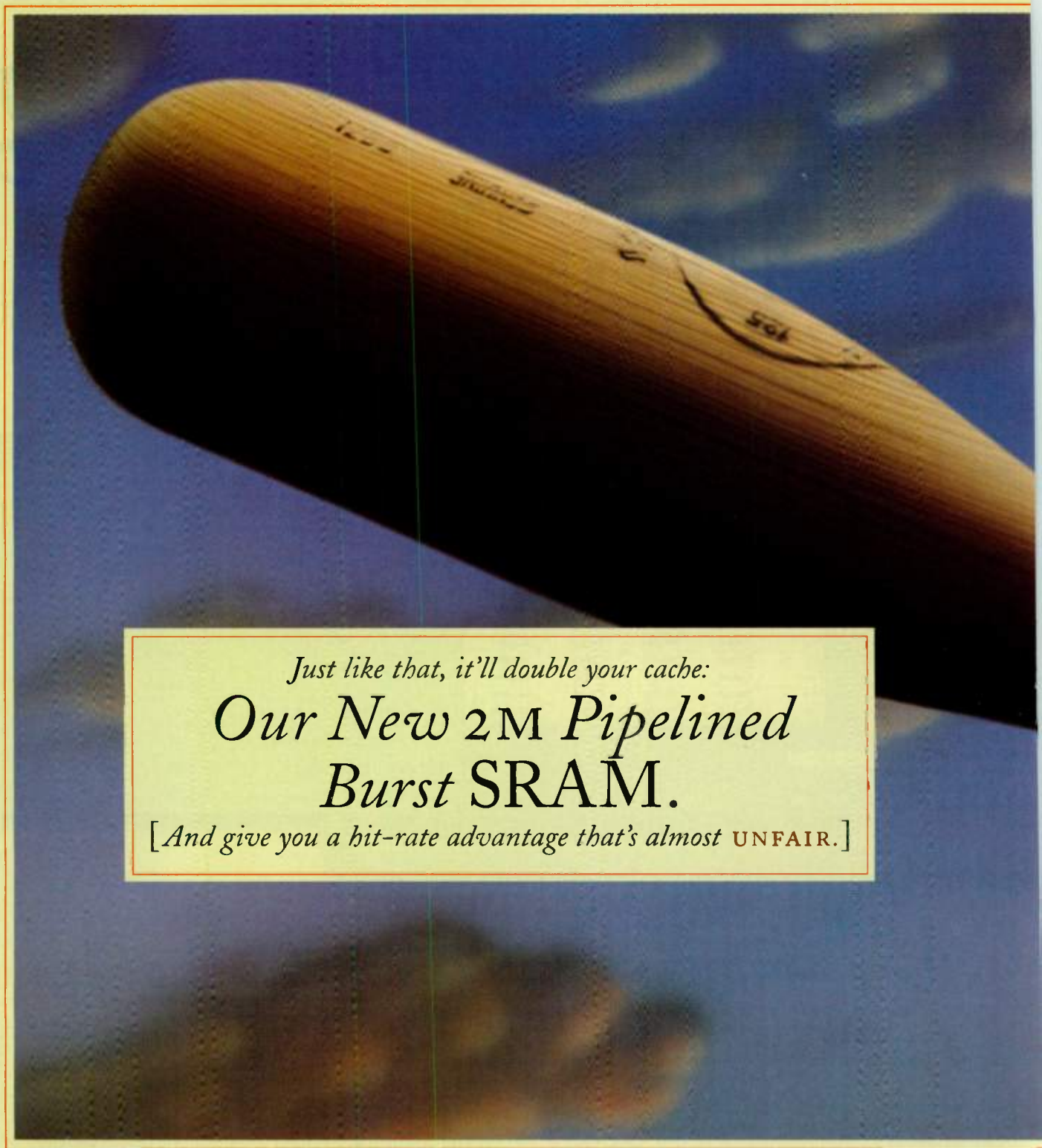
FIRST IN WINDOWS EDA



Just like that, it'll double your cache:

Our New 2M *Pipelined Burst* SRAM.

[*And give you a hit-rate advantage that's almost* UNFAIR.]

Juiced ball? Corked bats? Ridiculously oversized strike zones?

Whatever went on this past baseball season, expect to start seeing comparably astronomical hit rates in PCs.

Because at Samsung, the industry-standard design for PC cache SRAMs—synchronous pipelined burst—is now available in a double-sized density: 2 megs.

This is the design that's cost-effective. The design that gives Pentium-based systems the performance they were meant to have. And the design that we at Samsung pioneered to spark an entire revolution in PC configuration.

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We offer the 2M pipelined burst part for 133-MHZ and 100-MHZ systems, and we also offer a flow-through synchronous version for 100-MHZ systems.

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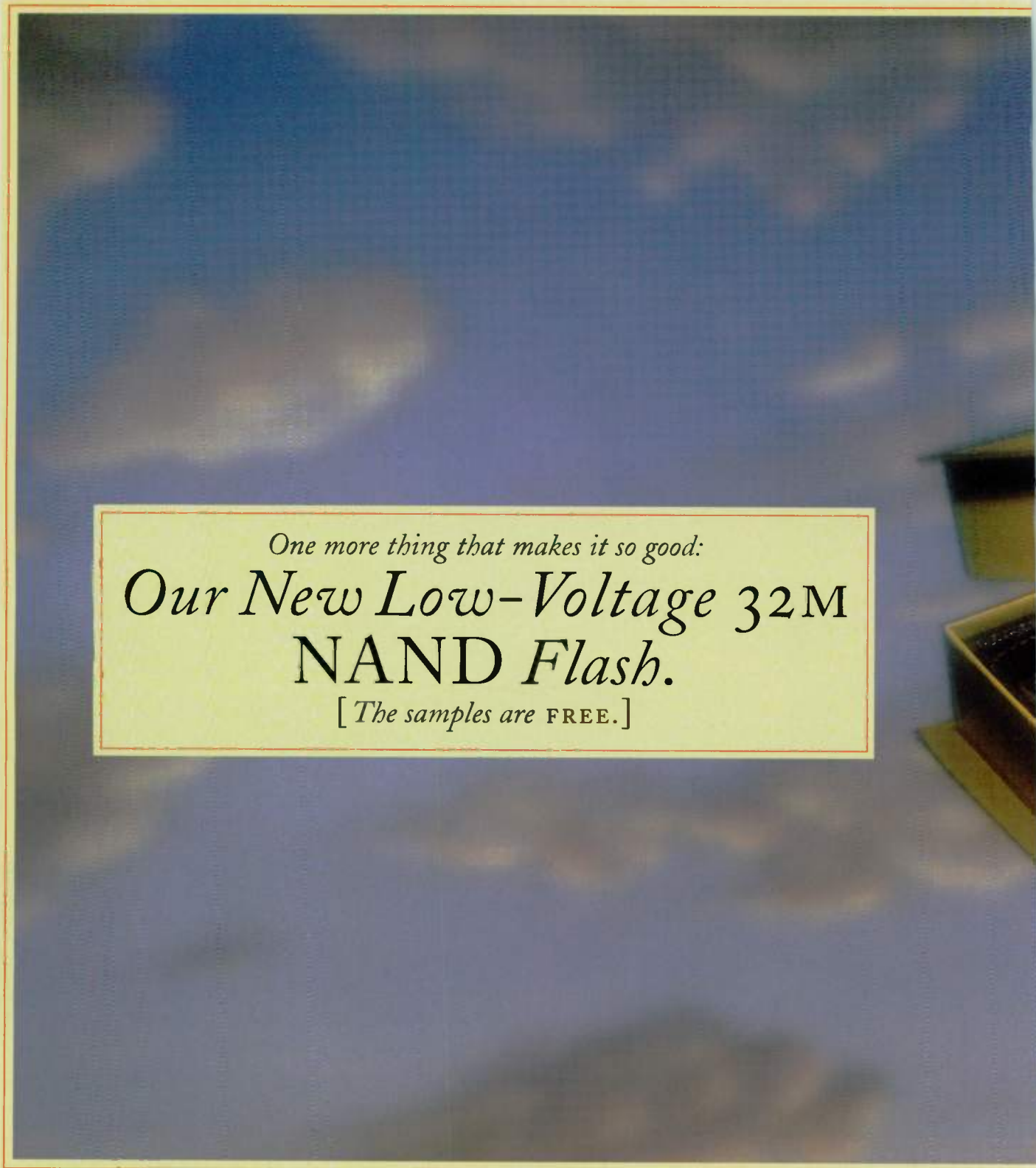
READER SERVICE 190



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(and in the case of the samples—a *lot* less).

A sweet part indeed.

Beyond that, with this new NAND Flash, Samsung is extending its leadership position in memory in one more way—something we plan on doing for a long time to come.

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QUICKLOOK

HOT PC PRODUCTS

The Epson Expression 636 is a 36-bit color scanner that is available in four different configurations, targeting the business, graphic arts, and power markets. The Expression 636 comes bundled with TrueScan, Epson's proprietary technology that features improved, vibrant color, tighter image reproduction, and fast scanning speeds. TrueScan recognizes over 68 billion colors, with a maximum resolution of 4800 by 4800 dpi. Additionally, the scanner comes with PhotoQuick technology which turns photo negatives into positive images. Epson offers the Expression 636-Executive for the PC and Expression 636-Executive for the Mac for $899, the Expression 636-Pro for the PC and Expression 636-Pro for the Mac for $1799, and the Expression 636-Artist for the PC and Expression 636-Artist for the Mac for $1299. All of the packages come with full version software for creating graphically rich presentations. For the professional who already has all the software he/she needs, Epson also offers the Expression 636 upgrade, available for under $799. The upgrade only includes the scanner, drivers, and cable. For more information, contact Epson America Inc., 20770 Madrona Ave., Torrance, CA 90503; (800) 463-7766; Internet: http://www.epson.com.

QUICK NEWS

By The Sea—Two new Travan drives from Seagate Technology are external storage solutions targeting the home and small office market. TapeStor 800 and TapeStor 3200 tape drives hold up to 800 Mbytes (compressed) and 3.2 Gbytes (compressed) of data per cartridge, respectively. The drives are bundled with Tape-it software. Tape-it uses the drag-and-drop mechanism to activate the TapeStor drives in both backup and fully-functional removable storage applications. The software was developed by PGSoft. It works in conjunction with Windows 95 and 3.x, bringing the drive up as a letter icon, just like the hard, disk, or floppy drives. The TapeStor drives' external closure and retail packaging were designed by frogdesign inc., of Apple Macintosh and Acer Aspire fame. The blue TapeStor drives stand upright, saving precious desk space. The TapeStor 800 retails for $149 and the TapeStor 3200 retails for $249.

For more information, contact Seagate Technology Inc., P.O. Box 66360, 920 Disc Dr., Scotts Valley, CA 95066; (408) 438-6550; fax (408) 429-6356; Internet: http://www.seagate.com.

Fabulous Fabless—New numbers from the Fabless Semiconductor Association (FSA) have lowered the three-year compounded annual growth rate for silicon wafers from 40% to 30%. The revised Wafer Demand Survey (the first publication of the survey this year came out in March) brings the 1996 wafer demand down from 39% growth over 1995 to 14%. Companies who responded to the survey cite slower overall demand, customer inventory issues, yield improvements, and the availability of more advanced technologies for the reduction in growth forecasts. Still, 30% of the fabless concerns that responded to the survey met or exceeded their earlier forecast. For the survey, Ernst & Young asked 56 fabless companies to give actual wafer purchase for the first half of 1996, compared to the forecasted purchases and a revised estimate, if necessary, of the third and fourth quarters, as well as 1997 and 1998.

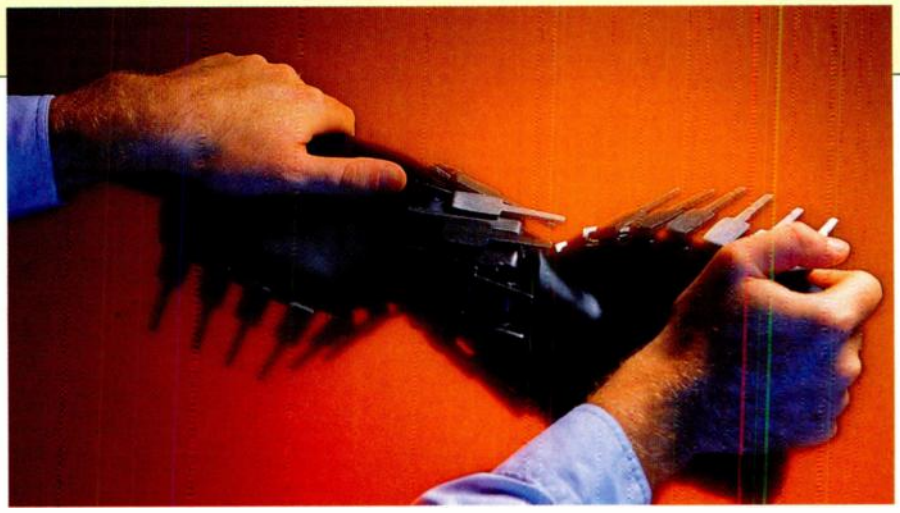
For more information, contact the Fabless Semiconductor Association, 13355 Noel Rd., Suite 1345, Dallas, TX 75240; (972) 239-5119; Internet: http://www.fsa.org/info.

Itsy-Bitsy Regulators—Meeting market demand for smaller packages with greater battery efficiency, two new ICs from National Semiconductor, the LP2981 and the LP2982, are housed in TinyPak SOT23 packages. The LP2981 is the first linear regulator specified for 100-mA output current and 150-mA transient peak output from within a TinyPak package. The LP2982 reduces output noise to 30μV typical. Applications such as RF circuitry in cordless and cellular phones are ideal for the the LP2982 regulator. Allowing National's new regulators to extend battery life and minimize circuit board space are low dropout voltages (120 mV at 50 mA output current for the LP2981) and the TinyPak package. There is also a sleep mode which brings quiescent current down to less than 1μA (max) over temperature. Other applications include liquid-crystal displays, modems, portable PCs, and disk drives. The LP2981 units are priced at $1.50 apiece, and the LP2982 is priced at $0.85 apiece, when purchased in lots of 1000.

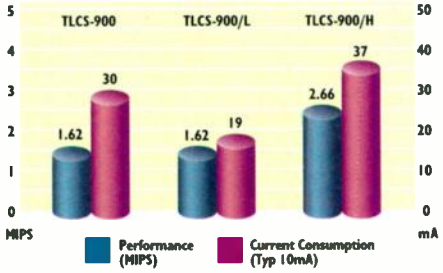
For more information, contact National Semiconductor Corporation, 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; (408) 721-5000; Internet: http://www.national.com.

Toshiba TLCS-900 16-bit Microcontroller Family

When you've squeezed your current micro for all it's worth.



You've milked it for every last drop of functionality. Now it's time to take a look at Toshiba's new 16-bit family of microcontrollers, which will give you the perfect combination of performance and integrated peripherals.



The TLCS-900 increases performance four times over a typical 8-bit MCU, while the higher-performance TLCS-900/H is eight times faster. The low-power TLCS-900/L rounds out the family. All are highly integrated, featuring on-chip peripherals that include A/D and D/A converters, DRAM controllers, serial interfaces, real-time clocks, and ROM, RAM or Flash memory. This degree of integration yields a lower parts count, reduced system costs and increased reliability.

The flexible architecture of Toshiba's 16-bit micros means ample room for expansion without having to add design steps to the process. So while the core size of the current TLCS-900 is one of the smallest available, in the future when it's reduced even further there won't be any design change requirements. And because of its flexible architecture, we're able to offer numerous derivatives. We can also provide a complete suite of development tools, as well as a number of third-party tools.

So if increased performance, flexible architecture, a wide peripheral mix, low power and competitive pricing sound appealing, look to Toshiba's TLCS-900 16-bit microcontroller family. For more information, call us at 1-800-879-4963, or visit us on the Web at **www.toshiba.com/taec**.

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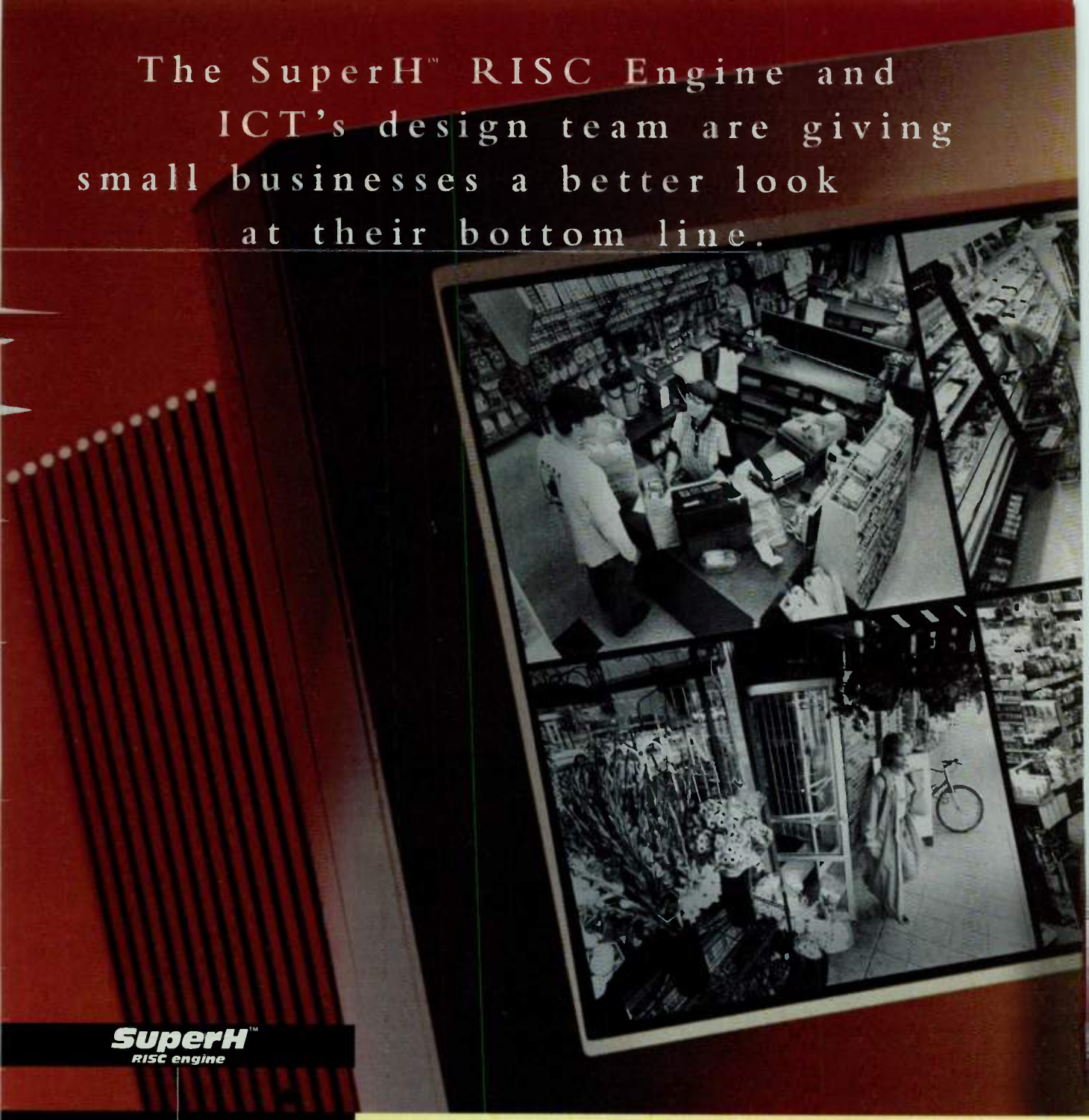

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The SH-1 embedded processor allowed ICT to build a remote-controlled, 16-camera, 32-bit video surveillance system that provides remote access to people who could never before afford it.

A Better Way to a Bigger Market. Designers at International Communication Technology (ICT) of Los Angeles, Calif. were justifiably proud of their PC-accessible, remote-controlled, video-surveillance system. But in defining their system roadmap, ICT realized that with a few added key features, and a lower system cost, they could hit the sweet spot in American business: the more than seven million small- to mid-size organizations that normally couldn't afford a system like theirs.

Custom logic was too expensive, used too much space and took too long to meet ICT's next-generation target. So they got creative. With the Hitachi SH-1 processor, ICT found they could solve their problem with software and a powerful, cost-effective RISC processor that offered a very high level of integration.

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A Bottom Line with a Future. ICT can sell their new PRO System 3A for just a quarter of the cost of its closest competitor! For ICT, there's another bottom line: without sacrificing their investment in code, their product roadmap now includes the ability to migrate performance or features upward or downward, virtually without limits.

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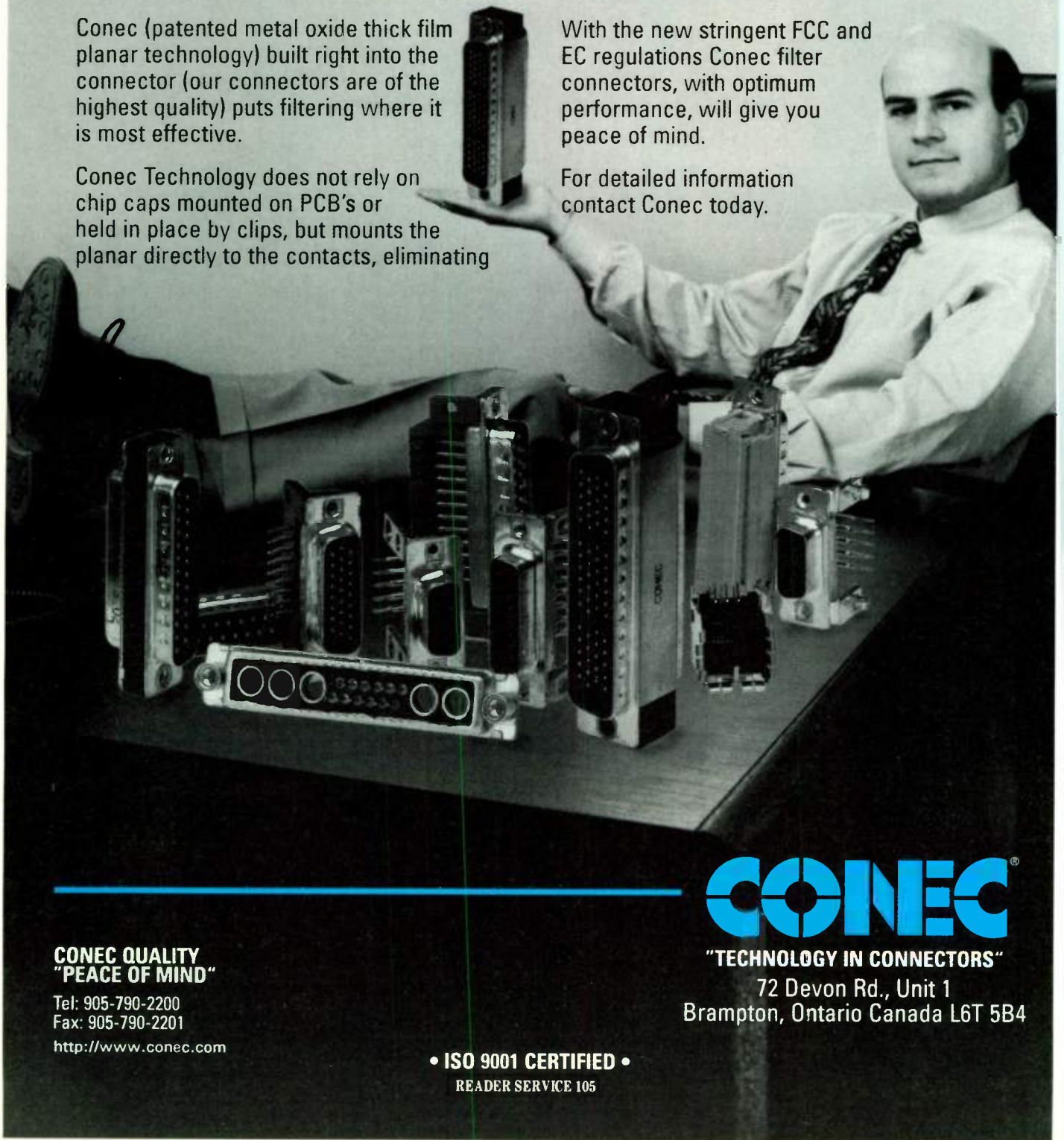

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QUICKLOOK

INTERNET NEWS

CERTICOM CORP. has updated its Elliptic Curve Cryptosystem (ECC), a feature of the Information Security Classroom section of its World Wide Web site. One interesting aspect of the section is the Java applet allowing the visitor to draw elliptic curves and select points.

ECC's high bit strength and efficiency minimize the requirement for large key sizes. The public-key system also is suited for such challenging security applications as high-volume web servers, smart cards, and wireless communications.

Designed to give an in-depth introduction into the field of information security technology, the Information Security Classroom has responded to feedback from visitors of the computer and communications industries' as well as government agencies by including more information about the next generation of public-key cryptography.

Certicom plans to include cryptographic components used by third-party developers to integrate ECC into their products and applications in their web site updates. Other features of the site include a section dedicated to Standards, and a link to the Institute of Electrical and Electronics Engineers (IEEE) site.

For more information, contact Certicom Corp., 200 Matheson Blvd. W., Mississauga, Ontario, Canada L5R 3L7; (905) 507-4220; fax (905) 507-4230; Internet: http://www. certicom.com.

LUCKMAN INTERACTIVE has acquired WebEdit, the web-page authoring tool for Microsoft Windows, from Nesbitt Software. Luckman will be supporting WebEdit as a standalone product through its web site.

WebEdit is an easy-to-use HTML editor that uses a WYSIWYG (What You See Is What You Get) preview window to directly edit the code. The editor supports the newest tags, including HTML 3.2.

Some WebEdit features include a customizable toolbar, dialog boxes, right-mouse activated menus, a help desk complete with HTML references and glossary, and Wizards. The Wizards can create frames and tables of contents, validate links, and enter multimedia features. Multimedia features that are supported include audio, video, JavaScript, and animation. In addition, WebEdit also includes an FTP feature that automatically copies all open documents to the web site, ensuring accurate updating.

Other features the full-feature editor sports include a spell checker, user-defined tag support, and multiple document design.

For more information, contact Luckman Interactive Inc., 1055 W. 7th St., Los Angeles, CA 90017; (213) 614-0966; Internet: http://www.luckman.com.

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Global Positioning Systems (GPS) are revolutionizing every aspect of travel, from hiking and boating to cross-country trucking. One of the greatest areas of impact is within the aviation community, where many pilots are routinely using inexpensive, handheld GPS units in preference to the traditional radio navigation equipment found in most planes. To get some perspective on this trend, the technicians at QuickLook Labs (actually, just me) extensively tested the SkyBlazer XL, manufactured by Magellan Systems Corp., San Dimas, CA.

About the size of a Walkman, the SkyBlazer's simple control panel and display make using its sophisticated features easy, even for the novice user. Within a few minutes after opening the box, I was out in the parking lot, getting a lock on the GPS constellation overhead. Even from a cold start, the unit quickly acquired its position and I was able to track my progress while walking across the parking lot.

The receiver has been designed especially for aviation applications, and features a ROM-based database of every airport and navigational aid in North America. (Other databases are available for operation in Europe and other parts of the world.) The XL's user interface has been optimized to reduce the effort required to access and read its various displays quickly and accurately—no small thing when things get busy in the cockpit.

The unit's basic navigational functions can be easily scrolled by using the four arrow keys on each side of the screen. Its moving map display functions can be used to present the pilot with critical information such as airspace diagrams, airspace boundaries, and runway diagrams. Besides illustrating the runway as seen from the air, the on-board database provides critical information about an airport, including radio frequencies for approach, tower, and ground control. Other cool features include a glideslope display, wind-drift correction functions, a flight planning calculator, and a "NEAREST" panic button that immediately lists the 10 closest airports.

In the interest of fully evaluating the XL, I volunteered to use it under actual flight conditions. The test involved piloting a light aircraft on a flight to and from an electronics conference in Boston—about 250 miles each way. Programming the receiver for the flight was easy, adding only a few minutes to the normal flight planning chores. The XL's memory has room for 20 flight plans, each with up to 20 waypoints along the way. A waypoint is defined as an airport, a navigation aid from the unit's database, or one of 200 user-programmable locations stored in its nonvolatile memory.

The XL proved easy to install and use, even in the cramped confines of the 4-place rental aircraft. The factory-supplied yoke clamp allowed it to be mounted on the plane's steering wheel, and its external power adapter was connected to the plane's electrical system to conserve the four-hour life of its internal batteries. For in-cockpit operation, its flip-up quadrafillar antenna can be removed and a remote active antenna can be attached with a 9-foot coaxial cable. The remote antenna's suction cup mount allows the XL to attach to either the windshield or dashboard, allowing it an unobstructed view of the sky for optimum reception.

During the trip, the XL was initially used as a backup for the rental plane's traditional center-the-needle-and-pray VOR radio navigation receivers, but the pilot (me) rapidly came to rely on the GPS system with the VORs playing second fiddle. The XL's easy-to-read primary navigation screen gives you a simulated directional gyro indicator that shows the current course of your plane with respect to your next waypoint. The same screen also supplies you with distance-to-target, time-to-target, ETA, ground speed, and numerical readouts of heading and bearing.

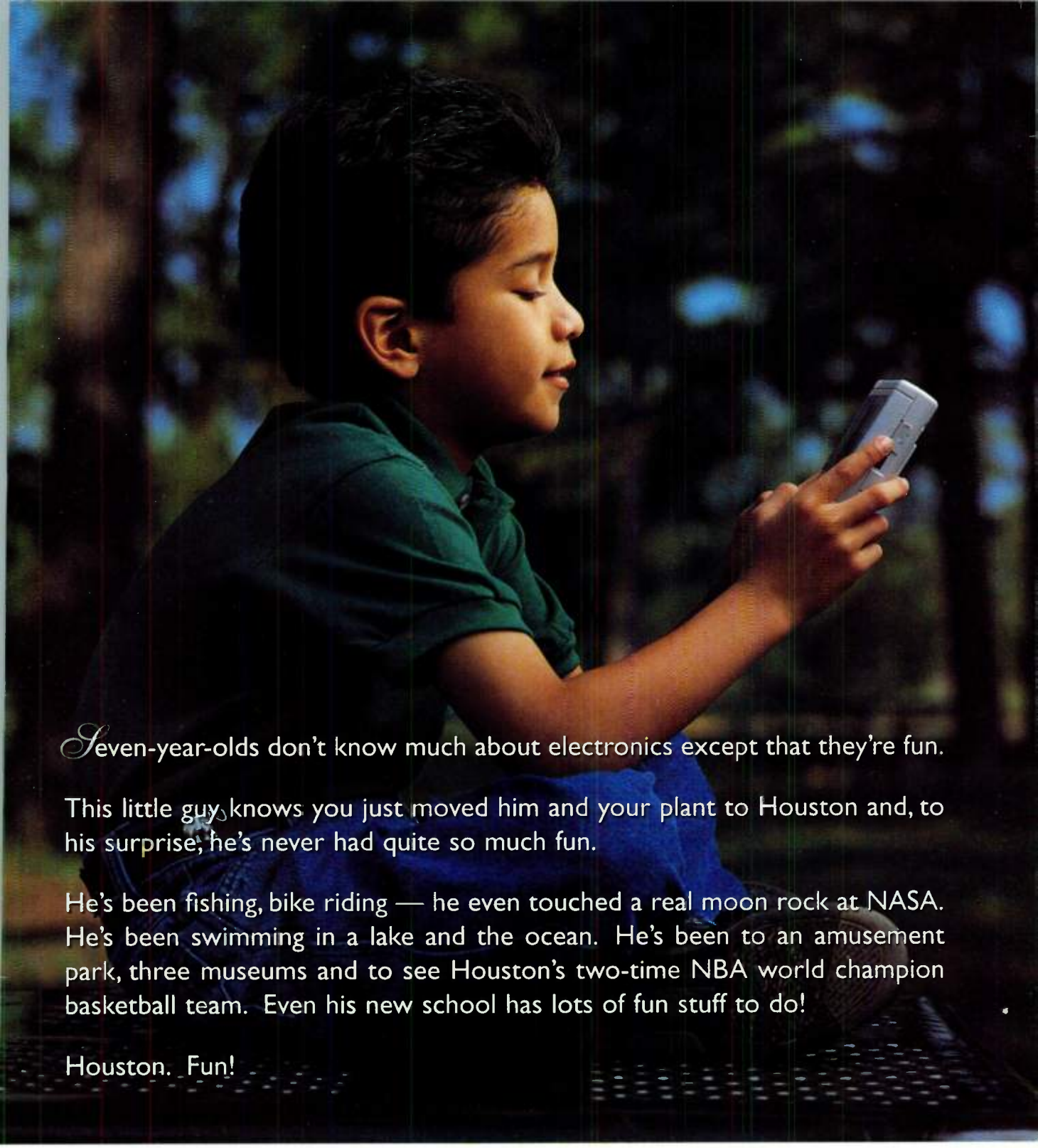
The unit's moving map feature was somewhat difficult to use, requiring familiarity to read and interpret. For the purposes of the test flight, I decided to rely on the more conventional paper charts for basic navigation information.

While no product is flawless, Magellan seems to have come close. Other than the slightly challenging moving map display, the only other gripe is the operating time (about 4 hours) provided by the receiver's three internal AA batteries. Selecting the display's backlight feature can significantly reduce this time even further. An external rechargeable battery pack might make an excellent accessory for the XL.

Although the XL is Magellan's top-of-the-line handheld, it retails for only $699. It is interesting to note that their lower-priced ($499) LT model, and even their low-end $200 Trail Blazer (for hikers and campers) unit, shares the same top-notch receiver technology found in the XL. For those with more disposable income (about $1799), Magellan offers the EC-10X, a clipboard-sized electronic chart that combines the capabilities of a fully featured GPS system with a 4.5-by-6-in., high-resolution, high-detail electronic map that rivals the resolution of a paper chart.

If you have the urge to get a hold of one of these serious toys, check your local aviation or sporting goods stores, or contact the manufacturer directly at Magellan Systems Corp., 960 Overland Ct., San Dimas, CA 91773; (909) 394-5000; fax (909) 394-7050.

LEE GOLDBERG



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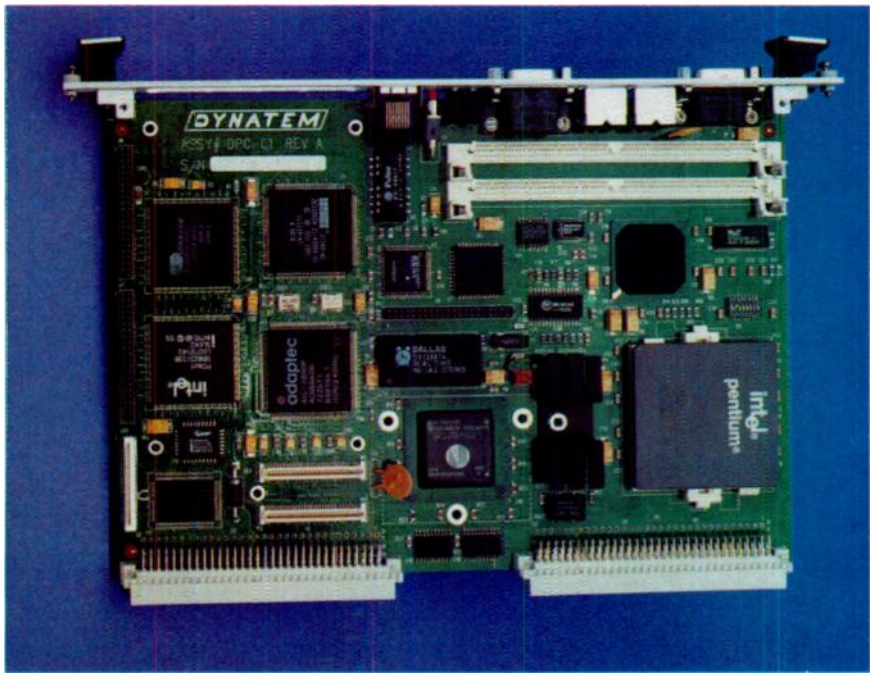

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High-End Boards Continue To Raise Performance Bar

RICHARD NASS

Designers Must Decide Which CPU Architecture Is Most Appropriate For Their Application.

The term "high-end boards" conjures up images of 19-in. rack-mounted systems, VMEbus boards, power supplies, and the like. While the overriding trend in the computer industry is to downsize, those big boards just won't go away. In fact, the VMEbus market continues to grow at a healthy pace. The biggest change in today's boards from a few years ago is the functionality that's crammed onto a board.

Today's leading-edge CPU board is aptly named a single-board computer (SBC). In most cases, most of the general functions needed for the entire computer are contained on one board. In addition to the microprocessor, the board will house memory, networking, serial and parallel ports, SCSI interfaces, and so on. Customization of the board can be done through PCI mezzanine cards (PMCs), which are small daughterboard modules that sit directly on the SBC, and connect electrically through the PCI bus.

So how do high-end board manufacturers individualize their products? One way is by the CPU they choose. The choices are plentiful and continue to grow. Some of the current popular choices include the Motorola 68000 family, the PowerPC (currently manufactured by both Motorola and IBM), the Alpha series, developed by Digital Equipment Corp., and the Sparc—with all its variations—produced by a host of companies.

One such Sparc chip comes from Fujitsu Microelectronics Inc., San Jose, Calif. The company's TurboSparc operates at 170 MHz and is aimed at high-end workstations. The chip is built with a nine-stage pipeline and has 16 kbytes of both instruction and data cache memory. Up to 1 Mbyte of secondary cache is supported. The TurboSparc is compatible with SunOS, Solaris, and all Sparc applications. It offers performance ratings of 143 SPECint92 and 119 SPECfp92.

CHECK THE LIST

When designers look at the available CPU architectures, there's a checklist of points that help simplify the task. First on the list is the performance level that's required from the CPU. The second point is the availability of software tools, operating systems, compilers, and debuggers. And, the third point is the application for which the board is intended. It's important to note that most of the architectures can be forced to comply with each of the points. But, the im-

portant question is, which CPU is *best* suited for each of the points.

In the words of Ray Alderman, executive director of the VME Internation Trade Association (VITA), Phoenix, Ariz., "When you start to push the application, that's when specific architectures or CPU environments start to exert themselves and stand out."

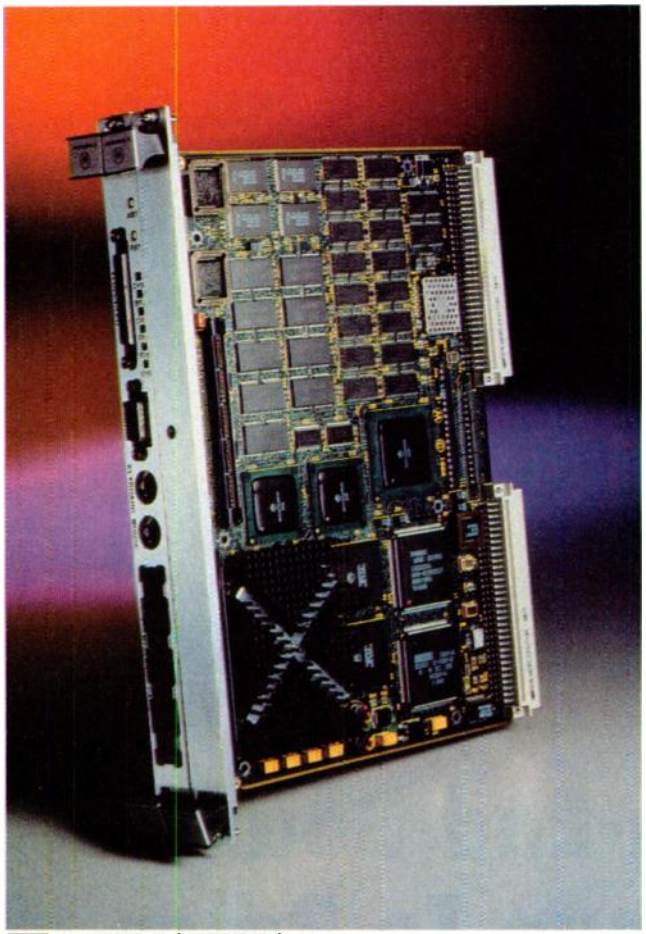
The software issue is probably the most important aspect that's often overlooked. Users must understand which software and development tools are available, including operating systems, compilers, debuggers, and simulators. And, if available, they must all work cohesively.

According to Jerry Gipper, product marketing manager at Motorola Computer Group, Tempe, Ariz., "One of the big selling features for our PowerPC boards is the operating-system support. It runs lots of different operating systems. We find that in some larger companies, where they want to standardize on one microprocessor, the more different operating environments it works under, the easier it is to standardize on the hardware platform."

Motorola's MVME3600 PowerPC VMEbus board is based on the company's PowerPlus VME architecture *(Fig. 1)*. A memory-controller ASIC helps take advantage of the PowerPC's address pipelining, and controls two-way interleaved access to main memory. The result is a processor-to-memory bandwidth in excess of 400 Mbytes/s. The MVME3600 consists of a processor-memory module and base module, both fitting a 6U VME form factor. A PMC slot lets users tailor the board for specific applications. A PCI expansion interface permits an optional I/O carrier for two additional PMC modules or four Industry Pack mezzanine modules.

Designers who decide on a Pentium-based board typically aren't involved with real-time applications because the CPU wasn't built for that type of environment. The software tools for the Pentium tend to quite prolific, though, such as the operating systems and development tools. The performance of the processor itself is adequate for general-purpose applications, but in many demanding applications, such as those that are event or interrupt driven or real time, it can't stand up. Going through the checklist, if the application isn't real time, the Pentium is a good choice. However, if the application is more demanding, then designers should think of looking elsewhere for a CPU, such as a PowerPC. The PowerPC is a good event-driven processor—better than the Pentium, so it fits the first criteria.

The next point is the software tools. They're available, but not as plentiful as the Intel-based tools. If the PowerPC's processing capabilities suit the application, the designer might ask whether the available tools are adequate. If so, it's on to point three—is the architecture suited for the particular application. If the answer is "yes," the design process works. If it's "no," other architectures, such as Sparc, may work better.



1. THE POWERPC microprocessor is the brain behind Motorola's MVME3600 VMEbus board. The board is based on the company's PowerPlus VME architecture.

Another advantage of the PowerPC family is that it is multi-sourced, meaning that it is manufactured by two sources, IBM and Motorola. While chips from the two suppliers have identical cores, the packaging and process methods are different, so there are subtle differences between the two.

Another factor in CPU selection is price-performance, or raw processing power for the price. According to Harry White, President of VI Computer Inc., Encinitas, Calif., "The PowerPC wins hands down against Sparc-, MIPS-, or Alpha-based machines in terms of price-performance. Alpha is probably a little closer than the others."

VI Computer offers a 166-MHz PowerPC 604-based SBC that operates according to the VME64 specification. The 6U board supports the 100Base-TX Fast Ethernet standard for high-speed communications *(Fig. 2)*. Requiring just one slot in the VMEbus backplane, the board is suited for embedded and real-time applications. It supports up to 288 Mbytes of DRAM and 8 Mbytes of flash memory. Connections to the PCI bus are made through the Motorola MPC106 PowerPC-to-PCI bridge chip. The Power 4B supports VxWorks, Windows NT, and Solaris operating systems.

The Sparc processor offers a high level of performance. There are many Unix-based software tools available—not as many as those supporting the Intel architecture, but a good number. RISC-based processors, like the Sparc, tend to be very capable number crunchers, but light on the event-driven real-time requirements. As a result, the Sparc-based boards typically show up in embedded applications running some kind of Unix op-

handheld-constrictaphobia an abnormal fear of designing hand-held terminals and not having a processor that allows a flexible and customized solution for specific applications.

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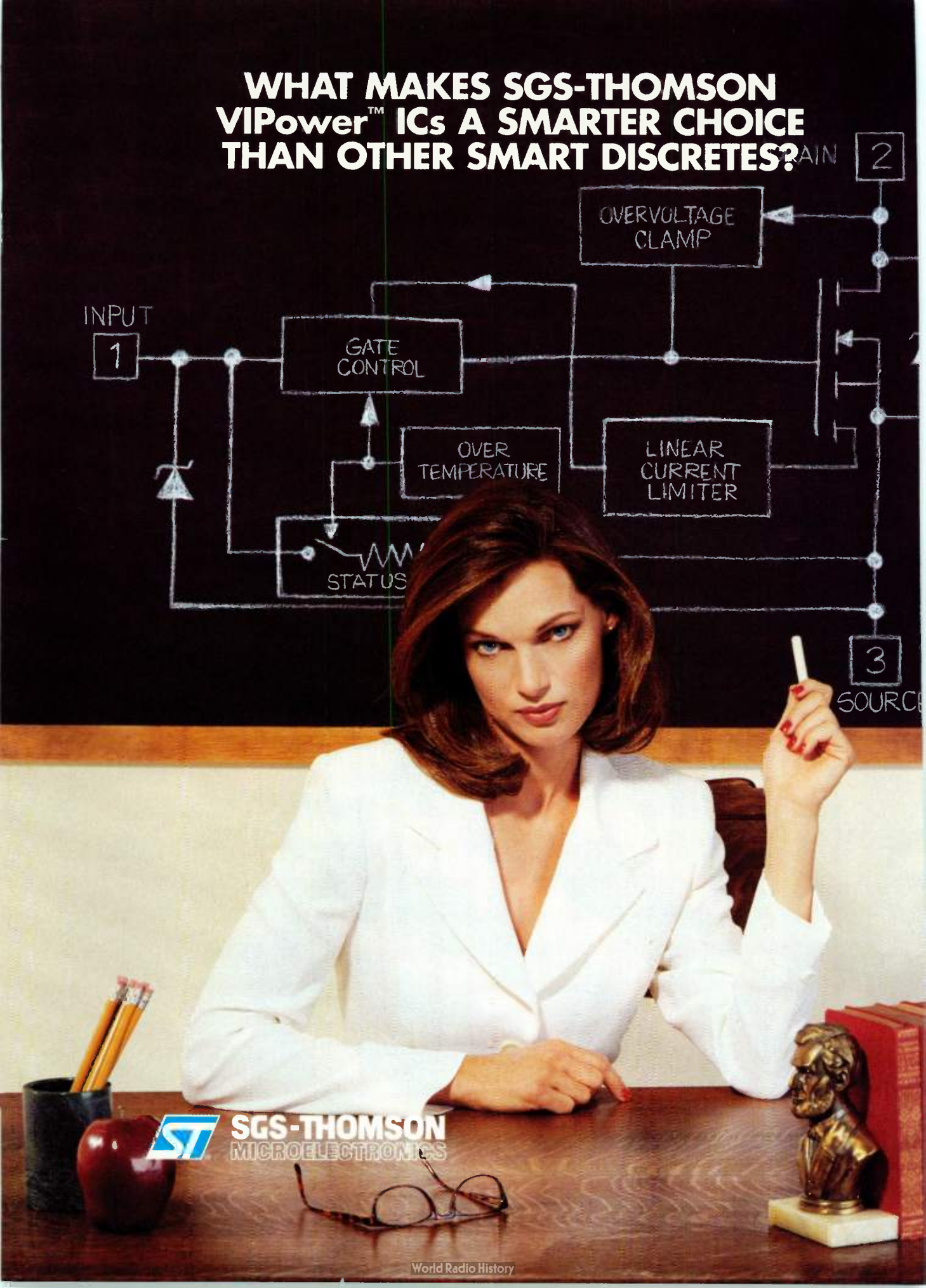

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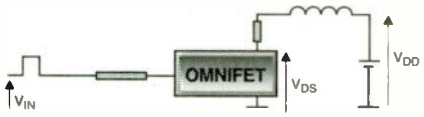


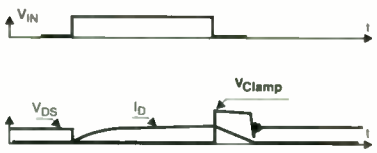
OVERVOLTAGE CLAMP

FEATURES

>Unrivaled energy handling
>Clamp internally set from 42V to 70V

BENEFITS

>No damage due to overvoltage spikes



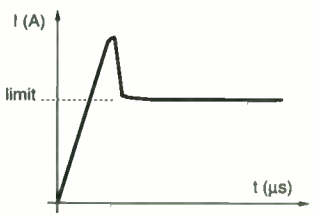
LINEAR CURRENT LIMITER

FEATURES

>Linear current limitation
>Fast step response

BENEFITS

>Load protection
>Adjustable current limit by changing the metal mask



GATE CONTROL

FEATURES

>Analog driving due to direct access to the gate of the Power MOSFET
>Logic-Level operation from a TTL/CMOS driver circuit

BENEFITS

>Pin to pin compatibility with standard MOSFET

OVER TEMPERATURE

FEATURES

>Short circuit protection
>Overtemperature protection
>Automatically restarts at 135°C

BENEFITS

>High safety in all environmental conditions

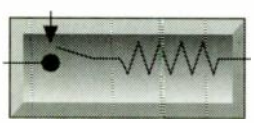
STATUS

FEATURES

>Overtemperature feed back through input pin

BENEFITS

>Real time monitoring



OMNIFETs - AUTOPROTECTED POWER MOSFETs

Type	V_{Clamp} (V)	$R_{DS(on)}$ (mΩ)	Package
VNW100N04	42	12	TO-247
VNW50N04	42	12	TO-247
VNP49N04	42	20	TO-220
VNP49N04FI	42	20	ISOWATT220
VNV49N04	42	20	PowerSO-10
VNB49N04	42	20	D2PAK
VNP35N07	70	28	TO-220
VNP35N07FI	70	28	ISOWATT220
VNV35N07	70	28	PowerSO-10
VNB35N07	70	28	D2PAK
VNP28N04	42	35	TO-220
VNP28N04FI	42	35	ISOWATT220
VNV28N04	42	35	PowerSO-10
VNB28N04	42	35	D2PAK
VNP20N07	70	50	TO-220
VNP20N07FI	70	50	ISOWATT220
VNV20N07	70	50	PowerSO-10
VNB20N07	70	50	D2PAK
VNP14N04	42	70	TO-220
VNP14N04FI	42	70	ISOWATT220
VNV14N04	42	70	PowerSO-10
VNB14N04	42	70	D2PAK
VNK14N04FM	42	70	SOT-82FM
VNP10N07	70	100	TO-220
VNP10N07FI	70	100	ISOWATT220
VNV10N07	70	100	PowerSO-10
VNB10N07	70	100	D2PAK
VNK10N07FM	70	100	SOT-82FM
VNP10N06	60	300*	TO-220
VNP10N06FI	60	300*	ISOWATT220
VNK10N06FM	60	300*	SOT-82FM
VND10N06	60	300*	DPAK
VND10N06-1	60	300*	IPAK
VNP7N04	42	140	TO-220
VNP7N04FI	42	140	ISOWATT220
VND7N04	42	140	DPAK
VND7N04-1	42	140	IPAK
VNK7N04FM	42	140	SOT-82FM
VNP5N07	70	200	TO-220
VNP5N07FI	70	200	ISOWATT220
VND5N07	70	200	DPAK
VND5N07-1	70	200	IPAK
VNK5N07FM	70	200	SOT-82FM

*V_{IN}=7V

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erating system.

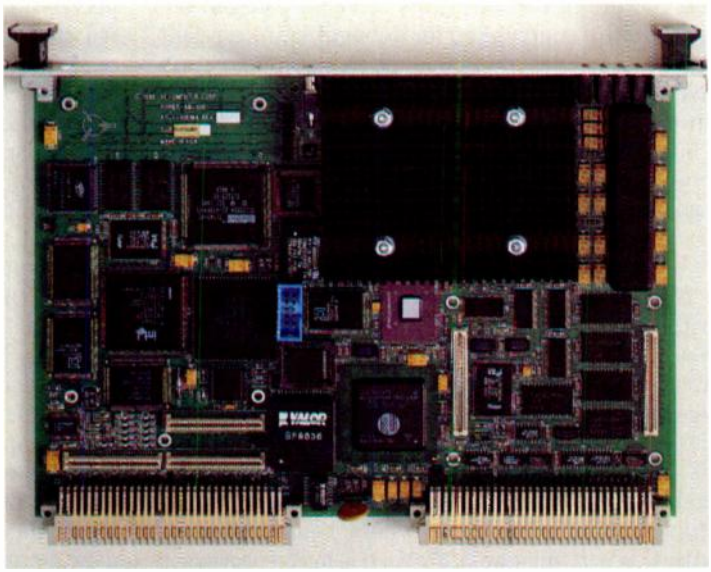
The applications where Sparc will perform the strongest are those that require a lot of data moving—such as file servers—due to the processor's wide bus and 1.3-Gbyte/s peak bandwidth. Audio and video data, which typically require a high bandwidth, are also candidates for the Sparc CPU.

The USP-1 UltraSparc VME64 engine was developed by Themis Computers, Fremont, Calif. The platform holds a 167- or 200-MHz UltraSparc processor and is aimed at such applications as telecommunications, imaging, and embedded processing. It is 100% compatible with Sun's UltraSparc Model 170 workstation. The USP-1 is a two-board set. The first board contains the processor module, while the second is the I/O module, which includes dual Ethernet and fast SCSI 2 ports and a VME64 interface. A third board accommodates two SBus cards.

Aimed at intranet servers, the SparcEngine Ultra AX board is also powered by the family of UltraSparc processors *(Fig. 3)*. The board, designed by Sun Microelectronics, Mountain View, Calif., runs the Solaris operating system, which supports a host of network-computing software, including Java. Built to a PC ATX form factor with a 64-bit, 66-MHz PCI bus, the Ultra AX is cost-reduced by employing some standard PC-based components, such as memory, peripheral cards, and power supplies.

68000: Not Dead Yet

Boards based on the 68000 processor tend to be at the heart of the real-time, end-of-the-application spectrum. There are a prolific number of tools available for the 68000, such as compilers, kernels, and debuggers. In addition, the large installed base of code helps ensure a long life for the 68000-based products. Force Computers Inc., San Jose, Calif., says they still sell a 68000-based board that was developed in 1984. Many users of high-end boards not only want long-term availability of products, they expect and demand it.



2. THE POWER 4B BOARD SUPPORTS the VxWorks, Windows NT, and Solaris operating systems. Designed by VI Computer, the board offers a 166-MHz PowerPC and requires just one slot in the VMEbus backplane.

White says that most of his customers want five to seven years of product availability, while the military wants 10 or 12 years of support (meaning inventory and parts). White states, "In many cases, we'll have to do a redesign to work around obsolete parts. The key is that, at the board level, we are providing a form-fit function-equivalent product."

Digital Equipment Corp., Maynard, Mass., claims that its Alpha microprocessor is a clear-cut winner in the performance category. But, because users often decide on the operating system first, the processors that support those operating systems come as the second contention point. The Alpha runs Windows NT in an emulation mode and DEC's version of Unix in a native mode, however, the DEC Unix is not a dominant player in the market.

As part of DEC's strategy, the Alpha processor also complements the Intel architecture with a high degree of compatibility. This attribute shows up in several ways. The most obvious is an easy exchange of data between the two platforms when running under the Windows NT operating system.

The latest Alpha RISC processor, the 21164, runs at speeds up to 500 MHz, performing 15.4 SPECint95 and 21.1 SPECfp95. With a peak execution rate of 2 BIPS, the chip is suited for applications such as video conferencing, 3D modeling, multimedia authoring, image rendering, and animation. At the highest speed, the processor disipates 30 W.

One of the black marks against the Alpha processor traditionally has been the power it consumes and heat that's dissipated. Russ Doty, a graphics product manager at DEC, says, "There are not real big concerns about the power and heat. Most of the high-end chips soak up a lot of power. So the power-dissipation and cooling requirements are quite similar to the Pentium and other processors. Basically, what we have learned through experience is that you put a big heat sink on it, point a fan at it, and don't worry about it."

In many applications, power consumption *is* an important factor. For example, an embedded system such as a copier should have a power-down mode. However, designers of such systems are not usually concerned about the active-mode power consumption.

The PowerPC 604 and 620 processors only have a full-on mode. As a result, they can't be put into a power-savings mode (the 603 family, which is aimed at portable systems, has a power-down mode). There aren't too many methods of power reduction if the CPU doesn't have a low-power mode.

Some of the peripherals can be shut down, but they don't draw too much power anyway. SCSI controller chips only consume power when in use, so they don't take a lot of power. Memory hardly draws any power at all. An Ethernet controller isn't usually put into a sleep mode, because if there's traffic on the bus, by the time the chip wakes up, it will have missed the data that was coming.

The processor is the biggest power draw, in many cases consuming up to 50% of the board's total power. On the positive side, a board designed with a PowerPC 604 or Alpha chip doesn't need much other logic on the board. In these cases, the CPU could be drawing up to 70% of the board's power.

Board Expansion

Early on, expansion on a high-end board was typically done with some kind of proprietary mezzanine connector (although, many vendors usually maintained that their mezzanine was an "open" standard). Many of the expansion buses on today's boards employ some facet of PCI as the local bus, regardless of the CPU architecture.

A typical board is built with three main buses. The buses are the processor-memory bus, the interface to the cache memory, and the DRAM. The processor-memory bus is often a proprietary type, depending on the processor architecture. The second bus is often a bridge from the processor to the PCI bus, which connects to the on-board peripherals, such as Ethernet, SCSI, and graphics. The final bus is used to connect expansion modules. A traditional motherboard might use standard PCI expansion slots, or a PMC connection.

Bridging to the PCI bus is made easier thanks to the QSpan, a chip that connects Motorola-based processors (both 68000 and PowerPC families) to the PCI bus. Developed by Tundra Semiconductor Corp., Kanata, Ontario, Cananda, the part serves as the interface between the processor and the PCI bus *(Fig. 4)*.

In some cases, the board contains a connector that allows the user to directly access the processor-memory subsystem for the highest performance. The connector is often a cache expansion slot. This technique is similar to Intel's proposed Advanced Graphics Port (AGP) specification, where they've defined a direct connection to the processor bus. Designers tend to employ this technique by default as a way to debug the board. With today's dense packaging technologies, such as ball-grid arrays, the chips can't be plugged and unplugged for debugging. As a result, designers include this secondary connector for debugging. Although it's a fairly common design concept, there's no standardization as to the type or location of that connector, leaving the user at the mercy of the board designer.

The growing use of the PCI bus lets the traditional high-end board manufacturers leverage PC technology. Many of the desktop PC ICs are being utilized on the high-end boards. Because these chips are produced in such high volumes for PCs, high-end board makers can take advantage of the low margins placed on the chips.

One place where board designers must be concerned is in the processor-to-PCI chip set. Intel designed their chip sets for their own processors, such as the Pentium and Pentium Pro. Motorola and IBM didn't do a lot of chip-set development for the PowerPC series. As a result, board manufacturers are left to design their own chip set. But, there's an upside to that—board manufacturers can customize the chips for particular applications.

A slightly different CPU-architecture approach is taken by Ariel Corp., Cranbury, N.J., which employs digital-signal processors on the VMEbus. The company's HyperHydra V100 contains up to eight TI TMS320C44 DSPs for 480 MFLOPS of peak performance *(Fig. 5)*. Featuring a 64-bit master-slave VME64 system-bus interface, the board employs a system-wide Harvard architecture. The HyperHydra also contains twelve external 20-Mbyte/s communication ports, dual mezzanine connectors, and a JTAG port for multiprocessor debugging. The board wrings out optimal performance by taking advantage of the DSPs' dual memory-bus architecture. Each processor is equipped with two banks of private SRAM (up to 2 Mbytes per bank). One bank is dedicated to the global-memory bus, while the other connects to the local-memory bus. The shared memory banks can be accessed through the VMEbus.

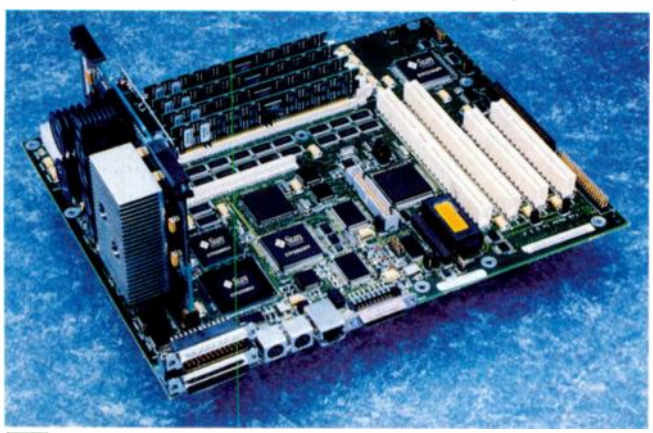
Sun Microelectronics was one of the early adopters of 64-bit, 66-MHz PCI. The high-speed bus is shipping on current products. As stated by Robert Feretich, director of platforms engineering at Sun, "As part of the data-moving concept, if you are going to be moving data in and out of the CPU, you have to get it to the peripherals fast, also," hence the need for the fastest available PCI. Sun also incorporates a high-performance graphics port into their boards, which is similar to the AGP, but is at twice the number of bits and at higher frequencies (64 bits at 83 MHz).

Serial Buses

One specification that was designed for PCs, but may quickly migrate to high-end boards is the Universal Serial Bus (USB). According to Gipper, it'll appear on Motorola boards by early next year. On VMEbus boards, USB will connect to mice, keyboards, drives, and the like. USB makes sense for VME boards because the VMEbus is somewhat pin-limited. Theoretically, by adding a USB port to the board's front panel, serial and parallel ports can be eliminated.

The current problem is that the USB chips aren't very integrated, yet. Board designers don't want to give up the real estate required by a USB interface chip. The logic needs to be integrated into another chip. Motorola plans to design their own USB chip.

USB discussions often lead to talk about what many call USB's "big brother," the IEEE 1394 standard, also known as Firewire. Also a se-



3. WHEN SUN MICROSYSTEMS' designers build a board, networking applications are usually at the forefront. That's exactly the case with the SparcEngine Ultra AX, which is powered by the family of UltraSparc processors.

Biomedical Research Application Note

Application: Develop a simple test for use in muscle-response research.

Solution: TestPoint's drag-and-drop environment makes it possible to collect and analyze data on the first day of use. Included are integrated functions for moving averages, min/max, and zoom to examine critical information. A single Keithley MetraByte DAS-1800AO provides stimulus and simultaneously measures muscle EMG and force signals.

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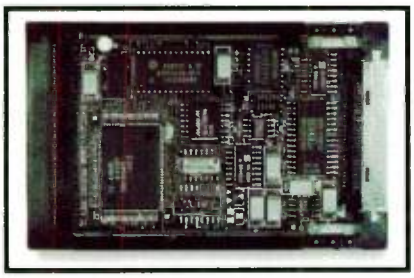
Temperature Profiling Application Note



Application: Measure temperatures on surface mount boards passing through a 4-zone convection reflow oven.

Solution: Keithley MetraByte's AD612 measures temperatures for just $300, including display software, signal conditioning and screw terminal connections. Standard software provides thermocouple conversion, Windows display panel and stores data to disk without requiring any programming. Results analyzed using Microsoft Excel. Six inputs on one module allow temperature profiling of the board in one pass.

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Production Test Application Note

Application: Develop a high-throughput, flexible functional test system for programmable thermostat boards.

Solution: A fast, yet easy-to-use and maintain system. TestPoint software controls a two-bay system optimized for high throughput, where one board is tested while the next one is loaded. Maintenance is simplified because all the I/O is done through a single Keithley MetraByte DAS-1602 data acquisition board with an interface chassis and bed-of-nails fixture.

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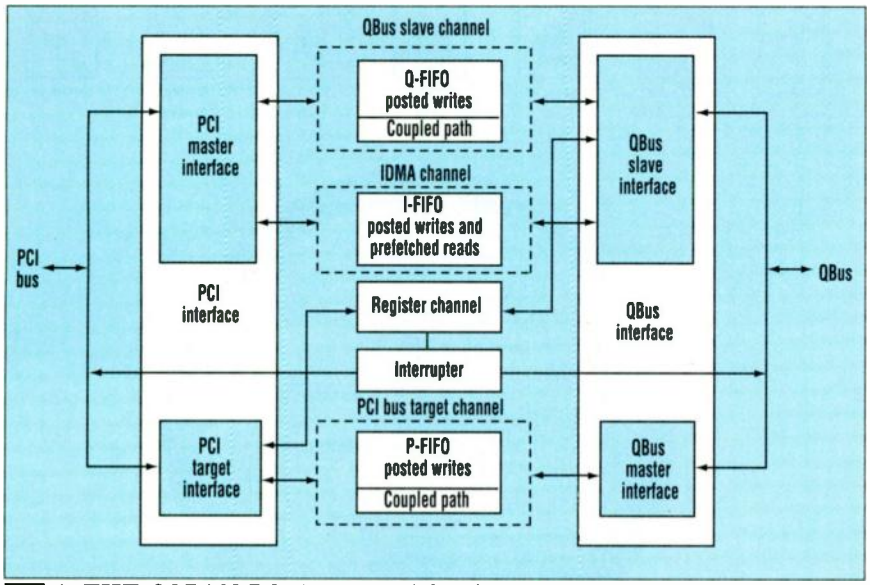

4. THE QSPAN PCI INTERFACE CHIP supplies a glueless solution for both the Motorola 68000 and PowerPC processor families. The part resides between the PCI bus and the processor.

rial bus, Firewire is currently specified to 400 Mbits/s, with a migration path to 1 Gbits/s (USB runs at about 12 Mbits/s). VMEbus' specification authors hedged their Firewire bets about two years ago when writing the VME64 specification. Originally, the VMEbus had a pair of serial lines, designated B21 and B22 on the P1 connector, marked as Serial Clock and Serial Data. The definition of those lines was changed to Serial A and Serial B, making them generic signals. Also, the pair had been terminated with a Thevenin terminator, just like other VMEbus lines. By removing the terminators, designers were free to use any type of serial channel. On these signals, board makers can implement a serial channel such as Firewire.

A second set of serial pins were added later, called Serial Prime A and Serial Prime B. With these four serial lines, designers can implement both USB and Firewire. According to Alderman, the first implementations of USB and Firewire on VME will be in the next six months, "It'll come from a Pentium-on-VME board first, then a PowerPC board."

The Sparc architecture has found a home in many technical and industrial applications. One of its biggest advantages is its ability to run the Solaris operating system, which since its inception, has been aimed at networking and telecommunications applications. Solaris applications are developed directly on the workstations on which they will run, giving designers a transparent path to their target environment. Solaris also claims to have more applications than any other flavor of Unix. While the high-end applications had been the property of the Solaris camp for many years, Windows NT is trying to gather a portion of that market. The Intel-based machines are typically optimized for Windows NT.

While Solaris runs on other architectures, the fewest portability issues come when running on native Sparc platforms. Solaris is a robust operating system for symetric-multiprocessing (SMP) applications.

"Solaris 2.5 has the most efficient thread in an SMP environment," claims Bill Kehret, president of Themis Computers. "That's basically what everyone else is trying to catch up to. Solaris also has real-time attributes, such as deterministic scheduling and preemptible interrupts," says Kehret. Solaris also supports the minimum Posix requirements necessary for the military and federal-systems markets.

While some would argue the point, Steven Dow, vice-president and general manager of Force Computers Inc., San Jose, Calif., feels that the Intel architecture is keeping up with the others in terms of raw performance, "They've either been in the lead or at least competitive. And with Pentium Pro, they can now do multiprocessing. The only one with a leg up for multiprocessing is Sparc. There are no convenient ways to do multiprocessing with PowerPC unless you develop some expensive custom gate arrays."

One of the biggest reasons for employing the Intel architecture is its ease of integration. All of the Intel processors use PCI as their local bus. The availability of both hardware and software lets designers bring their products to market more quickly. Users can also develop their application software faster. As with the Sparc-based platforms, developers can develop and deploy on the same platform, eliminating cross development.

Built with an Intel Pentium running at speeds up to 200 MHz, the DPC1 is a 6U VMEbus board that requires just one slot. The board, developed by Dynatem Inc., Mission Viejo, Calif., offers a flat-panel interface, 100Base-TX Fast Ethernet, and fast and wide SCSI 2. Further expansion is handled with a PMC connector. A Tundra Universe chip attaches the local PCI bus to the VMEbus and is capable of VME64 data transfers at rates up to 60 Mbytes/s. Decoupled transfers let the PCI bus move data at the rated PCI speed without any hindrance from the VMEbus. Drivers are available for Windows NT, Windows 95, VxWorks, and LynxOS.

The Intel architecture isn't very popular on VME because it requires an "Intel-to-VME" adapter, as well as all the necessary drivers. But it does make a good fit for the Compact PCI platform.

THE NEW KID

Many of the traditional VMEbus houses see Compact PCI as a good business opportunity. But it is important for these companies to position it correctly—as a complement to VME, rather than an alternative. Otherwise, they could be cannibalizing their own business. Force Computers recently developed a system that can house both VMEbus and Compact PCI boards in the same enclosure (ELECTRONIC DESIGN, *Sept. 3, p. 185).*

One of the application areas that's

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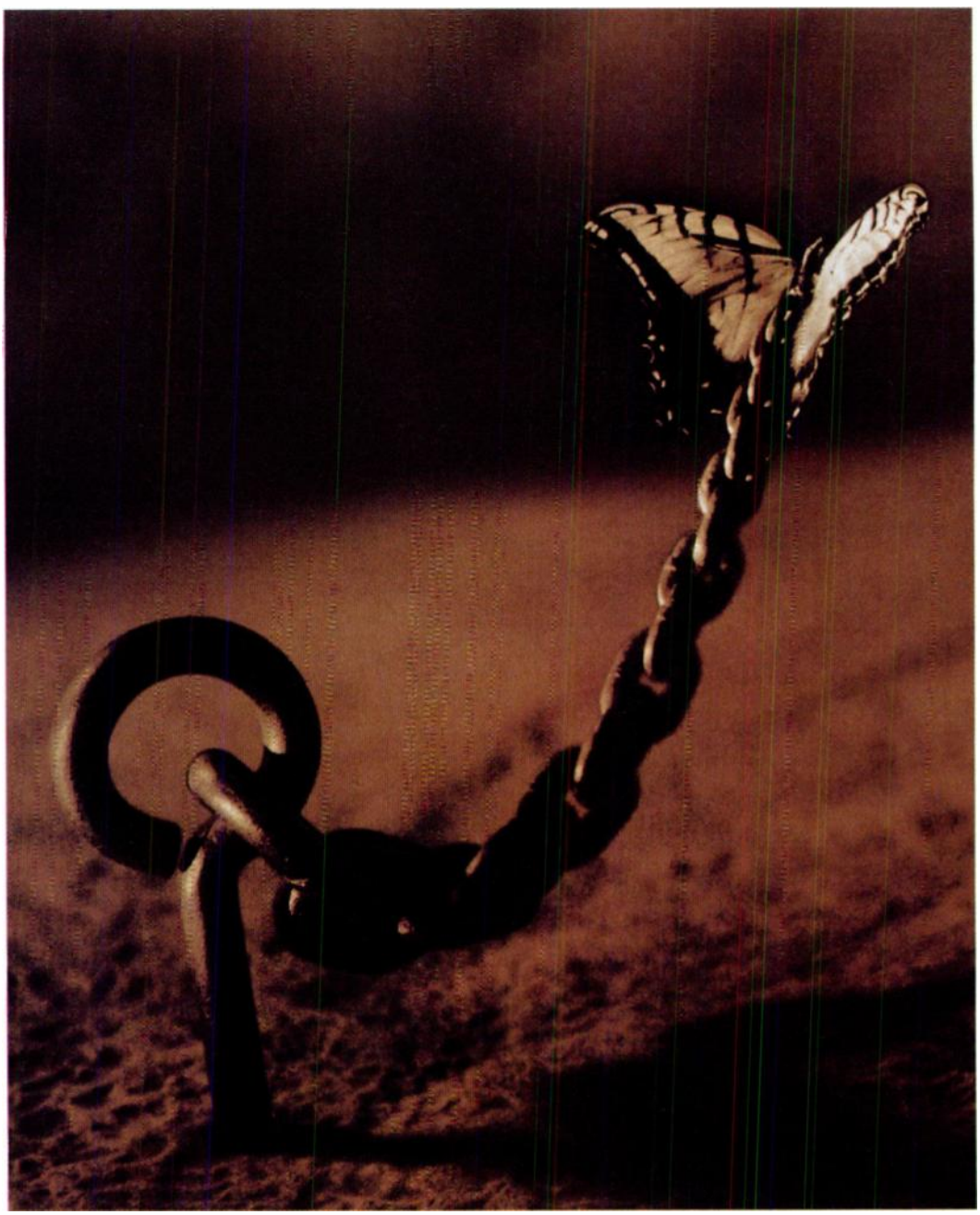

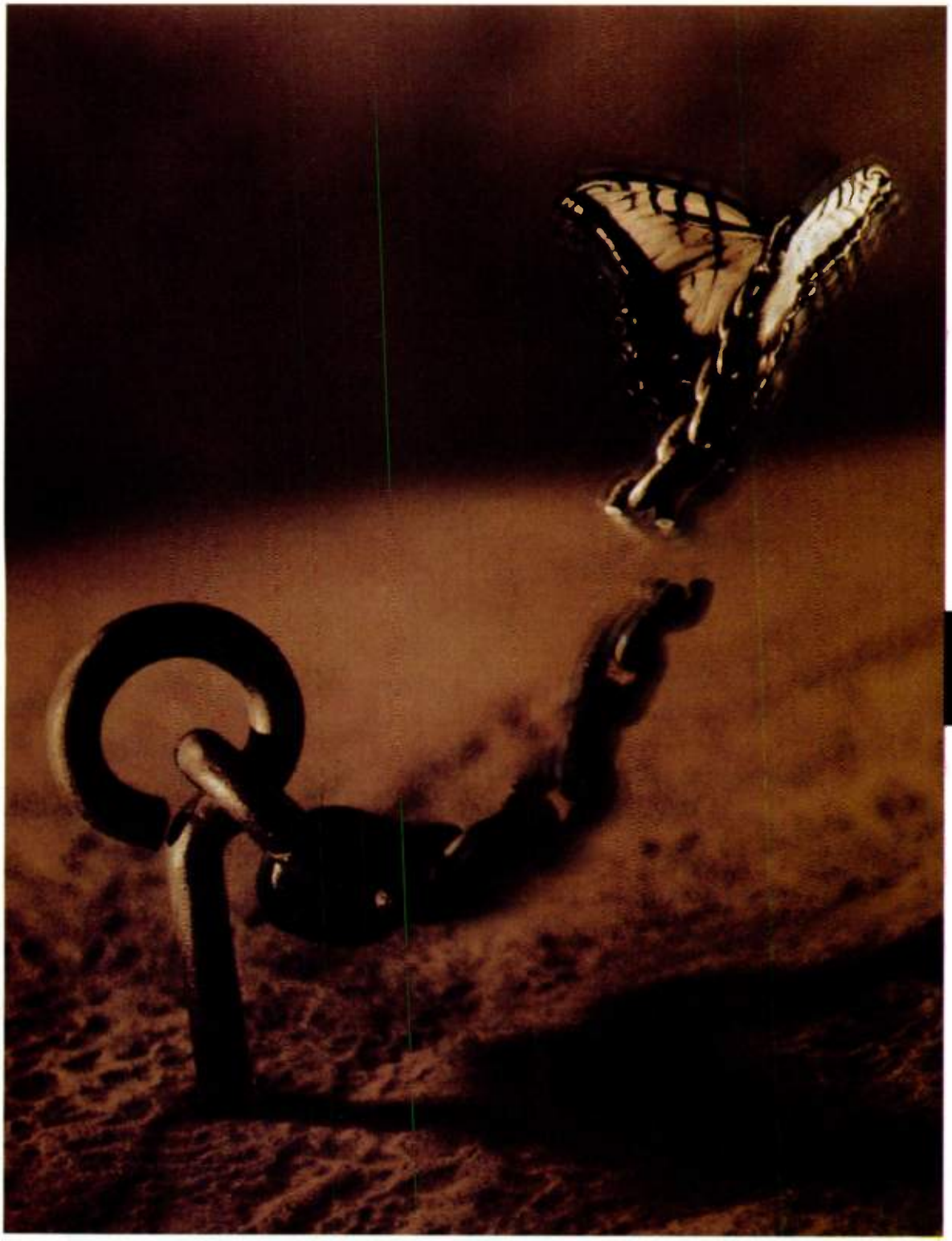

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currently getting a lot of interest for VME is telecommunications. Yet, these same customers are asking about Compact PCI, seeing it as a way to reduce their costs. One of the biggest trade-offs for Compact PCI is that it currently doesn't offer as many expansion slots as VME, which can be an issue, depending on the specific application.

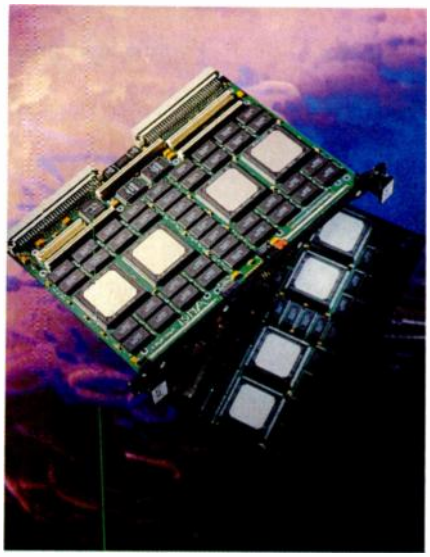
Pro-Log Corp., Monterey, Calif., recently developed a Compact PCI system that keeps the telecommunications market in mind. For example, it offers rear-panel I/O. All I/O connections plug into a "back board," a rear board mounted behind the front-mounted processor. The back board plugs into the rear of the backplane, into a double-headed connector that protrudes through the backplane. Users also like the front-mounted processor which can be easily swapped out without disturbing the I/O connections.

Pro-Log's CDP6000 Dual Pentium Processor board plugs into the company's 9615 19-in. chassis. The board holds up to 512 Mbytes of DRAM, and has an on-board EIDE interface. The dual bus interfaces support the chassis' 15 expansion slots (the CPU board plus 14 6U expansion cards).

While Motorola won't be jumping into the Compact PCI market right away, they are hedging their bets, says Gipper, "A few months ago, when we introduced some new PowerPC products, we did some ASICs to support the PCI bus and the memory controller. If you look at that architecture, it's very easy to convert that to Compact PCI. So, it won't take a huge effort to do a Compact PCI card. All we have to do is re-lay out the board with the new connectors."

The biggest push for Compact PCI, so far, has been in the traditional industrial applications, such as programmable level controllers (PLCs), assembly and production equipment, and factory-floor systems.

"When people ask 'why Compact PCI?' It is really pretty simple," states Joe Pavlot, vice president of product development at Pro-Log, and also president of the PCI Industrial Computers Manufacturers Group (PICMG). "People want the performance that they've come to know and love on the desktop. They want to use Windows NT, plug-and-play, and off-the-shelf software. But, they need better packaging they can get on the desktop."



5. UP TO EIGHT digital signal processors drive Ariel's HyperHydra V100 VMEbus board. It features a 64-bit master-slave VME64 system-bus interface, twelve external 20-Mbyte/s communications ports, dual mezzanine connectors, and a JTAG port for multiprocessor debugging.

Most of the initial Compact PCI boards were developed with Intel CPUs for the simple reason that most of the companies have been traditionally Intel houses. Although, it may not be any easier to design with an Intel CPU. For the most part, it's all based around PCI, which is obviously the underlying technology. PCI is used to connect the processor to the bus, video, hard-disk-drive controller, and so on.

One Compact PCI board that doesn't employ an Intel CPU comes from Creative Electronic Systems, Geneva, Switzerland. The company's RIO3 is a real-time board built with a PowerPC 603 or 604. In addition to all the standard I/O, the board accepts PMC modules for customization. The board supports most popular real-time operating systems, including VxWorks and pSOS.

HOT-SWAP

A subject within the PICMG that's getting a lot of attention from a specification standpoint is hot swapping. It's also the most complicated of all the issues currently under discussion. There are both electrical and software issues that need to be ironed out. The electrical issues revolve around PCI's reflected-wave technology that requires that the impedances of all traces, connectors, and interface chips be constant. Maintaining this state has proven to be a significant issue.

On the software side, the operating system must be able to recognize that a card has been unplugged and replaced by a new card. The system must be re-initialized, and currently, there is no provision to do that.

Says Pavlot, "It is software issues that are potentially more difficult to solve that make a truly flexible hot-swap scheme. Microsoft is writing some drivers. But, it'll be at least a year before all these issues work themselves out."

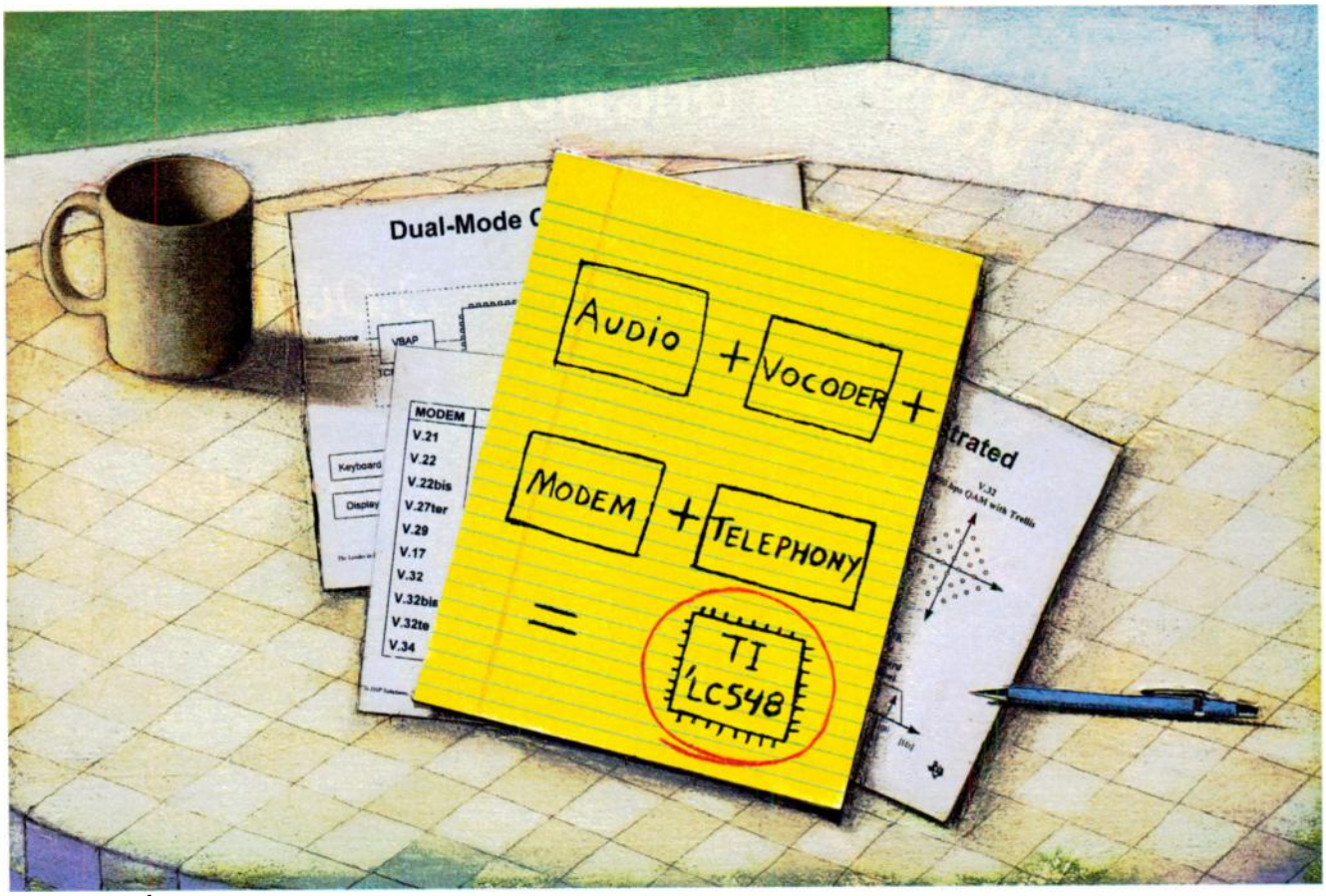
One of the items on the drawing board for VITA is the high-availability issue, a condition where users can plug and unplug boards without powering down the system. This technology is also known as hot-swap. The most difficult facet of hot-swap is dealing with a CPU board that's running the operating system. There are current strategies in place to deal with I/O boards. The ability to remove the active CPU is necessary if manufacturers want to sell fully fault-tolerant products, but most board makers will stay away from that market.

High availability is basically one early level of fault tolerance. The more fault-tolerant a system is, the more feedback mechanisms (redundancies and check points) are required.

In the works, now, are extensions to the existing VMEbus specification. The extensions contain high-speed protocols for block transfers. Because much of the foundation for high availability is contained in the extensions, the high-availability issue is tentatively on the back burner. □

Richard Nass' e-mail address is: richnass@class.org.

HOW VALUABLE?	CIRCLE
HIGHLY	525
MODERATELY	526
SLIGHTLY	527



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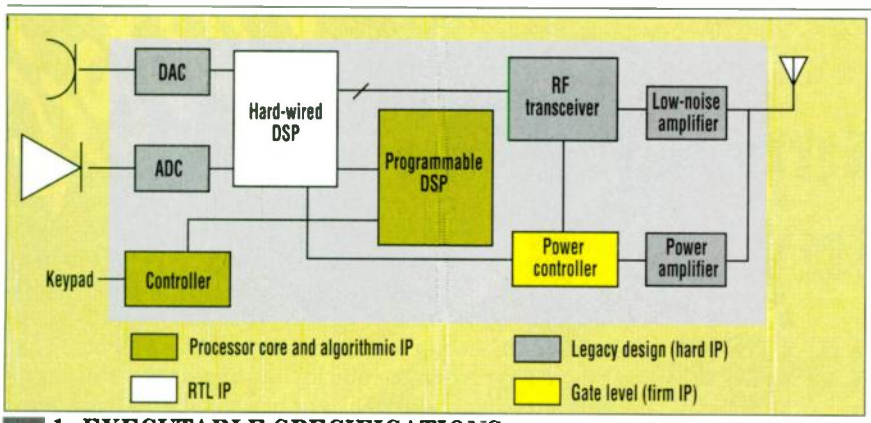
ity. Unfortunately, these goals often conflict. Additionally,



1. EXECUTABLE SPECIFICATIONS of IP building blocks are integrated within a mixed-level verification environment to model a complete system. The system design is then completed by refining each IP block until sufficient detail has been added to realize a hardware or software implementation for that particular block.

the lack of open standards in this area has been deemed by many industry analysts to be the major barrier to putting a greater number of systems into silicon. The more flexible an IP component, the more vulnerable it is to wrongful copying or modification.

The most widely accepted approach to this problem is for IP vendors and system designers to work with different-level representations of IP at different stages in the design. One representation, which contains all the modifiable design elements, is at a higher level of abstraction and omits the design information the IP vendor wants to protect. Another representation, which is synthesized from the first, is protected and non-modifiable. This representation contains the IP vendor's protected design information, modified according to the parameter values specified by the system designer using the first representation.

For example, an IP vendor with an RTL architecture of a linear-adaptive equalizer might provide a user with a parametrizable algorithmic-level model for which parameters such as word length, latency, and throughput can be specified. The IP vendor then uses the algorithmic model as input to a module generator that generates the lower-level, non-modifiable model that the designer implements in his system. In general, IP vendors can circumvent reverse engineering by providing their customers with models of IP blocks that are at least one level of abstraction higher than the level containing the design information that the IP vendor is trying to protect.To address the IP packaging/interface problem, the electronic-design-automation (EDA) industry has started two major initiatives directed at solving the IP-packaging problem: the Virtual Socket Interface (VSI) Alliance and the Open Model Forum (OMF). Cadence Design Systems has been instrumental in driving both of these initiatives as part of its Worldwide IP Network (WIN) development program.The VSI Alliance, established in September of this year, has proposed open technical standards that enable integration of IP from multiple sources, similar to the way in which components are integrated on pc boards today. The alliance, with nearly 40 members, includes most major EDA companies and IP vendors in the world. A baseline standard has been proposed that specifies the requirements for "virtual sockets" as a means for integrating "virtual components" such as system-level macros, cores, and megacells.The proposal also includes guidelines for delivering design data, enabling IP vendors to produce and maintain a standard set of deliverable documentation along with their IP.

TABLE 1: VSI SYSTEM-LEVEL IP MODEL DELIVERABLES

VSI System-level Deliverables	Formats	Purpose
•User Guide Information (performance specification, version history, known bugs, application notes, component description, block diagram, register description, timing diagram, clock distribution, bus I/F, I/O configuration, test description)	ASCII	Enable user to evaluate/select IP components, understand functional operation, applicability, and estimate cost of implementation.
•System Evaluation Model (SEM) (algorithmic/behavioral models)	C, C++, HDL, OMF	Enable user to test IP executable specifications within the system environment and do trade-off analysis.
•Verification Test Bench (functional, timing delay verification patterns)	HDL, PLI	Basis for regression-testing when soft IP is being modified by the designer. Simulation environment for verifying manufacturing test vectors generated by user of soft IP. Functional and timing-delay verification for hard IP ported to another vendor.
•Behavioral Model (cycle-accurate)	C, C++, HDL, OMF	Models functionality of non-processor IP components. Useful for co-verifying IP blocks in a design, and for hw/sw co-verification.
•Processor Model (DSP, microprocessor, microcontroller), (instruction-set models, code-size estimators, software development tools, run-time libraries)	C, C++, HDL	Models processor functionality. Required for hw/sw co-verification.
•Bus Functional Model (pin-in/out, ports, interface-timing, bus protocol sequences)	HDL, OMF	Model interfaces between IP blocks in a design.

VSI Alliance Members (alphabetically):
Actel, Advanced RISC Machines, Advanced Logic, Alcatel Mietec, Altera, ASPEC Technology, Cadence Design Systems, Cirrus Logic, Compass Design Automation, CompCore Multimedia, DSP Group, Excellent Design, Fujitsu, Hitachi, Integrated Silicon Systems, iReady, Mentor Graphics, National Semiconductor, NEC, Object Oriented Hardware, Phoenix Technologies (Virtual Chips), PrairieComm, RAPID Association, SAND Microelectronics, Silicon Graphics, Sony, Summit Design, Sun Microsystems, Synopsys, Texas Instruments, 3 Soft, Toshiba, TSMC, Viewlogic Systems, VLSI Libraries, VLSI Technology, Xilinx

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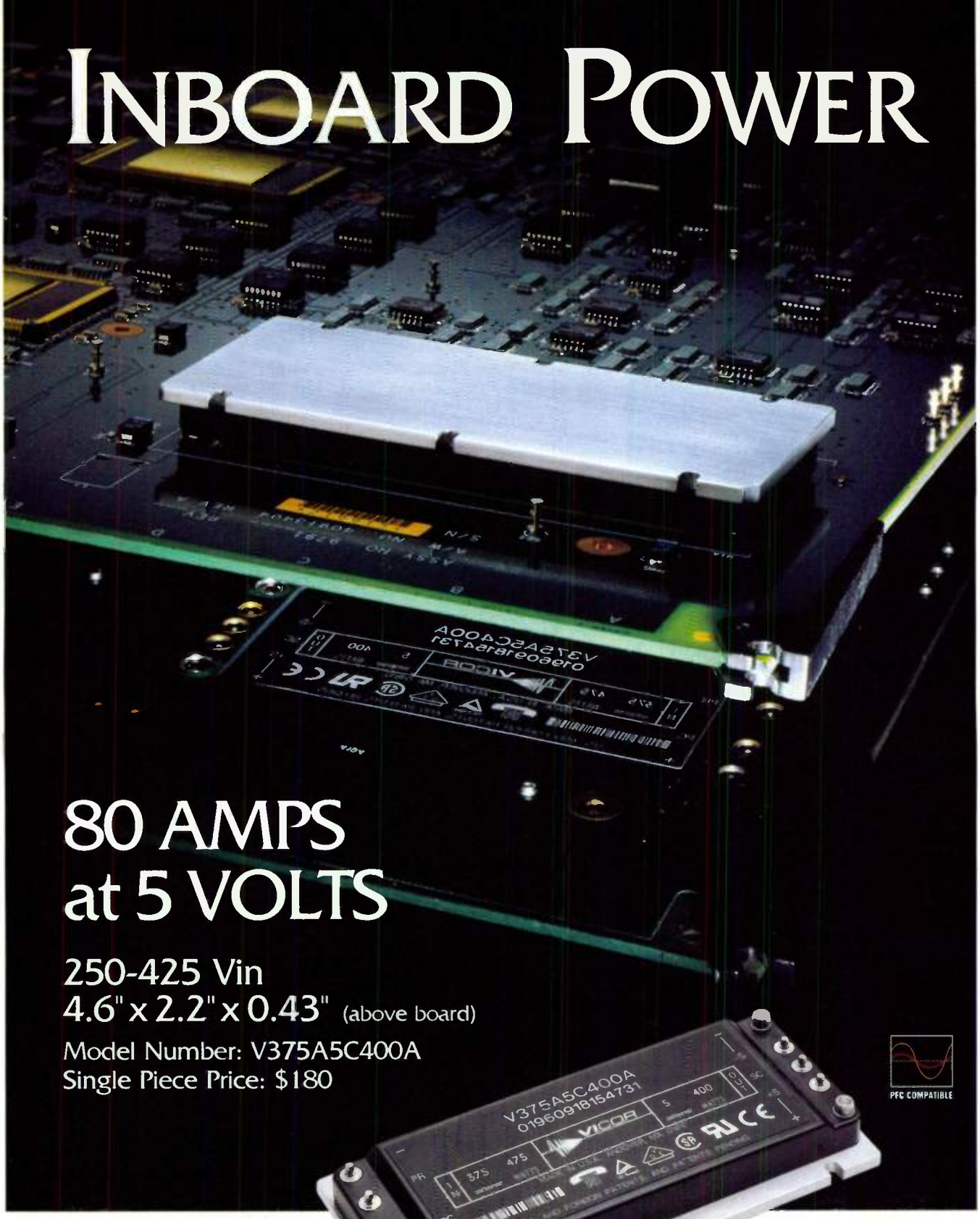

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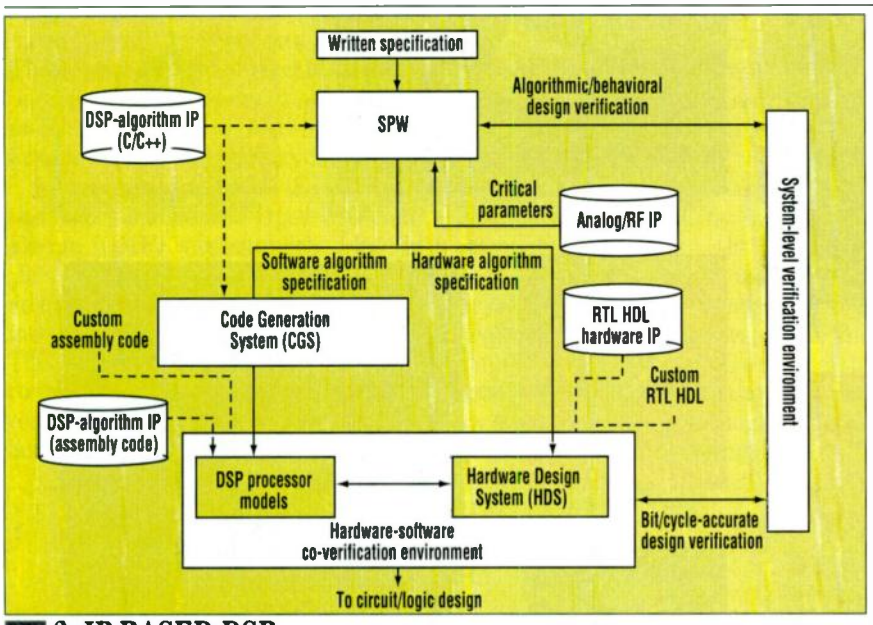

3. IP-BASED DSP system design is supported by Alta Group's Convergence simulation architecture. This figure shows a design flow from specification through hardware-software architecture development. At each stage of the design, IP in various forms can be integrated with the rest of the system.

rate in a design can take weeks. With common data-delivery standards, this might conceivably be reduced to days or even hours.

KNOWN-GOOD IP

System designers require IP building blocks to have been fully tested and verified before they can integrate them into their designs. Bear in mind that there are a number of categories of IP *(Table 2)*. Because this testing and verification process is especially complex and time-consuming with soft, firm, and hard IP, vendors are beginning to create system-level evaluation models (SEMs). SEMs are algorithmic/behavioral versions of IP that designers can use to verify system-level performance and functionality within their designs. A key advantage of using algorithmic/behavioral representations of IP components is that they can be more easily verified within a system-level context. The system can be tested using simulated real inputs such as voice, data, and video images instead of sets of test vectors, resulting in faster and more effective evaluation. For its part, the Alta Group of Cadence has developed verification environments for wireless-communications applications. These environments consist of standards-compliant reference designs for testing and evaluating IP components. Currently supported standards include GSM, IS-95, and IS-136. Currently, IP and EDA vendors are cooperating to provide system designers with increased IP test/verification capabilities, especially in the domain of SEMs for soft, firm, and hard IP. Developing such IP gives vendors early design wins, enabling them in many cases to sell IP without first having to implement and verify the performance in silicon. Because the NRE for a semiconductor manufacturer dealing with a single silicon iteration is typically into the six-figure range, having this capability can result in major cost savings.

GO WITH THE FLOW

Having examined the requirements underlying IP delivery, let's now turn to the subject of an IP-based design flow. Part I of this series showed that IP-based design consists of integrating executable specifications of different components to form complete systems, and how this leads to two fundamental requirements. One is having design components represented at different levels of design abstraction. The other is having a system-development environment that enables the designer to integrate executable specifications of the various system components and test their performance within an operational context.

Once the overall system functionality is verified, a process of continuous design refinement is applied to each component, adding implementation-level detail while continually verifying system-level performance within the operational context. As an example, take the case of a cellular-phone design *(Fig. 1)*. The following paragraphs will examine the IP-based design flow in more detail and show how the IP-component design-refinement process can work *(Fig. 2)*.

INTEGRATING IP

The top portion of Figure 2 shows how IP-based design at the algorithm/behavioral level consists of integrating parametrized C/C++ SEMs of IP components. Defining the system-level functionality and integrating the functional blocks can be done relatively quickly. Because the signals, interfaces, and functionality are described using a high level of abstraction, the number of functional blocks in the system is very manageable, and all the blocks are rapidly simulated. Using algorithmic-level executable specifications, the designer takes real-world inputs (voice and data), processes them through the system, and plays back the output to verify that the system contains all the required functionality. The baseline VSI standard specifies that at the algorithmic/behavioral level, SEMs are defined at a very abstract level. The purpose is to describe block-level functionality to facilitate system-level evaluation of IP. For example, specifying cycle-accurate functionality at this stage is optional, and no hardware-synthesis information (such as standard-cell library information or timing models) is required. However, the standard recommends that an SEM's performance be verified against RTL and lower-level representations of the same model in the IP-vendor's library. So, when algorithmic IP components are combined, they can generate accurate system-level testbenches to be used as initial regression test suites in subsequent stages of the design process. For many system designers, the ability to differentiate their products from those of their competitors is critical. IP-based

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IP-behavioral models are used for all classes of IP (soft, firm, and hard) to verify non-processor (custom logic) IP functionality. These C/C++ or RTL HDL models are used with processor models and BFMs to co-verify functionality with other IP components and to perform hardware/software verification. In addition to the standard information represented in an RTL architecture (such as bit-true interconnects, registers, and clock distribution), the baseline VSI standard requires that behavioral models for firm and hard IP contain additional information such as detailed timing/delay specifications, test patterns, and power consumption. The standard also recommends that secure or encrypted models be provided in OMF-compliant format.

A Logical Conclusion

The bottom portion of Figure 2 shows different routes for completing the circuit/logic level design of the system hardware. For digital hardware, the process for converting architecture-level components into gate-level components (logic synthesis) is automatic for many classes of digital designs. For example, logic-synthesis techniques convert an RTL netlist into a gate-level netlist. Because there are generally only a few efficient ways to map RTL components to a netlist of gates (for example, there are only a few ways to build an efficient n-bit adder), the task of transforming an RTL netlist into a gate-level netlist is straightforward.

For these reasons, today's logic synthesis, datapath synthesis, and memory-compiler technologies are relatively mature. It's a stark contrast to the much greater task of transforming sets of algorithmic-level components into netlists of RTL components, or migrating a design from the algorithmic/behavioral level to the architectural level. This technology is usually referred to as high-level synthesis, and is applicable only to certain classes of designs.Unfortunately, for analog and mixed-signal hardware, the process is even more difficult. This drawback is due largely to the challenge of accurately modeling a transistor's analog behavior. In fact, RF IC design is so difficult that it's very often the key factor in determining time-to-market for wireless products. Unlike digital designs, getting first-time working silicon for analog designs is the exception rather than the rule. Traditionally, RF designers have used Spice-class simulators to model their circuits. These simulators work quite well for analog design at baseband, but become intolerably slow at high frequency.

To address these issues, several EDA companies, including Alta Group and Cadence, are developing algorithmic approaches to analog modeling. For example, Cadence's SpectreRF simulation product models transistor-level analog-RF behavior from 10 to 1000 times faster than Spice-class simulators (depending on the benchmark). Alta Group's SPW RF Library models system-level behavior of RF components even faster, thanks to higher levels of modeling abstraction. As in the case of modeling digital hardware, the fundamental trade-off comes down to level of abstraction versus speed. Once RF designers are satisfied with the performance of their transistor-level design model, they use schematic-capture tools to complete the design and output a netlist for silicon implementation.

The High End

In the preceding paragraphs, we described primarily those capabilities supporting IP-based design that will be available in a year or two. It's worthwhile taking a moment to explore what is actually available off the shelf today *(Fig. 3)*.

The example shows how Alta Group's Convergence simulation architecture is currently applied to an IP-based DSP system design. Starting with a written specification, designers use SPW to integrate algorithmic/behavioral IP components and verify their performance within an overall system. Alta Group's verification environments provide reference designs of different system components as well as environmental models for testing system performance under various conditions.

Designers then use the software- and hardware-component executable specifications generated by SPW's Code Generation System (CGS) and Hardware Design System (HDS), respectively, to produce C/C++ software or RTL hardware executable specifications. SPW, CGS, and HDS are capable of reusing and integrating design IP in various forms. Using one of several DSP models already captured in SPW, the HDS tool, and a verification environment enables bit-accurate and cycle-accurate hardware/software coverification.

After hardware/software coverification, the designer automatically generates RTL Verilog or VHDL for logic synthesis and datapath synthesis. The custom-logic resulting from logic/datapath synthesis is finally integrated with a firm or hard model of the DSP core. This last step is usually handled by semiconductor vendors or by design-specialists from EDA vendors.

The purpose of this two-part series was to explore the motivation and means for applying IP-based design to DSP, and to show how the concept of a Worldwide IP Network is fast becoming a reality *(Fig. 4)*. IP-based design is growing in importance because semiconductor technology enables increasing amounts of functionality on a chip, leading to mounting business pressures for those companies developing systems-on-a-chip. Today, few companies are capable of designing and maintaining all the functional building blocks needed to offer designers a total system-on-a-chip solution. Becoming part of a Worldwide IP Network that effectively supports design reuse will enable companies to focus their unique design expertise and resources in those areas where they can deliver maximum value to the marketplace. □

Steve Svoboda manages development and marketing for Alta Group's Signal Processing WorkSystem (SPW). He holds a BSEE and BA in economics from Johns Hopkins University, Baltimore, Md., as well as graduate degrees in both electrical engineering and engineering management from Stanford University, Palo Alto, Calif. Svoboda has two patents pending in the U.S. for inventions in the field of FM co-channel interference cancellation.

How Valuable?	Circle
Highly	558
Moderately	559
Slightly	560

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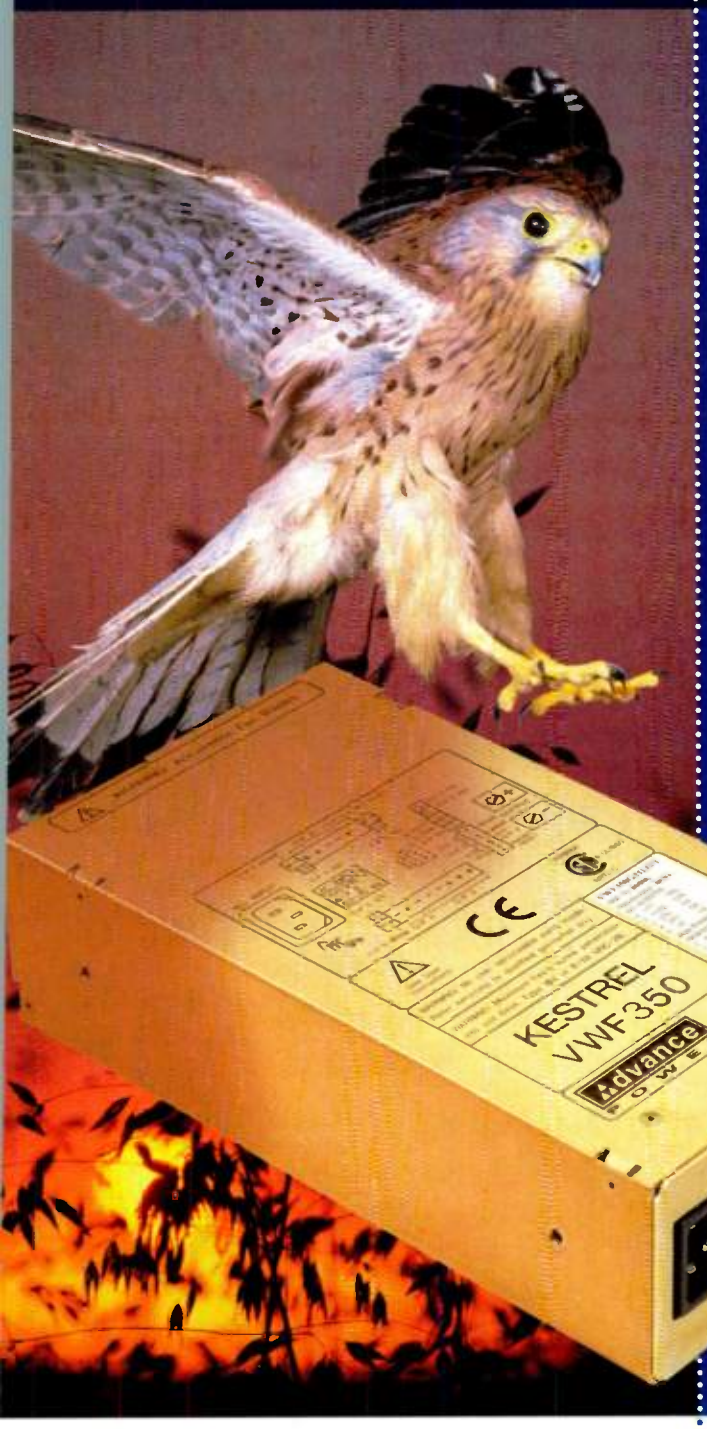

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PROCESSOR AND MEMORY DESIGNS: WHERE ARE THEY HEADING?

NAGI MEKHIEL

Are processor and memory designs actually competing to limit the computer-performance growth curve? Consider the improvements in advanced processors: *Can systems benefit from the growing power and speed of the new processors, or there is a limiting factor that will prevent the computer industry from utilizing this growth?* What about memory designs using advanced DRAMs? *Can computer systems use this technology to increase their performance?*

The answer to these questions is, unfortunately, NO. The performance growth of advanced processors has hit a wall imposed by the lack of organization between the processor and main-memory designs.

Over the years, processor performance (speed) has steadily improved and main memory (DRAM) capacity has increased. This has created a growing gap between the processor speed and the main-memory speed.

The traditional solution to the speed-gap problem has been the use of a cache system. But this solution may have created yet another, and more difficult, problem.

The cache system stores parts of the program that can be used by the processor later on, and executed at a speed that matches the processor's speed. The problem with using the cache is that not all processor references will be found in the cache, so the processor has to visit main memory (DRAM) to get the cache misses. Cache misses cannot be eliminated even with the best cache design. There also are compulsory misses (cold start) that the processor has to retrieve from the main memory (DRAM).

With the cache system, the processor can run parts of program at its rated speed. Naturally, the speed of the cache has to be the same as the processor. That's why processor designers include a cache in the processor chip (which makes matching cache speed to processor speed easier). On the other hand, the DRAM manufacturers are producing faster and more advanced DRAM chips such as fast page, cache, multibank, 3D, and synchronous.

You would think this would be an improvement because the processor is getting faster and more powerful (using larger caches), and the main memory can use available, advanced DRAM chips. Unfortunately, the performance of the overall system (the important parameter) will not necessarily improve. *In fact, these advancements could be considered counterproductive.*

DRAM is organized as an array of rows and columns of cells. In the fast-page mode, an access to the same row could be accessed at a much faster rate (using fast-page-access mode) compared to an access occurring at a different row. For example, the synchronous DRAM uses two banks, with each bank keeping a latched row. If the access occurs in the same latched row, it could use the fast-page mode. The cached DRAM transfers all DRAM accesses (in one row) to the internal DRAM cache, and provides the system with accesses from the cache at a hit rate equivalent to the fast-page hit rate.

But introducing an intercepting cache between the processor and main memory causes a problem. The cache will intercept the accesses from the processor, leaving the main memory (DRAM) with poor locality of accesses.

The new DRAM designs with special access modes like fast page and the internal DRAM cache are affected by the external cache. The performance improvements of these designs depend on the DRAM page cache hit rate. A poor program locality, therefore, causes the DRAM page/cache hit rate to decrease. In other words, the main memory (DRAM) must be exposed to the processor for the system to benefit from the advanced DRAM designs.

With a good external cache design (in the processor, or between the processor and the DRAM, such as L2), only misses from this cache will be seen by the DRAM system. This produces a poor locality of references to main memory causing a low DRAM page/cache hit rate. Simply put, the processor, when using a cache system, does not completely decouple the processor from the main memory. This results in poor references localities and a low hit rate for the fast-page/cache DRAM designs.

To analyze the impact of this problem, I compared the results of fast-page/cache DRAM miss rate with the same DRAM system with an intercepting cache. The study used simulation and assumed that the main memory uses multibank interleaving with fast-page or cache DRAM.

My assumptions were based on using a variable number of DRAM banks that are interleaved around a DRAM page size for best page hit rate. The cache is assumed to be a write back, direct mapped with variable size and block size parameters. The simulation traces are taken from Stanford University ATUM type traces for uniprogramming and multiprogramming. The traces were compared against the results of real workloads running in wide range of computers and workstations.

The simulation results for the system without an intercepting cache, gives DRAM page/cache miss rate of about 10% for a DRAM system that uses 8 banks mapped around a DRAM page size (for best performance). The miss rate decreases to less than 5% when the number of banks reaches 32.

With an intercepting cache between

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the processor and the same DRAM system, the miss rate drastically increased. The DRAM page/cache miss rate increased to 25% with a 16-kbyte cache and to 35% with a 64-kbyte cache. This is an increase of 200% to 700% in the miss rate for the same system.

Increasing the cache block size, affects the DRAM page/cache miss rate even more drastically than increasing the cache size. A 16-kbyte cache with a 4-byte block size produces a DRAM page/cache miss rate of about 20%. This miss rate increases to 35% when the cache block size increases to 16 Bytes. It reaches 50% if cache block size is 64 bytes. A 50% miss rate represents an increase of up to 10 times or 1000% in page miss rate compared to the system with no intercepting cache. The dimension of the problem can be summarized as follows:

1. It's imperative to improve main memory (DRAM) performance to boost overall system performance.
2. Advanced designs improve system performance through multi-bank and fast-page or DRAM cache techniques.
3. Processor uses an internal cache to speed up large portion of programs but has to interact with DRAM when the cache misses.
4. A cache, intercepting processor references to DRAM, has a dramatic effect on DRAM performance (destroys localities of references).
5. A good cache design is bad for the DRAM system performance and a good DRAM system design can not perform optimally because of the intercepting cache.

To tackle this problem, the following suggestions are offered:

1. Get rid of the cause of the problem, the cache concept, (because we cannot build a perfect cache). This will require that the DRAM manufacturers offer DRAM designs with speeds that match the new processor speeds—at a reasonable cost. It's probably possible to do this with an innovative design that allows some accesses to get SRAM speed from the DRAM cells. The processor will then be relieved from using a cache, and this reduces its cost and complexity.
2. Processor designers could leave the primary cache design to the DRAM designers. It's easier to optimize DRAM and primary cache performance when the cache design is included with the DRAM. This also reduces processor complexity and cost.
3. The best solution could be achieved if the processor designers and the DRAM designers agree on a common cache design that works to the advantage of each side. For example, the internal processor cache uses a hashing function that reduces an intercepting cache's effect on DRAM page/cache miss rate. The DRAM also can be reorganized in a special arrangement of columns and rows—so the intercepting cache has a minimal effect on the DRAM miss rate.

Currently, system designers have no control of either processor designs or DRAM designs. Therefore, it is advisable to evaluate the performance gain from using an extra cache, or an advanced DRAM design, and compare it with the increase in system cost and complexity.

In conclusion, a broader view of the problem is needed—one that uses nontraditional solutions for both processor and main memory designs. We cannot keep going in the current direction (increasing processor power and speed and independently increasing DRAM performance). The time has now come for the industry to make a detour toward a more open road, although it might be harder and take longer to travel it. □

DISCLAIMER: Private opinion, not representative of employer.

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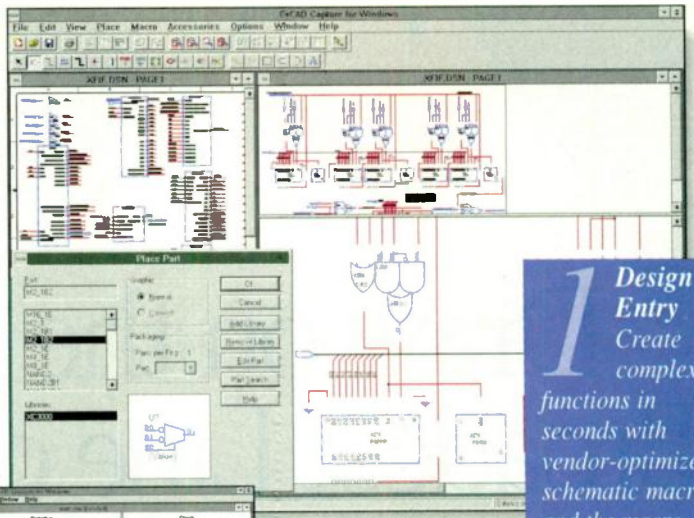
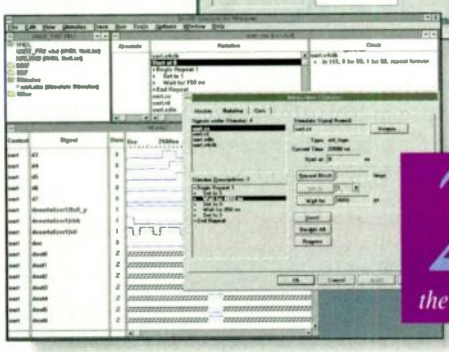


1 Design Entry *Create complex functions in seconds with vendor-optimized schematic macros and the macro recorder.*



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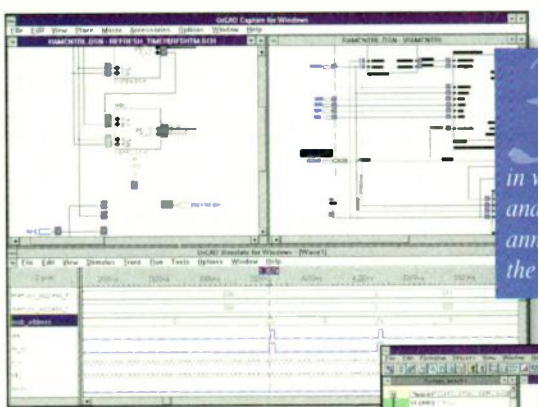
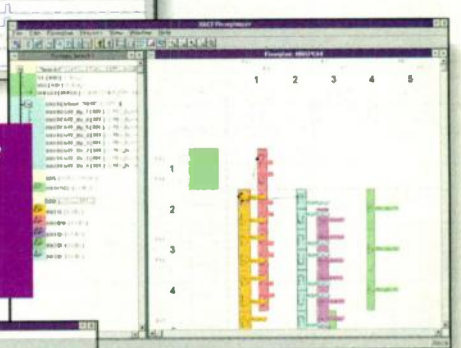
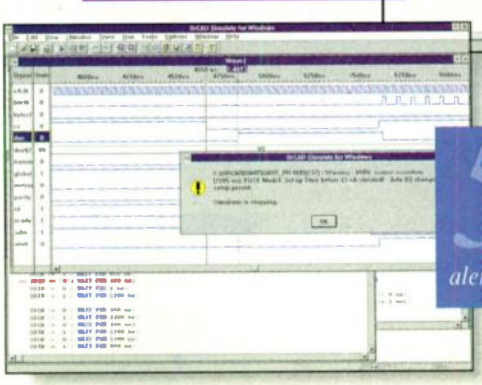


3 Functional Simulation *View results in waveform windows and see signal states annotated directly on the schematic.*



4 Place-and-Route *Press a button to create a netlist for the chosen device vendor's back-end tool.*



5 Timing Simulation *Check the corrected post-route timing in waveform windows, with automatic alert for common violations.*

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ISC	Molded, shielded, wirewound technology, moisture resistant, excellent size-to-inductance-range ratio.	1210: .01µH-100µH 1812: .01µH-1000µH	Call 800-487-9437 Document #305
ILB	Multi-layer shield beads, ideal for EMI and RFI suppression. 1206 and 0805 sizes. (0805 Preliminary)	Impedance values range from 19Ω to 600Ω	Call 800-487-9437 Document #314
ILS	Multi-layer, shielded inductor. 1206 and 0805 sizes. (0805 Preliminary)	1206: .047µH-33µH 0805: .047µH-33µH	Contact Factory
TJ	High current, vertical mount reduces PC board size, toroid design decreases EMI, 7 sizes. Current ratings up to 20 Amps.	1.2µH-5600µH	Call 800-487-9437 Document #309
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TA	Audio, telephone coupling style designed to meet FCC Part 68. Frequency range: Data/voice = 300 to 3500Hz, Data = 800 to 3500Hz. 26 models.	———	Call 800-487-9437 Document #311
LPT	Low profile surface mount, toroidal core, 2 separate windings, 4 terminals, 4545: .450" diameter. 3535: .350" diameter.	10µH-1200µH	Call 800-487-9437 Document #301
IM	Standard and "R" level E-Rel models. Axial leads, flameproof molded epoxy coating.	Standard: .10µH-10,000µH ER: .10µH-33µH	Call 800-487-9437 Document #308
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CIRCLE 520

PM DC Motor Speed Control

KLAUS ACHLEITNER, University of Cape Town, Dept. of Chemistry, Rondebosch 7700, Cape Town, South Africa, telephone: +27-21-650-2525; fax: +27-21-689-7499; e-mail: Klaus@psipsy.uct.ac.za.

Speed control of permanent-magnet (PM) dc motors with the aid of optical or dc tachometers is generally inconvenient and difficult, particularly on motors with integral gearboxes. The high-speed shaft of the motor that drives the gearbox isn't always accessible and the speed of the geared-down shaft often is too low for tachometers.

Described here is a single-supply regulating speed-control circuit that doesn't require a tachometer. It keeps the motor torque high under load by using positive feedback to compensate for the drop due to armature resistance. In unregulated variable-speed PM dc motor systems, the drop in speed under load is particularly pronounced at low motor supply voltages.

The positive-feedback generates a negative resistance that compensates for the nonlinear effects caused by armature resistance and thereby ensures that the speed-control input voltage (V_i) linearly controls the speed of the motor.

A PM dc motor can be modeled by the equivalent circuit shown in the figure. The steady-state equation for this motor is equal to:

$$V_t = E + I_A R_A \qquad (1)$$

where E = back-EMF (V); R_A = armature resistance (Ω); V_t = applied voltage (V); I_A = armature current (A); and L = winding inductance (H), and:

$$E = nK_E \qquad (2)$$

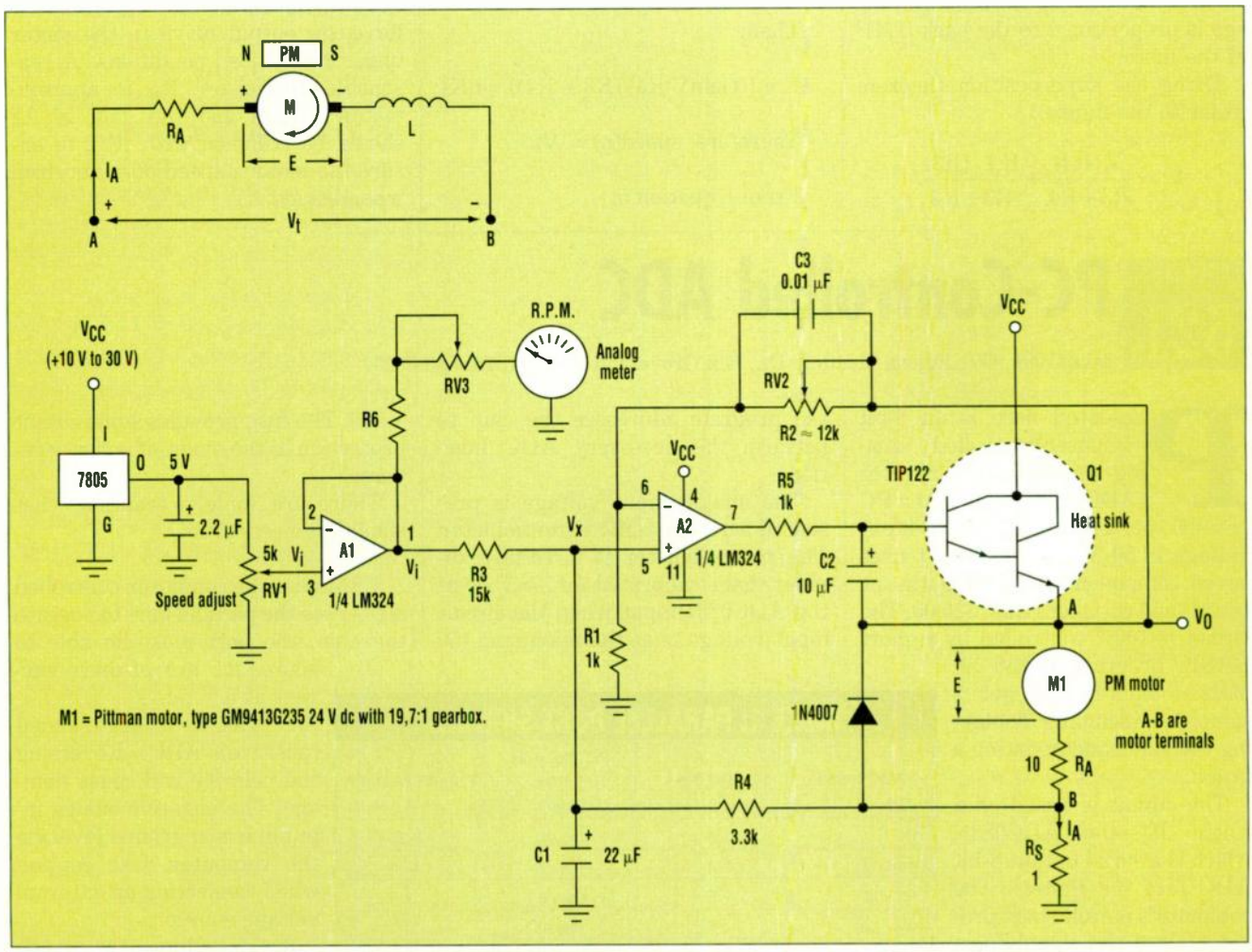
where speed = n (rpm); K_E = constant (volts/rpm); and K_T = torque constant (N-m/A).

Therefore, from equation 1:

$$V_t = nK_E + I_A R_A \qquad (3)$$

Consequently,

$$n = \frac{V_t - I_A R_A}{K_E} \qquad (4)$$



THIS SINGLE-SUPPLY SPEED-CONTROL circuit for permanent-magnet dc motors doesn't require a tachometer and keeps the motor torque high under load by using positive feedback. The positive feedback compensates for the drop due to armature resistance.

The torque is proportional to the armature current:

Torque $T = K_T I_A$

where T = damping torque + friction torque + load torque (N–m)

The power output from the motor shaft is:

$P_{out} = T\omega$(watts), i.e., at the motor shaft

where ω = shaft speed in rad/sec., and P_{out} = power in watts.

From Equation 4, if the motor slows down due to increased mechanical load, the armature current I_A increases due to the drop in back-EMF E (proportional to the speed). To linearly control the speed of the motor, the term $I_A R_A$ in Equation 4 must be compensated to ensure that the speed-control voltage is proportional to the back-EMF of the motor.

Using the superposition theorem (refer to the figure):

$$V_x = \frac{V_i(R4)}{R3+R4} + \frac{R_s I_A(R3)}{R3+R4}$$

where $R_S I_A$ = voltage proportional to armature current I_A.

Voltage gain for the input noninverting signal = [(R2/R1) + 1] = Gain

$V_O = V_X[(R2/R1) + 1]$

$V_O = E + I_A R_A + I_A R_S = V_X[(R2/R1) + 1]$

where:

$$E + I_A(R_A + R_s) = \frac{V_i(R4)\text{Gain}}{R3+R4} + \frac{R_s I_A(R3)\text{Gain}}{R3+R4}$$

Rearranging:

$$E = \frac{V_i(R4)\text{Gain}}{R3+R4} + \frac{R_s I_A(R3)\text{Gain}}{R3+R4} - I_A(R_A + R_s)$$

However, in the above equation, if:

$$\frac{R_s I_A(R3)\text{Gain}}{R3+R4} = I_A(R_A + R_s) \quad (5)$$

Then:

$E = [(\text{Gain} V_i R4)/(R3 + R4)] = nK_E$

Therefore, speed(n) $\propto V_i$.

From Equation 5:

$$\frac{R_s I_A(R3)\text{Gain}}{R3+R4} = I_A(R_A + R_s)$$

Therefore, armature resistance compensation is achieved if:

$$R_s = \frac{R_A}{[\text{Gain}(R3)/(R3+R4)] - 1}$$

The divider action of R3 and R4 together with the Gain reduce the value required for R_S to minimize the power dissipation.

C1 and R4 damp the positive-feedback signal's response time, but they also form a low-pass filter and attenuate the motor current noise fed to the A2 input. The maximum output voltage swing from A2 is approximately V_{cc} - 2 V, and there is a 1.2-V V_{be} loss by T1. This implies that the supply voltage V_{cc} should be about 5 V above the maximum desired motor voltage in order to allow for extra output drive to the motor under heavy load conditions. A reasonable choice for R_S is approximately RA/10 and the gain of A2 should be trimmed with RV2 to ensure the motor's speed does not drop when loaded. □

CIRCLE 521

PC-Controlled ADC

BARRY VOSS, 9901 Falcon Meadow Dr., Elk Grove, CA 95624; (916) 686-5027.

Presented here is an 8-bit computer-controlled analog-to-digital converter (ADC) that plugs into a PC parallel port. The maximum input voltage is 50 V dc. The circuit uses seven components (including the pc board) and costs less than $20.00. The circuit is 100% controlled by a short BASIC program. A 286 10-MHz computer can get 2 samples/s, including displaying the value and updating a graph.

The circuit is based on a single IC—the ADC0831, which is a serial output 8-bit ADC *(see the figure)*. The computer's parallel port provides all of the signals necessary to operate the chip *(Table 1)*. Table 2 shows how the program addresses the chip to perform the necessary ADC functions.

The analog input voltage is presented across a 1-MΩ potentiometer. The potentiometer is a voltage divider that's calibrated for +5 V dc at the ADC0831 input when the circuit input voltage is at the maximum (50 V dc). The fuse provides some circuit protection in the event of polarity reversal.

There are some precautions that should be heeded:

1. Because the computer-controlled ADC uses the parallel port to operate the chip, the port must be able to source 2.5 mA of drive current at 5 V dc.
2. This is a single-ended (positive) ADC. Reversing the polarity will cause damage. The negative analog input line is at ground level via the computer. Use caution when connecting an external voltage source.
3. Exceeding the maximum voltage that has been established (50 V dc) will

TABLE 1: PARALLEL PORT SIGNALS

ADC name	ADC pin	Parallel port name	Parallel port pin
-CS	1	data 3	5
IN-	3	ground	18-24
ground	4	ground	18-24
ref volt	5	data 0	2
data out	6	+busy	11
clock	7	data 1	3
Vcc	8	data 2	4

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POS-50	25-50	-110	-19	20	11.95
POS-75	37.5-75	-110	-27	20	11.95
POS-100	50-100	-107	-23	20	11.95
POS-150	75-150	-103	-23	20	11.95
POS-200	100-200	-102	-24	20	11.95
POS-300	150-280	-100	-30	20	13.95
POS-400	200-380	-98	-28	20	13.95
POS-535	300-525	-93	-26	20	13.95
POS-765	485-765	-85	-21	22	14.95
POS-1025	685-1025	-84	-23	22	16.95
NEW POS-1060	750-1060	-90	-11	30*	14.95
NEW POS-1400	975-1400	-95	-11	30*	14.95
NEW POS-2000	1370-2000	-95	-11	30*	14.95

*Max. Current (mA) @ 8V DC.
Notes: Tuning voltage 1 to 15V required to cover freq. range. 1 to 20V for POS-1060 to -2000. Models POS-50 to -1025 have 3dB modulation bandwidth, 100kHz typ. Models POS-1060 to -2000 have 3dB modulation bandwidth,1MHz typ.
Operating temperature range: -55°C to +85°C.

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K-POS1 $124.95 (contains 1ea. all models except POS-1060 to -2000).
K-POS2 $79.95 (contains 1ea. all models except POS-75,-150,-300, -1060 to -2000)
K-POS3 $79.95 (contains 2ea. models POS-1060,-1400,-2000).

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cause damage.

In the BASIC program, the parallel port is selected by the code "addout = XXX." To select the correct address for your computer, change the line of code to read:

addout = 888 (a PC clone)
addout = 956 (IBM-type computer)
addout = 632 (using LPT2)

```
'.....
'program EDCCADC written in BASIC  Barry Voss
'for use with the computer-controlled ADC pc board
'.....
'define variables
    DIM addout AS INTEGER
    DIM addin AS INTEGER
'graph
    DIM graph(3000)
'variables used
   'bitin input bit for building a digital word
   'word is the binary built from bitin
   'lastvoltage is the previous voltage value. used for determining
        'the number of characters in the previous display
   'voltage is the calculated voltage to be displayed
'.....
'SETUP                                                    '
'.....
'setup display
   SCREEN 2: WIDTH 80: CLS
'header
   LOCATE 1, 10: PRINT "Computer Controlled Analog to Digital Converter"
   LOCATE 2, 58: PRINT "voltage ="
'footer
   LOCATE 24, 1: PRINT "<ESC> to quit";
'draw the graph box
   LINE (1, 59)-(601, 161),,B
'.....
'address of parallel port                                 '
'the next line should read:                               '
'addout = 888 if you have a PC clone                      '
'addout = 956 if you have an IBM (type computer)          '
'addout = 632 if you are using LPT2                       '
'.....
   addout = 888
   addin = addout + 1
'.....
'main program                                             '
'.....
DO UNTIL INKEY$ = CHR$(27): 'do until escape key pressed
 'get data from ADC
    'clear the old data
        REDIM bitin(8) AS INTEGER
        word = 0
    'select the ADC
        OUT addout, 5
    'clock the chip this starts the conversion
        OUT addout, 7
        OUT addout, 5
    'get the 8 bit word
        FOR a = 7 TO 0 STEP -1
    'clock the chip high
        OUT addout, 7
    'the bit is present after the negative clock edge
        OUT addout, 5
    'get the status word
        bitin(a) = INP(addin)
        NEXT a
    'de-select the ADC
        OUT addout, 13
    'reconstruct the word MSB is first
        FOR r = 7 TO 0 STEP -1
        IF bitin(r) < 128 THEN word = word + (2 ^ r)
        NEXT r
    'calculate the voltage
        voltage = 50 * word/255
    'printing the voltage with formatting
       IF LEN(lastvoltage) > LEN(STR$(INT(voltage * 100)/100)) THEN LOCATE 2, 69: PRINT " "
        voltage = INT(voltage * 100)/100
        LOCATE 2, 69
        PRINT voltage
        lastvoltage = voltage
    'update the graph
        GET (3, 60)-(600, 168), graph
        PUT (2, 60), graph, PSET
        PSET (599, (160 - (100 * (voltage/50)))
LOOP
'escape pressed end the program
   'clear the parallel port
       OUT addout, 0
END
```

When setting up, the computer-controlled ADC should be plugged into the parallel port with *no voltage connected* to the analog input jacks.

The software is set up to read 0 to 50 V dc. Since this is an 8-bit ADC, the resolution is 50 V dc/8 bits = 196 mV.

Calibration is a three-step process:

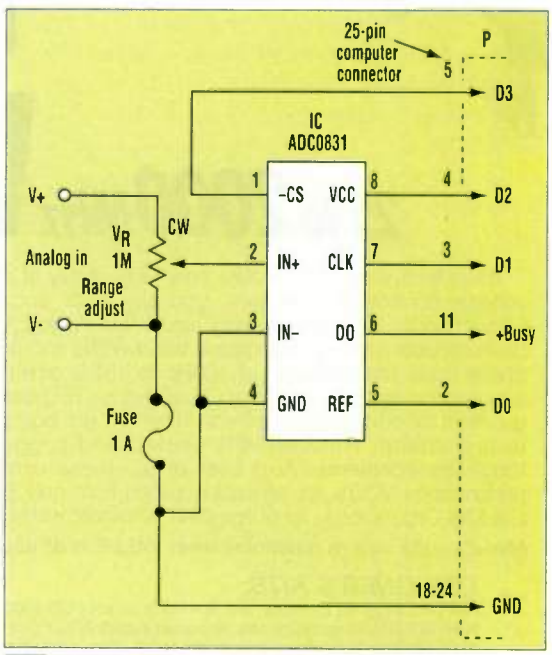
1. Adjust the input range potentiometer on the ADC fully counter-clockwise.

2. Apply a known voltage to the input of the ADC (less than 50 V dc).

3. Adjust the input range potentiometer on the ADC until the voltage displayed is the same as the known voltage.

TABLE 2: ADC COMMANDS

Parallel port data	ADC operation
00000	All off
00100	Select ADC
00101	Clock low
00111	Clock high
01101	Deselect ADC



THIS SIMPLE, INEXPENSIVE computer- controlled ADC plugs into a PC parallel port. The 8-bit peripheral device requires only seven components to implement and is completely controlled by a short BASIC program.

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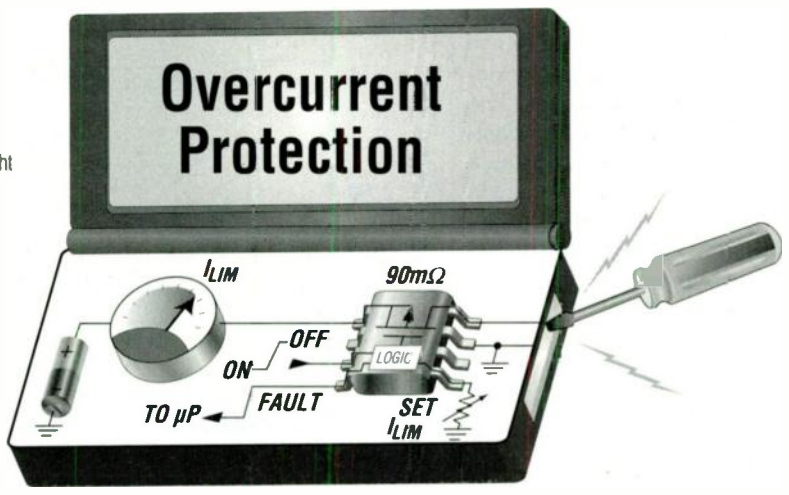

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Once the line of code in the software is changed and the calibration is done, all that's needed is to run the BASIC program. The main program obtains readings in real-time and provides the current value as well as a graph of the 600 previous values. The speed of the updating is a direct function of the computer speed. □

VOTE

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CIRCLE 522

Tunable Phase-Shift Network

J. ALVIN CONNELLY, Georgia Inst. of Technology, School of Electrical and Computer Engineering, Atlanta, GA 30332-0250; (404) 894-2911; fax (404) 894-4239.

Frequently, the need arises to control the phase shift or delay of an audio signal. The task becomes more challenging if the control must be from a voltage source rather than tuning via the usual potentiometer adjustment. The all-pass active filter shown performs this function *(Fig. 1)*. The transfer function has the form:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1 - sRC/V_c}{1 + sRC/V_c}$$

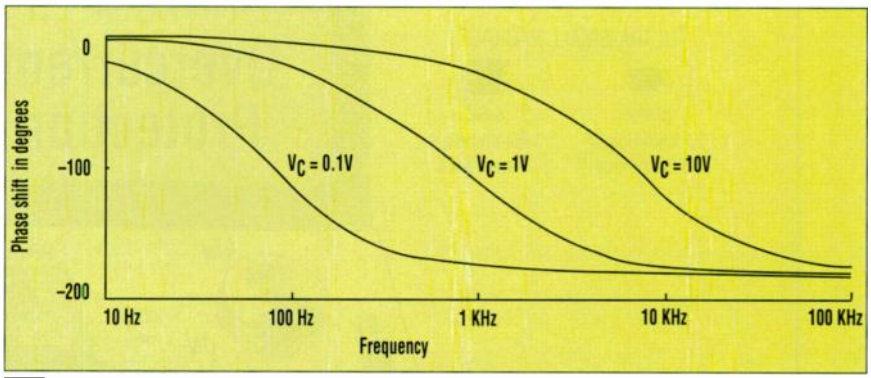
where V_c is the control voltage and $V_c > 0$. As a result, this filter has unity voltage gain for all frequencies. However, the phase shift between the input and output is given by:

$$\phi = \angle T(s) = -2\tan^{-1}\omega RC/V_c$$

and V_c can be used to vary the phase over the theoretical range from $-180^\circ \le \phi \le 0$.

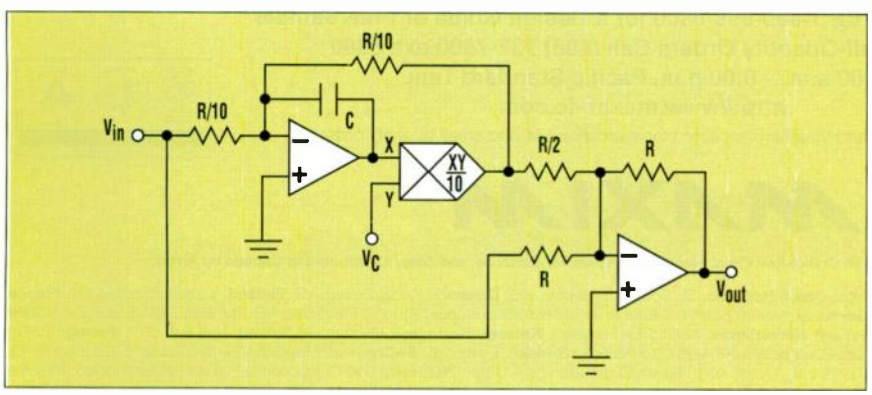
In the circuit, the left op amp and analog multiplier combination produce an inverting, first-order, low-pass filter whose pole frequency is set by the control voltage according to $\omega_p = V_c/RC$. The right op amp forms the inverting sum of the original input with a doubling of the output of the low-pass filter stage. This summation yields the desired T(s).

Generic op amps can be used for most audio frequency applications. An MC1495 analog multiplier has an adjustable scale factor, which in this case is set to 0.1 for convenience. Choosing a center frequency of f_O at the geometric mean of the audio range, or $f_O = \sqrt{20} \times 20k = 633$ Hz centers the phase shift at -90°. For $V_c = 1$ V dc, and using the relationship $f_O = V_c\omega_O/2\pi = V_c/2\pi RC$ sets the RC time constant to 252 μs. Selecting R = 10k makes C = 25 nF.



2. THE VARIATION OF PHASE SHIFT with control voltage and frequency.

Figure 2 illustrates the phase response for $V_c = 1$ V. Varying V_c from 0.1 V to 10 V shifts the phase response accordingly. Making V_c too large will restrict the amplitude of the input signal due to dynamic range limitation of the multiplier. □



1. IN THIS ALL-PASS ACTIVE FILTER, the analog multiplier provides voltage control of phase shift.

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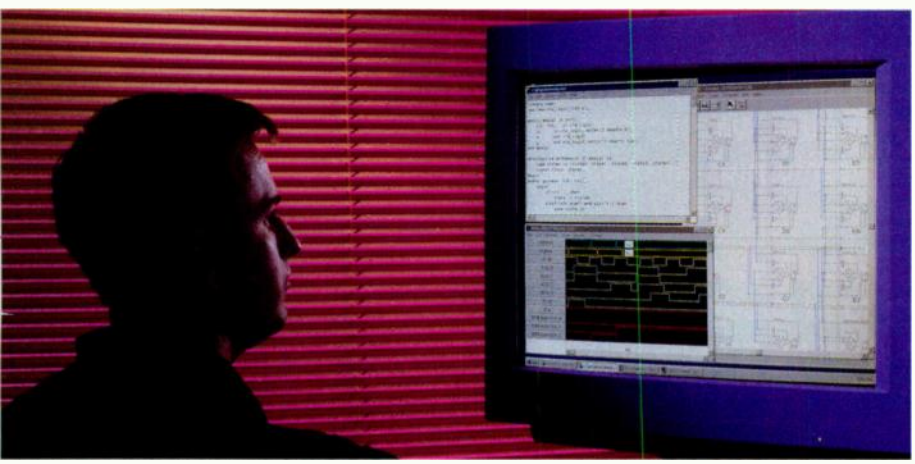

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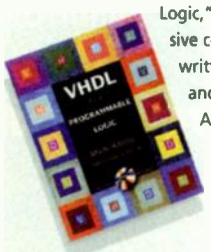

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BOB'S MAILBOX

Dear RAP:

Recently I was shown a memo explaining that all manufacture of polystyrene capacitors will cease in five years, because the only manufacturer of polystyrene film stock has quit the business. If your circuits really *need* polystyrene, you should contact your favorite capacitor supplier to make your one-time buy now. Then start redesigning your circuits.

JIM WILLIAMS
LTC, Milpitas Cailf.

For many applications, teflon, polypropylene, or NPO ceramics are just about as good as polystyrene. But in special cases where the tempco or the linearity of tempco of polystyrene is ideal, you may have to go Back to the Drawing Board. Or the Bench. Or both.—RAP

Dear Mr. Pease:

In your September 16 "Bob's Mailbox,", there was a letter from Robert L. Nuckolls, III, Consulting Engineer, Wichita, Kansas, who told about having a Tandy Model 100 that he bought via Compuserve that held 32k of RAM. He took it along on trips because it fit in his briefcase. He could do lots of writing with this Tandy 100. Then on his return from the trip, he could dump the contents into his computer.

Well, I called both Tandy and Compuserve, and neither one of them could tell me anything about such a device. I wondered if you can identify it further so I might look into buying one, or something similar. I do a little writing myself, although retired, and would find it very handy.

Incidently, I enjoy your columns, and have read all of your "What's All That Stuff About..." and found them very entertaining. I sent that magazine containing those articles to a writer friend, Sam Wilson; I'm sure he will enjoy them.

JOE RISSE, PE
Dunmore, Penn.

Read the next letter.—RAP

Dear Robert:

Regarding your September 16 column: I have info that might be useful in finding yourself a Tandy 100. It seems this early laptop is still used by newspaper reporters, and a small company exists to buy, sell, and support it: Richard Hanson, Club 100, P.O. Box 23438, Pleasant Hill, CA 94523-0438; (510) 932-8856 voice, (510) 937-5039 fax, (510) 939-1246 bbs.

I use a Tandy 200 for the same reasons as reader Robert Nuckolls. It's a model 100 with a bigger 15-line display. It's harder to find than a 100, but I think the extra lines are worth the trouble. The model 102 is a "slimmer, lighter" 100. I'm told the 600 is an orphan.

In case you'd like further details, enclosed are a spare Club 100 catalog, a copy of their most asked questions page, and copies of the pertinent pages in a 1987 Tandy Computer Catalog.

ROY W. GARDNER
Santa Ana, Calif.

P.S. Did you hear Kaiser Steel and Intel are merging and are going to produce Liberty Chips?

Roy, thanks for the info on "Appropriate Technology." I may buy one myself, since it is apparently easy to interface a Model 100 to a DOS computer.—RAP

Bob:

I was very glad to see the anthology of "What's All This..." Regarding your "Mother May I?" article, here is my favorite MMI story.

A long time ago, there was this old computer system connected to a well-used bit of analytical instrumentation. The user had run out of pre-formatted 8-in. floppies to store the data for his dissertation, and the company that made the system was no longer in business. He tried to format a standard 8-in. floppy using the system and had no luck. Thus came the request for help to me.

I used the "help" command on the system and found the brief instructions on how to use the format command. I tried formatting the disk and it asked me, "Are you sure?" I answered "Yes". It asked me "Are you positive?" I again answered "Yes."

Nothing happened. I tried again. "Yes" twice again. Nothing. "Y." "yes." "YES." "yEs." Nothing got me past the second MMI. I sent the user on a futile search for the manual. It was long lost.

I finally got so peeved at the system that I started typing all sorts of affirmative responses to the "Are you positive?" question. Some of them couldn't be printed in mixed company.

You may have guessed it by now. I finally tried "positive" as the answer to "Are you positive?", and I was rewarded with the "formatting..." response and a happy chunking in the disk drive. Needless to say, I was less than impressed with that computer system. Keep up the good work.

JOHN STANLEY
Corvallis, Oreg.

With Computers like these for friends, who needs enemies? When old computers get balky like this, they either make that happy chunking sound, or I "chunk" them off a roof.—RAP

Dear Bob:

I've been following your discussions of audiophile power amplifiers and speaker wires. Perhaps you can clarify a question that's been nagging me for several years on this subject:

If we look at the whole system, the controlled output we really care about is the position of the speaker cone, not the amplifier output voltage. In the limit, why not put a position sensor on the speaker cone and close the loop around that? For normal voice-coil-operated speakers, the displacement of the cone is proportional to the current through the speaker coil (though this is probably a first order approximation, it is certainly closer than saying the displacement is proportional to the voltage across the speaker). Therefore, why aren't audio amplifiers designed with closed loops around

PEASE PORRIDGE

their output currents?

About 15 years ago, I worked for a company that made linear magnetic-deflection amplifiers (i.e. closed-loop current out, voltage in). Some of the techs took these home and had good results using them as power amplifiers for their stereos. I never delved into this further. An added benefit of closing the loop around the output current is that the amplifier is intrinsically short circuit protected. Shorted outputs used to be, and probably still are the leading cause of power amplifier failures. This seems so obvious, I'm sure I'm missing something. Am I?

HERB PERTEN
Phillips Scientific
Ramsey, N.J.

I am sure some engineers have done this, or even closed the loop with a sensor for cone position. Maybe this did not produce "the right sound." I've heard that the natural low-frequency distortion of most speakers "sounds right," and speakers that don't distort at 20 Hz do not sound very "impressive." Maybe less distortion is not as right as more.—RAP

Dear Bob:

Re the Sept. 16 Bob's Mailbox: The "thunk" Mike Middleton hears when he turns on his TV is the high inrush of current to the degaussing coil. Hit the degauss button on your large-screen color monitor and you will hear the same sound as when it's initially turned on. It sounds impressive, but probably doesn't stress any components except for the MOV in the degauss circuit.

DIRCK SPICER
Durham, Conn.

Still, if you turn on the TV or monitor 1000 times a day, that's probably not a good idea. If the degaussing coil or the MOV don't wear out, the switch probably will.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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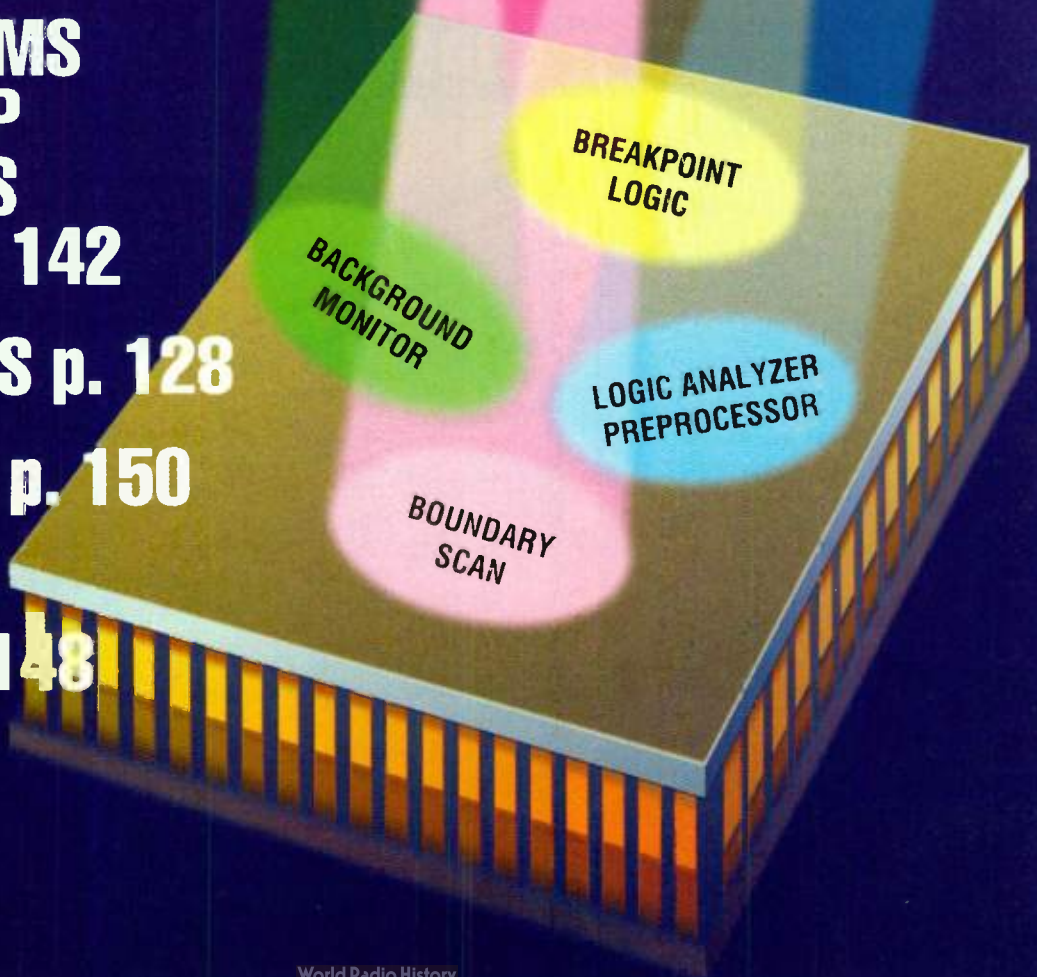

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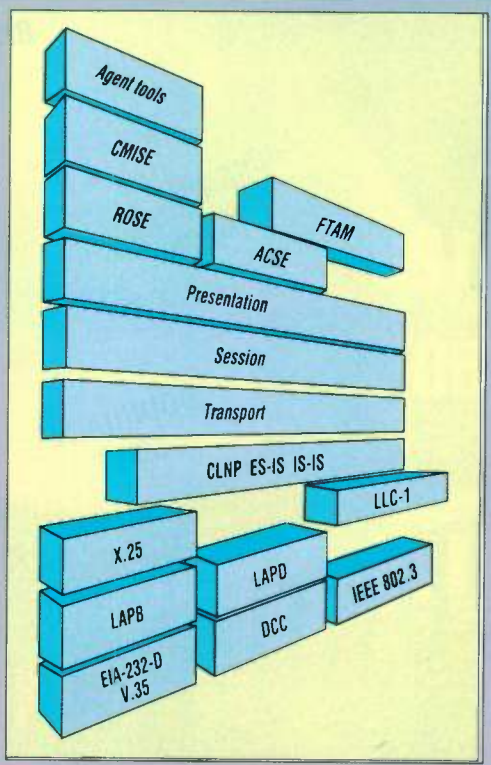

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In the last few years, this balance has been threatened by the gradual disappearance of a debugging tool that was a mainstay of embedded development. Since the days of the venerable "blue box," a programmer has been able to observe and control the operation of an embedded processor in real time. A hardware emulator could replace or augment the microprocessor in an embedded system and provide the information needed to isolate the most difficult software bugs. The emulator might be expensive and have more than its share of idiosyncrasies, but it was there when needed. For a variety of reasons, full-function hardware emulators are becoming harder to find for high-performance embedded microprocessors, resulting in what can be described as an "emulator gap." In the absence of full-function emulators for the latest microprocessors, designers need ways to bridge the gap by using other tools.

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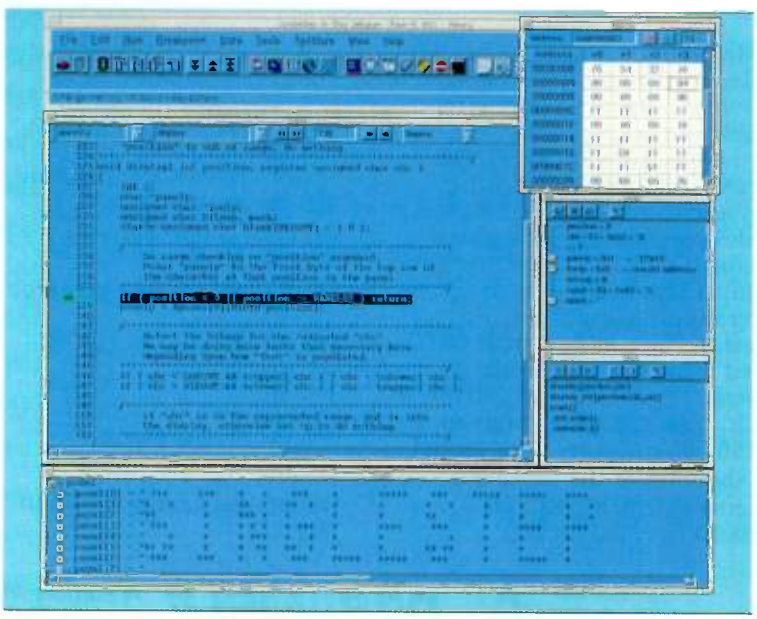

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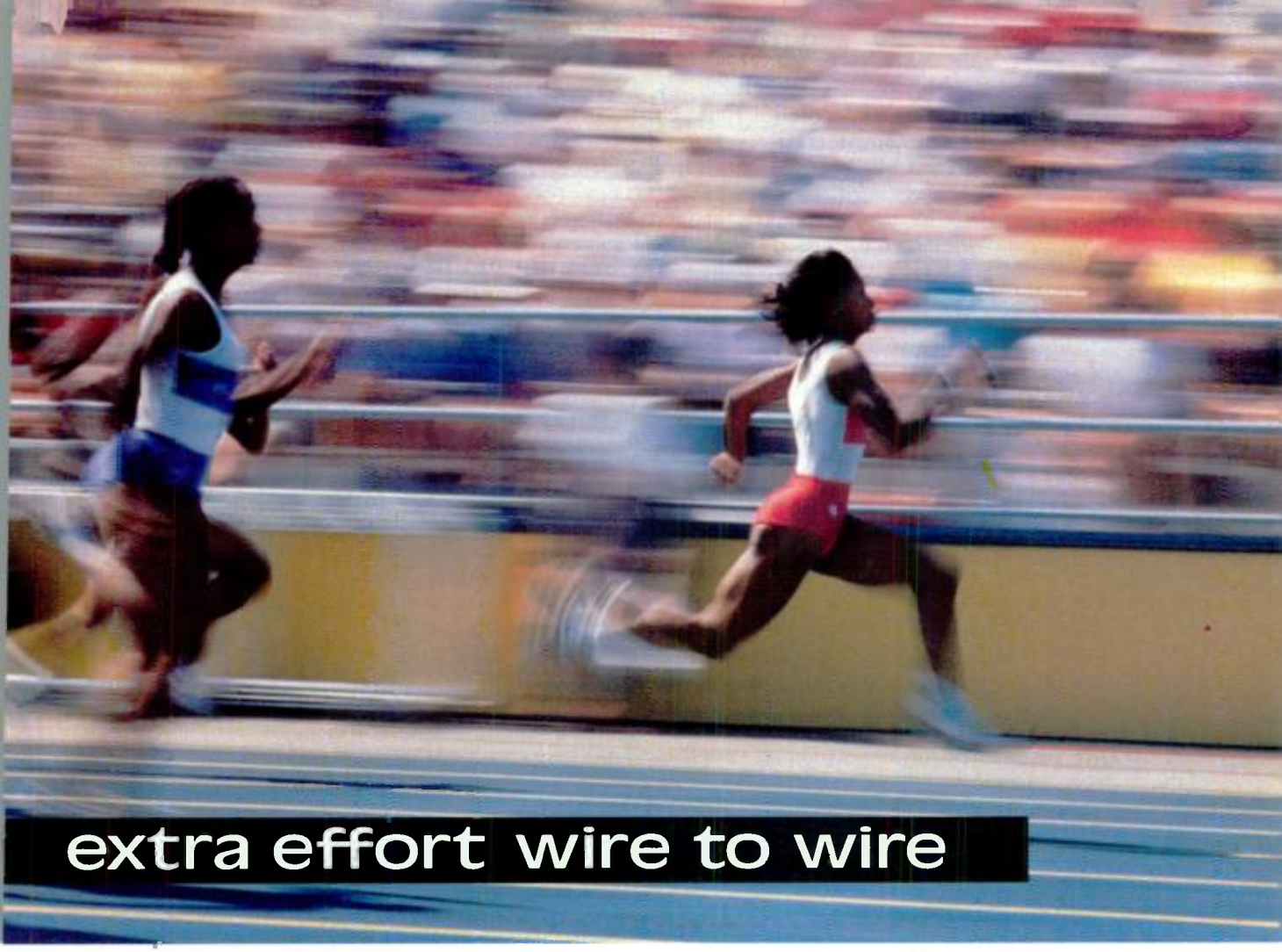

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emulators were able to keep up with all of these changes and still deliver real-time trace and execution control. In the last few years, however, performance increases have accelerated by several routes. First, instruction and data caches were added. Next, the microprocessor's internal clock rate was increased to some multiple of its input clock rate. The most recent performance increase has been achieved by executing more than one instruction in each internal clock cycle.

These more recent techniques conceal most of the instruction execution and data access activity from an observer outside the microprocessor. To determine what has actually been executed and accessed, a hardware emulator is forced to replicate much of the acceleration circuitry and needs to process clues from deep inside the microprocessor. Economic considerations have made developing emulators that can correctly see into this new generation of processors very difficult.

Embedded microprocessors are a big business, and the companies that design and manufacture them are generally very large and well capitalized. They can afford to use the most advanced design tools and semiconductor processes because of the huge volumes involved. In contrast, the market for hardware emulators is much smaller. It is serviced by small companies or small divisions of larger companies. The low unit volumes limit the tool and semiconductor technology that can economically be applied to designing and manufacturing emulators. Until a few years ago, hardware emulator designs were much less complex than those of the microprocessors they observed and controlled, so this technological disadvantage was easy to overcome. Now that they must replicate a significant portion of the microprocessor's circuitry and keep up with its high internal clock rate, the hardware emulator's technological disadvantage is much more telling. In practice, designing an emulator that can trace the execution and access activity of a modern high-performance embedded processor ranges from very difficult to nearly impossible.

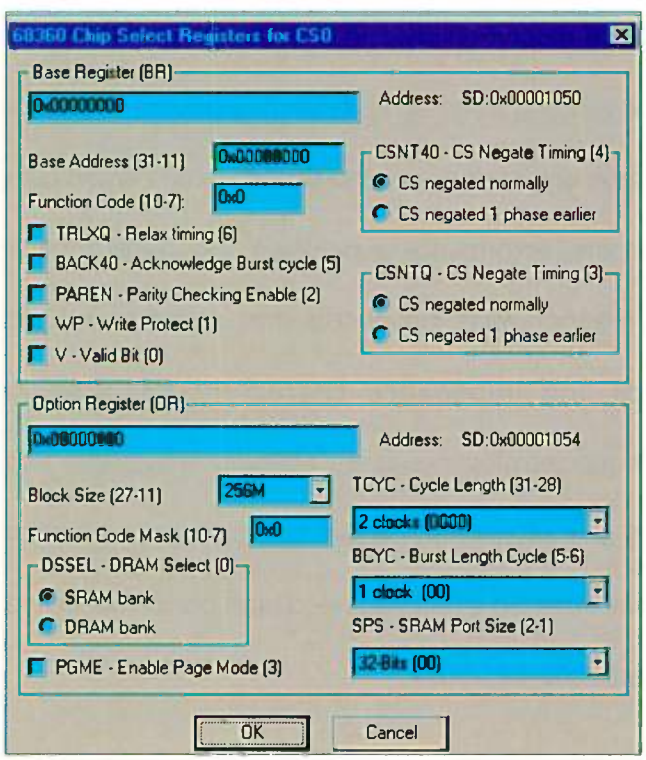
This difficulty results in delay. Developing a full-function emulator for a high-performance embedded microprocessor has become so difficult that the emulator may not be available until long after the chip starts shipping, if ever. Ensuring that the "clue" signals provided by the microprocessor are handled correctly by the emulator in all possible circumstances also is very difficult. A semiconductor manufacturer may be understandably reluctant to revise and replace its chip just to fix a diagnostic signal that has no effect on normal operation. That can mean that an emulator's execution and access tracing may not be fully debugged until after the chip has been eclipsed by the next generation of microprocessor technology. Debugging software without real-time execution and access traces and without the execution control facilities that depend on those traces has become a fact of life for many engineers. This "emulator gap" is not going to go away, but will only become more widespread as the acceleration techniques used in today's high-performance microprocessors find their way into tomorrow's midrange chips.

ON-CHIP DEBUGGING

Maximizing the ratio of performance to cost is always the highest priority in the design of a new high-end embedded microprocessor. However, facilitating efficient chip- and board-level testing also is an important consideration. The ability to observe and control the microprocessor's I/O pins and its internal state without drawing on the chip's normal operating resources makes it much easier to get better hardware test coverage and fault isolation. To this end, microprocessors began about twelve years ago to incorporate a serial test port and logic for "boundary scan" testing on the chip. In the ensuing years, a standard interface to this test logic was developed (IEEE 1149.1) that has been widely embraced. Today, many microprocessors have a serial test port that can be used to examine and manipulate most or all of their resources. Some of the newest debuggers have learned to extract software debug information from the on-chip test ports *(Fig. 1)*.

Although initially designed for hardware test, a microprocessor's serial test port can be used to perform the low-level observation and control operations that are needed to support software debugging. Since little external hardware is required to operate the serial port, a debugging tool designed to use it can be very economical. These "on-chip" debuggers started appearing about six years ago and are widely used today. An important refinement available with some microprocessors is the addition of "background monitor" logic that shortens the serial test port sequences most used for software debugging.

Speeding up the memory access sequence shortens download time and speeding up the register access sequence improves single-step time. Using only boundary scan operations, it could take several hundred clock cycles on the serial test port to load and sequence the processor states needed to read a register and return its value. With a background monitor, it takes only a few dozen clock cycles to send down the read command and register number and then get back the value. The background monitor is faster because it accepts concise commands and it has a special state machine that "cheats" and uses some of the processor's normal operational resources to move the information around the chip. This makes the internal regis-



2. DEPICTED IS THE VISUAL AIDE *for background debug mode.*

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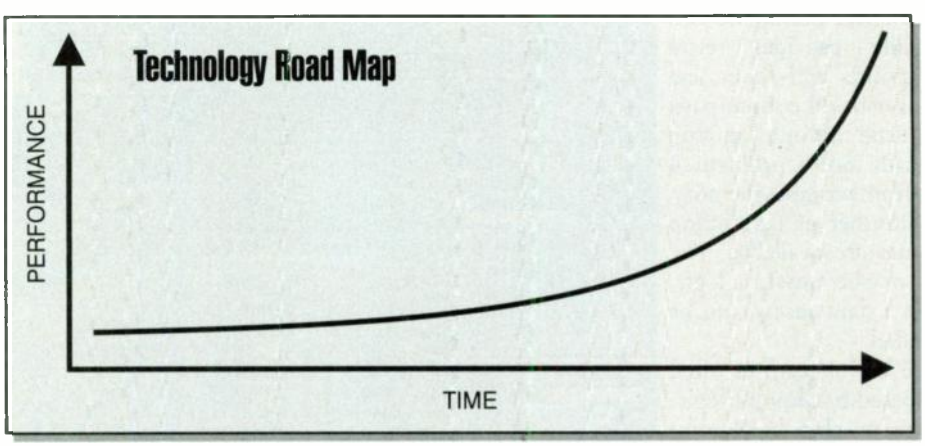

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ters available through a debugger interface that is familiar to the software developer *(Fig. 2)*. This cheating is done in a way that does not change the normal operating state of the processor.

In all, a serial test port and background monitor make it possible to display and modify system state in every way that a hardware emulator could, and at a much lower cost. There also are fewer side-effects on the target system, since no operating signals are delayed or even probed. An on-chip debugger falls short of being a full-function emulator since, by itself, it cannot trace instruction execution or data accesses in real time. It is, however, an important component of any bridge across the emulator gap. This is a case in which the microprocessor designers, however unintentionally, have built-in debugging hardware that helps solve a problem that their acceleration hardware helped to create.

When code is run from writable memory, execution can be controlled in real time by using illegal opcodes to implement instruction execution breakpoints. When code is run from ROM or if the desired break event is a data access, a full-function emulator's real-time trace of executed instructions and accessed data can be tapped to trigger the break *(Fig. 3)*. Due to pipeline delays, the break may not occur until four or more clocks after the break event. These emulator-sourced breakpoints can substantially shorten the process of finding out why an embedded system is failing. They would be sorely missed if there were no alternative. Fortunately, and in this case quite intentionally, the microprocessor designers have moved in to take up the slack.

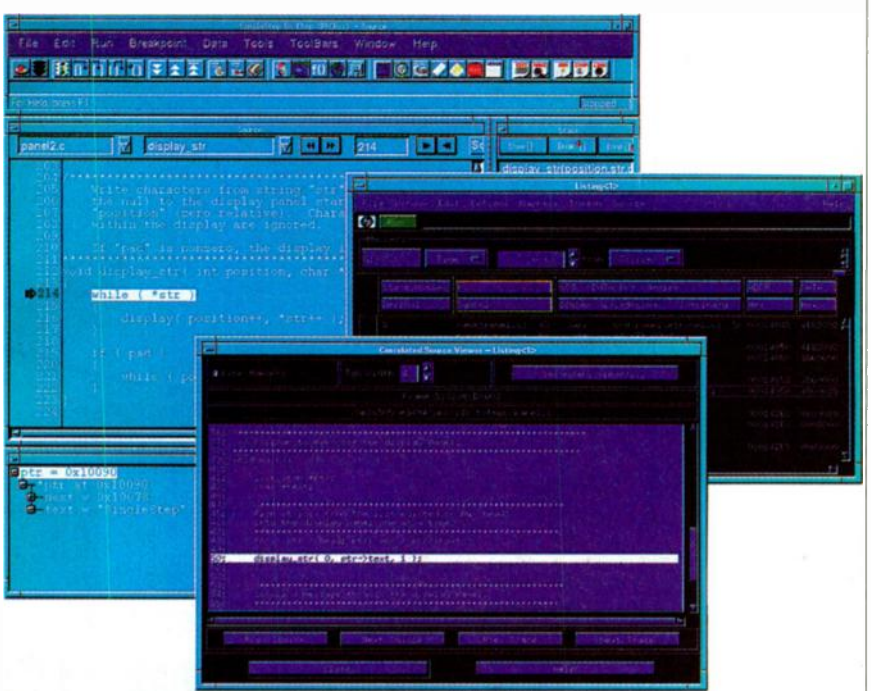
Because of the declining availability of full-function emulators, and also its relatively low cost, most high-performance embedded processor designs include some breakpoint logic. Since it is on the chip, the breakpoint logic can see every instruction execution and every memory access. When a match occurs, it can stop the processor just a clock or two later. On-chip breakpoint logic has none of the timing or loading issues that an external circuit might have, and its address input is more likely to be accurate in every possible circumstance. On the other hand, the on-chip logic generally provides fewer simultaneous breakpoints and fewer features than its emulator-based counterpart. Working with as little as one on-chip breakpoint is generally not a problem if the code is running from writable memory, and an unlimited number of instruction execution breakpoints are available. The special capabilities of the on-chip logic, such as breaking on a data access, can be conserved until needed.

One of the more useful features often found in emulator-based breakpoint logic, but often missing in on-chip breakpoint logic, is the ability to break on a combination of address and data values. One way to achieve this combination is to let the on-chip logic can break on the address. The data value can then be a condition evaluated by the debugger after it has been notified that the address break occurred. The system will pause briefly after the break occurs while the debugger accesses the data, evaluates it, and restarts the processor on a mismatch. If the chip has a background monitor and the debugger only brings up what it needs to evaluate the condition, the pause should not last long enough to materially affect the operation of the system.

A useful feature not present in most on-chip logic is breaking either inside or outside of a range of addresses. One way to do this is to set the memory or cache management hardware on the chip to cause an exception if any access in the range of interest occurs. Another method is to let the access pass off the chip where a logic analyzer can see it. Depending on how the range is bounded, it may be necessary to move the object(s) that define the range and relink so that it can be singled out by the memory or cache manager. When an access in the range occurs, either the exception handler or the logic analyzer will get the attention of the debugger, which could then do some additional qualification before breaking the processor. This approach makes a small change in the state of the memory or cache management hardware, but it is likely that it can be done without affecting any other aspect of the system's operation.

A third feature often found in emulator-based logic is breaking after a particular sequence of operations has occurred. Another way to achieve this is to set breaks for each operation in the sequence and to use a debugger variable to track the progress through the sequence. As each break is reported to the debugger it will test and update the variable, advancing or resetting it as appropriate. Only when the break for the last operation comes in and the variable indicates the other operations have all been seen in the proper order will the processor stay stopped.

Whenever any operation on the list occurs, this approach will pause the system briefly while the debugger updates the tracking variable. If this is too intrusive, an alternative is to place a noncachable access in the code adjacent to each operation in the sequence to make them all visible outside the



3. WHEN CODE IS RUN FROM MEMORY *or when data access is the desired break event, the real-time trace of executed instructions and accessed data produced by a full function emulator can be tapped to trigger the break.*

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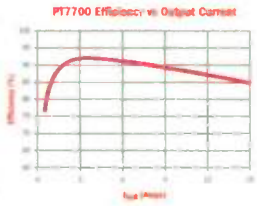

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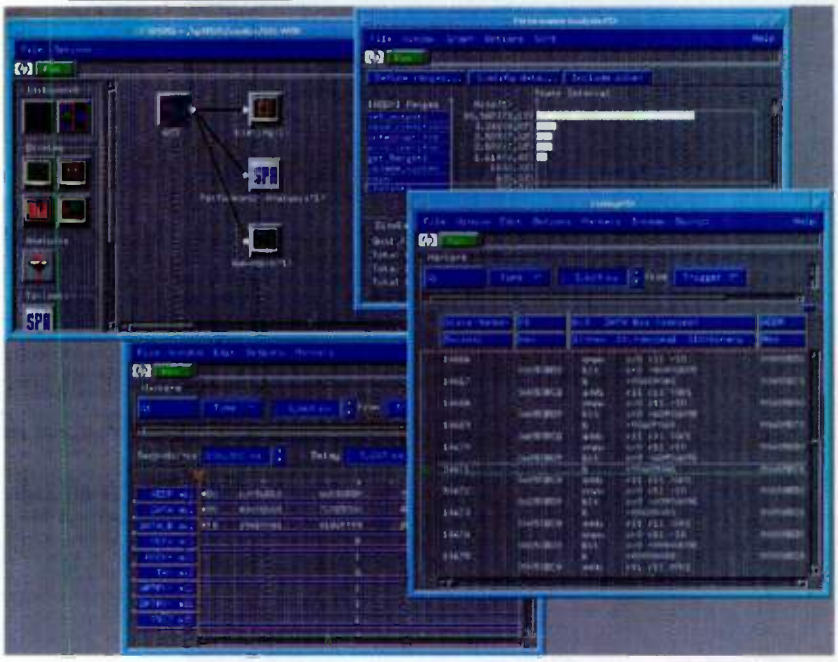
chip. A logic analyzer programmed to detect the sequence can notify the debugger when it occurs and then the debugger can break the processor. The alternatives described above illustrate the approaches that need to be considered when working without a full-function emulator. Generally, a small change in system operation or a small change in system state can provide the desired control or information. There is often a trade-off between using breakpoints and instrumenting the code. Breakpoints are more intrusive but the code modifications take longer to prepare. The challenge is in choosing changes that are easy to make and have no undesired side effects.

On-chip breakpoint facilities are increasing in the newest high-performance embedded processors. For example, the Motorola 5xx/8xx PowerPC microprocessor can compare four instruction addresses, two data addresses, and two data values at the same time. It can test for greater than, less than, not equals, as well as equals, and can be configured to require successful comparisons in sequence before breaking. Putting this level of functionality on-chip can sharply reduce the need to intrude on system state or system operation.



4. The HP 16505A *display clearly depicts the components of a logic analyzer software preprocessor: The disassembler, the combined source and trace component and the performance analyzer.*

A few of the newer microprocessors have taken a step beyond logic for real-time execution control and now include logic that provides real-time execution trace. For example, the IBM PowerPC 403 can be configured to output portions of its taken branch addresses on special trace pins. The addresses can be captured and interpreted with a small amount of external hardware. It is hoped that some of the next generation of high-performance embedded processors will go even farther in this direction, and provide execution and access trace information that can be captured with a logic analyzer.

LOGIC ANALYZER PREPROCESSOR

While full-function emulators have become harder to find, preprocessors for even the newest high-performance embedded microprocessors are available from the major logic analyzer manufacturers. These preprocessors consist of one hardware and several software components that enable a logic analyzer to perform many of the functions of a hardware emulator *(Fig. 4)*. The hardware component of a preprocessor is the microprocessor probe.

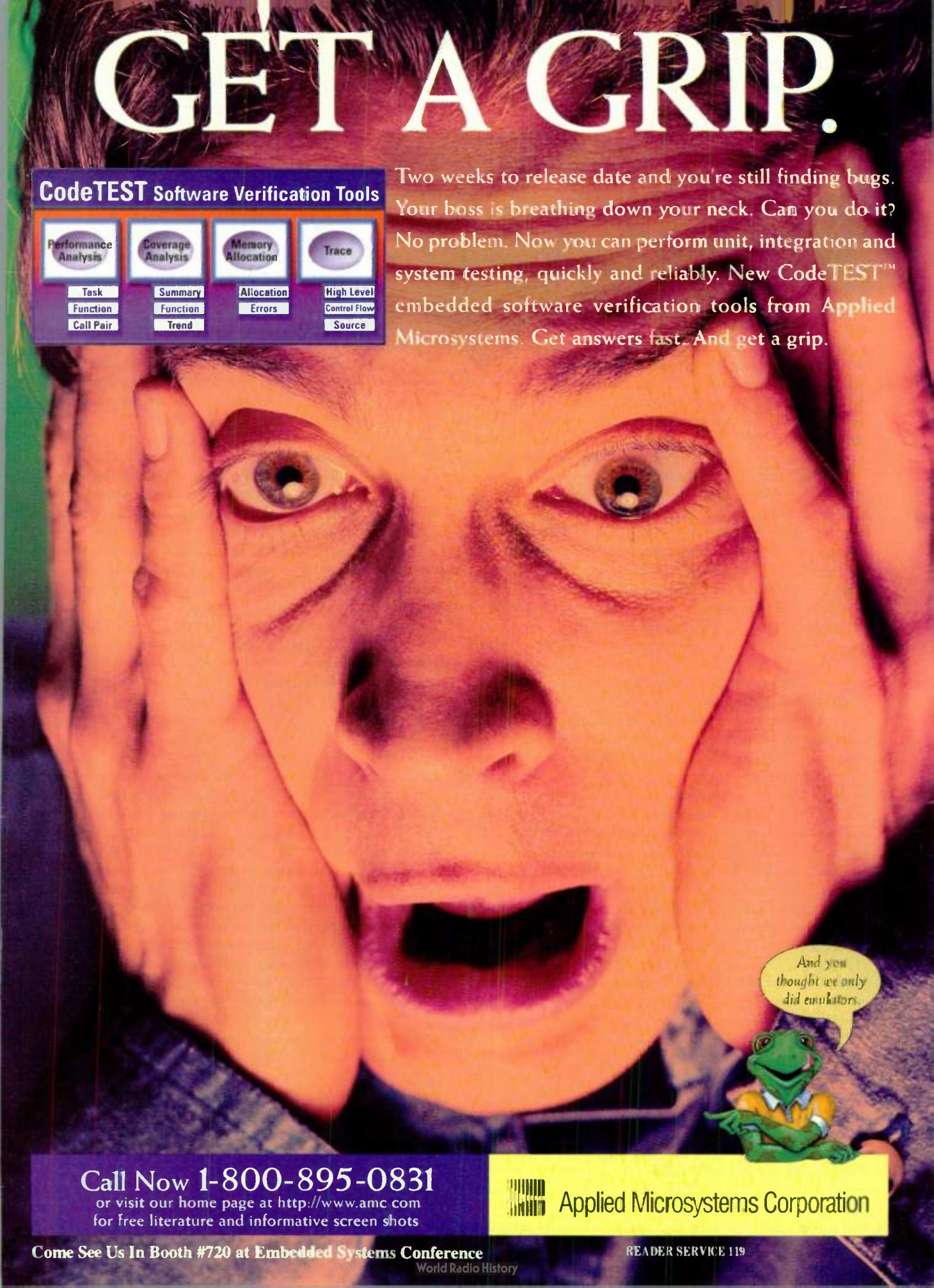
The first software component of a preprocessor is a disassembler. The disassembler divides the logic analyzer trace of the microprocessor's bus activity into address, instruction, data, and control fields and disassembles the instruction field. This rudimentary display is better suited for isolating hardware bugs, but was the best that could be obtained just a few years ago.

The next software component is the symbol processor, which adds symbol names for instruction and data addresses to the disassembled trace. This makes it much easier to relate the bus activity to the corresponding source code. The symbol processor need only know which logic analyzer and object file format is being used. It works the same regardless of which microprocessor is being observed.

The next software component combines source code with trace data to display the logic analyzer trace in a mixed mode. Each line of source code is grouped with the corresponding symbolic, disassembled bus activity. It also is possible to suppress the display of bus activity; therefore, the trace must be viewed solely in terms of executed source statements. This is the tool that lets a programmer interact with the data captured by a logic analyzer on his own terms. Ideally, this tool should be aware of the microprocessor it is observing. This should enable it to suppress the display of both prefetched instructions that were never executed as well as speculative reads that were never used.

The last software component of a preprocessor is the performance analyzer. The preprocessor extracts address information from an object file and uses it to determine how much execution time is being spent in each of a program's functions. It also can be used to help pinpoint where time is being spent inside a function. Performance analyzers generally act on full buffers of trace data, where the logic analyzer's triggering facility has been used to ensure that only the desired activity has been captured. The accuracy of the analysis is a function of the sample size, but with buffer capacities reaching to one million entries these days, getting reliable results is not hard. As with the source-level trace tool, it is best if the performance analyzer is aware of the microprocessor being observed and hence able to discount prefetched instructions that were never executed. If the analyzer cannot do this, a compiler option may be available to "pad" the end of each function with no-ops, so that prefetching after the last return will not run into the next function.

The main limitation of a logic analyzer with a preprocessor is that it can only record bus activity. When the instruction and data caches are on, the analyzer will not be able to trace most of the microprocessor's operations. Just turning off the caches when a trace is desired will not work if the reduced processor performance masks the current problem or causes a new one to appear. Given their high internal clock rates and large internal caches, today's high-performance microprocessors may slow down by a factor of five or more when caching is disabled.



Such a large change in performance may well make it impossible to reproduce the original failing behavior. Debugging with trace when caching must be enabled much of the time calls for working out creative ways to get at the needed information. Oftentimes, caching can be turned off for short periods so that a particularly revealing sequence of operations can be traced. Other times, useful status can be written by the microprocessor to a noncachable location so that it can be traced when it appears outside the chip. Both approaches will change the way the system operates, but the change can generally be kept small enough to ensure that the current problem will not be masked or replaced by another one.

There are several benefits to using a logic analyzer with a preprocessor to trace software operation. One advantage is that a preprocessor, unlike an emulator, will probe the microprocessor's signals but will never delay them. Anyone who has ever had their system become unstable or just stop working after attaching an emulator will appreciate the difference. Another benefit is the relatively small incremental cost of the preprocessor if the logic analyzer is already available. Next is the ease with which the analyzer can be shifted to another purpose, even to another microprocessor, when necessary.

The last, and largest, benefit becomes apparent when a problem involving both software and hardware behavior must be debugged. Due to its high maximum sample rate, a logic analyzer can observe and respond to subcycle timing relationships. Furthermore, since many analyzers are configured with one or two digital oscilloscope channels, they are often able to observe and respond to analog behavior as well. The three different views of the system: Software operation, timing relationships, and analog behavior can all arm and trigger each other. As a result, a problem that manifests as an intermittent software failure but is caused by a signal timing or level violation can be tracked down very efficiently.

BRIDGING THE GAP

In the absence of a full-function emulator, the clever use of other tools can help bridge the emulator gap. On-chip debugging through a serial test port with a background monitor makes it possible to display and modify system state in every way that a hardware emulator can, and with fewer side effects. On-chip breakpoint logic can be more reliable and acts with less latency than emulator-based breakpoint logic. However, it provides fewer simultaneous breakpoints and fewer features. Running from writable memory to make an unlimited number of instruction breakpoints available can offset having fewer on-chip breakpoints. Compensating for the missing features with alternative techniques, however, can be a bit more intrusive or take a bit more effort.

A logic analyzer with a preprocessor can provide the same symbolic, source-level trace information as a full-function emulator, but only when the on-chip caches are disabled. Compensating for this inability to see into the chip requires techniques that intrude to some degree on system operation. Care must be taken to ensure the intrusion is not large enough to obscure the problem being debugged. To balance this, the logic analyzer with a preprocessor is less likely to upset system timing. In addition, it is more economical and flexible, and is better able to cope with problems that involve both hardware and software behavior.

DEBUGGING EXAMPLES

The following examples illustrate some of the techniques used to isolate hard to find bugs with an on-chip debugger and a logic analyzer. They are intended to show something of the general approach as well. Note that intrusive measurements and operations are kept to a minimum and are introduced gradually. The system is run again after each change to ensure that it still fails the same way.

1. Using the PowerPC 603 processor in an interrupt-intensive, data collection and processing application, we observed intermittent errors that seemed to originate at several different points in the code. The system would back up and then take itself off-line if we turned off the cache or stopped the processor for more than a few hundred milliseconds. We picked one error that seemed to be occurring more frequently than the others. The error would form a character string that was occasionally truncated by a varying amount. A conditional instruction breakpoint was placed at the exit of the string-building loop. The break would display the count of remaining characters if it was other than zero and then resume execution. The short pause in execution caused by the breakpoint did not appear to affect the operation of the system. The break showed us that the loop would occasionally terminate with a nonzero count.

We added another instruction breakpoint at the start of the string-building loop that disabled the cache and then resumed execution. The breakpoint at the exit of the loop was modified to turn the cache on again. Running slower through just this piece of code did not appear to affect the operation of the system. The logic analyzer was programmed to start tracing with the first instruction fetched after the cache was disabled and then stop after the last fetch before the cache was turned on again. Finally, we changed the exit breakpoint to stop the processor if the exit count was nonzero. The logic analyzer showed the final, failing execution of the loop code. An interrupt had been processed in the last iteration, and the trace showed that the interrupt service routine was executing an instruction that modified the condition code register prior to saving it. This was a good example of using breakpoints and trace to isolate the problem in a way that did not materially affect the operation of the system.

2. Using the IBM PowerPC 403 processor in a networking application, we observed that packets that were received and then forwarded occasionally got sent out with a shorter message length. Only one in a few hundred packets were being affected and we could discern no pattern in the failing packets. If the system was stopped for more than a few seconds, the other processors stopped sending to it. The same problem occurred after about twenty seconds if the cache was turned of.

We wrote a short script that put a temporary breakpoint near the beginning of the packet receive code. This break called the script and then resumed execution if the packet destination was this node, and otherwise stored the received packet ID and length into debugger variables and then resumed execution. A regular breakpoint was placed near the beginning of the packet send code. This breakpoint compared the ID and length of the packet to be sent to the ones stored in the debugger variables. If both matched, the receive code breakpoint script was run. If the ID matched but the length did not, the values were displayed. In all cases, execution was resumed. These breaks did not appear to affect the operation of the system and they would occasionally, but correctly, report a short packet.

At this point, we modified the receive code breakpoint script so that the break near the beginning of the code would disable the cache. A new temporary breakpoint was inserted near the end of the receive code to turn the cache back on.

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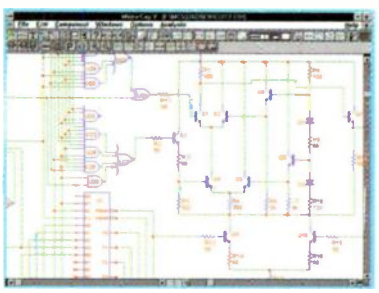

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The transmit breakpoint was modified to read from a noncachable address if the ID matched and the length did not. These new changes did not appear to affect system operation. The logic analyzer was programmed to record the execution of the receive code until it saw the noncachable read issued when the transmit code breakpoint detected an error. After the next failure and some searching in the trace buffer, we found a complete record of the reception of the failed packet. Closer inspection revealed that a mask variable that was being ANDed with the length was wrong. We used the Grep editor to search the source code for all instances where the mask variable appeared on the left side of an assignment. We found only two. One of them was the bug! A routine that ran occasionally to reclaim buffer memory was updating the wrong variable. This example adds a new trick, using a noncachable access initiated by a conditional breakpoint to control the logic analyzer.

3. Using the PowerPC 603 in a multitasking environment, we observed a failure caused by an illegal opcode trap. The system would start up and run for as little as ten seconds or as long as two minutes before the processor would stop. After each failure, the program counter and stack pointer were corrupt and the task status was indecipherable. If the caches were turned off, everything ran correctly. Using the logic analyzer to find where things had gone wrong was not much help. Following the trace back into the area of memory where the program was loaded led to a different place each time, and the source files for the kernel code were not available. We recompiled the user's code for performance measurement and located the measurement data table in noncachable memory.

The code added by the compiler to measure performance did not seem to affect system operation and it continued to fail as before. The logic analyzer was programmed to trace all accesses to the measurement data table. The trace showed that the last access to the table came from the same function on every failure. We could not find anything wrong in the source code, so we modified the failing function to run with caching disabled and recompiled. The system continued to fail as before and the logic analyzer trace showed an interrupt being serviced when we thought all interrupts were disabled. This observation led us directly to the bug. This example shows how instrumented code can work with a logic analyzer to get the necessary information off the chip without making any material change in system operation. ES

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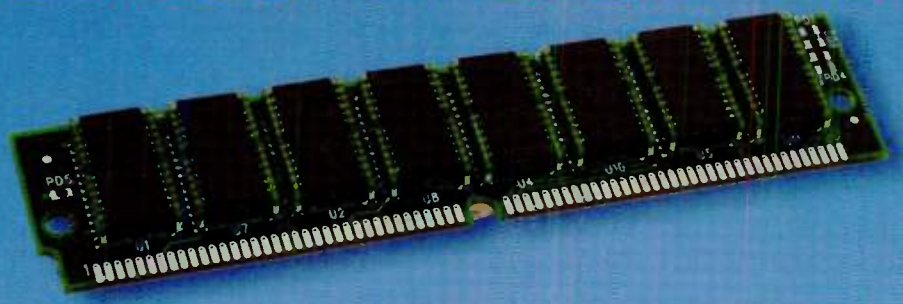

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Since many Unix programmers know and understand STREAMS, it can serve as a familiar platform on which protocol vendors can develop an application programming interface (API) that provides a constant interface across a diverse combination of hardware platforms and operating systems. In conjunction with the API, a standard Data Link Provider Interface (DLPI) can be used to define a STREAMS-based message interface for the exchange of protocol-specific messages between applications and the protocol software on the controller. The net result is an environment for software developers that reduces time-to-market and software development costs, and facilitates development of portable applications over a wide range of platforms.

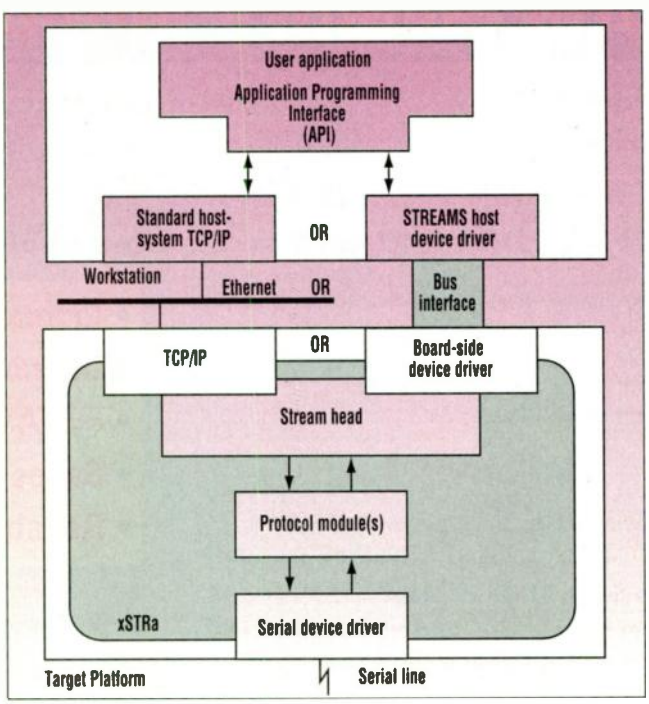
Faced with the task of developing an application for use with the vendor's platform, the system integrator must quickly come up to speed on the vendor-supplied software. For embedded communication controllers, this usually amounts to a device driver interface. For Unix device drivers, the vendor typically provides standard functions such as *open()*, *close()*, *read()*, *write()*, and *ioctl()*. However, the implementations of these functions, the associated parameters, and return values normally differ from vendor to vendor. Rather than focus on the task of developing the application, the developer is constantly challenged with mastering yet another interface.

If this is not frustrating enough, the same vendor may provide an unfamiliar interface to a new hardware platform and refer to it as an "upgrade." The software developer must support both platforms by either adding conditional logic or isolating device-specific code into separate modules. The application becomes unwieldy and software maintenance issues arise as other programmers are required to develop enhancements to the application.

Similar challenges are presented if the developer seeks to port his application to an embedded controller on a new host computer with a different bus interface, or to a LAN-based communications server that is accessed from the host via a TCP/IP connection over an Ethernet interface. In the latter case, the developer must modify the application to use TCP/IP sockets and the appropriate socket style function calls to perform *open()*, *close()*, *read()*, *write()*, and *ioctl()* operations.

Finally, once the application has been completed, the developer's engineering manager invariably will request porting the application to a different operating system. Once again, the developer is faced with the task of tackling a new environment and adapting his application accordingly.

Wouldn't it be nice to have a single Application Programming Interface (API) that presents a familiar interface to the developer, a standardized interface to all platforms, and is consistent across all protocols and operating systems? One example is the UconX API.



A STREAMS-*based API provides developers with a standard interface to a client's TCP/IP software or host driver and consists of a set of library routines that provide a session layer interface between the client and server.*

UCONX API

The UconX API provides a simple, easy-to-use interface to protocol software that runs on a LAN-based server accessed over Ethernet or a communication controller installed locally in a system's backplane. The API provides a standard interface to the client's TCP/IP software or host driver. This makes application programs easily portable among client operating systems as well as the various UconX server and embedded controller platforms.

The UconX software architecture consists of a set of library routines that provide a Session Layer interface to the transport services available between the client and server *(see the figure)*. These routines are provided in source form,

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built into a library, and linked with client applications. An application running on a client interacts, through the API, with a protocol running on the server. *xSTRa* (the UconX executive for STREAMS applications) provides a STREAMS-based environment on the server. Each connection established by a client application corresponds directly to a stream on the server. The API provides a STREAMS-compatible interface familiar to many programmers. The following functions are included in the API:

MPSopen—Open a connection
MPSclose—Close a connection
MPSputmsg—Send a message on a connection
MPSgetms—Get a message from a connection
MPSwrit—Send data on a connection
MPSread—Get data from a connection
MPSioctl—Send a control message on a connection
MPSpoll—Monitor connections
MPSperror—Display system error message

The prefix *MPS* (Multi-Protocol Server) is affixed to the name of each function to avoid conflicts with standard UNIX function calls.

The caller supplies the *MPSopen()* function with a general structure that specifies parameters to be used to open a connection to a protocol running on the server or controller. One of the parameters in the structure passed to *MPSopen()* is the server name. For a LAN-based server, the caller specifies the name of the server as it appears in the client's */etc/hosts* system file and the desired type of service as specified in the client's */etc/services* system file. The transport services available for LAN-based servers are connection-oriented (TCP/IP), and connectionless (UDP/IP). For embedded controllers, the caller need only to specify the local device name as defined in the system/*dev* directory.

If the server name is located in the */etc/hosts* file, the API opens a connection to the server over TCP/IP or UDP/IP, depending on the desired type of service specified in the *MPSopen()* request. Otherwise, the API attempts to open a connection to the embedded controller's device driver. Regardless of which type of connection is established, the application is returned a unique connection identifier to be supplied on subsequent API function calls. The *MPSclose()* function may be used to terminate the connection established by the *MPSopen()* call.

Once the connection has been opened, the client application may use the *MPSgetmsg()* and *MPSputmsg()* calls to receive and send protocol messages. Protocol messages can have a control part, data part, or both. The *MPSgetmsg()* and *MPSputmsg()* functions are equivalent to the STREAMS *getmsg()* and *putmsg()* functions. Similarly, the client application may use the *MPSread()* and *MPSwrite()* functions to receive and send data messages. These functions are equivalent to the standard UNIX *read()* and *write()* functions.

MPSioctl() is provided to send an I/O control or other special request on a connection. A typical use of this function is to set the I/O type for subsequent requests to blocking or nonblocking. The *MPSpoll()* function may be used to monitor connections for various events, such as the arrival of incoming messages. This function is equivalent to the standard UNIX *poll()* function. Finally, the *MPSperror()* function, which is equivalent to the standard UNIX *perror()* function, may be used to display error message text that is associated with an error returned by an MPS library routine.

Since the API functions are modeled after standard STREAMS functions that are familiar to many programmers, applications may be developed quickly. The programmer is not required to learn a new interface. Operating system specific details are embedded within the API, meaning that the application interface is the same whether the client machine runs Solaris, SunOS, HP-UX, Windows NT, or VMS. The application ports easily because the API is independent of protocol, hardware platform, and operating system.

EXCHANGING MESSAGES

The UconX API provides functions that allow applications to establish connections and exchange data with protocol software running in a LAN-based server or embedded controller. On the other hand, the content of the messages exchanged between the application and the server software is defined by the particular protocol. In order to achieve consistency across protocols, it is desirable to use a standard methodology of exchanging messages. This is normally referred to as a Data Link Provider Interface (DLPI).

For most protocol products, UconX uses a DLPI derived from the *Data Link Provider Interface Specification* published by the UNIX International Inc. OSI Work Group (Version 2.0.0, Aug. 21, 1991). It defines a STREAMS-based message interface between a service provider and an application. The DLPI consists of a set of primitives and structures that define the format and content of messages and the rules for using the primitives.

The general overview of the DLPI is as follows: The Data Link User is the user's application linked with the UconX API and the Data Link Provider is the protocol running on a LAN-based server or embedded controller. The user accesses the provider using *MPSopen()* to establish a stream to the provider. After the stream is created, the user and the provider communicate via the agreed upon DLPI interface. The user application sends Request/Response primitives to the provider and the provider sends Indication/Confirmation primitives to the user.

The DLPI primitives are generic in nature and thus do not imply any protocol-specific behavior. The actual content of the individual primitives will vary from protocol to protocol. This allows applications to be written within the framework of a generalized interface and thus promotes portability across protocols.

EXAMPLE APPLICATION

Once a stream has been established to the Data Link Service provider via the *MPSopen()* request, DLPI primitives are exchanged between the user application and service provider using the UconX *MPSputmsg()* and *MPSgetmsg()* API functions.

For example, the routine *send_file()* sends a text file over a connection to a service provider, and the routine *recv_file()* receives a text file from a service provider. Both routines in the example assume that blocking I/O will be used for the connection.

The *MPSputmsg()* call in *send_file()* specifies a message with both a control part and a data part. The control part and data part are distinguished by the use of the separate parameters *ctrl* and *data*. Each of these parameters must

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point to an *xstrbuf* structure with the following format:

```
struct xstrbuf
{
    int    maxlen;
    int    len;
    char *buf;
};
```

The *len* field indicates the size of the data area, to which *buf* is a pointer. The *maxlen* field is not used by *MPSputmsg()*. If the *len* field of *ctrl* is zero, the message is created without a control part. If the *len* field of *data* is zero, it has no data part. The *send_file()* routine builds a DL_DATA_REQ primitive, indicating this primitive type in the control portion of the message. The message data is included in the data portion of the message.

The *MPSgetmsg()* call in *recv_file()* is used to receive data on the connection. As was the case for *MPSgetmsg()*, both a control part and a data part are specified as parameters in the request. The *buf* field points to a data area, and *maxlen* indicates the size of that area. On return, the *len* field indicates how much data *MPSgetmsg()* has stored in *buf*. If the *len* field of *ctrl* is zero, there is no control part of the message (the example assumes there is a control part). If the *len* field of *data* is zero, there's no data part. If a DL_DATA_IND primitive is received, data is available and written to disk.

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FFTs Using Assembly Language

Philip Chen / *INTEL CORP., FM5-161, 1900 Prairie City Rd., Folsom, CA 95630; (916) 356-1688.*

Fast Fourier Transforms (FFTs) are used in several scientific and signal processing applications to compute the Discrete Fourier Transform (DFT). This transform has traditionally been implemented in C.

However, if speed is an extremely critical issue, one might also consider implementing the transform in assem-

```
DATA    SEGMENT USE16
...{BUFFER_REAL,BUFFER_IMAG,RESULT_REAL,
RESULT_IMAG} DQ ASIZE DUP(0)...
...{DELTAT,CON1,CON2,ZR,ZI,AAR,AAI,BBR,BBI,
TRASH} DQ 0...
...{POWER,IA,IB,IC,ID,IE,MM,LL,KK} DW 0...
TWO     DQ   2.0
TSIZE   DW   ASIZE
INV     DB   0
DATA    ENDS

C0DE    SEGMENT USE16 'CODE'
SCRAMBLE      PROC
        MOV   BX,AX
        MOV   AX,0
        MOV   CX,POWER
SCR1:   SHR   BX,1
        RCL   AX,1
        LOOP  SCR1
        RET
SCRAMBLE      ENDP
GET_POWER  PROC
        MOV   AX,ASIZE
        MOV   CX,-1
PW1:    SHR   AX,1
        INC   CX
        JNC   PW1
        MOV   POWER,CX
        RET
GET_POWER  ENDP
CALC_CON1     PROC     ;calculates 2*pi/N
        FILD  TSI2E
        FLD   TWO
        FLDPI
        FMUL
        FXCH
        FDIV
        FSTP  CON1
        RET
CALC_CON1     ENDP
        CALC_DELTAT   PROC   ;calculates 2*pi/N
        FILD  TSIZE
        FLD   TW0
        FLDPI
        FMUL
        FXCH
        FDIV
        FSTP  DELTAT
        RET
CCACL_DELTAT   ENDP
CALC_CON2     PROC
        FLD   CON1
        FILD  IE
        FMUL
        FSTP  CON2
        RET
CALC_CON2     ENDP
FFT     PROC
        M0V   AX, ASIZE
        SHR   AX, 1
        MOV   IA, AX    ; IA = ASIZE/2
        M0V   IB, 1     ; IB = 1
        CALL  CALC_CON1
        MOV   LL, 1
FFT_L00P1_T0P:
        MOV   AX, LL
        CMP   AX, POWER
        JA    FFT_LOOP1_EXIT
        MOV   IC, 0
        MOV   AX, IA
        MOV   ID, AX    ;id-ia
        MOV   KK, 1
FFT_LOOP2_TOP:
        MOV   AX, KK
        CMP   AX, IB
        JA    FFT_LOOP2_EXIT
        MOV   AX, IC
        M0V   DX, 0
        MOV   BX, IA
        DIV   BX              ; AX = IE/IA
        CALL  SCRAMBLE  ; SCRAMBLE AX
        MOV   IE, AX          ; scrambled ie/ia
        CALL  CALC_CON2
        FLD   CON2
        FSINCOS
        FSTP  ZR              ; STORE ZR
        CMP   INV, 0
        JE    FFT1
        FLD   ZI
        FCHS
        FSTP  ZI    ;NEGATE ZI
        JMP   FFT2
        FFT1:   FSTP  ZI
        FFT2:   MOV   AX, IC
                MOV   MM, AX
                FLD   ZI
                FLD   ZR
FFT_LOOP3_TOP:
        MOV   AX, ID
        DEC   AX
        CMP   MM, AX
        JA    FFT_LOOP3_EXIT
        MOV   EBX, 0
        MOV   BX, MM
        MOV   EDX, 0
        MOV   DX, IA
        ADD   EDX, EBX  ; ebx=mm, edx=mm+ia
        {FLD  BUFFER_IMAG
              [EBX*TYPE BUFFER_IMAG]
        FLD   BUFFER_REAL
              [EBX*TYPE BUFFER_REAL]} X2
        {FLD  ST (1)} x2
        FMUL  ST, ST (6)    ;xr (mm+ia) *zr
        FINCSTP
        FMUL  ST,ST(6)      ;xi (mm+ia) *zi
        FDECSTP
        FADD
        FLD   ST (0)
        FADD  ST, ST (4)          ; bbr+aar
        FSTP  BUFFER_REAL
              [EBX*TYPE BUFFER_REAL]
        FSUBR ST ST (3)           ; aar-bbr
        FSTP  BUFFER_REAL
              [EDX*TYPE BUFFER_REAL]
        FMUL  SR,ST(5)
        FINCSTP
        FMUL  ST,ST(3)
        FDECSTP
        FSUBR
        FCHS
        FLD   ST (0)
        FADD  ST, ST (3)  ; st=bbi+aai
        FSTP  BUFFER_IMAG
              [EBX*TYPE BUFFER_IMAG]
        FSUBR ST, ST (2)  ; aai-bbi
        FSTP  BUFFER_IMAG
              [EDX*TYPE BUFFER_IMAG]
        {FSTP  TRASH} X2
FFT_LOOP3_BOTTOM:
        INC   MM
        JMP   FFT_LOOP3_TOP
FFT_LOOP3_EXIT:
        {FSTP  TRASH} X2
        MOV   AX,IA
        SHL   AX,1
        PUSH  AX
        ADD   AX,IC
        MOV   IC, AX
        POP   AX
        ADD   AX, ID
        MOV   ID, AX
FFT_LOOP2_BOTTOM:
        INC   KK
        JMP   FFT_LOOP2_TOP
FFT_LOOP2_EXIT:
        SHR   IA, 1
        SHL   IB, 1
FFT_LOOPI_BOTTOM:
        INC   LL
        JMP   FFT_LOOP1_TOP
FFT_LOOP1_EXIT:
        CMP   INV, 0
        JE    FFT3
        CALL  NORMALIZE_INVERSE
FFT3:   RET
FFT     ENDP
NORMALIZE_INVERSE   PROC
        MOV   CX, ASIZE
        MOV   EBX, 0
        FILD  POWER
        FCHS
NORM1:  FLD   BUFFER_REAL [EBX* TYPE BUFF-
ER_REAL]
        FSCALE
        FSTP  BUFFER_REAL[EBX* TYPE BUFF-
ER_REAL]
        FLD   BUFFER_IMAG
              [EBX* TYPE BUFFER_IMAG]
        FSCALE
        FSTP  BUFFER_IMAG
              [EBX* TYPE BUFFER_IMAG]
        INC   EBX
        LOOP  NORM1
        FSTP  TRASH
        RET
NORMALIZE_INVERSE     ENDP
CALC_SIN      PROC
        MOV   CX, ASIZE
        MOV   EBX, 0
        FLD   DELTAT
CALCS1: MOV   IA, BX
        FILD  IA
        FMUL  ST, ST (1)
        FSIN
        FSTP  BUFFER_REAL
              [EBX* TYPE BUFFER_REAL]
        INC   EBX
        LOOP  CALCS1
        FSTP  TRASH
        RET
CALC_SIN          ENDP
UNSCRAMBLE    PROC
        MOV   EDX, 0
        MOV   EDX, 0
UNSCR1:
        MOV   AX, DX
        CALL  SCRAMBLE
        {FLD  BUFFER_REAL
              [EDX*TYPE BUFFER_REAL]
        FSTP  RESULT_REAL
              [EAX*TYPE BUFFER_REAL]} X2
        {MOV  ESI,DWORD PTR BUFFER_REAL
              [EDX* TYPE BUFFER_REAL]
        MOV   DWORD PTR RESULT_REAL
              [EAX* TYPE BUFFER_REAL] ,ESI}
{repeat again for BUFFER_REAL+4, then
 BUFFER_IMAG and BUFFER_IMAG+4)...
        INC   EDX
        CMP   EDX,ASIZE
        JNE   UNSCR1
        RET
        UNSCRAMBLE    ENDP
        START:  MOV   AX,DATA
                MOV   DS,AX
        CALL  {GET_POWER, CALC_DELTAT,
               CALC_SIN, FFT, UNSCRAMBLE}
        EXIT:   INT   20H
        CODE    ENDS
        END   START
```

bly language.

The following is one such example: A series of discrete points separated into real and imaginary parts (BUFFER_REAL AND BUFFER_IMAGE) are arguments to a procedure which computes the FFT and stores the results in their real and imaginary counterparts (RESULT_REAL and RESULT_IMAGE).

The procedure works by first computing the power needed, then goes through a nested set of inner and outer loops to compute the transform.

Furthermore, given the FFT's reciprocal nature, the procedure can also be calibrated to compute the inverse FFT by setting the variable INV to 1 instead of 0 (the divide by number of points part will have to be done by hand, though).

To vote for this item as the "Best of Issue" in Software Ideas for Design, circle 621.

Convert Number Base To Any Other Base

ALAN M. LAND / *KEYSTONE DIGITAL CO., 107 Poplar St., Pittsburgh, PA 15202; (412) 921-5943.*

With this program, BASEist, written in Microsoft QBasic, you can enter the base of an input number, the number itself, and then the desired output base (from 2 through 36), and wham—out comes the new number in the requested base. You can reuse the input number as many times as you want with the REIN function, and you can also reuse the output number as REOUT.

Care must be taken with entering numbers with this program. The worst that can happen is that your overflow, and end up back in Basic.

The allowable ranges are:

Bases: 2 through 36.

Digits: 15 fractional digits, such as 0.999999999999999 (all bases).

base 2: 22 integer digits
base 3: 14 integer digits
base 4: 11 integer digits
base 5: 9 integer digits
base 6: 8 integer digits
base 7: 8 integer digits
base 8: 7 integer digits
base 9: 7 integer digits
base 10 through 14: 6 integer digits
base 15 through 24: 5 integer digits
base 25 through 36: 4 integer digits.

The input is not case sensitive—your input is automatically converted to upper case. However, note that although you will get results if you enter the wrong digit modulo, those results will be incorrect.

The digit modulo is always 1 less than the base. The same applies to alphabetic characters whose values are 10 through 35.

A much more advanced version of this program is available from the author.

To vote for this item as the "Best of Issue" in Software Ideas for Design, circle 622.

```
first:  CLEAR : CLS: DIM f(15): DIM i(23): DIM g$(2): DIM q(23)
        CLS : LOCATE 2, 1: w1$ = STRING$(36, "#")
main:   PRINT w1$; "MENU"; w1$: PRINT "1 EXIT  2 NEXT  3 REIN  4 REOUT ";
        INPUT a%: ON a% GOTO ex, nex, rein, reout
        GOTO main
ex:     END
nex:    PRINT "Enter base of input number";
        GOSUB bin: b1% = b%:  PRINT "Input base";  b1%;  "number";
        GOSUB regs
        GOSUB in
cutnex: PRINT "Enter base for output number";
        GOSUB bin: b2% = b%
        GOSUB regs
        GOSUB cruxt
        PRINT z$; "base"; b1%: PRINT "-> ("; z; "base 10) ->"
        PRINT p$; "base"; b2%: GOTO main
rein:   GOSUB regs: b% = b1%
        GOSUB cutin: GOTO cutnex
reout:  GOSUB regs: b% = b2%:  b1% = b2%: z$ = p$
        GOSUB cutin: GOTO cutnex
regs:   ERASE  f, i, g$, q: RETURN
bin:    INPUT b%: IF b% < 2 OR b% > 36 THEN GOTO bin: RETURN
in:     INPUT z$: z$ = UCASE$(z$)
cutin:  n% = LEN(z$):  d% = INSTR(1, z$, ".")
        IF d% = 0 THEN GOTO whole
        IF d% = 1 THEN GOTO frac
        i% = d% - 1: f% = n% - d%: GOTO char
whole:  i% = n%: f% = 0:GOTO char
frac:   i% = 0: f% = n% - 1
char:   IF f% = 0 THEN GOTO skpf
        g$(2) = MID$(z$, d% + 1, f%)
        FOR k% = 0 TO f% - 1
        a% = ASC(MID$(g$(2), k% + 1, 1))
        GOSUB ask
        f(k%) = a%
        NEXT
        IF i% = 0 THEN GOTO mac
skpf:   g$(0) = LEFT$(z$, i%)
        FOR k% = 1 to i%
        a% = ASC(MID$(g$(0), k%, 1))
        GOSUB ask
        i(i% - k%) = a%
        NEXT
mac:    x = 0: y = 0: z = 0: IF f% = 0 GOTO ads
        FOR k% = 0 to f% - 1: y = y + f(k%) * b% ^ - (k% + 1): NEXT
ads:    IF i%=0 THEN GOTO sum
        FOR k% = 0 TO i%: x = x + i(k%) * b% ^ k%:  NEXT
sum:    z = x + y
        RETURN
ask:    IF a% < 58 THEN  a% = a% -48
        IF a% > 64 THEN a% = a% - 55
        RETURN
cruxt:  IF x > 0 THEN GOSUB mint
        IF y = 0 THEN GOTO show
        g$(1) =".": GOSUB mfr
show:   p$ = g$(0) + g$(1) + g$(2)
        RETURN
mint:   e% = INT(LOG(x) / LOG(b%)):  q(0) = x
        FOR k% = 1 TO e% + 1
        q(k%) = INT(q(k% - 1) / b%):  i(k% - 1) =  q(k% -1) MOD b%
        NEXT
        IF q(e%) = 0 THEN i(e%) = q(e% - 1)
        IF q(e%) > b% - 1 THEN GOTO bug
        GOTO fig
bug:    i(e%) = 0: i(e% + 1) = 1: e% = e% + 1
fig:    FOR k% = e% TO 0 STEP -1
        a% = i(k%)
        GOSUB conv
        g$(0) =  g$(0) + a$
        NEXT
        RETURN
mfr:    FOR k% = 0 to 15: y = y * b%: f(k%) = INT(y): y = y - f(k%): NEXT
        j% = 15: DO WHILE  f(j%) = 0: j% = j% = 1: LOOP
        FOR k% = 0 TO j%
        a% = f(k%)
        GOSUB conv
        g$(2) = g$(2) + a$
        NEXT
        RETURN
conv:   IF a% < 10 THEN a$ = CHR$(a% + 48)
        IF a% > 9 THEN a$ = CHR$(a% + 55)
        RETURN
```

SPREADSHEETS FORM DATA-ANALYSIS TOOL

DADiSP, the graphic spreadsheet for scientific data analysis, now works with Microsoft Excel to offer seamless integration and data exchange. Engineers now can transfer collected data from Excel spreadsheets into DADiSP to exploit its powerful analysis and graphic features. DADiSP provides hundreds of functions in a menu environment, enabling users to build complex programs or analysis chains, without programming, by linking functions through a series of interactive analysis cells. As new data is entered, or as functions change, all cells recalculate and update automatically and graphically. DADiSP's data management and display capabilities allow users to work with data series, matrices, waveforms, and signals. From DADiSP, users can initialize Excel, retrieve data from Excel, send data to Excel, transfer data automatically as cells update, and execute commands. From Excel, users can retrieve analyzed results from DADiSP, send data to DADiSP, and activate DADiSP commands. A student edition of DADiSP is available free of charge to students registered at accredited institutions from the company's World Wide Web home page (http://www.dadisp.com).

DSP Development Corp., *One Kendall Square, Cambridge, MA 02139; (617) 577-1133.*

CIRCLE 860

VISUALIZATION TOOL BOOSTS PRODUCTIVITY

Version 7.0 of Tecplot software adds a new graphical interface, animation, and page layout to help engineers and scientists visualize and plot large amounts of data. This version promotes increased user productivity when working with data sets generated by numerical simulation (such as computational fluid dynamics), statistical analysis, data acquisition, and other sources. Tecplot not only helps users interactively explore and analyze multidimensional data sets, but also supports the preparation of high-quality plots for reports and presentations. The software can transform millions of data points into two- or three-dimensional images such as wire-mesh plots, contour lines, vector fields, light-source shaded plots, and XY plots. Other viewing options include multiblock, curvilinear grids for depicting objects from aircraft wings to car engines to soil structures, unstructured finite-element grids, 3D surface and volumetric models, animation, and customized results through data manipulation. The software lets users interact with data in point-and-click fashion. Also easily accomplished is switching plot types and views to get different perspectives on data. A unique page-layout capability lets users produce presentation-quality outputs without moving plots to another software package. Tecplot runs on most Unix workstations (under Motif) and PCs running

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Microsoft Windows (3.x, Windows 95 and Windows NT). Tecplot will soon be available on VMS, Linux, and Windows NT for the DEC Alpha. Single-user pricing ranges from $995 to $3195, depending on the platform and the license type.

Amtec Engineering Inc., *P.O. Box 3633, Bellevue, WA 98009-3633; Mike Perry, (206) 827-3304, ext. 206.*

CIRCLE 861

NUCLEUS POSE JOINS NEST CLIENT SDK

The integration of Nucleus POSE SDK from Accelerated Technology with Novell's NEST Client SDK allows developers to build NEST applications directly onto a PC using Borland's tools. The Nucleus POSE SDK is designed for developers who already have the NEST Client SDK. With Nucleus POSE SDK, a user can build a reference platform using the Nucleus PLUS operating system. The software includes all the scripts necessary for building the demonstration system, a limited version of the Nucleus PLUS kernel, and POSE layer for Nucleus PLUS. As shipped, a developer can use the Nucleus POSE SDK to build the NEST protocol stack and run it on a standard PC. The Novell Protocol test tools can then communicate with the protocol stack. The limited version of the Nucleus PLUS kernel allows one additional task (several are used by the NEST protocol stack) to be created for implementing a true NEST application. By simply changing the compiler and linker options in the build scripts and developing an Ethernet driver, applications developed on a PC can be running on an embedded target in a short time.

Accelerated Technology Inc., *720 Oak Circle Dr. East, Mobile, AL 36685; (334) 661-5788 or (800) 468-6853; e-mail sales@atinucleus.com.*

CIRCLE 862

SOFTWARE TOOLSET SUPPORTS MOTO DSPs

The DSP56000 from BSO/Tasking is for programming all variants of Motorola's family of 16- and 24-bit DSPs, including the DSP56002, DSP56005, DSP56007, DSP56009, DSP5656156, DSP56166, and DSP56300 cores. The toolset is built around the company's Embedded Development Environment—a package of program building, editing, code generation and debugging tools that includes ANSI C and C++ compilers, a Motorola-compliant assembler with pipeline optimization, and the CrossView source-level debugger. The compiler package maximizes the instruction set of the DSP65000 architecture and offers code efficiency without violating the ANSI-C standard. Code is generated through support for a number of language extensions and inline functions, as well as a range of optimization techniques. These techniques include common subexpression elimination, loop recognition, and variable-usage analysis. The compiler also supports three memory modules for the DSP56000 family—reentrant, static and mixed reentrant/static—to ensure code efficiency. The macroassembler performs optimization techniques such as instruction parallelizing, nop insertion and delay slot filling, nop removal, and branch optimizations for optimal in-

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struction sequences. The assembler also supports numerous controls and pseudo instructions to save memory. The high-level-language CrossView Windows debugger supports Motorola's Application Development System environment for the DSP56000, DSP56100, and DSP56300 controllers. It can debug C and assembly-level source programs using the DSP56000 family's On-Chip Emulation debugging facilities. CrossView also provides different run-time views of the application, including stack, registers, and simulated I/O, and uses the debug information from the compiler and assembler. Pricing for the complete package is $3950, and includes 12 months of maintenance. Individual tools are priced at $995. Platform support includes DOS, Windows, Sun Sparc, HP9000/700, and Digital Alpha.

Boston Systems Office/Tasking, *333 Elm St., Dedham, MA 02026; (617) 320-9400; e-mail vaughn@tasking.nl.*

CIRCLE 863

ORBIX/ADA GIVES ADA DEVELOPERS CORBA

A joint development by IONA Technologies and Objective Interface Systems has produced Orbix/Ada 1.0, which binds the Ada95 language to IONA's Orbix object request broker. Orbix is IONA's implementation of the Object Management Group's CORBA 2.0 (Common Object Request Broker Architecture) specification. Orbix allows developers to create distributed, component-based applications that interoperate across a variety of operating systems. Orbix/Ada interoperates with all other versions of the Orbix product (including Orbix/C++), enabling cross-language and cross-platform integration. Orbix/Ada uses the Ada95 object-oriented programming language, which retains the integrity of the Ada83 standard while meeting the requirements of modern software-engineering platforms. The marriage of CORBA and Ada95 allows developers of mission-critical systems to produce distributed Ada applications that interoperate seamlessly with services and components implemented in other languages. Orbix currently runs on 20 different operating systems from a single code base. Platforms include Windows 3.1x, Windows NT, Windows 95, OS/2, Macintosh System 7.5, 12 different Unix systems, OpenVMS AXP, MVS, and significant real-time operating systems. Orbix for Windows allows OLE-enabled applications to transparently invoke remote and local CORBA objects. OrbixWeb is an implementation of the CORBA specification in the Java programming language to enable the creation of downloadable applets that can access multiple shared backend CORBA services located across intranets and the Internet.

IONA Technologies Inc., *201 Broadway, Floor 3, Cambridge, MA 02139; (617) 679-0900 or (800) 672-4948; e-mail tgolden@iona.com.*

CIRCLE 864

SOFTWARE TOOLS MANAGE SNMP NETS

Based on the PATROL SNMP Agent Development Kit from BMC Software Inc., the SNMP Master Agent network-management software and SNMP Development Toolkit from Lynx Real-Time Systems enables software engineers to develop sophisticated communications products by simplifying and accelerating the building of SNMP subagents and management information bases (MIBs). Users of the toolkit can reduce both time-to-market and development costs. Available with the latest release of PosixWorks, the two products result from a joint development agreement with PEER Networks, a division of BMC Software Inc. The PATROL SNMP Agent Development Kit is part of the PATROL suite of application and data management products from BMC Software. Using an open multi-MIB architecture, the technology is used by customers and third-party vendors to create a master agent and subagents to provide SNMP-based management support for applications and devices across a computing enterprise. The software comes free with version 2.4 of LynxOS Development Systems. It provides the communications pathway between the network manager and the embedded system's MIB. The toolkit provides a modular development environment, a high-level API., and doesn't require engineers to be well-versed in SNMP technology. Selling for $9900, the toolkit is available in a version of native LynxOS running on x86/Pentium platforms. Source code for both the SNMP Development Toolkit and the run-time master agent

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also is available. In addition to the SNMP Classic, Lynx's Master Agent software supports the emerging SNMPv2 standard. LynxOSv2 is available for x86/Pentium, PowerPC, Motorola 68000, and microSparcII platforms, with continued support for microprocessor memory management units.

Lynx Real-time Systems, *2239 Samaritan Dr., San Jose, CA 95124; Susan Wells, (408) 879-3900, ext. 124; Internet: http://www.lynx.com. BMC Software Inc., (713) 918-8800 or (800) 841-2031; Internet: http://www.2Ebmc.com.*

CIRCLE 865

SOFTWARE ENHANCES GRAPHING, ANALYSIS

Axum 5.0 technical graphics and data-analysis software from MathSoft Inc. comes with new features that help reveal hidden patterns in data. New enhancements and features include panel plots, the ability to customize Axum's toolbars and menus, and a link for automatically creating PowerPoint presentations. The graphing package allows users to condition data on multiple variables and examine different relationships in the data. With point-and-click graphing, users can create graphs instantly by selecting data from a built-in data sheet and clicking on one of over 80 2D- and 3D-plot buttons. Axum 5.0 has a seamless link with Microsoft's PowerPoint. With a click of a button, Axum's PowerPoint Wizard appears, the user specifies which Axum graphs are to be included, and the PowerPoint presentation is created. Axum also links seamlessly with MathCad technical calculation software from MathSoft. Axum 5.0 provides full 16- and 32-bit support, and is compliant with Windows 95 and Microsoft Office. Pricing is $395.95, and academic versions go for $195.95. Registered users can upgrade for $149.95. Axum 5.0 runs under Windows 95, Windows NT, and Windows 3.1x. Upgrades can be obtained from MathSoft by calling 1-800-MATHCAD.

MathSoft Inc., *101 Main St., Cambridge, MA 02142-1521; Ellen Koup, (617) 577-1017, ext. 741.*

CIRCLE 866

FLASH OS SUPPORTS CONSUMER PRODUCTS

A flash operating system for consumer electronics and embedded sys-

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tems the use of low-cost flash memory devices in any software-controlled electronic product as a read/write storage medium. Because FLite is based on the FTL standard and the DOS-FAT standard file system, it provides data compatibility with desktop and laptop computers. A primary application of FLite will be used with flash Miniature Cards and PC Cards in consumer products such as digital cameras and voice recorders. Other applications include digital cellular communicators, PDAs, communications systems, Internet terminals, and embedded computers. FLite brings FAT file system and FTL interoperability to non-DOS applications for transparent data interchange with PCs. FLite also may be used for internal onboard flash arrays to implement low-cost, nonvolatile data storage in applications having no file system and requiring read and write capability. FLite contains built-in MTDs for most leading flash devices, and provides a built-in interface to standard flash sockets. It can be customized down to a code size of only 14 kbytes, with a RAM requirement of less than 1.5 kbytes. Written in portable ANSI-C, FLite can be customized to any CPU, flash technology, and operating system, from 8-bit microcontrollers to RISC CPUs. FLite is available to OEMs as the FLite-OAK (OEM Adaption Kit) containing full source code, documentation, demonstration aids, and integration tools.

M-Systems Inc., *4655 Old Ironsides Dr., Suite 200, Santa Clara, CA 95054; (408) 654-5820; e-mail info@ccm.msyscal.com.*

CIRCLE 867

TOOLBOX ENHANCES PROCESSING SOFTWARE

ORINCON Technologies has added real-time image-analysis capabilities to the signal-processing functions of its RIPPEN real-time interactive programming and processing environment. Originally oriented toward signal and information processing applications, the new tools now enable RIPPEN to address image restoration, enhancement, and segmentation, in addition to feature extraction and pattern recognition. A set of data control tools support parallel processing and region-of-interest processing. RIPPEN runs on open architectures based on i860, C40, and C80 processors, and will be ported to architectures based on SHARC and PowerPC processors in the future. RIPPEN offers a click-on display to allow users to monitor in real time the processing results at each stage. For non-real-time applications, the IISD (Interactive Image Script Designer) has been added to allow developers to define image-understanding pipeline processing scripts for subsequent execution under RIPPEN. This action provides for interactive analysis of individual frames and comparison of the results on the screen. IISD allows users to move the bars on the histogram or frequency spectrum on the screen while viewing the processed image from a split-window display. IISD also provides a working area where original images can be dragged-and-dropped or put back on the stack. Also included are tools for converting different image formats among TIFF, GIF, JPEG, MPEG-1, and raw images. An IISD-RIPPEN script translator converts a script built under IISD with

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a set of tools and certain GUI parameters into a RIPPEN script with the same tools and parameters. The RIPPEN Image Processing Toolbox is available to existing RIPPEN users for $5000 for a single-user license. Runtime licenses are available at no charge.
***ORINCON Technologies Inc.**, 9363 Towne Center Dr., San Diego, CA 92121-3017; John Carbone, (619) 455-5025.*
CIRCLE 868

EXPERT SYSTEMS TOOL LINKS WITH C/C++

Fifty times faster than previous versions, CLIPS/R2 from Production Systems Technologies is the first version to use the proprietary Rete II rule engine. CLIPS/R2 is upward-compatible with CLIPS 6.04, and supports forward-chaining rules, backward-chaining rules, objects, and conventional procedures. Its backward-chaining-rule engine supports certainty factors, ANDs and ORs in rules, and HOW and WHY explanations. CLIPS/R2 rule bases can be embedded in C or C++ programs. The CLIPS Interface Definition Compiler enables the CLIPS/R2 rules to operate transparently on existing C structures and C++ classes. The system is available for Windows 3.1, Windows 95, Windows NT, and Unix systems.
***Production Systems Technologies Inc.**, 5001 Baum Blvd., Pittsburgh, PA 15213; Diana Connan, (412) 683-4000; e-mail dconnan@pst.com.*
CIRCLE 869

LIBRARY SPEEDS IMAGE DEVELOPMENT

Optimized for the Texas Instruments 'C80 digital signal processor, the 'C80 IP library from Precision Digital Images offers over 100 algorithms for implementing industrial machine-vision applications using PDI's Precision MX image-processing engine. The Precision MX integrates PDI image capture, 'C80 digital signal processing, and real-time VGA display into a single slot for the PCI bus. Combining the library tools and the processing power of the 'C80 (four parallel processors for two billion ops) enables users to accelerate the development process and focus on the end result of their software application. The library allows developers to write normal C/C++ programs and call functions from the library while avoiding the complexities of direct 'C80 coding. A complete list of functions and performance benchmarks is available on the company's web site at http://www.precisionimages.com.c80.htm.
***Precision Digital Images**, 8520 154th Ave. NE, Redmond, WA 98052; Mike Grady, (206) 882-0218.*
CIRCLE 870

GENERATOR PRODUCES MULTI-THREAD C++ CODE

BetterState PRO version 4.0 now generates both single- and multi-threaded C++ source code for Windows 95 and Windows NT applications. This advance enhances BetterState's capability to represent and realize various interpretations and implementations of concurrent activities within statecharts. Statecharts, or Harel diagrams, are the de facto standard for state-machine and reactive system design in markets such as SEMI (manufacturers of semiconductor manufacturing equipment), object-oriented programming and design, and EDA.
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One of the most powerful features of statecharts is the ability to visually capture concurrency and synchronization. Where earlier versions of BetterState realized concurrency using a single thread of computation, the new code generator uses the underlying Windows 95 or Windows NT operating system to realize a true preemptive, multi-threaded application. Under Windows NT, such code also can be used for a true multiprocessor system. BetterState is a PC-based design tool for statecharts with VisualBasic (V3 and V4), Delphi, C, C++, C++ for MFC, VHDL, Verilog, SpoxOS, and ParallelC code generation. BetterState PRO is priced between $625 and $995. A custom code generator is available for $1995. NetState, a tool for automatically generating CGI scripts for the Web from statecharts, costs $1995.

R-Active Concepts Inc., *20654 Gardenside Circle, Cupertino, CA 95014; Doron Drusinsky, (408) 252-2808; e-mail doron@ractive.com.*

CIRCLE 871

KIT ENHANCES CROSS-DEVELOPMENT TOOLS

The Back-End Developer's Kit from Wind River Systems adds new connection strategies to the company's Tornado cross-development environment. The kit enables background debug mode (BDM), in-circuit emulator (ICE), and other hardware vendors or customers to provide back-end Tornado integrations with minimal effort. The kit consists of a C++ class library with extensive documentation and examples to help hardware vendors create a back-end connection strategy in the form of a dynamically linked library. The framework for the back-end is an abstract base class that allows developers to reuse proven debugged code. Tornado provides an interactive cross-development environment comprised of coordinated tools that impose little or no overhead on target resources. This environment consists of the Tornado tool suite, the VxWorks scalable real-time operating system, and a full range of communications options such as Ethernet, serial line, ICE, or ROM emulator for the target connection to the host. Tornado also supports the use of third-party and custom tools. The Back-End Developer's Kit is available free of charge.

Wind River Systems Inc., *Alameda, Calif.; Stephanie Schwarz (510) 814-2573 or (800) 545-WIND; e-mail steph@wrs.com.*

CIRCLE 872

DEVELOPMENT TOOLS FOR MULTIPROCESSORS

The graphical multiprocessor development capabilities of BetterState by Co-Active Concepts, and the multitasking and multiprocessing facilities of 3L Parallel-C by 3L Ltd., have been combined to form BetterState for 3L Parallel-C to simplify the development of DSP applications. BetterState supports the entire software-development cycle, including graphical design, code generation, and visual verification. It also automates the design of signal-processing functions, which may be used standalone or incorporated within a main C program via function calls. BetterState projects are implemented as a collection of controllers defined at the behavioral level. Parallel C is a multiprocessing upgrade to the compiler tools from Texas Instruments for communication and synchronization. A

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real-time microkernel handles multitasking, timer queues, and interrupts. Configuration software allows developers to assign multiple software tasks to different processors throughout a network under programmer control. BetterState's code generator automatically produces C source code for each controller. It then is interpreted as Parallel C tasks and integrated, scheduled, and synchronized using all of the usual Parallel C facilities. Controller tasks may be implemented on a single- or multiple-processor environment using the Parallel C configuration utility. The BetterState code generator supports parallel processing and multiprocessing, automatically detects race conditions, and offers a choice of code styles (if-then-else or case). The Animated PlayBack facility visually shows state-transition sequences in the order they have occurred. Using VCR-like controls for stepping, running, stopping, and back/forward, programmers can navigate through the design and track the controller's actual behavior. BetterState costs $1495 for the Pro version and $795 for the Lite version.

Co-Active Concepts Ltd., *P.O. Box 633, Ofakim 80300, Israel; telephone: 972-7-961434,960641; fax: 972-7-926581; e-mail: coactive@netvision.net.il.*
CIRCLE 873

DEVELOPMENT TOOLS FOR MCS 251s

Embedded-system development tools created by Boston Systems Office/Tasking (BSO/Tasking) support the latest variants of the MCS 251 microcontroller family, including the 8xSP/SQ/SA/SB, Intel's 92930, and Temic/Mahtra MHS MCS 251 derivatives. Compatible with existing 8051 software, version 1.2 of the toolset exploits the capabilities of the second-generation MCS 251, including increased memory mixing and addressing (16- and 32-bit), and high-level language support. The startup code allows users to specify the chip configuration, and the locator description file supports the 256K external addressing of B-stepping. The toolset includes two C compilers, a macroassembler, and the CrossView ROM monitor debugger. It also contains the Embedded Development Environment, which lets users access all tools through a common Windows environment. The compiler package enables applications to run in source or binary code. Users can access special features of the MCS 251, such as extended bit memory, user in-line C functions, multiple address modes, special-function registers and interrupt functions, without violating the ANSI standard. The macroassembler has a linker, locator, librarian, and object format utilities for translating MCS 251 assembly language into relocatable object code. It also produces relocatable object code from Intel-compatible assembler source programs. BSO/Tasking's CrossView ROM monitor debugger environment can be used with any MCS 251 evaluation board running Intel's RISM. CrossView communicates with the monitor on the target board through an RS-232 interface. Support has been added to the toolset for access to MCS 251 emulators, evaluation boards, real-time kernels, device drivers, and fuzzy logic tools. Toolset pricing is $1895, with individual tools starting at $395. The toolset runs on DOS, Windows, Sun Sparc, HP9000, and Digital Alpha platforms.

Boston Systems Office/Tasking, *333 Elm St., Dedham, MA 02026; (617) 320-9400; e-mail: vaughn@tasking.nl.*
CIRCLE 874

Technology Begins

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Wireless Systems Design

Voice-Storage IC Has Novel Message Management

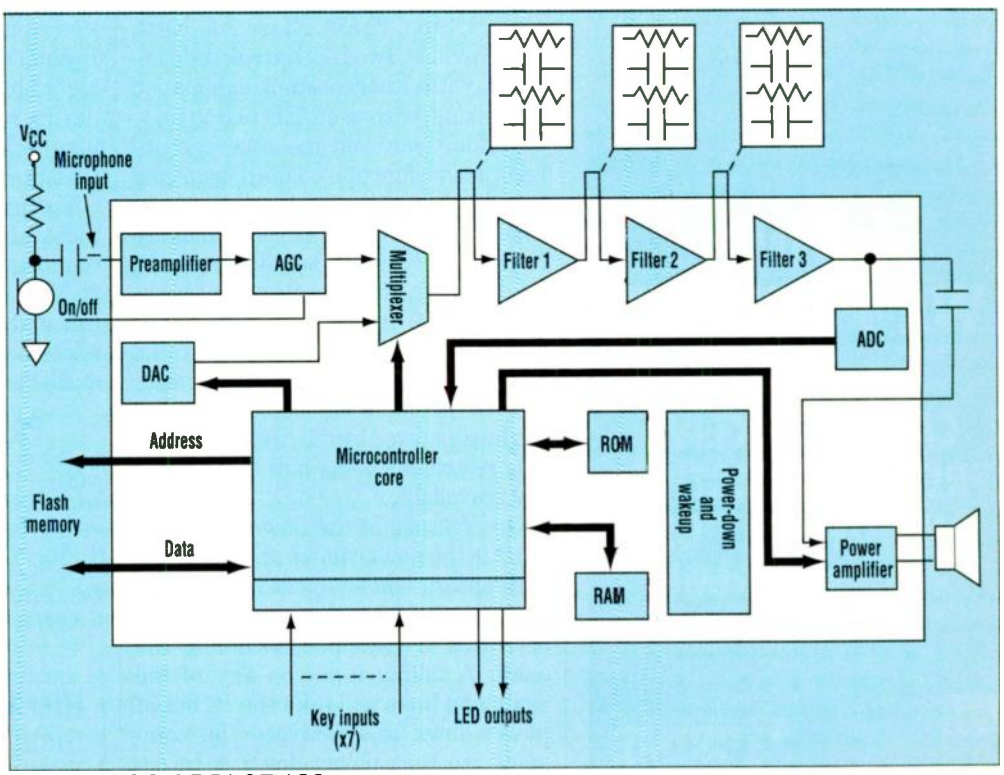
PAUL MCGOLDRICK

Target Applications For This Mixed-Signal CMOS IC Include Voice Recorders, Voice Organizers, Educational Toys, and Cellular Answering Machines.

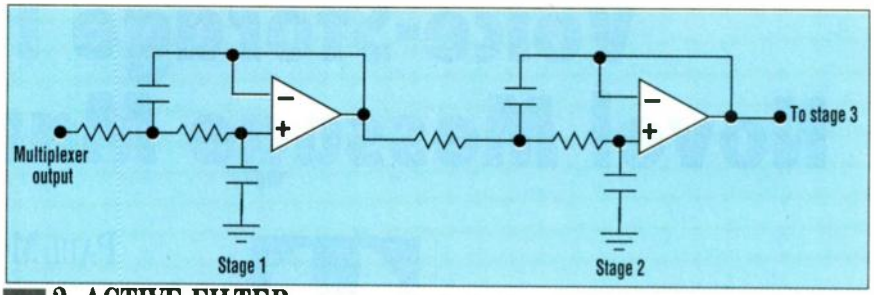
The TR83100 is a single-chip voice controller for storage applications. The IC is designed in 0.6-µm CMOS technology. It includes all the blocks required in the digitization, storage, and playback of voice signals, with a minimum of external components. An on-board compression/decompression engine uses a memory controller to allow voice data to be stored in parallel flash memory.

The device is designed to accept an electret microphone, ac-coupled into a preamplifier, with automatic gain control (AGC) of up to 20 dB. This set up allows for inputs from 30 to 200 mV *(Fig. 1)*. AGC also can be disabled with a 20-dB fixed gain in its place. The output feeds a 2-channel multiplexer which has a second input from the playback channel. The filter stages described below are used during both the record and playback processes. Intelligent power management shuts down the input circuits during playback and the output circuits during record.

The active parts of the filter are three unity-gain op amps forming a low-pass sixth-order filter. Its characteristics are controlled through external resistors and capacitors forming a Chebyschev, or Butterworth filter *(Fig. 2)*. (Fourth- or fifth-order filters also could be implemented.) The filter output is ac-coupled to the power amplifier on playback, and to a 10-bit linear analog-to-digital converter (ADC) on record. This coupling feeds the compression algorithm in the microcontroller core. The playback path starts with the decompression in



1. BLOCK DIAGRAM of the TriTech TR83100 voice-storage circuit. The TR83100, which has analog and digital functions on-chip for up to 6.5 minutes of storage, handles inputs of 30 to 200 mV.



2. ACTIVE FILTER components for the first two stages of the TR83100. The third stage is similar. The op amps are internal and the passive components external to the IC.

the core, with the output feeding an 8-bit digital-to-analog converter (DAC). It then moves into the multiplexer and filters. The power amplifier can be used to directly drive a low-cost, 32-Ω loudspeaker with 3 V available across it.

The key inputs into the microcontroller are simple ground closures. They provide a message-management system with "voice mail" features, offering random access and control of messages. Implementation is based on the concept of a message pointer that is used to address voice messages of varying lengths. Once a message has been addressed, it can be played or erased. A recorded message is always added at the end of the list.

Commands available include Play, Record, Stop, Erase, Erase All, Next, and Previous. Two LEDs track the commands with either constant illumination or blinking, with one LED tied to play-type functions, and the other tied to record-type functions. The de-bouncing time for most of the commands is 30 ms. The Erase and Erase All commands are held low for 0.5 seconds and 1.0 seconds, respectively. An optional buzzer tone at 1 kHz for 100 ms is available as a tactile feedback. If selected as a mode to be active, the tone is stored in flash memory. An unlimited number of messages can be supported by the circuit, with the only restriction being how much memory is available.

One feature of the power management is the power-down state that the chip enters whenever keys have not been pressed for three seconds. All activities are stopped, including the clock. A falling input on any of the command lines will take the IC out of power-down and activate the command, so that power-down is transparent to the user. Designed for a +5-V supply, the TR83100 consumes a maximum of 58 mA in playback and 33 mA in record (the difference being the consumption of the power amplifier). During power-down, current falls to a maximum of 10 μA.

Flash memory is used for data storage, allowing nonvolatility with the expectation that it is going to be more cost-effective than DRAM. Parallel flash memories from Amtel, Samsung, and SST are supported. The controller takes full responsibility for interfacing; it selects the read/write algorithm depending on the memory used. One or two devices can be supported. If there are two, they must be of the same type. Up to 6.5 minutes of storage is supported by 8 Mbits of memory in the High position where compression is at 20 kbits/s. A Low position compresses signals at 10 kbits/s. Both compression schemes are PCM algorithms. The compression used during recording is recognized during playback, automatically activating the appropriate decompression.

External components needed include those of the filters, microphone, and coupling capacitor. Also required are a 20-MHz crystal with a couple of capacitors and resistors, and the LEDs with series resistors. An evaluation board is available from TriTech. □

PRICE AND AVAILABILITY

Prices of the TR83100 from TriTech (a Singapore Technologies company) are from $6.00 each for sample quantities. Deliveries are available immediately. It is packaged in an 80-pin PQFP.

TriTech Microelectronics International Inc., 2290 N. First St., Suite 204, San Jose, CA 95131; (408) 894-1900; fax (408) 894-1919.

CIRCLE 502

HOW VALUABLE?	CIRCLE
HIGHLY	534
MODERATELY	535
SLIGHTLY	536

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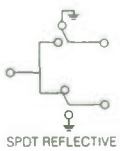
MSWA-2-20 (Absorptive)	DC-2.0	1.3	+27	40	3.45
MSWT-4-20 (Transfer)	DC-2.0	1.8 TX ② 2.0 RX ③	+28 TX ② +27 RX ③	30	3.95

① Midband, 500-1000MHz ② Transmit ③ Receive

All Units: SOIC 8pin Package

Actual Size



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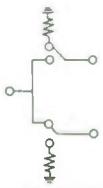
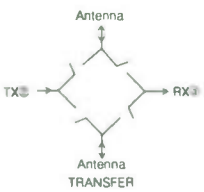


SPDT ABSORPTIVE



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F 74 Rev A

LDO Controller Handles 250-A/μs Load Transients

A Speedy Regulator-Controller And A Power MOSFET Eliminates The Tens Of Tantalum Capacitors Required By The V_{DD} Of Advanced Microprocessors.

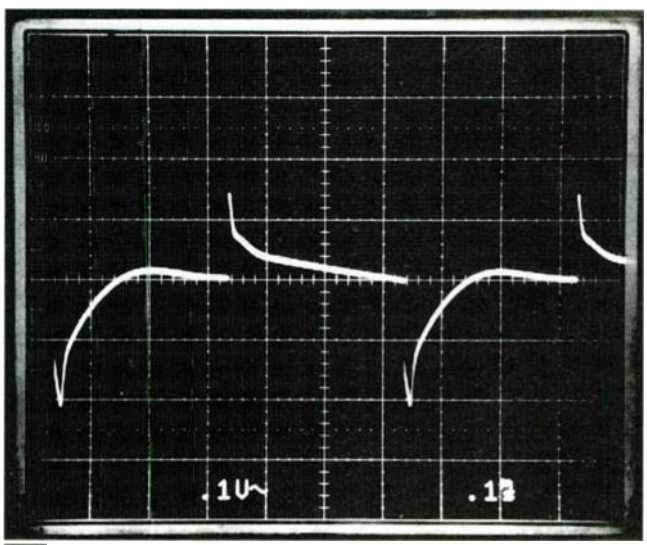
FRANK GOODENOUGH

The supply rail for many of today's microprocessors (such as the Pentium and the PowerPC) cannot vary more than ±100 mV while handling load transients (as the processor is power-managed by software) on the order of 5 A with 20-ns rise and fall times. In other words, the current slews at 250 A/μs. Some low-cost systems built with the latest processors have ignored this requirement. That's because meeting it requires a large bank of bulky, hard-to-get, expensive capacitors. And these supplies must be inexpensive.

Linear Technology has now come up with an ultra-fast LDO controller IC—the LT1575. This chip, along with a discrete n-channel power MOSFET, eliminates the need for most of those capacitors, cutting as much as $2 off the cost of a supply. The pc board that holds the LT1575, the FET, and the processor must be laid out correctly to handle these load-current transients. To simplify board layout, LTC makes available to customers an evaluation board and layout that handle the load transients.

Today, the lowest-cost power rail for these processors, in systems with a stiff (well-regulated) 5-V rail, consists of a high-current low-dropout (LDO) linear regulator built with a high-current discrete pnp pass transistor (usually a D45H8). This LDO is driven by a low-current general-purpose LDO regulator such as National Semiconductor's LM2951. Most general-purpose LDO regulators are built on relatively slow bipolar processes, with little design effort devoted to making them fast. And pnp transistors are not known for their blazing speed.

Due to the slow response of these low-cost regulators, the system designer must hang hundreds of microfarads of expensive, bulky, hard-to-get, low-ESR (equivalent-series-resistance) tantalum capacitors on their output (the supply rail) directly at the processor-chip's V_{DD} pins. In addition, several 1000-μF bulky aluminum electrolytics and at least two dozen 1-μF ceramic capacitors must be added to this expensive capacitor bank. Moreover, all of these additional capacitors (particularly the ceramics) must be located as close as possible to the V_{DD} pin of the processor, or the parasitic lead inductance between capacitor and pin will destroy their effectiveness.



1. MANY LOW-DROPOUT REGULATORS, such as this one from a typical motherboard for an advanced microprocessor, cannot hold their output within ±100 mV when subjected to a current load that continually swings back and forth between 5 A and 200 mA in just 20 ns.

Early versions of these processors were quite tolerant of systems unable to

handle such output load transients. But now, most new processors can't handle them. In fact, pc motherboards have been built that do not hold to the ±100-mV specification for a load swing from 200 mA to 5000 mA in 20 ns. On a real motherboard, the supply rail instantly dropped over 200 mV when a 5-A load was applied *(Fig. 1)*. About 200 µs later, when the load was cut back to 200 mA, the rail went 150 mV positive. In this instance, the supply couldn't handle the transients and the system (a low-cost PC clone) refused to work.

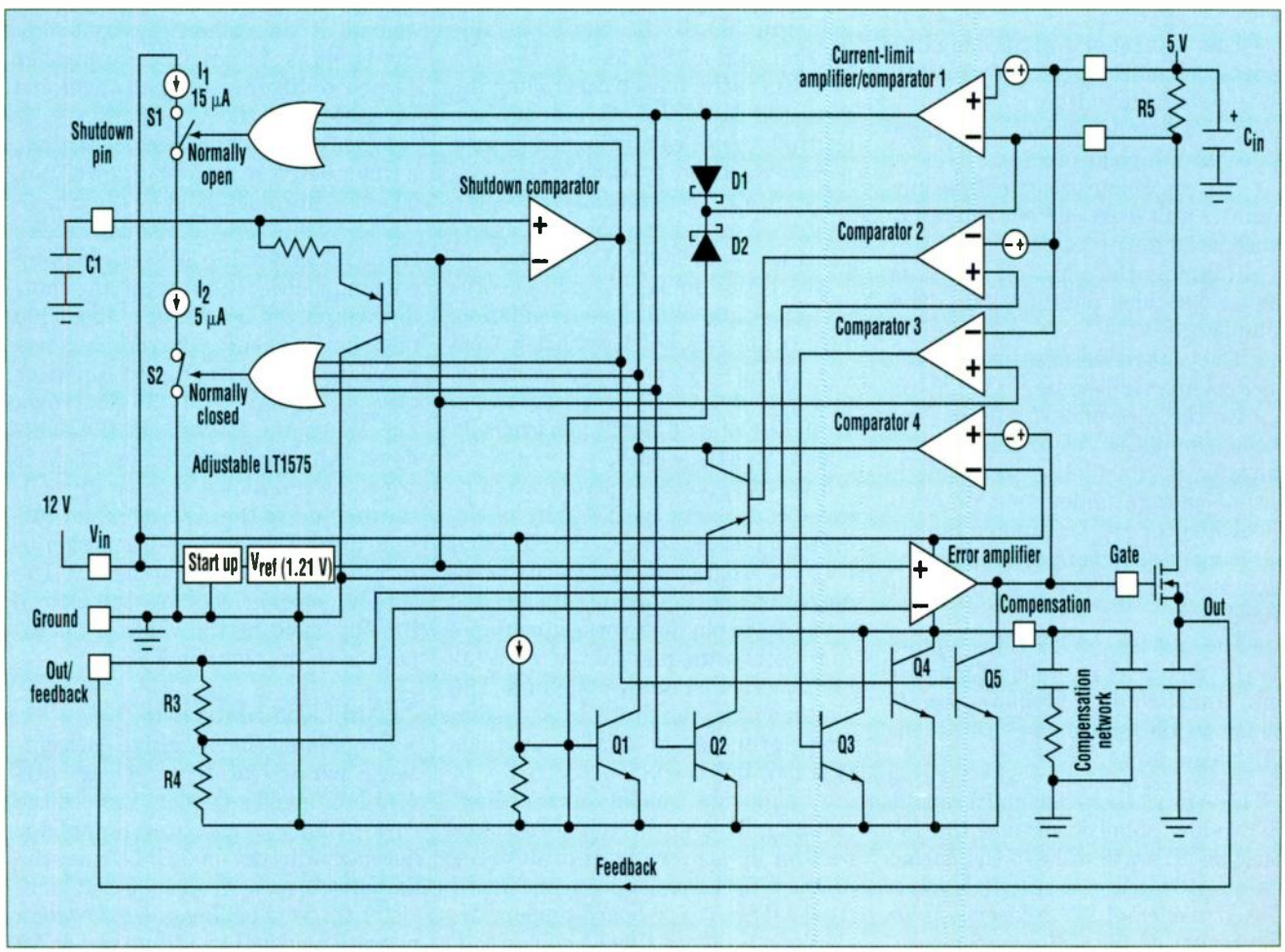
To combat this problem, designers at LTC came up with the LT1575, an ultra-high-speed LDO-regulator controller designed to drive an n-channel power MOSFET connected as a source follower *(Fig. 2)*. The circuitry in the controller and the MOSFET drive runs off a 12-V supply applied to the controller's V_{IN} pin, while the drain of the FET connects to the lower-voltage high-current rail (usually 5 V). An LT1575-based controller needs only the 24 1-µF ceramic capacitors to meet the transient-current load. Each tiny ceramic capacitor runs about 80 by 50 by 50 mils. Not only does it save board space, but the low-cost LT1575 does not require purchasing the bulk capacitance.

When an LT1575-based regulator replaces the bank of tantalum and aluminum electrolytics on a "real" motherboard, only tiny 50-mV spikes appear on the regulator's output *(Fig. 3)*.

The use of the MOSFET in lieu of a pnp transistor not only adds speed, but more importantly, the dropout voltage at any desired current becomes strictly a function of the chosen MOSFET. The lower the FET's on-resistance, the lower its dropout voltage. And many currently available discrete power MOSFETs have on-resistances of less than 10 mΩ.

According to available information, tantalum capacitors can explode under some fault conditions, creating a potential fire hazard. As a result, some motherboard users (system designers) now require that the tantalums be fused. But the fuses raise the capacitor's ESR, and it will take three times as many capacitors to do the job. And as noted earlier, the LDO regulator built with the LTC controller does not require any tantalum capacitors.

LTC's designers came up with two high-speed controllers. They are based on the single LT1575 and the dual LT1577. The LT1577 contains a pair of functionally-identical controllers. In a typical application, one controller sets its output at 3.3 V; the other sets its output at 2.8 V. These dual LT1577s are designed for what are known as "split-plane" systems in which the processor I/O logic runs off 3.3 V and its core runs off 2.8 V. In addition, there are six versions of the



2. THE LT1575 CONTROLLER and an n-channel power MOSFET form an LDO regulator. The regulator can successfully handle 5-A, 20-ns load-current transients without thousands of microfarads of capacitance hanging on the output.

LT1575 ranging from an adjustable-output controller to controllers with fixed outputs of 1.5, 2.8, 3.3, 3.5, and 5 V. The LT1577 can also be made available with a combination of output voltages other than 3.3 and 2.8 V.

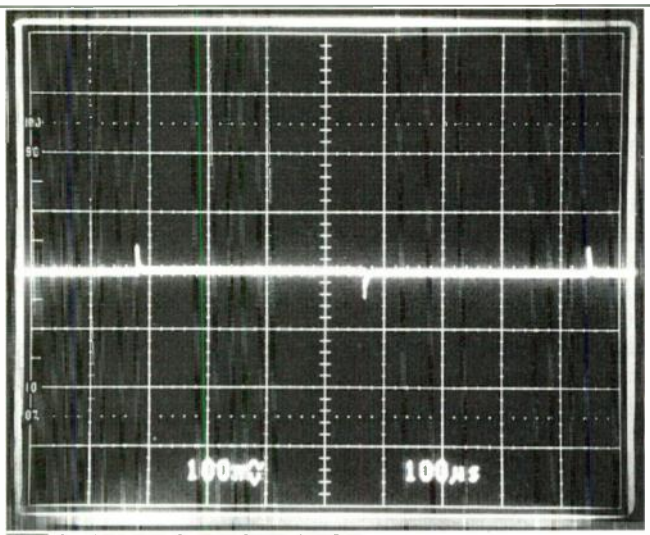
SPEEDY AND ACCURATE

The controller's compensated control loop typically sports a unity gain bandwidth, including the MOSFET, of approximately 1 MHz. That's several orders of magnitude faster than the bandwidth of most of the available high-current low-cost regulators used to power microprocessors.

To achieve such system speed (the complete regulator can be considered a system), LTC's designers employed the following techniques:

- The controller's error amplifier sports an uncompensated 75-MHz unity-gain bandwidth.
- The controller is built on a high-speed 22-V bipolar process.
- The controller uses plenty of current. Its quiescent current can run as much as 20 mA.
- Running the chip off 12 V or higher provides plentiful gate-drive compliance.
- The controller uses mostly fast vertical npn transistors.
- In the presence of large load steps, amplifier saturation would cause large time delays, resulting in output-voltage undershoot or overshoot. To prevent this problem, amplifier stages are clamped, preventing saturation and keeping amplifier speed high.
- The power MOSFETs, significantly faster than general-purpose pnp transistors, contribute significantly to the quick response of the LDO regulator.

These processors demand a rapidly responding supply rail, and the rail must be accurate to keep the output within ±100 mV of a specified value. The controller's 1.2-V reference holds accuracy to within ±1% over temperature. The error amplifier's open-loop gain ensures that the regulator's output voltage performs similarly (minimum large-signal open-loop voltage gain runs 69 dB for the adjustable version, and a little less for the others). Since the power controlling device (the MOSFET) is off-chip, the controller runs cool, minimizing temperature changes by what is already a very low-drift reference. That is, the chip's reference need not sport a temperature coefficient (TC) of zero.



3. AN LDO REGULATOR based on the LT1575 controller and a low on-resistance power MOSFET needs just 24 1-μF ceramic capacitors at a microprocessor's V_{DD} pin. The capacitors hold the output to these tiny 50-mV spikes when subjected to 5-A, 20-ns load-current transients.

The error-amplifier's gain ensures effective line and load regulation. That is, line regulation (with help from the MOSFET) runs a virtually unmeasurable 0.03%/V for a V_{in} between 10 and 20 V. Load regulation typically runs better than 1 mV.

Like most power-control ICs today, these controllers sport a suite of circuits that protect the IC, the FET, and the load from fault conditions during operation and at start-up. Included is a shutdown pin that works in conjunction with a unique pair of current-limit/thermal-shutdown circuits. The shutdown pin can protect the system from overvoltage and/or provides thermal shutdown.

A high-side sensing current-limit amplifier looks at the voltage across a resistor in series with the drain of the MOSFET. The resistor can be formed from a length of pc-board copper. The chip's data sheet explains how to construct such a resistor. This high-side current sensing does not affect the gain of the FET or the closed-loop gain of the basic feedback loop from the supply's output to the feedback pin.

When the voltage across the sense resistor exceeds 50 mV, the chip goes into action. First, the current-limit amplifier turns on transistor Q2, clamping the positive swing of the compensation node (at the "compensation" pin) to a voltage that calls for an output (load) current of 50 mV/R_{sense} (50 mV divided by the resistance of the sense resistor) *(Fig. 2, again)*. That is, the MOSFET's gate drive is reduced to a value that keeps the voltage across the sense resistor at 50 mV. Simply put, the regulator changes from a voltage source to a current source. It stays in that condition as long as the fault exists. However, after a certain amount of time, under the control of the supply's designer, the controller can be configured to shut down and turn off the FET.

When current limit becomes active, a timer starts at the "shutdown" pin. The pin, normally held low by the 5-μA active pull-down current source I_2, turns off and a 15-μA active pull-up current source, I_1, turns on (the shutdown pin's voltage limits at about 100 mV above ground). Current I_1 starts a linear ramp, charging the capacitor $C_{shutdown}$ hanging on the shutdown pin. When the voltage on the shutdown capacitor/pin reaches 1.2 V, it trips the shutdown comparator C1, shutting down the controller and cutting the FET's power dissipation to zero. The circuit then latches off. The supply designer controls the charge time by choosing the value of the capacitor on the shutdown pin.

SENSELESS LIMITING

Grounding the negative current-sense pin activates "senseless" current limiting. The action disables the current-limit comparator/amplifier because Schottky diode D1 clamps the amplifier's output, preventing transistor Q2 from pulling down the Compensation node. In addition, Schottky D2 turns off the normally-on pull-down transistor Q1. When it's on,

LOW-POWER DESIGN

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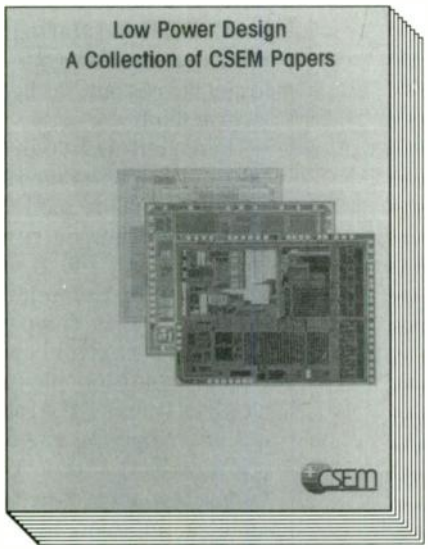

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transistor Q1 holds the output of comparator C4 low. With transistor Q1 off, comparator C4 monitors the IC's Gate pin that drives the FET's gate. Comparator 4 detects saturation at the positive rail and starts the previously described shutdown timer. When the circuit "times out," as before, the FET is turned off.

This "senseless" current limiting does not limit the current while the timer runs. This mode of operation can easily result in currents on the order of 50 to 100 A. On the other hand, keeping the timer period short limits the FET's temperature rise.

To restore normal operation after a fault condition has been cleared requires turning the input power off and on or driving the shutdown pin below 1.1 V (100-mV hysteresis) from a low-impedance current sink such as an open-collector gate or transistor. Unlike many similar circuits, the two supply voltages (as noted typically 12 and 5 V) may be applied to the circuit in any order. An undervoltage lockout circuit (comparator 3 and transistor Q3) ensures that the output remains off until the input rises to approximately 1.2 V. It also ensures that there will be no high current spikes when the low-voltage supply comes on after the high-voltage supply. In addition, the inherent speed of the regulator guarantees that little or no overshoot occurs at turn on.

Comparator C2 monitors the difference between the input and the output voltage and inhibits the shutdown timer starting if the difference is less than 500 mV. This feature permits a normal start-up when the regulator must charge the ceramic capacitors. Such a condition can exist when one is operating at, or close to, dropout.□

PRICE AND AVAILABILITY

The members of the LT1575 family come in 8-pin DIPs and SOICs. Those of the dual LT1577 family come in 16-pin SOICs. Pricing in quantities of 1000 begins at $2.40.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487, Jim Pflasterer, (408) 432-1900. **CIRCLE 501**

HOW VALUABLE?	CIRCLE
HIGHLY	531
MODERATELY	532
SLIGHTLY	533

PRODUCTS NEWSLETTER

Crypto-Button Dispenses Secure E-Mail Cash

A small but powerful cryptographic engine, housed in a 16-mm stainless-steel case (about the size of a hearing-aid battery), now makes secure transactions over the Internet or other public e-mail systems possible. The DS1954 Cryptographic iButton contains a fast microprocessor that includes 32 kbytes of ROM, 6 kbytes of RAM, a random number generator, and an arithmetic accelerator. Should malicious tampering of any sort be detected, the iButton is designed to ensure destruction of the chip's sensitive information. It's read by touching any portion of the iButton's case to an inexpensive Dot Receptor unit, which is attachable to most PCs' serial ports. The unit's ROM can be programmed to support various secure transaction schemes, including the highly regarded public/private key algorithm. Available in the first quarter of 1997, the simplest version of the iButton will cost as little as $1.59 each, in 1000-piece lots. The Dot Receptor reader will go for around $15. Contact Dallas Semiconductor, 4401 S. Beltwood Pkwy., Dallas, TX 95244-3292; (972) 371-4448, fax (972) 371-3715; e-mail: http://www.ibutton.com. *LG*

CIRCLE 565

Fast Ethernet Repeater Chip Supports RMON

Building manageable LAN equipment has become easier thanks to the BCM5012R, the industry's first Fast Ethernet hub controller chip to incorporate traffic statistics collection and other remote-monitoring (RMON) functionality. The repeater controller contains 13 ports and can support any Fast Ethernet PHY interface chip using 100Base-TX, -T4, or -FX connections. Besides its integrated RMON support, the BCM5012R also can communicate with SNMP-based (simple network management protocol) management systems, making it compatible with a most earlier LAN management technologies. Designed to work with the hub controller or in standalone NICs, the BCM5100 ($25 cost) is a single-chip 100Base-T4 transceiver optimized for 10/100 combo applications that supports PHY addressing in all modes. It can significantly cut the size and cost of hub designs. Pricing for the BCM5012R is $108. The BCM5010, priced at $72, offers all of the BCM5012R's features except RMON support. Broadcom Corp., 16251 Laguna Canyon Rd., Irvine, CA 92718; (714) 450-8700; fax (714) 450-8710. *LG*

CIRCLE 566

Shrinking ShBoom Chip Pushes Performance Marks

The next-generation ShBoom microprocessor promises improved performance thanks to a reduced core size. By employing an advanced IC manufacturing process, Patriot Scientific Corp., San Diego, Calif., was able to reduce to the core to 0.5 µm. Also known as the PSC-1005, the ShBoom will offer a nominal clock frequency of 90 to 100 MHz and processing power of 28 MIPS at 3.3 V. The greater speed coupled with lower power consumption will result in further drop in MIPS costs to the customer. Demands put forth by such diverse applications as Internet set-top boxes, network computers, printers, robotics, and so on can be met by the PSC-1005, according to Michael A. Carenzo, Patriot's president and CEO. He also anticipates the PSC-1005 to be available in the first quarter of 1997. For further information, call Paul K. Berlin at (619) 679-4428; or "sh-boom, sh-boom" onto their Web site at http://www.ptsc.com. *RE*

CIRCLE 567

Probe Provides Emulation Support For 80296SA

Emulation support for Intel's latest entry into its MCS 96 architecture, the 80296SA microcontroller, is offered by the DProbe296SA. The probe is the newest member of Kontron Elektronik's (Newport Beach, Calif.) DProbe family of personal debug tools. Attributes of the probe include support of the microcontroller's entire voltage range, and the ability to run up to its maximum clock frequency of 50 MHz with zero wait states. The controller's bus activities can be thoroughly monitored thanks to 64k samples of qualified trace. The probe meets European EMI requirements. A key feature in the overall probe family is a flexible construction principle called K-SET (Kontron Scaled Emulation Technology), which allows the company to provide emulation support for new processor and controller architectures at the time of their introduction. Contact Kontron at 1 (800) 566-8766; e-mail: dtsales@kontron.com; Internet: http://www.kontron.com. *RE*

CIRCLE 568

Edited by Roger Engelke

EUROPEAN PRODUCT NEWSLETTER

The products listed are available in Europe but may not be available in other market areas of the world.

Durable mini rotary switch

The miniature rotary switch 07R, which has a volume of about one cubic centimeter, comes equipped with a solid stainless-steel spindle. It isn't affected by rapidly changing environmental influences, such as temperature, humidity, and vibration. The stable solder tags in a 2.54-mm grid are tinned, while the contacts are plated with a 2-µm-thick gold layer. The 07R switch is built for a service life of 10,000 switching cycles and is available with a maximum of four switching positions in four basic versions: for horizontal and vertical fitting with steel-spindle or screwdriver operation. The switch in a thermoplastic package also is available with an optional watertight threaded bush. AV

Elma Electronic AG, *Hofstrasse 93, 8620 Wetzikon, Switzerland; telephone: +41 933/41 11; fax: +41 933/38 12.* **CIRCLE 630**

DSSS IC family

Typically, DSSS (direct sequence spread spectrum) systems are optimized for niche markets that require extremely high communications reliability, such as industrial networks for process control and monitoring. Following that lead, a modular family of DSSS ICs was developed for use in satellite communications systems and terrestrial communications networks. One of the chips, the Programmable Mobile Communications Modem (PMCM), is a digital transceiver that performs baseband and IF functions at low impedance losses. The chip , suited for 10 Mbits/s, supports code lengths of up to 1024 in VSAT communications systems. AV

Imec vzw, *Kapeldreef 75, 3001, Leuven, Belgium; telephone: +32 16/28 12 11; fax: +32 16/22 94 00.* **CIRCLE 631**

New facilities for REAL/32 OS

Planned for exhibition at this week's Comdex Fall in Las Vegas is the new version 7.6 of REAL/32, a real-time, multiuser, multitasking operating system. With this latest version, software developers will be able to deliver preemptive, real-time, multitasking applications in Windows and DOS environments thanks to the addition of remote Windows support, TCP/IP, LANtastic, and NetWare 4.1 connectivity. Remote Windows support allows users to execute Windows applications running on a REAL/32 host via a remote terminal connected over a modem or network link. This ensures that only keyboard and screen input commands are relayed over the remote link. The system targets numerous applications, such as process control, database application servers, and remote access/maintenance for LANs. RE

Intelligent Micro Software Ltd., *3 Archipelago Business Park, Lyon Way, Frimley, Surrey, England GU16 5ER; telephone: (011) 44 1276 686569; fax: (011) 44 1276 686510; e-mail: afreeman@imsltd.com; Web: http://www.imsltd.com.* **CIRCLE 632**

Analyzer tests ATM services, equipment

The DA-30C LAN/WAN internetwork analyzer tests the services carried and equipment used in ATM networks. Operating in real time at full line rate, the instrument not only monitors and troubleshoots ATM networks, but also analyzes any LAN traffic entering, leaving, or in transit on the ATM network. The DA-30C allows network service providers to perform complete port-to-port monitoring and testing of "any-to-any" networks operating with ATM service. For example, a single DA-30 can monitor and test Ethernet-to-ATM, FDDI-to-ATM, or HSSI-to-ATM configurations (the company claims that no other analyzer offers these joined capabilities). The OC-3/STM-1 ATM Analysis Package consists of hardware modules plugging into a DA-30C slot plus software programs that can be loaded into the DA-30C processor. AV

Wandel & Goltermann GmbH & Co., *P.O. Box 12 62, 72795 Enningen u.A., Germany; telephone: +4 7121/86 16 16; fax: +49 7121/86 13 33.* **CIRCLE 633**

Attach peripherals via PCMCIA slots

The PCMCIA Connection IC enables users to attach any popular interface peripheral, such as CD-ROMs, tapes, magnetooptical disks, removable media devices, printers, and scanners, to notebook computers and desktops via PCMCIA slots. Cards equipped with this IC will provide connection to EPP/ECP according to IEEE/1284, ATAPI, and SCSI interfaces. Transfer speeds of up to 2 Mbytes/s are possible depending on the host system's capability. Furthermore, the PCMCIA IC offers hot-swap capability, and it operates under DOS, Windows, and Windows 95. The manufacturer delivers either just the IC or a complete solution with the IC integrated in a PCMCIA Type II adapter card. AV

Shuttle Technology Ltd., *Alba House, The Mulberry Business Park, Wokingham, Berkshire RG41 2GY, England; telephone: +44 1734/77 04 41; fax: +44 1734/77 17 09.* **CIRCLE 634**

SOFTWARE

ANALYSIS TOOL PACKAGE VERIFIES SCHEDULING IN REAL-TIME SYSTEMS

PERTS 2.2, a suite of analysis tools to create static models of systems, can analyze and validate hard and soft real-time systems. Developed by Tri-Pacific Consulting, Alameda, Calif., PERTS 2.2 (for prototyping environment for real-time systems) lets system designers test software models against various design scenarios and see how different implementations can affect performance.

One of the major analysis tools is rate monotonic analysis (RMA). RMA is a collection of quantitative methods and algorithms that lets engineers analyze and predict the timing behavior of real-time software systems. RMA then can be used to set up rate monotonic scheduling (RMS) algorithms. The PERTS 2.2 tool hides the mathematical algorithms behind a graphical user interface that lets the designer analyze the system in terms of tasks and resources.

A task is characterized by the time in which it must be completed and the amount of work—processing—it requires. Tasks also are characterized by the resources they require, such as CPU, memory, I/O, etc., and by the interconnectivity parameters that indicate dependencies among tasks.

Resources are characterized by usage and timing parameters. Usage indicates reusability, preemptability, and number of units. Timing parameters include processing rate, acquisition time, and deacquisition time. Resources are grouped as units that contain CPU, memory, bus, and so forth. The schedulability analyzer then tells you which tasks can and can't be scheduled and makes suggestions as to what you can do about it.

RMS concerns itself only with tasks and scheduling them according to their timing characteristics. There may be very high priorities that must preempt other tasks, even if it means those tasks won't meet their deadlines. That's an issue for modeling. Analysis can aid in modeling by clarifying what the consequences of such preemption may be and/or suggesting how it may be accomplished without seriously compromising the system.

In addition to RMA, PERTS 2.2 also offers earliest-deadline-first (EDF) analysis. EDF provides a way to ensure that tasks with impending deadlines have first priority in the design sequence. This provides a more dynamic way to see if the design as a whole will execute in a timely manner. Another method, cyclic executive analysis, lets designers simulate using round-robin scheduling paradigms. This represents a more traditional technique for systems whose tasks run in harmonic intervals.

Using the various techniques, the schedulability analyzer will show results and suggest how ensure schedulability. In some cases it may indicate a simple solution such as simply increasing the speed of the CPU by some increment. In other cases, difficult contention problems may indicate a need to repartition the system. Nonetheless, the ability to identify scheduling problems early avoids having to go back and rework the architecture when a schedulability problem shows up after the system has been built.

To analyze a design in progress, PERTS 2.2 can be used along with requirements analysis and CASE tools to capture the timing and resource requirements. Tasks can be grouped or partitioned based on scheduling requirements revealed in early stages of analysis.

PERTS 2.2 can be used to analyze and validate a design in progress, or analyze an existing system. Analyzing an existing system requires capturing run-time data from a task visualization tool, such as Wind River Systems' WindView or eSP from Integrated Systems. Such tools analyze and visually display system behavior in terms of the system calls, flags, interrupts and semaphores. PERTS 2.2 takes the log data and defines a system from which it can make a static model. That model then is run through the schedulability analyzer in order to determine worst-case scheduling characteristics.

PERTS 2.2 runs on popular Unix platforms, including SunSPARC and UltraSPARC, HP-9000 Series 700, and IBM R6000. The tool suite is priced at $4500 to $5000 per seat in a multi-node installation.

Tri-Pacific Consulting, *1070 Marina Village Pkwy., Suite 202, Alameda, CA 94501; (510) 814-1770.*

CIRCLE 690

■ TOM WILLIAMS

DEVELOPMENT KIT ADDRESSES EMBEDDED APPS

The VRTX x86/spm application development kit is a cost-effective solution for developing protected-mode embedded x86 applications using a segmented memory model. The protected mode is typically used for more complex applications such as office equipment, telecommunications equipment, industrial control, medical electronics, transportation equipment, and handheld devices. Developers can select from flat (fpm) or segmented (spm) memory models. The flat model presents a 32-bit memory space for ease of use, and the segmented model offers hardware-based multitasking support, virtual memory, and the ability to detect and correct software errors on-the-fly. The segmented model is useful for building mission-critical applications such as in avionics and life-support systems. Using VRTX x86/spm, applications developed in C can be transferred from the real to the protected mode. The kit provides an embedded multitasking operating system along with a set of compatible PC-hosted development tools, C compiler, macroassembler, linker/locator, and object module librarian. Also included is the XRAY x86 Debugger for Windows, which provides an overview of system status, task states, and system object usage. In addition, it allows VRTX/OS functions to be called interactively from XRAY Debugger. Users can step through and view source code, monitor variables and expressions, trace function calls, and set breakpoints. VRTX x86/spm supports cross development on IBM-compatible PCs. Support packages are included for the Intel 80386EX and National Semiconductor NS486SXF evaluation boards. Overall, pricing for the VRTX x86/spm starts at $3495. ML

Microtec, *2350 Mission College Blvd., Santa Clara, CA 95054; (408) 980-1300 or (800) 950-5554.* CIRCLE 691

INSTRUMENTS

HIGH-ACCURACY DATA-ACQUISITION UNITS WORK WITH MAC OR PC NETWORKS

The instruNet family of data-acquisition products offers accuracies down to the tens of microvolts. The system houses the analog electronics in an electrically quiet box outside the host computer. The box's output consists of digital signals connected to a controller board in the host. This topology allows multiple data-acquisition devices to be daisy-chained together in networks hundreds of feet long.

The external network devices contain signal-conditioning amplifiers for each channel, so sensors can be connected directly to the unit. The controller boards include a 32-bit microprocessor with 256 kbytes of RAM that manages the external network devices. This processor handles all real-time tasks, relieving the host computer of this burden. Digitizing can be triggered off any channel. The aggregate sample rate is 166 ksamples/s, with each channel able to digitize at its own rate. Also, users can set up each channel in software to be filtered independently with low-pass, high-pass, band-stop, or bandpass filters.

Currently available is the instruNet 100 network device, which has 16 single-ended (eight differential), 14-bit analog inputs with ranges of ±5-, ±0.6-, ±0.08-, and ±0.01-V ranges. It features eight ±5-V analog outputs, and eight digital I/O channels. The device is available with 44 screw terminals or with 16 BNC connectors for the analog inputs.

Controllers are available for x86-based PCI and ISA-bus computers running Windows 95 and for Nubus and PCI Macintosh computers running system 7.0 or higher. The controllers include 10 counter-timer channels that can function as digital input bits, output bits, or clock input channels, or make period measurements.

All systems come with the instruNet World application program, which manages, monitors, and operates the instruNet network. The software also digitizes long continuous waveforms, spools them to disk, views incoming waveforms in real time, and then allows post-acquisition viewing. It includes a spreadsheet-like environment and drivers that are callable from any 32-bit C compiler.

The instruNet controllers each cost $590. Macintosh units are available now; PC versions are scheduled for December 1. The iNet-100 network device costs $790. The BNC version (iNet-100B) goes for $950.

***GW Instruments Inc.**, 35 Medford St., Somerville, MA 02143-4237; (617) 625-4096; fax (617) 625-1322; http://www.gwinst.com.* CIRCLE 692

■ JOHN NOVELLINO

TEST RECEIVER SIMPLIFIES EMI PRE-CERTIFICATION

The ESPC is a compact, lightweight test receiver for pre- and post-certification measurement of electromagnetic interference (EMI). The instrument's built-in firmware and Windows-based software for AT-compatible PCs allow non-EMI specialists to qualify their equipment with simple measurements. The software automates commercial EMI testing and generates graphs and printouts of peak, quasi-peak, and average data values. Standard coverage is from 150 kHz to 1 GHz. Optional extensions cover down to 9 kHz and up to 2.5 GHz. A wide range of preselection filters are automatically coupled to the frequency to which the receiver is tuned. Overload detectors at all receiver stages set the correct attenuation to ensure maximum valid dynamic range. The ESPC differs from full-compliance receivers in that it has a lower 1-dB compression point and sensitivity. But it offers a better noise figure and signal overload capability than most spectrum-analyzer-based solutions. The unit is made by Rohde & Schwarz, Munich, Germany, and sold in North America by Tektronix Inc. The ESPC costs $28,950, with delivery in six weeks. JN

***Tektronix Inc.**, Measurement Business Div., P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200, code 478; http://www.tek.com/Measurement.* CIRCLE 693

HANDHELD OTDR LOCATES FAULTS IN COMM NETWORKS

The Lynx is a handheld optical time-domain reflectometer that measures loss and locates faults in single-mode optical fiber communications networks to an accuracy of 1 m at distances up to 80 km. Versions are available for either 1310 nm, 1550 nm, or

both wavelengths. The unit measures location, loss, and reflectance of every splice on the network and displays results on a backlit 320-by-240-pixel LCD screen. Dynamic range is 22 dB at 1310 nm and 20 dB at 1550 nm, and loss resolution is 0.1 dB. Users can obtain a link budget with one button push. More complex analysis also is possible, including a display of the reflectometer curve, and zooming of up to 30 m and 0.25 dB per division. Measurement time ranges from 30 seconds to 10 minutes, depending on the complexity of the test, and the Lynx stores 25 sets of measurements in nonvolatile memory. An RS-232C interface is standard. The instrument measures 8 by 6.5 by 2.5 in. and weighs 2.2 lbs. It runs up to 6 hr. on its removable NiCd battery pack, which recharges in 1 hr. Prices start at $8400. Delivery is in 30 days. JN

***Boonton Electronics Corp.**, 25 Eastmans Rd., P.O. Box 465, Parsippany, NJ 07054-0465; (201) 386-9696; fax (201) 386-9191; e-mail: boonton@boonton.com.* CIRCLE 694

INSTRUMENTS

TOOL EMBEDS BIST STRUCTURES FOR TEST OF EXTERNAL MEMORIES

As the first product in the sysBIST family of embeddable built-in self-test (BIST) tools for board- and system-level testing, memBIST-XT addresses the difficult problem of testing external memories. The sysBIST family, which is based on the company's ICBIST products for ICs, extends BIST to pc boards, multichip modules, and systems.

As a front-end solution, memBIST-XT employs the appropriate information about the target memory cluster, the BIST configuration, and tool controls. It then supplies the BIST controller and controller interface-logic design objects as either synthesizable register-transfer-level Verilog or VHDL descriptions. It also supplies a test bench (in Verilog or VHDL) to verify the functionality of BIST structures in simulation, and synthesis scripts targeting a single ASIC or FPGA. The tool supports any type of read/write memory: SRAM, DRAM, or SDRAM.

The controller, which uses about 1000 gates, can reside on either an ASIC or FPGA that's interfaced with the target memory. Because it runs at system speed, the controller can test the memory at-speed, which isn't possible with external test methods.

Besides allowing at-speed testing, embedding the test function directly in the silicon cuts memory test time by up to two orders of magnitude, reduces the need for expensive manufacturing test equipment, and lowers the labor cost involved in testing. The company states that a comprehensive memory test of a workstation with 400

Mbytes of memory takes only a few seconds if memBIST-XT is used in the design, compared to about 20 minutes with external testing.

The memBIST tool is licensed on a per-design basis, with fees starting at $20,000 per design for the first three designs. It will be available in the first quarter of 1997 on Hewlett-Packard and Sun SPARC standard platforms.

LogicVision Inc., *101 Metro Dr., Third Floor, San Jose, CA 95110; (408) 453-0146; fax (408) 453-0150; info@lvision.com; http://www.lvision.com.*

CIRCLE 695

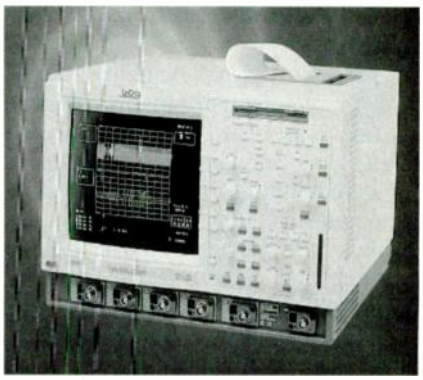
■ JOHN NOVELLINO

DSOS OFFER INNOVATIVE DISPLAYS, LONG MEMORIES, ADVANCED MATH

The LC334 and LC534 families of digital storage oscilloscopes offer a series of features aimed at making it easier for engineers to troubleshoot circuit problems. The four-channel scopes use a 9-in. color CRT display with special functions, a record length of up to 8 Mbytes on one channel, and a set of advanced diagnostic, troubleshooting, and documentation tools.

The three LC334 models have a 500-MHz bandwidth and the three LC534 scopes have a 1-GHz bandwidth. All of the units digitize at 500 Msamples/s on each channel. Within each series, memories of 100 kbytes, 500 kbytes, and 2 Mbytes per channel are available. The sampling capability and acquisition memories of unused channels can be combined to deliver up to 2 Gsamples/s and 8 Mbytes of memory in one-channel operation. In order to handle the very long arrays of acquired data quickly and maintain a fast front-panel response, the scopes incorporate a 96-MHz PowerPC microprocessor, a memory-management system, and up to 64 Mbytes of processing RAM.

The color display offers the traditional color-graded persistence mode and a new "analog persistence" mode. When the user is examining multiple signals, the screen colors can be made "transparent" so



that the shape of each signal can be seen even when they overlay each other. Also, a full-screen mode allows users to view a signal using the entire screenarea.

The scopes comes with an advanced math package that includes integration, differentiation, square root, absolute value, exponential, and log functions, as well as six selectable digital filters. Math functions can be daisy-chained into a series. The FFT package resolves up to 4 million time-domain samples into the frequency domain. Other features include measurement of over 40 signal parameters with worst-case analysis (maximum, minimum, average, and standard deviation). A pass-fail package tests each channel against separate masks and combines mask testing with go/no-go testing of key signal parameters. For fast identification, the display highlights failed points in a waveform using a bright color.

Besides internal memory, standard documentation tools include a floppy-disk drive and IEEE-488 and RS-232 interfaces. Among the options are a PCMCIA 170-Mbyte portable hard drive, a PCMCIA 512-kbyte memory card, and an internal high-speed graphics printer.

Prices range from $16,490 for the LC334 (500 MHz, 400 kbytes total memory) to $30,490 for the LC534L (1 GHz, 8 Mbytes total memory). Delivery is in four weeks for the LC534 series and eight weeks for the LC334 models.

LeCroy Corp., *700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977; (914) 425-2000.*

CIRCLE 696

■ JOHN NOVELLINO

REFERENCE-DESIGN KIT DESIGNED TO SIMPLIFY VIDEOCONFERENCING

The VideoFlow chip set and a companion support chip form the heart of a reference design that implements a complete video-communications subsystem. The reference design provides video e-mail, and performs CD-ROM recording and video storage playback, desktop videoconferencing over ISDN or standard telephone lines, and video capture and editing. The bill of materials cost is about $200—a fraction of the cost of systems with comparable functionality. Developed by Array Microsystems, the VideoFlow chip set and the personal-video-communications (PVC) reference board provide a flexible, predesigned solution for OEMs needing quick time-to-market as well as a solution that adds value to the system.

The chip set consists of the a77100 image-compression coprocessor and the a77300 motion-estimation coprocessor, which together perform most of the image-processing operations. The third chip, the a77200, contains logic that performs the timing and image resizing operations, and helps reduce the task of designing all of the support functions. The high throughput of the data-flow architecture in the VideoFlow chip set—over 1 billion operations/s—allows the circuitry to perform real-time MPEG-1 encoding and decoding at data rated from 100 kbits/s up to 2.4 Mbits/s. Furthermore, both I-frame and motion JPEG capture can be done at up to SIF resolution, and JPEG capture done at up to CCIR-601 resolution.

On top of that, the chip set supports H.261/H.263 protocols for standards-based videoconferencing, as well as the H.320 and H.324 protocols for ISDN and POTS (plain-old telephone system) videoconferencing. Consequently, the PCI-based reference board performs videoconferencing with either full CIF or QCIF picture sizes at up to 30 frames/s, with variable frame rates matching the network used. This capability, which is fully H.320-compliant, will incorporate selectable G.711, G.722, or G.728 audio coding.

Also included in the PVC reference design is the ability to handle H.324 POTS-based videoconferencing at image rates of from 7 to 10 frames/s (QCIF image size) and G.723 audio using standard 28.8-kbit/s modems. In the videoconferencing mode, document-sharing programs can be used, and both point-to-point and continuous-presence multipoint conferencing are possible.

For CD-ROM recording, video storage, and video playback, the design can handle real-time (30 frames/s) MPEG-1 IBP encoding at SIF and QSIF resolutions—with a variable bit rate (up to 2.4 Mbits/s). By using this capability, VideoCD white-book-compliant CD-ROMs can be created, or pre-recorded CD-ROMs from any source can be played back. Furthermore, existing video-editing tools may be used to create "professional-looking" video materials for applications such as training, home entertainment, corporate communications, etc. Data rates of up to 30 frames/s using motion JPEG are achievable.

Supporting the reference design is a full applications programming interface (API) for the Microsoft Windows 95 operating system, sample applications (such as the videoconferencing program), and full circuit-board schematics and design information. There are three levels of support products: a hardware evaluation kit (the a77650KT) that contains the PCI-based circuit board with executable software for demonstration and test; the a77652KT basic reference design kit that adds design documentation, reference-board schematics, API software source code, and sample applications; and the a77655KT, which adds the videoconferencing user interface to the previous kit. The full design kit sells for about $10,000; the other kits are available for considerably less.

Array Microsystems Inc., *987 University Ave., Ste. 6, Los Gatos, CA 95030; James Bohac, (408) 399-1505.*

CIRCLE 697

■ DAVE BURSKY

CPLDs DELIVER TOP I/O COUNTS

With pin-to-pin logic delays of just 10 ns and operating frequencies of 100 MHz, the super I/O members of Lattice Semiconductor's ispLSI 3000 family provide the shortest delays for complex programmable logic devices that pack up to 256 I/O lines. The 12,000-gate ispLSI 3256E and the 9000-gate ispLSI 3192 provide 256 and 192 I/O lines, respectively, which makes them some of the fastest, high-I/O-count CPLDs currently available. Furthermore, the ispLSI 3256E crams in double the I/O pin count of the original 3256 and is the only CPLD that can handle four 64-bit bus interfaces.

As with all other ispLSI family members, the 3256E and 3192 include dedicated boundary-scan test logic to enhance system-level testability, and can be programmed in the system with a 5-V supply through the on-chip IEEE 1149.1 standard boundary-scan-test access port. Using this scheme, Lattice created a programming time chain that depends only on the largest device in the chain to set the programming time. Thus, the CPLDs can be programmed at over 10,000 gates/s, thanks to a technique it calls ISP Turbo Download.

The high-I/O-count CPLDs are needed due to the proliferation of 32- and even 64-bit buses. And to meet those needs, Lattice claims to be the first supplier to provide high-density super-I/O CPLDs without sacrificing performance. Both chips use the company's ispLSI 3000 architecture, which features a set of programmable twin generic logic blocks.

The ispLSI 3256E, which comes in 70- and 100-MHz speed grades and is housed in a 304-lead metal quad flat package, sells for $165 and $199 each, respectively. The ispLSI 3192 also comes in both speed grades but is housed in a 240-lead MQFP. In 1000-unit lots, it sells for $104.50 and $159.50 each, respectively.

Lattice Semiconductor Corp., *5555 N.E. Moore Ct., Hillsboro, OR 97124; Steve Stark, (503) 681-0118; Web address: http://www.lattice-semi.com.*

CIRCLE 698

■ DAVE BURSKY

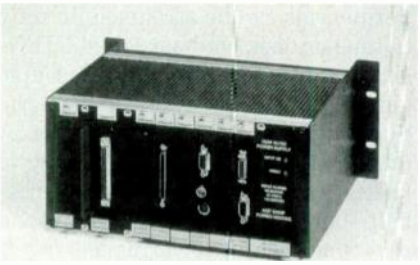
COMPUTER BOARDS

COMPACT PCI RACK, CPU BOARD SUIT RUGGED APPS

The ZT 6200 Eurorack card enclosure contains eight Compact PCI slots and a 150-W removable power-supply module. The card cage is designed for rugged environments, where shock and vibration, high temperatures, and electrical noise exist. One of the slots is dedicated to the CPU card, such as the ZT 6500 Pentium-based board. The remaining slots can hold various Compact PCI peripherals boards. Up to six masters can be used within the backplane, including the system CPU.

The ZT6200 supports 32- or 64-bit PCI transfers at rates up to 33 MHz. Maximum burst transfer rates are 128 Mbytes/s for 32-bit transfers and 256 Mbytes/s for 64-bit transfers. A wide variety of power-supply modules are available.

Designed in a 3U Compact PCI form factor, the ZT 6500 CPU board is fully PC software-compatible, running such operating systems as Windows 95, Windows NT, OS/2, and QNX. The



Card is available with CPUs ranging from 75 to 200 MHz. Up to 48 Mbytes of DRAM and 4 Mbytes of flash fit on the card. The flash memory can be used as a solid-state disk for embedded applications. A 256-kbyte cache module is available. Other features of the ZT 6500 include 24 points of digital I/O (in three 8-bit ports), a parallel port and two serial ports, a keyboard controller, a real-time clock, and a watchdog timer.

Ziatech Corp., *1050 Southwood Dr., San Luis Obispo, CA 93401; (805) 541-0488.*
CIRCLE 699

■ RICHARD NASS

CREDIT-CARD-SIZED MODULES FEATURE HIGH-END 486S

The comPCard series of credit-card-size PCs has grown with two new members, the 486-50 and the 486-100. The 486-100 employs an Intel 486DX4 microprocessor, operating at 100 MHz. The 486-50 also runs with an Intel processor, but at 50 MHz. Both modules are fully functional IBM PC/AT motherboards that measure about 3.4 by 2.2 in. The dual comPCards offer a shock resistance of 100 g and a vibration resistance of up to 15 g. The cards support all of the functions of a PC/AT motherboard through a 236-pin connector. This includes interfaces for the ISA bus; IDE, floppy-disk drive, serial, parallel, keyboard, and mouse ports; CRT or LCD; and infrared connectivity. Power-management modes also are incorporated. From 1 to 16 Mbytes of DRAM is supported. Because the comPCards support PCMCIA-ATA boot functions, a PCMCIA-based hard-disk card can be employed to reduce overall system size. In addition, a 3.3-V supply leads to an overall power consumption of about 1.5 W. The suspend-resume function reduces the power draw to about 60 mW. RN

Okidata, *532 Fellowship Rd., Mount Laurel, NJ 08054; (609) 235-2600.* CIRCLE 700

SPARC CPU-20VT FOR SCALABLE SOLUTIONS

The sparcSTATION 20 compatible CPU-20VT has two Mbus slots for up to four 150-MHz hyperSPARC processors. It comes equipped with dual SCSI and dual Ethernet interfaces, providing superior scalability for a wide range of performance applications. The CPU-20VT features field-upgradable ECC mezzanine memory. These modules are available in 64- or 128-Mbyte versions for up to 512 Mbytes of on-board DRAM. In addition, the board also offers two Sbus slots for graphics and flexible I/O expansion. Dual, independent SCSI-2 and Ethernet channels provide data protection from drive and network failures. The dual SCSI-2 interfaces allow for independent connection to storage devices. Automatic fail-over and recovery configurations can be realized using standard software. Pricing starts at $19,995 per unit. CM

Force Computers, *2001 Logic Dr., San Jose, CA 95124; (408) 369-6000.*
CIRCLE 701

HALF-SIZE SBC HOLDS 200-MHZ PENTIUM

In a half-size SBC format, the VIPer820 supports an Intel Pentium microprocessor running at speeds up to 200 MHz. Aimed at industrial applications, the board offers such features as 256 Mbytes of DRAM, 4 Mbytes of flash memory, a fast SCSI 2 interface, and PCI-based video operates works with a flat-panel display or a CRT. The boot-block BIOS is stored in the board's flash memory so that data is protected in the event of a power failure. A PC/104 connector lets users customize the board with modules designed by third parties. Most popular I/O interfaces are available. The VIPer820 contains serial, parallel, keyboard, and mouse ports. With a 75-MHz processor, 256 kbytes of synchronous cache memory, and 1 Mbyte of video DRAM, the board is priced at $1559. RN

Teknor Industrial Computers Inc., *7900 Glades Rd., Boca Raton, FL 33434; (407) 883-6191.* CIRCLE 702

PCI RAID CONTROLLER SUPPORTS ULTRA SCSI

An Intel I960 32-bit RISC microprocessor forms the brains of the DAC960PD-Ultra, a disk-array controller built to the Ultra SCSI specification. The board supports disk arrays for RAID levels 0, 1, 5, 0+1, and 5+0. The three-channel controller works with PCI-based systems, allowing data-transfer rates across the PCI bus at rates up to 132 bytes/s. The controller supports Fast-20 data transfers of 40 Mbytes/s on each channel. Up to 45 drives can be connected in total, 15 on each channel. In addition, up to eight controllers can be employed in one host system. With the board, the disk drives appear as one logical device to the operating system.

Support is included for NetWare, Unix, Windows NT, and OS/2. Single- and dual-channel products also are available. Prices for the DAC960PD-Ultra range from $1350 to $1775, depending on channel configuration. RN

Mylex Corp., *34551 Ardenwood Blvd., Fremont, CA 94555; (510) 796-6100.* CIRCLE 703

COMPUTER BOARDS

MIX MODULE SENDS HIGH-SPEED DATA TO SCSI SUBSYSTEMS

A high-performance fast and wide SCSI-2 interface adapter supports high-speed data transfers between VMEbus-based DSP and data-acquisition components and SCSI devices. Complying with the Intel MIX mezzanine standard, the Model 4260 features two TI TMS320C40 comm port interfaces, high-speed SRAM and FIFO buffers, a fourth-generation SCSI controller, and a front-panel serial interface. The MIX interface is a stacking daughtercard system that supports 40-Mbyte/s data transfers with 32-bit data and address buses. Up to three modules can be attached to a baseboard.

The 4260 employs a 16-bit bus to move data at rates up to 20 Mbytes/s. Because all transfers take place locally over either the MIX bus or the front panel ports, full host bus bandwidth is maintained. The 4260 can be connected to C40 comm-port peripheral boards such as ADCs and DACs, digital receivers, and telecom interfaces. Data from these DSP boards or peripherals can be streamed directly to tape or disk. On-board dual FIFOs simultaneously buffer and decouple disparate transfer rates between the SCSI device and I/O data paths. A dual-port SRAM supports staging of large data blocks. These resources help boost overall throughput and real-time system performance.

The module's intelligent SCSI-2 processor, which runs at 25 MHz, handles high-level script commands, performs complex bus sequences without interrupts, and supports variable block sizes. On-chip features include two 32-bit FIFOs—one for synchronous transfers and one for 32-bit burst mode DMA transfers. The SCSI-2 bus interface incorporates active bus termination circuitry for improved noise immunity. The Model 4260 fast/wide SCSI-2 interface adapter is available now for $2495.

Pentek Inc., One Park Way, Upper Saddle River, NJ 07458-2311; (201) 818-5900. CIRCLE 704

■ RICHARD NASS

POWERPC BOARD BUILT FOR VMEBUS

The Galaxy PowerPC is a VMEbus-based single-board computer designed to address the needs of a cross-section of users in aerospace, military, scientific, telecommunications, and electronics industries for embedded-systems applications that may require a graphical user interface. It uses the PowerPC 604 processor, running at 100 MHz and higher, to offer a smooth transition to the expected large CHRP/PReP (Power PC Common Hardware Reference Platform) specification software base. The Galaxy desktop version runs WindowsNT, AIX, and Solaris; the embedded version runs VXworks and OS-9. It contains three on-board buses—a processor, PCI, and ISA—which run independently and concurrently. In addition, it includes the Tundra Technology Universe chip, and features 256 or 512 kbytes of L2 cache; up to 4 Mbytes of flash ROM; and a low-cost DRAM memory interface. Call the company for price and availability. CM

***Omnibytes Corp.,** 1078 Ponca Dr., Batavia, IL 60510; (800) 638-5022 or (708) 406-1333.* CIRCLE 705

PCI 2.0-COMPATIBLE BACKPLANE PROVIDES 9 PCI SLOTS

The 9-slot Model 15018-02 is the latest addition to ICS's 150xx series of ISA/PCI backplanes. It combines active elements with a passive backplane-style architecture. The backplanes allow users to install from four to nine PCI feature cards, depending on the number of chassis slots available. The heart of the backplane, the DEC PCI-to-PCI bridge chip, enables the high-performance throughput features of the PCI bus, as well as bus mastering, to be maintained across all PCI expansion slots. The bridge chip extends the standard PCI bus to allow additional loading and bus linking without degrading throughput handling capabilities. The 15018-02 is available now, with prices starting at $2849. CM

***Industrial Computer Source,** 9950 Barnes Canyon Rd., San Diego, CA 92121; (800) 523-2320.* CIRCLE 706

SBC INTEGRATES 200-MHZ PENTIUM, PCI

Embedded applications are the target for the VNS-686 Pentium-based single-board computers. The SBC supports CPUs with clock speeds up to 200 MHz and containing up to 128 Mbytes of EDO DRAM or SDRAM. On-board peripherals include a PCI interface, flat-panel-compatible SVGA, fast Ethernet, and fast and wide SCSI. The SVGA subsystem contains 2 Mbytes of video memory and supports most popular flat panels, including TFTs and 3.3-V models. There's also an interface for direct digital video input. The network interface features 10Base-T or 100Base-T operation with an AUI port for other media. Other functions include a watchdog timer and power-management modes. The board is specified for extended temperatures. Available by year's end, the VNS-686 SBC sells for $1845. RN

***Adastra Systems Corp.,** 26232 Executive Pl., Hayward, CA 94545; (510) 732-6900.* CIRCLE 707

PCI-BASED HOST ADAPTERS SUPPORT ULTRASCSI

Using the SYM22801 and SYM22802 host-adapter boards, OEMs can quickly get to market with a PCI-to-SCSI multifunction solution that requires just one PCI slot. Based on the SYM53C876 controller with dual wide UltraSCSI channels, the boards are suited for high-end desktops and servers with RAID subsystems. The difference between the two boards is that the SYM22801 is for dual single-ended applications, while the SYM22802 is aimed at dual differential applications. Both can handle throughputs up to 80 Mbytes/s. Among the included features are termination controls that automatically sense a cable connection to properly enable or disable a termination; a configuration utility that permits simple changes to default settings; and LEDs to indicate the absence of power. Drivers are included for Netware, UnixWare, OS/2, SCO OpenServer, and all versions of Windows. Sample boards will be available by the end of the year. RN

***Symbios Logic Inc.,** 2001 Danfield Ct., Fort Collins, CO 80525; (719) 533-7597.* CIRCLE 708

FAST ETHERNET TRANSCEIVER ON SINGLE CHIP FOR UNMANAGED REPEATERS

Representing the only 100Base-TX PHY (physical layer) fast Ethernet transceiver for unmanaged repeater applications, the ICS1891 offers significant power, space, and cost reductions for multiple port locations. The chip easily connects to all popular repeater controllers by providing both a standard 100-Mbit/s media independent interface (MII) and a 5-bit physical-coding-sublayer (PCS) interface. A 100-Mbit/s physical layer port, compliant to IEEE 802.3u, can be implemented with one IC and four resistors; total power consumption is less than 1 W. The ICS1891 interfaces directly to a transmit and receive isolation transformer and can support unshielded-twisted-pair (UTP) category 5 cables over 100 m.

The ICS1891 is essentially a nibble/bit-stream processor that takes, during transmission, sequential nibbles at the MII and translates them to a serial bit stream to the medium being used. It then takes the bit stream from the medium upon reception and translates the data to sequential nibbles for presentation to the MII. The processor has no knowledge of the nature of the underlying structure of the multiplexed signal frame it is passing. During transmission the frame, complete with preamble, it's encapsulated with start-of-stream and end-of-stream delimiters (SSDs and ESDs). When received, the SSD is stripped off and the normal preamble is substituted. After that, the preamble is presented to the MII until the ESD is detected and presentation is ended. The reconciliation layer thus sees an exact copy of the transmitted frame.

When no frames are being transmitted or received, the IC detects the idle condition and higher levels are allowed to check the integrity of the connection. A continuous stream of scrambled "1s" is transmitted to signify the idle condition in the 100Base-TX mode. The receive channel includes logic that looks for this pattern to confirm link integrity.

Easy connection to repeaters that only support a 100Base-TX 5-symbol interface can be made through the five-symbol interface, allowing access to raw groups with lower latency. This IC is the third generation of 100Base-TX solutions, featuring the highest levels of integration to date. Stream cipher scrambling, adaptive equalization, and baseline-wander correction circuitry are included on the 200-mA CMOS chip. The ICS1891 is available immediately in 64-pin QFP packaging (14 mm^2). It will sell for $16.30 in lots of 10,000.

Integrated Circuit Systems Inc., *1271 Parkmoor Ave., San Jose, CA 95126; (408) 297-1201; fax (408) 925-9460.*

CIRCLE 709

■ PAUL McGOLDRICK

ATM SAR SUPPORTS UNI 4.0 SPEC AND MPEG CELLS

Targeted for high-speed, high-bandwidth servers and switches, the TC35856F Meteor is among the first single-chip, 155-Mbit/s, ATM SAR chips to implement the new ATM Form UNI 4.0 specification. Its ability to support the new available bit rate (ABR) service protocol, which supports rate-based traffic management, simplifies the task of connecting legacy LANs to an ATM backbone. In support of UNI 4.0, the Meteor generates and processes ABR RM cells and provides per-VC rate control without host intervention. Support for other classes of service, allowing zero-cell-loss, best-effort QOS with increased reliability, is provided via raw 52-byte cells. Equally important, it supports MPEG transport cells, allowing designers to include features that will support multimedia applications. In addition, it can support constant-bit-rate (CBR) and unspecified-bit-rate (UBR) traffic.

The Meteor SAR, which contains a DMA engine that interfaces directly to a 33-MHz, 32-bit PCI (version 2.1) host system bus, uses host system memory for its segmentation and reassembly buffer functions. Interface to physical-layer devices is accomplished through the chip's 8-bit UTOPIA Level II-compliant interface. It also is capable of reverse-UTOPIA operation, making it possible to connect the device to a switch fabric through the same mechanism as all other ports on the switch. Both GFCR and Digital's FLOWmaster flow-control algorithms are supported

The TC35856F Meteor is sampling now, with full production scheduled for the end of 1996. Housed in a 208-pin PQFP, it operates on a 3.3-V power supply internally, with 5-V PCI-bus I/Os. The Meteor is priced at $65 each in 1000-piece quantities. LG

Toshiba America Electronic Components Inc., *9775 Toledo Way, Irvine, CA 92718; (800) 879-4963, (714) 455-2000, or (408) 749-5703.*

CIRCLE 710

OC-3 SONET/SDH TRANSLATOR SHIPS CELLS, FRAMES PACKETS

The PM5362 TUPP-Plus tributary processor provides a seamless interface for transporting Fast Ethernet, ATM, Frame Relay, and IP/Point-to-Point Protocol (PPP) over SONET networks at OC-3 speeds. Targeted at emerging datacom applications such as fiber-to-the-curb, systems, and SONET-based local loops, the TUPP-Plus can be combined with an HDLC controller to support direct mapping of Frame Relay or PPP traffic into SONET/SDH tributaries. Ethernet data can be similarly mapped using an Ethernet MAC and the TUPP-Plus. ATM applications also can be supported by employing a variety of ATM chips, including the PM7344 Quad T1/E1 S/UNI/PHY and the PM7345 T3/E3 S/UNI/PHY.

Intended for demanding applications in PSTN environments, the tributary processor meets all applicable ITU, ETSI, and Bellcore specifications, including ITU-T G.707, ETSI TM1015, and Bellcore GR-253. Typical applications include add/drop multiplexers, broadband cross-connects, and fiber-to-the-curb systems. The PM5362 provides front-end processing for low-order tributary pointers and overhead. Additional controls, such as the V5 and overhead indicator, eliminate the need for costly downstream pointer interpretation logic. Available now, the PM5362 TUPP-Plus comes packaged in a 160-pin PQFP and is priced at $116 each in quantities of 10,000 units. LG

PMC-Sierra Inc., *105-8555 Baxter Pl., Burnaby, British Columbia, Canada, V5A 4V7; phone (604) 415-6000; fax (604) 415-6200; Internet: http://www.pmc-sierra.com.* CIRCLE 711

HARDWARE/SOFTWARE CODESIGN TOOL ALLOWS FOR OPTIMUM PARTITIONING

Selecting the best hardware and software architectures for a given design can be a tedious and time-consuming task. For most real-time systems designers, though, getting the optimum hardware/software mix is crucial. To cut through the difficulties associated with identifying the most optimum partitioning between software and hardware, Omniview Inc., Pittsburgh, Pa., came up with the Performance Modeling Workbench (PMW). It's a VHDL-based hardware/software codesign tool designed specifically for use early on in the design process.

The main goals for the tool are to find optimum hardware/software architectures and to model system performance once a design is complete. This information, along with expected performance data, then can be confirmed using a hardware/software verification tool prior to any silicon being built. The architectures are captured graphically using either built-in editors or elements from PMW's generic parametrized VHDL model library that contains processors, memories, communications elements, and input and output devices. Elements also can be imported from upstream tools.

PMW works by enabling accurate modeling of the hardware/software architectures in VHDL. The models then can be simulated and analyzed for performance metrics such as latency, throughput, and utilization. With the debug mode, designers can view communications and task activities and, if needed, single-step through a simulation. Once a potential problem is localized, analysis tools, performance metric analyzers, histograms, and activity timelines can be called on to address the problem as well as enable designers to find the most optimum solution.

Hardware/software "Design Editors" are available to support unlimited levels of hierarchy and multiple element models at each level. A "Mapping Editor" allows designers to assign software tasks to processing elements, while a suite of graphical analysis tools makes it possible to quickly identify potential bottlenecks and overdesigns. For example, the "Hot Spot Analyzer," based on a pseudo-temperature scale with the color red designated as the high-end of the scale, colors the blocks in the hardware architecture to show how a performance metric, such as utilization, varies over time. Using this color system, the designer can instantly identify bottlenecks by their red color and underutilized blocks by their blue color.

To monitor detailed performance metrics on either hardware blocks or software tasks, individual "Performance Metric Analyzers" can be employed. An added feature, the "Analysis Control Panel," gives designers a wide range of flexibility to run a simulation forward or backward in time, change playback rate, and even adjust the step size and start time. The designer can opt to control multiple hot spot analyzers, performance metric analyzers, histograms, and activity timelines all from a single control panel. For comparison purposes, the designer also can choose to designate a different control panel for up to eight different designs.

Because the tool allows for separate modeling, as opposed to the more conventional integrated method of modeling of hardware and software, it's possible for designers to examine and compare the performance outputs of various hardware/software architectures. PMW also allows for the exploration of trade-offs between single- and multiple-threaded implementations. As an added benefit, the VHDL-based nature of PMW's models enables designers to create testbenches and evaluate the performance of VHDL behavioral models created downstream in the design process. The first production release is scheduled for the fourth quarter of this year, and will be available on both Sun SPARCstation and HP9000 platforms. Pricing information has yet to be finalized.

***Omniview Inc.**, 100 HighTower Boulevard, Pittsburgh, PA; (412) 788-9492.* CIRCLE 712

■ CHERYL AJLUNI

DESIGN KIT FOR VHDL TEACHES DESIGN TECHNIQUES

A synthesis tool kit for FPGA design, the VHDL Discovery Kit, runs on Windows-based platforms and provides a full synthesis environment based on Exemplar's Galileo synthesis engine. It also contains the Esperan interactive multimedia VHDL training course. Along with the synthesis engine, the tool includes the HDL Logic Explorer for Windows and VHDL language support with architecture-specific logic optimization and the ModGen operator library. The kit accepts VHDL as input and offers synthesis and optimization for a single FPGA library from any one of several companies—Actel, Altera, Lucent Technologies, or Xilinx. The Discovery Kit offers users a migration path to the company's full Galileo or Leonardo design environments. The kit's multimedia course covers topics such as design definition, VHDL constructs, rules for manipulating signals and data types, and mixing concurrent and sequential statements. Ideal for new users, the courseware allows designers to learn synthesis and optimization techniques and reduces the time needed to become productive using the tools. The kit sells for $3495 in the U.S. and $4000 elsewhere. DB

***Exemplar Logic**, 815 Atlantic Ave., Ste. 105, Alameda, CA 94501-2274; Ashena Massoumi, (510) 337-3720.* CIRCLE 713

TRANSLATOR UTILITY OFFERS EASY DOCUMENT CONVERSION

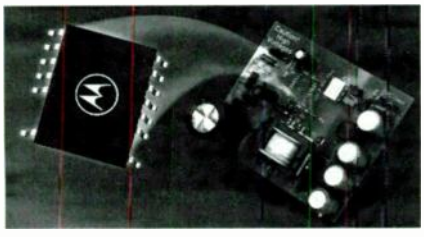
The latest product offering in a family of translator utilities, the OrCAD SDT to McCAD translator, is specially designed to convert standard OrCAD schematics documents to McCAD ASCII format documents. The McCAD EDA software tools address all aspects of the design solution, from schematic capture and simulation to pc-board layout and autorouting. Thanks to this utility, designers using the Macintosh OS environment can quickly and easily import OrCAD documents and libraries into the McCAD EDA software toolsuite environment. The translator utility will work with McCAD Schematics version 3.4 and higher. CA

***VAMP Inc.**, 6753 Selma Ave., Los Angeles, CA, 90028; (213) 466-5533; fax (213) 466-8564.* CIRCLE 714

POWER

SWITCHING REGULATORS INTEGRATE POWER SWITCH

The MC33362 and -63 monolithic switching regulators simplify design by integrating the high-voltage power switch and startup transistor on chip. These regulators are ideal for off-line



power supplies and for dc-dc converters with high-voltage input and/or output. Their heat tab power package eliminates the need for an add-on heat sink. The MC33362 is designed for rectified 120 V ac line operation. It contains a 500-V, 2-A SenseFET power switch, 250-V active off-line startup FET, duty-cycle-controlled oscillator, and current-limiting comparator with a programmable threshold. Also included is circuitry for double pulse suppression, a high-gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle-by-cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. The MC33362 is likewise equipped, but designed for rectified 240-V ac line operation. Both are suitable for use in flyback or other converters having a single grounded switch. They operate over the range of –25°C to +125°C. VB

***Motorola Inc.**, Analog Marketing, MD EL340, 2100 E. Elliot Rd., Tempe, AZ 85284; (602) 413-3615.* CIRCLE 715

SMALL DC-DC CONVERTERS SUIT RUGGED ENVIRONMENTS

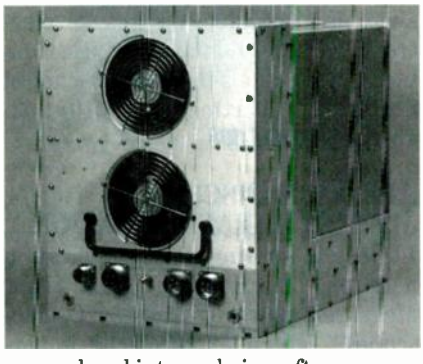
Measuring just 1 by 2 in., the IMX7 family of 7-W dc-dc converters also is available for rugged environments. Available operating input voltage ranges are 8.4 to 36, 16.8 to 75, and 40 to 121 V dc. Standard models offer a single output from 3.3 to 48 V, or dual outputs from ±5 to ±24 V dc. It delivers full output power at –25 to +71°C or –40 to +85°C without derating. It provides 1500-V isolation, input transient voltage protection that meets IEC 801 standards, and low radiated EMI to meet EN55022, level B. Remote on/off and voltage trimming are

standard. Options include surface-mount packaging, an output good signal, and a "power OK" LED. VB

***Melcher**, 187 Billerica Rd., Chelmsford, MA 01824; (508) 256-1812.* CIRCLE 716

AC-AC SWITCHER TARGETS AIRBORNE APPS

This 10-kVA, ac-ac frequency converter/switching supply is aimed at airborne and mobile applications. Its topology, which includes power-factor correction, allows seamless transfer between two ac sources, such as



ground and internal aircraft power, or between two engine generators. This eliminates drop-outs that might disrupt sensitive avionics systems. It's cooled by internal fans. Operating at altitudes up to 40,000 ft., the switcher is consistent within the temperature ranges of –55 to +71°C. Weight is approximately 130 lbs. VB

***Custom Power Products**, 85 Horsehill Rd., Cedar Knolls, NJ 07927. (201) 267-2047.* CIRCLE 717

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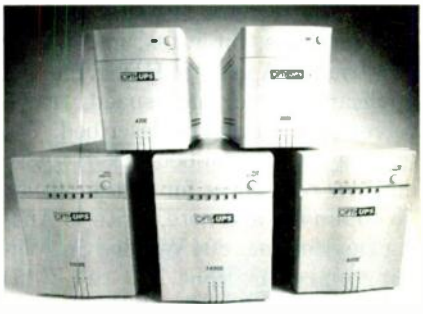
The model 412CE servoamplifier is the first in Copley's line to conform to all three relevant European Community standards (electromagnetic emissions, electromagnetic immunity, and product safety). As a result, the unit surmounts the barriers that otherwise mitigate against European import of American equipment. The amplifier features an output of ±85 V at ±20 A (peak current). It develops four-quadrant power from a single-polarity 24-to-90-V dc supply. Operation is at a switching frequency of 25 kHz, which permits 3-kHz bandwidth, and accom-

modates motors with inductances from 200 µH to 40 mH. Protection is provided against overvoltage, undervoltage, heat-sink overtemperature, and short circuits. Color LEDs are supplied for operational status display. Pricing is $299 in quantities of one to nine with delivery in four weeks. DM

***Copley Controls Corp.**, 410 University Ave., Westwood, MA 02090; (617) 329-8200.* CIRCLE 718

UPSs' SOFTWARE SUITE GIVES USERS CONTROL

The OPTI-UPS line of uninterruptible power supplies now includes the Power Management Software Suite for advanced user control and moni-



toring. The software also supports Windows 95 automatic installation via Microsoft Plug and Play. In the event of a power outage, the suite provides unattended shutdown for several operating systems and closes all open files. With the addition of the suite, OPTI-UPS models 280E through 1400E include everything users need to simplify use. Retail pricing for the systems starts at $139 and ranges up to $599. DM

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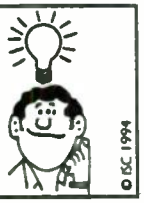

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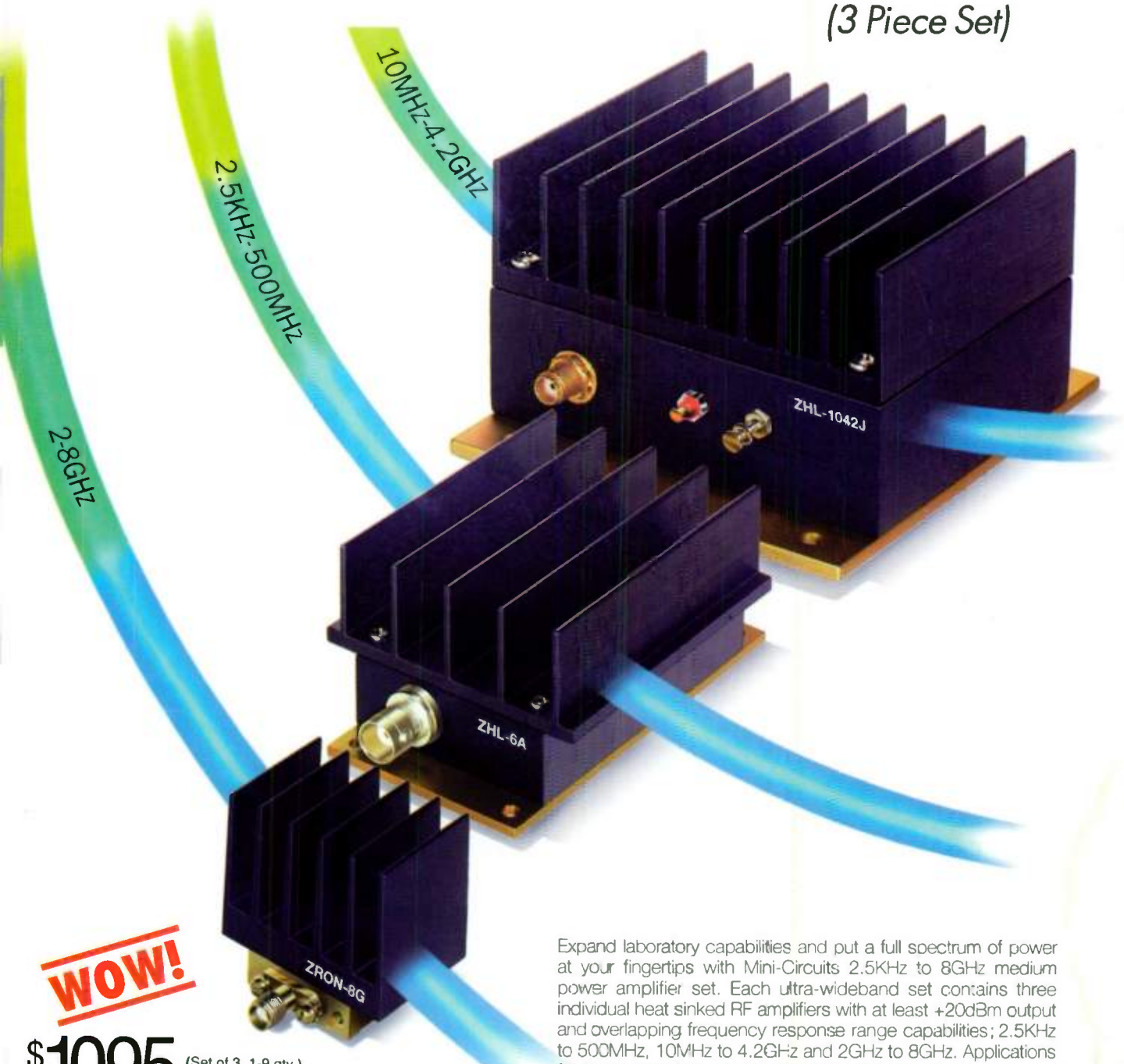

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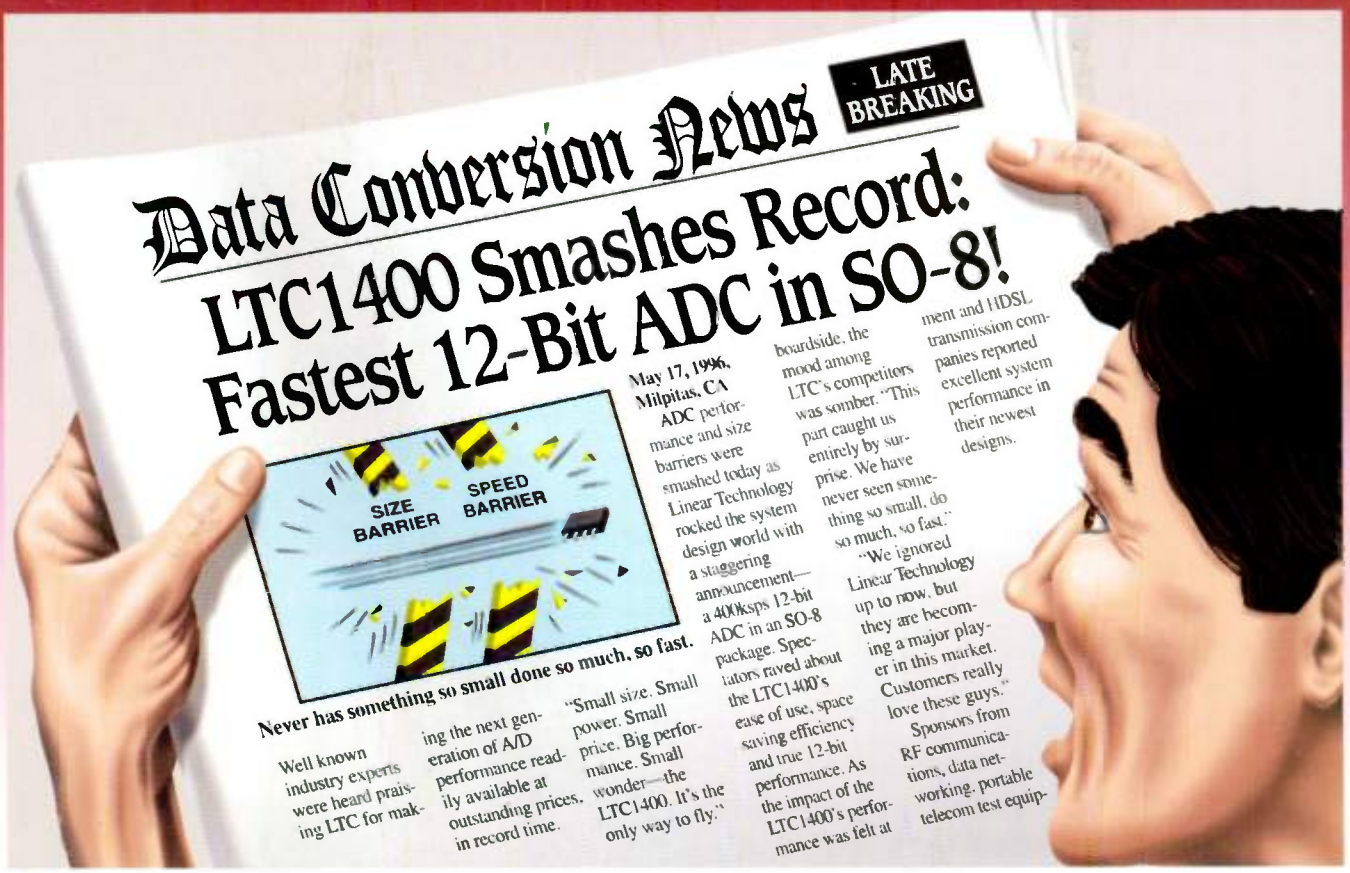

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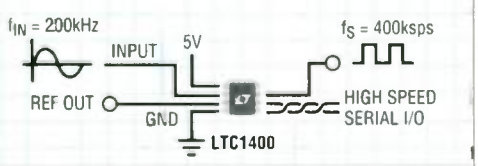
Fastest 12-Bit ADC in SO-8



Want to learn more about this tiny speed demon? Contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, (408) 432-1900. Fax: (408) 434-0507. For literature only: **1-800-4-LINEAR**.

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