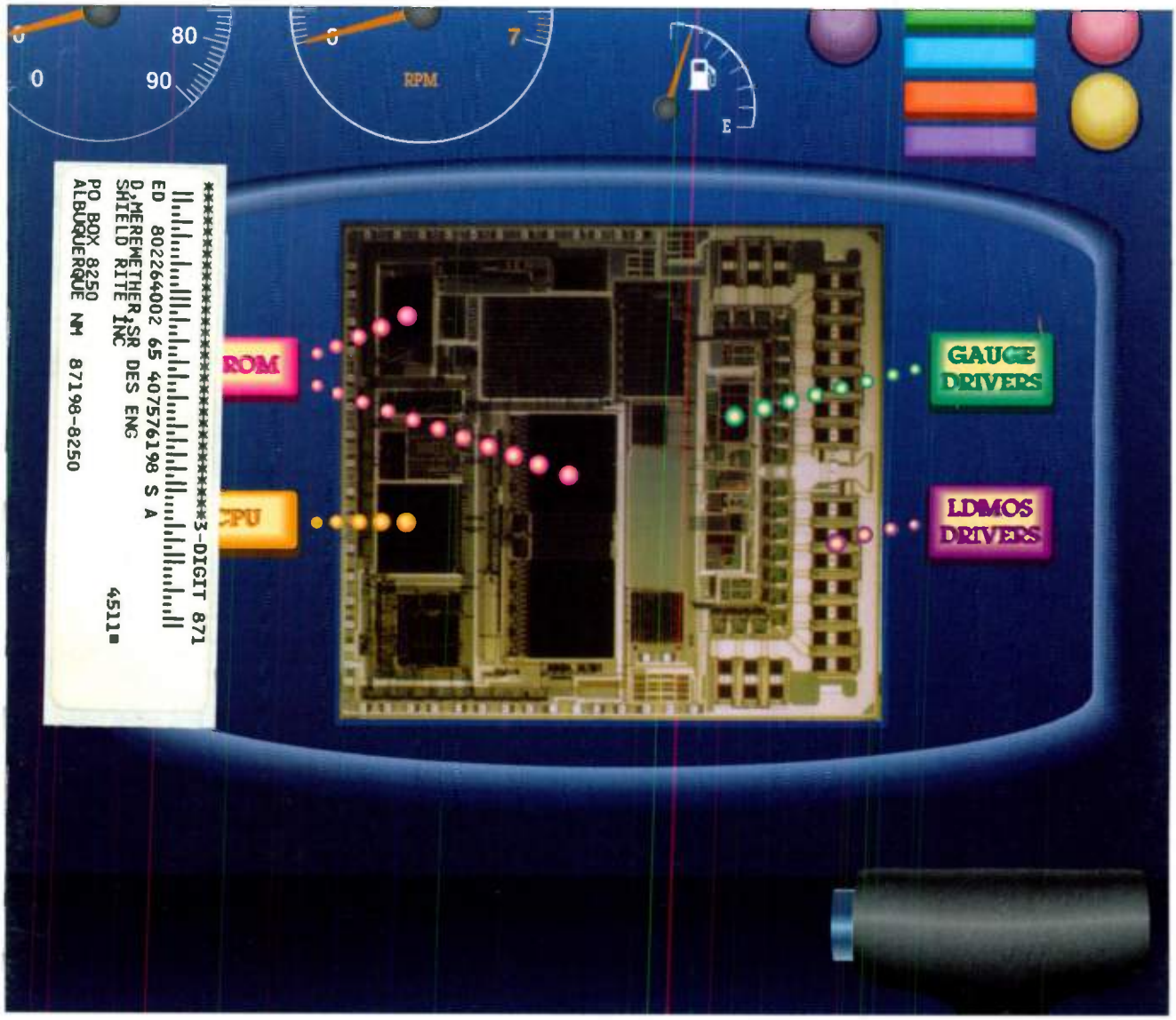
ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

A PENTON PUBLICATION $10.00

DECEMBER 2, 1996



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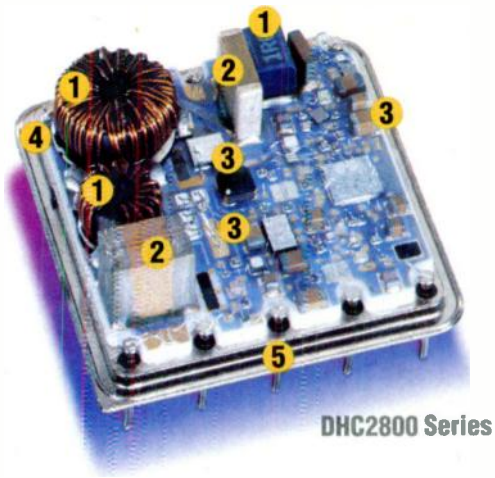

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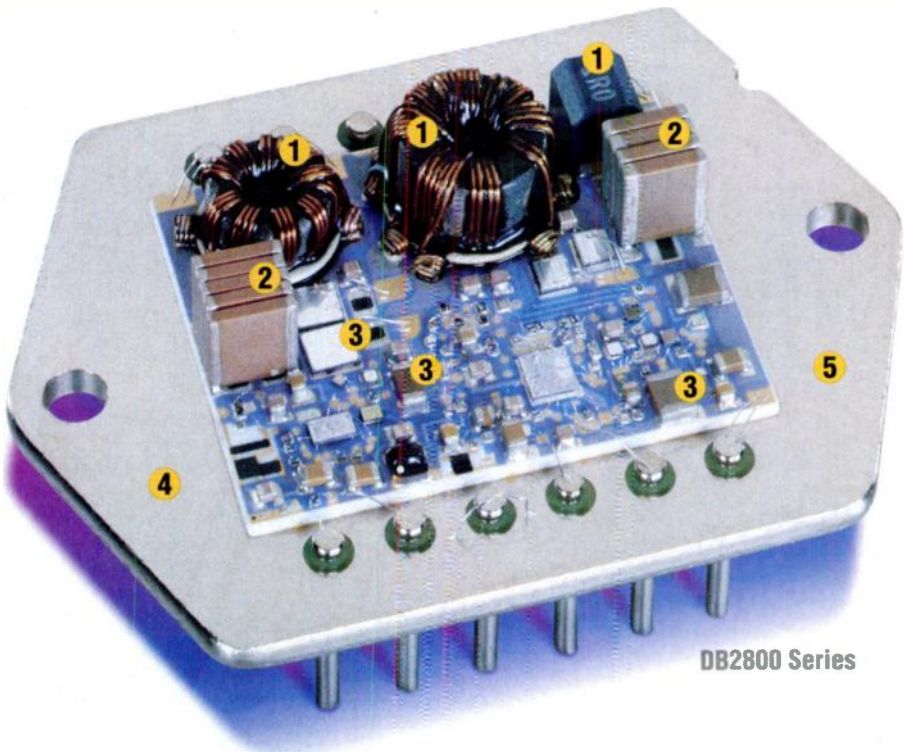

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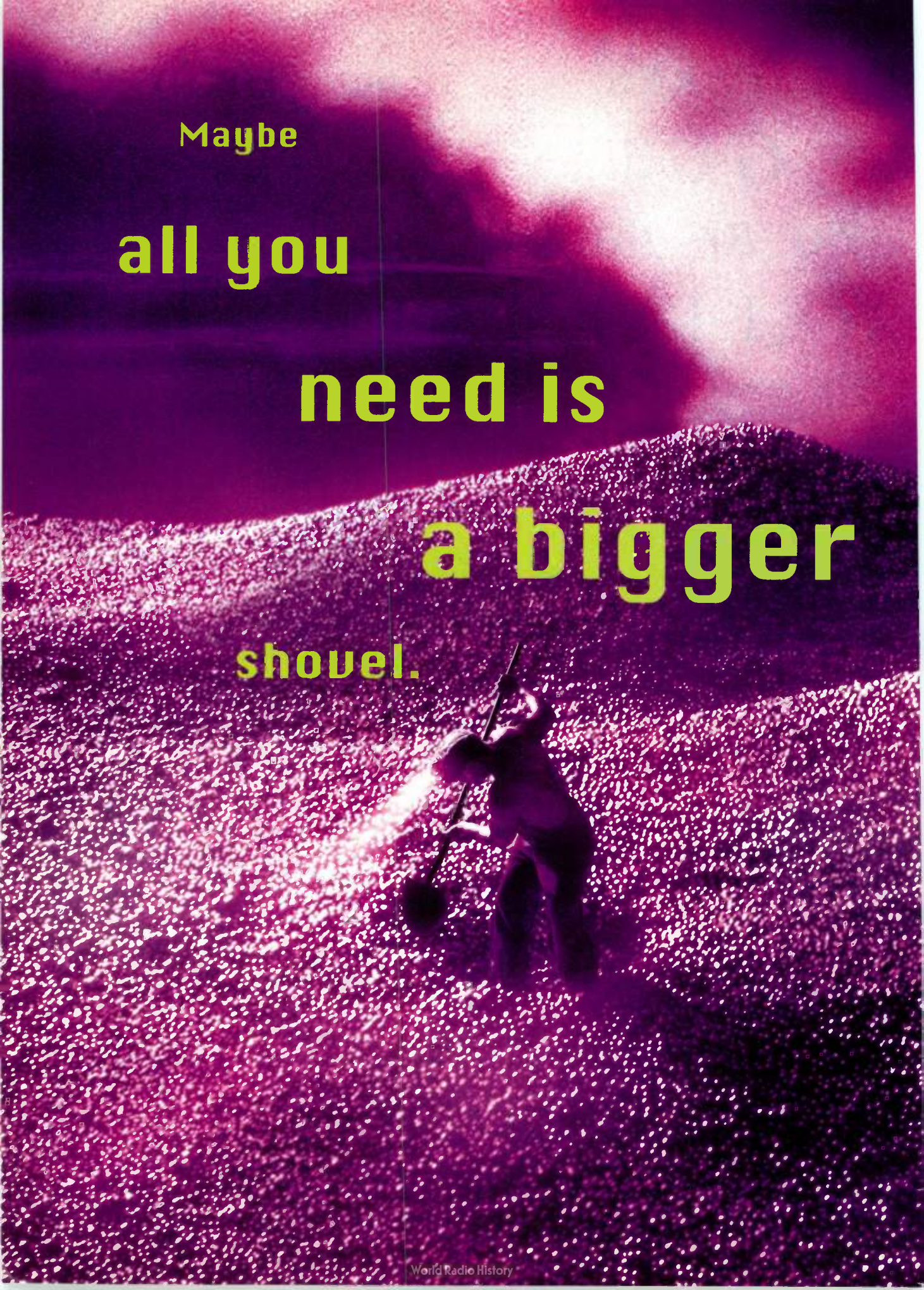

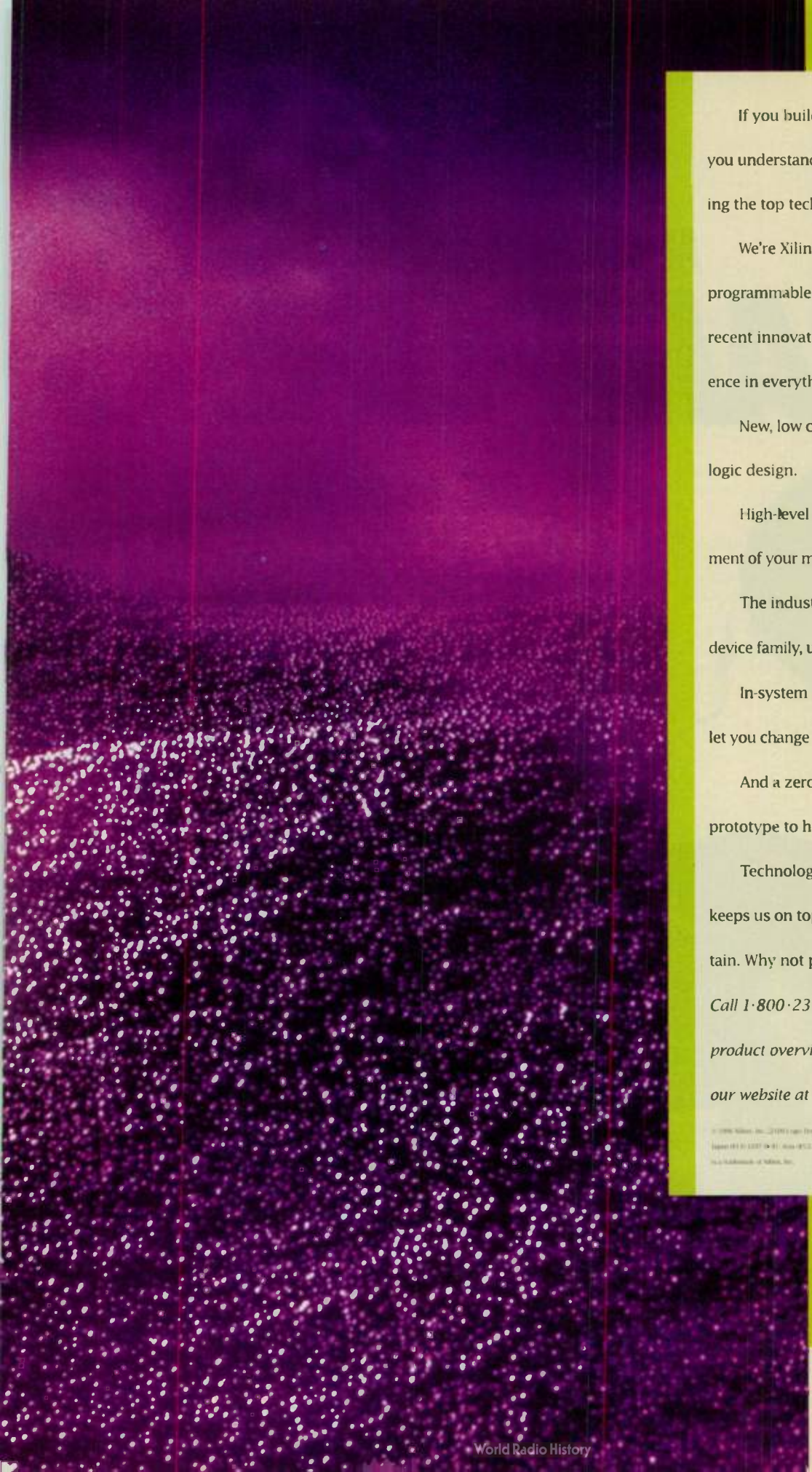

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Model	*Freq (MHz)	Gain (dB)	Max. Power Out (dBm @ 1dB Comp)	Dynamic Range NF(dB)	IP3(dBm)	①Price $ ea. (10 Qty.)
ERA-1	DC-8000	11.6	13.0	7.0	26	1.80
ERA-1SM	DC-8000	11.0	13.0	7.0	26	1.85
ERA-2	DC-6000	14.9	14.0	6.0	27	1.95
ERA-2SM	DC-6000	13.1	13.0	6.0	27	2.00
ERA-3	DC-3000	20.2	11.0	4.5	23	2.10
ERA-3SM	DC-3000	19.4	11.0	4.5	23	2.15
ERA-4	DC-4000	13.9	▲19.1	5.2	▲36	4.15
ERA-4SM	DC-4000	13.9	▲19.1	5.2	▲36	4.20
ERA-5	DC-4000	19.0	▲19.6	4.0	▲36	4.15
ERA-5SM	DC-4000	19.0	▲19.4	4.0	▲36	4.20

Note: Specs typical at 2GHz, 25°C.
▲ Typ. numbers tested at 1GHz. At 2GHz, Max. Pwr. Out may decrease by 0.4dB & IP3 by 3 to 4dB.
* Low frequency cutoff determined by external coupling capacitors.
① Price (ea.) Qty. 1000: ERA-1 $1.19, -2 $1.33, -3 $1.48, -4 or -5 $2.95. SM option same price.

DESIGNER'S AMPLIFIER KITS:
K1-ERA: 10 of each ERA-1,-2,-3 (30 pieces) only $49.95
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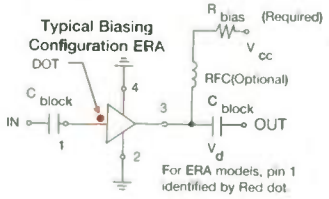
K2-ERA: 10 of each ERA-4,-5 (20 pieces) only $69.95
K2-ERASM: 10 each ERA-4SM,-5SM (20 pieces) only $69.95

Chip Coupling Capacitors at 12c each (50 min.)

Size (mils)	Value
80x50	10, 22, 47, 68, 100, 220, 470, 680, 1000, 2200, 4700, 6800, 10,000 pf
120x60	.002, .047, .068, .1 µf

ERA-1 ERA-1SM
ACTUAL SIZE



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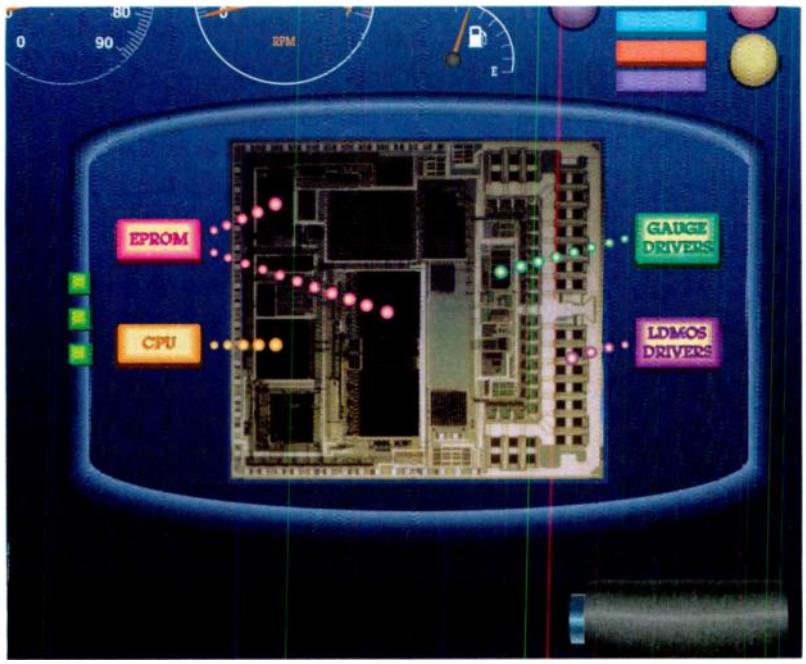
ELECTRONIC DESIGN

December 2, 1996 Volume 44, Number 25

COVER STORY



Integrated 8-Bit MCU Handles High-Power Applications p. 85

With both high-current and high-voltage drive, MCU tackles automotive systems and more.

THE ANNUAL 1996 IEDM

Annual IEDM Conference Previews Cutting-Edge Device Developments p. 41

New processes for analog, digital, and mixed-signal devices, and the latest developments in device modeling and simulation, are on the agenda.

IEDM Showcases Tomorrow's Analog Semiconductors p. 42

IEDM Spans Image Sensors Through RF p. 54

Novel Processes, Structures To Yield Advanced Digital ICs p. 60

Modeling And Simulation Make Designing Easier p. 68

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DESIGN APPLICATIONS

Ease System Simulation With IBIS Device Models p. 93

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published twice monthly except for 3 issues in May and 3 issues in October by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $105 U.S., $185 Canada, $210, $255 International. Periodicals Postage Paid at Cleveland, OH and at additional mailing offices. Editorial and advertising addresses. ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393 0204. Printed in U.S.A. Title registered in U.S. Patent Office.

 For subscriber change of address and subscription inquiries, call (216) 696-7000. Mail your subscription requests to: Penton Publishing Subscription Lockbox, P.O. Box 96732, Chicago, IL 60693.
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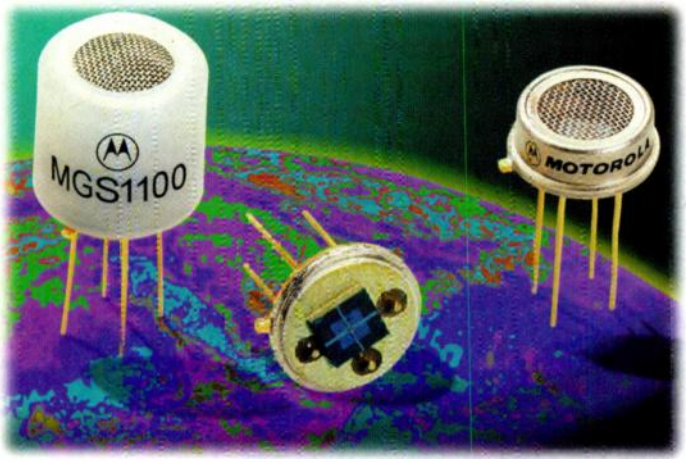
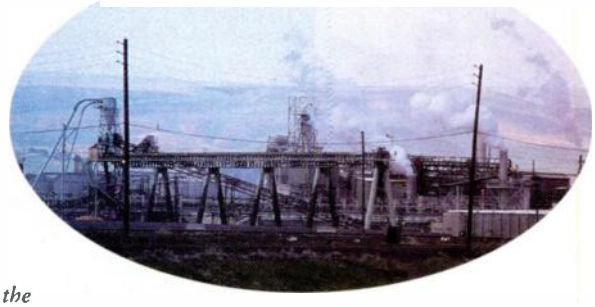
GAS SENSORS BY MOTOROLA

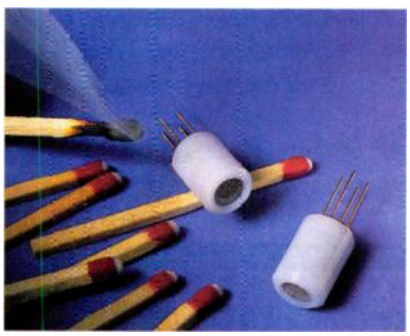


Senseon™ gas sensors improve your ability to detect the presence of a variety of hazardous gases, for a proactive solution to sensing the environment and the world around us.



Senseon gas sensors for cabin air quality sensing.

The compact size of the Senseon MGS1100 carbon monoxide sensor allows it to fit virtually any design configuration.



Senseon MGS1100 carbon monoxide sensor is ideal for commercial and industrial detector applications.

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- The MGS1100 combines with related Motorola products for a total system solution and,
- We're committed to the future. The Motorola gas sensor family plans to introduce the MGS1200 methane (CH_4) sensor along with new MGS1100 enhancements throughout 1997.

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ELECTRONIC DESIGN

December 2, 1996 Volume 44, Number 25

DEPARTMENTS

Jesse H. Neal Editorial Achievement Awards: 1967 First Place Award; 1968 First Place Award; 1972 Certificate of Merit; 1975 Two Certificates of Merit; 1976 Certificate of Merit; 1978 Certificate of Merit; 1980 Certificate of Merit; 1986 First Place Award; 1989 Certificate of Merit; 1992 Certificate of Merit

COVER ART: MARGARET ENDRES

40 YEARS AGO

Cable Fault Finder Uses Pulse Radar

Problems of cable and connector inspection and maintenance are simplified by the model 60A fault finder. This is accomplished by applying the pulse radar principle of time interval measurement between a transmitted and reflected pulse. Cables with lengths between 10 and 200 ft may be checked for the location of open circuits as well as grounds and short circuits.

The characteristic impedance of cables may be determined by using the Model 60A with a calibrated variable resistance connected across the end of the cable. With the cable terminated in its characteristic impedance, no reflections will be seen on the screen. Radar Eng., Dept. ED, 401 E. 45th Street, Seattle 5, Wash.*(Electronic Design, December 15, 1956, p. 79)*

What are the chances that this company, based in Boeing's home town, developed these early time-domain reflectometers for use on aircraft wiring harnesses?—SS

Waveform Generator Transistorized

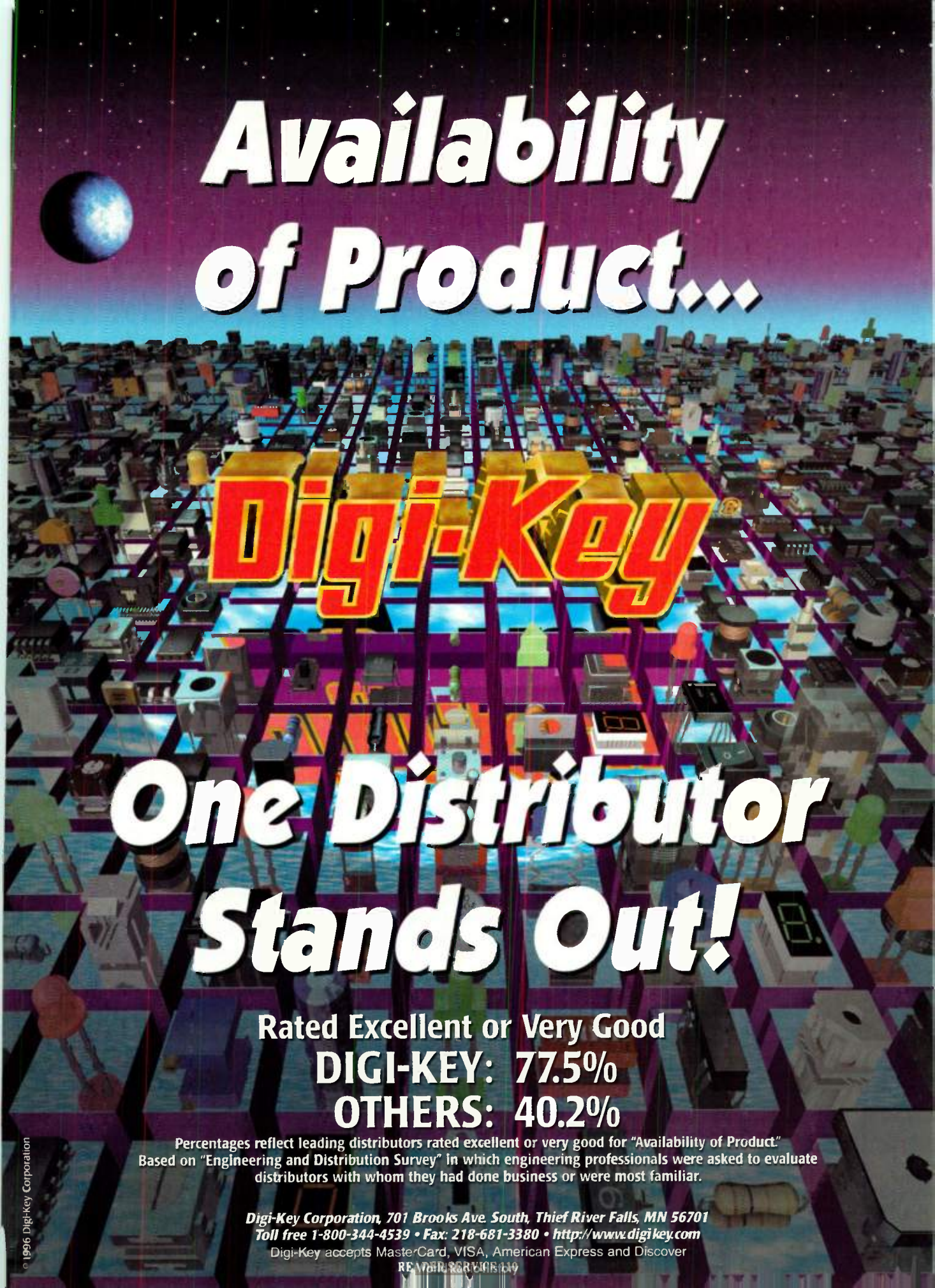
The first of a line of full-transistorized, battery-powered test equipment, the Model 500 waveform generator provides clipped-sawtooth and rectangular waveform output with a variable repetition rate from 10 cps to 50 kc. A square wave output is available from 5 cps through 25 kc. With one change in a capacitor, these repetition rates may be reduced to one every 5 seconds. At full battery voltage an output of seven volts at 2000 ohms impedance is available. The rectangular wave shape is continuously variable in pulse width from 5 to in excess of 200 usec. With a total power drain of 300mw, the anticipated life of the 22-1/2 v battery is better than 500 hours. As the battery output voltage drops off, there is no deterioration in wave shape or stability. Cubic Corp., Dept. ED, San Diego, Calif.*(Electronic Design, December 1, 1956, p. 49)*

Cubic Corp. was one of the innovators in transistor-based instruments.—SS

Earth Satellite Launching Vehicle

Critical tolerances constitute the outstanding manufacturing feature of the Vanguard Launching vehicle which will attempt to place the world's first man-made satellite in its orbit 300 miles above the surface of the earth. When fueled for take-off, Vanguard will weigh approximately 11 tons. Every pound of the structural dead weight eliminated in a rocket yields an increase in the vehicle's attainable velocity. The vital importance of weight saving with a consequent velocity gain is apparent when it is considered that if the vehicle fails to attain the initial altitude of 300 miles and a velocity of approximately 25,000 ft per second (about 18,000 miles per hour) the satellite will fail to orbit and will spiral down to earth.*(Electronic Design, December 15, 1956, p. 79)*

Things didn't quite work out the way they were planned, and Vanguard was not the first man-made satellite in orbit—the U.S.S.R's Sputnik preceded it into orbit late the following year (October, 1957). I can recall standing outside the first night we got the news and looking upward, trying to see this foreign object that was intruding on our space—it was an eerie feeling. Soon, President Eisenhower pulled out all the stops to catch up in the space race and technical education was a side beneficiary, with more federal money pouring in.—SS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Editorial Headquarters: 201 393-6060
P.O. Box 821, Hasbrouck Hts., N.J. 07604

Field Correspondents:
West Coast Executive Editor:
Dave Bursky
Western Regional Editors:
Cheryl J. Ajluni
Paul McGoldrick
Tom Williams
2025 Gateway Place, Suite 354
San Jose, CA 95110
(408) 441-0550

London: Peter Fletcher
16 Maylons Road
Hextable, Kent, UK
44 1 322 664 355
Fax 44 1 322 669 829

Munich: Alfred B. Vollmer
Eichenstr. 6
82024 Taufkirchen (near Munich)
Germany
49 89 614-8377
Fax 49 89 614-8278

Chief Copy Editor: Michael Sciannamea
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Advertising Production:
(201) 393-6093 or Fax (201) 393-0410

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Si3455DV/X	30	0.100	0.19	±3.5	P-Ch
Part No.	V_{DS} (V)	V_{GS} = 4.5 V	V_{GS} = 2.5 V	I_D (A)	Gender
Si3442DV/X	20	0.07	0.095	±4.0	N-Ch
Si3441DV/X	20	0.10	0.135	±3.3	P-Ch

(Almost actual size.)

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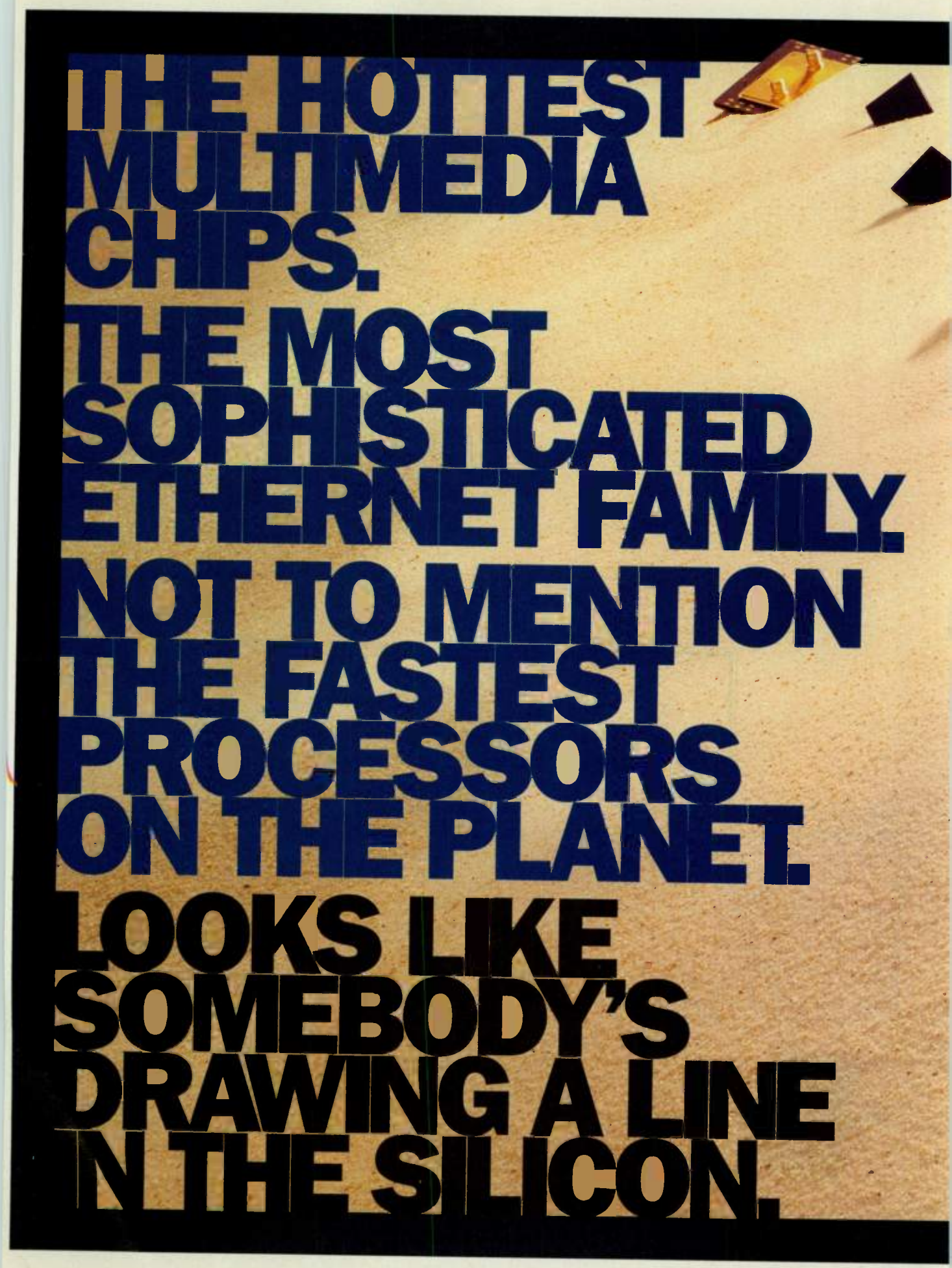
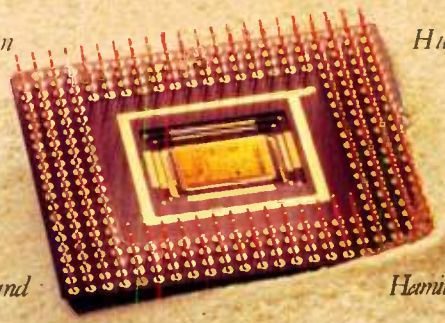


DIGITAL SEMICONDUCTOR

Everyone who makes semiconductors starts with the same raw materials. Not everyone starts with the same raw ambition. How else to explain the steady stream of world-class chips from Digital Semiconductor? Case in point: a family of PCI Ethernet chips that includes the world's leading Ethernet and Fast Ethernet controllers.

Case in point #2: the world's first PCI-to-PCI bridge chip, created to liberate designers once and for all from load limits. And satisfy a marketplace hungry for more expansion slots. (In fact, Digital Semiconductor is a founding member of the PCI Special Interest Group, with a powerful commitment to advancing PCI architecture. Not exactly the sign of a one-chip wonder.) Speaking of wonders, we've also created the first PCI Bus Master graphics controller that merges lightning-fast graphics with full motion-video, all on a single chip. Our powerful 3D graphics accelerator is shipping now. And our video codec is waiting in the wings. In a newly minted partnership with Advanced RISC Machines, Ltd., we'll codevelop the StrongARM family of high-performance, low-power RISC processors. They'll light up interactive TV and multimedia games, personal digital assistants, smart phones and digital cameras—the hot new consumer electronics of the late '90s. And Digital Semiconductor doesn't just create new designs. We've also created one of the planet's most advanced foundries to produce them: our showcase FAB-6 in Hudson, Mass., supporting 0.35 micron to 0.18 micron technologies. Just as important, we've forged new links with distributors and manufacturers' reps worldwide, like Wyle, Pioneer Standard and affiliate Pioneer Technologies, and Hamilton Hallmark. To get chips into your hands easily, quickly, and in volume. And yes, this is the same Digital Semiconductor that created the Alpha chip family. Nothing less than the fastest microprocessors on earth. Call 1-800-332-2717, extension 19, or see us at http://www.digital.com/info/semiconductor to learn more about Digital Semiconductor's line. We think it'll be some time before anyone steps across it.



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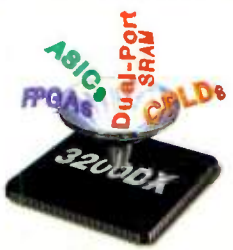
WHATEVER IT TAKES

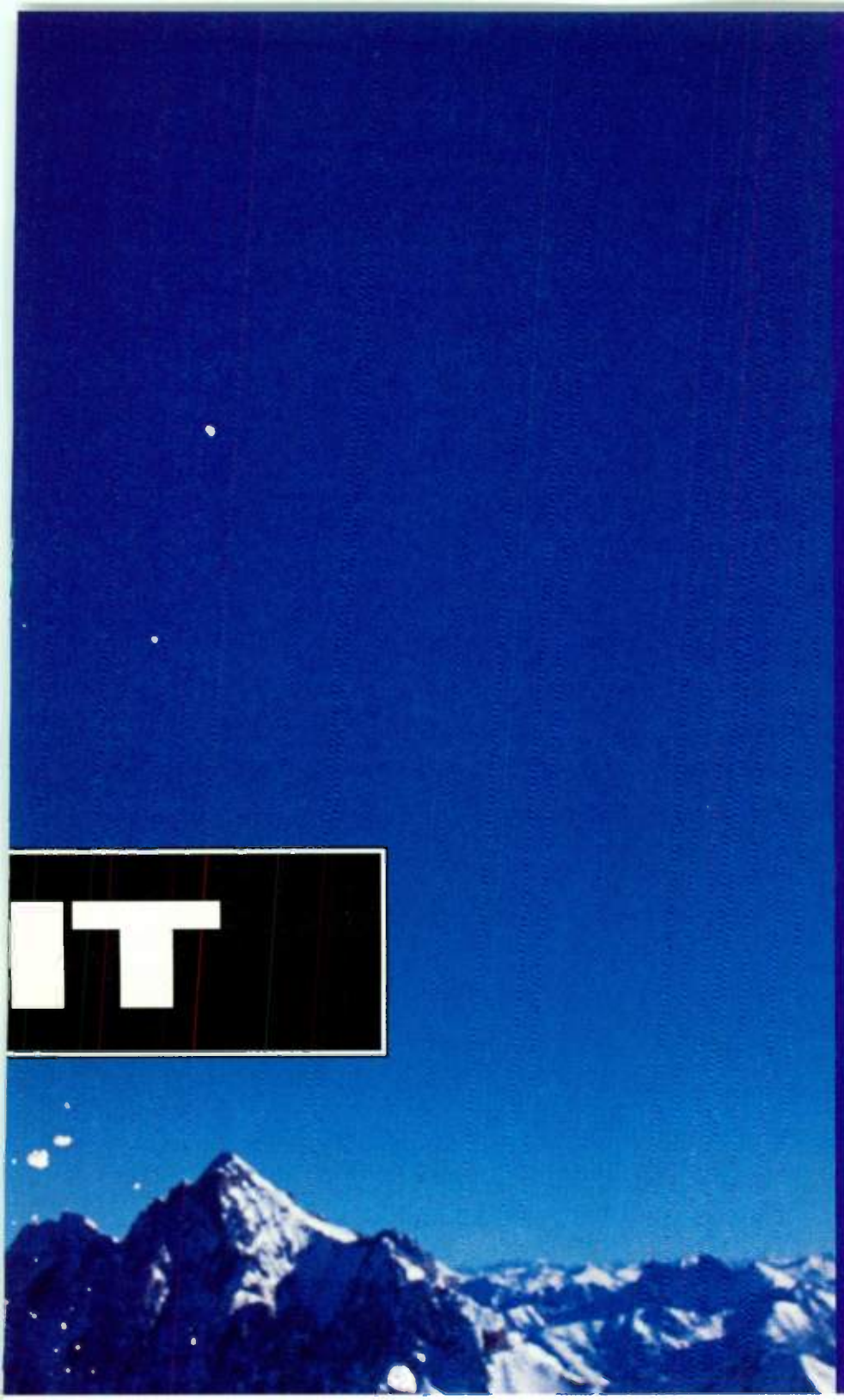
Get the most from your high level designs with Actel's 3200DX—system logic integrated on a single chip.



Integrator Series

Get total system logic integration and fully deterministic design with Actel's 3200DX FPGA Family.

By bringing together a balance of the right silicon and the right design tools, the 3200DX Family lets you focus on where you want to go, instead of how to get there. You'll get 5 ns dual-port SRAM speed, 7.5 ns decode, 200 MHz data rates, and up to 40,000 usable gates.



"The complexity of our design required us to design in Verilog HDL. We were able to utilize 94% of Actel's 14,000 gate 32140DX device, yet were unable to fit the design into other FPGA vendor's comparable parts that claimed to be 40% larger. We were surprised at the ease-of-design with Actel. The Designer Series place and route software, coupled with Actel's DirectTime editor and the device architecture allowed us to quickly and easily achieve our performance goals. Place and route was two to three times faster than alternative FPGA options, allowing us to perform multiple iterations in an eight-hour day."

<<<<<<<<<<

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UPCOMING MEETINGS

DECEMBER

35th IEEE Conference on Decision & Control, Dec. 11-13. International Conference Center Kobe and Portopia Hotel, Kobe, Japan. Contact Hidenori Kimura, Faculty of Engineering, Osaka University, Suita, Osaka 565, Japan; (810) 6 877 5111, ext. 5121.

Miniature Card Implementers Forum Info Workshop, Dec. 12. Austin, TX. Contact Kevin Randolph, (800) 462-1042 or (619) 673-0870; fax (619) 673-1432; e-mail: mcif@annabooks.com; Internet: http://www.annabooks.com.

JANUARY 1997

USENIX 1997 Technical Conference & Linux Applications Development & Deployment Conference, Jan. 6-10. Marriott Hotel, Anaheim, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

USENIX Technical Conference, Jan. 6-10. Marriott Hotel, Anaheim, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

Annual Reliability & Maintainability Symposium (RAMS), Jan. 20-23. Philadelphia Marriott, Philadelphia, PA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Asia & South Pacific Design Automation Conference with EDA Technofair (ASP-DAC 97), Jan. 28-31. Makuhari Messe Convention Center, Chiba, Japan. Contact Yoko Nishikawa, ASP-DAC '97 Secretariat, CONVEX Inc., Ichijoji Bldg. 2-3-22 Azabudai, Minato-ku, Tokyo 106 Japan; (81) 3 3589 3355; fax (81) 3 3589 3974; e-mail: convex@po.iijnet.or.jp; http://www.jesa or jp/ASPDAC/.

Second Annual Pan Pacific Microelectronics Symposium, Jan. 29-31. Sheraton Maui Resort, Maui, HI. Contact JoAnn Stromberg, Pan Pacific Symposium, 5200 Wilson Rd., Suite 215, Edina, MN 55424; fax (612) 929-1819.

FEBRUARY

IEEE Aerospace Conference, Feb. 1-8. Snowmass at Aspen, Colorado Contact Stephen Franklin, Deputy Program Chair, 4800 Oak Grove Dr., Pasadena, CA 91109; (818) 393-0814; fax (818) 393-0530; e-mail: stephen.f.franklin@jpl.nasa.gov.; Internet: http://chirp.plk.af.mil:1050/ieee/index.html.

IEEE Power Engineering Society Winter Meeting, Feb. 2-6. New York Hilton & Towers, NY. Contact Frank E. Schink, 14 Middlebury Ln., Cranford, NJ 07016-1622; (908) 276-8847; fax (908) 276-8847.

IEEE International Solid-State Circuits Conference (ISSCC 97), Feb. 6-8. San Francisco Marriott Hotel, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Suite 300, Washington, D.C. 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@mcimail.com.

Second International Conference on Chip-Scale Packaging, Feb. 20-21. Sunnyvale Hilton Inn, Sunnyvale, CA. Contact Subash Khadpe; (610) 799-0419; fax (610) 799-0519; e-mail: skhadpe@semitech.com.

IEEE Applied Power Electronics Conference and Exposition (APEC 97), Feb. 23-27. Westin Peachtree Plaza Hotel, Atlanta, GA. Contact Pam Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 347-5900; fax (202) 347-6109.

SOUTHCON 97, Feb. 25-27. Greater Ft. Lauderdale/Broward County Convention Center, Fort Lauderdale, Florida. Contact Joan Carlisle, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668 ext. 243; fax (310) 641-5117.

MARCH

IPC Printed Circuits Expo 97 and 40th Annual Meeting, March 9-13. San Jose Convention Center, San Jose, California. Contact JoAnn Galluzzi (847) 509-9700; Internet: http://www.ipc.org.

European Design & Test Conference (ED&TC 97), Mar. 17-20. CNIT Conference & Exhibition Centre, Paris-La Defense, France. Contact ED&TC Conference Secretariat, CEP Consultants Ltd., 43 Manor Pl., Edinburgh, EH3 7EB, UK; (44) 131-300 3300; fax (44) 131-300 3400; e-mail: edtc@cep.u-net.com.

Communication Design Engineering Conference, Mar. 24-26. Washington, DC. Convention Center, Washington, DC. Contact Denise Chan, Miller-Freeman Inc., (415) 278-5231.

Sixth International Verilog Conference, Mar. 31-Apr. 2. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: ivcinfo@ivc-conf.com.

APRIL

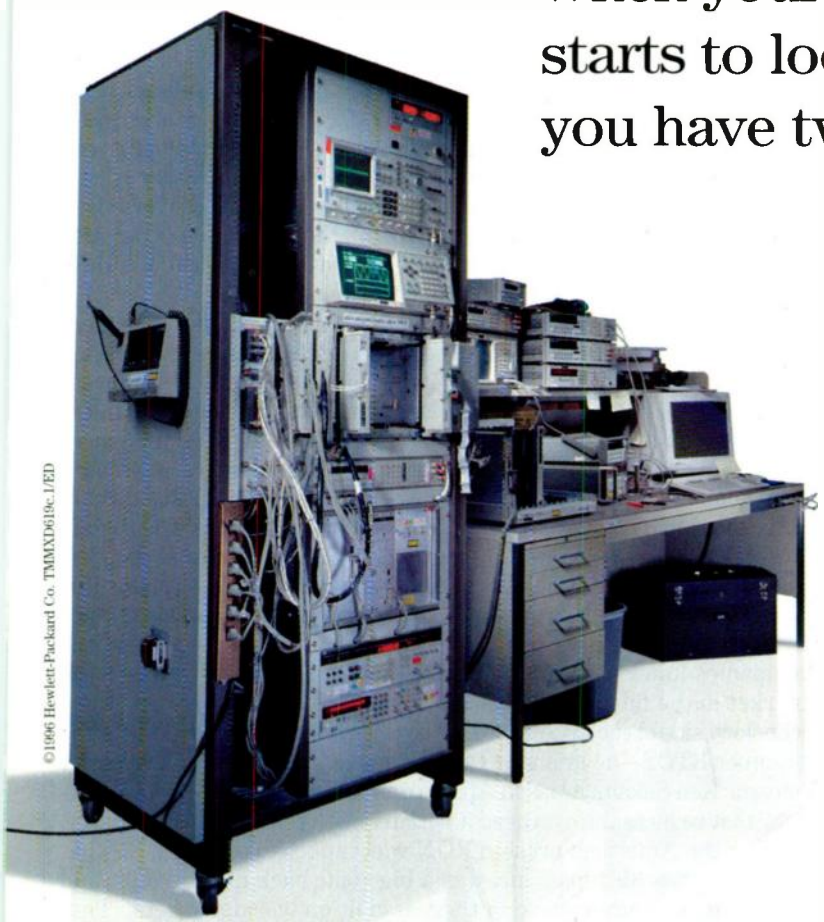
INTERMAG 97, Apr. 1-4. Hyatt Regency Hotel, New Orleans, LA. Contact John Nyenhuis, School of Electrical Engineering, Purdue University, West Lafayette, IN 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: nyenhuis@ecn.purdue.edu.

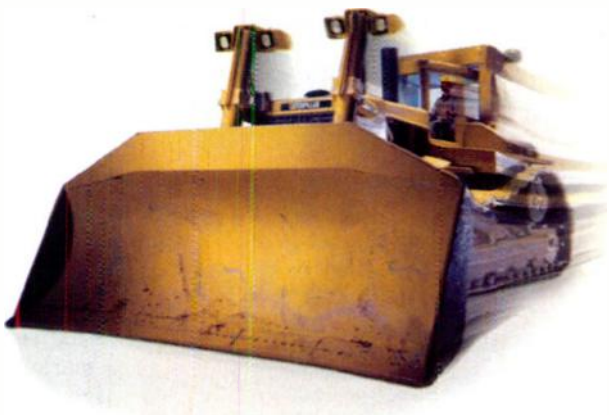
IEEE International Reliability Physics Symposium, April 7-10. Adams Mark Hotel, Denver, CO. Contact IRPS Publishing Services, P.O. Box 308, Westmoreland, NY 13490; (315) 339-3971; fax (315) 336-9134; e-mail: 103227.2074@compuserve.com.

IEEE Conference on Computer Communications (INFOCOM 97), April 7-11. Kobe, Japan. Contact Tatsuya Suda, Dept. of Information & Computer Science, University of California, Irvine, California 92717-3425; (714) 856-5474; fax (714) 856-4056; e-mail: suda@ics.uci.edu; Internet: http://www.ics.uci.edu/infocom/ (North America); http://arpeggio.ics.es.osaka-u.ac.jp/infocom.html (Japan).

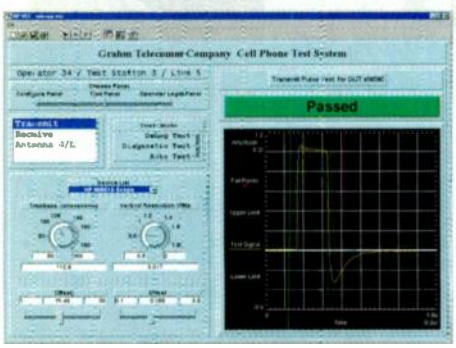
IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 97), Apr. 21-24. Gasteig Cultural and Convention Center, Munich, Germany. Contact Bernd Girod, Lehrst.f.Nachrichtentechnik, Univ. of Erlangen Nuremberg, Cauerstr. 7, D-91058 Erlangen, Germany; (49) 91-3185-7101; fax (49) 91-3131-30840; e-mail: b.girod@ieee.org.

When your test system starts to look like this, you have two options.





Here's one.



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READER SERVICE 123

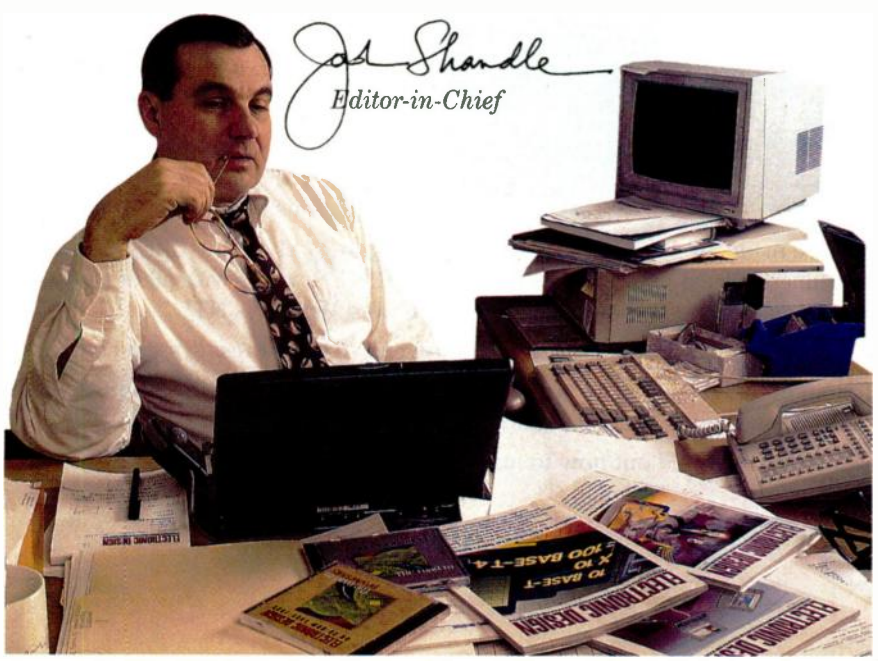
Son Of Tron

At least three Japanese consumer electronics giants are well down the road toward cooperating on at least a de facto software standard for running the ever more complex assortment of electronic appliances and gadgets. The standard may be a full-blown real-time operating system (RTOS) or simply an application programmers interface (API). Whatever it is, it will be a boon to consumers who are comfortable with the simplicity of operation that consumer appliances have offered over the past 40 years (with a few notable exceptions, such as setting a VCR's clock) and don't want to lose it.

Several interesting points can be made about this alliance. First, the clear indication that the long-awaited convergence of consumer, computer, and communications is upon us. One of the seldom-noted implications of convergence is that the interface consumers are likely to see will be more complex unless something drastic is done behind the scenes (in software) to keep appliances easy to use. The talk about a standard--and a software standard to boot--means that Japanese companies are diverging from their policy of the past 30 years that very little should be compatible with anything else. The idea was to gain market share by locking consumers into proprietary architectures and sell generation after generation of single use products (no upgrades). Finally, it is a significant challenge to the U.S.-dominated PC industry and to its software juggernaut, Microsoft. After watching the PC wars from the sidelines, the Japanese companies know that the only way they can hope to dominate the consumer market in the future is to elbow Microsoft out of it.

On the technology side of the issue, there are two home-grown contenders for the Japanese consumer RTOS—a variant of TRON, the 1984 brainchild of University of Tokyo Professor Ken Sakamuara, and Apertos, an RTOS built around an object-oriented center that reduces the overhead associated with remote file access.

As reported in the American press, TRON was supposed to be the OS that would take over the world. Japan Inc. was a big topic back in the 1980s, and TRON was treated as another wave in their assault on world markets. That was probably a misrepresentation. As I recall, there were three versions of TRON and only one—for microprocessors—failed. The version tailored for industrial automation and embedded systems is still around. Whether it will make it as an RTOS for consumer products remains to be seen, but it can't hurt to have 10 years experience under its belt. *jshandle@class.org*



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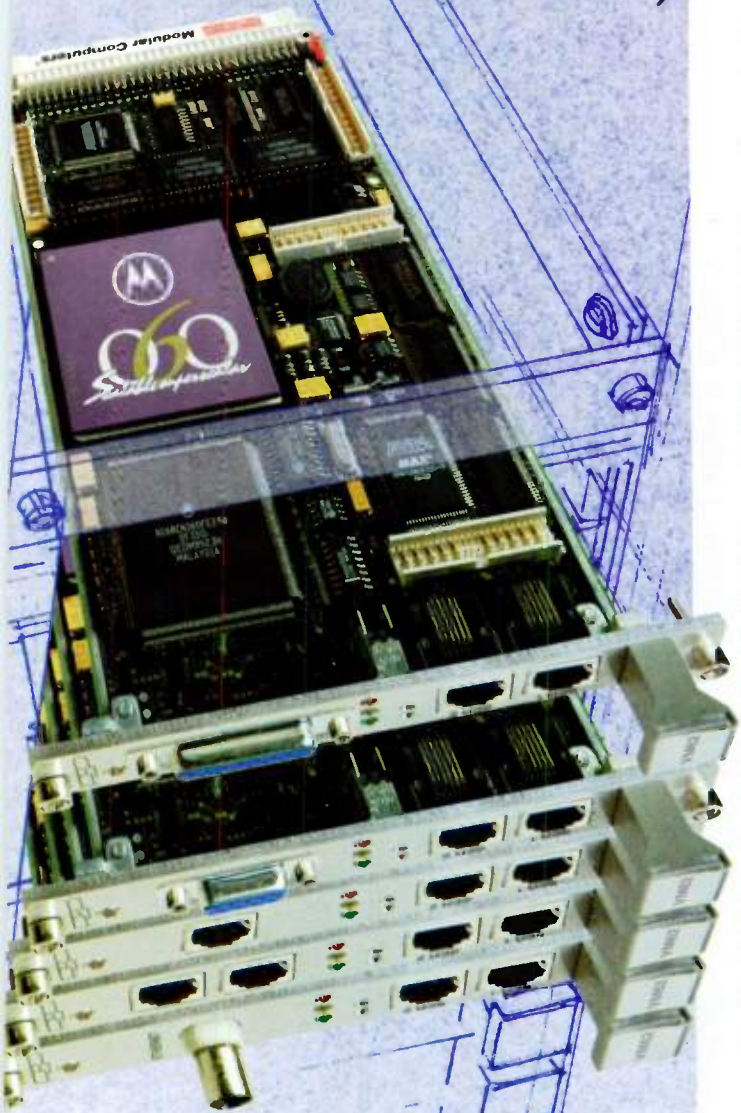

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AutoBahn Ready: Data transfer speeds up to 200 MBytes/second

CXC 96-Pin Mezzanine Interface: Choose from dozens of CXM I/O modules

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Software: RTOS support for OS-9, VxWorks, pSOS+ and VRTX/OS

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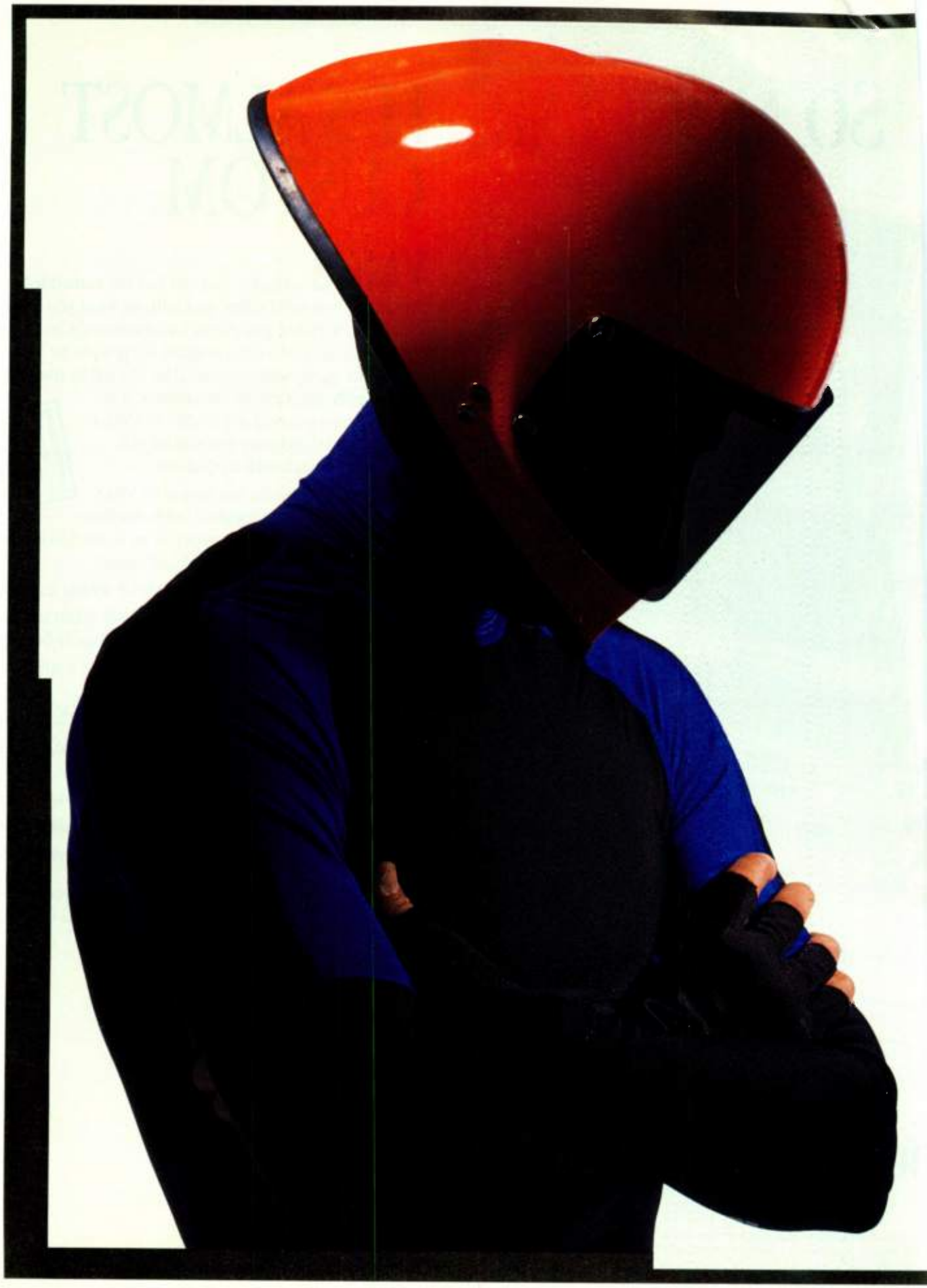

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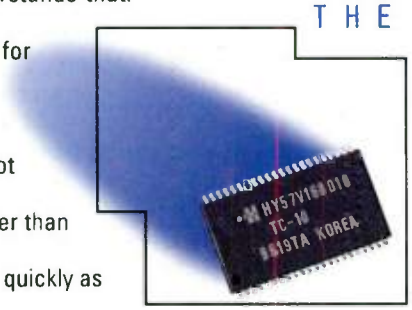
THE 16M SDRAM



Config.	Volt.	Speed	Refresh
4M x 4	3.3V	66/83/100MHz	4K
2M x 8	3.3V	66/83/100MHz	4K
1M x 16	3.3V	66/83/100MHz	4K

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READER SERVICE 125

WHAT'S REALLY GOING ON IN EDA?

As some of you may already know, I recently took over Lisa Maliniak's slot as the EDA editor at *Electronic Design*. Her shoes will indeed be difficult to fill, but I've thrown myself into it full force by taking on the formidable task of trying to talk to just about every EDA-associated company I can find. The result of this quest for understanding has left me inundated with huge amounts of disassociated information and to be honest, feeling an awful lot like a deer stuck in the glare of an oncoming car's headlights.

Thanks to conversations I've had with very knowledgeable people at some of the leading companies, the fog has finally lifted. I've been able to boil down all of this information into six points of interest that I believe will play an important role in shaping the industry as it moves into the 21st Century.

1. There are two distinct factions in the EDA industry. The first consists of companies who make tools for the cutting edge of technology. They are the "movers and the shakers," the ones who develop and introduce advanced technology that will significantly shape future design paradigms. The other faction is made up of those companies who work in the mainstream, developing tools for the everyday designer who isn't designing million-gate devices or high-speed boards—the designer for whom deep submicron might as well be an alien from another planet. The first faction represents technology that is "sexy," while the second targets the nuts and bolts of the day-to-day activity commonplace for today's designers.

CHERYL J. AJLUNI
WEST COAST EDITOR

2. The EDA marketplace is fiercely competitive. On the one hand, companies have to be competitive to maintain market shares. They do this by continually introducing new tools, upgrades to tools, and pushing the technological edge. But they also need to make a commitment to provide their customers with easy-to-use tools. The bottom line is that what most end users really want is a way to make the tools they are using more user-friendly and work well with a wide variety of point tools.

3. Design paradigms will have to change to accommodate deep-submicron designs (DSMs). Traditional design methods will no longer work since estimations and numerous iterations will not always converge on a solution.

4. No single company yet has a clear-cut solution to the DSM problem. While many are positioning themselves to provide a solution, as witnessed in part by the many company mergers and acquisitions of late, the truth is that no one is sure what company will come up with the solution that will show the most promise.

5. Intellectual property is not just a passing fad. It will define the way designers work in the future, and impact the type of designs they create, as well as the end products that end up in the hands of the consumers.

6. When the EDA industry began years ago, it was made up of about four companies. As it has matured, many more have joined the ranks. However, with all the mergers and acquisitions, one has to wonder if we aren't seeing a resurgence of an industry dominated by just a few companies.

Ultimately, I think what this means is the infusion of new life into an industry that in the past few years has not experienced a whole heck of a lot of change; in short, an EDA renaissance. 1997 promises to be a year of many challenges and changes in the EDA industry.

I'm sure many of you will have thoughts and insights on my comments. I think part of what will make these next few years exciting in the EDA industry is a fostering of communication between companies and end users who are the ones to truly drive any change. It is often said that the journey of a thousand miles begins with one step. For me, that means getting a handle on the EDA industry and I hope that my journey, of which you are all a part, will bring us closer to understanding how the tools and technologies of this industry can be utilized to bring about better designs. *cjajluni@class.org*

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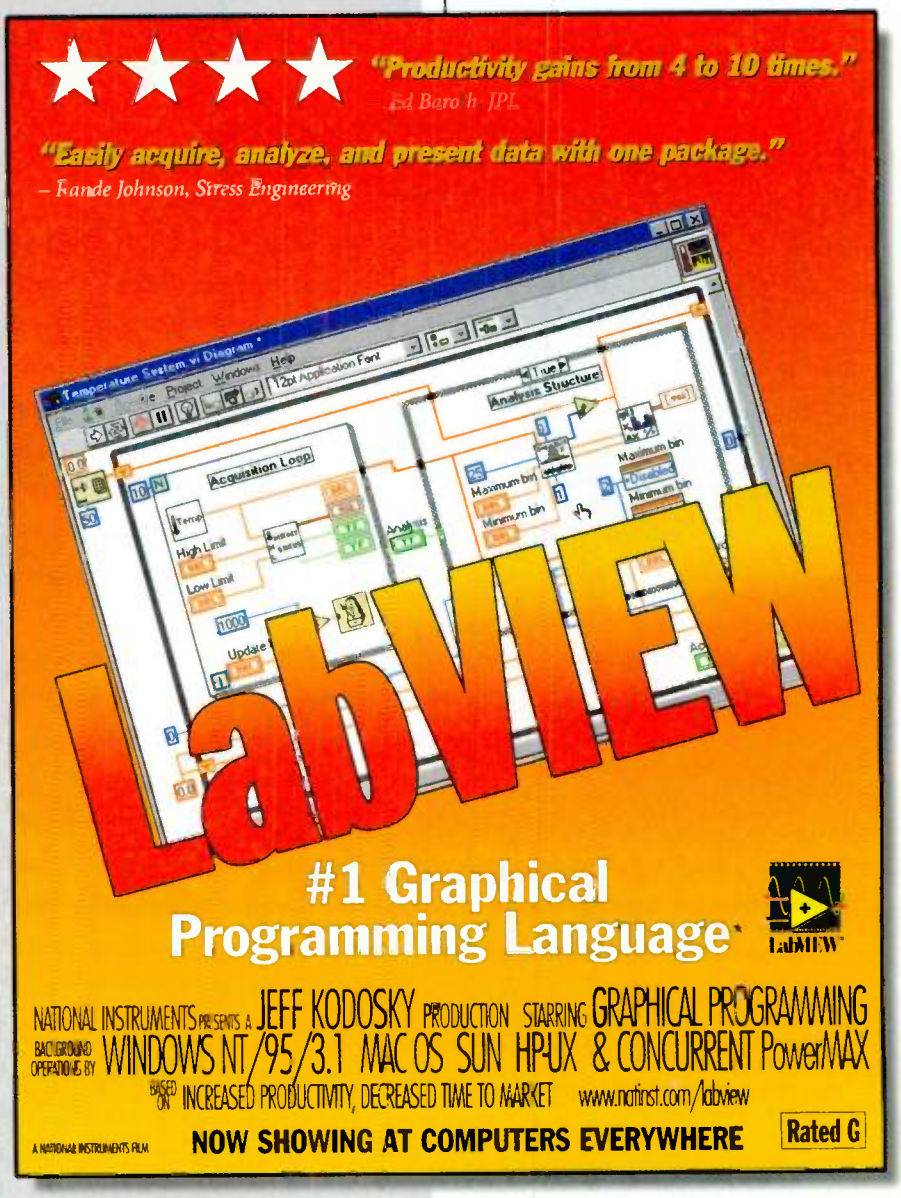

*As shown in T&M World Marketing Insight Study, 1995; Sensors Data Acquisition Survey, 1995; PE&IN Data Acquisition Survey, 1996

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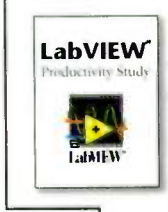

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50ns EDO DRAM AVAILABILITY CHART

DENSITY	ORGANIZATION	VOLTAGE	AVAILABILITY
DRAMs			
4 Meg	256K x 16	5V	Now
16 Meg	4 Meg x 4	5V/3.3V	Now
	2 Meg x 8	5V/3.3V	Now
	1 Meg x 16	5V/3.3V	4Q96
64 Meg	16 Meg x 4*	3.3V	4Q96
	8 Meg x 8*	3.3V	1Q97
DRAM MODULES			
8 Meg	2 Meg x 32	5V	Now
16 Meg	4 Meg x 32	5V	Now
	2 Meg x 64	3.3V	Now
32 Meg	4 Meg x 64	3.3V	Now
	4 Meg x 72	3.3V ECC	Now
64 Meg	8 Meg x 72	3.3V ECC	Now

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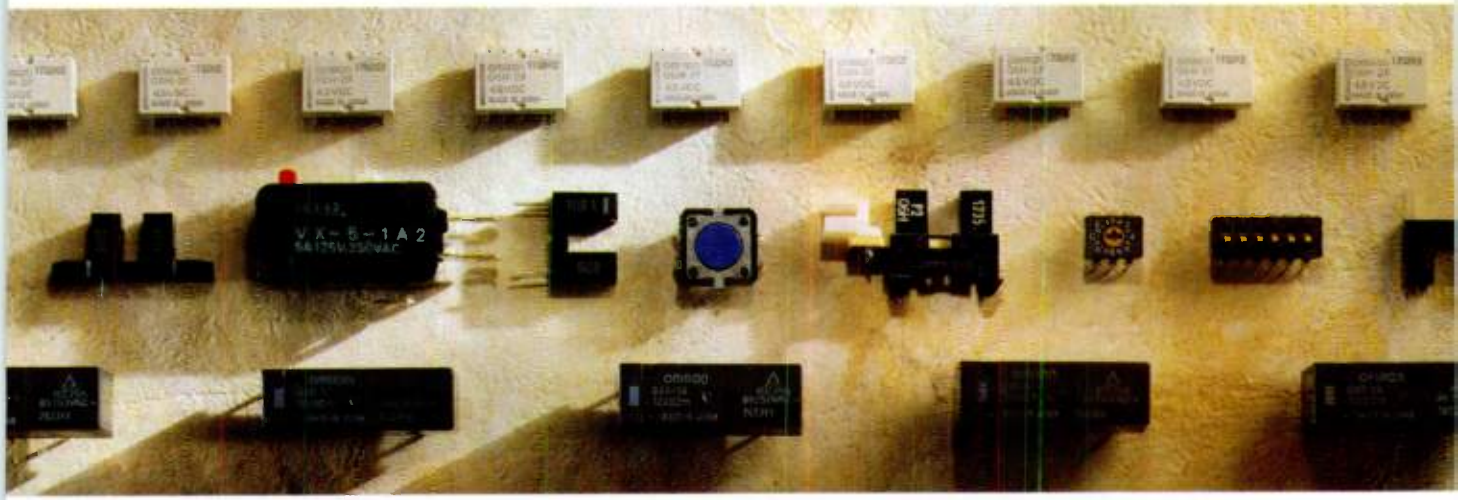

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DREAM TEAM

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TYPICAL GATES	TYPICAL GATES	TYPICAL GATES	TYPICAL GATES	TYPICAL GATES	TYPICAL GATES	TYPICAL GATES
10,000	20,000	30,000	40,000	50,000	70,000	100,000
USABLE GATES	USABLE GATES	USABLE GATES	USABLE GATES	USABLE GATES	USABLE GATES	USABLE GATES
7,000-31,000	15,000-63,000	22,000-69,000	23,000-93,000	34,000-116,000	46,000-118,000	62,000-158,000

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READER SERVICE 94

TECHNOLOGY NEWSLETTER

Algorithm Simulates Five Speakers With Just Two

Sound quality obviously is crucial when creating a home theater, and typically that requires multiple (five) speakers. But most users either don't want five speakers lying around their living room or they don't want to spend the money for them. An alternative developed by Spatializer Audio Laboratories Inc., Mountain View, Calif., involves a real-time processing algorithm that simulates the use of five speakers with just two. Called DVS-5.1, the technology enables Dolby AC-3 digital audio playback from two speakers or headphones. Developed on the Dolby-certified Motorola 56009 decoder, DVS-5.1 is suited for PCs or consumer electronics. It also can be ported to other processors, requiring about 5 to 15 MIPS of processing power for implementation and a memory requirement of under 1 kword. DVS-5.1 relies on a highly refined set of Head-Related Transfer Functions (HRTFs). Because the HRTFs vary from person to person, the algorithms were developed for the broadest user base. The DVS-5.1 processing immediately follows the AC-3 decoding, resulting in a two-channel signal that can be fed to a conventional stereo amplifier or speaker pair. For more information on the DVS-5.1 technology, contact Spatializer at (415) 428-0400. *RN*

Disk Drive Ups Spin Rate To 10,000 RPM

One way to boost a disk drive's performance is to increase the spin rate of the media. Mainstream drives spin at about 4500 to 5400 rpm, while the higher-end models could reach 7200 rpm. Seagate technology Inc., Scotts Valley, Calif., now pushes the envelope with a drive that spins at 10,000 rpm. the result is a faster access time and a higher transfer rate. The high-speed drives are part of the company's Cheetah family, which offer capacities of 4.55 and 9.1 Gbytes. With the high spindle speed, the internal data rate jumps to 15 Mbytes/s, about 40% higher than typical 7200-rpm drives. The average latency time falls under 3 ms. To accommodate the high transfer rates, the drives are built with UltraSCSI or Fibre Channel Arbitrated Loop (FC-AL) interfaces. Suitable applications for this technology include network file servers and professional multimedia systems. The 9.1-Gbyte drives fits a half-height form factor, while the 4.55-Gbyte model employs a low-profile form factor. For more information, contact the company at (408) 438-6550. *RN*

Laser Increases Possible DVD Capacity Threefold

While the last touches have been put on an agreement to enable the first DVD roll-outs this Christmas, Toshiba has been working on the next generation of development with the design of a 417-nm blue/purple laser source that can operate at room temperature. A pulsed version of such a laser, compared to the pulsed red laser (at 650 nm) of current designs, would increase the potential storage capacity of a standard DVD to 15 Gbytes per side. Also under development is a continuous-emission version of the source that would increase capacity even further. The new laser, which won't be ready for commercial launch without further refinement, uses gallium nitride (GaN). Toshiba claims it's more suitable for short wavelength beams than the current zinc-selenide materials. To get laser emission from a quantum-well structure, the company fabricates thin crystals using its own metal-organic chemical vapor deposition technology. This potential increase in capacity will make it practical for a DVD to hold full-length features in an HDTV format. *PMcG*

Semiconductor Laser Surgically Precise

By making several simple modifications to semiconductor lasers, researchers at the University of Rochester, N.Y., came up with a laser that's the power and precision demands of laser surgeons. Today, most laser surgery today is performed with costlier and less durable gas lasers because their semiconductor counterparts usually lack the power necessary for most surgery. Typically, the useful power output of semiconductor lasers is limited by the tendency of their beams to fragment into a number of parallel but weaker beams, known as "filamentation," which limits them for surgical purposes. The work done by the researchers essentially cleans up the beam produced by a semiconductor laser, creating a much more sharply focused beam. The new laser produces a unified beam no wider than a grain of sand, with the power efficiently packaged in the center. They did this by inserting two extra layers of slightly modified semiconducting material on either side of the active layer of gallium arsenide, where the beam is formed. Rochester researchers believe the new design makes possible semiconductor lasers with 6 to 12 W of power, two to four times as powerful as current devices. *RE*

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ISO 14001 Certification Gathers Momentum

Since its final approval in June of this year, the set of environmental guidelines developed by the International Standards Organization (ISO) has begun to find acceptance within the electronics manufacturing community. Titled ISO 14001, the standard was developed to enable a company to manage its environmental obligations and responsibilities much like the ISO 9001 standard implements management processes that raise quality awareness throughout an organization. It outlines a process of obtaining environmental certification that includes five major elements: a corporate environmental policy, planning activities, an implementation strategy, an auditing program, and a management review. Besides pollution reduction, ISO 14001 requires that companies commit to actively prevent pollution as it designs new products and processes, rather than simply cleaning up after the fact.

Acceptance has come faster in Europe and Asia, with companies like SGS Thomson, Canon, and Nippon Steel being among the first to achieve certification of compliance to the draft standard—even before it won final approval. European firms operating within America are setting an example for their competitors, with SGS Thomson having the first ISO 14001-certified operation in the U.S. at its wafer fab in San Bernadino, Calif. Inroads are being made in the U.S., however, with such firms as Eastman Kodak and National Semiconductor pursuing certification for some or all of their facilities. One of latest to achieve full ISO 14001 status is the Schurter Corporation. Based in Lucerne, Switzerland, and Eindigen, Germany, Schurter makes circuit protection and power conservation devices. To learn more about the ISO certification process, or Schurter's experience with it, contact Joseph Hamilton at (800) 848-2600, ext. 223; fax (707) 778-6401, e- mail: 73024.2314@compuserve.com, or http://www.schurterinc.com. *LG*

Battery, IC Makers Promote Smart-Battery Standard

A group of battery and semiconductor manufacturers have banded together to develop and share ownership in the Smart Battery System (SBS) specification. A smart rechargeable battery contains a microprocessor to accurately report its remaining capacity, as well as other information that helps increase the battery's life. Such batteries, which are currently employed in a host of notebook computers, will migrate to other portable devices, such as camcorders, video games, and PDAs. The ten companies involved include Benchmarq Microelectronics, Duracell, Energizer Power Systems, Intel, Linear Technology, Maxim, Mitsubishi, National Semiconductor, Toshiba Battery Company, and Varta. Microsoft also is supporting the SBS standard and will ship smart-battery drivers that comply with the standard in upcoming operating-system releases. The current release of the SBS specification can be implemented in standard-size or custom battery packs. The standard is downloadable from the Internet at http://www.mediacity.com/~sbs. *RN*

ITU Approval Speeds Up V.34 Modem Standard

The International Telecommunications Union (ITU) has approved an amendment to the V.34 modem standard allowing data rates up to 33,600 bits/s. The amended standard was accepted at the World Telecommunication Standardization Committee (WTSC), which convenes every four years from work done by Study Group 14 of the ITU's Telecommunications Standardization Sector, under the guidance of Richard Brandt of Motorola. The acceptance gives the go-ahead for equipment manufacturers to start the delivery of new products. Line "probing", the ability to seek lower data rates based on telephone line quality, is retained in the new version. There's also support for a half-duplex mode for fax and auto-moding in existing V-series modems. The auxiliary channel, which features a synchronous data-signaling rate of 200 bits/s, is intended to convey modem control data. Identifying the remote modem leads to shorter connect times, and the multi-dimension trellis coding has a high immunity to telephone line noise and impairments. The new standard is available from the ITU sales service at a cost of SFR 29. They may be contacted at +41 22 730 6141; or through their Web site at http://www.itu.ch. *PMcG*

Edited by Roger Engelke

New Product Update

Analog Front End Chip for HDSL/MDSL Systems

AFE1103, **AFE1104**, and **AFE1105** are the first members of a family of Analog Front Ends (AFEs)—these single-chip solutions greatly reduce the size, cost and power requirements of an E1/T1 rate HDSL or MDSL system by providing the active mixed signal circuitry needed to connect an HDSL digital signal processor to the existing telephone company's twisted pair infrastructure. Designed for HDSL systems from PairGain Technologies, Brooktree, and Metalink, they feature a scaleable data rate to allow operation over a range of 196kbps to 1.168Mbps. Their transmit and receive filter responses change automatically with clock frequency. Each device is composed of transmit and receive sections. Applications for HDSL systems with these AFE chips include Internet access, T1/E1 transmission, MDSL, wireless base stations, network switches, routers, and internet-working. Key specs are: scaleable data rate, 250mW dissipation, and +5V single power supply. Packaged in a 48-pin SSOP and priced from **$13.40** in 10,000s.

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12- & 16-Bit Sampling A/Ds with 4-Channel Multiplexer

ADS7824 and **ADS7825** are low power, monolithic 12- and 16-bit sampling A/Ds with 4-channel input multiplexer and a parallel/serial output µprocessor interface. Both can be configured in a continuous conversion mode to sequentially digitize all four channels—ideal for industrial process control, and test & measurement. Key specs: ±2 LSB max INL (ADS7825), 0.5LSB max INL (ADS7824), 16 bits DNL no missing codes, single +5V supply, and 50µW power down mode. Available in a 28-pin 0.3" DIP or 28-lead SOIC. **ADS7824** is priced from **$12.30** in 1000s; **ADS7825** from **$34.50**.

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12- & 16-Bit, 100kHz Sampling A/Ds with 0-5V Analog Input Range

ADS7820 and **ADS7821** are 12- and 16-bit, 100kHz sampling A/Ds. Their 0 to 5V input range, combined with single 5V supply, make them ideal for industrial process control, test and measurement, and analytical instrumentation applications. ADS7820 key specs: 72dB SINAD with 45kHz input, and ±1/2 LSB INL/DNL. ADS7821 key specs: 86dB SINAD with 20kHz input, ±3 LSB max INL, and no missing codes. Available in a 28-pin 0.3" DIP or 28-lead SOIC. ADS7820 is priced from **$10.25** in 1000s; ADS7821 from **$28.70**.

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DCP010505 is the first in a series of high efficiency, 5V input isolated DC/DC converters in industry standard JEDEC plastic molded packages. It can be assembled in high volume using standard processing and handling—no special reflow soldering processing required. Use it for point-of-use power conversion, digital interface power, ground loop elimination, data acquisition, and industrial control/instrumentation applications. Key specs: 1W power output at +100°C, 70% efficiency at full load, 1000Vrms isolation, and 400kHz switching. Packaged in a 14-pin DIP and priced from **$5.01** in 1000s.

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New SoundPLUS Low Cost Stereo Audio D/A

PCM1720 is a **Sound***PLUS*, low cost stereo audio D/A complete with 3rd-order ΔΣ modulator, digital interpolation filter, and an analog output amplifier. It accept 16- 20-, or 24-bit input data in either normal or I²S formats, and operates at sampling frequency up to 96kHz. Key specs: 256fs or 384fs system clock, single +5V power supply, multiple sampling frequencies, and left, right, mono, mute output modes. Packaged in a small 20-pin SSOP (fine lead pitch) and priced from **$3.30** in 1000s.

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PERSONAL COMMUNICATIONS CONFERENCE EXPLORES ATM, IP, AND FILTERING AND EQUALIZATION TECHNIQUES

The IEEE's fifth annual International Universal Personal Communications Conference (ICUPC) revalidated the old adage that behind every overnight technical revolution lies years of hard work. This chestnut is especially true in the case of the rapidly exploding world of personal communications. The area of personal communications relies heavily on advanced theoretical work in a variety of fields for the technology that will drive its future networks. Participants at the conference, held between Sept. 29 and Oct. 2, in Boston, Mass., wrestled with many of the most difficult issues that engineers will face when they get ready to roll out the next generation of communication networks.

While today's cellular, pager, personal communication system (PCS), and other wireless networks are making anytime/anywhere communications easier than ever, they still have limitations. The lack of integrated communications services often requires people to carry three, four, or more devices with them today, and global roaming is still only a dream for wireless telephone providers. Additionally, current personal communication systems do not have the bandwidth to provide highly desirable multimedia services. At ICUPC, solutions were explored in workshops and technical sessions, which covered a wide array of topics ranging from network-theory, traffic-management protocols, and smart antennas, to advanced filtering and equalization techniques.

Some of the hottest areas of discussion centered around wireless asynchronous-transfer-mode (ATM) and IP-based data, for both local-area and wide-area applications. One of the most significant challenges faced in developing wireless ATM is maintaining its connection-oriented virtual paths and virtual circuits (VPs/VCs) in an RF environment, while the terminals are handed off between base stations. One of the papers on this topic was "Virtual trees routing protocol for a wireless ATM LAN," by Irene Katzela of Columbia University, New York, N.Y., and Malathi Veeraraghavan of Bell Labs, Murray Hill, N.J. They discuss a new routing algorithm which simplifies hand-offs between base stations by reestablishing a set of virtual-path-identifier (VPI) trees, associated with each node in the LAN. While it does not precisely follow the general routing scheme prescribed by ATM, the algorithm greatly reduces the management load, when combined with a distributed routing protocol. It dynamically updates the routes of the VPI trees in response to repeated congestion or changes in network topology.

The problems surrounding the design of media-access-control (MAC) protocols for wireless ATM communications also drew significant attention. MAC protocols are a special concern in the ATM arena, since they provide many classes of service, many with guaranteed bit rates and demanding quality-of-service parameters.

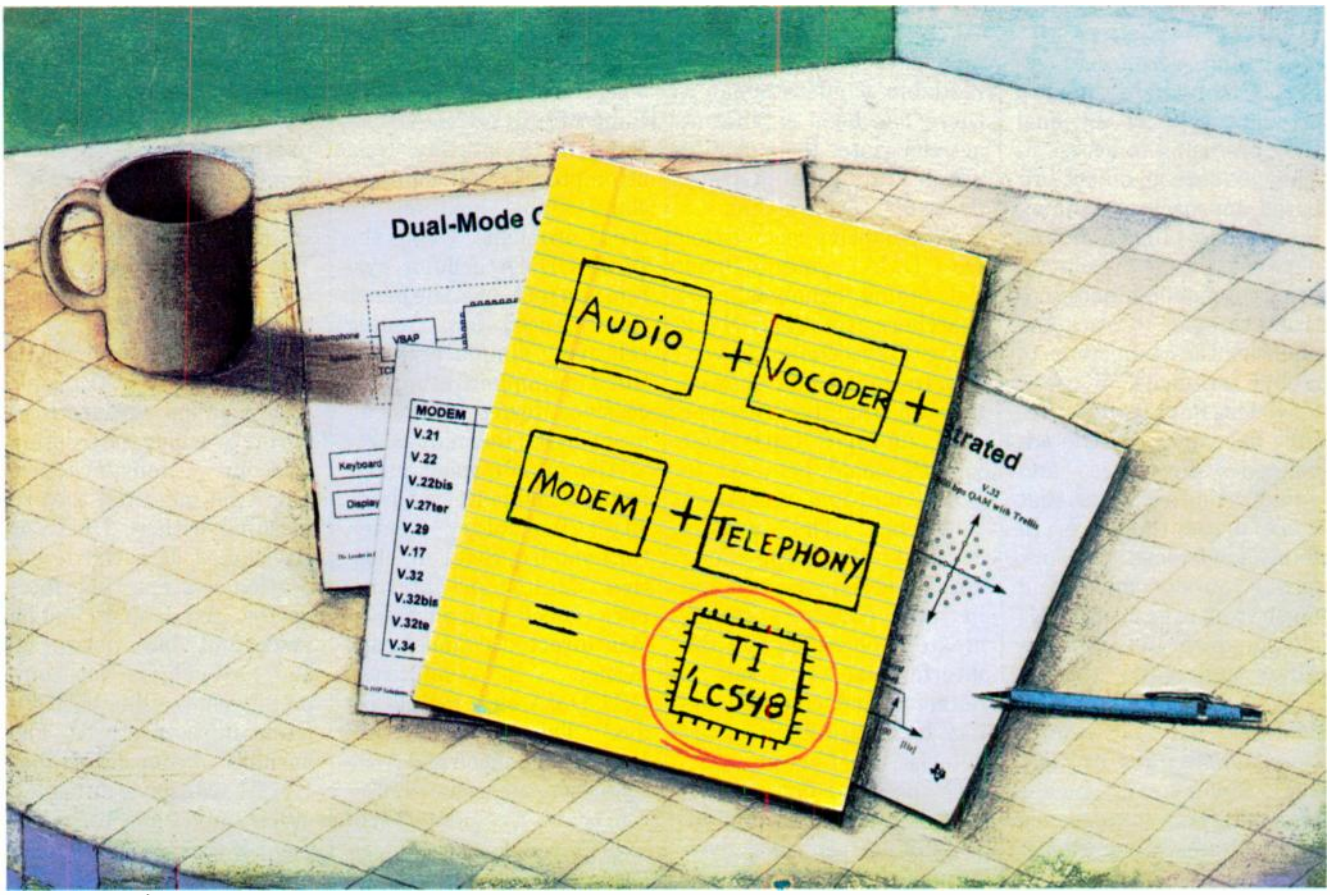
In Session 5A, Jyh-Cheng Chen from the State University of New York at Buffalo, and his collaborators from other universities presented "A framework for comparative analysis of channel access protocols for wireless ATM networks." Their concern was to develop some objective means of evaluating the efficiency, technical requirements, and robustness of MACs without needing to construct an entire test network. The paper presented a preliminary comparison of several proposed protocols, as well as the results of system simulations.

While much attention was focused on the subject of ATM, Session 10A addressed the fine points of implementing IP-based wireless data systems. There was a great deal of theoretical work involving hand-off control and network management. Some of the first real-world results from trials of early wireless data networks also began to trickle in.

In the paper "Trials of mobile computing applications using circuit-switched cellular and CDPD," Nina Nour, of the Mitre Corp., Bedford, Mass., actually evaluated the performance of a number of wireless services and technologies. The paper describes several demonstrations that were conducted, including wireless e-mail using both circuit-switched and cellular digital packet data (CDPD), as well as Internet access using CDPD. In presenting the trials in great detail, it documents both the good and bad results, yielding many valuable lessons for the design of future services.

One of the major issues in providing mobile computing services (such as wireless Internet access) is developing the connection management protocols to allow the seamless flow of data traffic between the Internet, the PSTN, and the many wireless services that are emerging. In their presentation "Mobile computing on wireless telecommunications networks," researchers Hiromi Wada and Hideaki Fukushima of Matsushita Electric's Multimedia Development Center, Tokyo, Japan, discussed a mobility support architecture (MSA). The MSA was conceived as an efficient means of connecting mobile IP nodes to the Internet over a wireless telecommunication network. Their work shows how MSA cooperates with the route optimization mechanism that was developed by the Internet Engineering Task Force (IETF) to provide optimal routing for IP traffic with a minimum amount of management overhead. In addition to a detailed architectural analysis, the paper also documents a performance analysis study performed on a prototype system that was developed by the authors.

The paper "A framework for universal personal computing," by Yalun Li and Victor Leung from the University of British Columbia, Vancouver, Canada, also was of significant interest to the IP community. In it, they discuss the demands placed on a "mobile computing-oriented" network that provides its users with the same personalized environ-



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08 1893

ment and resources, regardless of where they are or what type of terminal they are using to access it. They explore an object-oriented approach to defining the mobile objects in the network, and present a group of mobile-object control strategies to track and maintain the connections to mobile terminals.

No less important for future networks are the advanced filtering and equalization schemes that were presented here. In today's wireless systems, fading, outside noise, and noise from other terminals all conspire to limit the range and signal quality that's available. Future systems will face additional challenges as they use lower-level power transmitters, experience higher subscriber densities, and are asked to operate in very unpredictable indoor environments.

A significant portion of the activity in this area is devoted to improving the performance of systems using code-division multiple-access (CDMA) techniques. CDMA has gotten more attention in the past few years, thanks to its potential for high channel capacity and high noise immunity.

One of the unique problems that CDMA systems face is that of multiple access interference (MAI)—a result of the fact that CDMA allows many transmitters to be operating simultaneously on the same wideband channel. While CDMA's code-division scheme allows a receiver to pick out the desired transmitter from the others, all the radio activity does raise the channel's noise level. With enough traffic, the noise level can significantly degrade the bit-error ratio, or even make a signal unreadable. Understandably, there has been significant activity into technologies which can help CDMA overcome this problem.

In "Adaptive receiver for DS-CDMA systems over flat fading channels," researchers from The Hong Kong Polytechnic University, In Hong Kong, showed how an adaptive receiver with multiple tap-weight vectors could be used to cancel multiple access interference. The authors contend that the long spreading sequences, found in most CDMA systems, create a periodicity in the interference which can be detected and canceled using the digital filter's characteristics. System performance over flat and fading channels is evaluated. To further enhance performance, the team experimented successfully with a scheme that decodes the spreading code and uses the known bit sequence to lock onto the signal and further tune the filter's tap-weighting.

Another method of improving CDMA system performance is the use of multistage or successive-interference-cancellation techniques, whereby a single receiver is used to extract multiple user signals, using successive passes. Until now, there have been concerns about both the complexity of these kinds of receivers (impacting development time and production cost) and what the effect of slight-tolerance variations in receiver functions (quantization and tracking), might have on overall system performance.

In their presentation, "Practical implications of successive interference cancellation in DS/CDMA systems," Klaus Pedersen and others from the Wireless Information Network Laboratory (WINLAB) located in Piscataway, N.J., attempted to find commercially viable solutions to these problems. Using the IS-95 CDMA cellular system as a test case, the paper concentrated on finding relatively simple architectures for implementing successive interference cancellation (SIC) techniques.

Also of note was a paper from Chalmers University's Technology Center, Gothenburg, Sweden, entitled "Multistage interference cancellation with decision directed channel estimation in multirate DS/CDMA on a mobile radio." The authors, Ann-Louise Johannson and Arne Svensson, describe a system that is a combination of hybrid interference cancellation and decision-directed channel estimation technologies. It is used to enhance the performance of a multirate data transmission system which communicates over multiple radio channels. One unique aspect of this approach is that it actually uses dissimilar signal strengths from transmitters as a part of the detection process. If it is validated and accepted by the wireless community, there are several important ideas in this paper which could change the face of wireless systems over the next decade.

The dream of most technologists is to have a unified wireless communications system that carries everything from low-rate messaging to real-time video across a single, seamless network. This vision is taken very seriously at ICUPC, and a number of sessions explored possible infrastructures and migration scenarios. One of the more interesting papers, entitled "Evolution scenarios towards UMTS," was presented by researchers from the Telefonica I+D, Madrid, Spain, and DeTeBerkom, Berlin, Germany. The authors describe the Universal Mobile Telecommunications System (UMTS), currently under development in Europe, and examine various scenarios by which the existing telecom infrastructure might be migrated toward meshing with it. UMTS is envisioned as a third-generation system that integrates fixed and mobile voice and data networks, and as such, is not completely compatible with existing infrastructures. The authors contend that UMTS will have difficulty, or be impossible to implement if it requires a "forklift" roll-out scenario. Instead, they look for areas in which UMTS can co-exist with, or borrow from existing infrastructures, and build a new tier of services above it. Scenarios involving everything from using DECT/CT2 cordless telephone technology and the GSM network, to piggybacking the wired backbone onto cable television systems are explored.

The ICUPC '96 allowed those responsible for envisioning the next generation of wireless systems to come together, exchange ideas, and collaborate on their visions of the future. It gave the rest of us a glimpse into the technologies we will be using into the next century. For those interested in the future of wireless systems, the complete proceedings of the 1996 ICUPC conference is available from the IEEE (catalog #96TH8185) for $84 for IEEE members and $168 for non-members.

LEE GOLDBERG

FLASH-MEMORY METHOD DOUBLES STORAGE DENSITY, BUT TAKES UP ONLY 10% MORE AREA

A joint development from Matsushita Electronic Corp., Japan, and SanDisk Corp., Sunnyvale, Calif., has allowed densities of flash-memory devices to be doubled. The Double Density Flash technology is capable of producing 300-Mbyte PC Cards using 64-Mbit chips. The ICs will be manufactured on a 0.5-μm CMOS process. They are expected to ship by the end of the year.

Memory capacity is doubled because the Double Density technology enables the storage of two data bits in each flash cell, rather than the one-bit-per-cell style that's used on today's flash devices. This technique causes an increase in chip size of about 10% to accommodate the extra circuitry.

A second trade-off made for the higher densities comes in the chip's write speed. The Double Density Flash offers a write speed that's significantly slower than the speed of SanDisk's current flash products. The slow speed is due to the additional time required to program each cell to one of four distinct states, rather than one of two states employed by other flash devices.

On the other hand, memory read speed is about 50% faster than current products. Reads are based on a multi-state concurrent sensing implementation. The data that's stored within each memory cell is simultaneously sensed in a single-pass read operation. This technique is combined with a stream-read (pipelining) protocol, during which time the next piece of data is being sensed while the previous piece is serially shifted out of the controller. In addition, the output bus width has been doubled from two to four pins.

In addition to being intrinsically small and highly scalable, the SanDisk flash cell has a number of fundamental advantages over the main alternative flash approaches in production today. These include reliability, functionality, and production worthiness.

The new technique avoids the use of the ultrathin 100-Å or thinner oxides employed in other flash-memory technologies. By using a thicker-oxide, polysilicon-to-polysilicon tunneling structure, any data-retention reliability problems caused by the thinner oxides are avoided.

The use of a split-channel NOR cell also does not limit cell functionality by either by overerasing (as is the case with Intel's ETOX cell) or overprogramming (as is the case for Toshiba's NAND cell). Without such constraints, the cell offers a wider window of memory cell operation, an essential element in realizing a func-

tional, competitively performing multistate product.

Innovative design concepts, spanning both memory chip and controller/system design also have been essential elements in realizing a production-worthy Double Density Flash memory. For example, the chip incorporates parallel architecture and operation for ease of use, as well as multistate programming and reads. Erasing is performed at the sector level, wherein one or more sectors are selectable for simultaneous erasures, as required by the user. Erasures are automatically executed by the controller.

The 64-Mbit chip supports a shift-clock frequency of up to 20 MHz, corresponding to a 10-Mbyte/s transfer rate to the controller. The controller employed by the Double Density products was designed by SanDisk Corp. It contains newly developed algorithms, tailored to the Double Density 64-Mbit memory chips. The algorithms also incorporate error-correction codes and bit mapping.

The novel Double Density Flash memory operates from a 3.3- or 5-V power supply. For more information, contact SanDisk at (408) 542-0500.

RICHARD NASS

THE MICROPROCESSOR: 25 YEARS YOUNG AND THE BEST IS STILL AHEAD

It's hard to believe in this day of short-lived product cycles that the microprocessor has hit a major milestone—25 years of market proliferation in a myriad of variations from 4- to 64-bit word sizes and architectures. Although Intel Corp.'s Marcian "Ted" Hoff, an engineer there in the early 1970s, and Masatoshi Shima, an engineer for Busicom, a Japanese calculator manufacturer, are credited with developing the first microprocessor, they could not have envisioned the impact that the concept would have a quarter century in the future.

Today, there's hardly a home appliance or piece of consumer electronics that doesn't contain a microprocessor in one form or another. Similarly for office automation products from fax machines to copiers, and from automobiles to aircraft. The use of the microprocessor has become ubiquitous, with every technical school offering multiple courses relating to the design and programming of the chips and systems.

Today, there's hardly a home appliance or piece of consumer electronics that doesn't contain a microprocessor in one form or another. This also holds true for office automation products from fax machines to copiers, and from automobiles to aircraft. The use of the microprocessor has become ubiquitous, with every technical school offering multiple courses relating to the design and programming of the chips and systems.

When the 4004 was released in 1971, it took several years for system designers to understand and accept the premise that such chips could replace hardwired logic. And, through the development of the 8008, the industry was still on a steep learning curve to understand programming concepts that most designers today take for granted. However, it wasn't until the era of the 8080 in 1974 when many other companies, like Motorola Inc., Austin, Texas, with its 8-bit 6800 family, jumped onto the bandwagon. That's when the microprocessor market started to realistically develop.

Fig. 3. 8088 microprocessor

Today, the market for microprocessors totals about $17 billion, according to Dataquest Inc., San Jose, Calif., a market research company. Most of that is due to the use of such chips in desktop and portable computers, products that did not exist until the mid-1970s when MITS

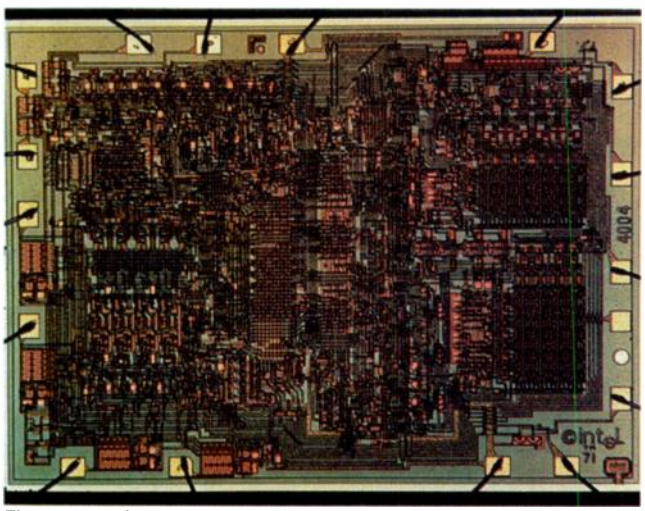

Fig. 1. 4004 microprocessor

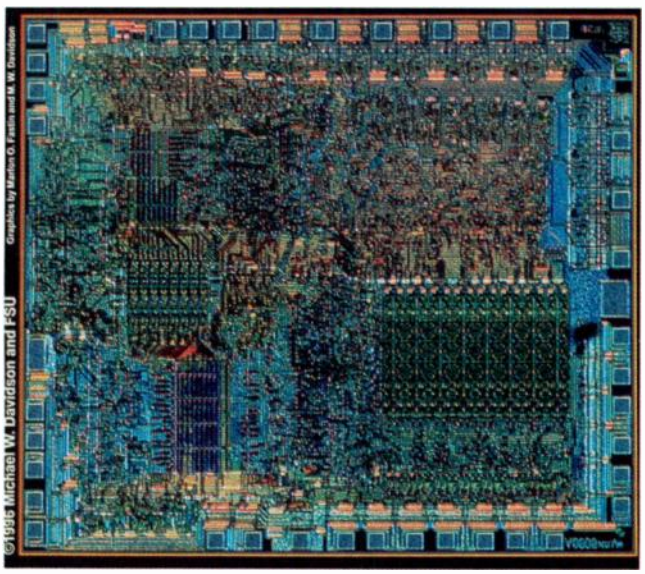

Fig. 2. 8080 microprocessor

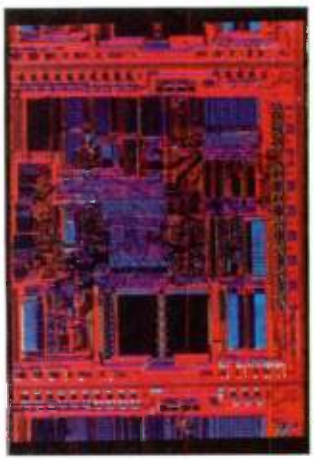

Fig. 4. 80286 microprocessor

Inc., Albuquerque, N.M., introduced a computer kit based on the 8-bit Intel 8080, and Apple Computer Inc., Cupertino, Calif., built the Apple II, the first consumer-class personal computer that was based on the 6502 8-bit microprocessor.

With an estimated compound annual growth of about 18% over the next four years, Dataquest estimates that the market will virtually double to $33 billion by the turn of the century. And again, most of that market will be driven by the huge quantities of personal computers that are expected to reach user's desks. In addition, the market for just the "embedded" microprocessors is currently estimated at about $2 billion, and that will grow by 50% to roughly $3 billion by the end of the century.

Although the 4004 microprocessor, when it was released in 1971, was the first chip to pull all the compute features together, there were other programmable solutions emerging in the form of a microprogrammable bit-slice architecture known as the PPS-4 developed by Rockwell Corp., Newport Beach, Calif. The PPS series provided designers with a means to define a processor from the instruction set to the system-word width in small building blocks. And although it was flexible, it required tremendous expertise to develop the underlying programming.

Fig. 5. 80386 microprocessor

The approaches in the early 1970s thus had system designers split between using the CPU on a chip approach from Intel—which progressed from the 4004 to the 8-bit 8008 and in the mid-1970s, to the 8080—and the bit-slice microprogrammed approaches of the early 1970s—the 4-bit PPS-4 which progressed to the 8-bit PPS-8. Those early PMOS bit slices were eventually superseded by bipolar bit slices such as the 2901 developed by Advanced Micro Devices Inc., Sunnyvale, Calif., and the 74S888 series from Texas Instruments Inc., Dallas, Texas. The bit slices, due to their high power consumption and complex

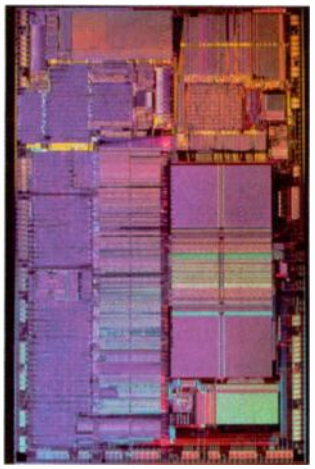

Fig. 6. 80486 microprocessor

programming, ended up being used in high-performance minicomputer systems and other applications that demanded top throughputs.

In the pre-8080 days, Intel was the only "integrated" solution, squeezing about 2300 transistors onto the CPU chip" a quantity of transistors that today would be hard-pressed to implement even a significant peripheral support function. In contrast, today's CPUs like the Pentium-Pro pack more than 2000 times that number—5.5 million transistors *(see Figures 1 through 8 that show the progression of the microprocessors that came from Intel through eight generations—the 4004, the 8080, the 8088, the 80286, the 80386, the 80486, the Pentium, and the Pentium-Pro).*

When NMOS processing was first employed in the mid-1970s, it allowed for significant density and performance improvements over the initial PMOS processes used by the 4004. Those improvements allowed many companies to develop competitive solutions to the 8080. Motorola Inc., Austin, Texas, crafted the 6800 family, and other companies at that time developed their own 8-bit families of microprocessors. Those other companies included MOS Technology with the 6502, National Semiconductor with the SC/MP, RCA with the 1802, Rockwell with an offshoot of the 6502, Signetics with the 2650, and Zilog with its Z80.

A few of these companies and products are still around today in various forms. Motorola has grown the 6800 into several generations of microcontrollers and 16- and 32-bit CPUs and MCUs *(Fig. 9)*. Several microcontroller suppliers offer 6502-based MCUs. An ASIC megacell of the 6502 core also is available, and the Z80 survives in many industrial applications and as a megacell for custom controller designs.

Over the years since the 8080 and 6800 were introduced, microprocessors have evolved and have spun out many varieties that range from complete single-chip solutions called microcontrollers that sell for less than $0.50 apiece in large volumes to the equivalent of supercomputers on a chip that pack millions of transistors and sell for about $1500 per chip. For general-purpose computing, the complex-instruction-set architectures have given way to reduced-instruction set approaches, which promise higher throughputs through simpler data-path structures and streamlined instruction sets.

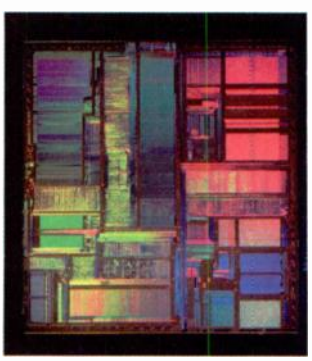

Fig. 7. Pentium microprocessor

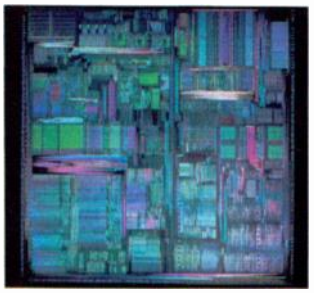

Fig. 8. Pentium-Pro microprocessor

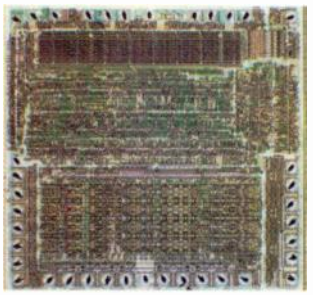

Fig. 9. MC6800 microprocessor

Microprocessor innovation has also spawned additional branches on the evolutionary tree—digital signal processors, for example, are very similar to microcontrollers or microprocessors. The main differences with DSP chips include their ability to perform multiplications and multiply-and-accumulate (MAC) operations much faster than the CISC processors they were designed to assist. Additionally, the DSP chips were able to execute instructions very quickly since in a sense, the first DSPs were a precursor to the overall definition of a RISC chip, except with a more focused instruction set.

However, with today's ability to reduce the size of the CPU logic, integrate millions of gates, and piece together various functions on a single chip, it is getting harder to justify generic DSP chips. More common now are processors that offer merged architectures, combining the best of RISC and DSP on a single chip.

Alternately, dedicated digital-signal processing chips are taking on more vertical and complex applications, such as MPEG1 and 2 encoding and decoding. There also various versions designed to tackle JPEG processing.

Has the microprocessor reached the end of its evolution? Not by a long shot. There are still many architectural enhancements, process improvements, and novel features that can be added to craft the next generations of CPUs. What features/changes might be seen? That's a bit harder to predict since as the CPUs evolve, they tend to become more market-specific.

CPUs for the personal computer market are adding large amounts of memory for caching, graphics, and multimedia functions to enhance their ability to handle video and audio information. They're also adding important power-management features to reduce power-consumption levels.

There are also processors for other markets. These may focus on other features like real-time control support, direct drives forLCD panels, high-resolution analog-to-digital and digital-to-analog converters (ADCs and DACs), and many other new functions.

What do you, the readers, think should be implemented? Send your suggestions via my e-mail address to dbursky@class.org and a wish list will be compiled and published in early 1997.

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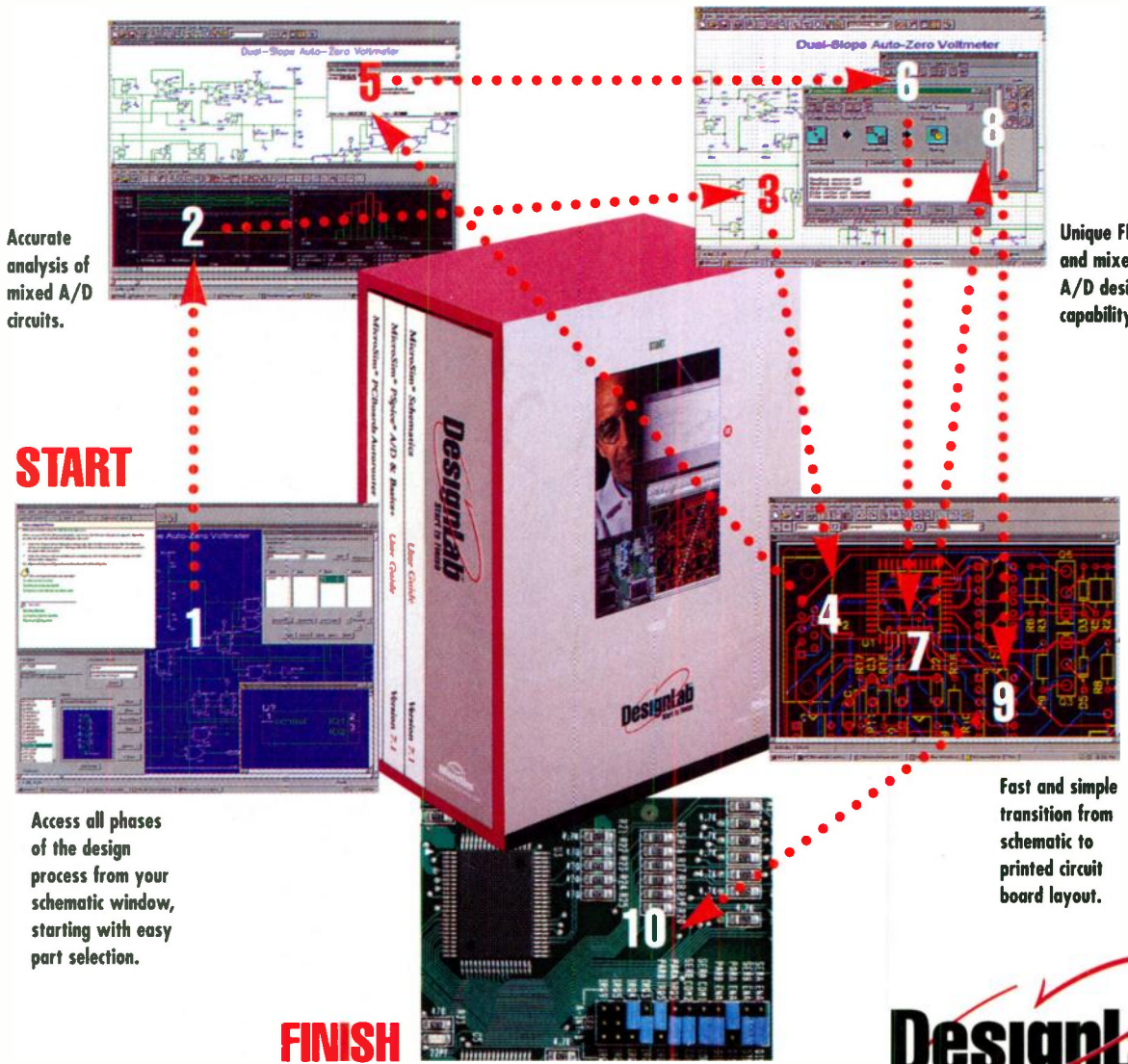

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Annual IEDM Conference Previews Cutting-Edge Device Developments

New Processes For Analog, Digital, And Mixed-Signal Devices, And The Latest Developments In Device Modeling And Simulation, Are On The Agenda.

What will the next generation of sensors, detectors, laser diodes, power and communications ICs, memories, and modeling and simulation tools be like? That's what the annual 1996 International Electron Devices Meeting will attempt to answer. The 35-session conference will take place Dec. 8-11, at the San Francisco Hilton and Towers Hotel, San Francisco, Calif. (see the table).

On Sunday, Dec. 8, two short courses are planned, "The back end at the forefront," and "DRAMs in the 21st Century." The former overviews changes over the last five years in backend processing and their economic impact. The latter exaines the dynamics of the DRAM business and how it can be sustained into the 21st Century. Plenary Session 1, on Monday, Dec. 9, addresses microelectromechanical systems (MEMS), silicon-on- insulator (SOI) technology, and the silicon foundry business.

1996 INTERNATIONAL ELECTRON DEVICES MEETING

Session 1 Plenary session	**Session 2** Quantum electronics and compound semiconductor devices—HEMTs	**Session 3** Device interconnect technology—lithography interconnects and advanced modeling	**Session 4** Solid-state devices—RF power devices and components
Session 5 CMOS devices and reliability—high-speed CMOS and SOI	**Session 6** Modeling and simulation—compact modeling	**Session 7** Integrated circuits—nonvolatile memory technology	**Session 8** Quantum electronics and compound semiconductors—III-V HBTs and MESFETs
Session 9 Emerging technologies	**Session 10** Solid-state devices—silicon heterostructures and novel devices	**Session 11** Integrated circuits—advanced SRAM technology	**Session 12** Detectors, sensors, and displays—vacuum microelectronics
Session 13 CMOS devices and reliability—thin dielectrics	**Session 14** Device interconnect technology—interconnects	**Session 15** Modeling and simulation—device modeling	**Session 16** Quantum electronics and compound semiconductors—lasers and quantum devices
Session 17 Device intrerconnect technology—shallow junction and salicide technologies	**Session 18** Solid-state devices—smartpower devices and technologies	**Session 19** Device interconnect technology—advanced dielectric technology	**Session 20** Detectors, sensors, and displays—MEMs I
Session 21 CMOS devices and reliability—advanced CMOS transistor architectures	**Session 22** Integrated circuits—DRAM technology	**Session 23** Modeling and simulation—interconnect and statistical modeling	**Session 24** Evening panel discussion—the people crunch
Session 25 Evening panel discussion—system on a chip, does it make sense?	**Session 26** Quantum electronics and compound semiconductors—detectors and photoreceivers	**Session 27** Device interconnect technology—memory dielectrics	**Session 28** Modeling and simulation—process modeling I—oxidation and implant
Session 29 CMOS devices and reliability—process-induced damage and reliability	**Session 30** Detectors, sensors, and displays—MEMs II and TFTs	**Session 31** Modeling and simulation—process modeling II	**Session 32** Device interconnect technology—advanced isolation
Session 33 Integrated circuits—high-performance technology	**Session 34** CMOS devices and reliability—hot-carrier effects and ESD of CMOS	**Session 35** Detectors, sensors, and displays—image sensors	

A. Auberton-Herve, of SOITEC, Grenoble, France, will talk about "SOI: Materials to systems." This will be followed by Ken Wise of the University of Michigan, Ann Arbor, who'll discuss "Microelectromechanical systems: Interfacing electronics to a nonelectronic world." Next, "Foundry technologies," will be delivered by F. Tseng of Vanguard International Semiconductor Corp., Taiwan, The Republic of China.

This year's luncheon speaker will be Gordon Moore, Intel's cofounder and chairman of the board. On Tuesday, Dec. 10, he'll address complex technology trends with his presentation "Silicon device fabrication technology revisited."

On Tuesday evening, two panel sessions are planned. They are "The people crunch" (Session 24) and "System on a chip, does it make sense" (Session 25).

The four reports that follow cover the highlights of this year's technical presentations.

IEDM Showcases Tomorrow's Analog Semiconductors

The Conference Focuses On The Latest Processes For Micromachined Sensors, Infrared Detectors, HBTs, Laser Diodes, LEDs, And Power-Control ICs.

FRANK GOODENOUGH

Attending the annual International Electron Devices Meeting (IEDM) can provide a good look at what may be forthcoming in the area of ICs. At this year's conference, advances in analog semiconductor processes will give engineers a preview of what they can expect to develop in microelectromechanical systems (MEMS), heterojunction bipolar transistors (HBTs), power-control devices, laser diodes, and LEDs.

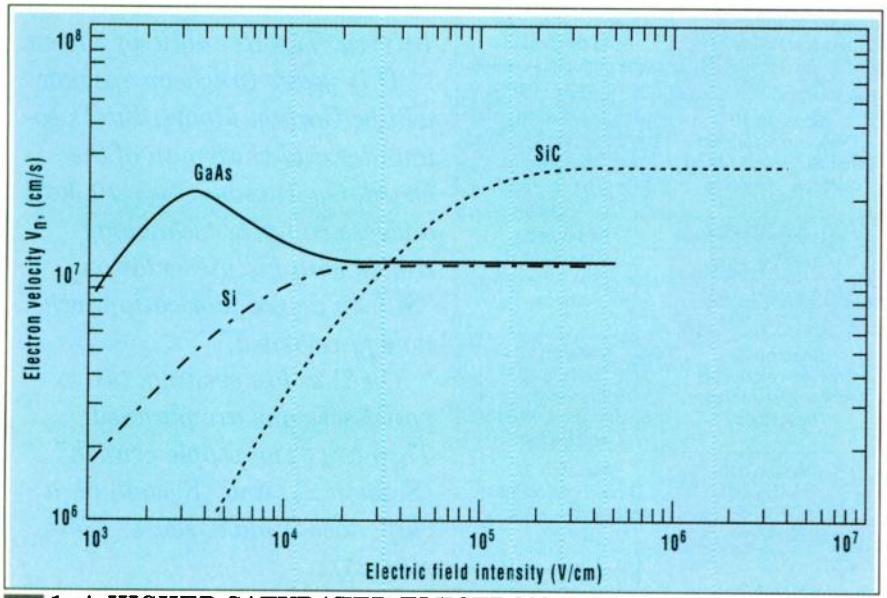
A number of papers cover MEMS. According to an invited paper in Session 20, "Detectors, sensors, and displays," by a team from the Physical Electronics Laboratory, ETH, Zurich, Switzerland, the field of MEMS includes not only micromachined actuators, but also a broad family of micromachined sensors, actuators, and complete systems using coupled electrical, mechanical, radiant, thermal, and chemical sensors. A second invited paper in the session by Kurt Peterson, founder of Cepheid, San Jose, Calif., and an early guru of micromachining, describes biomedical applications for MEMS.

Other papers cover submicron CMOS, biCMOS, and DMOS processes. These papers address the processes' active devices for digital, analog, display, and power IC applications. Silicon germanium (SiGe) and III-V processes also garner their fair share of papers. There are even two papers describing SiGe light detectors. A pair of invited papers cover silicon-carbide (SiC) devices for applications ranging from power to RF, and III-nitride devices such as aluminum-nitride (AlN), gallium-nitride (GaN), indium-nitride (InN) devices, and their alloy AlGaInN.

Session 9 "Emerging technologies," features three invited papers covering SiC, III-nitride, and biomedical MEMS. According to Session Chair Judy Hoyt of Stanford University, Stanford, Calif., all three technologies have now approached or recently reached commercialization.

SiC has been in the R&D labs for a long time. A paper on SiC by a team from Northrop Grumman, Baltimore, Md., and Pittsburgh, Pa., points out that the material is superior to both silicon and GaAs for many applications *(Table 1)*. For example, its high bandgap voltage of 3.25 eV results in an "intrinsic" temperature of 1650 °C, and its leakage is on the order of picoamperes at 400 °C. The bandgap voltage also suits it for use in ultraviolet detectors.

The material's saturated electron velocity, v_{nsat} is more than twice that of GaAs *(Fig. 1)*. It gives SiC devices a higher transconductance, a higher cutoff frequency (f_t), and lets them handle higher currents for a given device area. The paper points out that CMOS SiC has been used to fabricate ring oscillators, op amps, nonvolatile



1. A HIGHER SATURATED ELECTRON VELOCITY and breakdown field intensity of SiC, relative to that of GaAs and silicon, enables SiC devices to run at power densities four times those of either GaAs or silicon.

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PACKAGE	SOT23-5	BIGGER

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HOT RUNNERS

SiC's high breakdown voltage (E_{crit} = 3 MVcm) provides for RF power and power switching devices that can operate at three to four times the power density of similarly rated silicon or GaAs devices. Moreover, its superior thermal conductivity (θK = 4.9 W/cmK) is almost ten times that of GaAs and over 3 times that of silicon. This ability to take high temperatures permits taking maximum advantage of the power density.

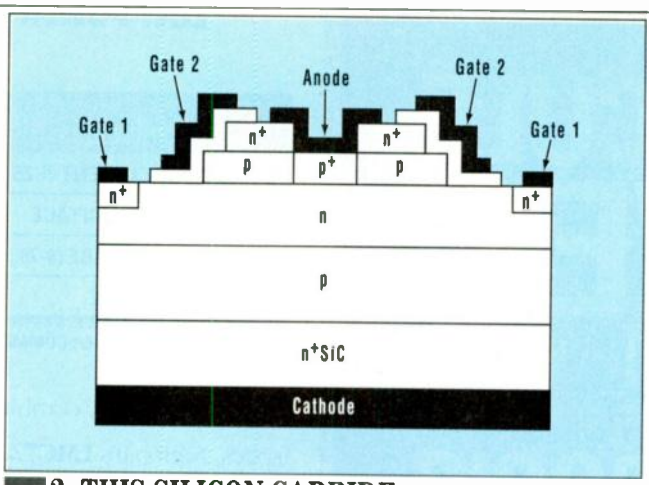
This mix of characteristics allows tiny, high-voltage, RF or low-frequency, SiC power devices to run very hot at near-room temperatures. Theoretically, the low leakage currents could let SiC DRAMs act as non-volatile memories at room temperature.

As of today, 3- to 6-GHz SiC static induction transistors (SITs) have been fabricated as well as 6- to 10-GHz MESFETs. Other SITs with 300-V breakdowns have put out 450 W at 600 MHz. A 1-kW multitransistor module has been built with them. This module transmitted HDTV over the air at the National Association of Broadcasters (NAB) convention in Las Vegas, Nev., this past April. A more recent version of that SIT yielded a voltage gain of 70, a g_m of 140 mS/cm, and a channel current of 650 mA/cm. And, it blocked 350 V. SiC MESFETs have been built with drain currents exceeding 500 mA/mm at breakdown voltages of over 100 V. The results of small-signal measurements on these devices have produced an f_{max} of 42 GHz and a gain of over 10 db at 10 GHz.

For low-frequency (relative to 1 GHz) power applications such as switching regulators, SiC Schottky diodes offer a turn-off time of 10 ns and they break down at over 1000 V. Their forward drop when conducting is about 2 V at a current density of 100 A/cm^2. SiC p-i-n diodes capable of running at 400°C provide breakdown voltage of over 4.5 kV. Their forward drop is about 4 V and their carrier lifetime is about 3 μs.

SiC gate-turn-off thyristors (GTOs) with forward and reverse blocking voltages of 900 V have been built. Their forward current ran 2 A at a current density of 625 A/cm^2 and at a forward drop of 3.9 V. Moreover, 1000-A/cm^2 current densities and operation at 500°C is possible. Due to minimum minority-carrier storage, these SiC GTOs have achieved turn-off times of 200 ns. While such GTOs look good for high-temperature, high-power control applications, GTOs require complex drive circuits. To simplify the drive problem, a SiC, MOS turn-off transistor (MTO) has been proposed *(Fig. 2)*. A positive pulse on gate 2 of the MTO's interdigitated n-channel MOSFET turns on the MOSFET, which then turns off the MTO.

Blue-green semiconductor laser diodes have been the Holy Grail of all light-emitter developers ever since relatively efficient high-power (bright) red and infrared emitters arrived. They (and similarly colored LEDs) are wanted for applications ranging from underwater LIDAR (light detection and ranging) and large TV displays to compact disks for both audio and ROMs. The LIDAR application needs them because blue-green is the only light color that penetrates water without severe attenuation. Large LED-based TV displays need them for true-color displays. And CDs need them because their shorter light wavelength permits closer spacing of the dots on the CD, since they can store more bits.



2. THIS SILICON-CARBIDE MOS-turn-off thyristor (MTO) consists of a gate-turn-off thyristor (GTO) controlled by BJT and MOSFET gates. Applying positive current pulse to gate one turns on the GTO. Applying a positive voltage pulse to gate two of the MTO, the gate of a highly interdigitated n-channel MOSFET, turns off the GTO.

An invited paper by a two-person team from Meijo University, Nagoya, Japan, describes the latest work in III-nitride materials. Bandgap energies at room temperature range from 1.9 eV for InN to 6.2 eV for AlN devices, which are also chemically and physically stable. The paper describes ultraviolet blue, bluish green, and green LEDs with efficiencies better than 1%. Their brightnesses and efficiencies compare well with those of GaAlAs-based red LEDs. The blue LED is commercially available. Room-temperature operation of violet and ultraviolet laser diodes also have been reported.

TINY SENSORS

According to Cepheid's Peterson, over 20 million disposable micromachined blood-pressure sensors are shipped every year for use during surgery and intensive care. Moreover, today's advanced micromachining processes build pressure sensors just 0.4-mm wide (the world's smallest) so they can be inserted in ultraminiature catheters for monitoring blood pressure inside the heart.

These advanced processes also make possible complete systems on a chip. Peterson's invited paper in Session 9 describes four of them in detail. These chips form the basis of four advanced biomedical instruments:

- A fast, blood-chemistry analyzer;
- A flow cytometry system;
- A polymerase chain-reaction sys-

TABLE 1. KEY ELECTRONIC PROPERTIES OF Si, GaAs, AND SiC

Property	Silicon	GaAs	SiC
E_g (eV)	1.12	1.5	3.25
v_{nsat} (× 10^7 cm/s)	1.0	0.8	2.0
E_{crit} (MV/cm)	0.25	0.4	3.0
θK (W/cmK)	1.5	0.5	4.9

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TECHNOLOGY	Voltage Feedback	Current Feedback	Current Feedback
BANDWIDTH	750MHz (A_V=1)	400MHz (A_V=2)	1200MHz (A_V=2)
2V RISE/FALL TIMES	1.5ns	0.9ns	0.8ns
SLEW RATE	1500V/µs	2000V/µs	2500V/µs
QUIESCENT POWER	70mW	48mW	120mW
DIFFERENTIAL GAIN/PHASE	0.015%/0.025°	0.02%/0.03°	0.03%/0.02°
PRICE (1000s)	$4.20	$1.95	$4.20

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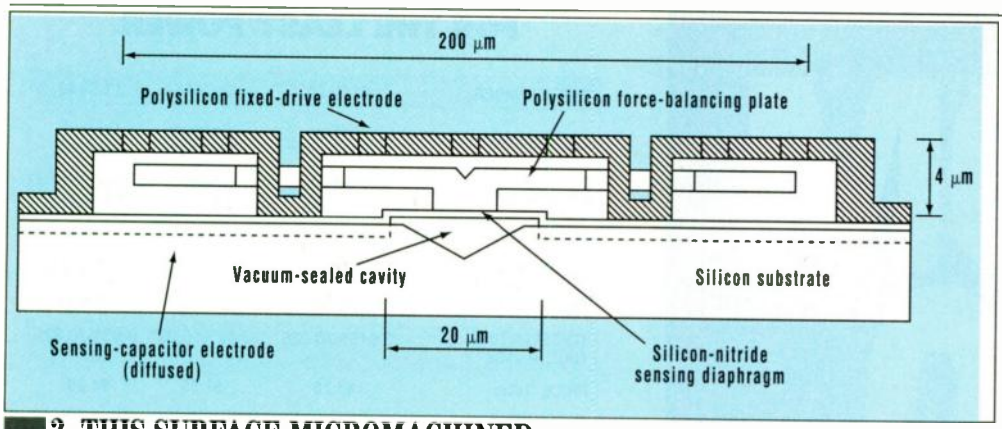

3. THIS SURFACE MICROMACHINED force-balancing pressure sensor employs force-multiplication similar to that in hydraulic braking systems. Electrostatic force applied to the large polysilicon force-balancing capacitor plate need be only one-quarter of that applied to the smaller silicon nitride (SiN) pressure-sensing diaphragm (capacitor plate).

tem; and

• An electrophoresis system.

Not only are they small, handheld instruments, whereas most available systems performing the same functions are big, bulky lab instruments, but their lower cost is coupled with superior performance.

Until now, blood-chemistry analysis involved taking a patient's blood sample, transporting it to a hospital's central laboratory, and waiting (even during an operation) over an hour for the results. Field analysis at an accident or disaster had been impossible. The handheld instrument from i-STAT of Princeton, N.J., eliminates those problems.

Flow cytometry measures some of the characteristics of collections of small particles such as populations of cells or pollen. Typical, desk-sized systems costing over $100,000 are now replaced by smaller, lower-cost, MEMS-based instruments. In them, complex hydrodynamic plumbing and detectors are built by etching channels on chips and bonding them together using conventional micromachining techniques.

CHIPS IDENTIFY HIV

Polymerase chain reaction (PCR) is used to identify DNA. Not only are conventional systems large, slow, and expensive, but they cannot capture and identify very small concentrations of DNA in a large sample—for example, a single count of HIV in a drop of blood. Silicon-micromachined MEMS have been built that are up to 10 times faster than existing systems. Moreover, they produce 30% more DNA. They also use very small quantities of genetic material and reagents. This technology represents a significant savings, because some reagents cost over $1000 per milliliter.

Electrophoresis also is used to identify DNA. Like the other currently available instruments, those for electrophoresis are large, slow, and expensive. Again, researchers have developed chips based on micromachining that will make possible small, handheld systems that are ten times faster than those now available. According to Peterson, a revolution has started. The days of a centralized hospital laboratory, full of large, slow, instruments costing $100,000 and up, are numbered. They will be replaced with these handheld, MEMS-based instruments to be used at the patient's side.

As paper 20.2 points out, many applications require pressure measurement at temperatures exceeding the maximum limits of silicon—albeit piezoresistive, pn-junction silicon sensors have reached 175°C and silicon-on-insulator (SOI) devices have operated at temperatures close to 500°C. However, above 500°C, silicon undergoes creep at minimum loads. Those facts instigated Kulite's development of a batch-built, diaphragm-based, 1000-psi full-scale range, piezoresistive SiC pressure sensor that performs well between 28 and 350°C. Kulite expects future versions to do the same at 600°C.

An IC MEMS, a force-balanced pressure sensor (paper 20.3) created by two researchers at the University of Michigan's Center for Integrated Sensors and Circuits, Ann Arbor, is made by surface micromachining. Electrostatic force balancing provides an output signal relatively independent of material properties and process variations. In the past, these

LATE PAPERS

A pair of interesting papers on analog developments were received at press time; the first described a sub-mm-wave monolithic resonant-tunnel-diode (RTD) oscillator, and the second highlighted integrated organic LEDs and amorphous-silicon thin-film transistors (TFTs) deposited on unbreakable metal-foil substrates.

At the University of California in Santa Barbara, researchers built a solid-state oscillator with an observed oscillation of 650 GHz, the highest known frequency for a monolithic oscillator (Session 8). The oscillator was made up of a 64-element array of sub-mm-wave monolithic RTD arrays and produces a record output of 28 μW at 310 GHz and an associated record power density of 440 W/cm^2.

Conventional LCDs are fragile because they're built using glass substrates. Now, researchers at Princeton University, Princeton, N.J., report on organic LEDs they developed that can emit light from the top side and do not have to be built on a transparent substrate (Session 30). The researchers put the LEDs on rugged stainless-steel foils that were then dropped 30 feet onto a concrete floor without any performance degradation.

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Quiescent Current (typ@100mA)	600µA	5000µA

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balancing forces have been employed in accelerometers and microvalves, but the high voltages required by pressure sensors has been incompatible with IC processes. However, this sensor reduces the voltage requirement to about 15-25 V with a mechanical force multiplication scheme. The voltage needed to balance the force on the small sensing diaphragm (sensing plate) is cut by the square root of the ratio of the areas of the sensing plate to the force-balancing plate. A ratio of 100 brings the voltage into the acceptable range.

The sensor consists of a 0.24-μm thick SiN_x small, sensing diaphragm (20 by 20 μm^2) built over a vacuum cavity *(Fig. 3)*. At atmospheric pressure, the diaphragm bends down. A central support connects the 1.1-μm-thick, large-area (200 by 200 μm^2) polysilicon force-balancing plate to the center of the sensing plate. A fixed, thick, polysilicon electrode is located 1 μm above the force plate. The electrostatic force voltage from a charge pump is applied to this electrode. The displacement of the midplate is sensed capacitively by electrodes diffused into the substrate.

Most conventional flat-plate Hall-effect-based IC magnetic field sensors do not lend themselves to the use of external magnetic field concentrators. To get around this problem, a three-person team from the Swiss Federal Institute of Technology, Lausanne, Switzerland, joined by an additional member from Sentron AG, Zug, Switzerland, developed a cylindrical Hall sensor with integrated concentrators. This Hall effect device senses the quasicylindrical magnetic field under the gap between the pair of field concentrators. A sensor of this type could measure the current flowing through a wire located in the gap. In the fabricated sensor, the aluminum and n^+ layers provide contacts to the active n-substrate region. The thick, 30-μm layer of ferromagnetic material forming the concentrators is glued over the SiN passivation layer. Photolithography defines the shape of the concentrators. As a current sensor, this Hall effect device sports a sensitivity of 1 mV/A. Unlike flat-plate Hall devices, the cylindrical Hall sensor is highly directive.

Another paper in Session 20 (20.8) describes an ultrasensitive, uncooled, heat-balancing infrared detector based on electrothermal principles. It consists of a six-transistor IC built on a standard CMOS process which is followed by simple postprocessing and micromachining.

Two of the six FETs, p-channel devices, are series connected and located in a p-well suspended by polysilicon beams over an etched cavity. This arrangement thermally isolates the devices from the p substrate. Because of their thermal isolation, the p pair are subject to heating by impending thermal radiation. The circuit, with its thermally isolated FETs, forms an electrothermal feedback loop that tends to maintain the temperature of the n well constant. Its output voltage rises as the temperature of the thermally isolated FETs rises, yielding a responsivity of 10^6 V/μW or 1 V/μW.

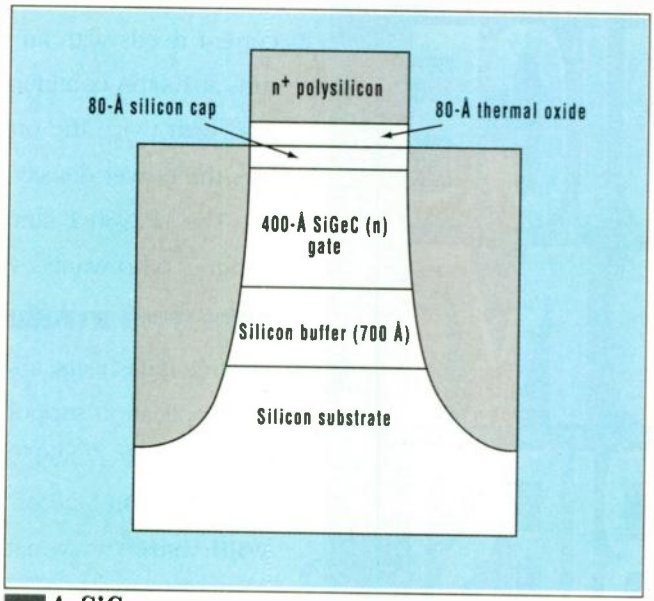
SUB-200-NM ANALOG CMOS

Depending on who you talk to and what they are doing, some researchers say sub-200-nm gate-length CMOS can perform any and all of the analog tasks required by semiconductors, including RF applications, for the foreseeable future. Other gurus insist we will always need a few npn BJTs around. Still other experts demand good fast pnp transistors.

Most of Session 5's papers describe the latest work on fully- and partially-depleted SIMOX thin-film SOI (TFSOI) CMOS for digital applications. However, at least two papers look at device processes for analog RF applications. One of them, paper 5.8, by a team from Motorola, Mesa, Ariz., describes the investigation of both MOS and bipolar devices on a TFSOI complementary-bipolar CMOS (CBiCMOS) process. The second, paper 5.1, by a Toshiba team, Kawasaki, Japan, describes the high-frequency analog characteristics of sub-200-nm gate-length tunneling-gate-oxide CMOS devices. SIMOX wafers are built by implanting oxygen below the surface of a silicon wafer and heating it. The heating forms a thin layer of silicon dioxide, with the implanted oxygen below the thin layer of silicon on the surface of the wafer. The heating also anneals ion-implantation-caused damage to the thin monocrystaline silicon structure on the wafer surface (the high-energy ion implantation changes the crystalline silicon to amorphous silicon). The annealing produces small areas of monocrystalline silicon that are usually sufficient for tiny digital CMOS devices, but not large enough or deep enough to hold the large vertical bipolar devices required for analog circuits.

The digital FETs built on SIMOX substrates sport effective gate lengths from 1.5 μm to less than 100 nm, and seem feasible. For the last few years, TFSOI proponents have indicated that it was the only way to go as gate lengths spurted below 1 μm. And, at each plateau (0.8, 0.6, 0.5, and 0.35 μm), TFSOI proponents have been wrong. SOI has not been needed. That's why some still prefer to see analog RF process developments aimed at both FETs and BJTs.

At least one of the digital papers is interesting from a dc



4. SiGe is presently known for its BJTs. However, it also can improve the performance of a MOSFET such as this p-channel FET. It has a relatively thick layer of SiGeC separated from the gate oxide by just 50 Å of silicon. Trans- conductance of devices with the SiGeC layer at a gate-source voltage of 2 V runs about 75 mS. That's 20% greater than that of silicon alone, and virtually twice that of similar FETs without the carbon added to the SiGe.

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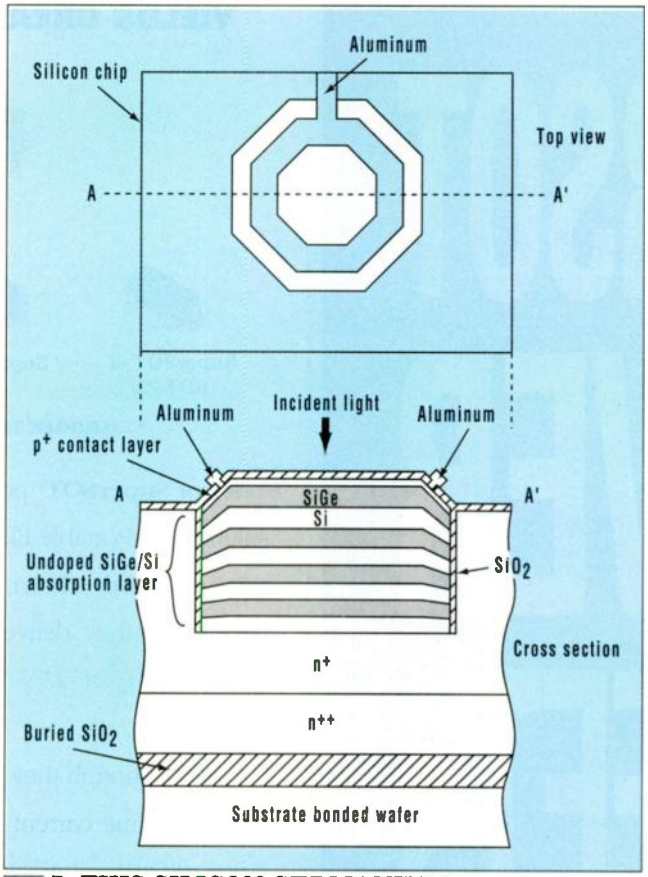
analog point of view. Paper 5.4, by a team from Tohoku University, Sendai, Japan, displays I_d-V_d curves for individual FETs running off supply rails as low as 100 mV at currents of several 100 mA. Put over 1,000,000 of those on one chip and chip current could run well over 100 A.

The n-channel FETs on the Toshiba process noted earlier achieve cutoff frequencies ranging from 20 to 245 GHz for gate lengths from 0.5 to 0.1 µm. Transconductance runs between 300 and 1000 mS/mm for a similar range of gate lengths. Cutoff frequency, an inverse function of g_m, runs from less than 10 GHz to over 200 GHz for g_m between 200 and 1000 mS/mm. The polysilicon gates on top of 1.5 nm of gate oxide are silicided with a layer of $CoSi_2$ (cobalt-silicide) that results in a sheet resistance of just 4 Ω/square. The drain and source contacts also are silicided to achieve similar sheet resistance. Noise figures of 1.5 dB were achieved at 5 GHz with a gain of 10 dB at currents ranging between 10 and 100 nA/µm.



5. THIS SILICON-GERMANIUM photodetector employs SiGe and a bonded-wafer silicon-on-insulator substrate to replace III-V material photodetectors in order to detect 1-Gbit/s data arriving on a 980-nm wavelength optical carrier.

According to the paper, the process is fairly simple requiring only seven major steps starting with a p substrate: Isolation by LOCOS, channel definition, gate oxidation by rapid thermal oxidation at 800°C for 10 seconds, and formation of the phosphorus-doped polysilicon gate. The source and drain are formed by the diffusion of phosphorous from the phosphosilicon glass wall on both sides of the gate. Cobalt silicidation and metalization steps follow.

The paper also describes n- and p-channel FETs with gate lengths of 170 nm and cobalt-silicided polysilicon gates on top of 1.5 nm of thermally-grown gate oxide (TOX). These FETs are used to build a 101-stage CMOS ring oscillator. Propagation delay per stage varies from 80 to about 18 ps for supply voltages between 700 mV and 5 V. These FETs indicating sub-200-nm CMOS may be able to handle RF applications at carrier frequencies greater than 2 GHz.

Mixed-Mode ICs

The Motorola paper notes the advantages of their TFSOI process for low-power RF mixed-signal applications. These include latch-up immunity, speed, and potential integration level, combined with process simplification, implying low cost. The paper also reports on the results of low-frequency (1f) noise tests on the FETs and BJTs from the process.

The process starts with a SIMOX wafer sporting a 100-nm layer of silicon on top of 400 nm of buried oxide. The process is based on a fully-manufacturable 500-nm gate-length, lightly-doped drain CMOS process that also builds high-frequency lateral BJTs *(Tables 2 and 3)*.

Today, many system designers are asking if SiGe processes are, like GaAs, the solution to tomorrow's problems. As mentioned earlier, the jury is still out on what processes are going to be used for which commercial ICs. The RF mixed-signal arena is still up for grabs. However, SiGe has lots to offer, and much of it is covered in the nine papers distributed over three IEDM sessions, Sessions 10, 26, and 33. In fact, several of the papers describe work performed to eliminate some of SiGe's warts, and make it easier to use.

Several papers describe the positive effects of introducing small amounts of carbon into the SiGe HBT to form SiGeC. A team from the University of Texas, Austin developed a SiGeC p-channel MOSFET located between a 700-Å silicon buffer and a 50-Å silicon cap *(Fig. 4)*. The carbon reduces the strain in the crystal lattice at the SiGe boundary. This, in turn, approximately doubles the g_m of the FET to over 75 µS.

A paper (10.2) by a team from Princeton University, Princeton, N.J., University of Virginia, Charlottesville, Va., and from Evans East, Plainsboro, N.J., describes the addition of carbon to the SiGe HBT structure. Carbon is added to reduce the outdiffusion of boron from the SiGe base into the silicon collector. The outdiffusion cuts the gain, speed, and Early voltage of the HBT npn BJTs. Their addition of carbon drastically reduces the boron

TABLE 2. KEY DEVICE PARAMETERS FOR TFSOI CBiCMOS TECHNOLOGY

Bipolar	SOI thickness	Emitter size	Peak current gain	f_T (GHz)	f_{MAX} (GHz)	C_{EB}	C_{CB}	BV_{CEO} (V)
npn	0.1 µm	0.1 by 7.2 µm²	65	14	22	4.1 fF	2.3 fF	>3.5
pnp	0.1 µm	0.1 by 7.2 µm²	40	9	—	3.5 fF	2.2 fF	>8.0

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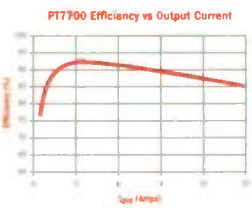

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TABLE 3. KEY DEVICE PARAMEERS FOR TFSOI CBiCMOS TECHNOLOGY

MOSFET	SOI thickness	Gate oxide	L_{eff}	Threshold	Subthreshold slope	I_{DSAT} @ 1.8 V	f_T (GHz)	f_{MAX} (GHz)	BV_{DSS} (V)
nMOS	0.1 μm	105 Å	0.44 μm	0.51 V	67 mV/decade	150 μA/μm	16	19	3.0
pMOS	0.1 μm	105 Å	0.45 μm	0.45 V	68 mV/decade	56 μA/μm	NA	NA	5.0

NA = not available

diffusion during postgrowth implantation and annealing procedures. The improvement is clear from V-I curves of devices with and without a mite of carbon in their bases. The epitxial layers creating the SiGeC npn transistors were grown by room-temperature chemical-vapor deposition.

A paper (10.3) by a team from Auburn University, Auburn, Ala., and IBM, Hopewell Junction, N.Y., investigates the effect of shaping the profile of germanium concentration across the base of a SiGe HBT to eliminate degradation of βV_A, f_t and f_{max} when operating at temperatures between –73 and +85°C. Working with IBM SiGe HBTs built on IBM's UHFCVD (ultra-high vacuum CVD) process and using a box profile, the team made devices with an f_{max} of 100 GHz and a βV_A of 10,000 while operating at a temperature of 300K.

Currently, most SiGe HBTs have breakdown voltages (BV_{CEO}s) on the order of 2 or 3 V. RF power devices need more than that. The Auburn IBM team also investigated the trade-offs between breakdown voltage and f_{max}. As a result future SiGe HBTs can be expected with a BV_{CEO} of 10. While the cut-off frequency will be lower, they still will offer RF performance superior to that of pure silicon BJTs.

To demonstrate the manufacturability of SiGe HBTs for RF applications, an IBM team from Hopewell Junction and Yorktown Heights, N.Y., describes the results (yields) from a run of 200 8-in. wafers with a total of over 4000 npn HBTs, in addition to large numbers of other devices. The npn transistors carried an f_t of 45 GHz and an f_{max} of 60 GHz.

The other devices include a pFET with an effective gate length of 430 nm; a gated lateral pnp transistor with a beta of 330 and an Early Voltage of 21; polysilicon and silicon resistors; MOS capacitors; 10-nH spiral inductors with a Q of 6 at 1 GHz; and varactor, p-i-n, and ESD diodes. The results included histograms of cutoff frequency, plots of ECL ring-oscillator propagation-delay per stage, and total base resistance. Other parameter variations plotted included beta and f_{max}. The yield is equal to or better than that achieved by similar CMOS devices.

SiGe Opto Detectors

An indication of the versatility of SiGe can be obtained by looking at the photodetectors that have been built with it. A team from NEC, Kanagawa, Japan, has built a vertical-cavity SiGeSi p-i-n diode photodetector array on a bonded-wafer SOI substrate. It replaces InGaAs and GaAs photodetectors performing similar functions. The IIIV-material devices have excessive crosstalk between array channels at data rates of over 1 Gbits/s *(Fig. 5)*. The parallel digital data is coming off multiple glass fibers operating at a light wavelength of 980 nm. Each fiber channel needs its own detector.

Each detector, composed of many alternating layers of silicon and SiGe, is octagonal in order to eliminate the need for a large facet at each corner. The sensor is one of many forming the array, that is grown on a silicon substrate containing an IC for each sensor. The ICs perform the additional detection and signal-conditioning tasks required to convert the signal current from the sensor to a useful form. The ability to grow the detector on silicon holding the ICs eliminates the need to bond III-V materials to the silicon—not a simple task.

The detector's low-dark current of 0.5 $pA\mu m^2$, mandatory for a high signal-to-noise ratio, is combined with a 3-dB frequency of 7.8 GHz, while back-biased with 5 V. Parasitic input capacitance runs just 0.2 pF with 2.5 V of back bias. A somewhat simpler, but similar p-i-n photodiode has been developed by a team from the University of California, Los Angeles (UCLA) for similar applications. It can operate with input data rates of 2.5 GHz. The team uses a silicon substrate, but adds carbon to the SiGe to achieve an efficiency-bandwidth product two and a half times that of earlier SiGe designs without the carbon material.

Power Control

The IEDM always carries a few power-control papers, and this year is no exception as seen in Session 18 consisting of seven papers. They cover technologies ranging from a 0.6-μm bipolar-CMOS-DMOS, to one offering 300-V, 300-mA gate-controlled SCRs on a bonded SOI substrate. Several of the papers cover detailed analysis of existing biCMOS and DMOS device processes. They also have suggestions for reducing well-known warts.

The 0.6-μm bipolar-CMOS-DMOS process is the subject of paper 18.1, an invited paper by a team from SGS-Thomson, Milan, Italy. It describes the fifth generation of this process which combines fine-geometry 5-V CMOS and nonvolatile EEPROM memory with low-voltage (20-V) npn and pnp transistors with power-control devices (lateral DMOSFETs) that are able to stand off 80 V. A full menu of active devices from the process is listed *(Table 3)*.

A team from Supertex, Sunnyvale, Calif., and Planar Systems. Beaverton, Ore., describes in paper 18.3 an integrated power switch designed to drive the individual pixels in electroluminescent and plasma-addressed flat-panel color TV displays. Built on a 20-V CMOS process on a bonded-wafer substrate, the team employs n- and p-channel logic gate-controlled MOS SCRs that can stand off 350 and 310 V, respectively. Both devices can pass 300 mA. The process also builds a diode rated at 390 V. All the high-voltage ratings are achieved while the devices are passing 1 μA. □

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IEDM Spans Image Sensors Through RF

An Enormous Range Of Technologies Show That There Is Still More Room For Developments In Process Technologies.

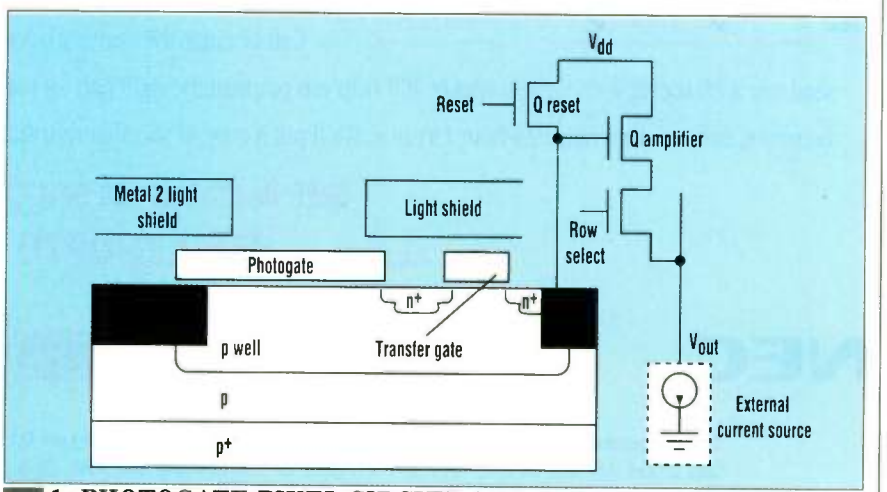
PAUL MCGOLDRICK

The invited paper in Session 35, "Detectors, sensors and displays—image sensors," is a good example of the range of technology innovations this year's IEDM presents in imagers and sensors. The paper, "CCD imagers for broadcast applications," from Philips Imaging Technology, Eindhoven, the Netherlands, presents the latest advancements of transfer CCD technology with the presentation of a 2/3-in. array with 600k pixels for an NTSC format. The image format is such that it combines a 4:3 and 16:9 aspect ratio, while maintaining horizontal resolution and frequency response. Using the flexible-clocking possibility inherent in the device technology, a tunable, vertical, anti-aliasing filter is built on-chip. A new design approach is used where the light-sensitive part is composed by repetition of a single-gate electrode using polysilicon for high sensitivity, especially for blue light. The technique also has a profiled p well, giving anti-blooming protection of 10,000 times its overexposure.

Philips Imaging also discusses another frame-transfer CCD imager that's VGA-compatible (640 by 480 pixels progressively scanned at 60 frames/s) with a 1/8-in. optical format. The imager maintains an optimal light sensitivity, high charge-handling capacity, and vertical anti-blooming functions. The sensor uses two ultra-thin polysilicon layers and a modified shunt-wiring technology with other optimizations.

In the same session, NEC Corp., Kanagawa, Japan, describes work on a two-phase, single-layer electrode CCD register with a charge-injected floating gate. The techniques allow the single-layer advantage and lower power consumption of smaller cells, while maintaining high-speed operation. A floating-gate photosensor also is described by the Naval Research Laboratory, Washington, D.C., and the University of Maryland, College Park, Md., exhibiting sensitivities of 10 nW, a rise time of 35 ns, and a dynamic range up to 10^5:1. The ac-coupled sensor has a square-root compressing transfer function for large photo signals. The potential uses of the sensor are in infrared local-area networks (LANs) and as optical disk laser sensors.

A high-resistivity n-type silicon substrate is used in a



1. PHOTOGATE PIXEL CIRCUIT AND DEVICE schematic for CMOS active pixel image sensor.

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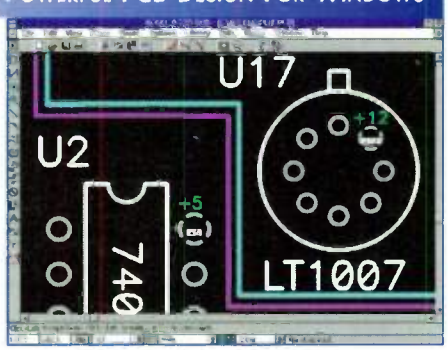

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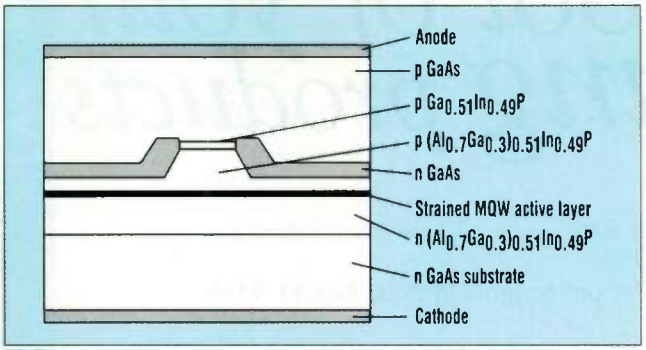
200-by-200-pixel sensor that uses back-illumination to increase blue-light response. The sensor is being developed by Lawrence National Laboratory of Berkeley University, Berkeley, Calif., and the Lick Observatory of the University of California at Santa Cruz. The sensor is otherwise conventional except that the substrate is totally depleted, removing any red-fringing problems. Theoretical work by IBM's Thomas Watson Research Center, Yorktown Heights, N.Y., and SRDC, Hopewell Junction, N.Y., looks at experimental results of CMOS imagers using 1.8-V, 0.25-μm CMOS logic technology. Use of the newer CMOS processes promises the potential of lower costs compared to CCDs, random access of the data, and lower voltages and powers. It also offers the alluring possibility of combining the signal electronics of processing and drivers on the same IC *(Fig. 1)*. Pixel size also is the smallest reported to date at 7 by 7 μm.



2. SCHEMATIC CROSS-SECTION of the transverse-mode stabilized AlGaInP laser.

PHOTORECEIVERS AND LASERS

Session 26, "Quantum electronics and compound semiconductor devices—detectors and photoreceivers," opens with an invited paper from AT&T Research Labs, Holmdel, N.J. The paper points out that integrated photoreceivers have been the most investigated optoelectronic IC (OEIC). The authors summarize the last five years of work on long-wavelength receivers and the different approaches reported from several laboratories for the integration of HBT-based OEICs. They also discuss their own approach in the integration of the p-i-n photo-detectors with the HBT-based preamplifier. Single-channel receiver modules for long-haul systems have been operated up to 20 Gbits/s for a bit-error-rate of 10^{-9}, while 8-channel receiver-array modules have been fabricated for wavelength-division multiplexing (WDM) applications. These have an average measured sensitivity of –25 dBm at an operating speed of 2.5 Gbits/s for a bit-error-rate of 10^{-9}.

WDM applications are also the focus of a paper from the University of Michigan, Ann Arbor. In this case, the problems of crosstalk in arrays are discussed as the major limitation of sensitivity in the current generation of high-responsitivity photo-detectors and low-noise preamplifiers. A novel solution is offered with a monolithically-integrated crosstalk-shielding metallization-blocking optical crosstalk. It greatly limits electrical crosstalk due to air-radiation modes. Crosstalk is shown to be reduced by 17 dB on a test array.

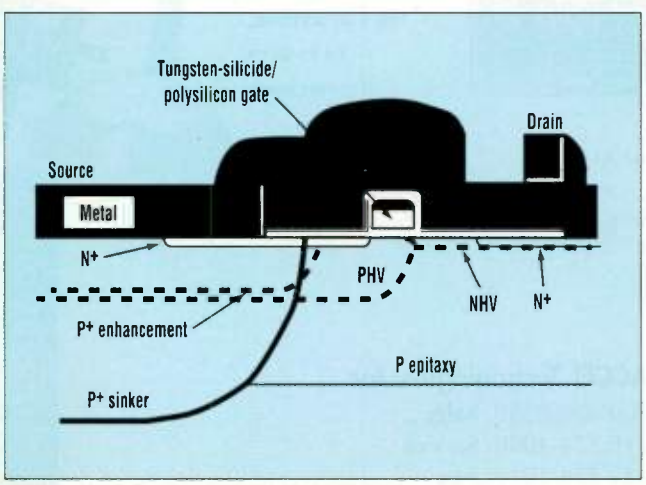
In Session 16, "Quantum electronics and compound semiconductors—lasers and quantum devices," Stanford University, Stanford, Calif., reports on a broadly-tunable vertical-cavity surface-emitting laser (VCSEL) that uses a surface-micromachined movable reflector as a top mirror. Broad-range wavelength tuning without mode-hopping is possible, simply by direct tuning of the optical path length of the cavity. This tuning is limited to 1%, however, but with the micro-mirror, a tuning range of 4% is possible, with a 1.8% range in laser oscillation without mode-hopping.

Matsushita, Osaka, Japan, explained its work on a high-power (30-mW) visible laser as a promising device for erasable DVD use. High temperature and excellent reliability of 650-nm-band AlGaInP lasers are achieved using a hydrogenated α-Si film which has a low optical absorption coefficient at the rear facet of the laser *(Fig. 2)*. Degradation problems are the subject of a paper from the Nagoya Institute of Technology, Nagoya, Japan, where GaAs-based laser diodes on silicon suffer from the formation of dark-line defects (DLDs). The DLDs are caused by the different material properties. The authors show that AlGaAs/GaAs laser diodes with self-formed GaAs islands are effective in improving the reliability of both the laser diode and LED on silicon.

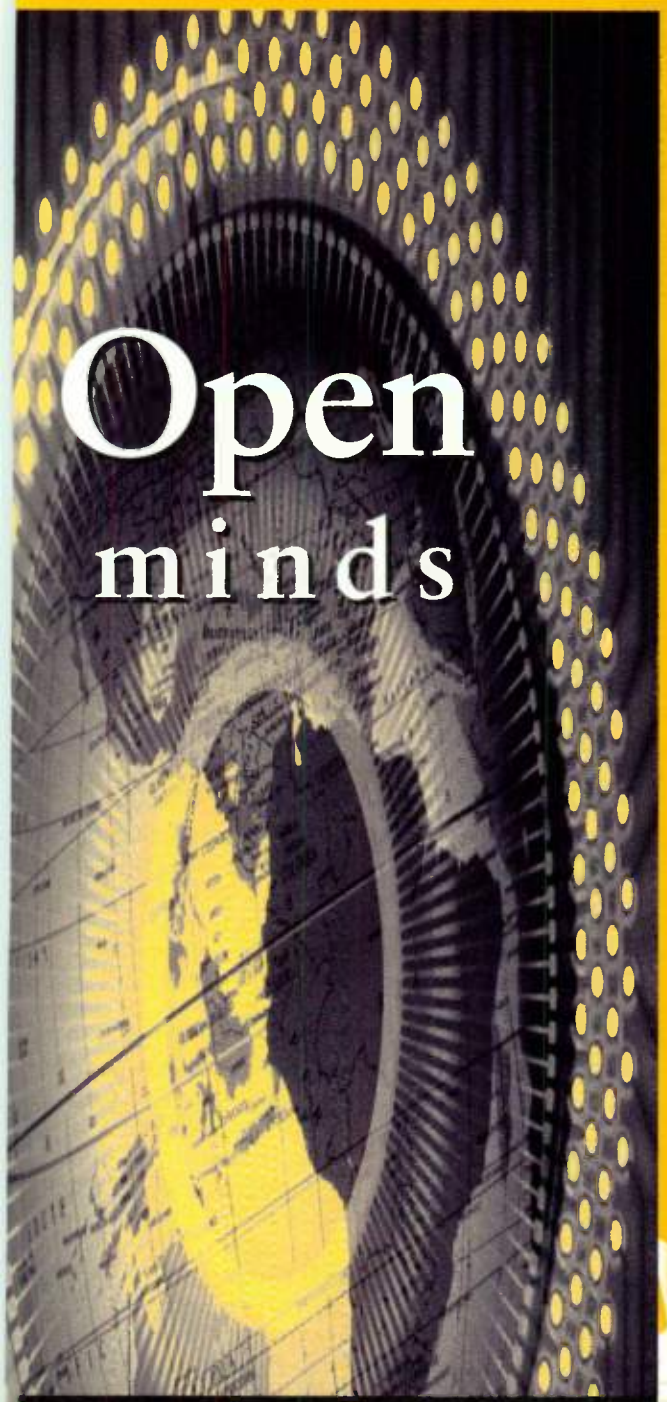
HEMTs

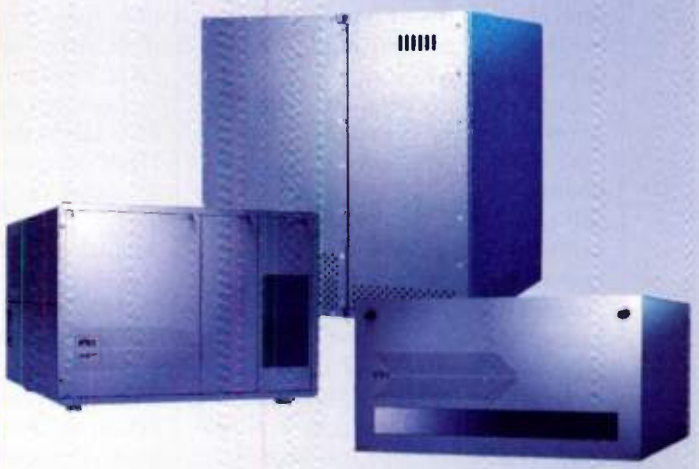
HEMTs seem to be appropriate vehicles for improved devices in power amplifiers and high-speed ICs. The keynote paper in Session 2, "Quantum electronics and compound semiconductor devices—HEMTs," deals with recent advances in III-IV nitride devices. Coming from APA Optics Inc., Lane Blaine, Minn., the University of Virginia, Charlottesville, Va., and Cornell University, Ithaca, N.Y., the paper discusses experimental and theoretical studies of AlGaN-InGaN devices showing high mobility at room temperatures. Monte Carlo simulations predict that GaN should have a peak velocity well above GaAs, and should be superior to other types in FET designs. Five transistors combined in parallel to form a 0.75-mm gate-width device provide a measured 0.3 W/mm at 10 to 15 GHz. This value seems to be limited by the thermal conductivity of the sapphire substrate used.

A new predictive model for tunneling-limited breakdown in power HEMTs is proposed by authors from the Massa-



3. LDMOS CROSS-SECTION of 1-gate finger. A device is made of 1 to 108 cells, and each cell contains 22 gate fingers.





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LATE PAPERS

A pair of interesting papers on high-electron-mobility transistors (HEMTs) and one on full-chip optical imaging of logic-state evolution in CMOS circuits were received at press time.

Researchers at the University of California at Santa Barbara report on the first demonstration of a p-type HEMT on a GaAs-on-insulator (GOI) substrate in Session 2. A buffer layer of AlAs was grown on a standard GaAs substrate which was next oxidized and then devices were built on top of that. The resultant HEMT promises have high-output resistance, high efficiency, and high linearity, attributes attractive for high-frequency communication applications.

At Texas Instruments, Dallas, Texas, researchers devised a power pseudomorphic HEMT with a 600-μm-wide gate which they describe in Session 4. At 20 GHz, the device delivered output power of 501 mW, 60% power-added efficiency, and 11-dB power gain when biased at a V_D of 8 V. When the same-size device was biased at very low drain voltages of 1.2 and 2 V, record power-added efficiencies of 65.9 and 68.4, respectively were achieved.

At the IBM Research Division, Yorktown Heights, N.Y., researchers figured out a way to monitor an IC chip's performance by taking a video of bursts of luminescence using a microchannel photomultiplier as a detector. As they describe the technique in Session 5, they were able to measure fast switching speeds on thousands of gates at speeds exceeding 10 GHz.

chusetts Institute of Technology (MIT), Cambridge, Mass. Experimental evidence indicates that tunneling and/or thermionic field emission largely determine off-state breakdown. The lack of predictive models greatly hampers first-pass design success. The model can predict the tunneling current and resulting breakdown voltage limit in high-power HEMTs.

Cornell University, and the U.S Army Research Laboratory, Fort Monmouth, N.J., have changed the composition of the group III elements in an InP-based MODFET, and have stayed within the critical layer thickness to enhance the carrier confinement. Channel quantization and temperature are examined by a team from the Universities of Padova, Modena, and Parma, Italy, and Hughes Research Laboratories, Malibu, Calif., with respect to breakdown effects in composite-channel and conventional InP-based HEMTs. The results show great control of breakdown by quantization.

MMIC Control

OKI Electric, Tokyo, Japan, presents work that has been done on the control of electro-chemical etching for 0.1-μm gate formation for V-band circuit applications. This is an important control element for producing the required device characteristics in MMICs. Observed anomalies in the etching process suggest that isolation regions behave like p GaAs. An f_T of 86 GHz and an f_{max} of 250 GHz were extrapolated from the test data with voltages closely controlled and highly uniform.

A paper from the University of Illinois, Chicago, presents what its authors believe is the first implementation of an enhancement- and depletion-mode HEMT suitable for large-scale ICs fabricated on a semi-insulating InP substrate. This technology is of considerable interest in the area of low-power, high-speed communications. The measured output conductance is 18 mS/mm and 25 mS/mm, leading to a maximum voltage gain (g_m/g_o) of 35 and 18 for the enhancement- and depletion-mode HEMTs, respectively. Both devices also exhibited an f_T of 100 GHz.

Vacuum Microelectronics

The invited paper in Session 12, "Detectors, sensors, and displays—vacuum microelectronics," is about molybdenum microfabricated field-emission arrays and their more interesting application in microwave devices. Originating from SRI International, Menlo Park, Calif., the paper reviews progress in developing an emitter array for operation at 10 MHz in a 50-W klystrode amplifier. The ratio of g_m (conductance) to C (capacitance) in the power equation for drive to an array is notable, as it is desirably as large as possible.

The Korean Institute of Science and Technology, Seoul, Korea, discusses field-emitter arrays and their electron-emitters that use diamond-like carbon (DLC) films possessing negative-electron-affinity characteristics. The coating has been found to be improved. Toshiba, Kawasaki, Japan, looks at low-operating-voltage field-emitter arrays using low work-function materials.

Power Silicon

"Solid-state devices—RF power devices and components," Session 4, shows, that, perhaps, GaAs for high frequencies is not the sole solution. Toshiba, for example, describes high-efficiency 2-GHz power co-salicided silicon MOSFETs with low-voltage operations, but reasonable breakdown voltages. Power-added efficiencies of more than 50% are obtained at 2-GHz operation with supply voltages as low as 1 V.

Higher-power silicon for 2 GHz is discussed by Motorola, Phoenix, Ariz., with their sub-micron silicon LDMOS *(Fig. 3)*. The high-gain, highly-linear RF power transistors, designed for base-station operation, have been tested to a 1-dB power compression of 63 W with a drain efficiency of 44% under single-tone excitation. Two-tone excitation gives a power gain of 11.2 dB, a 34% drain efficiency, and an output power of 60 W PEP with supply voltages of 26 V. A second Motorola paper discusses the same basic LDMOS technology employed in lower-power FET devices at low voltages. The second-generation devices can deliver 70% power-added efficiency with 12 dB gain, and 31.5 dBm output power at 3.4 V and 850 MHz. □

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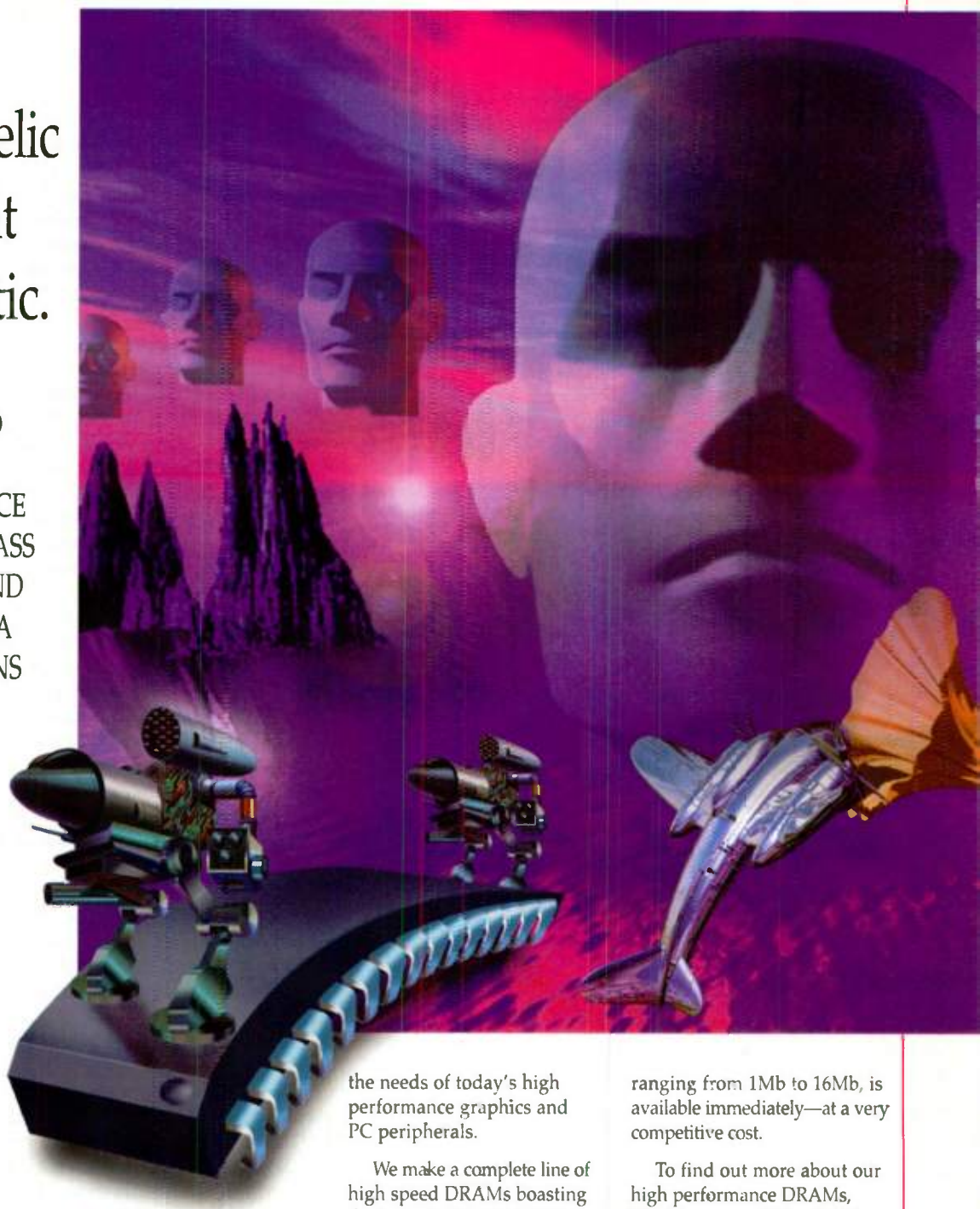

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Novel Processes, Structures To Yield Advanced Digital ICs

0.1- And 0.18-μm Fine-Line Processes Will Herald 4-Gbit DRAMs, 256-Mbit Flash Memories, And Magnetoresistive RAMs.

DAVE BURSKY

Even as most companies struggle to put their 0.35- to 0.25-μm processes onto production lines, researchers at this year's IEDM Conference are presenting the details of chip fabrication processes that employ design rules of between 0.1 and 0.18 μm. Such fine-line processes will allow the fabrication of 4-Gbit dynamic RAMs (that's 500 Mbytes on a single chip, folks!), 256-Mbit flash memories, and merged DRAM/logic chips that will truly become the system on a chip.

One of the densest technologies detailed at the conference is in a presentation in Session 22 by researchers from Toshiba Corp., Tokyo, Japan, and the LSI Laboratories of Nippon Telegraph and Telephone Corp., Atsugi, Japan. Through the use of X-ray lithography, they fabricated a DRAM array that employs 0.12-μm features, and has a memory-cell pitch of just 0.24 μm. The result is a memory cell that occupies an area of 0.115 μm^2, and could make possible memory chips with densities of 4 Gbits.

To achieve the small features, a self-aligned contact structure was developed and a very shallow junction of just 0.04 μm was used under the contact plug so that the memory cells could be formed on a 0.24-μm pitch. The plug itself is formed through the in-situ deposition of phosphorous-doped polysilicon, and the aforementioned shallow junction is formed by phosphorous diffusion from the plug. The fine patterning with X-ray lithography is combined with 0.12-μm isolation regions formed from shallow trenches (0.18-μm deep).

Building the storage nodes for such high-density memories is another challenge, and researchers at NEC Corp., Tokyo, Japan, detail in Session 27 the design of a stacked capacitor cell for 4-Gbit DRAMs. The cell employs a novel bottom electrode structure that uses titanium-nitride/titanium-silicide/polysilicon contact plugs (titanium-nitride capped plugs) under storage node contacts formed with ruthenium-oxide/ruthenium (RuO_2/Ru) *(Fig. 1)*. This structure prevents lateral oxidation of the titanium nitride, thereby keeping the cell extremely small.

The actual storage node is formed on top of the RuO_2/Ru contact through the use of an electron-cyclotron-resonance (ECR) plasma metal-organic chemical-vapor-deposition (CVD) system that deposits a high-dielectric-constant barium-strontium-titanium oxide (BST) thin film that delivers the equivalent of a 40-Å-thick layer of silicon-dioxide. On top of the BST film, a top electrode of ruthenium or aluminum/titanium-nitride is formed. Such a structure achieves a capacitance of 25 fF, sufficient for memory capacities of 4 to 16 Gbits.

Also studying the use of BST thin films, researchers at Texas Instruments Inc., Dallas, in conjunction with the University of Texas at Austin, developed an iridium-based electrode structure that eliminates the generation of alpha particles typically encountered with noble metals such as platinum. Detailed in Session 27, the iridium electrode also provides better adhesion to the silicon than platinum and it does not require the deposition of an adhesion layer. Furthermore, it can be deposited with a straightforward CVD process and has leakage currents within acceptable limits at temperatures of up to 100°C.

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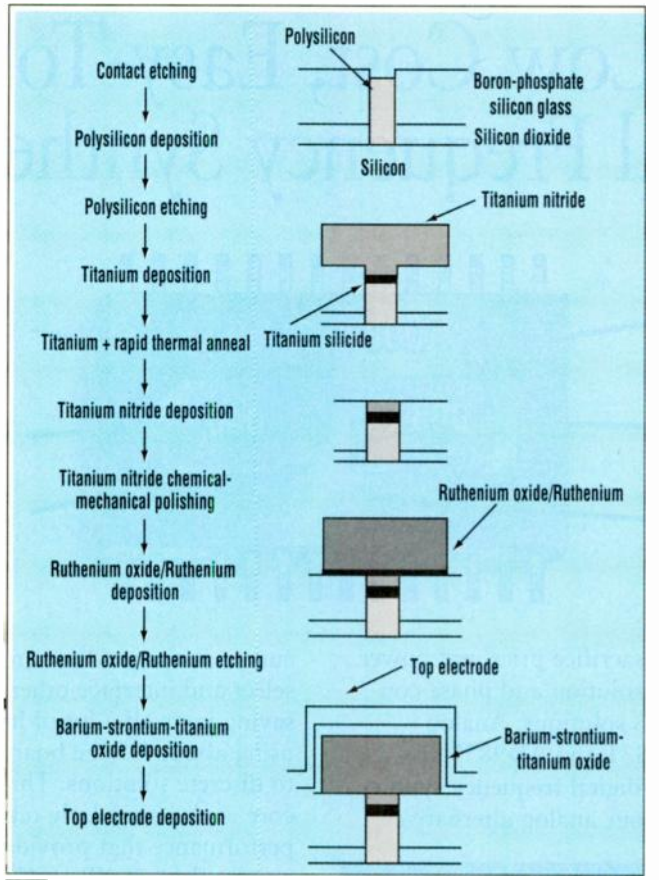
The use of a BST thin film also is the subject of another paper in the same session, this time by researchers from Toshiba Corp., Tokyo, Japan. In their paper, researchers detail the creation of a BST capacitor through the epitaxial growth of the BST film and the use of a strain-induced ferroelectric effect that results in a large rectangular hysteresis region with low leakage currents. Consequently, a large ferroelectric polarization can be obtained using a film with a thickness of less than 300 Å—the thinnest ferroelectric film reported to date.

The epitaxial capacitor was developed on a silicon wafer by first creating a single-crystal silicon plug and then adding a platinum/titanium-aluminum-nitride bi-layer barrier metal *(Fig. 2)*. That layer is a fully epitaxially grown structure consisting of BST/strontium-ruthenium-oxide/platinum/titanium-aluminum-nitride/silicon with all crystal layers having a 001 orientation of their lattices. The resulting cell can withstand process temperatures of up to 800°C, is free from oxides that have high vapor pressures and high diffusion rates in solids, has a flat and smooth capacitor surface (which helps minimize dielectric breakdown and large leakage currents), and, as mentioned earlier, is very thin—about a tenth that of other advanced capacitor structures.

A sort of cross between DRAM and flash memory is a new cell structure developed at the National Tsing-Hua University, Hsin-Chu, Taiwan. The cell is volatile, but has a long refresh time—it employs a low-power Fowler-Nordheim tunneling scheme through nanocrystalline silicon to provide short-term (1000 seconds) storage without any refreshing. This development is an extension of work first reported at last year's conference by IBM, and employs a stacked gate structure with nanocrystalline silicon films in which the nanocrystalline silicon file is extended to a floating polysilicon layer to improve the volume of charge storage. As a result, the structure provides a separation between two levels and alleviates word-line/bit-line disturbances. The resulting structure demonstrated low-power operation, high write speeds, and long refresh times.



1. THIS STORAGE cell developed by NEC could lead to DRAM chips that pack 4 Gbits or more. It employs a novel bottom electrode structure that uses titanium-nitride/titanium silicide/polysilicon contact plugs under storage-node contacts formed with ruthenium oxide/ruthenium layers. The actual storage node is formed on top of the RuO_2/Ru contact. A high-dielectric-constant barium-strontium-titanium oxide (BST) thin film delivers the equivalent of a 40-Å-thick layer of silicon dioxide—a capacitance of about 25 fF—sufficient for memory capacities of 4 to 16 Gbits.

Ferroelectric storage cells and other nonvolatile cells are well-covered topics at this year's conference as well. In the ferroelectric area, a joint paper from Sharp Corp., Tenri City, Nara, Japan, and Virginia Tech, Blacksburg, Va., details a high-temperature electrode-barrier structure that can be used for stacked memory cells. The electrode structure described by the paper in Session 27 consists of layered platinum-rubidium-oxide/platinum-rubidium/platinum-rubidium-oxide and is stable at temperatures of up to 700°C, allowing the manufacture of a highly reliable memory cell. That cell has reduced fatigue in the lead-zirconium-titanate (PZT) capacitor between the electrodes, which showed no decrease in remnant polarization in up to 10^{10} cycles.

Additional ferroelectric research, presented in Session 19, details a metal-ferroelectric-semiconductor FET structure developed by the Electronics and Telecommunications Research Institute, Taejon, Korea, and Cheong-Ju University, Cheong-Ju, Korea. The MFSFET employs a polysilicon source/drain and can used with ferroelectric thin films such as barium-magnesium-fluorine since the source and drain are formed prior to the formation of the gate dielectric. The dielectric constant is about 13, which provides a high value for implementing the storage element in a single transistor, and forms the basis of a high-density nonvolatile memory.

A novel nonvolatile memory cell, based on magnetoresistive technology, is the subject of a presentation in Session 7 by researchers from Motorola Inc., Tempe, Ariz. Deep-submicron memory cells based on a sandwich of giant-magneto-resistive (GMR) materials can be integrated with silicon CMOS to form a magnetoresistive RAM (MRAM).

The key element is a patterned strip of two nickel-iron-cobalt layers (less than 100 Å) separated by a nonmagnetic copper interlayer only 40 Å thick *(Fig. 3)*. Resistance of the film is high when the magnetic moments of the two magnetic layers are anti-parallel, and low when they are parallel. Both read and write operations in the MRAM require simultaneous application of sense and word currents (to generate the necessary magnetic fields), and allows for two-dimensional cell selection at the crossing of the sense and word lines. Very high memory densities are possible since the memory cells do not require one transistor per cell.

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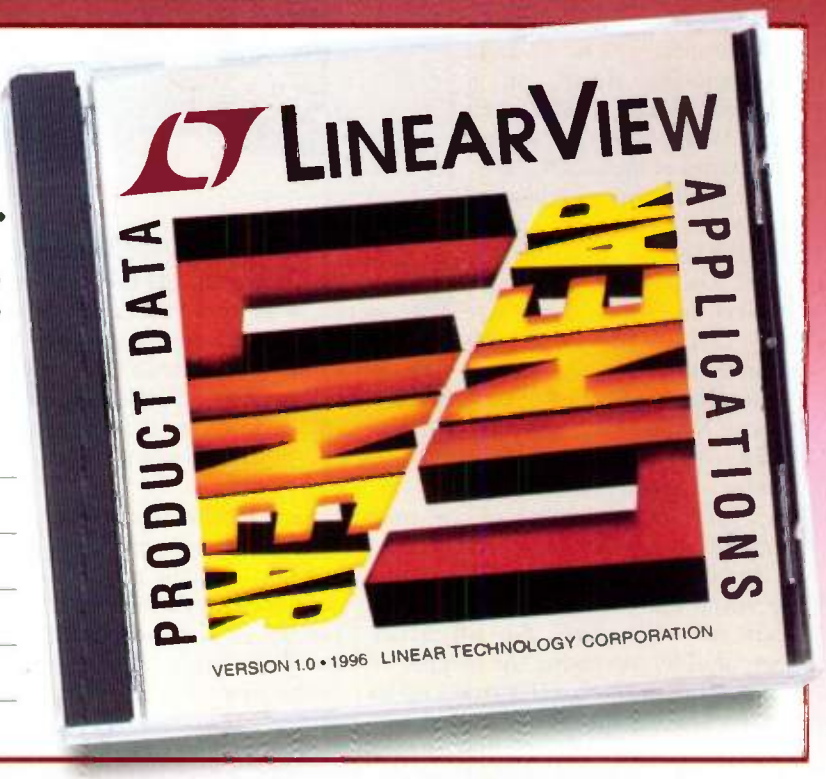

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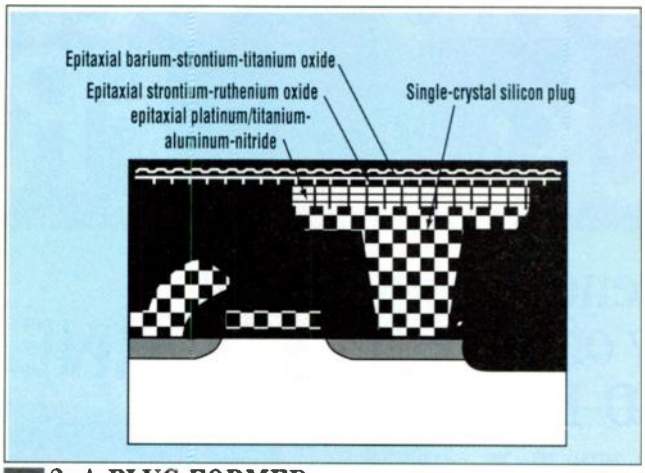
tional flash-memory technologies also is showing promise. A number of papers in Sessions 7 and 13 detail advances with various nonvolatile memory cells. The highest-density paper in Session 7 is a discussion by Samsung Electronics Co. Ltd., Kyungki-Do, Korea, on a shared bit-line NAND cell that would allow chips with capacities of up to 256 Mbits.

The cell employs a booster plate and a polysilicon-spacer local-oxidation isolation region. That booster plate ups the cell current so that a current of 4 μA flows in the 32-transistor cell string—a value larger than that of the conventional NAND flash memory with 16 transistors. That higher current provides better biasing and control of the programming and sensing operations.

Improved circuit densities also were achieved with the shared-bit-line structure since it reduces the cell layout overhead by increasing the number of transistors in the NAND string up to 32. By sharing the bit line so that two NAND strings and a bit-line contact and metal are grouped together, the number of bit-line contacts can be reduced by 50%, and that eases the metallization and chip scaling challenges. In addition, the structure uses a direct contact method instead of butting contacts for the selection transistors. This scheme also leads to simpler processing requirements, lower operating voltages, and zero program disturbances.

To improve overall cell endurance, designers at Mitsubishi, also in Session 7, described how they developed a self-limiting programming scheme to achieve high programming throughputs while avoiding overprogramming (and also early cell deterioration). The structure employs n-channel select transistors in a p-channel-based divided bit-line NOR memory array *(Fig. 4)*. The result: Lower power consumption, faster programming (4 ns/byte), and the ability to obtain a narrow program threshold voltage (V_{th}) distribution so that a bit-by-bit program verify can be used to prevent the overprogramming.

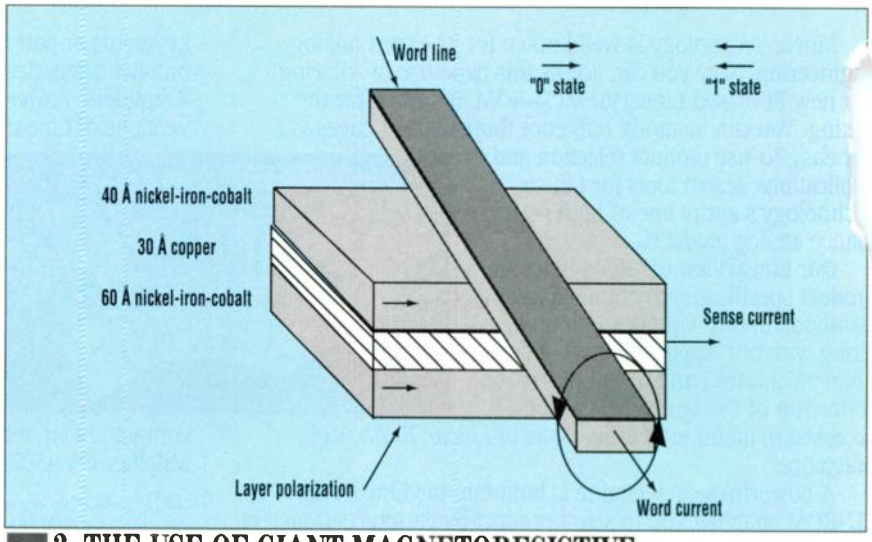
In the scheme, the n-channel transistors are used as the select transistors in the sub-bit lines that are each connected to 64 memory cells. There is no area penalty from the addition of a p-type well since the gate width of the transistor can be reduced. That reduction is possible since n-channel devices offer better current drive than do p-channel devices. To use the n-channel transistors, no additional circuits, such as sense amplifiers, can be added to the chip, and only very short, 0.1-μs −1.5–V pulses have to be added to the program pulses applied to the control gate. The small parasitic capacitance of the sub-bit line to be discharged contributes to the high-speed self-limiting program scheme.



2. A PLUG FORMED from single-crystal silicon is the foundation for a barium-strontium-titanium oxide (BST) capacitor created by Toshiba through epitaxial material growth in three stages. First a layer of platinum/titanium-aluminum nitride is grown, then a strontium/ruthenium-oxide layer is formed. Lastly, a BST layer completes the storage cell, which is just 300-Å thick—the thinnest ferroelectric film reported to date.

Another presentation by Mitsubishi in Session 19 examines the formation of the floating gate—a key aspect to ensure reliable flash-memory performance. In its work, Mitsubishi studied the impact of an in-situ nitrogen and phosphorous co-doped amorphous-silicon layer for use as the floating gate. The combination offers a scalable and reliable technology that can replace current floating-gate oxides.

In the process of manufacturing small-featured flash memory cells, high-energy plasmas are often used for etching and deposition. However, the plasma also can potentially cause damage to the many materials on the silicon, thus degrading storage-cell performance. That's exactly what researchers at Toshiba discovered—newly observed plasma-induced damage that creates two types of leakage currents that affect the performance of circuits fabricated with features below 0.25 μm. To minimize such damage, more careful evaluation of the plasma-



3. THE USE OF GIANT MAGNETORESISTIVE structures, similar to those used in disk-drive read heads, form the basis of a magnetoresistive RAM developed by Motorola. Two nickle-iron-cobalt layers are separated by a 30-Å non-magnetic copper layer to form the storage node. The word line is then routed on top of the storage node. When the word line and sense lines are simultaneoulsy pulsed, the pulse creates a localized magnetic field where the two lines cross, and that field can change the polarization of the NiFeCo layers.

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based equipment should be done along with more in-situ measurements with a fast-feedback mechanism to evaluate new test structures.

In another analysis detailed in Session 13, researchers from Rockwell Semiconductor Systems, Newport Beach, Calif., and the University of California, Irvine, examined the performance of split-gate flash-memory cells. They found that conventional processing of the interpolysilicon oxide layer reduced memory performance, versus the use of a composite oxide formed from thin thermal-oxide and deposited TEOS, which delivers about a threefold improvement in performance and reliability.

Work on creating a model to predict stress-induced leakage currents in flash EEPROM chips is the subject of another paper in Session 13. The work done by IMEC, Leuven, Belgium, resulted in a quantitative model that allows designers to predict the disturb behavior of tunnel-oxide-based devices after write-erase cycling. To implement the model, only a measurement of the oxide quality on capacitors and transistors and the collection of some basic cell characteristics is needed.

A reemergence of the diode-based programmable ROM of the late 1960s might occur if work done by researchers at the Philips Research Laboratories, Eindhoven, The Netherlands, bears fruit. They developed an antifuse-based one-time programmable diode-based storage cell. The small cells allow high-density memory arrays; and when used in arrays, access times of the arrays are comparable to serial mask ROMs and NAND-based EPROMs. When implemented with 0.6-μm design rules, a 103-mm^2 32-Mbit nonvolatile test chip demonstrated full operation.

The merged diode and antifuse cell is fabricated by first implanting an n well and a masked buried p^+ layer into an n-type substrate and then growing a 1-μm-thick n^- epitaxial layer. The buried layer reduces the series resistance in the bit lines and acts as a PMOS source/drain. NMOS source/drain regions and a p^+ channel stopper are then implanted and next, deep but narrow trenches are etched to below the buried layer. The trenches are then filled in with oxide and polysilicon. A thick oxide layer on top of the trenches, and a 50-nm-thick gate oxide for the peripheral logic, are then grown.

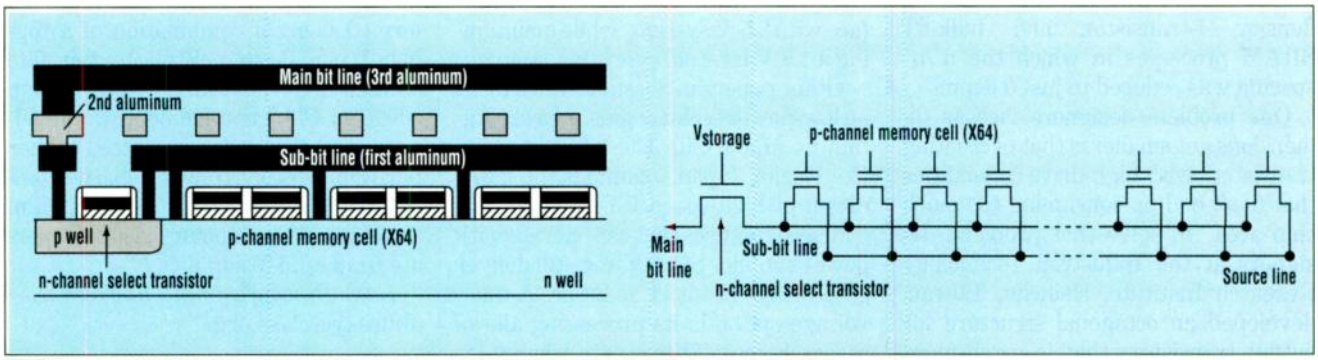
After a p^- implant in the bit lines and PMOS source/drain areas, a 6-nm-thick gate oxide is formed in the memory array. Contacts to silicon are then opened and polysilicon is deposited and n^+-doped to form work lines, transistor gates, and diodes in the periphery. Lastly, one layer of metallization and a passivation layer are added. In all, the 11-mask process is relatively simple and should allow the memories to be fabricated quickly and at minimal cost.

When implementing high-density memories or other products, the minimization of the separation between elements on the chip becomes especially critical when hundreds of millions of transistors must be crammed together. Consequently, trench-type isolation schemes have become very popular since they result in very tight spacing. However, etching the trenches is a critical step and simpler processes such as local oxidation of silicon (LOCOS) would be preferred if they could achieve the reduced spacing.

One such improved LOCOS process, detailed by Samsung Electronics Ltd., Kyungki-Do, Korea in Session 32, employs a nitride-cladded polysilicon spacer with LOCOS that eliminates the bird's-beak encroachment to achieve spacings that would make possible gigabit-density DRAMs. To do the fabrication, researchers employ a specialized rapid-thermal CVD system to deposit the very thin silicon-nitride layer. The result is that devices in the memory's peripheral logic area can be placed just 0.32 μm apart, thus improving circuit density.

In the same session, researchers at Texas Instruments explored the combination of LOCOS and trench schemes for a CMOS process that employs 0.18 to 0.25-μm features. One problem with trench technology is the leakage currents and electric fields that are often found at the corners of the trenches. A new approach detailed by TI researchers performs trench corner engineering which rounds corners, creates a sloped trench wall, and provides other benefits to reduce electrical stress in the trenches. Intrawell isolation spaces of 0.3 μm (limited by i-line lithography) and interwell n^+ to p^+ isolation spaces of 0.6 mm are achievable and CMOS drive currents of 660 μA/mm for NMOS and 290 μA/mm for PMOS (40 Å/1.8 V) have been obtained.

Another paper in the same session that explores corner rounding to reduce stress is presented by Toshiba. Focused on the benefit to flash-memory cells fabricated with 0.25-μm design rules, the paper examines the stress-induced



4. A COMBINATION OF N-CHANNEL SELECT TRANSISTORS and p-channel memory cells form the basic 64 memory cell sub-block that connects to a sub-bit-line in the divided bit-line NOR flash memory (right). Developed by Mitsubishi, the n-channel select transistors replace p-channel transistors and do not add any area penalty, even though a p well must be formed (left). No penalty is encountered since the gate width of n-channel devices can be reduced versus the gate width of p-channel devices, since n-type transistors have much higher current-drive capabilities if the gate widths were equal.

LATE PAPERS

Four exciting late papers on digital developments were received at press time involving a GaAs MOSFET, an aluminum plug technology, and two papers on single-electron silicon memories.

Researchers at Bell Laboratories, Lucent Technologies, Murray Hill, N.J., report on the first demonstration of an enhancement-mode p-channel GaAs MOSFET realized directly on a semi-insulating GaAs substrate with full ion implantation (Session 10). The device has a 40-by-50-μm gate and shows very good dc characteristics with transconductance of 0.3 mS/mm and an excellent gate-breakdown field of more than 3 MV/cm. The process employed is compatible with commercial GaAs MESFET processes.

At Fujitsu Laboratories Ltd., Astugi, Japan, researchers devised a novel high-aspect-ratio aluminum plug for logic/DRAM LSI ICs using a polysilicon-aluminum substitute (PAS) (Session 14). The single-crystal aluminum plugs have aspect ratios of over 7. To form the plug, a via hole was first filled with polysilicon by CVD and aluminum was deposited on the planarized polysilicon plug. An aluminum plug was substituted for the polysilicon by annealing. Via holes having a minimum diameter of 0.175 μm and a depth of 1.7 μm (a greater than 10 aspect ratio) were filled with aluminum. According to the researchers, the process looks promising for future CPUs and DRAMs.

Room-temperature operation of a silicon single-electron memory with a self-aligned floating-dot gate also was achieved by researchers at Fujitsu (paper 21.9). The memory, which promises to make single-electron devices extremely practical, is composed of a narrow-channel FET device that's fabricated with an ultra-small gate.

Researchers at the University of Minnesota in Minneapolis also demonstrated a silicon single-electron MOS memory with a nanoscale floating gate and a narrow channel (Session 21). Channel width is on the order of 7 nm. A nanoscale polysilicon dot (on the order of 7 by 7 nm) is used as the floating gate and is embedded between the channel and the control gate.

leakage and how the rounding process helps reduce the electric field and thus the stress. That would greatly improve the reliability and data-retention capability of flash-memory chips with densities of 256 Mbits and larger.

Avoiding some of the traditional problems with 0.25-μm trench technology, designers at United Microelectronics Corp., Hsin-Chu, Taiwan, have crafted a novel shallow-trench isolation technology. The shallow-trench structure eliminates the field crowding at the active edge, which, in turn, minimizes the kink effect that distorts the drain voltage versus current curves, thus providing excellent isolation and better transistor characterists. Designers at UMC applied the technology to high-density 4-transistor, and bulk-6T SRAM processes in which the n^+/p^+ spacing was reduced to just 0.6 mm.

One problem designers face as dimensions get smaller is that of creating transistors with high-drive capabilities that don't end up consuming too much chip area. To solve that problem, designers at the Industrial Technology Research Institute, Hsinchu, Taiwan, developed an octagonal structure for output transistors that is much more area efficient than previous approaches. Detailed in Session 34, the cell structure for the buffer allows a maximum sink current of 13.12 $\mu A/\mu m^2$ for NMOS devices and half that for PMOS devices, which is almost 48% better than possible with a traditional fingered-transistor layout.

Low-voltage operation is another issue that researchers will pay a lot of attention to at this year's conference. For instance, in Session 33, Intel Corp., Hillsboro, Ore., describes a high-performance 0.25-mm CMOS process that can operate from a 1.8-V power supply. Used to implement a 4-Mbit static RAM, the process, along with five layers of metal (three for internal cell connections and two for power and word-line straps that would meld in with 5-level metal logic processes), keeps the cell size to just 10.26 μm^2 for a six-transistor memory cell. Special I/O circuitry allows the technology to interface with 2.5-V systems while maintaining a 1.8-V internal operating voltage.

Other papers in Session 21 also focus on low-power technologies. A presentation by Matsushita Electric Industrial Co., Osaka, Japan, examines the fabrication of high-speed 0.1-μm dual-gate CMOS structures that can operate with power supplies of 1.5 V and still deliver gate delays as short as 28 ps. A dual-voltage option in its processing allows researchers at TI to create a sub-0.18-μm CMOS technology that delivers high performance when operated with a 1.5-V supply, and low power with a reduced speed of just 40 ps (for an inverter stage) when operated from a 1-V power supply.

Low-voltage static RAMs also are a topic of interest in Session 11. Mitsubishi and NEC, among others, show off combinations of novel technology and innovative processing to implement megabit memories that operate at 1.5-V supply levels. Also finding a way to reduce cell size drastically, designers at Mitsubishi created a C-switch cell (complementary-switch cell) that uses a high-performance p-channel thin-film transistor for the access transistor in addition to the load transistors. Such an approach reduces the cell size by 84% versus cells fabricated using straightforward projections of the technology.

A more conventional SRAM cell was formed using a combination of a top-gated p^-/n drain polysilicon thin-film transistor for loads and 0.3-μm design rules. A 64-kbit test memory was developed, and it has demonstrated higher performance than conventional bottom-gated lightly-doped offset thin-film transistors. The memory also can operate from a 1.5-V supply. □

Dave Bursky's e-mail address is: dbursky@class.org.

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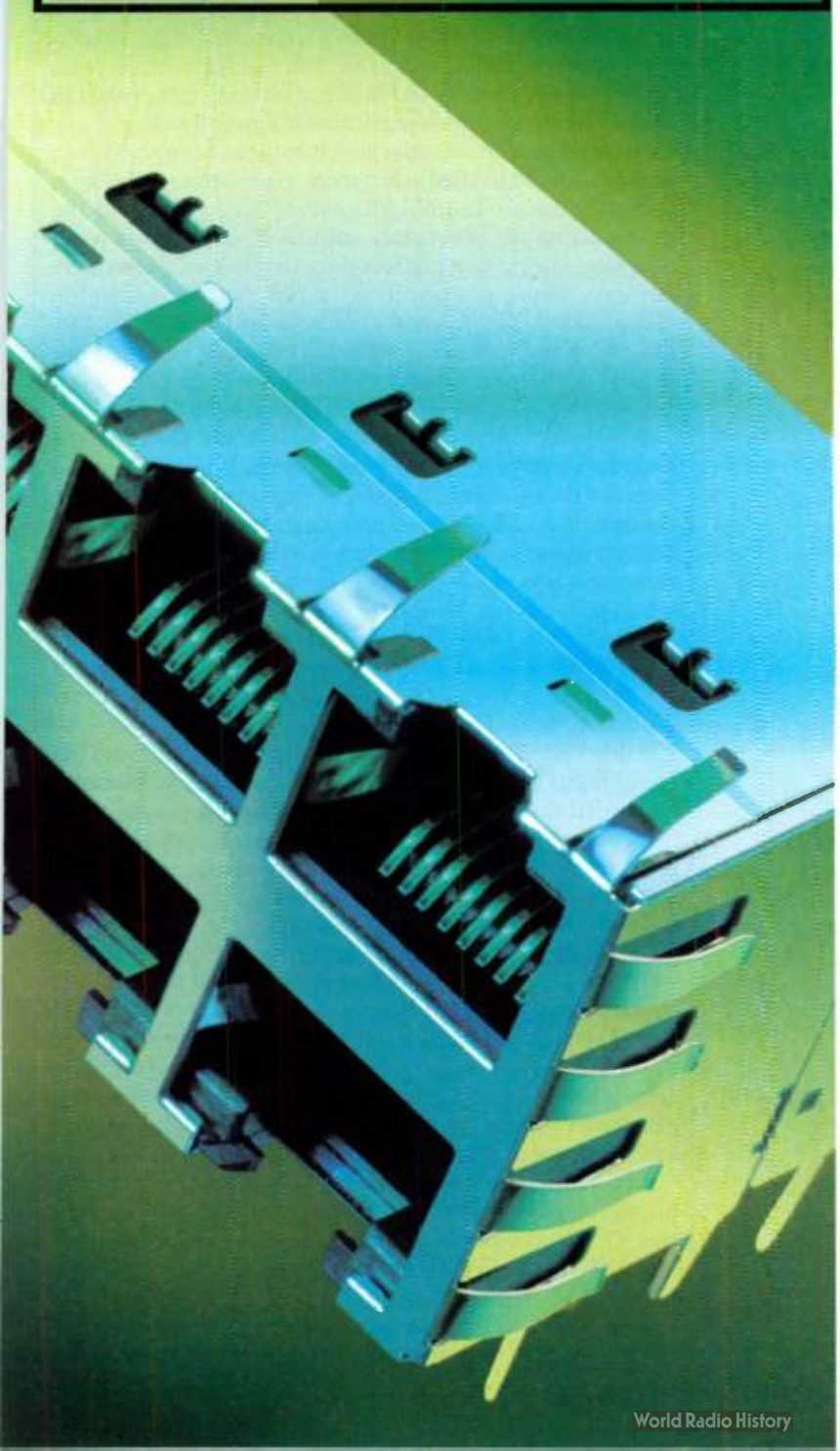

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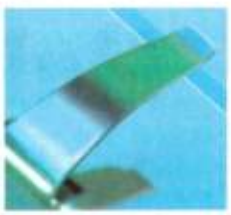

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Modeling And Simulation Make Designing Easier

Advances In The Development Of Modeling And Simulation Tools Offer Increased Predictability And Optimized Design Capabilities.

By Cheryl Ajluni

Modeling and simulation take an important seat at this year's IEDM conference with no fewer than five sessions dedicated to investigating advances in everything from oxidation and implant modeling to interconnect and statistical modeling. The need for accurate design models and efficient simulators is obvious. Accurate modeling leads to properly characterized designs by enabling the development of databases of parameters and guidelines the designer uses to optimize a design. It can provide the designer with the predictive ability to perform analysis, and make simulations easier and quicker to run. Efficient simulators come into play because they use information from the models to predict whether or not a particular design will work.

In certain instances in the past, it only has been possible to simulate the individual component pieces that make up a particular design. The difficulty with this is that although the pieces may work as separate entities, their integration can sometimes bring about interactions that not only cause performance issues not previously noted, but also cause the design to fail. With current trends toward shorter product life cycles and increased performance needs, new and improved models and simulators have become crucial tools in the design cycle and key enablers of successful designs.

Session 6, "Compact modeling," specifically addresses the need for accurate models and good simulation by focusing on both newly devised and upgraded compact models for circuit simulation. With RF-based applications becoming more popular, it's no wonder why four of the scheduled seven papers hit on some aspect of RF circuit applications. Researchers from Texas Instruments, Dallas, for example, will discuss the development of a CAD-compatible non-quasi-static (NQS) formulation for silicon MOSFET models. Based on numerical device simulations, this model is much more accurate than previously developed NQS models.

A joint effort out of Stanford University in Calif., and the Hong Kong University of Science & Technology, Kowloon, succeeded in developing a physical model for planar spiral inductors on silicon. Details of this effort, including insight into the recent attention on the use of planar spiral inductors on silicon for RF communication circuits, will be presented.

From the University of Florence and the University of Bologna, both in Italy, comes an accounting of multifinger effects in models for GaAs MESFETS. The last paper on RF circuits discusses the development of a PISCES-HB-based circuit simulation tool for the harmonic distortion analysis of GaAs MESFET circuits. A joint effort by Matsushita Electronics Corporation, Osaka, Japan, and Stanford University, Stanford, Calif., features details of an analysis of intermodulation distortion characteristics also will be offered.

Of particular interest in the session is a paper entitled "A physically-based built-in Spice polysilicon (thin-film transistor) TFT model for circuit simulation and reliability evaluation". With the maturation of polysilicon TFT technology, many analog and digital circuits not before possible have now become feasible. Without accurate circuit models though, circuit integration is severely limited. Development of an

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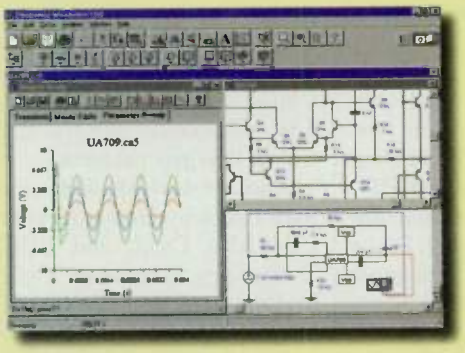

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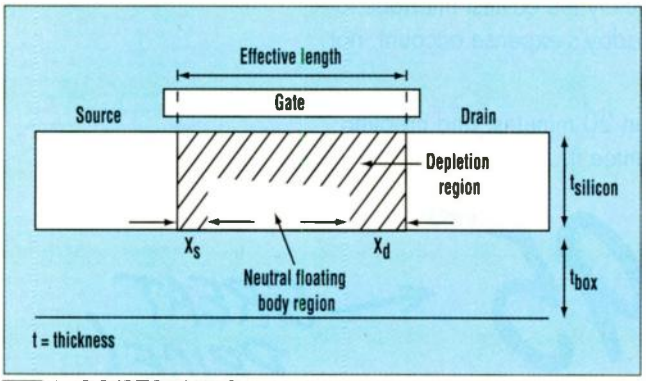
accurate polysilicon TFT circuit model is crucial. While there are some models available today, they have yet to be implemented in a commercially available circuit simulator. The model developed by the National Chiao Tung University, Taiwan, offers a solution not only in Spice, but can be combined with a device degradation model to evaluate circuit reliability. According to the developers, Steve Chung, Darren Chen, C. Cheng, and C. Yeh, part of its completeness lies in the fact that "in the I-V model, not only are the trap density and potential barrier height modeled, but also the small geometry effect, parasitic BJT effect, off-state and subthreshold current are considered. In the C-V model, consistent-derivation charge conservation is obtained and the BJT effect is also considered."



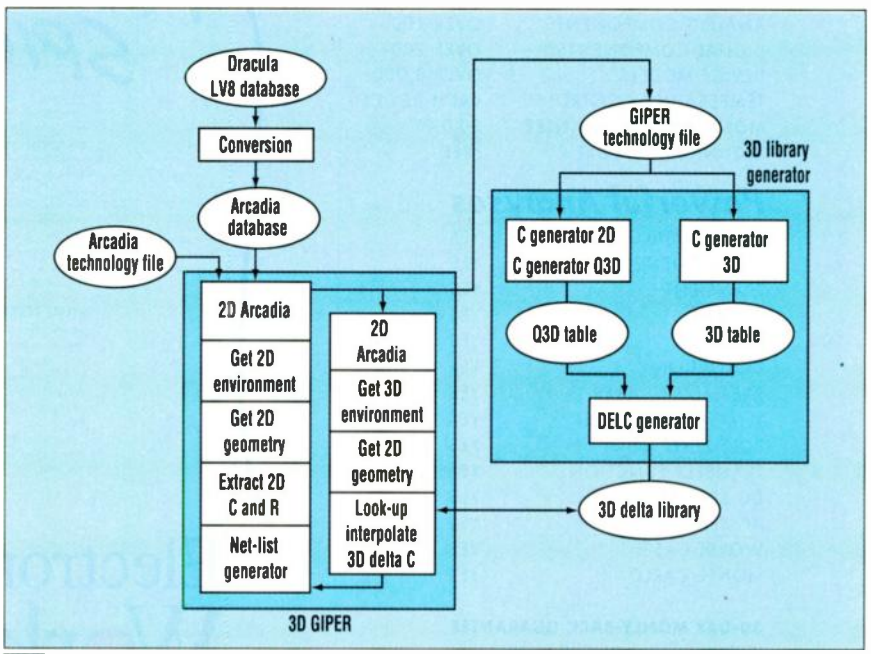
1. SCHEMATIC of the SOI device structure. The extent of the body depletion region depends on the silicon film thickness, channel length, and applied bias conditions.

Another interesting development is discussed in "A continuous compact MOSFET model for SOI with automatic transitions between fully and partially depleted device behavior". The development, a fully-continuous compact-SOI model for circuit simulations that automatically accounts for the correct body depletion condition, differs from previously available models in that it accounts for the possible transitions between fully-depleted (FD) and partially-depleted (PD) behavior during device operation *(Fig. 1)*. Details of the model, which can be used for analysis and design of SOI circuits, will be presented. Specific attention will focus on how a surface potential solution was coupled with the full depletion condition for body charge to derive a general-compact SOI model.

In Session 15, "Device modeling," seven papers all address issues related to both hot-carrier and transport phenomena in silicon MOSFETS. One of the more notable developments comes out of Purdue University, West Lafayette, Indiana. It focuses on the use of an alternative treatment of carrier transport to create a simple analytical model that can be applied to short-channel device issues. The importance of this development lies in its ability to provide a new, physical picture of the small MOSFET, while acting as a tool useful in interpreting experiments and detailed simulations. Details of this new approach are presented in "Scattering theory of the short-channel MOSFET".

Session 23 on "Interconnect and statistical modeling" offers insight into a number of topics including interconnect models for critical path, signal integrity, and substrate coupling analysis; and statistical models for device geometry, device performance, and Spice model generation. In "A statistical critical dimension control at CMOS cell level," the methodology calls for the integration of response surface functions (RSF) and aerial 3D image simulation to model CD distributions in a manner so powerful, sensitivity of whole gate patterns at the CMOS cell level is possible. According to the developers, "Response surface functions for the CD in the lithography are designed by using a full 3D aerial image simulator. The RSF is extended to the CD in line/gap patterns. A new relationship for the CD in line and arbitrary gap patterns is further found. Response of gate patterns at CMOS cell level is calculated from the new relationship and the RSF for the CD in line/gap patterns".

Another development comes out of a joint effort by Hewlett-Packard Labs, Palo Alto, Calif., and EPIC Design Technology, Sunnyvale, Calif. Funded by Sematech, the 3D GIPER project has developed a 3D global interconnect parameter extractor that provides a practical extraction tool for full-chip global critical path analysis. The GIPER tool can extract interconnect parameters of a typical global interconnect within several minutes per net on



2. BLOCK DIAGRAM of the 3D GIPER. GIPER consists of a 3D delta library and 2D/3D Arcadia. First, 2D Arcadia extracts all 2D capacitances and resistances. Then, GIPER converts Arcadia technology file into its own technology file and generates a 3D delta library. The 3D Arcadia identifies 3D geometries, extracts 3D geometry parameters, and corrects for 3D fringing capacitance by looking up the GIPER 3D delta library. RC extraction time in GIPER is significantly improved while maintaining accuracy.

an HP workstation *(Fig. 2)*. Compared to a full 3D simulator, the GIPER has an accuracy of within 5%.

This development is significant because until now modeling tools and methodologies for the global interconnect, especially parameter extraction, have not been well defined. Today's conventional tools use 2D models, but to truly take into consideration multilevel interconnect capacitance, 3D fringing is needed. Without it, errors in total capacitance of up to 20-30% can occur. The tool makes use of 3D fringing, while maintaining reasonable CPU times. Details are given in "3D GIPER: global interconnect parameter extractor for full-chip global critical path analysis."

While the benefits of simulation seem obvious for things like IC and pc-board design, it's not usually thought of as a step in display device design. Although, in much the same way that pc-board design must take into account a multitude of constraints and component interactions, AMLCDs consist of a number of different components such as TFTs, LCDs, and optical components that also must be considered during the design stage. Also, judging the success of a display design based solely on the performance of its components can be a difficult and relatively inexact task at best.

Liquid, a simulation tool for AMLCDs, from Technology Modeling Associates, Sunnyvale, Calif., takes these considerations into account by providing, within one package, all the solvers needed to simulate the display. Controlled by a single GUI, it contains a number of simulation blocks including LCD, optical, TFT, cell electrical, array, and common electrode analyses. Each solver for the individual simulation blocks produces results in a look-up table. The tool works by simulating the entire display and presenting the results as a reconstructed image as it would appear on the display. The analysis provides results in minutes on a workstation. Details of the simulation tool, including insight into how individual simulation blocks operate and interact, can be found in "Liquid, a complete simulation system for AMLCDs."

Sessions 28 and 31, "Process modeling I—oxidation and implant modeling" and "Process modeling II—Diffusion," respectively, address different components that are crucial for the modeling of these processes.

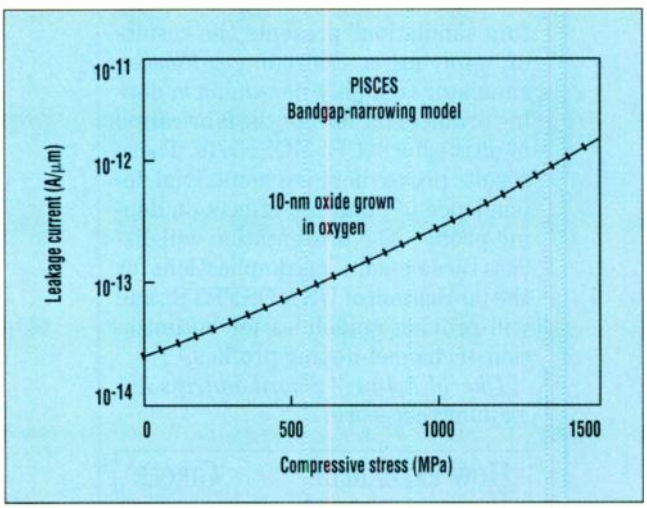
For example, in "The influence of oxidation-induced stress on the generation current and its impact on scaled device performance," the influence of such a component in the fabrication of junction and gated diodes and NMOS FETs is discussed. As device dimensions continue to decrease, the impact of the isolation process on device performance becomes increasingly important. Consequently, the buildup of localized stress near the isolation edge, a factor contributing to the formation of dislocations and device characteristic alterations, becomes a major concern when scaling LOCOS and shallow trench isolation structures (STI).

The presentation will report on the results of an experimental model based on stress-induced bandgap narrowing, which prove that even when no dislocations are formed, a reduction in isolation pitch can severely degrade device characteristics caused by high localized stresses. According to the developers, Peter Smeys, Peter Grifin, Zofia Rek, Ingrid De Wolf, and Krishna Saraswat, "As the active area pitch decreases, an increase in stress is observed. This may in part explain the increased leakage currents often observed in scaled STI isolation devices. In order to estimate the effect of this stress on leakage current, the bandgap narrowing model has been incorporated into the device simulator PISCES *(Fig. 3)*. The same trend is observed as in the experimental stress dependence of the perimeter leakage current."

The introduction of a physically-based ion-implantation damage model to predict both the as-implanted impurity profiles (SIMS) and the damage profiles (RBS), as well as amorphous layer thicknesses for high dose implants, is the aim of a paper entitled "Monte Carlo simulation of the ion-implantation damage process in silicon." Because ion-implantation damage is a required element for transient enhanced diffusion (TED) simulation, and for simulating the defect dechanneling effect, a model such as the one presented in this paper is a prime commodity. Previous damage models have failed to accurately predict damage profiles due to over-simplified incomplete physical models. This new model, however, developed at the Microelectronics Research Center at the University of Texas in Austin, explicitly simulates the defect production and its subsequent evolution into the as-implanted experimentally observed profiles.

Key to this damage model is that, for the first time, it enables simulation of the defect diffusion and interaction/reaction at or near room temperature after each ion cascade. The presentation will highlight the model's details, gives examples of single and multiple cascades from arsenic and boron implants, and examines the implications of the damage-model's ability to provide insight into the fundamental physical processes in implantation damage.

In "Modeling of boron, phosphorous, and arsenic implants into single-crystal silicon over a wide energy range (few keV to several MeV)," one comprehensive model, combined with previously developed models for damage accumulation, is used to cover the wide range of energies, as well as on-axis and off-axis implantations and to allow physical-based simulation of 3D profiles. According to the developers, S. Morris, B. Obradovic, S. Yang, and A. Tasch, "The key to having a single, comprehensive model over such a wide energy range is to correctly model



3. PISCES SIMULATIONS of diode leakage current as a function of uniform compressive stress along the width direction. A constant stress across the junction is assumed in this case.

IEDM—SIMULATION/ MODELING

the electronic stopping of the ion. This stopping in a crystal constitutes a significant fraction of the energy loss, and for light ions or high energies, it can be the dominant energy loss. Understanding the components of this electronic energy loss is crucial to establishing a model which can be successfully applied over such a wide energy range and for multiple implant species." The final form of the comprehensive model combines the proton stopping model with the appropriate components of the ionization model, and the energy stripping criteria. Details of the model's implementation as well as its implications will be discussed during the session.

The second part of the series will address advances in several aspects of TED, including high-energy implants, combined TED and oxidation enhanced diffusion, and the effects of temperature ramps, together with applications to the reverse short-channel effect in devices. In "Modeling transient diffusion following high energy implantation," Researchers from Bell Laboratories' Lucent Technologies, Murray Hill, N.J., present data to substantiate the energy dependence of TED for shallow markers. This dependence was discovered during simulation to design a high-energy implant tub process flow that could act as a replacement for an existing 0.5-μm CMOS process flow. Details of this discovery as well as the tub replacement fabricated using a high-energy implant process will presented.

"Optimization of channel profiles for ultra-short MOSFETs by quantum simulation" presents the results of applying a Schrodinger-Poisson simulator to highly non-uniform doping profiles suitable for the fabrication of ultra-short (US) MOSFETs. These results prove there is a non-trivial dependence of quantum effects on doping profile. The presentation will discuss these results, the implications for the fabrication of US MOSFETS., and will provide guidelines for optimization of channel-doping profiles. □

Cheryl Ajluni's e-mail address is: cjajluni@class.org.

How Valuable?	Circle
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Moderately	538
Slightly	539

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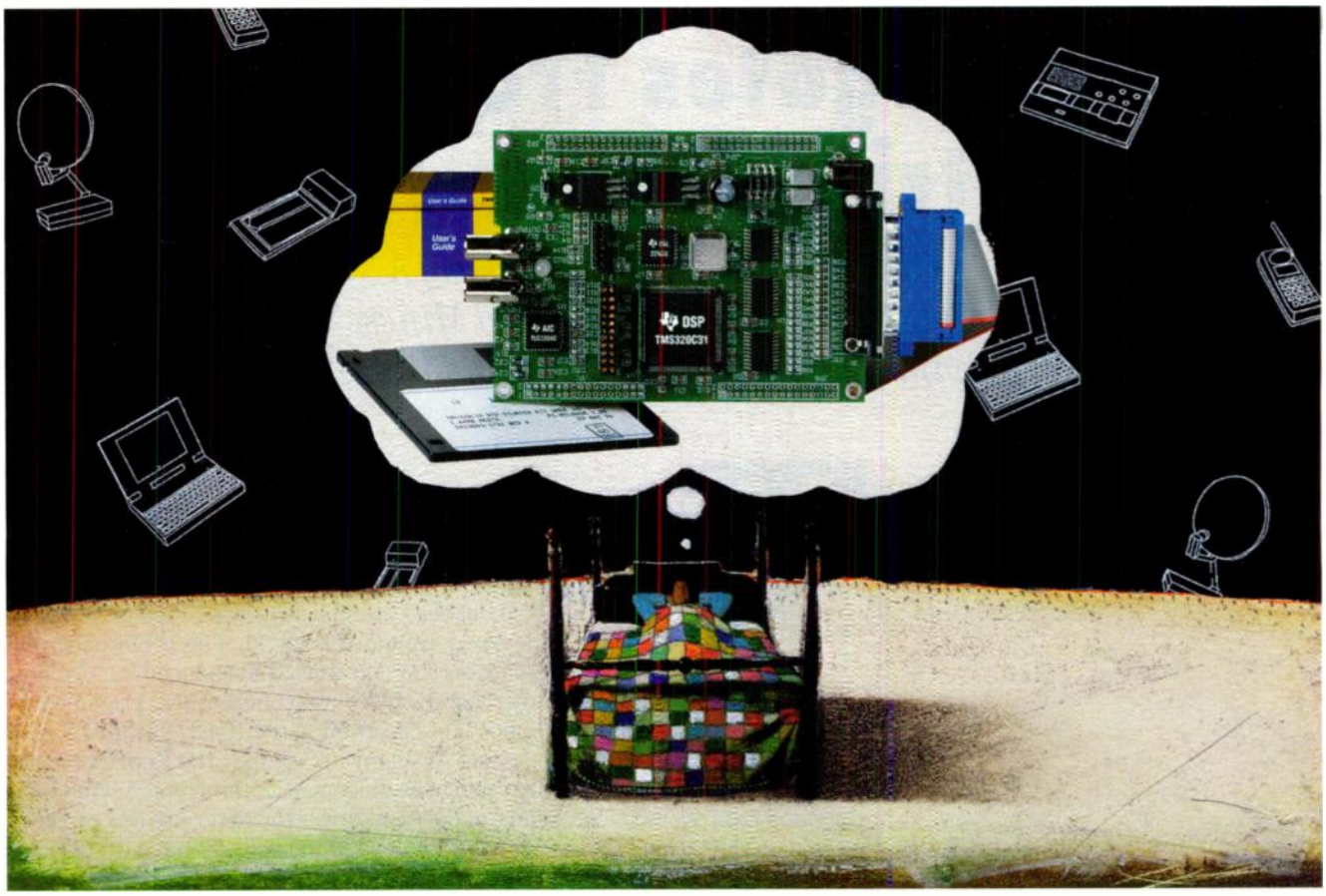

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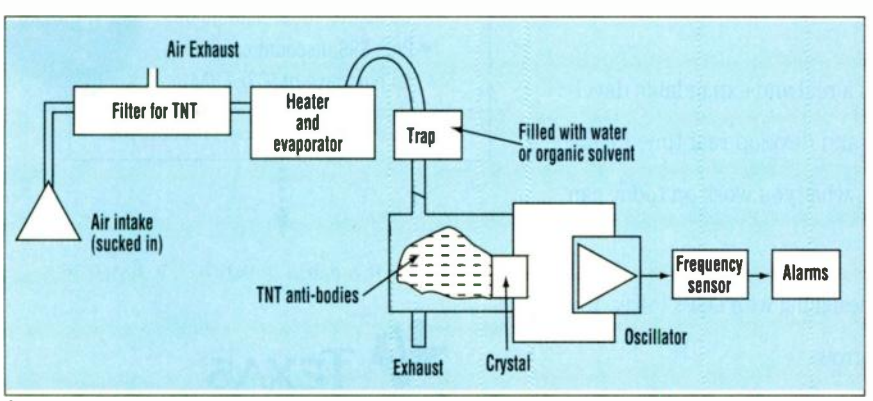
Creative Technologies Seeking A Solution To Abandoned Land Mines: An Impressive Spread Of Hope And Dignity.

PAUL MCGOLDRICK

There surely cannot be a better expression of civilization than to show and work for one's fellow man. For three days (Oct. 7-9), hundreds of delegates from 21 countries gathered in Edinburgh, Scotland, to talk about the potential solutions to the problems of abandoned land mines around the world. The conference, the EUREL Conference on The Detection of Abandoned Land Mines, was sponsored by the U.K. Institution of Electrical Engineers in association with the Chinese Institute of Electronics, the IEEE in the U.S., the Institute of Physics, the U.S. National Academy of Sciences, the Remote Sensor Society, and the South African Institute of Engineers, with the support of the Joint Research Centre of the European Commission. It was the first conference ever to be held on the technology that may be involved in the detection and destruction of abandoned land mines.

As Professor Roger Voles, chairman of the organizing committee, pointed out, at the same time the conference was being held, 100 more people would be killed, 10,000 new land mines would be laid, and only 1000 would be cleared. The present means of detecting and removing mines are basically unchanged since World War II: Teams of men with bayonets prod the terrain, and when they find a possible target, the object must be uncovered, identified, and if it is explosive, destroyed. The ratio of false targets to actual targets is in the 100s-to-1 because of battlefield shrapnel and other mines that are nonexplosive. Metal detectors are still the primary sensor for the mines and they are, of course, useless with minimal-metal or plastic devices.

Dr. Rolf Linkohr, one of the two keynote speakers, is a member of the European Parliament and a physicist by training and inclination. He has sought a research grant of 50 million ECUs (about $65 million) for a 30-month R&D program to be run by the Joint Research Centre of the European Community to identify a probable solution to mines clearance. It is, however, hardly a European problem alone. The former Yugoslavia is a mine-infested area, but apart from the former Soviet Union—where the state of abandoned mines is unknown—it is the only territory within expanded European boundaries that is infected.



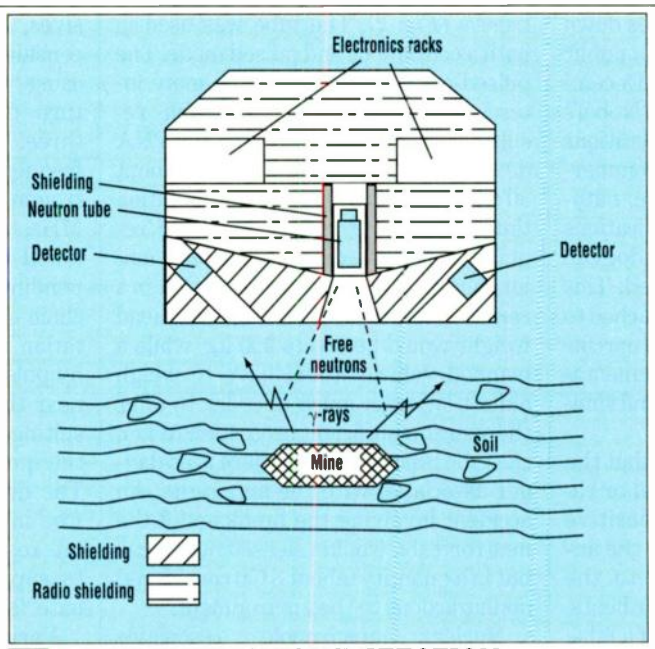
1. PRINCIPLES OF THE BOFORS antibody gas detection system with the mass of a crystal being changed in the presence of a known explosive.

The crash program was detailed by Professor Rudolph Winter, director of the Space Applications Centre of the JRC at Ispra, Italy, who said that the number of abandoned mines was estimated to exceed 100 million and that another 150 million are stockpiled around the world. Some 67 countries have reported mine incidents, with 20 of those countries reporting serious problems; 75 different types of mine have been identified; and with 2 to 2.5 million more mines laid every

year, the humanitarian clearance of 100,000 per year can never catch up.

At an average present cost of clearance of between $200 and $1000 per mine, the budgets to just keep pace would exceed $9 billion per year. JRC is seeking an immediate 50-fold increase in the rate of clearance—while knowing that the solution will not be perfect—with a major concern being the ability to declare an area noninfested in a very short time. Although international law requires the combatants in a war to record the locations and types of mine that have been laid, this does not, of course, happen, and a great deal of demining time is wasted in declaring safe areas that are and always were, in fact, clear. Until this happens, the local populations do not enter the areas and some countries are now in a state where a lack of usable land for food production has created a potential famine problem.

The JRC envisions that their program will not rely on a single-sensor solution and that the combination will probably include a 3-axis induction gradiometer, ground-penetrating radar and infrared (IR) imaging. The most important constituent, however, is believed to be the image-processing system where vast amounts of data from the sensors can be combined and processed in as near to real time as possible. The ambitious plan allows for five months for design, 14 months for development of the basic hardware and software, eight months for integration, and three months for testing. All the clocks would start running as soon as the budget is approved, which the EC has done in principle, but not by due process. It has been made a condition of funding that no companies that have been involved in the production of mines will be allowed to be involved, even though it is appreciated that they might have a unique perspective on the locating of their own products.



2. THE IRRIDIATION/DETECTION head of an FNA/TNA neutron-interrogation analysis system.

COPYING THE CANINE

One of the best tools in a minefield is the dog. The Alsatian (German Shepherd) has a nose that is extraordinarily sensitive; it is believed that it can detect TNT in concentrations of five parts per billion, with the result that it can detect even a buried anti-personnel mine at a distance of five meters. The dog needs to be trained (for about six months), needs to be handled correctly, needs to be fed, and like a human being gets tired—with fatal results. Achieving results like a dog using a "technology nose" would be a massive breakthrough in the detection of the explosive content of the mine or unexploded ordinance (UXO) without regard to whether the packaging is metal, minimal metal or plastic. Nonmetal mines continuously leak explosive vapors, while metal devices will start to leak within a few weeks or a month depending on the moisture levels in the soil.

Professor J. W. Leonhardt of the Berlin Institut fur Umwelttechnik, an expatriate of the former Soviet Union, has the task of clearing all the battle and training grounds of the former East Germany of ordinance that is lying there. The spread of weapons, including chemical devices, is immense. One of his groups has been working on an ion-mobility spectrometer (IMS) that sucks in gas from the target area where it enters an ionization chamber in a tube. The ionizing source has its molecules driven through a shuttered grid, focusing potential rings and through an aperture to a collector. The current that passes from the collector is in time-terms a description of the content of the gas. Each molecule provides a unique signature. It is possible, says Professor Leonhardt, that the system could be made sensitive enough for individual device location, but certainly it's usable for an area's general all-clear, or for an area's quality-control after mine clearance has taken place.

As an aside in the conference, a representative from Daimler-Benz Aerospace noted that they were working on integrating an IMS on a single chip.

But perhaps the biggest canine-copying device to date came from an unexpected source. The Bofors company of Sweden has made its fortune from the developments of its founder, Alfred Nobel. Bofors has now formed a new company, Bofors Applied Technologies AB, that is working on defeating its 100 years of violent history. The biosensor they are working on is being developed by a research team in Israel. It is, essentially, a chemical device that requires gas from a contaminated site to be liquefied after being gathered from the immediate atmosphere *(Fig. 1)*. The liquid passes over a crystal that is part of a standard oscillator circuit running between 8 and 9 MHz.

At this frequency, of course, the natural oscillation frequency is very sensitive to the mass of the resonator. Located on the crystal are living antibody organisms for the type of explosive being detected. If, for example, you are looking for TNT—as Bofors are at the moment—then the presence of any TNT vapor that has been liquefied will cause antibodies to detach themselves from the crystal and attack the molecules. The concentration of vapor will define how many antibodies are detached—the larger the number, the greater the change in frequency of the oscillator, with frequencies up to 300 Hz being quite possible.

To detect other explosives, the crystal could be loaded with a mixture of suitable antibodies or a string of individually-tuned crystals could be mounted in a single liquid sample. The belief is that this system will be better

than the canine with sensitivities down to <10 pg. Bofors hopes to give a public demonstration of the system on December 10, the 100th anniversary of Nobel's death. If proven, and their expectations are high, the system could be in commercial use by mid-1998. There are, naturally, many other possible applications for the device: Anywhere that a dog can be used, the system can be used. This means that antibodies can be attached to look for the whole range of illegal narcotics, and commercially the implementation for the security of airports and similar areas could be immense.

A negative of the process is that the crystal will have to be replaced or recharged after a number of positive detections have been made, as the antibodies cannot be returned to the crystal after reaction with their hosts. There is, however, no chance of a false detection and the fundamental frequency of the oscillator circuit will clearly indicate the quantity of antibodies left on the crystal.

Neutrons And Nuclear

Fast and thermal neutron interrogation analyses (FNA and TNA) have been qualified by France's SODERN as being powerful close-distance methods for identifying the presence of explosives from all the constituent elements: Carbon, nitrogen, oxygen and hydrogen, as well as some of the other constituents of soil, such as silicon, calcium, and aluminum. Nuclear methods are based on the excitation of elements—from the soil, and any explosives—by gamma rays or neutrons, and on the detection of emitted gamma rays or neutrons. Work has been focused on excitation using a 14-MeV sealed neutron tube. Shown is an indication of the typical composition of soil and a mine *(see the table)*.

The gamma emission from each of these elements is in the range of 1 to 12 MeV, either in FNA or in TNA modes. As a consequence, the maximum measurement depth has been found to be sufficient, while limited by the mean-free path of neutron and gamma rays, and by the noise coming from equipment and from soil around the mine. A good screening by collimation and by time selection allows the detection of the elements of interest in a simple way.

A mockup of such a system was made using a neutron tube emitting 10^8 neutrons/s *(Fig. 2)*. The tube was used in both a continuous and pulsed mode. The pulsed mode proved to be the more interesting and yielded comparable results between a spilt FNA and TNA detector with observed depths to about 30 cm with relatively small computation times. The nature of the shielding required in the detector is, however, a major concern and it is anticipated that in a remotely-controlled vehicle, the head weight would be 300 to 400 kg, while a manned vehicle would have to weigh almost twice as much in order to offer the operator sufficient protection. When the tube is not powered, there is no danger associated with the apparatus. An accident involving the breakage of the neutron tube would release tritium gas but in a quantity (about 3 Ci) considered nonhazardous to the environment.

Nuclear quadrupole resonance (NQR) is under investigation by King's College, London, U.K. The principle of NQR is that applied radiation drives transitions between the different energy levels of an atomic nucleus. The levels arise because the charge distribution of many nucleii is not spherically symmetrical but behaves as if it consisted of two electric dipoles back-to-back. One orientation of a nucleus, such as that of ^{14}N, has a lower energy level than the other. Higher-level nucleii will tend to orient themselves to the state of the lower level. Because they also have spin, they behave as gyromagnets and respond by precessing about the axis of the electric-field gradient at the quadrupole precession frequency, whose amplitude depends on the moment and the gradient of the field. In the general case, there are three levels and three allowed transitions. Frequencies are related by one being the sum of the other two.

These frequencies can only be detected in solids and they have been observed in all three principal high explosives, RDX, PETN, and TNT, but at considerably different frequencies because of the chemically different nature of the nitrogen atoms in the three. For example, the set of three frequencies in RDX, from the ring nitrogen nuclei, are 5.2, 3.4, and 1.8 MHz, whereas those from TNT are found between 730 and 900 kHz depending on whether it is the monoclinic or orthorhombic form. The excitation for level changes can be made by pulsed RF with the frequency at or near the NQR frequency, and the resulting frequency can be monitored in the quiescent periods between pulses. The first signal seen is known as the free induction decay (FID) and there are resulting echoes that can be used to support measurements and eliminate false signals.

Various RF probes and antennas have been investigated but a number of real-life problems exist in the implementation of a practical system. Those materials that have NQR frequencies lower than 1 MHz exhibit results with poor signal-to-noise ratios. Quartz in sandy soils can affect the response from ^{14}N sources, or even mask them. Heavy uses of nitrogen fertilizers may affect the results. Work is, however, continuing on the problems to find pulse, modulation, and detection schemes that will work unambiguously in the field.

Using Your Oven!

Lawrence Carter, a Senior Lecturer at the University of Auckland, New Zealand, has been working on a novel use of a microwave oven. Using the standard 750-W magnetron output (at 2.45 GHz) from the horn antenna in the oven, the New Zealand team showed that a 60-second cycle of irridiation produces a clearly measurable temperature difference on the

THE COMPOSITION OF SOIL AND A MINE IN TERMS OF DENSITY

Element	Soil density (10^{22} atoms/cm^3)	Explosive density (10^{22} atoms/cm^3)
Carbon	0.12	2.95
Hydrogen	1.5	6.4
Oxygen	6.9	2.56
Nitrogen	(see note 1)	1.28
Silicon	1.9	(see note 2)
Calcium	0.038	Not available
Aluminum	0.056	Not available

Notes: 1. Possible fertilizer or chemical. 2. Possible silicon from glass or steels.

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COMPUTERS, COMMUNICATIONS, MICROELECTRONICS

READER SERVICE 119

surface of soil between the area where an object is buried and the remainder. Work has been done on the power reflectivity of different soils under different moisture conditions. The work shows some promise for a possible secondary sensor with measurements down to 0.25 m of buried objects.

The time lag is of concern for real-time searching as is the method of delivering/coupling the energy into the soil. There also has to be concern at the possibilities of the microwave energy causing a spark in the trigger circuit of a mine, and probably of less concern, the heating effects in any metal object that may be buried. These limitations can probably be overcome.

GROUND-PENETRATING RADAR

Of all the techniques potentially available in looking for buried or hidden objects, ground-penetrating radar offers the most current potential and is furthest along in development from numerous sources. The conference proceedings cover these techniques in considerable detail. The essentials seem to be that the lowest frequencies offer the best penetration, but wideband techniques appear to be necessary in order to get the best detail and the highest likelihood of removing clutter. It also is essentially true that all ground-radar techniques are going to be effective only with extremely sophisticated signal-processing techniques, and the systems absolutely require that devices' signatures are either programmed in or are learned in operational conditions. Although the world's major armed forces undoubtedly have examples of just about every mine ever manufactured, their cooperation in allowing signatures to be developed cannot be guaranteed.

The first effective work in ground-penetrating (or ground-probing) radar was reported by Professor Leon Peters, Jr. of Ohio State University in 1979 after the Vietnam War *(Proceedings of the IEEE, Vol. 67, No. 7, pp. 991-1000)*. He demonstrated the location of plastic mines using simple radar and classic predictor-correlator detection techniques. Further work was necessarily undertaken during the Falklands conflict when the Royal Engineers successfully located all of the nine types of mines laid during the conflict; six of those types were plastic or minimal-metal with three being anti-tank and three anti-personnel. Experience was gained with these types in various terrains under extremely wet weather conditions. It was believed that the high success rate was due to the fairly limited range of devices being detected.

Work was discontinued after the conflict as there was no on-going operational necessity for continuation and the leading figures in the RE went on to civilian occupations, taking their detection experiences with them. Even so, for example, using the basic techniques developed during that time, it has taken eight years of development and three versions of hardware and four generations of software for one of the companies, EMRAD, Godalming, Surrey, U.K., to launch a commercially-viable detection system for plastic utility pipes. Development of their Pipe Hawk was funded by the New York Gas Group after extensive review by the Gas Research Institute of Chicago. It can be seen therefore that the development of a system for mines—which, by necessity, must recognize all potential threats—could be some time in development.

KEEP IT SIMPLE, STUPID

As a reminder of how overcome with technology people can be, Mr. K.G. Spouse, a retired engineer, pointed out some fundamentals that could well be relevant in the real world. Remembering that the technology used for mine detection must be simple—because the workers that will be using the equipment will be in the worst imaginable environments with the most basic training possible—Mr. Spouse went back to the basics of induction with eddy currents, an effect that does not depend on a material being conductive. The detector he suggests consists of an inductive probe, the coil of which is mounted vertically in a search probe. This, plus the associated transistor circuitry and a battery, completes the instrument. The inductive probe and capacitor form a tuned circuit that is self-excited at resonance. When the probe is placed close to the soil, there is an eddy current loss caused by the conductivity of the soil, reducing the Q. The losses are less when the coil is above a low-conductivity object, such as a plastic mine, and the output signal increases compared to tracking across soil.

The object is, in fact, analogous to a hole in the ground, acting like a single-turn inductor which is resistively-loaded and inductively-coupled, lightly, to the probe primary. The sensitivity of the system is dependent on the intrinsic Q of the tuned circuit, which is dependent on the frequency used and the length-to-diameter ratio of the search coil. The Q can be increased if the coil is included as part of a regenerative circuit oscillating in the marginal mode, with the loop gain barely exceeding unity at the resonant frequency.

Practical problems in implementing a system really depend on the mechanics of how to search with a constant distance between search coil and the soil (or how it can be corrected automatically) and how the search area can be widened. Otherwise the method becomes another slow system for plastic, complementing the existing, slow, system for metal detection.

WHERE FROM HERE?

The future is not clear. Many of the techniques described at the conference will work. They need considerable future development in order to make them practical solutions in a field where mistakes kill the operator. The fact that a further conference on this matter is being planned for two years ahead is an indication that further work and consolidation will be needed. The most viable solutions will probably be those that offer a commercially attractive secondary market. High on that list must be the Bofors gas-detection system and those systems that can be used by utilities in their normal day's work. It continues to be true that whatever is developed will be of little use if the rate of planting of these devices does not slow down. Only international agreement will do that.

The conference proceedings are available from the IEE at their Publication Sales, P.O. Box 96, Stevenage, Herts., SG1 2SD, U.K.; telephone +44 (0) 1438 313311; fax +44 (0) 1438 742792. Refer to Conference Publication No. 431 at GBP 45. □

Paul McGoldrick's e-mail address is: 102447.346@compuserve.com.

HOW VALUABLE?	CIRCLE
HIGHLY	543
MODERATELY	544
SLIGHTLY	545

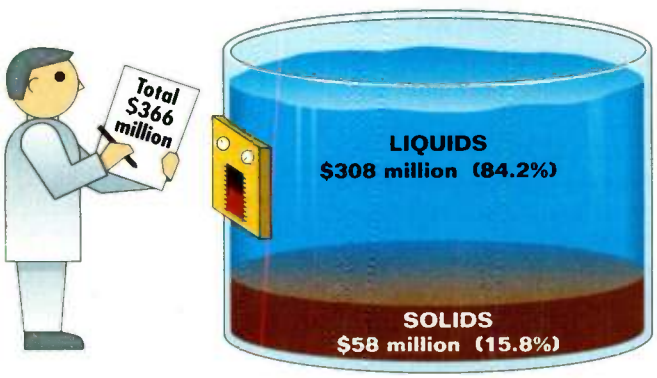
ELECTRONIC DESIGN QUICK LOOK

EDITED BY MIKE SCIANNAMEA AND DEBRA SCHIFF

MARKET Facts

Quality control inspectors keep their cool when they know that they have reliable instruments and when they know that the manufacturing process is in control. Having level measurements for in-process control and inventory management is paramount in the chemical/petrochemical, petroleum, food, and pharmaceutical industries. According to "The U.S. Level Measurement and Inventory Tank Gauging Industry, Fifth Edition," a new study from Venture Development Corporation (VDC), there are opportunities for growth in the liquids and solids level measurement devices market. In 1995, the study shows that the U.S. process level measurement device market hit $366 million, forecasted to rise to $427 million by 2000. The growth is at a compound annual growth rate (CAGR) of 3.1%. The chemical/petrochemical segment of the process level measurement device market was 26.5% (translating to $97 million), in 1995. The study projects that the market will top $123 million by 2000, keeping a 4.7% CAGR. One of the reasons why this market will experience consistent growth is the pressure on manufacturers to answer to the environmental regulatory demands. On the other side of the coin, limiting the growth is the migration of manufacturers overseas, rather than keeping processes within the U.S. Liquids dominate the process level measurement market, with 84.2% of the devices purchased going to liquids applications. The petroleum segment of the U.S. process level measurement market was the second largest consumer of those devices with a 23.8% share (equalling $87 million) in 1995. But the highest level of growth in the market belongs to the pharmaceutical industry at 6.2% CAGR. VDC predicts that the pharmaceutical segment, which accounted for $3 million in solids measurement devices in 1995, will rise to 8.9% CAGR. The increase is credited to greater demand for much higher degrees in accuracy. The Food and Drug Administration's ever-increasing regulations also are driving the measurement device demand. VDC's study also points to the food industry as the second largest consumer of devices for solids applications in 1995. Food companies ate up 20% ($11.5 million) of the solids market. In the study's look at inventory tank gauging, VDC found that total U.S. system consumption added up to $63 million last year. The petroleum industry ranked number one in the study, accounting for 53.3% ($33.6 million) of the inventory tank gauging market. Expected to grow at 3.9% CAGR to 2000, the petroleum segment of the market is expected to slow during the next four years due to a lull in manufacturing facility construction. The chemical industry came in a far second in the market at 19.6% ($12.4 million) in 1995. Environmental Protection Agency requirements are expected to push the market through 2000. The VDC study forecasts the chemical industry to grow at 5.5% CAGR. Again, the pharmaceutical industry garnered the highest forecast growth rate, checking in at a 15.6% CAGR for the next four years, despite the small ($1.6 million) share of the total U.S. consumption in 1995. The study is priced at $4950 and can be purchased through Venture Development Corporation, One Apple Hill, Natick, MA 01760; (508) 653-9000; fax (508) 653-9836; e-mail vdc4u@aol.com.—*DS*

Where the Level Measurement Device Dollars Went in 1995



Source: Venture Development Corporation

New Electronics Society Announced

ISHM, The Microelectronics Society, recently announced that its members and the members of the International Electronics Packaging Society (IEPS) have ratified the merger of the two societies to form a new organization called The International Microelectronics and Packaging Society (IMAPS). The new organization claims to be the largest microelectronics society in the world.

According to James R. Drehle, 1997 ISHM President-elect, the purpose of IMAPS will be to advance and expand the use of packaging in all levels of electronic and microelectronics packaging through professional and public education, the dissemination of information, and the promotion of the society's portfolio of technologies.

For more information, contact ISHM at 1850 Centennial Park Dr., Suite 105, Reston, VA 22091; (703) 758-1060; fax (703) 758-1066; e-mail ISHM@aol.com.

KMET'S KORNER

...Perspective on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439;
(702) 345-1455; fax (702) 345-0804

Sometimes markets turn in a negative direction, taking the fortunes of an organization and its employees with it. But these markets, with significant help from the companies that serve them, return to grow and prosper. Consider the following scenario:

The Semiconductor Industry Association's book-to-bill ratio headed for the stratosphere for a period of years. During this time, markets expanded, engineers prospered, and companies grew as profits provided fuel to the semiconductor business engine. Fortunes expanded over this period, all news was good news. Most semiconductor companies lost sight of the cyclical nature of the business beast. Many individuals who experienced past downturns viewed the available information and concluded that this time around it would be different. They became convinced that a downturn could not take place.

But then the book-to-bill fell below one. Initially, most reacted by saying this was just a one-month blip. Next month, the number fell below one again, this time bursting the euphoric bubble in the process. Executive managers began thinking defensively. And for many months now, the book-to-bill remains less than one. The longer it goes on, the greater the impact on engineering employment within the industry. Many firms now find themselves contracting rather than expanding. It's just another business cycle!

To rise to the challenge, some firms—who just a few months ago were hiring at a brisk pace—began laying off members of their engineering teams to save money.

Engineers performing on the margin become the first to go. From the company perspective this sounds good; executive managers think they can easily cut the engineering head count by 30% or more to conserve financial resources and not affect engineering performance. Wrong! In the firms that set high hiring standards, it's difficult to identify even 5% of the team as marginal performers. Nonetheless, the management team must identify weak performers based on objective criteria. Then, the company acts to sever these employment relationships—it will no longer have to pay the wages, taxes, and benefits for those terminated. But, because the head count is so small, the money saved is, oftentimes, not enough. Next, to save a few more bucks, do you cut into the lean engineering muscle mass?

Hopefully not! Your company needs this talent to work out of its slump. The market will come back, but as it does, you will have to be there with new products to meet the new challenges. The time-to-market clock does not stop! You cannot recover without a dedicated, talented, engineering force behind the company. To keep this team in place and highly productive do the following:

Reduce operating expenses to a minimum. Do this by scaling back recruiting, travel, supplies, equipment, outside contractors, outside services, and project materials expenses.

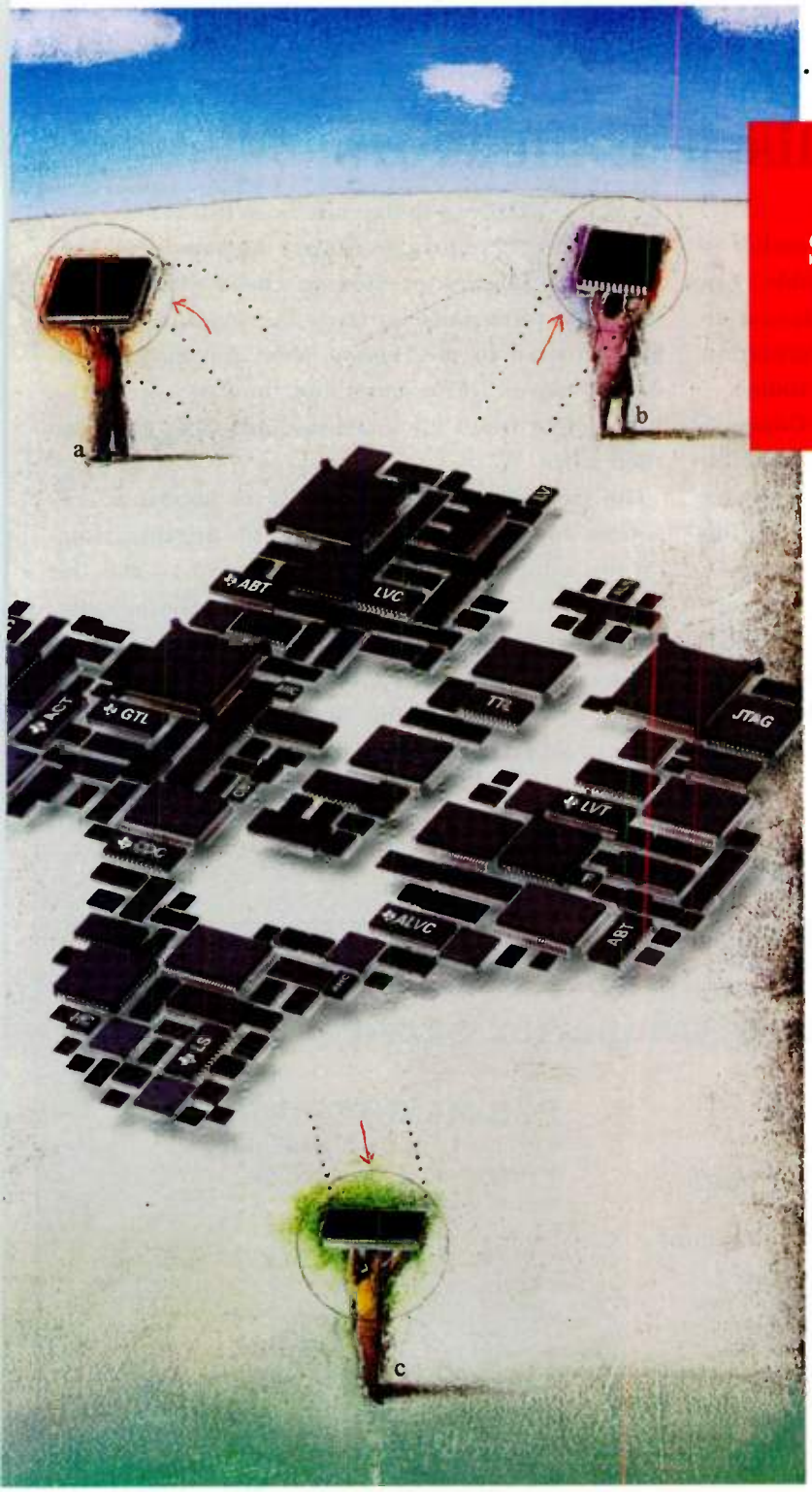
Put the engineering team on a reduced schedule for reduced pay program. The engineers take 1 day off within a 10-day work period to effect a 10% reduction, or 1 day off within 5 to realize a 20% reduction.

The combined effect of the above actions reduces engineering expenses by 30% or more without a layoff.

Your engineers, free from thinking about looking for another job, then go to work on critical new product programs. As they do, their loyalty to the company builds. Trust between employee and employer creates a dynamic, competitive, business force.

Readers may contact Ron Kmetovicz at Time to Market, P.O. Box 1070, Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804. To obtain an e-mail copy of "The Complete List of Reasons for a Late Product Introduction," contact Mr. Kmetovicz at kmetovicz@aol.com.

A D V A N C E D S Y S T E M L O G I C



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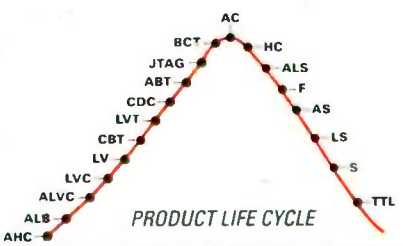

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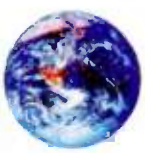

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TEXAS INSTRUMENTS

08-2001

Compaq Contributes to Journalistic Endeavors

THE PRESSURE ON JOURNALISTS TO BRING the most accurate stories to the widest audience possible (in the shortest time frame possible) can be tremendous. As a result, using the Internet to check sources and research historical information has become an integral part of journalism today.

Relieving some of the pressure is Compaq Computer Corporation. Compaq has donated 30 Deskpro XL PCs, 31 QVision 17 in.-monitors, and a ProLiant 1500 5/133 mission-critical server to the National Journalism Library in Washington, D.C. at the National Press Club. The PCs are Pentium-based with 32 Mbytes RAM and 2.1 Gbyte hard drives. The Deskpros are loaded with Windows NT 3.51 and Matrox MGA Millennium Graphics. The server uses 6.3 Gbytes storage, and has 64 Mbytes RAM, CD-ROM capability, and SmartStart.

The recently renovated library, known as the Eric Friedheim Library, previously closed whenever instruction took place so that the computers would be dedicated to the classes. Now, the library conducts classes while users continue to access the Internet or other applications needed to continue their work.

The Eric Friedheim Library is an important resource for journalists whose news organizations do not supply the training they need to use the Internet to their greatest advantage. Historically, members of the Press Club have used the world-renowned library for its educational and informational offerings, but the new additions will likely have prospective members signing applications.

QUICKLOOK

FLIPPING THROUGH THE INTERNET ROLODEX

...numbers you need to know

http://www.sme.org: The media can access this home page to obtain press releases and interact with the Public Relations team of the Society of Manufacturing Engineers (SME). Users can view corporate background information, a calendar of SME events, information on SME conferences and expositions, and information on SME honors and awards. Access also is provided to SME's home page search engine.

http://www.duracellnpt.com: Tap into Duracell's site to obtain technical information on Duracell primary and rechargeable batteries, including in-depth tutorials on each battery system, battery data sheets, battery system comparisons, technical notes, and updates on Duracell innovations. Users can review the material on-line or download the documents for later printing, and also can e-mail link to the company's headquarters in Bethel, CT.

http://www.siecor.com: Get the latest information on fiber optic and copper communications products for voice, data, and video applications from Siecor's site. Information is provided on the private networks marketplace, including a reply card for users to request additional information. A corporate profile, up-to-date press information, and telecommunications glossary also are available on the site.

http://www.sipex.com: Users may access data sheets from Sipex Corporation's Data Converter Products Catalog, data sheets from the 1996/1997 Interface Products Catalog, and/or product information from the El Lamp Driver circuit offering. The site is complete with up-to-date information on what's new at Sipex, a listing of Sales Representative and Distributor locations worldwide, and a literature request form. Information can be downloaded using Adobe Acrobat, which can be downloaded for free off the Internet.

http://www.crydom.com: No need to cry about this site, which offers information about Crydom's Solid State Relays. The site features complete and comprehensive product information on-line to view, print, or download. Input and output specifications, mechanicals, derating curves, and general product parameters are available. The site is organized by product categories with basic product ratings and parameters for ease of selection.

http://www.matrix.com: Visit Matrix Corp.'s site for a listing of current VMEbus board-level products and enclosures outlined in easy-to-read tables. Environmental classes from commercial/industrial to MIL-rugged are defined for each board product. Users can download more detailed product specifications and request free catalogs.

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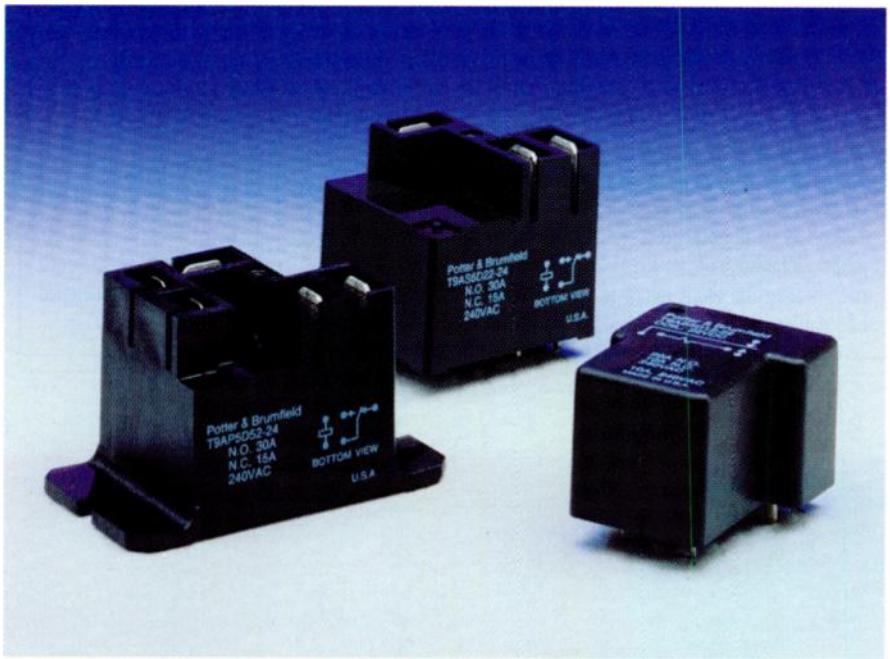

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READER SERVICE 163

1601A

The Search Is On

The National Mail Order Association (NMOA) is searching for the 500 most unique and interesting products in the United States. The product search is meant to help small to midsize manufacturers and inventors get publicity for their products. It also helps merchandise buyers find new products for their company to sell.

All 500 selected products will automatically receive free publicity in "Mail Order Digest," the association's international newsletter. Mail Order Digest goes to the merchandise buyers from mail order companies, catalog companies, infomercial companies, and other direct marketers, both nationally and internationally. The best product from each state will be featured on the NMOA Internet site for an entire year.

According to NMOA's Chief Manager John Schulte, "You never know where that next hot product will come from. It's like having your product picked by QVC, only better! The products we select will be exposed to hundreds of merchandise buyers from around the world, adding export possibilities as a bonus."

Manufacturers of all sizes are invited to participate, even the one-man shop. Products can be of any type, and should be tailored for the general consumer or business to business. Firms wishing to enter a product should contact the NMOA by phone, fax, or mail for a product entry form. Completed entries must be submitted no later than December 31, 1996. NMOA will notify all entrants concerning their products' status.

For more information about the contest, contact NMOA, US 500, 2807 Polk St. NE, Minneapolis, MN 55418-2954; (612) 788-1673; fax (612) 788-1147; Internet: www.nmoa.org/.

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READER SERVICE 141

Engineer Develops Vehicle Steering Aid

Most cars today have cruise control to help drivers maintain safe, steady speeds. Future vehicles also may have steering control for safer highway driving. How is that possible? A technology developed by an electrical engineer from Texas A&M University may have the answer.

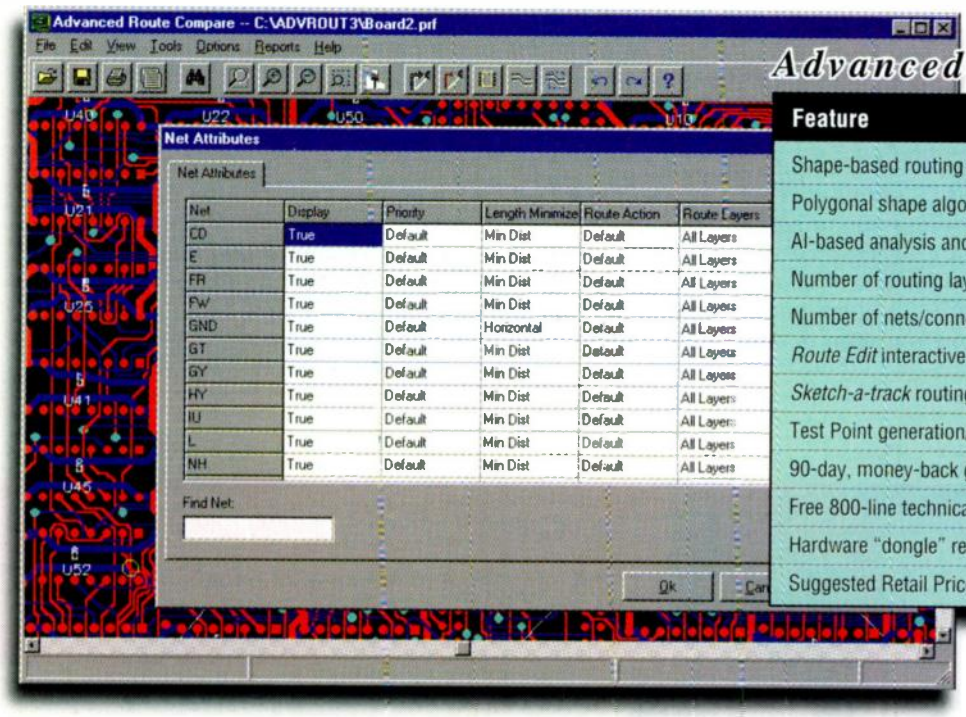
Don Parker's patented method for automatic vehicle steering and lane sensing uses infrared light to retrieve data from reflective stripes sprinkled with high-index glass—the same material used for reflective road signs and lane division stripes.

His prototype fits underneath the car, in front of the radiator, and behind the front bumper. It's a small box with one transmitter that projects an infrared beam to the road surface and two receivers. The device steers the vehicle so that both receivers measure equal reflections, keeping the vehicle aligned in the lane. A signal tells the driver when the lenses need cleaning, and a self-adjusting component increases the beam's intensity for paint that's faded or obscured by dirt or rain. Driving information also could be provided by the stripe, making it "essentially a bar code for cars," Parker said. "Anything that appears on road signs—turnoffs, exits, even rest stops or service stations—could be encrypted in the stripe." Reflected light "read" by a processor would control speed or even display information to the driver, if the car has an on-board computer screen. "The display could help drivers navigate an unfamiliar city or find an exit at night in rainy weather," says Parker.

Parker notes that in actual use, a stripe would be placed in the center of a highway lane using conventional pavement painting technology. Repainting the special stripes would be easy, he added, because "the same steering technology can also operate the boom to paint over the perimeters of the existing lane stripe." But first, the demand for the technology and concurrence among the states' departments of transportation to coordinate the specially painted stripes are needed, he emphasized.

For more information, contact Dr. Don Parker at (409) 845-7564; fax (409) 845-6259; e-mail parker@ee.tamu.edu.

Shaped-based routing from Protel®



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Number of nets/connections/pins	Unlimited	Unlimited
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Sketch-a-track routing option	Included	
Test Point generation/DFM option	Included	Optional
90-day, money-back guarantee	✔	–
Free 800-line technical support	✔	–
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READER SERVICE 165

Virginia's Virtua To Automate European Libraries

VTLS Inc.'s third-generation system, Virtua, has been chosen to automate both the European Parliament Library, Luxembourg and L'Universite catholique de Louvain (UCL), Louvain-la-Neuve, Belgium.

UCL, one of the world's oldest universities, was established in 1425. Maintaining arts and humanities, economics, law, medicine, philosophy, psychology, and science libraries, the school had been using three different systems that couldn't keep up with the technology. The university spent a year putting different products through their paces, choosing Virtua for its support of Unicode, its multilingual capabilities, its graphical options, and its use of Oracle. The first library in Belgium to install Virtua, UCL also will act as a testing site.

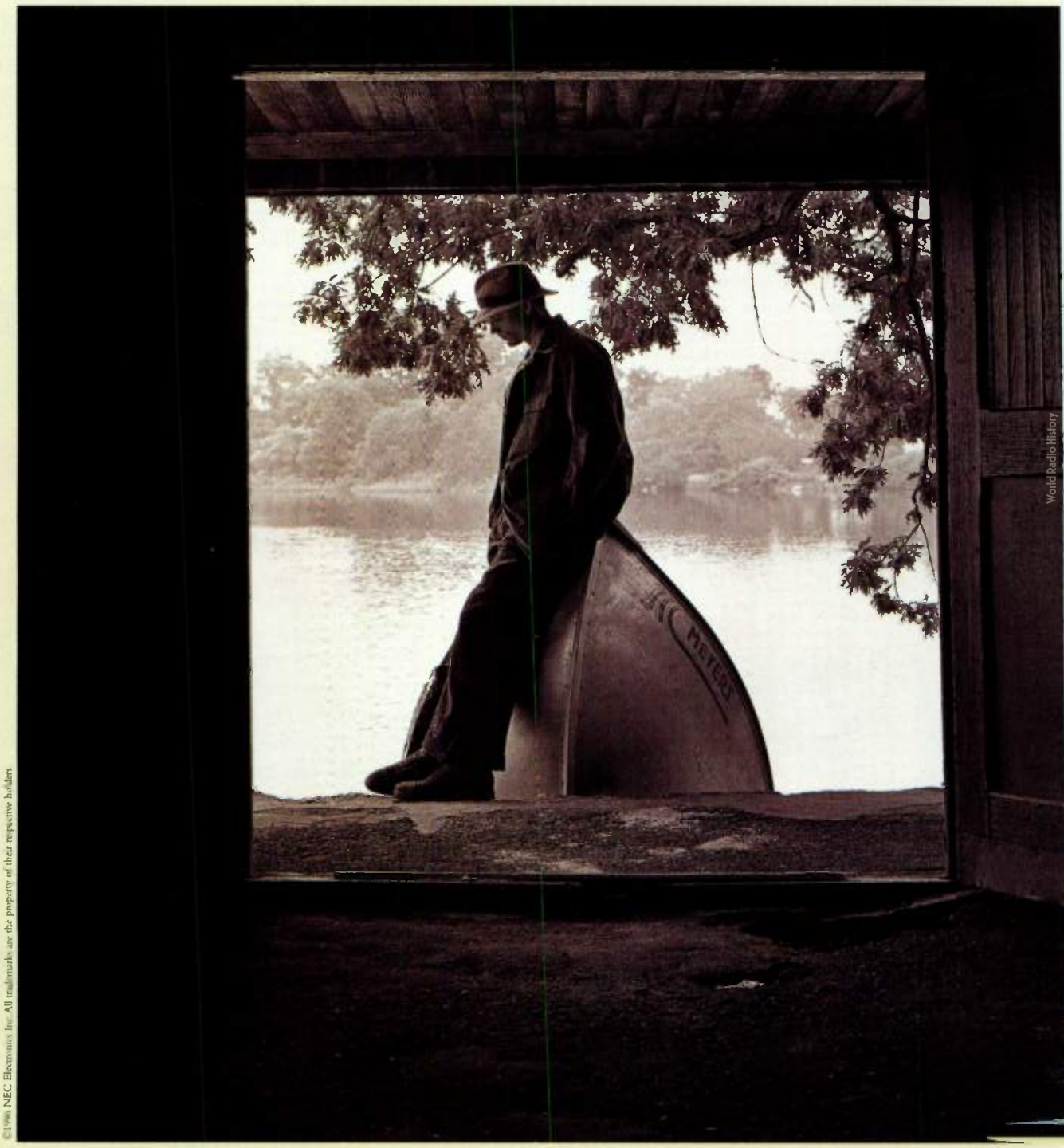
The European Parliament Library also chose the Virtua system for its Unicode support and multilingual capabilities. The Library houses a collection comprised of eleven different languages, necessitating a solution that could handle multiple character sets easily. Representing the 15 Member States of the European Union, the Library manages and provides documents in all of the official languages of the Union. First, the Library's Luxembourg site will have its homegrown mainframe replaced by Virtua, then the Brussels branch will be updated.

Virtua will be installed on the Sun UltraSparc platform, running under Solaris (Unix) and the Oracle Relational Database Management System with a 128-user level license for UCL. Virtua's basic subsystems include OPAC, Acquisition and Fund Accounting, Cataloging and Authority Control, Circulation and Status Monitoring, Serials and Bindery Control, and Statistics and Reporting. Other a la carte items chosen by the university are Ad Hoc Reporting, Document Delivery, ERL Interface, Interlibrary Loan, Reserve Room Control, and the Virtua-Web Gateway.

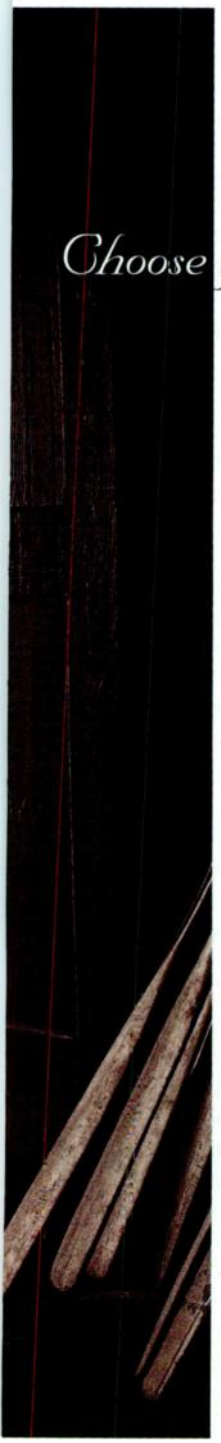
The European Parliament Library's setup is a 32-user license running on the Sun Solaris platform with Bibliographic Filtering, Document Delivery, and the Virtua-Web Gateway.

For more information contact VTLS Inc., 1800 Kraft Dr., Blacksburg, VA 24060-6351; (540) 557-1200; fax (540) 557-1210; Internet: http://www.vtls.com.

THERE'S A LITTLE BIT INTO EVERY



OF YOU *embedded* PRODUCT YOU DESIGN.



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This complex design you are working on. Numerous pieces, each with separate functions. But you make it whole. And then, you send it out into the world. A part of you that will become an extension of someone else.

In some ways, it resembles you. Which is why you shed the ordinary. And look for the best ways to improve your design.

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So what, exactly, led them to the V_R Series? Maybe it's the fact that NEC's V_R4300™ and V_R5000™ deliver far better MIPS per dollar than the PowerPC™ 603 or 604—providing remarkable performance for less than they ever imagined.

Or could it be our programs for companion chipsets? With NEC's V_R Series, you will get a comprehensive solution, including support for PCI Bus interface and laser printer control peripherals. We even assemble the third-party tools. So companies are able to bring their designs to market much faster.

But there's another reason forward-thinking companies select the V_R Series: Scalability. The V_R Series uses a common code library which enables "forward compatibility." So it's easy to upgrade to the latest generation of processor. That's important for two reasons. First, the incredible investment you have in developing code. And second, you can expect several new processors in the V_R Series line.

For more information, call *1-800-366-9782*. And ask for Info Pack 195. It really is the wise thing to do. Especially when you consider what really gets embedded into your design.

	V_R4300	PPC603	V_R5000	PPC604
Frequency	133MHz	80MHz	200MHz	100MHz
Bus Interface	32-bit	32/64-bit	64-bit	64-bit
I-Cache Size D-Cache Size	16KB 8KB	8KB 8KB	32KB 32KB	16KB 16KB
Pin Count/Package	120 PQFP	240 CQFP 256 BGA	272 BGA 223 CPGA	304 CQFP 256 BGA
SPECint92/SPECfp92	80/60	75/85	---	---
SPECint95/SPECfp95	---	---	5.5/5.5	3.29/n/a
Price in 1,000 Qty *	$45	$195	$300	$549

* PowerPC prices from PowerPC FAQ, 12/17/95. Prices subject to change.

V_R5000. Paramount performance, incredibly affordable. This is the ultimate embedded processor for advanced applications like internetworking.

V_R4300. A high level of performance at an extremely low price. Ideal for office automation products, video games and X-terminals.

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READER SERVICE 156

HOT PC PRODUCTS

The **Zoomed Video Port** standard is the result of Sigma Designs pairing with Cirrus Logic to offer full-screen broadcast quality video and CD-quality audio to notebook computers. Cirrus Logic's single-chip PC Card host adapters on the notebook side, plus Sigma's REALmagic Explorer chip set on the PC Card side communicate to bring Zoomed Video technology to notebook users. Compatible with Windows 95 and Open MPEG-1, the REALmagic Explorer chip set allows Zoomed Video port-capable computers to support new MPC3 standards for multimedia applications. Cirrus Logic host adapters that support the Zoomed Video specification include CL-PD6720, CLPD-6722, CL-PD6729, CL-PD6730, AND CL-PC6832. The Zoomed Video Port is compatible with CardBus slots and all of today's PC Card slots. For more information, contact Sigma Designs Inc., 46501 Landing Pkwy., Fremont, CA 94538; (510) 770-0100; (510) 770-2640; Internet: http://www.sigmadesigns.com.

PYST is a wacky parody newly released from Parroty Interactive, a new division of Palladium Interactive. PYST takes light-hearted swipes at the most well-known PC/Internet game, MYST. Poking fun at the fantasy game, PYST redesigns the trademark island scene to incorporate pollution as well as other industrial nightmares. Not only is PYST an interactive CD-ROM game, but there's a website—http://www.pyst.com, CD single (the "Theme from PYST"), and 900 number—(900) 288-PYST. The Enhanced CD single is sung by John Goodman, who also plays King Mattruss in PYST. There are 10 scenes on the disk, complete with audio, video, and animated features. Created by Firesign Theatre founder, Peter Bergman, PYST allows game players to link up to the comedy site and travel through the Members Only pages. The restricted areas encourage visitors to pen postcards, chat and post messages with other PYSTites, and download regularly-updated video and RealAudio clips. The PYST site also has links to other comedy sites. The hybrid CD-ROM is compatible with both Windows and Macintosh platforms. Retail price for PYST is $14.95. For more information, contact Palladium Interactive, 900 Larkspur Landing Cir., Suite 295, Larkspur, CA 94939; (415) 464-5500; fax (415) 464-5530; Internet: http://www.palladiumnet.com.

The **LGL4plus** and **LGL8plus** are two new line matrix printers from Digital Equipment Corp. The pedestal-mounted printers are designed for manufacturing environments and other mission-critical applications. The LGL4plus and LGL8plus units offer a low cost printing solution for invoices, bills, forms of all types, production reports, and bar coding. They support Windows 95 and NT, as well as UNIX and OpenVMS. Additionally, Digital has introduced the RapidPrint 500. Allowing many users to share the same printer across different network protocols, the RapidPrint 500 can be used with any printer, including the LGLplus printer line. The pocket-sized server supports AppleTalk, IPX, LAT, NetBios/NetBEUI, and TCP/IP network protocols. RapidPrint 500 is priced at $399, the LGL4plus at $5295, and the LGL8plus at $7695. For more information, contact Digital Equipment Corp., 200 Forest St., MR01/J18, Marlboro, MA 01752; (508) 467-7003; fax (508) 467-7512; Internet: http://www.printers.digital.com.

OFFERS YOU CAN'T REFUSE

Information from Japan on electronic display technologies is now available free of charge in a weekly e-mail newsletter titled "Display: The E-Mail Newsletter." The newsletter is published by InterLingua and consists of abstracts of articles from publications such as Nikkei Microdevices, listings of patents applications published in the display category within the past month, excerpts from special reports such as the Electronic Industries Association of Japan's survey of its members, original reports on trade shows and conferences, and summaries of important events that occur. Contact InterLingua, 423 South Pacific Coast Hwy., Redondo Beach, CA 90277; (310) 792-3636; fax (310) 792-3642; Internet: http://www.japanesetranslation.com.

QuadTech has launched THE QUADTECH STANDARD, a newsletter for OEM customers and other users of measuring instruments involved in prototype design, production test, R&D, quality control, incoming inspection, and calibration. The newsletter is dedicated to discussion of pertinent design, regulatory, application, and manufacturing concerns of the research and engineering community who demand the highest performance standards. Contact QuadTech, Inc., 100 Nickerson Rd., Marlborough, MA 01752-4696; (508) 485-3500; fax (508) 485-0295.

A CD-based "Designer's Guide and Data Book" from Texas Instruments includes a powerful search engine that will save designers time when they need to find the appropriate mixed-signal or analog device. The CD, called an InfoNavigator, is available free of charge and includes almost 15,000 pages of technical documentation on all of Texas Instruments' approximately 2,000 mixed-signal and analog semiconductors. Information found in the designer's guide includes data sheets, data books, application reports, reference designs and macro models, information on the availability of evaluation modules, seminar and trade show listings, and a glossary of pertinent terms. Contact Texas Instruments Inc., Semiconductor Group, SC-96041, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 5022; Internet: http://www.ti.com/sc/5022.

QUICKLOOK

I'm In The Book

Here's a great holiday gift idea (as if you haven't had enough already) from Luckman Interactive—the *1997 World Wide Web Yellow Pages*. The volume is 1200 pages long, with over 10,000 web sites. For those individuals who spend many of their on-line hours searching out the best that the Internet can offer, the book could become their surfing companion.

Published by Barnes & Noble, the *1997 World Wide Web Yellow Pages* features reviews and ratings on each of the sites listed. Luckman's first book published through Barnes & Noble, *Best of the Web*, became a best seller. Luckman's choice of publisher is also the leading retail bookseller in the U.S., with over 1000 bookstores in its distribution.

Luckman's editors and writers reviewed over 100,000 web sites in the production of the *1997 World Wide Web Yellow Pages*. They rated the sites by content, design, downloading time, and organization. The book uses a five start rating system, only featuring sites with three or more stars.

The *1997 World Wide Web Yellow Pages* features Uniform Resource Locators (URLs) for these categories: Art, Business, Children, Computers, Education, Entertainment, Government, Health, Humanities, Internet and the Web, Life Styles, Music, News, Regions, Science, Shopping, Sports and Recreation, and Travel. And, for those of you needing further organization, those 18 topics have been subdivided into 400 smaller categories.

Luckman's intent with the tome was to save people's time. The process of waiting for search engines to spew out their matches (some of which are no match at all), then checking out each of the links only to find that two hours later there is only one match was incentive enough to author the book. Lucky Luckmanites currently evaluate over 10,000 sites a month, preparing for another reference guide, no doubt.

Luckman Interactive's *1997 World Wide Web Yellow Pages* retails for $24.95. For more information contact Luckman Interactive Inc., 1055 West 7th St., Los Angeles, CA 90017; (213) 614-0966; (213) 614-1929; Internet: http://www.luckman.com.-*DS*

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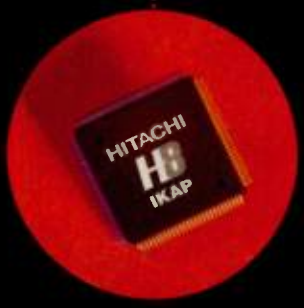

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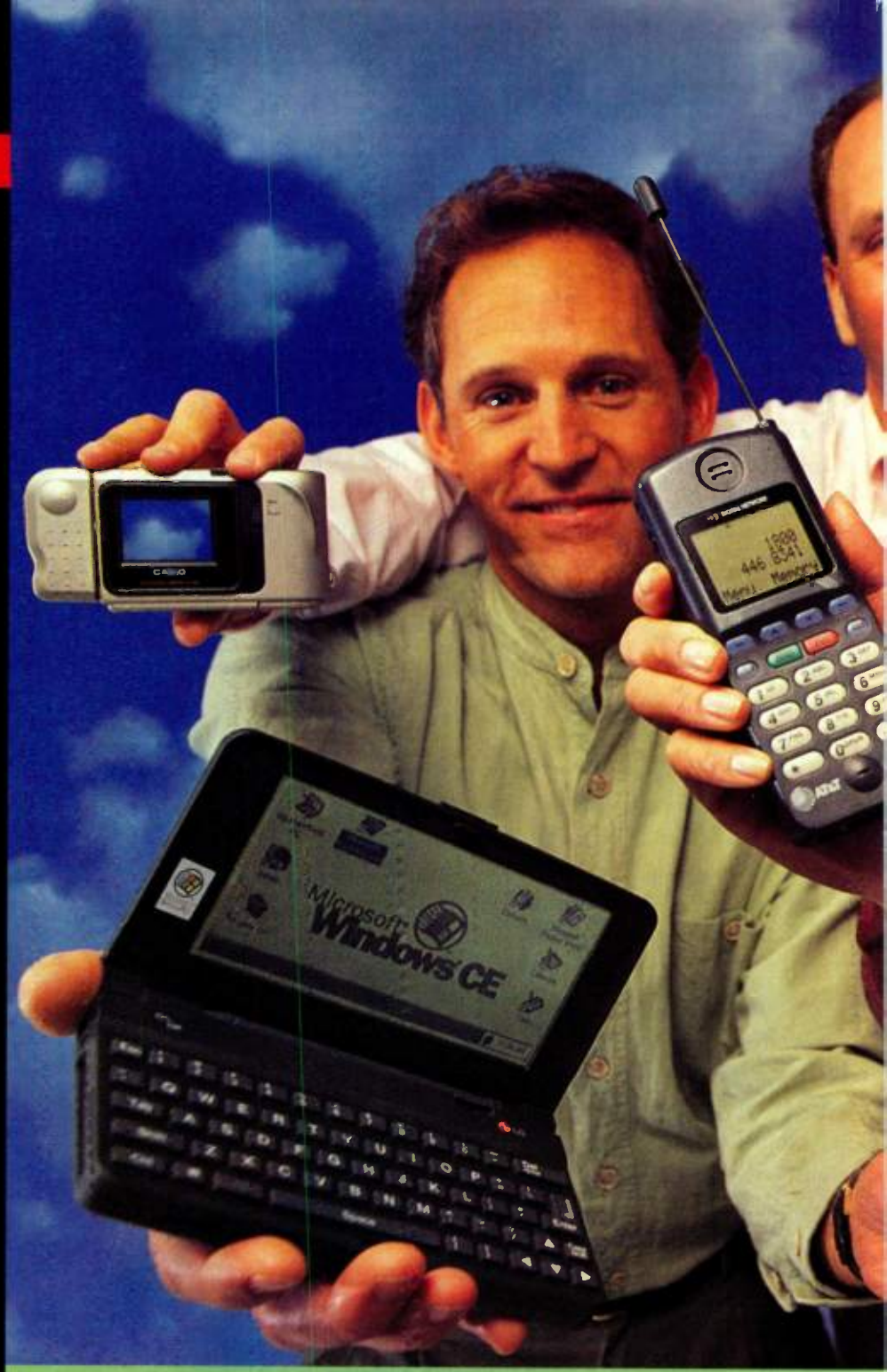

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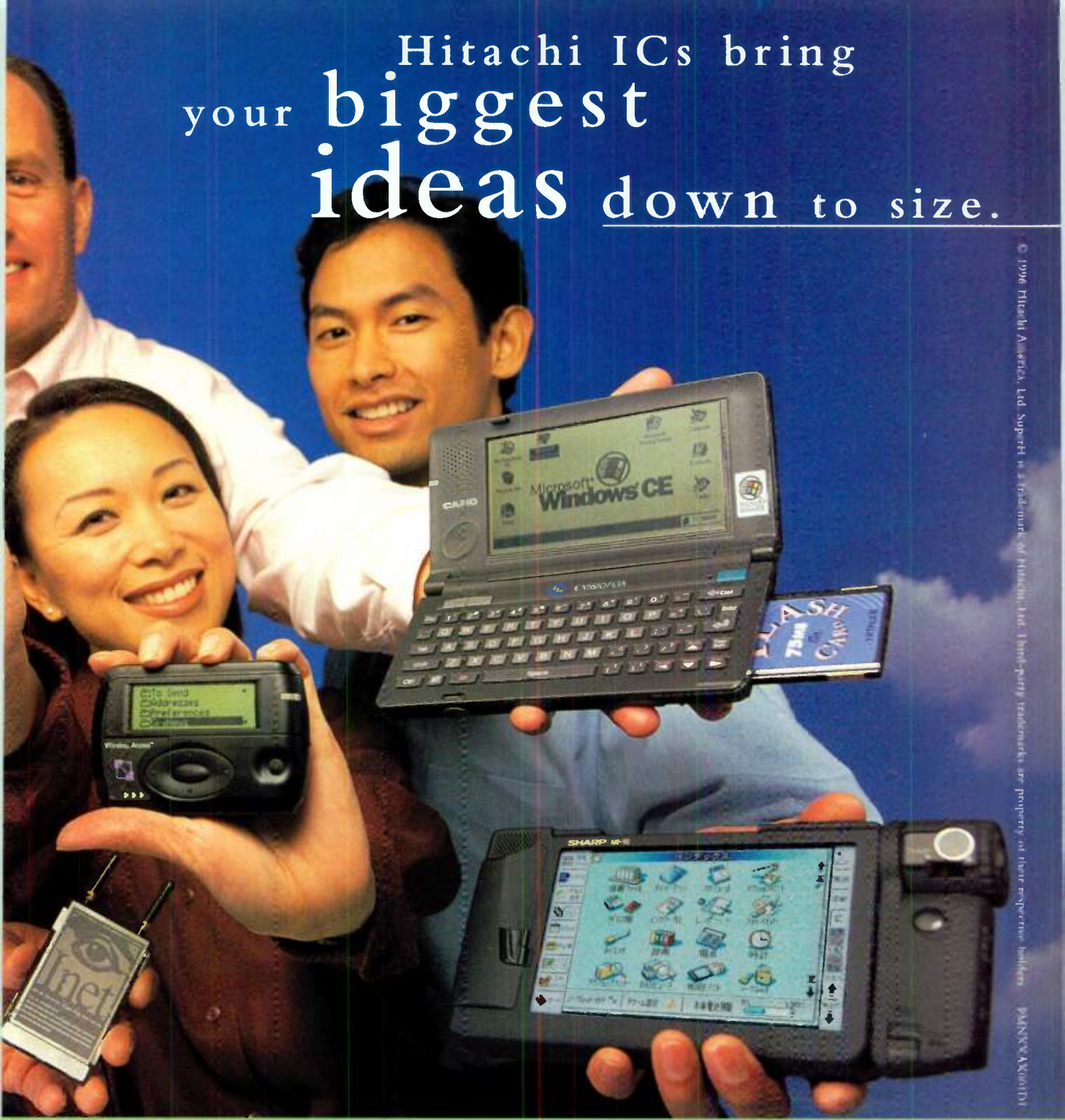

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Letters from London

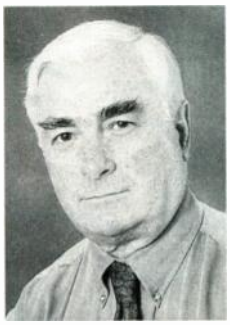
PC On A Table Napkin

Catching an industry insider off guard can sometimes put me in a spot. To put it basically, I'm nosy, and I like to know what's going on in the industry I love, so a casual conversation rather than a formal interview with everyone on their best behavior is too good an opportunity to pass up—I learn a lot more that way. But sometimes, people tell me more than what is good for them. My business is not about putting good people on the spot with their employers. So in some instances, I have to make an educated judgement about how much I can write.

But I'm sure that Robert M. Gregory, director of Strategic Marketing at Intel's PCI Components Division in Folsom, Calif., won't be in any trouble and I'm sure certainly wouldn't mind if I outline some thoughts we had together on the future of desktop PC architectures.

Robert recently stopped off in London on his way back from meetings with the European chapters of the PCI Special Interest Group. The original idea was for us to discuss what happened at those meetings. But that business was soon disposed of. We then proceeded to talk about PC architectures and the future of the "sealed PC."

We speculated that more and more powerful CPU chips are not the total answer. Important in the Intel scheme of things of course, but as the PC becomes more of a consumer electronics product, other factors begin to emerge as significant. For example, there are the issues of graphics and "multimedia" devices and components. There are conflicting factors at play here. On the one hand, street price and manufacturing costs have to be kept down, if as Robert puts it, they are ever going to hit the market's "sweet spot." On the other hand, what may be perceived by consumers as a television set capable of generating its own pictures rather than receiving them over the air has to pack a tremendous computing punch in order to be successful.



PETER FLETCHER

A quick sketch on a table napkin sets out a way how this might come about. In this model, the PCI bus becomes more of an internal backplane controlled by an Intel 440xx core logic device. The CPU, 3D graphics rendering engine, and the main memory access also are under the direct control of the core logic. Hooked onto the PCI internal bus is an I/O control device that provides an ATA interface for disk drives, plus facilities for an ISA bus device—although Robert thinks that might disappear in time—and a Universal Serial Bus (USB) interface for the outside world. The main problem here is to ensure that all of these devices are properly balanced with respect to each other to eliminate processing these kinds of bottlenecks.

Therefore, the 440xx device provides a 66 MHz, 32-bit Accelerated Graphics Port (AGP) to feed polygon data to the graphics processor and its dedicated frame and Z buffer memory. At the same time, however, the 440xx also can provide a direct high bandwidth path directly to main memory, where Robert believes that texture information will be stored. Output from the graphics rendered will be passed to the monitor over an IEEE 1394 "Firewire" high-speed serial line. Plug-and-play peripherals such as a keyboard, mouse, scanner, digital camera, and printer will be connected by the USB interface. Inside the sealed box, the PCI bus also will provide the parallel termination for another serial Firewire connection inside a "device bay."

As for the device bay, Robert explains that it is a standard 3.5- or 5.25-in. form factor slot accessible from outside the computer into which peripherals, such as disk and DVD drives, can be plugged in to the device bay.

That's the view for the long term. In the meantime, there has to be a transition from current architectures that are "open" in the sense that end users are encouraged to take the lids of their PCs to add functionality with internally mounted cards. Up to this point, Robert stresses that the views he expressed are just his thoughts spoken out loud.

But these thoughts have been formulated on the basis of an Intel corporate thought process. The watchwords that are repeated over and over are "innovate, migrate, integrate" according to Robert.

"We have this model—Innovate—a function starts as an add-in card or a plug in. That's the way niche markets are developed at a high price point. As they gain momentum, inevitable forces take over so the migration phase is to make the transition where it's valued by certain segments of the market—possibly integrated into the motherboard—it's a $10 to $20 bill of materials add-on but it's a new functionality. The third step is to then integrate the function into silicon."

And the time scales? "We should see the first computers that have the beginnings of this approach by the end of 1997."

Peter Fletcher is Electronic Design's U.K. correspondent. His e-mail address is: panflet@cix.compulink.co.uk.

handheld-constrictaphobia an abnormal fear of designing hand-held terminals and not having a processor that allows a flexible and customized solution for specific applications.

It starts with a tightness in the chest. You feel confined and utterly restricted. Relax, it'll be okay. NEC can release your pain. But first, you'll have to take hold of our HHT-ASSP processors--a crucial step on the road to total flexibility in hand-held terminal design.

With NEC's HHT processors, you get an X86 compatible embedded PC on a chip. Yes, a system on a chip. And since NEC's ASIC cores are already integrated, you can use our CB-C8 technology to easily add off-chip logic. And if quantity allows, you'll also have the flexibility to customize ASIC cores or add new ones on the chip to meet your specific application.

Here's some other ways we've removed the restraints. First, you'll be able to develop your code on a standard PC. And second, you're free to utilize off-the-shelf software products. Which means your designs will get out there faster and for far less cost.

We can also help with issues you have around speed and power. That's because our HHT-ASSP does 33 MHz at 3.3V and easily interfaces with 5V TTL devices. Furthermore, it allows you to utilize 0.5 micron technology for low power consumption in a compact 160-pin TQFP package.

And don't worry about your taste of freedom being short-lived. The HHT-ASSP is based on NEC's OpenCad design framework and standard macro library. Which means you'll have an easy migration path into future designs. Now if that doesn't make you breathe a little easier, you can always talk to one of our people on the phone. 1-800-366-9782. Ask for Info Pack 139.

READER SERVICE 155

NEC

INTERNET NEWS

Mercury Interactive has introduced their new visual web site management tool, Astra. Astra allows webmasters to view large sites in order to deal with issues such as broken links, congested paths, and dynamically generated pages. The Astra tool was designed to maximize Intranet and Internet application effectiveness, and to prevent dead links from appearing when customers and decision makers alike use the system.

Astra uses fast scan web site mapping to graphically display an entire site's architecture as a color-coded map. The mapping shows web changes on the fly. The scans map internal and external links, as well as static and dynamic pages.

The visual display of Astra shows web sites as hubs and spokes, rather than the traditional hierarchical tree structure. This arrangement allows webmasters to gauge the true complex and interrelated nature of their sites. The maps also have a split-screen displaying the web site's information in text format.

In order to monitor site usage, Astra graphically displays usage patterns by superimposing server-log data onto the maps. Following a color-coded key, webmasters can track the traffic of the site and analyze the site for weak and strong points.

Astra's Change Viewer allows webmasters to take views of two different days' architectures and compare the changes in the site. The Change Viewer features new, updated, or deleted pages and links. The tool also has an automatic Link Analyzer which highlights broken or unavailable links in red. The Link Doctor, also an automated feature, connects the webmaster to the broken link pages.

Available as a beta version, Astra is available for free at Mercury Interactive's web site: http://www.merc-int.com. The full version, expected to ship by the end of 1996, will be priced at $495.

For more information, contact Mercury Interactive Corporation, 470 Potrero Ave., Sunnyvale, CA 94086-9911; (408) 523-9900; fax (408) 523-9911.

Videoconferencing now has a new format—**ACS Innovations** and **Netscape Communications** have linked up to provide a solution that consists of ACS' Compro Digital Color Internet Camera and Netscape Navigator Gold 3.0. The package allows Internet users to author web pages, produce color images, and videoconference.

The digital camera setup is designed to provide low cost videoconferencing to corporate Intranets as well as corporations that use the Internet to communicate.

The camera can be used to provide color still and motion pictures to web sites and e-mail messages. It also can be used in other applications such as remote monitoring, product illustrations and demonstrations, desktop publishing, photo ID cards, medical and dental imagery, insurance claims, and property databases.

Compro users will not have to buy a separate video capture card or power adapter, since the camera uses D-Viewer software to capture the images directly to the PC. D-Viewer is a Windows application that features JPEG compression and image manipulation.

The digital camera uses 256 gray scales and 16.8 million colors. It has a resolution of 640 by 120, with motion video resolution at 160 by 120. In addition, the camera uses Automatic White Balance with manual color balance and saturation monitoring.

The Gold Package includes Netscape Navigator Gold 3.0, the Compro Digital Color Internet Camera, D-Viewer software, camera head and adjustable stand, parallel port pass-through interface unit, and keyboard intercept power cable. The package retails at $228.

For more information, contact ACS Innovations Inc., 3171 Jay St., Santa Clara, CA 95054-3308; (408) 566-0900; fax (408) 566-0909; Internet: http://www.acscompro.com.

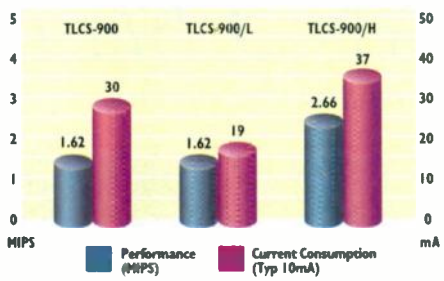
OFF THE SHELF

"Distributed Real-Time Systems: Monitoring, Visualization, Debugging, and Analysis" covers both the theoretical and practical issues involved in verifying and debugging distributed real-time systems (DRTs). The book details how to overcome timing verification difficulties and improve system performance and reliability. Also covered are real-world debugging approaches, instructions for design implementation in hardware and software, and descriptions of analytical techniques. The 317-page book is priced at $54.95. Contact John Wiley & Sons Inc., 605 Third Ave., New York, NY 10158-0012; (212) 850-6336.

The second edition of the **"Active Electronic Component Handbook"** provides the latest data, information, and design guidelines for all who design, manufacture, and use active components in electronic systems. The book offers readers an account of the nature and types of active components currently in use—and also discusses the importance of developing the right supplier-user team for optimizing the application of these components. The book features chapters on microwave and optoelectronic components, memory devices, hybrid and multichip module devices, and photonic components. The book is priced at $79.50. Contact McGraw-Hill, 11 W. 19th St., New York, NY 10011; (212) 337-5951; fax (212) 337-4092.

Toshiba TLCS-900 16-bit Microcontroller Family

When you've squeezed your current micro for all it's worth.



You've milked it for every last drop of functionality. Now it's time to take a look at Toshiba's new 16-bit family of microcontrollers, which will give you the perfect combination of performance and integrated peripherals.

The TLCS-900 increases performance four times over a typical 8-bit MCU, while the higher-performance TLCS-900/H is eight times faster. The low-power TLCS-900/L rounds out the family. All are highly integrated, featuring on-chip peripherals that include A/D and D/A converters, DRAM controllers, serial interfaces, real-time clocks, and ROM, RAM or Flash memory. This degree of integration yields a lower parts count, reduced system costs and increased reliability.

The flexible architecture of Toshiba's 16-bit micros means ample room for expansion without having to add design steps to the process. So while the core size of the current TLCS-900 is one of the smallest available, in the future when it's reduced even further there won't be any design change requirements. And because of its flexible architecture, we're able to offer numerous derivatives. We can also provide a complete suite of development tools, as well as a number of third-party tools.

So if increased performance, flexible architecture, a wide peripheral mix, low power and competitive pricing sound appealing, look to Toshiba's TLCS-900 16-bit microcontroller family. For more information, call us at 1-800-879-4963, or visit us on the Web at **www.toshiba.com/taec**.

We'll help take the pressure off you, and your micros.

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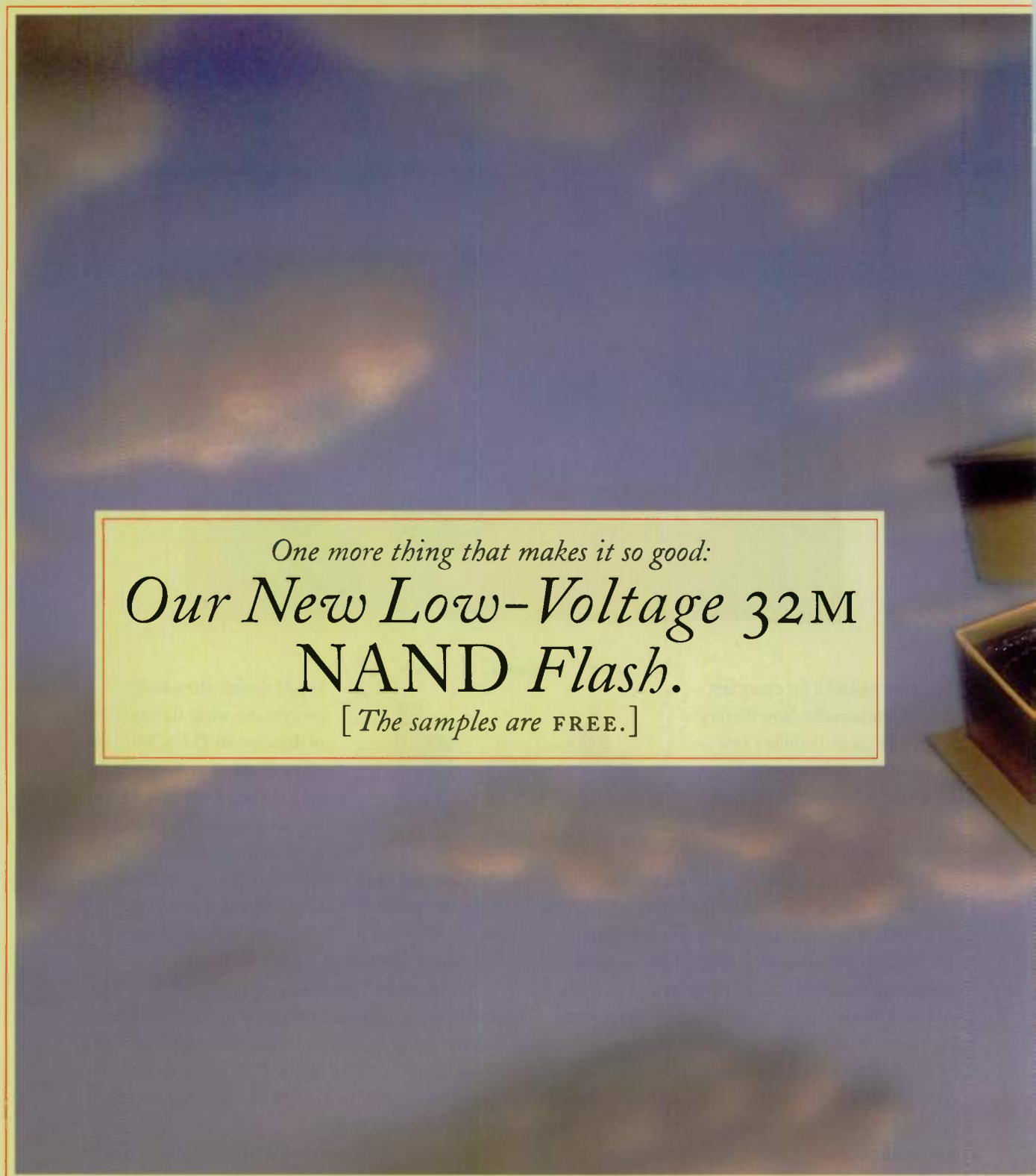

One more thing that makes it so good:

Our New Low-Voltage 32M NAND *Flash.*

[*The samples are* FREE.]

At Samsung, we're the world's first manufacturer to offer a 3.3-volt 32-meg Flash memory chip, and take it from us—these are some of the sweetest memories around.

We believe Flash is the perfect memory for an extremely wide range of nonvolatile storage applications. And to help prove that to you, we're offering free samples of our 32-meg to absolutely anyone who asks for them. (Making this ad into—yes—a kind of sampler.)*

As a low-voltage part, the new Flash will extend battery life. As a 32-meg part, it has extremely high capacity. And as a NAND Flash, it's better for data storage, has faster read/write, lasts longer, is easier to program, and costs less

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(and in the case of the samples—a *lot* less).

A sweet part indeed.

Beyond that, with this new NAND Flash, Samsung is extending its leadership position in memory in one more way—something we plan on doing for a long time to come.

As for our free samples: why not help yourself to a few right now? They're not even fattening.

Call 1-800-446-2760. Or write to Flash Memory Marketing, Samsung Semiconductor Inc., 3655 North First Street, San Jose, CA 95134.

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Still A *Generation* Ahead.

READER SERVICE 167

(A MOSFET IN THE HAND IS WORTH A HUNDRED IN THE BUSH.)

If our MOSFET *delivery times were any*

quicker,

they'd be there before you even call.

Okay, we'll admit it. Mental telepathy isn't our forte.

But that's probably what we'd have to have, if we were going to make our delivery and service in MOSFETS any better than it is already.

Because Samsung's manufacturing clout means that we have superior, ruggedized MOSFETS of practically every type, in stock right now in high volumes—and ready to be delivered into your hands almost immediately. Making for what have to be the shortest delivery schedules in the industry.

At a time when many of the best-known MOSFET makers are on 25-week-plus delivery schedules, we think our news is pretty compelling.

You'll find we offer more than 250 through-hole and surface-mount MOSFETS in a wide variety of packaging. We make an advanced line of micro MOSFETS for low-power applications. And throughout the whole line, we build to exacting ISO 9000 quality standards.

Using some of the largest and most sophisticated fabs on the planet.

You'll be able to deal either with us direct, or with some of the premier U.S. distributors, when you purchase Samsung MOSFETS. Which, by the way, come from the very same company you're probably buying memory chips from already.

Either way, count on helpful and intelligent service from the MOSFET experts at Samsung. And, of course, delivery times you'd have to be clairvoyant to beat.

Hey, you know, it sounds like right this second one of you decided you need parts.

Expect to have them in your hands very soon.

For details or distributor information, please call 1-800-446-2760 today. Or write to MOSFET Marketing, Samsung Semiconductor Inc., 3655 North First Street, San Jose, CA 95134.

SAMSUNG SEMICONDUCTOR

STILL A *Generation* AHEAD.

READER SERVICE 168

Study Reveals HDL Use Up In EUROPE

A survey of European-based designers revealed that the use of hardware description languages (HDL) is increasing. According to a study by VHDL International (VI), Santa Clara, Calif., a provider of educational information to electronic systems designers, systems designers, and other industry organizations, 60% of respondents indicated that they use HDL in their designs, ranging from communications systems, industrial controllers, computers, and peripherals.

According to Mahendra Jain, VI's executive director, the survey was conducted to gauge the European design community on HDL usage and trends. Of the 163 respondents who said that they used HDLs, 58% are VHDL based, 18% used Verilog HDL, and 12% used the C language. The remaining 12% design with other unspecified HDLs. Respondents were primarily design engineers who noted that they have used HDLs anywhere from one to eight years. Design engineering managers and engineering technical support staffers also replied to the survey.

Eighty percent of respondents indicated that they did not use multiple VHDL simulators. When asked which HDL they used for designing programmable devices, 58% said VHDL, 20% said Verilog HDL, and 22% said none. In addition, over 50% of the designers noted that Verilog HDL-VHDL co-simulation is not important.

When asked which HDL would designers expect to use in the future, 60% chose VHDL, and 12% said Verilog HDL. Close to 20% said C-language macros.

For more information on the study or VHDL International, contact the company at 3140 De La Cruz Blvd., Suite 200, Santa Clara, CA 95054-2046; (408) 492-9806; (408) 970-4274; Internet: http://www.vhdl.org/vhdl_intl.

—*MS*

QUICK NEWS

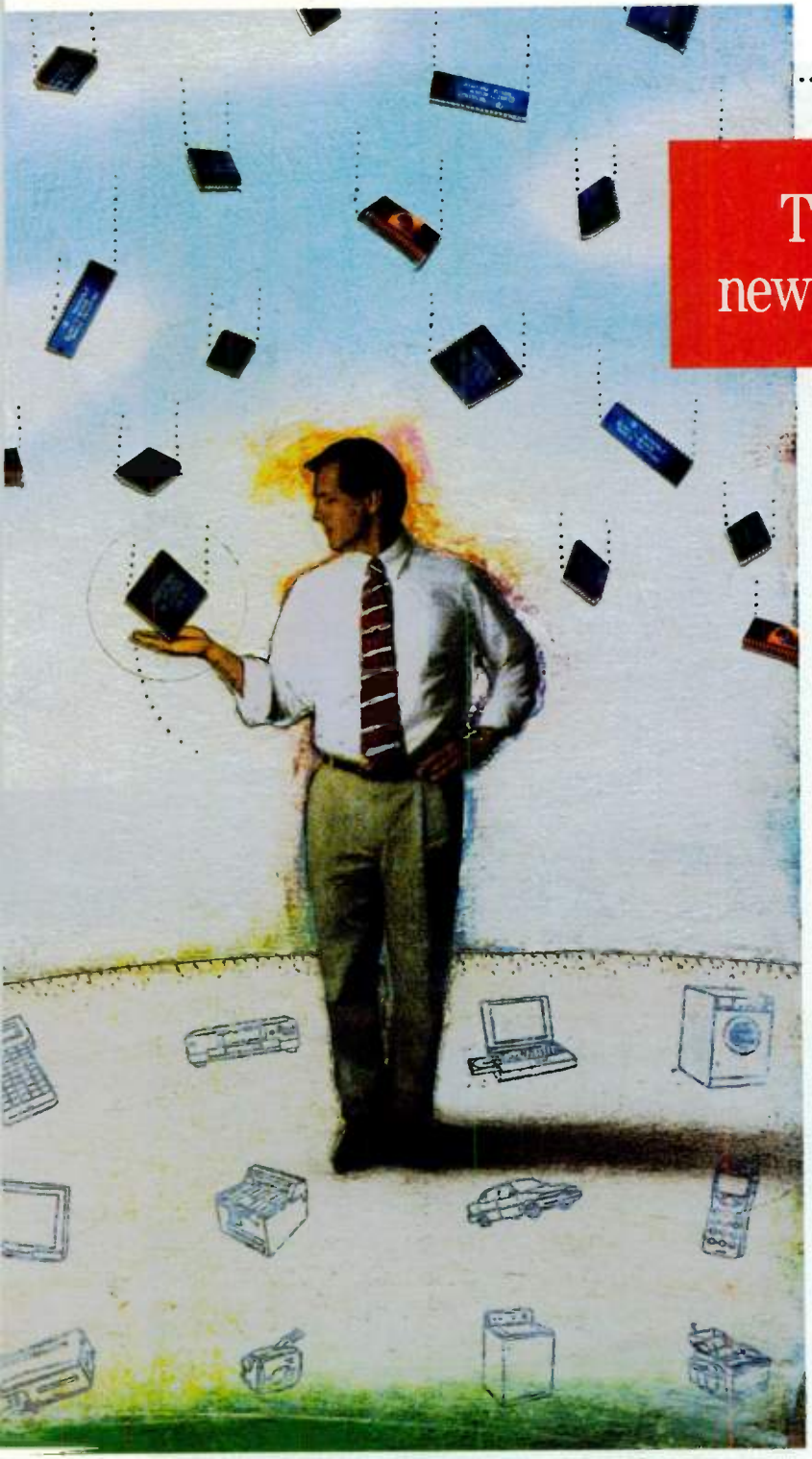
New Information Sharing System—The Electronic Industries Association (EIA) has announced the creation of an accessible on-line software platform to provide shared information between and among suppliers and end users of component parts and subsystems. The effort will include a coalition of companies from both the commercial and military electronics industries.

The types of data that would be made available include: EIA standards/part numbers, with cross references to other standards; design codes, ordering information, and universal technical data models for capturing and displaying component product attributes; and links to existing data sources, supplier profiles and World Wide Web pages; and technology road maps.

Known as the Component Information Management System (CIMS), the effort aims to provide designers, engineers, procurement personnel, and others with access to a database from which to select parts for design and replacement in the development or modification of products. The CIMS will allow for multiple delivery systems, including Internet access, scheduled downloads for the large users, and CD-ROM. EIA will link other databases to its own as long as their data meets the standards established for the CIMS approach.

For more information on the program, contact EIA, 2500 Wilson Blvd., Arlington, VA 22201-3834; (703) 907-7500; fax (703) 907-7501; Internet: http://www.eia.org.

M I C R O C O N T R O L L E R S



TI showers you with 73 new microcontroller devices.

Highlights of TI's TMS370 devices:

- Easy-to-use register-to-register architecture with small code size generation
- Reduced system EMI with optional PLL clock circuitry
- Times coprocessor functionality via Programmable Acquisition & Control Timer (PACT)
- Increased measurement capability with up to 15 ratiometric A/D converter channels
- I/O robustness offering Schmitt trigger on all inputs
- Highly efficient C compiler and common Compact Development Tool (CDT) emulator for all devices

Special $37 Starter Kit!

For a limited time, you can order a Microcontroller Starter Kit (MSK) for only $37 (normally $99)†. For more information, call 1-800-477-8924, ext. 6008, or visit http://www.ti.com/sc/6008

TI has more than doubled the TMS370 8-bit microcontroller family by adding 73 new devices, to give you one of the broadest fully compatible families in the industry. Choose from 13 subfamilies (135 devices) for your cost-effective solution among the ROM and OTP devices. And to make sure you're first to market, TI supports every device with technical documentation, application notes, an engineering hot line and easy-to-use development tools.

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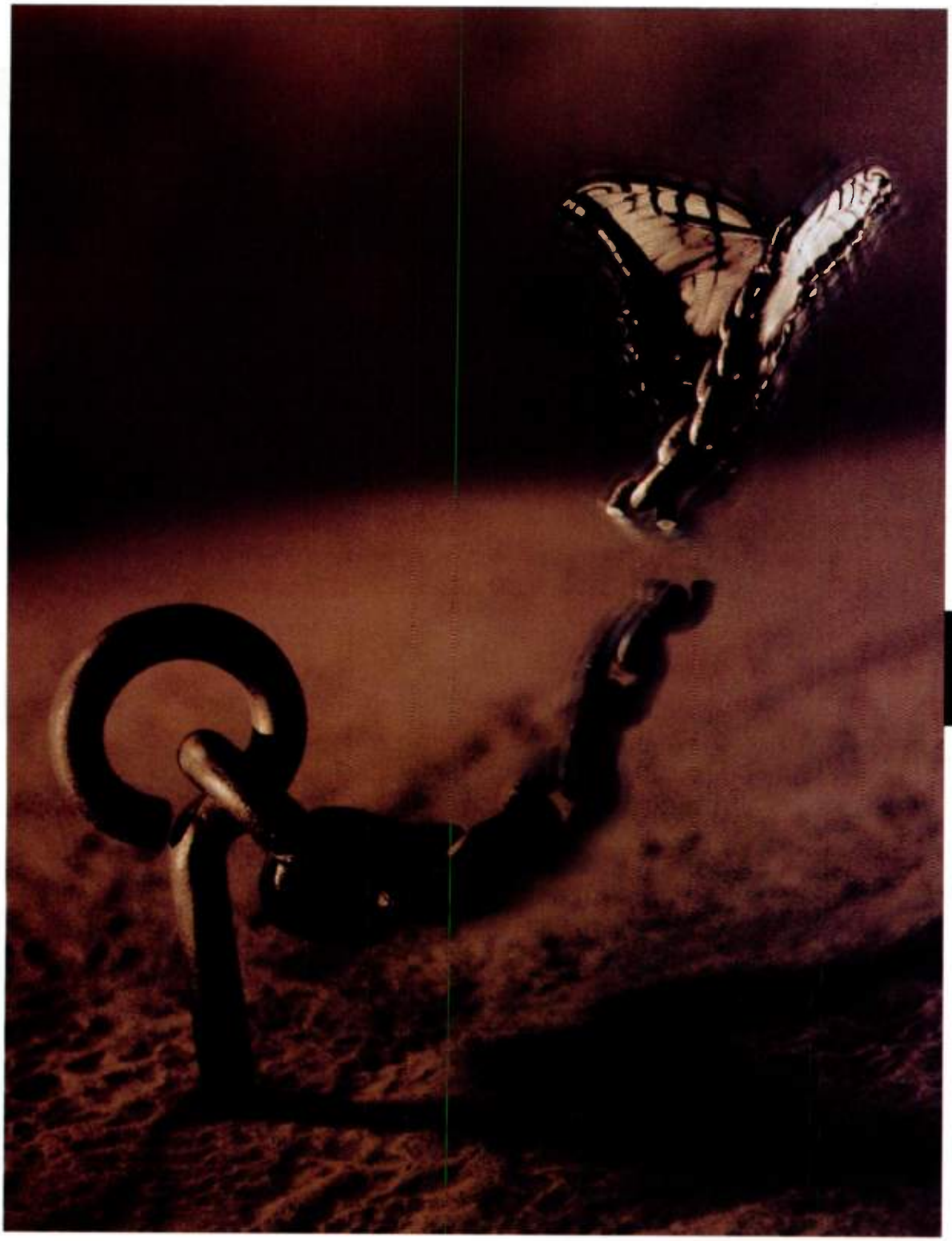

With all due respect to RISC/UNIX-based systems, we think you'll find the Compaq Professional Workstation offers something that's been sorely missing in proprietary workstations. Namely, freedom.

To begin with, you'll have plenty of power to run your specialized applications. This is made possible through a range of cutting-edge performance features. Including Compaq's advanced system architecture which is optimized for Windows® NT and can run up to two Pentium® Pro processors. And because our workstation is based on open systems standards, you'll find it will integrate easily into your existing network. So instead of having to work within the constraints of a proprietary system, you'll have the flexibility to accommodate your needs, whatever they are. Of course, with Distributed Access, you'll also be assured of a transparent connection to all the information you need throughout your enterprise. Even in RISC/UNIX environments.

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Another benefit is the result of our partnerships with leading independent software vendors like Microsoft, SDRC, Autodesk and PTC. Because these solutions have been thoroughly tested, you'll get optimum performance and compatibility.

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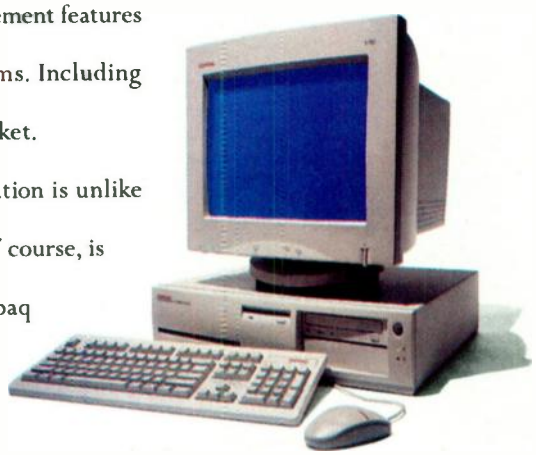
Finally, our workstation provides a lower cost of ownership—not only through price:performance but also through Compaq's industry-leading management features and comprehensive service and support programs. Including hundreds of resellers specially trained for your market.

All said, the Compaq Professional Workstation is unlike any workstation you've ever used before. Which, of course, is exactly the point. For more information on Compaq workstations or Distributed Access, visit us at www.compaq.com or call 1-800-318-7774.



So what's under the hood? 1–2 200MHz Pentium® Pro processors with NT 4.0, a 256K cache, up to 512MB of ECC DIMM memory, an Ultra-Wide SCSI controller, and advanced 2D/3D graphics accelerators.

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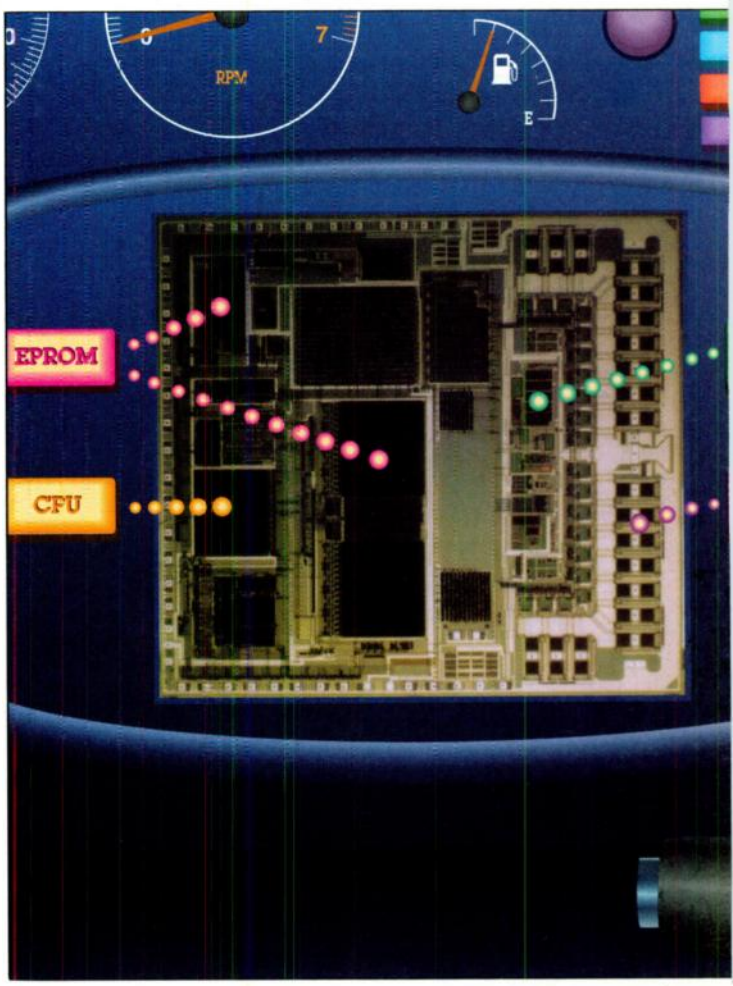
Integrated 8-Bit MCU Handles High-Power Applications

DAVE BURSKY



Although single-chip microcontrollers provide a one-chip solution for many systems, many applications demand capabilities that have not been possible or were too expensive to integrate on the same chip. Such capabilities could include high-current drivers, high-voltage drivers, or other functions that standard CMOS processing can't deliver. Applications such as automotive control systems, consumer appliances, and industrial control systems often require a mix of logic, high-current control, and high-voltage drive capabilities.

Until now, that combination often required at least two or three chips—the MCU for the logic, a high-current driver for motor control, and a high-voltage driver for display or gauge driving. However, thanks to several breakthroughs in process technology, the 8-bit microcontroller division of Motorola can offer MCUs that do it all on one chip. They combine the low-cost of CMOS for the digital logic with high-current drivers to directly control motors, and supply high-voltage drivers to withstand transient spikes and deal with applications such as automobile dashboard gauges.

The major challenge designers at Motorola faced was integrating the features without driving the cost of the controller through the roof. To accomplish this mission, designers crafted the 68HC705V12, an 8-bit member of the 68HC705 family *(Fig. 1)*. On the chip are vertical NPN transistors for the high-current drivers and non-self-aligned, lightly-doped MOS (LDMOS) devices to handle high voltages (transients of up to 40 V).

Unlike older products that may have skimped on the digital functionality to add the high-current or high-voltage capabilities, the digital portion of the V12 is feature rich. Included on the chip are 12 kbytes of EPROM and 384 bytes of RAM; 256 bytes of EEPROM (byte, block, or bulk erasable); a five-channel, 8-bit a-d converter; a serial peripheral interface; both an 8- and 16-bit timer; and a pair of 38-frequency 6-bit pulse-width modulators. All of these features are contained in a low-cost 68-lead PLCC package.

Although the V12, as the first version of the 68HC705V series, is aimed at automotive dashboard applications, that is just the proverbial tip of the iceberg. The same control and power-drive features are a good fit for motor

control in consumer products, toys, and office equipment. Having everything on one chip also opens up new packaging options and system configurations, due to the reduced area and the complexity.

The combined technologies on the V12 are a result of Motorola's internal System Chip initiative. Thanks to the move to integer design rules, the design layouts have been standardized, helping to minimize the differences between chip designs on the fabrication lines. As a result, designers can integrate high-voltage and high-current drivers into not only other MCUs in the HC05 family, but into other MCU families as well.

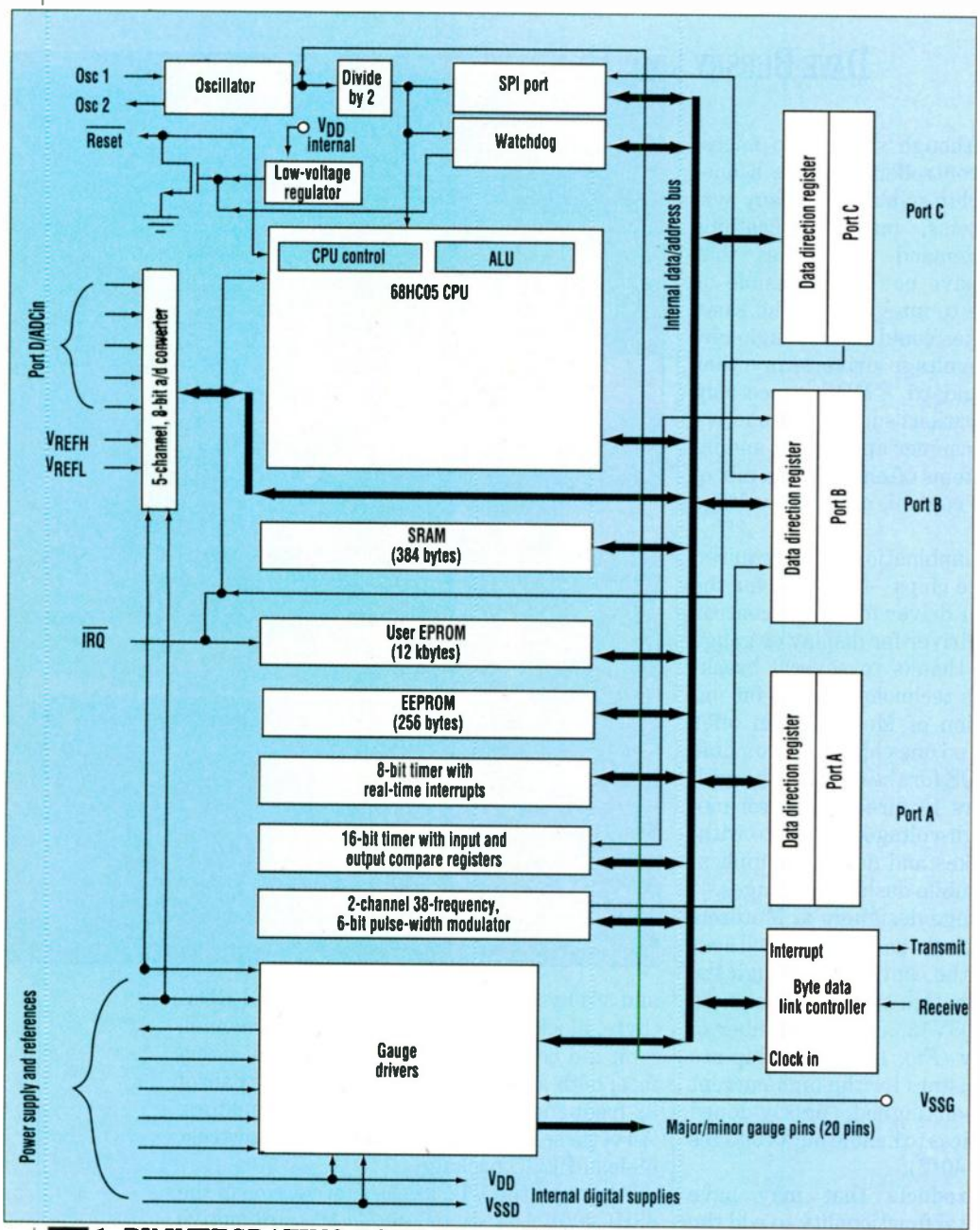
Future efforts at Motorola will move design teams to a unified design rule (UDR) approach to implement consistent chip designs in the newer deep-sub-micron design rules. Potential candidates include the 68HC08 and HC12 microcontroller families, and the popular 68300 embedded processors. Flash memory technology also can be added to the mix, allowing the processors to deliver unique, field-alterable/updatable solutions.

Motorola spent a lot of time analyzing the customers' needs to integrate the functions most efficiently. For example, there are several ways to drive automotive gauges. One approach might have been pulse-width modulation (PWM), but driving the load directly with a linear transistor was a challenge. Audio noise also was a concern (PWM drive could cause the gauge to hum). Consequently, the designers needed a new method. The search first led to a voltage drive scheme, but that idea was at the mercy of how well the coils matched, as well as the accuracy of coils.

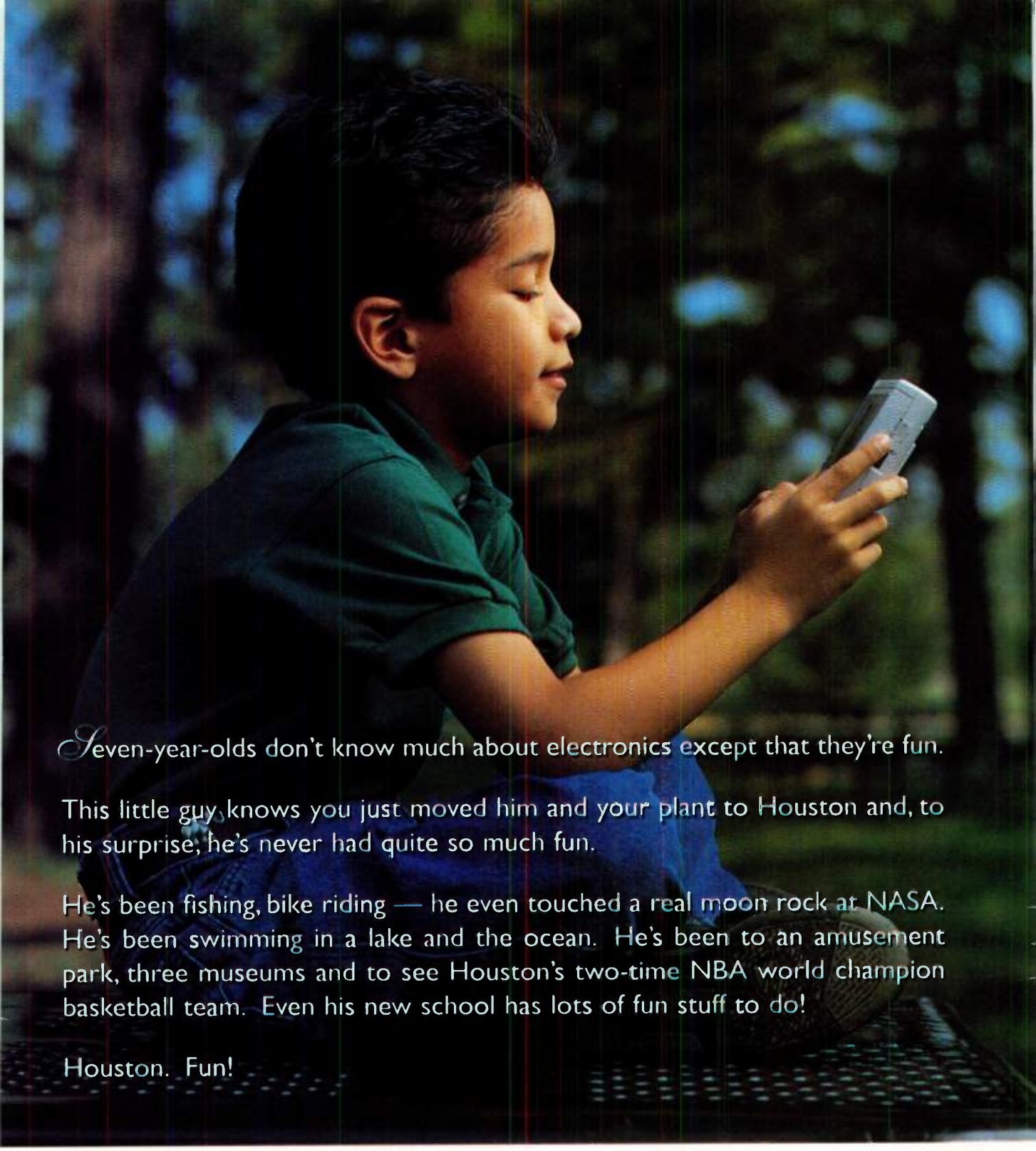
However, by turning the voltage source into a current source and using the current to drive the gauge coil, coil matching was no longer a critical issue (the coil impedance characteristics are less critical). An external resistor then sets the maximum current, which translates into a deflection of roughly 90°.

Implementing the current drive circuits on the microcontroller, though, presented two challenges: How to integrate vertical npn bipolar transistors and how to add high-voltage n- and p-channel MOSFETs that could handle 40 V. Neither of these additions could divert the wafers from the standard CMOS process flow. Motorola had already done the high-voltage circuitry for the 68HC705V8, so the main challenge was to keep that intact while adding the high-current LDMOS transistors for the V12.

The vertical npns are used for circuits that need good precision (better matching) and require less correction or trimming. These devices also are used on the chip to form a Brokaw-type bandgap reference, and for the current amplifiers that drive the H-



1. BY INTEGRATING BOTH HIGH CURRENT AND high-voltage drive capabilities, the 8-bit M68HC705V12 microcontroller provides a single-chip solution for controlling automotive dashboard gauges.



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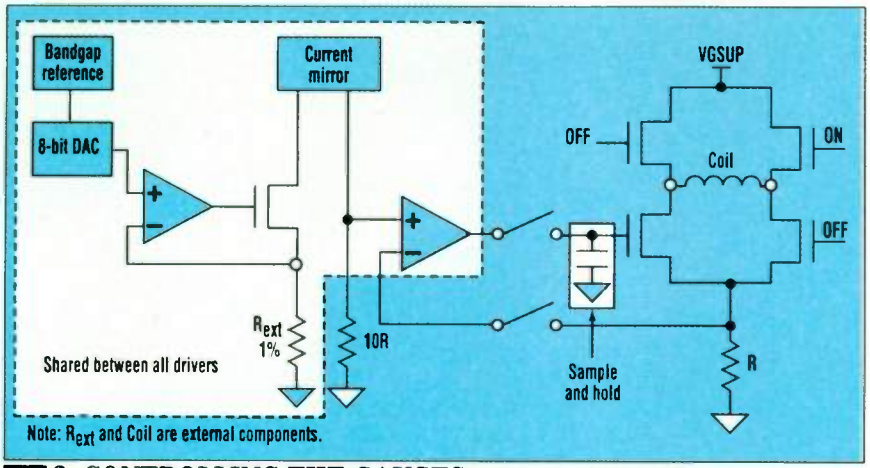


2. CONTROLLING THE GAUGES on a dashboard requires a combination of bipolar transistors forming a simple bandgap reference, and precision amplifiers to drive the LDMOS H-bridges that provide the current drive and high-voltage tolerance.

bridge LDMOS coil drivers *(Fig. 2)*. This reference is less complex than other reference types that would have had to be used if the vertical transistors weren't available. Other types of references also would result in a larger chip area for circuitry needed to compensate.

In total, the V12 employs several hundred vertical npn transistors in various circuits. Based in N-well diffusion regions, the transistors deliver f_T's of about 300 MHz, providing plenty of bandwidth for applications such as gauge driving *(Fig. 3a)*. Associated parasitic PNP transistors are present as well, but with proper biasing, they do not cause any problems.

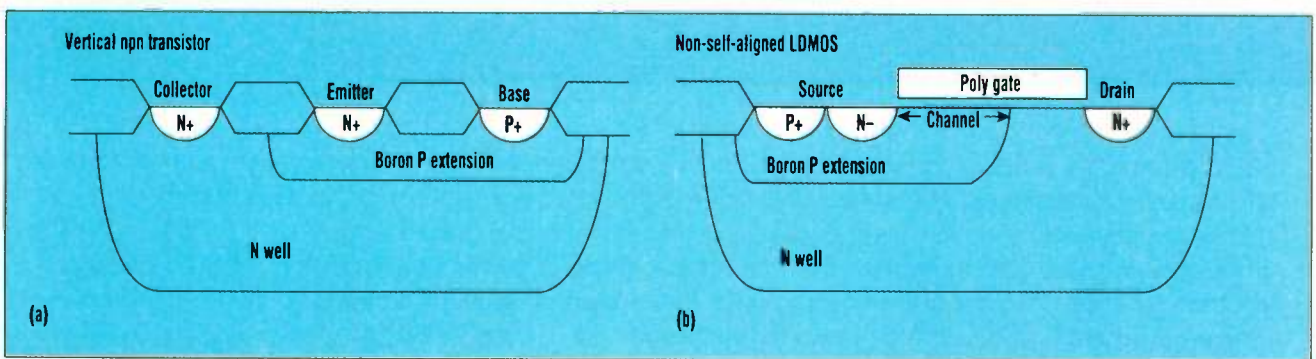
The LDMOS devices, able to withstand load transients of up to 40 V, are needed to handle the direct battery connection. These devices are formed in N-well regions and use a non-self-aligned fabrication sequence that keeps the structure very simple *(Fig. 3b)*. The LDMOS devices are added to all pins that directly connect to any automotive energy source in order to protect the rest of the microcontroller from transients.

When fabricating the transistors, the drains must be diffused separately. In a conventional flow, the gate polysilicon must be deposited first, followed by the diffusions. That rules out self-aligned techniques, and means that a more-precise lithography step is required to align everything. The LDMOS devices are not fully utilized; aspects of their performance may be used in other applications. For instance, they can switch currents of up to half an amp, firing a squib or other device to open an air bag or light lamps.

The LDMOS devices on the V12 are used in H-bridge configurations to drive the gauges. The V12 has enough LDMOS devices to drive six gauges. Two are 360° gauges (speedometer and tachometer) which have two coils in each, while the other four are single-coil devices with a more limited range of motion. Each of the two 360° gauges needs two full H-bridge output drivers. Each of the other four gauges needs one full H-bridge and a half-bridge. Altogether there are 36 LDMOS devices on the V12 (one H-bridge contains four devices to drive the coil in either direction). In addition to the LDMOS drivers and vertical npn transistors, the V12 provides interface and digital resources to provide the control and intelligence needed for the myriad of applications the chip may face.

For data transfers, the chip includes two interfaces: a byte data-link controller (BDLC) for communications over the J1850 automotive bus and a serial peripheral interface (SPI port) for chip-to-chip data and control transfers. The BDLC block fully implements the SAE J1850 class B data communication network interface standard and includes the receive/transmit buffers, the protocol handler, and the multiplexer interface to the J1850 transceiver. The SPI port provides the user with a simple serial interface through which other SPI-compatible support chips can be connected to add more memory or application-specific functions.

To tie into the real-word inputs from sensors, a five-channel 8-bit ratiometric analog-to-digital converter (ADC) delivers conversions accurate to within ±1 LSB, including quantization errors. The conversion process is monotonic, and has no missing codes. Each channel requires 32 clock cycles to perform a conversion. The clock must be running at a frequency of at least 1 MHz for the converter to function. If the master clock is running at less than 1 MHz, an internal RC oscil-



3. THE ABILITY TO INTEGRATE vertical npn transistors (a) and non-self-aligned, lightly-doped MOS devices (b) allowed Motorola to reduce the system complexity for applications such as motor control, lamp driving, or even squib exploding (air bag activation).

lator (nominally 1.5 MHz) can provide the timing for the ADC. This feature comes in handy when the CPU clock is reduced to conserve power.

For gauge or motor control, the dual pulse-width modulators on the chip provide 6-bit resolution and include programmable prescaling for up to 38 different frequencies. The prescaling enables the PWMs to deliver signals with duty cycles from 0 to 100%. The PWM outputs can be either active high or active low under software control by setting the polarity bit in the control register. When not in use, the PWMs can be shut off to conserve system power.

Additional support blocks on the chip include an 8-bit timer with real-time interrupt-handling capabilities, and a 16-bit timer with one input-capture and one output-compare register. A watchdog timer also is available.

In the single-chip mode the microcontroller includes 23 bidirectional I/O lines configured as two 8-bit I/O ports and one 7-bit I/O port. There also is a 5-bit input-only port. Individual lines on the bidirectional ports are programmable by the user as inputs or outputs under software control. The pins on one of the 8-bit ports also can serve as interrupt-request lines if the port is not actively performing a controlling function.

Since the microcontroller is software compatible with other members of the 68HC05 family, all existing development tools can be used to create the application software. The HC05 family is supported by a wide range of assemblers, debuggers, languages, and emulation tools that are available from Motorola Inc. and many of its partner companies. □

Dave Bursky's e-mail address is: dbursky@class.org.

PRICE AND AVAILABILITY

The M68HC705V12 will sell for about $17.50 each in lots of 10,000 units and for about $14.00 each in quantities of 100,000 units. Samples are available immediately.

Motorola Inc., Microcontroller Div., 6501 William Cannon Dr. W, MD: OE17, Austin, TX 78735; Betsy Hughes, (512) 891-6503, e-mail: rdgp60@email.mot.com. **CIRCLE 501**

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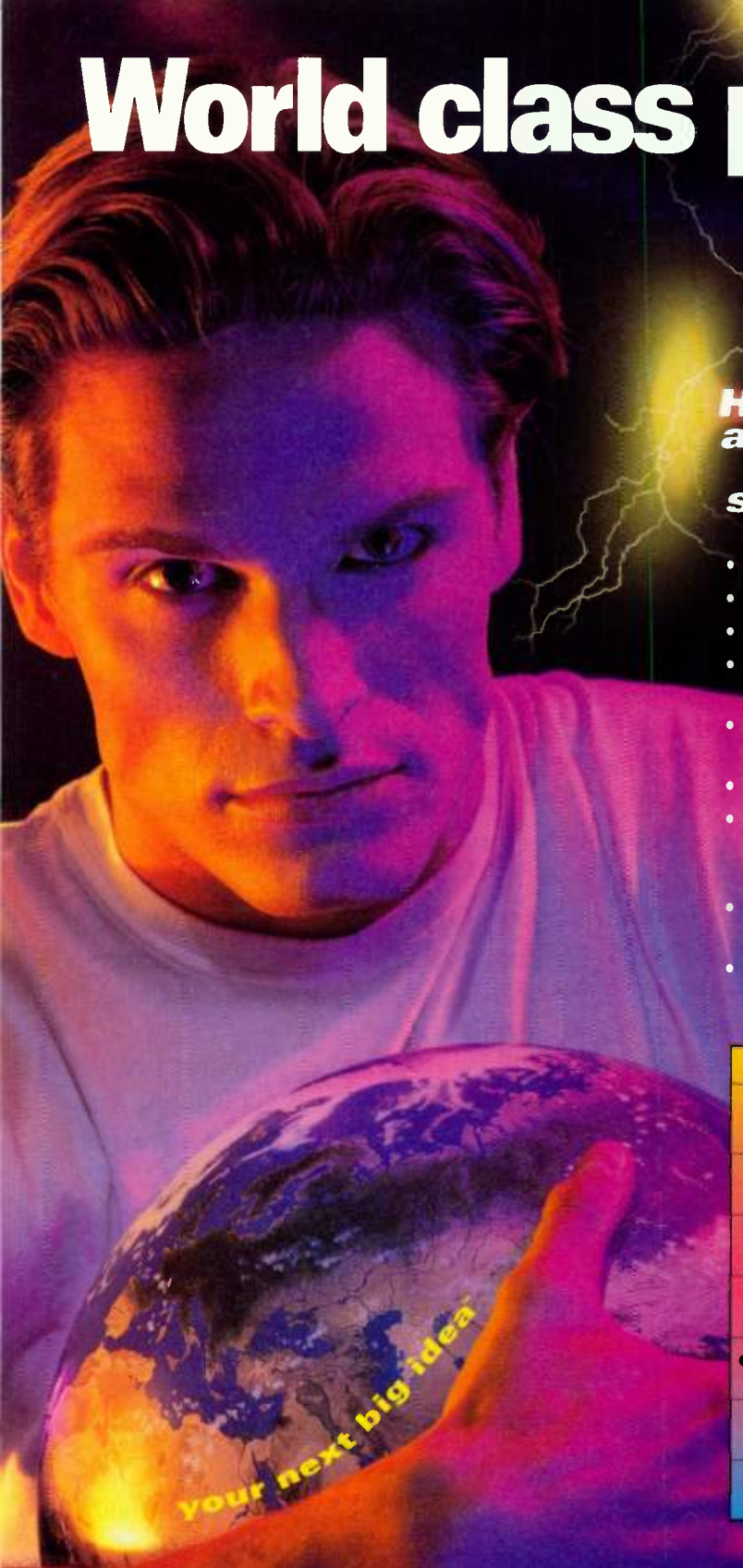

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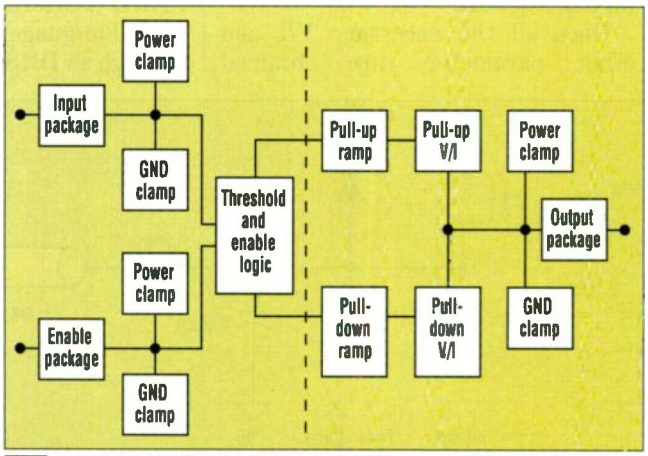
High-performance systems that incorporate features such as parallel processing or other complex functions, and operate at high clock speeds, place tough demands on the design of the boards that hold the circuits. Dealing with issues such as tight clock distribution and high-speed interfaces to meet forthcoming bandwidth-hungry applications are a few of the key challenges designers are facing today.

Therefore, the ability to simulate a design has become a critical factor in the success of a project. Design cycle times are getting shorter, and in many cases, the cost to build a prototype is no longer feasible. To solve these problems, designers need device models to perform intensive and accurate board-level simulation, since this capability has become a requirement rather than an option.

Now, the challenge is: How do you perform the board-level simulation if all the models for the board are not available? Thus far, SPICE has been the only consistent method by which circuit-level models are created today. However, semiconductor vendors that create the models for their chips could not readily give these models out since they often contained proprietary process and circuit information.

There is, however, a solution for modeling thanks to the creation of the I/O Buffer Information Specification (IBIS). This specification is a fast and accurate behavioral method of modeling input/output buffers based on V/I curve data derived from measurements or full circuit simulation. It uses a standardized software-parsable format in the form of an ASCII file to store the behavioral information needed to model device characteristics of integrated circuits. IBIS is compatible with virtually every simulator and EDA tool existent, and is supported by a wide range of industry leaders.



1. THE BEHAVIORAL DESCRIPTION of the input and output sections of a circuit can be defined in terms of a collection of simple functions to create an IBIS model. The main elements in the buffers include input package parasitics, power and ground clamps, threshold and enable logic. pullup, pulldown, ramp rates, and package output parasitics.

WHY IBIS?

The IBIS model file does not require proprietary information about the modeled circuit since no process or circuit design information is disclosed. On the other hand, a SPICE model can disclose substantial information that semiconductor vendors consider to be confidential—circuit nodal connections and process parameters, for example. The IBIS models are also accurate, since nonlinear aspects of I/O structures, as well as package parasitic and ESD structures, are considered in the model parameters.

Furthermore, since IBIS is behavioral, the simulation time for a model can run 25X faster than a structural model such as used in SPICE. In addition, IBIS does not have nonconvergence issues such as encountered in SPICE models, and can run on most

industry-wide platforms since most EDA vendors support the IBIS specification. In contrast, SPICE models from one vendor may not work on other simulators since each commercial version of SPICE has deviated slightly from the original SPICE2G.6.

Tool vendors have made improvements on the post processor in trying to differentiate their tools from other SPICE tools. Some semiconductor vendors also have their own internal SPICE engine that can be incompatible with commercial SPICE engines. By providing one IBIS model, a semiconductor vendor can be sure that it will work on most EDA tools (both SPICE and non-SPICE-based).

One of the most popular uses of IBIS is for signal integrity analysis of system boards. The models are easy to create since they can be made from bench measurements or from simulation data. Simulations of a few nets on a PCB can be done with SPICE, but as the number of nets increase and the PCB gets more complex, it is impossible to simulate the entire board on SPICE. A fast, accurate behavioral method like IBIS is ideal.

Learning To Use IBIS

To use IBIS, a model must be created (a fairly simple procedure). First, examine the behavioral block diagram of an input/output buffer structure and put the various blocks in IBIS notation *(Fig. 1)*. The model of the I/O block consists of many small elements, ranging from package factors to clamping elements to buffer characteristics (thresholds, rampup and rampdown, and pullup and pulldown performance.

Information is needed to model the input structure appears similar to a transmission-line model, with package capacitance, resistance, lead inductance, and I/O-pad capacitance all affecting the input signal *(Fig. 2a)*. C_pkg, R_pkg, and L_pkg are the package parameters. Power_Clamp and GND_Clamp define the ESD structures on the inputs, while C_comp is the input capacitance of the input pin. The V/I curve data defines these clamp structures.

Information needed to model the output structure follows a similar structure, but in reverse *(Fig. 2b)*. Pullup defines the V_{oh}/I_{oh}, Pulldown defines the V_{ol}/I_{ol}, and Ramp defines the dV/dt of the device. The Pullup and Pulldown data are created from the V/I curves. The remaining parameters are similar to the input structure except that they define the package parasitics of the output pin, as well as the output capacitance of the output pin.

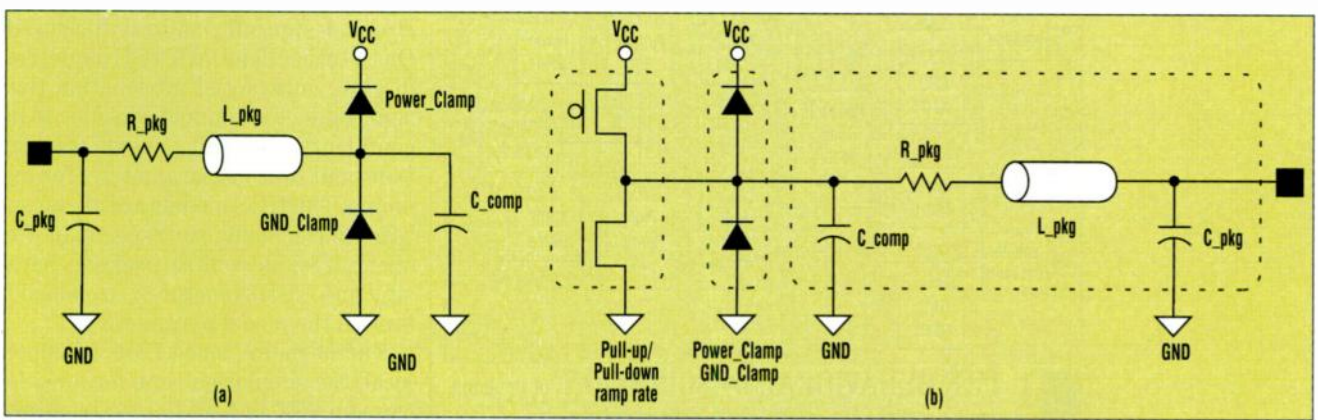
The Pullup and Power_Clamp data are "V_{CC} relative," meaning that the voltage values are referenced to V_{CC} and not ground. V_{CC} relative data is necessary for the simulator since the Pullupstructuredependsonthevoltage between the output and V_{CC}, and not the voltage between the output and ground pin. The IBIS standard also supports multiple types of output structures. Refer to the specification for more details.

Once all the necessary V/I and other parameters are obtained through measurements, simulation, or provided by the chip vendor, the model can be generated *(Fig. 3)*. First, the interconnect engineer creates the IBIS ASCII file following the format defined in the IBIS standard. The ASCII model file is then checked by the "Golden Parser" for possible syntax errors. If passed, the model is then imported into a simulator and validated for accuracy. Now the model is ready for use.

IBIS models can be generated from SPICE simulations or from actual empirical data. North Carolina State University has written a SPICE-to-IBIS converter program. A user can download the shareware program from the ERL (Engineering Research Lab) web site and create IBIS models (the web site's URL is *http://www2.ncsu.edu/eos/project/erl_html)*.

The program, *s2ibis2*, creates an IBIS model file that conforms to the IBIS v2.1 specification and uses HSPICE, PSPICE, SPICE2, SPICE3, or Spectre outputs as the source file. The *s2ibis2* source code, as well as the executable files for various computing platforms, are available from the web site. The source code also can be modified to work with proprietary SPICE engines. The first generation of the converter is called *s2ibis* conforming to the IBISv1.1 specification, and it also is available on the web site.

A handy utility for IBIS, *s2iplt*, is a PERL (Pattern Extraction and Report Language) script that reads through an IBISv2.1 or lower version



2. THE SCHEMATIC REPRESENTATION OF THE INPUT STAGE of a buffer defines various resistance, capacitance, and inductance parameters, as well as clamp characteristics, so that the IBIS input model can be created (a). Similarly, the output model employs many of the same parameter models, but in a reverse sequence (b). The one addition is the specification for the pullup, pulldown, and ramp rate.

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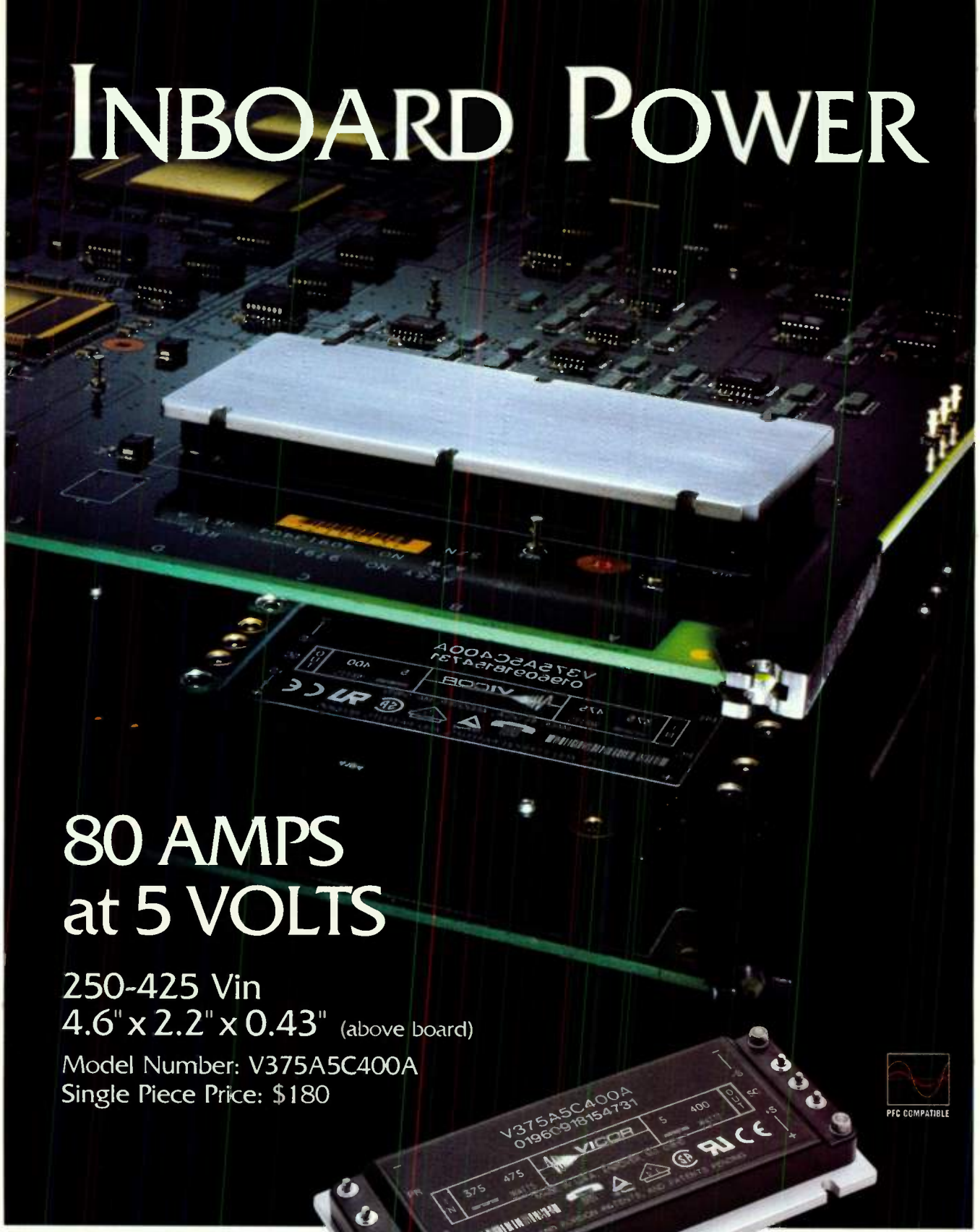

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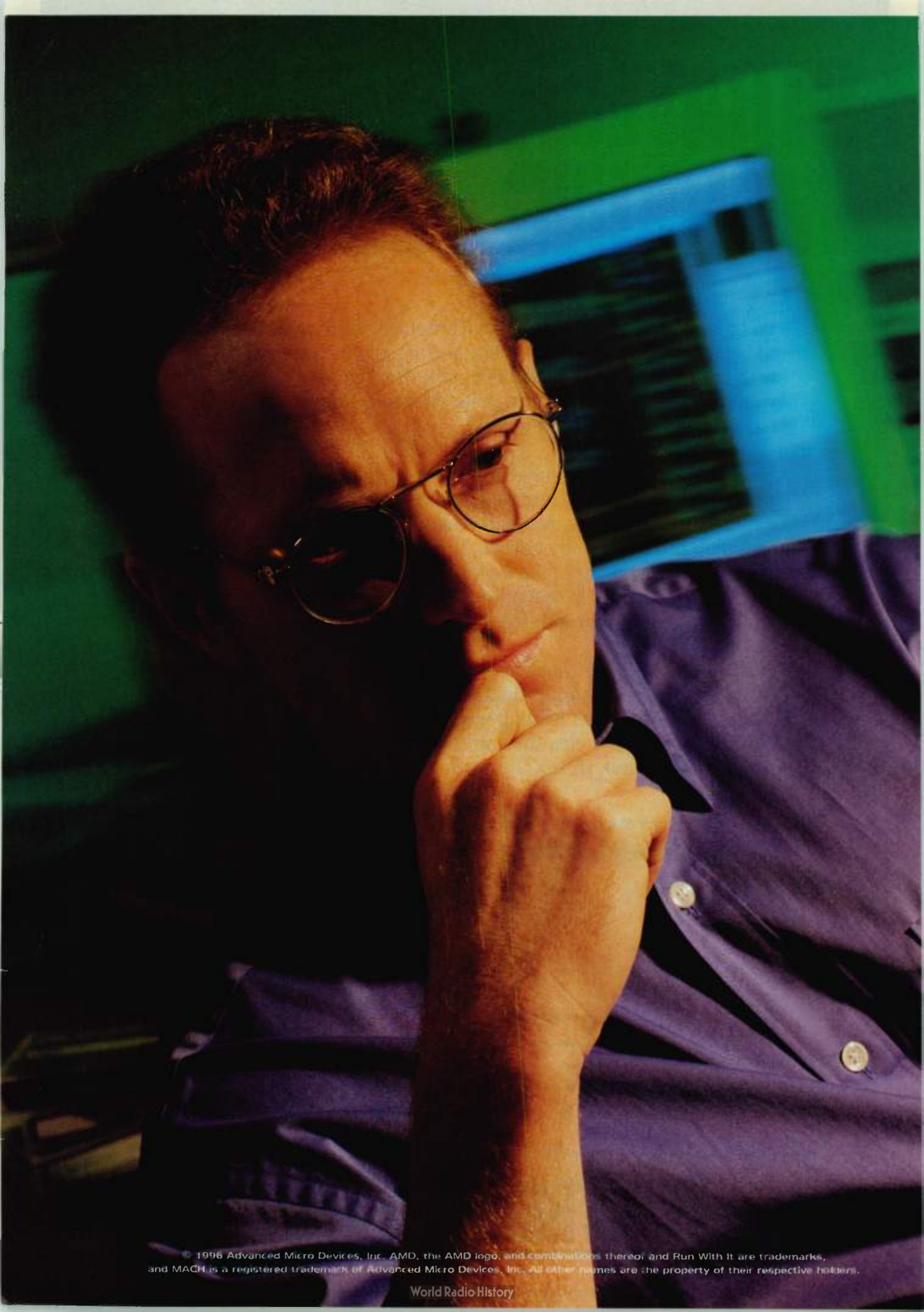

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model file calling *gnuplot* (a UNIX utility) to plot each V/I table. This is a handy utility for IBIS model verification. The V/I plots can give a good indication if something is wrong with the data or data entry.

MODELING AT GROUND ZERO

IBIS models, of course, also can be created from empirical data. To do that, first, identify the number of input and output models that are needed. If certain input/output pins have the same characteristic behavior, they can be grouped together into one model. The Power and GND pins are not modeled by IBIS.

In the model, IBIS requires a number of essential parameters and also gives the user the opportunity to include several optional parameters. These are all detailed in the full specification. To create the model, the following parameters are required:

C_comp: Device input or output pad capacitance

R_pkg, C_pkg L_pkg: Lumped value of package parameters

R_pin, C_pin, L_pin: Pin package parameters

[Pulldown]: V/I table for V_{ol}/I_{ol}

[Pullup]: V/I table for V_{oh}/I_{oh}

[GND Clamp]: V/I table of the ESD structure (low side)

[Power_Clamp]: V/I table of the ESD structure (high side)

[Rising Waveform]: Describes the waveshape of the rising waveform through V/T table

[Falling Waveform]: Describes the waveshape of the falling waveform through V/T table

dV/dT_r, dV/dT_f: Defines the ramp rate for rising and falling transitions.

Before the first measurements are taken, however, there are certain IBIS required formats that must be followed. The IBIS model specifies a range that an input or output structure must be swept. In most cases, these required ranges exceed the Absolute Maximum rating (ABS Max rating) of the device. But the model developer should not exceed the manufacturer's ABS Max rating since that would overstress the die, potentially causing severe damage to the die and corrupting the data. The input/output structure should be swept to the point where the structure starts to break down. Take all the data to this end range value, then extrapolate the linear region of the data to the IBIS specified range. Extrapolation of data to the end point is acceptable by the IBIS forum.

RANGES DEFINED IN IBISv2.1

Keyword	Low limit	High limit
[Pulldown]	$-V_{CC}$	$+2V_{CC}$
[Pullup]	$-V_{CC}$	$+2V_{CC}$
[GND Clamp]	$-V_{CC}$	$+V_{CC}$
[Power Clamp]	$+V_{CC}$	$+2V_{CC}$

Some simulators may not be able to extrapolate correctly. By providing the data across the entire range, the model is more usable across various SPICE or non-SPICE-based simulators. This further guarantees the model to work on various tools supporting IBIS.

After extrapolation, it's a good check to plot the data points to make sure linearity is maintained. A graphical plot may show abnormalities more readily then trying to go through a long listing of V/I data points.

When collecting the empirical data, the following ranges, as defined in IBISv2.1 should be used *(see the table)*.

As mentioned earlier, the [Power_Clamp] and [Pullup] structures are always referenced to V_{cc}. This means that once the V/I data is collected, the voltage table needs to be adjusted (offset) by using the following formula:

THE ORIGINS OF IBIS

The I/O Buffer Information Specification (IBIS) modeling format was originally developed by Intel and is now being driven by the IBIS forum with over 35 members, consisting of EDA vendors, computer manufacturers, semiconductor vendors, and universities. The initial standard, IBISv1.0, was released in April 1993 and is capable of modeling standard TTL or CMOS I/O structures. Later that year, an enhanced version, IBISv1.1, was released—the major changes consisted of more comments to the original specification.

IBISv2.0 was ratified in 1994, and represents a considerable improvement over IBISv1.1. Some of the added features include: Multiple rail support (ie. V+ and V-supply for RS-232), ECL, terminator models, open drain models, differential I/O, controlled slew rate/GTO buffers, and definitions of complex package parameters.

In late 1994, IBISv2.1 added more comments to clarify v2.0, and today, IBIS is an approved standard from the EIA (Electronic Industry Association), now referred to as ANSI/EIA-656. Work is now under way to extend IBIS for International Standardization.

Currently, the standards committee is working on adding additional features to the forthcoming v3.0 specification. Some of the new features will include: An enhanced package/connector definition, stored charge effect in diodes, feedback support, multiple drive level capabilities, parameter scaling effects, and a refinement of the simultaneous switching output model.

The software parser (which is commonly known as the "Golden Parser") validates the IBIS model file. The function of the Golden Parser is to check the syntax of the IBIS model file to confirm that the data format meets the IBIS specification. The object code of the parser is available for free from the forum. Simulator vendors or member companies may also purchase the source code for a fee.

Future versions of the IBIS standard will be backwards compatible with previous versions so all models created today using the present version of the specification are guaranteed to work with future versions of IBIS. The IBIS forum is continually defining new and improved ways of modeling complex and unique I/O structures and interconnects.

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runs over that GPIB connection comes from Metrics. This software includes various driver programs for the instruments such as the TEK370A and the HP4145. By using the Metrics software on a PC with GPIB capability, a user can network the bench measurement equipment to the PC and automate the measurement and data collection procedures.

The Metrics software does a quick sweep (single-shot) and collects the data. Data can then be plotted by the software, and is saved in an ASCII file in the V/I format as required by IBIS.

Another option is the Kiethley 220, a programmable current source that also can be tied to a GPIB networked PC. It should be noted that the DUT can heat up as the PC executes read/write sequences for each data point. Thermal feedback can alter the accuracy of the data being taken. Thus, thermal effects caused by the latency involved in executing GPIB read/write commands must be taken into account.

Another tool, the Interconnect Parametric Analyzer (IPA510), uses a TDR methodology along with DSP software to extract various interconnect models based on reflection profiles. This can be used for package parasitic measurements or to collect input/output capacitance values of semiconductor devices.

To perform the measurements the sequence of operations is relatively simple. For instance, to measure [GND_Clamp] and [Power_Clamp] for the input model use the following sequence:

(a) Apply power to the device
(b) Connect the "collector" from the curve tracer to the input pin under test
(c) Tie the "emitter" on the curve tracer to ground
(d) Sweep the input structure from 0.0 V towards negative voltage to the point the clamp structure turns ON to capture the [GND_Clamp] values and sweep the input from 0.0 V to positive voltage to the point where the clamp structure turns ON to capture the [Power_Clamp] data. Sweeps can be done on both clamp structures simultaneously to the point where breakdown first starts to occur.
(e) STOP the sweep and collect the V/I data. As explained earlier, extrapolation should be used to extend the data to the IBIS required range.

Note that on an automated bench setup, if the current values are very small ($\approx e^{-12}$), the resolution of the bench equipment may give positive and negative values of current for each voltage step until the value of the current increases significantly. Such data can violate IBIS rules for monotonacity. To compensate, the user can manually zero out the current readings. This effect can be experienced when sweeping the power clamp structure from 0.0 to 5.0 V. Typically, the current in this region is very small—just at the point that the diode starts to conduct.

AFTER EXTRAPOLATION, IT'S A GOOD CHECK TO PLOT THE DATA POINTS TO MAKE SURE LINEARITY IS MAINTAINED. A GRAPHICAL PLOT MAY SHOW ABNORMALITIES MORE READILY THEN TRYING TO GO THROUGH A LONG LISTING OF V/I DATA POINTS.

To measure [Pullup] and [Pulldown] for the output model, a simple procedure also can be set up. In a device datasheet, [Pullup] is referred to as V_{oh}/I_{oh} data, and [Pulldown] is referred to as V_{ol}/I_{ol} data. The measurement method is similar to [Power_Clamp] and [GND_Clamp] measurements.

(a) For a three-state output, the output [Power Clamp] and [GND Clamp] values should be measured with the output in its high impedance state. That isolates the [Pulldown] and [Pullup] data from the [Power Clamp] and [GND Clamp] V/I data. The [Pulldown] and [Pullup] data must represent the difference of the three-state and the enabled buffer V/I data. Such a requirement enables the simulator to sum the curves without the danger of double counting. The user must then force the device into a "High" state for [Pullup data] and into a "Low" state for [Pulldown] V/I data.
(b) For non-three-state devices, the [Pulldown] and [Pullup] data will contain the effects of the ESD structures ([Power Clamp] and [GND Clamp)]. In this case, there is no need to create clamp V/I tables for the clamp structures.
(c) Always plot the V/I tables to see if there are any anomalies due to possible data corruption.

The only ac measurement required for IBIS modeling, the dV/dt_r and dV/dt_f parameters also can be done with the automated equipment. The tests are similar to tests that perform risetime or falltime measurements for digital devices. This test requires only one datapoint measured between the 20% to 80% voltage value and the time value is recorded to get the ramp rate. The ramp rate should be measured with no loading on the output structure. A user should employ a high-bandwidth oscilloscope with a low capacitance probe to avoid loading effects. One such scope, the Tektronix 11801B (20 GHz) series with SD-14 probes (3 GHz), can readily handle the measurements.

Measuring the [Rising Waveform] and [Falling Waveform] values can be done by modeling the Gradual Turn On circuits (GTO) by using the assigned keywords. GTO circuits can be found in GTL, Crossvolt, and other devices. The Tektronix IPA510 along with the 11801B scope setup can be used to capture the Rising Waveform or the Falling Waveform in an ASCII V/T table format as required by the IBIS standard. The Docuwave software from Tektronix also can be used to create a

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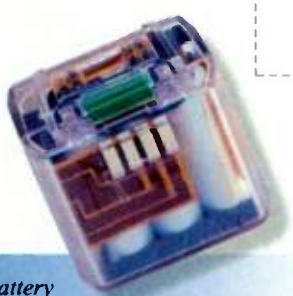

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High performance electronics and the high-frequency transfer of data in telecommunications are dealing with ever greater volumes of data. This also means ever-increasing demands being made on socket connectors. Starting with what originally were very simple mechanical connectors ERNI has developed high-pole systems which offer connection reliability, are simple to assemble and possess superior electrical properties: ERmet socket connectors.

The special feature of ERmet socket connectors is their optimum signal and transmission response which transfers data without any time delay or signal loss, without any reciprocal influence or other electro-magnetic interference. We are able to achieve this thanks to special design feature such as constant geometric conditions and conductor cross-sections as well as pseudo-coax arrangements of signal and earth-conducting pins.

With ERmet socket connectors we haven't actually superseded the laws of physics but just improved on the way they are translated. The basis for this comes from a series of extensive test programs on the responses of a wide variety of connector systems in the pico second range. These test results form the basis for simulation models which enable us to calculate the response of our socket connectors during the design phase itself. We can therefore reduce the development times and adapt our systems on a more targeted basis to meet the tasks required by our clients.

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Fax: ++ 65 83 50 948

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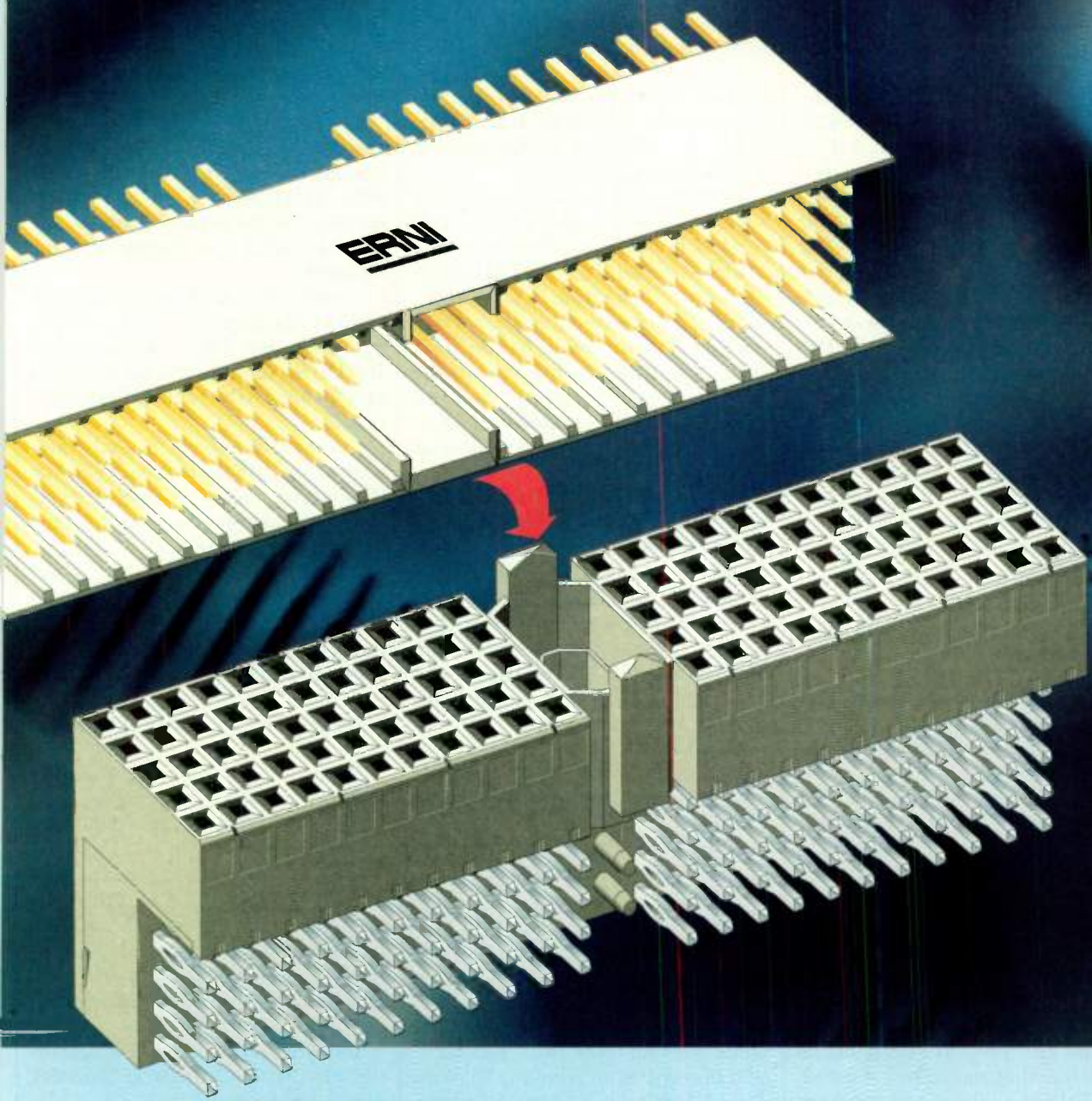


ERNI Components, Inc.

12701 North Kingston Avenue
USA-Chester, VA 23831
Phone: ++1 804 530 5012
Fax: ++1 804 530 5232

ERNI Components

1630 Oakland Rd Suite A 107
USA-San José, CA 95131
Phone: ++1 408 453 7077
Fax: ++1 408 453 7078

Further addresses can be found on the Internet under: http:\\www.erni.com or on request.

READER SERVICE 188

.CSV file that can be read into an Excel spreadsheet. The .CSV file again saves the waveform data in an IBIS-required V/T table.

Handling Model Files

The IBIS standard specifies the creation of MIN, TYP, and MAX models. It is difficult to take MIN, MAX data over process corners and temperature ranges, and such measurements can be best done by the respective semiconductor vendors. A TYP model can be created by an end user from the guidelines previously described. A DOS or UNIX text editor may be used to create the IBIS ASCII model file. The UNIX format is the preferred format but whichever is used, the model should always be checked by the parser to ensure IBIS compatibility.

The IBIS parser test uses the Golden Parser to make sure the model file conforms to the IBIS specification. The Parser does not indicate if you forgot to insert the proper "units," but it is robust enough to catch various IBIS specification violations. To invoke the Parser, just type:

% ibischk2 filename.ibs (Hit Return)

The Parser can run on various platforms and can be downloaded for free from the web site referenced at the end of the article.

The results of all the data collection and parsing is an ASCII table file that includes all the data points require to construct the model *(see the listing)*. Furthermore, all models must be validated for accuracy. This can be done by simulating the model with a known load and comparing the simulated data to actual bench measured data under similar loading conditions. Rise and fall times are some of the parameters that should be validated. If the IBIS model is generated from bench measurement, the measured and simulated data will match perfectly. □

Syed B. Huq is a Staff Applications Engineer for the Interface Products Group, and has been working at National Semiconductor for nine years. He also is involved with signal integrity analysis/simulations, IBIS device modeling, and Interconnect model extraction. He holds a BS degree in Electrical Engineering from Southern Illinois University. Syed is presently vice chairman of the ANSI/EIA-656 IBIS committee.

References—Where to find more information on IBIS:

IBIS: I/O Buffer Information Specification Overview, Intel Corp., Hobbs, W., Muranyi, A., Rosenbaum, R., and Telian, D.

vhdl.org: (198.31.14.3) has been a central location to find various IBIS-related information. This includes: Models, Golden Parser, BIRD (Buffer Issue Resolution Documents), Summit information, and a participating company roster listing. This is an anonymous ftp site and anyone can log on as *anonymous* and use their E-mail ID as a password. Dial-up modem access also is available at (415) 335-0110.

ANSI/EIA-656: This IBIS web site serves as a central location that will continually provide various tools and resources in helping to create IBIS models. IBIS related articles, FAQ (Frequently Asked Questions), Hypertext links to information on vhdl.org, Virtual Poster pages with hot links to member companies are some of the items available through this web site:
http://www.eia.org/eig/ibis/ibis.htm

North Carolina State University: The university provides SPICE-to-IBIS translator tools from their site at: *http://www2.ncsu.edu/eos/project/erl_html*

Hyperlynx: This company provides a tool called "winibis" that can be used to edit and plot IBIS models on a PC. The tool also supports syntax validation and has general template files for both v1.1 and v2.1. Winibis can run on Windows 95, Windows NT, Windows 3.1 and Windows for Workgroups. Follow the directions provided and download this tool from their web site at: *http://www.hyperlynx.com*

Semiconductor vendors providing models today: National Semiconductor provides IBIS models for various products that can be downloaded from their web site at: *http://www.national.com* Check the web site at *http://www.eia.org/eig/ibis/ibis.htm* under *models* for other semiconductor companies that currently provide IBIS models.

How to join the reflector or ANSI/EIA-656: *ibis-request@vhdl.org* To join, change, or drop from either the IBIS open forum reflector *ibis@vhdl.org*, the IBIS users group reflector *ibis-users@vhdl.org* or both. You must state your request.

ibis-info@vhdl.org: To obtain general information about IBIS, ask specific questions for individual responses, and to inquire about joining the EIA-IBIS open forum as a full member.

ibis@vhdl.org: To send a message to the general IBIS open forum reflector. This is used mostly for IBIS standardization business and future IBIS technical enhancements.

ibis-users@vhdl.org: To send a message to the IBIS users group reflector. This is used mostly for IBIS clarifications, current modeling issues, and general user concerns.

ibischk-bug@vhdl.org: To report *ibischk2* parser bugs. The bug report form resides on *vhdl.org* in */pub/ibis/bugs/bugform.txt* along with reported bugs.

Instrument/Software Suppliers:

Metrics Technology, 417 Tramway NE, Suite #2, Albuquerque, NM 87123; (505) 299-9591, fax: (505) 275-6261 or (800) 398-1490.

National Instruments with LabVIEW, (800) 433-3488 or (512) 794-0100, ftp site at: *ftp.natinst.com* Login: *anonymous*, Password: *your E-mail ID*. Look under: */support/labview/windows/instruments/lv30/gpib*

Tektronix Inc. P.O. Box 500, Beaverton, OR 97077-0001; (800) 835-9433. *http://www.tek.com*

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115.
http://www.keithley.com

How Valuable?	Circle
Highly	546
Moderately	547
Slightly	548

WHAT'S ALL THIS TEAMWORK STUFF, ANYHOW?

Once upon a time, many years ago, there was a playboy who attended Harvard. He did not play football, but he hung around the football team a lot. One day, he heard all his football-player friends bragging about how they were going to beat Yale this year. In fact, they bragged that they were going to shut them out!

This guy was not necessarily very bright, I must point out. So he went to his neighborhood bookie and bet $1000 that Harvard would shut out Yale. He came back and told his football friends how much confidence he had in the Harvard defense to hold Yale scoreless.

BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

His friends were horrified. I mean, bragging around the locker room is one thing, but to actually put down a lot of money, at long odds, was something else. So they calmly suggested to their playboy friend that maybe he should *hedge* his bet.

So he went off to the bookie and came back and proudly announced that he had bet another $1000 that Yale would hold Harvard scoreless. His friends just groaned—if he was that stupid, how could they protect him from himself?

Well, that was the year that Harvard played Yale to a scoreless tie, and the dumb fellow cleaned up, winning many THOUSANDS of dollars, while the football players were completely *astonished*.

Now, I asked my old Harvard friend, Malcolm, if Harvard's football team ever did play a scoreless tie against Yale. He told me yes, in 1929 and 1932. Still, this must be considered an apocryphal story. Quite possibly, this bet never happened. Quite *probably* it never happened. But still, it's a story. Or, maybe it's one of esaeP's Fables....

Recently, I happened to run into a couple of young NSC engineers who had just come out of a training meeting. They were very enthusiastic about the material they had just been studying. One said earnestly, "On this new project, we are really going to *CREAM* TI. We are going to *FLATTEN* Motorola. We are going to *DEMOLISH* Analog Devices. Because we have our Teamwork going for us." The other guy spouted some more phrases that indicated he really had taken to heart some of the training he had learned about "Teams." He said, "Since we are working as a team, we are invincible, and we can solve any problem."

I winced, closed my eyes and tried to clear my head. I had heard about some of the new "team leadership" training propaganda. I thought, from what I heard, it was mostly just a lot of gung-ho stuff, a bunch of baloney. But now, some of the young engineers were talking as if they believed it was absolutely true. Just like that Harvard playboy.

At that time, I did not engage in a debate with these guys, because I knew that our management believed in "teamwork," and I did not want to be an old negative SOB, not right at the start. I decided to lie low and learn what was going on in these training meetings. After all, if we can learn about Apples and Oranges and Taguchi Methods and Fuzzy Logic at these training courses, maybe the "Team Spirit" is just another wonderful new, modern technique.

But, if I ran into these guys again, gushing their platitudes about how GREAT we are going to be, *just* because we work in teams, I would take them quietly aside and ask them where they are getting their ideas from....

But I have seen that *more* and *more*, *team*work is proposed as the *right* way, the *correct* way, the *only* way to do anything here at NSC. If I am a hero, our *team* is supposed to get the credit. If I contribute to the *team*, then everything will be *fine*....

Ya know, that is a fine theory, but I am still a little skeptical. A team is still made up of *individuals*. If an idea is to be generated, it is *usually* generated by an individual. NOW, don't get me wrong. If you have a good team of people, and one guy asks a good question, which leads to another guy doing an experiment, and the data is analyzed by another guy, and one other person is then able to come up with a *SOLUTION*, hey, I am all in favor of THAT kind of teamwork.

You know darned well, one person operating in a vacuum, all by himself, can often do some brilliant work, but he can (even more often) make some stupid errors—preposterous errors. He (or she) can make dumb errors that he (or she) cannot see. One person on his own can expand these errors until the brilliant wisdom is completely overcome by the fatal flaw, and his efforts will fail. I am absolutely in favor of people checking each other out. I almost always try to get other people to check my work. BUT, that is NOT the same as "teamwork."

Let me say that another way: A mindless, Pollyanna-ish dependence on the CONCEPT of teamwork is NOT necessarily a good idea. The idea that the individual's effort should be in submission to the team spirit—that sounds to me a little like the spirit of the old Communists, or the Utopians. And we all know that the Communists had good intentions, but they could not always make it work.

Let me cite a couple of examples—not from Russia in 1934, but from NSC

in 1994. There was a study group to improve on the yield of a product. The yield started out OK, but the customers needed highest performance, and the highest yield on the tightest spec. And, the yield was LOUSY because that spec should never have been done. The study group was formed, as a TEAM, and had many meetings. It was harmonious. It was carefully run by a chairman. It had OARRs. (OARRs = Objectives, Agenda, Rules, Roles....) It had efficient meetings. Nobody shouted, nobody interrupted, nobody said anything politically incorrect. It came to several conclusions after several experiments.

Just one problem: It was wrong, and the experiments were misplanned, and the conclusions were wrong. The whole *TEAM* was headed in the wrong direction, because they did not have the right EXPERT on the team. How did I find out about this? Ah—I found a superfluous copy of the (very carefully and neatly typed) minutes of a team meeting left in the copy machine. I looked at this, and realized to my great concern, that the EXPERT on this subject did not seem to be on the Distribution List. I went to see that individual, and suggested that he should check this out and should invite himself onto the team,and straighten them out, and also see if he should not impose his wisdom onto the team and solve the problem. He did. The problem was solved, although there were delays along the way.

Who was the EXPERT not included on the TEAM? Robert A. Pease, the Czar of Bandgaps. How did the EXPERT solve the problem? He proposed a new layout, with better common-centroid layout of the main voltage-divider resistors. The new wafers finally came out of FAB, after some delays. The proof of the actual improvement had to wait until we got the parts assembled and baked, for it was the improved Assembly Shift and the short-term and long-term stability that proved this "improvement" was really good. These aspects of performance cannot normally be predicted by computers....

NOTE: Some people have argued that if we just use processes that are "well characterized with good models," we can always design circuits that will work as planned. But with analog circuits, there are many cases where the best "characterization" of process and parts, is not helpful, not enough. The computers and the simulation all FAIL, and are of no help, only a DAMNED HINDRANCE. As for the proposal that "good models" are helpful—I disagree. Not all models are helpful. Layouts and mechanical stresses, and thermal interactions, etc., are substantially IMPOSSIBLE to handle in any computer analysis.

I have seen many places where a team can delude itself, that they are "doing great," but actually they do not know what is going on. Example: I got on a team. I proposed an improvement that would help us a lot. I wrote it down, and sent out copies to the team. I specifically asked the team members if they saw anything wrong with my proposal? Nobody said anything. We began to plan an extra bonding pad for trimming a part after assembly. We almost ran a test pattern to find the best way to do double zener-zap trim after assembly.

Just one thing was wrong: There was no available bonding pad that could be connected for after-assembly bonding. So, all my work was a minor waste of time. Several people COULD have asked me, "Bob, are you sure that connection you want can be bonded out?" But, the bad kind of team mentality was in effect. Nobody said BOO. Nobody asked the right question.

Note: In TOO DARNED MANY MEETINGS the rules are in effect, that we must not all talk at once, and we must not contradict each other, and we must not criticize other people's ideas—NO MATTER HOW STUPID THEY ARE!!!!

Right now, I cannot prove this, but I am taking this occasion to call into question—that when an idea is STUPID ENOUGH, we must flag it, rather than let it go unquestioned. Now, I must admit, there are ideas that look (at first glance) stupid, but are in fact wise, and I want to protect these ideas so they are not trashed. It's not easy to do this. But we can discuss that later. NOW, I want to raise some fairly basic questions.

What is the right way to run teams?

Where is your company's basic philosophy coming from, for the teaching of teamwork? Where are the books? Who are the consultants? Do we really believe they are motivating our people properly?

Is this Utopian (Pollyanna-ish, I say) concept of a team, capable of doing harm? I think so. Namely:

Does it do any good to teach that teamwork will overcome all? I am nervous about any kind of absolutism. Teaching young people that they will surely overcome, because they work in teams, may be VERY DEMORALIZING when they discover they lost a test or game. Hey—the Dallas Cowboys are a team—a good one. And they have lost some games. So are the 49ers—and they can lose. I am annoyed to hear the Pollyanna freaks, saying, we cannot lose if we are a team. Because there are 12 teams going into the NFL playoffs—and 11 of them will end their season as losers.

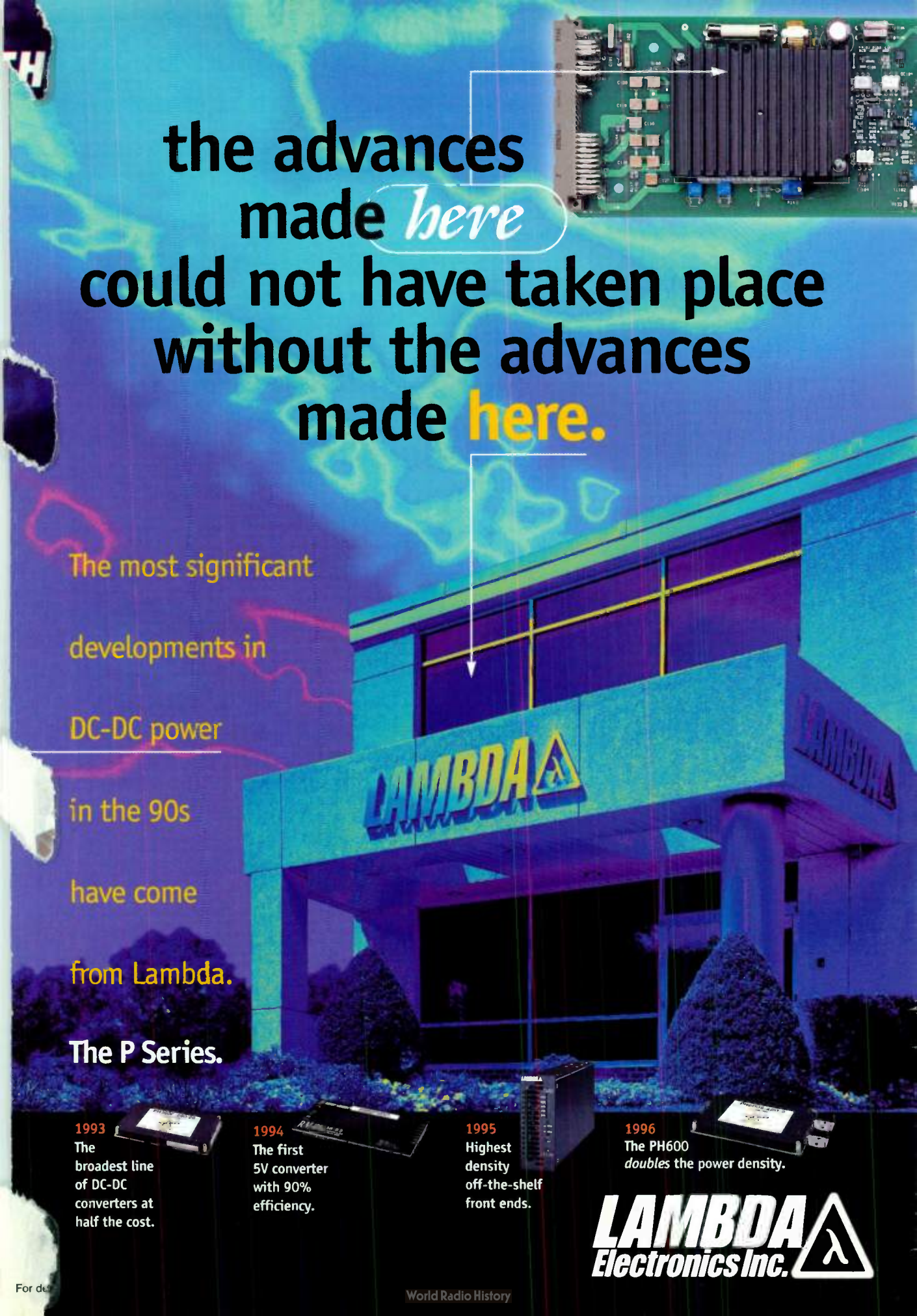
NOW, in business, we do not win every contract, but if we think about it wisely, we can be winners if we win *our share* of the business. If we get demoralized because we do not win every encounter with competition—well heck, that was never realistic in the first place....

When I sent the first draft of this column to Gil Amelio, he proposed to veto it, as he thought I did not have a sufficiently good understanding of teamwork. He suggested I read *The Wisdom of Teams** by Jon Katzenbach, so I would understand about teams, as teams are important to our future.

I read the book—every word in the book. I understood the whole thing. HOWEVER, I checked as I went along, and Mr. Katzenbach did NOT answer my questions about unbridled, unwarranted enthusiasm for teams. The author seemed to be incapable of commenting on unrealistic expectations. He did not seem to think that we needed to worry much about solutions for teams with problem people, or bad chemistry.

NEXT, I read *Why Teams Don't Work*** by Harvey Robbins. That book was not too silly, but not terribly helpful, either. Even when it tried to say "why teams don't work," it was not extremely negative about teams. But it did not deal with the problem of excessive optimism.

I re-sent my text and questions to



Lambda's P Series More modular

PH Series DC-DC Converters

Lambda's PH Series provides 151 high density (up to 62 W/in³) DC-DC converters from 50W-600W with 24, 48, 110 & 300V input voltages. They are available in low cost simple function modules, and fully featured modules for more complex systems. And all models feature 5 million hours MTBF. Lambda's P Series DC-DC converters make modular/scaleable and distributed power affordable for even the most cost sensitive applications. Page 4 and 5

RM Series DC-DC Converters

These 90% efficient DC-DC converters achieve maximum power without a heatsink. And since forced air is the only requirement, the slim 8mm profile provides for maximum power density–ideal for applications where high efficiency and low profile are critical. The RM Series is available in 18 models from 12W to 100W, with features that allow for hot plug, EMI filtering, integral diagnostics and control for the highest performance systems. Page 6

PM and PP Series DC-DC Converters

The PM and PP Series feature 161 single, dual and triple output fully isolated DC-DC converters from 1.5W to 30W. These low cost modules have an 8.5mm profile and are designed specifically for high density, on-board distributed power. In addition, the PM Series are the only converters which meet all the safety agency requirements for computer, datacom and telecom applications–including Bellcore and ETSI. Page 7 and 8

Component Front Ends

Lambda has a complete line of high density component front ends for distributed power or custom power solutions, including PFC front ends with either 48 or 360VDC outputs. Page 9

power solutions for more applications.

With the broadest selection of modules in the industry, Lambda has everything you need to tailor a power system to your application – and at prices that make the latest power architectures affordable.

Rectifier and EMI Filter Modules

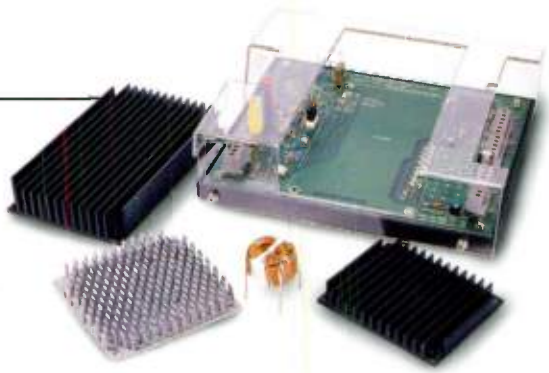
Lambda's PR and PN/PBP Series offer the complete input solution by meeting conducted EMI to FCC/VDE Curve A and rectifying the input for off-line applications. Page 9

Distributed Front Ends

New Models

Lambda has a complete line of bulk front end AC-DC converters and racking systems from 500W-6kW – ideal for hot-plug, fault tolerant applications. These high reliability solutions are available with PFC and worldwide input voltages for both 24V and 48V distributed systems. Page 10 and 11

Accessories



Lambda offers a complete line of Evaluation Kits and accessories to develop power module applications. The Evaluation Kits come with a printed circuit board and all the components and heatsinks necessary to evaluate a module within minutes. The heatsinks, thermal pads, sockets and noise chokes are available separately to minimize your development time. Page 12

Turn-key Solutions

Turn-key solutions using Lambda's reliable standard power modules can be easily configured to create custom power solutions. Whether the need is for fault tolerant N +1 hot-plug power, ATE or mass storage solutions, Lambda ensures minimal NRE and a very short low risk design cycle. Page 15

Full Function Modules

Lambda's Full Function P Series modules achieve 5 million hours MTBF. Active single wire current sharing coupled with a module good signal enables these low cost converters to easily accommodate N+1 and scaleable power systems. They feature an auxiliary power supply output designed to power external monitoring signals, +20%/-60% output adjustability and up to 90% efficiency–ideal for all computer and leading edge communications applications.

SELECTOR GUIDE: PH75 FXX-2 — **NOMINAL INPUT VOLTAGE 48VDC, 280VDC**

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OUTPUT POWER (W)	24V INPUT	MODEL 110V INPUT	48/280V INPUT	UNIT PRICE PER DELIVERED QUANTITY 1	10	100
2	15.00	30.00		PH75F110-2	PH75FXX-2	$109	$99	$81
2	20.00	40.00	PH100F24-2			150	136	111
2	30.00	60.00		PH150F110-2	PH150FXX-2	150	136	111
2	60.00	120.00		PH300F110-2	PH300FXX-2	236	215	175
3	15.00	45.00		PH75F110-3	PH75FXX-3	109	99	81
3	20.00	60.00	PH100F24-3			150	136	111
3	30.00	90.00		PH150F110-3	PH150FXX-3	150	136	111
3	60.00	180.00		PH300F110-3	PH300FXX-3	236	215	175
5	15.00	75.00		PH75F110-5	PH75FXX-5	109	99	81
5	20.00	100.00	PH100F24-5			150	136	111
5	30.00	150.00		PH150F110-5	PH150FXX-5	150	136	111
5	60.00	300.00		PH300F110-5	PH300FXX-5	236	215	175
12	6.30	75.00		PH75F110-12	PH75FXX-12	109	99	81
12	8.40	100.00	PH100F24-12			150	136	111
12	12.50	150.00		PH150F110-12	PH150FXX-12	150	136	111
12	25.00	300.00		PH300F110-12	PH300FXX-12	236	215	175
15	5.00	75.00		PH75F110-15	PH75FXX-15	109	99	81
15	6.70	100.00	PH100F24-15			150	136	111
15	10.00	150.00		PH150F110-15	PH150FXX-15	150	136	111
15	20.00	300.00		PH300F110-15	PH300FXX-15	236	215	175
24	3.20	75.00		PH75F110-24	PH75FXX-24	109	99	81
24	4.20	100.00	PH100F24-24			150	136	111
24	6.30	150.00		PH150F110-24	PH150FXX-24	150	136	111
24	12.60	300.00		PH300F110-24	PH300FXX-24	236	215	175
28	2.70	50.00		PH75F110-28	PH75FXX-28	109	99	81
28	3.60	100.00	PH100F24-28			150	136	111
28	5.40	150.00		PH150F110-28	PH150FXX-28	150	136	111
28	10.80	300.00		PH300F110-28	PH300FXX-28	236	215	175

Note: For complete electrical specifications, see page 13.

Simple Function Modules

The PH Series Simple Function modules are the highest density converters on the market today, achieving from 62W/in³. They feature 5 million hours MTBF and are designed for non-redundant applications–yet they can operate in a brute force parallel mode. The high density and low cost of the PH Series Simple Function modules makes distributed power viable in virtually any application. Additional features include remote on/off and a ±10% output adjustment.

SELECTOR GUIDE: PH50SXX-5 — **NOMINAL INPUT VOLTAGE: 48VDC, 280VDC**

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OUTPUT POWER (W)	MODEL 24V INPUT	MODEL 110V INPUT	MODEL 48/280V INPUT	UNIT PRICE PER DELIVERED QUANTITY 1	10	100
3.3	50.00	181.50			PH300SXX-3	$189	$172	$140
3.3	100.00	363.00			PH600S280-3	295	269	219
5	10.00	50.00	PH50S24-5	PH50S110-5	PH50SXX-5	79	73	59
5	15.00	75.00		PH75S110-5	PH75SXX-5	87	79	65
5	20.00	100.00			PH100SXX-5	106	96	79
5	30.00	150.00		PH150S110-5	PH150SXX-5	121	110	89
5	50.00	275.00			PH300SXX-5	189	172	140
5	100.00	550.00			PH600S280-5	295	269	219
12	4.20	50.00	PH50S24-12	PH50S110-12	PH50SXX-12	79	73	59
12	6.30	75.00		PH75S110-12	PH75SXX-12	87	79	65
12	8.40	100.00			PH100SXX-12	106	96	79
12	12.50	150.00		PH150S110-12	PH150SXX-12	121	110	89
12	25.00	300.00			PH300SXX-12	189	172	140
12	50.00	600.00			PH600S280-12	295	269	219
15	3.40	50.00	PH50S24-15	PH50S110-15	PH50SXX-15	79	73	59
15	5.00	75.00		PH75S110-15	PH75SXX-15	87	79	65
15	6.70	100.00			PH100SXX-15	106	96	79
15	10.00	150.00		PH150S110-15	PH150SXX-15	121	110	89
15	20.00	300.00			PH300SXX-15	189	172	140
15	40.00	600.00			PH600S280-15	295	269	219
24	2.10	50.00	PH50S24-24	PH50S110-24	PH50SXX-24	79	73	59
24	3.20	75.00		PH75S110-24	PH75SXX-24	87	79	65
24	4.20	100.00			PH100SXX-24	106	96	79
24	6.30	150.00		PH150S110-24	PH150SXX-24	121	110	89
24	12.50	300.00			PH300SXX-24	189	172	140
24	25.00	600.00			PH600S280-24	295	269	219
28	1.80	50.00	PH50S24-28	PH50S110-28	PH50SXX-28	79	73	59
28	2.70	75.00		PH75S110-28	PH75SXX-28	87	79	65
28	3.60	100.00			PH100SXX-28	106	96	79
28	5.40	150.00		PH150S110-28	PH150SXX-28	121	110	89
28	10.71	300.00			PH300SXX-28	189	172	140
28	21.43	600.00			PH600S280-28	295	269	219
48	6.25	300.00			PH300SXX-48	189	172	140
48	12.50	600.00			PH600S280-48	295	269	219

Note: For complete electrical specifications, see page 13.

RM Series 12W-100W DC-DC Converters

90% minimum efficiency characterizes the unique performance of the new RM Series. And forced air (no heatsink) is the only requirement to achieve maximum output power. This allows system designers to take advantage of the slim 8mm profile of the converter and maximize power density. The result is a power architecture which allows twice the power of traditional converters. The RM Series is ideal for ATM exchanges, LAN's, multi-media systems and other applications where high efficiency and low profile are required.

AT AMBIENT TEMPERATURE OF 85°C				UNIT PRICE PER DELIVERED QUANTITY			
OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OUTPUT POWER (W)	DIMENSIONS (INCHES)	1	10	100	MODEL
2	6.0	12.0	2.36 x 0.31 x 2.56	$135	$116	$90	RM30-48-2
2	6.0	12.0	2.36 x 0.31 x 2.56	149	128	116	RM30-48-2/TEL
2	10.0	20.0	2.36 x 0.31 x 3.86	175	145	108	RM50-48-2
2	10.0	20.0	2.36 x 0.31 x 3.86	193	160	143	RM50-48-2/TEL
2	20.0	40.0	2.36 x 0.31 x 4.57	200	185	150	RM100-48-2
2	20.0	40.0	2.36 x 0.31 x 4.57	220	204	183	RM100-48-2/TEL
3.3	6.0	19.6	2.36 x 0.31 x 2.56	$135	$116	$90	RM30-48-3.3
3.3	6.0	19.6	2.36 x 0.31 x 2.56	149	128	116	RM30-48-3.3/TEL
3.3	10.0	33.0	2.36 x 0.31 x 3.86	175	145	108	RM50-48-3.3
3.3	10.0	33.0	2.36 x 0.31 x 3.86	193	160	143	RM50-48-3.3/TEL
3.3	20.0	66.0	2.36 x 0.31 x 4.57	200	185	150	RM100-48-3.3
3.3	20.0	66.0	2.36 x 0.31 x 4.57	220	204	183	RM100-48-3.3/TEL
5	6.0	30.0	2.36 x 0.31 x 2.56	$135	$116	$90	RM30-48-5
5	6.0	30.0	2.36 x 0.31 x 2.56	149	128	116	RM30-48-5/TEL
5	10.0	50.0	2.36 x 0.31 x 3.86	175	145	130	RM50-48-5
5	10.0	50.0	2.36 x 0.31 x 3.86	193	160	143	RM50-48-5/TEL
5	20.0	100.0	2.36 x 0.31 x 4.57	200	185	166	RM100-48-5
5	20.0	100.0	2.36 x 0.31 x 4.57	220	204	183	RM100-48-5/TEL

Note: All models in the RM Series have an input voltage of 48 VDC. ("TEL" versions operate from 36 - 75 VDC).
For complete electrical specifications, see page 14.

PM Series 5W-30W DC-DC Converters

Lambda's low cost PM Series DC-DC converters conform to industry-standard pin-outs and a lower profile of 8.5mm, allowing direct replacement in existing systems. With UL, CSA, VDE, BABT, Bellcore and ETSI approvals, they're ideal for telecommunications applications. There are 96 single, dual, and triple output models with 12V, 24V, and 48V inputs, all incorporating EMI filtering. The PM Series is available from stock with four week production delivery.

SELECTOR GUIDE: PM10-XXS03 — **NOMINAL INPUT VOLTAGE 12VDC, 24VDC, 48VDC**

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OUTPUT POWER (W)	MODEL 12V, 24V OR 48V INPUT	UNIT PRICE PER DELIVERED QUANTITY 1	10	100
Single Output						
3.3	1.27	4.20	PM05-XXS03	$-	$47	$46
3.3	2.55	8.40	PM10-XXS03	51	48	47
3.3	3.75	12.40	PM15-XXS03	-	79	78
3.3	5.00	16.50	PM20-XXS03	84	83	82
3.3	7.50	24.75	PM30-XXS03	99	97	88
5.0	1.00	5.00	PM05-XXS05	-	47	46
5.0	2.00	10.00	PM10-XXS05	51	48	47
5.0	3.00	15.00	PM15-XXS05	-	79	78
5.0	4.00	20.00	PM20-XXS05	84	83	82
5.0	6.00	30.00	PM30-XXS05	99	97	88
12.0	0.42	5.00	PM05-XXS12	-	47	46
12.0	0.83	10.00	PM10-XXS12	51	48	47
12.0	1.25	15.00	PM15-XXS12	-	79	78
12.0	1.67	20.00	PM20-XXS12	84	83	82
12.0	2.50	30.00	PM30-XXS12	99	97	88
15.0	0.33	5.00	PM05-XXS15	-	47	46
15.0	0.67	10.00	PM10-XXS15	51	48	47
15.0	1.00	15.00	PM15-XXS15	-	79	78
15.0	1.33	20.00	PM20-XXS15	84	83	82
15.0	2.00	30.00	PM30-XXS15	99	97	88
Dual Output						
±12	0.21	5.00	PM05-XXD12	-	48	47
±12	0.42	10.00	PM10-XXD12	52	49	48
±12	0.63	15.00	PM15-XXD12	-	81	80
±12	0.83	20.00	PM20-XXD12	87	86	85
±12	1.25	30.00	PM30-XXD12	100	98	95
±15	0.167	5.00	PM05-XXD15	-	48	47
±15	0.33	10.00	PM10-XXD15	52	49	48
±15	0.50	15.00	PM15-XXD15	-	81	80
±15	0.67	20.00	PM20-XXD15	87	86	85
±15	1.00	30.00	PM30-XXD15	100	98	95
Triple Output						
3.3±12	7±1	30.00	PM30-XXT03-12	105	104	101
5±12	5±1	30.00	PM30-XXT05-12	105	104	101

Note: For complete electrical specifications, see page 14.

PP Series 1.5W-6W DC-DC Converters

For low power (1.5W to 6W) applications, Lambda's low profile, low cost PP Series is an ideal solution. They have industry-standard pin-outs, a height of only 8mm and are available in single and dual outputs with 5, 12/15, 24 and 48 volt inputs.

SELECTOR GUIDE: PP1R5XX5 — **NOMINAL INPUT VOLTAGE** 5VDC, 12VDC, 24VDC 48VDC

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OUTPUT POWER (W)	MODEL 5V INPUT	MODEL 12V, 24V OR 48V INPUT	UNIT PRICE PER DELIVERED QUANTITY 1	10	100
Single Output							
5	0.30	1.50	PP1R5-5-5		$24.00	$22.00	$19.00
5	0.30	1.50		PP1R5-XX-5	24.00	22.00	19.00
5	0.60	3.00	PP3-5-5		29.50	27.00	23.00
5	0.60	3.00		PP3-XX-5	29.50	27.00	23.00
5	1.20	6.00	PP6-5-5		42.50	39.00	32.50
5	1.20	6.00		PP6-XX-5	42.50	39.00	32.50
5	2.00	10.00	PP10-5-5		42.50	39.00	32.50
12	0.12	1.44	PP1R5-5-12		24.00	22.00	19.00
12	0.12	1.50		PP1R5-XX-12	24.00	22.00	19.00
12	0.25	3.00	PP3-5-12		29.50	27.00	23.00
12	0.25	3.00		PP3-XX-12	29.50	27.00	23.00
12	0.50	6.00	PP6-5-12		42.50	39.00	32.50
12	0.50	6.00		PP6-XX-12	42.50	39.00	32.50
12	0.83	10.00	PP10-5-12		42.50	39.00	32.50
15	0.10	1.50	PP1R5-5-15		24.00	22.00	19.00
15	0.10	1.50		PP1R5-XX-15	24.00	22.00	19.00
15	0.20	3.00	PP3-5-15		29.50	27.00	23.00
15	0.20	3.00		PP3-XX-15	29.50	27.00	23.00
15	0.40	6.00	PP6-5-15		42.50	39.00	32.50
15	0.40	6.00		PP6-XX-15	42.50	39.00	32.50
15	0.66	10.00	PP10-5-15		42.50	39.00	32.50
Dual Output							
±12	0.06	1.44	PPD1R5-5-1212		25.50	23.50	20.50
±12	0.06	1.44		PPD1R5-XX-1212	25.50	23.50	20.50
±12	0.12	2.88	PPD3-5-1212		33.00	30.00	24.00
±12	0.12	2.88		PPD3-XX-1212	33.00	30.00	24.00
±12	0.25	6.00	PPD6-5-1212		46.00	42.50	36.00
±12	0.25	6.00		PPD6-XX-1212	46.00	42.50	36.00
±12	0.42	10.00	PPD10-5-1212		46.00	42.50	36.00
±15	0.05	1.50	PPD1R5-5-1515		25.50	23.50	20.50
±15	0.05	1.50		PPD1R5-XX-1515	25.50	23.50	20.50
±15	0.10	3.00	PPD3-5-1515		33.00	30.00	24.00
±15	0.10	3.00		PPD3-XX-1515	33.00	30.00	24.00
±15	0.20	6.00	PPD6-5-1515		46.00	42.50	36.00
±15	0.20	6.00		PPD6-XX-1515	46.00	42.50	36.00
±15	0.33	10.00	PPD10-5-1515		46.00	42.50	36.00

Note: For complete electrical specifications, see page 14.

PF, PT, PD, PR, PN, PBP Series Component Front Ends, PFC, Rectifier, Filters and Transformer Modules

Lambda's PD Series Component Front Ends combine the functions of the PFC, DC-DC Transformer and EMI Filter along with all the discrete components required for a complete off-line or 48VDC solution. Or if you want to use individual components, Lambda has a complete selection of Transformers, Rectifiers, EMI Filters and PFC Modules.

Component Front Ends, PFC and DC-DC Transformer Modules

MODEL	OUTPUT VOLTAGE (VDC)	OUTPUT POWER (W)	INPUT VOLTAGE	DIMENSIONS (INCHES)	UNIT PRICE PER DELIVERED QUANTITY 1	10	100
PF1000A-360	360	1008	85-265VAC	3.38 x 5.75 x 0.5	$203	$183	$149
	360	1512	170-265VAC				
PF500A-360	360	504	85-265VAC	3.38 x 3.27 x 0.5	144	131	107
	360	756	170-265VAC				
PT500-48	48	500	360VDC	3.38 x 5.75 x 0.5	225	203	168
PT500-66	66	500	360VDC	3.38 x 5.75 x 0.5	225	203	168
PD800-230-48	48	500	88-265VAC	3.74 x 8.66 x 1.08	695	630	567
	48	800	170-265VAC				

Notes: 1. Lambda's PD Series Component Front Ends combine the functions of the PFC, DC-DC Transformer and EMI Filter, with all the discrete components required for a complete 48VAC solution. They provide 88-265VAC input with 90% efficiency, and feature full agency approvals including the CE mark (Low Voltage Directive). All models meet Class B EMI, and IEC-1000 (Input Transients).

2. The PF Series, Power Factor Correction modules are 90% efficient. Available in 500W and 1000W models, they are IEC/EN555-2 compliant, ensuring worldwide operation. All models have integral diagnostics, auxiliary supply and control circuitry with densities to 90W/in³.

3. The PT500 Transformer provides over 90W/in³ with 93% efficiency.

Rectifier Modules

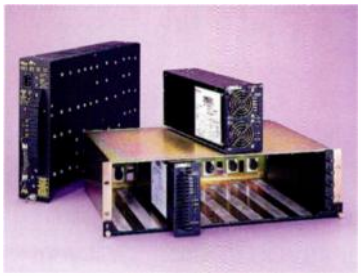
MODEL	OUTPUT VOLTAGE	OUTPUT POWER (W) 85-265VAC	170-265VAC	DIMENSIONS (INCHES)	UNIT PRICE PER DELIVERED QUANTITY 1	10	100
PR500-280	280VDC	500	750	3.38 x 0.5 x 3.27	$53	$47	$39

Note 4. Now the PR500 Rectifier is designed for off-line switching applications, providing 85-132 and 170-265VAC input with integral in-rush limiting, auxiliary supply, AC fail and in-rush control circuitry.

EMI Filters

MODEL	DIMENSIONS (INCHES)	RATING A	UNIT PRICE PER DELIVERED QUANTITY 1	10	100
Board Mount					
PPBP3201	1.26 X 0.70 X 0.87	1	$12	$11	$10
PBP3202	1.26 X 0.70 X 0.87	2	14	13	12
PBP3203	1.26 X 0.70 X 0.87	3	17	15	14
PBP3204	1.26 X 0.70 X 0.87	4	18	16	15
PN3207	3.38 X 2.44 X 0.50	7	40	35	29
PN3215	3.38 X 3.27 X 0.50	15	53	47	39
Chassis Mount (EMI Class B Compliant)					
PN1207F	5.20 X 2.05 X 1.38	7	107	102	89
PN1210F	5.64 X 2.64 X 1.38	10	144	38	120
PN1215F	6.73 X 3.75 X 1.38	15	192	84	160

Note 5. Lambda's high attenuation, low leakage, low profile PN/PBP EMI Filters are available from 1A to 15A for 110-240 VAC operation.



Lambda's FE Series, FE Series Racking System, R Series and PFHC Series Rectifier Modules are the ideal power foundation for distributed power architectures. These low cost, highly reliable front end solutions provide up to 6kW of scaleable power for telecommunication systems that require a high degree of modularity.

OUTPUT POWER (W)	MAX OUTPUT CURRENT (A)	OUTPUT VOLTAGE (VDC)	UNIT PRICE PER DELIVERED QUANTITY 1	10	100	MODEL
24VDC Output						
500	21.0	20.0-29.0	–	$630	$567	FE0500-24NA
500	21.0	20.0-29.0	$715	640	576	FE0500-24RA[1]
1000	42.0	20.0-29.0	–	896	806	FE1000-24NA
1000	42.0	20.0-29.0	1,015	911	820	FE1000-24RA[1]
1500	63.0	20.0-29.0	–	1,148	1,033	FE1500-24NA
1500	63.0	20.0-29.0	1,305	1,173	1,056	FE1500-24RA[1]
1500	63.0	24	925	875	–	R160-27-0-01[2,3]
2000	84.0	20.0-29.0	–	1,350	1,215	FE2000-24NA
2000	84.0	20.0-29.0	1,550	1,395	1,256	FE2000-24RA[1]
48VDC Output						
500	11.0	40.0-58.0	–	630	567	FE0500-48NA
500	11.0	40.0-58.0	715	640	576	FE0500-48RA[1]
1000	21.0	40.0-58.0	–	896	806	FE1000-48NA
1000	21.0	40.0-58.0	1,015	911	820	FE1000-48RA[1]
1500	32.0	40.0-58.0	–	1,148	1,033	FE1500-48NA
1500	32.0	40.0-58.0	1,305	1,173	1,056	FE1500-48RA[1]
1500	32.0	48	925	875	–	R160-55-0-01[2,3]
1500	32.0	48	1,000	950	–	R80-55-00-01[2,3]
2000	42.0	40.0-58.0	–	1,350	1,215	FE2000-48NA
2000	42.0	40.0-58.0	1,500	1,395	1,256	FE2000-48RA[1]
360VDC Output						
2600	7.2	360	836	722	–	PFHC-2600[3]

Notes: 1. Indicates a redundant, or-ing diode is internal to the module.
2. Indicates a convection-cooled rectifier module.
3. The R80 Rectifier measures 15.16 x 3.15 x 11 inches. The R160 Rectifier measures 15.16 x 6.3 x 11 inches. The PFHC-2600 measures 11 x 3.5 x 4.75 inches.

MODEL	FE0500	FE1000	FE1500/2000	MOUNTING[5]	UNIT PRICE PER DELIVERED QTY 1-9
Racking Systems					
FE4K-N-E	7			EIA	$1,195
FE4K-X-E	8			EIA	899
FE4K-N-N	7			NEBS	1,295
FE4K-X-N	8			NEBS	999
FE5K-N-E		4		EIA	1,195
FE5K-X-E		5		EIA	799
FE5K-N-N		4		NEBS	1,295
FE5K-X-N		5		NEBS	899
FE6K-N-E			3[4]	EIA	1,195
FE6K-X-E			3[4]	EIA	799
FE6K-N-N			3[4]	NEBS	1,295
FE6K-X-N			3[4]	NEBS	899

Notes: 4. FE4K and FE5K-N Racking Systems are compliant to FCC Class B EMI emissions standards for conducted emissions. All FE6K Racking Systems are compliant to Class B standards.
5. EIA mounting flanges are located on the front of the rack. NEBS mounting flanges are center-mounted per Bellcore NEBS requirements.

AC Input
line .....85-265VAC, 47-63Hz for FE0500, FE1000, FE1500.
170-265VAC, 47-63Hz for FE2000.

Efficiency
82% typical for 50-100% minimum without isolation diodes.

Power Factor/Harmonic Correction
0.95 minimum at full load. Compliant to IEC-1000-3-2.

Hold-up Time
Output will be maintained above lower limit of output voltage range for 16ms upon loss/disconnect of AC input.

Surge Immunity
IEC-1000-4-5 Level 3 for FE0500. Level 4 for FE1000, FE1500, FE2000.

Regulated Voltage
line and load
regulation .....1.0% from no load to full load. 85VAC-265VAC max.
ripple and noise.....250mV pk-pk max on 24V models. 500mV pk-pk on 48V model. EIAJ RC-9002A procedure (20Mhz bandwidth limit).

Overcurrent Protection
The power module limits the output current to less than 110% of the full power rating. The current limit characteristic has constant power down to V_o min. The converter withstands an indefinite short circuit without damage and is self-recovering.

Output Current Share
±10% of max unit load from 10% to 100% load with single or multiple A/B rail inputs. Current sharing is accomplished via a single wire connection. The power module operates in parallel without any derating of its maximum full load output current, with and without Or-ing diode option. The current sharing bus is not a single point failure mechanism. Current sharing is not required for parallel operation.

Temperature Drift
±2% over the entire temperature range and life.

Overvoltage Protection
Adjustable non-latching unit shutdown.

Overtemperature Protection
Internal circuitry prevents damage by turning off the converter in the event of reduced airflow or excessive ambient operating temperature. The output spontaneously returns when the overtemperature condition is cleared.

Hot Maintenance
Unit is capable of being inserted and extracted with all operational voltages present, with or without Or-ing diode option. Overshoot recovery and inrush current is the same as for turn-on.

Remote On/Off Signal
Standard. Contact closure to turn on. Contacts open to turn off.

AC Fail Signal
Open collector type signal under fault condition, 20V breakdown. During nominal operation, the AC Fail signal conducts up to 5mA maximum. There is a minimum of 16mSec hold-up time in the event of an AC failure or AC disconnect after the AC fail is activated.

Output/Inverter Good Signal
Open collector type signal under fault condition, 20V breakdown. During nominal operation, the Output/Inverter Good Signal conducts up to 5mA maximum. This signal will not alarm when the unit is in a parallel configuration with other units, batteries or at no load.

Auxiliary Bias Supply
12VDC at 50mA.

Front Panel Indicators
An AC present LED indicates that input power is applied to the unit. An output/inverter good LED indicates that DC output voltage is present and the inverter is operational. Operation is the same as output/inverter good signal. An overtemperature shutdown LED indicates that thermal shutdown has occurred. An output current meter LED ladder shows the approximate percentage of output current.

Operating Temperature Range
–40°C to +70°C ambient. From 55°C to +70°C, consult the factory for derating.

Storage Temperature Range
–40°C to +85°C.

Operating Humidity
0% to 95% (non-condensing).

Shock and Vibration
The FE Series is compliant with GR-63-CORE, Zone 4 Upper Level standards assembled in a NEBS-type FE Racking System.

Transportation
The FE Series is tested to MIL-STD-810E requirements.

Isolation Rating
Input/Chassis: 2.5k VAC
Input/Output: 3.0k VAC
Output/Chassis: 500VDC

Conducted Battery Noise
FE Series power modules comply with GR-1089-CORE and prETS300132-2 psophometric noise requirements.

Conducted EMI
FE0500 and FE1000 modules comply with FCC-CFR Part 15, Subpart J, Class A standards with 6dB of margin and with CISPR 22, Class A standards with 6dB of margin. When assembled into an FE-N standard racking system, the system is compliant with Class B standards.
FE1500 and FE2000 modules comply with FCC-CFR part 15, Subpart J, Class B standards with 6dB of margin and with CISPR 22, Class B standards with 6dB of margin.

Radiated Emissions
Class A specifications on modules and racks. FCC Part 15, Subpart J, EN55022.

Conducted Susceptibility (Output)
FE Series power modules comply with Bellcore GR-1089-CORE, 3A/meter and IEC-1000-4-6.

Radiated Susceptibility
All models comply with Bellcore GR-1089-CORE, 10V/meter and IEC-1000-4-3.

ESD
FE power modules comply with Bellcore GR-1089-CORE and IEC-1000-4-2.

Electrical Fast Transient
FE power modules comply with IEC-1000-4-4.

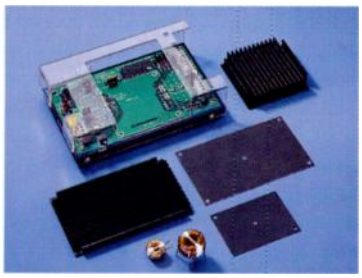
Lightning Surge
FE power modules comply with IEC-1000-4-5.

Physical Data

Model	Weight Lbs. Net	Weight Lbs. Ship.	Dimensions (inches)
FE0500	6.0	7.0	11.97 x 5 x 2
FE1000	7.0	8.0	11.97 x 5 x 3.3
FE1500/2000	9.0	10.0	11.97 x 5 x 5.5
FE4K	15.0	18.0	13.75 x 5.25 x 19
FE5K	15.0	18.0	13.75 x 5.25 x 19
FE6K	15.0	18.0	13.75 x 5.25 x 19

Safety Agency Approvals
The FE Series meets safety agency approvals per UL 1950, EN60950, CSA22.2-234. All models are CE marked (Low Voltage Directive).

Evaluation and Heatsink Kits, Sockets, Chokes and Thermal Pads



Lambda has a complete line of evaluation kits, sockets, chokes and thermal pads designed to facilitate complete system integration.

PKT Series Evaluation Kits

KIT NUMBER	APPLICATION MODE	UNIT PRICE PER DELIVERED QUANTITY (1-24)
PKTPFC	PF500 with PN3207 or PF1000 with PN3215	$245
PKTPR500	PR500 with PN3215	245
PKT300F	PH300F	195
PKT150F	PH150F	195
PKT150S	PH150S	195
PKT75F/100S	PH75F/PH100S	195
PKT50S/75S	PH50S/PH75S	195

NOTE: Each Kit contains a socketed printed circuit board (including test points), heatsink kits, thermal pads, mounting hardware, line cords, an instruction manual and all the discrete components required to evaluate a power module (power module not included).

PAH Series Heatsink Kits

KIT NUMBER	APPLICATION MODE	°C/W @600LF/M	FIN HEIGHT (mm)	FIN DIRECTION	UNIT PRICE PER DELIVERED QUANTITY (1)
PAH41L12	PH50S, PH75S	1.25	12	Length	$20
PAH62L12	PH75F, PH100S, PN3207	1.20	12	Length	20
PAH72L12	PH150S	0.70	12	Length	22
PAH83L12	PH150F, PF500, PN3215, PR500	0.70	12	Length	22
PAH83L12A	PH150F, PF500, PN3215, PR500	0.57	12	Length	35
PAH146L12	PH300F, PF1000, PT500	0.65	12	Length	27
PAH146L12A	PH300F, PF1000, PT500	0.40	12	Length	35
PAH146W12	PH300F, PF1000, PT500	0.65	12	Width	27
PAH41L23	PH50S, PH75S	0.80	23	Length	22
PAH62L23	PH75F, PH100S, PN3207	0.60	23	Length	22
PAH72L23	PH150S	0.40	23	Length	27
PAH83L23	PH150F, PF500, PN3215, PR500	0.45	23	Length	27
PAH146L23	PH300F, PF1000, PT500	0.30	23	Length	32

NOTE: Heatsink Kits include a heatsink, thermal pad, mounting hardware and instruction manual (these kits are already included in the evaluation kits). Call a Lambda Application Engineer for thermal design and heatsink recommendations.

PATP Series Thermal Pads

KIT NUMBER	APPLICABLE MODULE	UNIT PRICE PER DELIVERED QUANTITY (1-24) (PACKAGE OF 10)
PATP41	PH50S, PH75S	$22
PATP62	PH75F, PH100S, PN3207	26
PATP72	PH150S	27
PATP83	PH150F, PF500, PN3215	27
PATP146	PH300F, PF1000, PT500	35

NOTE: The PATP Series is electrically and thermally conductive, typically yielding less than 1°C temperature rise heatsink to baseplate at full power operation.

PAL Series Chokes

KIT NUMBER	VALUE	APPLICABLE MODULE	UNIT PRICE PER DELIVERED QUANTITY (1-24) (PACKAGE OF 5)
PAL03-1	3A 100mH	PH50/75X48-XX	$33
PAL05-1	5A 100 mH	PH100/150X48-XX	28
PAL10-1	10A 100mH	PH300F48-XX	33
PAL02-2	2A 200mH	PHXXXX280-XX	28

PAS Series Sockets

KIT NUMBER	DESCRIPTION	PIN SIZE (mm)	UNIT PRICE PER DELIVERED QUANTITY (1-24) (PACKAGE OF 10)
PASHC	High Current Socket (Input/Output)	2.0	$29
PASLC	Low Current Socket (Signal)	0.6	22

ADC Input

200 - 400VDC for 280V PH Series Modules.
88 - 185VDC for 110V PH Series Modules.
36 - 76VDC for 48V PH Series Modules.
18 - 36VDC for 24V PH Series Modules.

Efficiency

	2V	3.3V	5V	12V	15V	24V	28V
PH50S	–	–	80%	82%	83%	84%	84%
PH75S	–	–	81%	83%	84%	85%	85%
PH100S	–	–	81%	83%	84%	88%	88%
PH150S	–	–	82%	85%	85%	88%	88%
PH75F	67%	70%	81%	83%	84%	85%	85%
PH150F	68%	73%	82%	86%	87%	89%	90%
PH300F	68%	73%	82%	85%	86%	89%	90%
PH300S	–	80%	86%	88%	88%	88%	88%
PH600S	–	80%	86%	88%	88%	88%	88%

Regulated Voltage

line regulation .....0.4% or 20mV (whichever is greater) over entire input range with constant load.
load regulation .....0.8% or 40mV (whichever is greater) from no load to full load with constant input line.
temperature coefficient ...0.02%/°C.

Ripple and Noise

Output V_{out}	2V	5V	12V	15V	24V	28V
mVpk-pk ripple	100	100	150	150	240	280

Remote Sensing

Sensing connections are provided to the regulation caused by resistive drops in the output trace/leads. (Not available on PH50S, PH75S modules.)

Overvoltage Protection

150-180% on 2V and 3V models.
125-145% on 5V through 28V models.
Inverter shutdown. Input power must be recycled to restore operation.

Overtemperature Protection

Inverter shutdown protects the converters against excessive temperatures. Input power must be recycled to restore operation.

Overload Protection

Overcurrent protection will protect the module and load from overload with automatic recovery.

Output Voltage Adjustment

The output voltage on all PH Series modules can be programmed by an external potentiometer or voltage source (±10% on Simple Function Modules, +20 -60% on Full Function Modules). Adjustment below the -60% range is possible with the appropriate preload. Consult the P Series Application Notes for further details.

Overcurrent Protection

105% - 140% with automatic recovery.

Remote On/Off Signal

Short terminal CNT to SG to turn on.
Open circuit to turn off.

Parallel Operation

Full function PH Series modules have a single star point connection of PC terminal which enables modules to current share. Current guaranteed modules within ±5% when connected per the application notes (typically within 2%).

Series Operation

All modules can be operated in series. Refer to the PH Series Application Notes for detailed requirements.

Inverter Good Signal

Full function PH Series modules give an inverter good status at the IOG terminal when the module is healthy.

Auxiliary Supply

Full function PH Series modules have an auxiliary bias supply (8V at 10mA) which can be used to power interface circuits (i.e., optocouplers).

Operating Temperature Range

-20°C to +85°C base plate. -20°C to +100°C on PH300S, PH600S. Consult the factory for -40°C startup on all models.

Storage Temperature Range

-40°C to +85°C. -40°C to +100°C on PH300S, PH600S.

Cooling

PH Series modules are conduction cooled. Contact the factory for cooling recommendations.

Isolation Rating

3000VAC Input to Output.
2500VAC Input to Baseplate.
100MΩ at 500VDC 70% RH Output to Baseplate.

Physical Data

Package Model	Weight (grams)	Dimensions (inches)
PH50S, PH75S	100	3.38 x 1.61 x 0.5
PH100S, PH75F	150	3.38 x 2.44 x 0.5
PH150S	150	3.38 x 2.83 x 0.5
PH150F, PH100F	180	3.38 x 3.27 x 0.5
PH300F	250	3.38 x 5.75 x 0.5
PH300S	200	3.38 x 3.27 x 0.5
PH600S	300	3.38 x 5.75 x 0.5

Safety Agency Approvals

UL1950, CSA234, and EN60950 approved. BABT is under evaluation.

Guarantee

Two year guarantee applies to operation within published specifications and recommended application data.

DC Input

PP Series	5V Input 4.5-7.2VDC
PP and PM Series	12V Input 9-18VDC
PP and PM Series	24V Input 18-36VDC
PP Series	48V Input 32-63VDC
PM Series	48V Input 36-75VDC
RM Series	48V Input 36-60VDC
RM "TEL" Series	48V Input 36-75VDC

Efficiency

	Output Voltage			
	2V	3.3V	5V	12V, 15V
RM Series	80%	86%	90%	–
PM Series	–	73%	78%	79%
PP Series	–	–	65%	70%

Regulated Voltage

line regulation . . . . 20mV on the RM Series. 0.2% for main and dual outputs of the PM Series, 3% for auxiliary outputs of triple output PM Series modules over full input line range with constant load. 0.4% on the PP Series.

load regulation . . . 40mV on the RM Series. 1% for main outputs of the PM Series from 10% load to 100% load with constant input line .8% on auxiliary outputs of triple output PM Series models from 25% to 100% load, and with greater than 5W main output load. 0.6% on the PP Series.

ripple and noise. . . 100mV pk-pk on the RM Series. 75mV pk-pk on the 5V and 3V outputs of the PM Series. 120mV pk-pk for 5V outputs of the PP Series and 12V outputs of the PM Series.150mV pk-pk on 12 and 15V outputs of the PP Series.

Temperature Coefficient . . . . . 0.03% °C.

Setpoint Accuracy

±1% on the main outputs of PM Series modules. 1.5% for auxiliary outputs of PM Series. ±5% on PP Series.

Output Adjustment

The RM Series, PM15, PM20 and PM30 outputs can be adjusted ±10% using resistive or voltage programming.

Overload Protection

The RM Series has constant current limiting with shutdown after 0.5-1.5 seconds.
PM Series models have current limiting to protect the load and converter from overload.
Avoid overloading auxiliary outputs on the PP Series for greater than 30 seconds.

Overvoltage Protection

RM modules provide latching overvoltage shutdown.
All PM Series models are provided with overvoltage clamps:

Vo	Clamp Level
3.3V	4.0-4.7V
5V	6.2-6.5V
12V	13-14V
±12V	28-30V

Remote On/Off

The RM Series, PM15, PM20 and PM30 models include remote on/off via a TTL pin.

Alarm and Reset

RM modules are designed to give a TTL alarm status when the module output is below a specified value. This signal and the error status can be reset by applying a TTL reset signal.

Operating Temperature Range

-25°C to +85°C (+100°C Base plate) on the RM Series. Consult the factory for -40°C start-up.
-25°C to 105°C on the PM Series with derating (consult derating charts. Full load up to +70°C with forced air on all models. Consult the factory for -40°C start-up.
-20°C to +71°C on the PP Series. Derate linearly above +50°C from full load to 20% at +71°C.

Storage Temperature Range

-40°C to +105°C on the RM Series and the PM Series.
-40°C to +85°C on the PP Series.

Isolation Rating

RM Series: 1500VDC input to output; 50 VAC input to case; 500VDC output to case. (2500VDC input to output for the "TEL" versions.)

PM Series: 900VAC, 1500VDC, input to output on 48V input models; 500VAC, 700VDC input to output on 12/24 input models; 10MΩ output to chassis at 25°C, 75% RH.

PP Series: 500VAC (<5mA) input to chassis and input to output; >100MΩ output to chassis at 500VDC, 25°C and 70% Humidity.

Physical Data

Package Model	Weight (grams)	Dimensions (inches)
RM100,/TEL	170	2.36 x 0.31 x 4.57
RM50,/TEL	100	2.36 x 0.31 x 3.86
RM30,/TEL	62	2.35 x 0.31 x 2.56
PM05/10	28	1.00 x 0.33 x 2.00
PM15/20	43	1.60 x 0.33 x 2.00
PM30	71	2.50 x 0.33 x 3.00
PP1R5	15	1.29 x 0.31 x 0.81
PPD1R5	15	1.29 x 0.31 x 0.81
PP3	25	1.84 x 0.31 x 1.09
PPD3	25	1.84 x 0.31 x 1.09
PP6	30	1.84 x 0.31 x 1.65
PPD6	30	1.84 x 0.31 x 1.65

Agency Approvals

The PM Series Meets:

EMI: EN55022 Level B, FCC Part 15 Level B, Bellcore TA-NWT-001089 (an external capacitor and chip inductor may be required for some models. Consult the factory for application notes).

Input Transients: IEEE-C62.41-1980 (0-.5ms 100kHz ring-wave), ETSI Standard ETS300-132 (100V 10Joule pulse).

Inrush: ETSI Standard ETS300-132 (<50A peak), Bellcore.

Safety: UL1950, CSA234, EN60950. Consult the factory for BABT. CE Mark (Low Voltage Directive).

The RM "TEL" Series meets UL1950, CSA234 and EN60950.

Contact the factory for information on the RM Series and PP Series.

Guarantee

The RM Series is guaranteed for 3 years for operation within published specifications. The PM and PP Series are guaranteed for 2 years for operation within published specifications.

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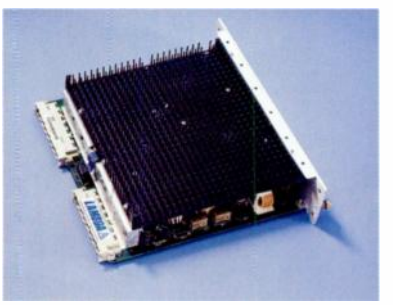

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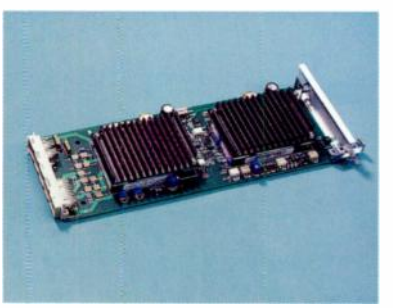

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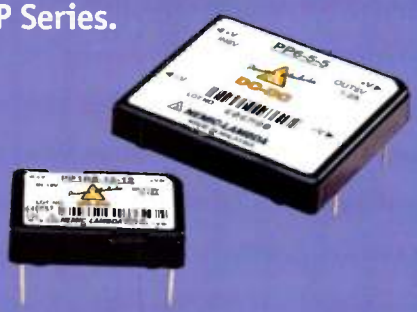

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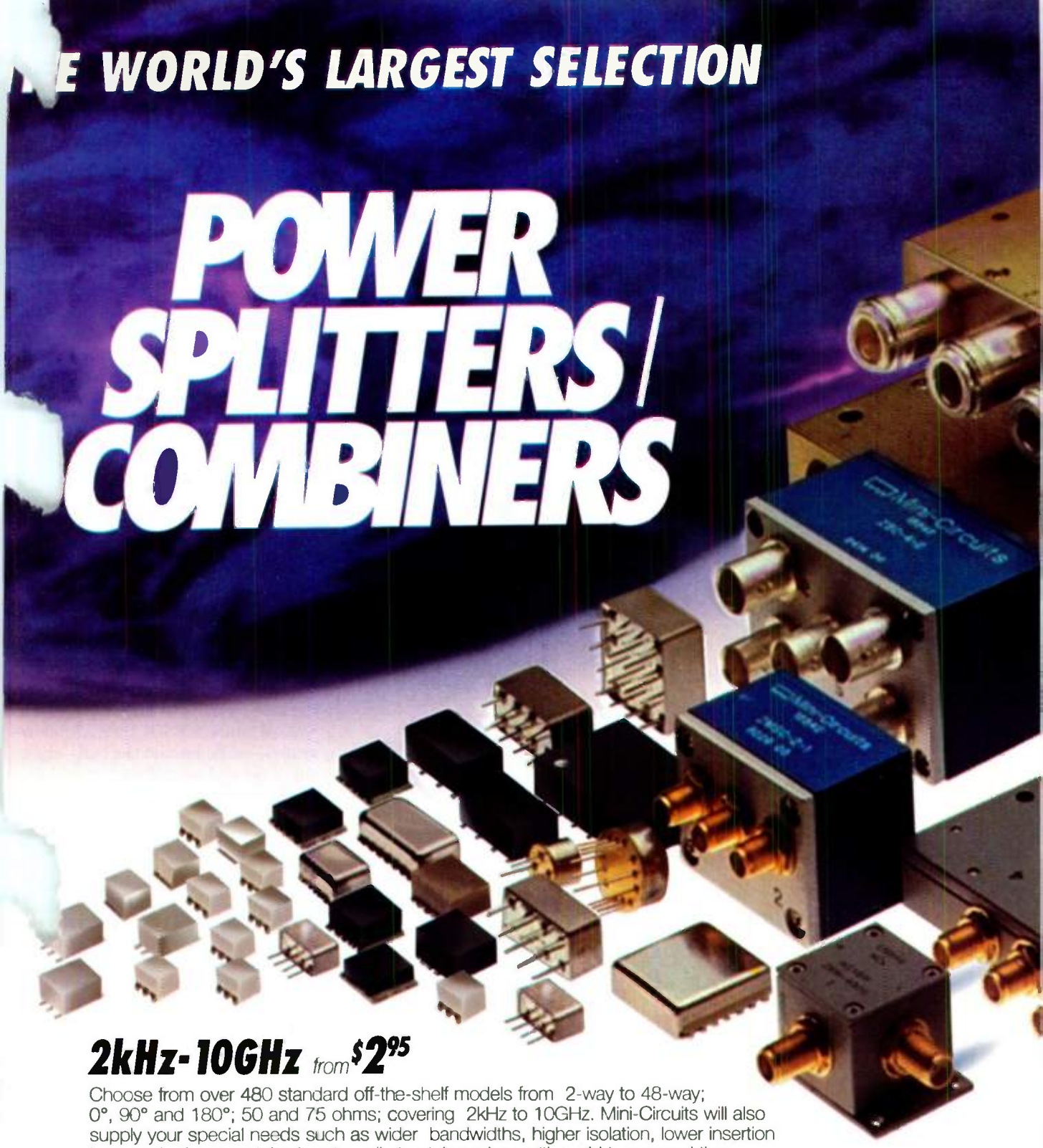

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PEASE PORRIDGE

Mr. Amelio, who had moved over to Apple. I got a prompt, brief reply. Gil was a good sport, and he agreed that if "team enthusiasm" was being proposed as an alternative for thinking, that was probably a mistake. OK, we got an agreement on that.

Let me finish with a second fable—a second *team* parable:

Did you ever hear the story about the second-string quarterback (who also was the team's punter), who was put in the game because the first-string quarterback got hurt? The coach, a very strict, tough guy, a martinet, told the kid, "Run the first two plays and then punt." And then the coach turned away, to find out about the injury to his star quarterback.

Well, the kid handed off to the halfback, and he gained about 30 yards. Then he threw a little pass, and the receiver gained 20 yards more. Then the kid handed off to the fullback, who carried the ball down to the 2-yard line. And what did the young quarterback do next? He knew the coach wanted him to ABSOLUTELY follow orders—so he punted the ball—right out of the end zone.***

Hey, it's not every day you get two esaeP's Fables in one column. What's all this "Following Orders" St Anyhow??

All for now. / Comments invited!
RAP / Robert A. Pease / Engine

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**The Wisdom of Teams: Creating The High-Performance Organization*, J. Katzenbach and D. Smith, Harper-Business, 1993, ISBN 0-88730-676-4. About $13.

***Why Teams Don't Work: What Went Wrong & How To Make It Right*, H. Robbins and M. Finley, Peterson's/Pacesetter Books, 1994, ISBN 1-56079-497-6. About $22.

***If you are not knowledgeable about football, I'll explain that the was quite absurd, to punt the away when you are within a co yards of scoring a touchdown!

UPCOMING MEETINGS

APRIL

Sixth System Administration, Networking, & Security Conference, Apr. 21-26. Baltimore Inner Harbor, MD. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; http://www.usenix.org.

IEEE International Conference on Robotics and Automation, Apr. 21-27. Albuquerque Convention Center, Albuquerque, NM. Contact Jerry Stauffer, Intelligent Systems and Robotics Center, Program Office, MS0949, Sandia National Laboratories, Albuquerque, NM 87185-0949; (505) 845-8966; fax (505) 844-6161; e-mail: jdstauf@isrc.sandia.gov.

First Convergence Technology & IC Expo, Apr. 22-24. InfoMart, Dallas, TX. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668, ext. 243; fax (310) 641-5117.

15th IEEE VLSI Test Symposium, Apr. 27-30. Hyatt Regency Monterey, Monterey, CA. Contact Yervant Zorian, General Chair, Lucent Bell Laboratories, P.O. Box 900, Princeton, NJ 08542-0900; (609) 639-3176; fax (609) 639-3197; e-mail: zorian@lucent.com.

MAY

IEEE Vehicular Technology Conference (VTC), May 5-7. Hyatt Regency at Civic Plaza, Phoenix, AZ. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, Post Office. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

IEEE Custom Integrated Circuits Conference (CICC 97), May 5-8. Santa Clara, CA. Contact Melissa Widerkehr, Widerkehr & Assoc., Suite 270, 101 Lakeforest Blvd, Gaithersburg, MD 20877; (301) 527-0902; fax (301) 527-0994.

ELECTRO 97, May 6-8. World Trade Center, Boston, MA. Contact Kathy Lott-Smith, Hickory International, 595 Gilman St., Bridgeport, CT 06605; (203) 334-1397; fax (203) 334-1397.

Electronics Industries Forum of New England, May 6-8. World Trade & Exhibition Center, Boston, MA. Contact Linda Hanson, (914) 779-0696

IEEE Power Industry Computer Applications Conference (PICA), May 11-16. Contact T.C. Wong, American Electric Power, 1 Riverside Plaza, Columbus, OH 43215; (614) 223-2235; fax (614) 223-2205; e-mail: t.wong@ieee.org.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 12-15. Wynham Hotel, Philadelphia, PA. Contact Barry Hornberger, Philadelphia Electric Co., 2301 Market St., Bldg N3-1, Philadelphia, PA 19101; (215) 841-4619.

Fifth IFIP/IEEE International Symposium Integrated Network Management (ISINM 97), May 12-16. San Diego, CA. Contact Ann Marie Lambert, BBN Systems & Technologies, 10 Moulton St., Cambridge, MA 02138; (617) 873-3819; fax (617) 873-37776; e-mail: isinm97@bbn.com.

IEEE Particle Accelerator Conference, May 12-16. Vancouver, BC, Canada. Contact M.K. Craddock, TRIUMF, 4004 Wesbrook Mall, Vancouver, BC V6T 2A3 Canada; (604) 222-7341; fax (604) 222-7309; e-mail: craddock@triumf.ca.

IEEE Radar Conference, May 13-15. Sheraton University Hotel & Conference Center, Syracuse, NY. Contact Michael Wicks, Rome Laboratory, 26 Electronics Pkwy., Rome, NY 13441; (315) 330-4437; fax (315) 330-2528; e-mail: wicksm@rl.af.mil.

17th Electronic Components & Technology Conference, May 18-21. The Fairmont Hotel, San Jose, CA. Contact Jim Bruorton, Electronic Industries Association, 2500 Wilson Blvd., Arlington, VA 22201-3834; (864) 963-6621.

IEEE Instrumentation & Measurement Technology Conference (MTC 97), May 20-22. Chateau Laurier, Ottawa, Ontario, Canada. Contact Robert Myers, Conference Coordinator, 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OEMed Midwest, May 21-22. Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

OEM Electronics Midwest, May 21-22. Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

Canadian Conference on Electrical & Computer Engineering, May 25-28. Delta Hotel, Newfoundland, Canada. Contact David Collett, Newfoundland & Labrador Hydro, P.O. Box 12400, St. Johns, NF, A1A 4K7, Canada; (709) 737-1372; fax (709) 737-1782; e-mail: t.d.collett@ieee.org.

Fifth IEEE International Conference on Properties & Applications of Dielectric Materials (ICPADM), May 25-30. Sheraton Walker Hill, Convention Center, Seoul, Korea. Contact Joon-Ung Lee, Department of Electrical Engineering, Kwangwoon University, 447-1 Wolgye-Dong, Nowon-Ku, Seoul, 139-701, Korea; (82)-2-910-5144; fax (82)-2-942-0107.

JUNE

IEEE International Conference on Neural Networks, June 1-5. Houston, TX. Contact Nicolaos B. Karayiannis, Dept. of Electrical & Computer Engineering, University of Houston, Houston, TX; 77204-4793 (713) 743-4436; fax (713) 743-4444.

IEEE International Conference on Communications (ICC 97), June 8-12. Montreal, Canada. Contact Celia Desmond, Stentor, Fl. 6b, 33 City Center Dr., Mississauga, Ontario L5B 2N5, Canada; (905) 615-6507; fax (905) 615-8421; e-mail: celia.desmond@tc.resonet.com.

IEEE/MTT-S International Microwave Symposium (MTT 97), June 8-13. Convention Center, Denver, CO. Contact John Dunn, Dept. of Electrical & Computer Engineering, University of Colorado, Campus Box 425, Boulder, CO 80309; (303) 492-5920; fax (303) 492-5323; e-mail: dunn@boulder.colorado.edu.

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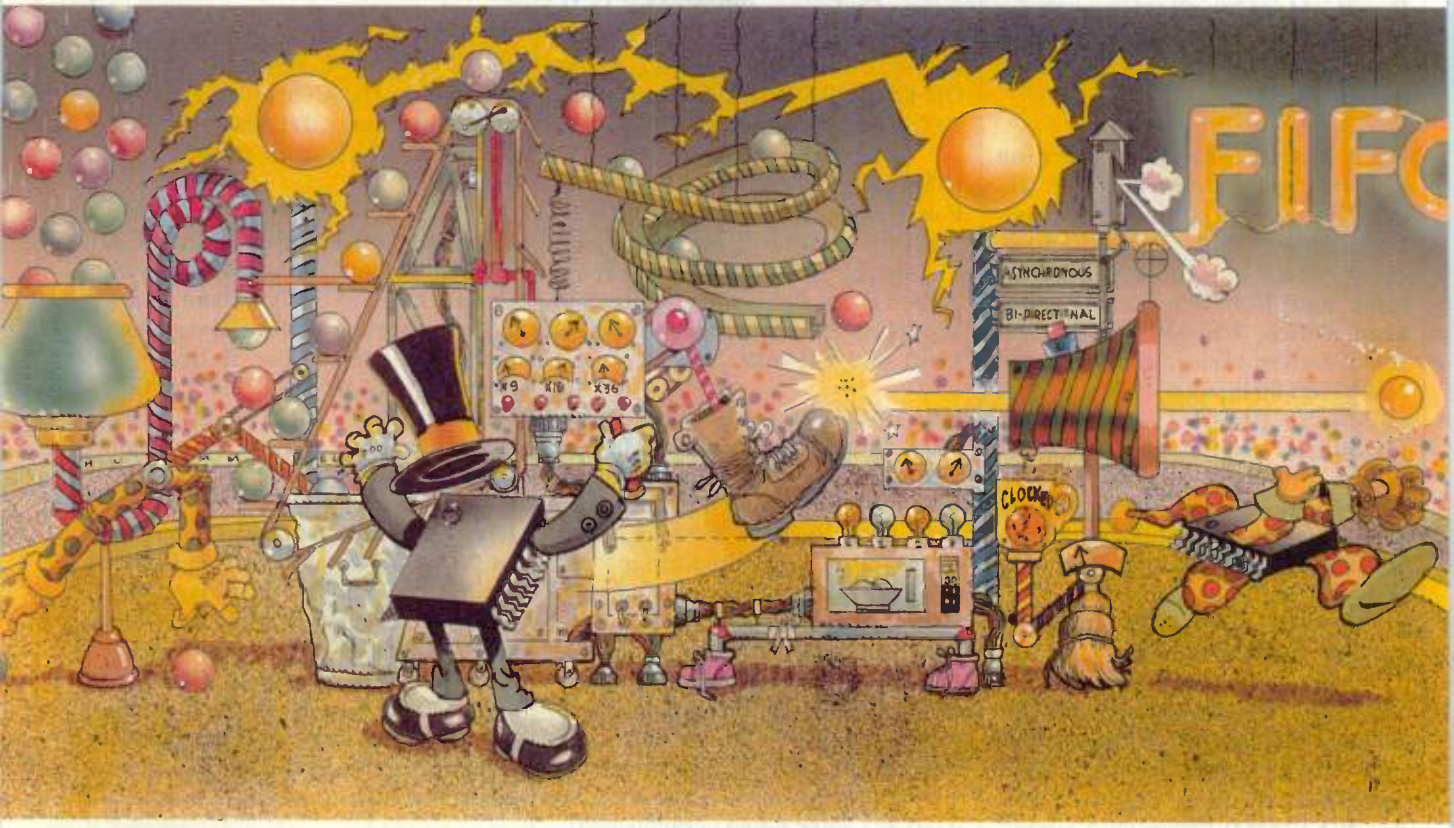

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Asynchronous FIFOs		
QS7201	512 x 9 with Buffer Memory	32, 28
QS7202	1K x 9 with Buffer Memory	32, 28
QS7203	2K x 9 with Buffer Memory	32, 28
QS7204	4K x 9 with Buffer Memory	32, 28
Clocked x9 FIFOs		
QS72211	512 x 9 Parallel Synchronous	32
QS72221	1K x 9 Parallel Synchronous	32
QS72231	2K x 9 Parallel Synchronous	32
QS72241	4K x 9 Parallel Synchronous	32
Clocked x18 FIFOs		
QS72215	512 x 18 Parallel Synchronous	68
QS72225	1K x 18 Parallel Synchronous	64
Clocked x36 FIFOs		
QS723611	512 x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS723620	1K x 36 Clocked FIFO with Dynamic Bus Sizing	132
QS723621	1K x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS725420A	256 x 36 x 2 Bidirectional Clocked FIFO	132, 144

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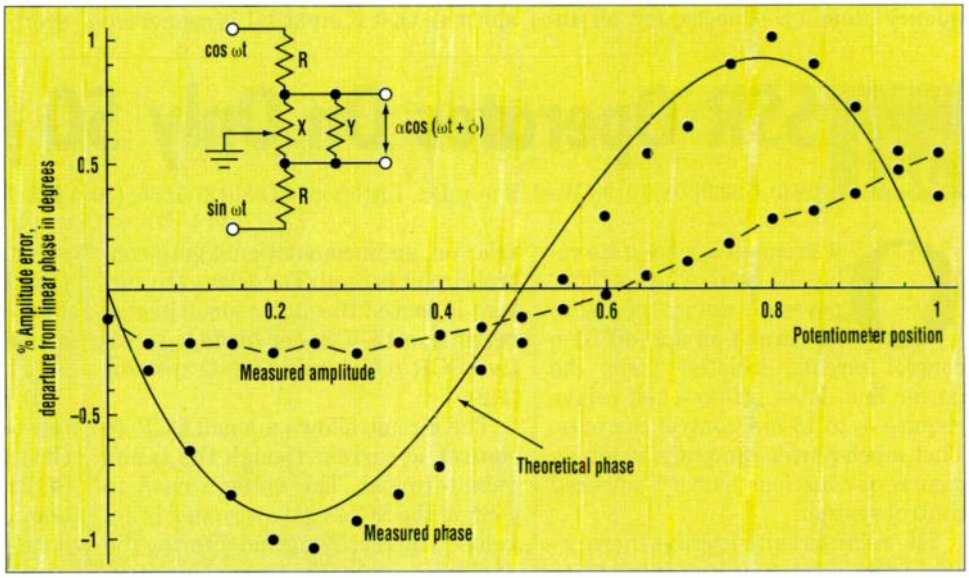
CIRCLE 520

Audio Interpolating Phase Shifter

D.I. HOULT, Institute for Biodiagnostics, National Research Council Canada, 435 Ellice Ave., Winnipeg, Manitoba R3B 1Y6, Canada; (204) 984-7459; fax (204) 984-6978.

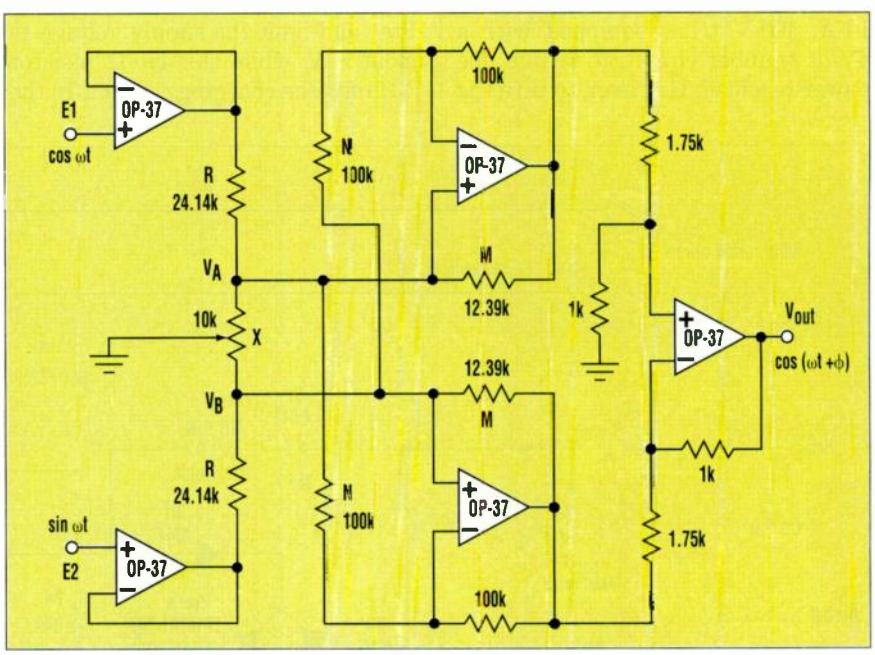
Numerous instances arise in which two quadrature phase analog signals are available but their phases need adjusting to be useful, or when a variable phase linear combination of the two is needed. The case that prompted this Idea for Design involved a radio frequency I-Q detection circuit. It delivered audio voltages $V_1 = \cos(\omega t + \theta)$ and $V_2 = \sin(\omega t + \theta)$, but the arbitrary phase shift θ could change in different applications and needed to be eliminated cheaply and conveniently. Progressive 90° phase shifts are easily made by "signal routing"—signal interchange and inversions. However, to produce smaller shifts $\phi \leq 90°$, linearly combining V_1 and V_2 with multiplicands $\cos\phi$ and $\sin\phi$ is usually advocated. This requires expensive cosine/sine potentiometers and analog multipliers, or digital methods.



1. INTERPOLATION BETWEEN COSINE and sine functions has constant amplitude and is almost phase linear with potentiometer position when resistance $R = (1 + \sqrt{2})X$ and $Y = -\sqrt{2}X$.

In searching for a lower-cost alternative, the circuit shown in Figure 1 was investigated. Obviously, as the potentiometer X is tracked from one end to the other, the phase ϕ of the difference voltage $\alpha \cos(\omega t + \phi)$ changes from 0 to 90°. It's not obvious, however, that if $R = (1 + \sqrt{2})X$ and $Y = -\sqrt{2}X$, the amplitude of α of the difference voltage stays constant at 0.586 as the potentiometer is turned, while the phase ϕ tracks from 0° to 90° almost linearly with potentiometer position. The departure from a linear law is shown in Figure 1; there's a maximum deviation of only ±0.9°. By contrast, if resistor Y is dispensed with and R is set to an optimal value of $X/\sqrt{2}$, there's a ±1.1% variation in amplitude α and a deviation in ϕ of ±4.6° from linear.

One problem does exist, though—resistance Y is negative. Fortunately, such a resistance can be generated with the aid of a high input impedance amplifier of gain +2 with positive feedback via a resistor of value Y. The amplifier input impedance is then –Y. The situation is complicated a little by the need to take the difference voltage, but a suitable circuit was created *(Fig. 2)*.



2. A SIMPLE INTERPOLATING PHASE SHIFTER places a negative resistance across potentiometer X to obtain constant-amplitude, linear-phase performance.

Practical results obtained at 1 kHz with a 0.5% tolerance in resistor values are shown in Figure 1—the better the accuracy, the better the performance. The positive resistance supplied by resistors N has been compensated by a change in Y to value $M = (1/\sqrt{2}X + 1/N)^{-1}$. Incidentally, a similar result can be obtained with a sum rather

than a difference output *(Fig. 1, again)*. However, the two resistors R are negative, which isn't very convenient. Note that as with most positive feedback circuits, good layout and short leads are needed for high-frequency stability. If necessary, all impedance values can be proportionately reduced, or 10-pF capacitors placed in parallel with each 100k resistor to prevent oscillation.

Finally, as $\cos(\omega t + \phi) = \cos(\omega t)\cos(\phi) - \sin(\omega t)\sin(\phi)$, it comes as no surprise that if input E1 is connected to ground and a direct voltage is put on E2, the output obtained is a good approximation to the first quadrant of a sine curve as the potentiometer is varied. If connections are reversed, a good approximation to a cosine is seen. □

CIRCLE 521

SSR Operates On Only 50 μA

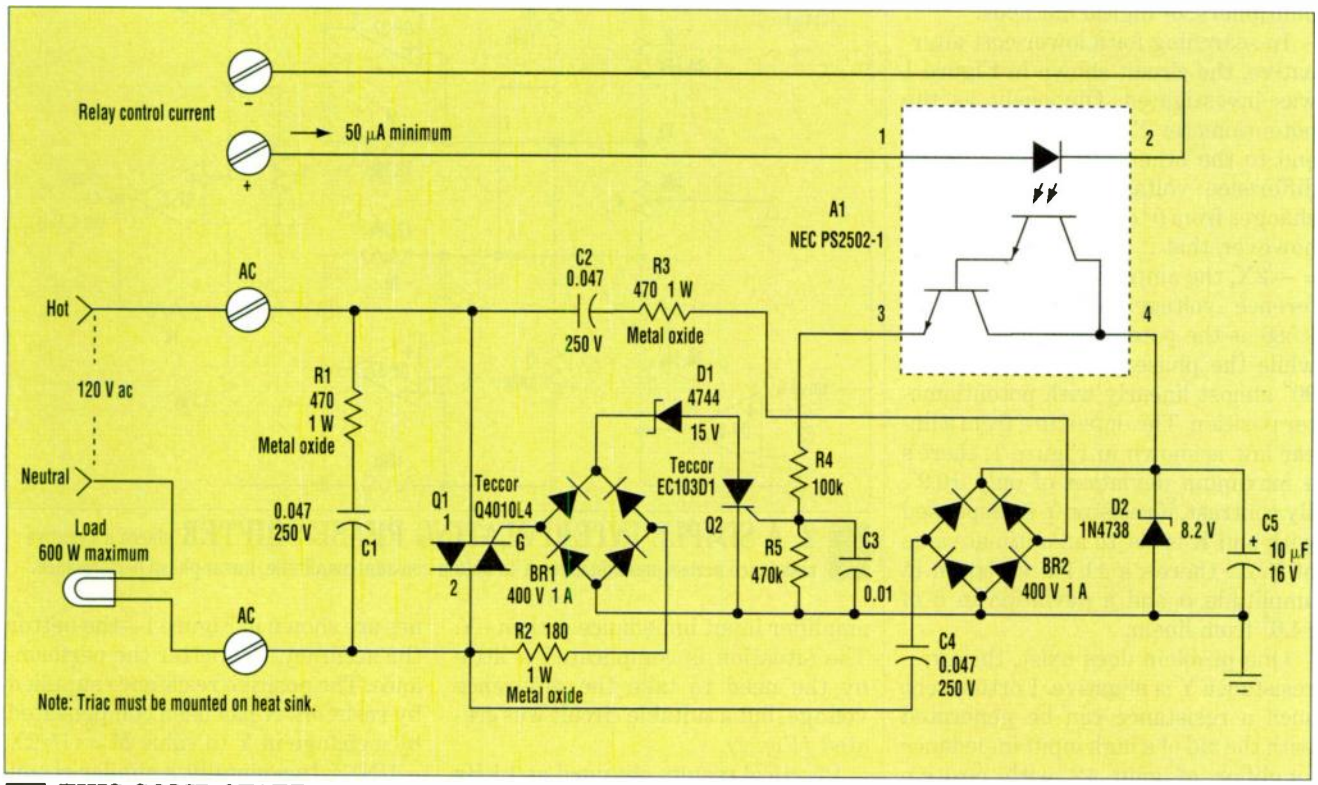
DAVID A. JOHNSON, 10198 West Berry Dr., Littleton, CO 80127-1856; (303) 973-8408; fax (303) 973-6600.

Often times, a solid-state relay is used when a line-powered device needs to be turned on and off by a control circuit, isolated from the power line. Most off-the-shelf relays require 3- to 15-mA control currents. That much power can put a strain on a current-conscious battery-powered control system.

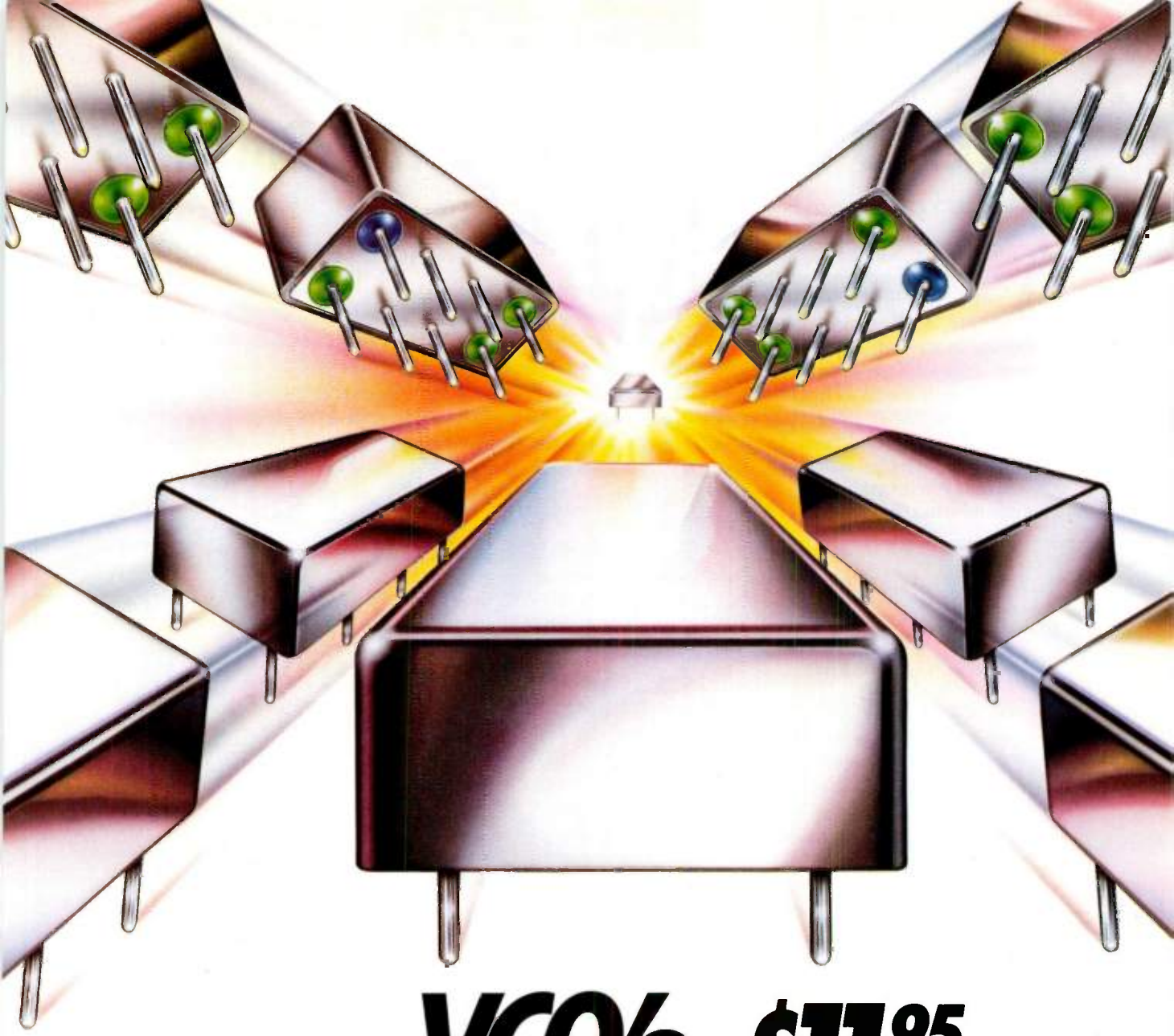
The relay circuit described here reduces the needed control current to a much more tolerable 50 μA, but can switch up to 600 W of 120 V ac power. The circuit employs a conventional 10-A, 400-V triac, equipped with a dV/dt snubber circuit, to switch line power to a load. However, to turn the triac on, an unconventional gate-control circuit is used. The triac gate current is routed through a small bridge rectifier, a 15-V Zener diode, a sensitive SCR (Q2), and a 180-Ω resistor (R2).

The circuit allows a small SCR to control ac current though the triac's gate terminal. The voltage need to control the SCR's gate terminal is developed by rectifying and filtering the ac voltage across the triac. Capacitors C2, C4, and C5, resistor R3, bridge rectifier BR2, and Zener diode D2 form the rectifier circuit. C5 and D2 filter and limit the supply voltage to about 8 V, while the 470-Ω resistor R3 limits the charging current. In the off state, the ac voltage across the triac is equivalent to the line voltage. In a conventional circuit, the voltage across the triac in the on state would only be a few volts.

To develop a slightly higher voltage (up to 30 V p-p), a 15-V Zener diode (D1) is inserted in series with the SCR. D1 delays the triac's conduction trigger point each half cycle and produces only a slight reduction in rms power to the load. The dc control voltage, produced by the rectifier circuit, is switched to the SCR's gate using a sensitive Darlington-type optoisolator (A1). Only about 50 μA of LED current in the isolator is needed to fully turn on the SCR. □



THIS SOLID-STATE RELAY CIRCUIT reduces control current to 50 μA, yet it still can switch up to 600 W of 120 V ac power.



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POS-75	37.5-75	-110	-27	20	11.95
POS-100	50-100	-107	-23	20	11.95
POS-150	75-150	-103	-23	20	11.95
POS-200	100-200	-102	-24	20	11.95
POS-300	150-280	-100	-30	20	13.95
POS-400	200-380	-98	-28	20	13.95
POS-535	300-525	-93	-26	20	13.95
POS-765	485-765	-85	-21	22	14.95
POS-1025	685-1025	-84	-23	22	16.95
NEW POS-1060	750-1060	-90	-11	30*	14.95
NEW POS-1400	975-1400	-95	-11	30*	14.95
NEW POS-2000	1370-2000	-95	-11	30*	14.95

*Max. Current (mA) @ 8V DC.
Notes: Tuning voltage 1 to 16V required to cover freq. range. 1 to 20V for POS-1060 to -2000. Models POS-50 to -1025 have 3dB modulation bandwidth, 100kHz typ. Models POS-1060 to -2000 have 3dB modulation bandwidth, 1MHz typ.
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K-POS2 $79.95 (contains 1ea. all models except POS-75,-150,-300, -1060 to -2000)
K-POS3 $79.95 (contains 2ea. models POS-1060,-1400,-2000).

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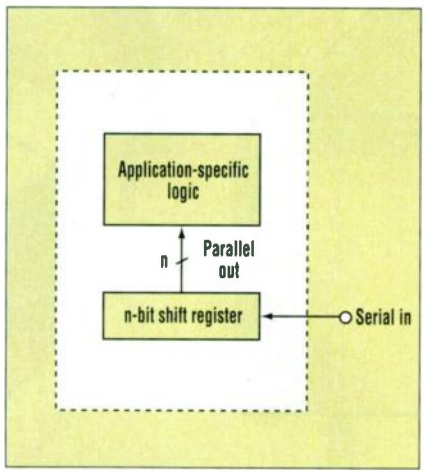
CIRCLE 522

CPLD Optimizes Serial Test Patterns

CHRIS JONES, Cypress Semiconductor Corp., 3901 North First St., San Jose, CA 95134-1599; (408) 943-2600.

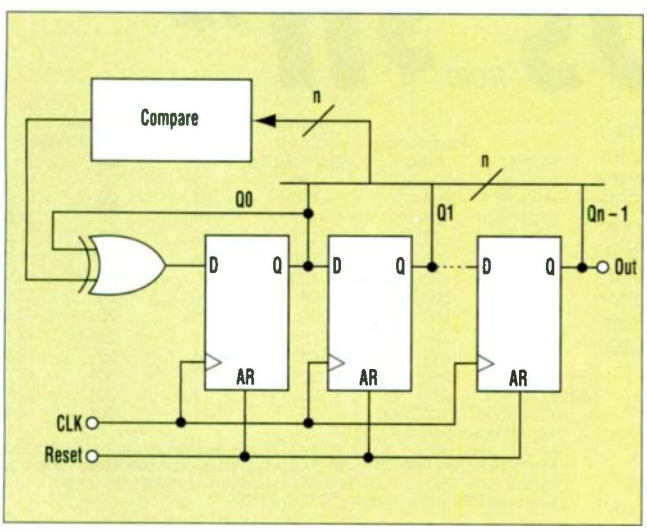
An n-bit serial-to-parallel shifter is a common circuit block contained in many different devices and applications *(Fig. 1)*. Transmitting data over a serial connection requires this type of circuit at the receiver end. When testing the operation of such a device, serial data should be supplied that when viewed as groups of n bits, contains all 2^n possible data combinations of 0s and 1s. This ensures that the logic responding to the shifter's parallel output acts correctly under all conditions. In addition, this serial data stream should be as short as possible to save test time. One way to do that is:



1. THIS SERIAL-TO-PARALLEL shifter is used in many common applications, including serial data communications.

VHDL CODE FOR SERIAL TEST PATTERN

```
library ieee;
use ieee.std_logic_1164.all;
use work.std_arith.all;

entity sequence is port(
  clk, reset:  in    std_logic;
  qout:        buffer std_logic);
end sequence;

architecture archsequence of sequence is

  constant width:integer := 4;
  signal qint: std_logic_vector((width-1) downto 0);
  signal compout: std_logic;
  signal nextbit: std_logic;

begin

  compout <= '0' when ( (qint >= 1) and (qint <= 2**(width-1)) ) else '1';
  nextbit <= ( (compout and not qint(0)) or (not compout and qint(0)) );

  shifting: process (reset, clk)
  begin
    if (reset = '1') then
      qint <= (others => '0');
    elsif (clk'event and clk= '1') then
      qint(0) <= nextbit;
      for i in 1 to (width-1) loop
        qint(i) <= qint(i-1);
      end loop;
    end if;
  end process shifting;

  qout <= qint(width - 1);

end archsequence;
```



2. THE SERIAL OUTPUT in this serial-test-sequence generator provides all 2^n combinations of n bits after only n shifts. The comparison block outputs a "0" when the n bits are in the range of $[1, 2^{n-1}]$. When not in that range, a "1" goes to the XOR gate.

Instead of placing all 2^n groups of n bits in a serial stream of $(2^n \times n)$ total bits, it can be accomplished in the optimal 2^n bits after n-1 initialization bits. For n equal to 4, the following string of 0s and 1s contains all 16 combinations of 4 bits:

0000111101011001000

The first three bits are initialization bits. After the fourth bit, the last four bits are 0000 (0); after the fifth bit, the last four bits are 0001 (1); after the sixth bit, the last four bits are 0011 (3); and so on. The 16 possible patterns are included in the order: 0, 1, 3, 7, F, E, D, A, 5, B, 6, C, 9, 2, 4, and 8. The sequence can be repeated if desired.

This optimal serial test pattern is generated for n bits as shown in the Figure 2 circuit. It's basically an n-bit shifter that loads the Q0 register with either its present state or the complement of its present state based upon the value contained in the entire register. The comparison block outputs a

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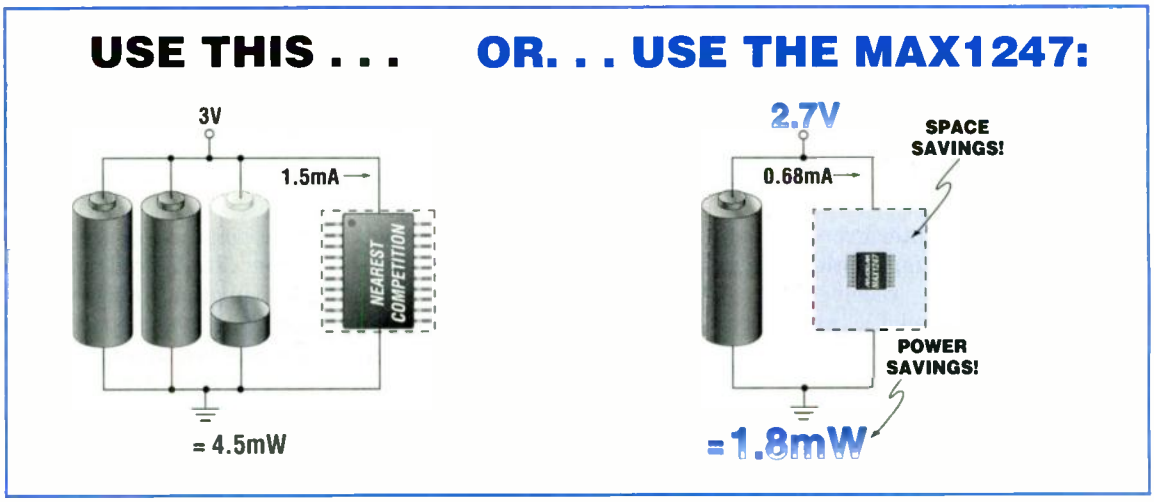

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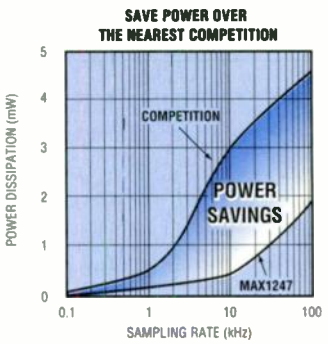

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"0" if the n-bit parallel bus value is in the range of [1, $2^{(n-1)}$], otherwise, it outputs a "1." This means that, when shifting, Q0 gets inverted if the shifter value is between 1 and $2^{(n-1)}$, while it doesn't get inverted for all other shifter values. See the listing for this circuit's VHDL code.

This simple test-pattern generator easily fits into a CPLD or FPGA. Cypress's 32-macrocell CY7C371i CPLD requires n macrocells, a single product term for all but one of the macrocells, and n product terms for the macrocell that contains Q0. The 1k gate CY7C382 FPGA from Cypress requires n logic cells for the n registers, and, depending upon n, either 0, 1, or 2 extra logic cells for the comparison.

The pattern generator also can be employed in other applications, such as to provide all possible addresses to a device that receives address bits serially. Using this pattern generator, a device starts at an address, does an operation associated with that first address, then moves to another address with only a single-bit shift. □

CIRCLE 523

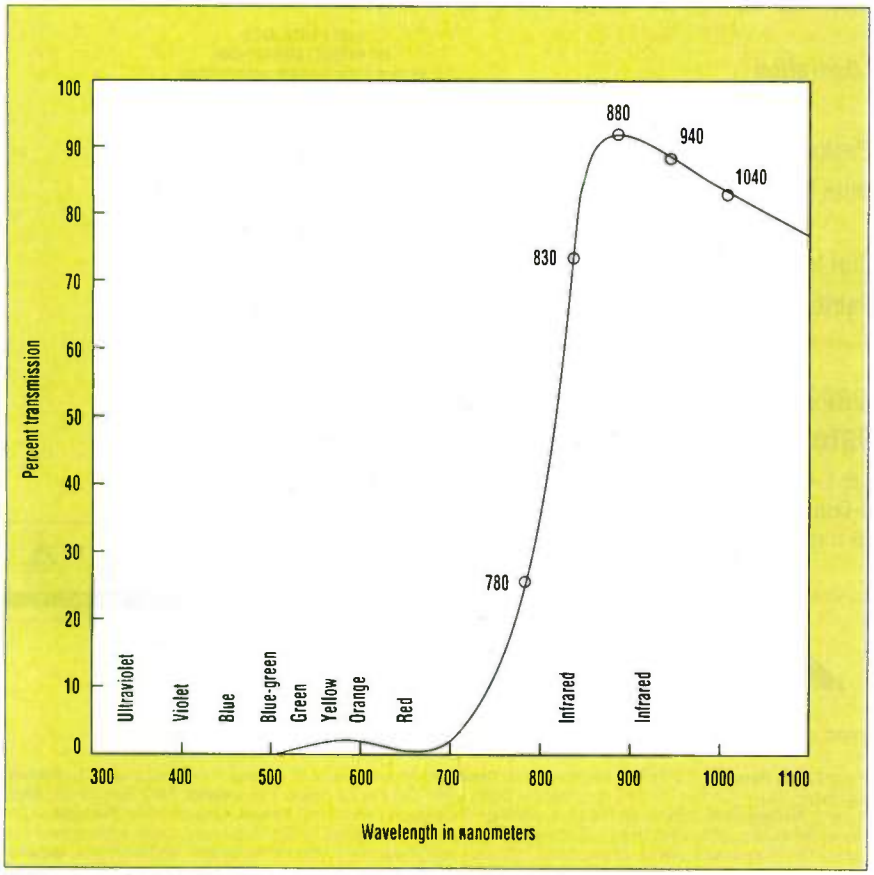
35mm Film Makes Low-Cost IR Filter

DAVID A. JOHNSON, 10198 West Berry Dr., Littleton, CO 80127-1856; (303) 973-8408; fax (303) 973-6600.

To minimize interference from room lighting, optical communications receivers and some infrared TV camera systems often place an infrared low-pass filter in front of the light detector. The filters are designed to block most of the visible light, allowing the near infrared light to pass and reach the detector. However, glass filters that are often used for these types of applications are expensive.

A less costly alternative is to use ordinary 35mm photographic film that's been exposed to fluorescent light and then developed. The color negative produced after the photographic developing process has a sharp cutoff at about 830 nm and completely blocks most of the visible spectrum *(see the figure)*.

The filter's transmission is perfect for many near infrared LEDs and lasers with wavelengths between 830 and 950 nm. Kodak's Kodacolor film with an ASA rating of 100 that's exposed to a "cool white" fluorescent light for five seconds works the best. The film processor should be told to develop the film in the usual manner but not make any prints. The color negatives become the filter material. A typical 36-exposure roll will cost only about $5.00. The film can be easily cut into any required size or shape. However, the film is *not* recommended for applications where it can become scratched or exposed to moisture. □



WHEN EXPOSED TO "COOL WHITE" fluorescent light for five seconds, the color negative (using Kodacolor 100 ASA film) produced after the developing process exhibits a sharp cutoff at about 830 nm.

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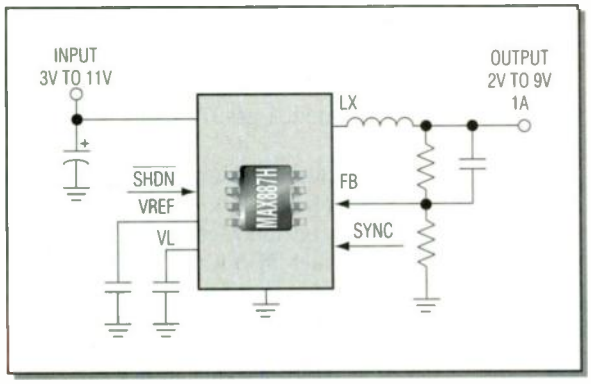

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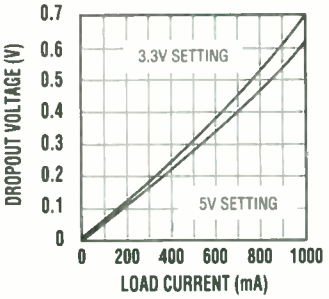

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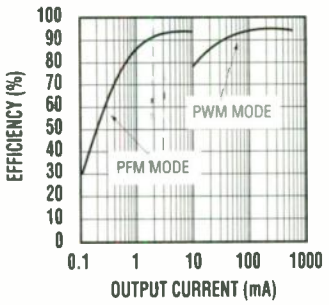

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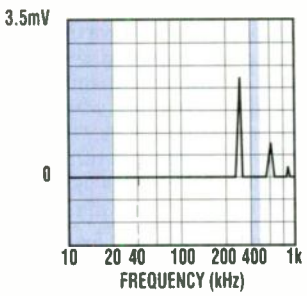

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UPCOMING MEETINGS

JUNE

IEEE International Symposium on Circuits & Systems (ISCAS 97), June 9-12. Hong Kong Convention & Exhibition Centre, Hong Kong. Contact ISCAS '97 Secretariat, Department of Electrical & Electronic Engineering, University of Hong Kong, Pokfalam Rd., Hong Kong; (852) 28592710; fax (852) 25598738; e-mail: iscas97@hkueee.hku.hk.

34th Design Automation Conference (DAC 97), June 9-13. Anaheim Convention Center, Anaheim, CA; Contact MP Associates Inc., 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; fax (303) 530-4334.

IEEE International Conference on Consumer Electronics (ICCE), June 11-13. The Westin Hotel O'Hare, Rosemont, IL. Contact Diane D. Williams, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397.

International Solid-State Sensors and Actuators Conference (Transducers 97), June 15-19. Hyatt Regency Hotel, Chicago, IL. Contact Kensal D. Wise, 1246 EECS Building, University of Michigan, 1301 Beal Ave., Ann Arbor, MI 48109-2122; (313) 764-3346; fax (313) 747-1781.

IEEE Digital Cross Connect Systems Workshop VII (DCS 97), June 16-19. Banff Park Lodge, Banff, Alberta, Canada. Contact James H. Simester, Lucent Technologies, P.O. Box 3030, Room 4J-526, 101 Crawfords Corner Rd., Holmdel, NJ 07733-3030; (908) 949-7336; fax (908) 949-2724; e-mail: sims@bostare.ho.att.com.

Third Conference on Object-Oriented Technologies & Systems (Coots 97), June 16-19. Marriott Hotel, Portland, OR. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; http://www.usenix.org.

IEEE International Conference on Systems, Man, and Cybernetics, June 16-20. Hyatt Orlando, Orlando, FL. Contact James M. Tien, Chair, DSES Department, Rensselaer Polytechnic Institute, Troy, NY 12180-3590; (518) 276-6486; fax (518) 276-8227; e-mail: tienj@rpi.edu.

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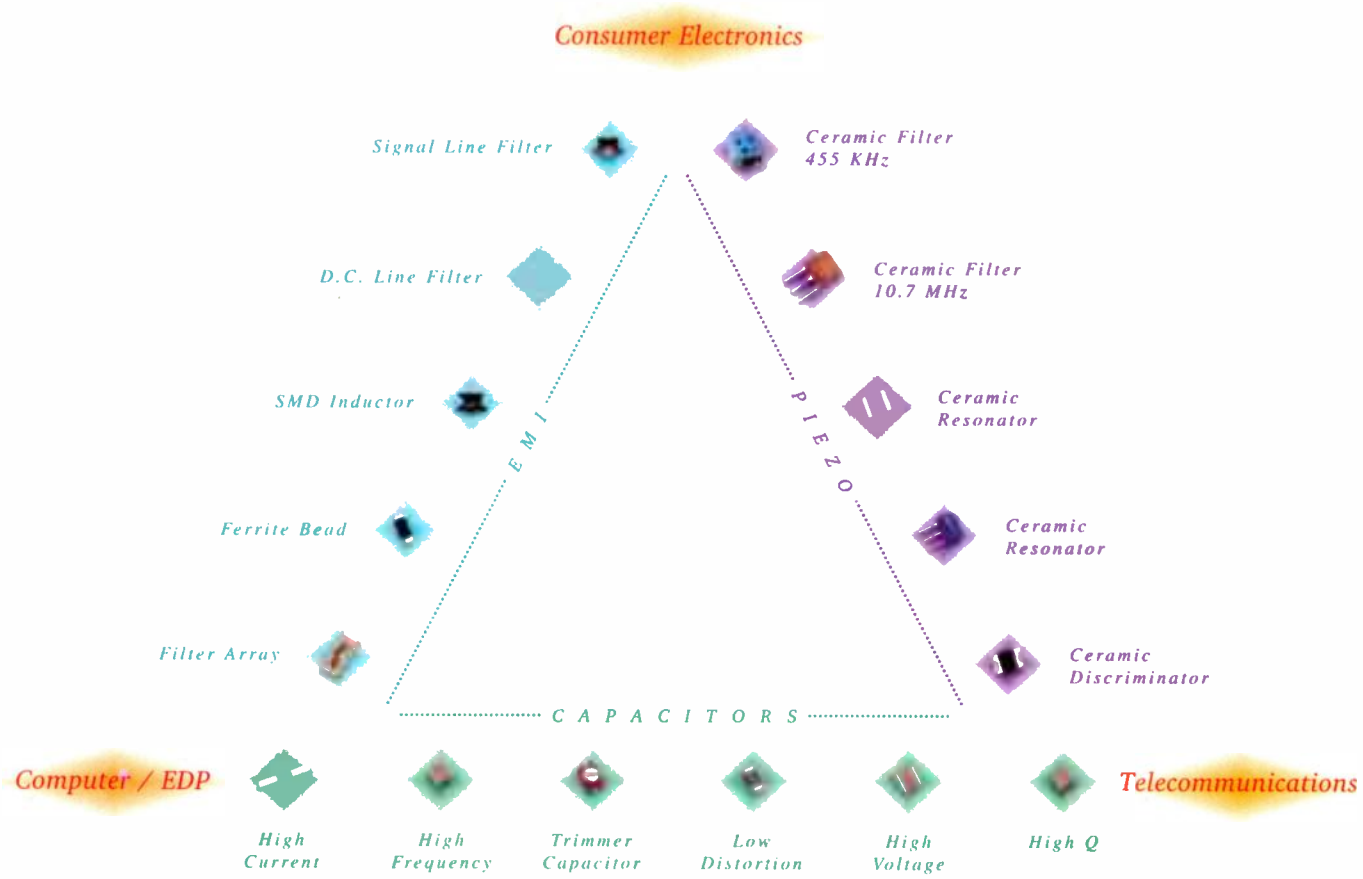

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MEETING THE STANDARD

Input-Device Integration

JOHN MILIOS, USAR SYSTEMS and BRUCE DEVISSER, FUJITSU

Embedded User Input Devices (UIDs) in portable systems come in different forms and form factors as they are tailored to fit specific system functions. When it comes to interfacing the input-device sensors to the host system, designers are faced with evolving alternatives defined by the capabilities of the host-system chip set. The selection of the right interface is a function of cost, power consumption, and suitability to the application.

UIDs in portable systems possess characteristics discrete from those of the external desktop input devices. For example, they are not standalone devices—they are embedded in the system box. Although this characteristic seems to give designers more flexibility in selecting the system interface, the UIDs still have to perform as primary boot devices. With proprietary architectures, this imposes little, if any, limitations because the operating system is created from scratch to the specific implementation. In standard-architecture systems, diversions from the dominant PS/2 interface require additional BIOS support to maintain compatibility with legacy software and hardware.

Unlike embedded UIDs, external peripherals must act in a standard fashion to provide end users with the greatest flexibility in selecting off-the-shelf parts. If an external UID is connected to a portable system, data streams from external keyboards and mice must be converted and merged with the embedded device data and are then relayed to the system through the common interface.

Another unique feature of portable UIDs originates from the role they often play in system-level power management. These portable UIDs provide the main link between the users and the system. Users invoke action through the input devices, causing changes in the system's power state. Consequently, input devices have to be functional at all times when the system is fully on or in suspended mode. As a result, the interface protocol that is selected should provide for minimum power consumption during the system's idle state.

Size is another limiting factor in portable systems. Each implementation imposes a number of different requirements on the pc-board area as to the space required to accommodate the electronics for the input device's sensor interface. Size is typically determined by packaging technology and the number of pins necessary to implement the interface.

In addition, special human factors have a direct impact on the operational characteristics and the method that the input-device subsystem integrates with the rest of the hardware and the operating system. These factors affect such areas as the scanning rate for portable keyboards, multilayered keyboard implementations, single-hand-operation support, and support for hot plug-ins of external devices.

The PS/2 port has been around for quite some time and has served sufficiently for basic keyboard and mouse input requirements. It's been used for interfacing embedded keyboard and pointer devices and for acting as an extension to supply more comfortable full-size desktop attachments. Architecturally, there are two alternative ways to implement the PS/2 port in portable systems—as a direct interface to the ISA bus, or as an interface to the PS/2 ports of an I/O chip.

In most cases, the PS/2 port is implemented with an 8042-compatible keyboard controller. This controller offers a register- and pin-compatible interface to the ISA bus, ensuring BIOS compatibility in PCs. At minimum, the keyboard controller supports scanning of the embedded keyboard, interface to an internal pointing device, and an 8042-compatible expansion port available to PS/2-compatible external keyboards and mice. The higher-end controllers support other types of system-specific functions, including LCD control, in addition to battery and power management.

The second method works in systems that employ chip sets with an embedded 8042 controller. In this case, the basic input device interface is implemented with a keyboard encoder. At the very least, the encoder provides keyboard scanning and the PS/2 keyboard interface to the system necessary to implement the standard PS/2 keyboard boot device. In more complex implementations, the encoder also will support an embedded pointing device, an 8042-compatible expansion port, along with other system-specific functions such as power management and LCD support.

Most portable systems typically offer at least one 8042-compatible expansion port to connect an external keyboard or a PS/2-compatible mouse. The keyboard controller must have the capability of supporting the swapping of the two types of devices on the same port, as well as hot-plugging. In addition, this feature requires that the newly-connected device is synchronized at the moment of connection with the internal BIOS state as well as with any embedded devices.

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486DX2	486DX4	486DX2/486DX4	5x86	Pentium processor	Pentium processor	Pentium Pro processor
66 MHz	100 MHz	100 MHz	100 MHz	200 MHz	200 MHz	200 MHz
None	Up to 1 Mbyte	Up to 1 Mbyte	Up to 1 Mbyte	512 Kbyte	512 Kbyte	512 Kbyte
16 Mbyte	32 Mbyte	32 Mbyte	32 Mbyte	64 Mbyte	64 Mbyte	64 Mbyte
SVGA 1024 x 768	SVGA 1280 x 1024	SVGA 1280 x 1024	SVGA 1280 x 1024	SVGA 1280 x 1024	SVGA 1280 x 1024	SVGA 1280 x 1024
One: Centronics	One: IEEE-1284	One: IEEE-1284	One: IEEE-1284	One: IEEE-1284	One: IEEE-1284	One: IEEE-1284
Two RS-232C	Two RS-232C	Two RS-232C	Two RS-232C	Two RS-232C	Two RS-232C	Univ. Serial Bus (USB) Two RS-232C
IDE	IDE	IDE	IDE	EIDE	EIDE	EIDE
No	No	No	No	SCSI-2	SCSI-2 Fast/Wide	SCSI-2 Fast/Wide
Optional	Optional	Optional	Optional	10BaseT and 10Base2	10BaseT, 10Base2, and 100BaseTX	10BaseT, 10Base2, and 100BaseTX
Optional	Optional	Optional	Optional	Via PMC	Via PMC	Via PMC
None	PC/104	PC/104	PC/104	PMC	PMC	PMC
VME via ISA bus	VME via local bus and VIC chip	VME via ISA bus	VME via local bus and VIC chip	Enhanced VME via Tundra/Universe	Enhanced VME via Tundra/Universe	Enhanced VME via Tundra/Universe
No	Yes	No	Yes	Yes	Yes	Yes
A32:D32	A32:D32 and BLT64	A32:D32	A32:D32 and BLT64	A32:D32 and BLT64	A32:D32 and BLT64	A32:D32 and BLT64
Yes	Yes	Yes	Yes	Yes	Yes	Yes
Yes	Yes	Yes	Yes	Yes	Yes	Yes
SGL	SGL, PRI, RRS	SGL	SGL, PRI, RRS	SGL, PRI, RRS	SGL, PRI, RRS	SGL, PRI, RRS
No	Yes	No	Yes	Yes	Yes	Yes
Yes	Yes	Yes	Yes	Yes	Yes	Yes
DOS, Windows	DOS, Windows, Windows NT™	DOS, Windows, Windows NT	DOS, Windows NT	DOS, Windows NT, LynxOS, VxWorks	Windows NT, LynxOS, VxWorks	Windows NT, LynxOS, VxWorks

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Serial Bus Sends Card Power Status, Commands

Take some of the complexity out of power management.

DAN SOWIN and JIM MOYER
Micrel Semiconductor Inc., 1849 Fortune Dr., San Jose, CA 95131; (408) 944-0800.

As PC architectures move into sophisticated power management, there's an increasing need to send data to peripherals in a rapid, yet inexpensive manner. In addition, PC Cards have proliferated, and with the adoption of CardBus, they are increasing in speed and functionality. The end result is an added demand on the host power system. These two evolutions call for a new approach to applying power and detecting faults in the legacy PC Card and CardBus slots, namely the PCMCIA Power Control (PPC) bus.

This serial bus specification has been adopted by an industry group representing PC Card controller and power-switch IC manufacturers. It is recommended as the approach to handle power-condition status reporting and control.

The status reporting can identify faults so that specific corrective action can be taken by the system that will conserve battery power, but still allow other portions of the system to function. The benefits are economic and functional, and will result in a more robust system. In addition, the PPC bus saves pins and board traces for high-density designs that are often found in notebook PCs.

The PPC bus closes the loop on power control by taking advantage of a duplex serial communication link. This technique allows commands to be sent to the PC Card power-switch IC from the controller, and the status of the power interface to be reported to the system from the power-switch circuits. Another key function is the bus' ability to report any slot power faults to the system fast enough for effective correction action to be taken *(Fig. 1)*.

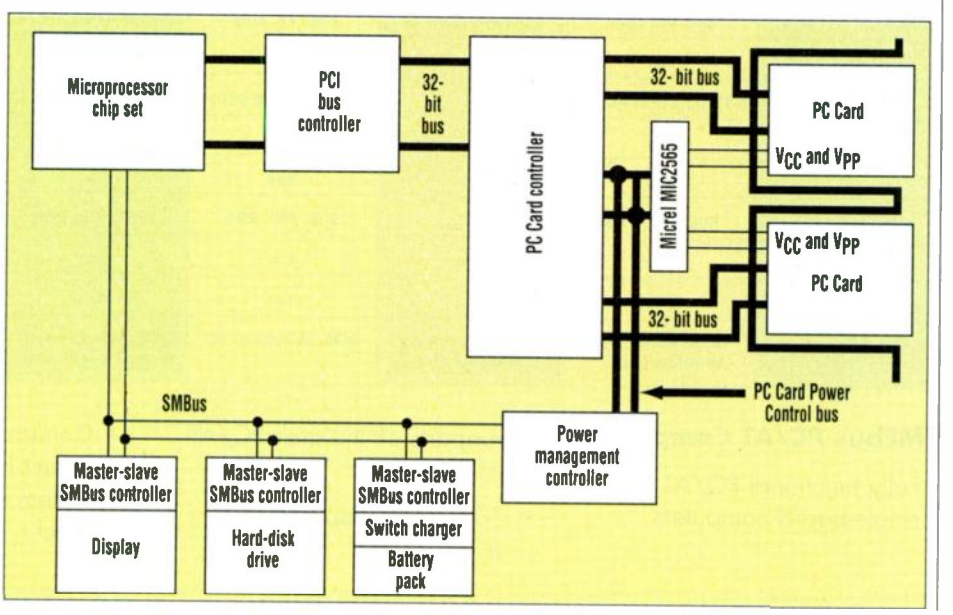
The power-switching IC or controller takes commands directly from a PC Card controller chip and switches power to the appropriate pins of the slot and the card that's plugged into it. The power is supplied from the host system, usually 3.3 V, 5 V, and 12 V, that switches to the batteries when the ac source is removed.

PC Card priorities for the power-switching IC are to supply the voltage through low-resistance switches with controlled rise and fall times, as described in the PC Card specification. This voltage is supplied to the card's V_{CC} and V_{PP} power pins. Other functions are to limit current output and thermal shutdown for sustained high current loads as in a dead short.

System priorities are to protect the battery charge, especially when the system is in a standby mode, so the system can easily reactivate. If a fault occurs in a card slot, the transient current load should be limited so that the power-supply voltage cratering (a momentary drop in voltage) does not occur. This can cause an erroneous reset to occur in the host system.

Status reporting could include a catastrophic fault in the PC Card slots, which could discharge the batteries. Therefore, a means of interrupting the system and identifying the fault must be added as part of the protocol. This type of fault could be classified as anything from an errant screwdriver in the slot to a faulty card.

This reporting method proposes a way of interrupting using the serial lines, which is more efficient than dedicating external pins to it. Because the serial bus is used to decrease the package's pin count, this method reduces the pin count and saves package size, board traces, and their associated costs. The serial bus allows for



1. The PPC bus can be used to handle power-condition status-reporting and control. It also is useful in reporting power faults.

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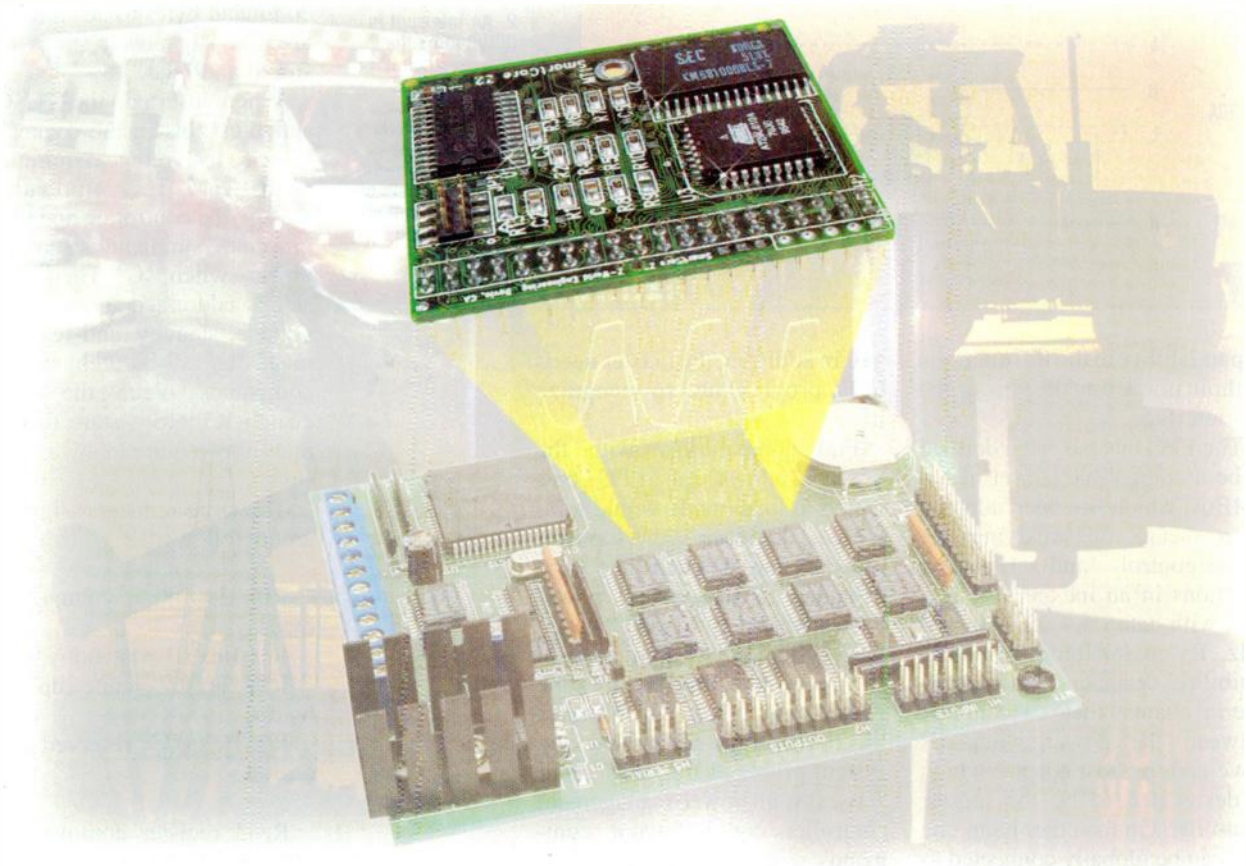

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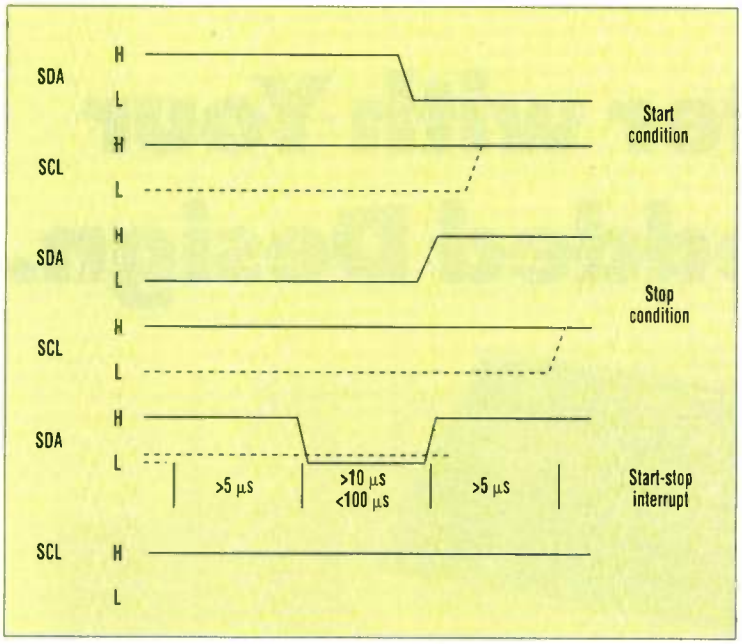

2. An interrupt is initiated by the power-switch IC on an idle bus when the clock and data signals are high for at least 5 µs. The interrupt consists of a start bit immediately followed by a stop bit.

expandability of the IC functions without impacting the pins or the bus interface.

The PPC bus has been defined to be a compatible subset of the SMBus, which has been adopted as a means of satisfying the power-control and reporting functions in an inexpensive format, with data rates of 10 to 100 kHz. By maintaining this compatibility, designers can employ a serial channel that is a local link between the power-switch IC slave and the host adapter which is designated to be the master controller. On the other hand, the link can be globally connected to other master controllers on the system's SMBus.

The SMBus, originally developed by Intel for battery management in controllers and chargers, also is useful for power management throughout the PC. It uses an I^2C bus backbone to transfer two-wire clocked synchronous duplex data from a master controller to multiple slaves. Note that the slaves also can function as masters.

Employing the SMBus in a different fashion allows it to be used to report catastrophic any faults without going through bus arbitration to put an interrupt on the serial bus. The condition is normally ignored in standard SMBus implementations, and is therefore not illegal. In addition, the master needs to be programmed to recognize it.

Full compatibility with the SMBus allows the PPC bus, which in local mode would transceive between the power switches and the controller, to be extended to the system power controller *(Fig. 1, again)*. This allows system power commands to be received directly by the power-switch IC, which saves time. The trade-off is that any system problems that may occur at the system power-management controller could corrupt commands sent to the power-switch chip. The danger here is applying the wrong power supply to a particular card.

The power-switch IC is an analog device, so it is relatively expensive to add bytes of register logic. Consequently, the bus interface is defined to be an SMBus slave. This reduces the circuitry by eliminating bus-arbitration logic. All command read and write transactions are initiated by the host controller. These commands are:

- Voltage Command: standard SMBus write-byte command
- Standby Command: standard SMBus write-byte command
- Read Status: standard SMBus read-byte command
- Read Interrupt Latches: standard SMBus read-byte command
- Interrupt Response: standard SMBus alert response

Command, status, and interrupt bytes are stored in nine registers on both the controller and power-switch IC (four for commands and five for read transactions). These registers allow command bytes to be stored, and also for slot power status to be stored and read.

When inserted, the PC Card activates pins in the socket that identify the voltage requirements of that card. This information is read by the controller, and the appropriate command is sent to the power-switch IC. The specific slot is addressed in each of the voltage, standby, and read commands by a 7-bit address. These commands place the power-switch IC into a state that supplies the required power to the slots.

The write-register assignments are as follows:

R0: Hex 00 = voltage codes byte
R1: Hex 01 = standby byte
R2: Hex 02 = interrupt mask byte
R3: Hex 03 = reserved for future use

Read register commands are differentiated from "writes" by sending a command byte that designates hex 8x for register Rx, instead of hex 0x. In addition, the read/write bit in the command message is set to logic "0."

Command-message data bytes are loaded into one of the registers R0 to R2. A Voltage Command addresses register R0 at hex address 00, and the Standby Command byte is loaded into R1. The interrupt mask bits in the Write R2 register (address hex 02) determine which corresponding status bits may interrupt the system. A logic "1" in a mask bit enables the corresponding status bit to generate an interrupt. The mask byte can be read by sending a Read Status Command for register hex 82.

A read command from the

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master will fetch a data byte from the bank of Read Registers R0 to R4. The Read Status Command will address read register R4 at address hex 84, which will fetch the byte with the following symbols:

h = thermal shutdown
j = V_{CC} OK status (has reached programmed voltage)
k = V_{CC} slewing
m = I_{CC} limit (in current limiting)
f = V_{CCPP} OK status
p = V_{CCPP} slewing
u = I_{PP} limit
O = reserved for expansion

Interrupt latch bits stored in read register R3 (address hex 83) can be set only by a positive-going transition of the corresponding status bit in read register R4. The register is cleared when it is read by a Read Status command. The Interrupt Latch bits are defined as follows:

h = thermal shutdown
j = V_{CC} OK status (has reached programmed voltage)
k = 0 not used
m = I_{CC} limit (in current limiting)
f = V_{CCPP} OK status
p = 0 not used
u = I_{PP} limit
O = reserved for expansion

The standby command is formatted like the voltage command, except that the register address is now hex 01, and the command byte is s = 1 followed by seven "don't care" bits. This command sets the power switches into a standby state, but that state is not defined in the bus protocol.

The next command format used by the controller to fetch the status bytes stored in the Read Registers of the power switch IC is the Read Status command, addressed to read register R4 (hex 84).

An interrupt is the one exception to initiating transactions in the controller bus master. It is initiated in the slave power-switch IC to signal the onset of a fault condition or a task completion. It can be initiated by the power-switch IC on an idle bus, when the clock and data are high for at least 5 µs *(Fig. 2)*. The data line (SDA) is pulled low for at least 10 µs, then is allowed to go high for at least 5 µs.

If there's a collision on the bus with another message, the transmitter waits for a clear bus, then retransmits. This requires the controller to respond by sending an Interrupt Response message, in which the initiating slave identifies itself by its assigned address, so the effect is similar to a vectored interrupt. The master can then immediately send a Read Status command to that particular slot register to identify the problem.

This rapid identification typically keeps the latency time of the response under 2 ms, or 1.2 ms for a 33-kHz clock. The interrupt signal is a start bit followed immediately by a stop bit *(Fig. 2, again)*. The Interrupt Response message is followed by a Read Interrupt Latches message, which is a Read Status command addressed to Read Register R3, at address hex 83.

Each PC Card slot is assigned an address. No address space is the SMBus is specifically reserved for the power-switch integrated circuit. Should a conflict occur, pick an address that is mutually exclusive with the other devices on this particular bus.

Dan Sowin is a graduate of the University of Washington, Seattle, with BSEE and MSEE degrees. He has over 20 years of semiconductor experience in applications, marketing, and sales.

Jim Moyer has a BSEE from Rice University, Houston, Texas. He has over 20 years experience in semiconductor designs and applications, and computer design.

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SYSTEM DESIGN NEWS

A highly-integrated single-chip decode engine takes aim at applications such as standalone digital versatile disk (DVD) players, DVD on a PC, and DVD in set-top boxes. The L64020 was developed by LSI Logic Corp., Milpitas, Calif., using its CoreWare libraries, and performs all the MPEG-2 decoding and control aspects needed for DVD. Included are nine core-based functions and 45 different memory blocks that contain about 2 million transistors in all. Some of the blocks incorporated on the chip include a Dolby AC-3 surroundsound decoder, an enhanced MPEG-2 audio/video decoder, support for features such as scan and pan, and letterboxing to view wide-screen movies on a conventional screen. An integrated subpicture unit adds graphics capabilities to support functions such as movie subtitling or karaoke text. The chip will make possible a DVD console that plays back movies with home-theater quality, or bring true multimedia capabilities to a PC, or create a set-top box that integrates DVD, or implement a video-game player that incorporates DVD capability. Housed in a 160-lead PQFP, the L64020 sells for less than $45 in large quantities and will be available in production quantities by mid-1997. Contact LSI Logic at (408) 433-8000, or on the web at http://www.lsilogic.com.

Also aiming at the digital set-top box, a family of highly-integrated digital-signal processors, the TMS320AV7000 series, contains all the functions needed to decrypt, decode, and display digital video. Developed by Texas Instruments Inc. (TI), the circuits combine the CPU and transport functions along with the audio/video decompression and overlay functions, and an NTSC/PAL video encoder to directly feed a signal to a TV or other display. Also included is a memory-subsystem controller that consolidates the various memory blocks used to buffer/store video data into a single 16-Mbit synchronous DRAM. The first family member, the TMS320AV7100, integrates a 32-bit ARM Thumb RISC processor, an advanced graphics accelerator, a transport demultiplexer, conditional access and decryption modules, an MPEG-2 video decoder, an MPEG audio decoder, and an NTSC/PAL video encoder with Macrovision copy protection. By supporting multiple simultaneous and overlapping windows, the chip's graphics accelerator allows the windows to be individually displayed with up to 256 colors or true-color graphics. The transport demultiplexer and the conditional access and decryption modules are optimized for digital satellite system (DSS) requirements. An updated version of the chip, the 320AV7110, has the same functions optimized for digital video broadcast systems and supports external multiple conditional access and decryption schemes used by different service providers. The dual 16- and 32-bit nature of the ARM Thumb instruction set allows set-top box manufacturers to minimize storage space for the application software since off-chip software can be stored in 16-bit mode commands instead of 32-bit commands. Samples of the AV7100 are now available; samples of the 7110 will be ready in February. Both chips will sell for under $45 apiece in 100,000-unit quantities. Contact TI at (800) 477-8924, ext. 4500, or on the web at http://www.ti.com.

Now available in a Windows 95-compatible version, the Magic Cap communications software/utilities from General Magic Inc., Sunnyvale, Calif., provides a suite of tools that handle e-mail, faxing, and Internet access, along with features such as a personal organizer and address book. Developed to meet the electronic communication needs of the small-office/home-office user, the software places the utilities into a user-friendly interface that hides the technology—using the metaphor of the desktop with graphic images of all the often-done tasks. Bundled are features for sending/receiving faxes, tying into the Internet with a bundled version of Microsoft's Internet Explorer software, a name-card database/address book, a datebook, a filing cabinet that organizes messages and e-mails, and features to help accentuate messages—graphics, animation, and voice annotation. System requirements are a 486/33 or higher-performance platform with Windows 95, 8 Mbytes of RAM, 10 Mbytes of available disk storage, and a 14.4 kbits/s modem. Retail pricing of the software is $49. A free 30-day trial version can be downloaded from the company's web site at http://www.genmagic.com. A trial CD-ROM can be requested by calling (888) 239-4824.

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▶ **CIRCLE 661**

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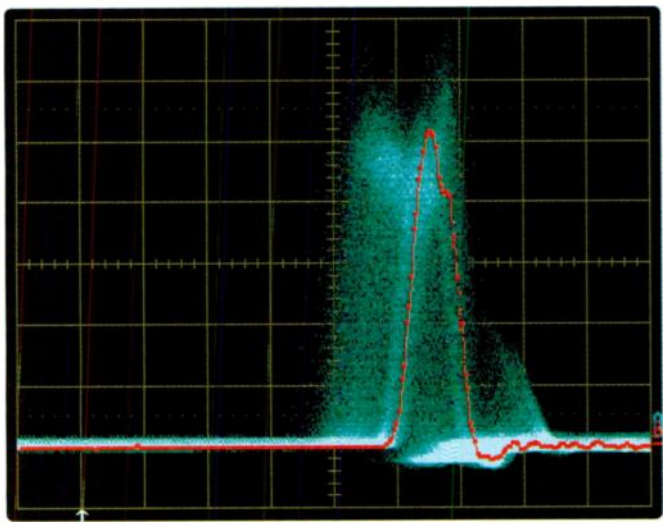

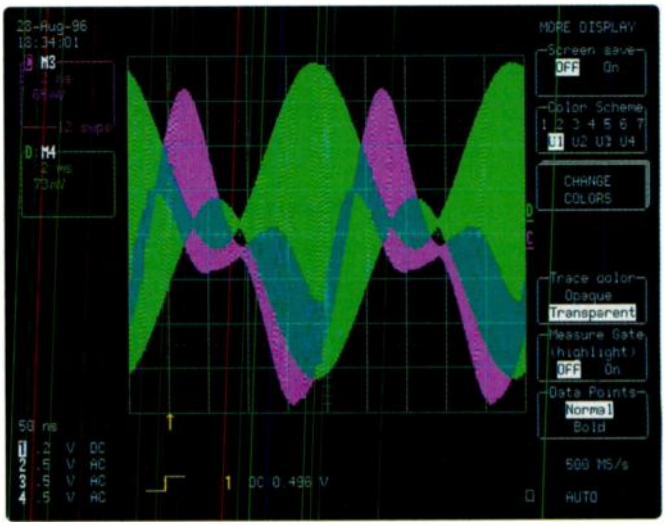

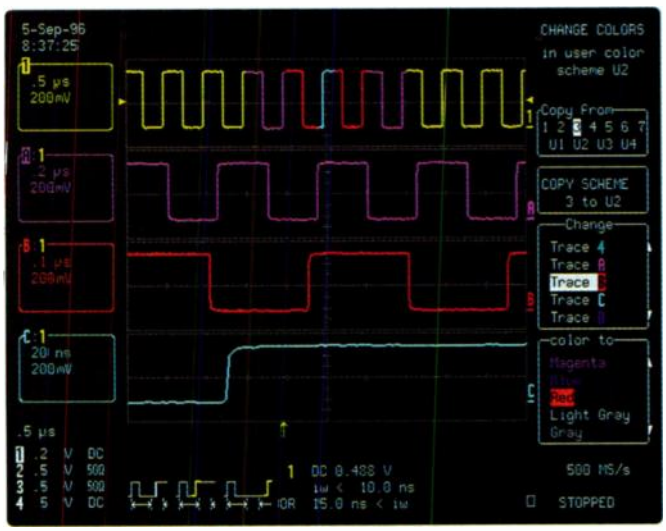

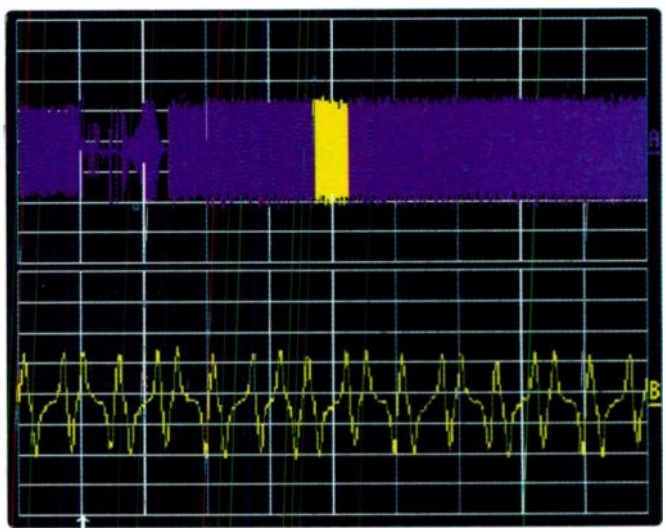

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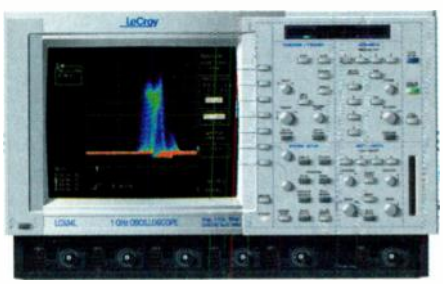

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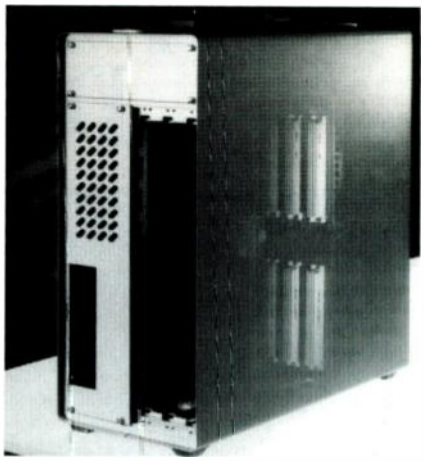
READER SERVICE 207

▼ THREE-SLOT VME CHASSIS AIDS IN DEVELOPMENT

The three-slot VMExcel VMEbus chassis can be used as a self-contained development environment or as the housing for a complete production system. The monolithic backplane is fitted with Auto Bus Grant connectors that eliminate jumper resetting when boards are inserted or removed.

The tower enclosure contains an 80/110-W power supply operating at a universal input voltage of 85 to 264 V. A removable module accepts 3.5-in. floppy- and hard-disk drives. A fan, mounted to the top-rear of the unit, draws air upwards through the active board area while pulling a separate air flow through the power supply. To maximize thermal efficiency, slot zero



is placed at the center of the unit, apart from the power supply and disk drives, separated by a full-height divider. The single-unit price for the development chassis is $1700.

VERO Electronics Inc.
1000 Sherman Ave.
Hamden, CT 06414
(203) 288-8001
http://www.vero-usa.com
▶ CIRCLE 662

▼ TOUCHPAD WORKS IN WET OR DRY ENVIRONMENTS

Increased performance, improved reliability, and reduced power consumption are the hallmarks of Interlink Electronics' latest touchpad. Built with a semiconductive technology, the touchpad employs a patented Force Sensing Resistor that uses physical touch to drive cursor positioning,

rather than the electrical capacitance of current touchpads. The semiconductive touchpad requires about 85% less power, operates in wet or dry environments, supports stylus pointing, and allows signature capture. The touchpad works with a fingertip, gloves, or a stylus. An OEM development kit is available now for $150.

Interlink Electronics Inc.
546 Flynn Rd.
Camarillo, CA 93012
(805) 484-8855
http://www.interlinkelec.com
▶ CIRCLE 663

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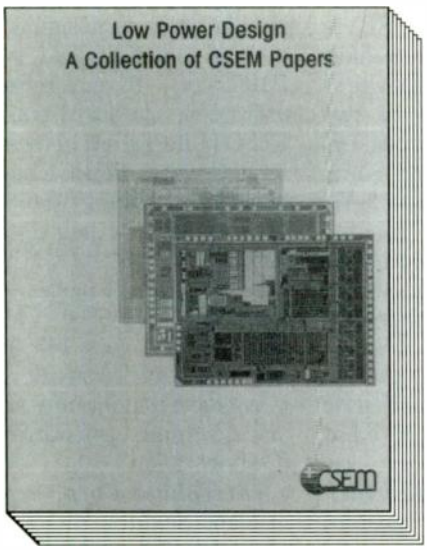

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Over the past decade, minimization of power consumption has become a critically important task in the implementation of electronics systems of all kinds, and especially for portable and battery-powered functions. The requirements for low-power will pervade systems and IC design to an ever increasing extent.

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▼ TERMINATORS REDUCE COST, IMPROVE PERFORMANCE

A pair of nine-channel SCSI terminators reduce cost while improving performance. Designated the LX5218 and LX5219, the two chips employ an adaptive nonlinear mode architecture. This eliminates the need for output capacitors, resulting in a performance boost, especially in UltraSCSI applications. Using the adaptive nonlinear mode architecture, the terminators' current acts as a complex, nonlinear function of current and voltage. The LX5218 and LX5219 are differentiated by their sleep-mode logic. The LX5218 is active-low, while active-high. The minimum operating voltage is 3.5 V. They also sink up to 60 mA of current, making them compatible with today's fast-active negation drivers. The chips are housed in 16-pin, wide-body small-outline packages or 20-pin TSSOPs. In lots of 1000, the parts sell for $2.08 each.

Linfinity Microelectronics Inc.
11861 Western Ave.
Garden Grove, CA 92841
(714) 372-8357
▶ CIRCLE 664

▼ PC SPEAKERS CONNECT TO USB

The Universal Serial Bus (USB) is used to connect the USB46 speaker system to the host PC. The speaker's three-piece design consists of two full-range shielded satellite speakers (rated at 6 W per channel) and a 4-in. long-throw subwoofer (rated at 20 W) with a frequency response ranging from 42 Hz to 20 kHz. User-interface software, which features an on-screen display, is also bundled. Other features of the USB46 include a smart automatic power-down mode and an electronic volume control. The USB46 USB-enabled speakers are priced at $149.

Altec Lansing Technologies Inc.
Routes 6 and 209
Milford, PA 18337
(800) 648-6663
http://www.altecmm.com
▶ CIRCLE 665

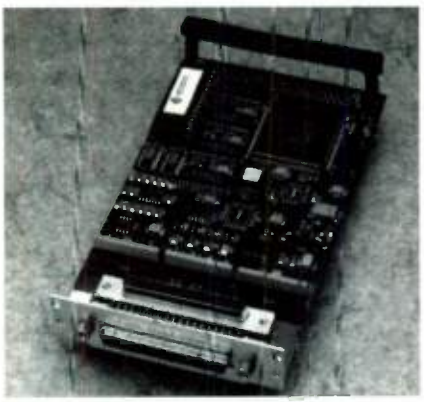
▼ BOARD CONNECTS PMCs TO VMEbus

PCI Mezzanine Cards (PMC) can be connected to the 6200 VMEbus baseboard, allowing for I/O expansion in VMEbus systems. The 6200 baseboard is a 6U VMEbus design with a PCI-to-VME64 interface and two standard PMC slots. To maximize bandwidth utilization, the board employs built-in FIFO buffers to write-post data transfers between the PCI bus and VMEbus. In addition, the 6200 offers block-transfer capability and implements a full suite of VMEbus address and data transfer modes. Available immediately, the 6200 VMEbus baseboard sells for $1395 in single quantities. A software development kit is available that includes sample UNIX drivers and software-development documentation.

Interphase Corp.
13800 Senlac
Dallas, TX 75234
(214) 654-5325
http://www.iphase.com
▶ CIRCLE 666

▼ ULTRA SCSI COMES TO THE SBus

Designed to operate with the SBus architecture, the PT-SBS450 adapter connects to Ultra SCSI peripherals. Offering a data-transfer rate of up to 40 Mbytes/s, the board operates in Ultra SCSI fast and wide modes. It's also backward compatible with older SCSI



peripherals. It supports Sun workstations running either the Solaris 2.X or Sun OS 4.1 operating system. The PT-SBS450 is built with dual processors. One is an embedded RISC processor that supervises operations, which minimizes the overhead placed on the workstation. The second CPU is an Ultra SCSI controller that runs all the SCSI commands. The dual-CPU design helps reduce interrupt latencies. The bundled software includes adaptive synchronous negotiation (ASN) to sustain 40-Mbyte/s transfer rates. The PT-SBS450 Ultra SCSI adapter is available with a single-ended or differential interface. The single-ended version sells for $1095, while the differential model costs $1145.

Performance Technologies Inc.
315 Science Pkwy.
Rochester, NY 14620
(716) 256-0200
http://www.pt.com
▶ CIRCLE 667

▼ VIDEO PROCESSOR BOARD CONTAINS DUAL DSPs

High performance and I/O flexibility are the key features of the Model 7280 Multimedia Video Processor (MVP) PCI board based on a TI TMS320C80 DSP chip. The full-length board captures and processes live video in real-time for applications such as virtual reality, videoconferencing, medical imaging, and machine vision (inspection and defection analysis). The board holds one or two 60-MHz processors. The architecture consists of twin processor cores connected to a common PCI interface. Each processor core has a C80 that's coupled to private memory and I/O resources. Up to 1.5 Gbytes/s of throughput can be achieved. The board also contains up to 16 Mbytes of DRAM, twin 2-Mbyte VRAM banks, and 512 kbytes of flash memory. The processors access private I/O through the serial access port of the VRAM banks. In addition, each processor can connect to a 16-bit daughterboard control interface. The Model 7280 MVP board costs $5295.

Pentek Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818-5900, ext. 720
http://www.pentek.com
▶ CIRCLE 668

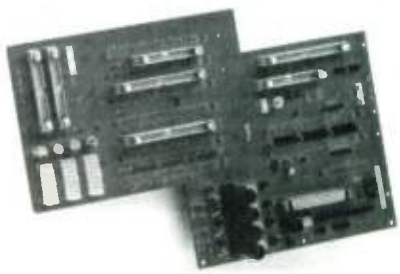
▼ PRML READ-CHANNEL ICs TRANSFER 240 MBITS/S

A pair of PRML read-channel ICs, the 32P4935 and 32P4937, are capable of data rates of 125 and 140 Mbits/s, respectively. Both are pin-compatible with previous-generation parts. The parts employ a completely analog method for Viterbi detection, which eliminates the need for an analog-to-digital converter and DSP techniques to convert the analog read-channel stream to a valid digital data stream. The result is faster performance. Other features include thermal asperity detection and correction which reduces errors caused by head-to-disk contact and the resulting heating offsets in the MR-head output. Prices, in lots of 1000, are $15 for the 32P4935 and $16 for the 32P4937.

Silicon Systems Inc.
14351 Myford Rd.
Tustin, CA 92780
(800) 624-8999, ext. 151
http://www.ssi1.com
▶ CIRCLE 669

▼ VME BACKPLANE HOLDS TWO SLOTS

The latest VMEbus backplane from Electronic Solutions features a two-slot, eight-layer architecture. Also integrated into the backplane are SCSI connectors, fuses, control LEDs, a test connector, a temperature sensor, and reset logic. It is built with automatic



daisy-chain circuitry and proprietary high-current-feed power connectors. Suitable applications include point-of-sale platforms. The dual-slot backplane is available immediately.

Electronic Solutions
6790 Flanders Dr.
San Diego, CA 92121
(800) 854-7086 or
(619) 452-9333
▶ CIRCLE 670

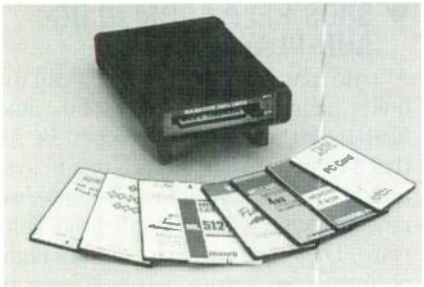
▼ CD-ROM DRIVE OFFERS A 12X SPIN RATE

The latest CD-ROM drives are spinning at 12X the standard rate. The FX120 is no exception. The high spin rate produces a data-transfer rate 1.8 Mbits/s and an average seek time of 130 ms. Performance is further improved thanks to the 256-kbyte cache buffer. The connection to the host platform is made through an ATAPI interface. The drive, which fits a standard half-height form factor, can be mounted either horizontally or vertically. The patented tray assembly holds the disk in place. The FX120 supports DMA transfers and the CD Plus and CD-I disk formats. Available now, the drive sells for $249.

Mitsumi Electronics Corp.
6210 North Beltline Rd., Suite 170
Irving, TX 75063
(214) 550-7300
▶ CIRCLE 671

▼ EXTERNAL DRIVE WORKS WITH PC CARDS

Designed as an add-on to notebook, palm-top, and pen-based computers, the IC Card Drive reads and writes to and from SRAM-based memory card. It supports flash, one-time-programmable, and UV-EPROM cards from most major manufacturers. The device, which complies with PCMCIA and JEIDA standards, can be used for memory-card duplication. The IC Card Drive connects to the host system through a serial or parallel interface. A 6-ft. serial cable is bundled with the 15-oz. drive. Automatic baud-rate selection is available from 1200 to 115,200 baud. Available now, it sells for $795.



Logical Devices Inc.
130 Capital Dr.
Golden, CO 80401
(800) 315-7766, ext. 202
http://www.logicaldevices.com
▶ CIRCLE 672

▼ PROCESSOR SIMPLIFIES PEN INPUT

Designers can build systems with a low-cost pen interface using the TR88802CS Pen Input Processor. The chip integrates all pen-input tasks into one device, including drivers for the digitizer tablet. It executes all of the signal processing and coordinate calculations required to supply pen-positioning data at 200 coordinates pairs/s. The chip contains all the analog circuitry necessary to drive the X-Y resistive planes, sense the relative voltages, and calculate the coordinates. In addition, the device incorporates the pen-detection circuitry needed for handwriting recognition. It also contains power-manangement modes. To detect the X-coordinate position, the chip applies a current to the X-plane resistive film and senses the voltage picked up by the Y-plane resistive film. This voltage is sensed by the processor, which is then used to calculate position. Working at 5 V, the TR88802CS has a standby current of less than 10 microA. Two versions of the processor are available. In a 28-pin SO package, the chip sells for $3.25. In a 16-pin serial-only configuration, the part costs $2.75.

TriTech Microelectronics
2290 North First St., Suite 204
San Jose, CA 95131
(408) 894-1900
▶ CIRCLE 673

▼ HARD-DISK CONTROLLER SUPPORTS ULTRA2 SCSI

Ultra2 SCSI support is built into the SYM201F40 hard-disk controller. What's the big deal, you ask? That means that the part supplies an 80-Mbyte/s transfer rate, a 160-Mbyte/s burst buffer bandwidth, and a 40-Mbyte/s disk transfer rate. The chip comprises a SCSI protocol controller, a host DMA and multi-context engine, a buffer manager, a disk formatter, error correction, and a microprocessor interface. Because each block is built with a central core methodology, integration with additional logic is simplified. Such external logic could include a microprocessor, embedded memory, servo and spin function, or an ASIC. The SYM201F40 supports greater device connectivity and longer cable lengths using the Low-Voltage Differential (LVD) technology. This permits tranfers over distances that previously required differential SCSI and external transceivers. Backward compatibility lets users switch bwteen LVD and single-ended modes. It also allows for use with previous generations of SCSI peripherals. The processor interface supports a standard RISC interface, including parts from Hitachi, Intel, Motorola, and Texas Instruments. The chip is housed in 144- and 176-pin TQFPs. Samples are available now, with production volumes coming shortly. A firmware development system, including a disk emulator, is also available.

Symbios Logic Inc.
2001 Danfield Ct.
Fort Collins, CO 80525
(800) 856-3093
http://symbios.com
▶ CIRCLE 674

▼ AUDIO MOVES TO THE PCI BUS

Mainstream PCs can be transformed into audio-enabled PCs using the Sonic Vibes audio processor. The single-chip device audio processor moves the audio acceleration from the ISA bus to the PCI bus for increased performance, while offering backward compatibility with the ISA bus. The part also adds wavetable synthesis to the motherboard. In addition, by supporting Microsoft's DirectMusic API, the part supplies an unlimited sound palette. Previously, sounds were stored in ROM, which allowed 128 general instruments. Now, those sounds can be stored in RAM, enabling the palette to be expanded. Available now in a 160-pin PQFP, the Sonic Vibes audio accelerator sells for $30 each in lots of 10,000.

S3 Inc.
2770 San Tomas Expwy.
Santa Clara, CA 95051
(408) 980-5400
▶ CIRCLE 675

▼ SBCS HELP FORM PLUG-AND-PLAY SERVERS

A true plug-and-play system can be built using the MSB133P0 and MSB166P0 single-board computers. All that's required to build a complete system is the SBC, Windows NT, internal modems, and Citrix WinFrame software. The resulting system offers high-performance remote access for up to eight concurrent users. Based on a Pentium microprocessor running at 133 or 166 MHz, the boards support up to 128 Mbytes of DRAM, 572 kbytes of cache memory, and 1 Mbyte of memory that's dedicated to the PCI-based graphics. The boards are compatible with Windows 3.1 and NT, DOS, OS/2, and Unix.

Multi-Tech Systems Inc.
2205 Woodale Dr.
Mounds View, MN 55112
(800) 328-9717 or
(612) 785-3500
http://www.multitech.com
▶ CIRCLE 676

▼ PC GRAPHICS ACCELERATOR TOUTS THE HIGH END

Based on the S3 Virge/VX graphics accelerator chip, the 9FX Reality 772 64-bit accelerator board handles video and 2D and 3D graphics. Aimed at the high end, the VRAM-based board comes with either 2 or 4 Mbytes. The board's 3D rendering capabilities include hardware texture mapping with perspective correction, bilinear filtering, 16-bit Z buffering, alpha blending, fogging, and support for compressed texture formats. It's also built with support for Microsoft's DirectX APIs, which include DirectDraw, Direct3D, and ActiveMovie. For video playback, the 9FX Reality 772 employs on-board color interpolation and X-Y video scaling for full-screen video playback at 30 frames/s. Available now, the 2-Mbyte version costs $199, while the 4-Mbyte model sells for $279. A 2-Mbyte upgrade costs $99.

Number Nine
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Lexington, MA 02173
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A SPECIAL EDITORIAL FEATURE

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ELECTRONIC DESIGN

So, You Want To Convert To An MCM?...

Proper planning, early in the design, can make for a relatively painless implementation process.

JEFF POWELL, SCOTT BECHTEL, and BRIAN DURWOOD

Maxtek Components Corp., 13335 SW Terman Rd., P.O. Box 428, Beaverton, OR 97075-0428; (503) 627-4133; e-mail technology@maxtek.com

For many years, multichip modules (MCMs) and hybrid circuits have been relegated to the military and other high-end applications for which they were originally designed, due to their complexity and subsequent high cost. Fortunately, recent advances in materials and processes have lowered the cost of MCMs to the extent that they are now a viable alternative in mainstream applications. However, a discrete solution is still less expensive, and in this extremely competitive environment, the decision to go with MCMs must not be taken lightly. Once the decision has fallen in favor of a full- or part-MCM implementation, steps can be taken in the early stages to make the process go smoothly.

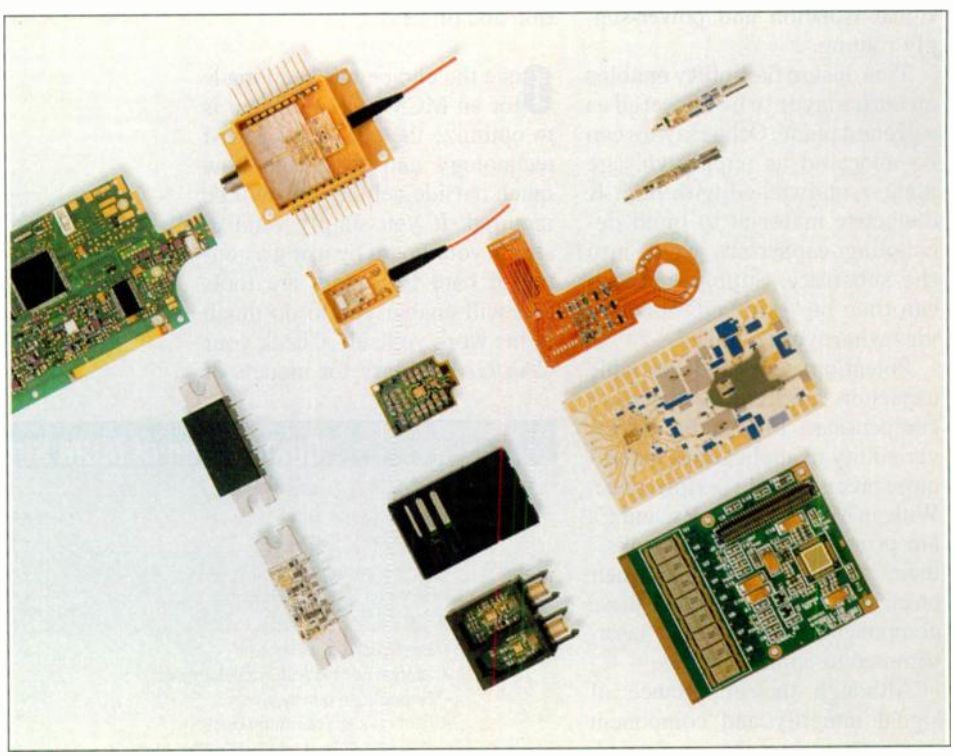
1. Advances in MCM and hybrid-circuit manufacturing have made these modules smaller, lighter, faster, and less expensive. These improvements have been the impetus behind the rapid deployment of MCMs from military and other high-end applications into mainstream applications in recent years.

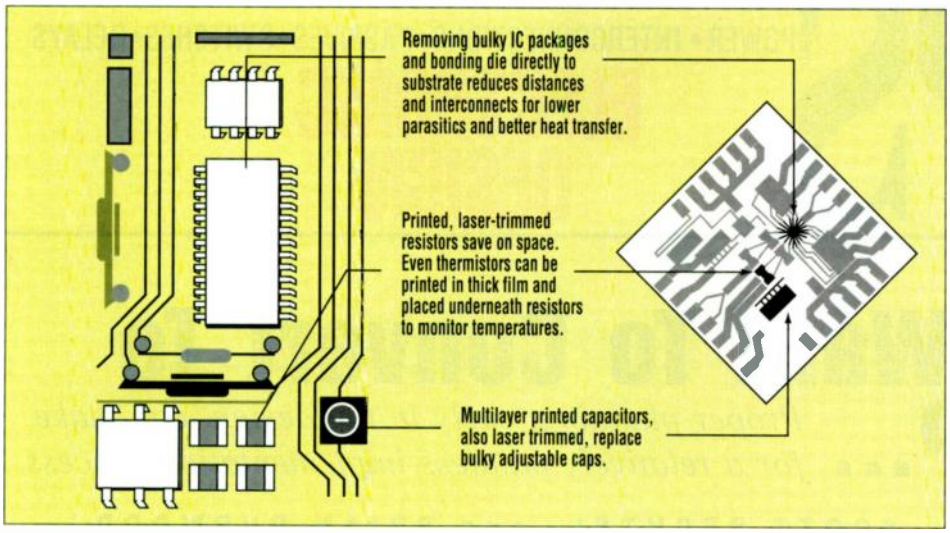
The advances in MCM technology have been numerous and wide-ranging. In addition to MCM-C chip-and-wire assembly onto ceramic substrates, it is now possible to wirebond to special low-dielectric-constant pc boards, giving improved high-frequency performance together with a reduction in material cost. Bare-die protection provided by relatively expensive ceramic covers can be replaced by a "glob" of special epoxy. Both chip-and-wire and solder assembly can be combined on one substrate, allowing components such as relays to be combined in close proximity with conventional miniature components in a single economical package. CAD layout and simulation tools also have greatly contributed to lower development costs.

All these advances have made MCMs and hybrid circuit modules smaller, lighter, and faster, and have made thick-film, thin-film, and cofired ceramic mature substrate technologies. Such improvements have supported the rapid deployment of MCMs into mainstream applications in recent years *(Fig. 1)*.

Despite the availability of the technology, it is still more expensive than a discrete solution, and comes with many nonrecurring development costs. Consequently, the decision to move to an MCM requires the designer to conduct a thorough evaluation of product requirements.

Given these concerns, when should you consider an MCM? Usually, the compelling reasons are performance, reliability, thermal management (e.g. power dissipation), and density. With respect to performance and





2. Eliminating subcomponent packages and replacing manually-adjustable elements (R, C, or L) with laser-trimmable components reduces parasitics, improving high-frequency performance.

reliability, eliminating subcomponent packages, providing short(er) signal and power runs, and replacing manually-adjustable elements (R, C, or L) with laser-trimmable components reduces parasitics at frequencies from as low as 100 MHz *(Fig. 2)*. Controlled-impedance transmission lines and multiple-plane layouts provide each IC with a direct voltage supply. This improved signal-path integrity and power-supply decoupling results in less noise, less ringing, and fewer oscillations in critical high-speed circuits *(Fig. 3)*. The multiplane layouts also provide flexibility in signal isolation and power-supply routing.

This design flexibility enables an entire layer to be allocated as a ground plane. Other layers can be allocated as supply-voltage planes sandwiched with high-K dielectric material to build decoupling capacitors right into the substrate. Supply voltages can then be "grabbed" through vias wherever required.

Potentiometers and variable capacitors are frequently used to compensate for active-device variability in applications that require precise circuit performance. With an MCM, the Ls, Rs, and Cs are printed in thick-film "inks," their shape determining their electrical value. During test, these components may be laser-trimmed to optimal values.

Although the importance of signal integrity and component accuracy cannot be overstated, heat dissipation is becoming increasingly problematic as power densities continue their upward spiral. MCMs can control and remove heat more easily than packaged ICs, as it is possible to mount the bare die directly to a ceramic substrate that has lower thermal resistance than a pc board. In some of Maxtek's more advanced module designs, the substrate has a cutout, enabling the IC to be directly mounted to an integral heat sink, yet still be wirebonded to the ceramic or organic substrate. Higher thermal conductivity can reduce thermally induced low-frequency effects (thermal distortion and offsets).

Once the choice has been made for an MCM, the next step is to optimize the circuit for MCM technology and to decide how much outside help, if any, will be required. If you simply want to shrink your board by using a couple of bare ICs, there are tools that will enable you to do much of the work yourself. Check your CAE/CAD library for models of the bare-die equivalent of your components, and for the required interconnection rules. A simple board often can be assembled fairly inexpensively. If there are performance questions or more complex issues, it may be best to consult with an MCM design house.

You should not be intimidated by this exercise—MCM's are not that "exotic." But you must have realistic expectations. You probably won't be able to reduce size, increase speed, and lower cost all at once, so you must get your priorities straight. Finally, pick a supplier whose focus matches your needs. MCM houses can be roughly classified as either Level 1, 2, or 3, with each having their advantages and disadvantages *(see the Table)*.

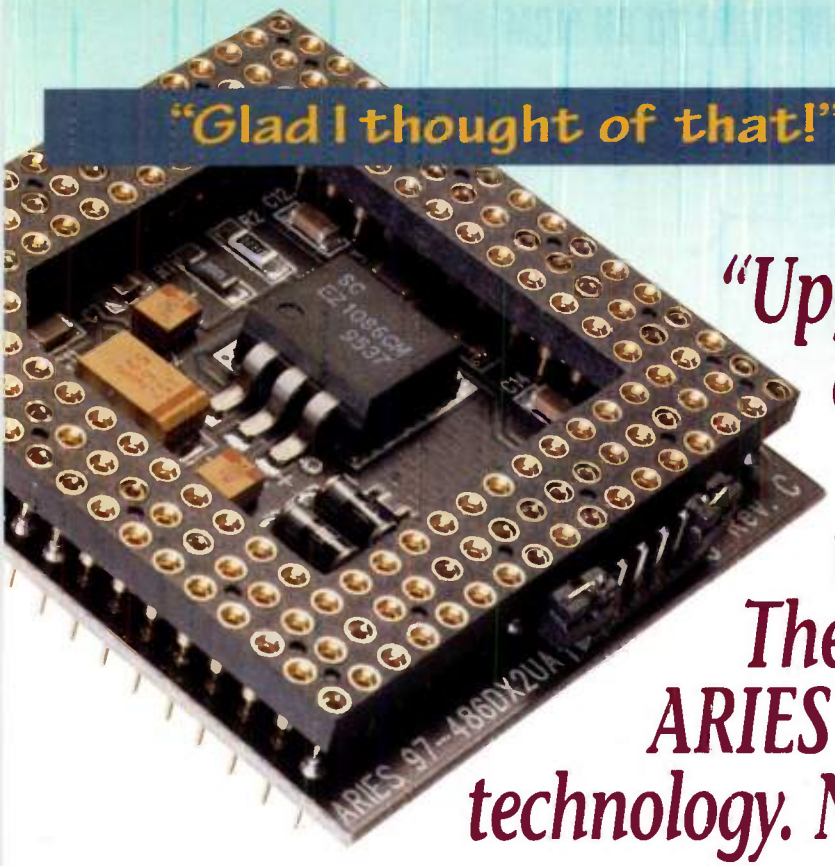
Level 1: A typical prototype shop or build-to-print subcontractor with limited assembly process capabilities, specializing in assembling to a print. At this level, networks/substrates are usually purchased and there will be no design expertise and limited test capability.

Level 2: Has some in-house layout and network fabrication (usually one or two types only). It should offer a broader selection of processes to chose from and have a formal quality system in place.

Level 3: Offers a broad line of technologies with full electrical and mechanical design services. It can assist in substrate/network specification, can modify schematics for lower cost and improved performance/yields, and can partition and design ASICs for cost reduction as volumes in-

Comparison of MCM Supply Houses

Level	Benefits	Risks
Level 1	• May be quick turn • Attention to customer	• Yield loss/catastrophe • Poor repeatability
Level 2	• More complete service level • Requires less hand holding	• Limited range of technologies • Unable to fix electrical problems or parametric shifts
Level 3	• Best chance of success • Stands behind ASIC development • Repeatable quality levels • Can handle volume production requirements in a cost-effective manner	• Very low risk



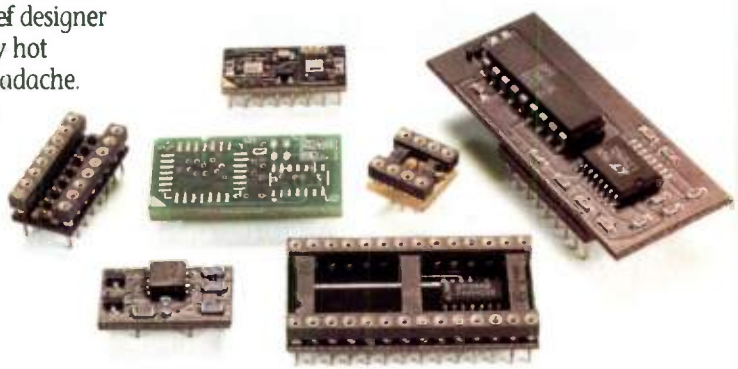
"Upgrading boards already in production used to be a nightmare. Then I discovered ARIES Correct-A-Chip™ technology. Now it's a dream."

THE PROBLEM

"Things change fast in this business...too fast, sometimes. Just when I'd get a new board into production, my phone would ring. The chief designer just had a vision! The boards must change!...we had some pretty hot discussions, let me tell you. *They* had a new toy – *I* had a new headache.

THE SOLUTION

"A friend at another company told me she used to have the same problem, and solved it with Aries Correct-A-Chip technology. She said Aries could let me change from through-hole to SMT, work with any kind of footprint, even crank up performance in the same board space. And she was right! Those design changes don't bother me anymore. In fact, now that I'm plugged into Correct-A-Chip, I sleep like a baby. Thanks, Aries!"



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e-mail: info@arieselec.com

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ISO 9002 CERTIFIED

THE PROOF

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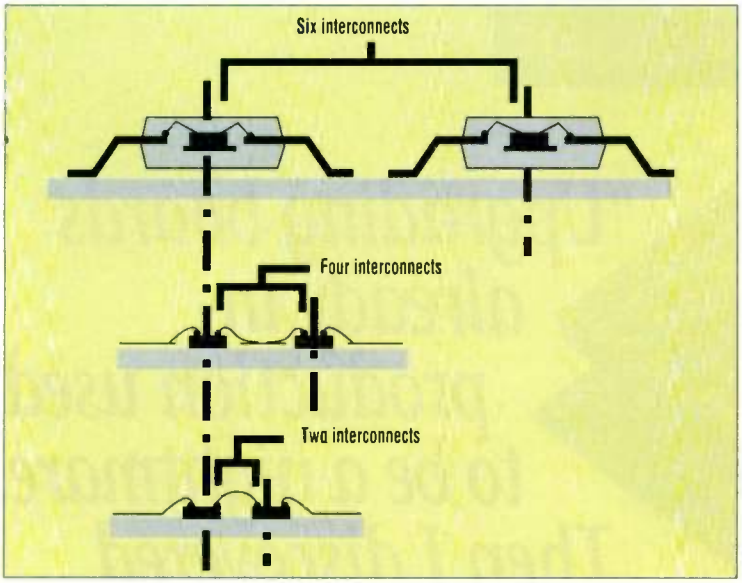
READER SERVICE 91



3. Shorter runs and fewer interconnects improve signal-path integrity, resulting in less noise, less ringing, and fewer oscillations in critical high-speed circuits.

crease. This supplier is typically ISO 9001 approved, with an established formal quality system, and is often part of a larger organization with strong funding.

The first step toward implementing an MCM is to optimize circuit partitioning, taking into account availability of components in microminiature form, ease of testing, power density, and thermal considerations. It is important to divide the circuit into functional blocks, which also will reduce the number of I/O pins required. Most suppliers will assist in circuit partitioning, optimizing the number and type of devices that go into the MCM. Many suppliers will provide you with their design rules (often similar, but ultimately unique for each house) so you can initiate your design. The design rules should list all relevant material characteristics, especially at high frequencies, to help you choose the appropriate technology. There also should be guidelines for thermal management, various package styles, and how to proceed to the second step, which is the choice of technology *(Fig. 4)*.

The design process is typically iterative—the supplier will expect to help with partitioning and circuit design, and take the lead on the rest, with respect to ASIC design, thermal analysis, electrical simulation, design for manufacturability, design for testability, process development (if required), manufacturing, and ac test. Along the way you'll need to make decisions. What means of

GLOSSARY OF TERMS

Following is a glossary of various terms that were used in the main text of this article on MCMs.

(Active) Laser trim: As part of the manufacturing process, the MCM is locked into a measurement fixture and printed resistors, capacitors, or inductors are trimmed with a laser to achieve specific parameters.

COCOF: Chip-on-ceramic-on-flex. Small thick- or thin-film or LTCC ceramic substrates attached to a flex circuit.

COF: Chip-on-flex. As above, but with a flexible substrate. Provides for some innovative packaging solutions.

Etched thick film: As above, but with an interim photomask process used to apply a UV-sensitive material that enables finer lines, spacing, and sharper-edged traces to be etched.

Glob top: Hysol (or similar potting compound) used to cover a die to provide environmental protection.

Hermetic: Air and water tight (measured by helium leak rate) to various degrees. Typically a welded package.

HTCC: High-temperature cofired ceramic-laminate substrate using refractory metals. May have embedded passives and carry a cost premium.

KGD: Known-good die—typically bumped and fixtured in order to test to ac parameters before use. May be tested at temperature or burned-in. May have significant cost premium.

Lines and spaces: Typically used as a measure of the capability of a specific MCM technology. Thick film may be capable of 5-mils between lines and 5-mil-wide lines, where etched thick film can bring this down to 3-mils. Smaller lines equate higher frequencies and packaging densities.

LTCC: Low-temperature cofired ceramic able to use conductive metals because of lower firing temperature. Typically lower development cost but higher materials cost than HTCC due to higher precious metals content.

MCM-C: Ceramic.

MCM-D: Deposition (thin-film).

MCM-L: Laminate (pc board such as FR-4, GETK, Polyimide).

Si-on-Si: Silicon on silicon where die is connected to a silicon "substrate."

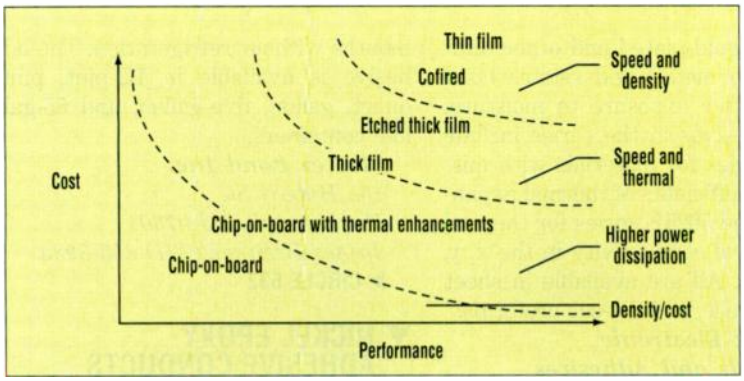
TGD: Tested-good die—typically tested and inked at the wafer level to provide assurance of functionality as a discrete device.

Thermal via: Column(s) of stacked vias filled with thermally conductive material, sometimes gold, for the purpose of moving heat from the die to the outside of the package (or to a heat sink).

Thick film: Pastes (inks) applied to a ceramic substrate via a sophisticated precision variant of silk screening (e.g. steel mesh screens).

Thin film: Sputtering-type deposition of gold, nichrome, or comparable materials on ceramic substrate.

Via: Vertical interconnection to go from one routing layer to another. Through vias or stacked vias cross multiple layers and bring vias can start and stop at specific layers, leaving room above and below for additional routing.



4. The choice of technology to use for the MCM package depends on a number of factors, including cost, performance requirements, speed, and heat dissipation.

thermal dissipation will work best with your overall system? There are choices from thermal vias all the way up to direct die mount on heat spreader, and even water or freon cooling. What type of packaging, interconnect, and sealing fits with your system? Package choices range from globbed chip-on-board to z-axis compression connectors to hermetically-sealed gull-wing packages. The resulting MCM should be one that your manufacturing equipment can handle as if it were a normal component.

Engineers can save on costs by working with their provider for partitioning, specifying packaged parts where possible and providing reasonable forecasts.

Simple MCMs resemble pc boards and may be tested for dc functionality and basic IPC rules; however, complex MCMs are often full subsystems with their own high-frequency, high-temperature, and packaging problems. In-line tests reduce costs by identifying problems before final lidding so that rework or component replacement can increase module yield. Final ac testing ensures that the entire MCM performs as if it were just another component. Be prepared to write or collaborate on a test specification, and make sure that your MCM house has the testing capability you need.

As your design evolves, the MCM evolves in multiple directions. Density may increase by converting circuitry to an ASIC. Cost can decrease by changing to less expensive materials. Speed often increases just by getting smarter about the design. For example, you might begin with a discrete-based thick-film MCM, and ultimately evolve to a chip-on-board MCM with more of the circuitry integrated on ASICs and the power dissipation handled by die mounted through board cutouts to directly contact a heat spreader.

As previously mentioned, MCMs are expected to be more costly than their traditional discrete counterparts. These additional costs are generated for three main reasons: An MCM adds a production step; an MCM adds material in the form of a substrate, a cover, or other packaging; and an MCM uses bare die, which in many cases costs more than the equivalent packaged device (due to lower volumes and special tests required in die form).

A rule of thumb to estimate the MCM cost is to take a multiple of your bill of materials (BOM):

1.3x: chip-on-board, high volume, minimal test.

1.5x: simple thick-film MCM.

1.8x: complex thick-film MCM with enhanced thermal capabilities and actively trimmed passives.

2.0x: as above but with extra processing, such as etched thick film or special RF shielding.

3.0x:—thin-film MCM.

4.0x:—hermetic, military style hybrids with burn-in.

But there are some cost savings to be considered if you intend to compare the cost of an MCM with its discrete equivalent. Due to the (sometimes considerable) space savings resulting from the use of an MCM, the size of the pc board and the ultimate product containing the MCM will be correspondingly smaller. This may be a significant cost saving if the pc board is a fine-line multilayer type. Also, the MCM is a fully tested functional block, saving some testing/rework at the pc-board stage. And there is only one component to purchase, stock and insert in the pc board in place of perhaps a hundred discretes. In other words, consider the total system cost when evaluating the cost impact of an MCM, rather than just the sum of the discrete parts involved.

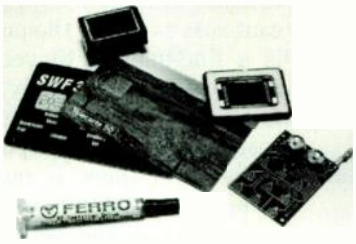
MCMs can be economical with volumes in the low thousands if they contain $50 to $200 worth of circuitry (use the above multiple as a divider to get to your BOM equivalent—but remember to take into account the ancillary savings resulting from smaller packages). This would pay for a double-sided thick-film circuit with laser-trimmed passives. On the other end of the scale, MCMs make sense again when you get into the hundreds of thousands: automotive circuits such as control systems or datacom building blocks like fiber-optic transceivers, executed on printed circuit boards or flex with "glob top" environmental sealing.□

Jeff Powell is a 30-year veteran of Tektronix with extensive experience in all aspects of hybrid and MCM technology.
Scott Bechtel is a 15-year veteran of the hybrid industry with experience in large, high-density military and industrial MCMs.
Brian Durwood has over 12 years in high technology, working with startup companies and programs from CAE software to high-frequency analog hardware. He is responsible for Business Development at Maxtek.

The authors wish to thank Mal Gilbert for his assistance.

▼ ONE-PART ADHESIVE IS CONDUCTIVE

Designed for the attachment of microtech silicon, 4FS1020 one-part silver adhesive provides long shelf life,



no bleed through, and low stress over a wide temperature range. The thermally and electrically conducting epoxy adhesive has low voiding upon cure and excellent adhesion to a variety of substrates.

Ferro Corp.
1621 S. Rancho Santa Fe Rd.
San Marcos, CA 92069
Vern Stygar (619) 591-3190
Fax (619) 591-0684
stygarv@ferro.com
▶ **CIRCLE 630**

▼ ADHESIVE BONDS TO GOLD SURFACES

The 550-series adhesive film is designed for gold-plated and other difficult-to-bond metals and retains bond strength after exposure to moisture. Other adhesives in the series include the 561 series for materials with mismatched coefficients of thermal expansion, and the 5025E series for thermal and electrical conductivity in the x, y, and z axes. All are available in sheet stock, slit rolls, and die-cut preforms.

Ablestik Electronic Materials and Adhesives
20021 Susana Rd.
Rancho Dominguez, CA 90221
Jilla Senkbeil (310) 764-4600
▶ **CIRCLE 631**

▼ ONE-STEP ADHESIVE IS RUGGED

The Supreme 10HT single-component structural adhesive has a temperature tolerance of -320° to 400°F, along with high peel and shear strength. Typical aluminum-to-aluminum bond strengths exceed 3,000 psi in lap shear and 30 pli in T-peel. The adhesive also has high resistance to mechanical vibration, impact, and shock, and has excellent adhesion to similar and dissimilar substrates. Curing occurs readily above 250°F and the shelf life is up to three months without refrigeration. The adhesive is available in 1/2-pint, pint, quart, gallon, five-gallon, and 55-gallon containers.

Master Bond Inc.
154 Hobart St.
Hackensack, NJ 07601
James Brenner (201) 343-8983
▶ **CIRCLE 632**

▼ NICKEL EPOXY ADHESIVE CONDUCTS

TRA-DUCT 2701 conductive nickel epoxy adhesive is an electrically conductive nickel-filled epoxy adhesive recommended for electronic bonding, sealing, and EMI/RFI shielding applications. The two-part paste is free of solvents, silver, copper, or carbon additives and bonds dissimilar materials such as metals, ceramics, glass and plastic laminates. The adhesive cures at room temperature and can be used for bonding and shielding heat-sensitive components.

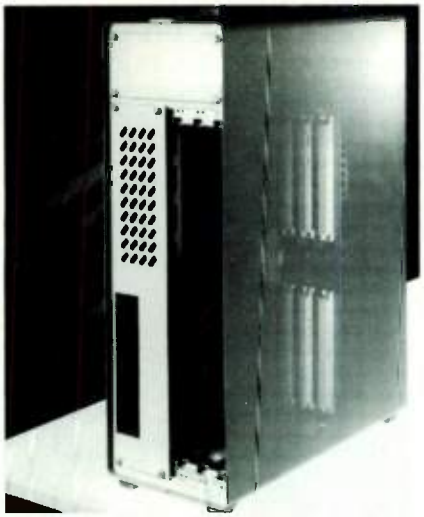
TRA-CON
45 Wiggins Ave.
Bedford, MA 01730
(508) 667-3805
Fax (617) 275-9249
▶ **CIRCLE 633**

MANUFACTURERS OF ADHESIVES

Manufacturer	Adhesion (lb/in^2)	Dispensible?	Shelf life	Printable?	Humidity resistance	Pot life	Curing temperature	Color change during cure?	Optically visible (human or machine)
Acheson Colloids Company **Ontario, California** **Tom Adcoch** **(800) 270-2228** **http://www.achesonindustries.com** **CIRCLE 490**	1000	Yes	Three months at 25°C	Yes	Yes	Greater than 8 hours	270°F	No	Both
Ablestik Electronic Materials and Adhesives **Rancho Dominguez, CA** **Paul Sauer** **(310) 761-1374** **CIRCLE 491**	5000 to 6500	Yes	One year at -40°C	Yes	N/A	Two weeks	150°C	N/A	No
Aremco Products Inc. **Ossining, NY** **Peter Schwartz** **(914) 762-0685** **CIRCLE 492**	2000	Yes	12 months	Yes	Good	One to 48 hours	200°C	No	No
Chomerics **Div. of Parker Hannifin Corp.** **Woburn, MA** **Steven Thornton** **(617) 939-4340** **CIRCLE 493**	650 to 1400	Yes, syringe, silk screening	Nine months	Yes	Excellent	30 min	Room temperature for 24 hours or up to 240°F for 15 min	No	Both
Grace Specialty Polymers **Lexington, MA** **Technical Service** **(617) 861-6600** **CIRCLE 494**	800 to 5000	Yes	Several months to one year	Yes	Yes	Hours to several days	25° to 150°C depending on product and end properties	No	Both

▼ 3-SLOT VMEbus CHASSIS IS EMC SCREENED

This three-slot VMEbus development chassis can be used as a self-contained EMC-screened development environment or as the housing for the complete production status system. The desktop tower enclosure comes with an 80/110-W power supply with an 85- to 264-V universal input. The VMExcel monolithic backplane is fitted with Auto Bus Grant connectors to eliminate resetting of the jumpers when boards are inserted or withdrawn. A separate removable module accepts 3-1/2-in. floppy and hard drives and a top-rear-mounted fan draws cool air up through th active board area. The J2 area at the rear of the backplane is fully accessible for I/O configuration. Pricing is $1700 and delivery is two to four weeks ARO.



VERO Electronics Inc.
1000 Sherman Ave.
Hamden, CT 06514
Christal Czaja (800) 642-VERO
http://www.vero-usa.com
▶ CIRCLE 634

▼ ADHESIVES CURE USING UV LIGHT

The NEA 123L, 123M, and 123K are single-component adhesives which form a tough, resilient polymer in seconds when exposed to UV light the range of 320 to 380 nm. All three bond to plastic, metal, and wires. The NEA 123L has a viscosity range of 6000 to 8000 cps, NEA 123M has a viscosity of 12,000 to 15,000cps, while

NEA 123K has a viscosity range of 80,000 to 100,000 cps.

Norland Products Inc.
PO Box 7145
North Brunswick, NJ 08902
(908) 545-7828
Fax (908) 545-9542
▶ CIRCLE 635

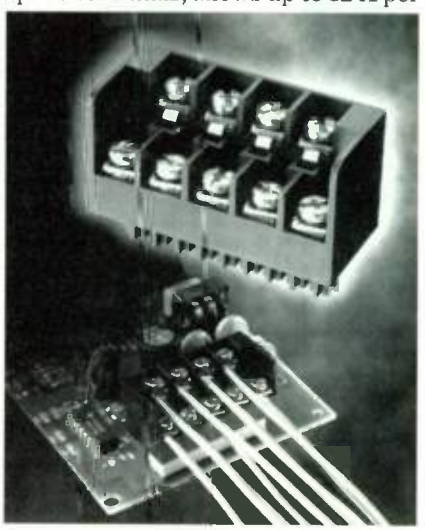
MANUFACTURERS OF ADHESIVES

Manufacturer	Adhesion (lb/in^2)	Dispensible?	Shelf life	Printable?	Humidity resistance	Pot life	Curing temperature	Color change during cure?	Optically visible (human or machine)
Heraeus W.Conshohocken, PA Christina Kistler (610) 825-6050 CIRCLE 495	Greater than 95	Yes	Six months	Yes	Yes	Three to five days	From 125°C for two min to 180°C for 60 s	No	Both
Instrument Specialties Co. Inc. Delaware Water Gap, PA Stephanie Arnold (717) 424-8510 ext.102 http://www.instrumentspecialties.com CIRCLE 496	4.0	Yes	Six months	Yes (with modification)	Excellent, after full cure	N/A	Room temperature	No	Both
Loctite Corp. Rocky Hill, CT Sales Dept. 800-LOCTITE CIRCLE 497	3400	Yes, either syringe, stencil print, or pin transfer	Nine months	Yes	Yes	Five days to one month	60 to 90 s at 150°C	No	Both
Master Bond Inc. Hackensack, NJ Robert Michaels (201) 343-8983 CIRCLE 498	Greater than 2000	Yes	Six months	Yes	Excellent	One to two hours	Room temperature to 250°F	None	Both
Multi-Seals Inc. Manchester, CT Ken Harvill (860) 643-7188 http://www.multiseals.com/users/mseals CIRCLE 499	800 to 2000	Yes, automated loading	One year	Yes	Yes, after cure	N/A	300°F for 15 min	No	Both
Quantum Materials Inc. San Diego, CA Anne Wojskowicz (619) 695-1716 CIRCLE 500	800 to 1500	Yes	One year at -40°C	No	Very good	48 hours	100° to 240°C	None	Both

PACKAGING

▼ TERMINAL BLOCK IS WIDELY COMPATIBLE

The EuroMate Series 93 terminal block is fully interchangeable with Eurostyle plugs and can withstand in excess of 10 in-lb of torque. The device accepts 1/4-in. OD wire lugs or spade terminals, allows up to 12 A per



line in a 3.81-mm spacing, and uses beryllium-copper contacts. Available with three to twenty poles with 0.150-in. centers, the EuroMate accepts wires from 14 to 30 AWG and has an operating temperature range of -35° to 105°C. The body is made from black polyamide UL 94V-O-compatible plastic. Pricing is $0.35 ea/contact in 1,000-piece quantities and delivery is four weeks ARO.

Beau Interconnect Systems
4 Aviation Dr.
Gilford, NH 03246
Brian Davies (603) 524-5102
Fax (603) 524-1627
▶ CIRCLE 825

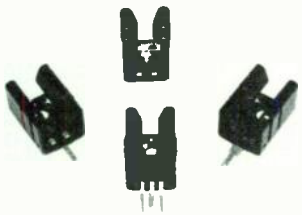
▼ 30-MM FAN COOLS NOTEBOOKS

The 1204KL Boxer Series cooling fan measures 30 by 30 by 10 mm and is designed for spot cooling of microprocessors and other devices. The fan runs off 6- to 13.8-V dc, provides up to 4 CFM of free-air performance, and weighs 8.5 g. A ball-bearing design ensures quiet operation. Pricing is from $8 to $10 in quantity.

NMB Technologies Inc.
9730 Independence Ave.
Chatsworth, CA 91311
Susan Shippey (818) 341-3355
Fax (818) 341-8207
sshippey@nmbtech.com
▶ CIRCLE 826

▼ HEATSINK CLIPS ONTO TO-220 COMPONENTS

Part of the company's Board-Level Stamped Products Heat Sink line, the 230 Series is a compact, slim, wavesoldreable, low-profile heatsink with self-locking features. Designed



for use with TO-220 semiconductors, the 230 Series provides a unique integral clip design that fastens the heatsink to the component. The clip ensures uniform force is applied to the component for effective and maximum thermal contact in horizontal or vertical mounting positions. Aboveboard heights for the heatsinks range from 0.500 in. for the horizontal-mount version, up to 0.750 or 0.875 in. for the vertical-mount versions. Rated at 57ÉC at 2 W and 7.5ÉC/W at 400 LFM in forced-convection environments, the heatsink has a footprint of 0.570 by 0.500 in. or 0.500 by 0.750 in. and is made from black anodized aluminum. Pricing is $0.27 ea/500 and delivery is stock to eight weeks.

Wakefield Engineering Inc.
60 Audubon Rd.
Wakefield, MA 01880
(617) 245-5900
▶ CIRCLE 827

▼ 3-SLOT VMEbus CHASSIS IS EMC SCREENED

This three-slot VMEbus development chassis can be used as a self-contained EMC-screened development environment or as the housing for the complete production status system. The desktop tower enclosure comes with an 80/110-W power supply with an 85- to 264-V universal input. The VMExcel monolithic backplane is fitted with Auto Bus Grant connectors to eliminate resetting of the jumpers when boards are inserted or withdrawn. A separate removable module accepts 3-1/2-in. floppy and hard drives and a top-rear-mounted fan draws cool air up through th active board area. The J2 area at the rear of the backplane is fully accessible for I/O configuration. Pricing is $1700 and delivery is two to four weeks ARO.

VERO Electronics Inc.
1000 Sherman Ave.
Hamden, CT 06514
Christal Czaja (800) 642-VERO
Fax (203) 287-0062
http://www.vero-usa.com
▶ CIRCLE 828

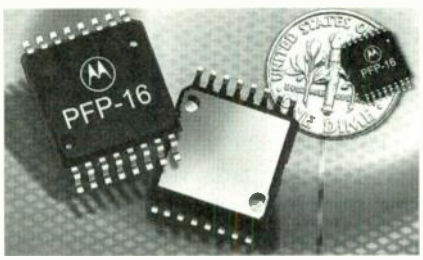
▼ ENCLOSURES ARE WATER AND DUST RESISTANT

This line of non-metallic IP 56 enclosures is available in both 75° and 115°C heat-resistant versions. The enclosures protect against water, saline solutions, and many bases, solvents, and acids. In addition, cable glands meet IP 66 specifications without either a washer or gasket. Up to 44 sizes are available. Pricing is from $4.99 to $174.99 each.

Connect-Tech Products, Inc.
2533 North Carson St., Suite 1370
Carson City, NV 89706
Clyde McAdams (800) 809-2751
Fax (702) 883-0986
▶ CIRCLE 829

▼ HIGH-POWER PACKAGE TARGETS RF APPS

The 16-pin Power Flat Package (PFP-16) is an RF-specific package with two rows of eight leads and an exposed plated-copper slug. Especially suited to packaging of RF inte-



grated power amplifiers popular in wireless handsets, the package can be soldered to a pc board using regular surface-mount techniques. Attaching the die to the slug not only provides superior electrical grounding, it also reduces device thermal resistance relative to common fused-lead SOIC packages. The package can dissipate up to 5 W.

Motorola, Inc.
2100 E. Elliot Rd.
Tempe, AZ
(602) 413-4730
RYCJ10@email.sps.mot.com
▶ CIRCLE 830

Micro-Cap V. Victory over the analog/digital simulation challenge.

The conflict's ended. And you're the winner—with this fifth generation of Micro-Cap, the industry's premier PC-based interactive CAE design tool. Incorporating a native digital simulator with PSpice®-compatible syntax, Windows-based Micro-Cap V™ seamlessly integrates analog/digital simulation and begins a whole new era.

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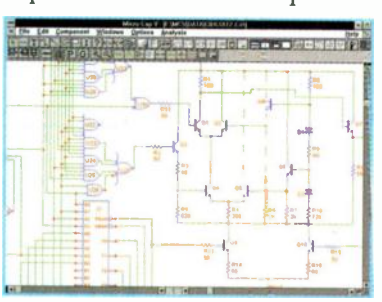
Further, this triumph comes at a very acceptable cost—$3495—less than half the price of would-be contenders.



Yet, while cost is strictly contained, design power is prodigious. A few samples? Analog behavioral modeling. Parameter stepping. Monte Carlo analysis. Nonlinear magnetic modeling. An optimizing model generator. Lossy transmission lines. On-schematic node voltage/state display. Real-time waveform plotting. Individual device temperatures.

We could go on, but our free brochure and demonstration disk can give you all the details. Ask for them. And begin reaping the rewards of total victory.

spectrum

Spectrum Software
1021 S. Wolfe Road
Sunnyvale, CA 94086
(408) 738-4387
FAX (408) 738-4702

READER SERVICE 185

▼ SHIELDS FOR EURO SUBRACKS REDUCE EMI/RFI

These perforated shields come with a honeycombed pattern for both EMI/RFI shielding and mechanical protection of a EURO subrack and its contents. Two models are available: the perforated shield-flat slides smoothly into grooves in the subrack's guilde rails, eliminating the need for assembly hardware; the perforated shield-grounding version also slides into the guide-rail grooves but assembles to the side plates with screws to assure positive grounding. Both models have 0.125-in. diameter holes on 0.187-in. staggered centers for a 40% open design. Pricing depends on size and quantity, but for a 3U x 160-mm rack ranges from $95.

Electro-Space Fabricators Inc.
300 W. High St.
Topton, PA 19562-0067
(610) 682-7181
▶ CIRCLE 831

▼ STRAIN-RELIEF BUSHINGS HAVE WIDE APPROVAL

The Z-Series of reusable strain-relief bushings meet UL, CSA, VDE, KEMA, and SEMKO standards for connecting power cables to appliances and instruments. The bushing allows US manufacturers to ship products without power cords, then supply the power cords and electrical plugs as required on site. A thin profile reduces the space required for clearance from one inch to half an inch. Installing the cable requires turning a hex nut 20°, yet the axial holding power is specified at 35 lb. or better. The bushings are made of self-extinguishing polyamide 6.6 nylon. Pricing is from $0.24 to $0.40 each per 1000. Delivery is three weeks ARO.

HSU Electronic Components Company
1461 SW 15th. St.
Boca Raton, FL 33486
(407) 393-8746
▶ CIRCLE 832

▼ 9-SLOT PCI BACKPLANE IN 20-SLOT CHASSIS

The 9-slot, PCI-compatible Model 15018-02 is the latest addition to the company's 150xx Series of ISA/PCI backplanes. Based on the DEC PCI-to-PCI bridge chip, the backplane provides for bus mastering on all slots and extends the standard PCI bus to allow additional loading and bus linking without degrading throughput. The backplane accommodates 486SX to Pentium/200 or Alpha/300 CPUs and comes with up to eight ISA slots. Pricing is $2,849 and delivery is stock to four weeks ARO.

Industrial Computer Source
9950 Barnes Canyon Rd.
San Diego, CA 92121
(800) 523-2320
▶ CIRCLE 833

▼ THERMAL PAD COOLS MICROPROCESSORS

The Thermflow T705 thermal interface pad is designed for use with high-performance processors. The pad consists of a thin, dry film that softens at microproecssor operating temperatures and has a thermal performance of 0.06°C-in.^{2}/W using Pentium processors with pin-fin heat sinks. The pads come with pressure-sensitive adhesive. Pricing ranges from $0.066 to $0.12, depending on size and quantity.

Chomerics, Div. of Parker Hannifin Corp.
77 Dragon Court
Woburn, MA
(617) 939-4163
▶ **CIRCLE 834**

▼ VMEbus ENCLOSURES ARE EMC-COMPLIANT

Available in 3-, 10-, and 20-slot versions, the ES Series of VMEbus enclosures meets the 89/336/EMC directive. The ES-3 enclosure measures 356 (H) by 315 (D) mm and has a three-slot, monolithic backplane with

a universal-input, 80-W power supply, and is cooled by a dc fan above the boards. EMC compliance is ensured through the use of in-line mains filtering, a VDE Level-A power supply, and conductive panels with overlapping joint fingers. The larger ES-10 and ES-20 models are 500 mm deep and come with a 10- or 20-slot backplane powered by a 450- or 750-W supply. Pricing for an ES-3 enclosure starts at $2,300 and delivery is four to six weeks ARO.

Radstone Technology Corp.
50 Craig Rd.
Montvale, NJ
(201) 391-2700
▶ **CIRCLE 835**

▼ ADHESIVE BONDS TO GOLD SURFACES

The 550-series adhesive film is designed for gold-plated and other difficult-to-bond metals and retains bond strength after exposure to moisture. Other adhesives in the series include the 561 series which bonds materials with extremely mismatched coefficients of thermal expansion, and the 5025E series which provides excellent thermal and electrical conductivity in the x, y, and z axes. All are available in sheet stock, slit rolls, and die-cut preforms.

Ablestik Electronic Materials and Adhesives
20021 Susana Rd.
Rancho Dominguez, CA 90221
Jilla Senkbeil (310) 764-4600
▶ **CIRCLE 899**

▼ DENSE CONNECTORS OFFER RELIABILITY

The Picoflex line of low-cost, high-reliability connectors offers designers many options for high-density applications where standard discrete-wire and flat flexible connectors are inappropriate. Available in circuit sizes from four through 20 and 26, the connectors mate with 0.050-in. cable. The connectors are tested to the high-vibration and high-shock requirements of the automotive and consumer-electronics industries to suit applications in car-audio systems, VCRs, television sets, computer peripherals, and telecommunication systems. Mated height is 6.4 mm for vertical mating configurations, which is about 15% than traditional 0.050-in. connector systems. A strong one-piece upper housing provides excellent cable retention. Pricing depends on quantity, style, options, and circuit size. For example, a 10-circuit vertical header with tin plating goes for $0.37 each in lots of 1000. Delivery is in four to six weeks.

Molex Inc.
2222 Wellington Ct.
Lisle, IL 60532
(800) 786-6539
▶ **CIRCLE 836**

▼ SHIELDED STEREO JACK MEETS AUDIO NEEDS

Applications can be found in the computer and multimedia markets for the ST-3200 shielded stereo jack. Designed for audio circuits, the 3.5-mm jack comes in a high-profile format for pc-board layouts requiring 6.5-mm above-board height. The threaded or non-threaded bushing, made of a copper alloy with nickel plating, provides grounding. Housing is of UL 94V-0-rated black PBT thermoplastic. The jack is shielded to provide EMI/RFI protection. It has a durability rating of 5000 mating cycles and an operating temperature range of –25 to 80C. Both three- and five-position versions are available. Pricing in lots of 5000 is $0.35 for the three-position unit and $0.37 for the five-position type. Delivery is in six to eight weeks.

Kycon Cable & Connector Inc.
1810 Little Orchard St.
San Jose, CA 95125
(408) 295-1110
▶ **CIRCLE 837**

▼ MICRO-COAX CABLE HAS LOW LOSS AT 18 GHz

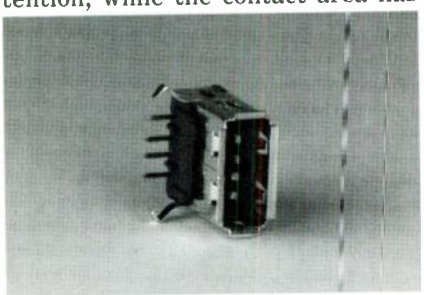
The UFB-311A is a UTiFLEX flexible microwave cable assembly that combines a dynamic bend radius of 4.75 in. with a low insertion loss of 0.20 dB/ft. at 18 GHz. The

cable has a power-handling capacity of 490 W CW at 5 GHz, RF shielding of at least -100 dB at 1 GHz, and an operating temperature range of -65° to 165°C.

Micro-Coax, A Division of UTE Corp.
Box 993, 245 West 5th. Ave.
Collegeville, PA
(215) 489-3700
▶ **CIRCLE 838**

▼ RECEPTACLE CONNECTOR IS USB A-TYPE

The KUSB-AS-1-N connector is USB compatible for the interconnection of computer peripherals. The connector's shell and contacts are phosphor bronze for contact retention, while the contact area has



gold plating and the solder tail is tin/lead over nickel. Double indentations on the shell provide a sturdy locking mechanism when plugged in. The black thermoplastic housing is UL 94-V-O rated. A plug kit is also available with standard cable lengths. Pricing is $0.57 ea/5000 and delivery is six to eight weeks.

Kycon Cable & Connector, Inc.
1810 Little Orchard St.
San Jose, CA 95136
(800) 544-6941
▶ **CIRCLE 839**

▼ DISK-DRIVE CONNECTOR IS SCA.2 COMPATIBLE

The FCN240 series connector comprises an 80-position (0.050-in. pitch), through-hole vertical-mount pc-board socket for the host system, and a straddle-mount surface-mountable plug for the disk drive. The SCA.2-compatible (single connector attachment) features four different contact lengths to accommodate 0.063-, 0.80-, and 0.110-in.-thick pc boards. Plastic ears on each end of the socket and plug provide keying.

For hot-swapping, two different-length leads along the inside of the connector provide sequential mating for various functions such as signal, power, last mate, and first break. The connectors are backward compatible with SCA.1 devices. Pricing is $3.75 ea/10,000 and delivery is from stock.

Fujitsu Takamisawa America Inc.
250 Caribbean Drive
Sunnyvale, CA 94089
(800) 380-0059
http://www.fujitsufta.com
▶ CIRCLE 840

▼ CRIMPLESS OPTICAL CONNECTOR SAVES TIME

Designed for use with the company's Versatile Link fiber-optic transmitters and receivers, the HFBR-453X series of connectors reduces installation time by using a snap-together assembly that eliminates the need for crimping and special tools. All that is required is a wire stripper, a pair of scissors, and 600-grit sandpaper. Fine polishing with 3-micron lapping film is recommended.

Made from flame-retardant ULTEM plastic, the connectors are available in latching and non-latching versions. Two non-latching versions can be snapped together for a duplex (transmit/receive) configuration. Features include a data rate of 40 kbits/s up to 155 Mbits/s over distances of up to 125 m using 1-mm plastic fiber. Color coding is provided. Pricing for both latching and non-latching devices is $0.33 ea/500.

Hewlett-Packard Company
Stevens Creek Blvd., PO Box 58059
Santa Clara, CA 95052-8059
(800) 537-7715 ext.2067
http://www.hp.com
▶ CIRCLE 841

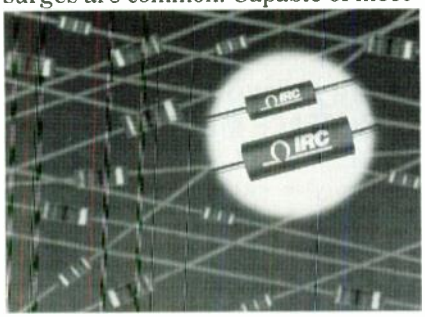
▼ PCB HEADERS ARE COLOR CODED

These color-coded pc-board-mounted headers are available in single colors or color combinations of red, green-yellow, white, and blue. Targeting both through-hole and surface-mount applications, the devices come in single-, double-, and triple-row configurations with 0.100-in., 2-mm, or 0.050-in. center spacings and can tolerate temperatures up to 260°C. Pricing is $0.02 each per line in volume.

Comm Con Connectors Inc.
1848 Evergreen St.
Duarte, CA 91010
(818) 301-4200
http://www.commcon.com
▶ CIRCLE 842

▼ METAL-FILM RESISTORS SUB FOR CARBON

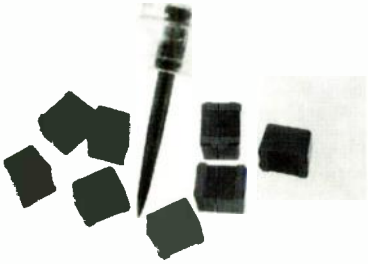
The RG Series of power metal-film resistors feature a power rating of 1 W at 70°C in a 1/4-W package and can substitute for carbon-composition resistors in applications where high surges are common. Capable of meeting or exceeding MIL-R-10509 and MIL-R-22684 standards, the resistors have an operating temperature range of -55° to 150°C and are offered in values from 1Ω to 5.1 MΩ. The devices are available in tolerances down to +/- 1% with temperature coefficient ratios to +/- 100 ppm/°C. Leads are 30/70 electroplated copper with high-temperature soldered terminations. Pricing is $0.057 ea/10,000 for the RG 1/4 100Ω +/- 5 % and delivery is stock to four weeks.



IRC
4222 South Staples St.
Corpus Christi, TX 78411
(800) 472-6467
Fax (512) 992-3377
▶ **CIRCLE 843**

▼ INDUCTORS OPERATE AT HIGH FREQUENCIES

The Model IMC-1210-100 inductor is available in a range of inductances from 0.01 to 0.100 µH with self-resonant frequencies up to 2500 MHz. Measuring 0.098 (W) by 0.126 (L) by 0.087 (H) in., the devices come with a molded covering for strength and moisture resistance and a non-magnetic core for high-inductance stability. Depending on inductance, models can be ordered with tolerances from +/- 5 % to +/- 20 %. Minimum Q values range from 15 at 0.10 µH, with both Q and inductance measured at 100 Mhz. Pricing for a typical model with a minimum Q of 0.01 µH, a +/- 20 % tolerance, and a 2500-MHz SRF is $0.208 ea/2000. Delivery is from stock to 10 weeks.



Dale Electronics Inc.
2064 12th. Ave., PO Box 609
Columbus, NE 68602-0609
Robin German
(402) 563-6417
FlashFax (800) 487-9437
▶ **CIRCLE 844**

▼ DUAL TRANSISTOR COMES IN SMD PACKAGE

The AT-32063 is a low-current dual transistor comprising two NPN silicon bipolar transistor chips in a single SOT-363 (2.0 by 1.25 by 0.9 mm) six-lead surface-mount package. The device may be used between 1 and 5 V with as little as 1 mA of current. At 900 MHz, the transistor features a 1.3-dB noise figure and 14 dB associated gain, and at 2.7 V and 20 mA provides +12 dB of output power. The two transistors can be used separately. The transistor is available in bulk and in tape-and-reel packaging. Pricing is $0.64 ea/10,000.

Hewlett-Packard Company
5301 Stevens Creek Blvd., PO Box 58059
Santa Clara, CA 95052-8059
Sales Dept.
(800) 537-7715 ext.2030
▶ **CIRCLE 845**

▼ LEDS COME IN MINIATURE PACKAGE

The SML-211 and SML-311 are 0805- and 0603-packaged, respectively, LEDs for power-sensitive applications. Based on AlGaInP technology, the devices output 7 mcd at 2 mA and come with peak wavelengths ranging from 590 to 630 nm. The operating temperature range is -30° to 85°C. Pricing starts at $0.12 ea/100,000 and delivery is 12 weeks ARO.

Rohm Corp.
3034 Owen Dr.
Antioch, TN 37013
(615) 641-2020
Fax (615) 641-2022
▶ **CIRCLE 846**

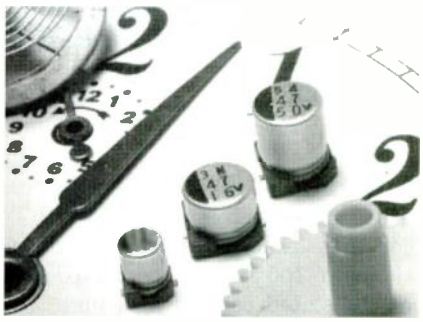
▼ ISOLATION TRANSFORMERS TARGET MODEMS

Part of the company's Datalink Series, the MIT-101, -115, -125, and -131 Series modem isolation transformers are intended for modems with speeds from V.29 up to V.34. All reflect 600 Ω on the primary, feature 1250-V-ac input-to-output isolation, and have an operating temperature range of -40° to 105°C. The MIT-101 and -115 reflect 470Ω on the secondary load, use wet-coupler construction, measure 23 by 24 by 12 mm, and are compatible with V.29 speeds. The MIT-125 and -131 devices reflect 374Ω on the secondary, use dry-coupler construction, measure 26 by 24 by 12 mm, and target V.32 and V.34 applications, respectively. Pricing: MIT-101/-115, $1.05; MIT-125, $1.28; MIT-131, $1.87 ea/10,000. Delivery is four to six weeks ARO.

CP Clare
Advanced Magnetics Products
601B Campus Dr.
Arlington Heights, IL 60004
(847) 797-7000
Fax (847) 797-7023
▶ CIRCLE 847

▼ POLARIZED CAPS ARE SURFACE MOUNTABLE

The Type MXM polarized aluminum electrolytic capacitors target surface-mount applications. Available in seven voltages ranging from 4.0



to 50 V dc, the capacitors feature an expanded capacitance range of 0.1 to 1000 µF and an operating temperature range of -55° to 85°C. The devices come in six case sizes ranging from 4 by 5.5 mm to 8 by 10.8 mm and are load-life tested for 2000 hours at 85°C and are anti-solvent (2 minutes). Pricing starts at $0.11 ea/5000 and delivery is from stock to 12 weeks.

Tecate Industries Inc.
1841 Friendship Drive
El Cajon, CA 92020
(619) 448-4811
Fax (619) 448-0912
▶ CIRCLE 848

▼ POLYMER ALUMINUM CAPS HAVE LOW ESR

The Type ESR polymer aluminum capacitors have an equivalent series resistance of 15 mΩ and come with capacitance and voltage values of 33 µF at 8 V, 22 µF at 12.5 V, and 10 µF at 16 V. The devices target operating frequencies of 100 kHz and above.

Cornell Dubilier
1605 East Rodney French Blvd.
New Bedford, MA 02744
Joe Rapoza (508) 996-8564
Fax (508) 996-3830
▶ CIRCLE 849

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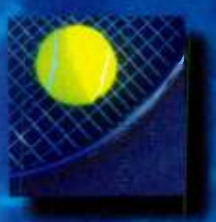

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PRODUCTS NEWSLETTER

Low-EMI Technology Upgrades K0 MCU Family

A low electromagnetic-interference (EMI) technology was implemented into NEC's K0 8-bit microcontroller product line, enhancing the devices for their targeted noise-sensitive applications, such as automotive, audio, consumer, and wireless communications. The technology was applied to several new versions within the K0 line by designing the internal ground and power buses and controlling current throughout the chip. With this new low-noise capability, board designers can use fewer parts, reducing the number of layers in their pc boards. In addition to reduced design complexity and size, they also help designers attain better than class B requirements. The devices operated for 1.8 to 5.5 V and contain peripheral devices like direct-drive LCD controllers, fluorescent indicator panel (FIP) controller/drivers, as well ADCs and DACs. Call (800) 366-9782 or (408) 588-6000; or visit the company's web site at http://www.nec.com. *RE*

CIRCLE 570

PC-Based Playback Adapter Works With DVD

Digital Versatile Disk (DVD) technology has made a lot of noise in the press over the last year, but actual products have only trickled onto the market. That trend may start to change with the introduction of the DVD Theater audio and video playback adapter. Developed by STB Systems Inc., Richardson, Texas, the adapter is suited for movies and interactive games on the desktop PC. The DVD Theater supports the latest standards for MPEG-2 video and Dolby Digital AC-3 audio. The adapter's output can be connected directly to a PC monitor or a standard television. Software support comes in the form of Microsoft's ActiveMovie driver, which operates with Windows 95 and Windows NT 4.0. Available before the end of the year, the DVD Theater should sell for under $200, depending on volume. For more information, contact STB Systems at (972) 234-8750, or on the Internet at http://www.stb.com. *RN*

CIRCLE 571

IC Series Implements CEBus In Consumer Electronics

Thanks to a new series of embedded communication ICs, announced at the Parks Associates' FORUM 96 conference in San Diego, Calif., the entire range of CEBus-compatible home-networked products is expected to provide consumers with an expanded level of security, comfort, and convenience in the home environment. The series, developed by Intellon Corp., Ocala, Fla., comprises three chips. The SSC P400 Power Line Network Interface Controller targets advanced home controller devices, custom installation products, utility meters, and gateways. That chip combined with the SSC P111 Power Line Media Interface IC results in a two-chip high-performance solution for CEBus Standard power-line communication. It provides network services required for advanced controllers like audio/video equipment. The third IC, called the SSC P200 Simplified Network Interface, homes in on cost-sensitive applications in security, appliance, and environmental controls and lighting. Because it provides all of the necessary CEBus Standard Data Link Layer (DLL) and Spread Spectrum Carrier (SSC) physical layer functions, simple devices such as lighting modules can be implemented with microcontrollers costing under $1. For more information, call (352) 237-7416; fax: (352) 237-7616; Internet: http://www.intellon.com. *RE*

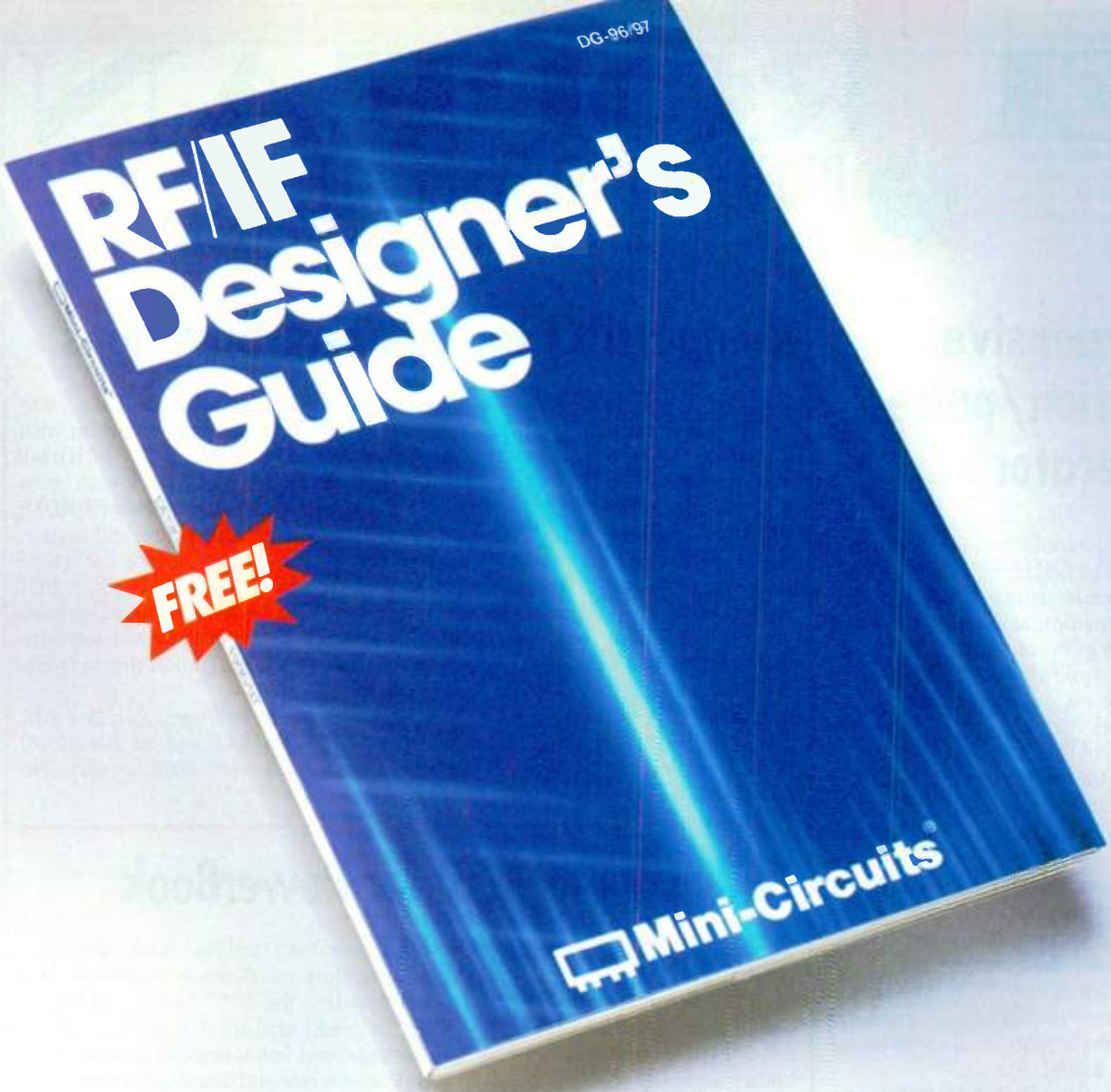
CIRCLE 572

Prices Tumble For Popular Microcontrollers

As part of its Continuous Microcontroller Service Initiative to the embedded-systems market, Motorola's CSIC Microcontroller Divisions announced price reductions in its 68HC05 and 68HC08 one-time-programmable (OTP) 8-bit families. In addition to the lower prices, the company is proposing the "7-Day CSIC Design Methodology" and the "MCU's-In-A-Day" program. The latter offers one-day shipment of many of Motorola's best-selling OTP microcontrollers, and if that's not met, enrolled customers get the programming for free (there are certain limitations, call (888) MCU-1DAY for details). Seven microcontrollers are experiencing price reductions, such as the 68HC705B16 dropping from $12.50 to $8.95 each, and the flagship part of the 68HC08 architecture"the 68HC708XL36"which falls from $14.00 to $8.95 each. The new suggested prices are for quantities of 1000 or more. For further information, contact the Motorola MCU Information Line at (800) 765-7795, ext. 860; fax (800) 765-9753; or WWW: http://design-net.com/csic. *RE*

CIRCLE 573

Edited by Roger Engelke



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CUSTOM PRODUCT NEEDS...Let Our Experience Work For You.

233 Rev Orig

EUROPEAN PRODUCT NEWSLETTER

The products listed are available in Europe but may not be available in other market areas of the world.

Inexpensive function/pulse generator

At an adjustable frequency range of 0.005 Hz to 5 MHz in seven overlapping decade ranges, the low-cost TG503 function and pulse generator is able to generate pulse, sine, triangle, and square waveforms. Fine adjustment is accomplished by a calibrated vernier.

More than 20 dB of vernier control is available within each attenuator range. For sinewave generation, distortion is less than 0.5% to 50 kHz and less than 1% to 500 kHz. All harmonics are more than 30 dB below fundamental on the 1-MHz range. Maximum output is 20-V p-p from 50 Ω. The dc offset can be set in the range ±10 V. A fixed TTL-level output at the same frequency and symmetry as the main output can drive 20 standard TTL loads.

Typically, the symmetry control varies the duty cycle from 1:19 to 19:1 to produce sawtooth and variable pulse-width waveforms. In the pulse mode, normal, double, or delayed pulses are generated with independently variable pulse width or delay.

Pulse period can be varied between 200 ns and 200 seconds (5 MHz to 0.005 Hz), with 100 ns (10 MHz) minimum perioed in double-pulse mode; while pulse width is adjustable from 50 ns to 50 ms, and delay from 100 ns to 50 ms. A complement mode also is available.

Operation can be trigger or gate mode; a start/stop phase control varies the triggered and gated start/stop point from –90° to +90° up to 500 kHz. Call for pricing. *RE*

Thurlby-Thandar Instruments Ltd., *2 Glebe Rd., Huntingdon, Cambs., PE18 7DX, England, phone: (01480) 41251; fax (01480) 450409.*

CIRCLE 626

CompactPCI targets real-time apps

The first CompactPCI real-time-oriented PowerPC card, called the RIOC, was unveiled by Creative Electronic Systems (CES). It comes in conjunction with the company's launch of its third-generation PowerPC VME platform (RIO3). Features are a 66-MHz PowerPC 603 and 166-MHz PowerPC 604ev with up to 1 Mbyte of L2 cache; 8 to 80 Mbytes of DRAM; up to 8 Mbytes of flash EPROM; 128 kbytes of SRAM; and Ethernet. Two serial ports, a keyboard and mouse, and TTL I/O signals can be connected via the front panel or the backplane connectors. The card has a primary PCI backbone with 2 PMC slots, a PCI extension for dual or quad PMC carriers, and a VME extension for an optional 6U VME D64 interface. Also included is a complete set of low-level software tools. Optional board support packages for most popular RT operating systems are available, such as VxWorks, pSOS, Chorus, etc. *RE*

Creative Electronic Systems S.A., *70, route du Pont-Butin, P.O. Box 107, CH-1213 Petit-Lancy 1, Genevia, Switzerland; telephone: +41 22 792 57 45; fax +41 22 792 57 48; e-mail: ces@lancy.ces.ch; Internet: http://www.ces.ch/CES_info/Welcome.html.* **CIRCLE 627**

ISDN adapter card for PowerBook

The industry's first PCMCIA Macintosh PowerBook qualified card, called ExpresSO PCMCIA, enables PowerBook computers to efficiently exchange data over the Internet and other networks. By using the PPP Internet standard dial-up format for making connections, the credit-card-sized Type II interface provides Internet access in only two seconds, and can download images at 64 kbits/s. Typically, modems have a 30-second access rate and download at 28 kbits/s. The card comes with the company's file-transfer software called Transfile, which transmits compressed data at 1 Mbit per minute while providing data security and access control. Also included are the Mac-OS driver, ISDN tools, and a serial port for Internet access. Installing the card and its associated software is simplified because Plug 'n' Play for Macintosh is supported. *RE*

SCii TELECOM, *5 Ter. Rue du Dome, 75116 Paris, France; telephone: (33.1) 44 17 44 22; fax (33.1) 44 17 44 19; e-mail: clarisse@sciitelecom.com.* **CIRCLE 628**

Octal UART offers high performance

The OX10864 octal UART provides serial communications of 3 Mbits/s on all channels simultaneously, surpassing the data rates required for connection to high-speed modems. UARTs typically provide 115 or 230 kbits/s. Among its features are deep FIFO buffers on each transmitter and receiver, which minimizes the interrupts thus lowering the overhead. Its user-selectable Intel/Motorola bus interface provides a "glueless" solution to most common applications. The chip has eight modem lines per channel, automated flow control, and special character recognition and generation, giving designers a simple solution to any asynchronous protocol. Fabricated in a 0.6-μm triple-layer metal process, the UART can be operated at up to 50 MHz with its on-board crystal oscillator. *RE*

Oxford Semiconductor Ltd., *68 Milton Park, Oxon OX14 4RX, United Kingdom; telephone: 01235 861461; fax 01235 821141; e-mail: jalil@oxsemi.demon.co.uk.* **CIRCLE 629**

DIGITAL ICs

3D GRAPHICS ACCELERATOR HANDLES TEXTURES, VIDEO

By adding arcade-performance 3D action graphics capabilities to personal computers, the Laguna3D family of multimedia accelerators can deliver up to 50 million perspective-corrected texels per second—about three times the throughput of most other 3D solutions currently in production. Developed by Cirrus Logic, the Laguna3D chips are optimized to support both the Microsoft Direct3D application programming interface for real-time 3D graphics, as well as the forthcoming accelerated graphics port from Intel.

The first Laguna3D chip, also known as the CL-GD5464, is a 64-bit multimedia accelerator that not only delivers high-quality 3D graphics, but also delivers fast 2D performance and handles motion video streams at up to 30 frames/s. This chip is optimized for PCI interface cards and direct use on the motherboards; a subsequent version will include the Intel AGP interface (the CL-GD5465).

To deliver the high bandwidth without employing extremely wide and thus pin-intensive memory buses, Cirrus designers opted to use the Rambus DRAM interface for the graphics memory. With a single RDRAM interface, data-transfer rates of 600 to 667 MHz can be achieved over the byte-wide memory data bus. Additional future enhancements will further increase graphics bandwidth by adding a second Rambus RDRAM memory interface, raising the maximum data transfer rate to 1.2 Gbytes/s. By optimizing the accelerator design to work with the RDRAM interface, functions such as texture management can be incorporated into the chip without using separate texture memory buffers, which simplifies system designs.

The texture-management scheme, called TextureJet, supports the 3D graphics by providing more realistic backgrounds and scenic effects. The high bandwidth possible with the RDRAMs allows the texture memory to be loaded and updated quickly from off-screen graphics memory. And, such textures will be used more frequently in applications such as games to provide more realistic images.

On average, in the games being developed today, programmers apply textures to about 75% of the pixels on the screen, and that percentage is expected to increase to 95% some time during 1997. The size and density of the textures range from 32-by-32 to 256-by-256 pixels for the texture elements, and the elements are used for fine- to large-area rendering, with from 12 to 24 different textures of varying sizes typically appearing in each scene.

To provide enough memory without duplicating the graphics memory, the TextureJet architecture developed by Cirrus consists of an on-chip texture-management engine that's part of the Laguna 3D controller. By incorporating on-chip address translation table, in conjunction with a 1-kbyte texture cache, the Laguna3D can keep track of virtually all of the memory locations of the textures being used. The tracking can be done regardless of the location of the textures in either the graphics subsystem memory or the main system memory, or if the texture is broken up and located in several regions of memory.

The Laguna3D chip can prefetch the data and cache the texture in its complete form; therefore, the active frame buffer can readily access the information. This is the same AGP programming model being put in place by Intel. As a result, the Laguna3D TextureJet engine will be easy to tie into the AGP since it uses PCI bus mastering and dynamic memory allocation along with a coprocessor architecture. The internal rendering engine on the Laguna3D processor employs a single-instruction/multiple-data approach to perform many operations in one pass. Concurrent processing is done on functions such as alpha blending, lighting/shading, transparency, dithering, fogging, filtering, perspective correction, and clipping. Thus, many of the 3D features can be computed with just a single pass of the rendering engine.

In addition to the 3D graphics, the Laguna3D provide 2D graphics resolutions of up to 1600 by 1200 pixels at 85 MHz and true-color operation at resolutions of up to 1024 by 768 pixels. An on-chip 230-MHz DAC and clock synthesizer as well as a full-featured VGA controller all contribute to the high 2D performance. Video playback also is possible on a scalable MPEG-2 video window. Moreover, the chip incorporates the company's V-Port interface for expansion. BIOS support is available for PCI, full IBM VGA compatibility, VESA BIOS extensions, plug-and-play, and display-data channel monitor signaling.

Housed in a 208-lead PQFP, the CL-GD5464 sells for $29.50 each in lots of 10,000 units. Production quantities are available immediately for the CL-GD5464; samples of the AGP version are expected late this year, with production to start in the first quarter of next year.

***Cirrus Logic Inc.**, 3100 West Warren Ave., Fremont, CA 94538; Saul Altabet, (510) 623-8300, or on the web at http://cirrus.com.*

CIRCLE 700

DAVE BURSKY

VIDEO-MULTIPLEXER MIXES GRAPHICS AND VIDEO

Able to combine video and graphics information onto the same display, the CH8439 multiplexer chip can work with displays featuring resolutions of up to 1280 by 1024 pixels and 16.7 million colors. The chip can accept full-bandwidth analog RGB graphics signals and control the mixing of digital video inputs using a programmable analog color key and high-performance gen-lock circuit. Included on the chip is the company's proprietary leakage suppression technology, which allows the chip to support color-key control while limiting graphics bleedthrough to less than one pixel. Additional features include dual analog wide-band drivers, and YUV-to-RGB color-space conversion. The CH8439 comes in a 64-lead PFQP and sells for $9.75 apiece in lots of 1000 . DB

***Chrontel Inc.**, 2210 O'Toole Ave., San Jose, CA 95131-1326; Ken Lowe, (408) 383-9328.* CIRCLE 701

DIGITAL ICs

HIGH-SPEED 486 CPU EYES EMBEDDED SYSTEMS

By upping the internal clock speed of the Am486 microprocessor core to 133 MHz, the Am486 DX5-133 is able to offer the highest-performance 486-class processor for the embedded-systems market. Housed in a low-cost, 208-lead, small quad-sided flat package, the CPU provides a 25% performance boost over the previous best-of-class version, the 100-MHz Am486 DX4. Developers can leverage the programmer's familiarity with the x86 instruction set because the CPU is fully compatible with x86 software that runs on desktop, portable, and x86 real-time OSs—no features were removed or reduced to achieve the high clock rates. At the 133-MHz internal speed, it performs like most 32-bit RISC processors. In lots of 10,000, the DX5-133 sells for $33.75 each. DB

Advanced Micro Devices Inc., *One AMD Place, P.O. Box 3453, Sunnyvale, CA 94088-3453; (408) 749-5703; Internet: http://www.amd.com.* CIRCLE 702

SPEEDY 2-MBIT EPROM PACKS 16-BIT DATA PATH

Organized as 128 kwords by 16 bits, the AT27C2048 UV EPROM is available in versions with access times as short at 70 ns. Fabricated with 0.5-µm design rules, the fast memory chip also is very small. This translates into two benefits: First, the chip can be housed in a small, windowless 10-by-14-mm TSOP, which lets the memory go into board-space-limited applications that need one-time programmability; second, the chip should cost less to manufacture, translating into lower chip prices. The short access time of 70 ns allows the EPROM to be used in many systems without adding wait states, which are often included to compensate for slower-access memories. At full speed, the device has a current drain of just 35 mA. The AT27C2048 comes in a PLCC, TSOP, or PDIP, and prices for the memory start at $4.25 apiece in quantities of 1000. DB

Atmel Corp., *2325 Orchard Pkwy., San Jose, CA 95131; Dirk Franklin, (408) 436-4110.* CIRCLE 703

FLASH-MEMORY MODULES DELIVER UP TO 32 MBYTES

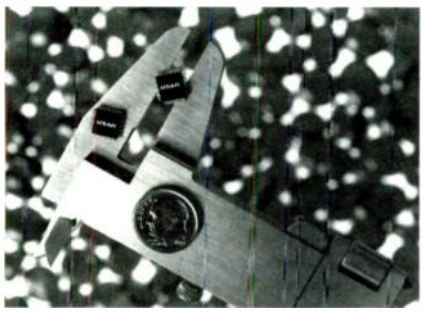
Organized as a 32-bit-wide memory, a family of flash-based single-in-line memory modules (SIMMs) provide nonvolatile capacities of 8, 16, and 32 Mbytes. All three modules are designed for operation from a 5-V supply for both read and write operations, and have maximum access times of 90 ns. The flash memories used in the 80-contact SIMMs are sectored devices (64 kbytes/sector), and the architecture supports full chip erase and the selective erasure of any combination of memory sectors. A two-step erase sequence ensures that memory contents aren't erased accidentally. The flash memories are guaranteed for a minimum of 100,000 write/erase cycles. Prices in 100-unit lots start at less than $200 each for the 8-Mbyte unit, less than $400 for the 16-Mbyte SIMM, and less than $800 for the 32-Mbyte stick. DB

White Microelectronics, *4246 E. Wood St., Phoenix, AZ 85040; Jack Bogdanski, (602) 437-1520.* CIRCLE 704

DIGITAL ICs

MINI 48-LEAD PACKAGE TRIMS BOARD-SPACE NEEDS

A reduced-size, quad-sided flat package, measuring just 7 by 7 mm, provides a significant reduction in board space for a family of low-power keyboard encoder chips. Ideal for applications in which board space is a premium, the 48-lead package is available for use with



the company's KeyCoder chips—the GreenCoder series for laptops and notebook computers, and the PlexiCoder series for handheld, battery-operated systems. The KeyCoder families are available for most input device interfaces, including PS/2 and XT for PC compatibles, serial, SPI, IIC, and on-board Access.bus/SMBus. The compact package helps save space, yet the high pin count avoids any sacrifice in functionality. Because the circuits will be equipped with self-power management, the device will consume less than 2 µA during inactive periods. The chips can sleep between keystrokes causing the percent of active time to be very low, thus minimizing active power. The chip draws only 2 mA when active. The small footprint package is available for orders of 2000 units and above. DB

USAR Systems Inc., 568 Broadway, Ste. 405, New York, NY 10012; (212) 226-2042. CIRCLE 705

ASIC LIBRARY TARGETS LOW POWER DESIGNS

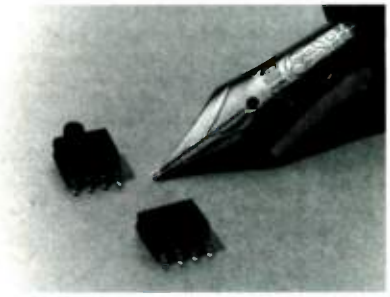
The SLA40000 gate-array family and companion design library offers systems and communications vendors a semicustom design methodology for high-performance, low-power, and low-voltage supply requirements. The CMOS arrays are based on 0.4-µm design rules. They contain raw gate counts of up to approximately 400,000 gates across a family of eight masterslices, and provide an average gate utilization of about 70% with triple-layer metal interconnections. Internal gates have delays of just 154 ps and consume just 1.1 µW/gate/MHz when powered by a 3.3-V supply. On-chip dual-level shifters allow for simultaneous 3.3- and 5-V operation. Embedded SRAM blocks can be added to any of the eight masterslices through a high-density stacked-via configurable-memory megacell. The library has more than 400 I/O cells that support bus interfaces such as PCI, GTL, and USB. The arrays come in various high pin-count package options (e.g., QFP and BGA). Nonrecurring engineering charges start at $25,000; final charges depend on design complexity and volume, among other factors. DB

S-MOS Systems Inc., 150 River Oaks Pkwy., San Jose, CA 95134-1915; Dev Chakravarty, (408) 922-0200. CIRCLE 706

ANALOG

0-To-100-PSI Pressure Sensor Comes In An SOIC-8

The NPP series of low-cost pressure sensors now are available in standard plastic SOIC-8 packages (0.150 by 0.194 in.). This makes them compatible with automated handling and insertion equipment. Operating over a temperature range of 40 to 125°C, they're available in absolute-pressure ranges of 0 to 15, 0 to 30, and 0 to 100 psi. They provide an unamplified full-scale output of 60 ±20 mV when excited by 3 V dc. Combined linearity hysteresis and repeatability error is less than ±0.3% of full-scale output. Static accuracy is within less than ±0.2% maximum of full-scale output. Input and output impedance is 5 kΩ ±20%. The NPP series of sensors is available for less than $3



each in OEM lots of about 10,000 to 50,000 pieces. Sample and production quantities are available now. RA

Lucas Novasensor, 1055 Mission Court, Fremont, CA 94539; (800) 962-7364; fax: (510) 770-0645. CIRCLE 707

Dual 10-Bit ADC Ideal For Video Decoding

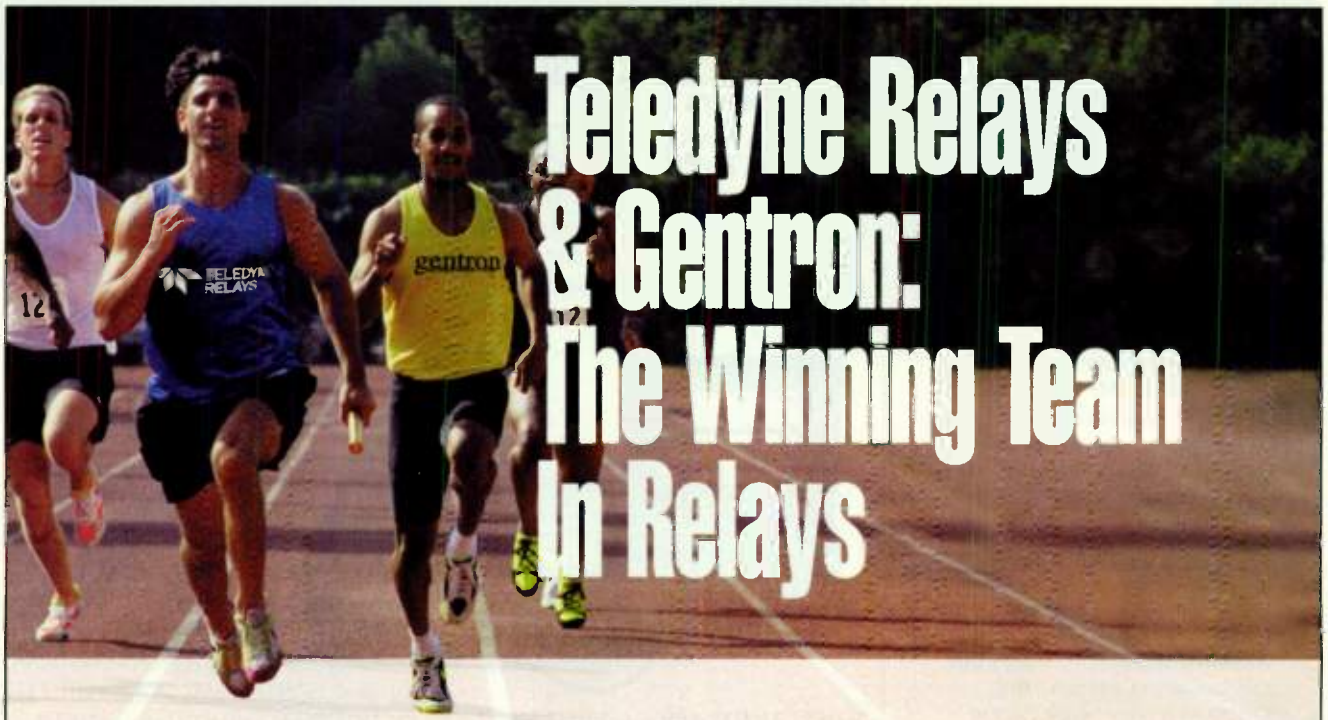
The SPT7852 integrates two 10-bit CMOS ADCs with sample rates up to 20 Msamples/s into a single device. Channel-to-channel crosstalk is better than 70 dB, and total power consumption is less than 160 mW. The dual channels make the IC ideal for the coherent processing of information like the I/Q processing paths of QPSK and QAM, and for S-Video digitizing, as well as composite digitizing for multiple video sources. Operating from a single supply of between 3.3 and 5 V, the SPT7852 comes in a 44-lead TQFP package and sells for $14.95 in 1000-piece lots. PMcG

Signal Processing Technologies Inc., 4755 Forge Rd., Colorado Springs, CO 80907; (800) 643-3778 or (719) 528-2300; fax (719) 528-2370. CIRCLE 708

Low-Power Triple DAC For High-Performance Video

The monolithic SPT5230 is a 10-bit, triple-video DAC supporting conversion rates up to 50 million words/s with power dissipation of only 280 mW. Designed for high-performance video uses, the chip offers 49-dB channel-to-channel crosstalk isolation and ±1 LSB differential linearity in a footprint of only 10 × 10 mm. A single external resistor controls the full-scale output current. All logic levels are TTL-/CMOS-compatible. The SPT5230, which comes in a 52-pin SQFP package, sells for $23.80 in 1000-piece lots. PMcG

Signal Processing Technologies Inc., 4755 Forge Rd., Colorado Springs, CO 80907; (800) 643-3778 or (719) 528-2300; fax (719) 528-2370. CIRCLE 709



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READER SERVICE 194

NEW PRODUCTS

INSTRUMENTS

PCMCIA CARDS USE JTAG FOR POWERPC EMULATION

A real-time emulator for the PowerPC processor line is housed in a Type II PCMCIA card that can be plugged into notebook PCs for use in the field. The PowerEM uses the PowerPC's IEEE-1149. 1 JTAG port to access the processor's on-chip debug facilities. This eliminates the need for external pods, reducing cost and electrical loading of the target system. Also, the emulator automatically supports any clock speed at which the target system runs, and it maintains processor access even when the PowerPC hangs or runs out of control. Users can download programs and data to any part of the system RAM through the JTAG port without a resident loader or ROM emulator. The four-wire JTAG interface can be connected to a PowerPC 403, 603, or 604. The IEEE-1149.1 controller used in the emulator features dual, independent test-access-port controllers, on-board memory, and a high test clock speed. The controller comes with a terminate-and-stay-resident client driver for automatic card configuration, as well as self-diagnostic routines and a scan function library. Overall pricing for the PowerEM starts at $4950, including a full-featured, Windows-based, source-level debugger. JN

Corelis Inc., 12607 Hidden Creek Way, Suite H, Cerritos, CA 90703; (310) 926-6727; fax (310) 404-6196.

CIRCLE 710

FUNCTION GENERATOR SWEEPS TO 20 MHZ

The TG120 function generator offers eight ranges, covering a bandwidth of 0.2 Hz to 20 MHz. It supplies sine, triangle, and square waves, as well as dc levels. A switchable bidirectional variable symmetry also allows users to generate variable duty-cycle pulse and sawtooth waveforms. The instrument can be run in sweep mode using an external sweep voltage at a range of at least 20:1. Frequency modulation also is possible. The generator outputs a maximum of 20 V p-p at 50 Ω. An amplitude vernier with a range of 26 dB combines with two 20-dB switched attenuators to supply levels down to 10 mV p-p. A variable dc offset of ±10 V is available using a center detent control. An auxiliary output provides a fixed +5-V level for driving TTL and CMOS loads. Call for current U.S. pricing. JN

Thurlby Thandar Instruments Ltd., 2 Glebe Rd., Huntingdon, Cambs., PD18 7DX, England; (44) (01480) 412451; fax (01480) 450409.

CIRCLE 711

2-GSAMPLE/S SCOPES BOAST COLOR DISPLAYS

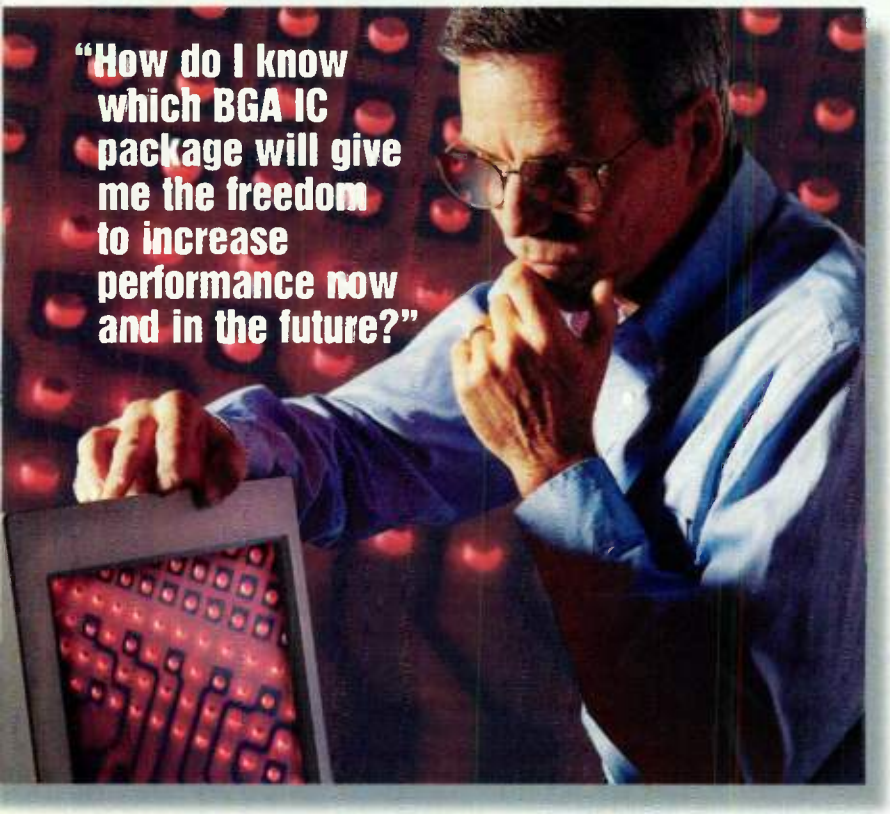
The TDS 782A and TDS 754A digital storage oscilloscopes deliver up to 2-Gsample/s sampling at a bandwidth to 1 GHz, while offering the company's InstaVu acquisition technology to capture infrequent glitches, metastable behaviors, and time jitter. The TDS 782A has a 1-GHz bandwidth and samples at 2 Gsamples/s on one channel and 1 Gsample/s on two channels. The TDS 754A has a 500-MHz bandwidth and samples at 2 Gsamples/s on one channel and 1 Gsample/s on each of four channels. Each of the scopes feature an industry-standard record length of 50k.

The TDS 754A offers a optional record length of 500k, while the TDS 782A offers 250k. They also feature the proprietary NuColor display technology. An advanced suite of trigger modes includes a new time-out mode, and a channel deskew function boosts the accuracy of timing measurements by compensating for external timing errors. Drivers for 22 types of printers are available for hard-copy output. The TDS 782A and 754A start at $21,995 and $18,500, respectively. Delivery is in eight weeks. JN

Tektronix Measurement Business Div., Literature Distribution Center, P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200, code 555; Internet: http://www.tek.com/Measurement

CIRCLE 712

Design In ▶ AMKOR



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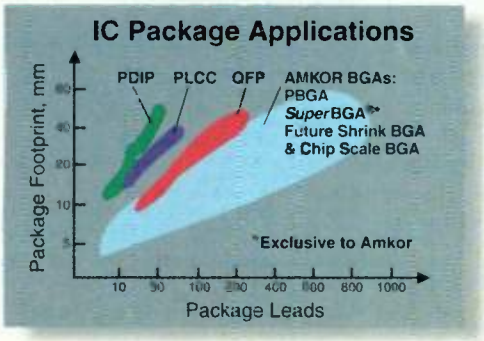

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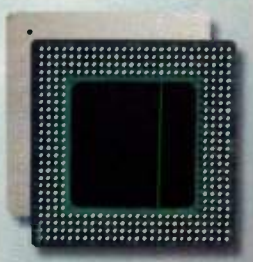

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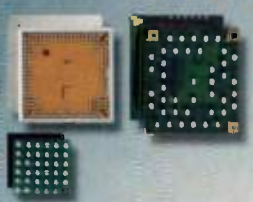

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NEW PRODUCTS

SOFTWARE

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Based on Texas Instruments' TMS320C203 digital signal processor, the C2xx DSP development system is for low-cost, high-performance applications. It can be used as a standalone development system or embedded into products using its I/O headers. Upgradable to future products in the C2xx family, the development system has on-board SRAM, flash memory, 16-bit data converters, and RS-232 serial interfaces. Also included are a 5-V power supply, a DOS-based assembler/linker and debugger, and GO DSP's Code Explorer. Single units of the system sell for $149. ML

Wyle Electronics, 15370 Barranca Pkwy, P.O. Box 19675, Irvine, CA 92713-9675; (714) 753-9953.

CIRCLE 713

TOOLSET ADDRESSES YEAR-2000 REENGINEERING

TestBed for MVS Cobol is a static- and dynamic-code coverage and analysis toolset for helping find, debug, and document efforts in reengineering legacy code for the year 2000. The year 2000 is a problem because many systems have just two digits to store the year portion of each date. This storage limitation can result in miscalculations using date information crossing the year 2000. Static analysis verifies source-code standards and integrity. Dynamic analysis involves executing an instrument version of user code to detect defects at run time. The two testing fields depict code quality and structure; trouble areas are highlighted for rework or removal. TestBed's testing capabilities include programming standards verification, structured programming verification, complex metric measurement, variable cross reference, unreached code reporting, control flow tracing, statement execution frequency analysis, and LCSAJ subpath coverage. TestBed supports C, C++, Ada, Cobol, Pascal, and assemblers on hardware platforms such as HP, Sun, and PCs. Prices start at $45,000 per MVS-based system. ML

Eastern Systems, 160 East Main St., P.O. Box 1087, Westboro, MA 01581; (508) 366-3223; fax: (508) 366-1520; e-mail: eastern@world.std.com.

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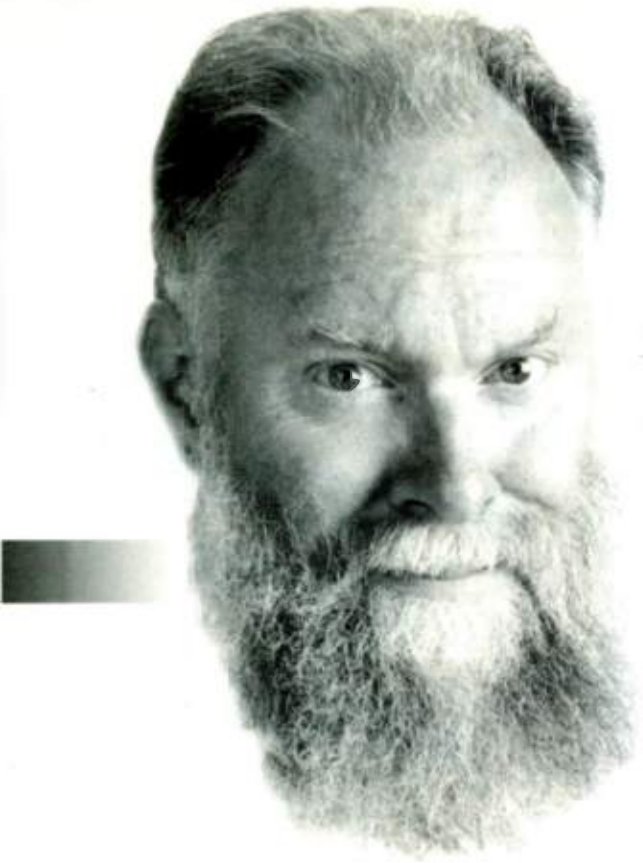

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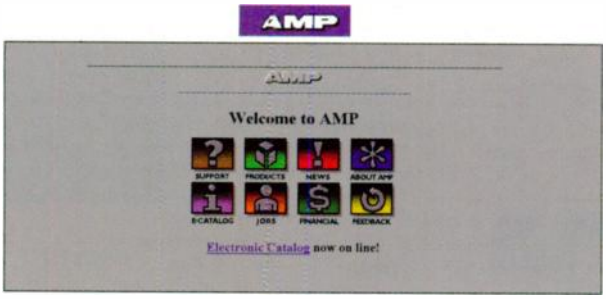

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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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CIRCLE 250

C&K COMPONENTS, INC.

CERAMIC RESONATORS

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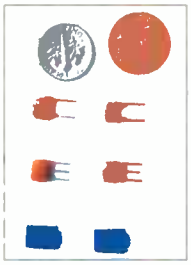
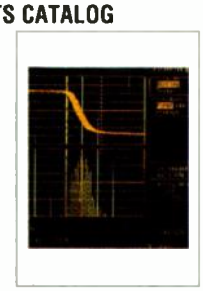


INTEGRITY TECHNOLOGY

CIRCLE 251

FREE T&M PRODUCTS CATALOG

The 1997 catalog from Lecroy offers complete technical information and pricing on our complete line of digital oscilloscopes. Also included are technical application notes covering many topics. 1-800-4LECROY



LECROY

CIRCLE 252

MOLDED PLASTIC PRODUCTS

New catalog features complete line of transfer, compression, and injection molded encapsulation shells and related services for electronic packaging. Included are sections on molding and tooling, standard products, mechanical and electrical properties of DAP and epoxies used in standard products, and available design, fabrication, screw machining, molding, tooling, terminal insertion, insert molding, drilling, and inspection/deflashing services.

CIRCLE 253

MARYLAND PLASTIC PRODUCTS

1997 PRODUCT SELECTION GUIDE

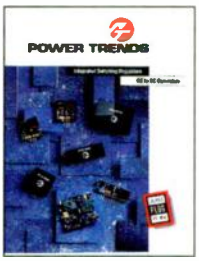
Pentek's new pocket-size 1997 Product Selection Guide describes Digital Signal Processing and Data Acquisition products for VMEbus, VXIbus and PCI/PMC bus. You'll find quick selection guides, capsule specifications and functional block diagrams. Get the latest information on the broadest line of DSP processors, I/O peripherals and world-class software tools. Send for your free copy today, or call (201) 818-5900 Ext. 532.

PENTEK, INC.

CIRCLE 254

NEW SWITCHING REGULATORS

Power Trends Inc., has released a new 80 page full line catalog for its Integrated Switching Regulators (ISRs) and DC to DC Converters. The catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product, along with mechanical configuration options and ordering information.



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POWER TRENDS INC.

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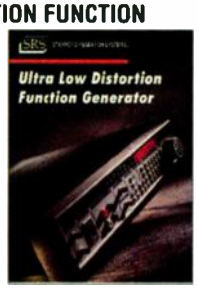

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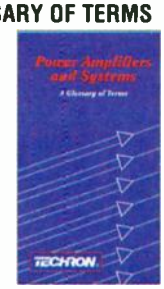
Variety of top return-on-investment engineering software,e.g.. SAUNA>thermal design and analysis; SUPERFILTER>filter synthesis and analysis; SPICEAGE>mixed mode simulator. These and many more described. Call for catalog, demo/evaluation pkgs.: Tel : 313-663-8810

TATUM LABS, INC.

CIRCLE 257

HANDY POCKET GLOSSARY OF TERMS

Techron, a manufacturer of power amplifiers and related systems for commercial applications, has developed a glossary of power amplifier terms. The illustrated document, available free from Techron, contains over 300 definitions-helping to provide a common ground of understanding among people with varying degrees of technical knowledge. For more information call (219)294-8300



TECHRON

CIRCLE 258

OMRON RELAYS, SWITCHES, MORE

Standard Product Catalog shows Omron's most popular relays, switches, and sensors. The 176-page catalog also includes card readers, time delay relays, totalizers, limit switches and temperature controllers. Literature sent only to addresses in the U.S.A. Omron Electronics, Inc. Call toll-free 1-800-55-OMRON or e-mail EDLit@oei.omron.com

CIRCLE 259

OMRON ELECTRONICS, INC.

SWITCH MODE INDUCTOR HANDBOOK

This 2nd edition of Torotel's Switch Mode Power Supply Inductor Handbook provides design guidance for over 600 inductors for power output filters, series mode power, common mode filtering and current sense applications. Phone: (816) 761-6314

TOROTEL PRODUCTS

CIRCLE 260

SWITCH CATALOG

APEM's 212 page catalog contains many extensive product lines. Included are the following categories; DIP & Rotary DIP switches, Toggle, Rocker & Lever switches, Pushbutton switches and more. A wide selection of process compatibles and SMT models are offered as well as numerous options and accessories. In addition, a broad family of Control knobs is also offered. Complete specifications and detailed ordering guides for all products greatly simplify selection.

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APEM

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CAD-MIGOS SOFTWARE

CIRCLE 262

ECLIPTEK CRYSTALS, OSCILLATORS

The International Source Book offers detailed specifications on Ecliptek's through-hole and surface-mount crystals, oscillators, and inductors. Visit our internet site at http://www.ecliptek. com/ecliptek/. Phone (714) 433-1200, Fax (714) 433-1234, or E-mail ecsales@ecliptek.com

ECLIPTEK CORPORATION

CIRCLE 263

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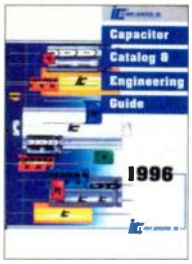
YOUR COMPANY

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

ILLINOIS CAPACITOR'S CATALOG

Illinois Capacitor's and Engineering Guide contains complete information on company's aluminum electrolytic, film, ceramic and power capacitors. It's all you need to make a knowledgeable capacitor selection. Available capacitance range, voltage ranges, operating temperature, case styles, IC authorized distributor listings, 208 pages.

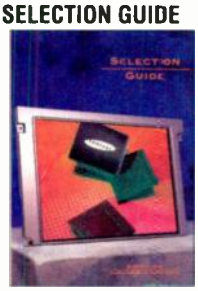


CIRCLE 265

ILLINOIS CAPACITOR, INC.

SAMSUNG PRODUCT SELECTION GUIDE

The latest catalog is available on request by calling 1-800-446-2760. It contains product and ordering information on Memory, Micro, TFT-LCD, ASIC and RE/Microwave products offered by Samsung Semiconductor, the world's leader in memory products.



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SAMSUNG SEMICONDUCTOR

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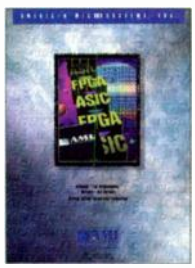
NETRANS™ and NETRANSplus™ from American Microsystems, Inc. provides proven netlist conversion technology. With over 800 FPGA to ASIC conversions to date, AMI has the most experience and greatest success rate for netlist conversions. For more information on NETRANS products, call (208) 233-4690 or visit our home page http://www.amis. com.

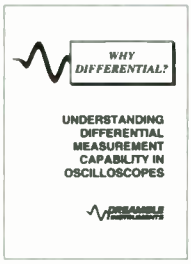


CIRCLE 267

AMERICAN MICROSYSTEMS INC.

DIFFERENTIAL MEASUREMENTS

A discussion of single-ended and differential scope measurements on ground referenced and floating signals. Differential amplifier characteristics such as common mode rejection ratio and common mode range are covered. 1-800-376-7007



CIRCLE 268

PREAMBLE INSTRUMENTS

MicroSim PSpice A/D with Schematics

Interface Technologies distributes the newly released Version 6.3 MicroSim PSpice A/D with Schematics. Version 6.3 supports network licensing for Windows 95 and Windows NT, IGBT device models, TOM-2 GaAs model, AMD MACH5 support, library browser and search engine, and full cross probing with MicroSim PCBoards. Call 1-800-357-1636 or browse http://www.i-t.com for more information.

CIRCLE 269

INTERFACE TECHNOLOGIES

AIN INSIGHTS INTO FUTURE TRENDS

This 14-page discussion of the competitive landscape created by the Telecom Act of '996 examines trends and technologies affecting the telephony market. Heurikon Corp., a division of Computer Products, Inc., used its communication system product development experience, customer and prospect interviews to develop this overview.

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HEURIKON CORPORATION

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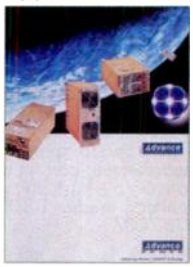
POWER SUPPLY CATALOG

Advance Power's 1996/97 Power Supply Catalog contains specs on units ranging from 15W to several kilowatts—including the new Kestrel VWF350 multi output switch-mode power supplies. Catalog also features a complete line of rectifiers for telecom applications.



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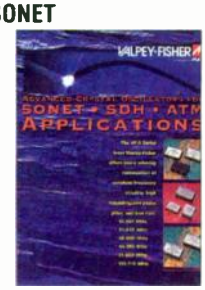

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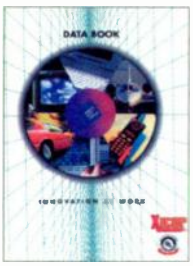

CIRCLE 274

XICOR

RF/IF DESIGNER'S GUIDE

180 page RF/IF Designer's Guide is loaded with informative features such as practical articles, definitions of terms, environmental and reliability test procedures, answers to frequently asked surface mount technology questions, and more! It also contains the most complete and up-to-date specifications and price information about all Mini-Circuits signal processing components. To receive a free Designer's guide, simply call (718) 934-4500

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MINI-CIRCUITS

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CIRCLE 276

PROTEL TECHNOLOGY

HI PERF CABLE ASSEMBLIES

Brochure for engineers needing to know the current level of advanced capabilities in the integrated design and manufacture of miniature cables and high density terminations.

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PRECISION INTERCONNECT

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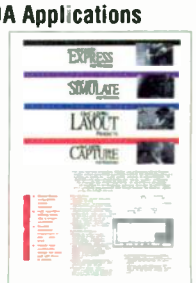

CIRCLE 279

OrCAD

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

ITHERMAL CLAD DESIGN GUIDE

New for 1996, Bergquist Thermal Clad Design Guide features the New Bond Ply Family of materials as well as updated technical information on Thermal Clad, Insulated Metal Substrate. THERMAL CLAD materials allow designers to reduce the number of thermal interfaces in the assembly and take advantage of the high thermal conductivity of the metallic layers of THERMAL CLAD.

CIRCLE 280

BERGQUIST COMPANY

CRYSTAL OSCILLATOR CATALOG

A new product catalog and selection guide from Champion Technologies features their full line of crystal oscillators. Technical information, specifications and mechanicals are featured in this catalog for over 60 of Champion's VXCOs, TCXOs, VCTCXOs, data clocks and related products. Frequency ranges up to 155.52 MHz for general purpose to high frequency or tight stability applications.
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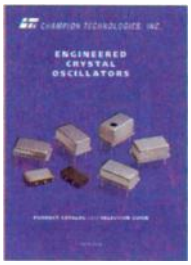

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CHAMPION TECHNOLOGIES

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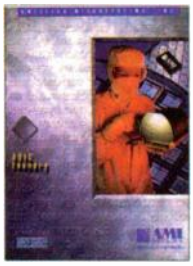
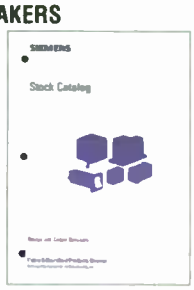


CIRCLE 282

AMERICAN MICROSYSTEMS INC.

P&B®RELAYS & BREAKERS

Catalog lists stock relays and circuit breakers from Potter&Brumfield® products Division. Describes electromechanical, solid state and time delays, as well as thermal and magnetic circuit breakers. Numerous options. Fax: (812) 386-072,e-mail:info@ae.sec.siemens.com



CIRCLE 283

SIEMENS ELECTROMECHANICAL

MECHANICAL ENCODER SOLUTIONS

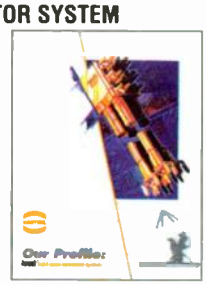
New Product Bulletin #698 lists the Series 25, single and multi-deck encoders. The Series 25 offers Binary, Binary Compliment and Gray code outputs in 1 deck through 4 decks. Choose from 4 to 36 switch positions for the selected code output. For an economical alternative, The Series 25L, single deck design, provides similar coding and position choices. The Series 25L is priced at $1.25 in production quantities.

CIRCLE 284

GRAYHILL

MINI COAX CONNECTOR SYSTEM

New 4-color brochure graphically illustrates the new har-pak® Mini Coax connector System. Color photographs, detailed technical data, drawings and part numbers provide comprehensive information.

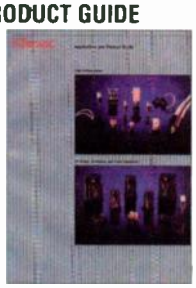


HARTING ELEKTRONIK INDUSTRIES, INC.

CIRCLE 285

APPLICATION AND PRODUCT GUIDE

Free 84-page catalog features detailed specifications on Kilovac's full line of high voltage relays, contractors and power controllers. Whether your applications call for 28V or 70,000V; isolation or power switching, Kilovac can meet your needs. Phone:(805) 684-4560, Fax: (805) 684-9679

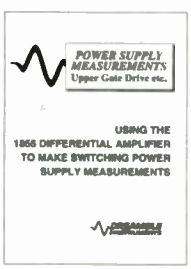


CIRCLE 286

KILOVAC

APPLICATION NOTE

Covers how to make safe and reliable measurements on switching power supplies operating on line, Includes such difficult measurements as upper gate drive and transistor saturation characteristics. Tells how to quantify measurement corruption caused by high dv/dt common mode. 1-800-376-7007



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GAGE APPLIED

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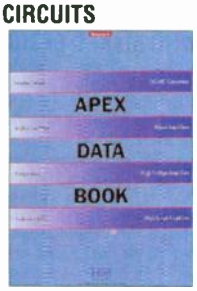
The 7th edition Apex Power Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's Power Amplifier, PWM Amplifier and DC/DC Converter product lines. Call: 1-800-862-1021; FAX: 1-520-888-3329; E-MAIL: Prolit@TeamApex.com.



CIRCLE 289

APEX

AUTOMATIC DATA COLLECTION

A 60 page, four color catalog from Intermec Corp. Everett, WA, the world leader in Automatic Data Collection technology. This new catalog includes thermal transfer bar code printers, scanners, handheld computers, network controllers, radio frequency data collection systems and much more.

CIRCLE 290

INTEMEC CORPORATION

FREE Instrumentation Reference

The National Instruments 1997 catalogue features the latest versions of the company's LabVIEW® , LabWindows®/CVI, and HiQ® application software products. New products include Bridge VIEW™ and Lookout™ software packages for industrial automation. In addition, our new line of IMAQ™ products features a complete hardware, software, and driver software solution for imaging.

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NATIONAL INSTRUMENTS

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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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MICROMINT, INC.

M/S ASIC CAPABILITIES

The Mixed-Signal Division of American Microsystems, Inc., is continually improving its analog, digital, and mixed-signal design and simulation tools. Adding cells to its cell library, reducing cost and time required to develop mixed-signal ASICs. For more information on MPD, call **(208) 233-4690** or visit our home page http://www. amis.com

CIRCLE 296

AMERICAN MICROSYSTEMS

RELIABILITY PREDICTION

Catalog describes the RelCalc2 software package, which automates Mil-HDBK-217 or Bellcore on your PC, and allows quick and easy reliability analysis of your electronic products.
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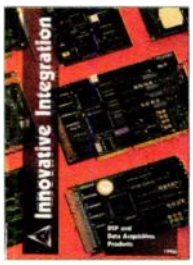

CIRCLE 298

INNOVATIVE INTEGRATION

FREE SPICE NEWSLETTER

The Intusoft newsletter is a free publication dedicated to discussing topics related to the spice circuit simulators. Each issue contains application notes, technical articles, and modeling techniques that help engineers simulate.

CIRCLE 299

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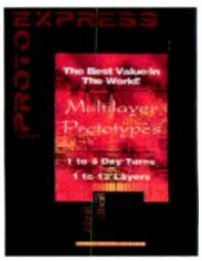

CIRCLE 301

PROTO EXPRESS

RELIABILITY SOFTWARE

The Relex Reliability Software for Microsoft Windows and the Mac provides Reliability Predictions per the MIL-HDBK-217, Bellcore, Mechanical, and CNET standards, as well as FMEA/FMECA analysis and Maintainability Predictions. The new four color 20-page catalog describes the flexible CAD Interface, extensive parts libraries, and stunning graphics.

CIRCLE 302

INNOVATIVE SOFTWARE

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DATA I/O

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CIRCLE 304

MASTER BOND INC.

IN CIRCUIT EMULATORS

Nohau Corporation is a manufacturer of In-Circuit Emulators for the following families: 8051, MCS251, P51XATM, 80C196, 68HC16, and 683XX families. Web Site Address:
http://www.nohau.com

CIRCLE 305

NOHAU CORPORATION

80186, 80196,8051 EMULATION

Signum Systems has released its 1996 catalog of in-circuit emulators. This full line catalog includes Intel processors, Texas Instruments DSP'sZilog controllers, and National Semiconductor HPC family. Call (800) 838-8012 for information. Internet address: ww.signum.com

CIRCLE 306

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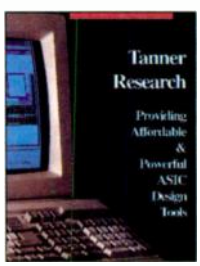

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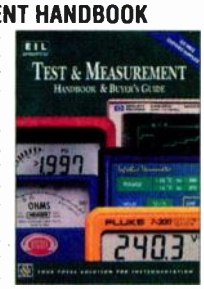

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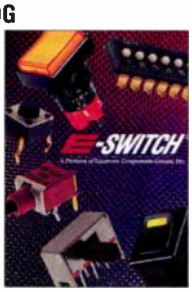

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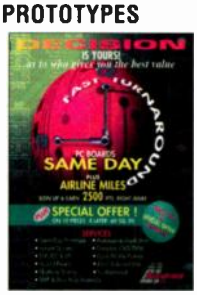

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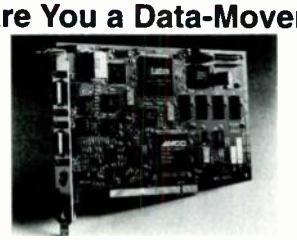

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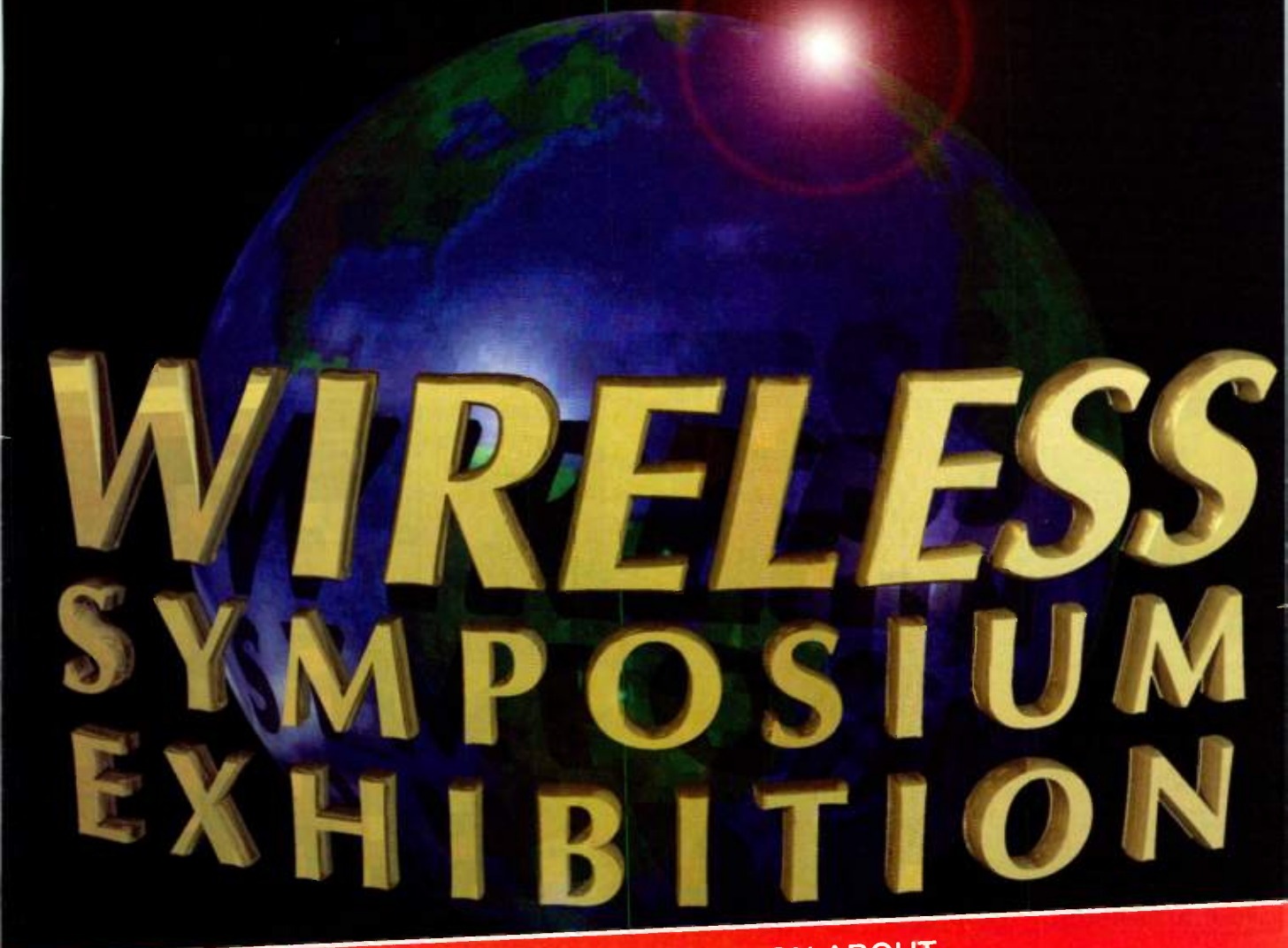

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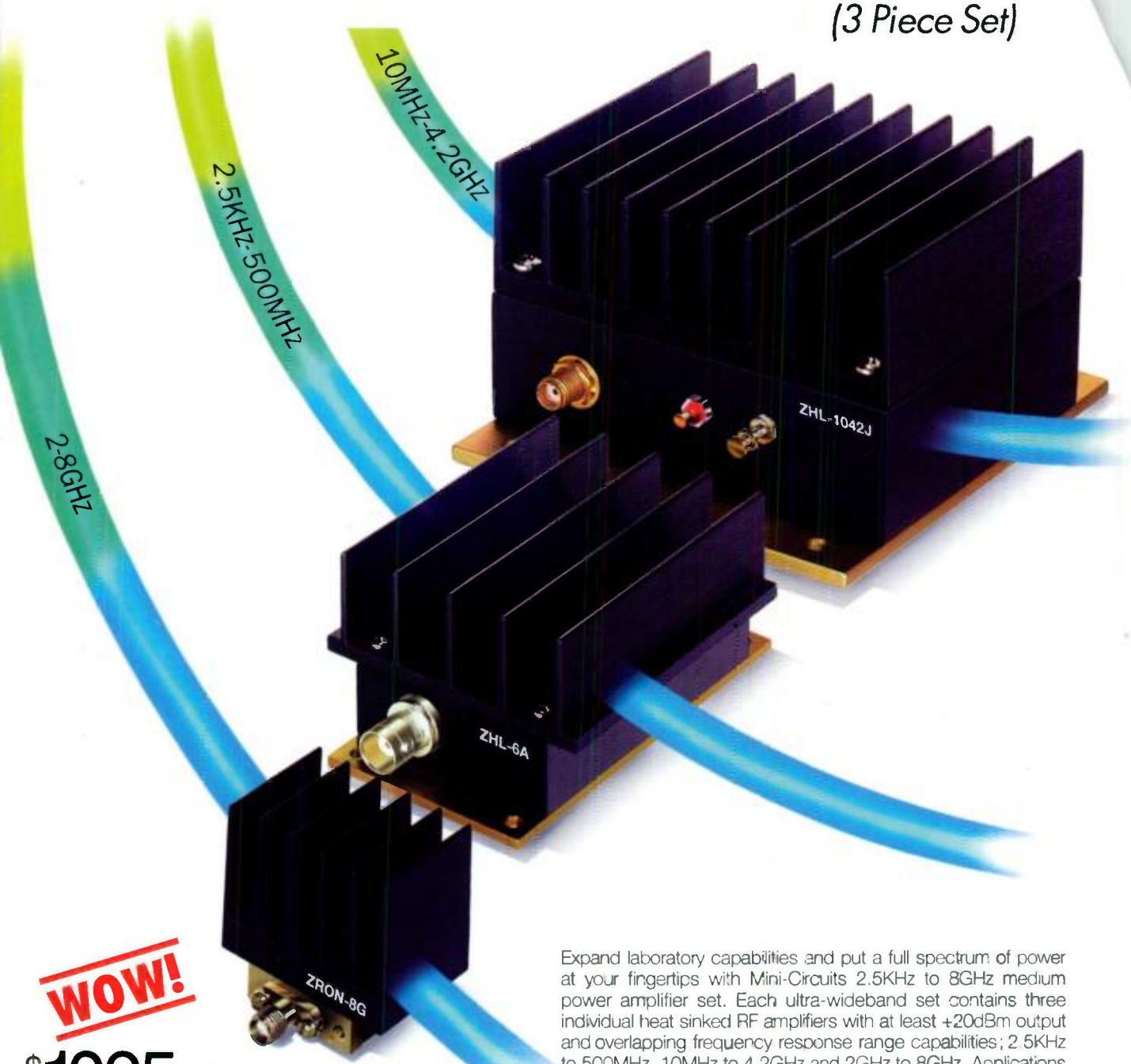

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