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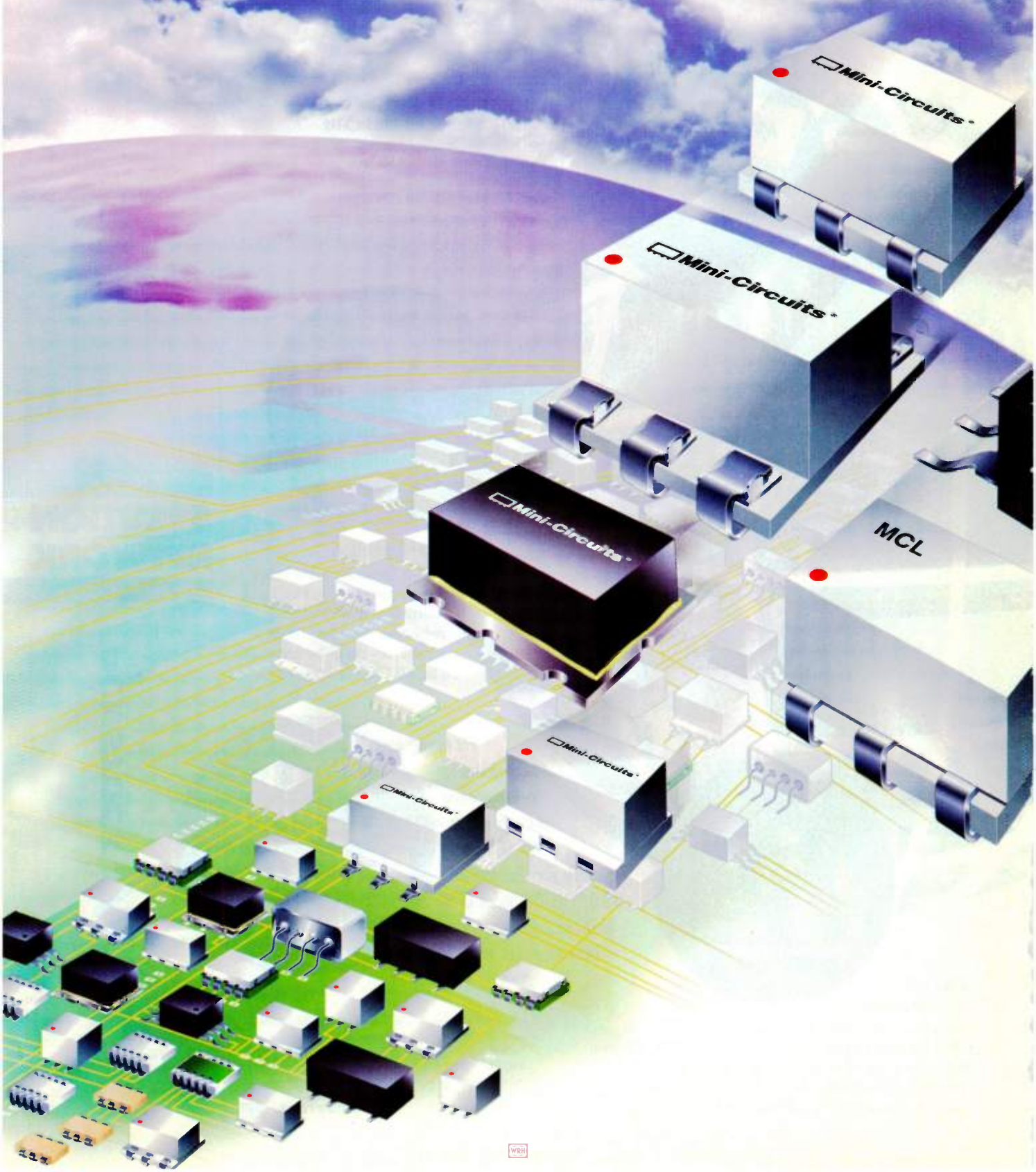
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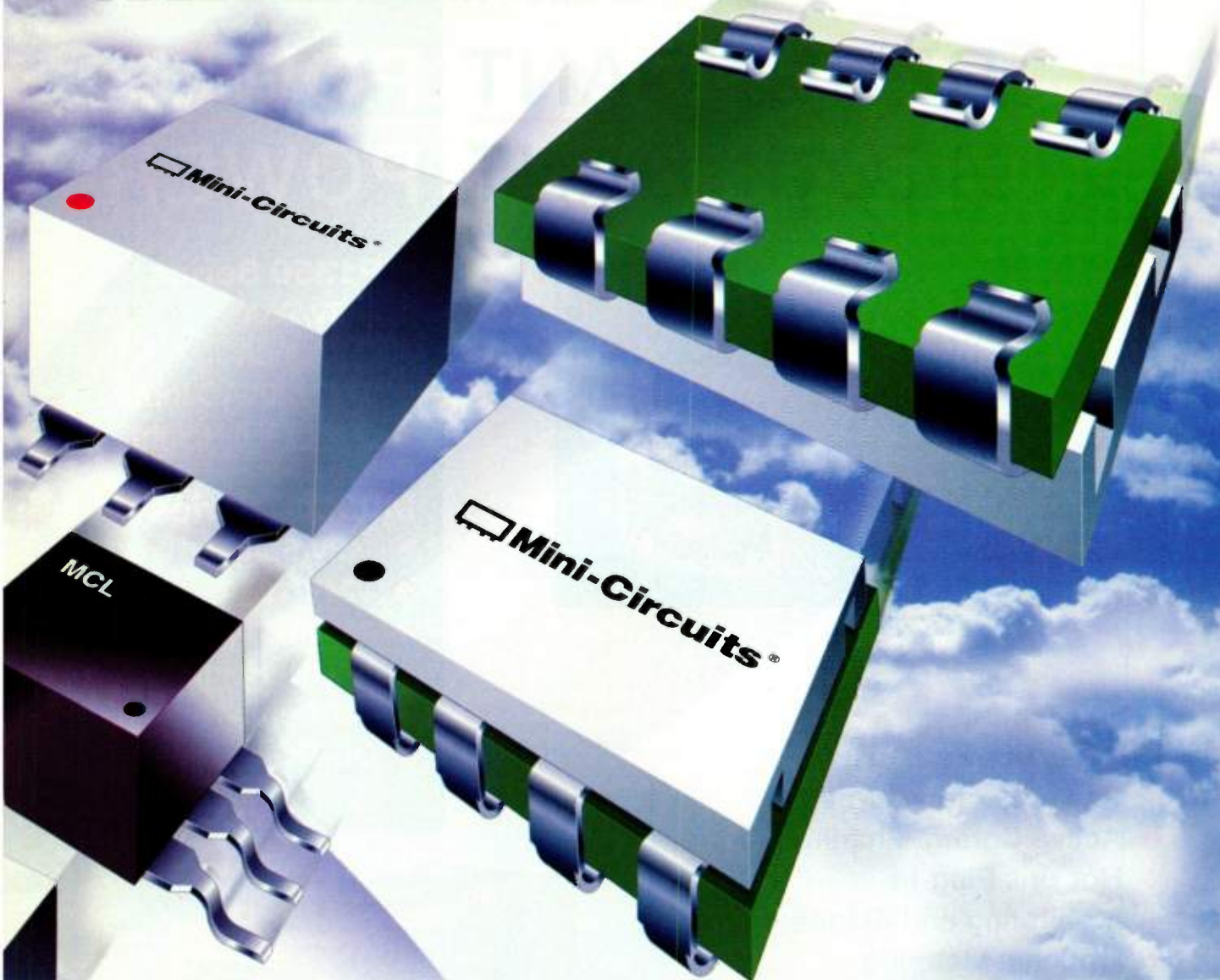
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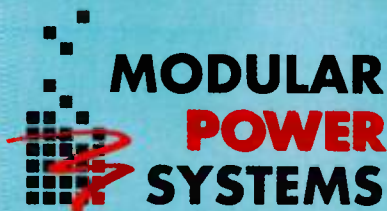
- ◆ -48V/25A
- ◆ +24V/50A
- ◆ 110/220VAC Input
- ◆ 5.25" (3U) Height

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- ◆ +24V/125A
- ◆ 220VAC Input
- ◆ 7" (4U) Height
- ◆ 16" Depth
- ◆ DC-DC Models

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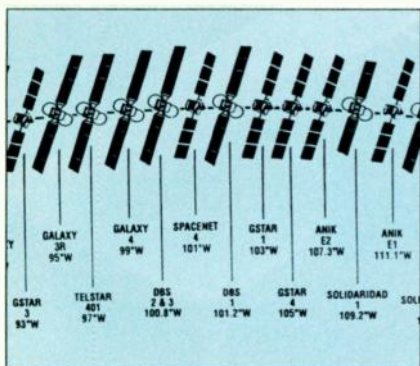
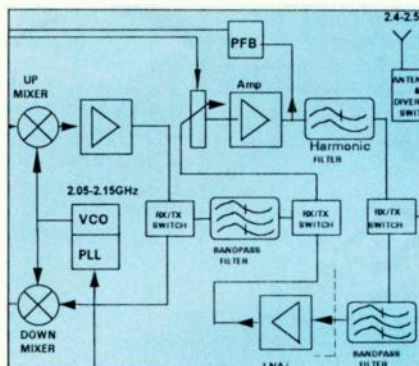
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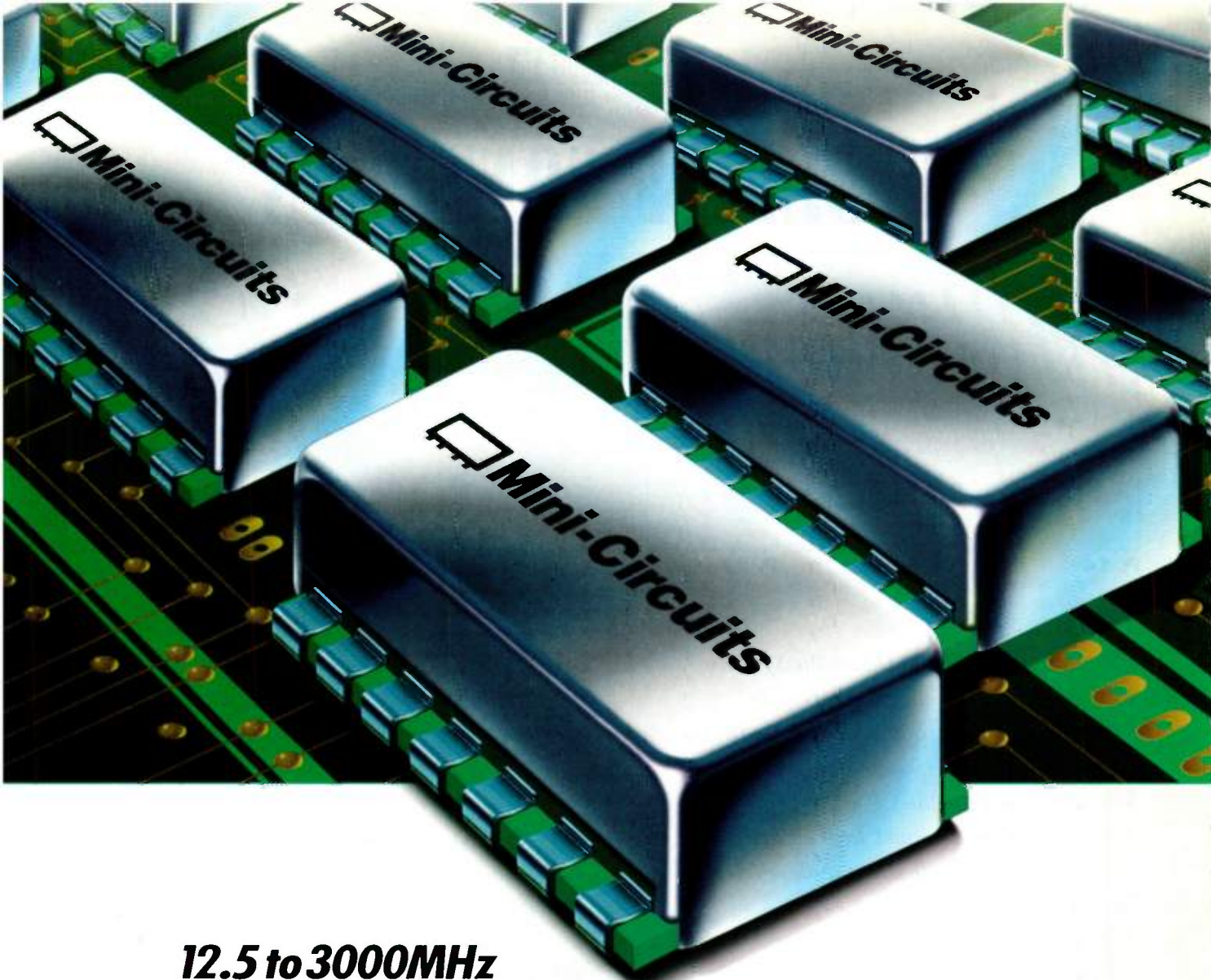
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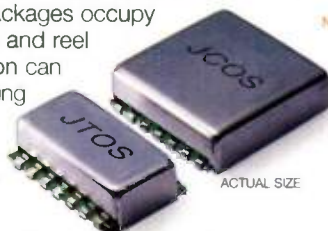
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12.5 to 3000MHz SURFACE MOUNT VCO's from \$13⁹⁵

Time after time, you'll find Mini-Circuits surface mount voltage controlled oscillators the tough, reliable, high performance solution for your wireless designs. JTOS wide band models span 12.5 to 3000MHz with linear tuning characteristics, low -120dBc/Hz phase noise (typ. at 100kHz offset), and excellent -25dBc (typ) harmonic suppression. JCOS low noise models typically exhibit -132dBc/Hz phase noise at 100kHz offset, and phase noise for all models is characterized up to 1MHz offset. Miniature J leaded surface mount packages occupy minimum board space, while tape and reel availability for high speed production can rocket your design from manufacturing to market with lightning speed. Soar to new heights...specify Mini-Circuits surface mount VCO's.



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JTOS/JCOS SPECIFICATIONS

Model	Freq. Range (MHz)	Phase Noise (dBc/Hz) SSB@ 10kHz Typ.	Harmonics (dBc) Typ.	V _{CC} 1V to:	Current (mA) @+12V DC Max.	Price Sea. (5-49)*
NEW JTOS-25	12.5-25	-115	-26	11V	20	18.95
JTOS-50	25-47	-108	-19	15V	20	13.95
JTOS-75	37.5-75	-110	-27	16V	20	13.95
JTOS-100	50-100	-108	-35	16V	18	13.95
JTOS-150	75-150	-108	-23	16V	20	13.95
JTOS-200	100-200	-105	-25	16V	20	10.95
JTOS-300	150-300	-102	-28	16V	20	15.95
JTOS-400	200-380	-102	-25	16V	20	15.95
JTOS-535	300-525	-97	-28	16V	20	15.95
JTOS-765	485-765	-98	-30	16V	20	16.95
NEW JTOS-1000W	500-1000	-94	-26	18V	25	21.95
JTOS-1000	665-1025	-94	-28	16V	22	18.95
JTOS-1200	900-1300	-95	-23	20V	30	18.95
JTOS-1500	1200-1850	-95	-20	13V	30	19.95
JTOS-1910	1625-1910	-92	-13	12V	20	19.95
JTOS-2000	1370-2000	-95	-11	22V	30 (16V)	19.95
JTOS-3000	2300-3000	-90	-22	---	25 (16V)	20.95
JCOS-820WLN	780-800	-112	-13	---	25 (16V)	49.95
JCOS-820BLN	807-832	-112	-24	14V	25 (10V)	49.95
JCOS-1100LN	1079-1114	-110	-15	---	25 (16V)	49.95

Notes: *Prices for JCOS models are for 1 to 9 quantity. **Required to cover frequency range. ***Tuning Voltage for JTOS-3800 is 0.5 to 12V, JTOS-820WLN and JCOS-1100LN is 0 to 20V. For additional spec information, and details about 5V tuning models available, consult RF/IF Designer's Guide or call Mini-Circuits.

DESIGNER'S KITS AVAILABLE

K-JTOS1 \$149.95 (Contains 1ea. all JTOS models except JTOS-25, -1000W, -1300 to -3000).
K-JCOS2 \$39.95 (Contains 1ea. JTOS-50, -100, -200, -400, -535, -765, -1025).
K-JTOS3 \$114.95 (Contains 2ea. JTOS-1300, -1850, -1910).

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INTRODUCTION

Earlier this year, *Electronic Design* and its sister publications, *Microwaves & RF* and *Wireless Systems Design* magazines, sponsored technical conferences and associated products exhibitions: The Portable By Design Conference and Exhibition and the Wireless Symposium and Exhibition. These two conferences presented technical papers written by the top designers in their respective fields. This supplement recounts the highlights of those two conferences and the products that were exhibited.

Basically, this supplement comprises a series of half-page summaries of many of the most significant papers presented at the two conferences. The papers chosen for such treatment were those which best lent themselves to this brief treatment: A single, important illustration or table, along with an edited version of the author's description, as published in the proceedings. Unfortunately, many excellent papers could not be summarized in this brief fashion. For the information contained in those papers, we refer readers to the full Proceedings for each conference.

This supplement also contains a reprint of an article that appeared in *Electronic Design* as a preview of the Portable By Design exhibits. Written by *Electronic Design* Computer Systems Editor Richard Nass, the article covers the many important devices and other products that were on display at the show.

Readers may want to make note of the date of the fact that, in 1998, the two shows will run simultaneously at the Santa Clara Convention Center, from February 9-13. Each will have its own technical program, while the exhibits area will be a joint effort. The technical programs for the 1998 Portable By Design Conference and the Sixth Annual Wireless Symposium are now being planned. If you are involved in designing portable electronic equipment or deal with devices or systems for wireless applications, we encourage you to share your experience with other designers by delivering a paper at one of the two conferences. You also should consider attending some or all of the sessions or workshops as well as take advantage of the opportunity to visit the exhibitors' booths in the show areas to discuss the vendors' latest products aimed at the portable and wireless marketplaces.

We hope readers find this Supplement, with its retrospective tour of the two 1997 conferences, useful.

STEPHEN E. SCRUPSKI
Editorial Director

Motorola Analog



High Voltage PFC Controller Saves Power

MC33368. A high voltage GreenLine™ active Power Factor Correction (PFC) controller functioning as a boost preconverter in off-line power supply, lamp ballast and battery charger applications. Integration of the high voltage startup function typically saves 0.7 W of power compared to resistor bootstrapped circuits. The MC33368 limits EMI to agency requirements, can be turned on/off and has control/protection features including under-voltage lockout, output overvoltage sensing allowing no-load operation, cycle-by-cycle current limiting, and a programmable output switching frequency clamp.

✓ Box letter A on coupon



Octal Serial Switch has SPI Input/Output

MC33298. This eight output low side power switch interfaces directly to a microcontroller, with control and fault reporting through an 8-bit Serial Peripheral Interface (SPI) port. Used to control various inductive and incandescent loads in automotive or industrial applications as well as control systems for robotics, each switch has a 3.0 A peak current output. Using SMARTMOS technology, the MC33298 has very low standby current, cascable fault reporting, an internal 65 V clamp on each output, independent shutdown of the outputs, and output-specific diagnostics.

✓ Box letter B on coupon



ICs Manage Power for GaAs MESFETs

MC33169. A support IC for GaAs Power Amplifier Enhanced FETs used in portable phones such as GSM, PCN and DECT. The device provides negative voltages for full depletion of MESFETs as well as a drain switch priority management circuit to protect the power amplifier.

MC33128. A power management controller for battery powered pagers and cellular phones. It has a low dropout voltage regulator with power-up reset for MPU power, two low dropout regulators to power analog and digital circuitry independently, and a negative charge pump regulator for full depletion of GaAs MESFETs.

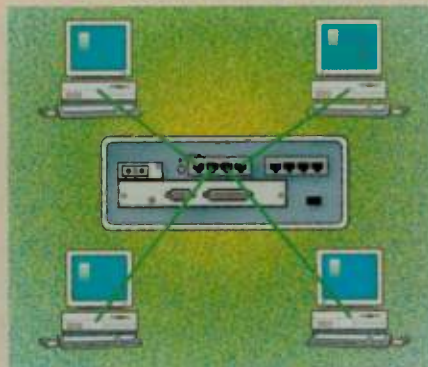
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Low Dropout Regulators Power Portables

Our family of LP2950/2951 micropower low dropout voltage regulators has grown. We've added 3.0 and 3.3 V fixed and adjustable voltage versions to our previous 5.0 V offerings. In addition, all three fixed voltage versions of the LP2950 series are now *uniquely* offered by Motorola in the DPAK surface mount power package. The low input-to-output differential voltage of 380 mV at a 100 mA load current, with a low bias current of 75 μ A, makes these devices ideal for battery operated and portable electronics such as cellular and portable phones, two-way radios, laptop computers, PDAs and camcorders.

✓ Box letter G on coupon



EEST Enables Two-Chip Ethernet Solutions

MC68160. Enhanced Ethernet Serial Transceiver (EEST) combines a serial interface adapter with an Ethernet transceiver. The EEST gluelessly interfaces to any one of Motorola's family of Integrated Communications Controllers, including the MC68EN302, MC68EN360 or MPC860EN, to provide a simplified two-chip solution for a completely functional Ethernet interface. The two chips offer the perfect internetworking solution for smart Ethernet hubs, branch offices and multi-protocol routers, remote access routers and industrial control networking.

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Hard Disk PRML Read Channel IC Achieves 200 Mbps Data Rate

The MC34250 is a fully integrated Partial Response Maximum Likelihood (PRML) 5 V hard disk drive read/write channel IC for high end mass storage applications. Using our advanced mixed mode 0.5 micron BiCMOS process technology, this analog implementation achieves 50 to 200 Mbps data transfer rates with only 800 mW of power dissipation in a single 10mm by 10mm 64-pin thin quad flat pack (TQFP). The IC is designed for zoned-recording applications requiring high linear densities and spindle speeds of up to 10,000 rpms.

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Product Review #2



1.8 V Rail-to-Rail™ Sleep-Mode™ Op Amp

The MC33304 quad op amp not only operates with a single 1.8 V supply, but can operate in a low standby power "sleepmode" state with a drain current of only 110 μ A per amplifier. When an input signal causes an amplifier to source or sink at least 200 μ A, it automatically switches to the "awakemode" state, allowing it to source or sink 70 mA to the load. The amplifier will automatically revert to the sleepmode when I_{out} drops below the threshold, and still operates as a micro-power amplifier. The MC33304 can swing within 100 mV of the input and output rails.

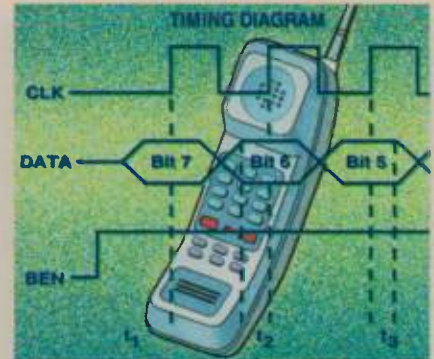
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Narrowband FM IF Receiver Eliminates Coil

MC13150. This narrowband FM IF subsystem IC has a coilless demodulator that eliminates the need for a conventional tunable quadrature coil, while providing better noise, linearity and AM rejection than traditional circuitry. The device allows many adjustments with non-precision external resistors and capacitors. Targeted at cellular and other narrowband applications such as PCMCIA wireless modems, the MC13150 provides a high level audio output of up to 2 V with a 3 V supply at a very low drain current of less than 2 mA, and an outstanding 0dBm input IP3.

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Programmable Line Interface IC for Cordless Phones and Digital Systems

The MC34016 is an ideal interface between an analog phone line and a codec in digital systems. Useful in digital cordless phones or modems, the IC provides improved noise and distortion figures. The adjustment of transmission parameters to conform to a variety of international standards is done with two 8-bit registers, accessible via a SPI bus and with external components. The device has double sidetone architecture and supports passive or active AC set impedance applications.

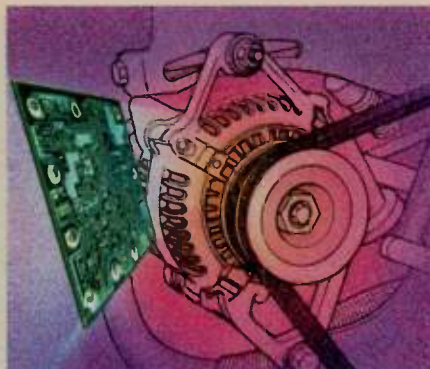
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PIP IC Provides TV Feature at Low Cost

The MC44461 Picture-In-Picture (PIP) controller IC provides a single-chip, low cost solution to a very complex, value-added TV feature. Designed with our 0.8 μ m BiCMOS process, the device contains all the analog signal processing, control logic and memory necessary for the overlay of a small picture from a second non-synchronized source onto the main picture of a TV. The MC44461 is NTSC compatible with all control and setup functions for the IC accomplished via a standard two-pin IIC bus interface. The IC implements switchable main and PIP video signals and two PIP sizes.

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Alternator IC Works in Harsh Environment

MCCF33095/MC33095. Flip-Chip/Surface Mount regulator control ICs are designed for use in automotive 12 V alternator charging systems, and need only a few external components for full system implementation to control the field current of a variety of alternators. Both ICs have internal detection and protection features to help withstand harsh physical and electrical automotive environments. Flip-Chip technology allows the MCCF33095 to operate at higher ambient temperatures than the SOIC version, and both withstand vibration and thermal shock with high reliability.

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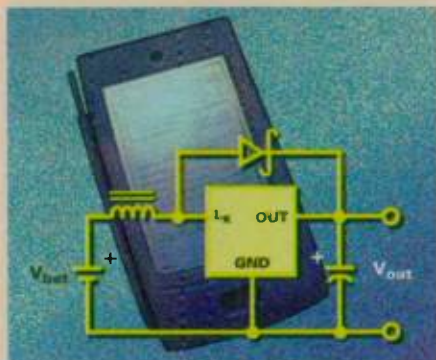


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Micropower CMOS DC-DC Converters Simplify Design of Portable Products

The MC33463/33466 series of micropower switching voltage regulators are available in 3.0, 3.3 and 5.0 V options, and are ideally suited for battery powered computer, consumer and industrial equipment. Both families are available in three-pin SOT-89 packages, with either an on-chip switch transistor or provisions for an external switch. The MC33463 devices are Variable Frequency Modulation controllers with a quiescent bias current of 4 μ A, while the MC33466 devices are Fixed Frequency PWM switchers with a quiescent current of 15 μ A.

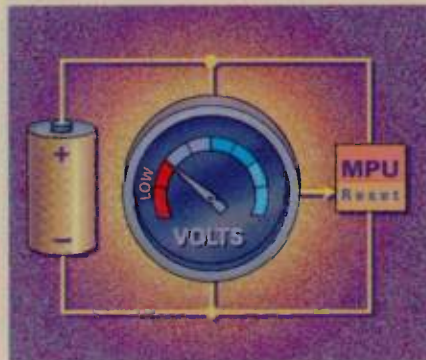
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Three Families of CMOS Micropower Linear Regulators have Ultra-Low I_q

MC78LCxx/78FCxx/78BCxx. Three series of micropower linear voltage regulators are designed for use in cameras, camcorders, VCRs, and hand-held communication products, and include voltage options of 3.0, 3.3, 4.0 or 5.0 V. The MC78LCxx series has an 80 mA output current, a dropout voltage of 0.7 V at 40 mA, and is available in SOT-23 or SOT-89 packages. The MC78FCxx family has an output current of 120 mA, dropout of 0.2 V, in a SOT-89. The MC78BCxx series is available in a SOT-23 and is designed for use with an external power transistor for higher output currents.

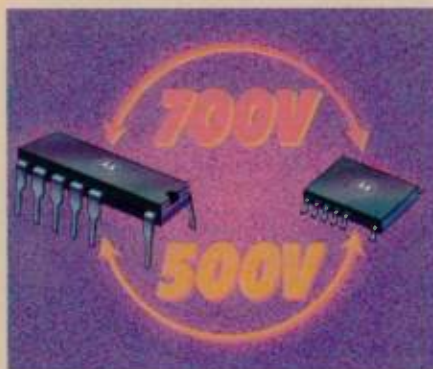
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CMOS Micropower Undervoltage Sensing Circuits Monitor MPU/Logic Supplies

The MC33464/33465 families of micropower undervoltage sensing ICs are designed for direct monitoring of MPU/logic power supplies in portable, appliance, automotive and industrial equipment. Both series are available with threshold voltages of 0.9, 2.0, 2.7, 3.0 and 4.5 V with a choice of open drain or complementary CMOS reset output configurations. The MC33464 family has a low quiescent current of 0.8 μ A and is available in SOT-23 or SOT-89 packages. The MC33465 series adds a programmable time delayed output, has a quiescent current of 1.0 μ A, and is packaged in a SOT-23.

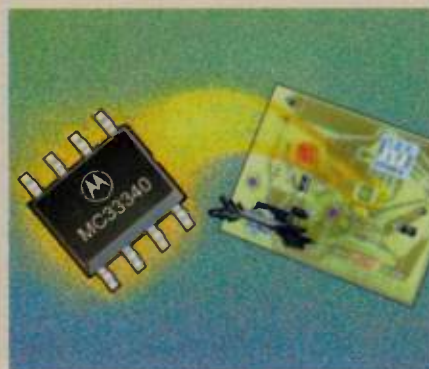
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High Voltage Switching Regulators Simplify Design of Off-Line Supplies

MC33362/33363. These ICs are designed to operate from a rectified AC line source for off-line power supplies, or from a high voltage source for DC-DC converter applications. The MC33362 is designed for rectified 120 Vac line operation and features an on-chip 500 V, 2.0 amp SenseFETTM power switch. The MC33363 is designed for 240 Vac rectified line operation with a 700 V, 1.0 amp SenseFET. Both devices are available in 16-lead through-hole and surface mount packages with pins eliminated to achieve high voltage spacing requirements.

✓ Box 7 on coupon



Battery Fast Charge Controller Simplifies NiCd and NiMH Charging

The MC33340 is specifically designed for fast charging of Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries using negative slope voltage detection. Accurate charge termination is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. The IC also supports secondary charging methods of either programmable time or temperature limits. Protective features include battery over and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout. A rapid test mode enhances end product testing.

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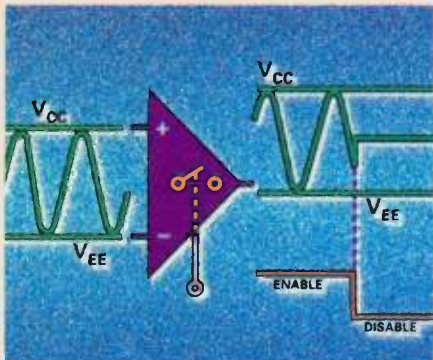
Subminiature Package Trims Board Space

We offer a variety of products in the new Micro-8 subminiature surface mount package. This package uses 50% of the board area of a traditional SO-8 surface mount package, and is narrower than TSSOP miniature packages. The LP2951 adjustable micropower low dropout voltage regulators, and MC33264 low dropout micropower regulators with on/off control are available in the Micro-8 package. The MC34064/34164 undervoltage sensing/micropower undervoltage sensing circuits, and the TL431A,B programmable precision references are also available in this space-saving package.

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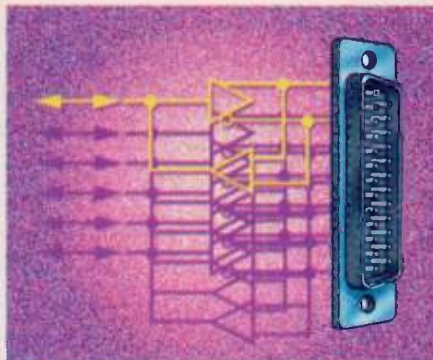
Product Review #3



Dual/Quad 1.8 V Rail-to-Rail Op Amps have Enable Feature to Extend Battery Life

MC33206/33207. These dual/quad op amps not only have input *and* output rail-to-rail capability, but also an enable mode that can be controlled externally. Typical drain current is $\leq 1.0 \mu\text{A}$ per amplifier in the standby mode, saving power and extending battery life. Each op amp in the MC33206 has its own enable pin, and the op amps in the MC33207 are enabled in two pairs. These amplifiers can operate with supplies as low as 1.8 V and ground, yet can still operate with a single supply voltage as high as +12 V.

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Hex Transceiver Meets SCSi-3 Fast-20 Specs

The new MC34059 contains six differential driver and receiver pairs in a 48-pin QFP for transmission of differential signals at 20 MBPS, meeting the requirements for SCSi-3 Fast-20 transmission systems. Control lines can enable/disable each driver and receiver as required, and an over-temperature sensing circuit will shut down any driver that gets too hot due to ambient temperature or a prolonged short circuit. The low quiescent current of 18 mA saves power in hard disk drive, backplane communications, and computer-to-computer data transmission applications.

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Low Cost FM Communications Receivers

MC13135/13136. These low cost, single chip, dual conversion FM receivers can be used as stand-alone VHF receivers or as the lower IF of a triple conversion system, with a low 2.0 V supply. The MC13135 is designed for use with an LC quadrature detector, while the MC13136 can be used with either a ceramic discriminator or an LC quad coil. Applications include cordless phones, radio controlled toys, baby monitors, walkie-talkies and scanners.

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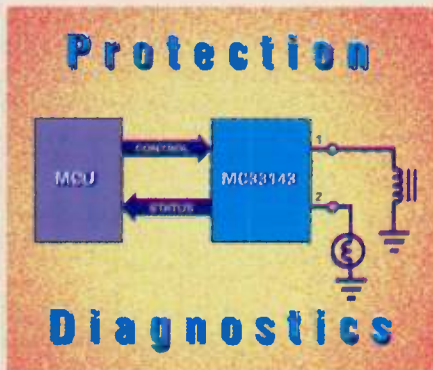
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New PIP IC Enables TV Feature Versatility

The MC44463 Picture-In-Picture (PIP) controller IC provides a wide variety of feature options that are all *software programmable*, requiring no printed circuit board changes. When combined with external memory, the device controls a replay mode of up to eight seconds that can be played back at four different speeds. The IC provides options of a single PIP, in either active or replay mode; and three or four PIPs, with one active and the remaining PIPs in a freeze-frame mode. In the multi-PIP mode, the user can choose which of the three or four PIPs is active.

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Dual High Side Switch has Protection and Diagnostic Features

The MC33143 dual high side switch is designed for solenoid control in harsh automotive applications, but can also be used to control incandescent lamps, relays, and small motors. This SMARTMOS™ IC has an on-chip charge pump to enhance switch performance, and an externally controlled Sleep-Mode™ for power savings. Each output has individual overcurrent and over temperature shutdown with automatic retry. The device detects and shuts down globally with any overvoltage condition. It also detects and indicates an open load or output short to the supply.

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Millimeter-Wave LEO Satellite Systems

The Table summarizes the information required by the ground-station antenna designer for some of the major upcoming communication satellite systems that have a significant millimeter-wave content. With the advent of low-Earth-orbit systems like Motorola's Iridium, which require sophisticated beams, LEO satellites may soon be carrying phased arrays and reflector antennas. The use of millimeter-wave frequencies allows these structures to be small and therefore more easily deployed on satellites.

The Teledesic system has by far the most millimeter-wave content. Using a constellation of several hundred low-Earth-orbit satellites, a global, broadband “Internet-in-the-sky,” Teledesic will enable affordable access to fiber-like telecommunications capability anywhere in the world. Approximately 840 satellites in 21

planes in sun-synchronous, inclined circular low earth orbits provide the services. Rather than targeting voice and supporting low bit-rate data as Odyssey and Iridium do, Teledesic focuses on providing wireless broadband services with a fiber-like quality, focusing on data and supporting voice.

The user terminal antennas have a diameter ranging from 8 cm to 1.8 meters, and an average output power ranging from 0.01 W to 4.7 W. The antenna diameter is determined by maximum output power, maximum channel rate, climatic region and availability requirements.

These proposed Ka-band LEO systems will offer the antenna designer a challenge to develop a large quantity of low cost millimeter-wave “user” antennas. More sophisticated (possibly scanning) antennas will be required for the gateways.

From "Antenna Technologies for New Millimeter-Wave Communications Systems," **John Sanford** and **Ray Blasing**, Endgate Corp., 1997 Wireless Symposium.

	Odyssey	Iridium	Teledesic
Mobile down-link frequencies (MHz)	2483.5 -2500.0 (S-band)	1616.0 -1626.5 (L-band)	Ka-band
Mobile up-link frequencies (MHz)	1610.0 -1626.5 (L-band)	1616.0 -1626.5 (L-band)	Ka-band
Feeder up-link frequencies (GHz)	29.1 - 29.4 (Ka-band)	27.5 -30.0 (Ka-band)	Ka-band
Feeder down-link frequencies (GHz)	19.3 - 19.6 (Ka-band)	18.8 -20.2 (Ka-band)	Ka-band
Inter-satellite Link (ISL) freq's (GHz)	N/A	22.55 -23.550	60
Beams per satellite	61	48	64 beams (supercells) 576 cells
Satellite antenna	Steerable, moving cells using directed coverage	Fixed, moving cells	Steerable earth-fixed cells
Orbit class	MEO	LEO	LEO
Altitude (km)	10354	780	695-705
Number of Satellites	12 + 3 spare	66 +6 spare	840 + up to 84 spare
Mobile terminal min. El. angle (deg.)	20	8.2	40

An Off-Line Flyback Power Supply

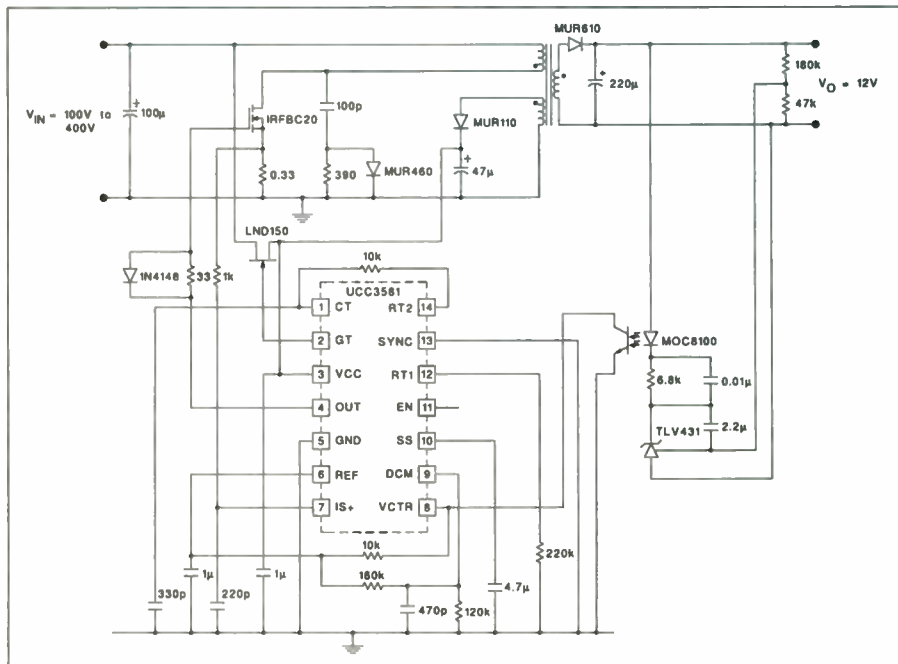
An off-line flyback power supply was designed for a nominal 50-watt load but with the added ability to operate efficiently at less than one-tenth that value, even with input voltages which can range from 85 to 280 V rms. The schematic for this application is shown in the figure.

Under nominal loading, this design runs with continuous inductor conduction at a fixed frequency of 100 kHz with a duty cycle which will vary from approximately 20% to 50% over the voltage range. The minimum pulse-width clamp was then set at just under the lower number at 1.8 msec by the action of the UCC3581 controller. In addition to changing the operation from fixed-frequency to fixed off-time, it should be recognized that there will also be a change from continuous to discontinuous inductor operation as the load drops to its standby mode. As can be seen from the

schematic, this design uses most of the techniques described above to reduce switching losses. Specifically, while the international input voltage range of this application requires a 600-V FET, the IRFBC20 has a total gate charge requirement of only 18 nC and its drain capacitance is held to 48 pF. The diode bypassing the gate resistance allows fast turn-off while slowing turn-on to ease the minimize the recovery characteristics of the output rectifier

While a dissipative snubber is shown, the frequency foldback of the circuit will reduce its loss contribution at light loading. Other loss-saving elements of this circuit include the use of the DN2530 depletion FET to remove startup power, and low current components on the secondary side.

From "Designing PWM Power Supplies for High Efficiencies At Micropower Levels," **Laszlo Balogh** and **Bob Mammano**, Unitrode Integrated Circuits. 1997 Portable By Design Conference.



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Rechargeable Alkaline Manganese Dioxide Zinc Cells

Intensive research and development activities carried out at Battery Technologies Inc. (BTI) and at the Technical University in Graz, Austria, in the late 1980s and early 1990s resulted in the successful commercialization of the rechargeable alkaline manganese dioxide zinc (RAM) system. BTI has sold licenses and production equipment for the manufacturing and worldwide marketing rights of its proprietary RAM technology. RAM cells are available, under BTI license, from Rayovac Corp., under the trademark Renewal in the U.S., Pure Energy Battery Corp., in Canada (Pure Energy trademark) and Young Poong Corp. (Alcava trademark) in South Korea.

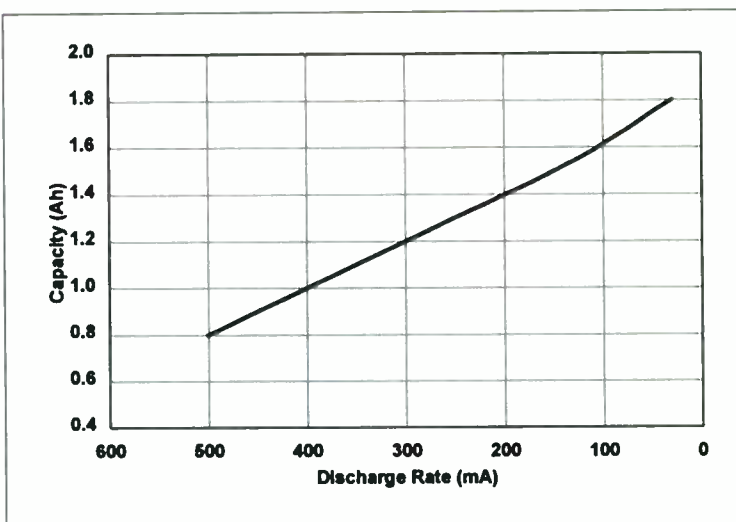
Depending on consumer use conditions, one RAM cell can replace 10 to 50 single-use alkaline or 30 to 150 single-use zinc-carbon cells.

The RAM system without mercury addition to the anode has reached a level of performance that rivals that of Ni-Cd batteries in consumer applications, especially in areas where intermittent operation at moderate loads and when an excellent shelf life at elevated temperatures is required. The more recent Li-Ion technology is not available as loose computer cells, but comes with OEM applications where sophisticated charge circuitry is required to ensure consumer safety.

In order to make rechargeable alkaline manganese dioxide zinc (RAM) cells function reliably in rechargeable operation, they are designed differently than single-use Alkaline Manganese cells. RAM performance on first discharge is usually 70% to 80% of the performance of single-use alkaline cells. The ampere-hour capacity of RAM cells increases with decreasing current rate, as shown in the figure. This also means that depth of discharge increases with decreasing current rate. Note also that the figure represents only the 0.9 V cut-off voltage.

RAM cells have a sloping discharge curve at all current rates. This provides a warning that cells need charging, e.g., by distorted sound, slower motor speed, dimmer light, etc. It also permits the use of simple low-battery warning circuitry. The discharge time and capacity of RAM cells decreases or fades with increasing number of discharge/charge cycles.

From "In-Application Use of Rechargeable Alkaline Manganese Dioxide/Zinc (RAM) Batteries," **Josef Daniel-Ivadj and Karl Kordes**, Battery Technologies, Inc. 1997 Portable By Design Conference.

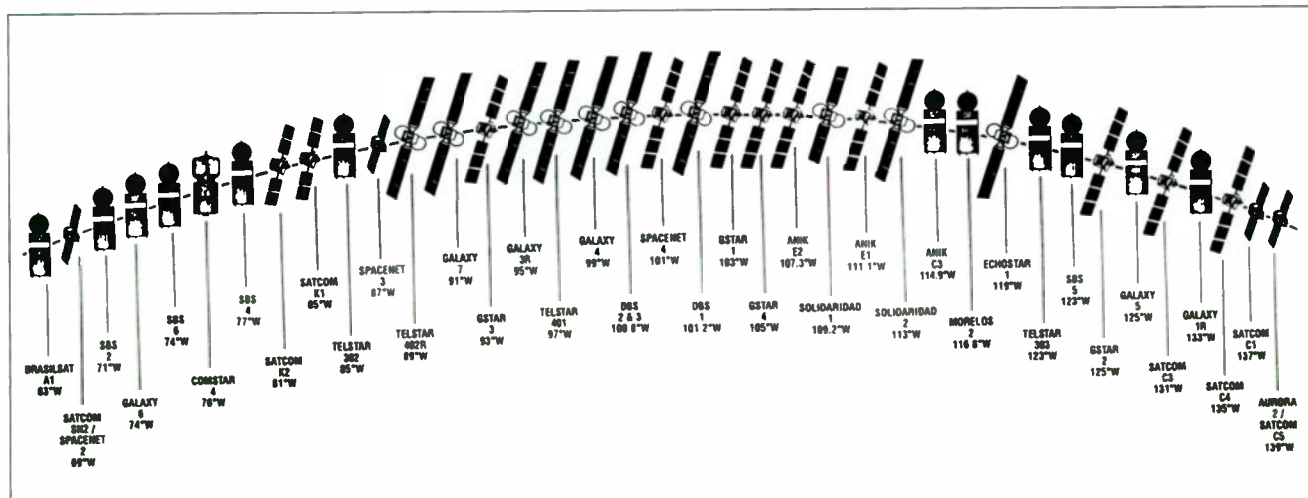


Identifying Satellites For Consumer Receivers

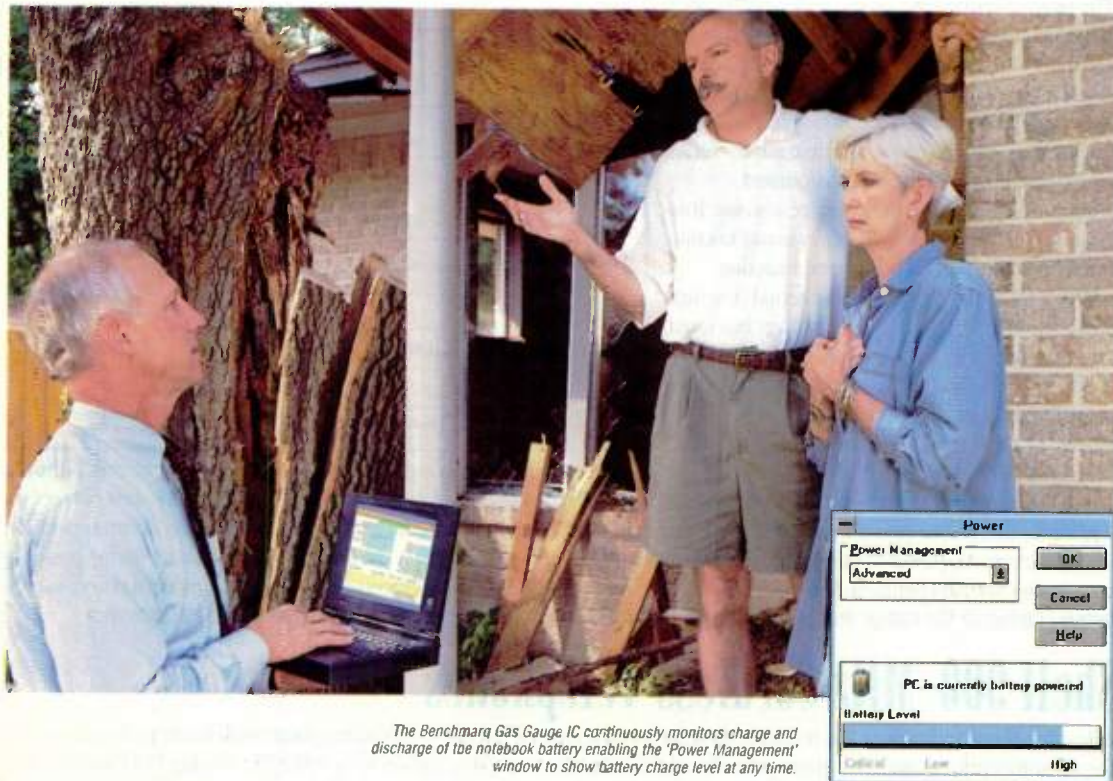
The figure shows a list of the available C/Ku band satellites over North America, ordered from east toward west. The Star Trak 800 consumer satellite receiver is able to automatically recognize some of about 44 North American C/Ku band satellites by adjusting the audio circuits to 7.02/7.11 MHz on which some satellites carry Morse code.

The audio signal is digitized and the receiver is able to move its antenna from east to west, to find and record maximum of signal strength, on both polarities and, in the reverse dish motion, to stop on peaked positions (where the satellites are) to listen to the Morse code and to identify satellite. In the group of 44 satellites, the receiver is able to recognize 6 to 12 satellites, while the positions of the others are calculated. The whole process takes about 20 minutes.

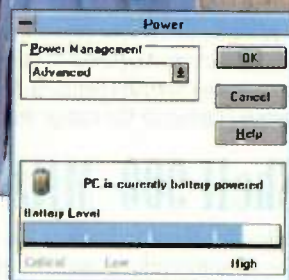
From "Automatic Satellite Identification for Consumer Analog Satellite Receivers," **Branko Kovacevic**, Tee-Comm "Electronics Inc. 1997 Wireless Symposium.



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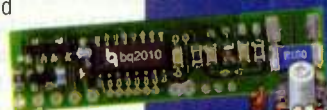
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bq2014	Gas Gauge IC with Ext. Charge Control	NiMH, NiCd and Li-Ion	16/0.150" SOIC
bq2050	Power Gauge™ IC	Li-Ion	16/0.150" SOIC
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Power Considerations In The USB

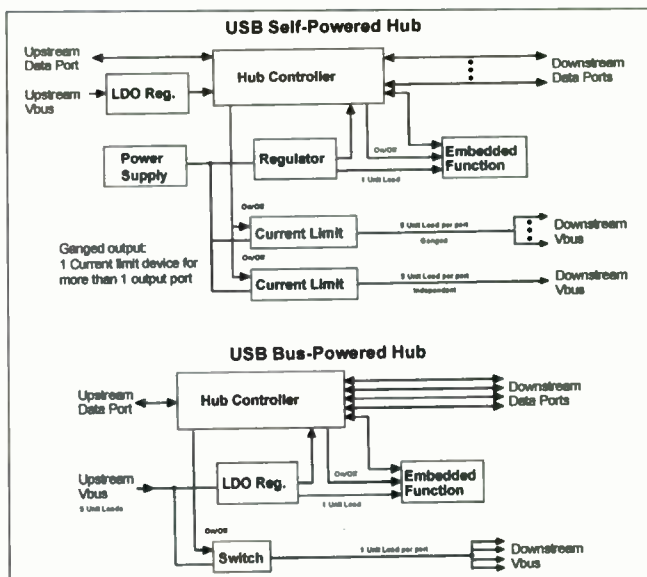
This paper provides an introduction to the Universal Serial Bus (USB) Interface as it relates to the power distribution requirements of the voltage bus. There are many requirements in the current USB specification (Version 1.0) concerning voltage regulation and the current limits of the system. The paper discusses the issues of the specification concerning real-world limitations and requirements for the voltage and current requirements of the USB voltage bus. The USB interface is a 12-Mbit/s multiplexed serial bus designed for low to medium speed PC peripherals. USB utilizes asynchronous and isochronous data transmission. USB is a four wire interface conceived for dynamic attach-detach (hot plug-unplug) of peripheral devices in the PC environment.

The USB specification provides for five basic device classes: Bus-Powered Hub, Self-Powered Hub, Low-Power/Bus powered Function, High-Power/Bus powered Function, and Self-Powered Function.

Bus-Powered Hub: Draws all of the power for all internal functions and output ports, for downstream loads, from its USB voltage bus input. A maximum of 500 mA can be drawn by a bus-powered hub. It will supply 100 mA (max.) to any downstream ports, and may consume any portion of the 500 mA, but limited to no more than 100 mA at power-up.

Self-Powered Hub: Power for the internal functions and downstream ports does not come from the USB voltage bus. The self-powered hub must be capable of supplying 500 mA to each of the downstream ports that it maintains. It may draw 100 mA from the bus to provide power to the USB interface. A host, by definition, is a self-powered hub. **Low power, bus-powered function:** All power to this device comes from the USB voltage bus. It may draw a maximum of 100mA (max.) during normal operation. **High power, bus-powered function:** All power to this device comes from the USB voltage bus. It may draw up to 100 mA (max.) during power up and up to 500 mA (max.) during normal operation. **Self-powered function:** host and SP hub devices receive power from an internal power supply.

From "USB Power Interface / Control Of The Voltage Bus," **Jonathan M. Bearfield**, Texas Instruments, Inc. 1997 Portable By Design Conference.

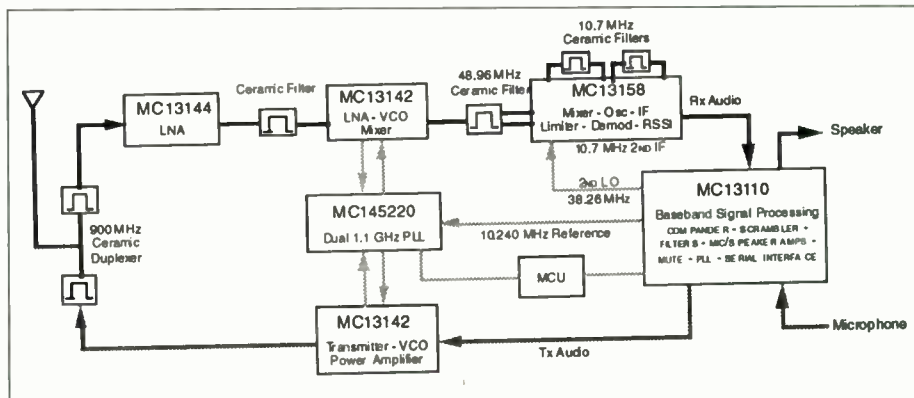


Off-The-Shelf 900-MHz Cordless Telephones

As 46/49 MHz cordless telephone technology has matured, there has been increased interest in a cordless phone with better performance over a longer distance in the consumer price range. This paper provides a brief, overall system description for a 900-MHz Analog FM Cordless Telephone. This design features a 900-MHz transmitter and dual conversion receiver and complete baseband signal processing. RF transmit and receive frequencies, and first and second IF frequencies were all selected based on filter availability. The channel spacing chosen for this application is 320 kHz, which allows for 10 channels within the given filter bandwidth and with an even division of the 10.24-MHz reference frequency. Narrower spacing may be used to increase the number of channels without using wider filters, however the wider channel spacing provides the fastest lock time and moves the reference spurs out on the PLL, in addition to better signal to noise ratio and receiver quieting with strong input levels. These features help provide a better quality telephone to the end customer and make use of the wider bandwidth allowed by the FCC in the 902-928 MHz band.

This chipset makes use of Motorola's MOSAIC5, MOSAIC 1.5 and 75% BICMOS process capabilities to achieve the maximum performance versus cost tradeoff. The receiver consists of an MC13144 Low Noise Amplifier (LNA) with 17 dB of gain and a 1.4 dB noise figure at 900 MHz, the MC13142 LNA/Down converter which is capable of another 14 dB of gain, and the MC13158 Down converter and Limiting IF/Demodulator. For the transmitter, the MC13142 has been reconfigured to provide the 900-MHz oscillator which is directly modulated using a varactor. The mixer is then unbalanced by pulling one input to ground through a 1.8-kohm resistor and it is used as an on-chip power amplifier. Both the MC13144 and MC13142 are fabricated on Motorola's low noise MOSAIC 5 RF process, while the baseband IC is designed in BICMOS to allow integration of the switched capacitor filters in the audio path and the digital control functions. The first LO frequency is high side injection to move it away from the US cellular frequency band, and is controlled by Motorola's MC145220 Dual 1.1-GHz Phase Locked Loop (PLL). The MC13110 performs the baseband signal processing for both the transmit and receive as well as providing the LO for the MC13158 and the MC145220 reference frequency.

From "Off-the-Shelf 900 MHz Cordless Telephone System: System Overview and Baseband Design," **Gaylene Phetteplace, David Babin, Rich Potyka, Harry Swanson**, Motorola Semiconductor Products Sector. 1997 Wireless Symposium.



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NDS8410A	NDS8435A	10	21	SO-8 
NDT455N	NDT456P	13	26	Power SOT 
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*SO-16 Contains 3 N-Channel and 3 P-Channel die in one package



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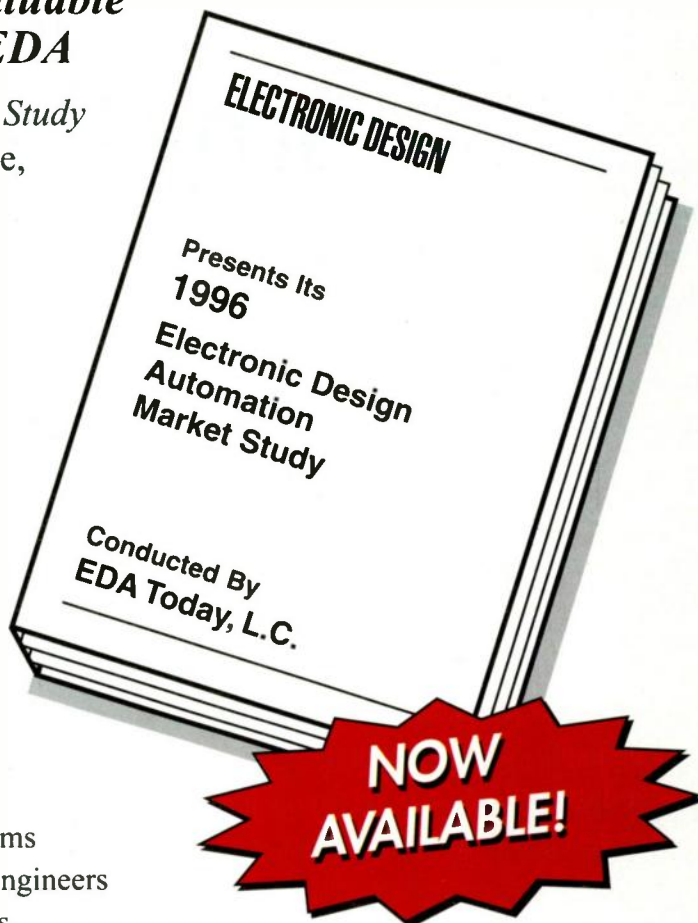
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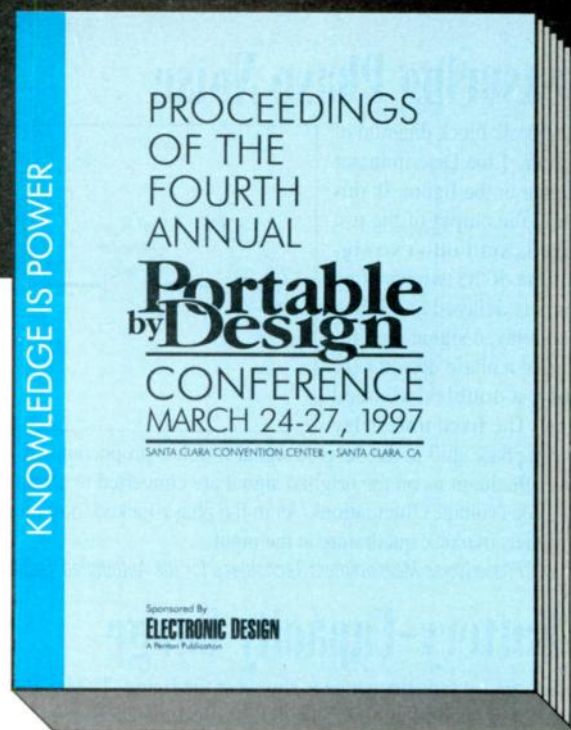
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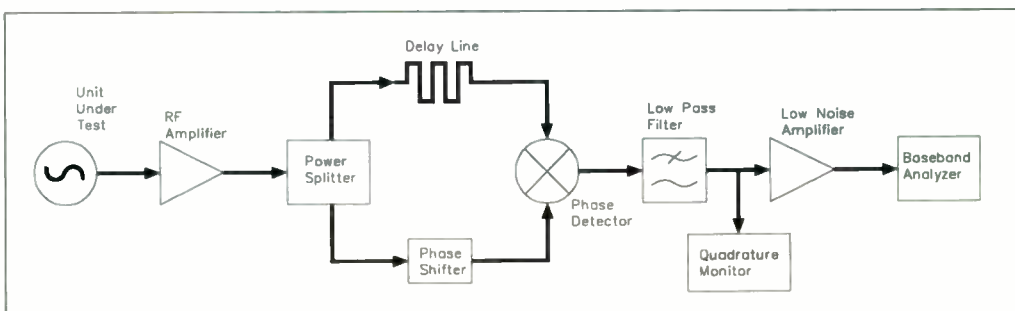
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Measuring Phase Noise

The basic block diagram of the Delay-Line Discriminator is shown in the figure. In this method the output of the test source is split into two signals. One of the two resulting signals is delayed and it and the undelayed signal are presented to a phase detector (as before, a double-balanced mixer).



causes a phase shift in the delayed signal which is proportional to the frequency. When compared to the undelayed signal from the other path, frequency fluctuations on the original signal are converted to phase fluctuations. These phase fluctuations are converted by the phase detector into amplitude (voltage) fluctuations. As in the phase-locked loop method, the phase-detector output is proportional to the input phase differences of two signals in phase quadrature at the input.

From "Phase Noise Measurement Techniques for the Automated Testing Environment," **Al Street and Joe DiBona**, RDL, Inc., 1997 Wireless Symposium.

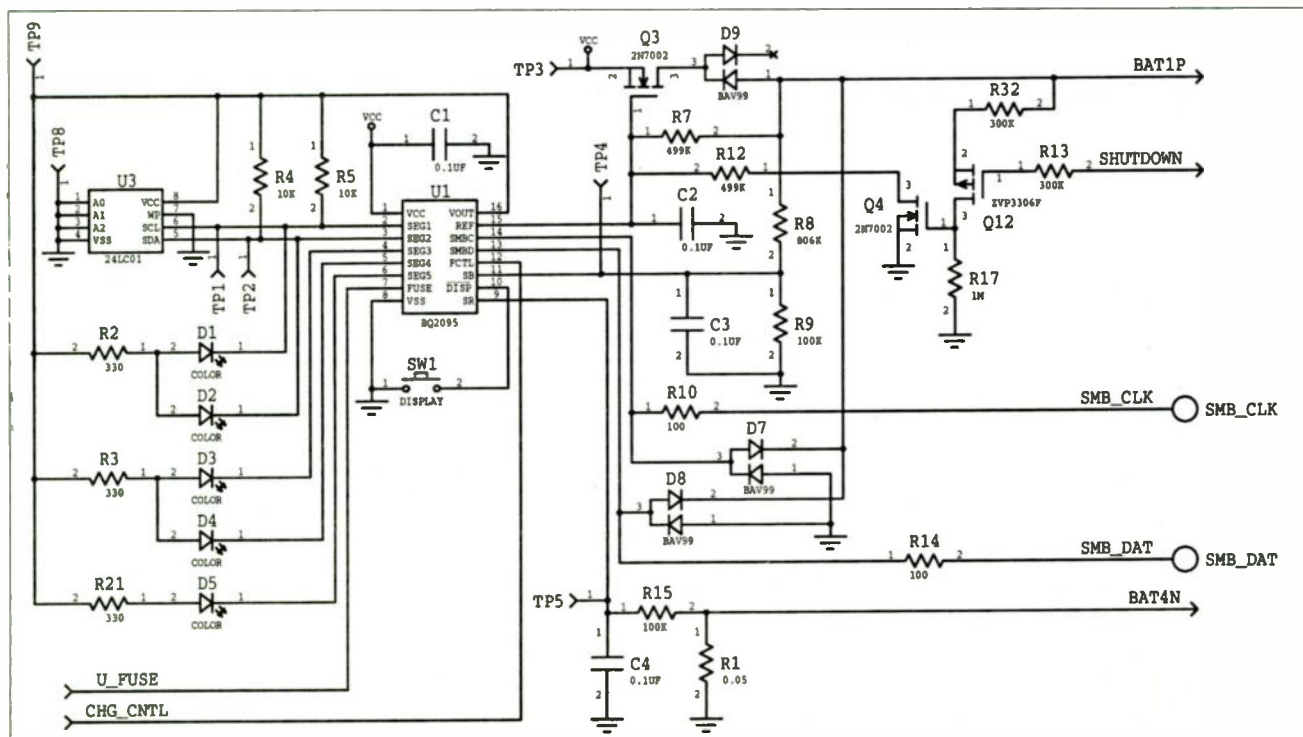
A Battery-Capacity Gauge

The primary capacity gauge is shown in the figure. The bq2095 monitors the current into and out of the battery by measuring the voltage drop across a low-value sense resistor, R1. The estimated charge replacement is compensated for rate and temperature. The remaining capacity is compensated under discharge for both rate and temperature. Self-discharge rate is compensated for temperature and capacity. The combining of the capacity gauge information with protector status provides complete battery management information.

The bq2095 may be used to test for charge FET failure. When fast charging is detected, the bq2095 turns off the charge FET and then monitors the charge current. If the charging current is found, then the a charge FET failure is indicated. The bq2095 capacity information can also be used to modulate the charge FET when the battery capacity indicates the battery is recovering from a deep discharge. During this time, the battery may be charged at a lower rate. The bq2095 broadcasts the required charge current to a smart charger. If a smart charger is not present, however, then the bq2095 is capable of adjusting the average current by modulating the charge FET.

When the battery is recovering from a deep discharge, the capacity gauge can be used to detect cell problems. After a small amount of capacity is returned to the battery, the bq2095 checks the battery voltage. If the battery voltage indicates that the state of charge does not agree with the capacity replacement, then a battery fault can be indicated. This provides the host system with diagnostics for the battery pack.

From "Integrated Pack Management Addresses Smart-Battery Architecture," **David Freeman**, Benchmarq Microelectronics, Inc. 1997 Portable By Design Conference.



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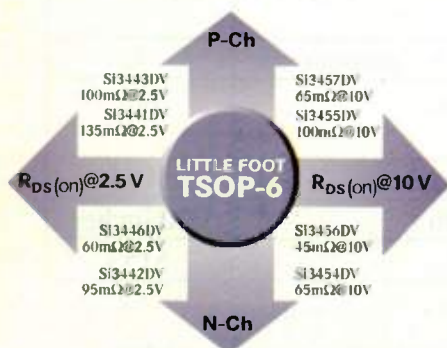
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A GaAs MESFET Voltage Converter

In DC-DC converter applications high efficiency and high switching speeds are of critical importance. For these applications we see GaAs MESFET technology having major advantages. We predict GaAs MESFET technology will make inroads into handheld applications such as cordless phones, cellular phones and pagers.

GaAs MESFET (Metal Semiconductor Field Effect Transistor) devices are similar to Si MOSFETs in that they are majority carrier devices. They switch quickly with no minority carrier storage as in bipolar devices. Because they are FETs they can act as switches in a charge pump configuration.

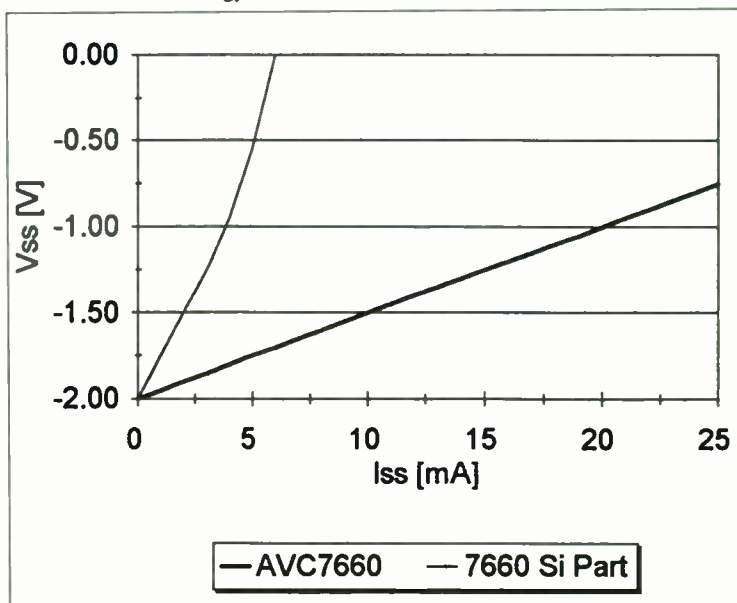
The primary advantages for using GaAs over Si are: low ON resistance; low voltage; fast switching speed; and semi-insulating substrate

The Anadigics AVC7660 GaAs dc-dc converter is the first product to leverage the advantages of GaAs technology in voltage conversion. This converter offers improved low voltage operation in a smaller package (SOT-25) than its silicon 7660-counterparts.

Typical silicon 7660 converters have a clock frequency of 10kHz and require 10- μ F external capacitors. The AVC7660 runs at 300kHz, resulting in smaller and lower cost hold and pump capacitors, typically on the order of 0.1 to 2 μ F. In fact, it now becomes feasible to use ceramic capacitors in some applications, thus saving cost and space. Use of the smaller SOT-25 package is made possible by the low ON resistance of GaAs MESFETs, resulting in a smaller transistor periphery and hence a reduced die size.

The figure shows how the output voltage of the AVC7660 converter changes with the load current. A typical silicon part is shown for comparison. The output impedance of the silicon part goes up exponentially with lower voltages, and the output voltage collapses at the same rate.

From "The Prospects For GaAs Mesfet Technology In Dc-Dc Voltage Conversion," **Shihab Al-Kuran**, Anadigics Inc. 1997 Portable By Design Conference.



An MCM Implementation Of A Processor Card

This paper discusses a multichip module implementation of a processor card that has a Pentium processor, L2 cache and PCI chip set as primary components. The module has been used in a commercial ultraportable design and has the attributes to be used in a high volume commercial application.

The MCM consists of an eight-layer L/D substrate with components mounted on both sides. The top side has the microprocessor, 2 SRAMs, PCI chip set and a thermistor. The bottom side has an inductor, tag RAM, several passive components and a 240-pin connector. The module interfaces with the mother board through the connector, which plugs into a socket on the mother board. Ideally, upgrading the system design involves unplugging the existing module and replacing it with the newer module. The module measures 50 mm by 50 mm on the sides, and has a mounting height of 9.5 mm.

The substrate consists of thin-film Cu / PI build-up layers on an FR-4 laminate core. The thin-film layers are used to route the signals and the laminate core houses the voltage reference planes. There are two thin-film build up layers on each side of the core and four copper planes inside the core, resulting in a total of 8 layers of metallization. The key attributes of the module are shown in the Table.

The Pentium processor and PCI chipset are highly reliable bare die, SmartDie technology, attached to the substrate using a flip chip technology called Bump Interconnect Technology (BIT). BIT is a peripheral flip chip technology that uses 85- μ m pitch gold bumps. The remaining devices are surface mountable packaged devices, attached using a conventional SMT process.

From "MCM's Shrinking Desktop Functionality To Portable Form-Factors," **Naveen Cherukuri**, Fujitsu Microelectronics Inc., and **Jeffrey P. Casazza**, Intel Corp. 1997 Portable By Design Conference.

Module Size	50 mm sq.
Module Height	9.5 mm
Module I/O	240
Total Power Dissipation	9.0 W
Number of Power Planes	2
Number of Ground Planes	2
Number of Signal Layers	4
Ave. Impedance of Signal Traces	36 Ω – 75 Ω
Number of Active Components	8
Number of Passive Components	127
Number of Connections	1086
Total Etch Length	600 inches
Number of Vias	5153

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Low-Power Modes Of Microprocessors For Handheld Systems

Motorola's Family of MPC8XX Processors incorporate many of the lessons learned from users' reactions to the first-generation PDAs. The MPC821 and MPC823 microprocessors combine all the peripherals on one chip and can operate at 2.0 V internally while the external buses run at 3.3 V. They also support a wide range of power management modes including: Full On, Doze, Sleep, Deep Sleep, and Low Power Stop. These are summarized in the figure.

In Full On mode, the processor is fully powered with all internal units operating at the full speed of the processor. Of course, the processor supports a PLL so the processor clock can be generated from a 32-kHz watch crystal and the operating frequency can be changed dynamically by the system software depending on the system performance needed. Doze mode further disables core functional units except the time base decremter, PLL, memory controller, RTC and LCD controller while placing the CPM in low-power standby mode. Sleep mode is the next lower power mode and disables everything except the RTC and PIT, leaving the PLL active for quick wake-up. The Deep Sleep mode additionally disables the PLL for lower power in systems. Low Power Stop disables all logic in the processor except the minimum logic required to restart the device, providing the lowest power consumption—less than 10 microwatts allowing the power to be removed from unused blocks until needed again.

The MPC821 and MPC823 processors also provide a separate set of power pins for the internal logic power rails in the device. These power pins can provide the device with a 2.0 V power source that can be used when the processor is operating at 25 MHz or less. This capability typically reduces the power consumption of the device by an additional 30%.

From "Considerations For Selecting A Microprocessor for Handheld Systems," Ken Edwards, Motorola. 1997 Portable By Design Conference.

Mode	Operating Modules					Wake-up Time	Power Consumption (mW)		
	Core CMMU	CPM	SIU	SPLL	Keep Alive		MPC821	MPC823	
Normal High						—	230	170	@25MHz
Normal Low						Asynchronous Interrupt 4 VCO/2 Clocks Synchronous Interrupt 4 System Clocks	120	90	@10MHz
Doze High							160	110	@25MHz
Doze Low							80	70	@10MHz
Sleep						4 VCO/2 Clocks	10	10	
Deep Sleep						<500 Osc. Cycles	40 μ	40 μ	
Power Down						<500 Osc. Cycles + Power-up	30 μ	30 μ	

Module Operating
 Module Clocks Stopped, No State Lost
 Module State Lost

An Integrated LCD Controller

This paper discusses the benefits of low-voltage one-time-programmable (OTP) microcontrollers using the PIC16C92X family and system tradeoffs required to operate LCD panels, time-of-day clocks and sensor interfaces. Topics for discussion include battery type determination, performance targets, and implementation tradeoffs including LCD panel.

The PIC16C924 provides several peripherals for low power interface. The figure shows a block diagram of the PIC16C924 system providing a keyboard input, LCD-based time-of-day clock, battery backup, temperature sensor, and piezoelectric audio alarm.

LCD panels provide many advantages over light-emitting diodes (LEDs) such as lower power, lower cost, and improved display quality. A major factor in the LCD advantage is the integrated charge pump that provides the panel voltage up to three times the power supply. Most LCD panels operate around 7 V for best display characteristics. Since the charge pump generates an increased voltage, a single lithium battery (3.0 V nominal) can be used to operate both the MCU and LCD panel during power interruptions. The charge pump requires only three external capacitors for operation.

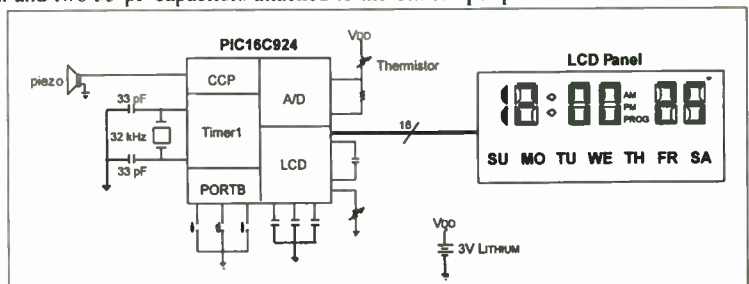
The time-of-day clock uses an external 32.768-kHz crystal and two 33-pF capacitors attached to the Timer1 peripheral module. Timer1 can be configured to operate with the external crystal during SLEEP mode for the rest of the system. In SLEEP mode at 32 KHz Timer1 consumes approximately 20 μ A. Once every 32,768 cycles (one second) Timer1 overflows and an interrupt is generated. The interrupt wakes the system from SLEEP, the time is updated and the system returns to the low power mode. (A complete listing of all software for the system is included in "AN649—Yet Another Clock Featuring The PIC16C924" from Microchip Technology Inc.)

The keys or keypad interface connects directly to the PORTB of the microcontroller. PORTB provides a wake-up on change feature for keypad interface. Internal weak pull-up resistors are included to reduce the external component count. When a change is detected on PORTB the process wakes from SLEEP and services the interrupt accordingly before returning to the low power mode.

The audio alarm system uses a piezo alarm driven by the Capture/Compare/Pulse-Width-Modulation (CCP) peripheral to provide sound feedback to the user during emergency events.

For temperature monitoring the system uses an external thermistor connected to the analog-to-digital converter (ADC) peripheral. Thermistors typically require several hundreds of milliseconds to stabilize at a given temperature so the 16- μ s conversion time is ideal for temperature measurements. For power management the ADC uses an internal RC oscillator for conversions during SLEEP mode. All other clocks can then be disabled until the conversion completes and the system wakes up to process the sample accordingly.

From "Integrated LCD Controllers Open Many Applications For 8-Bit Microcontrollers," Ron Cates, Microchip Technology Inc. 1997 Portable By Design Conference.



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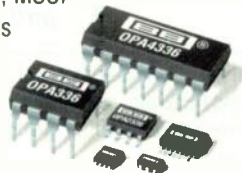
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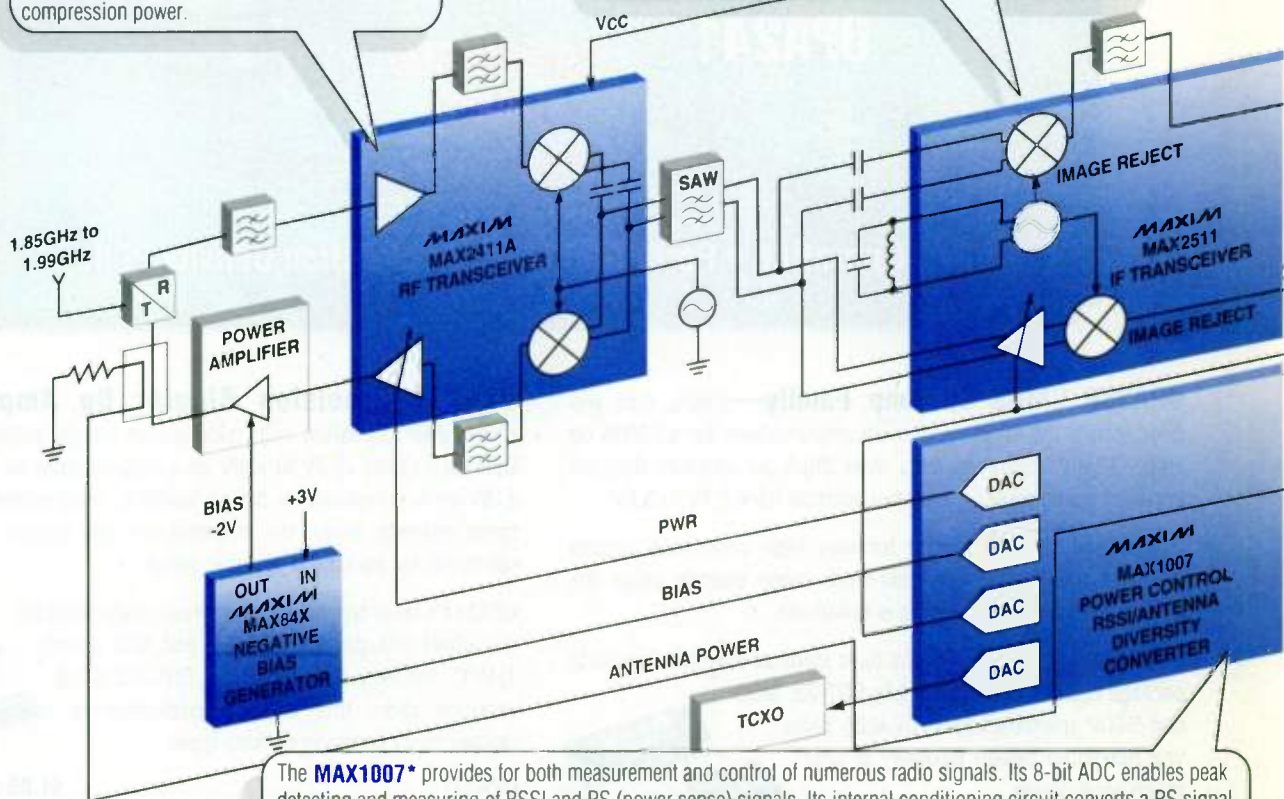
The **MAX2411A*** performs RF front-end amplification and frequency conversion in both receive and transmit modes. Its unique differential IF interface allows a single SAW filter to serve as a receive and transmit IF filter.

The MAX2411A has a 3.2dB combined down-converter noise figure and a -12.5dBm input IP3. The receive current is only 20mA with a 3.0V supply, and can be reduced below 1µA in shutdown. The transmit section includes an upconverter mixer, followed by a variable-gain power-amplifier predriver with +6dBm 1dB compression power.

The **MAX2511** performs IF frequency conversion, receive gain, transmit frequency conversion, and gain control functions. The receive mixer input and the transmitter output interface directly to one differential SAW IF filter to save space and cost.

The low-noise receive mixer has a unique image-rejection feature to keep spurious signals or image noise from mixing to the second IF. The RSSI output has excellent dynamic range (>90dB monotonic) and linearity (± 2 dB error over an 80dB range).

The transmit image-reject mixer generates a clean output spectrum to minimize filter requirements. It is followed by a variable-gain amplifier with +2dBm maximum output power.



The **MAX1007*** provides for both measurement and control of numerous radio signals. Its 8-bit ADC enables peak detecting and measuring of RSSI and PS (power sense) signals. Its internal conditioning circuit converts a PS signal into a DC signal, which is then converted by the ADC. For antenna diversity, the power detector circuit compares two RSSI signals.

The MAX1007 also includes four DACs. XDAC is designed to tune varactor diodes, while SDAC and KDAC adjust power-amplifier output power levels. GDAC provides bias control for GaAs amplifiers. All of the DACs are double buffered, allowing for simultaneous updating of the outputs.

* Available October 1997. Contact factory for engineering samples.

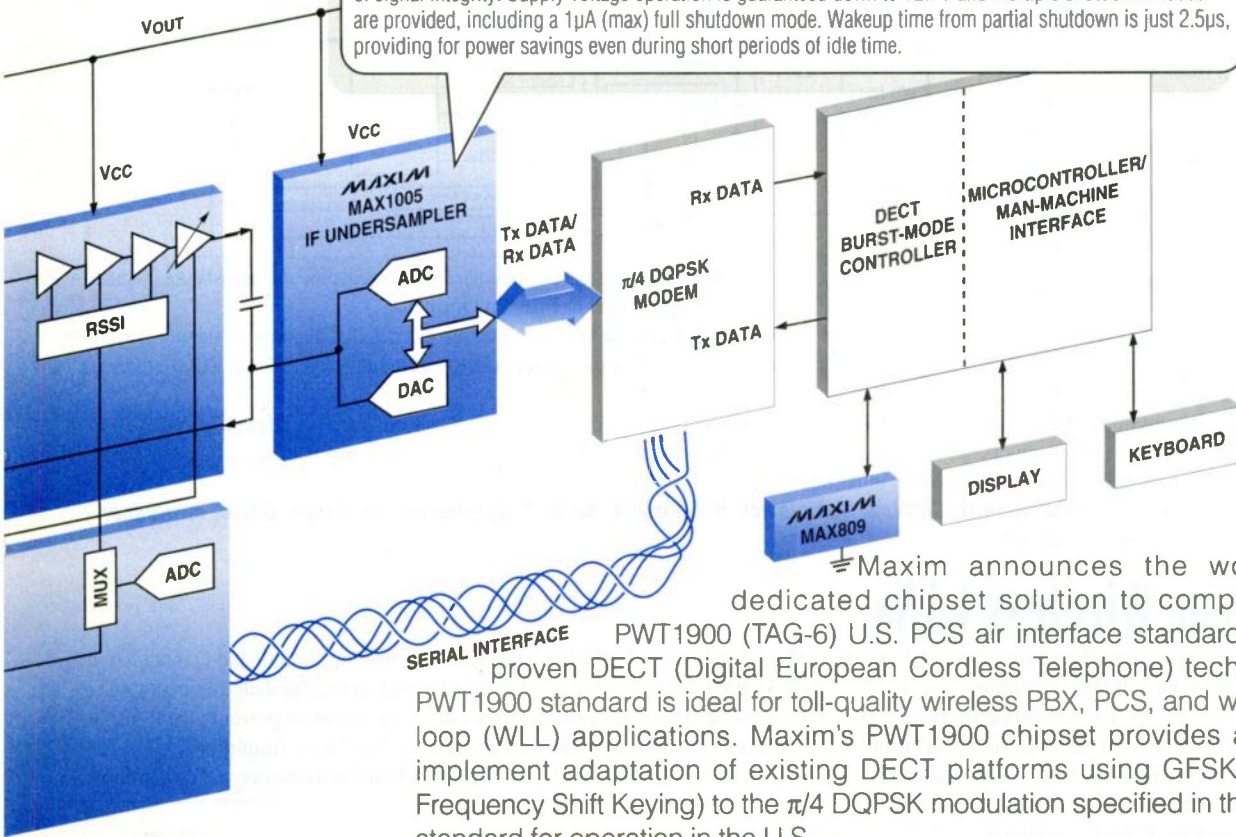
PWT1900 Rev 1

PWT1900 CHIPSET

Design Ready for the U.S. Market

The **MAX1005** includes an Rx ADC and Tx DAC plus voltage reference. In Rx mode, the ADC under-samples the data signal bandwidth centered on the IF. The ADC's 15MSPS conversion speed provides for 10-times oversampling of a 1.5MHz data signal. The wide input converter bandwidth provides for IFs in excess of 10.7MHz.

The MAX1005 requires very little power (13mA in Rx and 5.5mA in Tx mode) while providing a high level of signal integrity. Supply voltage operation is guaranteed down to +2.7V and multiple shutdown modes are provided, including a 1µA (max) full shutdown mode. Wakeup time from partial shutdown is just 2.5µs, providing for power savings even during short periods of idle time.



SERIAL INTERFACE

Maxim announces the world's first dedicated chipset solution to comply with the PWT1900 (TAG-6) U.S. PCS air interface standard. Based on proven DECT (Digital European Cordless Telephone) technology, the PWT1900 standard is ideal for toll-quality wireless PBX, PCS, and wireless local loop (WLL) applications. Maxim's PWT1900 chipset provides an easy-to-implement adaptation of existing DECT platforms using GFSK (Gaussian Frequency Shift Keying) to the $\pi/4$ DQPSK modulation specified in the PWT1900 standard for operation in the U.S.

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A Three-IC Chipset For Two-Way Paging

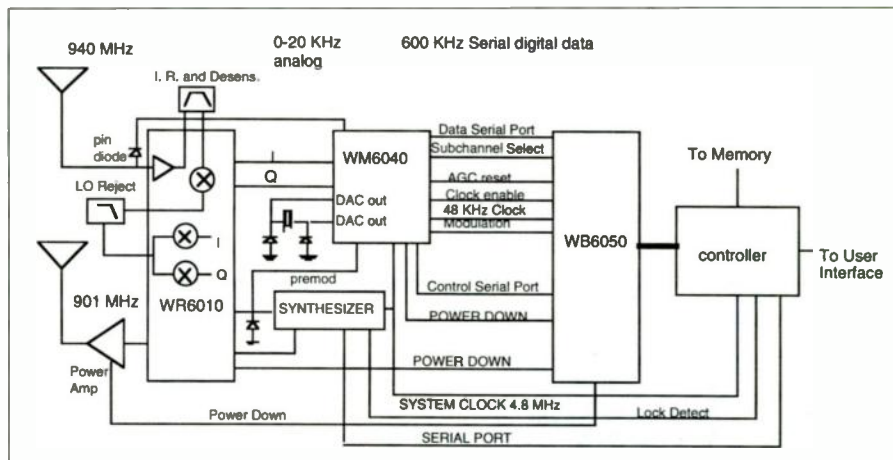
A highly integrated chipset for two-way paging systems based on a new double direct down-conversion scheme for the ReFLEX series of two-way paging protocols has been developed. A block diagram of the system is shown in the Figure. The three ICs are the WR6010 bipolar RF transceiver IC, the WM6040 mixed signal demodulation IC, and the WB6050 digital signal processing IC. The additional ICs which are required to complete the system are a synthesizer, power amplifier, and microcontroller. All system frequencies are derived from a single oscillator located on the WM6040. This oscillator is electronically tuned at manufacturing from a crystal with a room temperature tolerance of 15 ppm and temperature tolerance of 7.5 ppm.

An automatic frequency control algorithm which derives an accurate frequency from the received signal, tunes the oscillator to within 0.5 ppm during operation. The only external filters in the architecture are the front end blocking filter, and an LO reject filter which requires only a single LC resonator. All of the channel select filtering is accomplished in the WM6040. Adjustable gain control is accomplished within the WM6040 and via a pin diode attenuator on the front end. The attenuator boosts the dynamic range by 15-30 dB depending on the attenuator configuration (shunt diode only or series shunt). An electronic switch adjusts the channel select filter bandwidths and selects the single channel ReFLEX25 or multiple subchannel ReFLEX50 format.

Transmit modulation is accomplished through DACs located on the WM6040. The deviation values are extracted at the time of manufacturing. DAC outputs are provided to drive both the RF VCO and the reference oscillator. By using a combination of modulation on both VCOS, there is no high or low frequency cutoff for the modulation rate.

Since the power consumption is dominated by power down current and receive mode current, the emphasis on low power design is in these two modes. Very little time is spent in transmit operation and during this time, the power consumption is dominated by the power amplifier. Therefore, power optimization on the transmit path is of much less importance.

From "A Three IC Chipset for 2-Way Paging," K.R. Cioffi, S. Sanielevici, B. Ghosh, A. Shah, P. Stephenson, B. Ahrari, C. Kao, M. Rudner, Wireless Access Inc. 1997 Wireless Symposium.



Radios For Wireless LANs

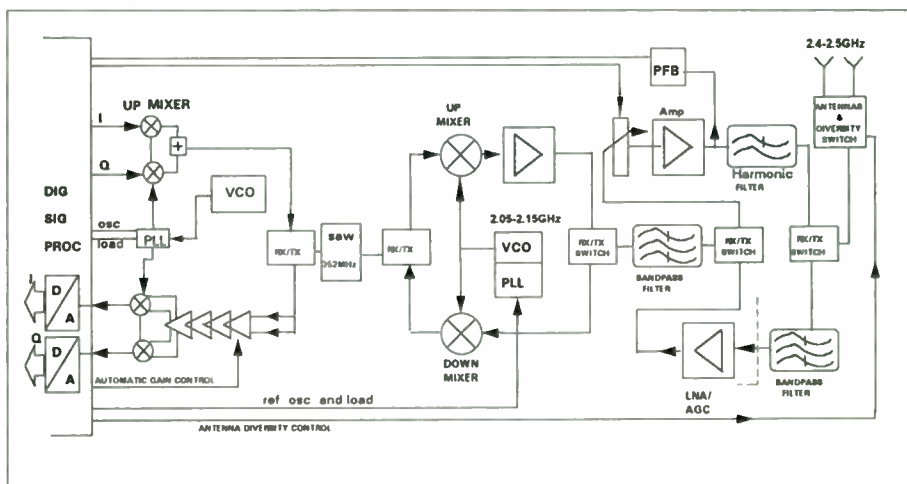
The radio block diagram (see the figure) shows a design for a DSSS radio in the 2.4-GHz band. The block diagram shows I and Q modulation and demodulation, into the digital signal processor. In the Transmit path the signal is via a mixer transformed an intermediate frequency (352 MHz), after filtering the signal is transformed to the 2.4-GHz band. A linear power amplifier generates the required output power to the transmit antenna. In the Receive path the signal is coming in via one of the antenna's (antenna diversity) and fed into the Low Noise Amplifier (LNA). The LNA is one of the most important pieces of the radio design since the sensitivity of this block can be directly translated into range. Further down the receive path the signal will be fed into the automatic gain control block to adjust the receive level on the inputs of the DSP.

The DSP chip is a very critical component in the Radio design; it carries the spreading and the modulation functionality. For LAN vendors to prepare for higher speeds, beyond IEEE 802.11, significant investments are required in DSP development. The only alternative for LAN vendors is to use off-the-shelf available chips which has its limitations with respect to migration to higher speeds.

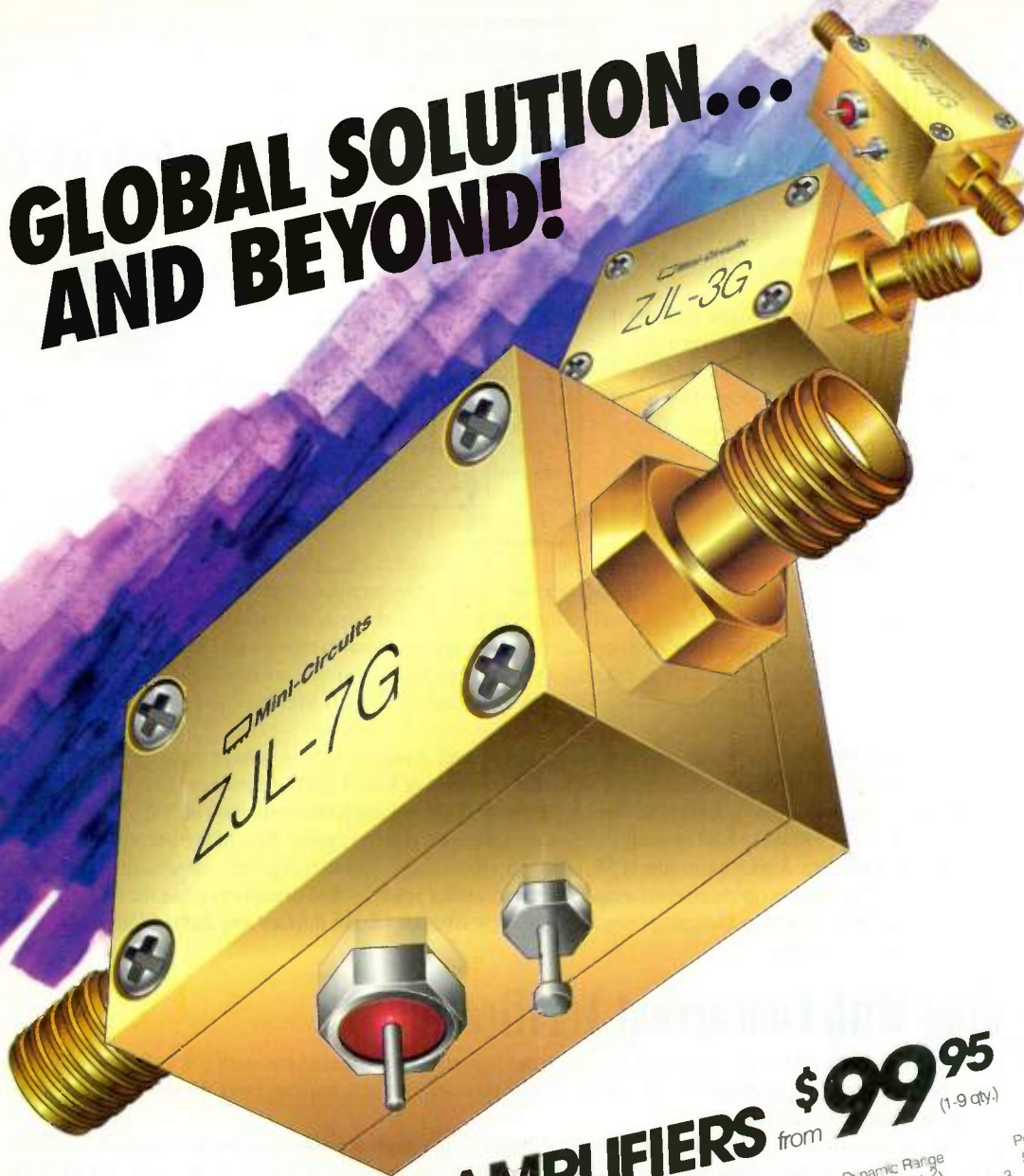
A look to the future suggests that DSSS will be the best technical choice for wireless LANs operating at two to five times current 2 Mbps/s speed as available today.

Our research indicates that DSSS has the potential to make a jump to 10-Mbps data rates. In such a case, three collocated access points could afford an aggregate throughput of 30 Mbps/s. Lucent Technologies has extensive experience in modulation algorithms and radio designs that will enable a move to 10 Mbps/s.

From "Wireless Lans," Vincent Vermeer, Lucent Technologies. 1997 Wireless Symposium.



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Model	Freq (MHz)	Gain (typ)		Max. Pout1 (dBm)	Dynamic Range (Typ @2GHz ²)		I(mA) ³	Price \$ea. (1-9)
		Midband (dB)	Flat (±dB)		RF(dB)	IP3(dBm)		
ZJL-5G	20-5000	9.0	±0.55	15.0	8.5	32.0	80	129.95
ZJL-7G	20-7000	10.0	±1.0	8.0	5.0	24.0	50	99.95
ZJL-4G	20-4000	12.4	±0.25	13.5	5.5	30.5	75	129.95
ZJL-6G	20-6000	13.0	±1.6	9.0	4.5	24.0	50	114.95
ZJL-4HG	20-4000	17.0	±1.5	15.0	4.5	30.5	75	129.95
ZJL-3G	20-3000	19.0	±2.2	8.0	3.3	22.0	45	114.95
ZKL-2R7	10-2700	24.0	±0.7	13.0	5.0	30.0	120	149.95
ZKL-2R5	10-2500	30.0	±1.5	15.0	5.0	31.0	120	149.95
ZKL-2	10-2000	33.5	±1.0	15.0	4.0	31.0	120	149.95
ZKL-1R5	10-1500	40.0	±1.2	15.0	3.0	31.0	115	149.95

NOTES:
1. Typical at 1dB compression.
2. ZKL dynamic range specified at 1GHz.
3. All units at 12V DC.



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An Intelligent Battery Application Using The Single-Wire Bus

This paper describes a low-cost fully functional intelligent battery-management system, which can be easily targeted for various battery chemistries. To minimize cost, the intelligent battery uses the Single-Wire bus to communicate with the host (e.g. laptop, cellular phone).

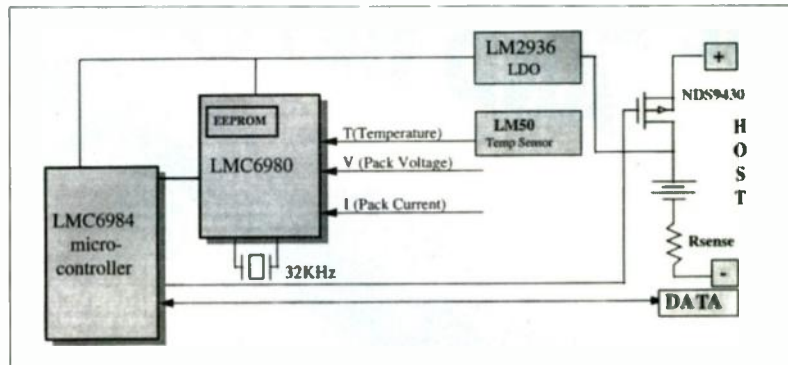
The intelligent battery must communicate with the host through a well-defined protocol. The two primary communication protocols currently in use are SMBus and Single-Wire bus. SMBus has been adopted for use by the Smart Battery System (SBS) data specification, and is endorsed by several battery and semiconductor manufacturers; Single-Wire bus has been adopted by Sony and has developed a large installed base. Single-Wire bus has a smaller command set and has a less complex physical layer than SMBus. This leads to a lower cost in terms of silicon implementation. Also Single-Wire bus requires fewer battery terminals than SMBus, leading to a further reduction in cost.

A simplified block diagram of an intelligent battery application with Single-Wire bus is shown in the figure. This particular application is a Nickel-based (NiCd/NiMH) battery solution. With some modification, this application can support a Li-ion battery pack and/or SMBus.

Three terminals are provided on the battery pack to interface with the host. These terminals are BAT+, BAT-, and DATA. A p-channel charge FET (NDS9430) is used for in-pack charge control, while a low drop out voltage regulator (LM2936) is provided to regulate the battery voltage to 5 V.

A mixed-signal device (LMC6980) constantly monitors the battery current, temperature, and voltage using the I, T, and V inputs. I reads the voltage across a sense resistor to determine the battery current with a resolution of 1ma. T reads the voltage (10 mV/degree C) from the temperature sensor (LM50) with a resolution of 0.1 degrees C. V reads the battery pack voltage with a resolution of $500 \mu V \times (\text{number of cells in series})$. The LMC6980 also provides EEPROM to hold chemistry dependent tables, to maintain critical data during battery shutdown conditions, and to store history and manufacturer data. A microcontroller (LMC6984) provides charge control, fuel gauge compensation, and host communications. It communicates with the LMC6980 to obtain current, temperature, and voltage readings, and to read or update the EEPROM data.

From "An Intelligent Multi-Chemistry Battery Application Using Low Cost Single-Wire Bus," Brian Burford and Zafar Ullah, National Semiconductor Corp. 1997 Portable By Design Conference.



Designing With Concurrent Verification

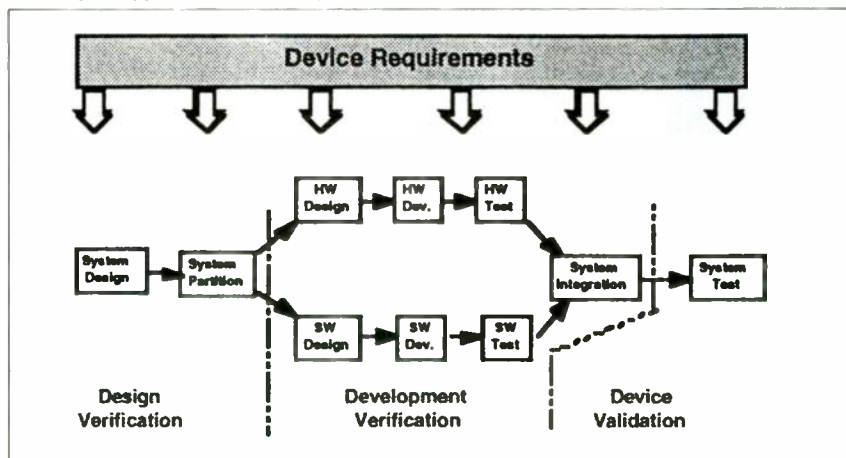
Concurrent engineering is the preferred solution for the disconnect between product design and testing. It calls for multi-disciplinary teams to jointly develop a product from design to delivery. However, making this concept work requires more than a Dilbertian dictate to engineers to henceforth engage in "concurrent engineering."

Concurrent verification is a process of validating an embedded device from a product perspective throughout the development cycle -from design to development, and then to integration and final delivery. The goal of concurrent verification is to begin testing the product at the earliest stages of its development.

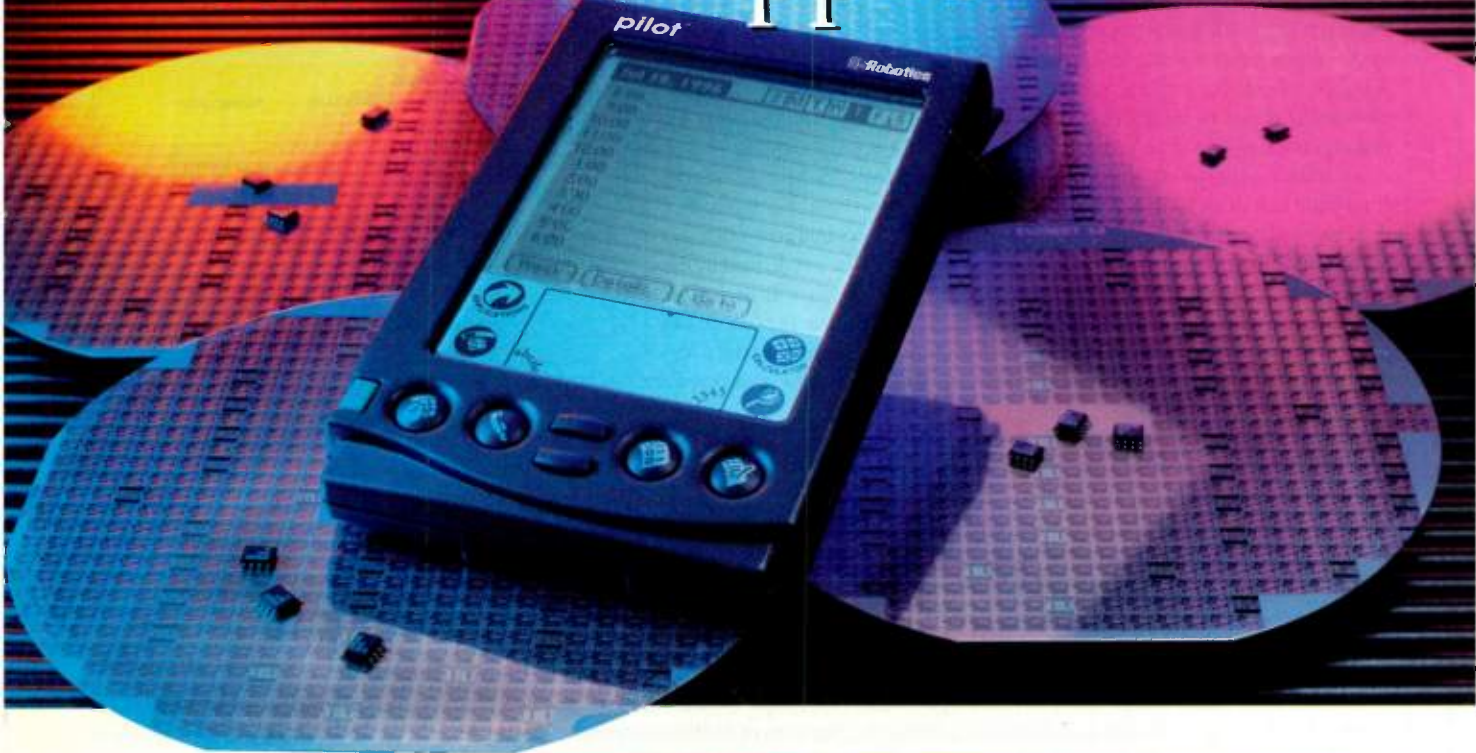
Concurrent verification consists of three stages: design verification, development verification and final validation. During the initial stages of the development cycle, the design must be verified to ensure that it meets the key requirements for the portable device. This means simulating the requirements model to ensure correctness. The environment around the portable device (the I/O etc.) must be accurately modeled during this process.

Development verification ensures that as the components of the portable device are being developed they are verified from an end-product perspective. The best way to accomplish this verification is to prototype the device. Components that have not yet been developed must be simulated to enable this prototyping to occur and the verification must be real-time and I/O-based. A key advantage of prototyping is to enable developers to make intelligent tradeoffs for the device. For example, developers may try out different versions of a processor or a memory device to make intelligent tradeoffs between performance, cost and functionality. The last stage of concurrent verification is product validation. After the portable device is "ready" it must be comprehensively validated. This validation must be comprehensive and real-time and must be done from a real-world perspective.

From "Designing Portable Devices with Concurrent Verification," by Moses Joseph, B-Tree Systems. 1997 Portable By Design Conference.



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SP4422A	2.2V to 6V	8mA ¹	•	Requires minimal board space	Remote Control Units, Portable Instruments, POS Terminals, LCD Displays
SP4423	2.2V to 6V	5mA ¹	•	Low Power	PDA's, Calculators, LCD Displays
SP4424	1V to 6V	6mA ²	•	Dual oscillator for coil and lamp control	Pagers, Digital Watches, LCD Displays
SP4425	1V to 6V	37mA ²	•	Max light output @ low voltages	Pagers, Cell Phones, LCD Displays
SP4430	1V to 3V	75mA ³	•	DC/DC converter	Cell Phones, PDA's, Pagers

1. V_{dd} = 3.0V 2. V_{dd} = 1.5V 3. V_{dd} = 1.0V



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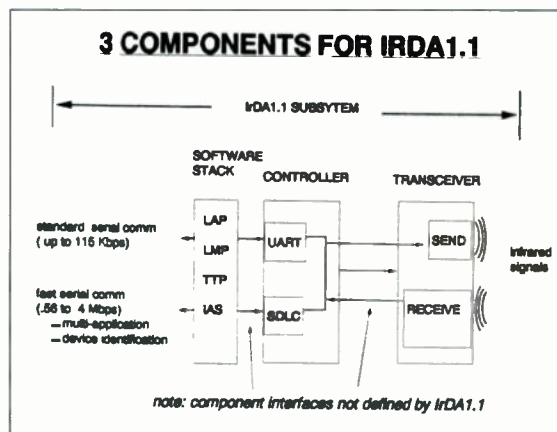
Inside The IrDA 1.1 Subsystem

In October 1995, through a combined proposal from HP and IBM, the IrDA (Infrared Data Association) approved the IrDA1.1 extension of the physical layer standard. This introduced two new speed capabilities of 1 and 4 Mbit/s. Another important extension approved at that October meeting was Ir/Comm, a new layer in the communication stack for emulating serial or parallel port cable protocols. As Microsoft and other operating system providers implement this new layer, the millions of copies of installed applications that use serial or parallel ports for making connections will be immediately infrared-enabled.

An IrDA1.1 subsystem supports infrared data transmission speeds ranging from 9600 kbits/s to 4 Mbits/s. An IrDA1.1 infrared subsystem is composed of three elements: an IrDA1.1 software protocol stack, a fast infrared controller, and infrared transceiver. The interfaces between these elements are not defined by the IrDA standards. In practice the technology providers work closely with each other to assure interoperability between components. However, due to some unexpected incompatibilities, there have been some combinations that produce less than IrDA-compliant performance. As providers revise their parts these incompatibilities are being removed resulting in a very attractive mix-and-match situation for product developers.

IrDA1.1 stacks are available from Microsoft, IBM, PUMA Technologies, Counterpoint, Okaya and Phoenix to name a few. Each of these stacks are enabled to support a variety of infrared controllers. These IrDA1.1 controllers are available as discrete devices from IBM for example, or embedded in super I/O's or Ultra I/O's from companies such as Standard Microsystems, National Semiconductor, or VLSI to name a few. Most controller providers support the IrDA1.1 transceiver solutions from the likes of IBM, HP, Temic, Sharp, Siemens, Novalog and also IrDA1.0 solutions from providers such as Rohm, Stanley and Unitrode.

From "IrDA Transceivers and Drivers for the Future Cordless Office," **Brian R. Ingham**, IBM Canada Ltd. 1997 Portable By Design Conference.



Multiple SMBuses and Hosts

Systems in the future will probably have multiple SMBuses, multiple SMBus hosts and private SMBus segments. The figure shows a block diagram of such a system. This system shows three different collections of SMBus components. The upper is of particular interest as an example of an embedded controller whose interface is reported to the operating system via ACPI (Advanced Configuration and Power Interface).

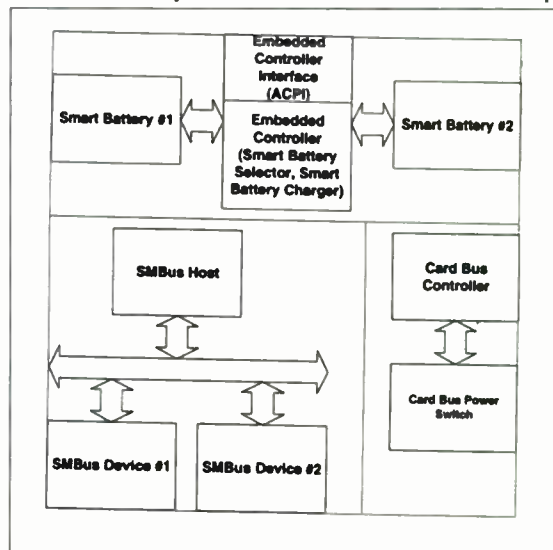
The key features are that the ACPI reports the location of the embedded controller register set; and the ACPI defines a set of commands to communicate with devices on the SMBus. This set of commands allows a standard device driver for the embedded controller to be included with the operating system. Since ACPI also supports the Smart Battery systems specifications, a standard battery device driver can be included with the operating system as well.

This example embedded controller also replaces the functionality of two Smart Battery system components, the charger and the selector. At the interface, it looks like all the components are on the SMBus, but the actual implementation is quite different, taking advantage of an embedded controller to replace functional blocks reducing component count and real estate. The example embedded controller emulates two SMBus segments to individually communicate with two Smart Batteries. It either operates in a master/slave mode or master only where it must poll the batteries for alarm conditions. When an alarm is detected or there is a status change in the Smart Battery system, the embedded controller issues an SCI (ACPI style event notification) which causes the operating system to identify issuer and service the interrupt.

In this example, the embedded controller may serve another purpose as well. There are some devices that should not be fully exposed. For example, a rogue piece of code could continually force the Smart Charger on the SMBus to charge the battery, potentially causing a battery failure or could command the SMBus power plane controller to turn off the main power plane. These SMBus devices can be "hidden" behind the embedded controller interface, available to the system, but totally inaccessible at the SMBus interface. The embedded controller can reject or ignore requests in order to maintain system safety and integrity. It should be noted that the embedded controller may perform many other system activities as well.

The lower left of the figure represents a chipset with a SMBus UART. In this case the SMBus host is a simple UART and is limited to communicating with devices on the SMBus. The lower right of the figure represents a pair of devices that use an SMBus segment to pass proprietary control, command and data between the devices. SMBus is attractive in this application because the implementation can be as simple as a pair of shift registers and a clock. Most if not all implementations of this type are expected to have a master only in one device and a slave only in the other. The system has no direct access to the SMBus.

From "SMBus Architecture and Implementation Review," **Robert A. Dunstan**, Intel Corp. 1997 Portable By Design Conference.



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ADS7817	12	± 1	12	200	2.3	71	-83	11369	109
ADS7822	12	± 0.75	12	75	0.54	71	-82	11358	110
ADS1286	12	± 1	12	20	1	72	-85	11335	111

*No Missing Codes. For Technical Information: <http://www.burr-brown.com/Ads/ADS7822-Ad.html>

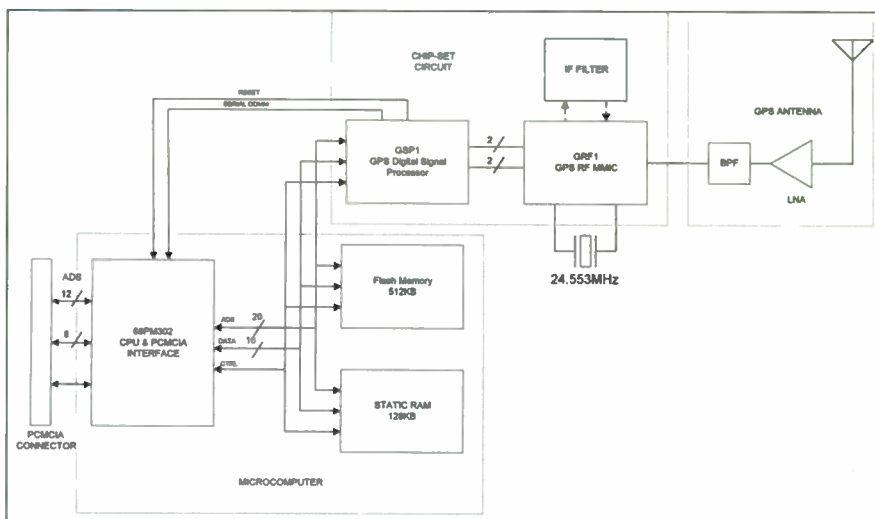
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A PCMCIA GPS Receiver

In this PCMCIA GPS receiver there are two major building blocks—the GPS chip-set and the microcomputer. The SiRFstar chip-set includes the GPS RF chip (GRF1) and GPS Signal Processor chip (GSP1). One implementation for a PCMCIA microcomputer is based on the 68PM302 microprocessor, which has a built-in PCMCIA interface, a flash memory for program space and specific data storage, and a static RAM for stack and variables (see the figure). With the SiRFstar chip-set a simple impedance matching network may be required to match between the antenna cable and the RF chip. Anyway it is not desirable to have the LNA and BPF on the card since these components are too tall to fit on the card, and their proximity to the antenna is beneficial for noise reduction.



An external IF filter is required for the proper operation of the RF chip. The GPS signal processor (GSP1) filters the signal in the digital domain, so only a two-pole LC filter is required for optimal operation. The bandwidth requirements are between 2 and 8 MHz, and only 10 inexpensive passive components are needed. An external crystal and two capacitors are required for the operation of the reference oscillator. This oscillator is designed to work with low-cost crystals with a price below one dollar. In addition to that the height of TCXOs does not fit into PCMCIA package. The 68PM302 CPU gives sufficient throughput to handle the GPS functions. Since this CPU also has PCMCIA interface built-in, considerable cost and space is saved. The flash memory is used as program space, and convenient for downloading updates through the PCMCIA interface. The on-chip decode logic of the GSP1 permits a 'glueless' interface to standard 8- or 16-bit wide memories as well as to the CPU.

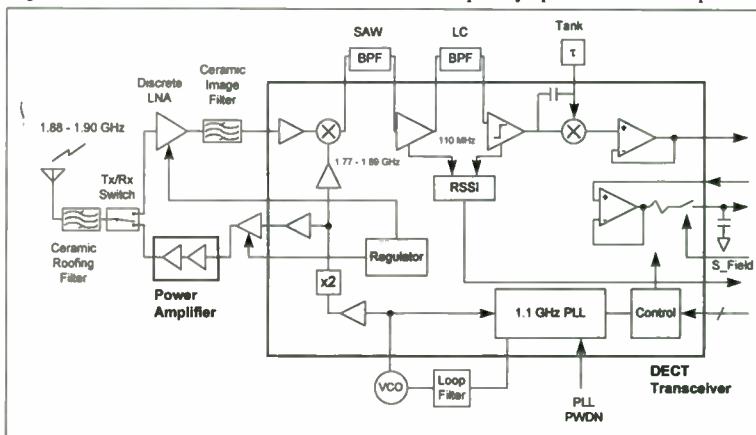
From "PCMCIA GPS Implementation," **Oded Yossifor**, SiRF Technology, Inc. 1997 Portable By Design Conference.

A Highly Integrated DECT Radio Transceiver

A complete radio transceiver for the Digital Enhanced Cordless Telecommunications (DECT) standard demonstrates a high level of integration along with reduced component count and board size. The transceiver chip consolidates receiver, transmitter and phase locked loop (PLL) subsystems. The chip also includes two regulated voltage outputs and three programmable CMOS outputs. Power control and register information is input via a three wire Microwire programming interface.

The PLL NCO runs at one half of the DECT frequency (880-950 MHz) and uses an on-board frequency doubler to synthesize the correct DECT frequencies. The use of a frequency doubler alleviates the effects of EMI radiation on the VCO from the power amp. The frequency doubler also decreases the effects of load pulling on the VCO by increasing the isolation between the power amplifier and the VCO.

The receiver subsystem consists of a down-converting mixer, an IF amplifier, limiting amplifier and quadrature demodulator. The modulated RF signal is first passed through a roofing filter to attenuate signals outside of 1880-1900 MHz, the DECT frequency spectrum. An inexpensive discrete LNA is then used to provide the first gain stage of about 14 dB with a noise figure of about 2 dB. Another ceramic filter is used to attenuate the image of the signal. The RF signal then comes on chip and is down converted to 110.562 MHz and passed through an off chip SAW filter to suppress the adjacent channel signals. Cascaded RF gain before the SAW filter is approximately 28 dB with a cascaded NF less than 6 dB. The signal comes back on chip through the IF amplifier (~25 dB gain) and then off chip through a discrete filter to remove wideband noise (~8-10 dB insertion loss). The signal is passed through a 60 dB gain limiting amplifier and then converted to baseband using a quadrature demodulator. The total gain in the IF section is approximately 80 dB. An off chip LC tank circuit is required to generate the 90-degree phase-shifted signal. The output of the quadrature demodulator goes off chip for low pass filtering, then back on chip for dc recovery using a sample and hold circuit.



The output of the quadrature demodulator goes off chip for low pass filtering, then back on chip for dc recovery using a sample and hold circuit.

The transmitter subsystem consists of a 1.1-GHz phase-locked loop, a frequency doubler and a transmit output buffer. Transmission is accomplished by direct, open-loop modulation of the 1-GHz VCO. In the time slot prior to transmission, the PLL is phase locked to one half the DECT transmit frequency and then powered down to open the loop during the desired transmit slot.

From "A Highly Integrated DECT Radio Transceiver," **Kendal McNaught-Davis Hess, William O. Keese, and Eric Lindgren**, National Semiconductor. 1997 Wireless Symposium.

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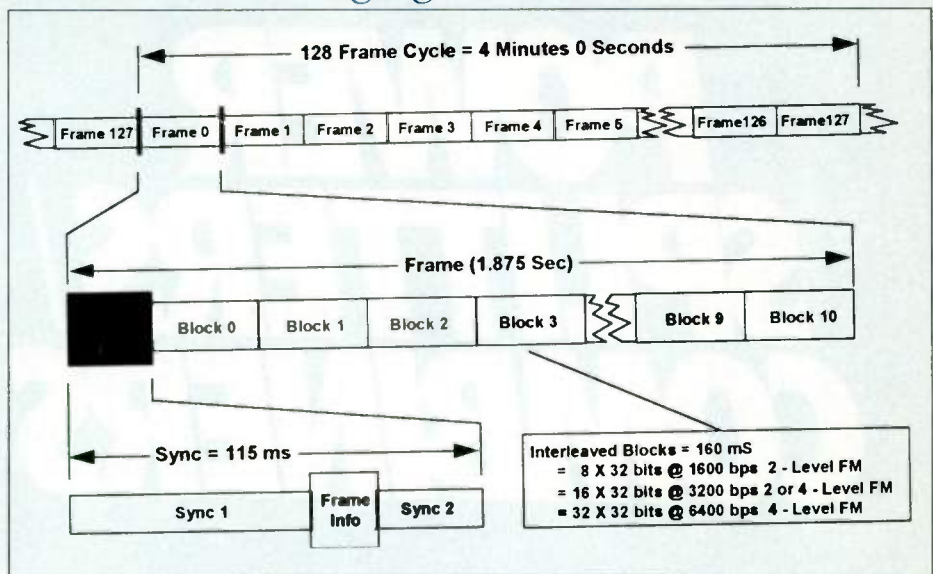
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FLEX: A Synchronous Wireless Messaging Protocol

This paper describes the implementation of incremental hardware and software required to give a handheld PC device wireless connectivity. The FLEX protocol is a synchronous radio messaging protocol where all subscriber devices must maintain synchronization to be able to receive a message. There are 128 frames in each 4-minute interval, synchronized to the hour. A frame is 1.875 seconds in duration, and each begins with a synchronization word pattern, followed by a "frame info word", followed again by another synch packet (see the figure). Each address is assigned a home frame, and any message for that address must be sent during that frame or more often depending upon the device and the system. Within each frame, address, vector, and data packets are sent in blocks 0



through 10, but are not bound to remain within any particular block. The block boundaries refer to the groups of bits that are interleaved. All addresses are transmitted at the beginning of each frame, followed by a corresponding group of vectors, followed by the corresponding data. Devices that do not have an address match will be able to power down early in the frame allowing for maximum battery life. When data rates are either 3200 or 6400 bps, two or four simultaneous streams of data, or phases, will be transmitted in the four level FM signal, allowing for maximum throughput while easily mixing numeric, alphanumeric, and e-mail messages. Each phase of information, as in the single frame case, will be packets of addresses, vectors, and data whose sizes are independent of one another and independent of the block boundaries.

From "Implementing A Wireless Data-Enabled Handheld PC Optimized For Size, Battery Life, And Functionality," Gary Oliverio, Motorola. 1997 Portable By Design Conference.

Reducing Power Levels In Microcontrollers

To develop low-power microcontrollers designers are applying advanced processes with finer geometries. As finer processes are used, the internal capacitance becomes smaller, and the power required to charge and discharge the internal interconnect wires and gates becomes lower. In addition to the reductions in current due to the smaller capacitance, as the voltages fall there is a reduction in the power that must be dissipated by the device that is due to squared effect of Voltage in the $P = fCV^2$ equation. The figure describes a low-voltage, low-power process roadmap for a 16-bit microcontroller.

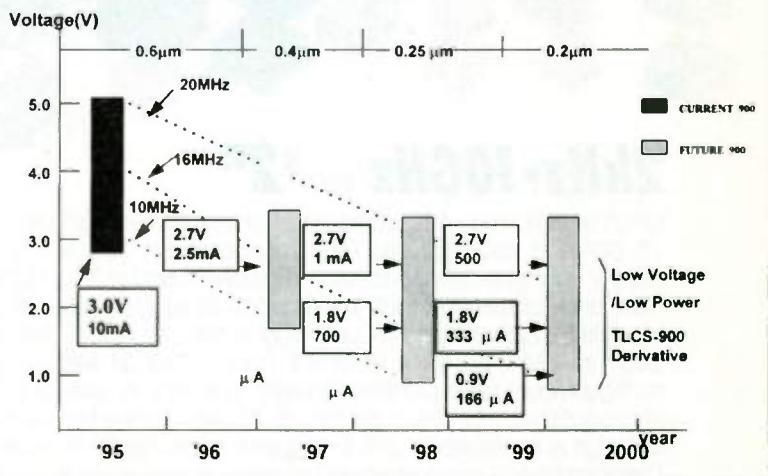
The dark block represents the current TLCS-900/H family based on a 0.6- μ m process. The low-voltage devices are currently produced with the 0.6- μ m process by limiting its speed of operation. Current microcontrollers can operate down to 2.7 V when the operating frequency is limited to 10 MHz with an operating current of 10 mA. Faster operation, 20 MHz, is possible with a 5-V power supply.

The next generation 0.4- μ m processes will allow 1.8-V operation at 10 MHz with a 1.8-mA current consumption. A 2.7-V operating voltage will be possible at 16 MHz with a 2.5-mA current consumption target. This allows greater operating speed at 2.7 V with a 75 percent reduction in current and power over the current product.

Future generations are targeting lower operating voltages and lower current consumption. At 0.25 μ m, a 0.9-V operating voltage will be possible at 10 MHz. This will allow portable equipment to be designed for single battery operation. The operating speed at 2.7 V will be increased from 16 to 20 MHz while reducing the current and power required by another 60 percent. The transition from 0.25 μ m to 0.2 μ m will be primarily targeted at increasing the speed of operation and reducing the current consumption rather than lowering the operating voltage of the device.

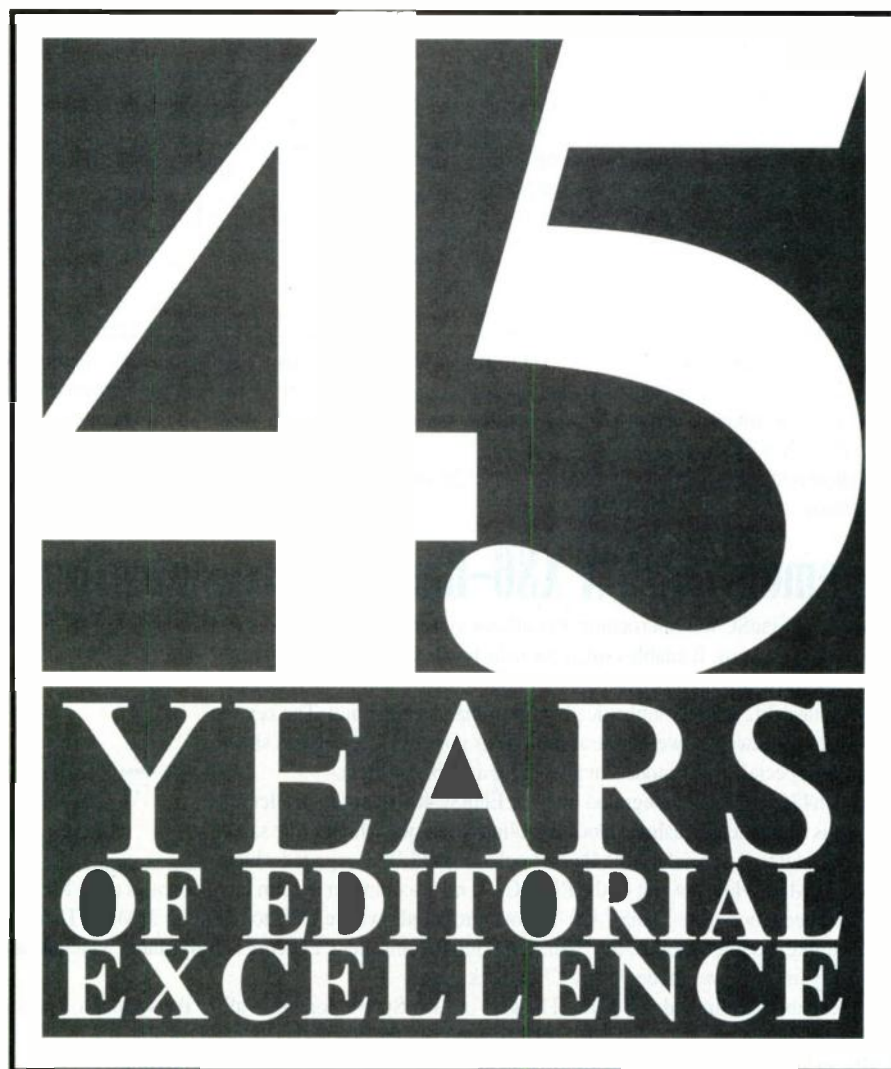
From "Lowering Power Levels To Meet Evolving Design Requirements In Low Power Systems," Donald J. Schneider, Toshiba America Electronic Components, Inc., Takeji Tokumaru, Toshiba Corp. 1997 Portable By Design Conference.

Low Voltage/Low Power Road Map



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A Minimal Overhead Universal Charging System

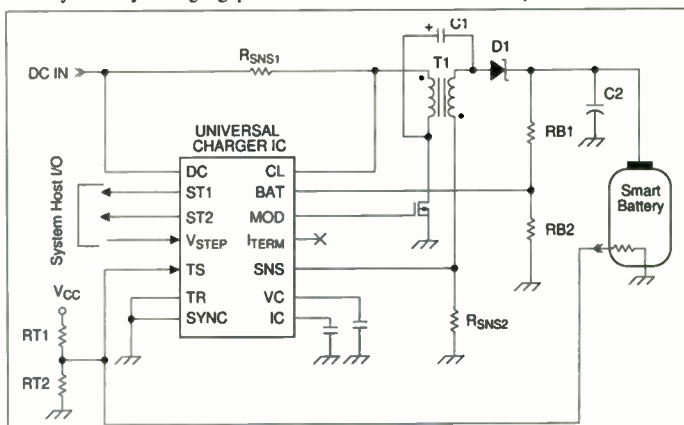
This paper discusses the SBS Charger and Selector specifications and their practical implications in a low-cost portable equipment subsystem and concludes with suggestions for the next step toward a universal battery charger for other mobile equipment.

The Intel/Duracell SBS technology is a solution to the multi-chemistry battery charging problem. It does not necessarily lend itself to the cheapest implementation. The entire solution cost must be considered prior to adopting any particular methodology.

Other technologies in use today meet the requirements for an universal intelligent battery charging solution. A case in point is the Benchmark bq2050H Power Gauge IC that communicates a pre-defined data-set over a 5k-baud serial line to the System Host. Unlike the SMBus, the HDQ serial interface only supports a point-to-point messaging protocol, simplifying the interface on both sides: the battery and the host. This type of system does not require a BUS selector as defined by the SBS specification. In this type of system, the battery charging requirements are determined by the host and communicated to the universal charger by way of two to three multi-level I/O pins.

The figure shows a block diagram of a universal charger design. In this implementation, the charger detects when the battery is fully charged. The charger uses the Smart Battery thermistor pin in two ways. First, it uses the thermistor to determine the battery chemistry type. Then it uses the same divider network to determine the $\Delta T/\Delta t$ termination threshold for nickel-based chemistries. The host has an option to override the charger based on information derived from the battery pack. This approach allows multi-chemistry charging without requiring the battery to communicate directly with the charger.

From "The Smart Battery Charger And Selector: A Cost-Effective Approach," by **Jehangir Parvereshi** and **Bill Bentley**, Benchmark Microelectronics, Inc. 1997 Portable By Design Conference.



Power Management With A X86-Based Microcontroller

The recently announced AMD ÉlanSC400 microcontroller allows system designers the flexibility to create a variety of mobile systems. It enables small form-factors because it is a highly integrated single-chip device, and provides high performance in both 33-MHz and 66-MHz clock speeds. It also provides long battery life with its sophisticated power management unit. The key to extending battery life is to get to the lowest power mode as quickly as possible. The Figures show six power modes, as well as two special power modes, available for a mobile system.

Hyper Speed Mode: The Am486 CPU core integrated into the ÉlanSC400 microcontroller allows 66-MHz operation. This is implemented using a clock doubling technique which is the same technique used in PC desktop systems. A special analog Phase Lock Loop (PLL) is engaged which allows the CPU to operate at 66 MHz while the rest of the ÉlanSC400 microcontroller system logic operates at 33 MHz.

High Speed mode: In High Speed mode, the ÉlanSC400 microcontroller allows the CPU to run up to 33MHz. There is no need for the special CPU PLL for Hyper speed. Unlike the Intel 486GX, the ÉlanSC400 microcontroller CPU core is fully static, which means that the CPU can toggle between high-speed and any lower power mode on any CPU clock edge.

Low Speed mode: Low Speed mode is limited to 8 MHz. The goal of Low Speed mode is to allow the system to operate when the primary battery is low but not yet dead. The end user will see degraded performance, but the benefit is extended useable life.

Standby: This is basically an idle mode; the goal of system designers is to get to Standby as fast as possible.

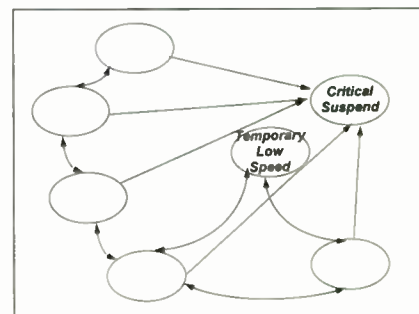
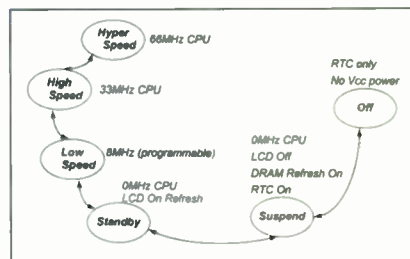
Suspend: The mobile system appears to be "off" to the end user. In Suspend mode, the ÉlanSC400 microcontroller gracefully powers off the LCD panel and other external devices. The DRAM is placed in a self refresh state. Then, the CPU and system logic are put in a no-clock state and the integrated clock synthesizing Phase Lock Loops are turned off. Only the RTC and the PMU are active. The PMU is clocked from the same 32-kHz crystal oscillator source as the integrated RTC. In Suspend, the ÉlanSC400 microcontroller only requires 50 μ A of current. Many months of shelf life are enabled by this low power control.

Off: In the Off mode, only the RTC portion of the ÉlanSC400 microcontroller has power. All other Vcc rails are powered down.

Critical Suspend: When BL2#, is asserted the ÉlanSC400 microcontroller immediately goes to Critical Suspend within 55 μ s. The goal of Critical Suspend is to get to the lowest power state extremely quickly in order to preserve the contents of the DRAM based data-store.

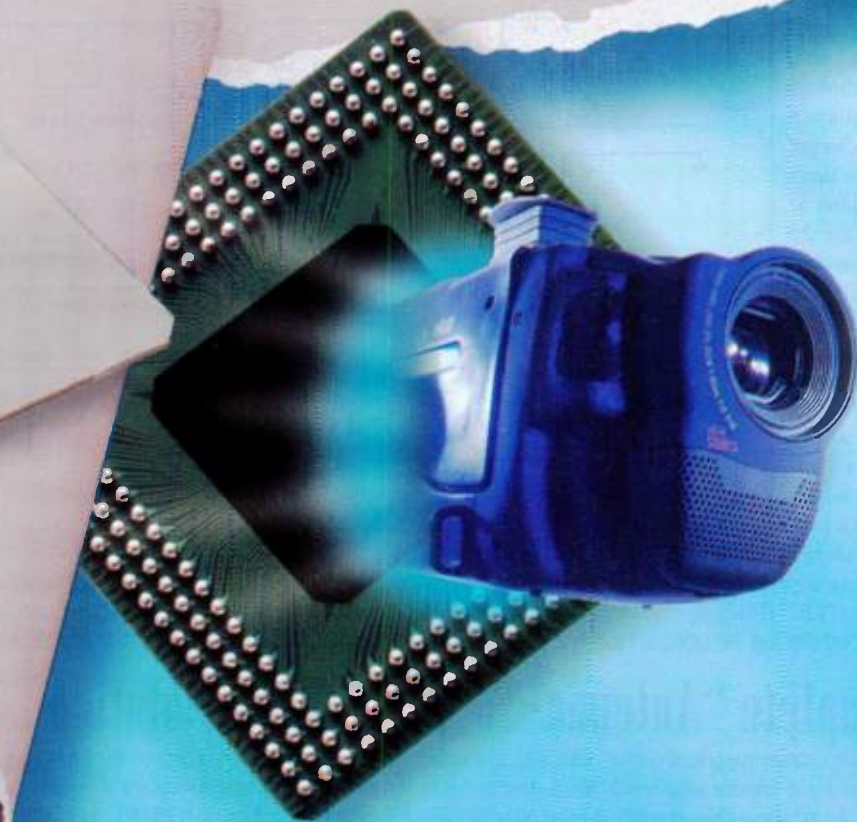
Temporary Low Speed: Temporary Low Speed mode is a special mode allowing the BIOS/HAL to process activities without leaving the current mode. The ÉlanSC400 microcontroller will move the system to Temporary Low Speed mode and interrupt the BIOS to inform it of the low battery warning.

From "Mobile Applications And Power Management Implementations With An X86 Based Microcontroller," **David Tuhy**, Advanced Micro Devices. 1997 Portable By Design Conference.



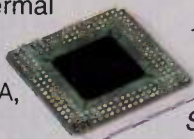
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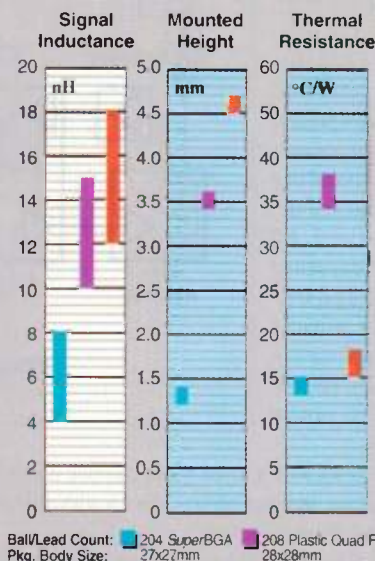


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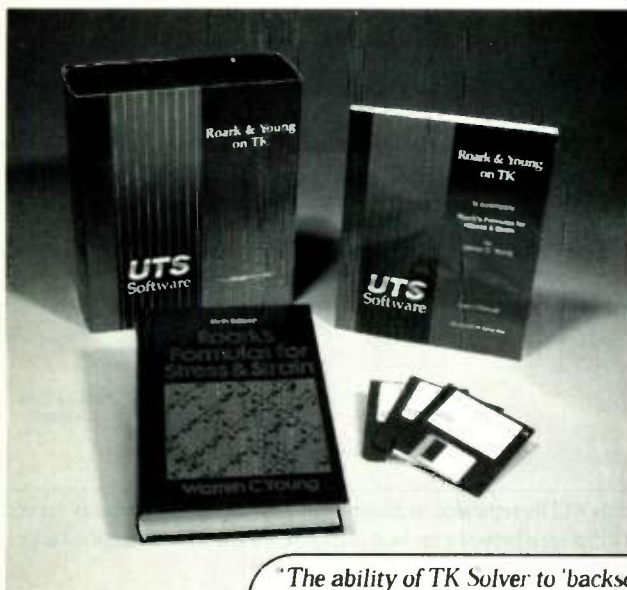
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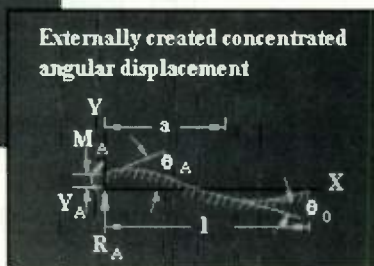
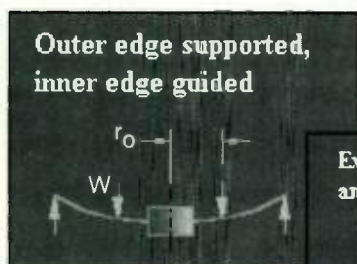
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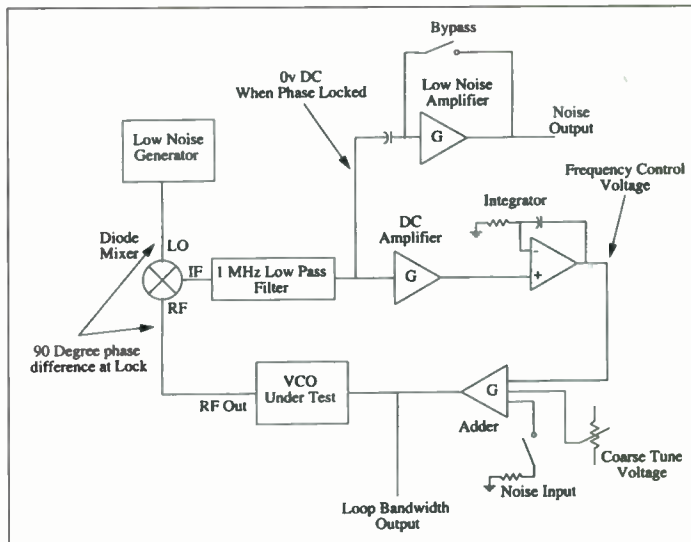
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Low-Cost Phase Noise Measurement

Phase noise levels in receiver local oscillators limit the signal-to-noise ratio and adjacent channel rejection. For an FM system 50 dB of signal-to-noise is desirable. Noise power is integrated from noise density over the range of offset frequencies that pass through the IF. A 3-kHz IF bandwidth requires about -85 dBc/Hz phase noise at a 300-z offset. With test margin about -95 dBc/Hz is needed in the test system. Adjacent channel rejection is noise density integrated over the IF bandwidth, at a one-channel offset from the carrier. 90 dB of rejection requires an oscillator with -125 dBc/Hz phase noise and a test system capable of -135 dBc/Hz. Channel spacing can be 10 kHz. Currently available spectrum analyzers do not have sufficient measurement range. A few phase noise test systems are available in the \$30,000-and-up price range, and implement the phase detector method described in this low-cost implementation.

The phase detector method allows a spectrum analyzer to make a phase noise measurement without viewing its internal phase noise. The block diagram is shown in the figure. Two signal sources are used with one being phase locked to the other. The phase-locked loop shown is initially in an open loop state. One signal is frequency-offset from the other. The difference frequency level is measured. Then the loop is connected. During phase lock the mixer IF port is at 0 V dc with superimposed noise. RF and LO port signals will be separated in phase by 90 degrees. Noise output is viewed after it passes through the LNA. Phase noise at a particular offset is the level difference between the beat and noise output with correction factors.

From "Low Cost Phase Noise Measurement," **Morris Smith**, Motorola. 1997 Wireless Symposium



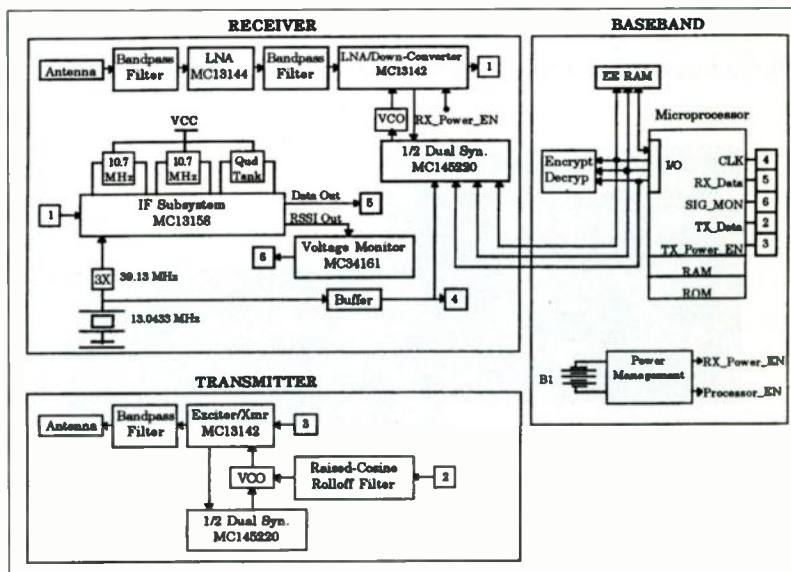
A Transponder For Wireless Vehicle ID

This vehicle-based transponder is a small, battery-operated unit that is composed of a 915-MHz transceiver, a microprocessor with nonvolatile RAM, and a power-management unit. A dual-conversion, wideband FM (WBFM) receiver is implemented having frequency agility when controlled by a dual PLL synthesizer. A custom-built printed circuit board (PCB) that uses "off-the-shelf" surface-mount components, it comprises a PCB trace antenna, two RF filters, a low-noise amplifier (LNA), a two-stage mixer, and a local oscillator (LO) as shown in the figure. The received signal is captured by the antenna and fed through a RF ceramic bandpass preselector filter centered at 915 MHz. The signal is amplified by a low-noise amplifier (MC13144 LNA) and passed through a second RF ceramic filter. The signal is fed into a single IC (MC13142) that consists of a second LNA, a downconverter, and a voltage-controlled oscillator (VCO). A 1.1-GHz dual PLL synthesizer (MC145220) controls the receiver first LO.

The output of the front-end section is sent to a 49.83-MHz IF filter (not shown in the figure) and an IF subsystem (MC13158) that consists of a second downconverter, IF and limiting amplifiers, wideband FM quadrature detector, and data slicer. Greater than 50 dB second image rejection is provided by the receiver back-end section. Frequency tripling the 13.043-MHz reference crystal oscillator provides the IF subsystem LO (receiver second LO); this eliminates the need for a second crystal source. The dual synthesizer is used to control both the first converter VCO and the transmitter oscillator/exciter. A data slicer (not shown) converts the analog output into a TTL waveform ready to be fed into the encoder/decoder software module. This design is used to achieve -90 dBm at 110 kbps with a very low error rate. Higher data rates of 300 kbps are achievable but cost is significantly higher.

The transmitter converts the vehicle identification number into an FM signal. To limit transmission bandwidth, a baseband data stream signal is routed from the microprocessor through a raised cosine-rolloff premodulation filter. The output of the filter is then fed into a VCO/exciter (MC13142) where it is modulated onto the 915-MHz carrier. The wideband FM signal is filtered by a 915-MHz RF ceramic bandpass filter and radiated by the PCB trace antenna. The baseband unit consists of a RISC processor with external nonvolatile RAM and rolling code encryptor/decryptor (XL107).

From "Wireless Vehicle Identification With Early Detection: An Alternative to Traditional Toll Collection Methods," **Carlos A. Medina**, I/O Test, Inc., and **Harry Swanson**, Motorola, Inc. 1997 Wireless Symposium.



A Dual Li-Ion Power Management System

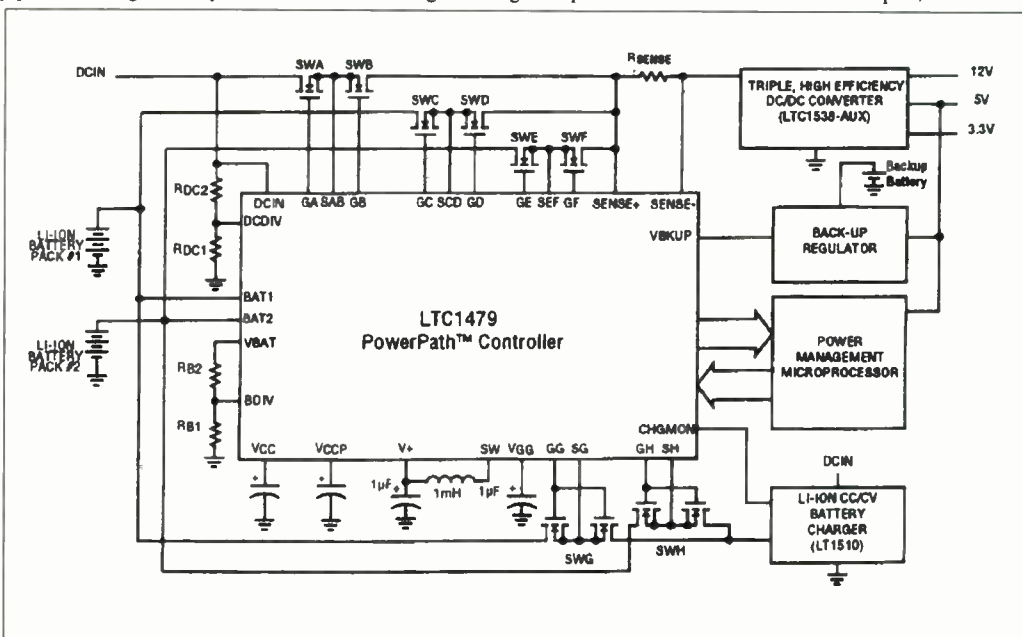
A typical dual Li-Ion battery power management system is shown in the figure. If "good" power is available from the ac adapter, both MOSFETs in switch pair SWA/B are on—providing a low-loss path for current flow to the input of the DC/DC converter. Switch pairs SWC/D and SWE/F are turned off.

The PowerPath Controller works equally well with Li-Ion and NiMH battery packs and their associated chargers. In this instance, an LT1510 constant voltage, constant current (CC/CV) battery charger circuit is used to alternately charge two Li-Ion battery packs.

The power management microprocessor decides which battery is in need of recharging by querying the smart battery pack directly. After the determination is made, switch pair SWG or SWH is turned on by the PowerPath Controller to pass charger current to the battery. The charging battery voltage is returned to the voltage feedback input of the CV/CC battery charger via a mux in the PowerPath Controller.

After the first battery is charged, it is disconnected from the charger circuit. The second battery is then connected through the other switch pair and the second battery charged. When the ac adapter is removed, the PowerPath Controller instantly informs the power management microprocessor that the DC input is no longer "good" and the desired battery pack is connected to the input of the dc/dc converter. (If battery power is lost, backup power is provided by a standby switching regulator powered from a small rechargeable "bridge" battery.)

From "Techniques for Simplifying Dual-Battery Portable Power-Management System Design," Timothy J. Skovmand, Linear Technology Corp. 1997 Portable By Design Conference.



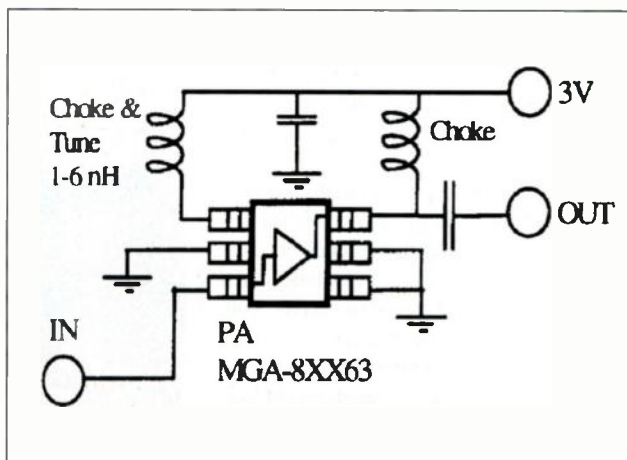
A 3-V Power Amplifier for Wireless Applications

The new PA is an extension of the MGA81563 and MGA-82563 medium power amplifiers. This amplifier will provide greater than 20 dB gain and 20 dBm output power over the 0.8 to 6.0-GHz range. Input and output are internally matched to 50 ohms for small-signal and linear application. Maximum power (saturated) is achieved with a simple output power match. The amplifier operates on 3.0 V applied to two package pins. For saturated (transmit) applications the amplifier can be operated at 3dB compression and typically produces 200 mW (23 dBm) of power. Power added efficiency is in excess of 45%.

The 20/20 PA is classic two-stage design. It consists of two FET gain stages, full feedback on the first stage (for match), and open drain on the second stage for maximum power. The first gain stage consists of a FET biased at a large percentage of I_{DSS} with the gate dc grounded. A capacitor and resistor network provide feedback on the first stage to improve match, provide stability, and flatten gain. The second stage is a FET also biased at a large percentage of I_{DSS} . A shunt resistor on the second stage provides the dc ground and lossy interstage match. A separate dc supply is used for each stage to improve stability and allow the interstage to be "tuned" for max gain and power. Separate source grounding pads and ground bonds are used to improve high frequency stability. The die size is approximately 0.44 mm (17.3 mils) by 0.36 mm (14.2 mils).

In an application, the PA is simple to use. The dc supply must be applied to two pins. These pins must be RF isolated to prevent unwanted feedback from leaking between stages. The output choke and dc blocking capacitor must be large enough and of enough quality as to prevent any interference in the application frequency. The inductor/choke to the input stage must be chosen as to set the input match. Typical values for this inductor are in the 1 to 6-nH range, depending on the frequency. For example, a 2.2-nH inductor is used for 2.4-GHz ISM band power amplifier. A small amount of shunt capacitance (0.5 to 2 pF) can be used on the output to improve power-added-efficiency for high power applications.

From "Miniature 3V LNA, VGA, and PA for Low Cost 5.4-GHz Wireless Applications," Henrik Morkner, Hewlett-Packard. 1997 Wireless Symposium.



Conference Shows The Lighter (And Low Power) Side Of Products

*Portable By Design Conference And Exhibition Gives Designers
 A Path Toward Portable-Related Components* **Richard Nass**

You've just been assigned the task of designing a portable system. That shouldn't be a problem—you've been designing desktop systems for years. Think again! There are many aspects of a portable design that differ from their stationary counterparts. To get your questions answered and to find some of the products that are built just for portable applications, check out the 1997 Portable By Design Conference and Exhibition, to be held at the Santa Clara Convention Center, Santa Clara, Calif., Mar. 25-27, 1997.

In addition to being exposed to some of the latest portable-related products, there will be some special events taking place, such as presentations by Jack Kilby, inventor of the integrated circuit, and Bob Pease, renowned analog engineer and columnist for *Electronic Design*. The keynote luncheon also will feature four individuals who will offer their views on the future of the portable industry: Tom Beaver, Vice-President of Worldwide Marketing, Motorola Inc.; Philip Wennblom, Director of Strategic Planning, Mobile and Handheld Products Group, Intel Corp.; Robin Saxby, President and CEO, Advanced RISC Machines (ARM); and Vaughn Watts, Director of Mobile Computing Architecture, Texas Instruments (See "Portable By Design: Special Events").

Over 80 portable-product manufacturers will display their wares at Portable By Design. Products include microprocessors, chip sets, memory chips and cards, batteries, thermal-management devices, transceivers, voltage regulators, and input devices.

With the unveiling of the Windows CE operating system, which is geared toward low-power, portable systems, the VR4101 microprocessor becomes an attractive CPU choice. Developed by NEC Electronics Inc., Santa Clara, Calif., the 64-bit RISC processor features 33 VAX MIPS performance and 132 MIPS/W at 3.3 V, as well as DMA capability. A high-speed multiply-and-accumulate (MAC) feature enables the chip to run DSP-like instructions. As a result, the chip can replace external hardware by running some of

the required functions in software.

The NEC device also integrates many of the functions required by a handheld platform. These include a modem and interfaces to an LCD, audio, a keyboard, and an infrared (IR) port. With a power consumption of 250 mW at 33 MHz, the VR4101 contains several power-savings modes. In standby, with the pipeline frozen, the part consumes 30 mW, while the suspend mode, which shuts down the pipeline and bus clocks, requires 10 mW. Hibernate mode freezes the internal phase-locked loop and requires just 240 W.

CSEM IC Design, Neuchâtel, Switzerland, will show its CoolRISC family of microcontrollers. The chips are designed from the get-go for low power dissipation. This comes from the use of gated-clock techniques and low-voltage cell libraries. The architecture allows for the execution of all instructions, including branch instructions, in just one clock cycle. The result is a performance level of 12 MIPS while consuming just 2.4

mW at 3.3 V. Other features include support for hierarchical memories, variable frequency modes, and multicontroller operation.

CONNECTING THE BRIDGES

A series of chips that connect to the microprocessor help form a complete system, including the bus interfaces, real-time clock, I/O ports, and docking connections. The chip set, called the Mobile System Solution, hails from National Semiconductor Corp., Santa Clara, Calif. The chip set consists of the PC87550 PCI system controller (North Bridge), the PC87560 system I/O controller (South Bridge), and the PC87570 keyboard and power-management controller. The parts also can connect to the company's previously-announced PT80C525 PCI-to-PCI bridge chip.

The North Bridge part is designed to work with Pentium-class processors. It supplies a CPU-to-PCI-bus interface, secondary cache and DRAM control, and active and pas-



1. The FKB7600 series of 85-key keyboards has a vertical height of just 6.5 mm. However, it retains a 3-mm, full-travel keystroke by employing a gear-link mechanism in the keyswitch.

sive power-management modes. It also supports hot, warm, and cold docking. The South Bridge provides PCI bus mastering for the chip's two Enhanced IDE channels, a USB host controller, and a 4-Mbit/s infrared controller. Lastly, the PC87570 can replace up to five chips. Based on an embedded RISC processor core, the chip handles power management and keyboard and system control. It also supplies analog-to-digital and digital-to-analog conversion.

A pair of 3-V pen-input processors deliver the low current consumption required for battery-powered handwriting recognition and verification products. Designed by TriTech Microelectronics International Inc., San Jose, Calif., the TR88L803 and TR88L804 can detect when pen input has stopped, then automatically places the system into a sleep mode until pen input resumes. The difference between the two ICs lies in their interfacing options—the TR88L803 offers a serial interface, while the TR88L804 comes with an 8-bit parallel interface.

The two parts contain all the circuitry needed to interface with the low-cost resistive digitizers employed in PDAs, electronic organizers, and feature phones. Using a 10-bit analog-to-digital converter (ADC), the TR88L803/L804 can resolve up to 1024 voltage levels, resulting in better than 200 dots/in. resolution on a 3- by 5-in. touch pad. Two additional ADC input channels are available under a multiplex mode to allow portable products to include such features as a battery gauge and handwriting pressure sensing. Positional transfer rates of 200 coordinate pairs/s are typical using a 1.8432-MHz crystal. A higher-frequency crystal increases the transfer rates.

On a subsystem level, the Cardio-486D4, which is a credit-card-sized PC-AT, now supports Windows NT 4.0. Designers taking advantage of the Cardio-486D4, developed by S-MOS Systems Inc., San Jose, Calif., can realize a savings in resources, development costs, and time to market. The embedded version of Windows NT 4.0 is offered by VenturCom Inc., Cambridge, Mass. The memory requirement for the operating system is 8 Mbytes, while the Cardio-486D4 can hold up to 16 Mbytes.

The SMX/386, designed by ZF MicroSystems Inc., Palo Alto, Calif., is a 2.2- by 3-in. module that combines standard motherboard functions in a 240-pin package. The device contains a 33-MHz 386SX microprocessor, core logic, a DRAM controller, an 8- or 16-bit ISA bus, serial and parallel ports, floppy and hard-disk controllers, and 256 kbytes of flash memory. It also holds an AT-compatible

BIOS and an embedded version of DOS.

One of the ways designers are implementing an embedded operating system or BIOS is with flash memory. Nexcom Technology Inc., Sunnyvale, Calif., offers a pair of high-density serial flash memories. Employing the standard 4-pin serial peripheral interface (SPI), the NX25F040 and NX25F080 memories hold 4 and 8 Mbytes, respectively. Based on the company's NexFlash technology, the chips are suited for such applications as digital cameras, voice and data pagers, voice recorders, and handheld terminals and data loggers.

Operating at either 3.3 or 5 V, the NX25F040 and NX25F080 are built with 536-byte sectors that program quickly, thereby maximizing battery life. Data can be transferred to and from the devices at 20 MHz. Typical program times are 2.5 ms/sector, allowing for sustained programming rates of over 200 kbytes/s, including erase time. Other features include byte-level addressing, double-buffered sector writes, auto-erase before write, and an advanced write protection.

The Miniature Card Implementers Forum, Folsom, Calif., will be displaying a host of products from its member companies. These products include storage devices that fit various consumer electronics products such as a digital camera, an audio voice recorder, and a handheld computer. The Miniature Card is a PC-compatible digital media that stores data in nonvolatile removable memory. The cards measure 38 by 33 by 3.5 mm and can hold up to 64 Mbytes.

The Miniature Card specification calls for both 3.3- and 5-V voltage levels, with lower voltages expected in future revisions. The

specification is a subset of the standard PC Card interface. As a result, transfers from a Miniature Card to a PC can be made with a low-cost Type II PC Card adapter. In addition, the Universal Serial Bus (USB) provides a means of transferring data to and from a card.

A similar form-factor product comes from Duel Systems, San Jose, Calif. The company offers a sonically-welded CompactFlash card package. Manufactured from insert-molded stainless steel and plastic, the rugged packages give designers the maximum real estate, and clean and rapid assembly. Before being welded, the package can be snapped together for testing purposes. Duel Systems also offers a line of PC Card packages, with a Type III card coming shortly.

One of the limiting factors of a notebook computer's size is its keyboard. That limit will shrink thanks to the FKB7600 series of keyboards from Fujitsu Takamisawa America Inc., Sunnyvale, Calif. (Fig. 1). Despite the keyboard's vertical height of 6.5 mm, it retains a 3-mm, full-travel keystroke by employing a gear-link mechanism in the keyswitch. Combined with an operating force of 55 g and a 20-g tactile force, the FKB7600 keyboard gives the user the needed key feedback. The 85-key model weighs 120 g and measures 287 by 109 mm.

Using a single IC, an operating system and BIOS can control any SMBus-compatible device that's connected to the IC's SMBus port. Developed by USAR Systems, New IC, an operating system and BIOS can control any SMBus-compatible device that's connected to the IC's SMBus port. Developed by USAR Systems, New York, N.Y., the UR5HC SMB BatteryCoder achieves its SMBus implemen-

Portable By Design: Special Events

For the first time, attendees will have an opportunity to mix and mingle with the manufacturers and suppliers of portable products on the exhibit floor during the Industry Reception, which takes place on Tuesday, Mar. 25, from 5:00 p.m. to 8:00 p.m. The casual atmosphere will provide a great forum for attendees to glean the information they need.

An added highlight to this year's Industry Reception: Jack Kilby, inventor of the integrated circuit, will present the First Annual *Electronic Design* Award For Technical Innovation. This award will be given to the author of Portable By Design's "Best Paper."

Simon Ellis of Intel Corp. also will make a presentation at the Industry Reception. He'll unveil his "Portable Videoconferencing Center" which will give attendees a peak at the future of one of the more anticipated technologies.

On Wednesday, Mar. 26, at 11:00 a.m., Bob Pease, renowned analog engineer and author of *Electronic Design*'s "Pease Porridge" column, will enlighten attendees with a unique presentation that only he can give. He'll come back at 1:00 p.m. on the same day to talk to the attendees and autograph copies of his *Electronic Design* Compendium of Pease Porridge columns.

tation through a set of PS/2 protocol extensions. Through these extensions, commands can be sent from the host through the 8042 port to the BatteryCoder. The subsequently sends the commands to the appropriate SM-Bus device. These devices include smart batteries and chargers, digital potentiometers, EEPROMs, port expanders, temperature sensors, and power-plane controls.

POWERING THE SYSTEM

One of the most essential components of a portable system is its batteries. As one would expect, there'll be no shortage of batteries at Portable By Design. For example, GP Batteries, San Diego, Calif., has developed a

1/3AAA NiMH battery with a nominal capacity of 100 mAh. The GP10AAAAM has a diameter of 10.25 mm, a height of 13.7 mm, and a weight of 5 g (Fig. 2). The recommended discharge current limits are from 10 to 300 mA with a typical service life of 500 cycles.

A second offering from GP Batteries is the GP80AAAAM, which fits the 7/5 form factor. With a capacity of 800 mAh and a AAA diameter (10.5 mm), the NiMH battery is a candidate to replace prismatic batteries. In a cellular telephone, the expected talk time is 140 min., with a standby time of 22 hours.

Battery Technologies Inc. (BTI), Ontario, Canada, has developed a rechargeable alka-

line manganese (RAM) battery available in AA, AAA, C, and D sizes. In addition to selling the batteries themselves, BTI will sell licenses and production equipment for third parties to build and sell the RAM batteries. According to the company, the batteries will hold a charge for up to five years and won't exhibit any memory effect, regardless of the usage pattern.

High energy density is the hallmark of the ELI-18650 rechargeable Lithium-Ion (Li-Ion) battery, developed by Energizer Power Systems, Gainesville, Fla. (Fig. 3). The 18-by-65-mm cell produces 3.6 V and 1350 mAh. Suitable applications include portable computers, cellular telephones, camcorders,

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S-MOS Systems Inc.

San Jose, Calif.
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Cambridge, Mass.
(617) 661-1230
Internet: <http://www.vci.com>



2. With a typical service life of 500 cycles, the GP10AAAM 1/3AAA NiMH battery offers a nominal capacity of 100 mAh.

and other handheld electronic devices. The battery contains a graphitic carbon anode and lithium-cobalt-oxide cathode in an organic electrolyte. Intelligent charging and fuel-gauge options are available. Because Li-Ion batteries require a specific charging technique for proper charging, Energizer will offer comprehensive technical and design support.

Portable Energy Products Inc., Scotts Valley, Calif., has developed an auxiliary battery pack that can power a notebook computer or a camcorder for up to 10 hours or a cellular telephone for a week. The battery is rated at 12 V and 5 A (60 Wh).

The LifeX BR1632DK2 computer backup battery for notebook computers is available from Rayovac Corp., Madison, Wis. The lithium coin cell offers a 130-mAh rating and can withstand rigorous thermal environments. Also from Rayovac is a charge-discharge controller, which lets designers test, measure, and evaluate the performance of the company's Renewal Rechargeable Alkaline batteries in their own devices. Co-developed with Benchmarq Microelectronics Inc., Dallas, Texas, the bq2902 and bq2903 work with up to two or four cells, respectively. The chips combine sensitive full-charge detection with a low-battery cutoff to provide overcharge protection. By maintaining proper charging characteristics, battery life can be prolonged.

Benchmarq also offers a series of products to monitor and supervise up to four Li-Ion cells. The bq2153, bq2150L, and bq2165L modules enable battery makers and system OEMs to implement protection circuits and battery electronics for Li-Ion packs without the lengthy design times typically associated with custom solutions. The 2153 is a pack supervisor; the 2150L is a power gauge; and the

2165L combines the functionality of the 2153 and 2150L. The three products are intended for such products as cellular telephones, portable PCs, handheld terminals, and other wireless communications devices. Each board can be configured to meet the specification of the particular battery pack, including the number of cells, the nominal pack capacity, and the battery type (coke or graphite anode).

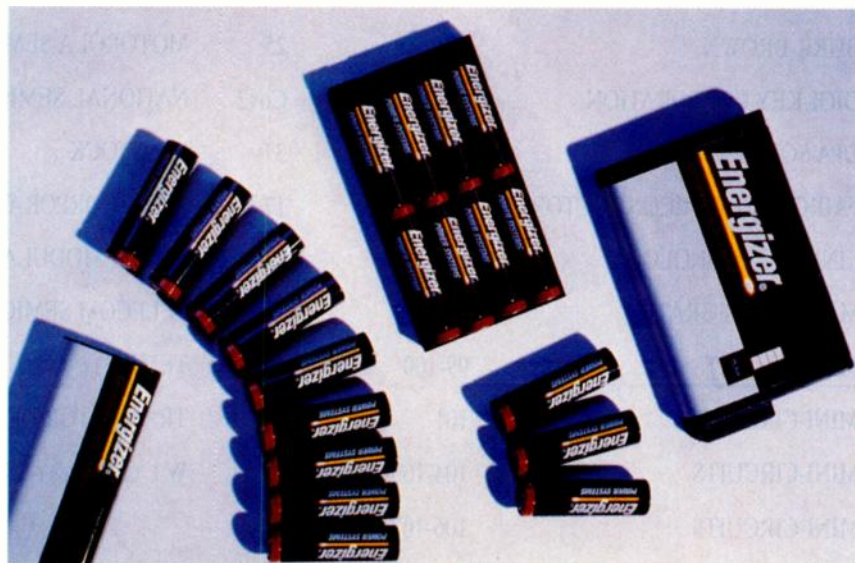
The on-chip series FET built into the UCC3911 battery-pack protector helps to reduce manufacturing costs and increases reliability. Designed by Unitrode Corp., Merrimack, N.H., the chip works with Li-Ion batteries. The part safeguards applications against battery-output short circuits and protects both Li-Ion cells in two-cell packs from overcharge and over-discharge.

The UCC3911 employs a bandgap voltage reference that detects when either cell is in an overcharged or over-discharged state. The series FET switch then opens, protecting the cells. A negative feedback loop controls the FET switch when the battery pack is in either the overcharged or over-discharged state and allows for pack recovery. In the overcharged state, the feedback loop only allows discharge current to pass through the FET switch, while in the over-discharged state, only charging current is allowed to flow. In addition, the chip enters a sleep mode in the over-discharged state until it senses the pack is being discharged.

A series of battery-management products from Dallas Semiconductor Corp., Dallas, Texas, can be placed into two categories—battery chargers and battery instrumentation and identification. The DS1333 charger works with Li, NiCd, NiMH, and lead-acid batteries. The part is programmed to attain any current-vs.-voltage curve the designer requires and uses either V_{max} or an on-chip timer to determine charge termination.

The DS2434, which falls into the Dallas Semiconductor's battery instrumentation and identification category, features an ID code that users can define so that the supporting electronics can identify the battery pack. The chip also removes the need for a thermistor in the pack because it contains a direct-to-digital thermometer. In addition, an integrated non-volatile memory lets designers enter data such as gas-gauge levels and warranty information.

There's now a cure for ill-behaved or power-unfriendly software applications and



3. The ELI-18650 rechargeable Lithium-Ion battery offers a high energy density—1350 mAh in an 18-by-65-mm cell.

drivers—the Intel Power Monitor (IPM). The free utility, developed by Intel Corp., Santa Clara, Calif., can be downloaded from the company's Internet site: <http://www.intel.com/ial/ipm>. Two versions are available, one for end-users and one for developers.

A second initiative resulted in a power-management specification—the Advanced Configuration and Power Interface (ACPI). When implemented, the ACPI allows a PC to instantly power up when accessed by the user or perform automated tasks when turned off. In other words, the ACPI enables PCs to enter a "sleep" state, rather than off. The specification, which can also be downloaded from the Internet at <http://www.teleport.com/~acpi/>, is fully compatible with existing power-management and configuration interfaces, while providing a processor- and operating-system-independent implementation.

In a typical portable design, board space is at a premium. The MultiGuard Series of four-element transient voltage suppressors (TVS), developed by AVX Corp., Myrtle Beach, S.C., can help save some of that valuable space. According to the company, the device consumes less than 10% of the board area required in an alternative solution. The part's

multilayer construction provides protection from voltage transients caused by ESD, lightning, and inductive switching. The TVS arrays can be used on any electronic printed-circuit board that contains multiple chips of the same voltage (energy) rating. The most frequent use for such a device is the I/O data lines in a portable computer or the RF amplifier in a cellular telephone.

One of the keys to a portable computer is its ability to communicate with other platforms. To facilitate this process, Temic Semiconductors, Santa Clara, Calif., has developed an IrDA-compatible transceiver that offers a transmission rate up to 4 Mbits/s. Housed in a top-view, surface-mount epoxy resin package, TFDT6000 measures just 13 by 7.5 by 5.65 mm. Integrated components include the diodes, emitter, and analog circuitry needed for a complete IrDA implementation. The TFDT6000 is aimed at designers that can't accommodate a side-view transceiver because of board-layout issues or packaging limitations. By integrating the receiver's preamplifier and the transmitter's driver stage, the TFDT6000 combines the functions of two ICs.

A second wireless communications product comes from Lucent Technologies, Murray

Hill, N.J. The WaveModem 2.4-GHz wireless LAN module lets system integrators offer high-speed data communications to their platforms. The device is suited for such applications as factory-floor monitoring, mobile point-of-sale terminals, scanning systems, bar-code readers, or notebook and handheld computers.

The WaveModem module incorporates Direct Sequence Spread Spectrum (DSSS) technology to provide reliable high-speed transmissions. The device incorporates a dual-antenna design to improve signal quality. Modem connections to the host platform are made using the WaveModem Modem interface.

A standard solution for various telecommunications and portable electronics devices comes from the 70AD male and female modular battery contacts. The contacts, designed by Bourns Inc., Riverside, Calif., are available in two- to six-pin configurations. Available in surface-mount or through-hole mount, high-temperature molded plastic maintains the 70AD's integrity for surface mount while captured contact springs prevent contact from being inadvertently damaged.

Originally published in Electronic Design, March 17, 1997.

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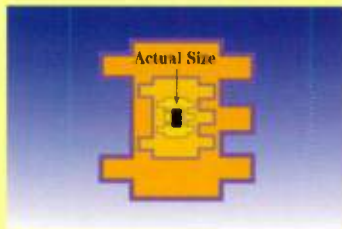
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- ▶ MIC6270—General purpose comparator
- ▶ MIC6251/2—Instrumentation amplifiers
- ▶ MIC7101/2—Single and dual operational amplifiers
- ▶ MIC7111—Rail-to-rail input and output amplifier
- ▶ MIC7211—Rail-to-rail input comparator



Extended Common-Mode Range

These devices feature an input common-mode range that extends beyond the supply voltage rails.

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Op Amps										
MIC6211	Bipolar	±2.5V to ±10V	2.0mA	2.5MHz	4μV/°C	—	6V/μs	2mV	50nA	—
MIC7101	CMOS	2.4V to 15V	250μA	1.0MHz	1μV/°C	—	1V/μs	3mV	1pA	—
MIC7102	CMOS	2.4V to 15V	250μA	1.0MHz	1μV/°C	—	1V/μs	3mV	3pA	—
MIC7111	CMOS	2.4V to 10V	25μA	50kHz	2μV/°C	—	15mV/μs	3mV	1pA	—
Comparators										
MIC6270	Bipolar	±2.5V to ±18V	300μA	—	—	—	—	2mV	25nA	1.3μs
MIC7211	CMOS	2.4V to 10V	7μA	—	1μV/°C	—	—	3mV	0.5pA	4.0μs
Instrumentation Amp										
MIC6251/2	Bipolar	±2.5V to ±18V	2.0mA	2MHz	7μV/°C	0.5% max.	6V/μs	4mV	50nA	—

IttyBitty SOT-23-5 Packaging

Micrel's IttyBitty and MM8 packages are the ideal solutions for designers of high-density systems such as cell phones, pagers, USB devices, PCMCIA cards and portable instrumentation. They are also ideal for applications where amplifier proximity to a sensor and/or short signal path is critical.

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Micrel's amplifiers carry performance beyond functionality. Operating from a single or split supply, performance is specified and guaranteed with supply voltages as low as 2.4V, most with supply currents less than 1mA.

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- ▶ Input common-mode range extends beyond supply voltage rails
- ▶ Guaranteed performance with supply voltages as low as 2.4V
- ▶ Low supply current
- ▶ Guaranteed performance over the full industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- ▶ IttyBitty SOT-23-5 package saves space and weight

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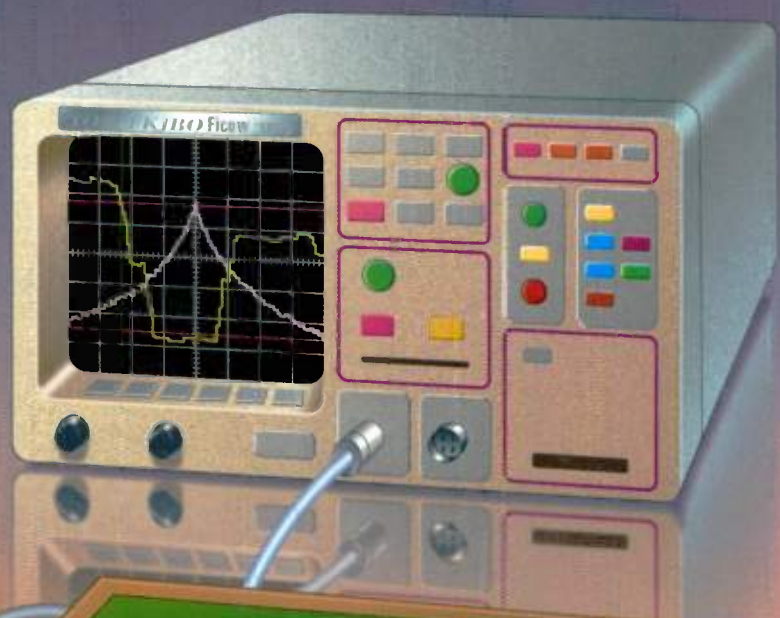
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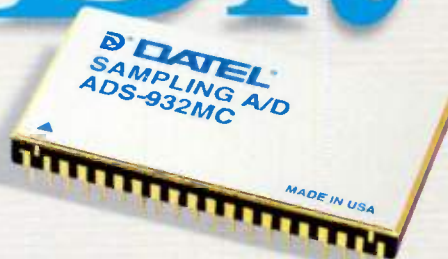
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^② Specified without distortion (for SNR) under Nyquist conditions ($f_{in} = 1/2 f_s$) with $V_{in} = -0.5dB$.

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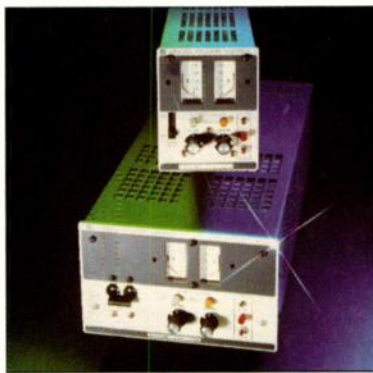
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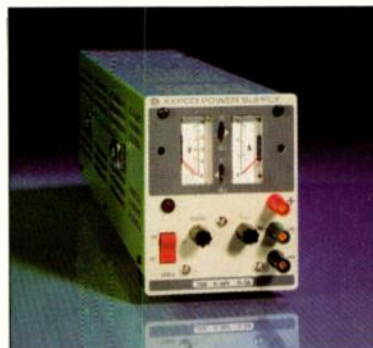
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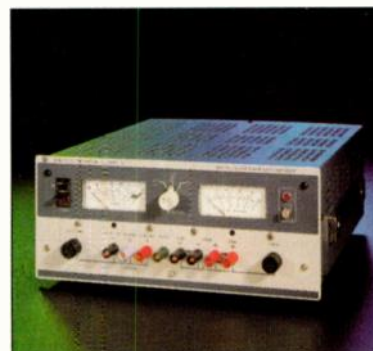
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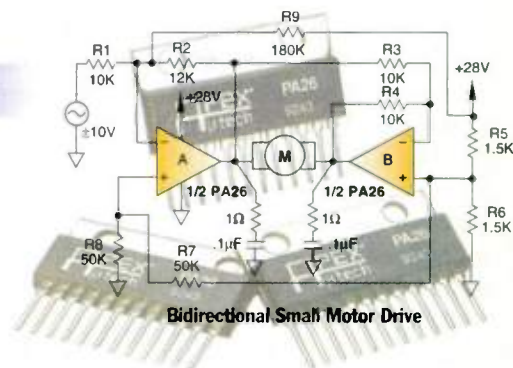
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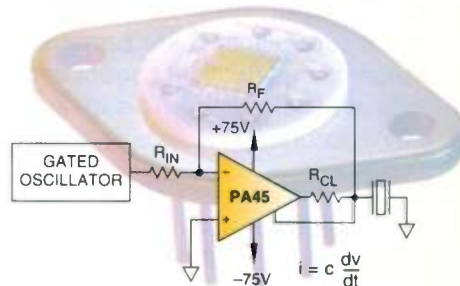
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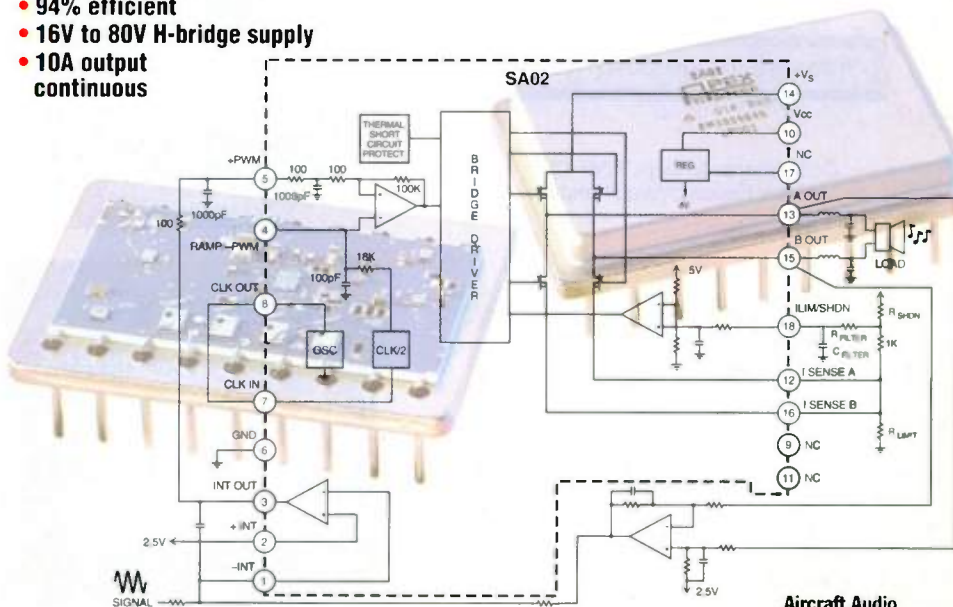


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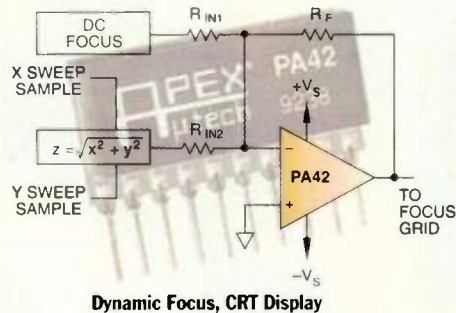
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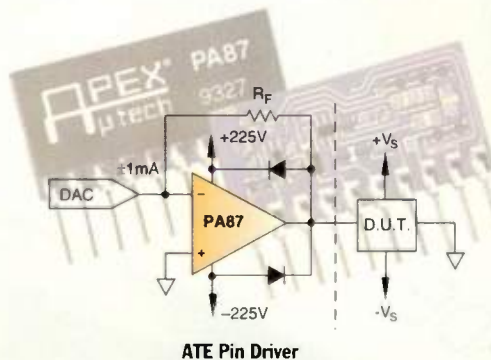
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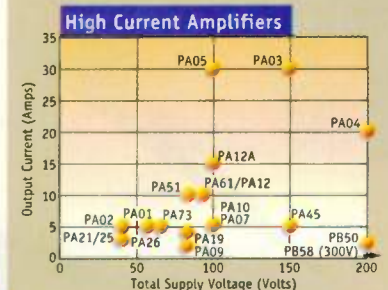
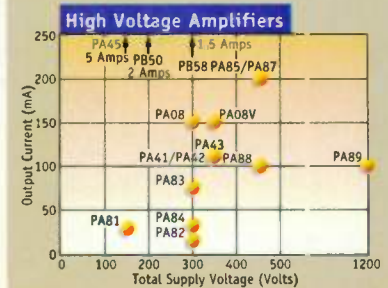
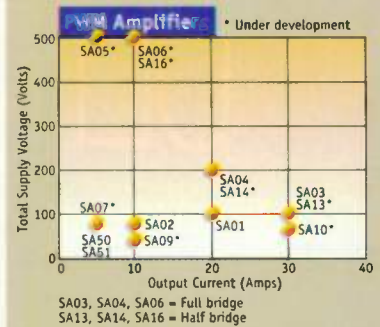
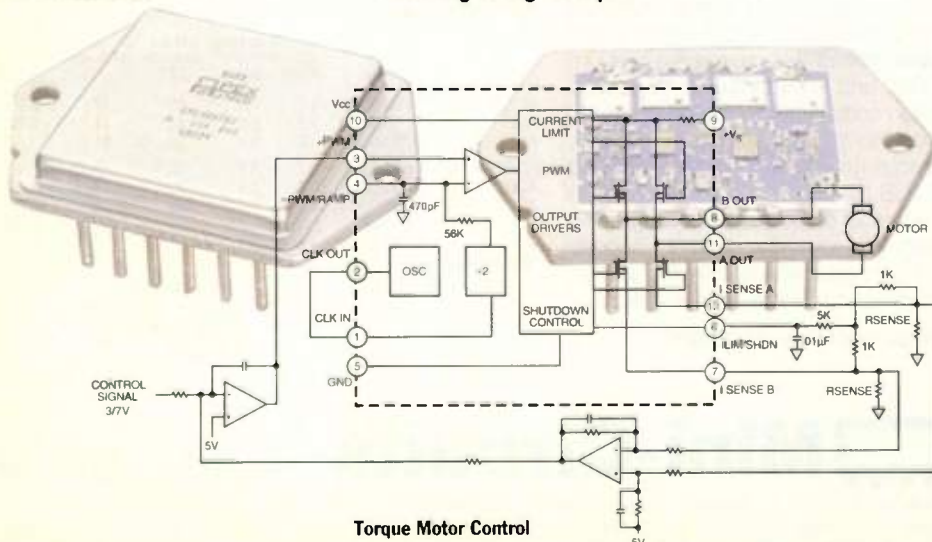
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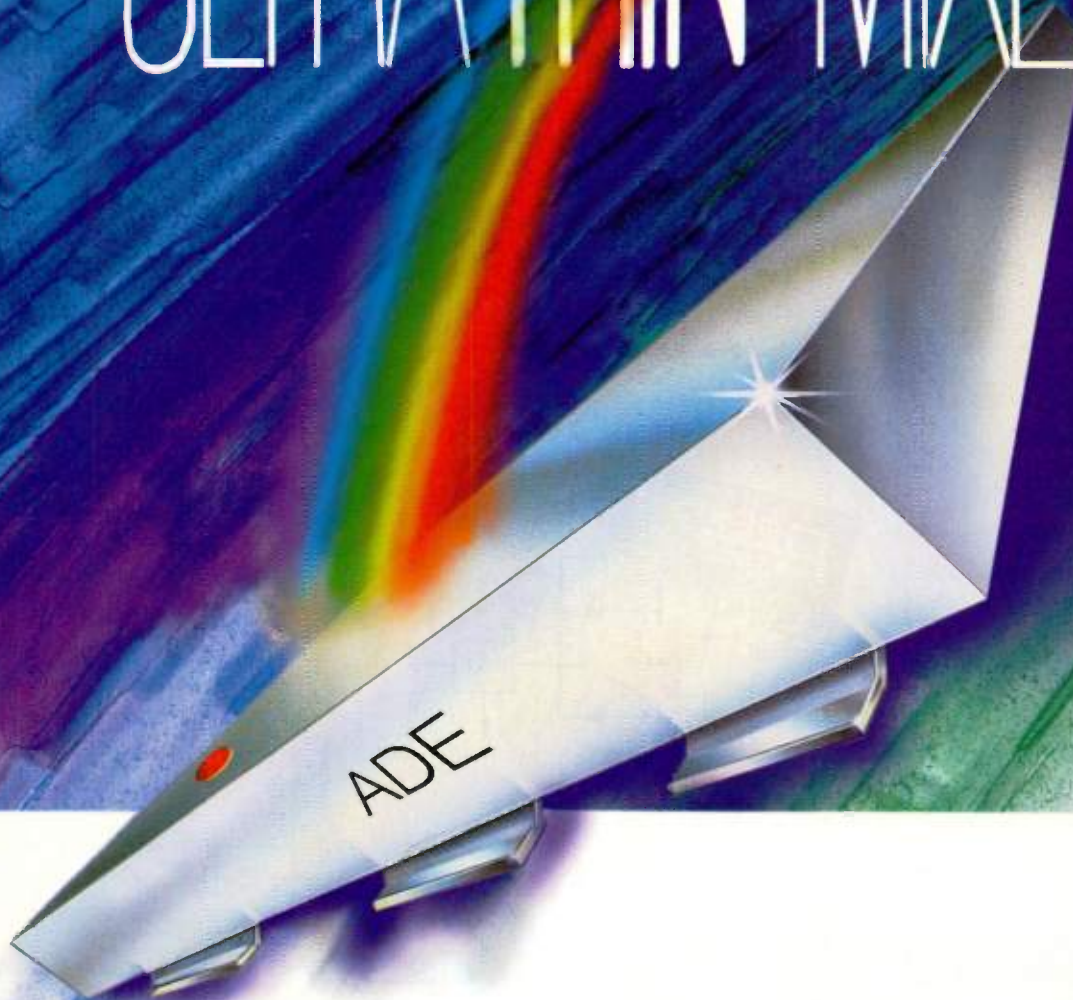
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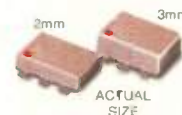
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ADE-901	3	800-1000	+7	5.9	32	13	2.95
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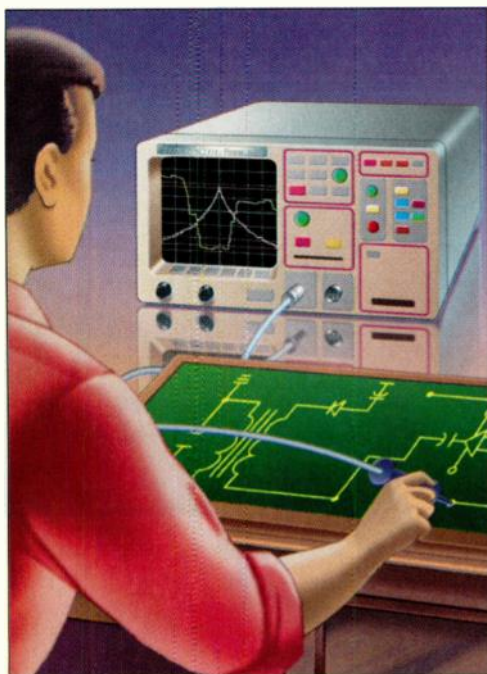
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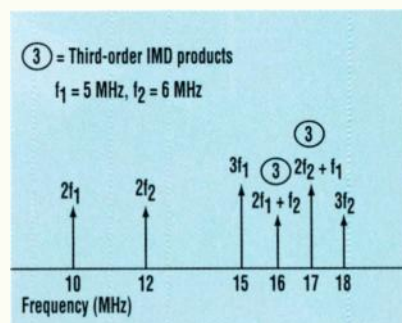
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10

A NEW GENERATION: SPECIFYING OP AMPS IN THE 90s

BY EAMON NASH,
Analog Devices Inc.

The current breed of high-speed op amps and applications are making manufacturers rethink the way they specify these devices.

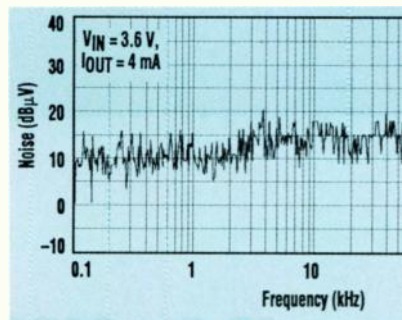


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DC-DC CONVERSION TECHNIQUES FOR NOISE-SENSITIVE APPLICATIONS

BY LEONARD SHERMAN,
Maxim Integrated Products

What are your options when strict noise constraints conflict with power-supply requirements?

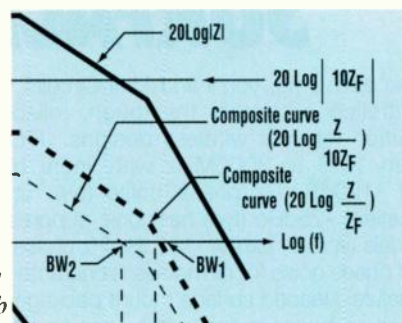


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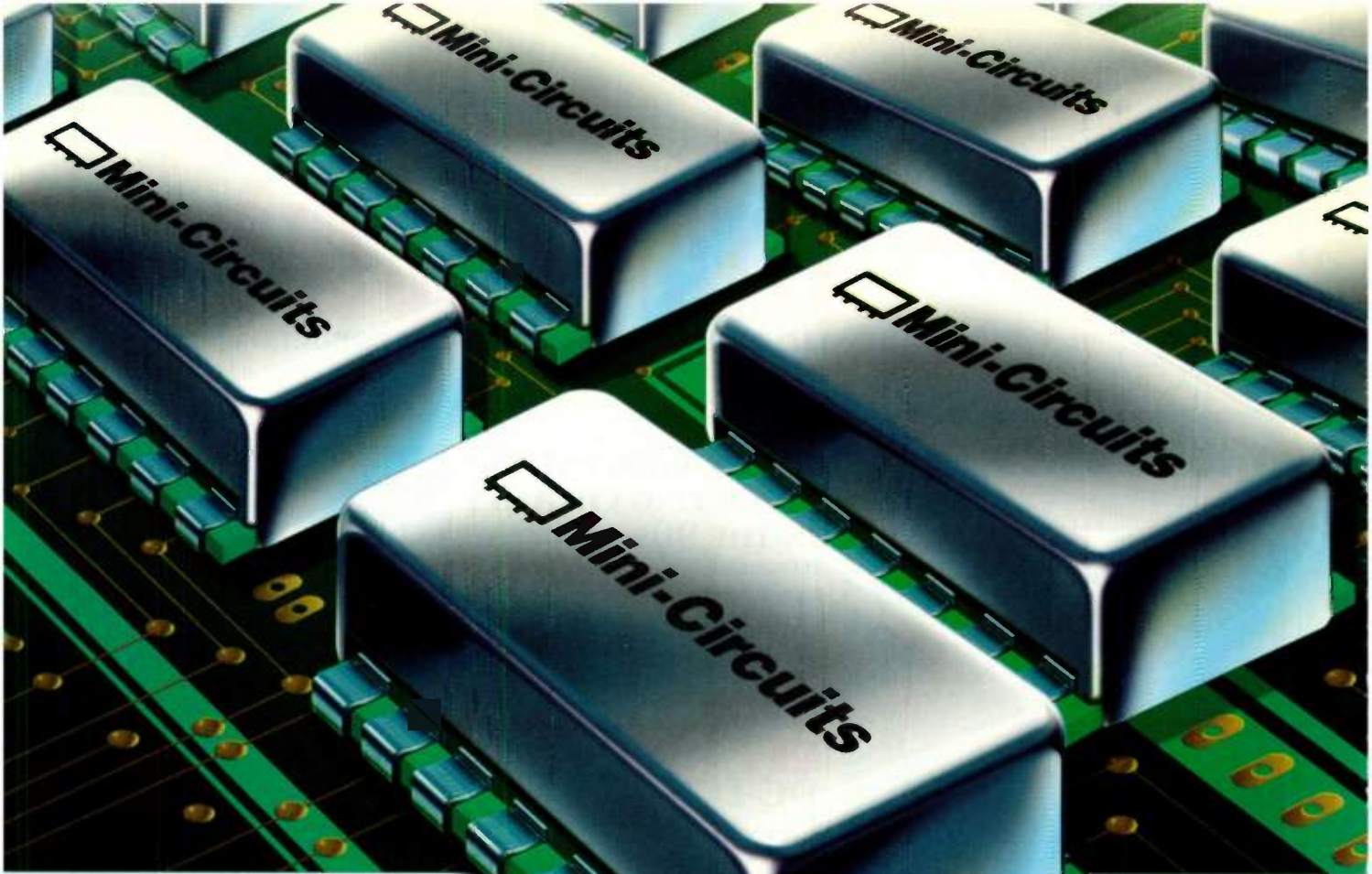
AN INTUITIVE APPROACH TO CURRENT-FEEDBACK AMPLIFIERS

BY JEFF LIES and RON MANCINI,
Harris Semiconductor

Circuits that combine high bandwidths, fast slew rates, and low power consumption are possible with design insight.



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ANALOG PRODUCTS

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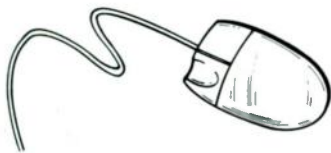
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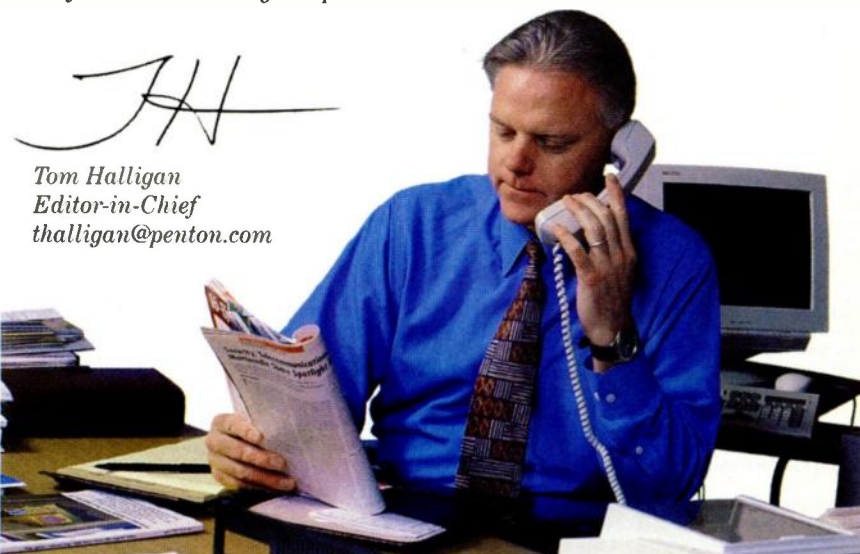
Analog just doesn't go away, does it? Your circuits have to be faster, smaller, quieter, more complex, swing from rail-to-rail, operate at lower supply voltages, and consume less power. Pretty challenging, isn't it? That's why we bring you these Analog Supplements—to help you keep pace. We scour the analog community, looking for cream-of-the-crop articles, and innovative useful circuit designs. And they're written by some of the best and brightest authors in the industry. You'll see some familiar contributors and some new ones—old-timers, newcomers, gurus, and gurus-in-the-making. You deserve nothing but the best. And we intend to keep giving you the best analog design information available. Let's take a peek at what's in store for you this time around.

Eamon Nash gets things rolling with a look at the new ways op amps are being specified. Specifications like spurious-free dynamic range, third-order intercept point, and noise figure relate better to today's (and tomorrow's) performance requirements. Next, everybody knows that switchers and noise go hand-in-hand. Well—not necessarily. Len Sherman takes us on a tour of dc-dc conversion techniques for noise-sensitive applications. Finally, Jeff Lies and Ron Mancini will get your brain cells working with an "intuitive" approach to understanding current-feedback amplifiers. It's really easy. All you need to know is how they differ from, and are similar to, voltage-feedback amplifiers.

Of course, no Analog Supplement would be complete without a few words from our regular columnists. If you thought Bob Pease exhausted the subject of thermostats in our last supplement, you were wrong. He's back—with "Thermostat Stuff, Part Two." And Walt Jung is always looking for an excuse to fire up his Audio Precision measurement system. (He loves those plots that extend beyond -100 dB.) This time, he tackles common-mode noise susceptibility.

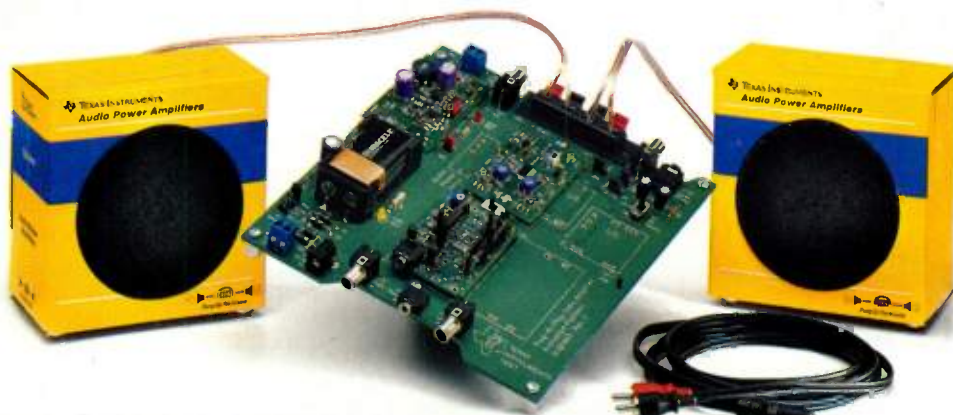
And we've got our usual potpourri of Analog Briefs that we're sure you'll find interesting. Here's a quick rundown: bet you haven't thought of turning an active bus terminator into a Class D audio amplifier. You'll also find a NiCd protection circuit that "fools" a radio into tripping its 0.75-V/cell memory/clock protection mode when the NiCds are actually at 1 V/cell. Or, how about a method for obtaining isolated feedback in a power supply without using optocouplers or an extra transformer winding? And we've got a nice baseline restorer circuit, a three-IC current-limiting power supply, a boost controller for extending alkaline cell usage, and a wideband current amplifier.

Sound interesting? Well, kick back your feet, take your eyes off that 75-dpi computer display, and peruse these hi-res 2400-dpi pages. Then let me know what you think at thalligan@penton.com.



TH
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 **TEXAS
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A New Generation: Specifying Op Amps In The 90s

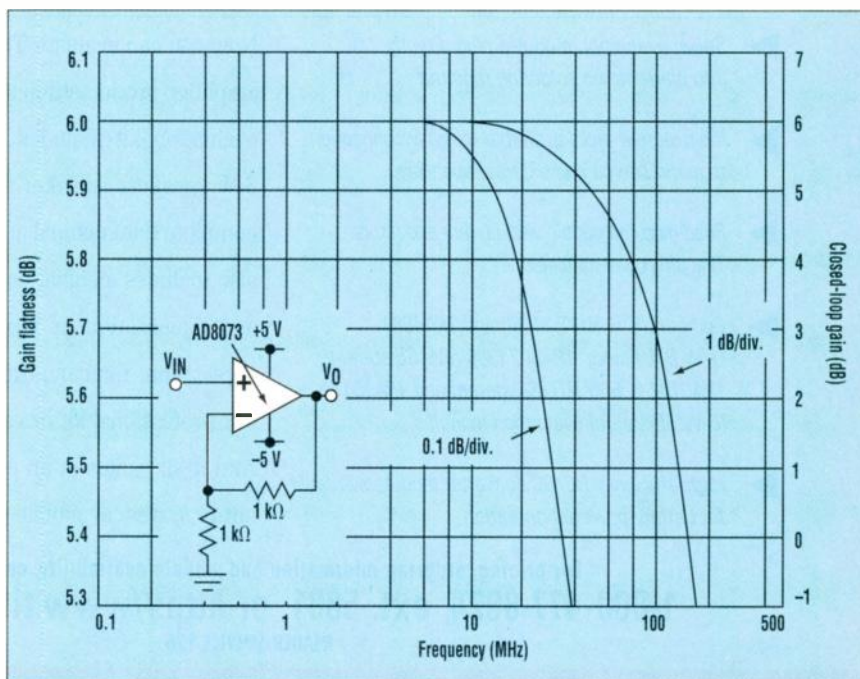
The Current Breed Of High-Speed Op Amps And Applications Are Making Manufacturers Rethink The Way They Specify These Devices.

Eamon Nash
Analog Devices Inc.

The semiconductor industry has basically been using the same specifications to characterize high-speed operational amplifiers for over 30 years, even though these devices have gone through many changes during this time.¹ More importantly, the number of applications in which these amplifiers are used has increased dramatically.

For example, in video applications where gain flatness over frequency is critical, a -3-dB bandwidth can be an unreliable selection criterion if interpreted incorrectly. With supply voltages dropping to 5 V and lower, it's increasingly important to have quantitative measures of op-amp performance at output voltage swings that go close to the rails. In telecommunications applications, RF designers relate much better to noise figure, third-order intercept, and 1-dB compression point than they do to noise spectral density, total harmonic distortion, and output voltage swing.

As a result, op-amp manufacturers need to continually reexamine the way high-speed operational amplifiers are specified. Tests performed in the past are not al-



1 The AD8073's frequency response at a closed-loop gain of +2 is flat to within 0.1 dB out to 14 MHz, while the 3-dB bandwidth extends to 100 MHz. A lack of flatness in the frequency response in the region of interest (up to 5 MHz in this case) will produce video artifacts in television applications.

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OP-AMP SPECIFICATIONS

ways relevant to newer devices. In some cases this testing can be wasteful, increasing production test time and ultimately leading to a higher selling price. In most cases, however, older specifications are still useful, but need to be augmented depending upon the specific application.

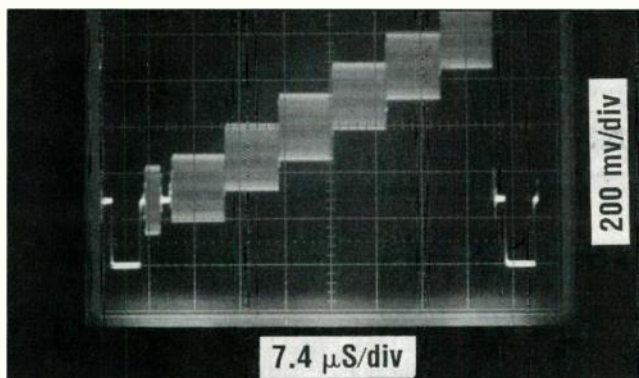
BANDWIDTH AND VIDEO

Composite television signals—NTSC, PAL, or SECAM—have a signal bandwidth of about 5 MHz. Any amplifier that's conducting such a signal shouldn't degrade the signal significantly. If the gain response of the amplifier starts to roll-off below 5 MHz, the sharpness of the picture will be degraded. Based on this fact, we could make the assumption that the bandwidth of a TV-video amplifier should be at least 5 MHz. But consider what we mean by the term bandwidth.

Look at the frequency response of the AD8073, a triple, low-cost, current-feedback op amp that's typically used in video-line driving applications (Fig. 1). The plot shows the bandwidth for a closed-loop gain of +2 on both 1-dB/div. and 0.1-dB/div. scales.

From the 1-dB/div. scale, we can read off the -3-dB bandwidth as 100 MHz. While -3-dB bandwidth and slew rate are the most common terms used to compare the speed of op amps, in video applications the frequency over which the gain is constant is of more concern. Therefore, the 0.1-dB/div. curve, which tells us that the AD8073's gain error remains within a 0.1-dB window up to a frequency of 14 MHz, is actually more useful. Gain flatness of 0.1 dB out to 14 MHz is quite acceptable for consumer video applications. However, for professional video applications that call for a flatness out to frequencies of around 30 MHz, a more appropriate device would be AD8002, which has a flat response out to 90 MHz.

If a 0.1-dB gain flatness specification is unavailable, the engineer can estimate its value using the -3-dB bandwidth. If the peaking of the frequency response is much less than 1 dB, the 0.1-dB bandwidth will



2 The color information in a single line of NTSC video is contained in the amplitude and phase (relative to the reference burst that comes after the sync pulse) of the 3.58-MHz signal that is superimposed upon the luminance ramp. Undesirable picture artifacts appear if the small-signal gain and phase of an op amp vary with the level of the quasi-dc luminance ramp.

be about one-seventh of the -3-dB bandwidth.

When peaking occurs at unity gain, it can be quite difficult to predict the bandwidth (-3 dB or 0.1 dB) of an amplifier at higher gains. Traditionally, voltage-feedback amplifiers are specified in terms of unity-gain frequency response. The circuit designer can then use the constant gain-bandwidth product to calculate the closed-loop bandwidth at a particular gain.

Calculating the closed-loop bandwidth is more complicated in the case of a current-feedback amplifier, where the closed-loop bandwidth is more constant for different closed-loop gains.² However, in both the voltage-feedback and current-feedback cases, the actual closed-loop bandwidth at gains greater than one will be less than the calculated value where the unity-gain response peaks significantly.

The most practical solution to this dilemma is for op amp manufacturers to either specify or supply plots of fre-

quency response for various closed-loop gains. This solution has become common in the case of current-feedback amplifiers, and is becoming increasingly popular in voltage-feedback amplifier datasheets.

Let's look at an oscilloscope photo of the time-domain representation of a single line of a color NTSC burst (Fig. 2). Most popular video standards, such as NTSC and PAL, combine chroma and luma information into a composite signal. The color information is contained in the 3.58-MHz sub-carrier burst that sits on the luminance

ramp. During the luminance ramp, the gain and phase of the burst are compared to the reference burst that comes just after the sync pulse. If a video amplifier alters the gain and phase of the color burst as the luminance level ramps, undesirable artifacts will appear in the picture.

Differential gain and phase are measures of the change in gain and phase of a small signal as the dc level of that signal varies. These specifications are, therefore, extremely useful in predicting the extent to which an op amp will reliably amplify a video signal. However, future video standards, most notably high-definition television (HDTV) and digital tv, are unlikely to use a ramped sub-carrier to convey picture information. As a result, the differential gain and phase specification of video operational amplifiers will become less relevant as new television standards are rolled out.

While the small-signal bandwidth of any amplifier is of interest, the

NOISE CALCULATION

Noise source	Calculation formula	Resulting output noise
R_G	$(\sqrt{4KTR_G})(R_F/R_G)$	8.44 nV/√Hz
R_S	$(\sqrt{4KTR_S})(1+R_F/R_G)$	9.27 nV/√Hz
R_F	$\sqrt{4KTR_F}$	2.78 nV/√Hz
i_+	$i_{R_S}(1+R_F/R_G)$	1 nV/√Hz
i_-	i_{R_F}	8.46 nV/√Hz
e_n	$e_n(1+R_F/R_G)$	20 nV/√Hz
Total output noise (N_o)	Quadratic sum of all sources	25.25 nV/√Hz
Input noise (N_i)	$\sqrt{4KTR_S}$	0.9 nV/√Hz
Noise figure	$20\log(N_o/GN_i)$	8.96 dB

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ERA-2	DC-6000	15.6	12.8	4.7	26.0	40	1.95
ERA-2SM	DC-6000	15.2	12.4	4.6	26.0	40	2.00
ERA-3	DC-3000	20.8	12.1	3.8	23.0	35	2.10
ERA-3SM	DC-3000	20.2	11.5	3.8	23.0	35	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32.5	65	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4.20
ERA-5	DC-4000	18.8	▲18.4	4.5	▲33.0	65	4.15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4.20
ERA-6	DC-4000	11.3	▲18.5	8.4	▲36.5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8.4	▲36.0	70	4.20

Note: Specs typical at 2GHz, 25°C. Exception: ▲ indicates typ. numbers tested at 1GHz.

* Low frequency cutoff determined by external coupling capacitors.

③ Price (ea.) Qty.1000: ERA-1 \$1.19, -2 \$1.33, -3 \$1.48, -4, -5 or -6 \$2.95. SM option same price.

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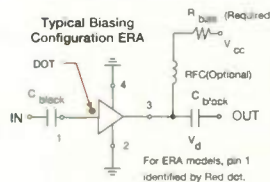
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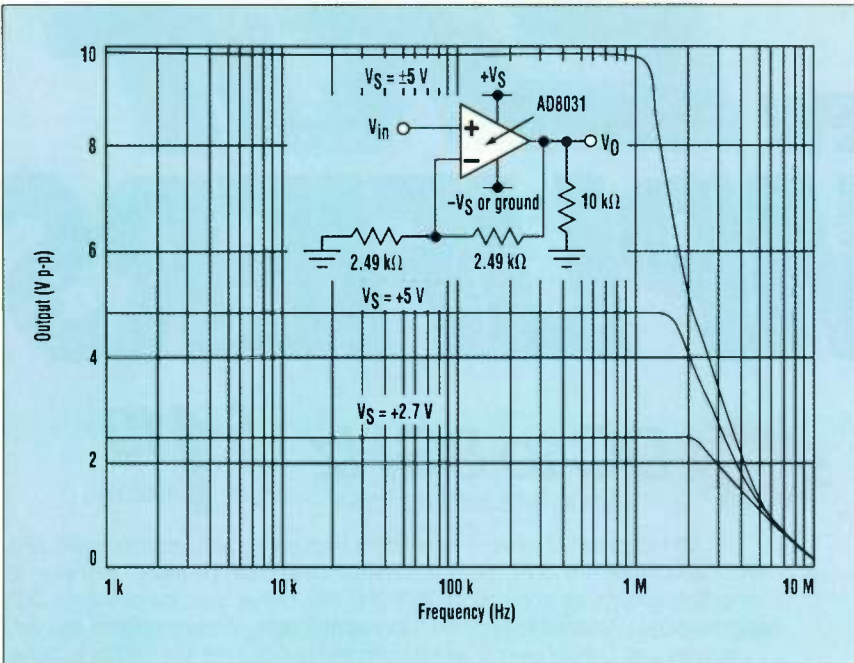
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OP-AMP SPECIFICATIONS



3 While the small-signal bandwidth ($V_0 = 400$ mV p-p) of the AD8031 op amp is 80 MHz, the device's slew rate limits the bandwidth when the output signal is made to swing close to the power supply rails.

large-signal bandwidth of a rail-to-rail amplifier is more relevant. If a rail-to-rail amplifier operating on a single +5-V supply is driving an analog-to-digital converter (ADC) with a 0- to +5-V input range, then the bandwidth specification of the op amp swinging from 0 to +5 V is important.

Front-page bandwidth specifications of an op amp are typically measured under small-signal conditions. Small signal is not clearly defined, but generally refers to a peak-to-peak output signal voltage of between 100 mV and 500 mV. The term large signal (sometimes called "full-power response") also is not well defined, but usually refers to a 2-V peak-to-peak output signal. So neither of these terms tells us how much bandwidth we will get if we want maximum available signal swing.

The term rail-to-rail also is poorly defined. Because no signal can swing all of the way to both rails, rail-to-rail is generally understood to mean the ability to swing close to both rails (where close means less than 200 mV). Non-rail-to-rail op amps, on the other hand, usually swing to within 1 V of the rails at best.

Consider a plot of bandwidth versus signal swing for the AD8031 (a low-power, high-speed, rail-to-rail am-

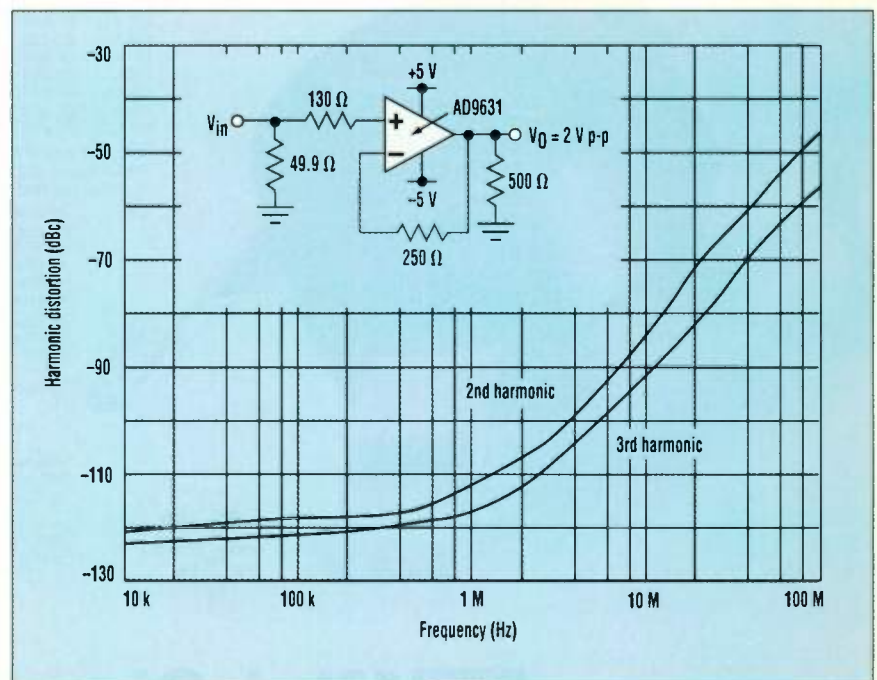
plifier) under three different power-supply conditions (Fig. 3). The small-signal bandwidth of the AD8031 is 80 MHz ($V_0 = 0.4$ V p-p). We can see from Figure 3 that the bandwidth decreases to about 1.06 MHz when the

output swings close to the rails on a ± 5 -V supply. At lower supplies (and consequently lower output signal swings) of +5-V single and +2.7-V single, the bandwidth improves slightly to 1.27 MHz and 3 MHz, respectively. However, all of these numbers are far away from the original 80 MHz.

If a plot such as the one referred to above is not to be found in the data sheet, an estimate of the output swing versus frequency can be made using the specified slew rate. Given the slew rate and the maximum output swing (both of these can be found in the specifications section of the datasheet), the full-power bandwidth can be calculated using the following equation:

$$\text{Bandwidth} = \frac{\text{Slew rate}}{\pi(\text{Peak-to-peak signal swing})}$$

It should be noted that in some cases, the slew-rate specification of an op amp is based upon unrealistic operation modes. For example, some op amps exhibit optimum slew rate when the output is heavily overdriven. This slew rate decreases when the operation is linear. In order to use the above equation to estimate bandwidth, the



4 Total harmonic distortion gives the quadratic sum of the first six harmonics of a signal, but it will usually be dominated by the second and third harmonics. Plotting these harmonics over frequency gives a good indication of the spectrum of the output signal at a particular frequency.

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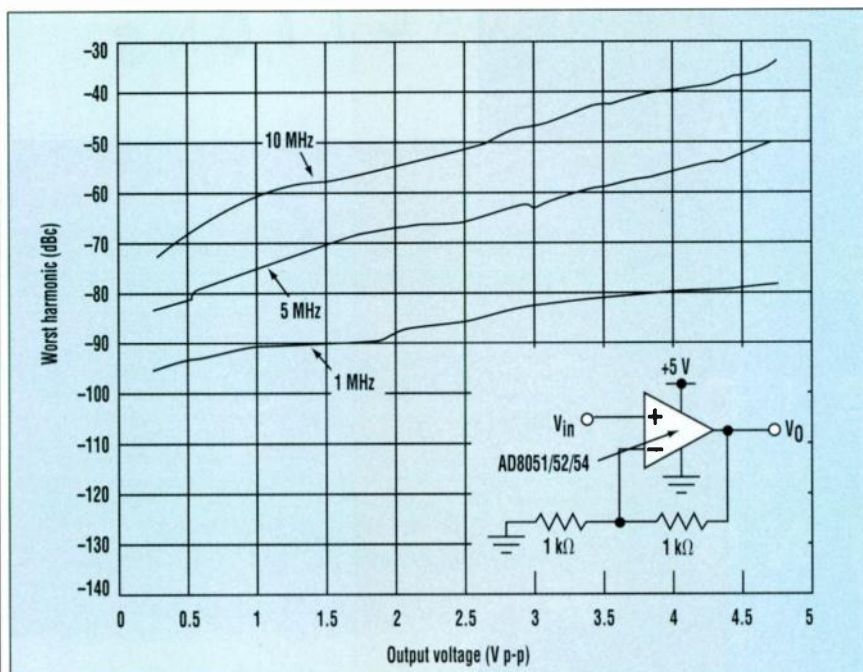


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OP-AMP SPECIFICATIONS



5 Data sheets usually specify distortion for low signal swings. Plots that show how distortion varies with frequency and increasing signal amplitude are more appropriate for rail-to-rail amplifiers where large signal swings are common.

op amp's slew-rate specification must be based upon linear operation.

THD VERSUS SFDR

Traditionally, total harmonic distortion (THD) has been used to specify the distortion of an operational amplifier. THD is defined as the ratio of the amplitude of the fundamental frequency to the root sum square of the harmonics. Because the higher-order harmonics decrease in amplitude, generally only the first five harmonics are used in the calculation:

$$\text{THD} = \frac{V}{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}$$

Total harmonic distortion has its roots in audio applications. It's customary and practical in audio applications to evaluate the quality of a signal in terms of how it sounds. As such, low THD correlates well with signals that sound good. THD, however, tells us little about the amplitude of the individual harmonics.

So it's possible that two devices with the same THD could have very different spectral profiles. The same value of THD can result from a single large harmonic or from multiple har-

monics of lower amplitude. All sampled-data systems (in other words, ADCs) have a limit below which signals can't be measured. So the device with multiple (lower amplitude) harmonics of equal amplitude might be more desirable than the device with a single large harmonic.

Spurious-free dynamic range (SFDR) is becoming popular as a way of specifying distortion. SFDR is defined as the amplitude of the worst spurious component (commonly called the spur) relative to the amplitude of a fundamental tone. In the case of amplifiers, this spur will be harmonically related to the fundamental, and is usually, but not always, the second or third harmonic. In the case of ADCs or digital-to-analog converters (DACs), the worst spur is not necessarily harmonically related to the fundamental.

Because second and third harmonics usually dominate the distortion of an amplifier, it's quite common for manufacturers to supply a plot over frequency of the second and third harmonics in addition to specifying the SFDR (Fig. 4).

The specified load resistance of 500 Ω would be common in applications where the op amp is driving the input

of a high-speed ADC. However, in communications signal chains, a load of 100 Ω (50- Ω back termination resistor and 50- Ω load impedance) is more common. The distortion performance will degrade as the op amp's load impedance decreases. This information would be best conveyed by a second plot, indicating the performance under heavier loading conditions.

SIGNAL SWING AND DISTORTION

While plots of output swing versus frequency tell us how much signal swing we can expect at a particular frequency, they tell us little about the quality of the output signal. To estimate the quality, we need specifications that relate signal distortion to output swing (Fig. 5). Just like bandwidth, front-page-distortion specifications can be deceptive, as they generally specify distortion for signals having significant head room to the rails (also true in the case of rail-to-rail amplifiers). However, in applications where a rail-to-rail amplifier is driving a rail-to-rail CMOS ADC, information about large-signal distortion may be necessary.

A plot of worst harmonic distortion (i.e. largest harmonically-related spur) versus output signal swing for the AD8051/52/54, a family of high-speed rail-to-rail op amps is demonstrated (Fig. 5, again). Even though these devices are rail-to-rail amplifiers, distortion degrades as the output signal approaches the rails and as the output frequency increases.

This plot could be considered to be more comprehensive than the previous plot (output swing versus frequency). In addition to telling us about the relationship between distortion and signal swing, it effectively tells what signal swing we can expect at a particular frequency. It should be noted that the distortion will get markedly worse at frequencies above 10 MHz. Also, at frequencies below 1 MHz, the distortion will not improve much more. As a result, this family of plots gives a fairly complete picture of the operating region (output voltage and frequency) of the AD8051/52/54.

We can deduce from Figure 5 that, in general, a signal should have up to roughly 100-mV headroom to each rail in order to achieve low distortion, even when using rail-to-rail ampli-



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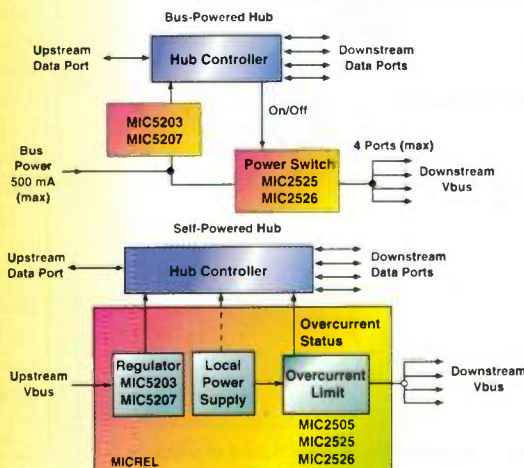
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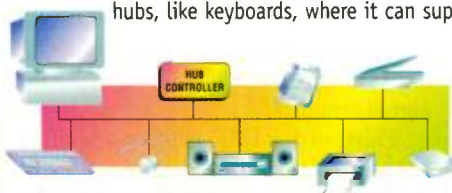
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Micrel offers the most comprehensive portfolio of products to satisfy any USB power distribution application. Our family of USB high-side switches offer fully compliant and exceptional protection for USB products such as PCs, monitors, printers, stand-alone hubs, and others. These switches provide a highly-integrated and cost-effective solution for both self-powered and bus-powered hubs. In addition, they give you the flexibility to design either global switching, for the lowest cost USB hub applications, or individual switching for more robust and flexible control for downstream devices.

Design Flexibility

For instance, the MIC2505 is a single, low-cost switch that will support four downstream ports for self-powered hub applications like USB monitors and printers.

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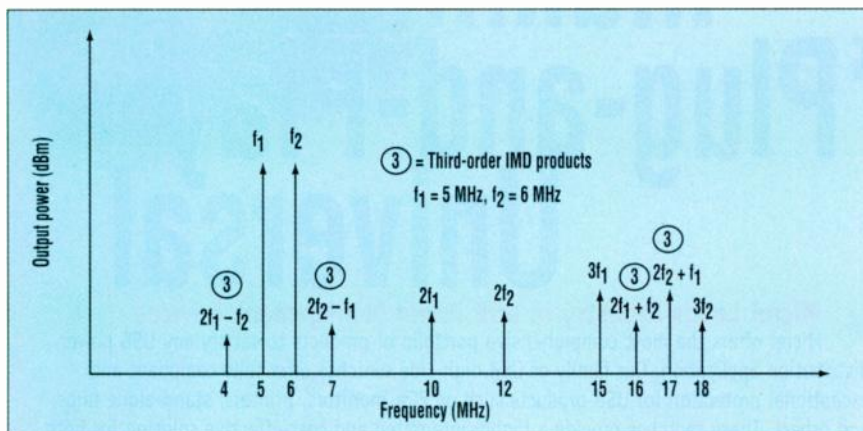
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OP-AMP SPECIFICATIONS



6 In multichannel communications applications, third-order intermodulation products can cause problems by masking small signals in neighboring channels. Harmonics of the fundamental signals are less of a problem, as they appear at multiples of the original frequencies.

fiers. Obviously, this figure will vary from device to device and over frequency (as shown). Also note that there is a large difference in the maximum frequency at which low distortion is attainable (10 MHz) and the closed-loop bandwidth (about 55 MHz for a gain of two) are attainable. This reinforces the idea discussed earlier that an op amp can rarely effectively amplify signals close in frequency to its -3-dB closed-loop bandwidth.

IMD AND IP3

Intermodulation distortion (IMD) products are of special interest in the RF area, and are a major concern in the design of radio receivers. While the harmonics of a single tone appear at multiples of the fundamental frequency, the third-order products that result from the intermodulation of two signals close in frequency, appear close to the fundamental frequency (Fig. 6). In multiple-channel communications applications, these third-order IMD products can mask a small signal in an adjacent channel.

Intermodulation is measured by applying two spectrally pure tones to the input of the op amp. The amplitudes of the fundamental and third-order products can be read by looking at the output signal on a spectrum analyzer. The level of intermodulation distortion will degrade with in-

creasing signal amplitude and increasing frequency.

Third-order intermodulation products increase 3 dB for each 1-dB increase in the amplitude of the fundamental tones. As a result, a spectral plot of IMD does not immediately indicate the level of IMD for a different signal amplitude.

Third-order IMD is often specified in terms of third-order intercept point (IP3). Because the amplitude of IMD products increases 3 dB for each 1-dB increase in the fundamental, a theoretical point can be reached where the amplitude of the third-order IMD products are equal in amplitude to the fundamental tones. This output level

is called the third-order intercept.

If IP3 isn't specified, as is commonly the case with op-amp datasheets, don't worry—it's simple to derive yourself (Fig. 7).

On a plot of output-signal amplitude versus input-signal amplitude (the gain of the circuit should be normalized to unity), draw a line with a slope of one through the origin. The output amplitude of one of the fundamental tones (both would normally be equal) is plotted on this line. Directly under this point, the amplitude of one of the intermodulation products (again, both should be equal) is plotted. Next, draw a line with a slope of 3 through this point. The vertical point at which the slope-of-one line and the slope-of-three line intersect is the third-order intercept.

Once the third-order intercept has been calculated, the output power of third-order IMD products can be estimated for other signal levels using the equation:

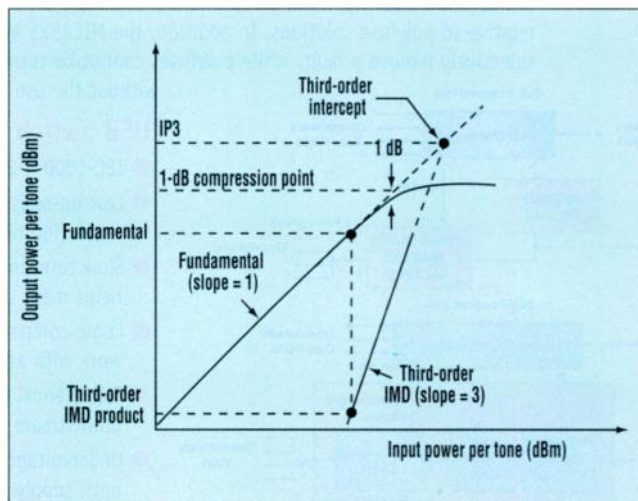
$$IP3 - P3 = 3 \times (IP3 - P_0)$$

where P_0 = output power in dBm, $P3$ = output power of third order IMD products in dBm, and $IP3$ = third-order intercept in dBm. This equation can be simplified to:

$$P3 = 3P_0 - 2IP3$$

In practice, the point will never be reached where the intermodulation products become equal to the output signal because the output signal will begin to soft limit or compress at some level. The power level in dBm at which the output is 1 dB below its ideal level is called the 1-dB compression point (Fig. 7, again).

RF engineers generally use the 1-dB compression point as a measure of the available signal swing. It's a useful alternative to simply specifying signal swing because it's a measurement of power, and as such gives an indication of the maximum output voltage and current levels for a particular load impedance (usually 50 Ω).



7 Third-order intercept is defined as the theoretical point at which the third-order intermodulation products become as large as the original output signal. In practice, the output signal will limit or compress before this point is reached.

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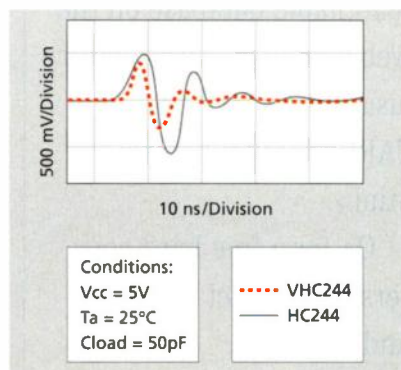
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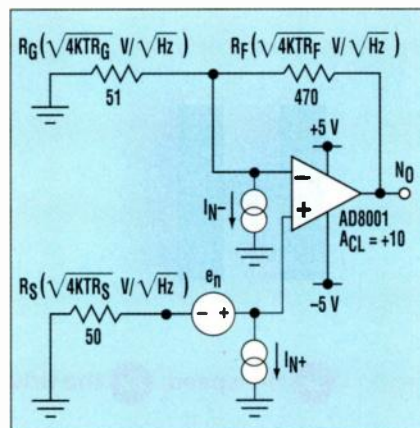
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ELECTRONIC DESIGN ANALOG APPLICATIONS

OP-AMP SPECIFICATIONS



8 The total output noise of an op-amp circuit is a function of the source impedance, the voltage and current noise sources in the inputs, the resistors used to set the closed-loop gain, and the closed-loop gain itself.

While RF designers generally use noise figure to compare amplifiers, op-amp noise has traditionally been specified in terms of noise spectral density. While this is becoming less acceptable in communications applications, there is a plausible reason for not specifying noise figure on an op-amp's data sheet.

Noise figure is defined as the ratio of the signal-to-noise ratio (SNR) at the device's output to the SNR at the device's input. The noise at the input is usually defined to be the Johnson noise of a 50-Ω resistor.

The noise figure specification is useful for (fixed) gain-block-type amplifiers. However, because op amps have configurable gains, the noise figure of the closed-loop circuit will vary depending on the closed-loop gain and on the size of the feedback resistors. As a result, it's difficult to assign a "one-covers-all" noise figure to an op amp. From a straight specification point of view, the best that a op-amp manufacturer could do would be to specify the noise figure for a particular closed-loop gain using specified resistor values.

But not to worry—noise figure is easily calculated if we know the input current and voltage-noise spectral densities of the op amp, along with the closed-loop gain and the size of the feedback resistors. Add together all of the noise sources in the closed-loop circuit. Let's use the following example: an AD8001 high-speed, low-noise op amp configured for a positive gain of

ten (Fig. 8). The (input-referred) voltage-noise spectral density is amplified by the closed-loop gain of the op amp. The noise current sources draw current through the source impedances to which they are connected, generating two noise voltages. Because the noise currents are not correlated (they are completely independent of each other), there is no possibility that they will cancel each other out in any way. This fact is true for both current-feedback and voltage-feedback op amps.

The feedback and source resistors contribute Johnson noise to the circuit. Depending upon the position of the resistor, the resulting noise voltages are amplified by the inverting gain, the noninverting gain, or not at all in the case of R_F .

We need to calculate each source's contribution to the overall output noise (see the table). Note that K refers to Boltzman's constant (1.38×10^{-23}) and T refers to the ambient temperature of 398 K (25° C).

In this example, we'll define the input noise to be equal to the Johnson noise of a 50-Ω resistor ($\sqrt{4KTR_S}$). The noise figure is, therefore given by:

$$\text{Noise figure} = \frac{\text{Output noise}}{(\text{Gain} \times \text{Input noise})}$$

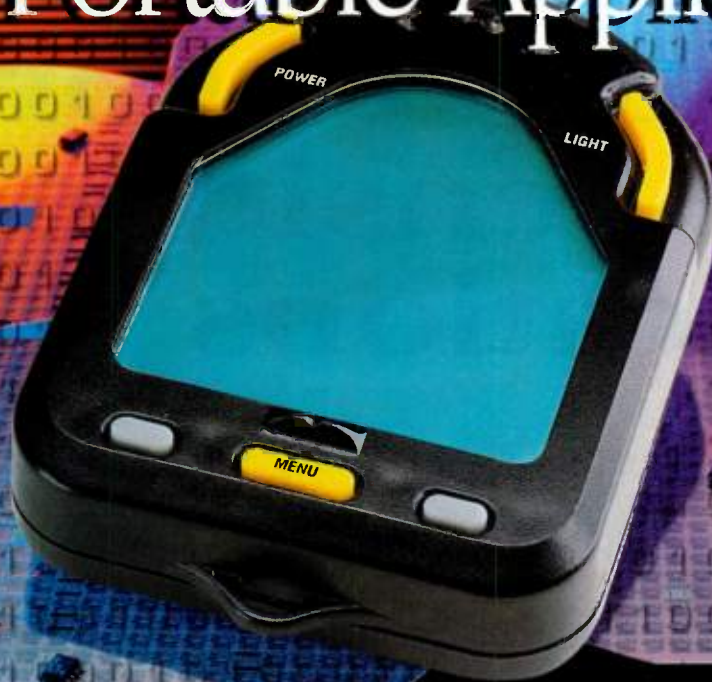
$$= 20 \log_{10}(25.25 / (10 \times 0.9)) \\ = 8.96 \text{ dB}$$

EAMON NASH is an application engineer at Analog Devices. He holds a B.ENG in Electronics from the University of Limerick, Ireland. Nash can be reached at Analog Devices Inc., 804 Woburn St., MS-125, Wilmington, MA 01887; (617) 937-1239; e-mail: eamon.nash@analog.com.

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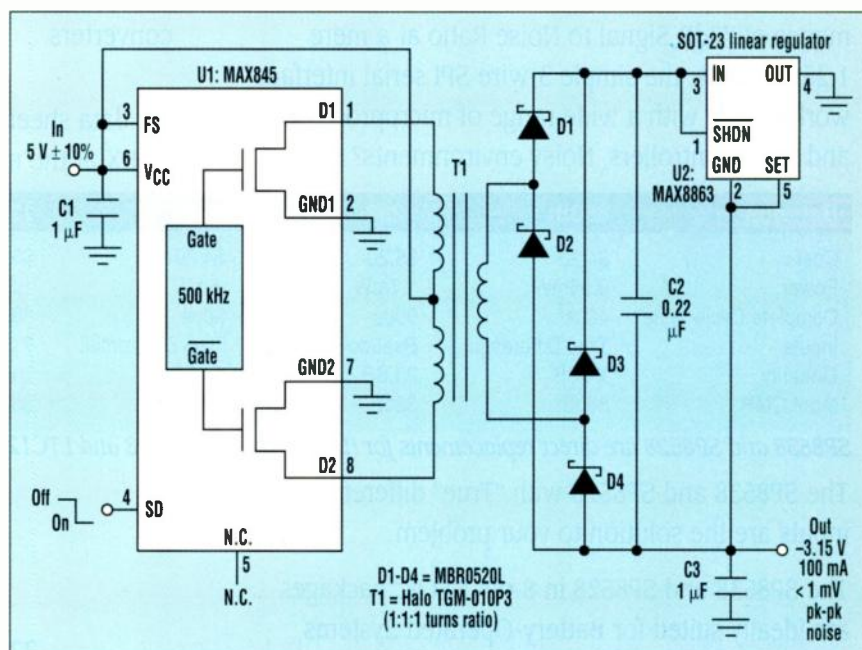
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Designers typically avoid dc-dc converter circuits in applications that demand low noise. The power for sensitive analog systems is often resigned to linear supplies that sacrifice portability and battery life to maintain performance of RF circuits, low-noise amplifiers (LNAs), read-channel preamps, and other sensitive analog functions.

Nevertheless, the rapid growth of portable electronic and computing products has lead to a sort of shotgun marriage between low-noise analog and RF circuits, and switching voltage conversion. This article will explore options open to designers to smooth this union of disparate goals when strict noise and performance constraints conflict with power-supply requirements.

In most cases, the path to low-noise performance doesn't require exotic circuit techniques or the latest in IC features. Many low-noise power-supply designs are mostly conventional, with tweaks or additions to address the sensitivities of the load circuitry. The new ground presented here is interesting partly for the results achieved, but also because some well-worn techniques have been re-



1 Push-pull voltage conversion offers orders-of-magnitude of improvement in both input and output ripple compared to conventional voltage inverters. Input ripple is about 10 mV p-p, as is the ripple going into the linear regulator. Peak-to-peak noise and ripple at the -3-V output are well under 1 mV.



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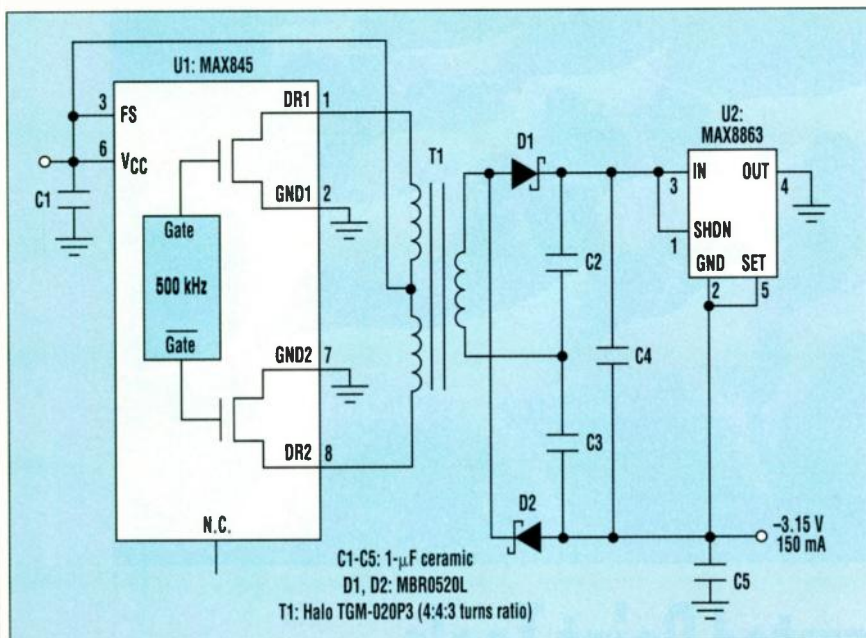
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cast for contemporary requirements.

The examples shown in this article focus on particular applications, but also can be adapted for other uses. The purpose here is not so much to provide canned circuits (however, they can be so employed), but to illustrate power-supply noise-reduction techniques that can be generally applied, usually without specialized ICs or exotic components.

PUSH-PULL CONVERTERS

Push-pull (sometimes called forward) dc-dc converters, are most popular in high-power (hundreds of watts) designs. This high-power image, and the fact that they require a transformer, may explain why the topology has rarely been considered for low-power or portable applications. Nevertheless, the characteristics that make these converters suitable for high power are the same qualities that, even when supplying only a few watts, can reduce noise, ripple, and EMI substantially when compared with other topologies.

A forward converter differs from the more common buck, boost, or inverting (inductor-based) dc-dc converter because energy is never really stored in the magnetic component. In a conventional inductor-based dc-dc

inverter, the inductor alternately collects energy from the input supply and transfers it to the output. The output filter capacitor alone must support the load while the coil is recharging.

The change in capacitor voltage during this cycle is responsible for output ripple, and the discontinuous input current waveforms cause ripple on the input supply as well. Output ripple is both a function of $(dV/dt) = I_{LOAD}/C_{FILT}$ and capacitor ESR. Also, inductor peak current must be much higher than the average output current because the coil can't be connected (and source current) to the load all of the time. It must toggle between the input and output at a duty cycle governed by the input/output voltage ratio.

In a push-pull design, the transformer doesn't store energy, but instead only transfers it. At any given instant, one of two switches is on, and current flows in the transformer's primary and secondary windings simultaneously. Note that this is not the case for all transformer designs because primary and secondary current do not flow simultaneously in flyback designs.

The push-pull design makes the ripple sources much more benign than with a conventional inverter because current flow in and out of the circuit is

nearly constant (if the load is constant), and peak transformer current is only slightly higher than the dc load current. Current is interrupted only during the break-before-make time between D1 and D2 turn-on. Because this interval is very short (<100 ns) filtering can be accomplished with very small capacitors.

The change in output voltage during a switching cycle depends on the capacity of the transformer core (the transformer's E-T product), and not capacitor size. The capacitor's primary job is to service the load during the dead-time between each half of the push-pull cycle. For an output capacitor this task is much easier than carrying the load current for a large fraction of a switch cycle, as is needed in a conventional inverter design.

The following two circuits employ a push-pull design in generating an ultra-quiet negative supply to power low-noise preamplifiers or other analog circuits that need split power supplies (Figs. 1 and 2). Negative supply noise often is critical in these designs because IC amplifiers many times exhibit poor rejection of noise on their negative rails.

An advantage of both of these circuits is that they achieve low input and output noise with low-value ceramic (non-electrolytic, non-tantalum) capacitors. This last issue is significant because ceramic capacitors provide superior reliability when compared to polarized types, especially under high-temperature accelerated testing. In addition, for low-capacitance values, ceramic capacitors consume the least board area.

The first circuit exhibits the lowest noise (<1 mV p-p), while the second trades a small increase in ripple for increased output current from the same size components.

A NEGATIVE RAIL

Magnetoresistive (MR) read/write heads in large-capacity hard disk drives present a challenge for quiet power-supply design. Most MR head preamps use both positive and negative power-supply rails. Single-supply MR preamps are available, but not with the same level of performance as split-supply designs.

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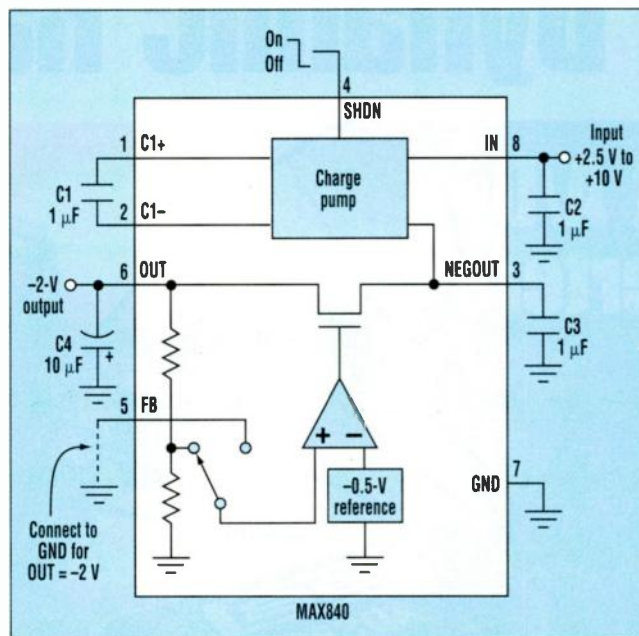
LOW-NOISE POWER CONVERSION

pass filtering) suffices for the positive rail, but the negative supply must be generated inside the hard drive. Because the motors in a hard drive use most of the power, efficiency is not a critical parameter for the preamp power supply. But cost, circuit size, and output noise and ripple are very important.

The circuit shown in Figure 1 generates -3.15 V (or other negative voltage) at 100 mA . It's built around a MAX845 push-pull transformer driver and a low-cost 2.4-mm-high surface-mount transformer. The push-pull design switches at 500 kHz , continuously transferring power to the output via the transformer and a four-diode full-wave bridge.

There are no large dI/dt current peaks or voltage peaks to be smoothed, therefore only $1\text{ }\mu\text{F}$ of capacitance is needed to fill during the dead time between switching cycles. The circuit generates both low-output and reflected-input noise. Peak-to-peak output noise and ripple are well below 1 mV p-p with only $1\text{-}\mu\text{F}$ or lower ceramic capacitors.

Without the linear regulator, peak-to-peak ripple is still only 10 mV . Input noise is dependent on the source impedance of the input supply, but when operated with a bench-type power supply it measures about 10 mV p-p at



4 In light-load applications, such as bias for GaAs power amplifiers, an internal regulator within a charge-pump IC reduces output ripple and noise to $< 1\text{ mV p-p}$.

50% load with $1\text{-}\mu\text{F}$ ceramic input bypass capacitance. With larger capacitance values, these amplitudes can be reduced further. The circuit's conversion efficiency is about 65% due to the use of a linear output regulator.

Because the transformer output floats, an added benefit of the topology is that a negative output can be regulated with a low-cost positive linear regulator. U2's OUT pin is connected to circuit ground while the regulated negative output is taken from the IC's GND pin. Incidentally, this trick can

be applied to any power supply where a transformer secondary, or other floating source, ends up providing a negative supply.

The connection in Figure 2 retains many of the low-noise characteristics of Figure 1, but increases output current to 150 mA without needing a larger transformer. Again, the floating output allows a positive linear regulator to control a negative output.

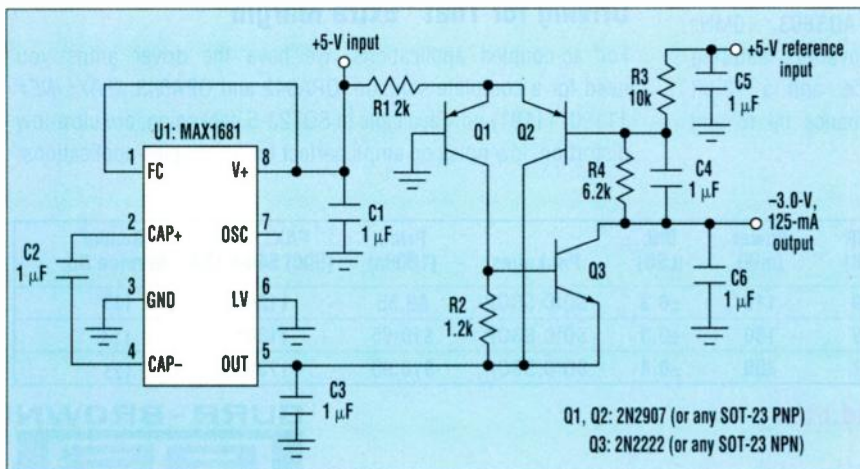
The circuit differs from Figure 1 in that it uses only a two-diode voltage-doubler configuration along with a transformer with a slightly lower secondary turns ratio ($4:4:3$ rather than $1:1:1$). This design does require C2 and C3 to store energy for half of each clock cycle, but the ripple waveforms on C2 and C3 are phased such that they nearly cancel, resulting in no more than 15 mV of ripple at the linear regulator input and less than 2 mV p-p at the output.

The two-diode rectifier reduces the voltage loss compared with the four-diode bridge, providing more headroom for the linear regulator, and thus greater output current before dropout. Input noise is similar to that of Figure 1 at about 20 mV . Output noise is about 2 mV p-p at 150-mA load current, and less than 1 mV p-p below 50 mA .

INDUCTORLESS DESIGNS

When noise sensitivity is a concern, such as in RF applications or where low-level signals are present, charge pumps may provide superior performance to other types of voltage converters. They also can allow voltage conversion to be used where previously only linear regulation could be considered. It's important to note that such advantages are by no means universal to all charge pumps.

The most direct advantage is the elimination of magnetic fields associated with the inductor or transformer. In other words, a significant EMI source is squelched. An EMI source that remains and can be troublesome in some designs is the high initial-charging current that can flow when the flying capacitors charge and dis-



3 A 1-MHz charge pump inverter teams with a very-low-cost discrete linear regulator to supply -3 V at 125 mA with less than 5 mV of peak-to-peak ripple and noise. Low-value ceramic capacitors are used.

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charge. The instantaneous current that flows is limited only by the resistance of the switch, which can be as low as a few ohms. These high dI/dt events can generate spike noise, whose elimination may require additional capacitance or post filters. However, in pump designs that have been tailored for low noise, such components aren't needed.

There are solutions for negative supply generation that forego inductors (Fig. 3). A capacitive charge pump inverts the +5-V input supply. Again, switching transients at the pump output preclude a direct connection to preamp negative bias input. However, a very cheap, but serviceable negative linear regulator can be fashioned from three transistors.

Unlike the previous transformer designs, a positive linear regulator can't be used because the output is no longer floating. As low-dropout negative regulators are not widely sold, a discrete design is used. For simplicity, the input supply serves as the reference. Therefore, output accuracy depends on input tolerance, which is adequate for most uses. Alternatively, a more precise reference source, if available, can be connected at R3 to improve output accuracy. Output ripple and noise for this connection are less than 5 mV p-p each, and output current is 125 mA at -3 V.

The use of a post regulator reduces noise more effectively than regulated charge-pump ICs that modulate either their internal switch resistances or switching rate. If 5-mV of ripple is still too high, larger filter values for C6 will further reduce it. The circuit operates with smaller charge pump capacitance (1 μF) than normal for the pump IC because only -3.0 V must be generated from a 4.5-V (min) input. The charge pump output can, therefore sag as much as 1 V from its ideal output ($-V_{IN}$) without impairing -3-V regulation. Like the

previous circuits, only ceramic capacitors no larger than 1 μF are used.

A drawback of the charge pump architecture is that transients on the input supply are larger than with the previous schemes. Measured peak-to-peak input ripple was 300 mV with a conventional bench supply as a source. This number can improve with a lower impedance source and/or filtering to isolate ripple generated at the input. Since the ripple frequency is high (1 MHz), it can be filtered effectively with small capacitance values.

In all of the previous circuits, the goal has been to generate a negative voltage. The designs, however, are not limited to voltage inversion. In the push-pull configurations, different turns ratios and secondary winding connections can easily create output voltages of either polarity. In charge-pump circuits, the input can be dou-

bled or multiplied by some other factor with other charge-pump ICs.

In light-load applications, low-noise post regulation can be included on chip as well (Fig. 4). In the circuit shown, the IC combines an inverting charge pump and a low-noise negative-output linear regulator to generate a very quiet negative bias voltage (-2 V at 4 mA) for GaAs FET RF power amplifiers from a 2.5- to 10-V dc input. A switching frequency of 100 kHz allows small-value capacitors to be used, while the on-chip regulator reduces output ripple and noise to only less than 1 mV p-p.

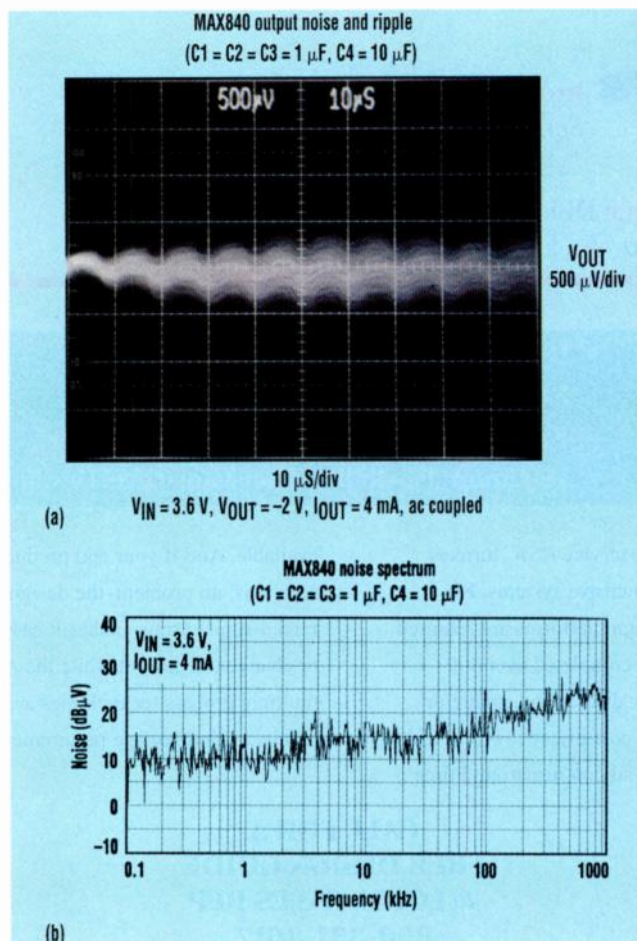
GaAs FET RF power amps are often preferred for portable communications because their efficiency is higher than that of bipolar power amps. The noise performance obtained from this design approach is particularly stunning for a switch-mode circuit (Fig. 5).

In fact, it's nearly as good as that of Figure 1. Figure 5 shows the output waveform and noise spectrum.

SYNCHRONIZED DESIGNS

The common weapons used on dc-dc noise involve some sort of suppression—typically filtering and shielding. An alternate approach that can save the cost and inconvenience of these solutions is to lock the dc-dc converter's operating (and noise generating) frequency to a clock source that confines the ripple and emitted spectrum to frequencies that don't interfere with the system.

This solution doesn't directly reduce the amplitude of ripple or radiated noise, but it can nudge the noise spectrum to less intrusive harmonics located away from, for example, the frequency of intermediate-frequency (IF) stages. Not only can this improve performance (RF sensitivity, for example), but it also can save money if the output then does not need additional filter stages, or shielding can be eliminated. A number of dc-dc converter ICs now offer a



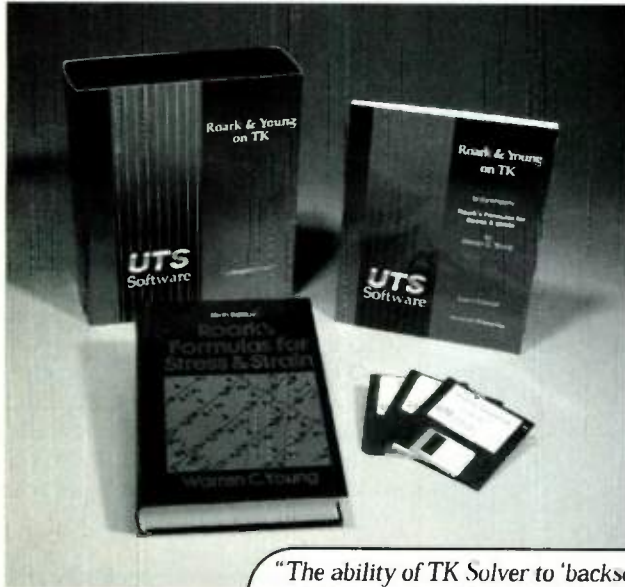
5 This peak-to-peak noise and ripple photo, along with the output noise spectrum of Figure 4's circuit, show nearly complete suppression of the 100-kHz ripple fundamental.

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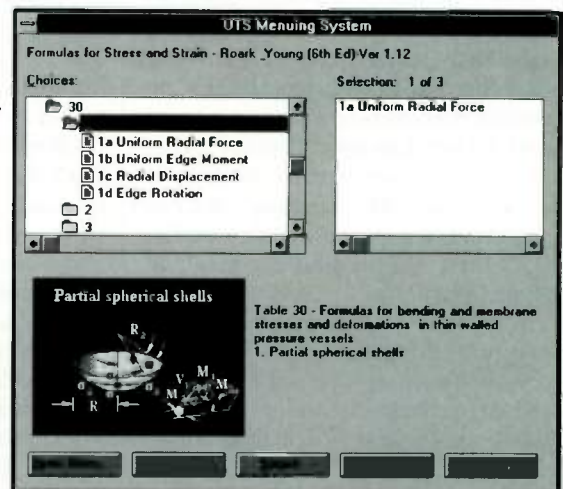
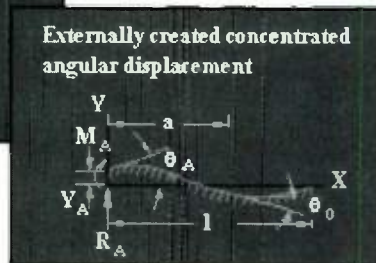
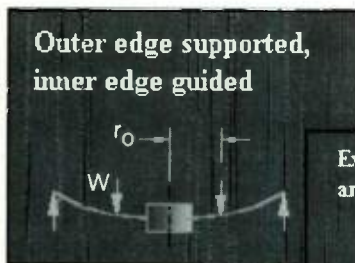
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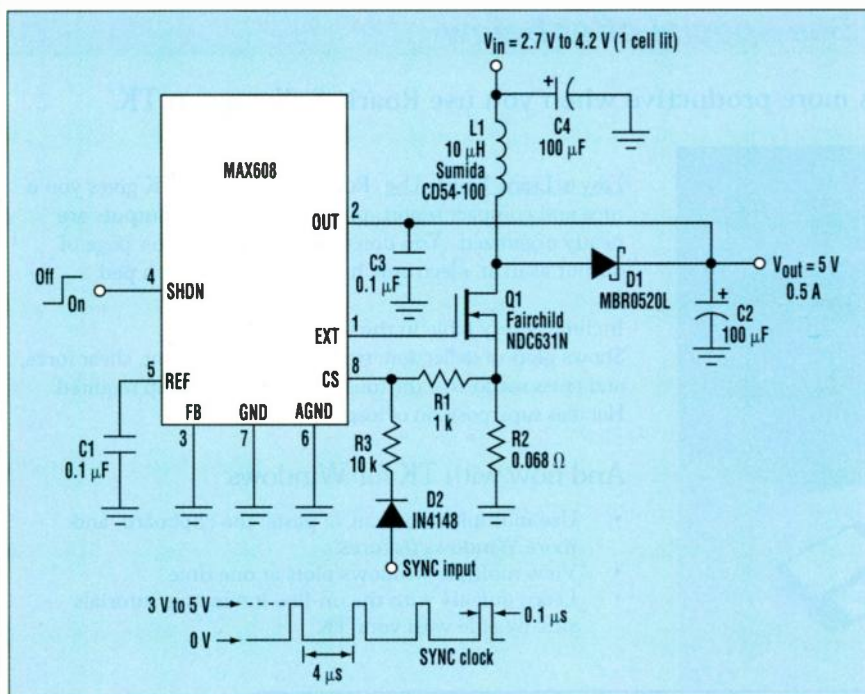


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LOW-NOISE POWER CONVERSION



6 Some variable frequency dc-dc converters can be synchronized through their current-sense inputs. An injected pulse train locks this low operating-current converter to an external clock.

SYNC input to lock the converter oscillator to an external clock source.

Very-low-power designs often employ variable frequency converters. These pulse-skipping converters are popular in handheld equipment because they can extend battery life by efficiently supplying a wide range of load current. In addition, the ICs' operating current is tenths of a microampere rather than several milliamperes. Because these converters often do not use a clock, synchronization is not considered. But a type of synchronization is, in fact, still possible for these designs (Fig. 6).

The basic control scheme of many low-power converter ICs involves a one-shot scheme whereby a switching pulse (to charge the inductor) begins when the IC senses a drop in output voltage. This pulse ends either when the inductor current reaches a current limit set by a current-sense resistor, or when it reaches a time set by an on-chip one-shot. If no drop is sensed then no pulses are initiated.

A type of synchronization can be added to such a converter by applying clock pulses to the current-sense input via D2 and R2 (Fig 6, again). Each clock pulse then ends any cycle in

progress, discharging the inductor into the output capacitor and the load. If no cycle has begun, then the clock pulse has no effect.

The net result is that each switching pulse is terminated (rather than begun) on a rising external clock edge. The switching frequency is not fixed, but switch pulses, when they occur, end in synch with the clock. In a boost dc-dc converter, the end of the switching pulse is the noisiest point in the switching cycle. It is at that point when inductor current is at its highest, and when the switching node exhibits the largest voltage swing.

Take a look at the noise spectrum for this circuit with and without the sync clock applied (Fig. 7a and 7b). In the synchronized case, spurs can be seen at the 250-kHz fundamental and at 500 kHz, 750 kHz, and 1 MHz. Without synchronization, the fundamental will move with load and line. When boosting from 3 V to 5 V at 300 mA, Figure 7b shows the fundamental landing at 57.5 kHz.

One limitation of this approach is that the period of the sync clock must be shorter than sum of the time it takes the inductor to reach current limit and the IC's minimum off time. If current

limit should terminate a switching pulse before a sync pulse occurs, then that pulse will not be synchronized. Synchronization is ensured in the Figure 7 circuit by determining that:

$$(I_{PK} \times L) / V_{MAX} + t_{MINOFF} = t_{LIM} > 1/f_{SYNC}$$

$$(1.5 \text{ A} \times 10 \text{ H}) / 4.2 \text{ V} + 2.3 \mu\text{s} = 3.57 \mu\text{s} + 2.3 \mu\text{s} = 5.87 \mu\text{s} > 1/250 \text{ kHz}$$

where I_{PK} is the peak inductor current, L is the coil inductance, V_{MAX} is the maximum input voltage, and t_{MINOFF} is a datasheet spec for the IC's minimum off time.

OTHER LOW-NOISE TRICKS

In addition to the above circuits, it may be useful to consider a few additional low-tech tricks that can help avoid or prevent dc-dc converter noise problems. Among these are:

Simple resistance-capacitance (RC) filter: When load current is low, this approach should never be ruled out because it's likely to be the lowest-cost choice, if it can be made to work. Feasibility will depend on whether a suitable filter resistance can be inserted in series with the load without suffering an excessive drop in the output voltage or degraded load regulation. For example, at a 10-mA load, a 10-Ω resistor will drop 100 mV, which may be acceptable. A 1-µF capacitor then adds a 15-kHz roll-off to the output.

Remember that often it's not necessary to filter the entire dc-dc converter output, but just the portion of the load or loads that need low noise. In this way, the current that passes through the post-filter resistance can be kept to a minimum.

One important note when using an RC post filter is to only add the filter after the circuit's feedback connection. Although placing the RC filter inside the feedback loop might at first make it appear that the load-dependent output changes caused by the series resistance will be eliminated, the added feedback delay will almost certainly destabilize most switching regulator circuits, hence creating more—not less—ripple.

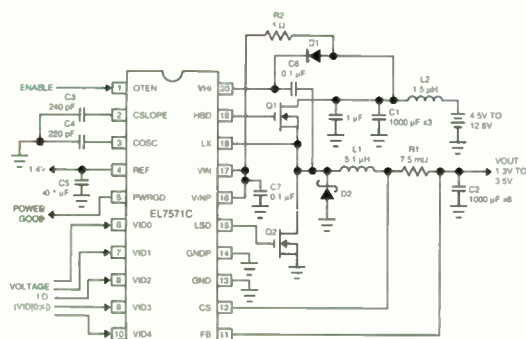
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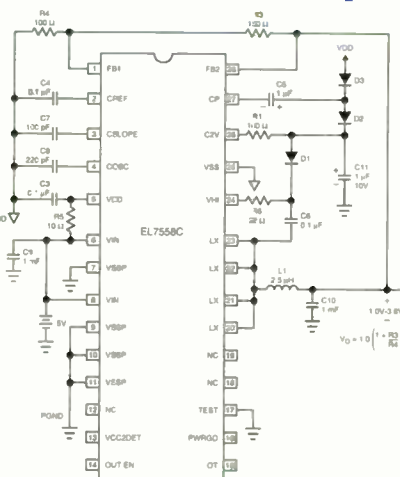
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only for a short time, such as when a synchronized receiver is turned on, it may be effective to just turn off the dc-dc converter and operate the circuitry from the storage capacitor during the low-noise event. The wisdom of this method will depend, of course, on the product of load current and duration.

For example, a 330- μ F capacitor that's loaded with 100 mA for 1 ms droops 303 mV. The disadvantage is that the load circuitry must be able to operate with a larger variation in output voltage than is typically experienced with a regulated supply. The advantage, however, is complete elimination of switching events during sensitive operations.

PC layout: This is the most common source of dc-dc noise problems. Although the root source of the noise is inductor fields, high dI/dt in circuit components and traces, and high dV/dt at circuit nodes can be severely aggravated by poor layout. Many poor layouts are generated by auto-routed layout software intended for logic design. Particular issues to watch are:

- Keep the switching nodes physically small. In conventional dc-dc converters, the nodes are where the coil, switch, and diode meet. These nodes are antennas. The larger they are, the more noise is radiated to surrounding circuits. The traces should be wide to carry high current, but also should be made to travel the minimum possible length.

- In any power-supply design with resistor-set feedback, locate feedback resistors right next to the IC feedback pin, and keep the trace area at the feedback pin minimized. The feedback pin is a high-impedance node, and therefore is susceptible to noise radiated from other parts of the circuit. Because the output and ground are low-impedance points, it's better to run long traces from the voltage output and ground to resistors located close

to the feedback pin. It's much worse layout practice to locate the resistors near the output and ground, and run long traces to the feedback pin.

- Identify the traces through which high currents are flowing and size them as wide and short as possible. In particular, pay attention to vias through the pc board, because these are poor conductors of high current, especially in high-speed switching circuits. It's best not to route high-current paths between board layers, but if this is unavoidable, use multiple vias in parallel. A rough guideline is at least one via per ampere of peak current.

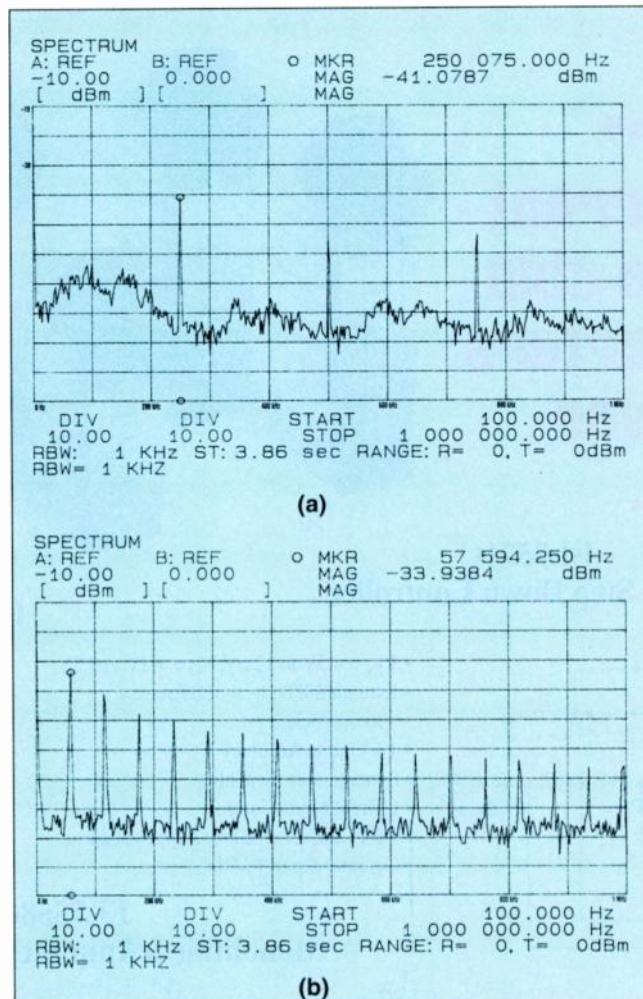
- Ensure that low noise grounds, such as those for feedback resistors, reference bypass capacitors, and the

IC analog ground pin(s) are not polluted by high currents from power ground traces. Although there isn't one universal best layout, the greatest likelihood of success is achieved by laying out separate ground planes for analog and power ground. The two planes then connect together with a single trace at one point where the IC's analog and power ground pins also are connected together. High current should not flow in the trace joining the low-noise and power grounds.

- Avoid cutting up the ground plane with too many long jumper traces. This is a common problem because the ground plane is usually layer two, and layer-one signal traces that must be jumpered are frequently sent through layer two. If these slices in the ground plane are not properly located, the quality of the ground can be degraded because return current then must take more serpentine paths. The solution is to move long jumpers to a layer other than ground.

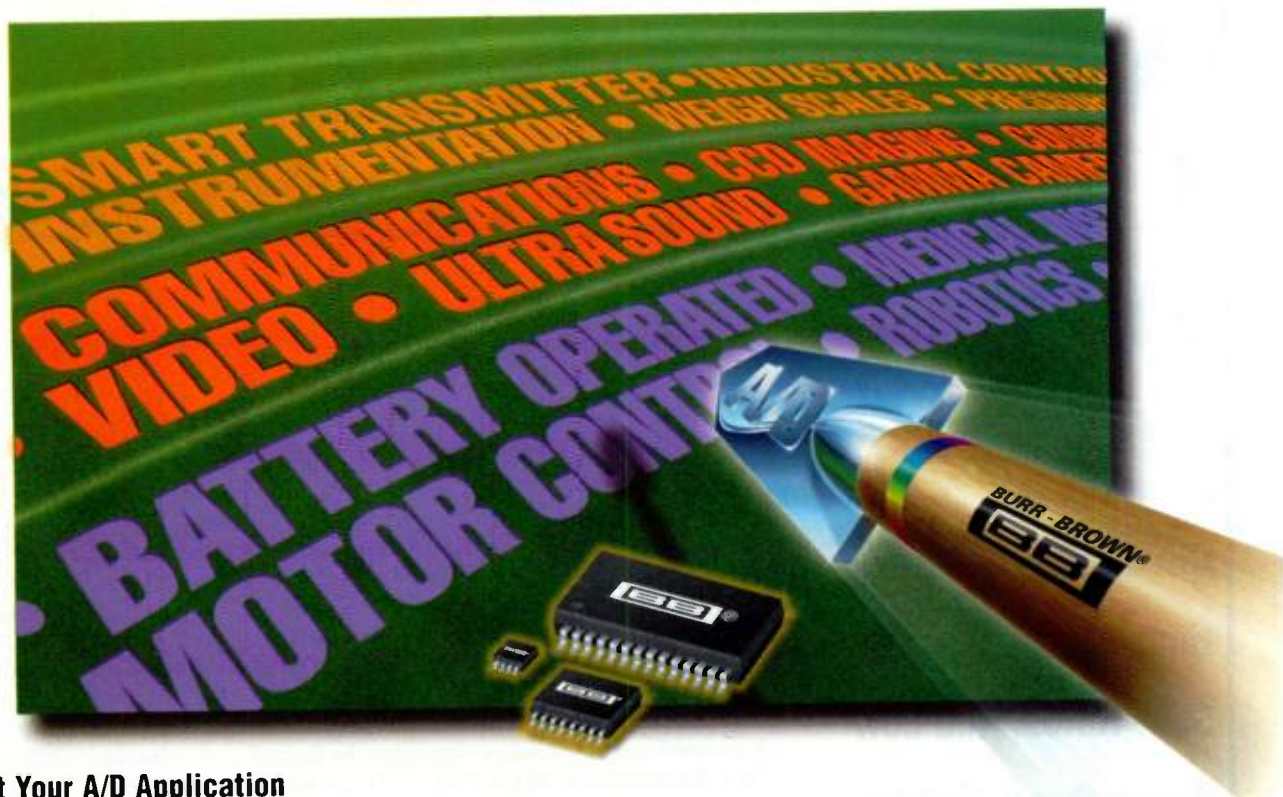
As has been shown, there are many ways to combat noise in dc-dc converter designs and many voltage conversion techniques need not be incompatible with sensitive circuitry such as low-noise preamps, RF receivers, and high-gain amplifiers. By understanding the real needs of the system, switch-mode voltage conversion often can be employed without sacrificing noise performance.

LEONARD SHERMAN is an applications engineering director for Maxim Integrated Products. He has a BSEE from the Massachusetts Institute of Technology, Cambridge. Sherman can be reached at Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600; e-mail: lensherman@earthlink.net.



7 Noise spectrum plots for the circuit in Figure 6 show the benefit of synchronization. With a 250-kHz clock applied, output noise is confined to 250 kHz and its harmonics (a). With no clock, noise occurs at less-controlled frequencies (b).

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ADS1212	±0.0015	±312mV to ±5V	22	16	1.4	\$7.25	11360	81
ADS1214	±0.0015	±20mV to ±320mV	22	16	1.4	\$7.25	11368	82

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ADS803	12	5	116	69	±0.3	82	+5	\$9.55	11398	84
ADS824*	10	75	315	59	±0.5	70	+5	\$8.50	11403	85
ADS930/931	8	30	66/63	46/48	±0.4	51/49	+3/+5	\$3.37/\$3.27	11349	86

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ADS7817	12	±1	12	200	2.3	71	-83	\$5.18	11369	88
ADS7822	12	±0.75	12	75	0.54	71	-82	\$4.64	11358	89
ADS7825	16	±2.0	16	40	50	86	-90	\$28.46	11304	90



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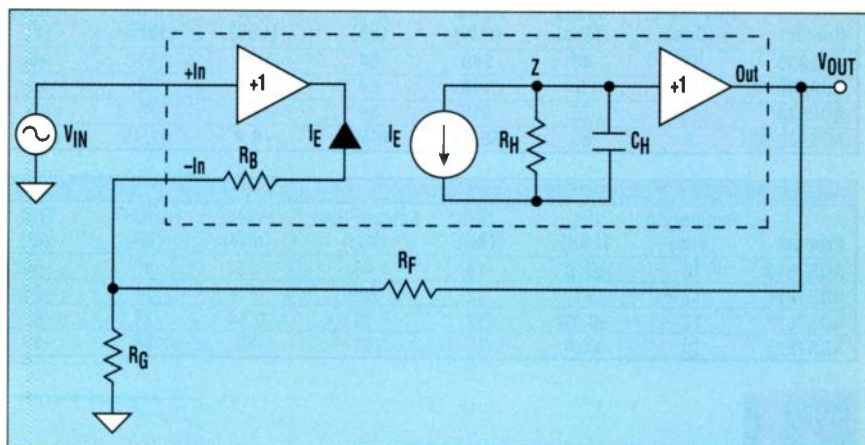
Jeff Lies and Ron Mancini
Harris Semiconductor

Some designers (especially digital designers doing analog design) are intimidated by current-feedback amplifiers (CFAs). As a result, they don't take advantage of the CFA's superior frequency performance. CFAs have become pervasive because they have an architectural advantage that delivers high bandwidth and slew rate at low supply currents. Indeed, a designer without CFAs in his arsenal is inadequately armed for today's high-speed design challenges.

The good news is that most of your voltage-feedback-amplifier (VFA) knowledge is applicable to CFA design because the ideal equations for both amplifiers are identical. The VFA attempts to drive the input-error voltage to zero, while the CFA attempts to drive the input-error current to zero, so understanding the VFA feedback mechanism simplifies the task of understanding CFA operation. Two characteristics of the CFA will take some getting used to: The closed-loop bandwidth is relatively independent of the closed-loop gain, and the amplifier's stability is dependent on the feedback resistor value. Both of these differences offer significant advantages for the CFA with very few drawbacks.

SIMPLIFIED CFA MODEL

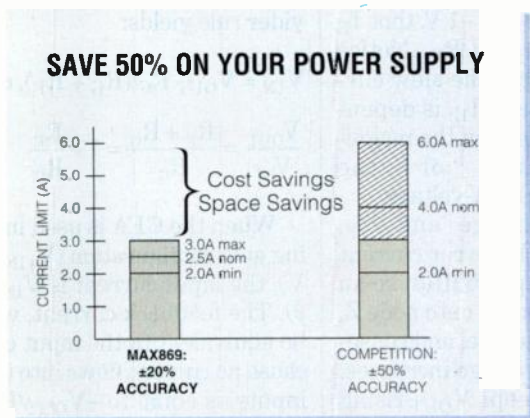
The simplified CFA model is shown in Figure 1. The external resistors, R_G and R_F , are the gain and feedback elements which determine the gain and bandwidth performance. The object is to determine the proper value for these resistors. When the circuit is configured for noninverting gain, the input for the circuit is $+In$ (Fig. 1, *again*). This terminal connects to a unity-gain buffer input, so it has the characteristics of high-input impedance and low-bias current. Con-



1 This simplified model demonstrates how the current-feedback amplifier (CFA) operates, and how it differs from the voltage-feedback amplifier (VFA). The controlled current source at node Z represents the transimpedance element.

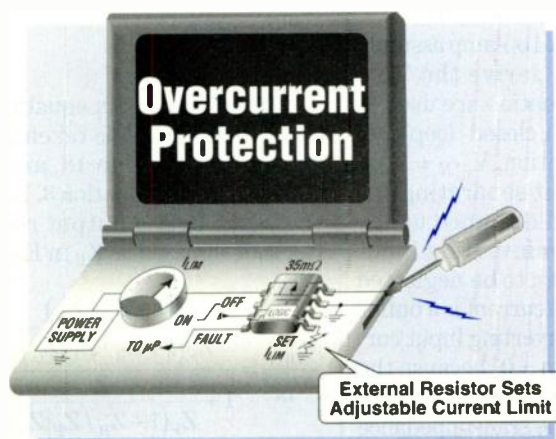
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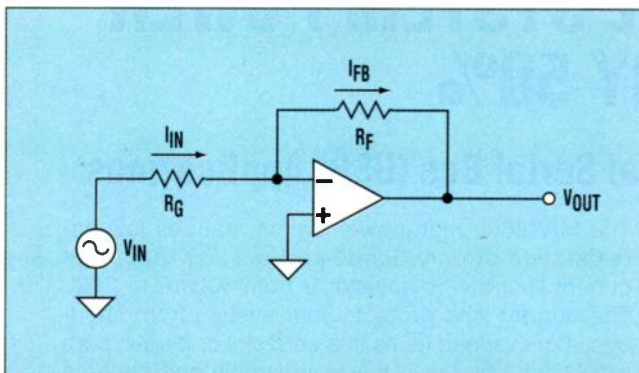
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CURRENT-FEEDBACK AMPLIFIERS



2 The inverting gain configuration for a current-feedback amplifier has input and feedback resistors just like a VFA. The circuit's gain equation is $(V_{OUT}/V_{IN}) = -(R_F/R_G)$.

versely, the $-I_N$ input connects to the output of the same buffer. R_B models the output resistance of the buffer, but it is usually a small value which can be ignored. The $-I_N$ input has the characteristics of a buffer output: very-low impedance and high current-sinking/sourcing capability. The high-current capability of the buffer output enables large transient currents to flow through the external circuits, and as will be shown later, this enables higher slew rates for the CFA.

The unity-gain input buffer forces $-I_N$ to follow $+I_N$ unconditionally. During quiescent operation only a small current flows through $-I_N$. This current is the error current, I_E , which is analogous to the error voltage of a VFA. The current flowing through $-I_N$ is always mirrored (represented by the current source I_E) onto a high-impedance node (Z) where it is converted to a voltage via the transimpedance gain of the CFA. Transimpedance gain serves the same function in a CFA that open-loop-voltage gain serves in a VFA; i.e., it is the driving force which closes the feedback loop. If the amplifier has a large transimpedance gain (Z) it will have a low error current because $I_E = V_{OUT}/Z$. The controlled current source in the simplified model represents the transimpedance element, and when the current flows through the terminating impedance, $R_H \parallel C_H$, a voltage is developed at the input node of the output buffer. The output buffer is another unity-gain buffer, and it provides the current capability for driving low impedance loads.

For example, consider a voltage fol-

lower ($R_G = \infty$) where at $t = 0$, $V_{+IN} = V_{OUT} = 0$. If at $t = 0+$, a unit step voltage is applied to the input, then at $t = 0+$, $V_{+IN} = V_{-IN} = 1$ V, and $V_{OUT} - V_{IN} = -1$ V, thus $I_E = -1 \text{ V}/R_F$. Notice that the slew current, I_E , is dependent on the magnitude of the output-voltage change and R_F .

This error current is sourced by the input buffer, so an equal current is mirrored onto node Z , causing the voltage to rise, and consequently the output voltage increases. The feedback loop keeps V_{OUT} rising until the error current is driven to the minimum value. At this point $V_{+IN} = V_{OUT}$ within the error tolerance. The same four ideal op-amp assumptions employed to derive the VFA closed-loop-gain equation are used to derive the ideal CFA closed-loop-gain equations. By definition, $V_{-IN} = V_{+IN}$ because the element separating the two inputs is a well-designed unity-gain buffer. The noninverting input current is low enough to be neglected ($+I_N = 0$) because this current is a buffer input current. The inverting input current equals zero ($-I_N = 0$) because the feedback loop drives the error current to zero. As long as the transimpedance gain is large the $-I_N$ current is negligible. The two input currents are totally uncorrelated, therefore the common VFA technique of canceling input-current errors by balancing the impedance seen at the positive and negative inputs is not recommended for CFAs. The transimpedance gain is extremely high, which enables the feedback loop to function properly, just like high open-loop gain does in a VFA.

The feedback network is constructed in the same way for both the CFA and VFA; a feedback resistor (R_F) is connected from the op-amp output to the inverting input, and a gain-setting resistor (R_G) is connected from the inverting input to ground in both cases. Because the feedback network is the same for the CFA and

VFA, and because the ideal op-amp assumptions are valid for both types, it is obvious that the VFA ideal closed-loop gain equation must hold for the CFA.

The noninverting gain formula, (Equation 1) is based on these assumptions; the voltage across R_G is V_{IN} because $-I_N$ tracks $+I_N$, so the voltage divider rule yields:

$$V_{IN} = V_{OUT} R_G / (R_G + R_F), \text{ or:}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F + R_G}{R_G} = 1 + \frac{R_F}{R_G} \quad (1)$$

When the CFA is used in an inverting gain configuration ($V_{+IN} = V_{-IN} = 0$ V), the input current is V_{IN}/R_G (Fig. 2). The feedback current, which must be equivalent to the input current because no current flows into the op-amp inputs, is equal to $-V_{OUT}/R_F$. Equating the currents yields:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G} \quad (2)$$

The nonideal gain equation for the noninverting CFA is taken from Reference 1, Equation 18, and it is repeated here as Equation 3. Notice that the input-buffer output resistance, R_B , is designated as Z_B in Equation 3.

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z(1 + Z_F/Z_G)}{Z_F(1 + Z_B/Z_F \parallel Z_G)} \cdot \frac{1}{1 + \frac{Z}{Z_F(1 + Z_B/Z_F \parallel Z_G)}} \quad (3)$$

If the input-buffer output resistance is zero, which is the goal of every CFA IC designer, Equation 3 reduces to:

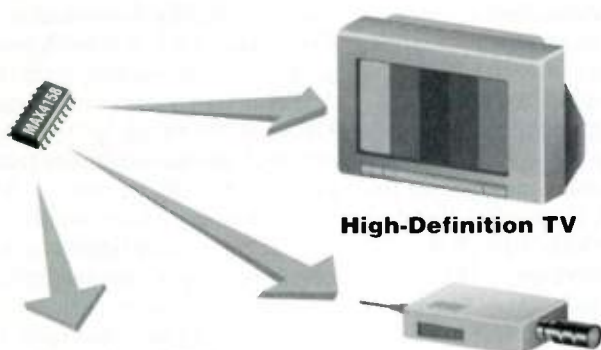
$$\frac{V_{OUT}}{V_{IN}} = \frac{Z/Z_F(1 + Z_F/Z_G)}{1 + Z/Z_F} \quad (4)$$

The transimpedance gain (Z) contains two or more poles, and these poles make the transfer function frequency dependent. If Z were independent of frequency, and Z_F and Z_G were purely resistive, the CFA would be independent of frequency.

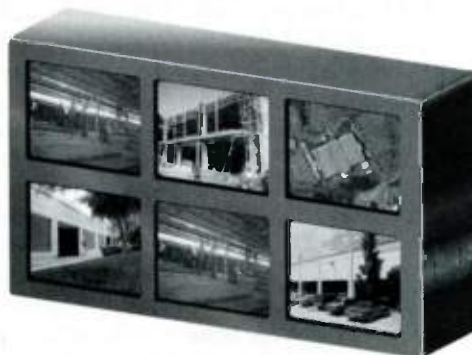
Equation 4 is in the form of the classic closed-loop-feedback equation $V_{OUT}/V_{IN} = A/(1 + A\beta)$. The sole determining factor for stability in a feedback system is the loop gain, often mathe-

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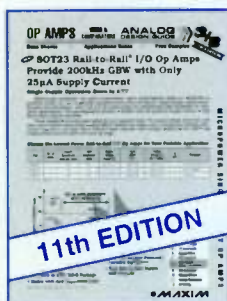
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CURRENT-FEEDBACK AMPLIFIERS

matically expressed as $A\beta$, and the loop gain in Equation 4 is the quantity Z/Z_F .¹ A fundamental conclusion is that the CFA's stability is completely dependent on the transimpedance and the feedback impedance. This situation is very different from the VFA where stability is dependent on closed loop gain ($A\beta = a/A_{CL}$).¹ Another important note about the CFA's loop gain is that because Z_F is in the denominator, Z_F cannot be zero ohms in a linear circuit. Therefore, a R_F is required even for unity-gain applications, and capacitive feedback is undesirable because it will cause Z_F to go to zero at some frequency.

A Bode plot is a log-magnitude plot of the gain and phase, and it evaluates stability very effectively.² This plot is a transimpedance gain plot for a CFA, where it would be a voltage gain plot for a VFA. The CFA Bode plot for the loop gain of Equation 4 (with the transimpedance plotted as a two-pole transfer function) is shown in Figure 3. Notice that the numerator and denominator of the loop gain are plotted separately and added graphically to obtain the final result. The criteria for stability is that the loop gain be less than one before -180° of phase shift is accumulated; i.e., $|A\beta| < 1$ at $\phi < -180$.

When the composite curve crosses 0 dB ($A\beta = 1$), the phase shift is -120° ,

so this particular CFA would have 60° of phase margin, and it would be very stable with that value of Z_F . On the Bode plot, $|Z_F| = R_F$ subtracts from the $|Z|$ curve. This moves the composite curve down from the Z curve, and moves the 0-dB gain-crossing point to the left, into an area of less phase shift.

The conclusion can be made that increasing R_F stabilizes the CFA by reducing the loop gain without impacting the open-loop phase shift. In other words, the phase margin has increased (Fig. 4). Note, also, that the amplifier's bandwidth (BW_1 , BW_2) decreases as R_F increases. These are critical conclusions because they indicate that the value of R_F can be adjusted to trade stability for bandwidth. This flexibility is the basis for the conclusion that the CFA bandwidth is inversely proportional to R_F .

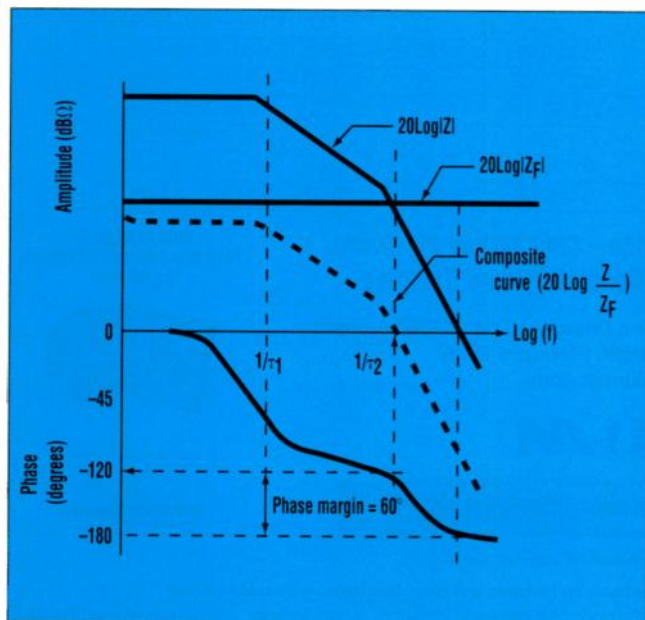
In actual practice, the designer will never decrease R_F so much that the CFA approaches instability, because gain peaking and overshoot increase dramatically long before the circuit becomes unstable. When increasing the closed-loop gain of a CFA circuit, decrease R_G rather than increase R_F .

Inspecting Equation 4 reveals that the closed-loop gain does not affect the stability or bandwidth of the CFA because it does not impact the loop gain or

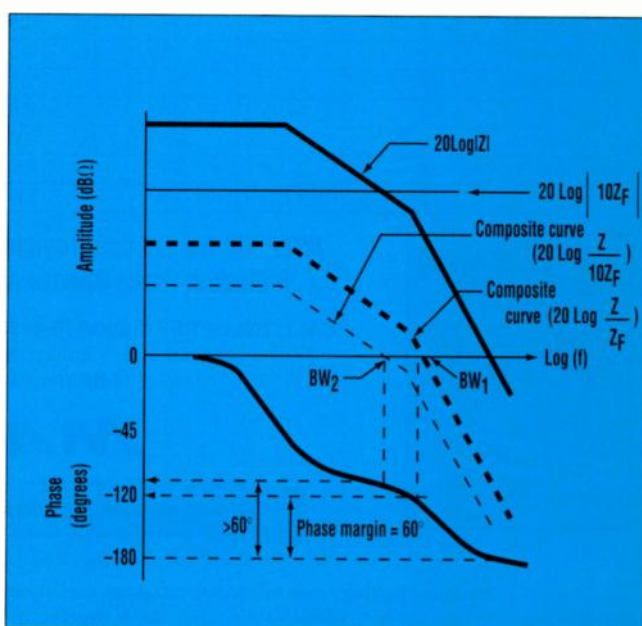
the pole-zero locations. Therefore, the CFA bandwidth is independent of closed-loop gain, except for the minor effect of the neglected Z_B term (demonstrated in Equation 3). When Z_B is taken into consideration, the CFA bandwidth becomes slightly dependent on closed-loop gain, but it is still much more independent of closed-loop gain than the VFA is. This phenomenon explains why CFAs make much better high-frequency, high-gain amplifiers than VFAs do. Z_B is usually an emitter-follower-type output impedance, which exhibits a zero in the transfer function at high frequencies. This description explains why CFAs tend to become peaky at high frequencies, especially when there is significant capacitance on the inverting input.

Slew rate is a measure of the amplifier's ability to transition from one output voltage to another in response to an input-voltage change. Fast slew rates are required for good pulse amplifiers because pulses contain fast rise and fall times.

The error current is multiplied by the transimpedance gain to form the unbuffered output voltage, so the sooner the error current is driven to zero, the faster the amplifier gets to its final output voltage. An earlier derivation established the formula for the unity-gain CFA error current as $I_E =$



3 This Bode plot of a CFA is useful for stability analysis. With a VFA, the amplitude scale would represent voltage gain. But in the case of the CFA, the amplitude scale shows the amplifier's transimpedance gain.



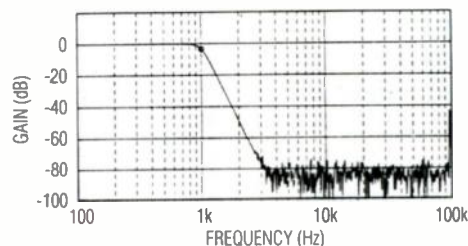
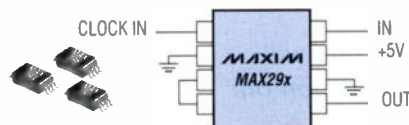
4 By adjusting the value of R_F , the designer can make a trade-off between stability and bandwidth. The bandwidth is inversely proportional to R_F .

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CURRENT-FEEDBACK AMPLIFIERS

$(V_{OUT} - V_{IN})/R_F$. If R_F is decreased or ΔV_{IN} is increased, more current is available to slew the internal high-impedance node, and faster slew rates result. Of course, the VFA has an internal current source which limits the maximum slew rate regardless of the voltage step size. If the input step size is doubled in a CFA, the current available for slewing is doubled, hence the rise/fall time is virtually independent of step size. The usual method of increasing slew rate in a VFA is for the op-amp manufacturer to increase bias current which also increases supply current.

Because the input buffer must first slew to follow the input signal, the input buffer's slew rate is a critical part of the overall slew rate. In high-gain configurations the input buffer does not go through a large voltage change compared to the output, so its slew rate does not contribute much error. In low-gain configurations the input buffer can significantly degrade the slew rate. For example, in unity-gain applications the CFA's input buffer must slew the inverting input the same amount as the output, often limiting the unity-gain CFA's slew rate. In inverting gain configurations, $-In$ is a virtual ground. Consequently, the input buffer doesn't have to slew much. So, the inverting configuration has the fastest slew rate.

Usually, the CFA can replace the VFA in most high-frequency applications—with better performance and lower cost. However, there are a few salient points to be aware of during the replacement. Most cases will require either minor or no pc-board changes. But remember that the CFA must *always* have a feedback resistor. It can't be substituted directly for a VFA in unity-gain applications where the output is shorted to the inverting input ($R_F = 0$).

The key to CFA stability is the feedback resistor. While higher R_F values are fine for VFAs, most CFAs are optimized for $R_F < 1\text{ k}\Omega$. Higher-than-optimum values degrade CFA performance dramatically. However, a value of R_F that yields stable operation can always be found. It is best to start with the manufacturer's recommended value, but graphical techniques can be used to select new R_F values if wider bandwidth or a higher closed-loop gain (reduce R_G rather than increase R_F) is desired.³

Remember, reducing R_F increases bandwidth while increasing ringing and overshoot. Don't drop the value of R_F too much or oscillation will result. Another factor that destabilizes CFAs when replacing VFAs is excessive capacitance on the inverting input or the output. A common source of ringing or oscillation in any high-frequency amplifier is a long pc-board trace length attached to the inverting input lead. This situation is exacerbated with a CFA.

Circuit configurations using feedback capacitors or diodes do not lend themselves to CFAs because these feedback components will approach zero impedance at some operating point and oscillation will result. Diodes in the feedback loop can often be replaced by input or output clamp diodes. Some CFAs, such as the HFA1135, provide the clamping function internally thereby eliminating the external diodes. Also, feedback capacitors can be neutralized by putting a resistor equal to the optimum value of R_F in series with them. Moreover, the classic inverting integrator cannot be implemented in a CFA, so the noninverting integrator often is used in its place.

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1. Harris Semiconductor, *Application Note AN9420*, Authors: Ronald Mancini and Jeffery Lies, 1995.
2. Bode, H. W., *Network Analysis And Feedback Amplifier Design*, D. VanNostrand Inc., 1945.
3. Mancini, Ronald, "Converting From Voltage-Feedback To Current-Feedback Amplifiers," *Electronic Design Special Analog Issue*, June 26, 1995, p. 37-46

What's All This Thermostat Stuff, Anyhow? (Part II)

I got several responses after I brought out my June column on thermostats (ELECTRONIC DESIGN, June 23 Analog Special Supplement, p. 61). A couple guys suggested that if you inquire in the right discount places, you can buy a replacement thermostat for your oven for MUCH less than \$288. That may be true in a big city, but it might be hard to find in a small-town environment, where there is really not a sufficient demand for inexpensive repair parts to keep a discounter in business.

But I did get one *intriguing* letter from a guy who worked for a thermistor company. He asked me if I could show him a good way to use a thermistor as a temp sensor for an oven. I thought about it. Hey, thermistors can work OK as linear temp sensors over a

narrow temperature range such as a 40°C span.

But your kitchen oven has to work from at least 35° to almost 300°C (+572°F), and if it is a self-cleaning oven, up to at least 400°C. Many thermistors are rated up to just 100 or 200°C, but there are some that are rated as high as 600°C. So, in *theory*, a thermistor could feed an oven controller.

BUT, thermistors are inherently logarithmic devices. A thermistor's impedance changes at a steep, rapid rate, such as -3.9%/°C. This means that at any one operating point, its gain may be *fat*—much larger than a platinum RTD sen-

sor's slope of +0.38%/°C. But when you change the temperature a lot, its change of R may be much too big or much too small in terms of (Ω/°C). So, if you have to cover a wide range, thermistors are really hard to apply. I wrote back to the guy and told him, "If you think thermistors are good for making a thermostat for your ordinary kitchen oven—and if you are so smart, *you tell me* how to do it. Because I don't think it's easy."

I pointed out that while some thermistors are *cheap*, a thermistor might need a very complicated circuit to get it to read out. We CERTAINLY don't want a nonlinear sensor, because controlling the temperature of an oven is hard enough without having the sensor's gain changing all over the place. More on this later.

I told this guy, "I don't care how cheap a thermistor is—it may not be cost-effective if the circuit is messy. Consider a thermocouple! They are very cheap. What's the cost of a pre-amp for a thermocouple?"

I scribbled out a circuit like the one in Figure 1. I said, "Even this circuit is a lot simpler than the thermistor one."

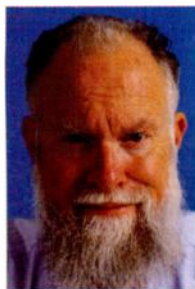
As I looked it, I realized: that really IS cheap. You need a few 1% resistors, but that's pennies. You need a decent op amp—but those are pretty inexpensive, too. The op amp needs to have a fairly decent tempco—but that's not hard: The LMC662 family is cheap, but its tempco of V_{OS} is typically 1 $\mu V/^\circ C$. Hey, compared to a thermocouple that puts out 40 $\mu V/^\circ C$,

that's not bad. Eight years back, I put into my old book (on page 24) an elegant thermocouple preamp with inherent cold-junction compensation, that Mineo Yamatake designed. It is MUCH better than 1/40° of error per degree of ambient. But for your oven, you don't need that.

So the circuit in Figure 1 really is NOT a bad deal. Its cold-junction compensation is simple yet adequate, so long as you keep the 1N914 at about the same temperature as the "cold junctions." It is easy to calibrate; nothing complicated—just trim the Offset Adjust pot to get V_X to match the actual oven's temperature, at 10 mV/°F, around room temp. If you plan to put in all necessary capacitors to keep the RFI out, it is still cheap and easy. So, this is *not* a bad circuit.

I should mention the time recently when one of our customers called and told me, "Bob, you have to get your op-amp designers to redesign the LMC662." I asked why. They said that in one of their new applications, they were using an LMC662 in a mouse application. The design had been carefully checked out and was working perfectly, until they started to test for the new European Directives for RFI rejection. This is the family of tests where you put your equipment into a chamber where it is subjected to an RF field of 10 V/meter, and swept over a range of frequencies from 1 to 1000 MHz in various orientations. When they did that, the mouse malfunctioned badly at 270 MHz, and they blamed it on the op amp.

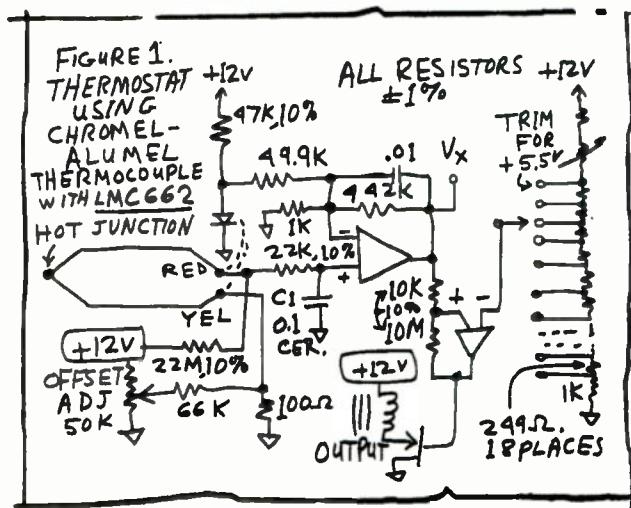
I asked the customer, "Do you have



BOB PEASE

OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

devices. A thermistor's impedance changes at a steep, rapid rate, such as -3.9%/°C. This means that at any one operating point, its gain may be *fat*—much larger than a platinum RTD sen-



any power supply bypass caps out by the op-amp circuit?" (No.) I asked, "Do you have any bypass capacitors on the signals or the inputs of the op-amp?" (No.) I asked, "Do you have any grounded shielding sprayed onto the inside of the mouse shell?" (No.) And I asked, "So, you really think we ought to redesign our op amps at the last minute to cover up the fact that you made a lousy layout and a poor design that only showed up in last-minute testing?" (Yes.)

I had to explain that what they wished for was not likely to happen. ESPECIALLY NOT on the time schedule they wished for. As I often say, "People in hell want ice water." (OR, "People in San Francisco want ice water.")

But National DOES have a set of applications notes listing the Ten Commandments of how to keep out of trouble with RF and EMI blasting down the throats of the poor little op amps, and other linear ICs, and other circuits. The major point we make is, "Test early and often." Suppose you test your system, and there is a circuit that's unhappy when blasted with RFI. The earlier you test, the better the chance of adding filter caps or bypass caps or swapping IC types until you have a circuit that is NOT going to go berserk when subjected to RFI. See the note at the end to request these notes.

Anyhow, by looking at the details of the circuit of Figure 1, I did put in a little 0.1- μ F ceramic disc (C1) to keep most of the RFI out of the input of A1. That's about all it needs. I put in 22 M Ω to indicate if the thermocouple becomes disconnected. This circuit is not much cheaper than the one with the Platinum sensor back in June. But since thermocouple wire is pretty cheap, barely a couple of dollars for a 3-foot length, this is a good candidate for a do-it-yourself project. (Maybe not better than using a \$20 platinum RTD sensor, but

cheaper).

I sent all this STUFF off to the guy at the thermistor company. I haven't heard back from him yet.

But then the other day, I got a letter from a guy requesting how to convert a sensor's resistance into a logarithm over a wide range. I thought about that. That was easy. I rewrote the other circuit I made for the thermistor guy (Fig. 2).

If the logarithmic characteristic of the thermistor is roughly constant with temperature, then this circuit's output is roughly linear, because it is a log function. But look at the problem with the wide range!! To go from 0°C to 100°C, most thermistors cover a resistance range of 30 or 40 to 1. To cover the range from 35°C to 300°C as mentioned above, a thermistor has a ratio of about

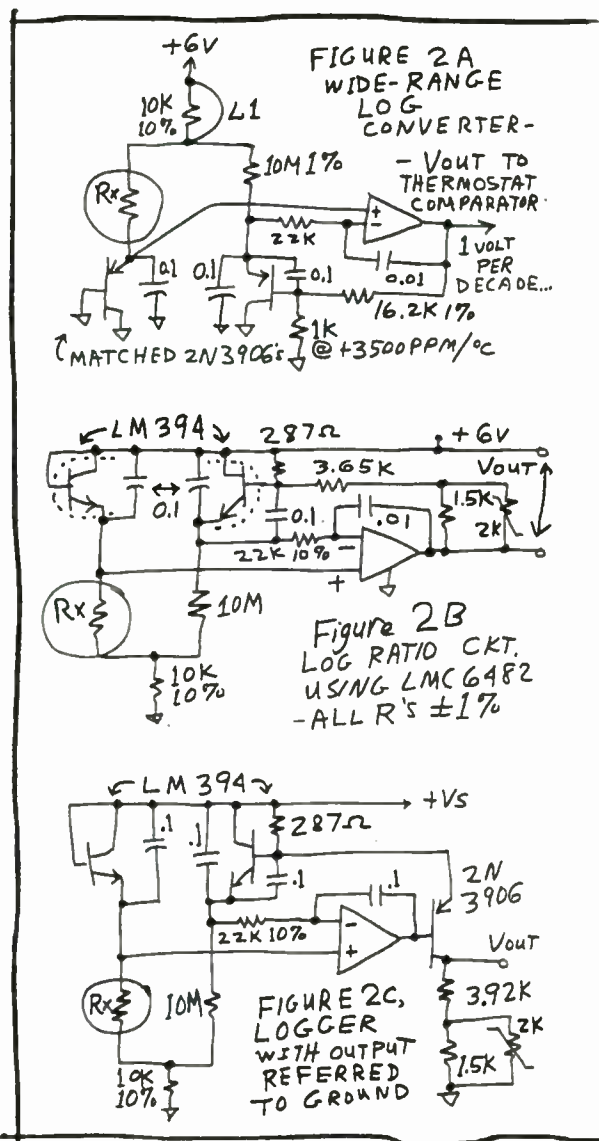
10,000:1. How can we properly accommodate a thermistor with a range from 10 M Ω to 1 k Ω ? Hell of a good question!

If you just set up a fixed voltage across two resistors, and one resistor gets very low, the current would get really big. Now what? That would tend to cause a lot of self-heating of the thermistor, which would cause gross errors. If we just run the circuit of Figure 2A with a fixed bias, the current through R_X can get quite big. For example, if it runs as low as 1 k Ω , the self-heating can be as big as 30 mW. But if we open up link L1, the ratio of currents through R_1 vs. R_X can cover a fairly wide range. However, the current never really gets out of hand. The self-heating would rise to only 0.6 mW.

I put in three versions of this circuit. The first one, Figure 2A, uses PNP transistors such as 2N3906s, which you have to match to better than 1 mV. (This assumes you can maintain temperature errors better than 1/4°C, when you bin the transistors in terms of their deviation compared to the V_{BE} of a STANDARD transistor. Lots of moving air!) (see "What's All This Box Stuff, Anyhow?" ELECTRONIC DESIGN, Aug. 22, 1991). The op amp has its common-mode near ground, so you can use an inexpensive LMC6082.

I'll assume that the operating temperature for this CIRCUIT will be 20 to 50°C, a normal "room" temperature. At 25°C, the transistors' log characteristic is 60 mV/decade. But over that temp range, the g_m of the transistors does change several percent. So, a simple 1-k Ω wire-wound resistor with a temperature characteristic of +3500 ppm/°C is needed to compensate for the changing g_m . These resistors are available from KRL ("Type Q"), or from Ultronix, Pacific Resistor Co., and from several other manufacturers of precision wire-wound resistors.

The second circuit, shown in Figure 2B, has turned the circuit upside down to take ad-



BOB PEASE

vantage of good matched NPNs such as LM394 (better than 150 μV of V_{BE} matching). These NPNs will have better accuracy and the best log conformity. But it also has the disadvantage that the output is referred to the + rail. If you didn't want that, that's a disadvantage. This circuit uses a thermistor-resistor network to compensate for the way the g_m changes versus temperature—but only over a narrow ambient temp range, about +20°C to 50°C.

Circuit 2C uses the op amp with a PNP transistor to force a signal current down into a resistor network connected to ground. Now this output voltage is referred to ground. This does not have a very low Z_{OUT} , but it's low enough. The resistor network (287 Ω , 3.92 k Ω , 1.5 k Ω , and a 2-k Ω thermistor) is designed to accommodate 60-mV VPTAT (Voltage Proportional To Absolute Temperature) with a constant 1 V/decade output. This works well only over a narrow temperature range, such as 20°C to 50°C, but often that's all that

would be needed.

In all of these cases, you need an op-amp with low I_{BIAS} , low offset voltage, and low tempco. An LM324 or LM358 won't cut it. Even the LM324A can have as much as 100 nA of I_{BIAS} (which would be MUCH too big) and 10 $\mu\text{V}/^\circ\text{C}$, which would cause considerable error. The newer LMC6482IN has 0.35 mV of offset and typically 1 $\mu\text{V}/^\circ\text{C}$. Also, its I_B is much less than 1 pA. And its common-mode range extends all the way to the + rail. So, this is a good choice. Even if it does cost \$1.74 for the low-offset version, it's worth it.

I have not yet built up this circuit, but I do plan to get it running to see how the thermistor plays over a wide range. Right now, it's just a paper design. But it will have to be optimized to go with the particular thermistor that's rated to work up to 400°C. Who makes those thermistors? I forget. But I'll find 'em. Does this thermistor put out a constant $\%/^\circ\text{C}$ slope? No, but it's a good ballpark. A sensitivity of about 1 V/decade (± 3 dB) is much better than working over a range of

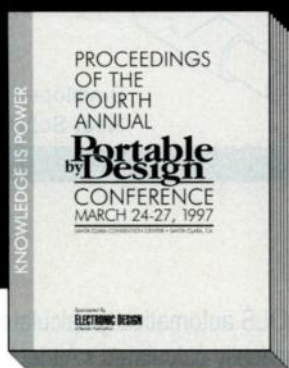
10,000 to 1 in gain slope.

- If you want to get a copy of the schematic for Mineo's thermocouple preamp, circle 550 on the Reader Response Card.
- If you want a copy of the Ten Commandments of RFI/EMI stuff, circle 551.
- If you want a list of the manufacturers that make temperature-compensating wire-wound resistors, such as +3500 ppm/ $^\circ\text{C}$, circle 552.
- If you are really tired of the thermostat topic, and never want to see it again, circle 553. (I may do that myself.)

All for now. / Comments invited!
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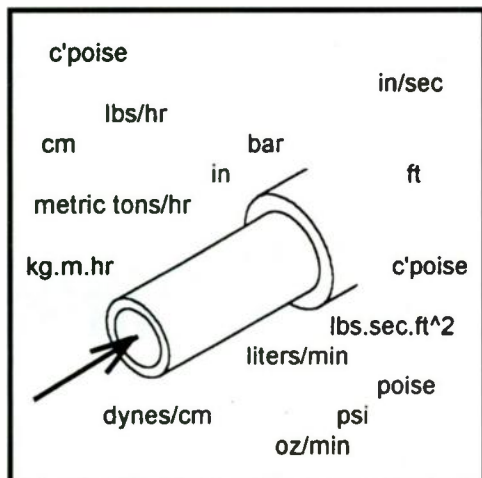
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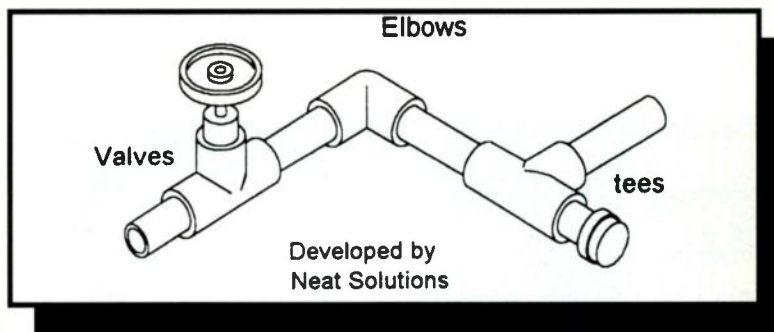
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Practical Circuits For Quiet Audio Transmissions

This Analog Special 'Tools and Tips' column is in response to all those readers who voted for more audio-oriented topics. While audio-oriented in terms of application examples, the concepts discussed also can be useful wherever high-quality analog signals require transmission.

In today's professional audio world, signals by and large get transmitted in a balanced, or differential mode. This fact is simply due to the much greater noise immunity of this method, vis-à-vis the more simple single-ended method. By its nature, the latter technique is highly susceptible to noise.

Yet, even within the professional audio world, there is no real unanimity on signal driver and receiver circuits for use within balanced circuits—they take on many different forms and have differing performance.

This column takes a brief look at some problems which impact overall circuit performance in terms of common-mode (CM) noise susceptibility, and illustrates how careful hardware choices can lower system cost and size, plus maintain excellent performance.

Source and Load Interactions: Some recent attention has focused on the general problem of noise susceptibility in audio system interfacing.^{1,2} The discussions below are concerned with how a balanced audio system driver and receiver can interact and produce undesired side effects in the form of noise susceptibility. Also, some suggestions for practical solutions are offered.

In most simple form, a balanced audio transmission system consists of a differential output driver, an interconnecting cable, and a differential input receiver. The driver produces nominally equal and out-of-phase output signals, with some characteristic (and matched) source impedance seen at the two terminals. As will be seen, from a noise susceptibility standpoint, it is highly desirable that these two impedances be well balanced, i.e., matched. The driver is connected to the input end of a balanced transmission line, typi-

cally a shielded twisted pair. At the opposite end of this line, a differential-input receiver receives the balanced signal, and (ideally) rejects CM voltages. As it turns out, the design of both the driver and the receiver have great influence upon how well the overall scheme works in transmitting a noise-free audio signal from driver to receiver. References 2 and 3 discuss different driver and receiver types, active and passive. These papers bring out the degradation in noise susceptibility active receivers can trigger if they do not have input characteristics that are an appropriate complement to the system driving impedances.

From a noise introduction point of view, the balanced transmission system we're talking about can be analyzed as a bridge circuit, such as that shown in Figure 1. Here, two source resistances R_{S1} and R_{S2} correspond to the output resistances of the differential driver voltage sources (which are not explicitly shown). Input resistances R_{IN1} and R_{IN2} correspond to the input resistances of the differential receiver.

It would be useful to examine some fundamental concepts of this bridge's behavior before focusing on any audio system specifics. Such a bridge, when maximized for output sensitivity, will produce a differential output V_{OUT} , which is highest as a function of an element unbalance when all four resistances are of the same order (for example, this is usually the case in a transducer bridge).

The following expression illustrates the intrinsic bridge common-mode rejection (CMR) sensitivity when R_{IN} and R_S are generally similar in value (for maximum sensitivity):

$$CMR(dB) = 20 \log_{10} \left(1 + \frac{R_{IN}}{R_S} \right) \frac{1}{K_R}$$

Some sample calculations with this relationship show that CMR is a minimum for a given change in K_R (a resistor deviation in fractional form) when $R_{IN} \sim R_S$. A CMR minimum is simply another way of saying that the bridge is most sensitive when $R_{IN} \sim R_S$.

TIP: On the other hand, bridge sensitivity is minimized when the upper arm resistances are low in relation to those of the lower arms. This improves substantially as R_{IN} becomes $\gg R_S$. Or, in an audio system, as the driver R_S is by design made much less than the receiver R_{IN} .

In the example shown, there is a 1/30,000 ratio between the R_S/R_{IN} upper/lower elements. This factor makes relatively high-percentage changes in either the upper (or the lower) arm resistances a somewhat harmless phenomenon, or in other words, value changes will have little CMR effect upon the output. For example, for the

Figure 1 values and a 10% change in one R_S , this produces an output which is about 110 dB down from the noise voltage V_{CM} . By contrast, if all the bridge values were equal, the same 10% deviation would produce an output only 26 dB down!

In a real transmission system, there will be inevitable noise potentials developed between the respective driver and receiver chassis com-

mon points, since they are located separately and are powered with different ac power sources. As a result, the noise voltage so developed, V_{CM} , in effect drives a bridge like Figure 1, formed by the differential driver outputs and the two downstream receiver inputs. As noted, dependent upon the bridge's relative sensitivity, some fraction of V_{CM} will appear as a noise component of V_{OUT} . Finally, it is important to realize that what has been discussed thus far addresses only how the most basic portion of this system generally impacts CMR. The line receiver design itself obviously also has a big influence, and this is discussed next.

A Buffered Line Receiver: The circuit of Figure 2 represents an example of a classic 3-op-amp instrumentation amplifier (in amp) topology, dressed up and optimized for use as an audio line receiver. The use of FET in-



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put stage buffers in amplifiers U1A and U1B allows megohm-level bias resistance to be used for R_{IN1} and R_{IN2} , which greatly desensitizes this receiver against source loading and the potential CM errors which can result. Protection resistors R_{p1} and R_{p2} allow overvoltages at the two inputs by limiting amplifier fault currents. The input stage can use either dual or single amplifiers, with performance options described below.

The differential gain of the U1 stage (or G1) is set by the R1-R3 network, as:

$$G1 = 1 + \frac{2R1}{R2}$$

where $R1=R3$, and $R2$ is used for overall gain programming.

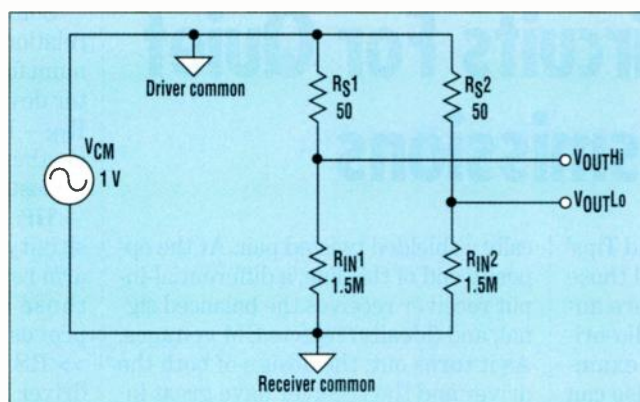
While the differential gain of U1 is as noted, the CM gain is nominally unity, since the connection simply passes CM signals to the output. Thus, both differential and CM forms of signal are presented to the inputs of stage U2. Note, however, because differential and CM signals are scaled differently by U1, there is a net potential gain in overall CMR. Practically, it means that this overall configuration can achieve useful CMR figures higher than the intrinsic CMR of U2, whatever that figure may be.

The U2 stage, a pretrimmed 4-resistor in amp, suppresses the CM component from U1, while amplifying differential signals by a factor of 1/2. This makes the net overall gain (G) of this line receiver:

$$G = 0.5 + \frac{R1}{R2}$$

For overall gains of 1, 2, and 4 times, the required gain resistance, $R2$ works out to be 10, 3.32, and 1.43 k Ω , respectively, using standard values.

Seasoned analog designers may already be wondering what's so new about this circuit, as it has been around for at least 30 years in solid-state form.⁴ While that's true, some refinements here lend it worthwhile audio



1. A conceptual diagram of a balanced line-driver source and a balanced line receiver with CM voltage can be shown as a bridge circuit.

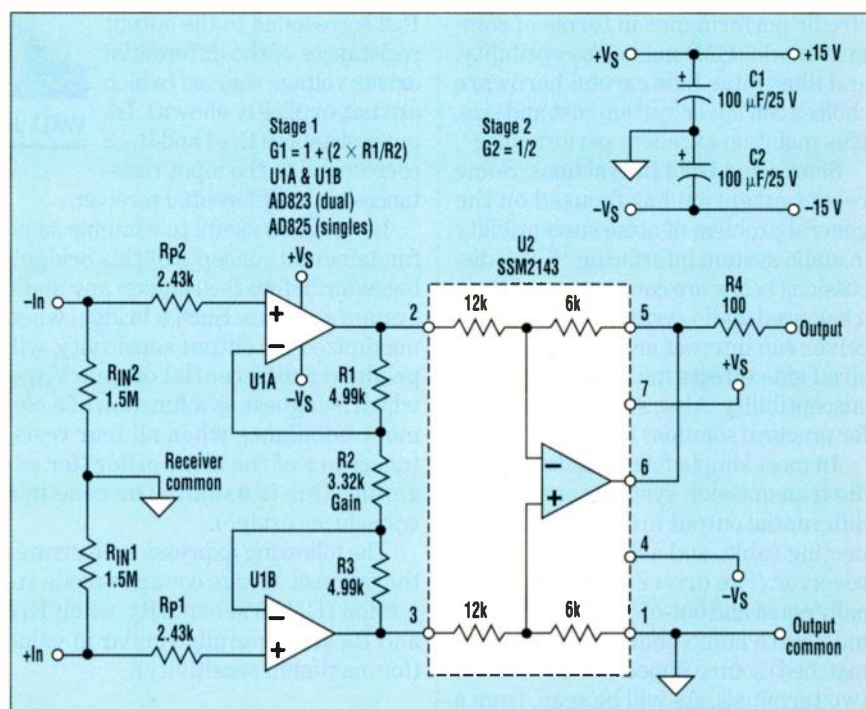
Resistances R_{S1} and R_{S2} are the source resistances of the two driver outputs, while R_{IN1} and R_{IN2} correspond to input resistances of the two receiver terminals. Noise voltage V_{CM} , which appears between the chassis common points of the driver and receiver, can, dependent upon the bridge's relative balance, develop an undesired noisy output signal. This noise voltage appears due to the CM to differential-mode conversion of the bridge, and once created, cannot be suppressed. Key to controlling this noise-injection mechanism is the control of impedances R_S and R_{IN} and their relative balance.

tance values used for R_{IN1} and R_{IN2} .

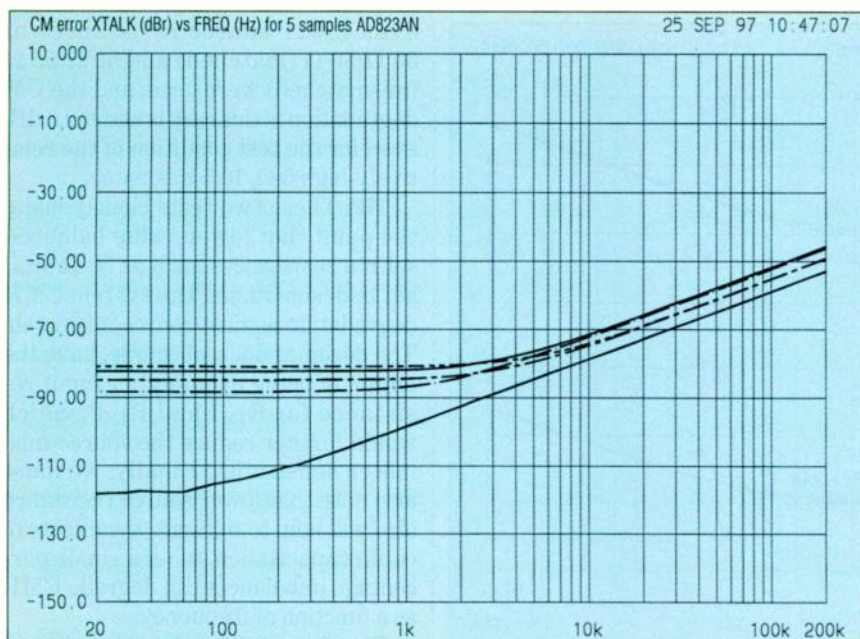
While FET amplifiers are most useful here, they must not be the general purpose types prone to sign-reversal, which could possibly come about with combined large-signal and CM inputs. Both of the types listed have unique N-FET input stages, with CM ranges that approach both rails without danger of anomalous phase reversals. Wideband U1 operation also is a virtue, as this allows better high-frequency performance before CM degradation sets in. Finally, an FET input structure is less susceptible to RF rectification problems, which can be critically important in an audio line receiver used within an RF environment.⁵ In general, as digital signal process-

ing with resolutions greater than 16 bits becoming more prevalent, good CM rejection to frequencies appreciably higher than audio bandwidths becomes increasingly important.

ing with resolutions greater than 16 bits becoming more prevalent, good CM rejection to frequencies appreciably higher than audio bandwidths becomes increasingly important.



2. The buffered input line-receiver circuit shown can be used to maintain high-audio system CMR, even for instances where the source impedance may be unbalanced. Key to the operation is the use of FET-input amplifiers for stages U1A and U1B, and a high CMR in amp IC for stage U2. With proper selection of devices, CMR of 90 dB or more is possible up to several kilohertz, and as high as 80 dB at 20 kHz. Gain of this amplifier is programmable by selection of $R2$.



3. The CMR performance of five AD823 samples operating in the circuit of Figure 2 at a gain of 2 is shown. Measured low-frequency CMR ranges from about 82 to 88 dB for four units, with one device showing an anomalous 118-dB CMR. 20-kHz CMR for the devices is centered around 75 dB.

Selection of the U2 device also has a great bearing on performance. Although there are a number of unity-gain 4-resistor in amps available for the U2 function, the choice here is for less than unity gain (in this case 0.5). Although the U1 stage's output must swing twice that of U2 for U2 to approach clipping, this isn't a problem.

Performance: To demonstrate these concepts, a number of measurements were made on the Figure 2 line receiver circuit, using both AD823 (dual) and AD825 (single) op amps for the U1A and B positions, an SSM2143 for U2, and also with and without an isolation transformer preceding the amplifier. Although this basic 3-amplifier in amp structure can, in principle, offer potential gains in CM performance over the intrinsic CMR of U2, this phenomenon is less pronounced at relatively low overall gains, as is the case here (i.e., gains of 1, 2, or 4 times). And, it also is dependent upon the specific U1 and U2 performance. Thus, the CMR of both the U1 and U2 stage devices can and will effect the final measured CM performance.

The test setup used employs an Audio Precision System 1 in a modified crosstalk test mode, where channel A drives the test circuit, which in

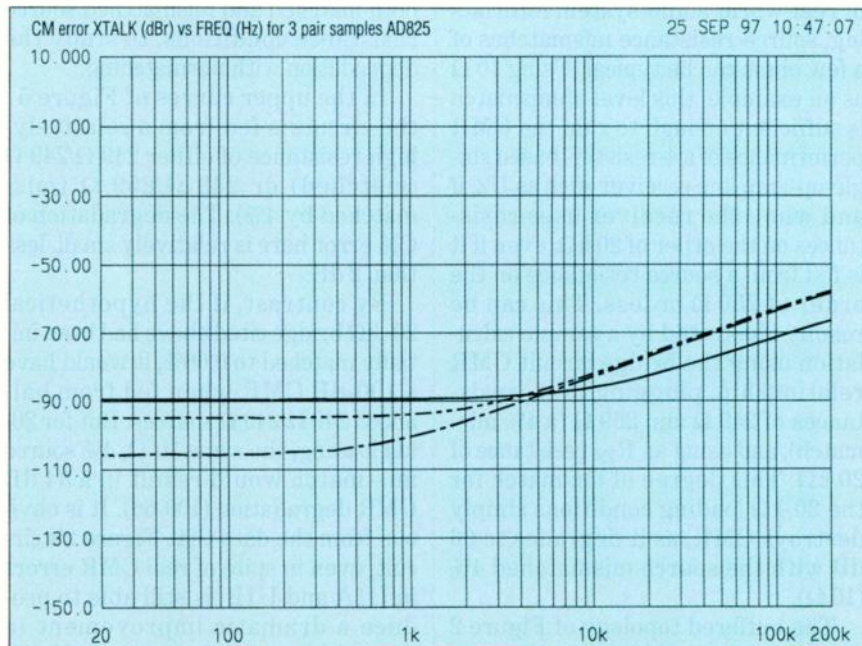
turn, has its output monitored by channel B. This allows a swept narrow band tracking analysis, over a dynamic range approaching 150 dB at low frequencies, and ranging from 20 Hz to 200 kHz.

For initial test purposes, five U2 devices were tested alone, with low

frequency CM error ranging from -77.27 to -85.16 dB. From this group, an intermediate device was then used in the complete circuit's testing (CMR = ~80 dB). In the results following, the CM error curves displayed are in all cases referenced to a 0 dB calibration output level from U2 of 1, 2, or 4 V rms, for the various gains. The test input level to the Fig. 2 circuit was 1 V rms.

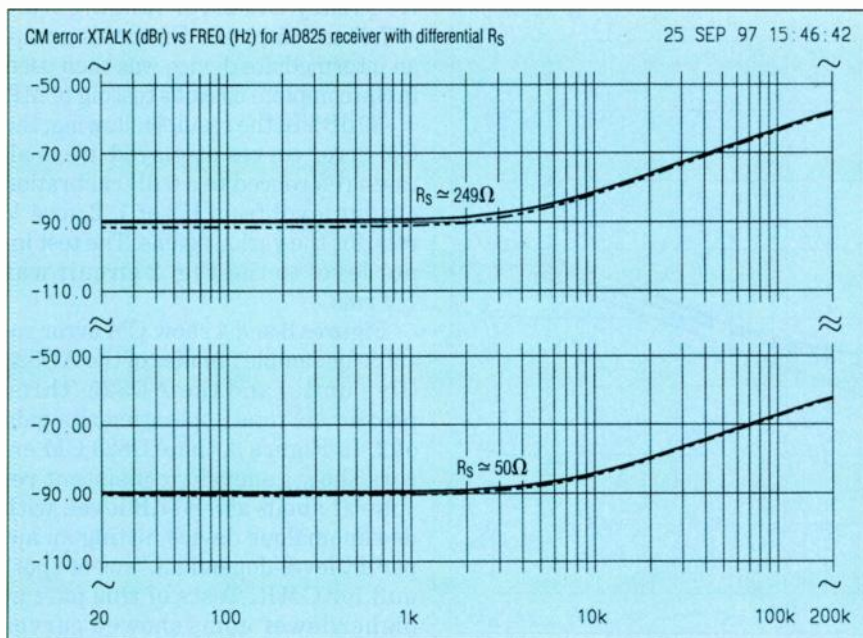
Figures 3 and 4 show CM error results for sample families of the AD823 (five units) and the AD825 (three pairs or six total), operating at a gain of 2. In Figure 3, the AD823 CM errors show generally consistent results at about an -85-dB level, with one anomalous device hitting an apparent level-dependent "sweet spot" null for CMR. Tests of this part at higher/lower gains showed curves more like the general grouping of the other four devices. The CM error corner for these devices occurs at about 2 kHz, sufficient for all parts to achieve -50 dB or better CM errors at 100 kHz, and around -75 dB or better in the audio band.

In Figure 4, the AD825 CM errors show more consistent results, at about -90 dB or better levels. For these devices, the CM error corner occurs at 5 to 10 kHz, sufficient for all to achieve -60 dB or better CM errors at



4. The CMR performance of three paired (six) AD825 samples within the circuit of Figure 2 at a gain of 2 is shown. Measured low-frequency CMR ranges from about 89 to 106 dB for the pairs. 20-kHz CMR for these pairs is around 80 dB.

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5. The CMR performance of the 89-dB CMR AD825 pair within the circuit of Figure 2 at a gain of 2 is shown, as exercised with variable source resistance. In the upper plot, the differential CMR performance is shown for source resistances of 249 Ω /249 Ω (matched) and 249 Ω /259 Ω (mismatched), and the mismatched degradation is less than 2 dB. In the lower plot, the differential CMR performance is shown for lower source resistances of 50 Ω /50 Ω (matched) and 50 Ω /55 Ω (mismatched), and the mismatched degradation is less than 1 dB.

100 kHz, and around -80 dB or better in the audio band.

One criticism of active line receiver circuits has been high sensitivity to source resistance mismatches. In the relatively uncontrolled environment of real-world audio-system interfacing, source-resistance mismatches of a few ohms can be typical. Using 10 Ω as an example, this level of mismatch is sufficient enough to ruin the CMR performance of a 4-resistor-based single-op-amp line receiver such as U2, if and when the receiver uses resistances on the order of 20 k Ω , even if it is fed from a source resistance on the order of 250 Ω or less. This can be readily illustrated by a sample calculation using the bridge circuit CMR relationship, plugging in R_S resistances of 249 Ω and 259 Ω (a 4% mismatch), and using an R_{IN} resistance of 20 k Ω . This degree of mismatch for the 20-k Ω loading conditions simply destroys CMR, as it degrades to 66 dB with the source mismatched 4% (10 Ω).

The buffered topology of Figure 2 directly addresses this issue, as shown in the dual mismatched source resistance CM plots of Figure 5. In these tests, the Figure 2 circuit is exercised

using one of the intermediate performance AD825 op-amp-pair samples (-90-dB CM error), at a stage gain of 2. The circuit is fed from two separate conditions of absolute source resistance, each of which is operated under both matched and mismatched source resistance conditions, to study the degradation with mismatching.

In the upper curves of Figure 5, the circuit is fed from a relatively-high resistance of either 249 Ω /249 Ω (matched) or 249 Ω /259 Ω (mismatched by 4%). The degradation of CM error here is relatively small, less than 2 dB.

By contrast, if the hypothetical 20-k Ω bridge cited above had been initially matched to 0.08%, it would have a 100-dB CMR when fed from balanced 249 Ω /249 Ω sources. But for 20-k Ω loading, the same 10- Ω , 4% source mismatch would result in a 34 dB CMR degradation (100-66). It is obvious from the data that Figure 2's circuit, even in spite of real CMR errors in U1A and U1B, is still able to produce a dramatic improvement (a degradation of 2 dB for the buffered circuit, versus 34 dB for the same mismatch and 20-k Ω loading).

In the lower curves of Figure 5,

even lower source resistances of 50 Ω /50 Ω (matched) and 50 Ω /55 Ω (mismatched) were used, and the CM degradation in this case is about 0.8 dB, even for the test condition of the relatively-high 5- Ω , 10% mismatch.

TIP: These two tests clearly make the point that lower-value balanced source resistances such as 50 Ω /50 Ω aid in desensitizing the system CMR degradation against source mismatch. The designer does, of course, have the option of using even-higher input resistance for R_{IN1} and R_{IN2} , which would further reduce the source-mismatch sensitivity. Finally, we must also note that lower source resistance also will help to mitigate the effects of cable capacitance, where small-percentage imbalances can degrade CMR as a function of frequency.

Transformers: The classic solution to the CM isolation of audio signals is the line-input transformer.^{6,7} This device, usually a 1:1 wound unit, offers galvanic isolation and very high CM voltage-breakdown ratings. It is a preferred (or only) solution where true galvanic isolation is a necessity. A telephone line interface is one example.

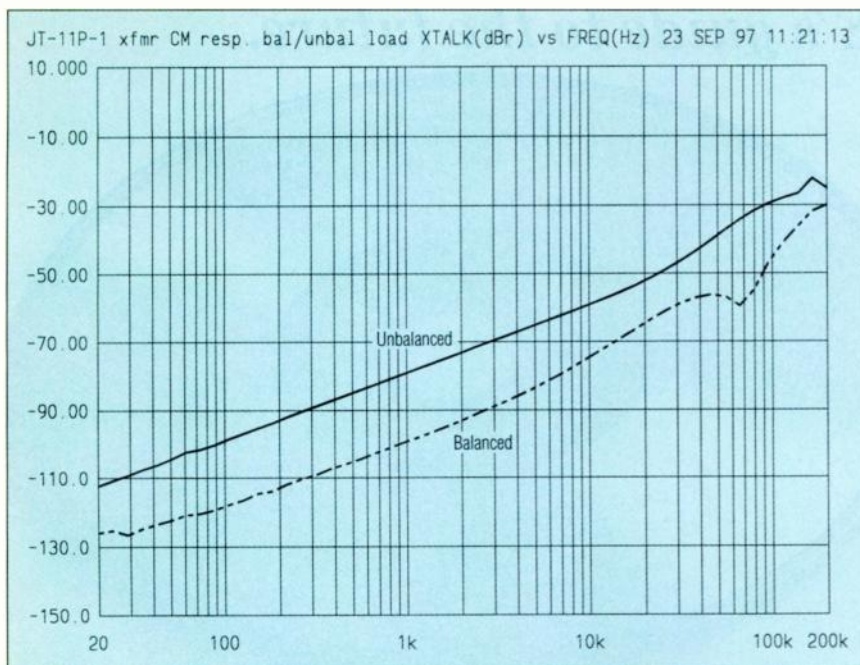
Transformers are also useful for high- and consistent low- to middle-audio-frequency CM performance, both from unit to unit, and also when immunity to varying differential source resistance is sought. These features do come at some cost however, as quality transformers are not only pricey, they occupy a relatively large package size vis-à-vis a solid-state equivalent.

All of the various factors above are the designer's ultimate decision points, dependent upon the exact requirements. When optimized for high performance, it is not likely that either a completely solid-state or a transformer-based line receiver solution will be considered either simple or low in cost.

Interestingly, when the near-ultimate in low-frequency CM rejection is required, a hybrid solution of a line transformer buffered by the Figure 2 in-amp circuit can offer very-high performance, as is shown by the data of Figure 6.

In this test, a JT-11P-1⁶ line transformer is operated with the secondary in both balanced and unbalanced termination modes, as buffered by the

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6. The CMR performance of a 1:1 line transformer with a buffer amplifier consisting of the Figure 2 circuit at unity gain is shown. In the upper curve, the transformer is operated with unbalanced secondary loading, and the CMR is above 110 dB at low frequency, degrading to just over 50 dB at 20 kHz. In the lower curve reflecting balanced loading, the CMR is generally about 20 dB better over almost the entire frequency range, actually approaching the noise floor at the lowest frequencies.

Figure 2 circuit operated at unity gain. The transformer secondary is terminated in a 10-k Ω (2×5 k Ω) resistance, which is either center tapped to ground (balanced), or grounded on one winding end (unbalanced). The test results show up to a 20-dB improvement for the balanced case, and the low frequency CM error is reduced to nearly -130 dB (approaching the noise floor of the instrumentation). While this buffered transformer circuit offers superlative low frequency CMR, it also can be noted that this degrades with rising frequency.

Summary: Both active and passive solutions to minimizing CM noise have been explored, each with their own set of characteristics. Readers should take these data for general trends, as opposed to absolute performance levels. Both higher-performance as well as lesser devices no doubt exist in the transformer universe, which should be explored before settling on a final solution. Similarly, there are numerous other op amps which could not be exercised for this brief study, and certainly both better and/or worse samples can likely be found.

The general problem of induced CM

errors in differential signaling systems (including balanced audio systems) is fundamentally rooted in CM to differential-mode conversion. As the Figure 1 bridge shows, once CM signals undergo mode conversion, they become part of the desired signal.

Errors of this sort are minimized by very carefully controlling CM loading of the differential sources, as shown by the example of Figure 2. Alternately, they are also controlled by maintaining differential mode (only) loading, as shown by the transformer example of Figure 6.

To summarize, the active line receiver discussed here offers excellent wideband CMR with low differential-source-resistance sensitivity, and can be customized in a variety of ways, including gain, CM input impedance, etc.

TIP: This solid-state line-receiver has the virtues of better high-frequency CMR, as well as better CMR versus frequency flatness. While the circuit shown works well, optimization for a production role may need some enhancement for worst-case minimum CMR. This can be done via careful trimming or selection of the U2 circuit, and/or selection of an optimum pair of

singles for U1A and U1B.

TIP: The buffered transformer approach to a line receiver offers good to superlative low-frequency CMR, combined with "no tweak" operation, and, if used with an in amp for balanced secondary buffering, even further CMR reduction is possible. On the downside, there are negatives of cost, size, and degradation of CMR with frequency.

Hopefully, this audio system performance discussion has been helpful. Comments are particularly welcome on experiences with noise-susceptibility issues in balanced systems. Keep those cards and letters coming, and watch this space for future enhancements to these circuits.

Acknowledgments: While preparing this article, review comments were received from Derek Bowers, Moshe Gerstenhaber, and Neil Muncy. Their contributions were much appreciated.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to *Electronic Design*, he can be reached via e-mail at Walter.Jung@Analog.com.

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Baseline Restorer Uses A Current Conveyor

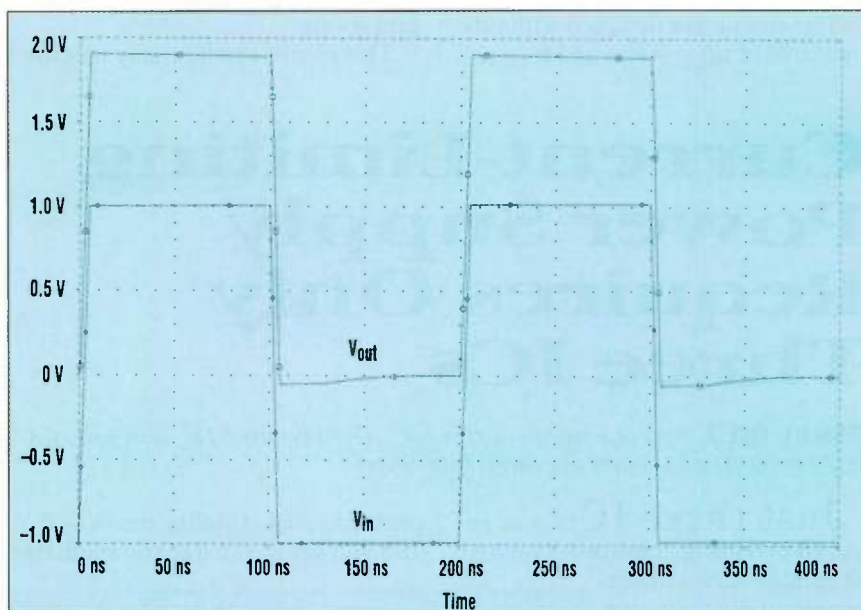
KUMEN BLAKE, Burr-Brown Corp., P.O. Box 11400, MS #206, Tucson, AZ 85734; (520) 746-7146; e-mail: blake_kumen@burr-brown.com.

Pulse-modulated signals often need level shifting to compensate for dc offsets, injected noise, or wander caused by ac coupling a variable duty cycle pulse train. The "baseline restorer" shown (Fig. 1) is an improved version of a circuit described in the paper "Baseline Restoration Using Current Conveyors," from the *IEEE Transcripts On Nuclear Science*.¹ It produces a pulse train with a constant baseline of 0 V (Fig. 2). This circuit uses few components, and is easy to design.

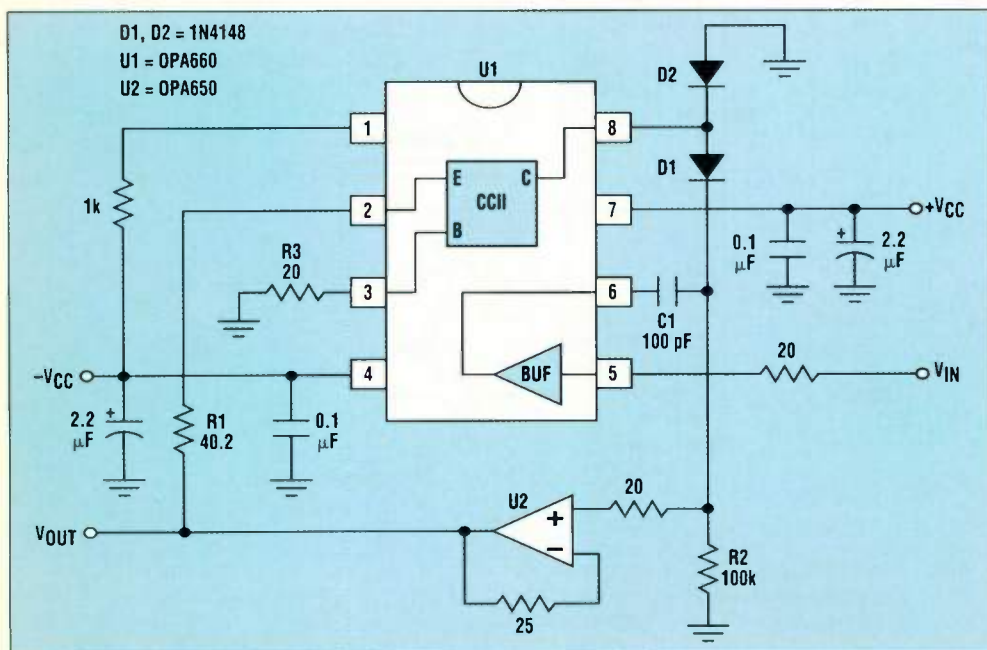
Lying at the heart of the circuit is the current conveyor (CCII), which is part of U1 (OPA660). The data sheet calls this a transconductance amplifier; but it also functions as a very good current conveyor with a current gain of 1. The impedance at E is low ($r_E \approx 16 \Omega$), and the output impedance of C (r_C) is high. The CCII's behavior can be described

with these equations: $V_E \approx V_B$, $I_C \approx I_E$ and $I_B \approx 0$. The output voltage at C (V_C) depends on the external circuit.

U1 also contains a unity-gain voltage buffer (BUF) that serves to buffer the input voltage. U2 (OPA650) buffers the restored signal from the output. It also converts V_{OUT} into a current into pin 2 of U1 (E). This current needs to be high so that D1 can



2 These waveforms depict the action of the baseline restorer. Although the input pulse train (lower trace) swings well-below ground, the restorer circuit's output has a 0-V baseline (upper trace).



1 At the heart of this improved version of a baseline restorer is an OPA660 transconductance amplifier. However, in this circuit, it functions as a current conveyor, with a current gain of 1.

recover quickly from reverse saturation.

When the output voltage (V_{OUT}) tries to go below ground, U2 and R1 produce the current $I_E = -V_{OUT}/(R1+r_E)$ at pin 2 of U1 (E). This current appears at pin 8 of U1 (C) as I_C , and goes through diode D1. It then is dumped onto C1. After D1 comes out of reverse saturation (with a propagation delay of t_{PD}), then V_{OUT} exponentially approaches 0 V with a time constant of $\tau_{REST} = (R1+r_E) \times C1$. This action overcomes the influence V_{IN} has on V_{OUT} . Thus, the baseline (the bottom of the pulses) is restored to 0 V each time a pulse at V_{OUT} tries to go below ground.

When the output voltage

(V_{OUT}) is above ground, V_{IN} is ac-coupled to V_{OUT} by C1. I_C goes through D2, which keeps the CCII's output from saturating, and thus doesn't affect V_{OUT} . R2 causes the output dc level to decay to 0 V with a time constant of $\tau_{DECAY} \approx R2 \times C1$. If τ_{DECAY} is too large, not all of the pulses would be restored to 0 V, because the wander plus pulse would increase faster than the decay.

This circuit was designed with time constants of $\tau_{REST} \approx 6$ ns and $\tau_{DECAY} =$

10 μ s. R1 was set to keep from overdriving the output of U2. The diodes used to produce Figure 2 are high-speed switching rectifiers (1N4148) with $t_{RR} \approx 4$ ns, which gave $t_{PD} \approx 25$ ns at the design point. Schottky or PIN diodes with lower capacitance and reverse recovery time can be substituted for better performance. Selection of the other components is described in the OPA660 and OPA650 data sheets.

This circuit can be easily modified

to restore the maximum output voltage to a dc level by reversing D1 and D2. The baseline voltage can be changed to an arbitrary level by connecting pin 3 of U1 (B) and R2 to a voltage reference.

Reference:

1. A. Miguel, et al., "Baseline Restoration Using Current Conveyors," *IEEE Trans. On Nuclear Science*, Vol 43 (3), June 1996, p. 1712-1716.

Current-Limiting Power Supply Requires Only Three ICs

GERALD L. KMETZ, *Micrel Semiconductor Inc., 1849 Fortune Dr., San Jose, CA 95131; (408) 435-3448; fax (408) 944-0510.*

Just three ICs are required to build an adjustable-voltage, adjustable-current-limit power supply that operates like a laboratory supply. It offers an output voltage range of 0 V to 25 V and a current limit range of about 10 mA to 1.5 A. The Micrel MIC29153 LDO Regulator has a ground-referred bandgap (reference) voltage. Other adjustable regulators with ground-based reference voltages also should work.

Looking at the lab supply schematic, amplifiers A1 and A2 implement output voltage control (Fig. 1). The output-voltage adjustment operates by controlling the ground reference potential of the feedback voltage divider. The internal bandgap-reference voltage, which is sensed via V_{ADJ} by A1,

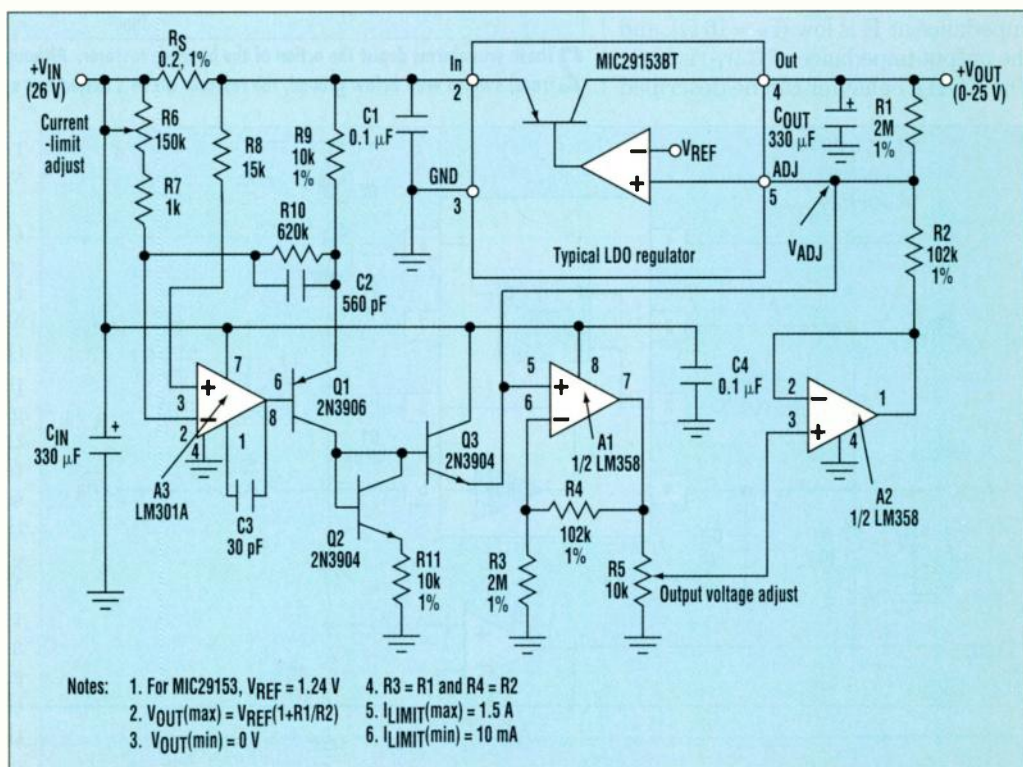
provides adjustability down to 0 V. The voltage at pin 5 of the regulator

remains constant when the closed-loop system is in regulation.

Using this technique facilitates output-voltage adjustability down to 0 V without using an external reference voltage. In this design example, the voltage gain required of A1 is determined as follows:

$$A_V = 1 + R4 / R3 = 1.05$$

When R5 is adjusted so that the input to voltage follower A2 is taken from the high side of the potentiometer, the gain of A1 will bias voltage di-



An adjustable-voltage, adjustable-current-limit power supply can be built with just three ICs. Output voltage range is 0 V to 25 V, while current-limit range is approximately 10 mA to 1.5 A.

vider R1 and R2. As a result, summing junction voltage V_{ADJ} will equal V_{REF} when V_{OUT} is 0 V. For the MIC29153, V_{REF} is 1.24 V. Note that the direction of current flow in voltage divider R1 and R2 is in the reverse direction from normal operation. The direction of current flow changes to "normal" when $V_{OUT} > V_{REF}$.

Conversely, when R5 is adjusted to provide ground (0 V) at the bottom of R2, the regulator output voltage is the designed 25-V maximum. Rotating R5 results in a smooth variation of output voltage from 0 V to the upper design value, as determined by R1 and R2. The following relationship specifies the highest output voltage:

$$V_{OUT(max)} = V_{REF}(1 + R1/R2)$$

Different maximum output voltages are readily achievable—first calculate new values for R1 and R2; then simply set $R3 = R1$ and $R4 = R2$.

Amplifier A3 provides the adjustable current-limit capability. It amplifies the voltage dropped by current-sensing resistor R_S . For $I_{OUT(max)} = 1.5$ A and $R_S = 0.2$ Ω , the differential input signal to A3 (pin 2) is +0.3 V. Lower gain settings for A3 correspond to higher output currents, while higher gains correspond to the lower output currents. The design approach is as follows:

For highest output current:

$$A_V(min) = \frac{V_{REF}}{V_S(1.5 A)} = \frac{1.24 V}{0.3 V} = 4.13$$

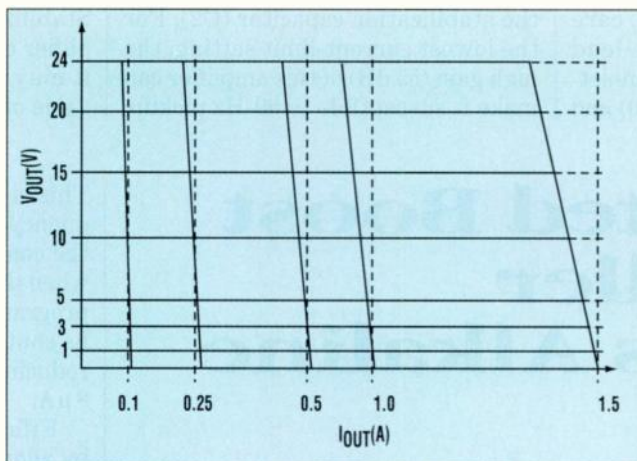
And:

$$A_V(min) = \frac{R10}{R6 + R7} = \frac{620 k\Omega}{151 k\Omega} = 4.11$$

For lowest output current:

$$\begin{aligned} A_V(max) &= \frac{V_{REF}}{V_S(10 mA)} \\ &= \frac{1.24 V}{2.0 mV} = 620 \end{aligned}$$

And:



2 Current-limit accuracy versus output voltage is given for the power supply. The vertical grid lines represent ideal current limiting.

$$\begin{aligned} A_V(max) &= \frac{R10}{R7 (R6 \text{ set at } 0 \Omega)} \\ &= \frac{620 k\Omega}{1 k\Omega} = 620 \end{aligned}$$

The current-sense amplifier output signal is the voltage developed across R11. Q1 produces the ground-referenced voltage required for feedback control of the MIC29153. Because the function of the current-limit circuitry is to reduce regulator output voltage, emitter follower Q3 essentially diode-couples its output signal to the regulator-loop summing junction. Diode-connected Q2 provides first-order temperature compensation for the V_{BE} of Q3.

In depicting the accuracy of the current-limit function, the voltage extends only to 24 V because in the circuit breadboard resistor tolerances limited the maximum output to about 24.6 V (24 V was the closest whole number convenient for making measurements) (Fig. 2). The vertical grid lines represent ideal current limiting. The

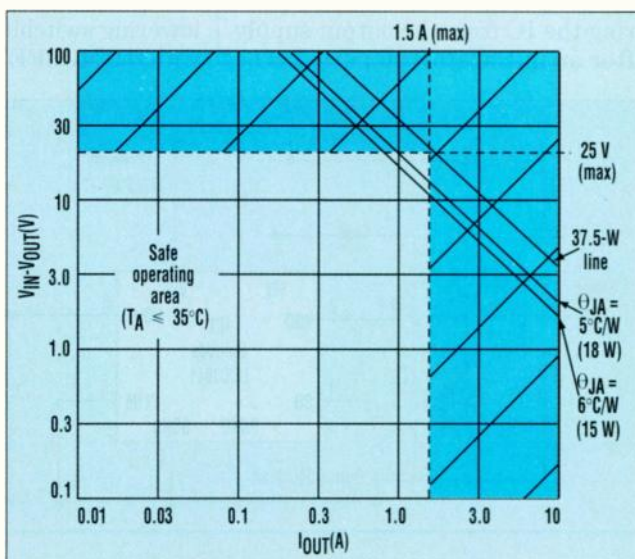
graph shows approximately worst-case performance.

Because of the wide input-to-output voltage range and current capability of this design, it's difficult to provide a sufficient heat sink to remain within the safe operating area (SOA). Nonetheless, an efficient heat sink is very important. The thermal shut-down capability of the MIC29153 will prevent destruction, but it's a nuisance to encounter shut-down in use. The SOA associated with this circuit at an assumed maximum

ambient temperature and two possible system thermal impedances is shown (Fig. 3).

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

A 35°C maximum ambient temperature allows for a 90°C junction temperature rise. Maximum allowed junction temperature for the regulator is 125°C. The 5°C/W and 6°C/W system θ_{JA} shown in Figure 3 are practical, but represent large (extruded) heat sinks. The θ_{JC} of a MIC29153BT (TO-220 package) is 2°C/W. Since θ_{CS} is typically 1.0°C/W, θ_{SA} must be 2°C/W ($\theta_{JA} = 5$) or 3°C/W ($\theta_{JA} = 6$).



3 The graph indicates the safe operating area associated with this circuit at an assumed maximum ambient temperature and two system thermal impedances. Here, $T_A(max) = 35^\circ\text{C}$, and $\theta_{JA} = 5^\circ\text{C/W}$ and 6°C/W .

When building this circuit, care should be taken to minimize lead lengths associated with the gain-setting resistors (R6, R7, and R10) and

the stabilization capacitor (C2). For the lowest current-limit setting, the high gain (55 dB) of this amplifier can make it susceptible to 60-Hz pickup.

Stabilizing the current-sensing amplifier circuit can be temperamental; it may be necessary to adjust the value of C2.

Integrated Boost Controller Extends Alkaline Usage

EDDY WELLS, *Unitrode Corp., 7 Continental Blvd., Merrimack, NH 03054; (603) 429-8906.*

Disposable alkaline batteries are used in many portable applications because of their low cost and availability. A single-cell alkaline battery has useful capacity from 1.6 V down to below 1 V, although this full range isn't usually exploited. By extending the input voltage range of the power converter to reflect the usable voltage of the cell, the run time of the portable device can be increased significantly.

The boost converter shown will start up and deliver full-rated current with a 1-V input, and will operate down to 0.4 V (*see the figure*). Low-voltage operation is achieved by powering the IC from the output supply after an initial startup period. The

UCC3941 comes in three versions of the main output: 3.3 V, 5.0 V, and adjustable. Of course, the overall efficiency of the converter also will influence battery usage.

Today's portable equipment can require hundreds of milliwatts when fully functioning, yet only a few milliwatts in low-power modes. Therefore, it's important that the converter is efficient over a wide range of load current. To achieve efficiency improvements, the boost converter shown uses synchronous rectification along with internal n-channel MOSFET switches.

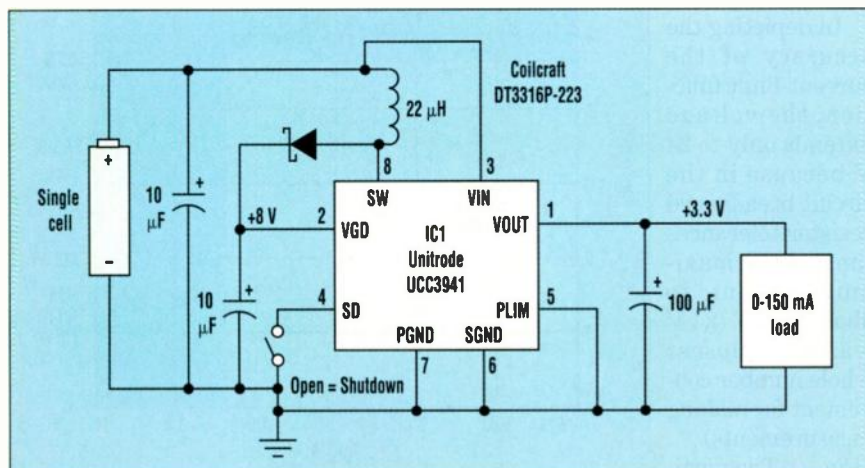
Light load efficiency is improved by lowering switching losses associated with the MOSFET gate capacitances.

This is accomplished by a pulse-frequency-modulation scheme, in which the converter only transfers energy when the output voltage falls below a programmed threshold. The part can be shut down by opening the SD pin, reducing current consumption to just 8 μ A.

Efficiency at full load is improved by allowing the converter to operate in the continuous conduction mode. This reduces conduction losses and increases the capability of the converter to deliver power to the load. A resistor can be connected to the PLIM pin to set the maximum continuous current for the converter. Grounding this pin allows the maximum peak current.

Conduction losses are further reduced by lowering the $R_{DS(on)}$ of the MOSFET switches. Because the 3.3-V output will not fully enhance the MOSFETs, an 8-V output is created for the gate drive. This higher voltage often is generated by using a separate charge pump circuit. However, this technique increases component count and decreases system efficiency. The UCC3941 takes a novel approach to the problem of creating a higher gate drive voltage: the energy stored in the boost inductor is time-multiplexed between the main output and an auxiliary output used for the gate drive. An internal arbitration scheme decides which output receives the stored energy. This approach has minimal impact on board real estate, since the auxiliary voltage is created using only an additional diode and capacitor.

All capacitors used for the converter should have low ESR and ESL in order to minimize output ripple. Designers can also take advantage of the auxiliary output. The auxiliary output can be loaded with an additional 100 mW, allowing it to be used for a number of applications such as a liquid-crystal display, a communications interface, or to trickle-charge a secondary battery.



This integrated synchronous boost regulator generates 8-V of gate drive for the internal MOSFET switches, and a 3.3-V output from a single alkaline cell. The circuit delivers up to 500 mW to the load. When in shutdown mode (pin SD open), current consumption is reduced to 8 μ A.

Modified Totem Pole Simplifies Wideband Current Output Circuits

JERRY STEELE, National Semiconductor Corp., Tucson Design Center, 6377 E. Tanque Verde Rd., Suite 101, Tucson, AZ 85715-3839; (520) 751-2380; fax (520) 751-2379.

Typical methods of incorporating power amplifier circuits in current-output configurations inevitably rely on a current-sensing resistor in the output circuit, such as the Improved Howland. This causes the load impedance to become a portion of the feedback network. In the case of inductive loads, it complicates the frequency stabilization of the circuit in such a way that it limits practical bandwidth.

By comparison, current output topologies that take feedback from an emitter or source while taking output from a collector or drain are better realizations of true current output. In addition, feedback response is isolated from that of the load by virtue of the unilateral characteristic of a common-base bipolar or common-drain MOSFET. Furthermore, this circuit, when configured as a voltage output, provides gain in the output stage yet keeps the biasing requirements simple.

The trade-off of this topology is that it requires that both power supplies float. Modern power-supply technologies with toroid-based switching supplies makes this a much more practical option compared to pure line-operated linear power supply.

Though a single current-sense resistor could be used with either no emitter ballasts, or a couple of small emitter ballasts (R_{E1} and R_{E2}), the setup in Figure 1 provides the optimum trade-off of component count versus bias stability. Two (relatively) large resistors in each emitter act as both current sensing and ballasting. This then requires the feedback to be

supplied from two separate sensing resistors.

Note how the feedback resistors work. Assuming that only one current source is active at a time, the feedback resistors then form a voltage divider with a 0.5 attenuation factor. Therefore, minimum gain is 2. The resultant gain equation is:

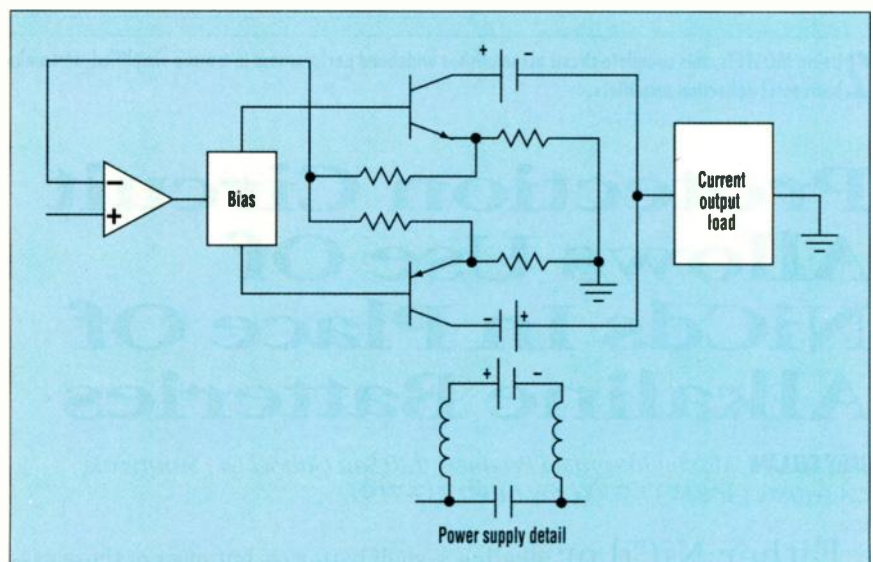
$$I_{OUT} = (V_{IN} * 2) / R_E$$

Figure 2 depicts a complete realization (MOSFETs are used here) of what is needed to achieve wideband performance, such as that required for a horizontal deflection amplifier. The first problem stems from the stray capacitance of the floating power supplies. This is overcome by isolating the

supplies with chokes, and including a high-frequency coupling capacitor so that the supplies resemble level-shifters as shown. The second problem is the Miller effect of the power devices, since they exhibit voltage gain in this topology. This is solved by cascoding the output devices.

Finally, an LM56 thermostat IC is included which shorts the input to the circuit in the event the power devices become overheated. Unlike a voltage amplifier, simply shorting the input ensures zero current output by virtue of the fact that this is, after all, a current amplifier (a voltage output configuration with zero input has a near zero output impedance that will allow reactive current to continue to flow). This quick current shutdown does, however, require the power devices include back-EMF diodes for voltage protection.

The circuit in Figure 2 may require a lot of current from the op amp regardless of whether it drives MOSFETs or bipolars. The LM7171, which is capable of a 100-mA output, is specified to meet this requirement. When used with MOSFETs, the LM7171 must be powered from ± 15 -V supplies, even though it's desirable to operate it at ± 5 V with bipolar output devices. Typically, wideband current source circuits that are stability-friendly, like this emitter/source feedback topology, will inevitably still require some com-



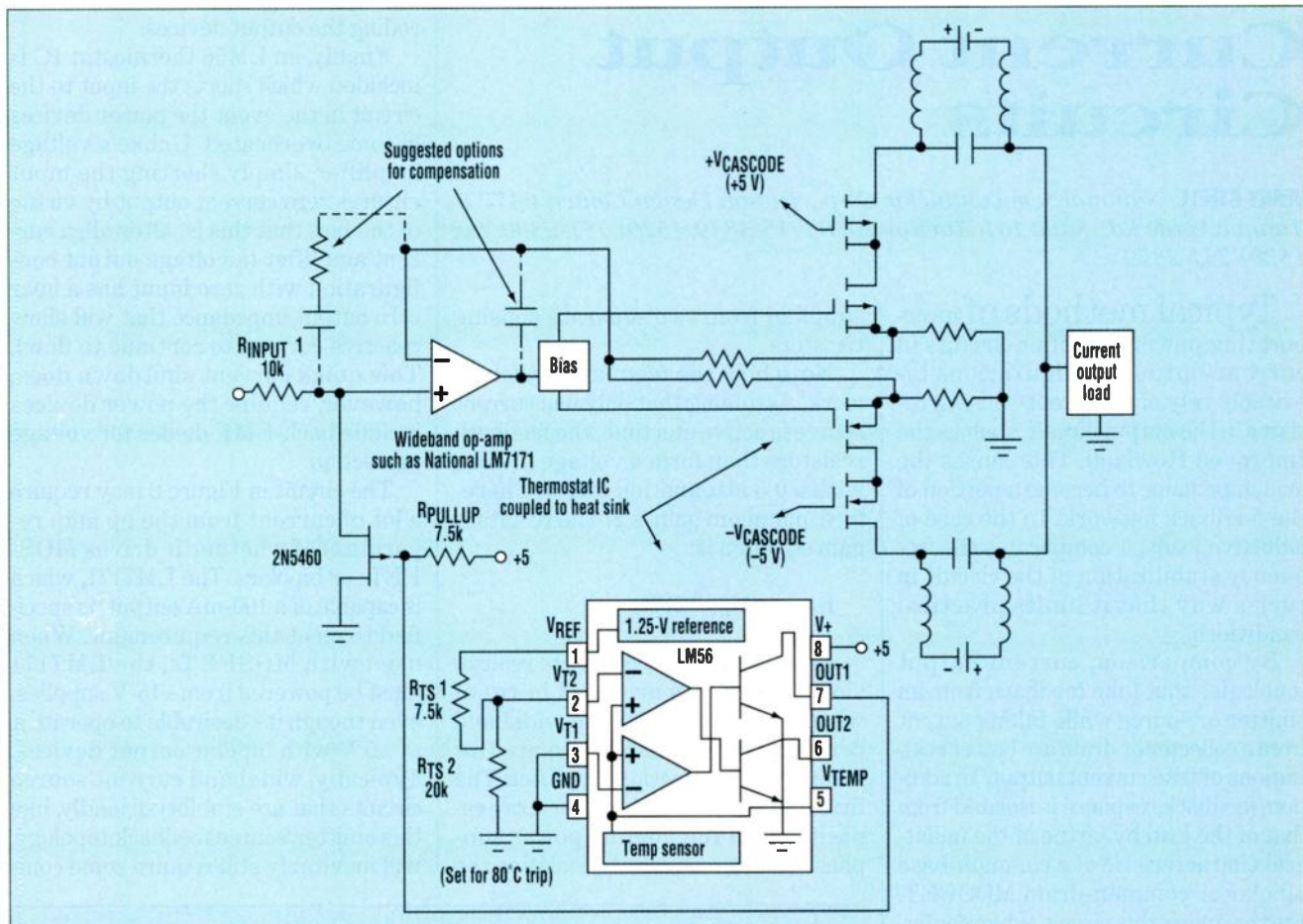
1 Although it requires floating supplies, optimum trade-off of component count versus bias stability is provided with this basic topology for a wideband current output amplifier.

pensation. Locations are indicated on the schematic; however, determination of component values for these is beyond the scope of this short application brief article and are covered thoroughly in the references cited.

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Graeme, Jerry, "Optimizing Op Amp Performance," available from Gain Technology; (520) 628-9000, or: <http://www.gain.com/gainsbooks.html>.

"Apex Power Integrated Circuits Databook," Volume 7, Application Notes 19 and 25; both available from Apex Microtechnology by calling (520) 690-8600; or: <http://www.teamapex.com>.



2 Using MOSFETs, this complete circuit accomplishes wideband performance in a more simplified, streamlined approach. It's well-suited for applications such as horizontal deflection amplifiers.

Protection Circuit Allows Use Of NiCds In Place Of Alkaline Batteries

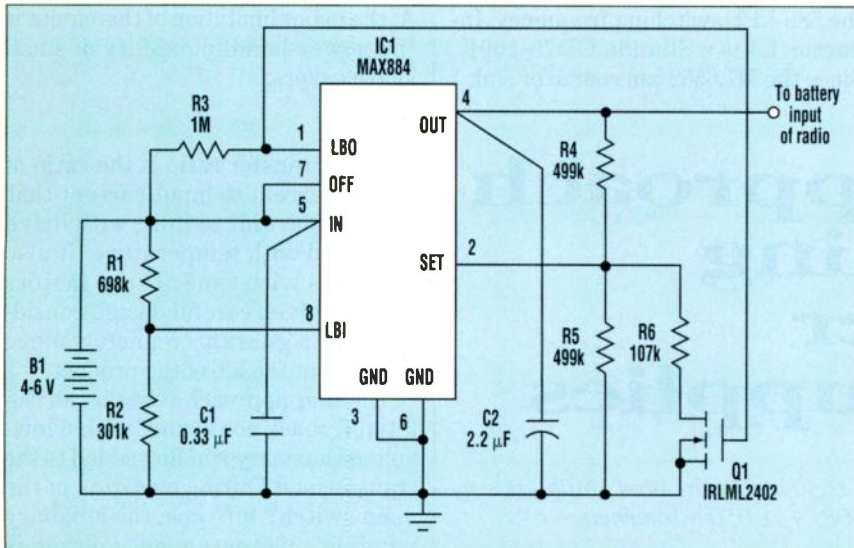
GARY SELLANI, Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600; fax (408) 737-7194.

Either NiCd or alkaline batteries will work in a system designed for use with standard off-the-

shelf batteries, but most of these systems are optimized for one battery type and not the other. Products de-

signed for the single-use alkaline batteries seldom include battery-protection circuitry; as a result, they may shorten a NiCd battery's lifetime (number of usable cycles) by discharging it too deeply.

The circuit shown ensures that a system will disconnect its load at a discharge level of 1 V/cell (appropriate for NiCds), rather than the typical 0.6 V to 0.8 V/cell for alkaline-battery systems that disconnect the load as a memory-protection measure (see the figure). The product shown is a radio that normally discharges its four-cell stack to 0.75 V/cell, then enters a



Interposing this circuit between battery and load protects NiCd batteries from excessive discharge. When the battery stack drops below 1 V/cell, IC1 produces an output voltage equivalent to 0.6 V/cell. This "fools" the radio, and it goes into its memory/clock-protection mode (0.75 V/cell trip point).

memory/clock protection mode.

IC1 is a low-dropout voltage regulator that includes a comparator for

detecting low battery voltage. The R1/R2 divider causes this comparator to trip when the battery voltage de-

clines to 4 V. Above 4 V, the comparator output (LBO) is high, allowing R3 to turn on Q1 by pulling its gate to the battery voltage. R5 and R6 are then in parallel, producing a SET voltage (IC1 pin 2) that varies from 0.9 V to 0.6 V as the battery voltage declines from 6 V to 4 V. This condition forces the regulator into dropout—a mode in which it acts as a 1-Ω switch between the In and Out terminals.

LBO goes low when the stack voltage drops below 4 V, turning off Q1 and producing a SET voltage as determined by R4 and R5. For this condition, the IC begins to regulate, creating an output of 2.4 V (0.6 V/cell) and a SET voltage of 1.2 V. Thus, low output voltage causes the product to enter its standby mode without discharging the NiCd batteries below 1 V/cell.

Load current for normal operation are about 100 mA peak, so the 1-Ω on-resistance yields only 10 mW of power dissipation. Heat sinking isn't required for this application.

Simple Class D Amplifier Is A Real Audio Workhorse

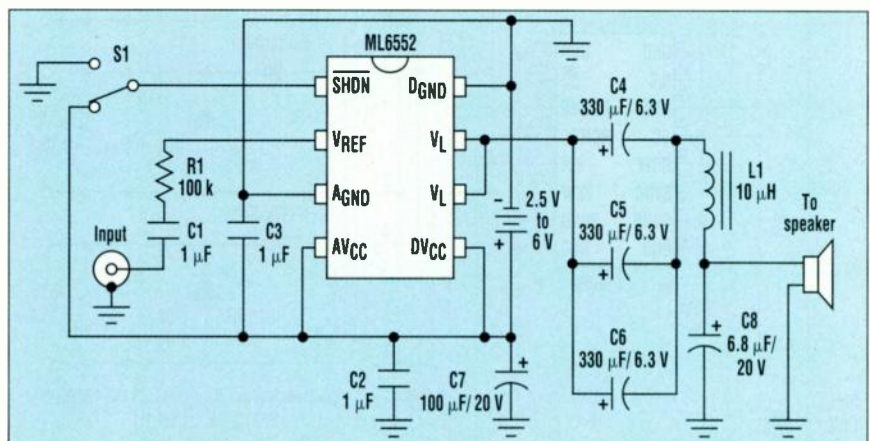
DAN NORMAN, Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; (408) 433-5200; fax (408) 432-0295.

Sometimes an IC designed for one purpose can be used very efficiently in an entirely different way. The ML6552 is such an IC. Originally designed for use as a high-speed active bus termination, the part makes an efficient audio amplifier with adequate sound quality. Basically a switching regulator, the device was designed to convert voltage supplies into a desired output or termination voltage. However, because it can source and sink current, the IC can be easily converted into a Class D amplifier by superimposing the input signal onto the internal reference.

The ML6552 operates over a V_{CC} range of 2.5 V to 6 V, which is compati-

ble with most common power-supply and battery voltages. Ten external components (most surface-mountable), are all that are needed to produce a very-efficient, low-cost amplifier (see the figure).

Switch S1 puts the circuit to sleep. Under that condition, only 20 μA of current flows. As far as performance is concerned, the upper and lower 3-dB points are below 20 Hz and above 30 kHz, respectively. With a 5-V supply,



All it takes is a handful of external components to turn this active-bus-termination IC into a Class D audio amplifier suitable for driving small speakers. Note that the audio input is superimposed onto the internal reference.

the efficiency is 54.8%. Total harmonic distortion is 0.8%. Also, there is a clear separation of the audio channel from

the 588-kHz switching frequency. Inductor L1 is a Sumida CD75-100K. Since the ML6552 can source or sink 1

A, the major limitation of this circuit is the power-handling ability of small loudspeakers.

A Novel Approach To Designing Low-Power Isolated Supplies

KURK MATHEWS, *Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7417; (408) 432-1900; fax (408) 434-0507; Internet: <http://www.linear-tech.com>.*

The last thing a digital or even an analog designer wants to worry about is the power supply. Oftentimes, size, efficiency, and input requirements dictate the use of a complex switching power supply, which exacerbates the situation. When voltage isolation is added to this list, visions of custom transformers, optocouplers, and noise send all but the most experienced designers scrambling in search of expensive power modules. Fortunately, recent advances aimed at low-power appli-

cations offer many advantages over traditional methods of obtaining isolated feedback.

The most popular method of isolated feedback relies on the optocoupler operating in the linear region. The advantages of this method include excellent output regulation and the ability to adjust output voltage from the secondary. The disadvantages include parts count, variable gain (due to current-transfer ratio), variable bandwidth, and common-mode transient susceptibility. The

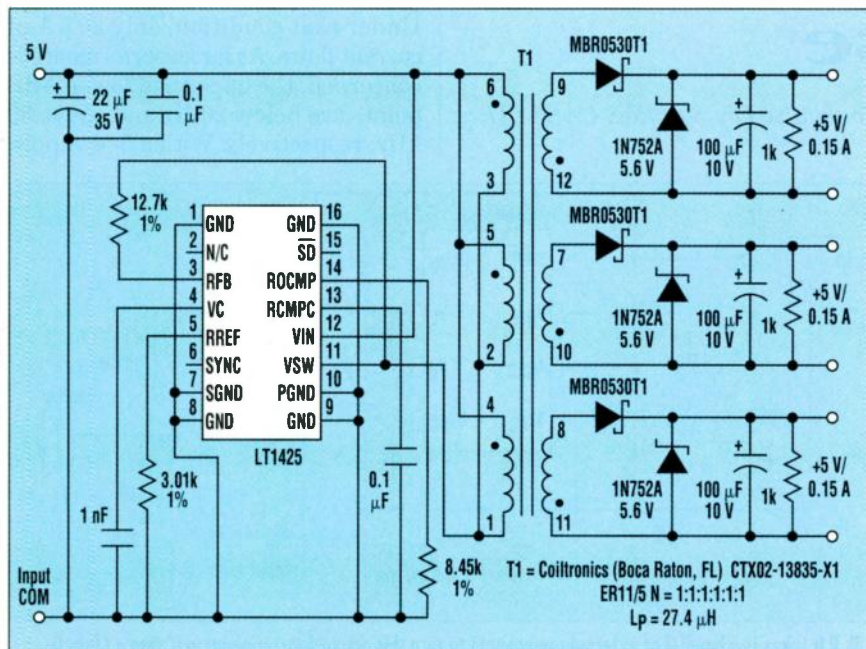
current-transfer ratio is the ratio of output current to input current that varies from unit to unit, with drive level, and with temperature. It also degrades with time. These factors must be given careful design consideration to guarantee performance throughout the life of the product.

Another approach relies on an isolated flyback converter with a low-voltage auxiliary winding added to the transformer. During a portion of the main switch's off-time, the auxiliary winding's instantaneous voltage is proportional to the output voltage. This voltage is peak-rectified to become the feedback and bias voltage. This approach eliminates the optocoupler and secondary reference at the expense of an extra winding, poor output voltage regulation, and slow response. The main drawback of this method of feedback involves the sampling technique. The average value of feedback voltage varies with input voltage, and with load in the case of discontinuous mode, when the transformer's energy is fully exhausted during each cycle.

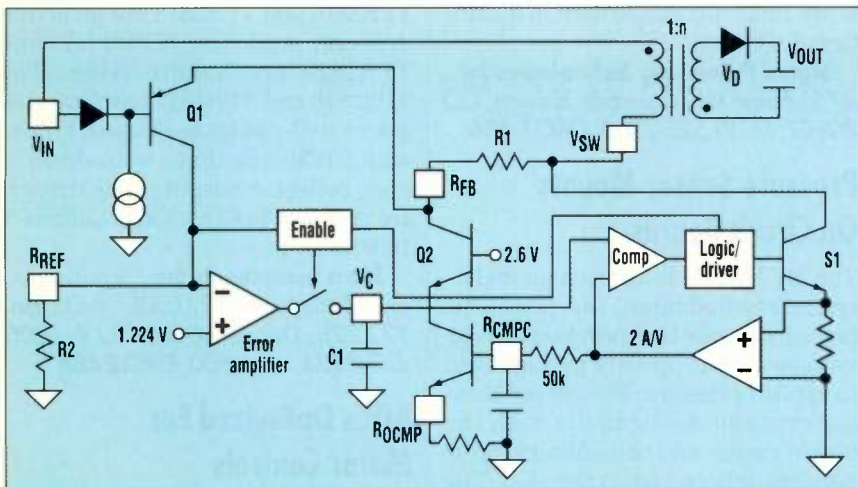
A new switching regulator, the LT1425, overcomes many of the issues previously associated with isolated feedback. The schematic in Figure 1 depicts a triple 5-V isolated supply for RS-232, RS-485, or similar circuits. Load regulation is better than $\pm 2\%$. Worst-case cross-regulation (one output unloaded and the others fully loaded) adds another $\pm 5\%$ error. Note that cross-regulation error results from nonideal components and is relatively independent of the feedback method used. Zener diodes were added to clamp unloaded outputs in the event of a short on an adjacent winding.

The secret to well regulated output voltage without using optocouplers is careful sampling. During a portion of S1's off-time (Fig. 2), a feedback current approximately equal to:

$$(V_{OUT} + V_D)/(n \times R1)$$



1 Using an LT1425 switching regulator, this triple 5-V isolated supply for RS-232, RS-485, or similar circuits features a load regulation better than $\pm 2\%$.



2 Neither optocouplers or an additional transformer winding are needed to achieve isolated feedback with the LT1425. Instead, the feedback current is generated through R1 during a portion of S1's off time.

is generated through R1. Q1 causes the same amount of current flow into R2, where it's converted to a voltage and compared to a 1.2-V reference by a transconductance (error) amplifier.

The output of the error amplifier is connected to C1 during the time when the feedback current is valid (after the leakage inductance spike and before S1 turns on or the primary

voltage collapses, in the case of discontinuous mode). An additional current, proportional to the average switch current, is subtracted from the feedback current (via Q2) to compensate for transformer, diode, and output capacitor parasitics over load. As a result, typical load regulation is improved over previous methods to better than $\pm 3\%$ over line and load. Isolation voltage is limited only by the transformer.

To minimize external component size, the LT1425 operates at a nominal 275-kHz switching frequency and may be synchronized from 320 kHz to 450 kHz. In this design, 275 kHz was chosen to avoid harmonics near the 455-kHz IF used in telecommunications equipment. A number of manufacturers provide off-the-shelf, surface-mount transformers with 500 V of winding-to-winding isolation. The LT1425 operates from 3 to 29 V and draws only 7 mA of quiescent current (20 μ A in shutdown mode).

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ANALOG PRODUCTS

FRED Diode Family Adds Muscle To Its Lineup

Advanced Power Technology has increased the breakdown voltage rating of its Fast Recovery Epitaxial Diode (FRED) family to 1200 V to get faster recovery times while maintaining soft-recovery characteristics and low forward voltage. This improved performance allows converter circuits to operate at higher voltages or provides added voltage margins when the diode is used in off-line applications susceptible to damaging line surges.

Forward-current rating is 60 A and maximum forward voltage is 2.5 V. Typical reverse-recovery characteristics at 60-A forward current are 70 ns at 25°C and 130 ns at 150°C. Maximum reverse recovery current is 30 A at 25°C and 40 A at 150°C with a forward current of 60 A and a recovery rate-of-change of 480 A/μs.

The FRED diode family is available as a single diode in a TO-247 package (APT60D120B) and as a dual parallel configuration in an SOT-227 package (APT2X61D120J). Target applications include antiparallel diodes, free-wheeling diodes, and snubber diodes in switch-mode power supplies, inverters, converters, UPSs, and motor controls. Small-volume pricing ranges from \$10.00 to \$30.00 each. ML

Advanced Power Technology, 405 S.W. Columbia St., Bend, OR 97702; (541) 382-8028. CIRCLE 485

Track-And-Hold Amplifier Samples At 125 Msamples/s

Serving as the front end for analog-to-digital converters (ADCs) lacking track-and-hold functions, the SPT9101 track-and-hold amplifier samples analog inputs at up to 125 Msamples/s with an 8- to 12-bit resolution. Trim-programmable internal hold and compensation capacitors provide an input bandwidth of 350 MHz and enhance slew rate versus noise performance. Acquisition time is 7 ns, and minimum aperture jitter is less than 1 ps. The SPT9109 operates with ±5-V inputs and delivers a continuous 60-mA output current. Package options are 20-lead SIOC and LCC. Both packages are available in the industrial temper-

ature range for \$29.30 each in quantities of 100. ML

Signal Processing Technologies Inc., 4755 Forge Rd., Colorado Springs, CO 80907; (719) 528-2300. CIRCLE 486

Pressure Sensor Mounts On Circuit Boards

The MPXT2010 is a silicon piezoelectric, stress-isolated, top-piston-fit pressure sensor that provides a linear voltage output directly proportional to applied pressure. The sensor housing contains a silicon die with the strain gauge and thin-film resistor network integrated on the chip. The sensor is laser-trimmed for precise span and offset. Full-scale span calibration is 25 mV for 0 to 10 kPa (0 to 1.45 psi), and temperature compensation is effective over the range of 0 to +85°C. Within the 8-pin sensor housing, a silicone gel isolates the die surface and wire bonds from the environment, while applying the pressure signal to the silicon diaphragm. Maximum output linearity is ±1.0%. The sensor typically operates on a 1-V supply and draws 6 mA. Output voltage is ratiometric to the supply voltage. Unit pricing is \$10.40 in quantities of 10,000, with production quantities requiring a four-week lead time. In addition, devices can be shipped in tape-and-reel and rail forms for automated assembly. ML

Motorola Inc., P.O. Box 179927, Denver, CO 80217; (602) 244-3381. CIRCLE 487

SOT-23 MOSFETs Drive Large Loads

MOSFET drivers in SOT-23 packages are rated to drive large loads, such as those in motor-drive, power-supply, and automotive applications. The TPS2816, TPS2817, TPS2818, and TPS2819 are single-channel MOSFETs that provide up to 2-A peak currents while driving capacitive loads, minimizing shoot-through currents and consuming just a 50-μA supply current. An on-board linear regulator extends the 4- to 14-V normal operating range up to 40 V. Maximum rise and fall time is 20 ns, and maximum propagation delay is 30 ns. The

TPS2816 and TPS2818 are inverting drivers, and the TPS2817 and TPS2819 are noninverting. The TPS2816 and TPS2817 have internal active pull-ups on the inputs for use with PWMs that have open-drain or open collector outputs. The drivers are priced at \$0.64 each in quantities of 1000 units. ML

Texas Instruments Inc., Semiconductor Group, SC-97033, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500. CIRCLE 488

ADCs Optimized For Motor Controls

A family of simultaneous-sampling analog-to-digital converters (ADCs) from Analog Devices are suited for motor-control systems and other applications requiring synchronous sampling and signal conversion. The AD7862 is a 256-ksample/s, dual 12-bit ADC, and the AD7863 is a pin-compatible 200-ksample/s dual 14-bit device.

Both parts contain a pair of successive-approximation ADCs, two track-and-hold amplifiers, an internal 2.5-V reference, and a high-speed parallel interface for connecting to microprocessors, microcontrollers, and digital signal processors. Also included are two-channel multiplexers for each internal ADC for vector motor control. When controlling a three-phase motor, for example, one pair of inputs can monitor instantaneous current in two of three phases to determine field position, while the other pair monitors the voltage of two phases to obtain rotor information.

The AD7862 and AD7863 have maximum conversion times of 3.6 and 4.5 μs, respectively, and are available in 28-pin SOP, DIP, and SSOP packages. Operating on a 5-V supply, typical power consumption is 60 mW for the AD7862 and 75 mW for the AD7863. Specified for the standard industrial temperature range, versions are offered with inputs of ±10 V, ±2.5 V, and unipolar 0 to 2.3 V. For 1000-piece quantities, the AD7862 and AD7863 are priced at \$11.00 and \$16.00, respectively. ML

Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887; (617) 937-1428. CIRCLE 489

ANALOG PRODUCTS

**14-Bit Sampling ADC
Runs At 20 MHz**

The ET2473 is a true 14-bit sampling analog-to-digital converter (ADC) that runs at 20 MHz for demanding applications such as radar, data acquisition, imaging, and test instrumentation. Performance at near-Nyquist frequencies provides a spurious-free dynamic range of 93 dB. Other key specifications include a 79-dB signal-to-noise ratio, signal-to-noise plus distortion of 86 dB, and a differential nonlinearity of ± 0.5 LSB. Housed in a 2.5-by-2.5-by-0.375-in. shielded metal case, the ET2473 TTL-compatible device requires no external components. Its 6.8-W power consumption requires no external heat sink. Unit pricing is \$2200 in lots of 100, with small-quantity delivery available from stock to four weeks. ML

Edge Technology Inc., 40 Salem St., Lynnfield, MA 01940; (617) 246-3800 or (617) 245-3888; Internet: <http://www.edge-technology.com>. **CIRCLE 490**

**Sampling ADC Features
On-Board FIFO**

The ADS-931 16-bit analog-to-digital converter offers 10-MHz sampling with guaranteed no missing codes over the military temperature range (-55 to $+125^{\circ}\text{C}$). Consuming just 1.85 W from a single ± 5 -V supply, the ADC is intended for high-speed, high-resolution, signal-processing applications such as medical imaging, radar, sonar, CCD imaging, analytical instrumentation, and digital communications.

Key characteristics in the frequency domain are -89 -dB THD, -89 -dB peak harmonics, and 83-dB SINAD. For the time domain, the device has a 87-dB SNR, ± 0.5 LSB differential nonlinearity, and 60- μV rms noise. An on-board, 16-bit-wide, 16-word-deep FIFO facilitates post-processing of output data by digital signal processors and CPUs. Simultaneous read and write operations minimize the number of interrupt cycles sent to the host processor. The analog input is ± 2.75 V.

Housed in a 40-pin ceramic TDIP, the ADS-931 requires only the rising edge of a start-convert pulse to initiate its conversion process. Unit pricing for lots of 100 units is \$397 for the commercial

temperature range and \$497 for the military temperature range. Production quantities are available in six weeks. ML

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000. **CIRCLE 491**

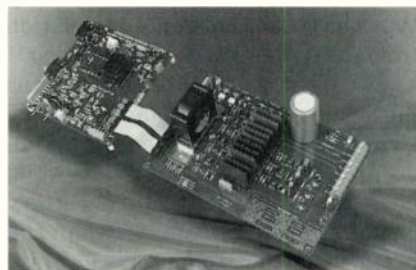
**Power Rectifier Has
Soft Reverse Recovery**

Motorola's MSR860 power rectifier is a free-wheeling diode for use in variable-speed motor controls and switching power supplies. Coupled with the company's E-Series IGBT products, the diode provides solutions for a range of home-appliance applications. Supplied in a TO-220 package, the MSR860 has a 150°C operating junction temperature, low forward voltage, and low leakage current. Peak repetitive reverse voltage is 600 V, average rectified forward current is 8 A, and peak repetitive forward current is 16 A. Other available package types are D-PAK, SMC for surface-mount applications, and 3A axial-lead type. Unit pricing in quantities of 50,000 is \$0.45. Lead time for production quantities is 8 to 12 weeks. ML

Motorola Inc., P.O. Box 17927, Denver CO 80217; (303) 675-2140 or (800) 441-2447. **CIRCLE 492**

**Toolset Simplifies
Motor Drive Design**

A two-piece toolset from Motorola for developing ac and dc motor drives consists of a digital motion-control board and an IGBT power-stage board. Containing the MC68HC708MP16 8-bit



microcontroller, the ITC137 motion-control board provides all basic motor-control functions, such as on/off, forward/reverse, and speed control. A serial port allows changing motor-control parameters real time from a PC.

The 8-MHz CPU has two timer-interface modules (four-channel and two-

channel) with input capture; output compare; an 8-bit, 10-channel ADC; and a 6-channel, 12-bit pulse-width modulator. The PWM features programmable frequency and polarity, center or edge alignment, dead-time generation and compensation, distortion correction, hardware fault pins, and 20-mA sink capability. Also included are SCI, SPI, low-voltage reset, a crystal or ceramic resonator, and 37 bidirectional I/O lines. Packaged as part of a kit (KITC137/D), the ITC137 comes coded with a basic turnkey program, which also is supplied on a diskette.

Also packaged as a kit, the ITC132 power-stage board provides a direct interface between microcomputer-based controllers and brush-dc, brushless-dc, and ac induction motors. It accepts six logic inputs that control three IGBT half-bridge outputs. The board also provides current-sense, temperature-sense, and bus-voltage feedback terminals. The two boards can work independently or together, requiring only a power supply and motor for a complete motor-drive system. Pricing for each board kit is \$375 per unit. ML

Motorola Inc., Customer Response Center, 423 N. 44th St., Suite 100, Phoenix, AZ 85008; 800-521-6274. **CIRCLE 493**

**Audio Amplifier Drives
Computer Speakers**

A stereo audio amplifier from Texas Instruments can drive headphones and small unpowered speakers in notebook computers, desktop computers, and consumer audio products. The TPA302 delivers 250 mW of continuous average power into an 8- Ω load with less than 0.06% THD+N from a 5-V power supply. Gain is externally set by two resistors per channel and doesn't require compensation for setting from 1 to 10. Features include a shutdown function for power-sensitive applications as well as thermal and short-circuit protection. For driving 32- Ω loads in headphone applications, the amplifier delivers 60 mW of continuous average power. Furnished in an 8-pin SOIC package, the TPA302 goes for \$1.19 each in lots of 1000. ML

Texas Instruments Inc., Semiconductor Group, SC-97034, P.O. Box 172228, Denver, CO 80217; 800-477-8924, ext. 4500. **CIRCLE 494**

ANALOG PRODUCTS

Controller Chip Ties Multiple Cards To ISA Bus

The NM95MS18 controller chip allows several circuit cards to share a single interrupt channel in ISA-Bus systems.



**Plug-n-Play
Solution for
ISA-Bus
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tems. The controller also supports non-plug-and-play platforms such as Windows NT, DOS, Windows 3.1, Unix, and Novell. The controller is ideal for add-in cards like SCSI controllers, network controllers, fax modems, sound cards, serial/parallel cards, video cards, and I/O controllers.

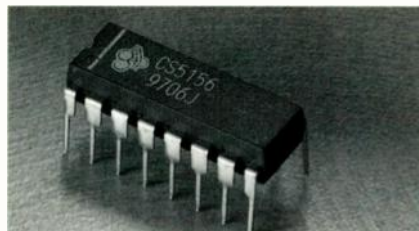
Two configurable types, TTL O/P and open-drain O/P, are supported to allow sharing of the interrupt channel in open-drain mode. One logical device is supported to enable a choice of direct memory access, interrupt, and I/O address-decoding features. An on-chip write-protected EEPROM provides 2 kbits for plug-and-play resource data and 2 kbits for 31 power-on legacy configurations. The controller operates in DMA or extended interrupt mode, and supports PC-97 requirements. Available in a 52-pin PLCC package, the NM95MS18 is priced at \$4.50 in quantities of 1000, with a lead time of 6 weeks ARO.

Fairchild Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (800) 272-9959.

CIRCLE 495

Buck Controller With 5-Bit DAC Powers Pentium Processors

The CS-5156, a nonsynchronous buck controller that includes a 5-bit digital-to-analog converter (DAC), generates operating voltages for various Pentium II processors and their associated core logic circuits. The chip's fast (100-ns response time) feedback loop



requires no external compensation. The slow loop needs a 0.1- μ F capacitor for compensation and system stability. Built-in protection features include programmable soft start and lossless short-circuit protection. The controller operates on supply voltages from 4 to 20 V, with 12 V powering the controller and 5 V powering the processor and core logic. Peak output current is 1.5 A, and operating frequency is over 1 MHz. Package options are 16-lead plastic DIP or plastic surface-mount narrow-body. Pricing is \$2.10 each in quantities of 10,000. ML

Cherry Semiconductor Corp., 2000 South County Trail, East Greenwich, RI 02818-1530; (401) 885-3600.

CIRCLE 496

Battery Disconnect Switch Integrates Level Shifter

The Si4720CY from Temic Semiconductors integrates p-channel power MOSFETs and level-shifting circuitry for switching NiCd and NiMH batteries, and lithium-ion cells in the power supplies of portable computers and instruments. The device provides the reverse-blocking capability needed by power supplies using multiple battery types or those that require isolation from the power bus during charging.

Two p-channel MOSFETs serve as high-side switches to allow battery switching to be controlled from a microprocessor. The two switches can be used separately to control battery charging or to switch between the battery and an ac adapter. They also can be used with Schottky diodes to provide reverse blocking when switching between two battery packs. With an on-resistance of 20 m Ω per MOSFET, the Si4720CY handles up to 6 A of continuous current. Two independent inputs allow 6- to 30-V operation. Off-state current is 1 μ A. Packaged in an SO-16 housing,

the switch sells for \$1.95 each in quantities of 100,000. Production quantities require an 8- to 10-week lead time. ML

Temic Semiconductors, 2201 Laurelwood Rd., Santa Clara, CA 95056-0951; (408) 567-8220. **CIRCLE 497**

Read-Channel Device Handles 375 Mbits/s

The latest EPR4 (Enhanced Partial Response Type 4) read channel increases the speed capability of hard-disk-drive read channels by discriminating error-free data at 375 Mbits/s



while operating at 4 V, one volt below its rated supply voltage. The 32P4105 read channel's front end features a five-tap least-mean-square FIR filter with an eight-state Viterbi detector for data discrimination. The device operates at 280 Mbits/s from a 5-V supply, and provides a growth path to 500 Mbits/s over the next few years.

Other members of the EPR4 family include the 200-Mbit/s 32P4101 and the 240-Mbit/s 32P4103. All versions are drop-in replacements of popular PR4 chips, and also offer SNR improvements of over 2.0 dB at a User Density of 2.5. This translates to 20% gain in linear bit density. Other features include a monitor that tracks channel margins based on Viterbi data, and keeps a running log of drive performance. A real-time adaptive facility with autocalibration accommodates MR head asymmetries, and thermal asperity detection and correction maintains data integrity following head/media contact. Sample pricing for the 32P4105 is set at \$9.95. Sample prices for the 32P4101 and 32P4103 are \$7.95 and \$8.95, respectively. ML

Silicon Systems Inc., 14351 Myford Rd., Tustin, CA 92780-7068; 800-572-0882. **CIRCLE 498**

ANALOG PRODUCTS

Transient Suppressors Guard Sensitive Data Ports

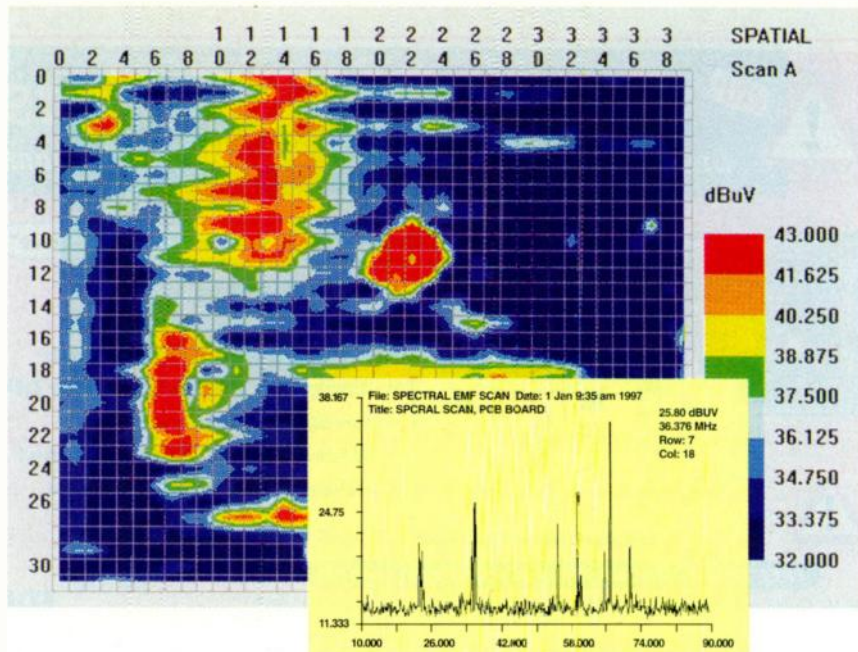
The SLV series of transient-voltage suppressors prevent overvoltages (caused by electrostatic discharge, lightning, and electrical fast transients) from reaching sub-5-V circuits in power, video, and communications ports for portable and video applications. The suppressors comply with the IEC 1000-4 Standard, which applies to products shipped to Europe. The SLV Series provides board-level protection for products used in networking and communications, and peripheral subsystems such as printers, scanners, I/O devices, and test equipment. Suppressors are available with 2.8-V operation and come with up to four bidirectional lines (SLVDA) in an SO-8 package. Single unidirectional (SLVU and SLVG) and bidirectional protection also are available in SMT packages. In 1000-unit quantities, the single-line SLVU2.8 costs \$0.62 each and the 4-line SLVDA2.8 costs \$3.26 each. The SLVG and SLVE are similarly priced to the SLVU. ML

Semtech Corp., 652 Mitchell Rd, Newbury Park, CA 91320-2111; (805) 498-2111; fax (805) 498-3804. **CIRCLE 499**

Analog-To-Digital Converter Handles Transducer Signals

The AD7730 is a complete front end for weigh-scale and pressure-measurement applications. Low-level signals from a transducer are fed to a programmable-gain stage, followed by a low-pass programmable digital filter that adjusts filter cutoff, output rate, and settling time. The output is a serial digital word. Two buffered differential programmable-gain analog inputs are provided along with a differential reference input. Operating from a single +5-V power supply, the AD7730 has four unipolar and bipolar analog input ranges between 0 V and 80 mV. Peak-to-peak resolution is 230,000 counts. The serial interface can be configured for three-wire operation and is compatible with microcontrollers and digital signal processors. Package options are 224-pin plastic DIP, SOIC, and TSSOP. ML

Analog Devices Inc., One Technology Way, Norwood, MA 02062-9106; (617) 329-4700. **CIRCLE 500**



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BURR-BROWN	80-90	33
DATel INC	94	Cov2
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MAXIM INTEGRATED	101-102	35
MAXIM INTEGRATED	103-104	37
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MINI-CIRCUITS	112-113	13
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TANNER RESEARCH INC.	120	64
TEXAS INSTRUMENTS	126	9
UNITRODE INTEGRATED	121	Cov3
VERIBEST INCORPORATE	122	23

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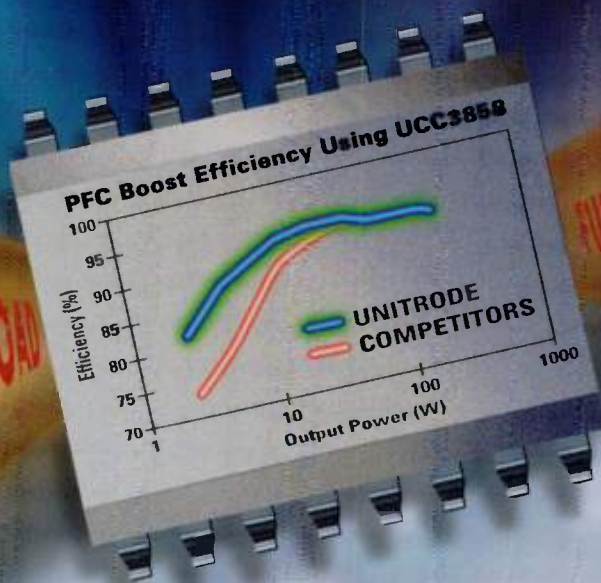
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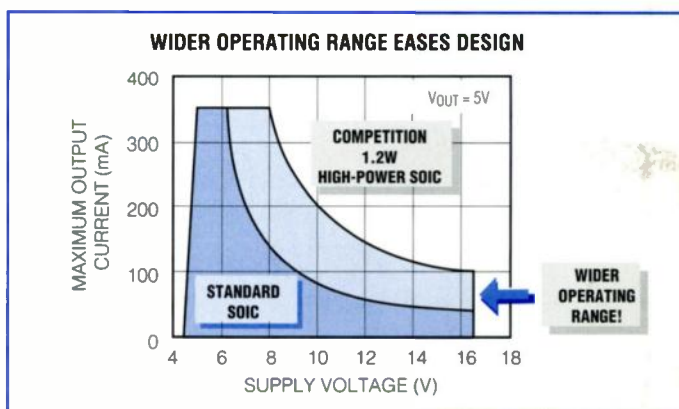
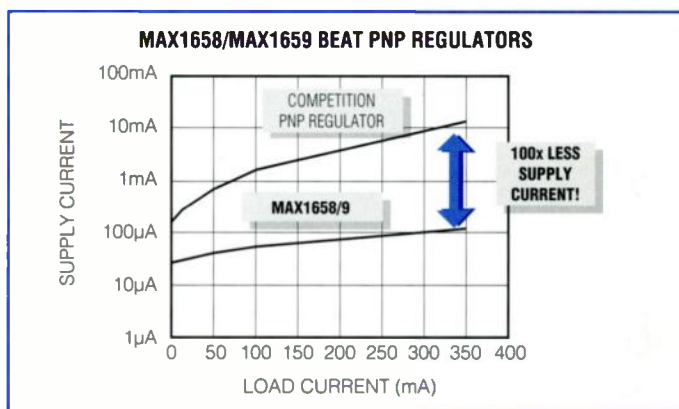
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