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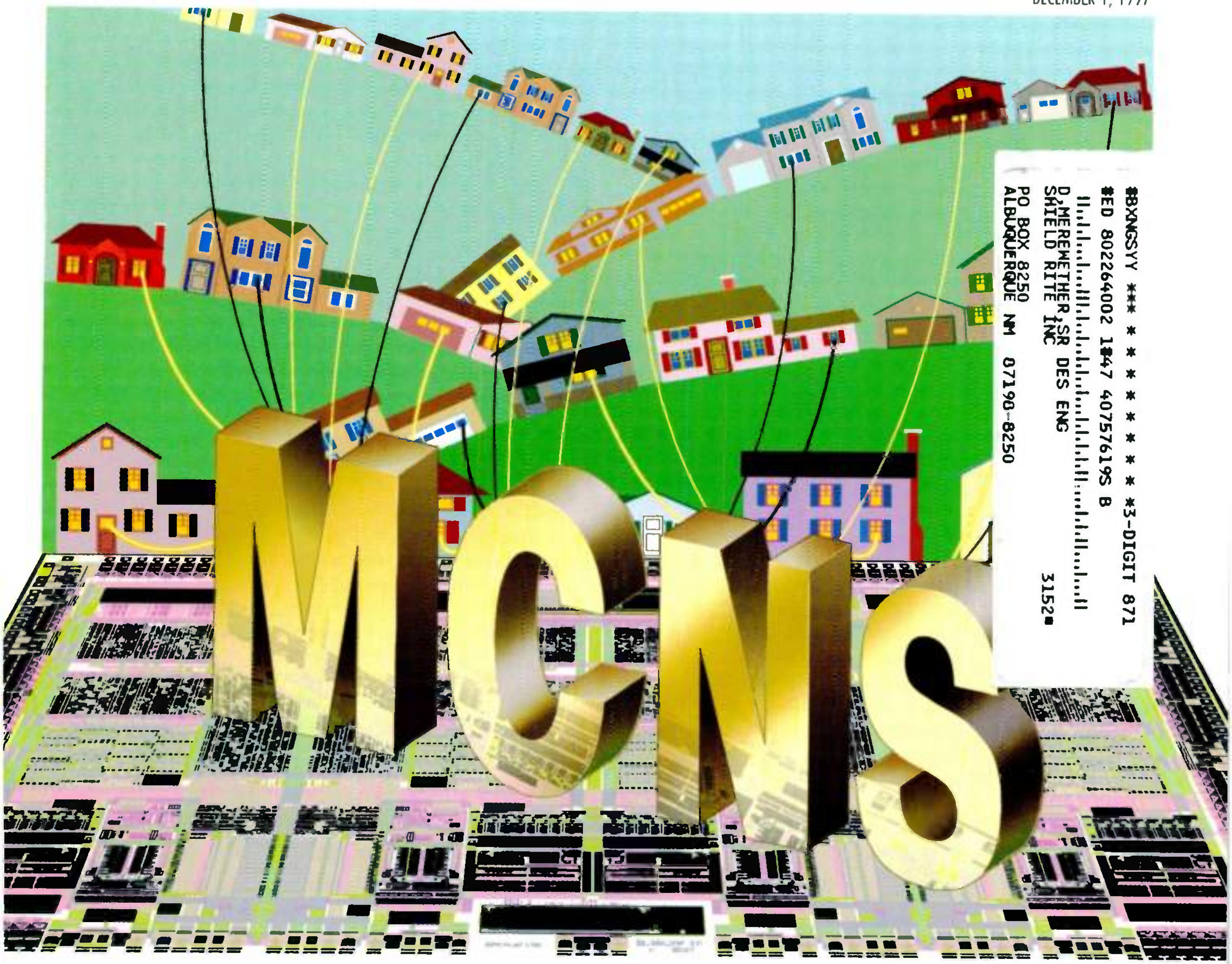

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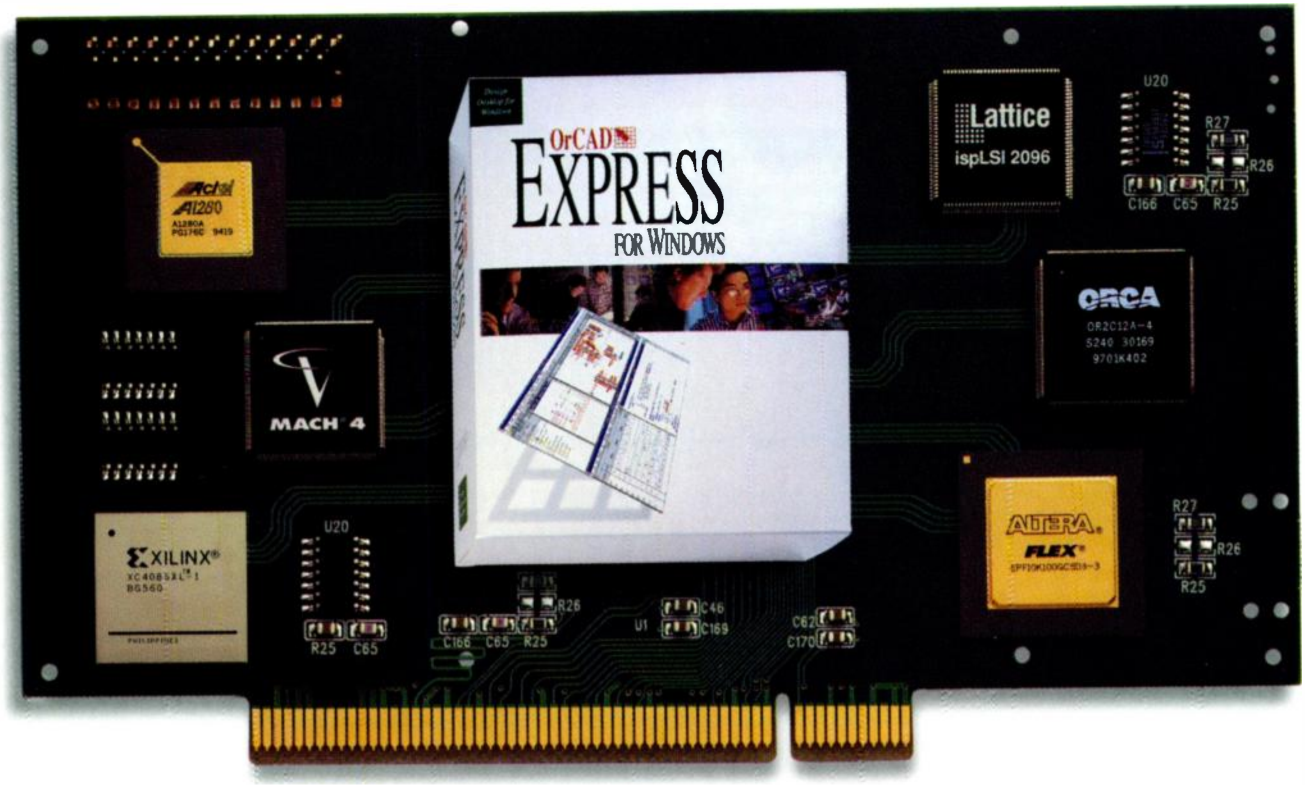

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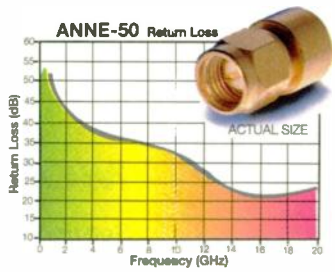

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December 1, 1997 Volume 45, Number 27

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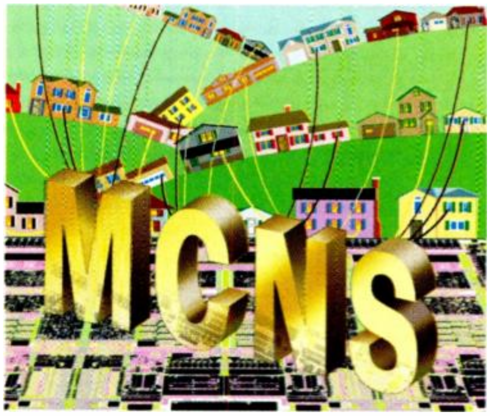

TECH INSIGHTS

TECH INSIGHTS

COMMUNICATIONS TECHNOLOGY

COVER STORY

DEPARTMENTS

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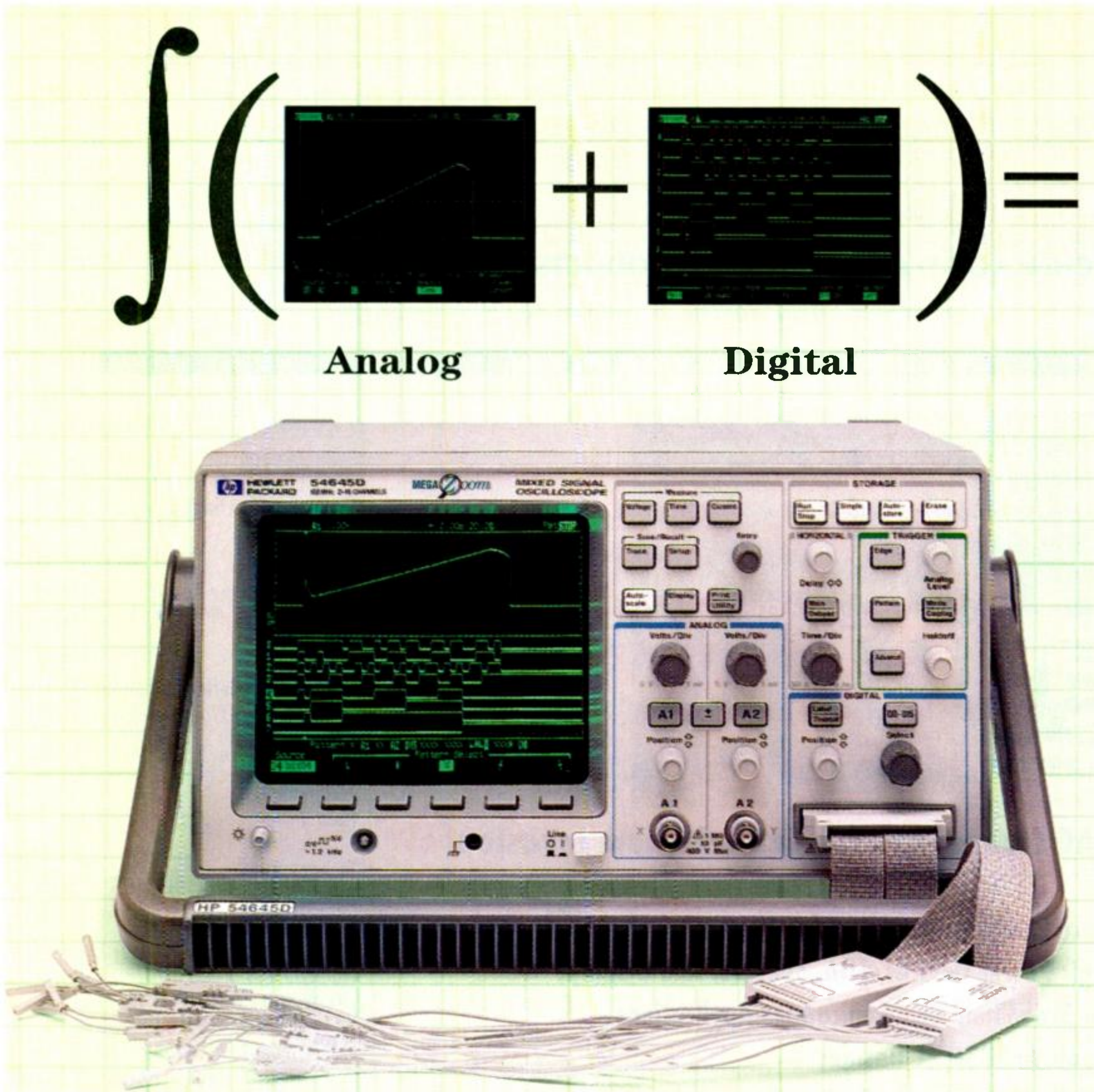

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December 1, 1997 Volume 45, Number 27

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1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

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JANUARY 1998

Seventh Joint Magnetism & Magnetic Materials Conference (INTEMAG), January 6-9. Hyatt Regency Embarcadero Hotel, San Francisco, California. Contact John Nyenhuis, School of ECE, Purdue Univ., West Lafayette, Indiana 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: smag@ecn.purdue.edu.

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Photonics West, Jan. 24-30. San Jose, CA. Contact The SPIE Exhibits Dept., P.O.Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, TX. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, FL. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, FL 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY 1998

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

Portable by Design, February 9-13. Santa Clara Convention Center, Santa Clara, California. Contact Rich Nass, Electronic Design, 611 Route 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6090; fax (201) 393-0204; e-mail: portable@class.org.

The Wireless Symposium and Exhibition, February 9-13. Santa Clara Convention Center, Santa Clara, California. Contact Bill Rutledge, Penton Publishing, 611 Rte. 46 West, Hasbrouck Heights, New Jersey 07604; (201) 393-6259; fax (201) 393-6297; instant faxback (800) 561-7469; Internet: http://www.penton.com/wireless.

Asia-South Pacific DAC (ASP-DAC '98) and EDA TechnoFair (EDATF), Feb. 10-13. Pacifico Yokohama Convention Center, Yokohama, Japan. Contact ASP-DAC '98 Secretariat, c/o Convex Inc., Ichijoji Bldg., 2-3-22 Azabudai, Minato-ku, Tokyo, 106 Japan; +81 3-3589-3355; fax +81 3-3589-3974; e-mail: convex@po.iijnet.or.jp.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), February 15-19. The Disneyland Hotel, Anaheim, California. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., #300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

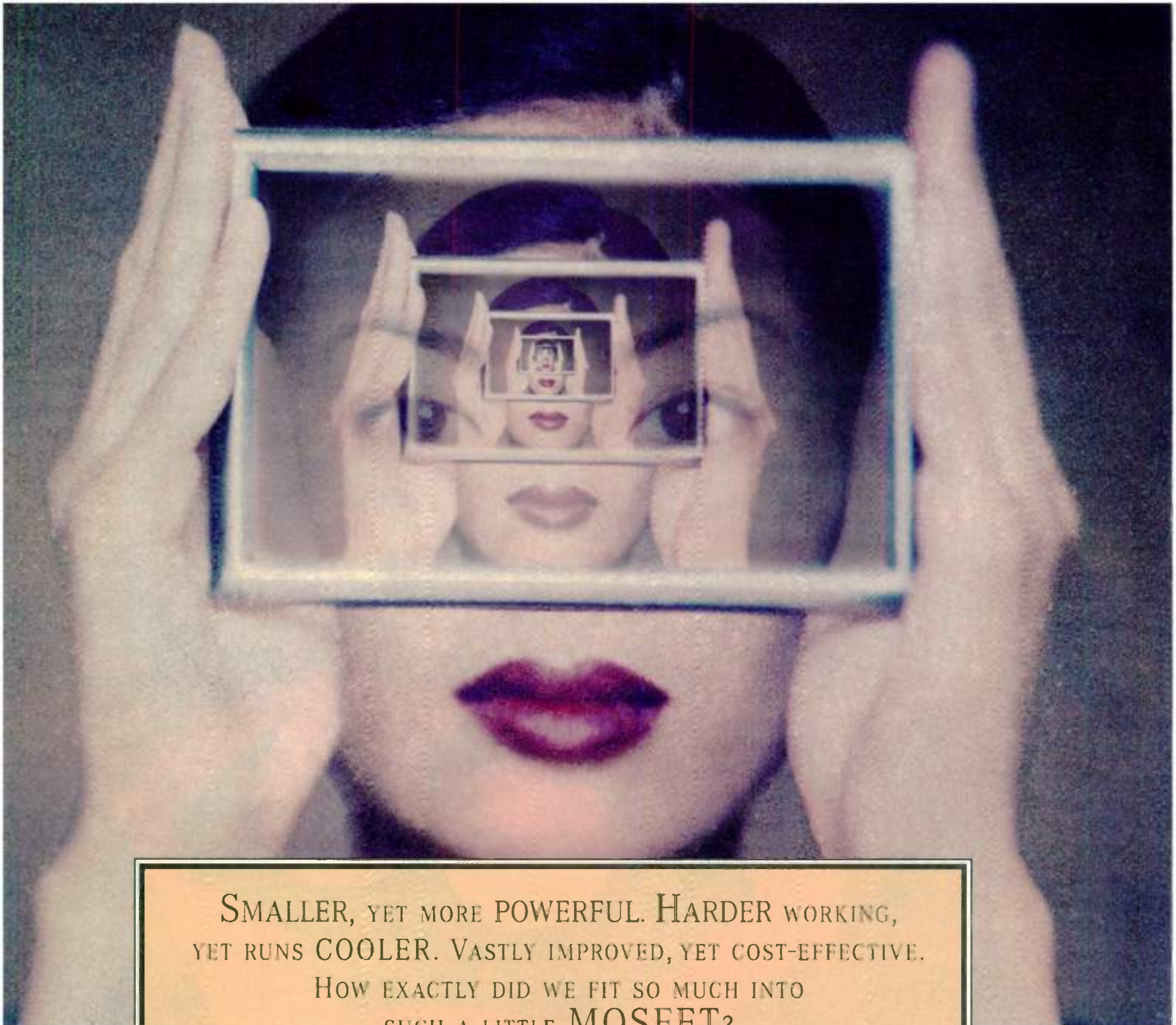
Conference on Optical Fiber Communication (OFC '98), February 22-27. San Jose Convention Center, San Jose, California. Contact Lisa Myers, OSA Conference Services, 2010 Massachusetts Ave., N.W., Washington, D.C. 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: ofc.info@osa.org.

Design, Automation, and Test in Europe Conference and Exhibition (DATE '98), Feb 23-26. Le Palais des Congres de Paris, Porte Maillot. Contact European Conferences, 11C Wemyss Pl., Edinburgh EH3 6DH, UK; +44 131-225-2892; fax +44 131-225-2925.

38th Israel Conference on Aerospace Sciences, February 25-26. Tel-Aviv and Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH 1998

Computer Telephony Conference and Exposition '98, March 3-5. Los Angeles Convention Center, Los Angeles, California. Contact Computer Telephony '98, 1265 Industrial Highway, Southampton, Pennsylvania 18966; (215) 355-2886; fax (215) 355-4112.



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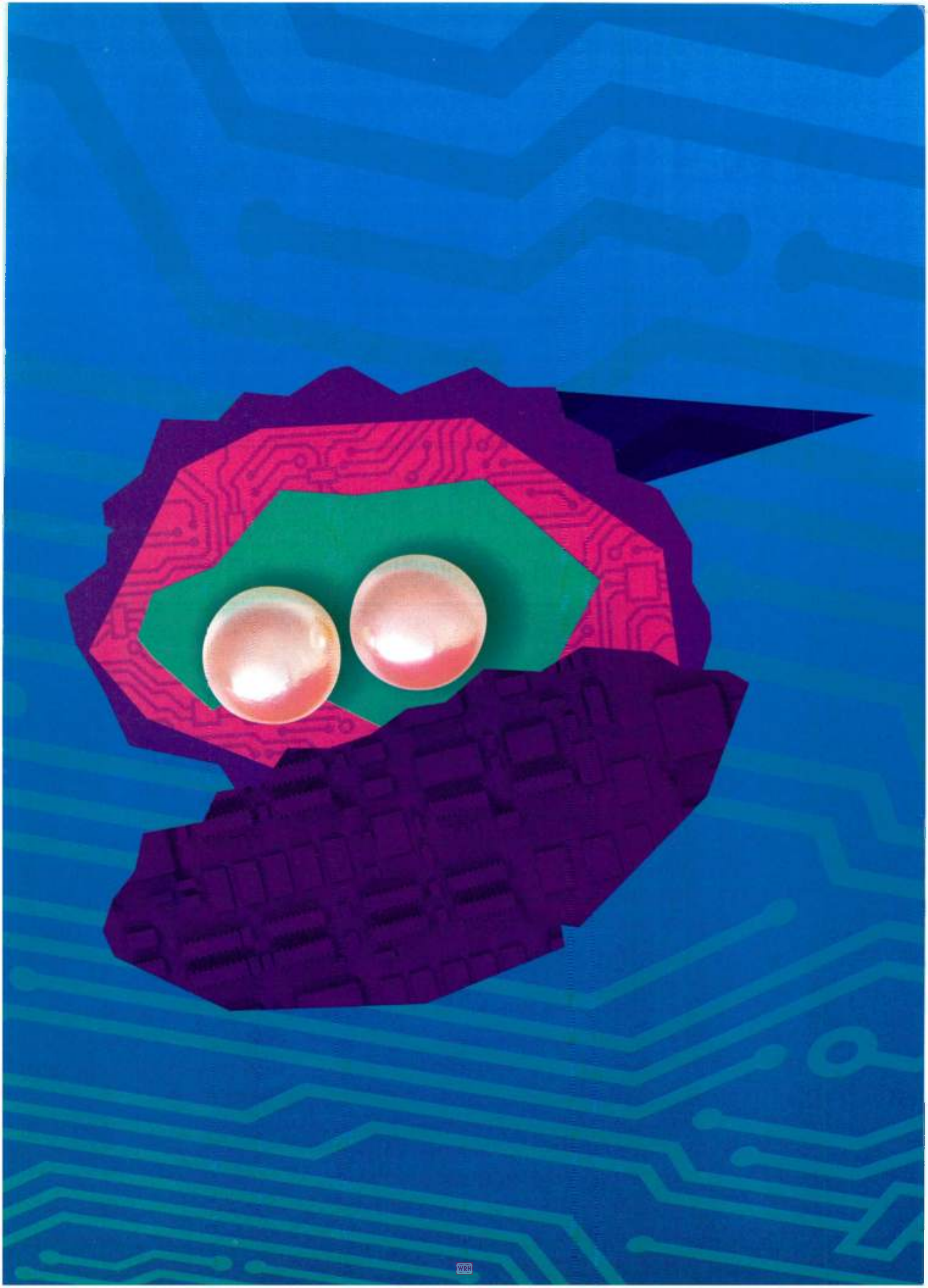


MARCH 1998

International Verilog Converfence and VHDL International User Forum (IVC/VIUF), March 16-19. Santa Clara Convention Center, Santa Clara, California. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, Colorado 80301; (303) 530-4562; fax (303) 530-4334; e-mail: lee@mpa-net.com; Internet: http://www.hdl-con.org.

IEEE Aerospace Conference, Mar. 21-28. Snowmass Confernce Center, Snowmass, CO. Contact Mike Johnson, 2225 Roscomare Road, Los Angeles, CA 90077-2222; (310) 472-8019; e-mail: johnson@ee.ucla.edu.

Second Intellectual Property in Electronics Seminar (IP '98), Mar. 23-24. Westin Hotel, Santa Clara, CA. Contact John Whitaker, Miller Freeman Technical Ltd., +44 181-316-3297; e-mail: ed98@cityscape.co.uk.

INFOCOM '98, March 28-April 2. Hotel Nikko, San Francisco, California. Contact Ramesh Nagarajan, Lucent Technologies, 101 Crawford Corner Road, Rm. 3M-318, Holmdel, New Jersey 07933; (732) 949-2761; fax (732) 834-5906; e-mail: rameshn@lucent.com.

IEEE International Reliability Physics Symposium, March 30-April 2. Reno Hilton Hotel, Reno, Nevada. Contact Ann N. Campbell, M/S 1081, Sandia National Labs., Post Office Box 5800, Albuquerque, New Mexico 87185-1081; (505) 844-7452; fax (505) 844-2991; e-mail: ancampbe@sandia.gov.

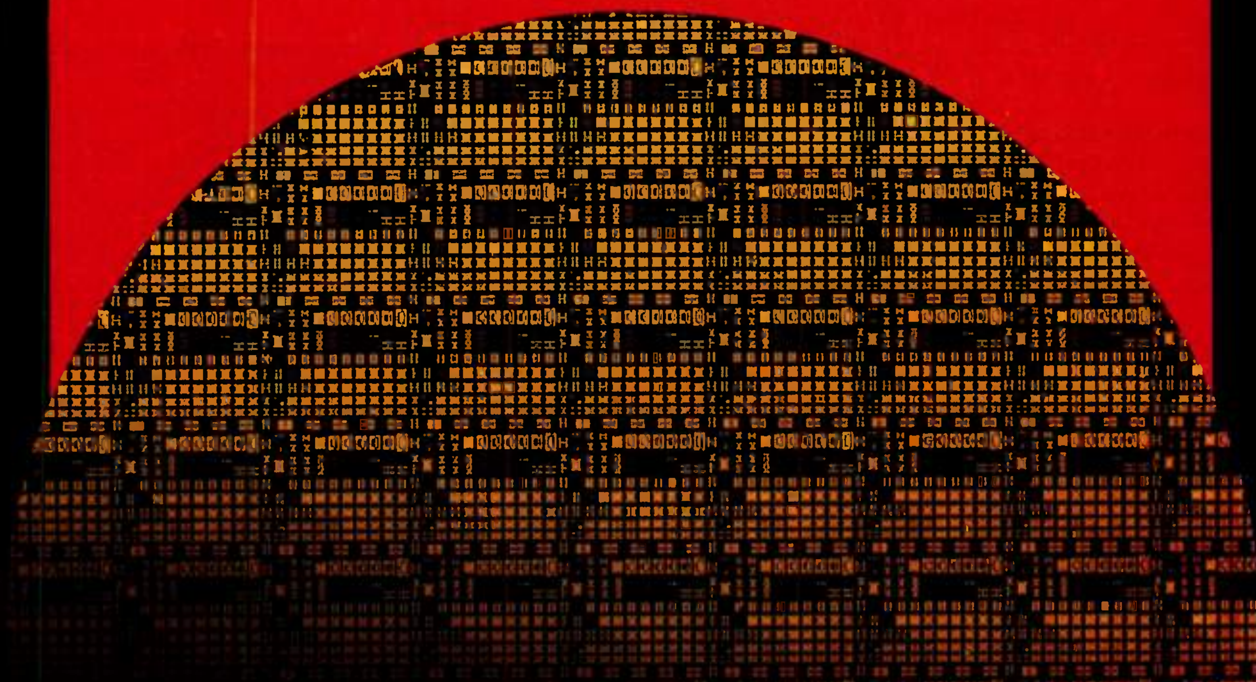
IEEE International Parallel Processing Symposium/IEEE 9th Symposium on Parallel and Distributed Processing (IPPS/SPDP), Mar. 30-Apr. 3. Delta Orlando Resort, Orlando, FL. Contact Viktor Prasanna, EEB-200C, Department of EE Systems, University of Southern California, Los Angeles, CA 90089-2562; (213) 740-4483; fax (213) 740-4418; e-mail: prasann@ganges.usc.edu.

Sixth Annual Embebbed Systems Conference East, Mar. 31-Apr. 2. Chicago's Navy Pier Festival Hall, Chicago, IL. Contact Miller Freeman Inc., 600 Harrison St., San Francisco, California 94107; (415) 905-2354; fax (415) 905-2220; Internet: http://www.embedsyscon.com/.

APRIL 1998

20th IEEE International Conference on Software Engineering, Apr. 19-25. Kyoto International. Conference Hall, Kyoto, Japan. Contact Koji Torii, Graduate School of Information Sciences, Nara Institute of Science & Technology, 8916-5 Takayama-cho, Ikoma-shi, Nara-ken 630-01, Japan; +81 7437-2-5310; fax +81 7437-2-5319; e-mail: torii@is.aist-nara.ac.jp.

Southeastcon '98, Apr. 24-26. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.



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16th IEEE VLSI Test Symposium, Apr. 26-30. Hyatt Regency Monterey, Monterey, CA. Contact Rob Roy, Intel Corp., MS:JFT-102, 5300 Elam Young Pkwy., Hillsboro, OR 97124-6497; (503) 264-3738; fax (503) 264-9359; e-mail: robroy@ichips.intel.com.

IPC Printed Circuits Expo '98, Apr. 26-30. Long Beach Convention Center, Long Beach, CA. Contact Dan Green, The Institute for Interconnection & Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847) 509-9700 ext. 371; fax (847) 509-9798.

MAY 1998

Conference on Lasers & Electo-Optics & The International Electronics Conference (CLEO/IEC), May 3-8. The Moscone Center, San Francisco, CA. Contact Amy Hutto, OSA Conference Services, 2010 Massachusetts Ave. N.W., Washington, DC 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: cleo. info@osa.org.

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE Radar Conference, May 12-14. Contact Scott Ramey, 2501 West University, MS 8056, McKinney, TX 75070; (972) 952-4409; fax (972) 952-3071; e-mail: sramey@ti.com.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE (FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

IEEE International Conference on Robotics and Automation, May 16-21. Katholieki Universiteit, Leuven, Belgium. Contact Georges Giralt, LAAS-CNRS, Toulouse, France, +33 61-33-63-48; fax +33 61-33-64-55; e-mail: giralt@laas.fr.

IEEE Power Electronics, Specialist Conference (PESC '98), May 17-22. Sea Hawk Hotel & Resort, Fukuoka, Japan. Contact Tsutomu Ogata, NTT Integrated Information & Energy Systems Labs., Midori-cho, Musashino, 180 Japan; +81 422-59-2350; fax +81 422-59-2347; e-mail: ogata@ilab.ntt.jp

IEEE Vehicular Technology Conference (VTC), May 18-21. Westin Hotel, Ottawa, Ontario, Canada. Contact Tara Hennessy, Industry Canada, 300 Slater St., Ottawa, Ontario, K1A OC8, Canada; (613) 990-4711; fax (613) 952-5108; e-mail: hennessytara@ic.gc.ca.

48th IEEE Electronic Components & Technology Conference (ECTC '98), May 25-28. Sheraton Hotel & Towers, Seattle, WA. Contact Components Group, EIA, 2500 Wilson Blvd., Arlington, VA 22201; (703) 907-7536; fax (703) 907-7501; e-mail: judya@eia.org.

IEEE International Symposium on Circuits and Systems (ISCAS '98), May 31-June 03. Monterey Conference Center,Monterey, California. Contact Sherif Michael, Department of Electrical and Computer Engineering, Naval Postgraduate School, Monterey, California 93943; (408) 656-2252; fax (408) 656-2760; e-mail: michael@ece.nps.navy.mil.

JUNE 1998

International Conference on Consumer Electronics (ICCE), June 2-4. Los Angeles Airport Marriott, Los Angeles, California. Contact Diane Williams, Conference Coordinator, 67 Raspberry Patch Drive, Rochester, New York 14612-2868; (716) 392-3862; fax (716) 392-4397,e-mail: d.williams@ieee.org; Internet: http://www.icce.org.

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., Post Office Box 1521, MS 3T15, Baltimore, Maryland 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JULY 1998

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, Washington. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Drive, Seabrook, Texas 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel and Marina, San Diego, California. Contact Terry Snow, San Diego Gas and Electric, Post Office Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, California. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

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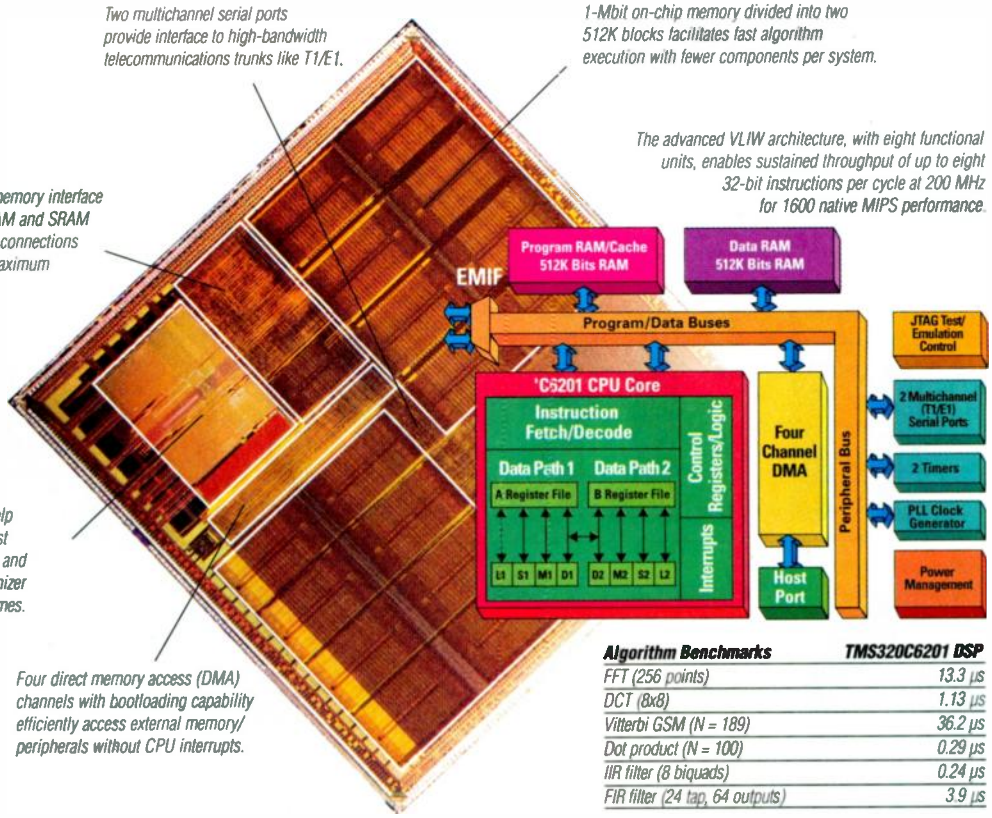
1-Mbit on-chip memory divided into two 512K blocks facilitates fast algorithm execution with fewer components per system.

The advanced VLIW architecture, with eight functional units, enables sustained throughput of up to eight 32-bit instructions per cycle at 200 MHz for 1600 native MIPS performance.

32-bit glueless external memory interface supports SDRAM, SBSRAM and SRAM and provides high-speed connections to external memory for maximum sustained performance.

RISC-like instructions help enable the industry's most efficient DSP C compiler and first DSP assembly optimizer for faster development times.

Four direct memory access (DMA) channels with bootloading capability efficiently access external memory/ peripherals without CPU interrupts.



Algorithm Benchmarks	TMS320C6201 DSP
FFT (256 points)	13.3 µs
DCT (8x8)	1.13 µs
Viterbi GSM (N = 189)	36.2 µs
Dot product (N = 100)	0.29 µs
IIR filter (8 biquads)	0.24 µs
FIR filter (24 tap, 64 outputs)	3.9 µs

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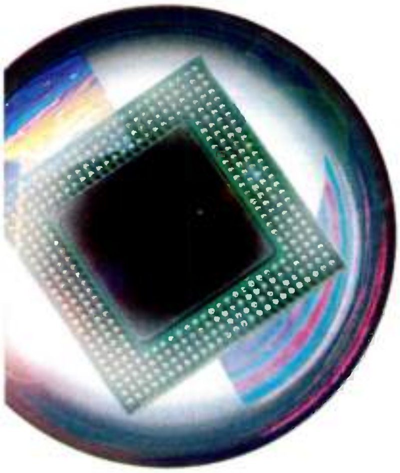

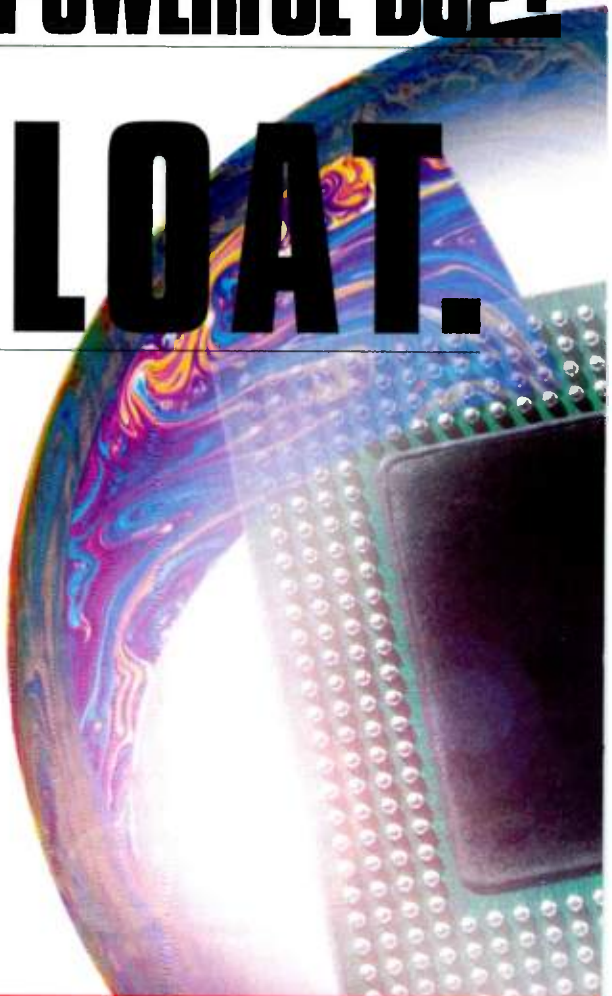

THE WORLD LEADER IN

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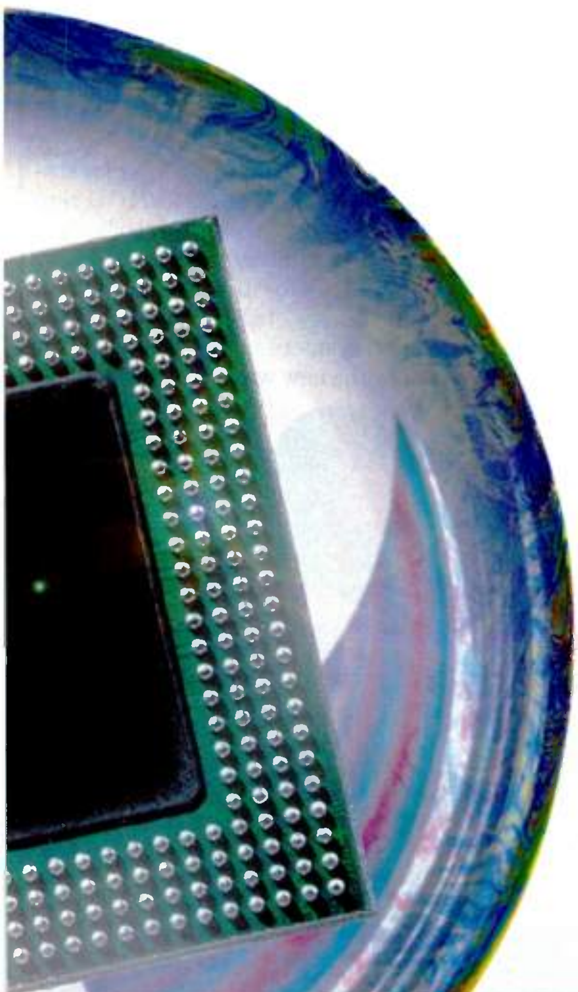
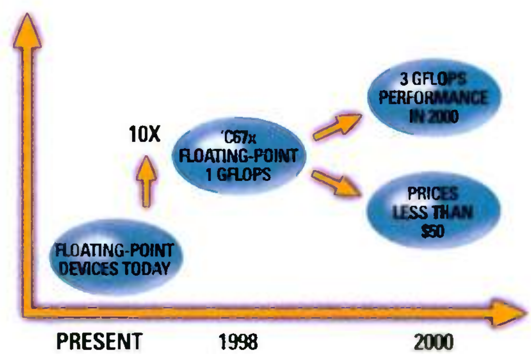
One GFLOPS performance is coming, and it's closer than you think – thanks to floating-point DSP technology from Texas Instruments. When the first of these new floating-point DSPs begins sampling in the second half of 1998, the TMS320C67x will be the world's most powerful 32-bit floating-point DSP. With 1 GFLOPS (1 billion floating-point operations per second) performance, the 'C67x will provide 10 times the processing power of any other floating-point DSP on the market.





And for the first time ever, fixed and floating-point DSPs will be code compatible. As a member of the 'C6x generation of DSPs from TI, the 'C67x will be code compatible with the 16-bit fixed-point 'C62x DSPs. Which means you can start developing code for the 'C67x immediately, using currently available 'C6x fixed-point tools.

So, if you're looking for the world's most powerful floating-point DSP, look no further than Texas Instruments – the world leader in DSP Solutions.

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14-7368

DSP SOLUTIONS

TEXAS INSTRUMENTS

Tiny Engines Fuel A Revolution

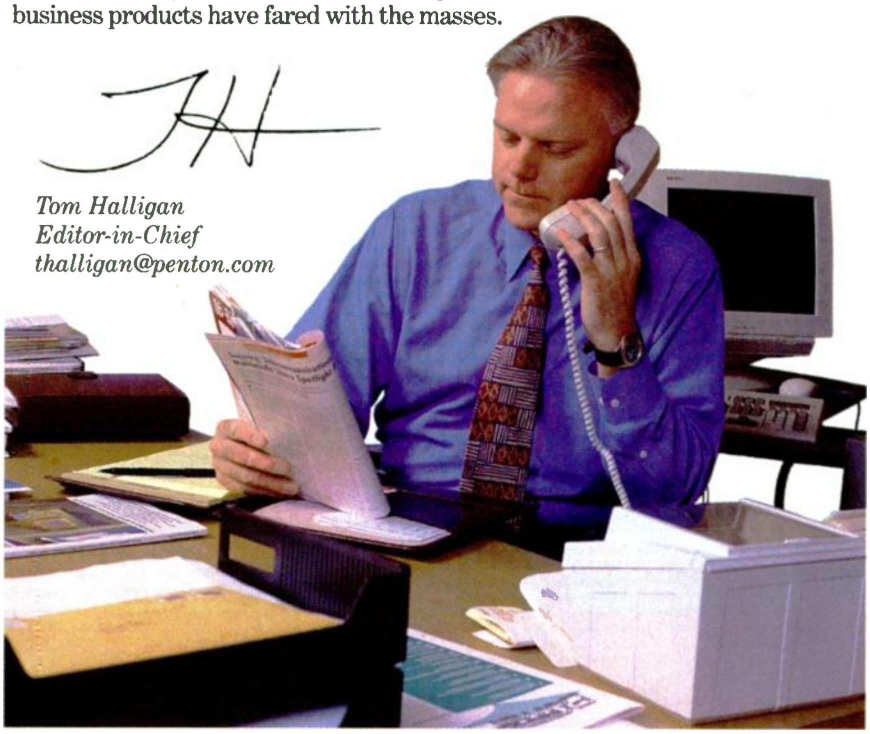
A semiconductor analyst from Frost & Sullivan says that embedded controllers "have quite simply become the miniature engines of the modern technological revolution." Another analyst from Dataquest predicts that "a single microcomponent design-win in a next-generation consumer product can generate huge volumes and revenue for a semiconductor company."

Obviously, the industry watchdogs are very high on embedded controllers, which are defined as either a microprocessor (MPU) or microcontroller (MCU) used in an embedded application. The market, according to Frost & Sullivan, for 16-, 32-, and 64-bit MPU and MCU embedded controllers is predicted to grow by 50% in 1997 and continue on to top 150 million units by 2001. The 4-bit MCU market is on the decline because embedded system designers are moving up to the 8-bit MCU to provide more intelligence in products such as computer mice and personal pagers.

What's fueling MPU/MCU shipments is consumer demand for more intelligence in everything ranging from toys to global positioning satellite systems (GPS). The 16-bit MCU can provide greater intelligence and can handle digital technologies to improve the capabilities of cell-phones, video disks, and other consumer and business products.

The high-growth market segments, according to the industry analysts, are the 32- and 64-bit embedded controllers, with the 64-bit segment seeing the latest growth, with an annual compound growth rate of 53%. Besides the ever-present digital video games, other products such as watches with GPS capability, web browsers, servers, and telephone-switching equipment have all contributed to the growth of the 32-bit embedded controller industry. On the other hand, the market analysts say that the highest demand is in the 64-bit MPU segment. Due to the success of the Nintendo 64 and the Sony Playstation, the MIPS architecture captured nearly 33% of the 1996 MPU/MCU chip unit market share in next-generation consumer systems, with a total of nearly 17 million chip shipments, according to Dataquest. Nintendo Corporation by itself has consumed in excess of 1 million 64-bit MPUs for its 64 Game System.

Even with a volatile stock market, with its constant twists and turns, consumer confidence is still high, albeit cautious. It will be very interesting to see after all of the post-holiday numbers are crunched just how the new wave of consumer and business products have fared with the masses.



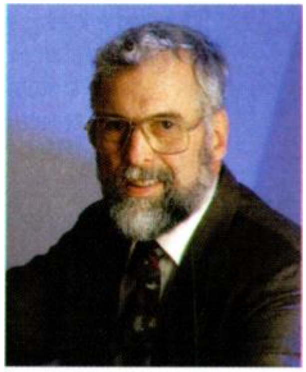
Tom Halligan
Editor-in-Chief
thalligan@penton.com

Consumer Electronics' Potential

I've been subjected to a deluge of literature and perhaps just a little bit more hype in recent months about the wonders of using digital signal processors (DSPs) in consumer audio and video equipment. The quality of sound that can be achieved is truly amazing. Some systems can even replicate the acoustics of actual historical concert halls and opera houses. The possibilities appear to be limitless, and I should be feeling truly inspired with wonder and great hope for the future of consumer audio. Instead, I'm doing a slow burn.

It's not about features that may or may not be available in a given piece of equipment. That's a choice that consumers must make based on their own budgets and good old-fashioned shopping. On the contrary; my burn is being fueled by a computer industry view of products that are taking on much of the power offered by digital technology, but still sticking it to the customer in terms of upgrading equipment. Given the technical sophistication available to the consumer audio industry and the rapid development of new standards, we computer-oriented types expect to be able to upgrade our systems with new software and perhaps minimal additions in hardware. That just isn't happening.

Some time back I settled in to watch a recent laser disk release on my big-screen home theater with Dolby Pro-Logic surroundsound—you can picture the scene. The techno-weenie was happy. At the same time, I idly started to read about a new development called "AC-3 Dolby Digital." Ooh, gotta have that! The fear of being a little behind the technology wave began to loom like a depressing shadow. Ruined the whole movie. Of course, it would all soon be available. And, of course, I'd need a new laser disk player and a new receiver/amplifier. You can almost hear those cash registers making that familiar sound: $$ca-ching$$.



TOM WILLIAMS
EMBEDDED SYSTEMS/SOFTWARE

Now, admittedly, if you're going to move up in raw processor performance, you're going to buy some serious new hardware. But, if you've already got a 200-MHz DSP buried inside a piece of equipment, you should be able to track changes in formats like Pro-Logic, AC-3, THX, DTS, and so on. And you should be able to do it with relatively minor hardware upgrades and new software, not by investing in whole new systems. This is an entirely different issue than not the much-touted combination of the PC with the TV. That would be like grafting the head of a duck onto a toad and expecting it to sing "Aida." This is all about harnessing the vast potential of embedded computer technology.

In fairness to the home entertainment industry, I have to say that such upgrade potential is only now becoming feasible. Expectations always outpace reality and there have been many hardware hurdles to cross. But the oncoming generation of digital versatile disk (DVD) technology should offer a rich enough medium to allow for improvements that are backward-compatible. And, it should have enough capacity to allow it to be a stable medium for a good many years to come. Once high-definition television (HDTV) gets established (if ever) in the consumer marketplace, there should be a solid hardware environment that users can enhance incrementally without having to abandon their investments.

After that, we should expect to be able to upgrade our home entertainment systems through software with perhaps some plug-in modules to support; for instance, the additional channels required by some as yet undreamed-of format. A standard would be nice, but that's too much to hope for. A Sony plug-in module and driver software will not be the same as those from Panasonic, but that's OK. If the home entertainment industry can sculpt its entertainment systems to exploit the capabilities of the embedded computer systems that lie at their hearts, consumers will be happier. Innovations in audio and video experience also will come about faster and in more varieties than ever before possible. *tomwillm@ix.netcom.com.*

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Speedpass Revolutionizes The Purchase Of Gasoline

Introduced to major metropolitan areas last month, the Mobil Speedpass car tag will enable customers to fill-up and drive out of a service station without ever opening their wallets or purses to get cash or credit cards. The compact Speedpass car tag transponder adheres to a vehicle's rear windshield. The transponder immediately activates the gasoline pump when a driver enrolled in the program stops at a pump equipped with the technology.

Similar to the electronic payment technology used to reduce waiting time at highway tollbooths, Speedpass is a proprietary technology that employs radio-frequency signals. The electronic system located in the pump "talks" with miniature transponders located in the car tag or key tag. Together, these electronic devices provide access to gasoline by automatically charging fuel purchases to a credit card.

The miniature transponders in the tags are small radio-like devices that are preprogrammed with a unique secure ID number. When a customer uses a Speedpass tag at a station equipped with Speedpass technology, the gasoline pump sends out a radio signal that powers the tag, allowing it to send back its unique ID code. Immediately, the Speedpass system recognizes the individual customer and activates the pump. The system contacts Mobil's centralized credit department to verify current credit information, and then charges the customer's designated credit card (customers can designate any of the wide range of credit cards accepted by Mobil). The credit card number remains outside the Speedpass signal system to maintain confidentiality.

The technology for Speedpass was developed for Mobil in cooperation with Texas Instruments TIRIS (Texas Instruments Registration and Identification System). TIRIS is an advanced radio-frequency identification (RFID) technology that controls, detects, and tracks valuable objects as well as people. For more information, call (703) 849-5520. RE

Environmental Protection Drives Emissions Reduction Effort

Perfluorocompounds (PFCs) often are used and generated during semiconductor manufacturing operations such as chemical-vapor-deposition-chamber cleaning and the plasma etch of materials such as nitride, oxide, and polysilicon. Unfortunately, the semiconductor industry's reliance on PFCs has increased significantly in recent years. These chemicals now are suspected of contributing to the harmful effects of global warming.

To combat this trend, a number of members within the semiconductor industry have voluntarily signed a memorandum of understanding (MOU) with the U.S. Environmental Protection Agency (EPA). Armed with this MOU, they will attempt to find ways to measure, control, and reduce PFC emissions. One such company, American Microsystems Inc. (AMI), Pocatello, Idaho, is seeking to reduce the emissions and replace them with compounds that don't trigger global-warming concerns or other potential adverse effects.

Under the terms of the MOU, over a three year period, AMI will research and determine a strategy for perfluorocompound-emissions reduction. The company also will continue tracking and reporting on emissions of six gases, which include nitrogen trifluoride, sulfur hexafluoride, and others. This data then will be used to optimize internal processes and methods for PFC emission minimization and elimination. In turn, the EPA will develop a clearing-house of information and data on successful strategies for reducing PFC emissions. It also will be responsible for conducting a preliminary assessment of possible substitutes for these products and report on them to the industry. For additional information, contact American Microsystems at (208) 233-4690, or check out the company's web site at *http://www.amis.com*. CA

Power-Supply Specification Allows PC To Sleep

By taking advantage of the Power Supply '98 dual-mode power-supply specification, desktop PC designers can implement the features that are typically associated with notebook personal computers. The specification, developed by Intel Corp., Santa Clara, Calif., has control when the PC is in either the active or sleep mode. It encompasses both the Advanced Configuration and Power Interface (ACPI) and the PCI Power Management and Wired For Management Initiatives.

According to the specification, the PC should be instantly available to users, even when it's powered down. This brings the PC closer to being a true consumer-electronics device. One of the key enabling features is that the power supplies must support the suspend-to-RAM feature. This means that the system stores its context in DRAM and continues to support "wake-up" peripherals. Such peripherals could include a telephone-answering system or a LAN connection. In the standby mode, the total power consumption should be under 15 W. In the sleep state, the consumption should drop to under 5 W.

Power Supply '98 defines new output voltages, called dual outputs, that let the system operate at 5 V in the high-capacity mode and at 3.3 V in the sleep mode. When in standby mode, the supply continues to power the system and logic. More information on the Power Supply '98 specification can be found on the Internet at *http://intel.com/pressroom*. The complete specification can be downloaded at *http://www.developer.intel.com*. RN

"In the MIPS RISC game, it's not whether Philips wins or loses. It's finding new ways to let our partners down gently."

"When our partners get a design win, we all win. When LSI Logic wins, we gloat. But just a little."

I/O Specification Helps Eliminate ISA Bus

The Low Pin Count (LPC) Interface Specification is aimed at handling legacy I/O, with the intent of easing the transition from the 8-MHz ISA bus to the 33-MHz PCI bus. Developed by Intel Corp., Santa Clara, Calif., the specification allows legacy I/O motherboard components, typically integrated in a Super I/O chip, to migrate from the ISA bus to the LPC Interface, while maintaining complete software compatibility. This also will drive OEMs to the next generation of higher performance I/O alternatives, such as USB and IEEE 1394.

The specification permits a three-phase legacy migration. First, on-board ISA-bus legacy I/O peripherals, such as the floppy-disk controller, parallel port, and keyboard controller, will move to the LPC Interface. Nonlegacy functions, such as modems, should transition to USB. The second phase is to remove the internal ISA slots. Internal connections should be made using PCI slots, while "out-of-the-box" peripherals would connect through either USB or 1394. The final phase removes the legacy serial and parallel ports from the PC, also being replaced by USB and 1394.

The LPC Interface specification defines an interface between the core logic chip set and the motherboard legacy I/O functions and describes memory, I/O, and DMA transactions. To help facilitate the move to the ISA-less system, National Semiconductor Corp. has released an LPC-based Super I/O device. The company's PC87360 integrates multiple functions into one IC.

More information on this IC can be found on the Internet at *http://www.national.com*. For the LPC Interface specification, go to: *http://intel.com/pressroom*. The complete specification can be downloaded at the address: *http://www.developer.intel.com*. RN

TIA Standard Addresses PCI Interoperability

A new standard to address the issue of personal-communication-interface (PCI) interoperability was recently published by the Telecommunication Industry Association (TIA), Arlington, Va. Referred to as the TIA/EIA-663 Personal Communications Interface Interoperability standard, it governs the two-way internetworking between fixed and portable radio devices operating in the unlicensed frequency band allocated for personal-communication services.

The standard specifies the essential requirements for monitoring, accessing, and relinquishing a radio-frequency channel and the means by which the specified data structures are modulated onto the channel. It also specifies how the two ends of a radio link become and remain synchronized, as well as the provision of signaling or marker channels; generation and interpretation of digital control; and generation and implementation of digital speech and data.

The standard, which was created by the TIA's TR-41.6 Subcommittee on Wireless User Premises Equipment Systems, is now available. To obtain copies of the document standard, contact Global Engineering Documents at (800) 854-7179, or visit its web site at *http://global.ihs.com*. CA

I/O Architecture Enhances Performance, Adds Slots

The Enhanced I/O Architecture, a next-generation interface for networking peripherals, was recently announced by Hewlett-Packard Co., Palo Alto, Calif. In addition to increasing the bandwidth, the architecture requires less power and employs a smaller form factor than traditional I/O, thereby increasing the number of slots that can be designed into a system. Called EIO, the architecture will be built into HP's next generation of LaserJet printers. Later, it will appear on the company's JetDirect print-server boards. The technology is also a viable communications medium for such devices as disk drives, memory, and coprocessors. EIO is a 32-bit technology that runs across the PCI bus at 33 MHz. This replaces today's 8-bit architecture. More information on EIO can be found on the Internet at *http://www.hp.com*. RN

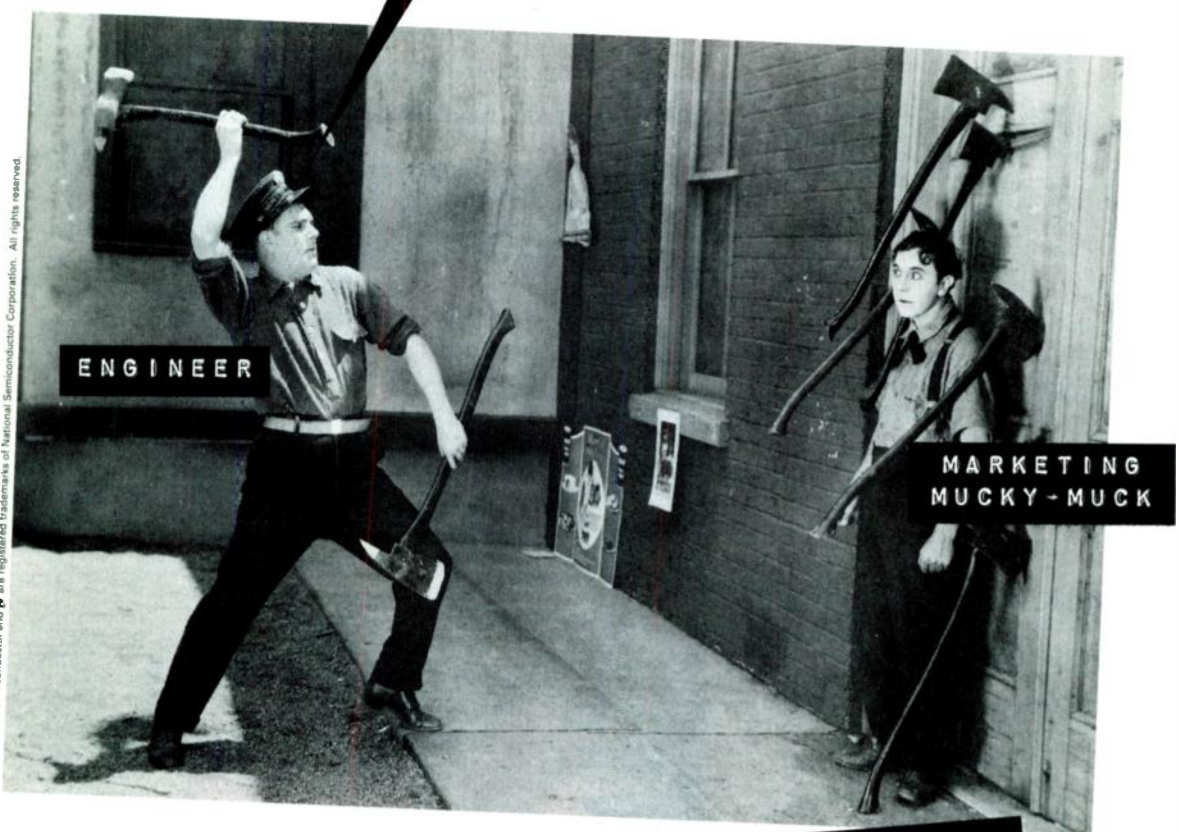
Project Formed To Find IP Voice And Video Solutions

Cable Television Laboratories Inc., Louisville, Colorado, and its members have established a project aimed at identifying and qualifying suppliers and products available for providing telephone calls, videoconferencing, and other packet voice and video services over cable networks and the Internet. The services would be delivered using the Internet Protocol (IP) technology that's used to send data via the Internet.

CableLabs, which is a research and development consortium of cable television system operators representing North America and South America, intends to find a vendor or vendors and work closely with them to develop IP voice and video for consumers within the next nine to 12 months. Once the proof of concept is established, CableLabs will reopen the process to any interested vendors. Because this technology is still in the development stage, this project will not result in an approved list of vendors, nor will there be purchasing recommendations. For more information, call (303) 661-9100; fax (303) 661-9199; or surf into the Internet at: *http://www.cablelabs.com*. RE

Edited by Roger Engelke

"Mess around with
my website, huh?
How 'bout we mess with
your haircut first."



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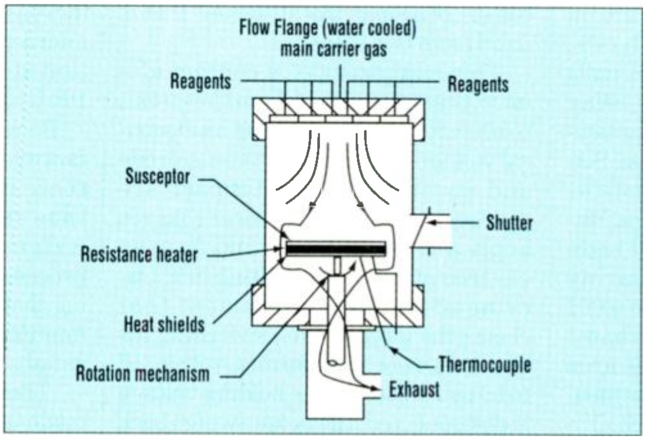
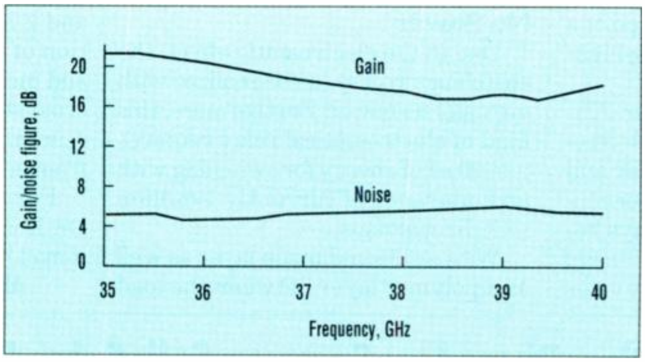
35-GHz 0.5-W GaAs pHEMT Points The Way Toward Low-Cost Volume Production Of MOCVD MMICs

In a collaborative research program with their subcontractor M/A-COM Inc., Lowell, Mass., EMCORE, Somerset, N. J, has developed pseudomorphic HEMT (pHEMT) monolithic microwave and millimeter-wave (MMIC) devices that registered a landmark cutoff frequency of 35 GHz at an output power level of 0.5 W. The device, made of gallium-indium-arsenide (GaInAs), was formulated on a metal-organic chemical-vapor-deposition (MOCVD) epitaxial process. Such performance equates to an estimated 30% reduction in MMIC manufacturing costs.



1. Schematic of the high-speed disk reactor used by EMCORE to make a 35-GHz GaAs pHEMT at 0.5 W of power.



2. Gain and noise figures for a 38-GHz power amplifier MMIC made by EMCORE using a double pHEMT structure.

Until recently, compound-semiconductor epitaxial growth was deemed too expensive to consider for serious device production. However, with the perfection of MOCVD tools and an unprecedented ramp-up in epitaxial foundry services, that image is quickly changing. Unlike silicon epitaxial growth, where multiple pieces of equipment are required, compound semiconductor epitaxial growth requires only one deposition tool to accomplish 90% of the device's design.

The EMCORE development is a breakthrough that surpasses its R&D rival growth method, molecular-beam epitaxy (MBE). MBE continues to dominate the R&D scene where device "tweaking" abounds. However, EMCORE's MOCVD development, which has broken through a barrier in the fabrication of MMIC power devices previously dominated by MBE processes, shows that MOCVD is now a serious choice for volume production of compound-semiconductor devices.

An Enabler

MOCVD is an enabling technology that's behind other cutting-edge device developments. These include blue laser diodes which are a the heart of next-generation CD-ROMs and DVDs. MMICs are the next devices, which are responsible for catapulting GaAs-based compounds into volume production, in turn helping fuel the rise of wireless applications.

Three-Inch Wafers

The pHEMT structures were grown in a standard EMCORE Discovery 180 high-speed, rotating-disk MOCVD reactor system that holds 3-by-76-mm 3-in. wafers per run *(Fig. 1)*. Thulium-gallium (TmGa), tellerium-gallium (TeGa), thullium-aluminum (TmAl), and thullium-indium (TmIn) metalorganic sources are used The hydride (group V) source was 100% arsine (AsH_3) and disilane (Si_2H_6) diluted with hydrogen for the n-type planar doping. The buffer layers were grown using TmGa, and were carefully controlled to give high-resistivity p-typematerial, ensuring low leakage currents. The rest of the layers were grown using the TeGa. Care also was taken to ensure abrupt transitions in composition at the layer interfaces. Spacer layers were AlxGa1-xAs, with x = 0.22, while the pseudomorphic channel layer was InxGa1-xAs, with x = 0.20. The planar-doped layers had target sheet carrier densities of 5 x 10^{12} cm^{-2} for the upper layers and 1 x 10^{12} cm^{-2} for the lower layers.

The Initial work on GaAs-based pHEMTs, preformed under Phase II of an SBIR program, resulted in 38-GHz low-noise-amplifier MMICs with >18 dB gain and a noise figure of less than 4.5 dB *(Fig. 2)*. RF and dc yields were comparable to those obtained with MBE-grown material processed in the same way.

With a further design iteration, the research team feels they can easily obtain 1 W of output power from the 35-GHz pHEMT, and as a result, will yield higher-performance MMICs for roughly two-thirds the cost.

For more information, contact EMCORE Corp., 394 Elizabeth Ave., Somerset, NJ 00873; telephone (732) 271-9090; fax (732) 271-9686; Internet: http://www.emcore.com.

Jo Ann McDonald

Jo Ann McDonald is a journalist and marketing consultant who specializes in emerging technologies. Samples of her on-line newsletters, as published by SEMI, can be accessed over her website: http://legacy-ranch.com. She may be contacted at The Legacy Company, Legacy Ranch in Placid, RR 1, Box 68, Rochelle, TX 76872; (915) 463-5345; fax: (915) 463-5346; e-mail: joann@legacy-ranch.com.

0.1-mm Electrostatic Microrelays Switch At Up To 100 GHz

While normal relays operate on an electromagnetic basis, where an electromagnet pulls or pushes the contacts, a new relay type developed by German scientists works on an electrostatical basis. Scientists at the Fraunhofer-Institut (IFT) for Solid State Technology, Munich, Germany, have developed high-frequency microrelays measuring just 0.1 mm to a side (less than 0.001 in.), taking up an area of less than 1 mm^2. The major portion of this area will be covered with the contacts measuring 0.3 mm by 0.3 mm each. Together with Rohde & Schwarz, also of Munich, a manufacturer of RF measurement devices and systems, they manufactured the first prototype of a microrelay capable of switching high-frequency signals.

As project leader Prof. Dr. Kozlowski of the IFT points out, electrostatical microrelays are smaller and less sensitive to vibrations than conventional electromagnetic relays because they can survive vibrations of more than 6000 g. The new devices consist of a small metal "beam" that is fixed from two sides.

This beam carries a contact element that is insulated from the circuit to be switched. By applying an electrical voltage of about 10 V, the electrode and its flexible counterpart are charged. Contrary electrical charges apply attractive forces and form an electrostatical field resulting in a lowering of the contact element that closes the circuit. This switching action is currently performed within 2.5 to 50 µs As soon as the holding voltage is disconnected, the beam swings back into its startup position and the circuit is open again.

No Power

Due to the electrostatic effect, the switching process can be realized with virtually no power. Furthermore, this kind of electrostatical relay requires just 20 nJ of energy for switching with an endurance of currently 1 million switching actions.

With a silicon-dioxide layer as well as a polymer layer between the load and the control circuit, the galvanic isolation between the load and the control circuit is guaranteed. The maximum load current is about 10 mA, but the IFT scientists intend to increase this current to 50 mA. The micro-relays are suitable for operation at frequencies between dc and 100 GHz.

Because the microrelays are manufactured in a single-layer process, there is no need for extensive (and thus expensive) process steps like wafer or chip bonding. Maximum process temperature is 300°C, meaning that glass, as well as silicon or aluminum dioxide ceramics, can be used as substrates.

The manufacturing technology is made up of conventional semiconductor processes like sputtering, wet and dry etching, as well as plasma-etched chemical-vapor deposition (PECVD), and it allows the additional integration of sensors, electronic elements and mechanical switches within a microsystem. Series production might start in roughly two to three years from now.

For further information, contact Dr. Kozlowski at +49-89/54759-231 or e-mail him at: kozlowsk@ift.fhg.de.

Alfred Vollmer

Development Of Blue Phosphor Spawns Full-Color EL Displays

Color electroluminescent (EL) displays just got a major boost from the development of a stable blue phosphor. Developed by Westaim Corp., Calgary, Alberta, Canada, the phosphor results in an inexpensive multi-use flat-panel display.

Unlike competitive flat-panel display types, such as thin-film EL, the Westaim EL solid-state displays offer a wide viewing angle and can operate under most lighting conditions. This is because the EL display employs a surface-emitting technique, similar to what's used in a CRT. In addition, the EL displays can function in extreme temperatures and operating environments, since they have a high resistance to mechanical shock as well as vibration.

Before the Westaim development, the biggest obstacle to the use of EL displays had been the absence of full, rich colors. Red and green colors were readily available using a manganese-doped zinc-sulphide phosphor, but without the blue component, it was difficult to obtain a white light.

As a result, traditional EL flat-panel displays were mostly limited to those applications that employed monochrome displays. Or, they were relegated for use in industrial settings where the color differentiation was not a high priority issue.

Combining Films

The blue phosphor was developed by combining a conventional thin-film phosphor with a reliable thick-film screen-printing process. The result was the formation of a thick-dielectric electroluminescence (TDEL) film. The TDEL films measure about 20 mm in thickness, compared to the 1 or 2 mm used in conventional thin-film EL displays.

Because the TDEL display is less sensitive to contamination from airborne particles, it can be manufactured in a lower-level (and thus less expensive) clean-room environment. The result is a lower manufacturing cost. The process also reduces capital costs by replacing expensive thin-film deposition equipment with less complex thick-film screen-printing equipment.

Currently, the company is producing displays that measure 5 and 7 in. diagonally, with 14-in. and 17-in.-diagonal models on the way. Westaim claims that the process can produce displays featuring 30-in. diagonals without hitting significant yield problems.

For more information on the TDEL displays, contact Westaim by calling (403) 234-3103, or on the World Wide Web at http://www.westaim.com.

Richard Nass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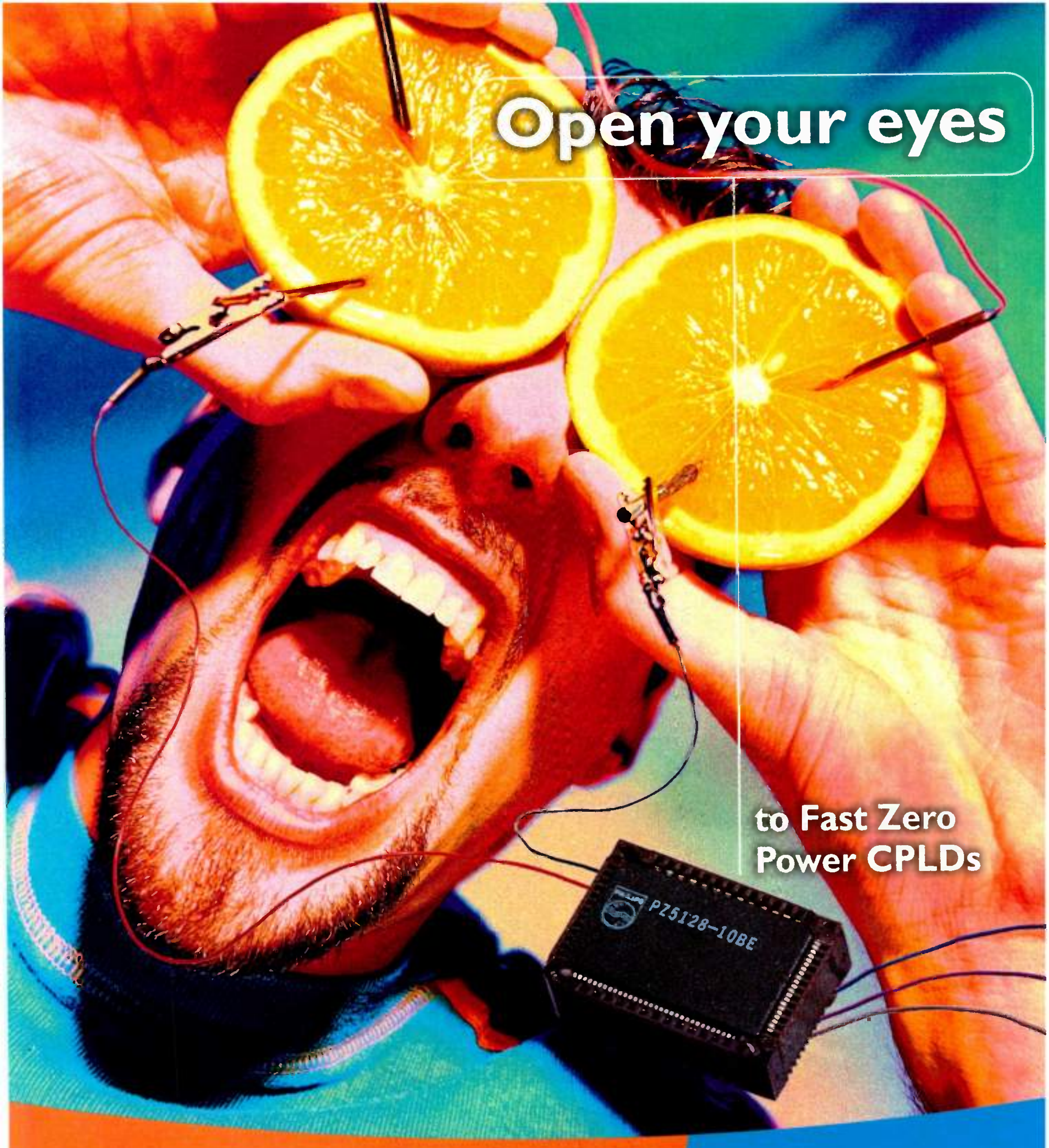
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■ Previewing the latest developments at the 1997 International Electron Devices Meeting

Annual IEDM Conference Examines Leading-Edge Device Developments

Hear About The Latest In Memory And Logic ICs, Compound Semiconductor Devices, Simulation Tools, And Sensors And Displays.

What will the next generation of electron devices look like? For an insight, attend the annual 1997 IEDM at the Washington Hilton and Towers Hotel, Dec. 7-10. Its rich technical program of 36 sessions covers a wide range of electron devices and the processes and tools to make them. These include digital memory and logic circuits, analog and power devices for RF, power and optical applications, the latest device EDA models, and cutting-edge sensors and displays.

The technical program begins on Monday, Dec. 8 (*see the table*). It is preceded by two short all-day courses on Sunday, Dec. 7: "Gigascale CMOS technology" and "Trends in RF devices and ICs for wireless applications."

On Monday at 9:00 a.m., the plenary session consists of three presentations: "Multimedia: Future and impact for semiconductor technology," "Pushing the limits of lithography for IC production," and "The significance of innovation in the semiconductor industry for performance in Chip Card applications."

The technical-paper program starts Monday afternoon with sessions 1 through 9 beginning at 1:00 p.m. Sessions 10 through 15 will begin Tuesday at 9:00 a.m., followed by the traditional luncheon at 12:20 p.m. with a presentation by James M. Early entitled ".....out to Murray Hill to play! An early history of transistors." In the afternoon at 2:15 p.m., sessions 16 through 21 will be held. That evening at 8:00 p.m., will be two panel sessions (22 and 23). Sessions 24 through 30 will start Wednesday at 9:00 a.m., and sessions 31 through 36, start at 1:30 p.m. The IEDM is sponsored by the Electron Devices Society of the IEEE. Its general chairman is Ken Galloway; Pierre Woerlee is technical program chairman; and Gary Bronner is program vice chairman.

1997 INTERNATIONAL ELECTRON DEVICES MEETING

Session 1 Plenary session	Session 2 ICs--advanced and embedded DRAM technology	Session 3 Solid-state devices--RF technology	Session 4 CMOS devices and reliability--thin-oxide reliability and characterization	Session 5 Device interconnect technology--low-resistance silicide integration	**Session 6** Modeling and simulation--interconnect modeling and manufacturability
Session 7 Quantum electronics and compound semiconductors--single-electron devices	**Session 8** Detectors, sensors and displays--image sensors	**Session 9** CMOS devices and reliability--advanced CMOS devices	**Session 10** Device interconnect technology--DRAM	**Session 11** ICs--flash memory technology	**Session 12** Modeling and simulation--RF modeling
Session 13 Emerging technologies	**Session 14** Solid-state devices--power devices	**Session 15** Quantum electronics and semiconductor devices--lasers and LEDs	**Session 16** CMOS devices and reliability--SOI devices and circuits	**Session 17** CMOS devices and reliability--plasma damage and hot-carrier effects	**Session 18** Device interconnect technology--device technology
Session 19 Modeling and simulation--process modeling I	**Session 20** Detectors, sensors and displays--TFT technology	**Session 21** Quantum electronics and compound semiconductors--FETs	**Session 22** Manufacturing in the next millennium: the emerging role of foundries	**Session 23** Lithography for 100-nm device fabrication	**Session 24** ICs--large-scale SOI ICs
Session 25 Device interconnect technology--FeRAM	**Session 26** CMOS devices and reliability--gate electrode and dielectrics	**Session 27** Device interconnect technology--device isolation technology	**Session 28** Modeling and simulation--process modeling II	**Session 29** Detectors, sensors and displays--field emitter arrays and advanced electron sources	**Session 30** Quantum electronics and compound semiconductors--heterojunction transistors and photodetectors
Session 31 Device interconnect technology--interconnects	**Session 32** Solid-state devices--advanced bipolar and MOS devices	**Session 33** CMOS devices and reliability--advanced CMOS: gate/channel engineering	**Session 34** ICs--high-performance technology and its application	**Session 35** Modeling and simulation--advanced device simulation	**Session 36** Detectors, sensors and displays--detectors and MEMS

Memory And Logic Structures Are Getting Faster And Denser

Designers Detail Advanced Process Techniques And Finer-Dimension Design Rules At IEDM To Build Next-Generation Memories And Logic.

Dave Bursky

Advances in cell structures for 1- and 4-Gbit DRAMs, 1-Gbit flash memories, and process improvements will make possible ferroelectric storage devices and single-electron switches. These are just some of the digital developments that will be showcased at this year's IEDM. Improvements in the basic cell structures, of course, are the precursors to full chips that can implement memory capacities thought impossible just a decade ago, or achieve switching speeds for CMOS that were once the exclusive realm of bipolar ECL or gallium arsenide technologies. In addition, digitally oriented sessions at the conference will cover advanced metallization technologies, new isolation approaches, and new device structures for high performance.

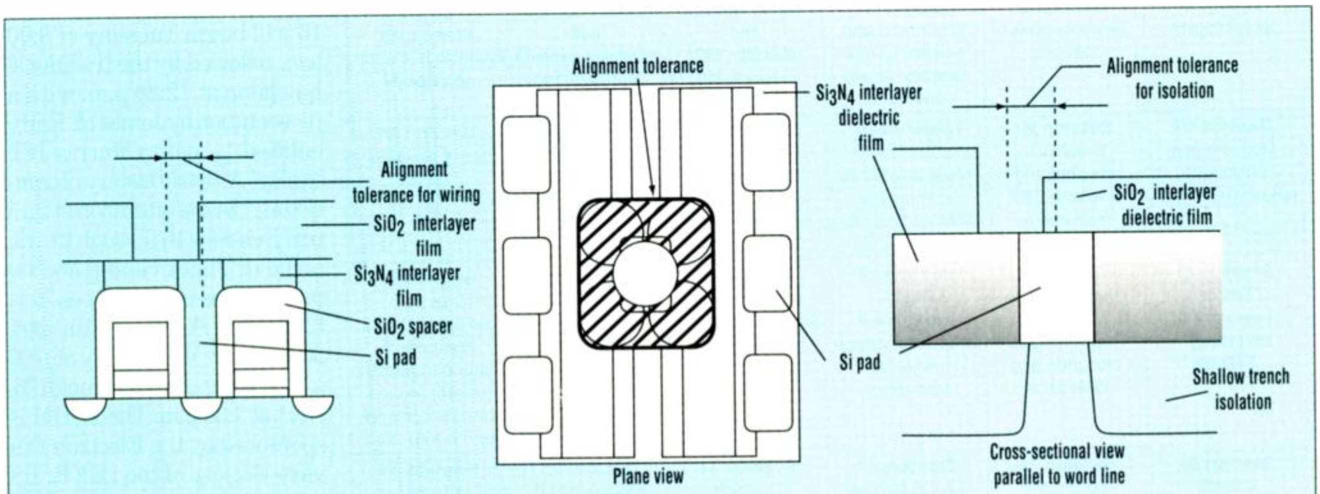
Even though production has not yet begun on the 1-Gbit DRAM, designers are hard at work devising basic cell structures for next-generation 4-Gbit memories. In a pair of papers in Session 2, and several papers in Session 10, researchers from NEC Corp., Tokyo, Japan, Fujitsu Labs Ltd., Atsugi, Japan, Texas Instruments (TI) Inc., Dallas, Samsung Electronics Co., Kyungki-Do, Korea, and Toshiba Corp., Tokyo, Japan, detail experimental memory cells for just such high-density chips.

The research done by NEC described in paper 2.1 has led to a memory cell with an area of just 0.135 µm^2 using 0.12-µm design rules. In such a small cell, alignment tolerance between contact holes and wiring is one of the most important manufacturing aspects, since hard-to-control tolerances will adversely affect yield. The self-aligned-contact cell was designed with a two-dimensional borderless contact pad to provide a large alignment tolerance, not only for wiring, but also for isolation *(Fig. 1)*.

The contact-pad structure is formed with a germanium-added anisotropic, selective, epitaxial-silicon growth and a silicon-nitride insulator planarized with chemical-mechanical polishing (CMP). Except for its top surface, the silicon pad is buried by the silicon nitride interlayer dielectric film, which works as an etch stop. The resulting structure allows designers to obtain an alignment tolerance of 0.07 µm for both wiring and isolation, thus easing manufacturing.

A novel high-aspect-ratio pillar structure capacitor was developed by Fujitsu for use in COB-style STC DRAM cells. When fabricated with 0.15-µm design rules, the storage cell, described in paper 2.2, occupies an area of 0.21-µm^2. In the peripheral area, due to the capacitor height, high-aspect-ratio vias are formed by via-pillars fabricated simultaneously with the capacitor pillars. That keeps the surface flat so that the multiple-layer-metal interconnects can be formed without requiring high-aspect-ratio via-hole etching or metal filling as performed in a conventional via process. Well-established oxy-nitride or tantalum-pentoxide dielectric films can be used in the formation of the pillar capacitors rather than the more exotic and less-stable barium-strontium-titanate (BST).

A pillar height of 1.5 µm results in a



1. A two-dimensional borderless contact pad technology developed by NEC allows the creation of DRAM storage cells that occupy an area of less than 0.135 µm^2, a size that would permit memory densities of 4 Gbits on a chip when fabricated on processes with 0.12-µm design rules. The three views of the pad from left to right—planar, normal to the word line, and parallel to the word line—show the large alignment tolerance that will help improve yield by simplifying the manufacturing process.

storage capacitance of 17 fF/cell, and when formed with an oxy-nitride dielectric that has an equivalent oxide thickness of 4.1 nm, the cell has a leakage current of 0.058 fA. A tantalum-pentoxide film would yield a storage capacitance of 22 fF. The cell's fabrication sequence takes full advantage of self-aligned processing—self-aligned contact etching of the source and drain windows, self-aligned elevated source and drain through the use of a polysilicon damascene step, self-aligned titanium silicidation of the surface of the source and drain, self-aligned plug to the silicon-nitride encapsulated bit lines, and self-aligned patterning of the capacitor's plate electrode. The silicided elevated source and drain structures, and the flat surface also make the overall memory structure well-suited for merged DRAM and logic functions in the 4-Gbit DRAM era.

High-Density Stacks

Another stacked memory structure, described by TI in paper 10.1, is targeted at gigabit-density DRAMs, and uses a BST dielectric to gain the advantage of the material's higher dielectric constant. The process developed by TI also employs a platinum capacitor electrode and oxidation-resistant barrier and adhesion layers to enhance the thermal and physical stability of the bottom electrode structure. For successful integration with the entire silicon process flow, the storage capacitor must also withstand the subsequent back-end process (interlayer dielectric deposition and metallization), while maintaining good device properties.

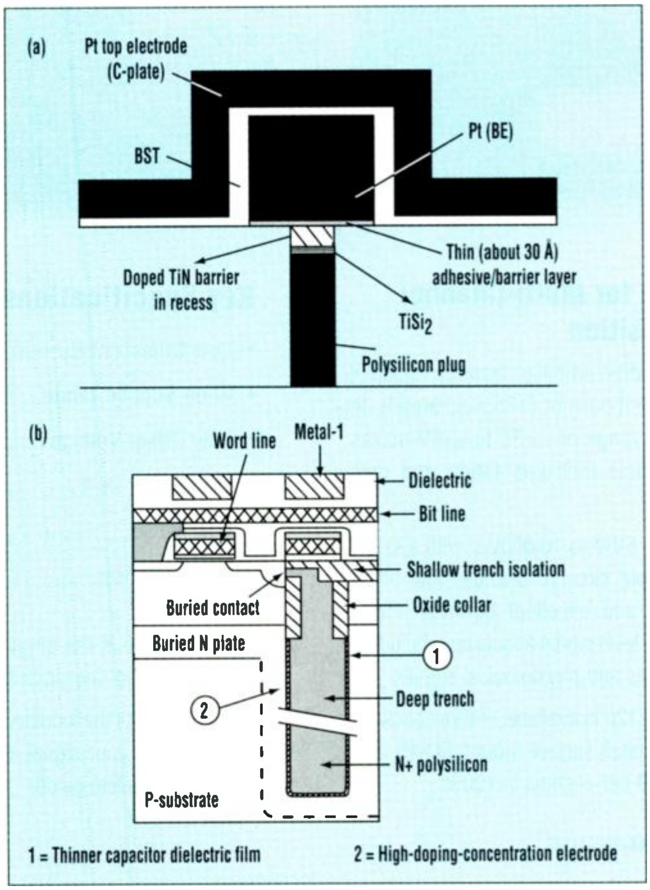
In TI's structure, via openings with diameters of 0.25-to-0.35-μm are first formed in a 500-nm-thick epitaxial silicon film and then filled with p-doped polysilicon *(Fig. 2a)*. Next, 50-nm-high plug recesses are formed with a polysilicon etchback stage. A silicide layer is now formed and the recess is filled with sputter-deposited oxidation-resistant doped titanium nitride. The silicide layer is then removed by using a CMP step, leaving only the titanium caps in the recessed areas. The caps protect the polysilicon plug/barrier and the electrode/barrier interfaces from the oxidizing atmosphere present when BST is deposited, and also reduce potential platinum adhesion problems.

Also eying BST as a storage-cell technology, researchers at Samsung Electronics have integrated a BST capacitor with platinum electrodes and a silicon-dioxide spacer that will be presented in paper 10.2. One of the key problems they had to deal with was the ability to etch the platinum to create a better shape for the storage node. The use of the silicon-dioxide spacers protects the titanium-silicon-nitride diffusion barrier from being oxidized and overcomes the poor conformality of the BST sputtering process. As a result, post-annealing process temperatures of up to 650°C are possible without barrier oxidation, while achieving a capacitance of 25 fF for a storage node—a level appropriate for gigabit-density DRAMs.

Also working on BST-based memory cells, researchers at Toshiba combined the BST cell with heteroepitaxial fabrication techniques on strontium-rubidium-oxide (SRO) electrodes. The resulting structure, detailed in paper 10.4, yielded an extremely-high dielectric constant in 20-nm-thick capacitors, which are equivalent to silicon-dioxide devices with ultra-thin dielectric thicknesses of 0.84 nm. The high-capacitance and low leakage currents are attributed to a controlled lattice deformation caused by the lattice constant mismatch between the BST and the SRO, and the cleanliness of their heteroepitaxial interfaces.

A second presentation by Toshiba in Session 10 (paper 10.6) examines the use of a single-layer nitride dielectric film along with a high-concentration doping scheme to create capacitor storage cells for 1- and 4-Gbit trench-style DRAMs. The approach chosen by Toshiba combines a silicon-nitride layer formed by a chemical-vapor deposition process with vapor-phase doping to reduce capacitance loss by forming high-concentration doping regions (8 ↔ 10^{19} cm^3) on the trench sidewall *(Fig. 2b)*.

The capacitor consists of the depletion layers of the electrode and the dielectric film. To decrease the equivalent thickness, the depletion layer width of both the storage node and plate electrodes should be reduced. But as the trench diameter is scaled down, the high-concentration doping provides the required concentration in the sidewalls.



2. The use of barium-strontium-titanate for the capacitor dielectric and platinum as a barrier electrode material allows Texas Instruments to achieve high-capacitance in a small cell area, thus making practical gigabit density memories (a). A single-layer nitride film and a vapor-phase doping scheme developed by Toshiba allows the company to craft a trench cell suitable for use in gigabit-density DRAMs (b).

Embedding The DRAM

In addition to searching for better capacitors to build denser memories, researchers are hard at work trying to find ways to meld DRAM technology into logic processes so that system logic chips can include dense blocks of DRAM.

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Product	INL (% FSR)	Input Ranges	Resolution (Bits at 10Hz)	Resolution (Bits at 1kHz)	Power Dissipation (mW)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS1212	±0.0015	±312mV to ±5V	22	16	1.4	$7.25	11360	93
ADS1214	±0.0015	±20mV to ±320mV	22	16	1.4	$7.25	11368	94

GENERAL PURPOSE A/D CONVERTERS *no missing codes

Product	Resolution (Bits)	INL (LSB)	DN* (Bit)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS7813	16	±2.0	16	40	35	87	$20.00	11302	95
ADS7817	12	±1	12	200	2.3	71	$5.18	11369	96
ADS7822	12	±0.75	12	75	0.54	71	$4.64	11358	97
ADS7825	16	±2.0	16	40	50	86	$28.46	11304	98

INSTRUMENTATION AMPLIFIERS

Product	Description	I_Q (µA)	Offset Voltage (µV) max	Offset Drift (µV/°C) max	I_B (nA) max	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
INA122	Single-Supply, *micro*Power	60	250	3	24	$2.50	11388	99
INA128	Precision, Low Drift	700	50	0.5	5	$3.38	11296	227
INA125	On-Board V_{REF}	460	250	2	20	$2.10	11361	228
INA126	Low Cost, MSOP Package	175	250	3	25	$1.60	11365	229

OPERATIONAL AMPLIFIERS

Product	Description (all are rail-to-rail output)	Single/Dual Quad	Power Supply Single (V)	I_Q (µA)	Price/Ch. (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
OPA241	*micro*Power, Precision	S	2.7 to 36V	24	$1.06	11406	230
OPA336	*micro*Power, CMOS	S, D, Q	2.3 to 5.5V	20	$0.47	11380	231
OPA340	High Speed, Rail-to-Rail I/O	S, D, Q	2.5 to 5.5V	750	$0.55	11404	232

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TECH INSIGHTS | IEDM—DIGITAL TECHNOLOGY

in large memory arrays. Cells can be reliably programmed using cell biases much lower than used in typical flash memories, but in equivalent time and with a fraction of the programming current used by other flash memories. Read voltages are as low as 1.8 V, while programming levels are between 3 and 5 V. Cell leakage currents are less than 10 nA. That will keep triple-well currents manageable, even for large arrays.

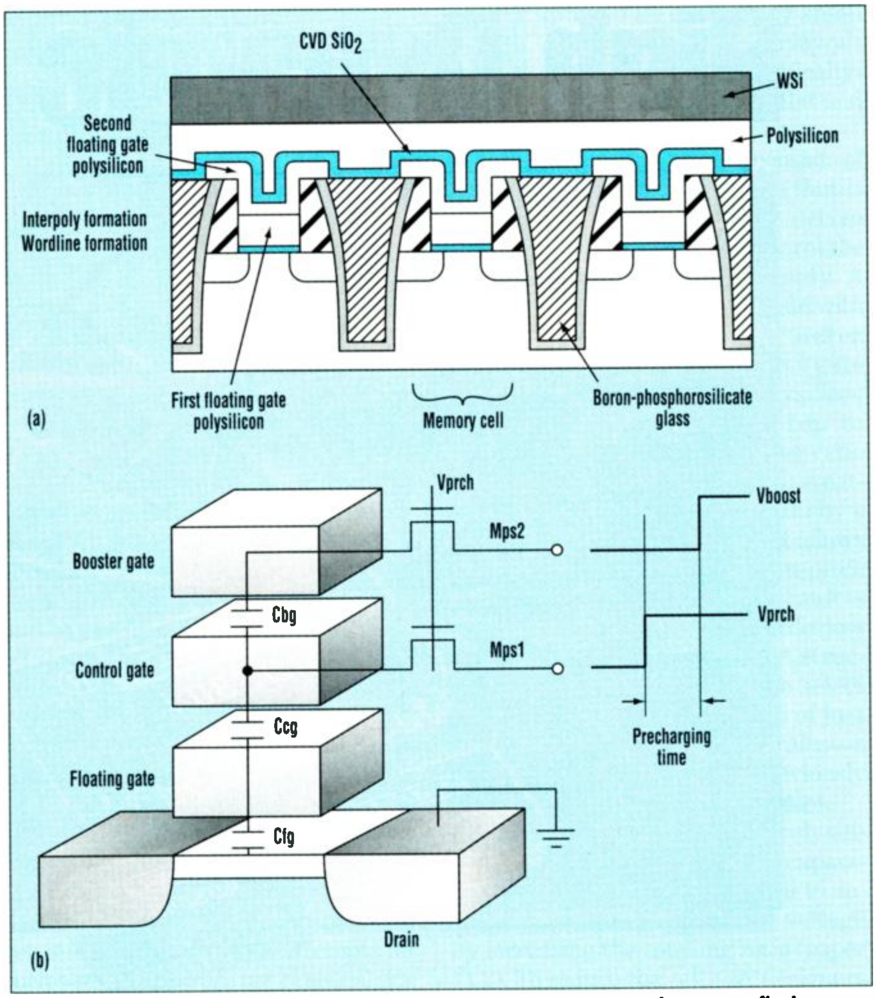
Also working on a low-voltage operating solution, researchers at Samsung Electronics have developed a triple polysilicon stacked flash cell that employs word-line boosting through the addition of a third gate that's simply stacked and self-aligned on the conventional control gate *(Fig. 4b)*. Detailed in paper 11.4, the stacked structure adds a successively-coupled booster-gate bias in addition to the precharged control gate voltage. The extra gate helps increase the floating-gate potential, thus lowering the programming voltage for NAND-type flash cells.

In addition to work done with floating-gate non-volatile storage cells, a full session (Session 25) will be devoted to ferroelectric memory technology, which is used both in non-volatile storage applications and as a high-dielectric material for DRAM cells. In the session, paper 25.1 from Matsushita Electronics Corp., Osaka, Japan, and Symetrix Corp., Colorado Springs, Colo., researchers provide details of a ferroelectric RAM that can retain data written with a 2.5-V signal for a period of 10 years, even with high levels of humidity and temperatures of up to 70 °C—a feat previous FeRAMs couldn't achieve.

These results are possible thanks to a newly developed ferroelectric material with mixed superlattice characteristics of the Y-1 material family and the integration technology that makes use of plasma-silicon-nitride passivation. The superlattice combination consists of layers of strontium-bismuth-tantalum-oxygen and strontium-bismuth-niobium-oxygen. The new structure will allow the fabrication of megabit-density FeRAMs.

A memory structure that combines a one-transistor/one-capacitor structure using a ferroelectric capacitor is the focus of paper 25.6 by Fujitsu Ltd., Kawasaki, Japan. Fabricated with 0.5-µm features, the memory structure lends itself to integration with CMOS logic processes and devices. With the cell, designers were able to integrate 68 kbits of FRAM and an 8-bit microcontroller. The ferroelectric capacitor is formed with lead-zirconium-titanate (PZT) films that are RF sputter deposited and then patterned with reactive-ion etching and then covered with an inter-layer dielectric.

Additional papers in the session examine various aspects of ferroelectric material deposition. In paper 25.2 researchers at Oki Electric Industry Co. Ltd., Hachioji, Japan, examine the proportion of thin films with ultra-high resistance to annealing in a hydrogen atmosphere. NEC in paper 25.3 examines the use of RF magnetron sputtering to control the PZT film crystal orientation to provide better memory endurance. Researchers at Sharp Corp., Nara, Japan, in paper 25.4, examine the use of a high-stability electrode technology with which they form stacked strontium-bismuth-tantalum-oxide capacitors. And, in paper 25.7, researchers from Samsung examine the use of an ultra-thin encapsulating barrier layer for ferroelectric capacitors to eliminate oxidation problems of the underlying electrodes.



4. Expected to allow the fabrication of 1-Gbit flash memories, a contactless-array flash memory structure developed by Hitachi combines 0.18-µm-wide self-aligned shallow-groove isolation for tight memory cell spacing and a high-capacitance boron phosphosilicate glass dielectric to form 3-D shaped floating gates (a). A triple-polysilicon floating-gate structure that employs the third gate as a booster to increase the floating-gate potential is the result of work by researchers at Samsung Electronics.

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Slightly	538

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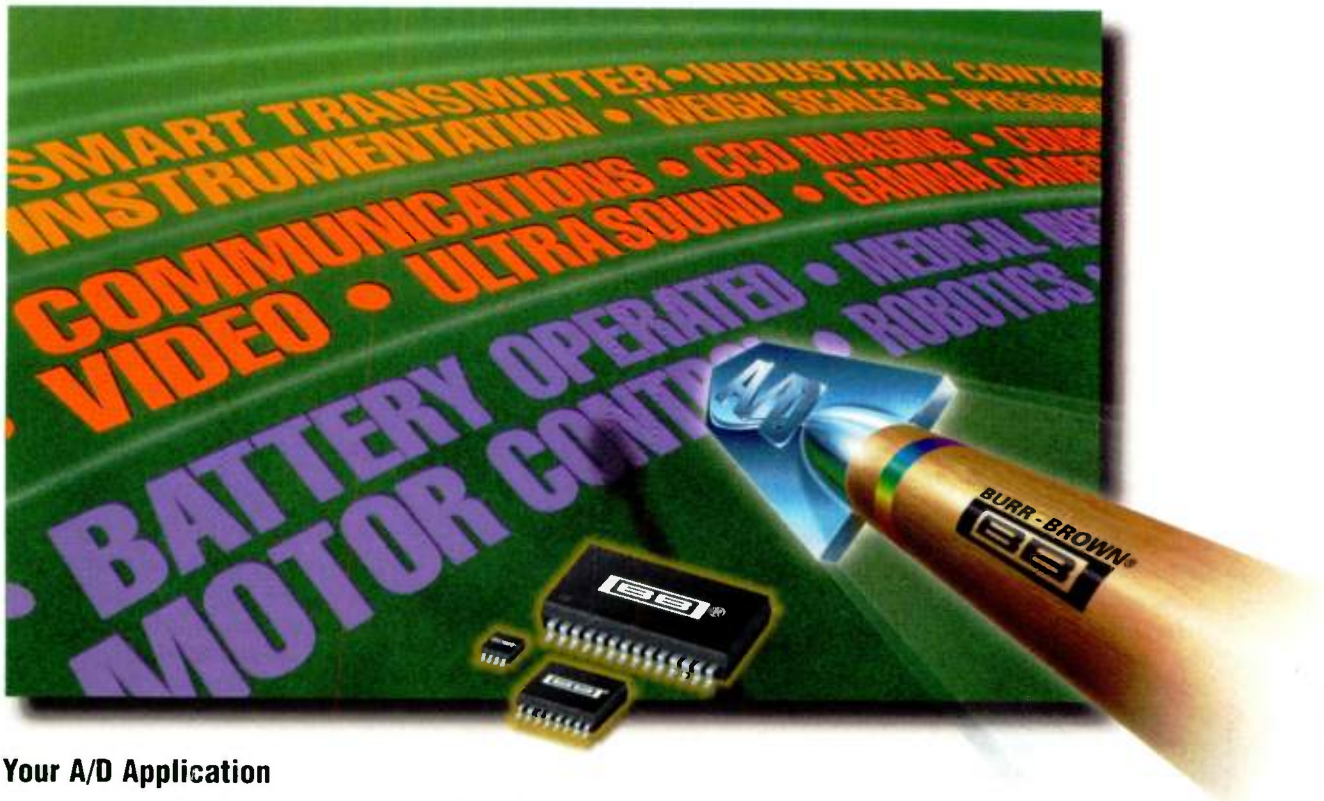

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ADS1210	±0.0015	±312mV to ±5V	24	20	26	$9.60	11284	80
ADS1212	±0.0015	±312mV to ±5V	22	16	1.4	$7.25	11360	81
ADS1214	±0.0015	±20mV to ±320mV	22	16	1.4	$7.25	11368	82

HIGH-SPEED A/D CONVERTERS **preliminary information*

Product	Resolution (Bits)	Speed (MHz)	Power (mW)	SNR (dB)	DNL (LSB)	SFDR (dBFS)	Supply (V)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS800	12	40	390	64	±0.6	61	+5	$29.00	11286	83
ADS803	12	5	116	69	±0.3	82	+5	$9.55	11398	84
ADS824*	10	75	315	59	±0.5	70	+5	$8.50	11403	85
ADS930/931	8	30	66/63	46/48	±0.4	51/49	+3/+5	$3.37/$3.27	11349	86

GENERAL PURPOSE A/D CONVERTERS **no missing code*

Product	Resolution (Bits)	INL (LSB)	DNL* (Bit)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	THD (dB)	Price (1kpcs)	FAX*LINE* # 1-800-548-6133	Reader Service #
ADS7813	16	±2.0	16	40	35	87	−90	$20.00	11302	87
ADS7817	12	±1	12	200	2.3	71	−83	$5.18	11369	88
ADS7822	12	±0.75	12	75	0.54	71	−82	$4.64	11358	89
ADS7825	16	±2.0	16	40	50	86	−90	$28.46	11304	90

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Rivalries Between Silicon And Exotic Semiconductors Abound At IEDM

SiGe And Vanilla Silicon Move Into RF And Optical Applications As Compound Semiconductors Stake Out Their Niches.

Lee Goldberg

A quick glance at IEDM's Session 32, "Advanced Bipolar and MOS Devices," reveals that great strides are being made to move silicon-based semiconductor performance into the realm occupied by GaAs and other exotic materials. After a long adolescence, SiGe seems to be delivering on many of the promises it made when it first came on the scene, nearly a decade ago.

In "130-GHz F_T SiGe HBT Technology," researchers from Hitachi Ltd., Tokyo, Japan, discuss how they refined the internal structure of an HBT to overcome previous problems. Rigorous hydrogen precleaning and careful control of doping gradients to properly shape the emitter-base region were key to delivering transistors with an f_t maximum of up to130 GHz *(Fig. 1)*.

Also contributing to the success was the use of ultra-high vacuum, chemical-vapor deposition (UHV/CVD) to selectively deposit SiGe. The insights this paper provides on the effect of dopant profiles on the ac and dc characteristics of SiGe HBTs will help to narrow the performance gap between silicon and more exotic III/V semiconductors.

Since it only costs around one million dollars to add UHV/CVD capability to a fine-geometry fab line, this technology could put many chip manufacturers into the RF-device business. Frank Goodenough, *Electronic Design's* analog editor, feels that this development is "one more stake in GaAs's heart."

Selective deposition of SiGe also was a critical factor in producing the 100+ GHz transistors described in "A Selective-Epitaxial SiGe HBT with SMI Electrodes Featuring 9.2-ps ECL-Gate Delay" in Session 32. In this paper, researchers from Hitachi Ltd.'s central research laboratory in Tokyo explored how self-aligned, stacked-metal/IDP (SMI) electrodes can be used to reduce contact resistances and improve the performance of selective-epitaxial SiGe HBTs *(Fig. 2)* .It was used to selectively stack tungsten film on the emitter and base region's polysilicon electrodes. Despite their relatively high current capacity (1 to 3 mA), the transistors displayed cutoff frequencies of up to 62 GHz.

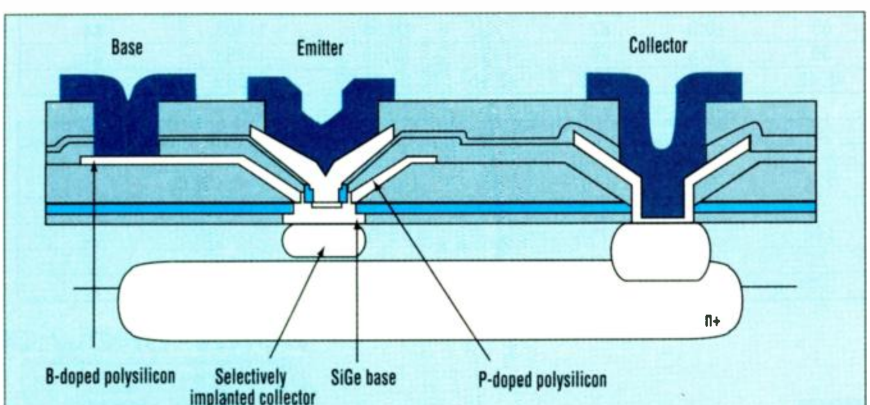
Another barrier to SiGe HBTs' theoretical performance is the outdiffusion of boron from their thin, highly doped base layers into the rest of the transistor. Occurring most heavily in the collector, this can seriously degrade transistor parameters unless it is held in check.

In their paper "The Effect of Carbon Incorporation in SiGe Heterobipolar Transistor Performance and Process Margin," a team of scientists from The Institute for Semiconductor Physics, Frankfurt, Germany, demonstrates how background doping of carbon within the SiGe layer limits outdiffusion by competing with the boron for the capture of silicon self-intersitials. They note that carbon implantation does not require any additional changes to the CMOS-based fabrication process, and yields f_Ts in the area of 64 GHz. Faster operating speeds are anticipated with the higher boron doping levels that the carbon stabilization process is expected to allow.

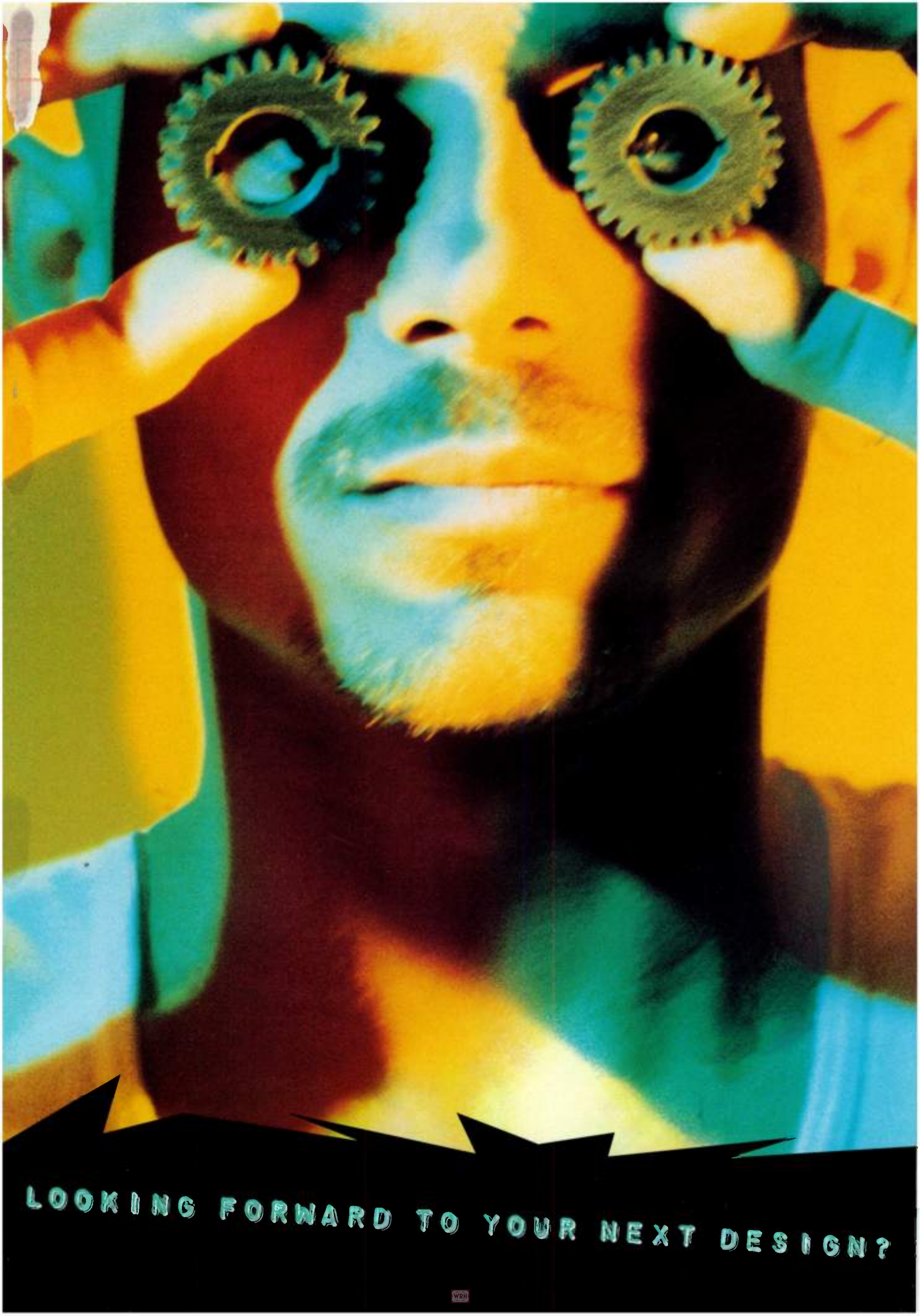
Standard silicon also showed significant promise for wireless frequency applications. In "A 54-GHz f_{MAX} Implanted-base 0.35-µm Single- Polysilicon Bipolar Technology," a consortium of French semiconductor researchers demonstrated a 0.5-µm bipolar technology that uses a single-polysilicon self-aligned structure to achieve transistors capable of operating above 50 GHz.

In their paper "Simulation Fabrication and Characterization of High-Performance Planar-Doped-Barrier," scientists from the University of Bundeswehr, Munich, Germany, describe another important step in making multigigahertz MOS devices. They found a way to employ velocity carrier overshoot found in sub-100-nm channel structures to gain higher transconductance speeds. By using a newly developed planar-doped-barrier FET (PBDFET) structure, they can overcome the avalanche multiplication and hot-carrier effects that previously made this impractical.

Session 3 at IEDM focuses on solid-state RF devices. Interestingly, four of the five papers are focused on technologies for producing inductors on ICs. As integration of high-frequency devices



1. The cross-section of this HBT illustrates the SiGe base region that was selectively formed using ultra-high vacuum/chemical-vapor deposition (UHV/CVD).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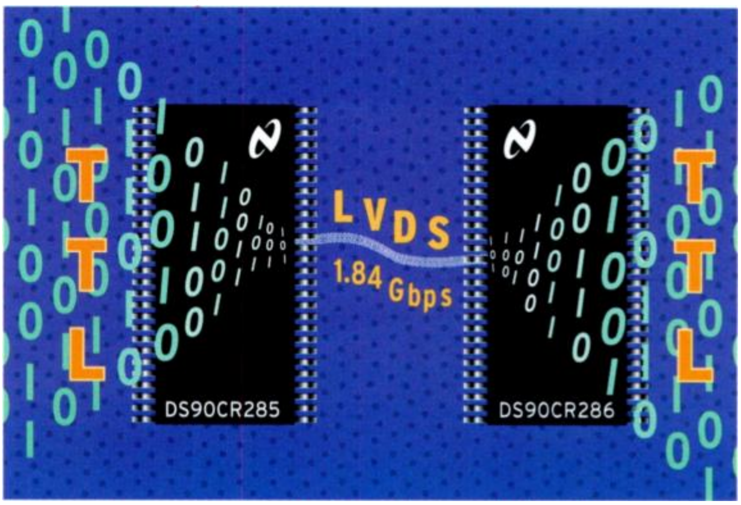

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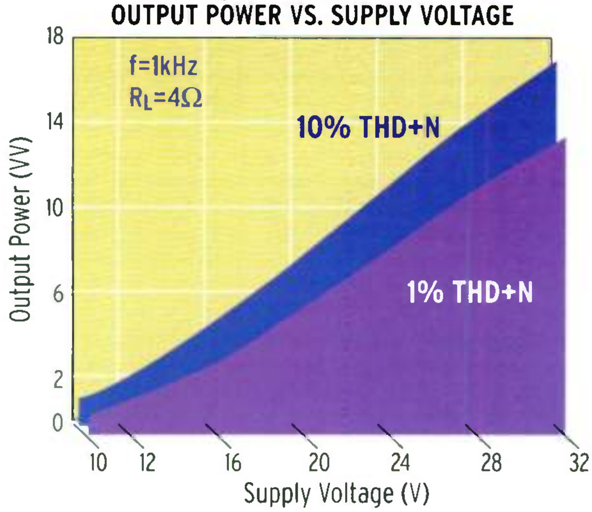

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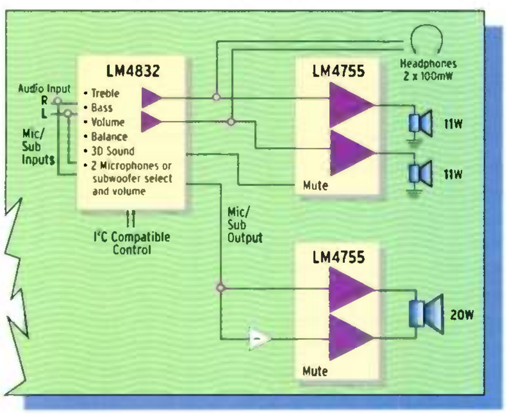

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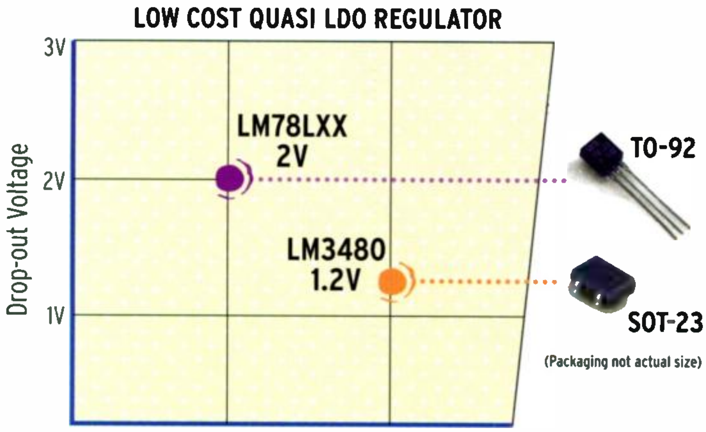

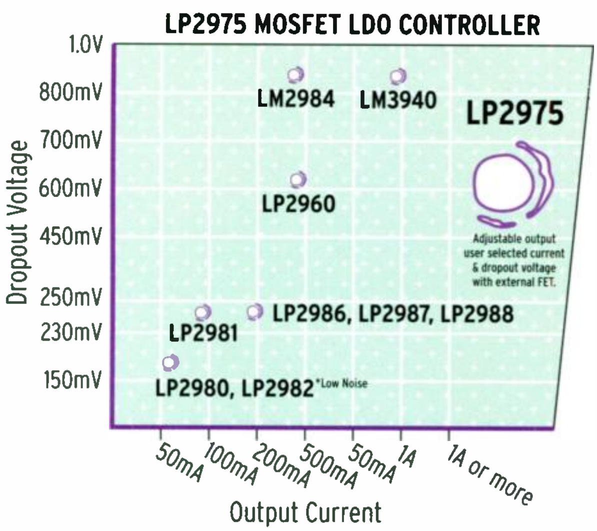

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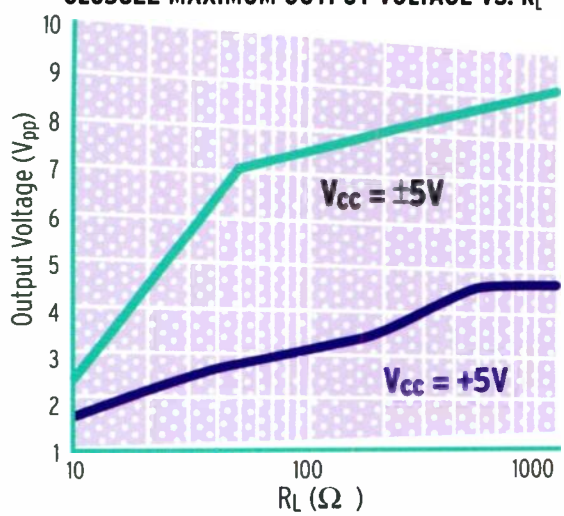

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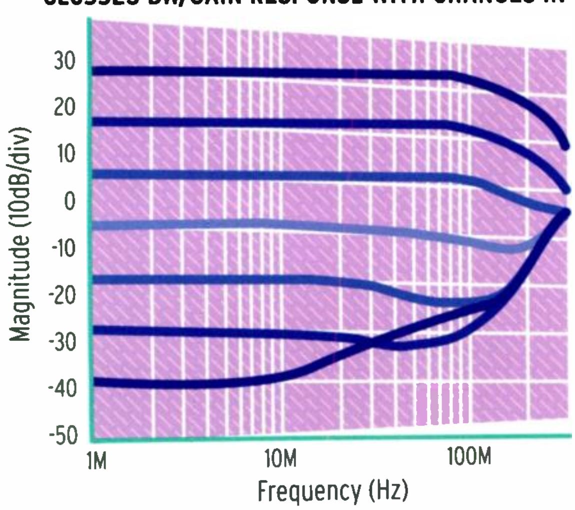

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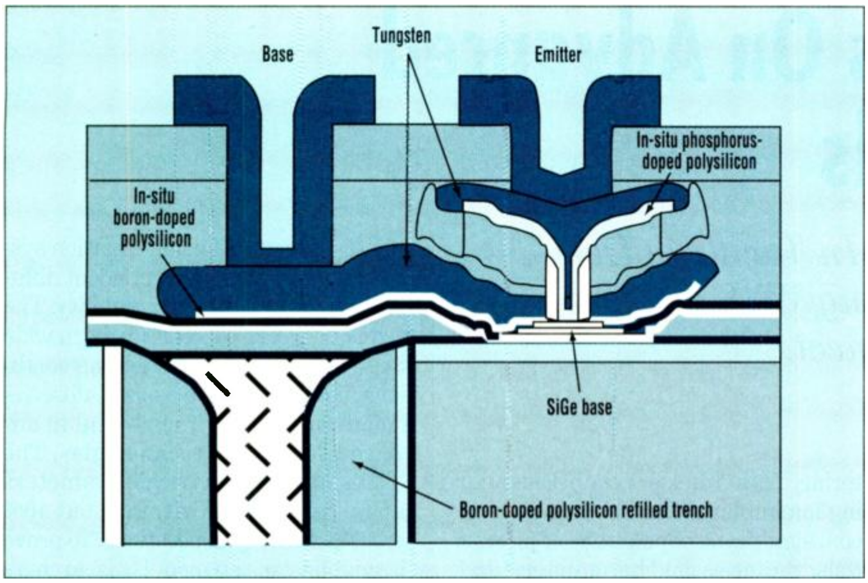


2. To reduce base and emitter resistances in this HBT, researchers used a self-aligned process to create a multilayer sandwich of tungsten and SiGe, in-situ doped materials.

increases, these inductors become increasingly necessary for intrastage matching, filtering.

In the session's paper "High-Q Microwave Inductors in CMOS Double Metal Technology and its Substrate Bias Effects for 2-GHz RF IC Applications," scientists from Korea's Electronics and Telecommunications Institute demonstrate how adding a biased pn junction beneath an inductor can raise its effective Q by 30%. By combining active junction substrates with thick-

Qs of 20 or more (at 2 GHz) for inductors ranging from 2.98 to 13.19 nH.

The paper from Rockwell Science Center, Thousand Oaks, Calif. "Extremely High-Q Tunable Inductors for Silicon-Based RF ICs," describes how a pair of inductors can be fabricated in so that their two coils run parallel to each other. By running a tuning current through the "drive" coil, the reactance of the inductor itself can be adjusted to nearly any desired level. Effective Q values of up to 2000 have been demon-

Another novel approach to fabricating inductors was discussed in the paper "Monolithic High-Performance Three-Dimensional Coil Inductors for Wireless Communication Applications," presented by students from the University of California at Berkeley and the Lawrence Livermore National Laboratory, Livermore, Calif. Instead of relying on existing silicon and aluminum planar processes, the researchers developed a low-temperature process that bonds microscopic coil cores to the chip's surface. The cores can be plated with copper and etched to form 3D spiral inductors. Qs of up to 22 have been demonstrated at frequencies of 1 GHz or more.

Power Developments

Session 14 concentrates on silicon power devices. The need for efficient, precise power control in nearly every vehicle, appliance, or tool we use has led to some important breakthroughs this year. In "A New Concept for High-Voltage MCCT With No-JFET Resistance by Using a Very-Thin Bulk Wafer," researchers from Fuji Electric's corporate research center describe a MOS-controlled cascode thyristor (MCCT). Employing an extremely thin (200 μm) bulk silicon wafer, the project used a special cell layout to avoid parasitic JFET resistance inherent to these devices, yielding a 1400-V operating voltage and a very low

IEDM Focuses On Advanced Device Models

Models Offer New Hope In Tackling Deep-Submicron Issues Dealing With Process Accuracy And Interconnect.

Cheryl Ajluni

The most recent advances in modeling techniques will be discussed at this year's IEDM. With the migration toward deep-submicron (DSM) geometries, we're beginning to see a move farther away from the silicon and the processes that make the devices. This change in direction brings up issues of accuracy and how to design to take full advantage of process technologies, instead of overdesigning or guardbanding silicon. The problem is that modeling a process and all of its associated effects can be difficult and time-consuming. In acknowledgment of this situation, two IEDM conference sessions this year focus solely on process modeling.

The first, Session 19, "Process Modeling I," focuses specifically on implantation and diffusion effects for DSM silicon CMOS. Various techniques are presented, such as a new 3D analytic model of ultra-low energy boron implantation, and a physically based model for simulating the boron segregation due to electric-field and boron transient-enhanced diffusion (TED) during the source-drain annealing process. Of particular interest is a physics-based modeling approach that can accurately simulate the diffusion, clustering, and subsequent activation of boron for a wide variety of implant and anneal conditions. This technique, a joint effort from the University of Florida, Gainesville, and Intel Corp., Santa Clara, Calif., is based on the Stillinger-Weber molecular dynamics calculation. It is summarized in paper 19.2, "A Physics-Based Modeling Approach for the Simulation of Anomalous Boron Diffusion and Clustering Behaviors," tering. These effects occur because during ion implantation of boron into silicon, significant populations of interstitials, vacancies, and boron-interstitials are created within the silicon bulk. When the silicon wafer undergoes thermal cycling in an attempt to correct implantation defects or activate and diffuse the boron, these populations become free to interact with each other and the silicon lattice. These bidirectional interactions are difficult to model.

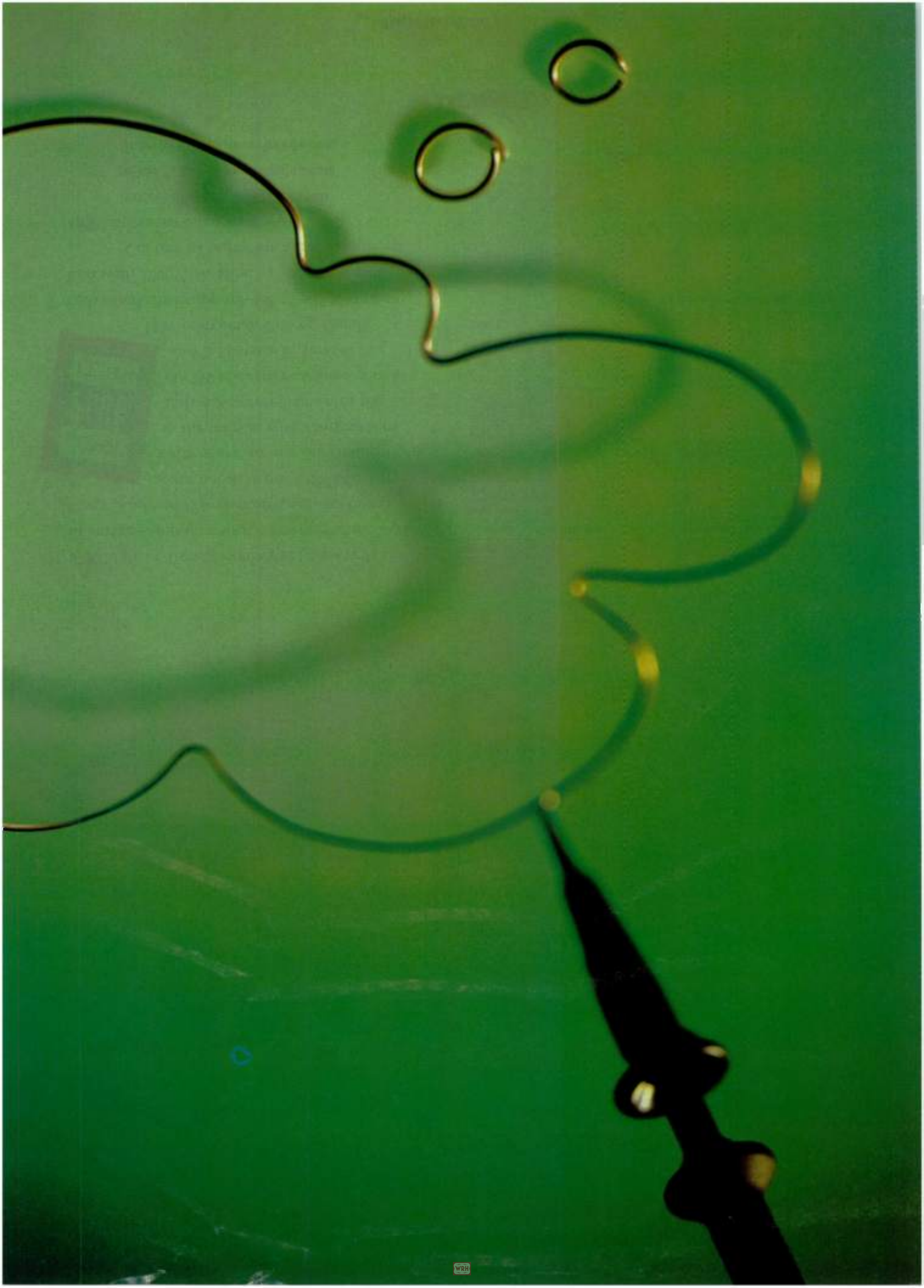
The model developed by the University of Gainesville and Intel can simulate not only these interactions, but also the nucleation and evolution of defects. The model enables better prediction of both threshold adjust implants and P^+ source-drain structures. Based on ab-initio calculations, it works by predicting many boron transient behaviors, including surface-dose loss effects. According to the researchers, this modeling approach holds great promise for the development of predictive boron diffusion and clustering models.

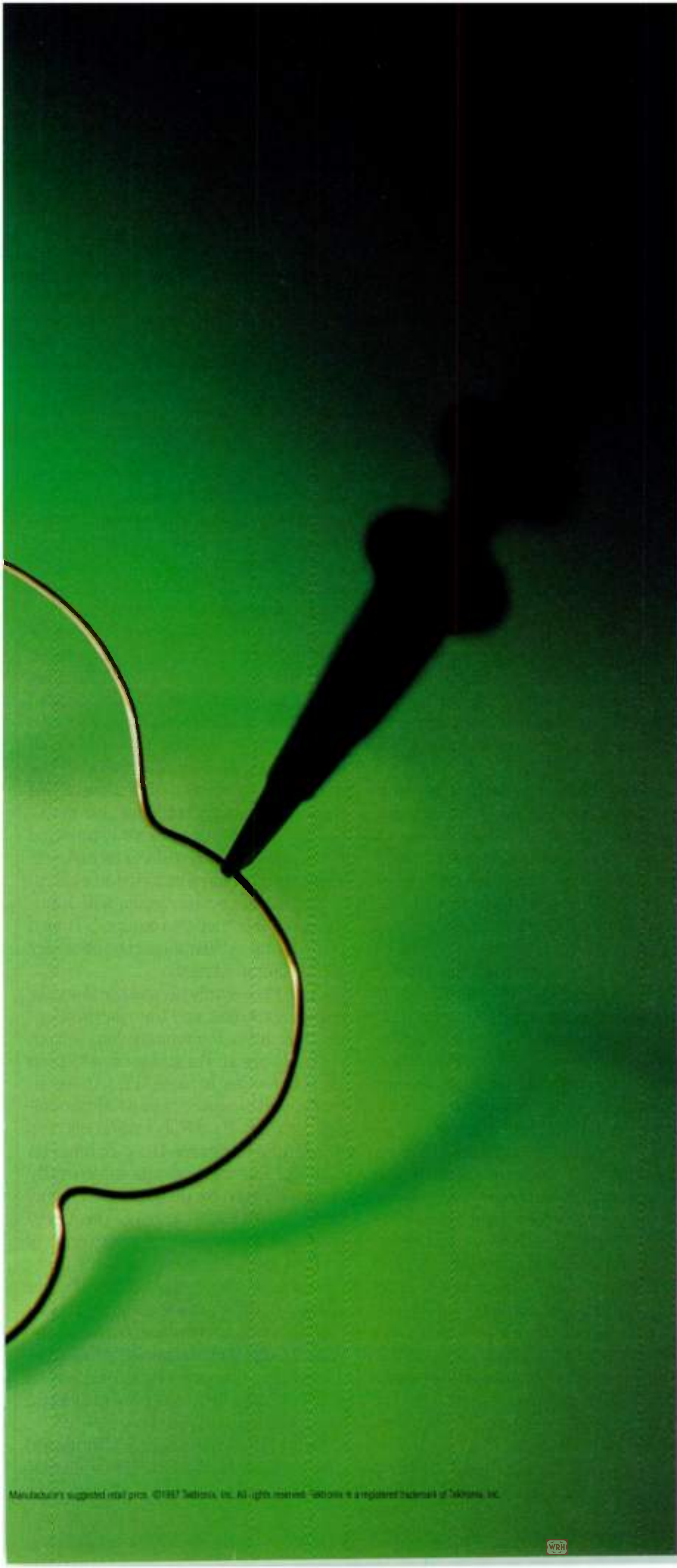
In a related development, a model for the calculation of TED for CMOS simulation is presented in paper 19.6, "Simulation of Transient Enhanced Diffusion Using Computationally Efficient Models." The model is based on damage-dependent diffusivity fields and dopant solubilities. It can accurately simulate multiple technology generations.

Until now, the methodology of choice for simulating TED has been a fully coupled approach that solves the continuity equations of all relevant defect types together with the dopant equations. Unfortunately, this approach has a number of drawbacks which subtract from its ef- only the dopant-diffusion equation system, but with damage-dependent diffusivity fields and dopant solubility. The technique works by reproducing a wide range of implant and annealing conditions, including the increased-dose/reduced-energy regimes found in advanced submicron technologies. The TED-sensitive electrical parameters can be reproduced within about 10% across technology generations. To prove the viability of the model, researchers have already begun successfully utilizing it as the main TED tool for technology support from 0.6-µm BiCMOS to 0.25-µm CMOS process development.

Session 28, "Modeling and Simulation—Process Modeling II," takes another stab at the process-modeling problem by dealing specifically with applications of process modeling to device modeling. In the first half of the session, suppression of reverse short-channel effects, and the application of inverse modeling and scanning capacitance microscopy to doping profile extraction are addressed. The second half of the session deals with the impact of nitrogen implants on the channel profile under the gate, the effects of arsenic diffusion through gate oxides, and the effects of lattice distortions on stress-induced leakage currents.

A proposed use of inverse modeling and scanning capacitance microscopy for doping profile extraction warrants special attention due to its diversity of application. This approach, as summarized in paper 28.2, "Inverse Modeling of MOSFETs Using I-V Characteristics in the Subthreshold Region," was developed by researchers at the Massachusetts Institute of Technology, Cambridge. What they developed is a 2D doping profile-extraction technique optimized for use with submicron MOS transistors. This method is especially critical because as MOS transistors are scaled to the submicron regime, the 2D distribution of dopants begins to have a significant ef-





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region to obtain the 2D doping profile. Once this task is accomplished, the channel length can then be easily obtained.

This techniques offers a number of significant advantages including the ability to extract 2D doping profiles of devices having very short channel lengths. The advantage is that the technique is immune to parasitic capacitances and noise. The technique also exhibits a low sensitivity to gate-area variations and a low dependence on mobility models, is nondestructive in nature, and has a simplistic approach to data collection and preparation. Further development of the technique may involve matching both I-V and C-V data simultaneously to use the best of both techniques for 2D doping profile extraction.

Paper 28.3, "An Advanced MOSFET Design Approach and a Calibration Methodology Using Inverse Modeling that Accurately Predicts Device Characteristics," from researchers at Motorola, Austin, Tex., proposes a design technique to address the increasingly difficult problem of predictive modeling of sub-0.2-µm devices using the traditional TCAD approach of process and device simulation. The difficulty stems from a lack of reliable models and difficulties in calibrating available process models. While there have been a number of other proposed approaches to creating and calibrating analytic-doping-profile representations, none have included a comprehensive and parameterized analytic description of the device structure that is scalable and, at the same time, fully calibrated to a set of current and capacitance data for many lengths.

By comparison, Motorola's MOSFET design approach provides a means for physical measurements either directly, or indirectly (inverse modeling), to be easily substituted for processes which are difficult to reliably simulate with today's process simulators. In effect, the approach not only provides an analytic model for the doping profiles in a MOSFET, but an accurate physical description of the device calibrated and scalable to subnominal dimensions as well. The model includes a description of the device structure and doping profiles that has been parameterized for optimization and sensitivity studies. The parameterized description provides the structural details of the oxide and nitride spacer thickness, silicide thickness, and gate bird's beak.

One of the benefits of the proposed design approach is its scalable extracted-doping description. This design is possible because the model can predict the performance of a subnominal device. Such an advantage is crucial for device designers because it enables a logical and systematic extrapolation to smaller device geometries prior to the availability of suitable lithography.

The Interconnect Problem

With shrinking process geometries comes a host of design issues that designers previously did not have to face. Below 0.35 µm, circuit performance becomes increasingly limited by interconnect and circuit manufacturability, which is limited by difficult device and interconnect variation issues. Session 6, "Modeling and Simulation—Interconnect Modeling and Manufacturability," specifically addresses the design issues arising from designing in a DSM environment. In particular, the session details a number of modeling approaches for accurate assessment of interconnect performance and device/circuit manufacturability.

One modeling approach comes from the IBM Austin Research Laboratory, Austin, Tex., and is detailed in paper 6.1, "Hierarchical Interconnect Modeling." This hierarchical extraction and modeling approach is specifically intended to overcome the difficulty of full chip-level 3D interconnect analysis. It works by decomposing the problem into smaller models which can then be efficiently simulated and correctly recombined.

As interconnect delays begin to drive gate delays, it becomes increasingly critical to properly model the interconnects, in addition to the devices, to generate accurate voltage and current waveforms during circuit simulation. Accomplishing this requires all interconnect models to be generated by an accurate 3D analysis, a process which generates huge volumes of data. The hierarchical extraction/modeling approach proposed by IBM provides a means of dealing with this need for accuracy, while handling the quantity of generated data. The technique also can provide variable modeling accuracy across different domains with a method of interfacing the boundaries between the different models, and to the devices.

In paper 6.2, "Automated Extraction of Capacitances and Electrostatic Forces in MEMs and ULSI Interconnects from the Mask Layout," from the Swiss Federal Institute of Technology, Zurich, and Albert Ludwig University, Freiburg, Germany, presents an automated approach to link layout, process, geometry, and electrostatic simulation for advanced MEMs and ULSI technology evaluation. Accurate and efficient electrostatic simulations are crucial for capacitance and electrostatic force calculations in ULSI interconnects, as well as in emerging MEMS technologies. Conventional simulations center on complex 3D geometries and various boundary conditions. These simulations often involve time-consuming and error-prone specification of the geometry, necessitate the construction of a 3D mesh suited to numerical computation, and require the use of an efficient and accurate electrostatic simulation engine.

In place of this lengthy procedure researchers devised a fully automated approach to electrostatically characterize the microstructures devices. Based on the boundary element method (BEM), the technique uses the mask layout and a process description as the input for the geometry definition. BEM techniques incorporated include multipole acceleration and error estimation with sophisticated meshing techniques. This solution allows automated electrostatic parameter extraction with minimal user interaction required. It also provides an estimation of the accuracy of the computed result.

A process-synthesis methodology for reducing the cost and time for developing derivative technology comes from researchers at Texas Instruments in Dallas. Detailed in paper 6.7, "An Application of Process Synthesis Methodology for First-Pass Fabrication Success of High-Performance Deep-Submicron CMOS," this method was successfully demonstrated by designing a CMOS gate shrink that was able to meet performance and manufacturability criteria on first-pass silicon. To achieve first-pass silicon, the methodology relies on the use of compact device and process models, such as response surfaces, for rapidly exploring large design spaces. These models come from a variety of sources including experimental data, historical data and simulation.

While accurate process simulation and modeling plays a crucial role in DSM


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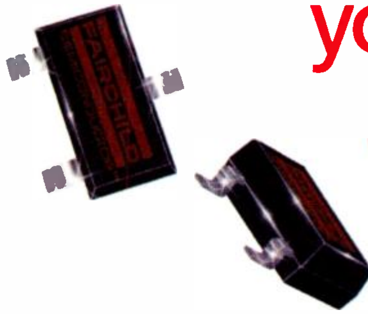


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Zero Standby • NM93CxxLZ • V_{CC}: 2.5V - 5.5V • Iccstdby: <1µA • 256bit - 16Kbit • X8 or 16 org	**Zero Standby** • NM24CxxLZ • V_{CC}: 2.5V - 5.5V • Iccstdby: <1µA • 256bit - 16Kbit	**Zero Standby** • NM25CxxxLZ • V_{CC}: 2.5V - 5.5V • Iccstdby: <1µA • 256bit - 16Kbit

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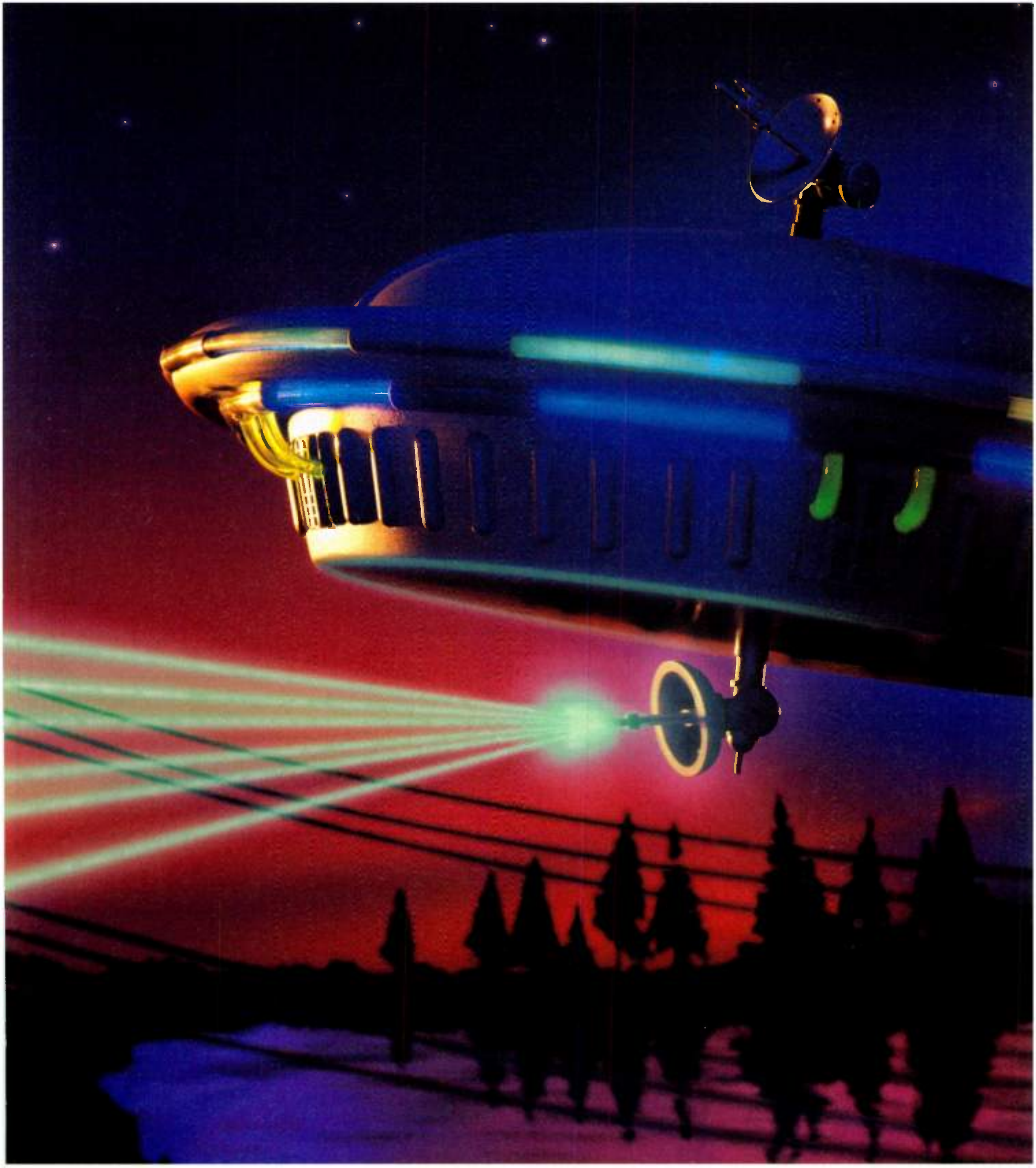

design, it is only half of the equation. The other half revolves around accurately modeling devices and the various types of components that comprise a given design. Session 35, "Modeling and Simulation—Advanced Device Simulation," focuses solely on the problem of providing advanced models for device simulation. One such model is detailed in paper 35.1, "Physical Oxide Thickness Extraction and Verification Using Quantum Mechanical Simulation." This proposed model, from Texas Instruments, uses quantum mechanical simulation to extract physical oxide thickness, and then applies accurate models to the interpretation of experimental results. Similarly, paper 35.2, "Assessment of Quantum Yield Experiments via Full-Band Monte Carlo Simulations," from Bell Labs, Lucent Technology, Murray Hill, N. J., and the University of Parma in Italy, applies Monte Carlo simulation to interpret quantum yield experiments.

Of particular interest is paper 35.5, "A Unified Substrate Current Model for Weak and Strong Impact Ionization in Sub-0.25-µm NMOS Devices," from Texas Instruments. Here researchers propose a unified substrate current model capable of consistently simulating both weak and strong impact ionization in sub-0.25-µm n-channel MOSFETs. This model requires the input of only three parameters which can be easily extracted from a single measurement. Its implementation in a circuit simulator provides the capability to include hot-carrier and electrostatic discharge (ESD) effects into circuit design optimization—a feature essential for achieving design-in-reliability targets. The three parameters that must be captured to model the substrate current include the effect of gate bias on impact-ionization and parasitic bipolar turn-on at high current levels, the peak substrate current at low currents, and the avalanche breakdown voltage of the drain junction.

Session 12, "Modeling and Simulation—RF Modeling," includes a number of papers concerning device and circuit modeling of RF applications. Some of the topics to be highlighted include unified microscopic treatment of noise in semiconductor devices and its suitability for low-noise FET design and wireless communication, and RF MOSFET Spice modeling accounting for distributed substrate and channel resistances. Also included in this session is a look at RF noise modeling of a 0.25-µm CMOS low-noise amplifier, non-linear noise analysis in semiconductor devices using the harmonic-balance technique, and simulation of substrate noise coupling through planar spiral inductors.

An interesting development is presented in paper 12.1, "Device Simulation for RF Applications." It details the development of device-level harmonic balance (HB) simulation for the direct extraction of performance factors such as intermodulation and harmonic distortion. This process can be used for a range of power RF device technologies. The technique, from Stanford University, Stanford, Calif., is applicable to silicon and GaAs.

HOW VALUABLE	CIRCLE
HIGHLY	545
MODERATELY	546
SLIGHTLY	547

Sensors And Displays Highlighted At IEDM

Advanced Device Structures And New Technologies Are Opening The Door For Emerging Display And Sensor-Based Applications.

Cheryl Ajluni

The "consumerization" of electronics has given a boost to sensor and display technologies. Consumer products are heavily dominated by portable applications, with sensors and displays playing key roles. Such components are the topic of five IEDM conference sessions.

In Session 8, "Detectors, sensors, and displays—image sensors," the use of CCD and CMOS imaging are discussed. Both technologies offer a number of features that make them suitable for applications such as digital still cameras and imaging. However, each has limitations that threaten their use in many emerging PC-imaging applications.

CCD sensors, for example, are a mature technology and offer high-performance capabilities, yet demand high-system power, are difficult to integrate on-chip, and only output an analog signal. However, CMOS sensor technology, is a relatively immature and unoptimized technology with low-performance characteristics. But, it does feature low system power, provides digital input and output, and is easy to integrate on-chip.

Many advances in active pixel image sensors (APSs) using standard CMOS are summarized in "MOS image sensors—recent advances and device scaling considerations" from the IBM Thomas J. Watson Research Center, Yorktown Heights, N.Y. The paper reviews advances in APS technology, devices, and pixel architecture, as well as on-chip circuit integration. It also addresses the compatibility of CMOS image sensors with standard CMOS technology.

An interesting development detailed in Session 8 is a high-resolution low-power CCD imager with a small pixel size and high charge capacitor. The imager comes from Philips Imaging Technology, Eindhoven, The Netherlands, and is well-suited for digital still cameras. It features good sensitivity and a real-time color preview mode.

DALSA Inc., Ontario, Canada, is responsible for an innovative architecture that allows the incorporation of large numbers of isolation pixels for the elimination of first-pixel droop in tapped CCDs. This architecture is specifically designed for use with a frame transfer area array sensor and does not require adding extra isolation rows beyond those already present in the device's storage region.

Session 13, "Emerging technologies," looks at the application of organic polymers to device circuitry and displays. These applications are addressed by Philips Research Laboratories in "Organic polymer devices and displays." A number of methods are underway to offer simpler and lower-cost sensors and displays that can be flexibly processed. To that end, the use of polymers as active elements in microelectronic devices is being eyed as the most likely solution. Polymers have traditionally been known for their ease of processing. They do not exhibit a temperature hierarchy and are highly flexible. As such, they're ideal for polymeric LEDs and logic. These developments are fully detailed in the Philips paper.

The polymeric LED consists of a patterned indium-tin-oxide (InTiO) anode, a conducting polymer layer, a fully conjugated polyphenylenevinylene derivative, and a low-work-function cathode. An 8-cm^2 area of the device is shown to operate at 4 V and can generate 100 cd/m^2 in the orange part of the spectrum. Lifetime for a device continually operating at this intensity is expected to be in the range of thousands of hours.

An advantage of this development is its low cost, due to its ease of processing, and its potential for high-volume production. By spincoating thin films and using only a limited number of process steps, electronic circuits wafers can be made on a variety of flexible substrates, and can literally be finished in less than an hour. To date, research has shown that 45 polymer transistors can be integrated onto a single chip. Higher circuit complexity with increased operating frequency and improved reliability is the focus of ongoing work.

In Session 15, "Quantum electronics and semiconductor devices—lasers and LEDs," seven papers highlight advances in light-emitting semiconductor diodes. An overview of the state-of-the-art of quantum dot lasers is presented in a paper from the Technical University of Berlin, Germany. In particular, techniques for realizing quantum dots (QDs) in a manner compatible with modern device technology are detailed.

This session also looks at the characteristics of QD room-temperature lasers based on self-organized semiconductor nanostructures, the first electrically tunable green light emission from AlGAP/GaP heterostructures at room temperature, and lasing in a square ring laser diode based on a GaAs/AlGaAs quantum-well heterostructure.

Thin-film transistor (TFT) technology holds the promise of becoming a viable option for the CRT replacement, offering a number of benefits that make it competitive with the heavily entrenched AMLCD (advanced matrix LCD). Some most recent advances in TFTs are presented in Session 7, "Detectors, sensors and displays—TFT technology." Two significant developments are a double-gate elevated channel conductivity modulated polysilicon TFT, which provides high drive current, large storage capacitors and EEPROM, and the first flexible amorphous-silicon TFT on an ultra-thin substrate of 25-µm stainless-steel foil.

The first development hails from

Hong Kong University of Science and Technology, Clear Water Bay, and is detailed in "A simple polysilicon TFT technology for display systems on glass." The proposed TFT device is referred to as an elevated-channel TFT (ECTFT). It is characterized by a low temperature of 600°C, and can provide efficient pixel switches, and high current digital and kink-free analog devices. This technology is expected to be utilized in the future to realize small or medium-size display systems on glass.

The flexible amorphous-silicon TFT comes from Princeton University, N.J., and is presented in "Thin film transistors for foldable displays." The device has stainless-steel foil substrate, and is planarized with a 0.5-µm-thick spin-on glass. The device's transistors remain operational under convex or concave bending down to a radius of curvature of 2.5 mm. This feature demonstrates the viability of foldable transistor backplane circuits for use in active matrices in highly rugged and portable applications such as a foldable intelligent map. Ongoing work will focus on the achievement of a smaller radii of curvature and on the integration of such foldable TFT backplanes with organic LEDs (OLEDs) to obtain flexible panels.

Session 29, "Detectors, sensors, and displays—field-emitter arrays and advanced electron sources," deals with FEAs and nonthermionic advanced cathodes for use in flat panel displays, and for powering switching devices and RF amplifiers. Of particular interest is a method for increasing the emission current density of MIM (metal-insulator-metal) cathodes as summarized in "Increased emission current from MIM cathodes through the use of a multilayer top electrode," from Hitachi, Tokyo, Japan. This is especially important because it makes FEDs (field emission displays) a viable solution for next-generation, high-resolution, high-brightness emissive flat-panel displays.

Until now, the MIM cathode has not been viable because its emission current density only ranged from 1 to 50 $\mu A/cm^2$—far below the required 1 mA/cm^2 for a high screen-voltage FED. Researchers at Hitachi found a simple solution: a multilayer top electrode that's durable under high electric field stress (12 to 15 MV/cm). The result is a device with stable electron emission and current density of 5.8 mA/cm^2.

Session 36, "Detectors, sensors, and displays—detectors and MEMs," discusses the latest developments in detectors and MEMS. One development comes from the Physical Electronics Laboratory in Zurich, Switzerland. As detailed in "Single-chip CMOS anemometer," researchers successfully developed a packaged single-chip anemometery microsystem. The device is based on a membrane composed of the entire sandwich of dielectric layers of the CMOS process. An integrated polysilicon resistor serves as a heater. Two polysilicon thermopiles are used to measure the temperatures at two different locations upstream and downstream of the heater. During operation, a gas flow over the sensor distorts the temperature distribution on the membrane. The resulting differential thermovoltage is dependent on air flow velocity and provides the output signal.

The anemometer is comprised of a thermal CMOS flow sensor with on-chip power-management, signal-conditioning, and analog-to-digital (ADC) circuits. The device is made on a standard IC process and post-processing micromachining. Its flip-chip package is implemented on a flexible substrate. The anemometer has a 0-38 m/s air-flow range, a 65-dB dynamic range, and 3 mW power consumption.

At Simon Fraser University, British Columbia, Canada, researchers developed a micromachined accelerometer that is simple, reliable, and inexpensive to make. It's composed of a small silicon substrate with an etched cavity for thermal isolation. A central heater is suspended in the cavity. When the accelerometer is heated, it lowers the density of the air surrounding it. Two temperature sensors, also suspended, are positioned at equal distances from the heater and measure the differential temperature. When acceleration is applied, the device is disturbed. The resulting temperature difference measured by the two temperature sensors produces an output corresponding to the applied acceleration. The device features 0.6 milli-g sensitivity and can theoretically be extended to the submicro-g level.

How Valuable	Circle
Highly	542
Moderately	543
Slightly	544

PRODUCT FEATURE

Visual Development and Automatic Code Generation Targets DSPs

Code Composer Version 5.0, designed by GO DSP, attempts to bring the same level of visual development tools to the DSP world that have become familiar for desktop and embedded microcontroller applications. It is an integrated development environment for DSP applications that incorporates⇓in one tool⇓wizard-based setup, visual signal analysis,

multiple window source and assembler editing, multiprocessor debugging, and project management.

To get started, there's a sub-tool called Memory Composer that lets you visually specify the memory configuration of the target system. As you modify the memory configuration, the changes are shown graphically. Next, all aspects of CPU configuration can be specified with a dialogue box that leads you through the process, offering defaults in cases where there may be doubt. The sub-tool then automatically generates a linker command file and initialization code.

Another sub-tool, the Application Framework Composer, offers a dialogue-based process for setting up all on-chip peripherals and creating code for their use. Initialization code, interrupt handlers, and vector table entries are all created simply by specifying their desired properties. You can also create buffers and connect them to the peripherals. The generated code blocks are tracked by a database and closely associated with the project-management facilities of Code Composer 5.0.

The integrated source code editor is designed to resemble that of Microsoft Visual C++, but is tuned for writing C and DSP assembly code. The editor features floating toolbars, colored syntax highlighting, and multiple windows for editing multiple source files. The editor is integrated with the memory and framework composers, and the debugger. As a result, you can click and move between them when working on the same piece of code.

The debugger also features multiple windows an displays interleaved source and assembly code. Conditional and hardware breakpoints can be based on full C expressions, which are local variables of CPU register symbols. The debugger can be set to automatically capture signal data at selected points for later analysis. For the TMS320C2xx, there's a JTAG monitor capability for capturing data without halting the processor. For large systems, a parallel debug manager provides synchronized control over multiple processors, which can be observed in separate windows and managed through a parent window. Global breakpoints also can be set for multiprocessor systems. A background compiler facility lets you compile while editing or debugging.

Code Composer 5.0 provides another type of breakpoint called a probe point. A probe point defines a point in an algorithm where you can inject signal data or take a snapshot of memory and display an oscilloscope-like trace. For example, at one probe point, known signal data can be injected from a disk to simulate input. At another probe point, the debugger can run a script to execute, for instance, a test script, and log data to disk. At a third probe point, it can display a graphical snapshot of memory. Moreover, you can attach probe points to different places in the algorithms and route them to the same data visualization window. This lets users watch how the signal progresses through an algorithm during debugging.

There are numerous kinds of data visualization available in Code Composer 5.0. You can choose general time and frequency domain analysis as well as windows designed for communications such as eye and constellation diagrams. There are 2D and 3D Cartesian grids, 3D parallel Cartesian grids and 2D polar graphs with color coding, among others. As an option, Code Composer 5.0 supports the 3D Logitech Space Mouse to help "fly" through data displays.

Code Composer 5.0 provides a visual project-management system and a workgroup development environment. The project-management system lets you use Project View to view file organization and access all files from a single window. Files are organized into functional categories such as source files, include files, and libraries. Files can be dragged and dropped from the Windows file manager to add them to a DSP project. A linker view displays a visual representation of the linker command file generated by the memory composer.

The workgroup environment provides an interface to Microsoft Source Safe or Intersolv's PCVS version control tools. This lets users on a network "check in" and "check out" files to work on from a central repository, and keeps track of the versions and revisions made to them. It also lets users connect to the appropriate target board over the network from their own host machine.

Code Composer 5.0 runs on Windows 95 and WindowsNT and supports Texas Instruments' TMS320 series of DSPs. Pricing starts at $2000, depending on options.

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CIRCLE 487

TOM WILLIAMS

Drag-and-Drop Integrated Development Environment Supports DSP Applications

A graphical development and prototyping environment for DSP and data acquisition applications uses a block diagram, device-independent approach to design. The real-time integrated development environment, called Hypersignal RIDE, supports

(continued on page 64)

(continued from page 63)
various available DSP and data acquisition boards and greatly reduces the need for software coding.

The RIDE environment is a superset of the Hypersignal Block Diagram tool from Hyperception and DSP hardware awareness and Windows DSP board drivers. The drivers handle communication and control of the DSP environment from the PC environment. The DSP hardware can be virtualized to eliminate the need for a plug-in board. The driver communicates with an installed board driver without dealing with the specifics of a given DSP. The development environment can be a mix of hardware (run the DSP) and simulated (on the host PC) functions.

The development process involves placing block functions, such as filters, FFTs, and multiplexers, on a worksheet and connecting them to form a data flow. Run-time parameters then can then be adjusted via pop-up dialog boxes. By clicking on a button, they'll run with the algorithm. In addition to the some 300 functional blocks supplied with the tool, you can customize existing blocks, create your own blocks using the block wizard, or use third-party block libraries.

RIDE includes a DSP object linker that links all referenced DSP object modules and library functions, builds the DSP application, and loads it into DSP memory. When a block diagram worksheet is compiled, RIDE creates and maintains a symbol table for each DSP resource. The symbol information is used for debugging with RIDE or for using third-party debuggers. An application can be exported to a DSP executable object file in common object file format (COFF). As an option, the design can be translated to ANSI C source code with the automatic code generator.

Profiling support includes displaying the number of times a block executes, the cycles for each execution, and the total number of cycles executed since reset. Relative execution statistics in terms of percentages can be displayed to view the relative resource utilization of all blocks. Profiling can be turned on even when the design is executing for on-the-fly analysis.

RIDE can provide a system summary for any selected DSP resource, including block, symbols, profiling, and memory information. For real-time applications, DSP interrupt support lets you associate any real-time block or block diagram with a particular DSP interrupt. This makes it possible to design interrupt handlers graphically without having to deal with the intricacies of interrupts on various DSPs.

Hypersignal RIDE is priced starting at $3995 and $8995 with the optional C source generator.

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CIRCLE 488
TOM WILLIAMS

FPGA Family Features Improved Flexibility, Lower Cost

The high density and small chip area of Actel's antifuse one-time programmable technology, now transferred to a 0.45-µm triple-level metal process, has allowed the company to craft a new high-density family of FPGAs called the MX series. With chip complexities from 2000 to 52,000 logic gates, the seven-member MX family offers enhanced routing resources over the company's previous-generation dual-level metal designs. It implements the arrays in smaller chip areas, and keeps silicon cost considerably lower than SRAM-based alternatives and cost-competitive to SRAM-based designs that employ 0.35-µm design rules.

Three of the seven A40MX family members will include selectable PCI support—the MX24, 36, and 52, which contain the equivalent of 24, 36, and 52 kgates, respectively. The chips also handle wide decoding of 24 or 28-bit wide data. The other family members—the MX02, MX04, MX09, and MX16—have gate capacities of 2, 4, 9, and 16 kgates, respectively. The arrays include dedicated flip-flops, ranging from 147 on the MX02 to 1888 on the MX52. I/O lines on the arrays range from 57 on the MX02 up to 240 on the MX52. Lastly, the two largest devices, the MX36 and MX52, include dedicated blocks of dual-port/single-port RAM that can access in just 5 ns—2500 bits on the MX36 and 3 kbits on the MX52.

Like other antifuse designs, the MX series requires no off-chip memory or configuration downloads, providing added system cost and board-area savings over systems that require EPROMs or other off-chip storage. And, the chips are ready to operate in under 100 µs—almost 1000 times faster than SRAM-based FPGAs.

The chips are logic-compatible with the company's Act 1, XL, and DX families and include redesigned clock buffers and clock-distribution networks to reduce the clock-to-Q (pad to pad) times to as little as 5.6 ns. That represents a 100% improvement over the company's XL- and DX-families. On-chip datapath structures can thus run at speeds of up to 270 MHz. For example, a 16-bit adder can run at 96 MHz, and a 16-bit counter at 156 MHz.

A key improvement in the MX series is a MultiPlex I/O cell that includes selectable enhanced 3.3-V input switching. Designers now can obtain optimum I/O performance when interfacing to 3.3-V components, or delivering full 5-V swings for 5-V systems. The MX devices can be set to operate in pure 5-V or 3.3-V systems or in mixed 5-/3.3-V systems.

Configuring the MX FPGAs is similar to similar Actel-family devices; the suite of design tools in the company ACT series provides 100% automatic logic synthesis, placement, and routing. In 50,000-unit quantities, prices for the MX-family FPGAs start at $2.90 apiece for the MX02 and increase to $69 each for the MX52 (prices are for purchases in mid-1998). Initial sample costs will be considerably higher. Samples of the MX02, 04, 09, and MX16 are now available, while the MX24 and MX36 will be released in the first quarter of 1998. The MX52 will be ready for sampling in the second half of 1998.

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http://www.actel.com
CIRCLE 489
DAVE BURSKY

ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

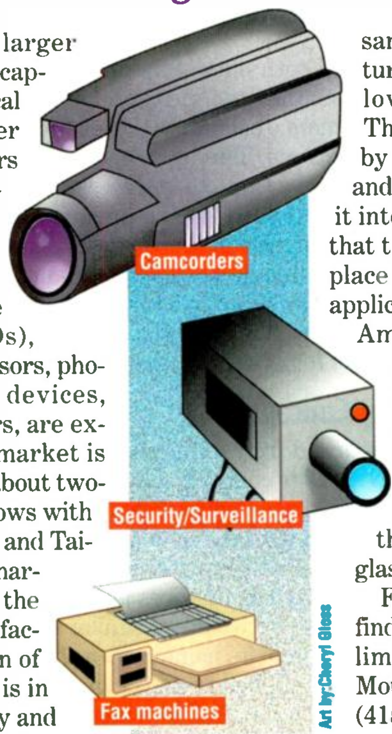
MARKET FACTS

Image Is Everything

If you've ever had the feeling of being watched, well you may have been right. The primary component in camcorders and security and surveillance cameras is becoming more technologically advanced and less expensive to manufacture. Thus, the products that use image sensors, such as digital still cameras, machine-vision cameras, security cameras, and videoconferencing are becoming available to a larger market. Based on silicon, image sensors capture an image and convert it to an electrical signal, which is then processed for either storage or display purposes. Image sensors are projected to jump from a $678.4 million market in 1996 to a $1.564 billion market in 2001, according to "Image Sensor Market Review and Forecast, 1997," from Strategies Unlimited. In the report, charge-coupled devices (CCDs), CMOS image sensors, contact image sensors, photodiode arrays, and charge-injection devices, among other categories of image sensors, are examined. The worldwide image sensor market is dominated by Japan. The country takes about two-thirds of the market. North America follows with about 20% of the market. Europe, China, and Taiwan make up the bulk of the rest of the market. Japan mainly produces CCDs, while the majority of the CMOS sensors are manufactured in the U.S. The largest application of image sensors, according to the report, is in camcorders (25% of the market). Security and surveillance cameras come in second, with fax machines trailing in third. The cameras you see at your local convenience store, gas station, or even traffic light typically use CCDs, but there is a move toward CMOS image sensors because the prices for these components are falling. The fastest-growing application of image sensors is in the digital still camera category. What companies are doing now is trying to produce mega-pixel sensors. These high-pixel (a million pixels or more) sensors were originally priced at over $1000 per sample in 1996. This year, sensor manufacturers are exploring sample pricing rates as low as $80 to $100 for high-pixel CCDs. These digital still cameras are mainly used by insurance adjusters, lawyers, publishers, and real estate agents, and have yet to make it into the consumer market. The real issue is that the resolution still isn't good enough to replace the 35 mm camera. Another interesting application is in the medical end of the market. Amorphous silicon sensors, which are more radiation-tolerant than CCDs, also are capable of producing a larger field of view for the physician. Typically, doctors had difficulties with distortion since the image had to be shrunk due to silicon limitations. Amorphous silicon sensors, on the other hand, use a layer of silicon over a glass substrate.

For more information on the report and its findings, readers may contact Strategies Unlimited, 201 San Antonio Circle, Suite 205, Mountain View, CA 94040; (415) 941-3438; fax (415) 941-5120; Internet: http://www.strategies-u.com.—**DS**

The Three Largest Markets for Image Sensors



Source: Strategies Unlimited

Purdue Teams With Industry

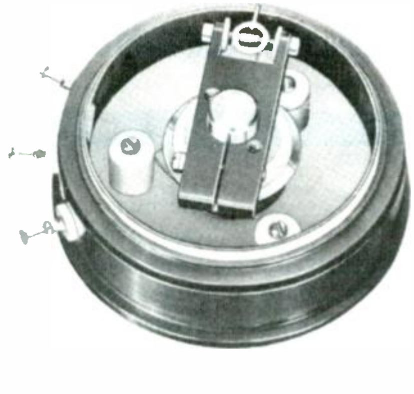
It appears to be a trend that's here to stay: universities pairing with national and international companies. Of course, there's the money, but more importantly, there's the research. One Purdue University associate professor of mechanical engineering, Raymond Cipra, says that in reality, the concept is based on exposing students to more open-ended projects earlier on in their careers.

One company, Dynamic Corp., asked the students in the Senior Design class to fashion a portion of the braking system for an electrical car. In the process, the students were guided by the company's engineers, who gained fresh perspective.

For further information on this program, readers may contact Purdue University, 1132 Engineering Administration Building, West Lafayette, IN 47907-1132; (765) 494-2096; fax (765) 494-0401; Internet: http://www.purdue.edu.—**DS**

40 YEARS AGO IN ELECTRONIC DESIGN

Vibration Resistant Balanced Potentiometer



A dynamically balanced wiper arm guarantees constant contact in this potentiometer. Accuracy and continuity are thereby assured, regardless of system vibration or operating speed. The resulting low wear gives the potentiometer a 5 million cycle life. The new potentiometer, developed by the Kintronic Division, Chicago Aerial Industries, 10265 Franklin Avenue, Franklin Park, Ill., matches mechanical performance to electronic precision. Previous potentiometer design used a cantilevered spring to provide contact with the wire. When subjected to vibration the unbalanced mass of the arm and spring caused it to rotate and give a positioning error. In applications requiring the wiper to rotate at high speeds, centrifugal force increases pressure on the winding, causing excessive wear.

When the mass of the wiper arm is balanced on both sides of the shaft, vibration or shock will not result in a rotational force on the arm, and therefore accuracy is not affected. Extending the concept of dynamic balance to the contact allows it to follow the winding under all conditions. The balanced contact assembly is mounted in jewel pivots at the end of the arm. As in the case of the arm, vibrations will not cause it to rotate or bounce. Standard linearity for these dynamically balanced potentiometers is 0.1 %. The units will give continuous operation with a minimum of noise when subjected to vibrations up to 2000 cycles at 30 g's. Maximum speeds range from 1000 to 3425 rpm depending on the size of the potentiometer. *(Electronic Design, Dec. 1, 1957, p. 29)*

These precision pots were part of the feedback loop in servo systems.—**SS**

The Magnetic Twistor: A New Memory Concept

A new concept in memory devices has emerged from exploratory work at Bell Telephone Laboratories, New York, N.Y. This concept, which has been named the "Twistor," is expected to make possible memory systems which are simpler to fabricate and more economical to manufacture than existing systems. The Twistor concept opens the way for the construction of magnetic memory arrays by merely interweaving horizontal copper wires and vertical wires, much as window screen is woven. Such a device would be similar in appearance to a ferrite core array. This new concept gets its name from a characteristic of wire made of magnetic material. Torsion applied to such a wire shifts the preferred direction of magnetization from a longitudinal to a helical path. The coincidence of a circular and longitudinal magnetic field can then be used to insert information into this wire in the form of a polarized helical magnetization, and the magnetic wire itself can be used as a sensing means.

In practice, the circular magnetic field is provided by a current pulse through the magnetic wire, and the longitudinal field by a current pulse through the copper wire, which is perpendicular to the magnetic wire. Thus, storing a bit requires two coincident current pulses. Readout is accomplished by overdriving the longitudinal field in the reverse direction. The readout signal is sensed across the magnetic wire. *(Electronic Design, Dec. 15, 1957, p. 6)*

This type of memory was used in the Bell System's first electronic switching system, the No. 101 ESS. Using transistor circuitry, these computers went into service in 1963 in Cocoa Beach, Fla., according to "A History of Engineering and Science in the Bell System," published by Bell Labs in 1982.—**SS**

JUST A REMINDER

If you've been working on your paper airplane (and even if you're not), there are a few things you might want to keep in mind while you are designing. Those individuals who are looking to bowl us over by producing (against all odds) a plane that will fly right out of the box should definitely label the box with warnings and include an audible signal when the box is opened. Also, we're going to need an explanation of your technology and design to help us in our judging.

Now, if you're completely lost, what I'm referring to is the First Annual QuickLook Paper Airplane Contest. *Electronic Design* and 1-800-BATTERIES are sponsoring the contest with the winners enjoying a first prize

1-800-Batteries

of a $150 gift certificate and a second prize of a $50 gift certificate, both to be used with 1-800-BATTERIES' catalog. The battery company also is offering a 3-V battery to the first 100 engineers who send us a self-addressed stamped envelope (SASE)—you'll find the address below.

Here's a quick breakdown of the rules, although, by this time you really need to have it done and be in the testing phase (reminiscent of Y2K):

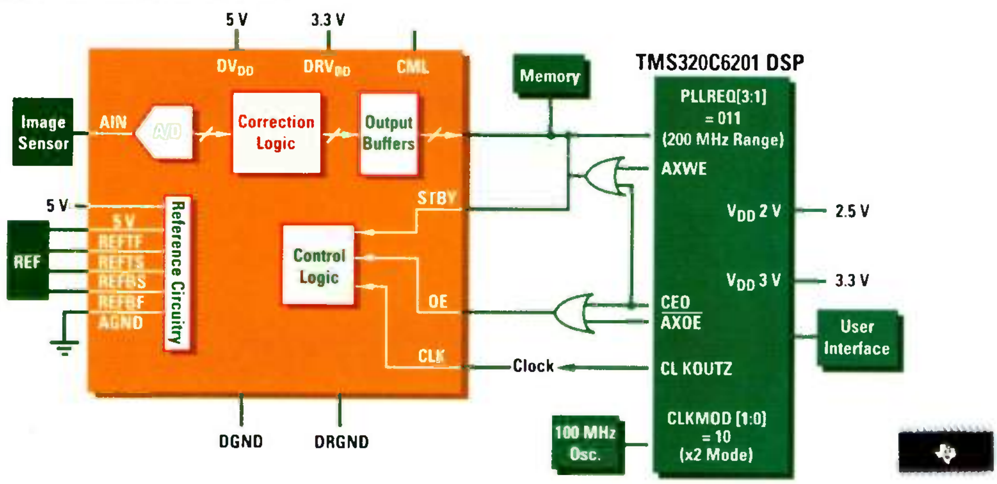
- Paper should be no more than one-eighth of an inch thick (and paper means paper, not balsa wood or plastic sheeting).
- The plane must be fully assembled when it gets to our offices.
- The plane can be no larger than 3 ft. in wingspan.
- The plane must be able to demonstrate properties of flight over a distance of 12 ft.

No planes will be returned, and the deadline for entries is January 1, 1998.

Send all SASEs and entries to QuickLook Editors, *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Any questions can be sent directly to Deb Schiff at: debras@csnet.net or (201) 393-6221. Good Luck!—**DS**

LOW-POWER, 10-BIT, 20-MSPS ADC.

TLC876 interface to 'C6x DSP



TLC876 starting at only $2.89*

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- *107-mW (typ) power consumption*
- *DNL = ±0.5 LSB*
- *5-ns vs. 105-ns enable and disable times improve bus efficiency*
- *2-V analog input range can include 0 VDC*
- *2X the impedance of the reference input*

**Price is per device in quantities of 1,000.*

Introducing the TLC876 from TI. A single-supply ADC that delivers the high speed and high resolution you need for high-performance applications like digital video systems, digital cameras, scanners and communications systems. And at only 107 mW, the TLC876 reduces power consumption 33% versus the competition. With enable/disable times reduced to only 5 ns, the TLC876 significantly improves bus efficiency and system throughput. The TLC876 delivers DNL of less than 1 LSB and 54 dB of SNR. Reference input impedance is 2X higher than the competition. And the TLC876 analog input is specified as low as ground, eliminating level shifting stages prior to the ADC, saving board space and cost.

For free data sheets or EVM information, contact us at:

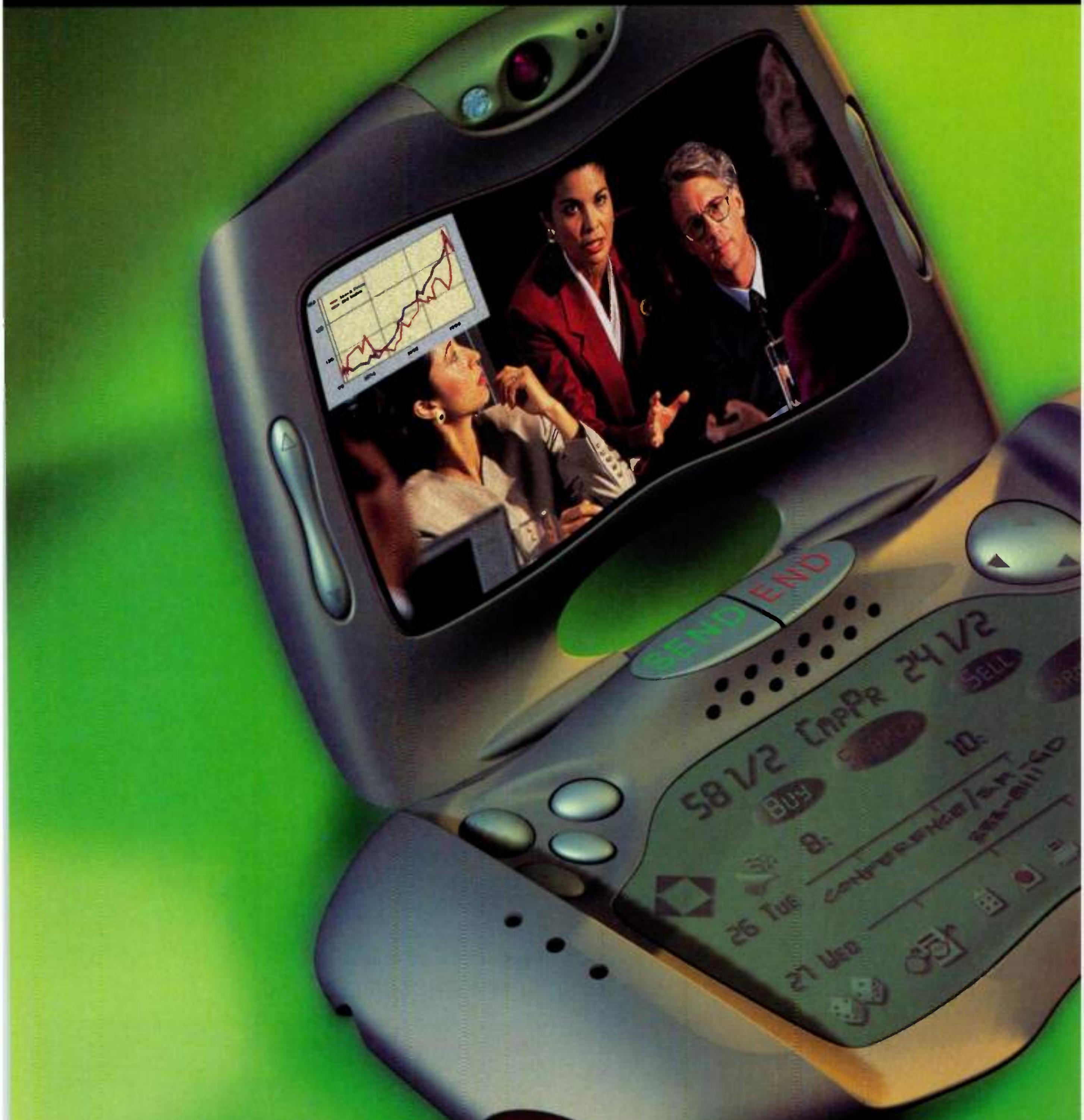
1-800-477-8924, ext. 5050, or www.ti.com/sc/5050

1830-03

MIXED SIGNAL & ANALOG

TEXAS INSTRUMENTS

READER SERVICE 178



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New Initiative For Attracting Talent In Scotland

A major training initiative has been launched to ensure that Scotland continues to attract the international electronics industry with the country's pool of highly trained labor at all technical levels.

The establishment of a National Microelectronics Institute (NMI) based in Heriot-Wall University, Edinburgh, was announced last year, but has now officially opened.

The Institute, housed in a 2500-square foot facility in the university's Research Park, will have a small central office of eight people by early next year, headed by chief executive Clive Dyson, formerly of GEC Plessey Semiconductors.

It has already held a number of workshops aimed at secondary education colleges. These workshops are designed to create common standards for technicians in collaboration with the semiconductor industry.

While facilitating training and strengthening the skills base is a primary function, the NMI also is talking aim at improving business processes; improving the industry's support infrastructure; and building on existing facilities in universities, colleges, equipment and material suppliers, and fabrication plants. NMI's aim is to provide the increased availability of skilled technicians and engineers for the industry and promote further development.

A Scottish site was chosen because of the high concentration of semiconductor fabricators and equipment suppliers in the country. The semiconductor industry in Scotland accounts for 60% of U.K. production. When the latest fabrication plant is opened by Hyundai in 1998, it will employ 9000 people.

The NMI initiative was led by Motorola, which has two plants in Scotland. It has strong support from the Scottish Electronics Forum, the Scottish Office, and Scottish Enterprise. Dr. George Bennett, head of Motorola's operation in Scotland, is the first chairman of the Institute. The board will comprise general managers or chief executives of the companies involved, in addition to a government representative.

Participating companies include Motorola, National Semiconductor, NEC Semiconductors, and Seagate Microelectronics based in Scotland; Siemens Microelectronics, Siemens AG Semiconductors, Fujitsu Microelectronics, GEC-Plessey, and Newport Wafer Fab, based in England and Wales.

There are now 24 wafer fabrication facilities within the U.K. at present. The NMI will be recruiting more members among those companies and their related suppliers.

For more information on the initiative, contact the Al Paul Lefton Company, 100 Independence Mall West, Philadelphia, PA 19106; (215) 923-9600; fax (215) 351-4298; Internet: http://www.lefton.com.—**MS**

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READER SERVICE 177

Another "Top Ten" List

And now, from the home office in Arlington, Va., it's the Electronic Industries Association's (EIA's) top 10 list of foreign markets for electronic exports, along with the top 10 trading partners for electronic imports for 1996! (Sustained applause follows.)

OK, maybe it's not the most glamorous introduction, but the information contained here is pretty important. The EIA, a national trade organization representing U.S. electronics manufacturers, has compiled a list of the U.S.' best import and export partners.

Heading the list of U.S. export markets for electronics equipment is Canada, with a total of $20.8 billion for 1996, a

Top 10 Export Markets for U.S. Electronics (millions of dollars not seasonally adjusted)

	1996	1995	% change
Canada	20,845	19,340	7.8 %
Japan	16,041	13,653	17.5 %
Mexico	11,413	8,824	29.3 %
United Kingdom	8,438	9,126	-7.5 %
Singapore	8,307	7,432	11.8 %
Germany	6,912	6,614	4.5 %
Korea	6,808	5,902	15.4 %
Taiwan	5,088	4,585	11 %
Malaysia	5,009	5,643	-11.2 %
Hong Kong	4,608	4,608	0.0 %

Top 10 Import Markets for U.S. Electronics (millions of dollars not seasonally adjusted)

	1996	1995	% change
Japan	38,078	41,837	-9.0 %
Singapore	17,034	15,322	11.2 %
Mexico	14,473	12,108	19.5 %
Taiwan	14,193	12,999	9.2 %
Malaysia	13,262	13,170	0.7 %
Korea	11,947	13,324	-10.3 %
Canada	10,398	9,648	7.8 %
China	9,285	7,929	17.1 %
Philippines	4,311	3,037	42 %
Thailand	4,155	4,066	2.2 %

Source: Electronic Industries Association

7.8% increase over 1995. Finishing in second place was Japan with $16 billion, a 17.5% jump over last year's total of $13.6 billion. Coming in third was Mexico with $11.4 billion, a whopping 29.3% increase over its 1995 total. According to the EIA's analysis of U.S. Department of Commerce export data, these three markets alone comprised 36% of the $135.4 billion total electronics export market for 1996.

And now for what the United States takes in. Of the top 10 major foreign suppliers of electronics products to the U.S., Japan retains the top spot with sales of $38 billion in 1996, despite a drop of 9% from last year's figures. Singapore ranks second with $17 billion, and Mexico finished in third place with $14.5 billion in sales. The top 10 markets accounted for nearly 87% of the total import market for 1996.

For additional information on the survey itself or on the organization's activities, interested readers may contact the Electronic Industries Association (EIA), 2500 Wilson Blvd., Arlington, VA 22201-3834; (703) 907-7500; fax (703) 907-7501; e-mail: publicaf@eia.org; Internet: http://www.eia.org.—MS

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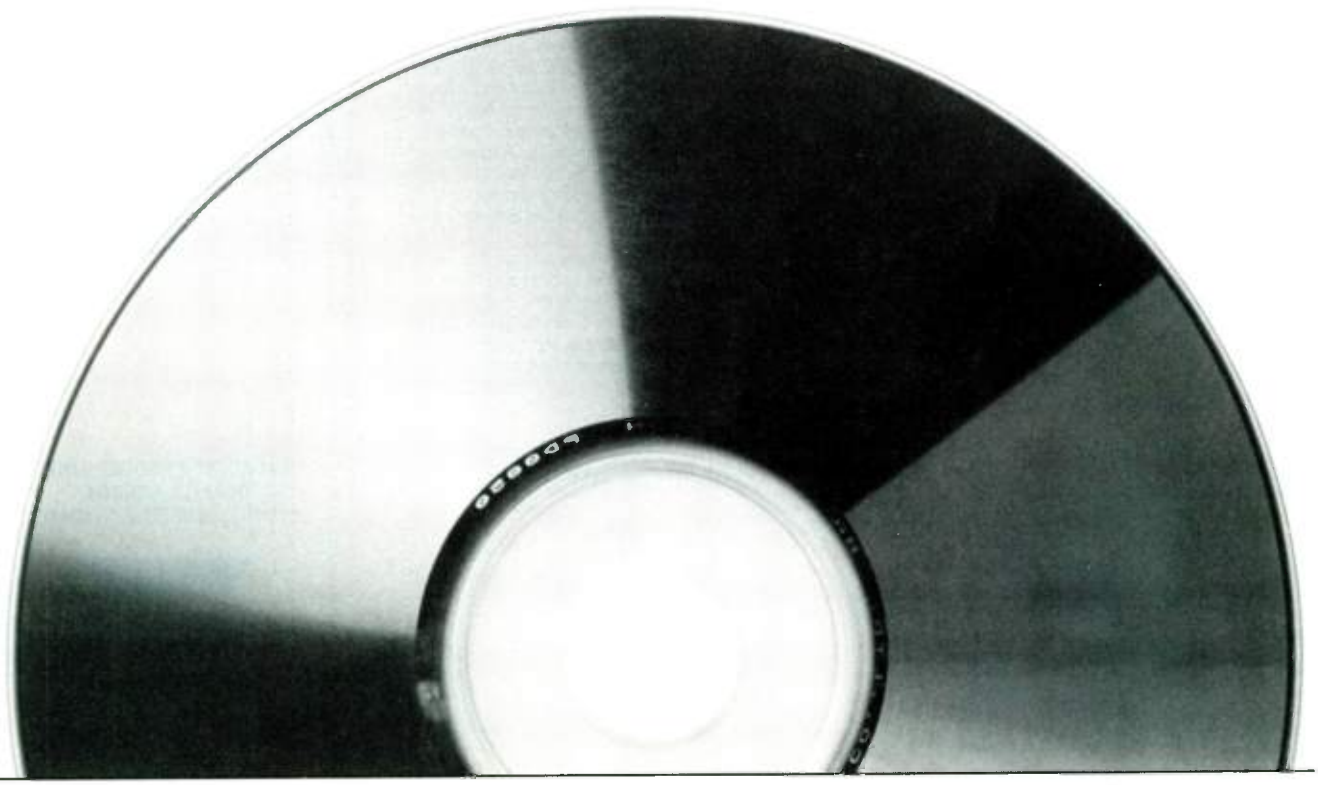

(WHEN A PIECE OF TECHNOLOGY LIKE THIS COMES ALONG, WE'RE GOING TO SUPPORT IT.)

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KMET'S KORNER

...Perspective on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

A fine product effectively marketed and sold sets the stage for business growth and prosperity. But in today's marketplace, product, marketing programs and sales efforts tend to blur together. As suppliers segment and then saturate markets, consumers face consternation in making a choice. Depending on market size, thousands of players compete for each individual purchase as they attempt to grow market share. If consumers are confused, think about what it's like inside the sales and marketing departments of companies trying to capture the consumer's money. All parties seem to shuffle from one trend to another, resembling the motion of Mike Ditka on the sidelines.

But occasionally, a truly inspiring market leader emerges from the pack. How do they do it? The following account leads to the answer.

I like music and maintain a modest home collection. When near my PC or stereo system, I insert a disk and turn up the volume. But I'm not always home, and I like to take my music with me. To do this, I duplicate a CD onto tape—a time-consuming process I detest. The tape then plays on the road or on a portable cassette player. Since portable players are cheap, I stuff my bag for each individual activity with a player of its own. So, as my CD collection grows, my tape collection expands proportionately.

A few years ago, CD players appeared on the market with shock protection.I bought one thinking I could bypass the tape-duplication process and play a CD on the move. Well, reality did not conform to my expectations. I couldn't ski, bike, or run with this unit—it could handle a waltz on a foam dance floor. I gave up on portable CDs and returned to messy, unorganized, undocumented, tapes.

Recently, I went out to buy a better portable CD player. Much to my surprise and bewilderment, I had to select one from over three dozen on display. I asked the saleswoman which one offered the best performance while in motion. She said that one unit was superior to all others, handed me a CD, and instructed me to figure it out for myself. I couldn't refuse the challenge!

I ran an in-store experiment and in ten minutes, found the most shock- and vibration-tolerant unit on display. I was impressed with its superiority. The saleswoman saw my smile and returned to congratulate me. She said this unit outsold all others in the store combined. I left with a Sony D-E301—a great product!

RON KMETOVICZ
CONTRIBUTING EDITOR

Yes, products with superior performance, offered at a reasonable price, command consumer respect. And amazingly, the best products need the least amount of marketing hype and sales push. It's the opposite—they sell themselves with limited marketing.

My message to product developers: focus on making a superior product for its intended application; restrict its features, and make it perform. With a great product in hand, establish a supportive marketing and sales effort. Don't think that marketing and sales can compensate for an inferior product.

To obtain an e-mail copy of "The Complete List for Late Product Information," readers may contact Mr. Kmetovicz at kmetovicz@aol.com.

Y2K UPDATE

We're here, we're old enough to be your parents (and grandparents in some cases), and we're going to fix the Year 2000 Date Change (Y2K) crisis. That may not quite be the anthem of The Senior Staff, but these over-50-year olds are giving a new meaning to the word empowerment. The Senior Staff 2000 is a well-equipped database of professionals who just happen to be over 50, and qualified to perform Y2K conversion. The database is seeing additions of 1000 people per month.

The group maintains a Job Information Databank that contains about 3000 professionals who are seeking full-time, part-time, and interim positions in manufacturing and service enterprises. These professionals are employed in any number of positions from receptionist to CEO. The international registry is free to information technology (IT) professionals. Employers pay a modest fee for detailed profiles of candidates with skills and experience. The Senior Staff is not an employment agency or headhunter; it's simply an information databank.

One of the biggest problem with Y2K conversion projects is that the younger crowd is uninterested in reprogramming computers that were designed in what they would term the dark ages. Therefore, more companies are turning to The Senior Staff for their compliance needs. Fujitsu Software, for one, is providing software and instructors to Senior Staff 2000 to retrain the retired programmers. The course on COBOL is given as part of a three-week course offered at the University of California, Santa Cruz Extension. There is a substantial discount to Senior Staff 2000 members.

The main draw to these programmers is that they are very familiar with the COBOL programming language that's historically been used with mainframe computers. These "ancient" mainframes are destined to fail at the turn of the century unless an experienced, knowledgeable programmer gets to the code and either repairs it or builds a bridge around it. The younger programmers, who've been trained in Java and C++, simply don't have the skills to do the work at hand.

Some of the Gartner Group's latest numbers concerning Y2K say that 600,000 programmers will be needed to solve the Y2K problem in time (already too, late for most, though, if they're only beginning to recognize the problem as you read this). But, there are only 200,000 available programmers in the "conventional" workforce. As a result, retired or consulting programmers are being enticed back into service. The companies choosing their nontraditional programmers (misnomer or pun, you decide) from many sources, but the biggest choices are listed with The Senior Staff.

The job candidates are proficient in over 70 languages and computing platforms. On a self-rated system, 70% of The Senior Staff members are, on a scale of one to five (with five being "Guru"), at a skill level of three or better. Many of the members are available for regional, national, or international assignments.

Contact The Senior Staff, P. O. Box 1382, Campbell, CA 95009-1382; (408) 371-9604; fax (408) 371-3255; Internet: http://www.srstaff.com.—**DS**

HOW DOES IT SOUND?

If a tree fails in the forest, can you hear it from six different perspectives? The real question is, if you're watching a tree falling in the forest on your new television, are you hearing every nuance of the tree crashing to earth in Dolby Surround sound? If you've been watching more TV than usual lately, it might just be because you have a set equipped with Dolby Surround or you have a home-entertainment setup that allows you to hear Dolby Surround. A few years ago, there weren't many programs transmitted in Dolby Surround, but that has changed drastically, with the fall season opening with over 69 regularly scheduled programs that are encoded with Dolby Surround.

According to Dolby Laboratories, over 15 million American households are watching and listening to televisions that are equipped with Dolby Surround decoders. Because the home-theater element of viewing a television program such as the "X-Files" is so important to many viewers, most production companies are incorporating Dolby Surround in their projects. Despite the fact that there are other surround formats on the market, production companies frequently turn to Dolby because they invented the system which is touted as the best.

Currently, over 28 million Dolby Surround decoders are in use worldwide. Additionally, there are more than 7000 programs encoded with Dolby Surround. If you walk into a theater, odds are that it's one of the more than 41,000 that use Dolby processors. Dolby Digital, the newest version of digital surround sound technology, is being used in over 1000 films. This technique uses 5.1 discrete channels of sound to produce the surround sound effect. Catching up to its older cousin, over 11,000 movie screens use Dolby Digital processors. As far as consumers are concerned, over 283,000 Dolby Digital decoders are in use today.

For more information on these developments, contact Dolby Laboratories Inc., 100 Potrero Ave., San Francisco, CA 94103-4813; (415) 558-0200; fax (415) 863-1373; Internet: http://www.dolby.com.

The AK7712A is an integrated Codec that provides a dynamic range of 97 dB for both the analog-to-digital and digital-to-analog channels. It performs this act by using a proprietary delta-sigma architecture. The new Codec yields 3D audio that gives a new meaning to turning the dial on a car radio.

AKM Semiconductor brought the new sound to the DSP through teamwork with Aureal, Dolby, QSound Labs, and SRS. The companies lent their high-end algorithms to enhance audio to the point where listeners not only hear the difference, but they feel it as well. Even with the 3D enhancement algorithms, the AK7712A still has enough power left over to add reverberation, echo cancellation, and other functions.

The Codec comprises a 20-bit stereo analog-to-digital converter (ADC), four 20-bit output digital-to-analog (DAC) channels, and a proprietary 24-bit fixed-point DSP. The AK7712A allows designers to play with 383 instruction cycles, with up to six operations per cycle. The audio sample rate is 48 kHz.

Japanese automakers are already using the AK7712 in their car audio applications. It features a smaller die and more competitive pricing. Its package is of the 100-lead LQFP variety, and is priced at $19.50 at 5000 pieces.

For more information, contact AKM Semiconductor Inc., 2001 Gateway Pl., Suite 650 W, San Jose, CA 95110; (408) 436-8580; fax (408) 436-7591; Internet: http://www.akm.com.

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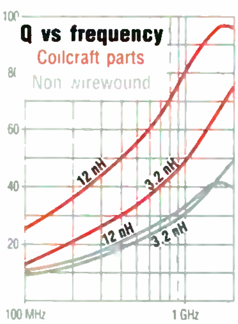

Compare our new 0603 coils to comparable non-wirewound parts, and you'll find significant performance advantages. Our Q factors are often twice as high, SRF's are 50 to 70% higher, and DC resistance is three to four times lower!

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100 nH	1400	830	.58	2 50

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QUICKNEWS

New Kid On The Block—Introduced at the Audio Engineering Society meeting in September, *V&T News* is the newest publication in the audio industry that addresses issues in the vacuum tube sector. The letters "V" and "T" stand for Valve and Tube. *V&T News* joins *Audio Electronics*, *Speaker Builder*, *Glass Audio*, *Voice Coil*, *The World Tube Directory*, *The Loudspeaker Industry Sourcebook*, and various educational books from Audio Amateur Corporation.

The publication is free to all qualified subscribers in North America and also is available outside North America for $50 a year.

The first issue highlights industry news and developments such as a new Class A stereo;a fully integrated amplifier from Rogers International; a Russian/American joint venture to produce electron power tubes and glass vacuum tubes; a new tube microphone design from Neumann USA; a new Class A 13-W per channel transformer-coupled triode amplifier; and tube amplifiers and preamps from GRAAF.

The *Industry Watch* section focuses on personnel changes, new web sites, improvements in manufacturing, new product releases, and new technologies. The publishers are interested in web site information, so feel free to contribute. Actually, they're interested in *any* contributions having to do with the tube-audio industry.

Don Jenkin's Test Bench gives a description of the steps to take while measuring and analyzing vacuum-tube characteristics. In this issue, performance data was examined from the standpoint of the relationship of the tube-plate current to grid bias, plate voltage, screen voltage, and plate-resistive loads.

Finally, there is a brief calendar listing. If interested, send information to: *V&T News*, P.O. Box 576, Peterborough, NH 03458-0576; (603) 924-9464; fax (603) 924-9467; e-mail: audiotech@top.monad.net.

How Does A Tape Drive?—Quantum Corporation and Compaq have linked Quantum's DLT 7000 tape drive on Compaq's servers and storage line. The result is the new Compaq 35/70 GB DLT drives, which are available in rack-mounted versions, storage arrays, and tabletop configurations.

Quantum's DLT 7000 offers a 70-Gbyte compressed capacity and a 10 Mbytes/s (compressed) data transfer rate. With a SCSI-2 fast/wide interface, the tape drive features single-ended and differential options.

The drive is of the standalone variety. Sporting a head life of 30,000 hours, the mean-time between failures is 200,000 hours overall. Quantum's DLT 7000 also features a media durability of 1 million tape passes.

For more information, contact Quantum Corporation, 500 McCarthy Blvd., Milipitas, CA 95035; (408) 894-4000; Internet: http://www.quantum.com.

XaQti's Big MAC—At the recent Networld + Interop Conference, XaQti Corp. premiered a XMAC II 0.35 µm low-power CMOS Gigabit Ethernet Media Access Controller. The new device is compliant with the IEEE 802.3z D3.1 proposal. It also can be used with gigabit buffered repeaters, switch uplinks, and probes. It supports full-duplex operation, carrier signal extension, and packet bursting. The chip is priced at $60 in 10,000-piece quantities.

Gigabit Ethernet designers may be interested in the Gigabit Development Kit that allows users to generate and process gigabit packets for prototyping and testing.

For more information, contact XaQti Corp., 1630 Oakland Rd., Bldg. A-214, San Jose, CA 95131; (408) 487-0800; fax (408) 487-0801; Internet: http://www.xaqti.com.

INTERNET NEWS

In December there's a vibration that rocks the New York metropolitan area for a week, and that's Fall Internet World (FIW '97). With the explosion of small start-ups in Silicon Alley and the blink-of-an-eye evolution of the Information Technology (IT) industry as a whole, it's no doubt that the workshops and conference sessions will be packed. Thousands of exhibitors also will be crowding into the Jacob Javits Center on New York's West Side to demonstrate their wares, distribute samples and demos, and talk to exhibition attendees.

The Fall Internet World 97 Conference and Exhibition runs from December 8-12, with such luminaries as Stephen Case, chairman and CEO of America Online; Alan Baratz, president of JavaSoft, Sun Microsystems; Michael Dell, founder and chairman of Dell Computer: Lawrence Ellison, chairman and CEO of Oracle; and John Sculley CEO of Live Picture making keynote speeches. The focus of the conference will be strategic business issues, specifically Internet implementation and developing technologies. Topics of workshops and conference sessions include international commerce, banking and finance, media and entertainment, publishing, sales-force automation, and public relations.

Monday, December 8's workshops include: Sun Microsystems Developer Day; Appliances, Thin Clients, and Hybrids Day; Internet Security Day; Webmaster HTML Fundamentals; and Internet Telephony. Highlights of Tuesday's offerings include: Electronic Commerce, Intranet Forum, and Web Infrastructure. Both days feature The Adweek Forum, which is a seminar about marketers who have built brands on the World Wide Web.

Wednesday's schedule covers e-commerce, intranets, push technology, firewalls, web system administration, and security. Conference sessions also on December 10 look at personalizing the Internet, on-line gaming, browsers, deregulation, JavaScript, different markets, and business strategies.

On tap for Thursday are workshops on web publishing, finance, Java, security, and server performance analysis. The conference sessions cover standalone Java applications, marketing, e-commerce in healthcare, content in the financial services, firewalls, advertising, demographics, content, CORBA, and distance education.

The last day of FIW '97 hosts workshops on ISP, Internet finance, knowledge management and search strategies, documentation, routing, scripting, and Java vs. ActiveX. Conference attendees can choose from Java applets, silicon alley, hacking, advertising, on-line communities, QuickTime authoring, gambling on-line, linking catalogs or SAP R/3 to web sites, web TV, dynamic HTML, and Internet video.

Interested readers may register for FIW '97 through the conference's web site: *http://www.internet.com*. Otherwise, you may call (800) 632-5337; fax (203) 226-6976; or write FIW '97, REG/Mecklermedia, 20 Ketchum St., Westport, CT 06880.

Internet users who have providers with less than satisfactory services may find use for a product such as Net.Medic. The browser companion from VitalSigns helps identify the source of a network bottleneck without contacting the provider. TechWorks, developers of performance enhancement products, will be bundling Net.Medic with various memory products.

The 800-kbyte application monitors computer performance by analyzing TCP/IP traffic. Elements examined by Net.Medic include client/server handshakes, incoming packet timing, and application-layer delays. When an issue has been identified, Net.Medic issues diagnostic packets to fix the problem.

TechWorks is offering Net.Medic 1.1 for $49.95, and is obtainable through their web site at: *http://www.techworks.com* or by calling (800) 688-7466.

For more information, contact TechWorks at 4030 W. Braker Lane, Austin, TX 78759-5319.

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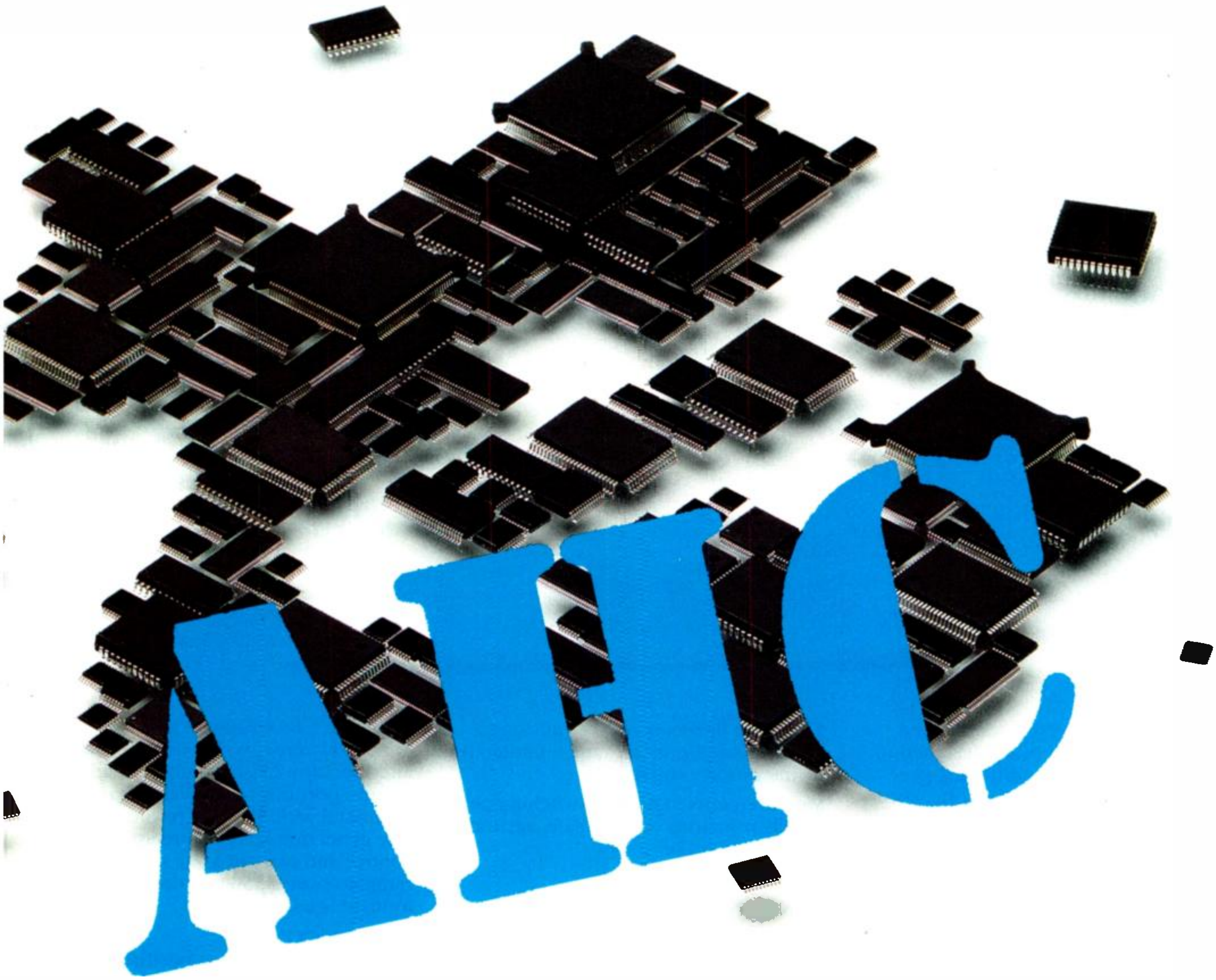

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14-1755

D U C T S

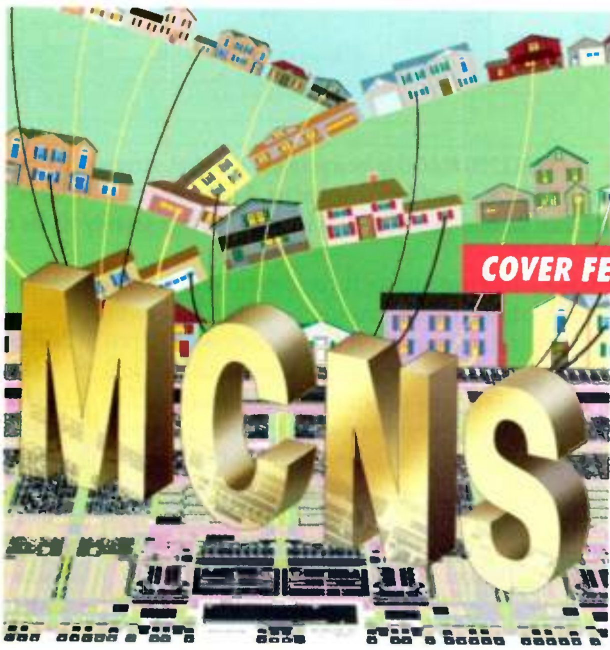
TEXAS INSTRUMENTS

MCNS/DOCSIS MAC Clears A Path For The Cable-Modem Invasion

The First Standards-Compliant Chip Means Affordable, Interoperable, Cable Modems, With Speed And Security Features.

Lee Goldberg

With the introduction of the BCM3220 multimedia cable networking systems/Data-Over-Cable-Service Interface Specification (MCNS/DOCSIS) compliant media-access controller (MAC) chip, the cable data revolution has begun in earnest. By rolling out the first integrated implementation of the cable industry's recently developed DOCSIS, Broadcom Corporation has paved the way for the rapid development of inexpensive consumer-oriented cable data appliances. This move could provide a critical jump-start for the emerging cable data industry. If the next year goes according to plan, we may see a device that delivers multimegabit downstream Internet access being sold at K-Marts and electronic discount stores at prices comparable to today's 56-kbit POTS modems.



COVER FEATURE

The Broadband Wars

The development of DOCSIS and the introduction of the BCM3220 mark the first hopeful chapter in the troubled history of cable media's efforts to maintain its dominant role in capturing the hearts, minds, and eyes of the American consumer. In the early nineties, the cable television industry faced a double threat: While saturated subscriber markets yielded flattening revenues, satellite television, sophisticated computer games, and Internet surfing began to erode cable's near-lock on passive leisure activities.

After several ill-fated adventures with video-on-demand, interactive shopping, and other attempts to dictate consumer taste, cable marketeers stumbled over the obvious hot application, broadband Internet access. Once early trials demonstrated the economic potential, it became clear that the only way to achieve a critical mass of users was to develop a transmission standard that would enable the production of mass-produced, inexpensive, interoperable cable modems and set-top boxes *(Fig. 1)*.

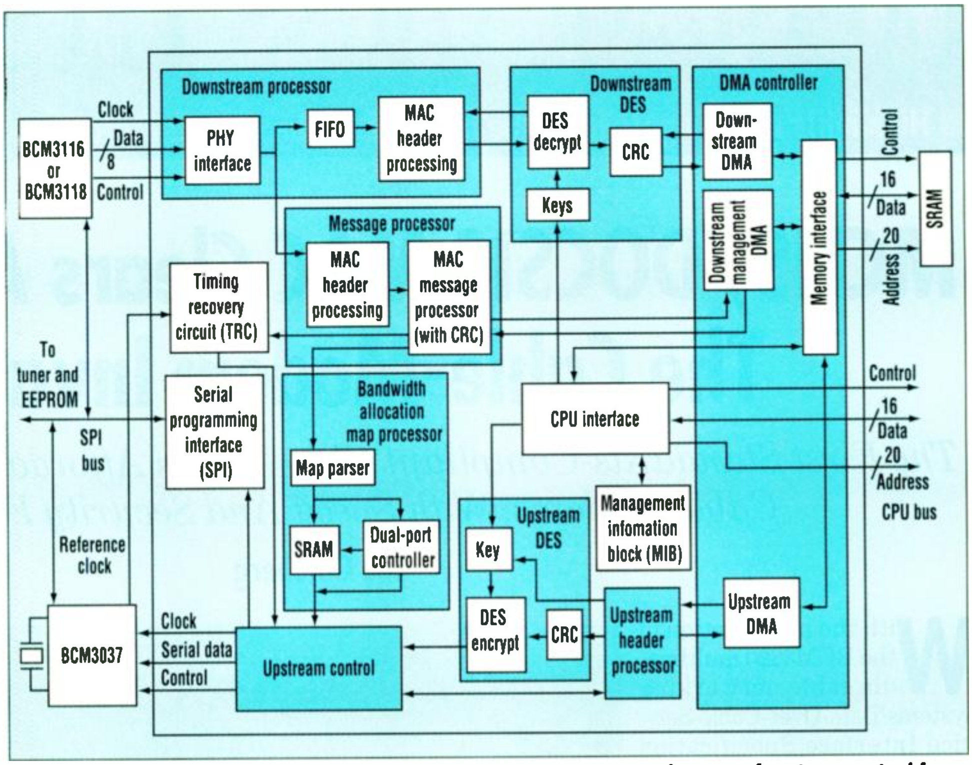
Frustrated by the slow progress of the IEEE's 802.14 cable data standards committee, a group of large cable interests formed the MCNS group. Comprised of heavyweights like Comcast and Time-Warner, MCNS teamed with the cable industry's research consortium, Cable Labs, Louisville, Colo., to produce their own open standard for moving data between cable network headends and subscriber's homes.

Enter DOCSIS

The first fruit of this alliance is the DOCSIS specification, developed by a group of manufacturers, under the direction of MCNS and Cable Labs. Participants in the initial development of DOCSIS included General Instruments, LAN City (now a part of Bay Networks), and Broadcom. This spec outlines the physical layer interfaces, MAC and transport protocols, security provisions, and other specifications necessary for designing interoperable cable data components. Subsequent fine-tuning was performed in an open forum hosted by Cable Labs and attended by most major players in the cable industry. The result is a standard that meets the needs of current users and anticipates the demands of future applications.

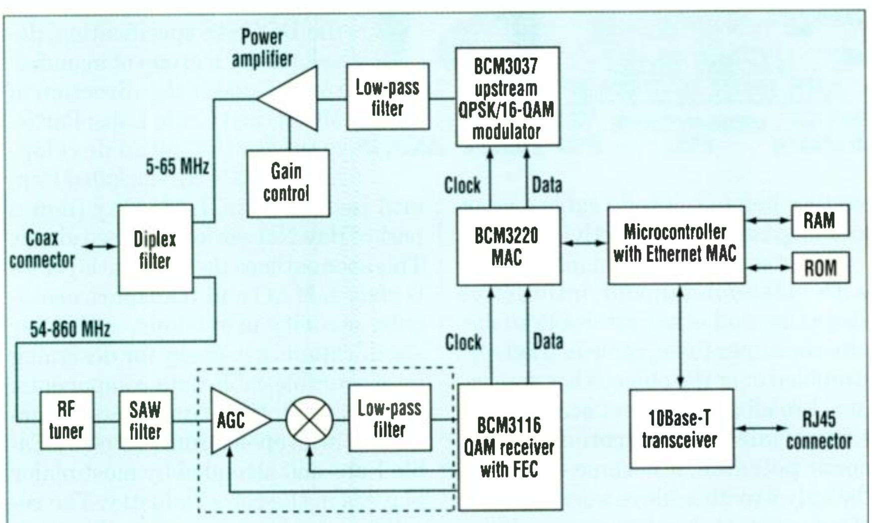
DOCSIS is designed to employ one or more unused video channels within the 54-to-860-MHz cable broadcast spectrum to transmit IP-based data across hybrid fiber coaxial networks. Complex phase/amplitude modulation enables each 6-MHz downstream channel to bring data into subscribers' homes at up to 38 Mbits/s. Depending on the bit rate selected by the operator, the shared downstream channel uses either 64- or 256-point quadrature-amplitude modulation (QAM). While little is known about what actual bandwidth requirements will be, initial results from field trials suggests that a single channel will provide groups of 200 to 1000 subscribers with Internet access that is substantially faster than today's best POTS-based services.

For communication from the home to headend, DOCSIS uses the 5-to-40-Hz sub-split band as a return path. Using QPSK today, or 16-QAM in subsequent versions, the upstream channel has a theoretical maximum throughput of 10 Mbits/s (*see "Broadband To The Home: Challenges On the Last Mile," Electronic Design, Oct. 2, 1995, pp 67-83).*



2. The BCM3220 MAC chip incorporates all control, stream-processing, and security functions required for a MCNS/DOCSIS-compliant cable modem. A memory-based DMA interface assures efficient data transfers to and from the host controller. Both baseline and high-security modes also are supported.

Since DOCSIS also is intended to support IP-based video, provisions have been made to support several levels of quality of service (QoS). This feature allows it to accommodate both traditional connectionless Internet traffic, as well as latency-sensitive multimedia streams. Selectable QoS also will let cable companies offer tiered services with various guaranteed bit rates and levels of latency to businesses which need them.



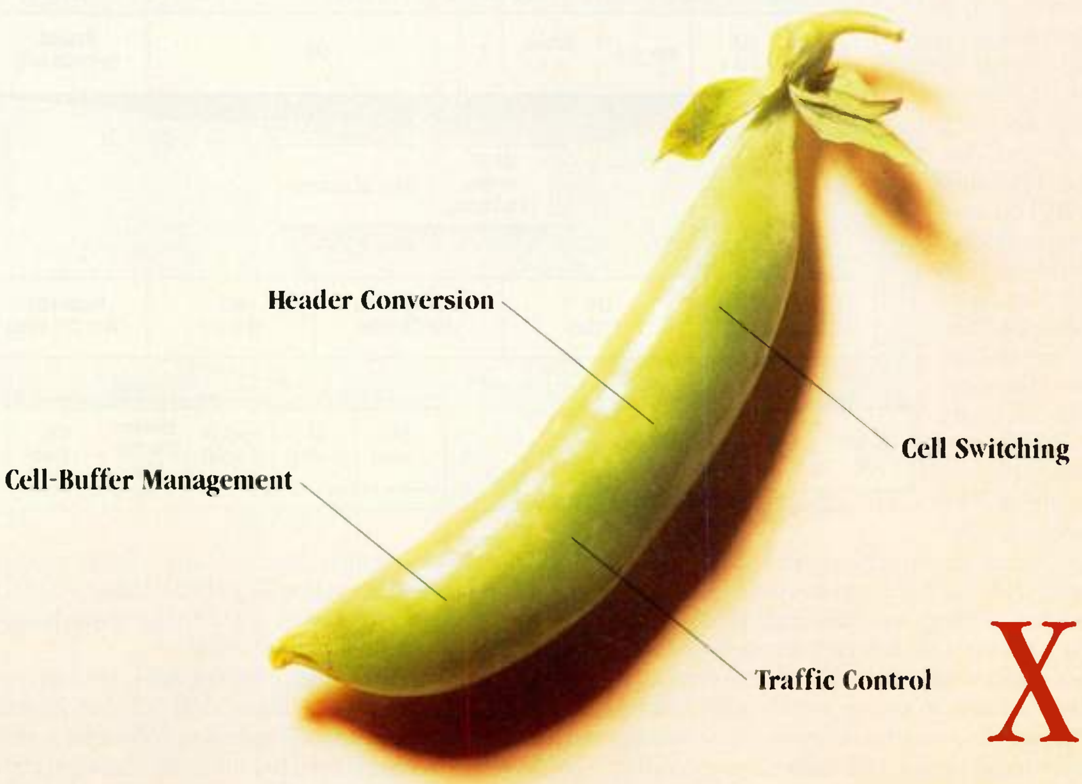
1. A DOCSIS-compliant cable modem receives its data over unused 6-MHz video channels within the normal cable spectrum. Upstream traffic is carried back to the system headend in the 5-to-45-MHz sub-split band. To ensure that the modem will operate properly and not interfere with other units, both the downstream receiver and upstream modulator/transmitter operate under the control of the BCM3220, or other DOCSIS-compatible MAC.

MPEG Everywhere

One interesting aspect of DOCSIS is that it uses MPEG II transport streams to move IP data. While not essential for today's applications, the standard's developers were looking toward the future. Today, MPEG encapsulation provides DOCSIS with a reliable, well-defined method of setting up multiple channels within a single data stream. In the near future, MPEG encapsulation will allow a single cable modem to support multiple sessions and multiple users, as well as delay-sensitive multimedia streams for voice or video over IP.

Using MPEG II transport streams also will allow DOCSIS to interoperate with the Open Cable standard for digital cable television that is currently under development. Open Cable also employs MPEG II transport streams for all of its media flows. This feature should greatly simplify traffic switching and processing within tomorrow's cable networks

Although it has some similarities to the carrier-sense multiple-access/collision-detect (CSMA/CD) protocol em-



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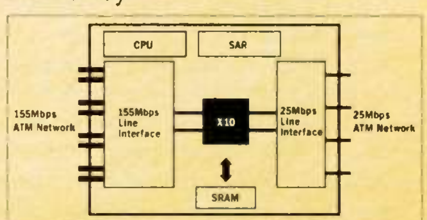

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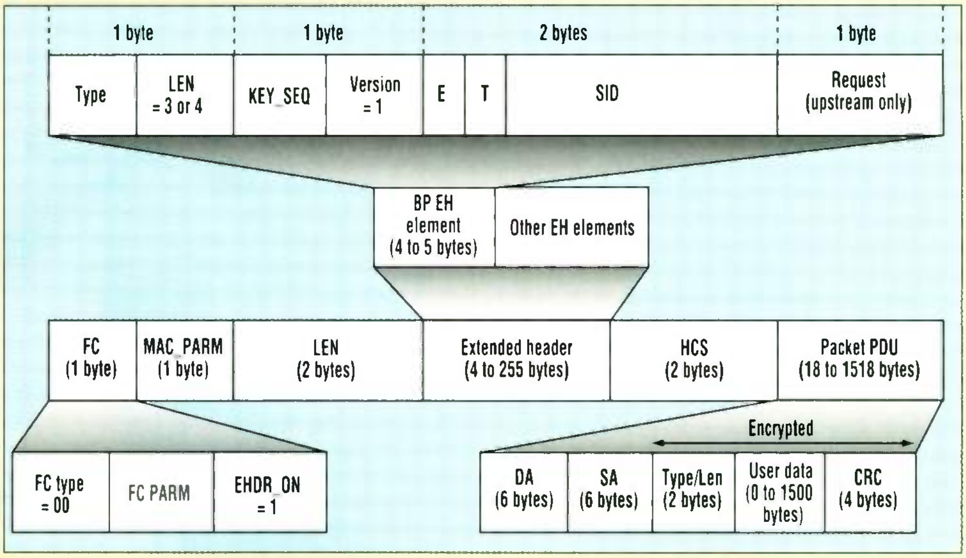
DOCSIS Security: Baseline Privacy



Security for the DOCSIS cable modem system is divided between an elaborate Full-Security Specification with removable, renewable security modules, and a low-cost, simpler scheme called Baseline Privacy (BPI). BPI is based on full-bodied concepts, beginning with the 56-bit Digital Encryption Standard (DES) Cipher Block Chaining algorithm, yet unburdened by some of the more costly and complex security features of its heavy twin. All DOCSIS cable modems are required to support BPI, ensuring that basic data privacy is maintained in the shared cable environment.

Privacy is more than sufficient for Internet access applications because it makes a number of assumptions on the application it serves, namely that Internet access is two way, and therefore not susceptible to passive theft of service; that it's not particularly valuable to anyone, but the user; that really important transactions over the Internet (like banking) will be secured with end to end application layer security; and that by changing keys often, individual keys are not worth the trouble of stealing. It also is much easier to detect clones and unauthorized users of cable modems because the service is two-way. The modem system is unlike broadcast pay-per-view video that can be hacked in private—clone modems must not only listen, but speak to be useful.

DES is a cryptographic algorithm that takes binary coded data and applies a known algorithm using a randomly generated 56-bit key to produce unintelligible or encrypted bits. The algorithm can be known by many but the data will be unintelligible unless the key is shared by both parties. This mutually shared secret allows encrypted traffic to remain private to those who have the keys. A 56-bit key has 70 quadrillion possible values, and the only guaranteed way of discovering a truly random key is to try all of them. Changing keys often reduces the likelihood of success even further. The challenge in this type of cryptography is how to exchange the secret keys easily, yet securely.

Cipher Block Chaining is a form of DES that increases the strength of the encryption by using an initialization vector sent down with the key to preset its encryption hardware state. For each eight-byte block encrypted, instead of resetting or reinitializing, the circuit retains the result from the previous block's encryption. This chaining of results from one block to the start of the next makes the cryptography stronger since a hacker would need to reconstruct the entire sequence to break the code instead of just one block.

Baseline Privacy uses a Service ID (SID) associated with traffic originating from or destined to a particular modem to identify a Traffic Encryption Key (TEK) to use. Each TEK is a pair of even and odd 56-bit keys. Each key also has a corresponding 56-bit initialization vector.

All DOCSIS frames have header fields that are never encrypted and include an optional field called an Extended Header. Mainly for protocol expansion, this variable area in the DOCSIS header is used to contain the Baseline Privacy Extended Header *(see the figure)*. The SID is contained in the BPI Extended Header for each frame to identify which TEK to use.

Each DOCSIS frame that will be encrypted must contain a Privacy Extended Header. The header contains a type and version field as well as the SID identifying a particular encrypted data flow. The SID field also contains an enable/disable bit that controls encryption for that particular frame and a toggle bit. The toggle bit is used to signify the current epoch; that is whether the even or odd key is in use for this frame. This toggle bit allows the protocol to set up a new TEK in the even key slot while actively using the odd key. When the first frame to use the new key is received, the toggle bit indicates that the epoch has changed and that the other key is now in use. The toggle bit also is the least-significant bit of the 4-bit sequence field that is used to track the history of up to 16 keys by the key exchange protocol.

Baseline Privacy encrypts data in both up and downstream directions of the cable plant using the extended headers to indicate what to do. DOCSIS MAC messages allow a simple key exchange protocol to operate between the headend (or cable modem termination system) and the cable modems. Keys are updated frequently and the registration databases are watched vigilantly for clones. This provides subscribers with a low-cost but vey effective "lite" security solution for ensuring data privacy.

Contributed by Thomas J. Quigley, director of the Residential Broadband Business Unit at Broadcom Corp.

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ployed by most other 802-flavored media, DOCSIS employs a time-slotted noncontention access scheme for most of its communication. In order to maintain order on a busy cable, the MAC chip in each subscriber's modem must keep track of network timing, as well as its place in the overall communications flow. In contrast to Ethernet's CSMA/CD protocol, this more orderly access scheme allows cable operators to fill their pipelines at up to 75% of their theoretical capacity. This factor is critical when subscribers are sharing bandwidth with 200+ neighbors.

To satisfy even the terminally paranoid, two layers of security are provided within DOCSIS, plus the potential for a completely shielded "tunneling" protocol for sensitive data transfers such as personal records or credit card numbers.

If DOCSIS seems a bit complicated, it's because it really is. The standard's rich feature set and traffic control scheme require approximately 100,000 gates (plus RAM) to implement, yielding an effective processing power of 30 to 40 MIPS. In practice, you'd probably need a much faster CPU to make sure it was available for all the demanding real-time operations. Despite the complexity, Broadcom was able to follow the evolution of the standard and deliver a product within nine months of its finalization, thanks to its close participation in the development committee.

Another factor that gave Broadcom an inside edge on delivering the MAC chip is its proprietary silicon compiler technology. Their specially developed software can translate algorithms directly to gate layouts optimized for minimal cross-talk, propagation delay, and other critical parameters. While it is primarily used to implement blindingly fast digital filtering and correlating algorithms in CMOS logic arrays, the same software also has been employed to lay out Fast Ethernet MACs and other control logic requiring complex signal paths and tight timing.

A Peek Inside

Examining the block diagram of the BCM3220 reveals the basic functions required to support full-duplex communication using the MCNS protocol *(Fig. 2)*. Many complex functions have been implemented plus encrypt/decrypt logic and a DMA-based, shared-RAM host interface that has been optimized for Motorola's QUICC series of 680xx and PowerPC-based controllers. To insure fast, efficient transfers, incoming and outgoing Ethernet packets are exchanged whole-cloth in a single operation, with no buffer copying or other overhead-intensive intermediate steps.

The downstream section of the BCM3220 interfaces directly with the BCM3116 QAM receiver. Since DOCSIS requires that data be encapsulated within MPEG II transport streams, the MAC is responsible for extracting it before passing IP frames to the host system. Broadcom's designers went the spec one better and included an MPEG II filter port in their device. This feature allows the BCM3220 to be programmed to pass through selected MPEG video streams to an external decode circuit— a handy feature when designing a combination cable modem/set-top box.

To Satisfy Even The Terminally Paranoid, Two Layers Of Security Are Provided Within DOCSIS, Plus A Fully Shielded "Tunneling" Protocol.

In addition to recovering and processing data, the downstream processor must perform decryption functions and receive synchronization and control messages from the headend. These messages enable the headend to tell the modem to adjust its data rates and other parameters to match changing line conditions.

To avoid conflicts in a shared-media environment, the MAC uses several tools to keep the modem synchronized with its neighbors and headend. First, the time-base recovery (TRC) function detects and interprets broadcast timing information. Since MCNS modems can be programmed for a variety of data rates and transmission parameters, upstream channel description (UCD) messages are used to tell the subscriber equipment what the headend is expecting to see.

SPI On Board

Part of the BCM3220's job is to interpret these messages and set the transmitter's modulation, timing, and FEC parameters accordingly. With this in mind, the MAC chip sports an industry-standard serial programming interface (SPI) bus master interface which can be used to configure and control both the QAM receiver and Burst modulator chips on the fly. If SPI-capable components are used elsewhere in the modem's design, the BCM3220 also can be programmed to set their operating values, such as tuner frequencies and amplifier gains.

The chip's upstream processing section is responsible for passing data to the headend. Interfacing directly to the BCM3037 QAM/QPSK modulator, it transmits MPEG-encapsulated data within a series of time slots that it shares with the other modems in the network. To accomplish this task smoothly, it places requests to the headend during specially designated time periods.

The BCM3220 MAC keeps these time periods straight by referring to the upstream bandwidth availability map that the headend routinely broadcasts. Stored in on-chip registers, this map tells the modem when it can request an upstream time slot, transmit its data, or perform network maintenance and management functions. For extended data transfers involving more than one block of data, the BCM3220 automatically requests a series of prescheduled piggyback time slots. This technique allows it to use a single transfer request to move multiblock files, increasing throughput and reducing access latency.

Pretty Darn Good Privacy

Of course, whenever you're using a broadcast media to transmit sensitive data, the issue of security always comes up. According to Tom Quigley, product manager at Broadcom, DOCSIS provides two grades of security at the hardware level. Both employ the date encryption standard (DES) algorithm and Rivest, Shamir, and Adelman (RSA) key exchange. The real difference between the baseline and

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full security is the use of a highly secure, removable hardware key for sensitive applications. In addition, full security uses the full authentication protocol and a 1024-bit key to encrypt the exchange of traffic keys.

The BCM3220 supports both levels of security. It performs the DES electronic-code-book (ECB) and cipher-block-chaining (CBC) functions in hardware, along with residual block termination (RBT). Normally, a 56-bit key is employed, although it can be programmed to run with a crippled 40-bit key for export applications. If desired, the MAC chip also lets designers include application-based security measures for a third layer of end-to-end protection *(see "DOCSIS Security: Baseline Privacy," p. 74)*.

The advent of the DOCSIS standard may prove to be a crucial turning point in the broadband wars between telephone and cable networks. While a shared-media system like cable will always be a less than optimal way to deliver data to homes, MCNS has done a very good job in making cable media as efficient, reliable, and secure as possible. For more information, contact the MCNS group at: *Cable Labs, 400 Centennial Parkway, Louisville, CO 80027; phone (303) 661-9100; fax (303) 661-9199.*

Rambo's Uzi

Broadcom's first silicon implementation of the DOCSIS standard will surely give rise to a first generation of low-cost, interoperable cable modems. Telco and xDSL advocates should not take this news lightly. Given the aggressive nature of the cable industry, providing them with a standards-compliant MAC chip like the BCM3220 will be like handing Rambo a loaded Uzi.

PRICE AND AVAILABILITY

Available in sample quantities now, the BCM3220 will be in full production during the first quarter of 1998. Pricing for the part is $30 each, in quantities of 10,000.

Broadcom Corp., 16251 Laguna Canyon Rd., Irvine, CA 92618; (714) 450-8700; fax (714) 450-8710; Internet: www.broadcom.com.

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DESIGN NOTES

LINEAR TECHNOLOGY

LTC1560-1: Tiny 1MHz Lowpass Filter Uses No Inductors

Design Note 169

Nello Sevastopoulos

The LTC®1560-1 is a fully integrated continuous-time filter in an SO-8 package. It provides a 5-pole elliptic response with a pin selectable cutoff frequency (f_C) of 1MHz or 500kHz. Several features distinguish the LTC1560-1 from other commercially available high frequency, continuous-time monolithic filters:

- 5-pole 0.5MHz/1MHz elliptic in an SO-8 package
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- 60dB or more stopband attenuation
- No external components required other than supply and ground decoupling capacitors

The LTC1560-1 delivers accurate fixed cutoff frequencies of 500kHz and 1MHz without the need for internal or external clocks. Other cutoff frequencies can be obtained upon demand; please consult LTC marketing. The extremely small size of the part makes it suitable for compact designs that were never before possible using discrete RC active or RLC passive filter designs.

Frequency and Time-Domain Response

Figure 1 shows a simple circuit for evaluating the performance of the filter. The LTC1560-1 offers a pin-selectable cutoff frequency of either 500kHz or 1MHz. The filter gain response is shown in Figure 2. In the 1MHz mode, the passband gain is flat up to $(0.55)(f_C)$ with a typical ripple of ±0.2dB, increasing to ±0.3dB for input frequencies up to $(0.9)(f_C)$. The stopband attenuation is 63dB starting from $(2.43)(f_C)$ and remains at least 60dB for input frequencies up to 10MHz.

The elliptic transfer function of the LTC1560-1 was chosen as a compromise between selectivity and transient response. Figure 3a shows the 2-level eye diagram of the filter. The size of the "eye" opening shows that the filter is suitable for data communications applications. Additional phase equalization can be performed with the help of an external dual op amp and a few passive components. This is shown in Figure 4, where a 2nd order allpass equalizer is cascaded with the IC. The allpass function is achieved through traditional techniques, namely, passing a signal through a low Q inverting bandpass filter and then performing summation with the appropriate gain factors. Figure 3b shows the eye diagram of the equalized filter.

DC Accuracy

For applications where very low DC offset and DC accuracy are required, the DC offset of the filter can be easily corrected, as shown in Figure 5.

The input amplifier stores the DC offset of the IC across its feedback capacitor. The total output DC offset is the input DC offset of the 1/2 LT1364 plus its offset current times the

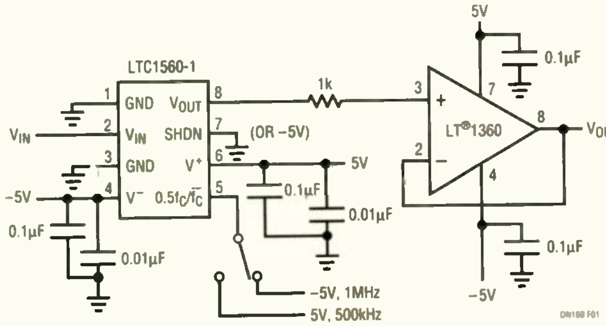

Figure 1. A Typical Circuit for Evaluating the Full Performance of the LT1560-1

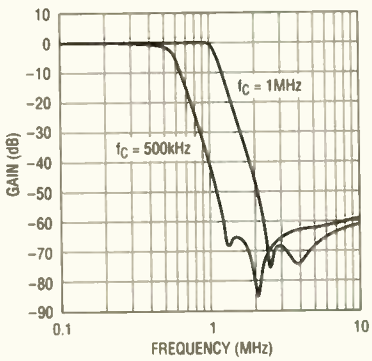

Figure 2. Gain vs Frequency of the 1MHz and 500kHz

10k resistor (less than 1.85mV). Upon power-up, the initial settling time of the circuit is dominated by the RC time constant of the DC correcting feedback path; once the DC offset of the LTC1560-1 is stored, the transient behavior of the circuit is dictated by the elliptic filter.

Conclusion

The LTC1560-1 is a 5th order, user friendly, elliptic lowpass filter suitable for any compact design. It is a monolithic replacement for larger, more expensive and less accurate solutions in communications and data acquisition.

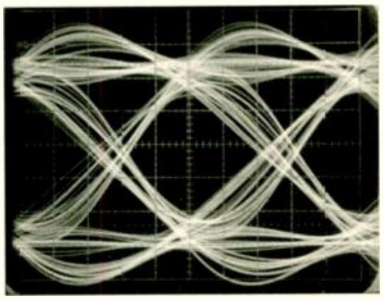

Figure 3a. 2-Level Eye Diagram of the LTC1560-1 Before Equalization

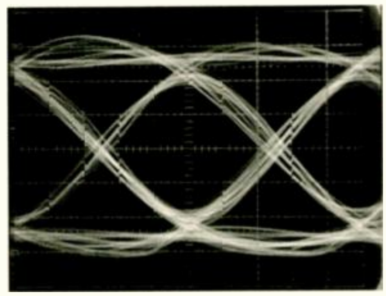

Figure 3b. 2-Level Eye Diagram of the Equalized Filter

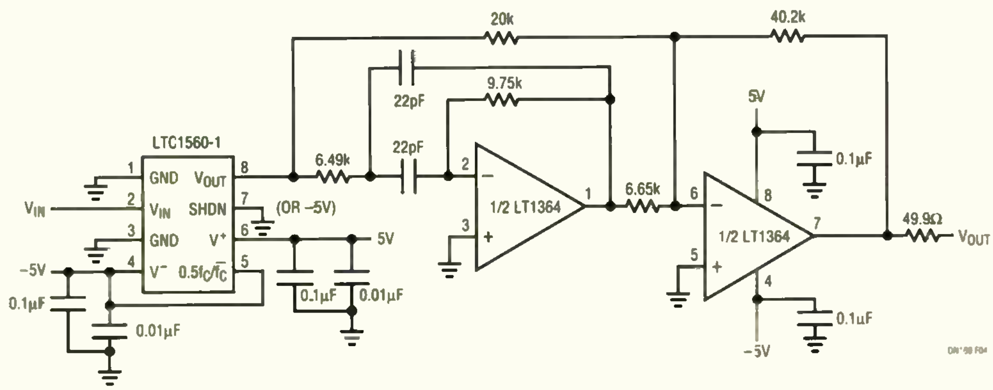

Figure 4. Augmenting the LTC1560-1 for Improved Delay Flatness

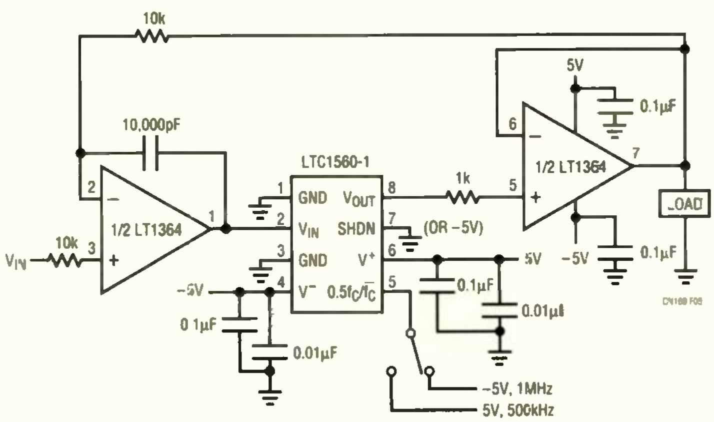

Figure 5. A DC Accurate 500kHz/1Mhz Elliptic Filter with an Output Buffer for Driving Cables or Capacitive Loads

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Line-Driver Design For Broadband Communications Applications*

Following Is A Fractical Guide To Designing Low-Power, Low-Distortion Circuits For XDSL And Cable Modem Systems.

EAMON NASH, Analog Devices Inc., 804 Woburn St. Wilmington, MA 01887; (617) 937-1239, e-mail: Eamon.nash@analog.com.
** This is a corrected version of the article which originally appeared in our September 2, 1997 issue. - ED*

Even though highly integrated chip sets for wired communications standards such as High Bit-rate Digital Subscriber Line (HDSL), Asymmetrical Digital Subscriber Line (ADSL), and Hybrid Fiber Coax (HFC) are being implemented using LSI CMOS technology, the line-driving function generally requires high-quality bipolar amplifiers.

Requirements vary, but in general, the line driver must be able to deliver high output current with low signal distortion. Bipolar technology is generally favored by IC designers when designing such amplifiers. However, because today's modems are predominantly digital, there is an increasing need for analog line-driving amplifiers to operate from low supply voltages, and sometimes from single supplies.

Within these constraints, the line-driver designer has a number of architectural degrees of freedom that make the design task a little easier. If a high signal swing (as compared to the supply voltage) is required, differential line driving can be used to double the available peak-to-peak voltage of the signal in question.

If transformer coupling is necessary, a step-up or step-down transformer can be used to optimize signal size. It should be noted however, this does change the current demand on the amplifier.

In power-critical applications, component selection is not a trivial matter of finding devices with low quiescent current. In considering the "total" power consumption of the driver, one has to look at the quiescent power consumption, the power delivered to the load, and the dynamic power, i.e. the power that the amplifier must consume to deliver the requisite power.

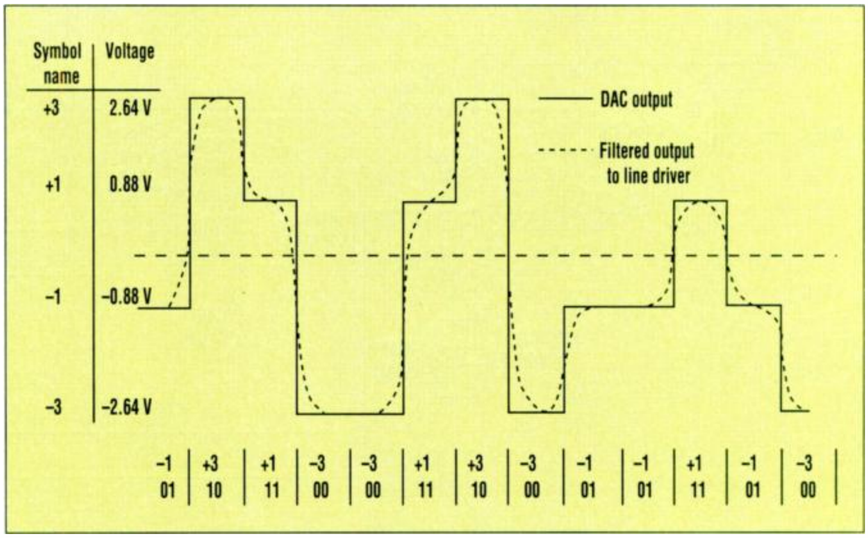
Driving HDSL Lines

HDSL is becoming popular as a way to provide full-duplex data communication at rates up to 1.544 Mbits/s (2.048 Mbits/s in Europe) over moderate distances via conventional telephone twisted-pair wires. Traditional T1 (E1 in Europe) requires repeaters every 3000 to 6000 ft. to boost the signal strength and allow transmission over distances up to 12,000 feet.

To achieve repeater-less transmission over this distance, a HDSL modem requires transmitted power level of +13.5 dBm (assuming a line impedance of 135 Ω). HDSL uses the Two Binary One Quaternary line code (2B1Q). A sample 2B1Q waveform is depicted in Figure 1. The digital bit stream is broken up into two-bit groups. Four analog voltages (called quaternary symbols) are used to represent the four possible combinations of two bits. These symbols are assigned the names +3, +1, –1, and –3.

The corresponding line voltages are produced by a digital-to-analog converter (DAC) that is usually part of an Analog Front End Circuit (AFEC). Before it's applied to the line, the DAC output is low-pass filtered and acquires the sinusoidal form shown in the dotted line of Figure 1. The filtered signal is then applied to the line driver. The line voltages that correspond to the quaternary symbols +3, +1, –1, and –3 are 2.64 V, 0.88 V, –0.88 V, and –2.64 V. This results in a peak-to-peak line voltage of 5.28 V.

Many of the elements of a classic differential line driver are shown in the HDSL line driver *(Fig. 2)*. A 6-V peak-to-peak differential signal is applied to the input. The differential gain of the amplifier ($1+2R_F/R_G$) is set to



1. Data transmitted on HDSL lines are coded with 2B1Q (2 bits I Quaternary) which consists of 4 discrete voltage levels. Each level or symbol corresponds to a 2-bit sequence. The discrete voltage levels are produced by a DAC, filtered and applied to a line driver. The line driver must deliver a peak-to-peak voltage amplitude of 5.28 V to the line. This corresponds to a power level of +13.5 dBm (R_L = 135 Ω).

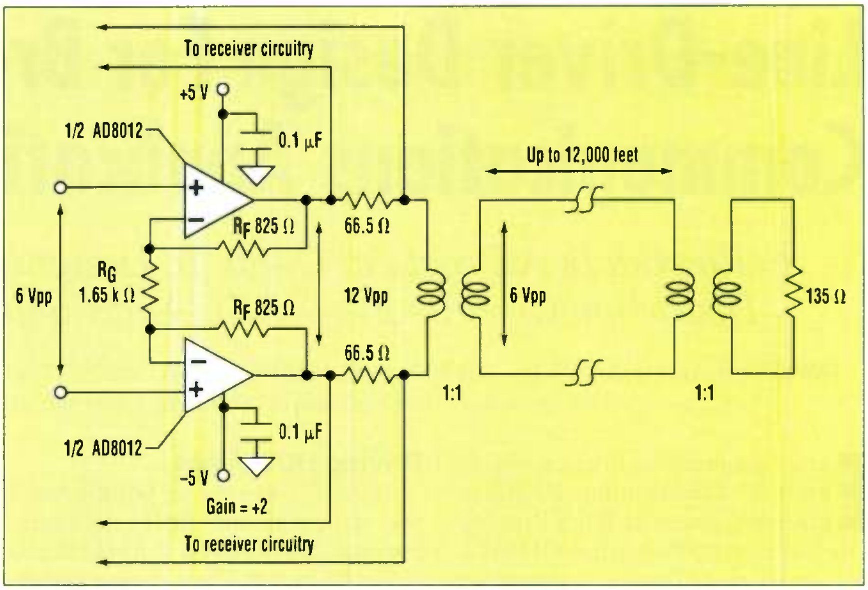
+2, so that the resulting differential output signal is 12 Vp-p.

As is normal in telephony applications, a transformer galvanically isolates the differential amplifier from the line. In this case, a 1:1 turns ratio is used. To correctly terminate the line, it is necessary to set the output impedance of the amplifier to be equal to the impedance of the line being driven (135 Ω in this case). Because the transformer has a turns ratio of 1:1, the impedance reflected from the line is equal to the line impedance of 135 Ω ($R_{REFL} = R_{LINE}$/Turns Ratio). As a result, two 66.5-Ω resistors correctly terminate the line.

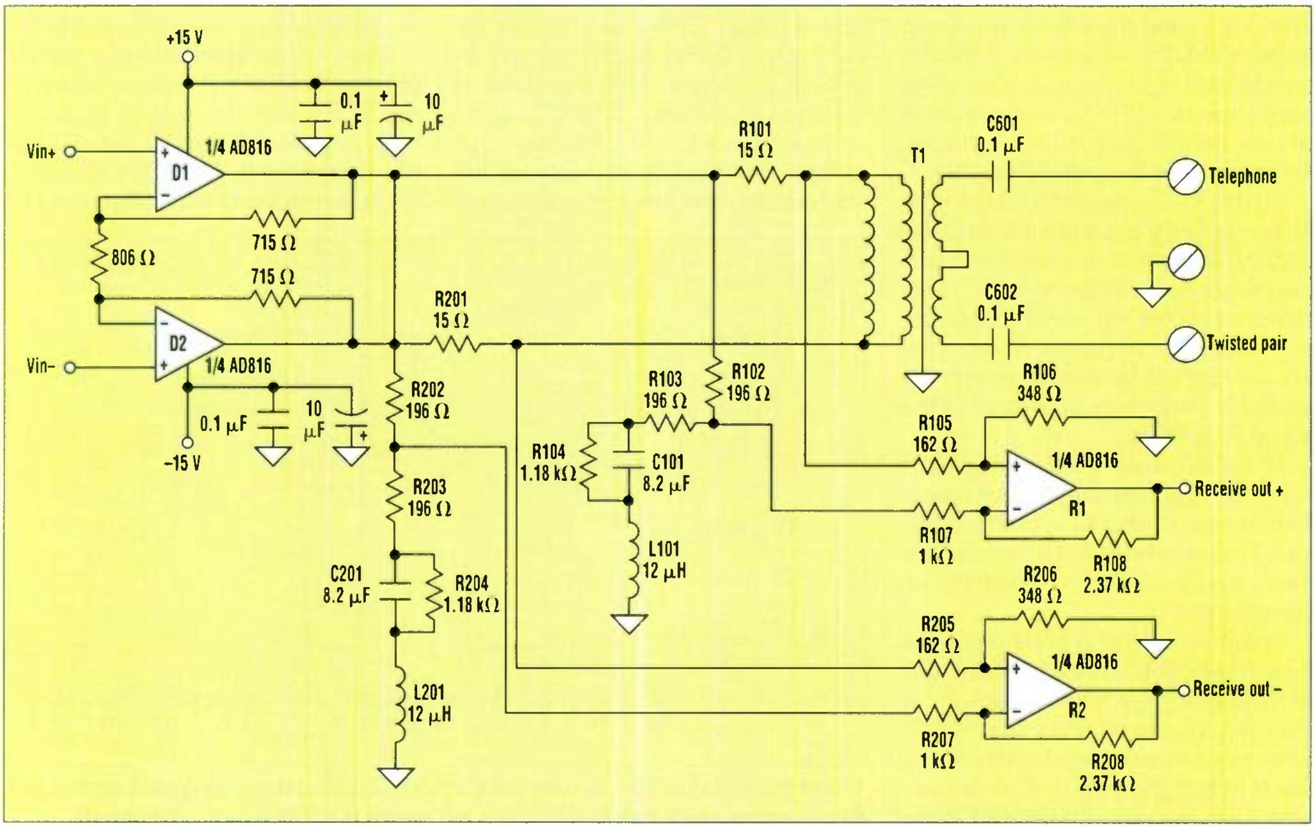
The immediate effect of back-termination is that the signal from the amplifier is halved before it is applied to the line. This doubles the power that the amplifier must deliver. The back-termination resistors do however play another important role.

Full-duplex data-transmission systems like HDSL simultaneously transmit data in both directions. As a result, the signal on the line and across the back-termination resistors is the composite of the transmitted and received signal. The termination resistors are used to tap off this signal and feed it to the receive circuitry. Because the receive circuitry "knows" what is being transmitted, the transmitted data can be subtracted from the digitized composite signal to reveal the received data.

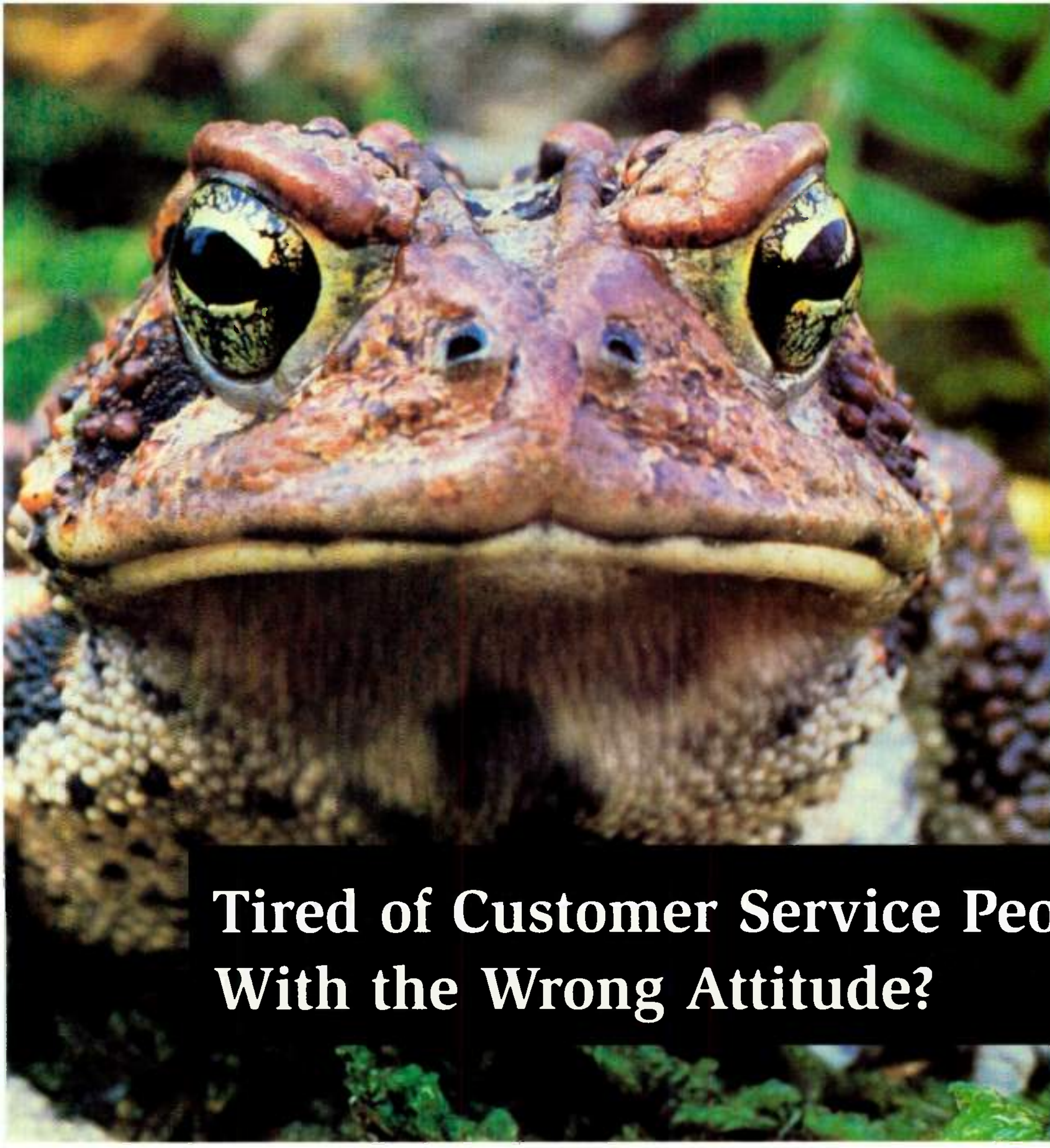
Driving a line with a differential signal offers a number of advantages over a single-ended drive. Because the two outputs are always 180° out of phase relative to one another, the dif-



2. A "classic" differential driver has an amplifier gain of ($2R_F/R_G + 1$). Because the line must be back terminated, the amplifier must generate twice the voltage that it ultimately transmits.



3. A complete ADSL transceiver can be built using a quad op amp. Two high-power devices provide a differential line drive of +20 dBm. Two low-noise op amps tap off the composite signal (sum of transmitted and received signal) on the back-termination resistors. Using frequency dependent impedance matching, the transmitted signal is eliminated from the receive amplifier, revealing the differential received signal.



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ferential signal output is double the output amplitude of either of the op amps. As a result, the amplifier can have a peak-to-peak swing of nearly 16 V (each op amp can provide a signal swing up to about ±3.9 V), even though the power supply is only ±5 V.

In addition to this, even-order harmonics (2nd, 4th, 6th, etc.) of the two single-ended outputs tend to cancel one another out. So, the total harmonic distortion (THD) decreases compared to the single-ended case, even as the signal amplitude is doubled. This is particularly advantageous for the case of the second harmonic. Being very close to the fundamental, post-filtering is quite difficult.

Differential line driving technniques also help to preserve the integrity of the transmitted signal in the presence of ElectroMagnetic Interference (EMI). EMI tends to induce itself equally on to both the positive and negative signal line. As a result, a receiver with a good common-mode rejection ratio (CMMR), will be able to amplify the original signal while rejecting induced (common-mode) EMI.

Choosing A Transformer

Increasing the peak-to-peak output signal from the amplifier in the previous example, combined with a variation in the turns ratio of the transformer, can yield further enhancements to the circuit. The output signal swing of the AD8012 can be increased to about ± 3.9 V before clipping occurs. This increases the peak-to-peak differential output of the amplifier to about 15.6 V. Because the signal applied to the primary winding is now bigger, the transformer turns ratio of 1:1 can be replaced with a turns ratio of about 1.3:1 (from amplifier to line). This steps the 7.8-V peak-to-peak primary voltage down to 6 V. This is the same secondary voltage as before, thus making the resulting power delivered to the line the same.

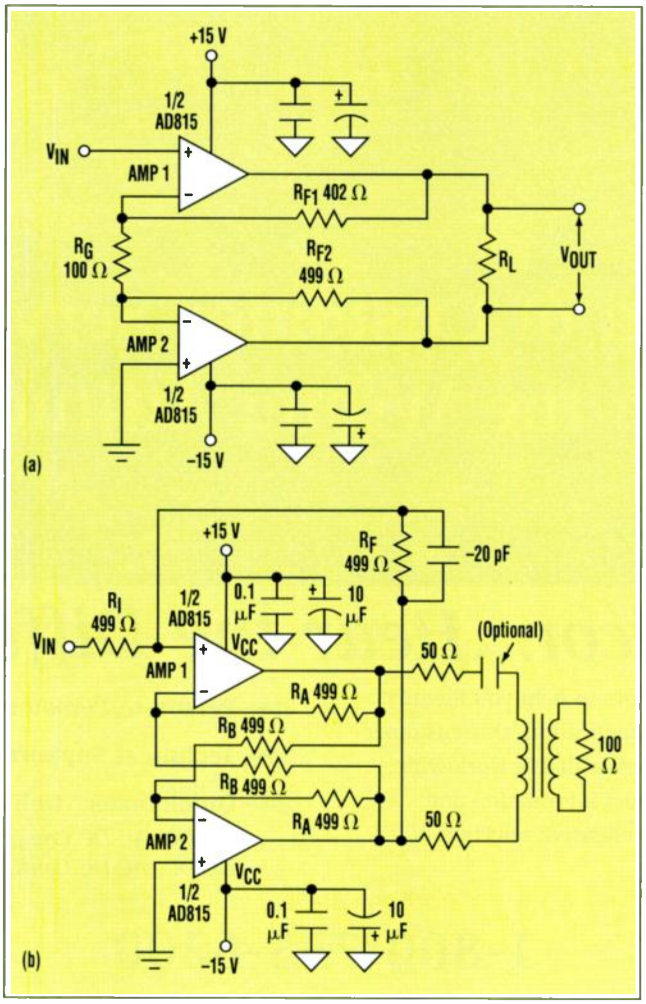
The received signal, which is small relative to the transmit signal, will however be stepped *up* by a factor of 1.3. Amplifying the received signal in this manner enhances its signal-to-noise ratio and is useful when the received signal is small compared to the transmitted signal.

The impedance reflected from the 135-Ω line now becomes 228 Ω ($1.3^2 \times$ 135 Ω). With a correctly-terminated line, the amplifier must now drive a total load of 456 Ω (114 Ω + 114 Ω + 228 Ω), considerably less than the original 270-Ω load. This reduces the drive current of the amplifier by about 40%.

Even more significant is the reduction in dynamic power consumption; that is, the power the amplifier must expend to deliver the power to the load. Increasing the output signal so that it is as close as possible to the power rails minimizes the dynamic power consumed in the amplifier.

But there is however, a price to pay in terms of increased signal distortion. Increasing the output signal of each op amp from the original ±3 V to ±3.9 V reduces the spurious-free dynamic range (SFDR) from –65 dB to –50 dB (measured at 500 kHz).

The theoretical limit to this signal maximization would be the case where an ideal rail-to-rail amplifier was used to transmit a square wave. Because the square wave would be swinging all the way to the limit of each rail, there would be no dynamic power consumption in the amplifier. This would reduce the power consumed within the amplifier to the simple product of quiescent current and the difference between the two power supply voltages.



4. Single-ended to differential conversion can be accomplished in a number of ways. A simple "three-resistor" amplifier works well at various gains (a). However changing the gain involves changing at least two of the resistors. In addition, the noise gains of the two op amps always differ by one. At the cost of some extra passive components, an alternative circuit can eliminate both of these problems (b).

A Differential Transceiver

ADSL is a means for exchanging data between a telephone central office (CO) and the home via conventional telephone twisted-pair (POTS). Originally envisioned as a technology to deliver video-on-demand over phone lines, ADSL's asymmetrical data rates (up to 6.144 Mbits/s downstream, and 640 kbits/s upstream) lend themselves very well to Internet surfing applications.

Most ADSL applications use either Carrierless Amplitude and Phase (CAP) or Discrete Multi-Tone (DMT) as modulation schemes. To transmit data over distances up to 18,000 ft., both standards call for a line power of +20 dBm to +26 dBm. This is based upon a line impedance of either 100 or 135 Ω.

A complete transceiver circuit for ADSL is shown using a quad op amp (AD816) that was designed primarily for providing an integrated solution for the transmit and receive functions of an ADSL modem *(Fig. 3)*. The transmitted signal is applied to the V_{in}+ and V_{in}– terminals of the differential amplifier formed by high-output power op amps D1 and D2.

Demystifying dBm: A Primer On Power

Signal levels in wired communications applications are usually specified either in dBm or dBmV. The drive capability of operational amplifiers on the other hand is usually specified in terms of peak output voltage and current. Because of differences in terminology, choosing a suitable line driving op amp can be difficult and confusing.

In order to understand how the two specs are related, it's a good idea to start with a few definitions.

Line Impedance: This is the size of the termination resistor on the line that is being driven.

Crest Factor: The peak to average (or rms) ratio of a signal. While a sine wave has the familiar crest factor of $\sqrt{2}$, the crest factor of modulated signals varies depending upon the modulation scheme. Crest factors typically range from 1.3 to 5.5.

Driver Load Impedance: The impedance that the amplifier has to drive. This impedance is the sum of the impedance that is reflected from the line and the amplifier's back termination resistors

The dBm unit is defined as the power level in dB relative to 1 mW, i.e.

Power(dBm) = $10\log_{10}$(Power/ 1 mW)

Since power in watts is defined as the rms voltage squared, divided by the line impedance, we can also write this as:

Power(dBm)= $10\log_{10}((\mathrm{Vrms}^2/R)/1\ \mathrm{mW})$

It follows that 0 dBm is equal to 1 mW, +10 dBm is equal to 10 mW, +30 dBm is equal to 1 W, etc... Because impedance is an integral component of this equation, it is always necessary to specify a line impedance value when talking about dBm levels.

The dBmV unit is defined as the voltage level, in dB, relative to 1 mV, i.e.

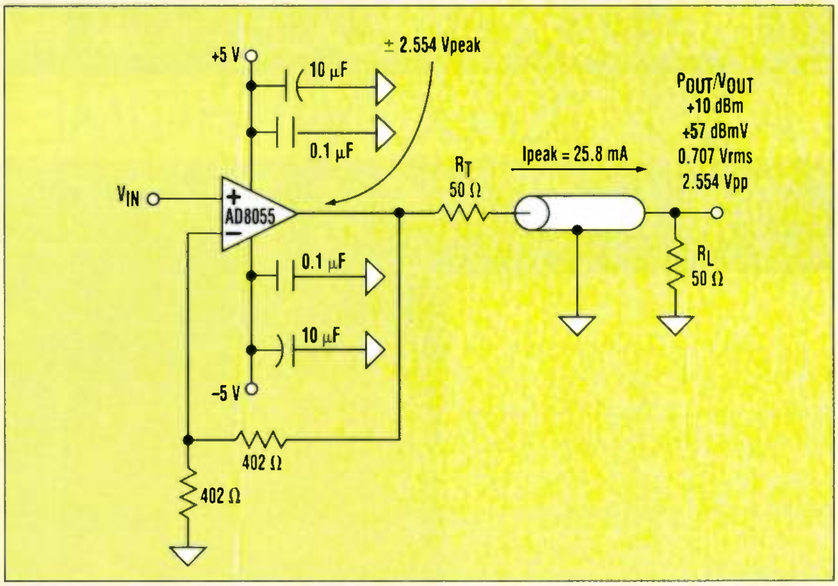
Voltage(dBmV)= $20\log_{10}$(Vrms/1 mV)

Therefore, 0 dBmV is equal to 1 mW, +60 dBmV is equal to 1 V, etc.

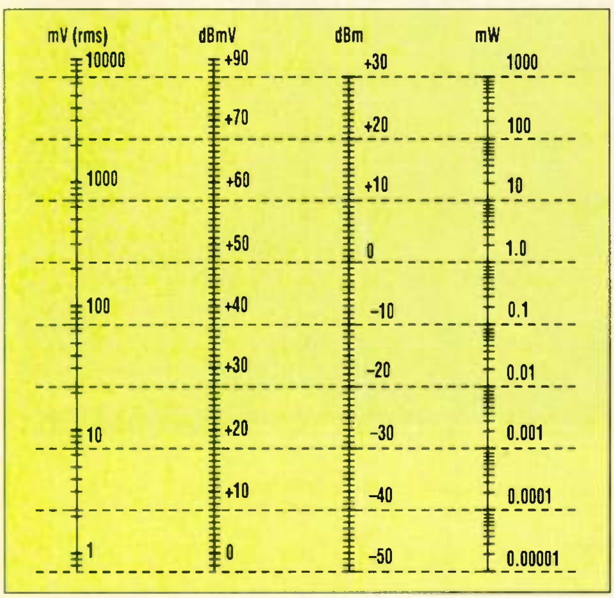
Figure b shows how mV, dBmV, dBm and mW relate to each other. This is, however, only valid for a load impedance of 50 Ω. If the load impedance were 75 Ω for example, the mV and dBmV scales will be shifted downward relative to the dBm and mW scales.

Consider this example. The operational amplifier in Figure a is required to deliver a power level of +10 dBm to a line which has a 50-Ω load impedance and is back-terminated. The signal being transmitted is determined to have a crest factor of 1.8.

A power level of +10 dBm corresponds to an rms voltage of 0.707 V (+57 dBmV). From the crest factor, the peak voltage is calculated at 1.27 V. Because half of the voltage is lost in the 50-Ω back-termination resistor, the op amp must be able to deliver a peak output voltage of 2.54 V. This corresponds to a peak output current of 25.4 mA.

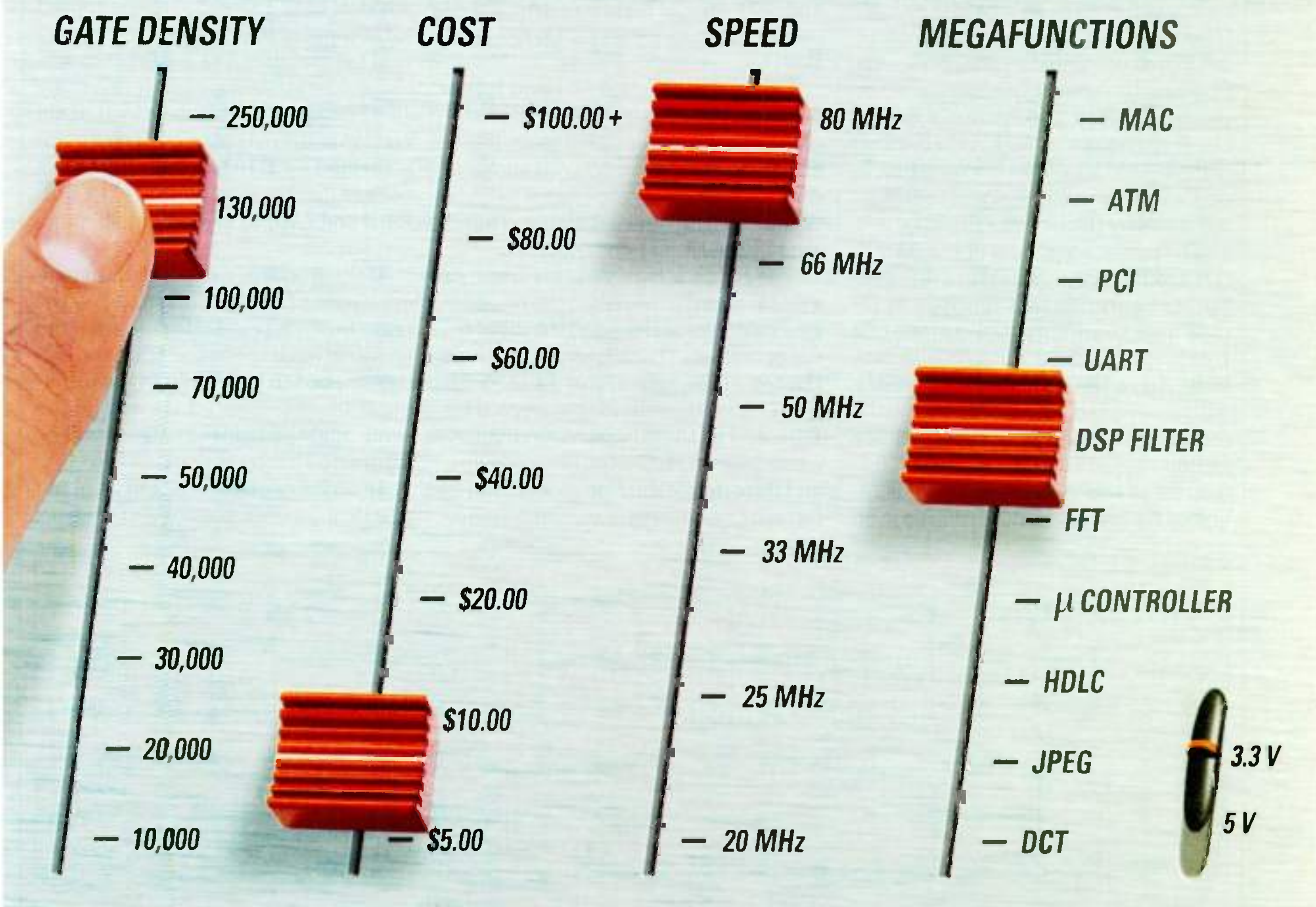


a. A line-power requirement (in dBm) alone does not give the designer enough information to select a suitable line driver. In order to convert the dBm power requirement back to peak voltage and current requiremen ts, the line impedance and the crest factor of the signal must be known.



b. Assuming a constant load impedance of 50 Ω, dBm and mW units can be related to dBmV and volts. For a different line impedance, the mV and dBmV scales will shift upwards or downwards relative to the dBm and mW scales.

The perfect mix.



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The ALTERA Advantage

The received signal is amplified by two low-noise op amps R1 and R2.

The transmit/receive block is commonly referred to as a hybrid, whose function is to deliver maximum transmit signal power to the line, while suppressing the transmitted signal in the receive circuitry. The figure of merit for the performance of the hybrid is called trans-hybrid loss. This is a measure, in decibels, of the suppression of the transmit signal by the receiver circuitry.

The power amplifiers of the AD816 (D1 and D2) are arranged in a differential configuration that receives its inputs from the differential outputs of a DAC. The amplifier outputs differentially drive the transformer primary with a turns ratio of 1:2. The line on the secondary side of the transformer has an impedance of 120 Ω. As a result, one quarter of this resistance (30 Ω) is required for correct back-termination on the primary side due to the impedance scaling by the square of the turns ratio. This resistance is divided in half (15 Ω) and put on each side of the drive buffers for symmetry (R101 and R201).

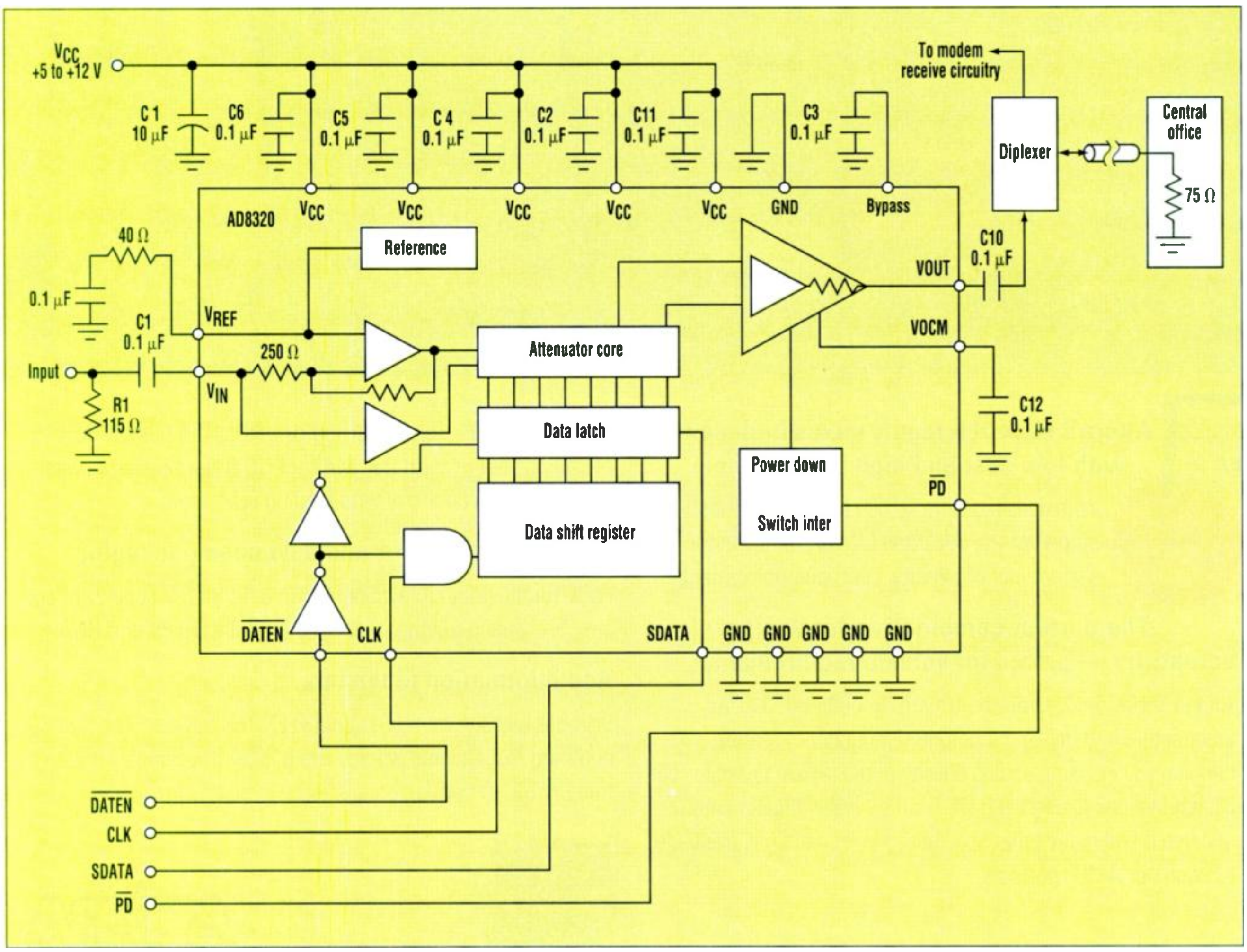
The receive section (R1 and R2) is configured as a pair of difference amplifiers that together produce a differential output. This received signal is composed of the receive signal in addition to the transmitted signal attenuated by the trans-hybrid loss.

The circuit is highly symmetrical, so a single-ended explanation can be easily generalized to understand the differential operation. The output of D1 drives the top of the primary of T1 through R101. A voltage divider is formed by R101 and all the downstream circuitry comprised of T1, the transmission line, and its termination. For an ideal transformer, transmission line, and termination, this will appear to be 15 Ω; thus the signal appearing at the input of T1 will be the output of D1 divided by two in the ideal case. This signal also is applied to the input of R1 via R105.

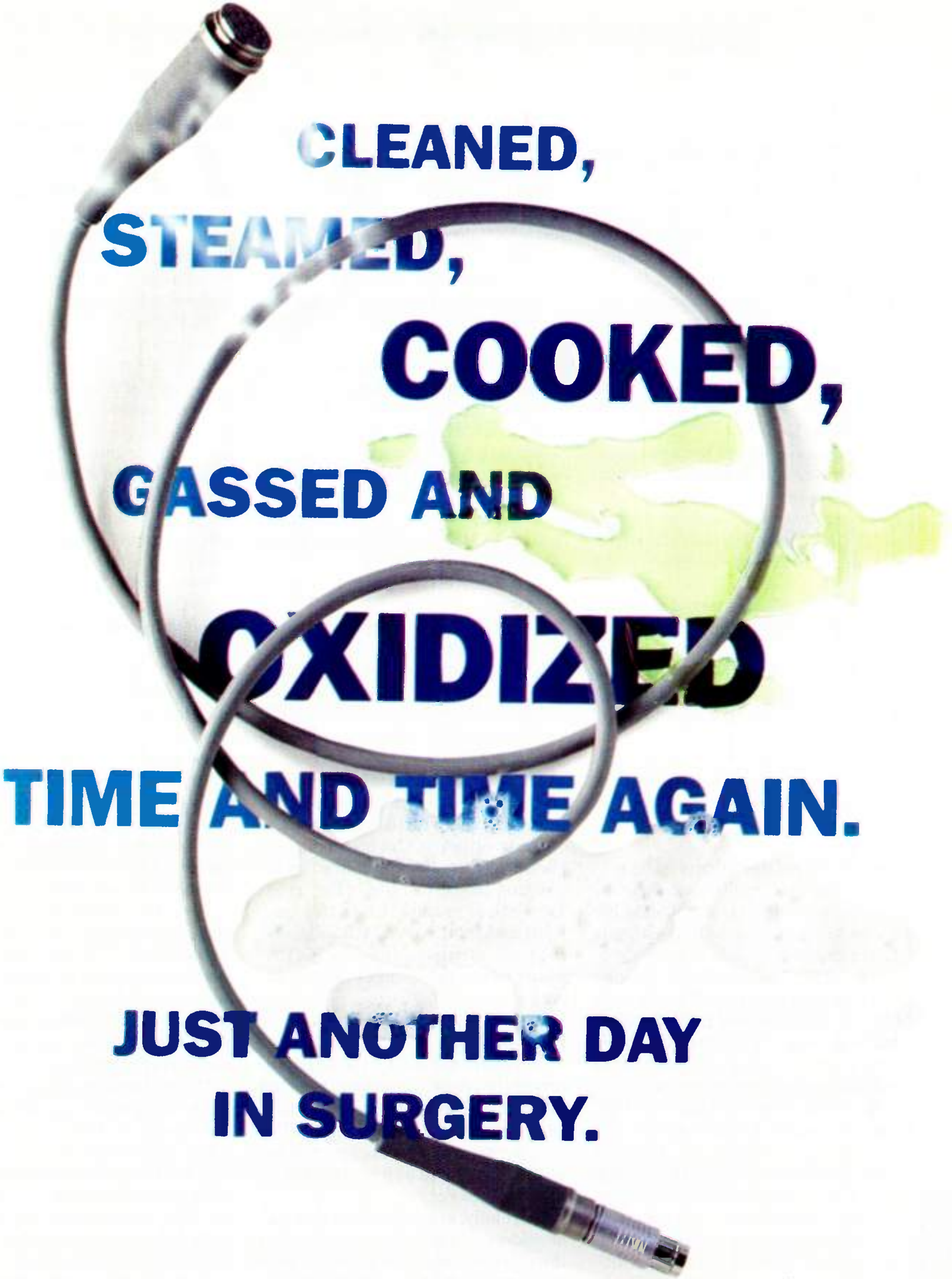
R1 is configured as a difference amplifier. The inverting input is driven by another signal that is a divided down version of the output of D1. This circuit is formed by R102 as one side of the voltage divider along with R103, C101, R104 and L101 as the other half of the divider.

If the frequency-dependent impedance part of this circuit matches the transformer, transmission line, and termination impedance, then the signals applied to both sides of the difference-amp-configured R1 will be the same, and the transmit signal will be subtracted out by the circuit.

In a real-world situation, it is not practical (or even possible) to subtract



5. A programmable-gain amplifier lends itself to driving a cable modem's upstream or return path. The use of a dynamic output impedance of 75 Ω cuts the required amplifier voltage swing in half, as compared to an externally terminated amplifier. This allows an output voltage of 3.1V peak-to-peak (+12 dBm) while operating on a single supply as low as 5 V.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OXIDIZED
TIME AND TIME AGAIN.
JUST ANOTHER DAY
IN SURGERY.

out all of the transmit signal (100% trans-hybrid loss) to provide a first-order cancellation. This, however, goes a long way toward reducing the dynamic range of the RCVOUT signal. The overall performance of this circuit depends on the ability to build a lumped element network that matches the impedance of the transmission line over the frequency range required for ADSL (from about 20 kHz to 1.1 MHz). The circuits formed by D2 and R2 and the AD816 are totally symmetric with those formed by D1 and R1 and work in the same fashion.

The receive signal from the telephone line creates a differential signal across the primary of T1. There is, however, a two-to-one reduction in amplitude due to the turns ratio of T1. This differential signal is applied to the + inputs of R1 and R2. The receive amplifiers buffer this signal and present a differential output. There is no significant receive signal applied to the negative inputs of R1 and R2. This is due to the attenuating effects of R101 and R201 and the low output impedances of D1 and D2.

As a result, the overall circuit provides first-order cancellation of the transmit signal and differential buffering of the receive signal.

Power Considerations

The line driver in this example delivers a power level of about +20 dBm to the line. With a line impedance of 120 Ω, this corresponds to an rms voltage level on the line of 3.5 V. Because the line interface transformer has a (step-up) turns ratio of 1:2 and because of the presence of the two 15-Ω back-termination resistors, each amplifier must deliver an rms voltage of 1.7 V

In ADSL systems that use DMT, there is a need to transmit signals with crest factors as high as 5.3. This high crest factor results from short (typically 10 µs) signal peaks that rarely occur (on average $1{:}10^{-7}$). But, the amplifier must supply the requisite voltage and current when these peaks occur.

Based on this, each op amp in the above example is required to occasionally deliver peak voltages of ±9 V (i.e. 5.3 × 1.7 V) and peak currents of ±300 mA. This peak-to-average ratio necessitates relatively-high power-supply rails (±15 V in this case).

The large amount of headroom between the supply rails and the rms signal level increases the dynamic power consumption in the amplifier to levels that are close to the amplifier's quiescent power. When doing power-consumption calculations for heat sinking purposes, it is important for the designer to remember that package power consumption is the sum of quiescent and dynamic power, not the sum of quiescent and load power.

It follows then, that dynamic power consumption can be reduced by reducing the circuit's power-supply voltages. While it would be prudent to reduce the power supply to a level that allows the op amps to deliver the required peak voltage (±9 V in this case), some signal clipping may be tolerable in some applications. In DMT applications, clipping of peak voltages tends to manifest itself as an increase in the level of the overall noise floor.

This will at some point begin to degrade the line's Bit Error Rate (BER). The best approach in such an optimization scheme would be to reduce the power supply voltages until the BER begins degrading below some acceptable minimum.

Some ADSL applications call for a line power of +26 dBm. Because there is little scope to further increase the output voltage of the op amps, this power level would be achieved by increasing the turns ratio of the transformer to as much as 4:1. In this case, R101 and R201 would be 3.75 Ω, and the peak current of the AD816 (1 A) would be the drive limit of the transmitter.

Heat Sinking

To ensure reliability, the temperature of the silicon die (usually referred to as the junction temperature) should be maintained at less than 175°C. For this reason, the IC package will require some form of heat sinking in most applications.

Normally, amplifiers like this will be soldered directly to a copper pad on the printed-circuit board. An important component of the resulting die-to-ambient thermal resistance (θ_{JA}) is the thermal resistance between the package and the copper pad. The lowest thermal resistance is achieved by employing a direct soldered connection between the package-to-copper pad. The use of heat-sink grease either with or without a washer will serve to increase this number.

Single-To-Differential Conversion

If the signal to be delivered to a line is single-ended, a single-ended-to-differential transformation must be implemented if the line is to be driven differentially *(Fig. 4)*.

In Figure 4a, Amp 1 has its + input driven with the input signal, while the + input of Amp 2 is grounded. Thus, the –input of Amp 2 also is driven to virtual ground by negative feedback. As a result, Amp 1 is configured for a noninverting gain of five ($1+R_{F1}/R_G$).

The –input of Amp 1, which has the same voltage as Amp 1's + input, serves as an input to Amp 2, configured as an inverting amplifier with a gain of –5 ($-R_{F2}/R_G$). Thus, the two outputs move in opposite directions with the same gain to create a balanced differential signal.

This circuit can work at various gains with proper resistor selection. But, in general, at least two resistor values have to be changed to change the gain of the circuit. In addition, the noise gains ($1+R_F/R_G$) of the two op amps will always differ by one (5 and 6 in this case). This gives the two op-amps differing closed-loop bandwidths. Signals at frequencies close to the closed-loop bandwidth will be unsymmetrically amplified as a result.

A second circuit that has none of these disadvantages is shown in Figure 4b. Each of the AD815's current-feedback op amps is configured as a unity-gain follower by the feedback resistors (R_A). Each op-amp output also drives the other as a unity-gain inverter via the two R_Bs.

If the + input to Amp 2 is grounded and a small positive signal is applied to the + input of Amp 1, the output of Amp 1 will be driven to saturation in the positive direction and the output of Amp 2 will be driven to saturation in the negative direction. This is similar to the way a conventional op amp behaves without any feedback.

Now, if a resistor (R_F) is connected from the output of Amp 2 to the + input of Amp 1, negative feedback is provided, which then closes the loop. An input resistor (R_I) will make the circuit look like a conventional inverting op-amp configuration with differential outputs.

The gain of this circuit from input to

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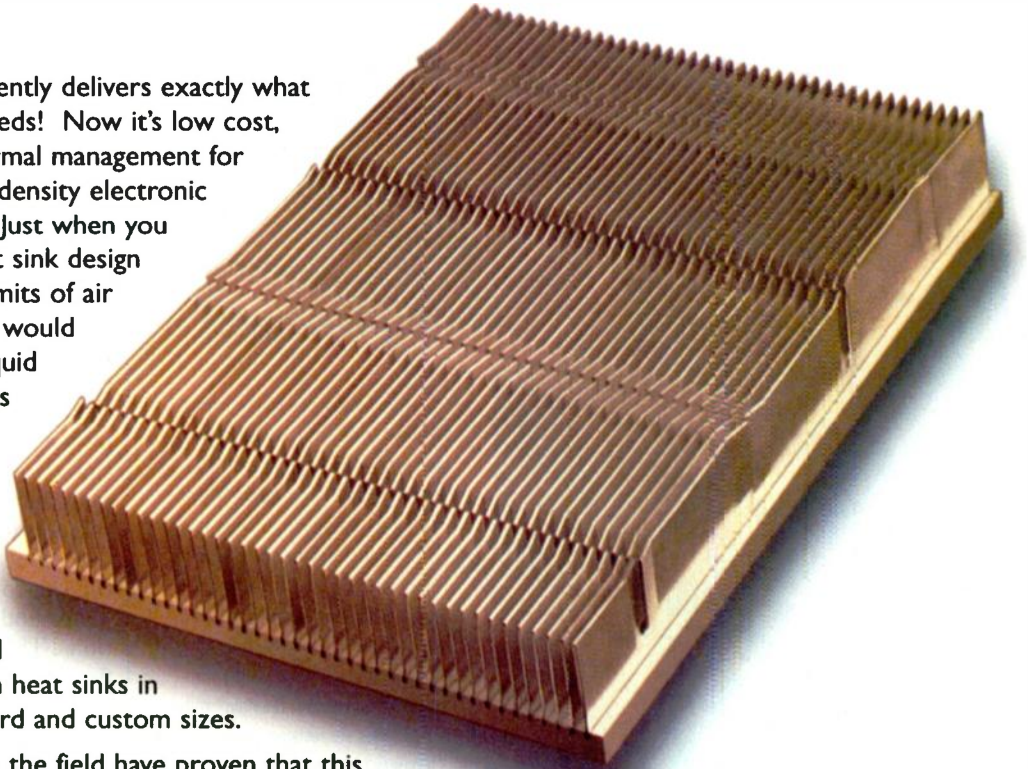

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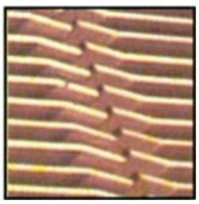

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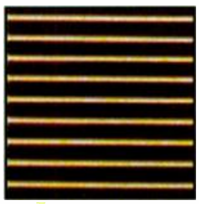

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either output will be $\pm R_F/R_I$. This also can be expressed as a single-ended-to-differential gain of $2 \times R_F/R_I$. With each output capable of swinging ±10 V (i.e., 20 Vp-p), the peak-to-peak differential output voltage is 40 V. The optional capacitor can be added to prevent any dc current in the transformer due to dc offsets at the output of the op amps.

Single-Supply Line Driving

Line driving in a single-supply environment presents some unique challenges. Signals must have a common-mode level that lies somewhere between ground and supply voltage, usually at $V_{supply}/2$. Because the output signal must swing within a smaller range, headroom between the signal and the power-supply rails also becomes an issue. Trying to get around this problem by using a rail-to-rail amplifier would seem to be an easy solution. However, in a line-driving context, there are some potential pitfalls to this approach.

Product datasheets usually specify the rail-to-rail performance of an amplifier under fairly light loading conditions. This may mean that the amplifier can only come to within 1 or 2 V of the rails when delivering high current. This problem is compounded by the reality that signal distortion generally degrades as signals swing closer to the power-supply rails (even under light loading conditions). Typically, a rail-to-rail amplifier should maintain at least 500 mV of headroom to each rail to preserve its specified distortion level.

Cable Modems

Emerging cable-modem standards are a good example of an application where the line driver must operate in a single-supply environment. Because this modem circuit is predominantly digital, needing only a single supply to operate, economic necessity demands that the analog line-driving circuit also make do with a single supply.

Depicted is a single-supply line-driving circuit for the "upstream" or return path of a cable modem (home to central office) *(Fig. 5)*. The input to the line driver, modulated in QPSK format, will generally be supplied by a DAC or a specialized QPSK modulator such as the AD9853. Because the input of the amplifier has a dc bias level of 1.9 V, the

input signal will normally be ac-coupled. The amplifier has an input impedance of 220 Ω. To give the circuit the 75-Ω input impedance, which is popular in video applications, an external 115-Ω shunt resistor to ground is added.

Cable modem standards in both Europe and the U.S. demand that the amplitude of the transmitted signal be variable. This allows the modem to compensate for the variation in signal attenuation as a result of differing distances to the central office. Either the line driver or the device driving it must therefore be able to vary the amplitude of the signal. In this example, the gain of the amplifier can be programmed over a 36-dB range (–10 dB through +26 dB) through an 8-bit serial interface.

To correctly terminate the line, the amplifier must present an output impedance also of 75 Ω. In this application, an external back-termination resistor is not necessary because the amplifier has a built-in or dynamic output impedance of 75 Ω. This halves the requisite output voltage compared to applications where an external back-termination resistor must be added. As a result, the amplifier is capable of delivering an output level of +12 dBm (about 3.1 Vpp) to the line, while operating on a single supply voltage of as little as +5 V.

Because data transfer by modem is intermittent, especially in the case of Internet access, upstream data is transmitted in bursts. While not transmitting, the amplifier can be powered down (by pulling the $\overline{\text{PD}}$ line low). This reduces the quiescent current to one-third of it's nominal value. However, the device's 75-Ω output impedance is maintained during power-down mode. This fulfills the requirement that all devices connected to a particular diplexer maintain a 75-Ω output impedance at all times so that the diplexer itself can maintain a 75-Ω impedance to the line.

Eamon Nash is an application engineer with Analog Devices' Advanced Linear Products Group. He holds a B.Eng in Electronics from the University of Limerick, Ireland.

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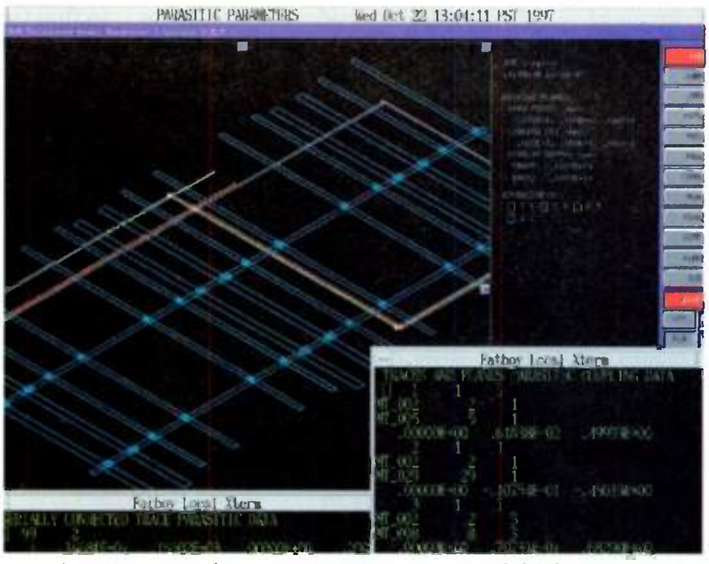
Cheryl Ajluni

SPECIAL REPORT

According to the National Technology Roadmap for Semiconductors, by next year, IC feature sizes will shrink to 0.25 µm and chips may contain as many as 28 million transistors. What many in the industry have already come to realize is that at 0.35-µm geometries, interconnect delays begin to dominate gate delays as the width of wires shrinks and the height increases. The problem only gets worse at 0.25 µm. In fact, it's estimated that at these feature sizes, interconnects will contribute up to 70% of the total delay.

This deep-submicron (DSM) design environment raises two important questions. First, how do you efficiently work with large-capacity designs? And, how do you ensure accuracy when device physics begins to wreak havoc? These are not easy questions to answer. Part of the solution lies in the process of accurately extracting a device's parasitics. The other part lies in the ability to accurately and quickly analyze parasitic information, and subsequently use it for design verification.

Earlier this year, this magazine attempted to weed out some of the many issues related to parasitic extraction and identify many of the proposed solutions (ELECTRONIC DESIGN, *Jan. 20, p. 111*). The only thing that has changed since then is industry perception and understanding of the true depth of the problems associated with parasitic extraction. It's clear that traditional extraction tools simply don't work at the DSM level. This fact has caused many companies to search for solutions and to attempt to answer the question: "What will a DSM design methodology look like?"



Art Courtesy: Pacific Numerix

To be honest, many companies still don't have an answer. After all, it's not easy to deal with issues of growing complexity, parasitic effects and the explosion of data it creates, shrinking time-to-market cycles, and verification. And these are only the beginning of a long list of issues that must be dealt with when designing in a truly deep- submicron environment. Recent tool developments may shed light on how to solve the problems associated with DSM design and parasitic extraction.

One of the stronger extraction product offerings comes from Simplex Solutions, Sunnyvale, Calif. Its multimillion-transistor-capacity solution, Fire & Ice, does full-chip hierarchical power-grid 3D extraction and is able to achieve accuracy to within 10% of measured silicon and Poisson solvers. It offers a number of features, such as the ability to handle extraction of multiple and conformal dielectrics and metal lines with high aspect ratios (height/ weight). This makes the 3D extracted data more manageable from a timing analysis viewpoint.

The tool's adaptive analytical models enable consistent accuracy results across a wide range of designs. A parasitic reduction option minimizes the size of the extracted parasitic net by using one of two approaches: either a detailed standard parasitic format (DSPF) reduction, which is within 1% of Spice accuracy and reduces typical signal nets by 90%; or a reduced standard parasitic format (RSPF) reduction that's within 10% of Spice accuracy, and produces a model of signal shape and delay for the net.

The company recently announced the expansion of its full-chip 3D extraction product line into support for DSM ASICs and application-specific standard products (ASSPs). Fire & Ice now provides overnight turnaround of extraction for all nets with no loss of modeling accuracy. The result is a highly accurate view of timing on multiple revisions of the design before first silicon, a benefit that can save weeks of work and, in some cases, millions of dollars.

Key to the overnight turnaround is a scope selection feature that allows designers to limit extraction to the minimum set of interconnect parasitics required for accurate timing analysis. This means that designers can make speed versus depth trade-offs, and refine how much design data is taken into account during extraction as the design is completed. Three techniques are used to limit extraction detail: black, gray, and white box. With black box, all signals or a group of signals of interest are extracted, but with no visibility into the underlying region such as a field of standard cells. Gray box extracts either all signals or a group of signals of interest while offering visibility into the underlying design data that interacts with it. White box, the default mode of operation, extracts all capacitances with full detail, including such things as interconnects within a cell.

Companies Mentioned In This Report

Frequency Technology
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CIRCLE 528

Mentor Graphics
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CIRCLE 529

Pacific Numerix
7333 E. Doubletree Ranch Rd.;
Ste. 280
Scottsdale, AZ 85258
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CIRCLE 530

Simplex Solutions
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Ultima Interconnect Technology
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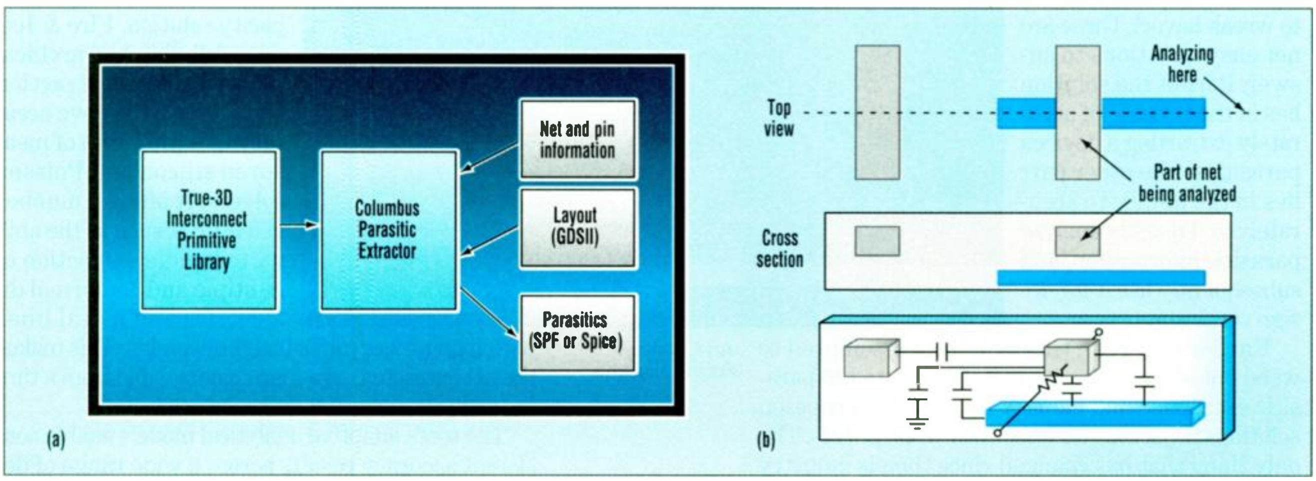
One of Fire & Ice's advantages is its integration with many standard place and route and timing-analysis tool suites. This allows designers to perform accurate 3D extraction of place-and-route data, analyze the timing, modify the routing, and then re-extract in significantly less time than it takes using other less accurate, non-3D extraction tools. The interface is based on standard formats LEF/DEF, DSPF, and RSPF. As an added benefit, Fire & Ice offers a net-by-net extraction capability. This feature is ideal for situations in which the designer is only interested in a few nets, or when a small change is made to the design and just a few nets need to be re-analyzed.

Simplex's Thunder & Lightning tool has now been enhanced with the company's newly developed SIFT (Signal Integrity Filtering) technology. This allows designers to analyze full-chip coupling networks and identify all nets in a design that are prone to fatal signal-integrity problems. At 0.25-µm design geometries and below, the probability of signal integrity failures increases dramatically. Since signal integrity problems can cause a design to fail, the SIFT technology capability is especially critical because it, in effect, offers designers a practical, and accurate way to find the nets at risk and verify designs for delay and noise problems.

Based on Thunder & Lightning's high-capacity transistor-analysis engine, SIFT can analyze multimillion-transistor designs with hundreds of thousands of nets in a matter of hours.



1. Columbus from Frequency Corp. accepts geometric and naming information about a design and produces accurate electrical equivalents for specified nets (a). A True-3D Interconnect Primitive Library supplies Columbus with a complete description of process interconnects (b). When analyzing at the point indicated, Columbus evaluates a 3D structure into primitives associated with this cross-section. It then looks up each primitive in the Interconnect Primitive Library to build the structure's equivalent electrical model, including resistance along the line it is analyzing and capacitive coupling to other nets and to ground.

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It does this by evaluating the effects of coupling capacitance, drive strength, and load on every net in the design. It calculates the aggressor-victim relationships between the nets and determines which ones may be adversely affected by other nets. SIFT then produces a short list of nets for further detailed analysis.

While Simplex, like other notable EDA companies, has chosen to offer a parasitic extraction and analysis flow for the designer, there are others who have opted for a much different approach. What some have come to believe is that no one company can provide all the pieces of the puzzle that will be necessary for design and verification in a true DSM environment. The solution, according to this camp, is to provide a common database that will act as the focal point for a DSM design and verification flow. With an open environment, each company could then focus on providing its core competency in the form of a plug-in tool. Since the tools would all work off one central database, consistency of data would be assured.

This approach is being proposed in a number of formats by industry associations and EDA vendors alike. Sematech, for example, is expected to soon release the API. While such an open environment approach may offer a number of benefits, the problem is that many EDA vendors have staked their company's success on not just providing point tools but true flows and methodologies from the front end to the back end. Many of these companies may not wish to give up their core strengths so easily in support of an open environment.

One of the companies offering an approach based on a common database is Mentor Graphics, Wilsonville, Ore. Its solution, Calibre, is proposed as a sort of de facto standard in much the same way as Dracula from Cadence, San Jose, Calif., has been for many years. At the center of this framework are two sets of databases: FDB (filtered database) and PDB (parasitics database). FDB stores all of the information, including full geometric and connectivity, collected from the critical nets in a design. This information is then input into the pattern-based parasitic extraction engine, where, using a hierarchical circuit recognition technology, connectivity for multimillion device chips can be generated in a manner of minutes. The resulting data is collected and managed in the PDB. This database consists of electrical models created by the extraction engine from the physical interconnect. Subsequently, as different analysis tools are called on downstream by the designer, the appropriate information can be imported from PDB to the analysis tool.

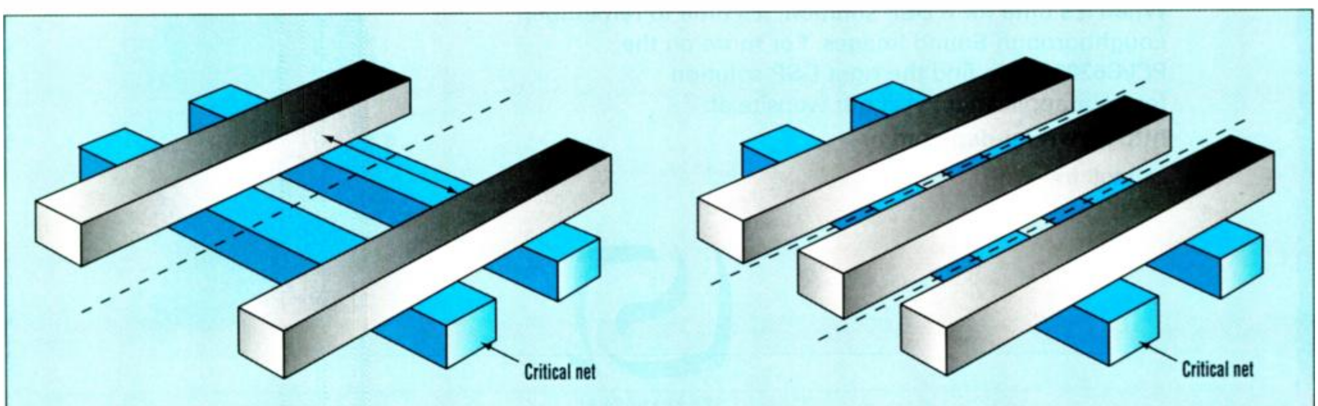
Mentor's parasitic extractor tool, xCalibre, can be utilized in the context of this framework. It is based on a pattern extraction engine and works by traversing the nets of a design and applying a set of models to patterns that it encounters. The models are based on templates, or fundamental cases, that have been developed by Mentor. The user has the option of encoding into the rules file a comprehensive suite of custom models based on these templates.

There is already some acceptance for Mentor's common database. Frequency, San Jose, Calif., for example, has developed a highly accurate DSM extraction solution that fits easily into Mentor's DSM Calibre environment. During typical operation, xCalibre might be used to screen a design for critical nets. Once these nets are identified, Frequency's tools can be employed for very accurate extraction.

Frequency offers a solution to extraction that focuses on bringing the process into the design flow in an effort to address the problem caused by the interconnect barrier. As the company explains, there are two sources of inaccuracy today when it comes to interconnects. The first source is attributed to not knowing the process well enough. As a result, designers are often faced with a garbage in, garbage out situation. Simply put, if you don't know what the process is, you can't solve the problem. The second source is the inability of current tools to meet the needs of a DSM design environment.

These inaccuracies in timing analysis occur in DSM designs because contemporary timing analysis software does not adequately model the effects of the interconnect. As a result, engineers have to overdesign their ICs, ending up with chips that are significantly larger and slower than the deep-submicron process is capable of producing. This, in effect, makes the interconnect a barrier to fast, efficient, and effective designs. To combat the inaccuracy, Frequency offers what it refers to as true 3D technology which it does not use to extract the transistors; but rather all of the nets from a particular design.

To address the issue of inaccuracy from the process, the company works with process owners to get all pertinent details related to the process and the design. From this information, it can de-



2. Boundary effects that are caused by net decomposition (cutting) are a major source of errors in the process of extraction. The Ultima-PE tool uses "smart cutting" that allows the designer to determine where it is safe to cut. For example, cuts can be made when the normal component of the field is negligible. Or, for dense layout structures, periodic boundary conditions can be applied.

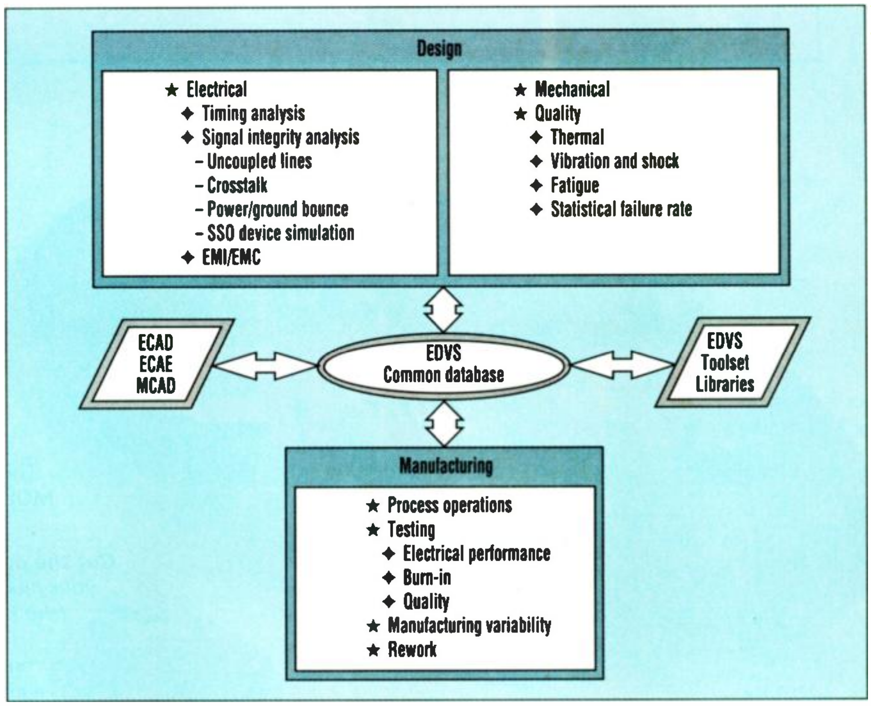
velop a library database consisting of physical dimensions of the process. This information can amount to an average of five layers, and a dielectric constant and spacing, among other things, for each layer. This process typically takes a couple of weeks to complete. All of the information is stored in the company's Interconnect Primitive Library, which consists of tens of thousands of interconnect primitives. Combinations of these process-specific primitives describe every piece of interconnect in a design. Each primitive is accurately analyzed using a compute-intensive field solver.

This information can then be used in Frequency's parasitic extraction tool, Columbus *(Fig. 1)*. Says Martin Walker, Frequency's president and CEO, "The best contemporary tools available offer a ±30% error in predicting the performance of DSM IC interconnect. Our True-3D Technology narrows that error down to a verified 10%."

True-3D technology works by extracting process-specific 3D design data from a completed chip layout. To do this, it first fills in the historical information gaps in process characterization with details from the Interconnect Primitive Library. Then, it utilizes advanced parasitic extraction algorithms for accurate analysis.

Columbus is not a full-chip parasitic extractor; instead, it's used only on critical nets where a single net is extracted at a time. It accepts standard net-, pin-, and layout-data formats and produces standard outputs for driving-timing analysis. During operation, the tool accesses the information stored in the Interconnect Primitive Library. Then, as it is applied to critical nets in a design, it is able to provide accurate electrical descriptions for each feature of a net. The resulting output data is then passed on to the timing analyzer. The tool interfaces to a number of existing EDA tools.

Since Frequency's tool focuses only on critical net extraction, it is complementary, rather than competitive, with many of the other full-chip extraction and analysis tools on the market. What the company does is provide the extraction. It lets other EDA companies focus on the analysis. One disadvantage of the tool is that currently the Interconnect Primitive Library must be created by Frequency and this process tends to take time. But in the future, the company will offer a tool that will allow customers to build the library primitives in-house.



3. Pacific Numerix's EDVS consists of a central database of information. A number of module-like analysis tools also are available to the user. When a particular module is accessed, all necessary information is immediately called up from the central database and imported into the tool. As a result, users can perform analysis for any level of design: IC, pc board, MCM, or system.

Ultima, Sunnyvale, Calif., also supports an open environment solution, whether it be Mentor's FDB and PDB, Sematech's API, or some other as-yet undefined environment. Like Frequency, Ultima focuses on the accuracy of critical net extraction. It differs in its approach to accomplish this goal. Ultima offers parasitic net extraction that is technology-dependent, but design-independent. It does extraction on a selective net, rather than a net-by-net basis.

The company recently introduced a parasitic extractor tool known as Ultima-PE. As a complement to the more conventional 2D or quasi-3D extractors, Ultima-PE is marked by three unique features. The first feature is its Library-based 3D extraction technology. This technology provides the performance of 3D extraction by using a 3D interconnect library. The library consists of pre-characterized 3D structures typically found in layouts.

Each structure is represented by a closed-form formula which provides results that are very close to a 3D field solver. Process variations are accounted for within the closed-form formulae. In comparison to Frequency's Interconnect Primitive Library, Ultima's library can be created automatically at the customer's site, by the customer, in one to three days. This is a key advantage of the tool since no extra time is needed upfront to create a library for a particular design.

The Ultima-PE tool incorporates a 3D field solver that is based on GIMEI (Geometry Independent Measured Equation of Invariance) technology. This technology is an improved version of the MEI computational electromagnetic technique. It is used for capacitance extraction of general 3D VLSI interconnects. The MEI technology is able to terminate the meshes very close to the object boundary while still strictly preserving the sparsity of the FD (Finite Difference) equations. As a result, the final system matrix encountered by MEI is a sparse matrix with size similar to that of integral equation methods. However, complicated Greens function and Sommerfield integrals make the traditional MEI very difficult, if not impossible, to be applied to analyze multilayer and multiconductor interconnects. The company's new GIMEI technology can directly address these inadequacies associated with the MEI technology.

Another unique feature of the Ul-

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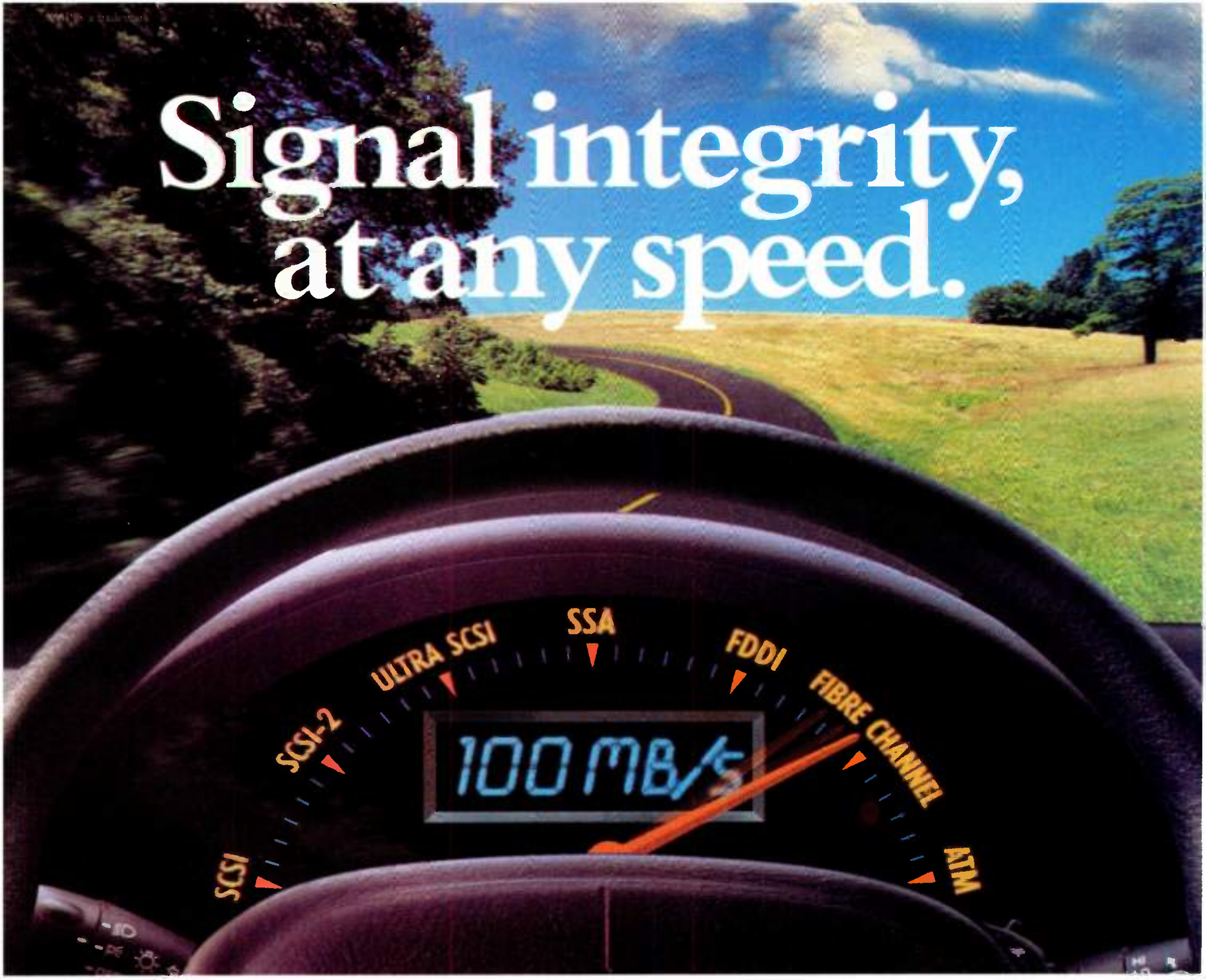
tima-PE tool is its smart-cutting capability *(Fig. 2)*. This feature, based on the company's smart-cutting algorithm, allows for the decomposition of long nets into smaller segments. Traditionally, cutting results in loss of accuracy due to boundary Boolean effects. The longer the nets, the more cuts that must be made. And, in turn, the more boundary errors that occur. This is especially true of high-capacity DSM designs. With the smart cutting algorithm, however, Ultima can control the boundary effects by cutting a little distance away from discontinuity where the normal component is negligible. As a result, Ultima-PE can extract chip-level nets with accuracy close to 3D solver solutions at speeds approaching 2D extraction.

Also offering a parasitic extraction tool based on a common database approach is Pacific Numerix, Scottsdale, Ariz. This relatively small and unknown company boasts a powerful set of highly integrated tools for the simulation of electrical and mechanical designs and manufacturing processes. The offering, known as the Electronic Design Validation System (EDVS), is the result of a multiyear project involving Pacific Numerix and IBM *(Fig. 3)*. It's comprised of a series of modules that handle any level of design—IC, first-level package, pc board, and system—to help electrical/mechanical engineering and manufacturing teams quickly and accurately predict proposed-design behaviors.

Specifically developed in anticipation of DSM designs, the analysis tools overlay existing infrastructures and operate off of a single database obtained from any combination of ECAD/ECAE systems. The EDVS tool suite, which provides virtual design to manufacturing prototyping, resides within a network and can be accessed by workstations or PCs. It utilizes an extensive library capability.

At the heart of EDVS is Parasitic Parameters, a general-purpose parasitics extractor that accurately extracts frequency-dependent resistance (R), inductance (L), capacitance (C), and conductance (G) parameters for any arbitrary 2D or 3D geometry. Geometry data can be obtained from AutoCAD DXF, Gerber, GDSII, IGES, or Pro-E with its built-in interfaces. Once data is retrieved, the tool has access to a number of advanced algorithms for extraction. The Boundary Integral Solution and



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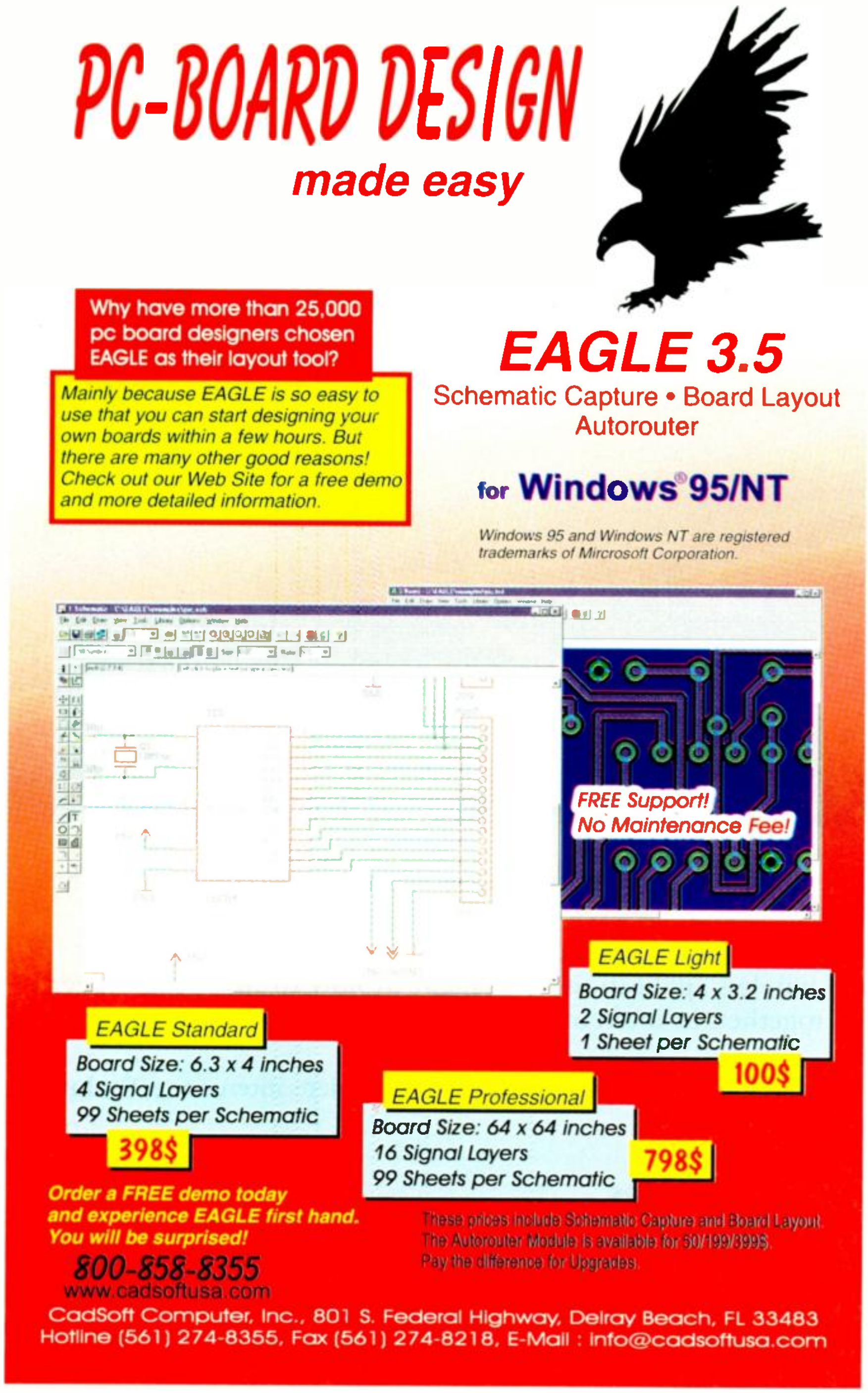

Green's Function are used to extract C and G parameters. The Partial Element Equivalence Circuit (PEEC), developed by IBM, and Neumann's Filament Formula are used to extract R and L parameters. The parasitic values can be output in Spice subcircuit format and simulations run to examine ringing, crosstalk, under- and overshoot, and power/ground bounce. The tool also provides full automatic 3D modeling of entire packages directly from Pro-E, IGES, and AutoCAD DXF. Power and ground bounce subcircuits containing 3D R, L, C, and G results matrices can be automatically generated and used as input into one of the company's signal integrity modules. Power and ground planes are automatically meshed non-uniformly to match input and output via patterns.

The same extraction technology found in Parasitic Parameters is used in Pacific Numerix's EDVS Signal Integrity Toolset. In particular, the Pre-Physical Design Signal Integrity tool relies on extraction technology to perform parametric studies on critical nets to determine early in the design cycle optimum conductor sizes and spacings, selection of dielectric and conducting materials, thickness of dielectric layers, and power and ground plane locations.

During operation, interactive routing creates the pin to pin trace and via geometry for a new net. Then, 2D or 3D parasitic models are automatically created for this new net geometry structure. Frequency-dependent R, L, C, and G parasitics can then be extracted and transmission line or Spice simulation performed. This tool is for use at the chip level and is specifically optimized to provide full support for the problems associated with design in a deep-submicron environment. Some of the signal integrity problems it can detect and correct include wave propagation delay, clock skew, waveform distortion, crosstalk noise, electromigration, power saturation, and ground bounce. The tool also features powerline current and voltage distribution analysis, and allows the interconnect delays to be back-annotated to logic simulators through an SDF interface.

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STANDARDS WATCH

Implementing Hot Swap On CompactPCI

Rob Davidson, Ziatech Corp.

The goal of hot swap for CompactPCI is the ability to hot swap adapter cards without disturbing the bus, and in a way that provides a standard means of notifying the software. The CompactPCI Hot Swap Committee, working within the PCI Manufacturers Group (PICMG), is getting close to finalizing this specification. The challenge for the committee has been to maintain the advantages of CompactPCI (PCI silicon, eight slots, passive backplane) and provide hot-swap functionality at a reasonable price.

An approach for the server market has been developed by Compaq Computer Corp. called "Hot Plug" PCI. This approach uses switches to isolate each slot and requires the operator to "disable" each slot through software. This is a good solution for the server market where the slots are limited. The cards could be any size and there will always be a monitor and keyboard present. However, it's not suitable for CompactPCI because the addition of control switches means the backplane is no longer passive. Switches reduce the number of slots that can be employed and CompactPCI systems are often found in embedded environments and have no user interface.

Currently, the most interest for hot swap is for high-end telecommunications and data-communications servers with large numbers of custom cards plugged into a system with a standard backplane and CPU. The ability to replace these I/O cards or add new ones to a running system is key to reducing down time and maintenance costs.

The CompactPCI Hot Swap approach takes advantage of the mechanical features of the IEC 1101.10 packaging standard and the 2-mm connector in the core CompactPCI specification. These features ensure that cards mate and unmate with the backplane in a controlled fashion that allows for power and enable signals to be sequenced. As a result, the backplane signaling is not affected by the addition and removal of a card. Ziatech recently demonstrated the Hot Swap approach with a working system under Windows NT.

The problem that arises is how to alert the operating system and application that a card's status has changed. The method being proposed for CompactPCI hot swap, called "Distributed Hot Swap" or "Dynamic Configuration," involves the addition of two pins and some registers to the PCI bus interface chip. This method defines an interrupt line and status registers and results in a particular sequence for hot swapping boards.

For removal, the user presses down on the card-ejector handle, breaking a microswitch that's connected to PCI interface chip. This chip drives the ENUM interrupt line to the host CPU, thereby signalling a change in status. The Hot Swap driver on the CPU reads the status register to determine which card is changing, and to what state. The Hot Swap driver stops the device driver for that card and signals PCI interface chip to turn on an LED on the board. This LED is an indication to the user that it's OK to go ahead and remove the card.

As the user removes the card, the enable pin breaks contact first, causing all the PCI signals on the card to be disabled. Those signals then break contact, followed by a disconnection of the power and ground pins. Software is then notified that the card has been removed.

For insertion, ESD is discharged by static strips on the card's edge and the front-panel pins. As the card meets the bus, the power and ground pins connect, followed by a connection of the PCI disabled signals. The enable pin contacts and PCI signals are enabled on bus, and the card drives the ENUM interrupt to signal the CPU. As a result, the Hot Swap drivers interrogate the status registers to determine the card's state. The Hot Swap driver enables the system driver. Therefore, full operation resumes.

Employing this solution means that a Hot Swap card for CompactPCI will require changes to the PCI silicon interface. However, it doesn't involve a large number of chips. In fact, the main suppliers of these chips, such as Digital Semiconductor, PLX, and Tundra, have already endorsed this approach.

It's interesting to contrast this approach with the Hot Plug approach that doesn't define the hardware interface between the Hot Plug device driver and the hardware, instead leaving that to the system vendor. This means that each system vendor must develop a Hot Plug driver for each operating system. Employing the CompactPCI approach, on the other hand, means that a driver can be developed once for each operating system and used on a wide variety of CompactPCI platforms. It also allows for Hot Swap and non-Hot Swap CompactPCI cards to be mixed in the same system.

Three-Dimensional Architectures

When a computer architecture can be drawn as a three-dimensional geometric figure (cubes, cylinders, pyramids, etc.), the behavioral characteristics tend to be three-dimensional. Buses, rings, and crossbar architectures, however, are two-dimensional in their structure and behave differently—some for the better and some for the worse.

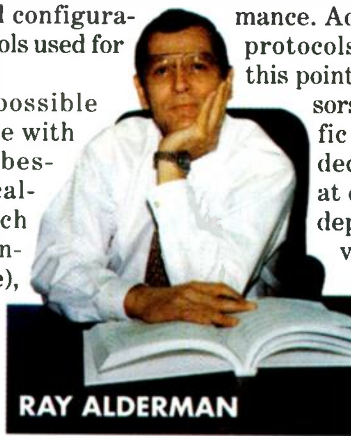
When we hook multiple nodes together in geometric 3D structures like cubes or pyramids, we can see behavioral similarities with other architectures. A cube structure acts much like a stack of rings connected at four points, like the Cox Communications Ring-In-Ring architecture discussed in my last column (ELECTRONIC DESIGN, *Nov. 3, p. 92*). A pyramid behaves much like a cube.

The primary aberrant behaviors of 3D architectures are the same as those of the ring, but only worse: routing latency and switching latency. The data paths between the points in the structures are point-to-point connections, eliminating the blocking latency we normally find on a bus.

When data is sent from any corner of a cube (or from any point in a pyramid, for that matter), the receiving corner node must read the address of the destination. If the address matches, the data is routed onto that node's local bus. If there's no address match, the node has two options—either send the packet to the next node on that plane of the cube, or send the packet up or down to another plane.

The behavioral difference between a ring and a cube is that the cube has two routing options at each node while the ring has only one. But, making that routing decision takes time, resulting in a routing latency. The switching latency occurs when one of the two paths is selected.

In a single cube with eight nodes (one node at each corner), the worst-case transaction latency occurs when there are three nodes plus three data paths. The best case is one path with no additional node overheads. This also depends on whether the connections in the cube are in a point-to-point or bidirectional configuration, and on the protocols used for transactions.


RAY ALDERMAN

There are many possible variations-on-a-theme with cubes involving cubes-within-cubes, vertical-stacked cubes (which looks like the Ring-In-Ring when you're done), or end-stacked cubes (which look like a group of train cars). When cubes are connected to other cubes in this fashion, all of the nodes have four connections instead of the typical three found in a single cube. This extra connection at each node gives a single cube, or stacked-cubes, more survivability than a ring. If several paths are cut in the cube, there are other ways to get the data to the destination. If you cut any section of a ring, it dies without a whimper.

In past years, some minicomputers were built with pyramid architectures, but they weren't very scalable. Some years later, the cube architectures were developed by the parallel-processing community using Transputer chips and an architecture called HIC (Heterogeneous InterConnect) and a protocol stack called DS-Links. A great number of these "Hypercube" machines were built to run applications like modeling and graphics. But, these architectures were never fully accepted for mainstream computer applications.

With a pyramid, you could connect five nodes, and that was all we needed back in the 1980s. The hypercube expanded that to eight nodes in the 1990s. Then, stacked cubes allowed us to add nodes to the structure four at a time without serious degradation problems in performance,up to a point.

Ultimately, all 2D and 3D architectures reach a "knee in the curve," where the next nodes added can't perform near 100% capacity, and their maximum scalability point is reached. Buses may work well up to about four processors, and then decline in individual processor performance. Adding cache-coherency protocols to the bus may raise this point to six or eight processors depending on the traffic patterns. Rings start declining in performance at eight to sixteen nodes depending on transaction volume. Cube architectures may reach the knee of the curve at 16 or 32 nodes. It all depends on the transaction mix and the transaction volume between nodes. That's why the model we use to calculate architectural performance is a dynamic statistical model, not a static linear model. Even after you do best-case/worst-case analysis, you still can't predict with any true degree of accuracy of how the architecture will really perform. Different applications create different traffic patterns and different transaction volumes on the data paths. So, your best analysis is still an educated guess.

The primary objective of the 3D architectures is to hook together a large number of nodes with very high bandwidth connections and minimum latency at a cost equal to that of buses and networks. This, however, is an architectural impossibility.

Ultimately, these 3D structures will be relegated to a small specialized segment of the computing spectrum for cost and complexity reasons. Every month, we find new ways to make 2D architectures like buses, and switch fabrics run faster without all the 3D headaches. Three-dimensional architectures are fun to play with, yet hard to program, and inappropriate for mainstream applications. They are technological bubble-gum for computer designer's minds—occasionally you get to blow a bubble, so it's worth all the chewing.

In a future column, I'll be taking a look at the super-scalable architectures, which includes Fat Trees and Clos Switches.

Ray Alderman is the Executive Director of VITA. He can be reached at exec@vita.com.

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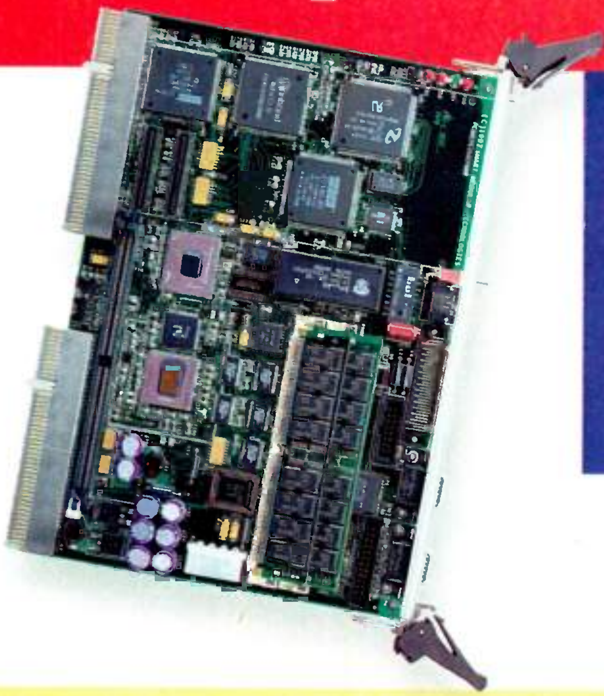

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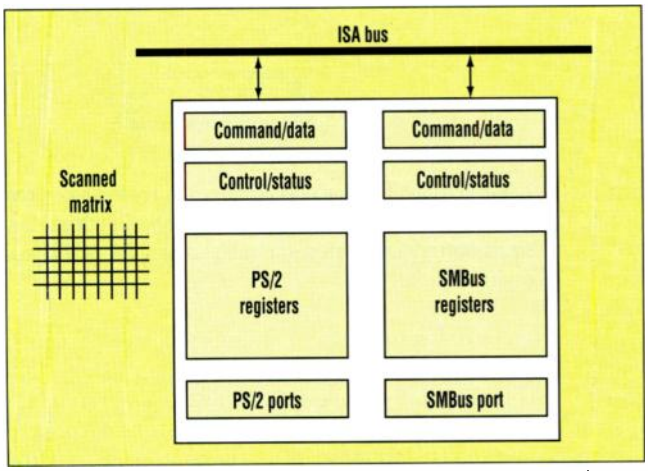
READER SERVICE 181

Harness The Power Of The ACPI/Smart-Battery Standard

Effective Implementation Yields Longer Battery Life Through Proper Charging.

JOHN MILIOS, USAR Systems, 568 Broadway, #405, New York, NY 10012; (212) 226-2042.

The Advanced Configuration and Power Interface (ACPI) provides a method for accessing devices that historically haven't been supported by bus standards in the PC architecture. Because they require specific hardware, portable computers will be one of the most significant beneficiaries of the new specifications. Smart batteries, chargers, selectors, LCD and power-plane controls, as well as several other components previously accessed only through proprietary methods, can now be designed and accessed directly by the operating system in a uniform manner. As a result, the Advanced Configuration and Power Interface reduces the development time and costs for new system designs.



1. Register addresses and specific interrupt numbers are not fixed in an ACPI-compliant system. However, controllers that deviate from what's defined in the specification must be supplemented within the BIOS describing the access method to the specific hardware.

Smart batteries and other related components, including smart battery chargers and smart selectors, are merely a subset of the system-management bus (SMBus) devices that are used in each system. SMBus devices at the bottom of the tree communicate upward through the signaling and command protocols, as outlined in the SMBus specification.

Specific device drivers and applications communicate with each SMBus device through the ACPI using either an ACPI-compatible embedded controller (EC) or other access methods described in the system's BIOS. Data is then communicated to each SMBus device individually, through functions consisting of one or more SMBus command protocols.

EC As A Key

Although new generations of chipsets for desktop and some laptop applications may come equipped with an I^2C port that can be used for communicating with specific SMBus components, employing an EC as an SMBus master is necessary in most portable implementations of the smart-battery system. The principle reason for this is battery-system safety.

Smart batteries and other related components, such as smart chargers and smart selectors, are merely a subset of the SMBus.

One of the most critical functions of the EC in this context is to block any commands originating from the operating system or applications that attempt to control specific smart-battery-system functions. Such accesses, intentionally or unintentionally, can jeopardize the system operation or, under certain conditions, may even create physical hazards.

Although register addresses and specific interrupt numbers are not fixed, the register functionality is fully detailed in the specification *(Fig. 1)*. Controllers that deviate from these specifications have to be supplemented within the BIOS, describing the access method to the specific hardware.

The EC registers occupy two addresses, one for bidirectional data transfers and one for status information and command control. Through these registers, device drivers and the operating system can access a second register block residing within the EC and used for SMBus control, as well as data transfers to and from any SMBus devices.

More than one EC can be used in the same system, if necessary. In a portable system, where both space and I/O requirements are at a premium, it's desirable to integrate the embedded controller with other necessary system functions, or with the user-input device controller. Depending on the general architecture of the chip set that's employed in the system, the designer has several options to choose from.

Dedicated EC

A dedicated EC is the preferred implementation in portable systems where a PS/2 keyboard controller is built into one of the multifunction ICs, PS/2 is not used at all, or extended I/O capabilities are required. A dedicated EC can be configured to perform a set of smart battery and system-control functions *(Fig. 2)*.

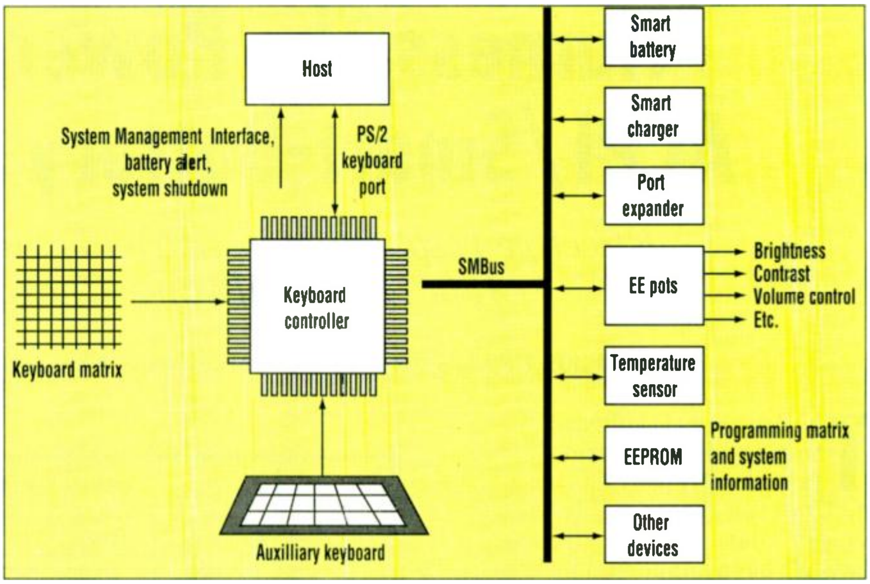
The added cost and necessary real estate associated with this implementation can be compensated for by integrating other SMBus functions into the EC, such as a smart charger, smart battery selector, and LCD control functions. Alternatively, these functions would have to be implemented using dedicated ICs.

On the USAR ACPITroller, an example of an EC, these additional functions are modeled as virtual SMBus devices, accessed through the standard ACPI register interface. The operating system and device drivers can communicate with these virtual devices employing standard ACPI methods without any additional software overhead.

Using a combination EC-keyboard controller, the EC function is combined with those of the PS/2 keyboard controller. The microcontroller implements two sets of registers—one for the PS/2 and one for the ACPI interface. The part also handles the embedded user-input devices and typically provides a set of PS/2-compatible ports for external input devices *(Fig. 2, again)*.

Another alternative is to employ a combination keyboard scanner-SMBus host device, which is suitable for single-board computers and chip sets with built-in keyboard controllers. In this configuration, the keyboard scanner acts as an SMBus host, routing SMBus data through the PS/2 keyboard port to which it's connected.

Because the ACPI prohibits access to the SMBus through the keyboard controller-registers, ACPI compatibility can be maintained by trapping I/O addresses through system management interrupts (SMIs). When the system must communicate with an SMBus device, it attempts to write to a virtual register, causing an SMI to occur. The SMI code takes control and communicates the data to the EC using the keyboard-controller registers and the PS/2 port.



2. When a multifunction IC is employed as the keyboard controller in a portable system, a dedicated EC is one method of implementation. Such an IC can be configured to perform a set of smart-battery and system-control functions. The part also can handle the embedded user-input devices.

When an SMBus device needs to communicate with the system, it issues a system control interrupt, signaling the system to read data through the I/O trapped addresses. This method works well in single-board computers, such as those that emulate the keyboard-controller functionality with system-management code. In systems that use a traditional keyboard controller, the method requires a dedicated SMI for SMBus byte transfers through the PS/2 port.

What's Next

Standardization of the smart battery system and power management through the operating system with the ACPI will shorten design time for new systems while increasing their reliability. SMBus implementations, as shepherded by the Smart Battery System Implementers Forum, are rapidly creating new devices. These are used commonly in portable systems, such as backlight controls, LCD contrast and brightness adjustment circuits, and temperature sensors. Such new devices, added to the hundreds of I2C devices already used in embedded systems, can be accessed through the operating system using standard methods, thereby eliminating the cost and complexity of a custom BIOS.

However, what's more important is that application programs are provided with better means of power-management awareness through the operating system. An application, for example, can interrogate the battery for remaining capacity, or even ask "what if" questions directly related to the power needs of specific tasks.

Power-management-aware applications also can self-adjust their operation based on information provided by both the operating system and the smart battery system components. For example, a word processor can adjust its auto-saving features based on information related to the battery's remaining capacity. Or, it can provide information to the CPU about the speed required for user-acceptable completion of the current task.

John Milios, President of USAR Systems, holds a Ph.M. degree from Columbia University, and an MSEE and a BS in Physics from the University of Athens, Greece.

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HUF75343P3/S3/S3S/G3	TO-220/262/263/247*	75	9
HUF75339P3/S3/S3S/G3	TO-220/262/263/247*	70	12
*HUF75337P3/S3/S3S/G3	TO-220/262/263/247	62	14
HUF75333P3/S3/S3S/G3	TO-220/262/263/247*	56	16
*HUF75329P3/S3/S3S/G3	TO-220/262/263/247	42	25
*HUF75321P3/S3/S3S	TO-220/262/263	31	32
HUF75321D3/D3S	TO-251/252	20	32
HUF75309P3/D3/D3S	TO-220*/251/252	17	70
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WHAT'S ON BOARD

Tackling the high-end of the storage spectrum, the second-generation Cheetah disk-drive family developed by Seagate Technology Inc., Scotts Valley, Calif., provides designers with storage capacities of up to 18.2 Gbytes and access times of just 5.7 ns—ideal for the next generation of high-performance desktop systems and servers. With a spindle speed of 10,025 rpm, the Cheetah 18, as well as the other two lower-capacity models, the 9LP and 4.5LP, all offer a data-transfer rate between 14.5 and 21.3 Mbytes/s off the head, and communicate to host systems over either an Ultra SCSI 2 or Fibre-Channel Arbitrated Loop (FC-AL) interface. The Cheetah 18 comes in a half-height 3.5-in. format, while the 9LP and 4.5LP, which hold 9.1 and 4.5 Gbytes, respectively, come in a low-profile sub-half-height format. The reduced number of platters in the lower-capacity drives also lets the drives access data slightly faster at 5.2 ms. The Ultra SCSI version of the 18-Gbyte drive consumes 15 W maximum, while the 9- and 4.5-Gbyte units consume 12 and 10.5 W, respectively. Fibre Channel versions consume slightly more—17, 14, and 12.5 W, respectively. Samples are available now, with volume production slated for early 1998. Single-unit prices are $1755 for the Cheetah 18 (ST18202), $1090 for the Cheetah 9LP (ST39102), and $655 for the 4.5LP (ST34502). Contact Seagate at (408) 438-6550, or on the web at http://www.seagate.com/vpr.shtml.

Able to lower the power consumed by high-resolution color LCDs, a low-power direct-drive column driver developed by Vivid Semiconductor Inc., Chandler, Ariz., not only trims active power, but also produces over 16 million colors, making true-color depth practical on portable computers. The VS3184 8-bit column driver also supports full-motion video for active-matrix TFT LCDs with XGA and SXGA resolutions. The VS3184 includes the company's patented extended voltage range architecture that allows the circuit to accommodate higher voltages than are normally associated with standard digital CMOS processes. This technology offers a 9.6-V dynamic range and 8-bit resolution that results in 256 distinct voltages/output, thereby enabling the chip to define over 16 million colors on a TFT panel. The chips are designed for use on direct-drive panels that employ pixel inversion—an approach that many manufactures previously considered too costly and power hungry. However, with the VS3184, power consumption drops to just 37 mW per driver and 296 mW per XGA panel. Included on the VS3184 are 384 output drivers and a high-speed data-loading capability that allows video data to shift in at speeds of up to 65 MHz over a dual port that accommodates six data buses. Samples sell for $15 and are available now in standard TAB packages. Call Donna Higgins at (602) 961-3200, or on the web at http://www.vividsemi.com.

A manufacturing kit that contains all that's needed to create low-cost portable PC cameras can now be ordered from Intel Corp., Chandler, Ariz. The 971 PC Camera kit includes a sample set of the PC camera silicon, software, schematics, design documentation, and suggested manufacturing procedures. At the heart of the kit is a new CMOS image sensor, an image processing unit, a microcontroller, and the PC imaging utility software. The kit allows cameras to be built that offer dual-mode operation—able to capture a digital still image when detached from the PC and capture digital video when attached. The sensing device, an affordable alternative to existing image sensors, offers a maximum resolution of 768 by 576 pixels with 24-bit color support. Images are temporarily stored in the DRAM during processing, then transferred to a flash memory card which serves as the electronic film. The utility software includes tools that perform general image-acquisition and storage tasks on the host PC. The tasks include decompressing the images and conversion to the FlashPix file format. Once stored in that format, the images can be enhanced or modified using such software as Storm EasyPhoto, MGI's PhotoSuite, and Microsoft's PictureIt! For details on the kit, go to the Intel website at http://www.intel.com/imaging.

CompactPCI SBC Holds PowerPC CPU

A 166-, 200-, or 240-MHz PowerPC 603e microprocessor is the basis of the SmartEngine/603cPCI, a single-board computer that fits a single-slot 6U Eurocard form factor for the CompactPCI standard. The board supports most popular real-time operating systems, including VxWorks, C-Executive, pSOS, and Nucleus. A PMC expansion connector lets users customize the board for specific applications. Interfaces are included for the PCI bus, an Ethernet LAN, and SCSI peripherals. Up to 128 Mbytes of DRAM can be employed, as well as 256 or 512 kbytes of secondary cache memory. Available now, the SmartEngine/603cPCI SBC sells for $1876 with a 166-MHz processor and 16 Mbytes of DRAM.

Smart Modular Technologies Inc., *4305 Cushing Pkwy., Fremont, CA 94538; (510) 623-1231; Internet: http://www.smartm.com.* **CIRCLE 485**

Integrated Fibre Channel Interface Boasts High Speed

The FC-1930/R is an intelligent Fibre Channel controller for VME64 and RACEway systems. It serves as an interconnect for high-throughput real-time systems, disk arrays, high-performance storage systems, and general-purpose computers. It sustains data rates of 84 Mbytes/s between RACEway and disk arrays, and 88 Mbytes/s for system-to-system transfers. Applications that require this throughput include radar processing, data acquisition, collection, and storage, signal and image processing, telemetry, remote sensing, and simulation.

The FC-1930 is fully ANSI-compliant, supporting FC Class 1, 2, and 3 operation in arbitrated loop, point-to-point, or switched systems. Compatibility with other Fibre Channel equipment is supplied through use of the Hewlett-Packard Tachyon Fibre Channel controller and Gigabit Link Modules. All software required for the FC-1930's on-board CPU is provided. Software libraries for the VxWorks real-time operating system are supported. Available now, the FC-1930 costs $10,000.

Myriad Logic Inc., *1109 Spring St., Silver Spring, MD, 20910; (301) 588-1900.* **CIRCLE 486**

Low-Cost ATM Module Delivers Real-Time Switching

Using the CPMC-ATM module, VME-based systems designers have a low-cost solution for direct connectivity to ATM (asynchronous transfer mode) local- and wide-area networks (LANs/WANs). The module provides high-bandwidth, low-delay packet switching and multiplexing of voice, video, and data for network applications ranging from military command and control to commercial data communications. The CPMC-ATM supplies deterministic network-access times, scalable bandwidth, and high-speed ATM networking capabilities up to 155 Mbits/s.

The single-slot board offers I/O flexibility, allowing designers to select among the common physical interfaces to ATM networks, including 155-Mbit/s STS-3C on single- or multi-mode fiber optics, UTP5 155-Mbit/s STS-3c, and 25-Mbit/s UTP3. The CPMC-ATM is bundled with an ATM software stack that includes LAN emulation, classical IP, RFC1483 IP over ATM, ATM Forum UNI3.1 signaling, and network management utilities. The CPMC-ATM is compliant with the PCI revision 2.0 interface and fits a standard PMC form factor. The module is available immediately for $790.

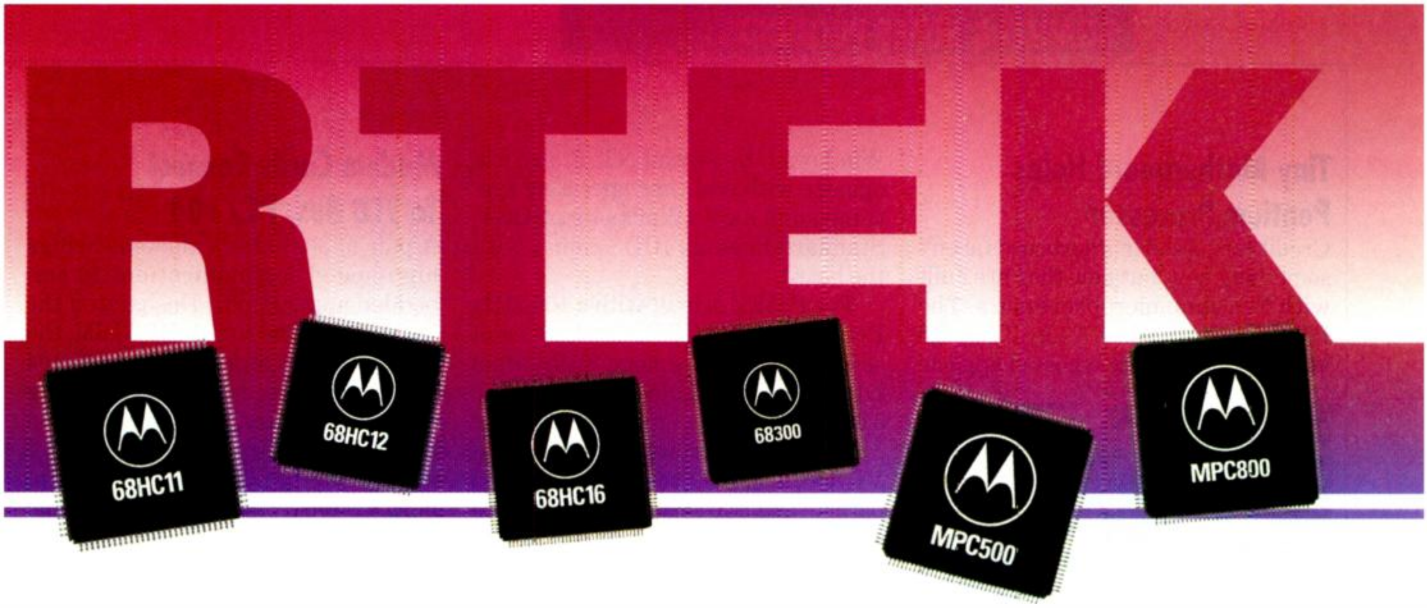
***Cetia Inc.**, 58 Charles Street, Cambridge, MA 02141; (617) 494-0987; http://www.cetia.com.* **CIRCLE 504**

Real-Time Networking System Handles Up To 144 Nodes

Multiple PCI and CompactPCI nodes can be shared through a central hub using the Broadcast Memory system. The real-time networking device allows a common memory to be shared

between 144 nodes. Transfer rates up to 42 Mbytes/s coupled with low latencies suit the system for deterministic data transfers. Due to the hub topology, a node or cable failure only affects that specific node. All other nodes continue to operate independently. Because traditional protocol stacks aren't required, the system reduces the host CPU overhead at each node. This feature comes in handy when the Broadcast Memory is employed in a real-time application. Prices depend on the specific network requirements. For example, a 16-node network with 256 kbytes of memory costs $4400, while an 8-node network with 2 Mbytes sells for $5200.

***SBS Technologies Inc.**, 2265 Camino Vida Roble, Carlsbad, CA 92009; (760) 438-5656; http://www.sbse.com.* **CIRCLE 505**



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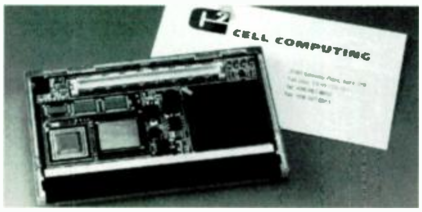
Tiny Motherboard Holds Pentium Processor

Credit card-sized motherboards aren't something new, but now they are built with Pentium microprocessors. The P55EZ measures just 3.4 by 2.1 by 0.8 in. and is suitable for a host of applica-



tions, including portable terminals, notebook or desktop PCs, office equipment, factory or industrial automation, test and measurement equipment, and automotives.

By incorporating the P55EZ into a design, engineers needn't worry about the issues surrounding a high-speed processor, including clocking and thermal issues. the card runs on standard operating systems such as MS-DOS, Windows CE, 95, and NT. It also can operate with real-time operating systems such as VxWorks or pSOS+. Standard Phoenix BIOS comes with the board.

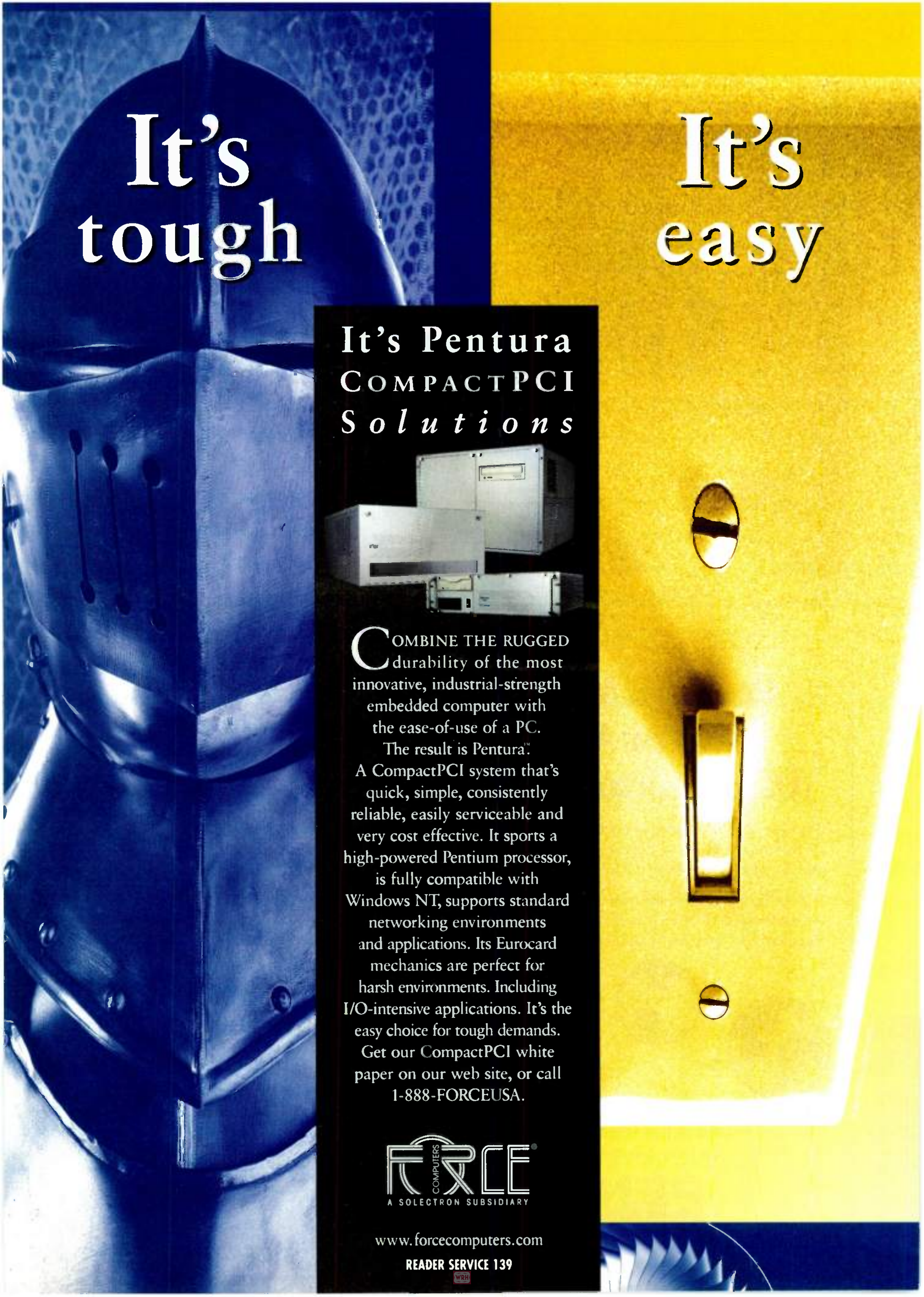
The P55EZ is built with a 166-MHz Pentium MMX CPU, 256 kbytes of secondary cache memory, 8 Mbytes of DRAM (expandable to 72 Mbytes), 512 kbytes of flash memory, a Super VGA controller with 1 Mbyte of VRAM, a disk-drive controller, and a parallel and two serial ports. The card uses a 236-pin EASI controller to bring out signal lines for an ISA bus, hard-disk drive, and other I/O. To reduce design time, the ISA bus can be converted to a PC Card connection. In addition, a small-outline DIMM sockets is available to add 64 Mbytes of DRAM. The maximum power draw is 13.1 W. The P55EZ is priced at $999 each in lots of 1000. A 133-MHz version, called the P54EZ, sells for $799.

***Cell Computing Inc.**, 2099 Gateway Place, #750, San Jose, CA 95110; (408) 967-8800; Internet: http://www.cellcomputing.com.* **CIRCLE 506**

Modem Cards Connect To STD Bus, PC/104

A pair of 33.6-kbit/s modems brings high-speed communications to embedded applications. Designated the PCM-33.6M and the MCM-33.6M, the modems are designed for the PC/104 and STD buses, respectively. Using error-correction and compression techniques, a throughput up to 115.2 kbits/s can be achieved. They support V.34bis, V.34, V.32bis, V.32 and other standard communication protocols. Both boards integrate the basic modem functions and a PC-compatible COM port. The PC/104-based PCM-33.6M measures 3.6 by 3.8 in. It requires a +5-V supply. It sells for $250. The MCM-33.6M contains both an STD Bus interface and an external serial RS-232 interface. It's available in an extended-temperature version.

***WinSystems Inc.**, 715 Stadium Dr., Arlington, TX 76011; (817) 274-7553; http://www.winsystems.com.* **CIRCLE 507**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READER SERVICE 139

Solid-State Storage Card Employs Tiny Form Factor

With a physical form factor of 32 by 24 by 1.4 mm, the MultiMediaCard (MMC) represents one of the smallest removable solid-state storage devices. Jointly developed by SanDisk and Siemens, the MMC is suited for devices that previously contained no removable storage, like mobile phones and pagers. It's initially available with 2- or 4-Mbyte capacities, with 10 Mbytes coming early next year. It employs a 7-pin serial interface that allows for easy integration into a design and also results in an inexpensive connector. The MMC operates at a voltage level ranging from 2.7 to 3.6 V. At 2.7 V, the power consumption is 62.1 mW for reads, 72.9 mW for writes, and 0.11 mW in standby mode. The card's write rate is 200 kbytes/s, while it can read at 2 Mbytes/s. The operating temperature is from 0 to 60°C. In large volumes, the 2-Mbyte MMC card costs $26, and the 4-Mbyte model costs $32. A developer's kit also is available.

SanDisk Corp., *140 Caspian Ct., Sunnyvale, CA 94089; (408) 542-0500; http://www.sandisk.com.* **CIRCLE 508**

Credit Card-Sized Computer Employs Low-Power CPU

The latest member of the Cardio PC/AT credit card-sized computer board is built with Intel's Hummingbird 80486 microprocessor, resulting in lower power and cost, and higher performance. With the Cardio486HB, embedded-systems designers can take advantage of features previously available to just the portable-design community for which the CPU was originally intended. Power consumption is 1.2 W at a 16-MHz clock rate. Other features include a video controller that supports color and monochrome on CRTs and LCDs, with a resolution up to 800 by 600 pixels, a keyboard and mouse controller, an IDE interface, and IrDA 1.0 compliance. Power supply requirements are 3.3, 5.0, and 12.0 V, depending on system requirements. Prices start at $300 each in lots of 1000. Evaluation boards are available.

S-MOS Systems Inc., *150 River Oaks Pkwy., San Jose, CA 95134; (408) 922-0200; http://www.smos.com.* **CIRCLE 509**

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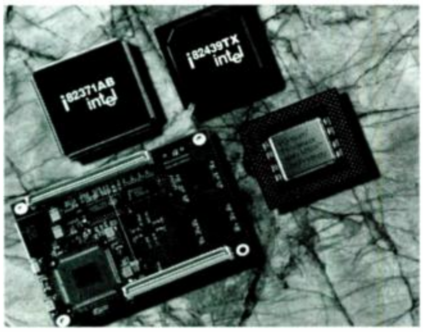
READER SERVICE 116

Embedded Designs Get Boost From Pentium Module

Designers of embedded PCs can boost performance using the Embedded Processor Module that contains a 166-MHz Pentium with MMX technology, a secondary cache memory, and the 82430HX PCIset chip set. In addition,



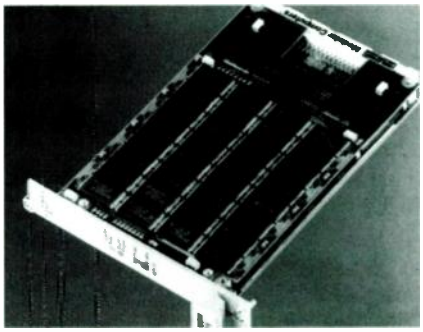
the 200-MHz Pentium processor will be available in a version that's easy for designers to embed into their systems—a 296-pin plastic pin-grid array. Lastly, the company will offer its 82430TX PCIset available to embedded-system designers. This chip set supports Ultra DMA and SDRAM, a feature that's needed for telecommunications applications.

Using the Pentium module, designers can offer an easy upgrade path to faster processors as they become available. The module interfaces with the PCI bus and DRAM and includes the same base I/O architecture that was employed with previous-generation modules. Reference designs are available. The 200-MHz Pentium processor sells for $252 each in lots of 1000. The 166-MHz Pentium module, available in the second quarter of next year, costs $400. The 82430TX PCI set is priced at $28.25.

***Intel Corp.**, 2200 Mission College Blvd., Santa Clara, CA 95052; Internet: http://www.intel.com/design/intarch.*
CIRCLE 510

3U VME Board Holds 192 Mbytes Of Flash Memory

Up to 192 Mbytes of flash memory can be housed on the VMEM-F1 3U VME-bus memory board. The baseboard holds the first 64 Mbytes, with the remaining 128 Mbytes fitting on a piggyback module. Write protection of the memory can be set in banks of 4 MBytes. Writing is possible in 128-kbyte blocks. The board is suited for applications that require fast access to



large databases, such as mobile data loggers and test systems that operate in harsh environments where traditional hard-disk drives wouldn't be used. Available now, prices for the VMEM-F1 flash-memory board start at $2660.

***PEP Modular Computers Inc.**, 750 Holiday Dr., Bldg. 9, Pittsburgh, PA 15220; (412) 921-3322.* **CIRCLE 511**

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Pick The Perfect Chassis To Ensure System Longevity

Improve System Integrity And Reliability By Matching The Right Type Of Chassis For The Particular Application.

MARK KAIDY, Solar Microsystems Inc., 201 Benton Ave., Linthicum MD 21090; (410) 859 5151; fax (410) 850-0493, e-mail: mkaidy@solarmicro.com.

So, you've designed the best circuit boards in the world and want to use them for your next ruggedized system in the jungles of Borneo. Have you given much thought to the kind of chassis they will go in? Probably not. But with electronics finding their way into environments ranging from the desktop to the desert, you may no longer be able to afford to leave the choice of chassis to the last minute if you intend to maintain your competitive edge. Choosing the right chassis must now become an integral part of the design process.

Because of the various environments in which electronic systems are to be found, shock, vibration, temperature control, water, dust, or even space consolidation and packaging, can greatly influence chassis choice. To arrive at the optimum design, a number of factors must be carefully balanced, including cost, shock, size, weight, and flexibility—with the application determining which gets priority.

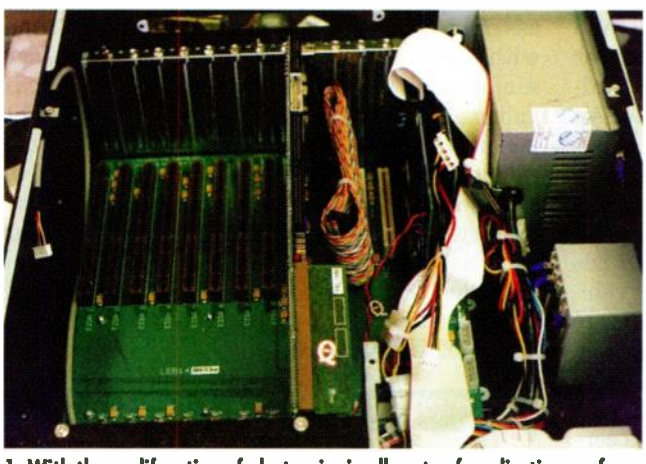
To design, build, and/or specify a rugged system chassis, note the following attributes. They are broken down here in no particular order:

Construction—Chassis construction depends on four things: weight, material, size, and how the chassis is fastened together. Weight and material and size are closely related to one another—with the material determining the weight. Of course, size also influences weight. The materials most often used for chassis construction are aluminum, steel, and plastic.

Aluminum's advantages are its light weight and the fact that it takes well to machining and welding. You can build a chassis that is just as light and strong in steel but, in this case, you have to be more careful with the steel thickness and lightening holes in the steel. Aluminum also can be anodized less expensively than steel can be plated.

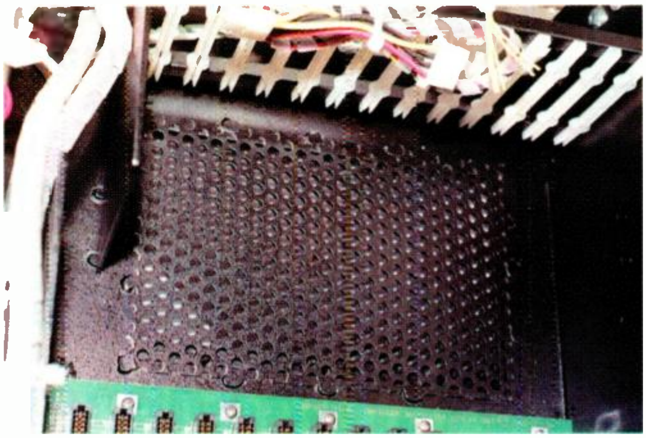
However, one of aluminum's big disadvantages is that it is not very forgiving. For example, suppose you need to put a threaded hole somewhere in the chassis and don't have room for an insert or other fastener. With a steel chassis, you can thread the hole and use it many times before it wears out. (This is a good feature if you have to install an unplanned bracket). On the other hand, in an aluminum chassis, a machine-threaded hole has to be deep. Also, if you cross-thread the hole by accident, the hole is destroyed. The same applies to sheet aluminum. In addition, aluminum yields more abruptly than steel.

Generally, you should use plastic for cosmetics, as in the front panel or bezel of a 19-in. rack-mount chassis. You also can use plastic or rubber as a protective skin, as in the case of a portable rugged computer over a metal internal structure. In addition, plastic has the advantage of being light, and it can be coated with electrically conducting paint. As a result, additional metal shielding (for radiated RF energy) is not required.



1. With the proliferation of electronics in all sorts of applications—from the office to the jungle—designers must pay careful attention to the degree of ruggedness they incorporate into their system if reliability is to be maintained without breaking their budget. With respect to the power supply, four grades are available—junk grade, commercial grade, industrial grade, and military grade. Each have their place.

Injection-molded plastic cases can be very cost-effective if your quantities reach into the thousands. However, if you are in doubt as to which material you should use for your next chassis design, go with either aluminum or steel, or both. Because of initial tooling costs, plastic can be used later on when your design has solidified and production quantities are sufficient.



2. The airflow within a chassis, whether forced air or convection, should generally be from side to side, bottom to top, or front to back. Care should be taken to ensure that the air flows between system boards. Airflow to right angles, such as a front intake and a side exhaust, is not a good idea. Make sure that components don't inhibit air flow.

Chassis Size

Chassis size depends on what goes into the chassis and where it will be mounted. A really big board, such as those used in a 9U VMEbus system, will require a really big chassis with its ensuing weight, internal cooling, and external mounting considerations.

If you are mounting in a 19- or 24-in.-wide rack, the width dimension is fixed. Since rack space is always at a premium, you should keep height to a minimum. Height for EIA-standard racks is parceled in increments of 1.75 in., or 1-U (one rack-unit) spacing. Depth can vary, but only to a distance that is practical. A depth of 26 in. is about the maximum distance prescribed for most rack-mounted applications.

Try to keep size to a minimum in all other cases, such as in instances where your customer's application will be installed in a helicopter. Space in a helicopter is super-precious; your chassis design should reflect that as well. And don't forget to ask your customer what flanges or other mounting hardware they need to secure the chassis to the helicopter.

In fact, installations in many vehicles make size a primary concern. For cars, small trucks, and even tractor trailers, chances are the customer has a lot of other equipment in their vehicle, and your chassis is just one more piece that has to fit. In submarines, some computers and monitors have to be sized so that they will fit through the hatch. And size also may be a concern for a shop-floor application. The shop floor may be a 300,000-square-foot warehouse and your system may need to be carted from one end of that warehouse to another. A three-foot-high cart is much easier to push than a nine-foot cart. And it's safer, too.

Another construction feature is how the chassis is fastened together. An all-welded chassis is the sturdiest. However, it also can present production difficulties, and is generally more expensive to build. Production difficulties include trying to put a weld where you need it, then discovering that because the chassis has a bend or fold, it then becomes impossible to place the weld. If you are in the process of designing an all-welded chassis, show your drawings to an experienced welder before you have your sheet-metal shop bend metal. You can save yourself a few headaches.

Riveted chassis are quick and easy to assemble; they do not, however, disassemble as easily. Chassis fastened with screws and nuts are easy to assemble and disassemble, thereby providing easy access to the internal components. But screws get lost and are prone to vibrate loose if you don't take additional measures. You can curb screw loss due to vibration by simply using a lock washer, applying a chemical called Lock-Tite, or by using fasteners that have holes in them so that they can be wired in place.

Power Supply

Basically, there are four types of supplies you can use (*Fig. 1*). They are:

Junk grade—Junk-grade supplies are used in standard budget desktop computers. Reliability is a toss-up. These supplies don't have any certifications (if they do, they are questionable). One big clue for identifying a junk-grade PS/2-type supply is the absence of a metal gasket between the power inlet (three-prong) and the supply case. If you're using a desktop application and price is an issue, these supplies are fine. For rugged applications forget about using them.

Commercial grade—These supplies are FCC-certified (usually, specifications are printed on the side of the supply). Commercial-grade supplies do not cost that much more than junk grade ($65 versus $20), but they are generally harder to find. Get paperwork if you are in doubt. Most certifications can be verified by an agency or the testing lab.

Industrial grade—These supplies have all the bells and whistles, including auto ac-input sensing (90 to 264 V ac), UL, CSA, CE, IEC, and FCC certifications, power factor correction, low ripple and noise, brown-out protection, N+1 redundancy, and so on. Industrial supplies cost about five to 10 times that of commercial grade. They are harder to integrate because there is no standard size. However, this absence of size standardization also makes them more versatile. Finally, there are many different power outputs and ratings available.

Military grade—These supplies adhere to military specifications for performance and are rarely worth the extra cost (1.5 to 2 times the industrial grade costs). Commercial off-the-shelf

TYPICAL COMPONENT CURRENT REQUIREMENTS

Component	Voltage (dc) 12	-12	5	-5
Motherboard	2 A	0.2 A	3 A	0.2 A
Hard-disk 1	1 A (3 A startup)	None	0.5 A	None
Fans (three, at 1 A each)	3 A	None	None	None
Hard-disk 2	0.9 A (2 A startup)	None	0.4 A	None

(COTS) is in vogue.

When choosing an appropriate supply, you should ask the customer (and yourself) the following:

What are the input voltages like at the final installation site? If the power is crystal clean and 110 V ac, a commercial-grade supply will probably do just fine. If the power is in a P3 military aircraft where 400 Hz is supplied, an industrial-grade supply is probably a better choice. (The same holds true in the jungles of Borneo.)

What do the components in the chassis require for voltage and current? Compile a list and do not forget to note the startup requirements of such components as disk drives and fans (*see the table*).

Make sure your supply can handle the power requirements of the components with at least a 25% margin. Also, make sure that the system board you are using does not require an unusual voltage level (such as –2.7 V dc, strictly regulated).

Note: If you are locked into using a certain supply and find that it does not provide enough current, you can add a second supply that delivers the same voltage. This second supply can be switched on using 5 V dc and a relay from the main supply. In that way, you still only need one power switch; the second supply is transparent to the customer (*Fig. 1, again*)

Heat Dissipation

Make sure that there is adequate airflow for dissipation of heat from the components in your chassis. Airflow should be between system boards (*Fig. 2*). In your chassis, decide whether airflow should be side to side, bottom to top, or front to back. Having airflow to right angles within the chassis (such as a front intake and a side exhaust) is generally not considered good practice.

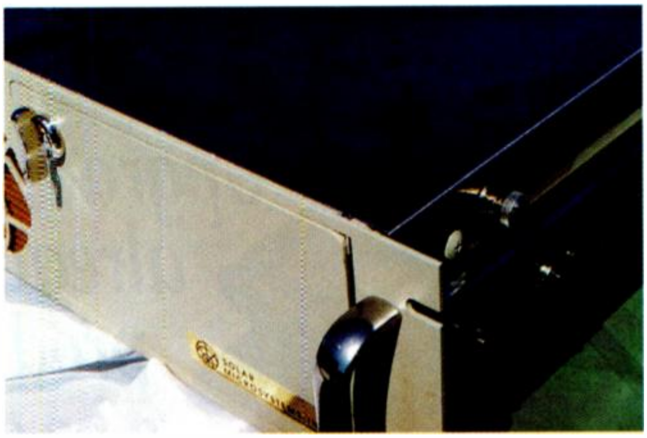
Make sure that the placement of internal components and cabling does not impede airflow. Push-pull airflow designs are prevalent and practical. Here, the intake flow is accomplished with one or more fans and the exhaust flow is accomplished with a different fan or fans. Push-pull flow is positive pressure because air flows through the chassis and does not just swirl around inside the chassis. Air filters are a great idea and should be included in the design. Easy access and service are key features.

Fans are chosen by the following criteria: physical size, displacement in cubic feet per minute (CFM), and power requirements (ac or dc). For about $20, you can purchase a 100-CFM, 12-V-dc/1-A fan measuring 4.75 by 4.75 by 1.5 in.

Determine the input air temperature and the operating temperatures of the components in your chassis. This will help you choose how many and how big the fans need to be. Remember, as you add fans, the chassis will run cooler, but you'll need a larger power supply, and more space to put the fans. Finally, in certain critical applications, it may be wise to include a fan alarm in case it malfunctions. Some fan manufacturers even sell fan-alarm ICs with their fans.

Versatility

What some call the "versatility attribute" of chassis design incorporates the real selling points of your design. Versatility not only means how clever your chassis design is, but also how flexible you are as a designer. For example, you must be prepared to respond positively when the customer says, "Oh yes, I forgot. Could you install some cutouts and another disk drive and could you...?"



3. A key aspect of a chassis design, the mean time to repair can be significantly reduced by using thumbscrews instead of screws. This technique also circumvents the tendency of screws to get lost.

Many system boards require different mounting methods. All standard PC motherboards—whether 286s or Pentiums—have been mounted in pretty much the same way for almost 20 years: on standoffs. Passive backplanes are also mounted on standoffs, but the hole patterns differ for the number of slots. For example, two-slot backplanes and 20-slot backplanes have different mounting holes. Also, a two-slot backplane from one manufacturer often has different mounting hole patterns than another two-slot backplane from a different manufacturer.

Other manufacturers' boards frequently require specific mounting capabilities. For example, some Sun motherboards are designed to use slide mounts.

The internal space needs for various system boards also are different. In PC motherboards, interface cards are mounted at right angles to the system board. Other manufacturers mount the interface cards parallel to the system board (which gives the whole system a lower profile). Be aware of these board-mounting issues. Examples of parallel board mounting to the system board include embedded and PC-104 type cards, Industry Packs, and many Sun motherboards.

Access to disk drives also is important. Ask how many 5.25- and 3.5-drive spaces are needed and how many need to be accessible from the front, removable, and so on. Can the drives be mounted vertically? (Don't forget shock mounting—that will be covered in more detail shortly.)

Choose components that have a high MTBF. Somewhere along the way you will get a call from your customer's reliability and Q&A department, asking for the MTBF numbers on all the components used in the chassis. (**Author's note:** I am no expert on failure analysis but if a product says on the box it has an MTBF of 100,000 hours—11.4 years—dutifully, I quote that to the customer. I still don't understand how they get this number when I know the product has only been out for only two years.)

Your chassis design also should

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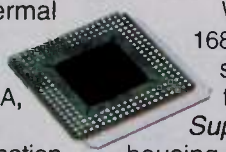

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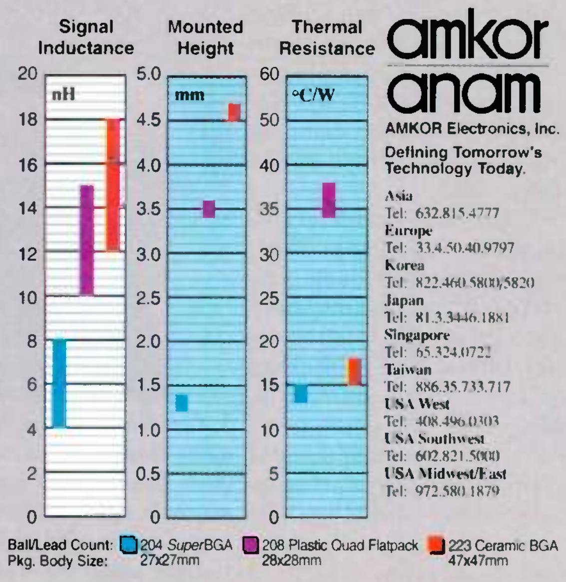

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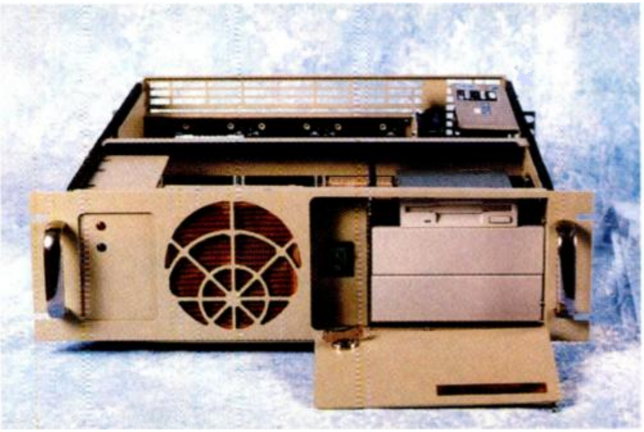
keep MTTR (Mean Time To Repair) to a minimum. Inevitably, repairs will be required; keep that in mind as the design progresses. Quick panel access with thumbscrews is practical and popular. Technicians that have to upgrade or repair your chassis will not be happy if they have to go through 15 screws to remove the top just to replace a video card (then they'll probably drop one of the screws in the chassis). Use thumbscrews: 30 seconds with a nonbattery-operated thumb, versus the typical three minutes or more with a power screwdriver (*Fig. 3*). Finally, use standard English threads such as 4-40, 6-32, or 8-32. Stay away from metric hardware; it's still not readily available.



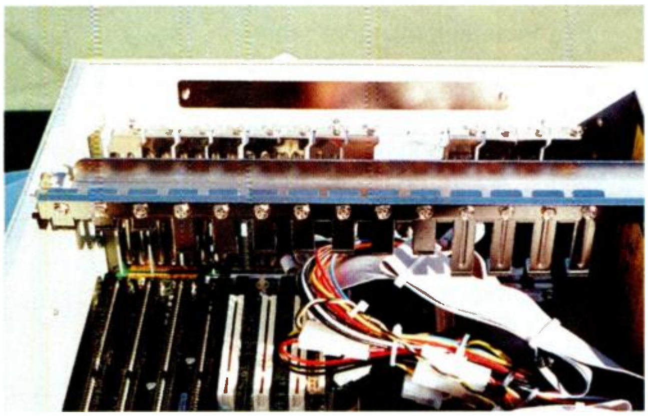
4. While doors are aesthetically pleasing, they should have a function, such as protecting drives from removal or the power switch from being turned off by a casual passer-by.

Doors are nice, but they're only good if they perform a function (such as protecting drives from removal or the power switch from being turned off by a casual passerby). If you are still going to use doors, make sure that a locking or latching option is available. If you have a lock, keys can get lost. If you have a latch, there is no key to lose (*Fig. 4*).

Shock and Vibration

Disk drives are the most obvious candidates for shock and vibration isolation. However, you also can isolate other components, such as the system board, power supply, and peripherals. You can isolate each component or the entire chassis or rack. Simple dynamics calculations will determine how much dampening is needed for a given shock value.

Vibration is trickier because harmonics can yield unexpected results during vibration testing that may have not been predicted in the design phase. Many different dampeners are available, such as rubber grommets, rubber cushions, and metal springs. The manufacturers of these dampeners can provide you with data on their spring-constant values (as well as cost). Also make sure that the components have little chance of moving within a subassembly, such as providing for cards to be securely fastened (*Fig. 5*).



5. Vibration is tricky because harmonics can yield unexpected results during vibration testing that may have not been predicted in the design phase. Many different dampeners are available, including: rubber grommets, rubber cushions, or metal springs. Make sure that the components have little chance of moving within a subassembly by fastening boards tightly to the chassis.

Certification And Testing

These are some common certifications, but you will probably see many more:

CE–Self certification for sale in the European common market. Governs safety and radiated emissions.

UL–Safety Underwriters Laboratory. UL has been around for years and has a number of certifications that may apply.

FCC–Federal Communication Commission. Governs internal and external interference emissions.

NEBS–Bellcore's standard for the telco industry. NEBS certification is expensive, exhaustive, and is based on a comprehensive specification. Achieving NEBS compliance requires careful attention to detail from early in the design process.

Mil 901D–Severe shock and vibration specification; used by the Navy.

Mil 810E–Shock and vibration method for testing specification that is less severe than 901.

Keep in mind that testing and certification has become an industry in itself. You may not be required to have any testing done if you are building a small number of chassis for a very specific application. Use common sense when it comes to ordering any test. The United States is a country sometimes stuck on liability and lawsuit, rather than good engineering. Your customer may include your chassis as part of a larger system that will be in turn tested and certified.

You also may be required to build to meet certain specifications but not actually test to them. If you do have to have a chassis tested and certified, it could cost you $4000 to $7000 for FCC and UL, and another $5000 to $8000 for CE. These are the three most common and could take as long as 10 weeks (depending how backed up the testing lab is). Choose a lab that is close to you and is accredited.

EMI/RFI

Be aware that EMI/RFI suppression may be required in your design. Make sure that grounding is to one common point, that metal-to-metal contact is made when finished parts overlap, that emissions are suppressed between components so that the internal components do not interfere with each other, and that doors or other panels are gasketed with special EMI/RFI gasket material. Anywhere there is a physical opening (this includes air intakes and exhaust) is a place where emissions can occur. Emis-

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sions can also be transmitted through a cable. Consult with the manufacturers of suppression components during the chassis design stage.

Finish And Coating

Painting is inexpensive and fast, and it also protects and electrically insulates the metal. Hence, any surfaces that need to make electrical contact must be masked prior to painting. Masking can be expensive.

Electro-coatings also are an option. The three most common forms of electro-coating are iroditing, anodizing, and plating. Iroditing and anodizing are used to finish aluminum. Iroditing is much less expensive than anodizing and comes in gold and clear, is electrically transmissive, and looks attractive. Anodizing can be done in a variety of colors such as blue, black, or red. Plating can be done with steel or aluminum and is generally more expensive than iroditing. Plating also can look attractive, comes in many varieties such as zinc, chrome, nickel, and is electrically transmissive.

Your customer may want to put their logo on your chassis. Silkscreening or labels are two options. Silkscreening must be done carefully, because you are working with ink and it can smear easily. Stick-on labels are quicker and easier to apply but are generally not used for lettering as in "Power-On/Off."

Cost

When deciding on cost, you'll want to address the following items:

Labor to assemble—If the chassis design is either poor or complicated (or both), assembly time will be increased significantly. That may be tolerable for a one- to five-piece run, but when the big quantities hit, you'll wonder where your profit is going. Remember, the longer it takes you to get the box out the door, the longer you'll have to wait to get paid.

Cost of Materials—Steel does not really cost any more or less than aluminum, but your electronic component choice should always be shopped prudently. Components, of course, include: power supplies, disk drives, those best circuit boards you designed, and so on.

Cost to Design—This is often a big

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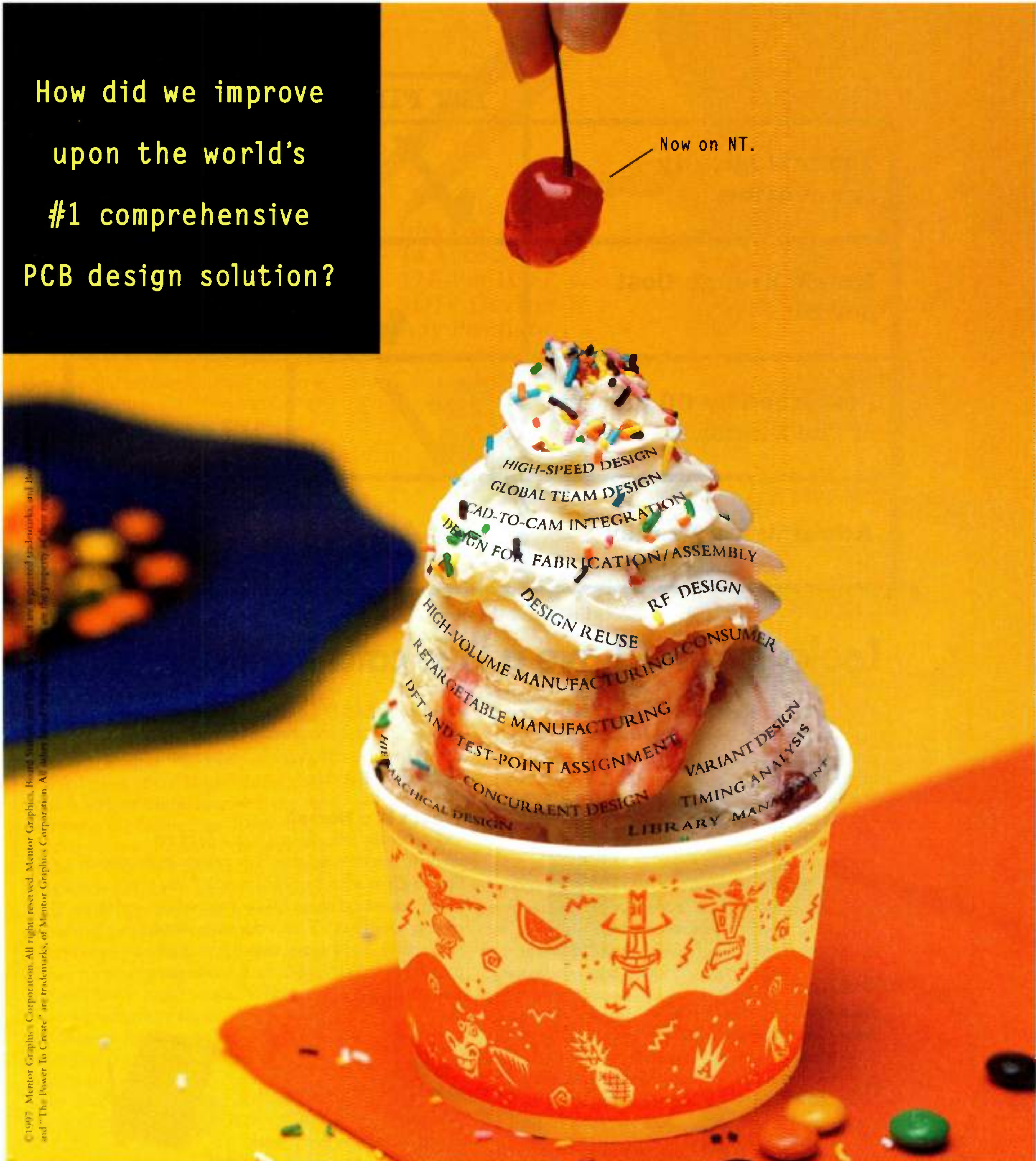

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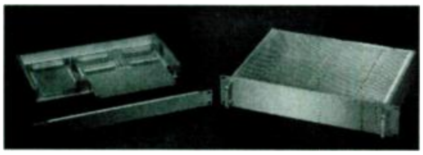
PRODUCT UPDATE: OSCILLATORS AND RESONATORS

Manufacturer	Device	Description	Price and delivery	CIRCLE
AVX Corp. Myrtle Beach, SC Nick Bogovich (803) 448-9411 Fax (803) 448-1943	PBRC Series	Part of the company's line of PBRC resonators, this device extends the line's frequency range up to 40 MHz. The ceramic, surface-mount, quartz-crystal device has a profile of 1.6 mm for applications where space is at a premium.	$0.20 to $0.50 each	490
Bliley Electric Company Erie, PA David Bliley (814) 838-3571 Fax (814) 833-2712 E-mail: info@bliley.com	T79C	This temperature-compensated, voltage-controlled oscillator comes in a single DIP package and operates over the frequency range of 1 to 4 MHz. Features include a temperature stability of ±1.5 ppm max over the range of -40° to 85°C, an HCMOS- or TTL-compatible output, and an aging figure of 2 ppm for the first year and 1 ppm thereafter.	30-MHz version, $65 each per 100; eight to 12 weeks ARO	491
Champion Technologies Inc. Franklin Park, IL Sales Dept. (847) 451-1000 Fax (847) 451-7585 http://www.champtech.com	49UB Series	These surface-mount crystals have a frequency range of 3.5 to 60.0 MHz with a frequency stability of ±100 ppm and an operating temperature range of -20° to 70°C. Extended-range versions also are available. The devices are compatible with pick-and-place and IR reflow processes.	$0.57 to $1.05 each per 1000	492
Epson America Inc. Torrance, CA Ken Nagai (310) 782-5314 Fax (310) 782-5320 E-mail: k_nagai@ea.epson.com	SG-8002 Series	With their low current requirement of 45 mA (max), these oscillators target portable electronic applications. Available in surface-mount and through-hole versions, the devices have an output frequency of 1.0 to 125 MHz at 5 V (up to 90 MHz at 3.3 V), and a frequency stability of ±100 ppm. The operating temperature range is -20° to 70°C.	From $1.35 to $1.70 each per 10,000	493
Fox Electronics Fort Meyers, FL Customer Service (888) GET-2-FOX Fax (941) 693-1554 E-mail: sales@foxonline.com http://www.foxonline.com	C-4 VCXO-C Series	These pin-through VCXOs have a profile of 0.197 in., an HCMOS/TTL output, and an output symmetry of 40% to 60% at 2.5 V. The devices have a frequency range of 1.000 to 30.000 MHz and a stability of ±1.0 ppm. The operating temperature range is -30° to 85°C; input current requirements range from 15 to 20 mA.	$5.10 each per 1000; stock to eight weeks ARO	494
	F3345/F3355	Targeting portable applications, these oscillators measure 0.295 by 0.197 in. and have a frequency range of 1.800 to 80.000 MHz and 1.800 to 50.000 MHz, respectively. Both have a frequency stability of ±100 ppm. Hermetically sealed in ceramic packages, the devices run off 4.5 to 5.5 V and require between 20 and 73 mA. Shock resistance is up to 3000 G, and the operating temperature range is -10° to 70°C.	10-MHz version, $2.26 each per 6000; stock to 11 weeks	495
MF Electronics Corp. New Rochelle, NY Martin Finkelstein (800) 331-1236 Fax (914) 576-6204 E-mail: sales@mfelec.com http://www.mfelectronics.com	M2900	These oscillators develop timing waveforms with frequencies up to 410 MHz, rise/fall times of 220 ps, and symmetry of 48/52. The output stability over the temperature range of 0° to 70°C can be guaranteed to ±20 ppm. Other features include a jitter of less than 100 ps peak to peak and dual complementary outputs.	$34.95 each per 100	496
	T3258	Surface-mount compatible, this miniature device measures 5 by 7 by 1.9 mm and provides time and reference frequencies over the range of 1 to 100 MHz over the temperature range of -40° to 85°C. The stability is ±100 ppm. Features also include tristate functionality, 45/55 output symmetry, and double-sided pc-board-construction compatibility.	$22.50 each per 1000	497
	W2901 and M2901	Operating in the 15- to 175-MHz range, these SONET-compatible VCXOs have rise/fall times of 225 ps, dual complementary outputs, and 48/52 waveform symmetry. Available capture spans are ±50 ppm, ±100 ppm, and ±150 ppm. The maximum variation of frequency with voltage is less than 2:1.	$55 each per 1000; stock to six weeks	498
Maxim Integrated Products Sunnyvale, CA Customer Service (408) 737-6087	MAX2620	When properly mated with an external varactor-tuned tank circuit, this oscillator exhibits a typical phase noise of only -110 dBc/Hz at 25-kHz offset from a 900-MHz carrier. The device outputs over the frequency range of 10 to 1050 MHz, runs off 2.7 to 5.25 V, and can reduce its current consumption from 9 mA (operating) to 0.1 µA (shutdown).	$1.98 each per 1000	499
Micro Crystal Arlington Heights, IL William Kaczmarski (847) 818-9825 Fax (847) 818-9915	CX1F and CC1F	Available with glass or ceramic lids, respectively, these crystals come in a frequency range of 30 to 100 MHz. They measure 8.1 by 3.8 by 1.5 mm (CX1F) and 8.1 by 3.8 by 1.8 mm (CC1F). Either can be configured to operate over the temperature range of either -40° to 85°C or -55° to 125°C.	50-MHz CX1F version, $3.30 each per 10,000; stock to eight weeks	500
Pletronics Inc. Lynnwood, WA Michael Monson (425) 776-2760 Fax (425) 776-2760 E-mail: ple-sales@pletronics.com	SM55/SM45/ SM40	Essentially a second source for Epson's MA406/506 and Fox's FPX series, these devices come in heights of 55, 45, and 40 mm, respectively. The devices output over the range of 3.5000 to 72.0000 MHz. The ±50-ppm calibration is standard at 25°C, but can be as tight as ±10 ppm. The operating temperature range is -40° to 85°C.	7.1 to 16 MHz, $0.52 each per 10,000; six to eight weeks	501
Raltron Electronics Corp. Miami, FL Sandy Cohen (305) 593-6033 Fax (305) 594-3973	Model RSR-433	This single-port resonator provides fundamental-mode frequency generation for continuous-wave transmitters operating at 433.92 MHz. The device can withstand 25 G of shock, is accurate to ±75 kHz, and ages at the rate of less than 10 ppm per year.	$1.25 each per 10,000; 10 weeks ARO	502
SaRonix Palo Alto, CA Sales Dept. (415) 856-6900 Fax (415) 856-4732 E-mail: saronix@connectinc.com	S1318 Series	Able to operate off 3.3 V dc, these oscillators output in the range of 32 to 120 MHz with a frequency stability of ±50 ppm and a pull range of ±25 or ±50 ppm. The operating temperature range is 0° to 70°C or -40° to 85°C. The devices come in standard six-pin J-leaded packages and are HCMOS and TTL compatible.	$7 to $18 each per 10,000; stock to 12 weeks	503

Low-Cost, 19-in. Rack Has Optional Shielding

The Multipac 19-in. aluminum chassis accepts horizontal boards and can be supplied with an optional EMC shield-

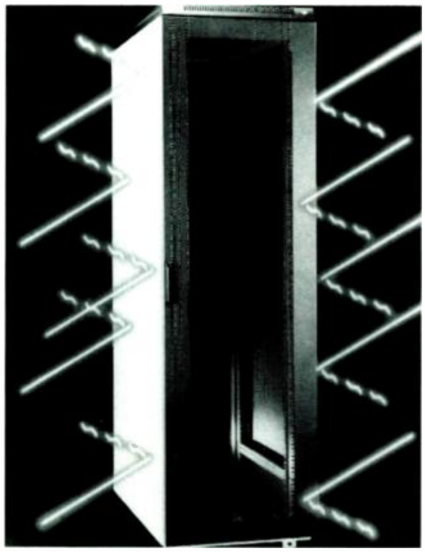


ing kit to enhance its shielding capabilities. The chassis can be supported on slide rails or on telescopic slides and comes in 1U and 2U heights with depths from 220 to 340 mm. Pricing begins at $43 for a 1U by 220-mm basic version.

Schroff Inc., 170 Commerce Dr., Warwick, RI 02886; Sales Dept., (800) 451-8755; fax (401) 738-7988. **CIRCLE 555**

Racking System Combines Style With Ruggedness

The VERAK heavy-duty racking system is a rugged cabinet that targets



industrial, office, or laboratory environments. Two screening levels are available—an IP55 rating is suitable for industrial networking applications, while the RFI-screened version is ideal for electronics and communications applications. Heights range from 27U to 42U with plan sizes of 600 by 600 mm, 600 by 800 mm, and 800 by 800 mm. Features include cabinet linking and the ability to handle up to 750-kg loads. Pricing is from $2000 to $3500, depending on configuration. Delivery is from 6 to 10 weeks ARO.

VERO Electronics Inc., 5 Sterling Dr., Wallingford, CT 06492; Chris Lockwood, (800) 642-VERO; fax (203) 949-1101; e-mail: vero@vero-usa.com; Internet: http://www.vero-usa.com. **CIRCLE 556**

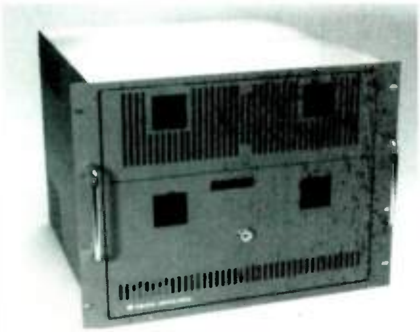
Electronic Enclosures Are Wall-Mountable

The WM Series of wall-mountable electronic enclosures come in a range of five standard sizes, ranging from 2 by 3 by 0.80 in. to 8 by 10 by 1.40 in. Custom options include exterior styling, flame-retardant materials, EMI/RFI shielding, and and modifications for LCDs and keypads. Pricing is from $2.50.

PacTec Div. of LaFrance Corp., 8425 Executive Ave., Philadelphia, PA 19153; Sales Dept., (800) 220-9800; fax (215) 365-4420. **CIRCLE 557**

Chassis Gives Flexibility To Large-Scale Systems

Designed for industrial and telecommunications applications, the 7700 series rack-mount chassis offers flexibility to systems requiring a large number of drives and board expansion slots. Six passive backplane options are available, as are both internal and external ac and dc power supplies. Features include up to 20 slots, up to eight half-height disk drives with secured access, and a hot-swappable 110/220-V-ac or 48-V-dc power supply. Power can be extended to 500 W.



Other features include split backplanes, PICMG and CE compliance, and UL approval. Pricing is from $2649 and delivery is from stock to two weeks ARO.

Industrial Computer Source*, 6260 Sequence Dr., San Diego, CA 92121-4371;Sales Dept., (800) 523-2320; fax (619) 677-0615; e-mail: sales@indcompsrc.com; Internet: http://www.indcompsrc.com.*

CIRCLE 558

Rackmount Expansion Chassis Offers Diversity

An addition to the FULLspectrum line of rugged enclosures, the FS-9602 is a rackmount peripheral expansion chassis designed to meet diverse industrial and military applications. The enclosure handles up to seven half-high SCSI peripherals, comes standard with a 275-W PFC supply, and meets MIL-STD-810E shock and vibration specifications. MIL-STD-461C specifications for EMI/RFI are optional. Pricing is from $5250 each.

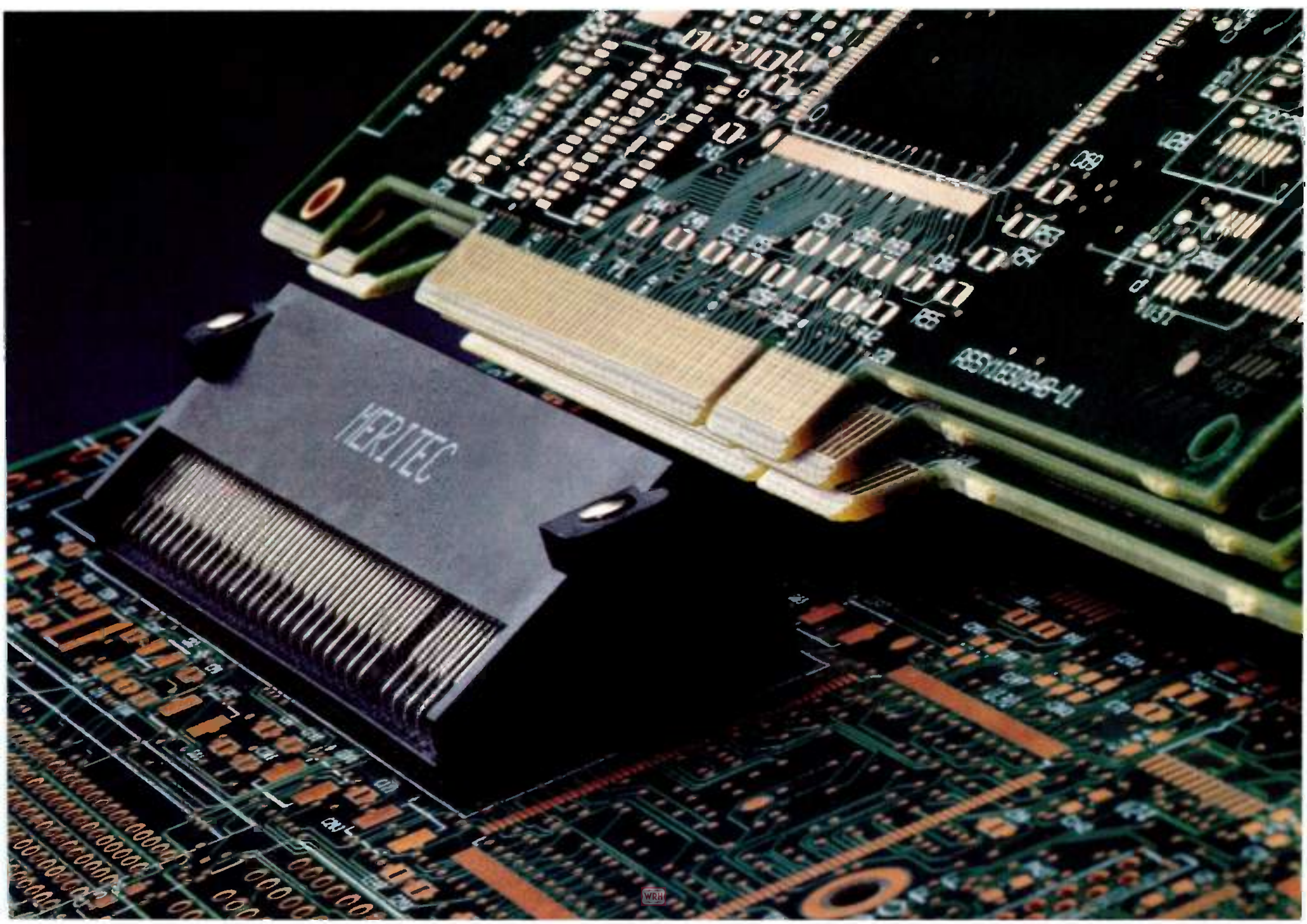
AP Labs*, 5871 Oberlin Dr., San Diego, CA 92121; Steve Gills, (619) 546-8626; fax (619) 546-0278; e-mail: steve@sd.aplabs.com; Internet: http://www.sd.aplabs.com.* CIRCLE 559

Embedded, Six-Slot Chassis Comes In ISA/PCI Version

A twist to MCSI's line of embedded, six-slot chassis, the 9060 chassis is an ISA/PCI version that measures 10.25 by 6.5 by 17. The chassis supports up to two ISA, three PCI, and one CPU full-length PC/AT cards, and includes a card hold-down bracket to ensure that the cards remain seated in high-vibration applications. Features include 16-gauge reinforced steel construction with internal fans, a 3.5-in. drive bay, and shock mounting. A 250-W power supply with switch-selectable 115/230-V-ac operation is optional. Pricing with supply is $525 each and delivery is from stock.

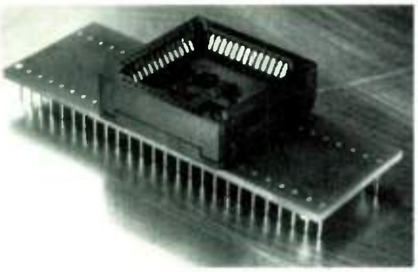
MCSI*, 2598 Fortune Way, Vista, CA 92083; Sales Dept., (800) 347-6274; fax (760) 598-2450; e-mail: mcsi@mcsi1.com; Internet; http://www.mcsi1.com.*

CIRCLE 560



Adapter Converts A 68HC11 PLCC To A Through-Hole DIP

The PC-PLCC/DIP-68HC11-01 allows a low-profile conversion of a Motorola 68HC11 PLCC device or emulator pod to a through-hole DIP land pattern or



socket. The assembly comprises a single-piece FR4 with a PLCC production socket on the top and through-hole pins on the bottom. Signal integrity is maintained using short trace lengths and gold-plated pins. Pricing is $180 each.

Ironwood Electronics, P.O. Box 21151, St. Paul, MN 55121; Sales Dept., (612) 452-8100; fax (612) 452-8400. **CIRCLE 561**

Lightweight 3/4 ATR Chassis Targets Avionics Applications

The DMV-965 is a 3/4 ATR, lightweight chassis for avionics applications. The chassis handles up to eight VMEbus boards on 0.8-in. centers, with sufficient space for an integrated 28-V-dc (optional 270 V dc) or 115-V-ac

power supply. Both supplies meet MIL-STD-704D specifications. Power-supply filtering and EMI/RFI seals on all mating surfaces provide EMI protection to RTCA/DO-160C/D and MIL-STD-461C. A unique flexi-rigid connector system allows users to map up to 350 external I/O connections on the front panel by adding backplane wire-wrap links to designated VMEbus J2 connectors. Cooling is provided by passing air through the hollow sidewalls. Pricing is $25,000 each and delivery is 16 weeks ARO.

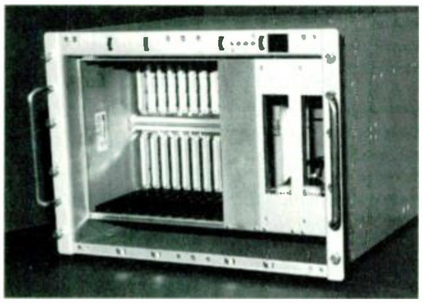
DY 4 Systems Inc., 333 Palladium Dr., M/S 212, Kanata, Ontario, Canada K2V 1A6; Duncan Young (613) 599-9199, ext. 298; fax (613) 599-7777; e-mail: sales@dy4.com; Internet: http://www.dy4.com. **CIRCLE 562**

19-in. VMEbus Rack Allows For Easy Access

The 8-18 Series of 19-in.-wide VMEbus enclosures are designed for I/O flexibility and easy access. The 8U enclosure measures 18 in. deep and comes with the company's monolithic J1/J2 backplane with 12 rear-justified slots and a mounting/wire harness for two half-height, 5.25-in. peripheral devices. The standard 350-W power supply is mounted behind and below the back-

(continued on page 144)

(continued from page 143)
plane to allow for total access to the P2 area. Cooling is via a fan tray with three tube axial fans located in the upper rear

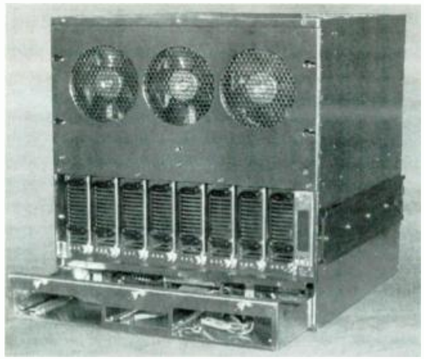


of the enclosure. Pricing is $2948 each and delivery is from six to eight weeks.

Hybricon Corp., 12 Willow Road, Ayer MA 01432; Sales Dept. (508) 772-5422; fax (508) 772-2963; e-mail: info@hybricon.com; Internet: http://www.hybricon.com. **CIRCLE 563**

NT Server Enclosure Is Fault-Tolerant

The H420 enclosure is designed to accommodate ATX, Alpha, or Sparc system boards, along with a PCI RAID controller, SCA system drives, and removable devices. For fault tolerance, the eight RAID drives, as well as the three N+1 300-W power supplies and



numerous fans, are all hot-pluggable. In addition, the lower drive tray, SCSI expansion connector board, and environmental microprocessor, are field replaceable. The entire enclosure is mounted on 175-lb-capacity slides for easy system access. A pluggable microprocessor with an LCD both monitors and gives status indication. Pricing is from $6999.

Trimm Technologies, 350 Pilot Rd., Las Vegas, NV 89119; Rob Smith, (800) 423-2024; fax (702) 361-6067; e-mail: rsmith@trimm.com; Internet: http://www.trimm.com. **CIRCLE 564**

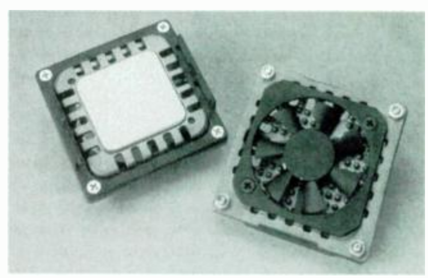
New Enclosure Caters To VME64-Extension Systems

Designed to meet the IEEE 1101.10 specification, the Power Cage II enclosure for VME64-extension systems has from 10 to 21 slots and includes a subrack, backplane, triple fan cooling, and a high-efficiency power supply (500, 750, or 1000 W). The cage accommodates 6U by 160-mm boards and uses a 10-layer backplane with active automatic daisy chaining. Pricing is from $3075.

Electronic Solutions, A Zero Corporation Company, 6790 Flanders Dr., San Diego, CA 92121-2902; Lori Mathios, (800) 854-7086; fax (619) 452-9464; e-mail: lorim@elsol.com; Internet: http://www.zero/elsol. **CIRCLE 565**

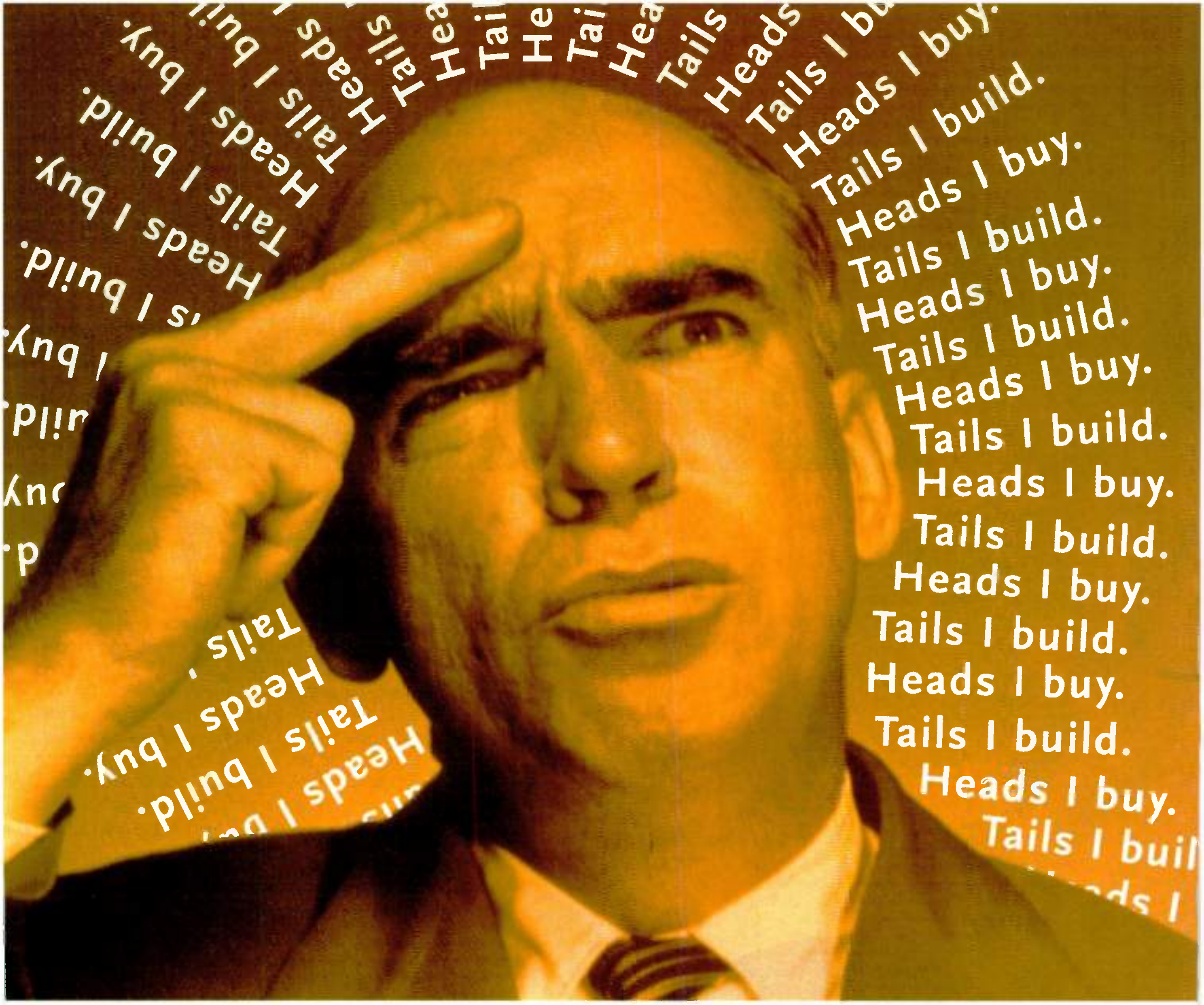
Super-Thin Heat Sink Cools High-End Processors

The LowPro is a super-thin heat sink/frameless-fan combination for high-end processors that measures 7.5-mm wide by 1/3-in. high. Designed for Intel, IBM, Cyrix, and Motorola



processors, the device uses a brushless dc fan, aluminum-alloy and ball-bearing construction, and weighs 28 g. Other features include an operating temperature range of –10° to 70°C and a noise level of 26 dB(A). Pricing is $11.25 each per 1000.

Chip Coolers, 333 Strawberry Field Rd., Warwick, RI 02886; Sales Dept., (800) 227-0254; fax (401) 732-6119; e-mail: sales@chipcoolers.com; Internet: http://www.chipcoolers.com.
CIRCLE 566



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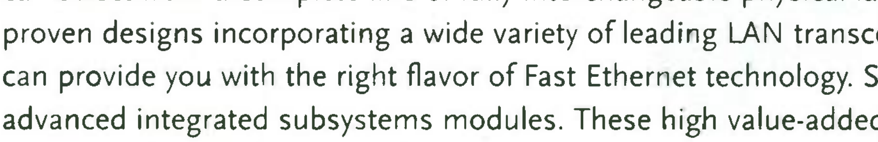

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Circle 520

High-Voltage Power Pulse Circuit

R.N. SCHOUTEN
Faculty of Applied Physics, DIMES, Delft University of Technology,
P.O. Box 5046, 2600A Delft, The Netherlands.

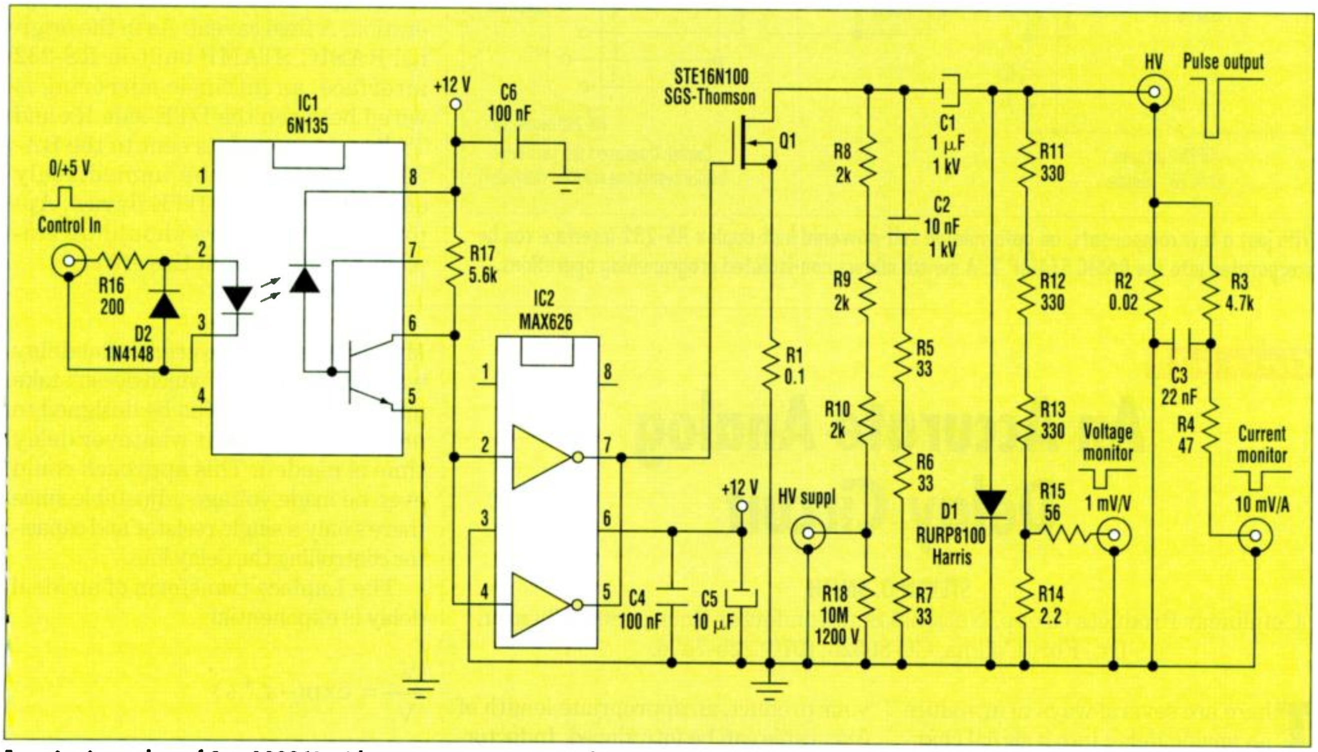
Fast rise-time high-voltage pulses have many uses ranging from EMC testing to device characterization.The simple, low-cost circuit described here deals with the latter. It's able to generate 0- to 1000-V pulses with currents up to 50 A, and a rise time of 100 ns for 800 V/30 A. The output can withstand short circuits, and capacitive and inductive loads. Pulse length and repetition rate are determined by an optically isolated TTL-input signal. Commercial equipment like pulse/function generators or a PC can be connected to this input. The pulse's amplitude is set by the HV supply; a low-cost photomultiplier-type supply (0, 5 ..5 mA) can be used when repetition rates are below 20 Hz.

The circuit operates as follows: when applying the HV supply, C1 is charged up to a voltage HV via R1 and D1 *(see the figure)*. A 0-V control signal keeps the PowerFET Q1 in the off state. A 5-V signal on the control input operates the driver IC2, from which a 12-V signal is presented on the gate of the PowerFET Q1, bringing it into conductance. The output of the circuit becomes −HV volts as the negative terminal of C1 is now grounded. The pulse ends by making the control signal 0 V. Useful pulse length is limited by he voltage drop during the pulse (caused by discharging C1) and by the 100-µs/64-A save limit of the PowerFET. For the values shown, the circuit voltage drop is 10 V for a 1-µs, 10-A pulse.

The short-circuit and overload protection is based on R1. When the output current is rising, the effective gate-source voltage of the PowerFET diminishes, enlarging the FET resistance. With the given 0.1-Ω value, the output current is limited to 50 A. In a short-circuit situation, capacitor C1 can be fully (and safely) discharged in the PowerFET. Reverse voltages caused by inductive loads are eliminated by D1. When the circuit isn't operating, R14 discharges C1 for safety reasons.

Circuit layout is very important—a groundplane is needed to keep inductance low. C1 must be a low-inductance pulse capacitor. Even the FET driver IC2 needs a low-inductance layout and decoupling. During the leading-edge gate currents, up to 2 A are needed to charge the FET input capacitance. Resistors R1 and R2 have to be made of at least 10 paralleled discretes to get a low series inductance. R4 and C3 compensate for the remaining inductance in R2 (the value of C3 can be changed for this). C2, R5, R6, and R7 form a snubber network to protect the FET against voltage spikes. The values for the voltage and current monitor levels are given for a 50-Ω load.

Higher currents can be obtained by duplicating the IC2-Q1-R1 stage and connecting them in parallel. R1 helps to equalize the current for each stage. A 100-A pulser has been successfully built in this manner.



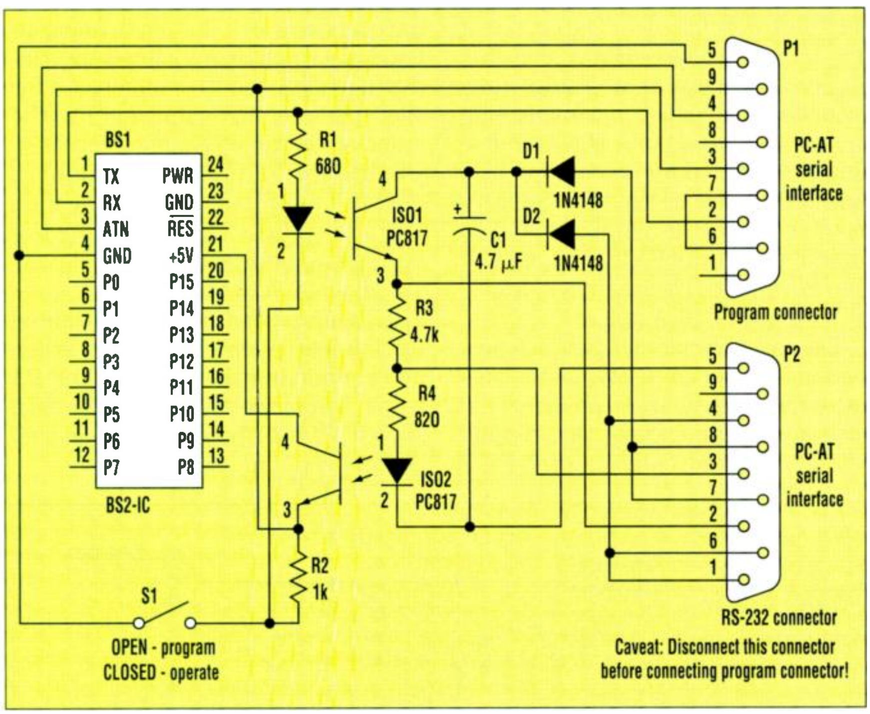
Fast risetime pulses of 0 to 1000 V, with currents up to 50 A, can be generated by this simple, low-cost high-voltage power pulse circuit.

Circle 521

BASIC STAMP 2 Has Optoisolated RS-232 Interface

ENRICO M. STADERINI
Staderini Strumenti Scientifici, Viale J.F. Kennedy,
141 00043 Ciampino (RM), Italy.

An optoisolated, half-duplex RS-232 interface can be added to Parallax's BASIC STAMP 2 with just a handful of low-cost components *(see the figure)*. The circuit implements a switch to change from programming (non-isolated) to normal operation (optoisolated). The operation in optoisolated mode has the same performance as the normal BASIC STAMP non-optoisolated connection using pins 1 and 2 of the internal built-in serial port.



With just a few components, an optoisolated self-powered half-duplex RS-232 interface can be incorporated into the BASIC STAMP 2. A switch allows non-isolated programming operations.

Diodes D1 and D2 feed positive-level power to optoisolator ISO1, which drives positive the serial out line (Rx line as seen from the host computer DTE). The negative drive on the serial out line is accomplished passively by mirroring the negative rest level of serial in line (Tx line from the host DTE) through resistor R3. This means that a real DTE device (generating ±10-V RS-232 signals) has to be connected to the RS-232 connector shown on the schematic. During receive operation, the Tx line from the DTE device drives the ISO2 LED, which turns on the common-collector phototransistor.

A switch is needed to disconnect ground for the optoisolators during programming. The BASIC STAMP isn't able to drive the serial line and the ISO1 LED at the same time. Otherwise, a "Hardware not found" message would immediately appear when attempting to download a program..

The program and RS-232 connectors should never be connected at the same time since, during programming, the phototransistor of ISO2 is subject to a high V_{ce} voltage with no current-limiting. Driving the ISO2 LED would burn out this transistor.

The system has been successfully tested up to 9600-baud half-duplex operation. A final caveat: As in the original BASIC STAMP built-in RS-232 interface, an intrinsic mirroring is wired between the DTE-side Rx and Tx line; i.e., any data sent to the BASIC STAMP will be immediately echoed back to the DTE device. Appropriate software should be employed to circumvent this effect.

Circle 522

An Accurate Analog Delay Circuit

STEVEN O. SMITH
Comlinear Products Group, National Semiconductor Corp., 4800 Wheaton Dr., Fort Collins, CO 80525; (970) 225-7576.

There are several ways to introduce an analog delay into a signal channel. If you have enough room in your product, an appropriate length of coax cable can be introduced. Inductor-capacitor delay lines can be purchased. My preference is to create the delay with active circuitry, which doesn't take up much space and can be designed to precisely implement whatever delay time is needed. This approach could even be made voltage-adjustable since there's only a single resistor and capacitor controlling the delay line.

The Laplace transform of an ideal delay is exponential:

$$\frac{V_o}{V_i} = \exp(-\tau * s)$$

(where τ is the desired delay), which re-

quires an infinite number of poles and zeroes to implement. Because the ideal form can't be implemented (practically), we need to use an approximation.

An accurate, simple approximation to the ideal can be achieved by using a technique known as Padé approximation. The first-order Padé approximation to an ideal delay has the following form:

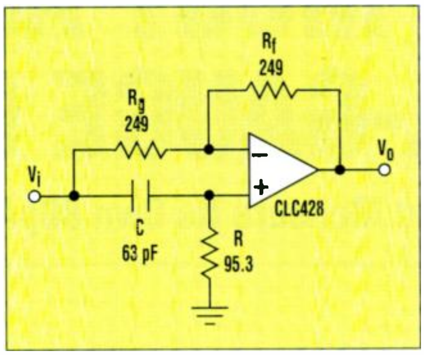
$$\frac{V_o}{V_i} = \frac{1 - \tau s/2}{1 + \tau s/2}$$

(where τ is the desired delay).

The circuit in Figure 1 has the following transfer function:

$$\frac{V_o}{V_i} = \frac{1 - R*C*s}{1 + R*C*s}$$

which has the same form as the first-order Padé approximation, with the R*C time constant equaling half the desired delay time.



This compact circuit provides a controllable analog delay that can be accurately predicted if an op amp with a wide bandwidth is selected.

The circuit was built with 1% resistors and a capacitor with a value measured at 63 pF. This combined with a resistor value of 95.3 Ω gives an R*C value of 5.94 ns. This R*C time constant corresponds to an overall delay time of 11.9 ns (τ is 2*R*C).

Measuring the delay time of this circuit with a 5-ns rise-time pulse gave a delay of 12.2 ns, which is a pleasingly accurate result. The accuracy for this short of a delay time can be attributed both to the success of the Padé technique and to the wide bandwidth of the CLC428 op amp used in the circuit. Using a slower amplifier will result in a less accurate delay.

Accurate delay values are easily accomplished using only a first-order approximation. The circuit works effectively, even for short delay times, if a fast enough amplifier is used.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $300 Best-of-Issue award.

Circle 523

DC-Controlled Low-Pass Filter Has Variable Breakpoint

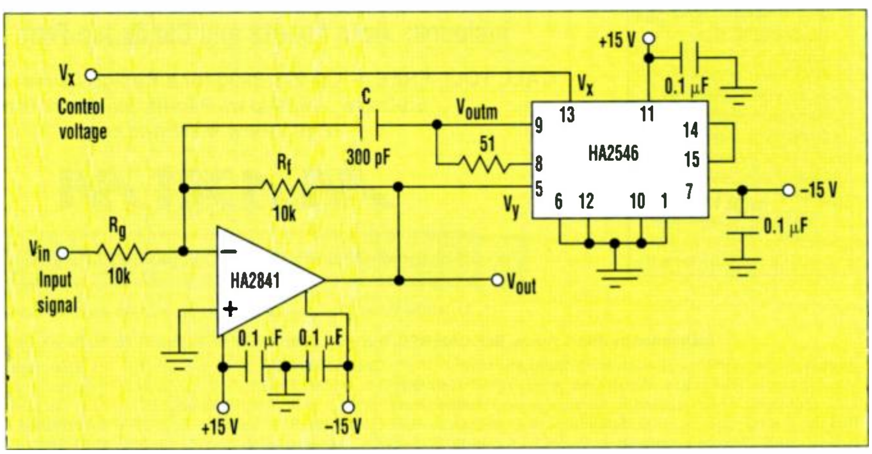
RONALD MANCINI
Harris Semiconductor, P.O. Box 883, M/S 58-095, Melbourne, FL 32902.

When maximum performance is demanded from communications systems, test equipment, or any other frequency-sensitive systems, it's imperative to get the point where the filter response is –3 dB (the breakpoint of the low-pass filter) placed exactly right. Placing the breakpoint correctly ensures minimum distortion in the passband while yielding maximum attenuation of unwanted frequencies in the stopband. This is very hard to accomplish in multiple frequency systems because when a break frequency is placed correctly for one task it is, usually by definition, wrong for another task.

The described low-pass filter has a breakpoint that's continuously variable over a range of 20 to 1 by varying the dc control voltage. The gain stays constant regardless of the breakpoint setting. If digital control is advantageous, a DAC can easily be interfaced into the control voltage port because the control voltage ranges from 0 to 1.5 V.

The HA2841 op amp is the main amplification element in the circuit, and it was chosen because it has excellent dc characteristics coupled with high frequency response *(see the figure)*. The input signal is amplified by the op amp, but only the dc portion of the output signal is fed directly back to the op-amp summing junction. This fixes the dc gain at $-R_f/R_g$. The ac portion of the output signal is passed through the HA2546 high-frequency multiplier before it's fed back to the summing junction.

The HA2546 was chosen for this application because it's extremely small time delay doesn't introduce distortion. The feedback capacitor (C) blocks any dc multiplier errors. As V_x changes, the multiplier gain changes, so the apparent value of C changes. Consequently, the breakpoint fre-



A dc control voltage can adjust the –3-dB breakpoint of this low-pass filter over a 20:1 range.

quency is forced to change. In the equation for the multiplier, V_{outm} is the multiplier output voltage:

$$V_{outm} = \left(\frac{V_x V_y}{2}\right) = \left(\frac{V_x V_{out}}{2}\right)$$

The equation for the complete circuit response is:

$$\frac{-V_{out}}{V_{in}} = \left(\frac{R_f}{R_g}\right)\left(\frac{1}{\left(1 + \left(\frac{V_x R_f C}{2}\right)\right)}\right)$$

$$\omega = 2\pi F = \frac{1}{V_x R_f C}$$

The control voltage (V_x), in conjunction with R_f and C, determine the breakpoint frequency, ω. R_f and C are used to center the frequency range, and V_x varies the frequency within this range. Both R_f and R_g set the gain, so there's plenty of flexibility in the component selection. The component values shown yield a frequency range from 1.7 MHz when V_x = 0.1 V to 80 kHz when V_x = 1.25 V. The control input is similar to an op-amp input, thus it needn't be driven by a low-impedance source. This input may be driven from a DAC to obtain digital control of the breakpoint, but the DAC output voltage must be level-shifted to 0 to 1.5 V.

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Circle 524

Turn An 8-Pin Microcontroller Into A Programmable Fractional Divider

YONGPING XIA

Teldata Inc., 8723A Bellanca Ave., Los Angeles, CA 90045.

The PIC12C508 is an 8-pin microcontroller that contains an RC oscillator (4 MHz) and power-on-reset circuitry. Two pins are for ground and power-supply connections, while the remaining six pins are dedicated for input/output. This tiny microcontroller provides a low-cost and space-saving solution for some applications that require fewer parts than if conventional logic devices are used.

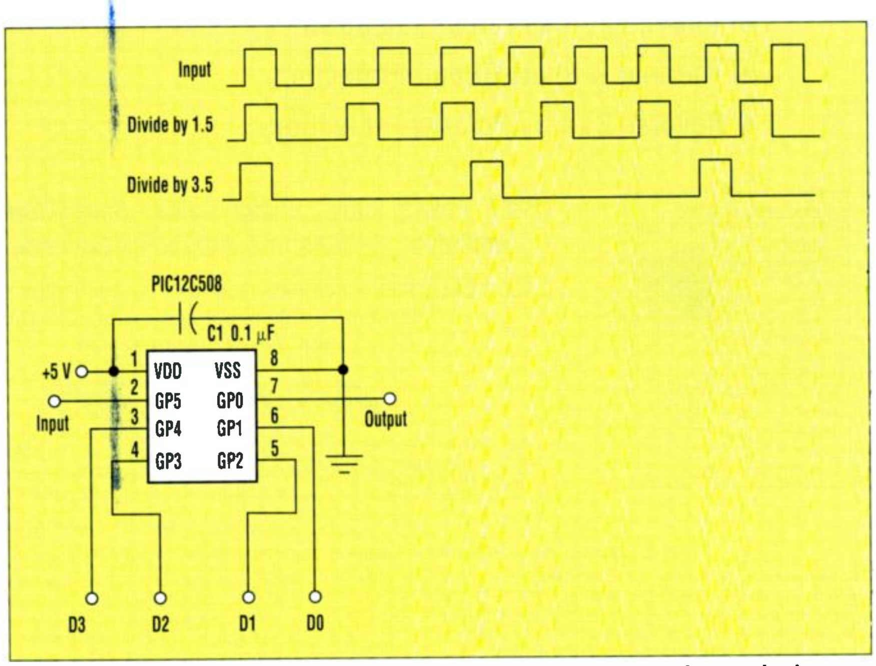
The circuit shown is used to implement a fractional divider using the PIC12C508 *(see the figure)*. The divide ratio produced is completely controlled by software. The microcontroller can divide an input signal by a factor of 1.5 to 16.5. D0-D3 selects the divide ratio. Note that the speed of the circuit is limited by the microcontroller's execution time. It can work reliably under 30 kHz with a minimum input pulse width of 6 µs.

```
LIST    P=12c508
STATUS          equ     0x03
GPIO            equ     0x06
Z               equ     0x02
pulse_number    equ     0x07
data_1          equ     0x09

                org     0x0
main            clrf    GPIO
                movlw   0xfe
                tris    GPIO
                movlw   0x80
                option

                movf    GPIO, 0
                andlw   0x20
                movwf   data_1
start
                movf    GPIO, 0
                andlw   0x20
                subwf   data_1, 0
                btfsc   STATUS, Z
                goto    start
                clrf    pulse_number
                bsf     GPIO, 0
                movf    GPIO, 0
                andlw   0x1e
                movwf   pulse_number
                incf    pulse_number,1
                movlw   0x20
                xorwf   data_1, 1
loop_1
                movf    GPIO, 0
                andlw   0x20
                subwf   data_1, 0
                btfsc   STATUS, Z
                goto    loop_1
                bcf     GPIO, 0
loop_2
                movlw   0x20
                xorwf   data_1, 1
loop_3
                movf    GPIO, 0
                andlw   0x20
                subwf   data_1, 0
                btfsc   STATUS, Z
                goto    loop_3
                decfsz  pulse_number.1
                goto    loop_2
                movlw   0x20
                xorwf   data_1, 1
                goto    start

                end
```



This low-cost 8-pin microcontroller is used to divide an input frequency by a fractional value.

JULY 1998

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, CA. Contact Jim Schwank, Sandia National Laboratories, P.O. Box 5800, MS-1083, Albuquerque, NM 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST 1998

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OCTOBER 1998

IEEE International Conference on Systems, Man, & Cybernetics, Oct. 12-14. Hyatt Regency La Jolla, La Jolla, CA. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855; (908) 445-3627; (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

NOVEMBER 1998

Photonics East & Electronic Imaging International Exhibition, Nov. 1-6. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Voice, Video & Data Communications Conference & Exhibition, Nov. 1-6. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhbits@spie.org.

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, P.O. Box 123; Broadway, NSW 2007, Australia; +61 2-330-2435; e-mail: samr@trnasmit.ee.uts.edu.au.

DECEMBER 1998

12th Systems Administration Conference (LISA '98), Dec. 6-11. Marriott Hotel, Boston, Massachusetts. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1999

Annual Reliability & Maintainability Symposium (RAMS), Jan. 19-21. Washington Hilton, Washington, DC. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 4. New York, NY. Contact Frank Schink, 14 Middlebury Lane, Cranford, New Jersey 07016; (908) 276-8847; fax (908) 276-8847.

FEBRUARY 1999

Photonics West, Feb. 6-12. San Jose, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

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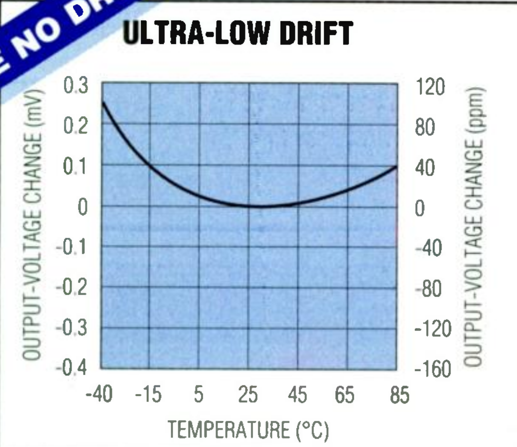

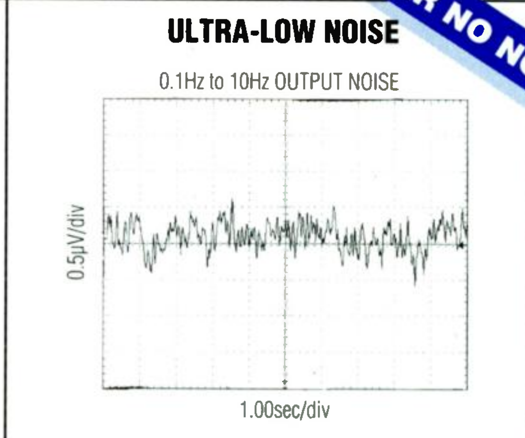

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MAX6225A/B	2.5	2.0/5.0	±0.04/±0.1	2.8	Yes	4.65/2.25
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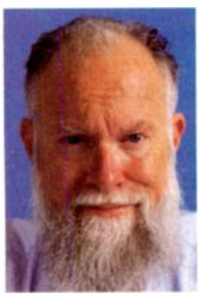
BOB PEASE

What's All This Camel Stuff, Anyhow?

Once upon a time, I worked at Teledyne Philbrick. Way back in 1975. We had had a good president, Bill Frusztajer, who came over from Crystalonics. But Teledyne decided to retire him and brought in a new president, Mr. Chechik.

Many people observed that Mr. Chechik was indecisive. Even with all of our help, he could not make up his mind for even a simple decision. In fact, there was a book that came out a few years later called *My Indecision is Final*. I immediately went out and bought the book—and was astonished to see that it was NOT about Mr. Chechik.

Finally, Teledyne decided to relieve Mr. Chechik of his problems, and they brought in a new president. His name was Bill Earley. We soon learned a lot about Mr. Earley. He had a unique way of arguing. If he asked you to explain a problem, and you gave him an explanation, after a minute he would likely stop you and say, "I don't understand your explanation. So you are a stupid explainer. You are wrong. I'll make a decision, and YOU LOSE because your explanation was lousy." In other words, he made his own stupidity an advantage, because he could claim at any time that his inability to understand your explanation was due to YOUR stupidity....



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Twenty years later, if we had to find a way to make Dilbert's boss look good, Mr. Earley could have done it. Bill Earley was not a real fan of engineers. He always thought that engineers were really dumb and had no sense. Product planning, he declared, was to be done by the marketing guys, and after they reached their conclusions, the engineers could just design what they were told to do. No, Mr. Earley did not make a lot of friends in Engineering.

Bill Earley thought that all engineers were only capable of designing products that nobody would want to buy. He told us all who was going to be in charge of new product planning.

Of course, at that time, most of the marketing guys at Philbrick had NO IDEA how to design a good product, but they were willing to try. AND of course at that time, there were engineers who had designed a lot of popular and successful new products, but our friend Bill didn't want to hear a peep out of them.

And the whole BUILDING had been paid for by the profits on the P2, which was designed by an engineer who knew that nobody asked for a P2, but he had confidence that if he made them, the business would come. If you want the detailed story about the P2, look up "What's All This Profit Stuff, Anyhow?" (ELECTRONIC DESIGN, *Nov. 7, 1991, p. 115*).

Well, the next few months after Mr. Earley arrived were not a lot of fun. He threw out a number of engineers who seemed to know what they were doing. Threw out a lot of good guys, including Dave Ludwig and George Lee. Other engineers just bailed out.

In the fall of 1975, I had some squabbles with manufacturing, because they told us that if we followed their guidelines and designed a good new product, the manufacturing guys could later tell us that they were NOT cost-effective, because we had designed them wrong. If we claimed that we had followed their guidelines, that did not matter. A new low-cost circuit could be shown *retroactively* (by the manufacturing guys) to be MORE expensive than the old design, NOT cheaper to build. (This was mentioned in my old column "What's All This Cost-Accounting Stuff, Anyhow?" (ELECTRONIC DESIGN, *Feb. 28, 1991, p. 87, or Aug. 19, 1996 reprints, p. 39*)

So, I had a squabble with Bill Earley and the manufacturing guys. I did not win any arguments, because the manufacturing guys argued like Bill Earley did—if you don't like my argument, YOU are stupid. Coming down to the end of 1975, I came to the conclusion that there was no future for me at that company. Engineers were supposed to just shut up and do what they were told.

Further, I had been given the task of designing a new low-cost ADC. But they wanted a package and pin-out that was completely nonstandard vs. any other existing product. And the cost was completely arbitrary, so if you designed a product that everybody initially agreed was better, according to all the guidelines, it could later be declared to be NOT lower in manufacturing cost. So, I decided to leave the company. I would resign on the last day of 1975.

Now, let me digress to an old story—an EsaeP's Fable: Once upon a time there was an Arab who wanted to cross a wide desert. So he fed and watered his camel well, and got all necessary supplies, and started out. The very first afternoon, a sandstorm began to blow. The Arab got off his Camel and pitched his tent and climbed in, to wait out the storm.

After a while, the Camel said, "Master, pray let me put my nose under your tent, for the sand is blowing in my nose. If I suffocate, I cannot carry you across the desert." So the Arab let the camel put his nose under the tent.

Shortly thereafter, the Camel said, "Pray, Master, let me put my eyes under your tent, because the sand is blowing in my eyes, and if I go blind, I cannot carry you across the desert." So the Arab let the Camel put his eyes under the tent. THEN after a suitable delay, the Camel asked, "Pray, let me put my ears under your tent, as the sand is blowing my ears."—etc. This was shortly followed by, "The sand is blowing on the cut on my shoulder, Pray let me put my Shoulder under your tent." And shortly the Camel pushed the Arab out of his own tent.

And THAT is the Fable of the Arab and the Camel. In other words, a Camel is anybody who can push you out of your own tent, by asking for just a little more....

For about 10 years at Philbrick, I had been giving out "Camel Awards" on the last day of the year. This was based on the concept that a Camel would ask for one specification, and then another, and another, and while not any one spec was prohibitively difficult, when the total picture was in focus, the combination of the specs made it *impossible.*

The perfect example was a guy who wanted one of our standard op amps, but with a little less voltage noise—and a little more gain—and a little less current noise, too ... until it became impossible. So every year for over 10 years, I gave out Camel Awards to various applications guys and sales guys.

I gave out plaques and certificates. I gave out little plastic camel figures that were painted gold. I zinged our marketing and sales guys, and heckled them for making various silly mistakes.

For the last day of 1975, I put together some real *zingers*. I made up a special award—not just a Bactrian, and not a dromedary, but a three-hump award. I fabricated it very carefully. Then I got an old 4701 Voltage-to-Frequency Converter, and doctored up the silk-screen to say "V-to-$ Converter"—because it really did convert into $$$. I put it under the first hump. Similarly, I put a 4702 Frequency-to-Voltage converter marked up to say "F-to-$ Converter," under the third hump.

On the last day of 1975, as I tootled my little camel flute, I went down to give out the Camel Awards. We went down to the marketing area. There, with 70 people AND Charlie Lohmiller, the Company Photographer (whom I had invited down, just in case there might be some good photo opportunities). I then gave out the awards. I started out with some zingy ones, and then I got nastier. Finally I unveiled the three-hump award, as a special award for Mr. Earley.

Oooh—aah—giggle. I explained to the group about the 4701 V-to-$ Converter and the 4702 F-to-$ Converter. Then, I explained that under the *middle* hump was—my resignation. I took it out and handed it to Bill Earley. I still have a photo somewhere of him smiling wanly as he started to read it. I explained that it was impossible to do my job any more with "management" doing what they did, and I walked out. Within four minutes, I started getting phone calls from old (ex-Philbrick) friends at Burr-Brown, Datel, and other competitors, congratulating me for doing such a good job on Bill Earley. Yeah, the news sure did get around fast.

Then, I went home for a New Year's Eve party with 30 friends. (I HAD told my wife I was quitting.) I told my friends that I had the 70 witnesses AND the Company Photographer, so there would be no mistake that I was REALLY resigning. No going back. And within a couple months, I moved out to California. But that's a whole 'nother story.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@webteam.nsc.com—or:

Address:
Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

P.S. On Friday morning, January 2, 1976, I drove down to work. When I got there, there was 5 inches of new snow all over the parking lot—and no cars. I laughed and laughed. The only guy to show up on that Friday was the guy who had just resigned. Nobody had told me that was a holiday. /rap

P.P.S. If you want to hear about how our Annapurna trek comes out, send me an e-mail or snail-mail request and I'll send you a report on ~Dec. 15. (It may take another month to get pictures on my web site.) We did get the trip filled up to 15 people. /rap

Circle **550** if you want to find out how exactly the three-hump award was constructed.

Circle **551** if you have you ever quit more emphatically than that.

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The SCC components offer modular, configurable, and cascadable analog signal conditioning. Each has one or two analog inputs. Users can plug any mix of SCC components into the SC-2345 carrier module, which provides power and wire strain relief for up to 16 modules. The PCI-6071E costs $1995, the PCI-6031E $2095, the PCI-6032E $1495, and the PCI-6033 $1595. SCC Series modules start at $30. JN

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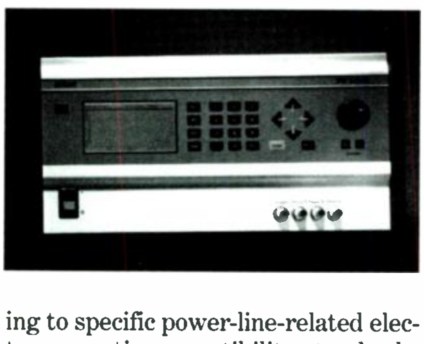

ing to specific power-line-related electromagnetic-compatibility standards. The SWAE and SWA-106 test devices to the IEC 1000-3-2 (EN61000-3-2) standard, which specifies limits for current harmonic distortion, and the IEC 1000-3-3 (EN61000-3-3) standard, which specifies limits for voltage fluctuations and flicker. The SWAE also supplies the waveform needed to test to IEC 1000-4-13 (EN61000-4-13), which is the harmonic/interharmonic voltage-immunity standard.

The units have a built-in reference impedance for flicker measurements. Three built-in arbitrary waveform generators allow for simulation of various line disturbances, including sub-cycle and multi-cycle dropouts, spikes, distorted waveforms, noise, sudden phase shift, over and undervoltages, and frequency changes. The SWA-106 can measure actual RMS voltage, amperes, watts, VA, power factor, and frequency. Prices start at $10,280. JN

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***Fluke Corp.**, P.O. Box 9090, Everett, WA 98206; (800) 443-5853; fax (800) 358-5332; e-mail: fluke-info@tc.fluke.com; Web: http://www.fluke.com.* **CIRCLE 593**

PCMCIA Data Cards Come In 12- And 16-Bit Versions

A series of data-acquisition cards based on the PCMCIA 2.1 standard offer 12- or 16-bit performance, with analog input, analog output, counter-timer, and digital I/O capability. The KPCMCIA-12AIAO (12-bit) and -16AIAO (16-bit) cards sample data at up to 100 ksamples/s and have 2-kbyte FIFO scan and data buffers for gap-free acquisition. The cards supply eight single-ended or four differential analog input channels with gains of 1, 2, 4, or 8 and a range of ±10 V. They also have two 12-bit, ±5-V waveform-quality analog outputs and a 16-bit counter-timer. The analog outputs are updated simultaneously at 100 kHz. Each card has four digital input lines and four digital outputs. Two other versions, the 12-bit KPCMCIA-12AI and 16-bit KPCM-

(continued on page 163)

(continued from page 161)

CIA-16AI, are high channel-count boards without the analog outputs. These cards can be configured for 16 single-ended or eight differential channels. The cards come with software for complete operation under Windows 95. The KPCMCIA-12AIAO costs $825; the KPCMCIA-12AI, $699; the KPCMCIA-16AIAO, $925; and the KPCMCIA-16AI, $825. Delivery is from stock. JN

***Keithley Instruments Inc.**, 28775 Aurora Rd., Cleveland, OH 44139-1891; (888) 534-8453; (440) 248-0400; fax (440) 248-6168; e-mail: product_info@keithley.com; Internet: http://www.keithley.com.* **CIRCLE 594**

Function Generator Offers Low Harmonic Distortion

The DS360 function generator features total harmonic distortion better than –100 dB. Functions include sine, square, two-tone, white, and pink noise over a range of 1 mHz to 200 kHz. Frequency resolution is 1 mHz and frequency stability is 25 ppm. Other capabilities include linear and log frequency sweeps, digital outputs (AES-EBU and SPDIF/EIAJ), and standard RS-232 and GPIB computer interfaces. The instrument comes with BNC, XLR, and banana output connectors for interfacing to various systems. The DS360 costs $2395. JN

***Stanford Research Systems**, 1290-D Reamwood Ave., Sunnyvale, CA 94089; (408) 744-9040; fax (408) 744-9049.* **CIRCLE 595**

Data-Acquisition Devices, GPIB Interface Plug Into USB

Three data-acquisition devices and a GPIB interface take the form of external peripherals that plug into the universal serial bus (USB) on Windows-based PCs. The DAQPad-4350 for USB ($1295) measures temperature with thermocouples, RTDs, and thermistors. Its ±15-V input range is ideal for low-bandwidth analog applications. The unit features a ±0.4°C thermocouple accuracy, six reading rates (10, 50, and 60 readings/s in one-channel mode; 2.8, 8.8, and 9.7 readings/s in multichannel mode), and eight digital I/O lines.

The DAQPad-6020E for USB ($1195) is a multifunction analog, digital, and timing interface. It has 16 single-ended or eight differential analog inputs and 12-bit sampling at 100 ksamples/s. Two 12-bit analog outputs and eight digital I/O lines are available. The DAQPad-6507 for USB ($695) has 96 parallel digital I/O lines. It uses 24-bit programmable peripheral interfaces, which can be divided into three 8-bit ports, and it can operate in unidirectional or bidirectional mode as well as handshake with peripheral equipment.

The GPIB-USB ($495) is a plug-and-play IEEE-488.2 interface for controlling up to 14 programmable instruments via the USB port. It needs no external DIP switches and users needn't restart the computer after installation.The data-acquisition devices come with the NI-DAQ driver software, and the GPIB interface comes with the NI-488.2M driver software. JN

***National Instruments Corp.**, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 258-7022; fax (512) 794-8411; e-mail: info@natinst.com; http://www.natinst.com.* **CIRCLE 596**

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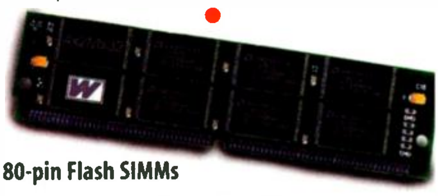
- 5V operation



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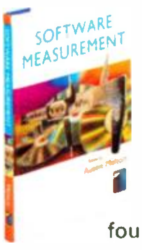

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Receiver-On-A-Chip Cuts GPS Costs

Incorporating a complete dual-stage downconverter and gain-control circuit, the UBP1004GS is a single-chip GPS receiver aimed at cost-sensitive consumer applications. Its bipolar silicon MMIC technology and dual-conversion architecture give it excellent out-of-band spurious signal rejection and reduced power consumption. The UBP1004GS consumes only 37.5 mA from its 3-V supply.

Requiring only a low-cost LNA at its front end, the receiver outputs a 5 MHz 2nd IF signal for digitization and processing by a GPS engine. The units' on-chip prescaler, oscillator, phase detector, and loop amplifier reduce a receiver design's overall component count to a handful of passives and three SAW filters.

Housed in a 30-pin SSOP, the UBP1004GS is priced at under $5 in production quantities. An evaluation kit, complete with pc board, connectors, receiver, and application notes, is available free of charge. LG

***California Eastern Laboratories**, 4590 Patrick Henry Dr., P.O. Box 54964, Santa Clara, CA 95054-1817; (408) 988-3500; fax (408) 988-0279.* **CIRCLE 597**

SONET/SDH Transceiver Meets Bellcore Jitter Specs For ATM

Targeted at jitter-sensitive wide-area network (WAN) applications, the CY7B952 clock and data-recovery transceiver meets the exacting specifications of both Bellcore and the CCITT for line jitter. Its on-chip phase-locked loop allows it to recover clock and data from OC-1 (51.84 Mbits/s) or OC-3 (155 Mbits/s) SONET data streams without the use of costly VCXOs or SAW filters. An internal loopback capability permits designers to easily implement self-test into equipment using this transceiver. Available now in an SOIC package, the CY7B952 costs $33.50 each in 1000-piece lots. LG

***Cypress Semiconductor Inc.**, 3901 N. First St., San Jose, CA 95134-1599; (408) 943-2600 or (800) 858-1810; http://www.cypress.com.* **CIRCLE 598**

Two-Chip GPS System Targets Auto, Marine OEMs

The SC1575 GPS correlator/controller and SA1570 front-end mixer form a two-chip solution for accurate, inexpensive OEM automotive and marine-navigation applications. Comprised of a 16-bit processor core with additional I/O and processing circuitry, the SA1575 processes incoming signals from the SA1570 to produce velocity, time ,and position data. The SA1570 front end includes a complete RF front-end mixer and IF synthesizer and performs all necessary RF processing. A full-up reference design, complete with documentation, an assembled system evaluation board, and sample host interface programs, is available to speed development efforts. Priced at under $20 in large volumes, the chip set is available immediately. LG

***Philips Semiconductor Inc.**, 811 E. Arques Ave., P.O. Sunnyvale, CA 94088; (408) 991-2722, (408) 991-4500, www.semiconductors.philips.com.* **CIRCLE 599**

Integrated 10/100 PHY-Ceiver Comes As Chip Or Standard Cell

The DP83843 PHYTER combines the physical (PHY) layer and transceiver functions for both 10Base-T and 100Base-TX Ethernet networks. Designed to reduce the power and space

requirements for both NICs, hubs, and switches, the single-chip PHY-Ceiver has standard MII and AUI interfaces, as well as connection auto-negotiation logic. For designers with special needs, the PHYTER is available as a standard logic cell, allowing it to be rapidly modified for custom interfaces, or incorporated into larger communications-oriented ASICs.

Its driver section can link directly to inexpensive magnetics for twisted-pair copper connections, or drive a standard E/O module for fiber applications. Its adaptive line equalization scheme exceeds the minimum performance specifications. Consequently, it can support full-rate, full-duplex, 100-Mbit/s transmissions over greater distances than the required 100 meters of Category-5 UTP cable, while maintaining low bit-error rates. The DP83843 has an on-chip carrier integrity monitor and a PHY status register. the 80-pin PQFP boasts a tiny 17-by-17 mm footprint and draws only 135 mA of 5-V power. Pricing is $13.00 each in quantities of 1000 pieces. LG

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-5000, http://www.national.com/PHYTER.
CIRCLE 600

Compression/Crypto Chip Speeds Files, Supports Multi-Protocols

Intended to provide security and increased throughput in routers, remote access devices, and virtual private networks, the 7711 data-encryption coprocessor supports most major internetworking standards. This includes DES, triple DES, and RC4 encryption, LZS and MPPC compression, as well as SHA and MD5 authentication specifications. The 7711 performs most of the low-level handshaking required to support IPsec, SS/TLS, PPP, PPTP, and L2TP connections.

Capable of supporting multiple high-speed communication links, the 7711 is fully programmable and can encrypt and decrypt streams at up to eight times the speed of a dedicated 155-MHz workstation.Designers can program the device to support any combination of compression, encryption, or authentication. If all three are chosen, the chip ensures that they are performed in the correct order. The 7711 consumes 0.5 W of 3-V power.

Available now, the 7711 comes in a 144-pin TQFP and costs $79.90, in quantities of less than 100 pieces. LG

Hi/fn, 2105 Hamilton Ave., Suite 230, San Jose, CA 95125; (408) 558-8066, fax (408) 558-8074, e-mail: sales@hifn.com; http:// www.hifn.com.
CIRCLE 601

Temp-To-Voltage Converters Emulate Thermistors

The TC1132 and TC1133 temperature-to-voltage converters have a linear voltage output with temperature to compete with thermistors in various applications. The temperature-measurement range of the TC1132 is -40 to 125°C with corresponding output voltages of 100 mV and 1750 mV. The output voltage of the TC1133 is calibrated in degrees Centigrade with outputs of –200 mV at –20°C to 1 V at 100°C. An external pull-down resistor to a negative voltage source is required for temperature measurement below 0°C. The sensors have a voltage-output slope with a temperature of 10 mV/°C and are available in TO-92 and SOT-23-3 packages. Output linearity is 0.8°C and accuracy at 25°C is ±3°C. Operating from a single supply ranging from 3.0 V (TC1132) or 2.2 V (TC1133) to 12 V, the sensors are priced at $0.34 and $0.32 for the TO-92 and TO-23-3 packages, respectively, in quantities of 10,000. ML

***TelCom Semiconductor Inc.**, 1300 Terra Bella Ave., Mountain View, CA 94039-7267; (415) 968-9241.*
CIRCLE 602

IGBT Modules Honed For Power Conversion

Two IGBT power modules developed by International Rectifier are optimized for low switching and conduction losses in high-frequency power-conversion circuits. Configured as single switches, high-side choppers, low-side choppers, and half bridges, the modules are intended for use in switch-mode power supplies, uninterruptible power supplies, and in welding and induction-heating systems. Typical application circuits include boost and buck converters, forward and double-forward converters, and half-, full-, and three-phase bridges. One series is rated at 600 V and the second at 1200 V, with current ratings from 50 to 500 A. The electrically isolated baseplate is exposed to allow direct mounting to a heat sink. Low thermal resistance allows operation at higher case temperatures while maintaining junction temperatures within safe limits. Pricing starts at $38.00 each in quantities of 10,000. ML

***International Rectifier**, 233 Kansas St., El Segundo, CA 90245; (310) 252-7105.* **CIRCLE 603**

Free Kit Accelerates Filter Development

A free design kit from National Semiconductor helps designers develop high-speed active filters. The kit contains support documentation for the CLC730061 evaluation board, which carries two CLC5602AJE dual op amps, the CLC111AJE high-speed buffer, and surface-mounted resistors and capacitors for interchangeability. On the board, the input buffer is followed by four cascaded Sallen-Key sections implemented by the dual op amps. To order the kit, follow the instructions at National's web site: http://www.national.com/see/activefilter. ML

***National Semiconductor Corp.**, 4800 Wheaton Dr., Fort Collins, CO 80525-9483.* **CIRCLE 604**

The **NJM2178** is a stand-alone monolithic **SRS** three dimensional sound IC with analog signal processing. The **NJM2178** is suitable for application in Computer, TV, Radio, Electronic Game, Keyboard, Musical Instrument, Home Stereo and other typical Audio Systems. The **NJM2178** uses analog signal processing derived from a patented Sound Retrieval System technology developed by SRS labs to achieve a "three dimensional" audio image from only two standard speakers.

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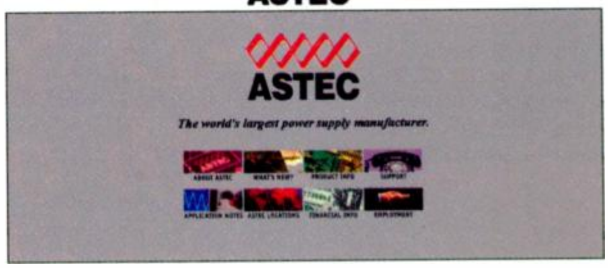

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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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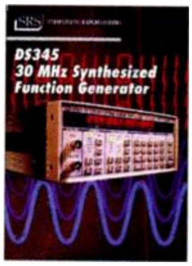
CIRCLE 250

CHAMPION TECHNOLOGIES, INC.

30 MHz WAVEFORM GENERATOR

The DS345 creates synthesized (DDS) sine, square, triangle and ramp waveforms with 1μHz frequency resolution. Arbitrary waveforms of up to 16k points with 12 bit resolution can also be generated. Capabilities include AM, FM, PM and burst mode as well as linear and logarithmic frequency sweeps. The GPIB and RS-232 interface option provides easy communication with computers and includes software for creating arbitrary waveforms. DS345 Function Generator — U.S. List Price $1,595. Call (408) 744-9040.



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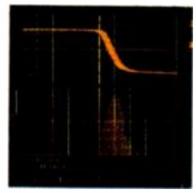

CIRCLE 252

LECROY

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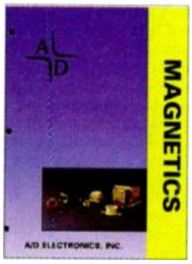

CIRCLE 253

A/D ELECTRONICS

APPLICATION NOTE

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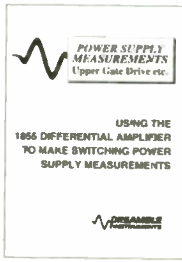

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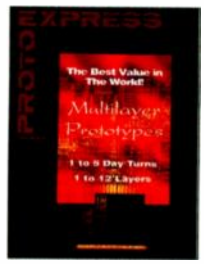

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CIRCLE 258

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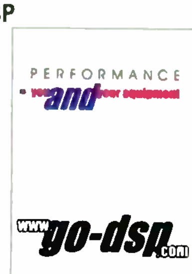

CIRCLE 263

GO DSP CORPORATION

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

INDUSTRIAL PC POWER SUPPLY

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CIRCLE 263

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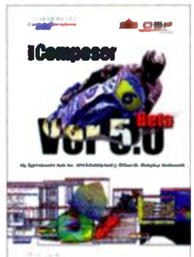

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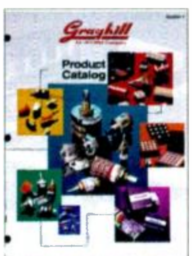

CIRCLE 320

GRAYHILL, INC.

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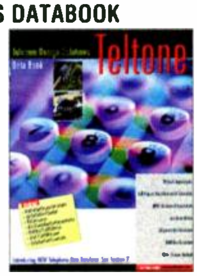
Teltone's 224-page Databook features a wide range of products for network interface applications, including: DTMF Receivers, DTMF Transceivers w/Call Progress Detection, MF Trunk Signaling ICs, Call Progress Tone Detectors, Line Sensing Relays, test tools including Telephone Line Simulators and ISDN Line Simulators, application notes, and more. For your copy call 1-800-426-3926 or 206-487-1515, E-mail at info@teltone.com.



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American Arium has been the primary market supplier of Pentium® processor In-circuit Emulators since 1991. In 1995, the company introduced their Pentium® Pro In-circuit Emulator. Recently, American Arium announced the release of Comet In-Circuit Emulators. These were specifically designed for the embedded software developer, with special attention paid to the 66Mz real-time trace engine and ultra-accurate breakpoints. The Comet ECM-54 is a portable low cost solution which provides processor control through the Intel defined, JTAG debug port. Comet TRC-54 is a full featured In-Circuit Emulator with American Arium Data Capture Technology.

CIRCLE 271

AMERICAN ARIUM

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Western Design Center's product selection and developer guide describes our 65C02-BASED CMOS low power IC microprocessors Included is information about our chips, boards and licensable cores.
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KEYSTONE ELECTRONICS CORP.

REVISED 1998 SWITCH CATALOG

The familiar E-Switch catalog has been revised, including new lines of sealed, illuminated pushbutton; illuminated rocker; slide; and SMT pushbutton switches. Specifications, technical schematics, ordering information for pushbutton, toggle, rocker, power, lever, slide, and rotary are included. Phone: 612-504-3525, Fax: 612-531-8235, http://www.e-switch.com, info@e-switch.com

CIRCLE 276

E-SWITCH

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

1998 PRODUCT SELECTION GUIDE

Pentek's new pocket-size Guide provides capsule specifications and functional block diagrams on our VME, PCI, PMC and VXI product lines. Get the latest information on our line of DSP processors; our new 'C60x, 'C80x and SHARC boards, advanced I/O peripherals; world-class software tools. For your free copy, email or call (201) 818-5900 ext. 803. http://www.pentek.com e-mail: pentek@info.com

CIRCLE 276

PENTEK, INC.

CRYSTALS & OSCILLATORS

The 1997 International source Book offers detailed specifications on Ecliptek's through-hole and surface-mount crystals and oscillators. Visit our internet site at http://www.ecliptek.com. Phone: (714) 433-1200, Fax: (714) 433-1234, or E-mail: ecsales@ecliptek.com.

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ECLIPTEK

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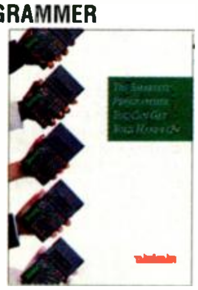

CIRCLE 282

DATAMAN

ENCLOSURES & ACCESSORIES

Bud Industries' new Standard Products Catalog provides technical data and ordering information on over 3,000 products ranging from large relay racks and cabinets to desktop and portable instrument cases including a full line of NEMA and other plastic enclosures. Also included is information on computer workstations, custom fabrication and a wide range of enclosure accessories.

CIRCLE 283

BUD INDUSTRIES, INC.

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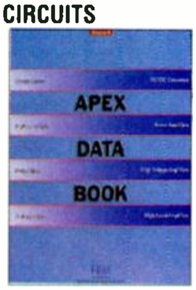

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APEX

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MICROTEC

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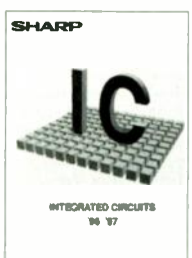

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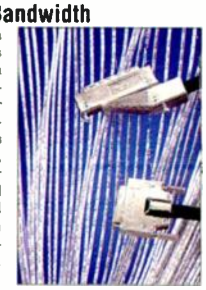
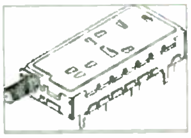


CIRCLE 319

AMPHENOL

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

SINGLE CONVERSION CATV TUNERS



Designed for reception of modulated digital data streams, CASD-series tuners are ideal for consumer set-top or PC add-in receivers. They feature PLL tuning, 62.5 kHz step sizes and low noise, with a return-path low pass filter in some models. F connector and PCP pin inputs available. Call 800-642-0261 for product information. For details via FASTFAX, call 800-833-9437, ext. 3000

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SHARP MICROELECTRONICS

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MODEL TECHNOLOGY

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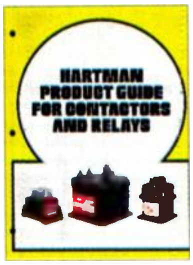
HARTMAN DIVISION



Hartman Division of CII Technologies provides high-reliability electrical contactors, relays and protective units for missiles, military and commercial aircraft, and ground support equipment.

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NEW POWER SOLUTIONS CATALOG

The new 36-page Vicor Express catalog, VE19, details the latest selection of AC-DC and DC-DC power components and complete, configurable power supplies available from Vicor Corporation, 23 Frontage Road, Andover, MA 01810. Contact Kathryn Johnson at (800) 735-6200.

CIRCLE 295

VICOR CORPORATION

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VERO Integrated Packaging Brochure details VERO Integrated Packaging (V.I.P) engineered solutions, including complete custom, fully wired systems (e.g., VME chassis, VXI mainframes) and off-the-shelf, modified or full custom system packaging.
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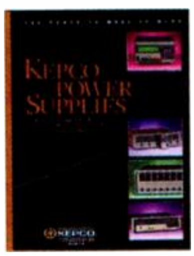
CIRCLE 297

C&K COMPONENTS INC.

KEPCO 1998 POWER SUPPLIES CATALOG



New 182 4-color pages provide engineering specifications on 4 categories of a-c to d-c power supplies. Instrumentation power: analog, digital. Modular power: industrial, commercial. Special-purpose: plug-in hot swaps, battery chargers. Custom power assemblies: hard-wired, user-configured. Tutorial explains programming capabilities. Tel: 718-461-7000; Fax: 718-767-1102. E-mail: hq@kepcopower.com URL: http://www.kepcopower.com

CIRCLE 298

KEPCO

SMI IMAGE PROCESSING LSIs GUIDE

A new Product Selection Guide by Sumitomo Metals Industries lists the features and functions of a variety of SMI image processing LSIs. Handy charts detail all capabilities: convolution, morphology, scan conversion, zoom and rotation, blob analysis, template matching, other processing functions. At higher speeds, lower costs and innovative technology available either off-the-shelf or custom, find the SMI image processor perfect for your project. 1-800-392-4447

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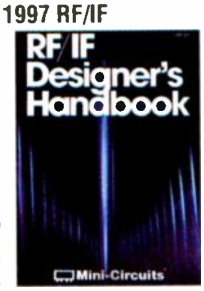
MICROTEK INTERNATIONAL

MINI-CIRCUITS FREE 1997 RF/IF



Mini-Circuits brand new 760 page RF/IF Designer's Handbook is now available for distribution worldwide. The handbook is loaded with fresh design and applications information, such as modern surface mount techniques, practical articles about VCO's, ERA MMIC amplifiers and more, answers to frequently asked questions, definitions of terms, convenient selection guides and handy conversion charts.

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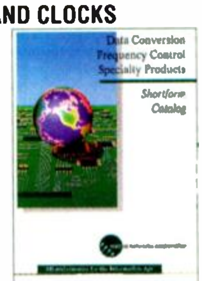
MINI-CIRCUITS

DATA CONVERSION AND CLOCKS



Micro Networks Corp. short form catalog covering standard data converters and frequency control products. Products are designed for commercial, industrial, and military applications in computers, communications and control circuits. Phone: (508) 852-5400

CIRCLE 326

MICRO NETWORKS CORP.

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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CONVERSION DEVICES, INC.

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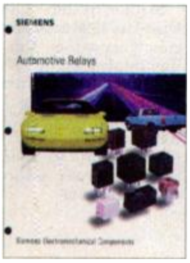

CIRCLE 304

SIEMENS ELECTROMECHANICAL

NEW SHORT FORM CATALOG

Omron's Control Components Short Form Catalog contains 200-plus pages of relays, switches, photomicrosensors, card readers, photoelectric sensors, power supplies, totalizers, digital displays, temperature controllers and timers. Call 1-800-55-OMRON. E-mail: SFC2_EDLit@omron.com

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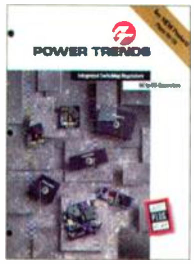
OMRON ELECTRONICS, INC.

NEW SWITCHING REGULATORS

Power Trends, Inc. has released a new 80 page full-line catalog for its complete line of Integrated Switching Regulators and DC to DC converters. the catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product along with mechanical configuration options and ordering information.



CIRCLE 306

POWER TRENDS, INC.

PRECISION SWITCH FOR APPLICATIONS

New Catalog 106 has 80 pages featuring new sealed snap-in rockers and toggles with available illuminated indication, plus an in-depth line of precision pushbutton, toggle, rocker, limit and basic switches. Sealed and unsealed construction. Industrial, commercial and military grades. Environment-free sealed. Sub-subminiature, subminiature, miniature and standard sizes.

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OTTO CONTROL

Partnership Innovation Technology

Techron's medical products brochure provides information about the companies capabilities as a supplier of gradient amplifier systems. Two new companion data sheets list specifications for the TEC7782 gradient amplifier and 8700 gradient amplifier systems. For information visit our web site at www.techron-amps.com, call: 219-294-8300 or e-mail to techron@crownintl.com.

CIRCLE 308

TECHRON

1998 Instrumentation Catalogue

The National Instruments 1998 Catalogue features hundreds of products for computer-based measurement and automation. Some of the new products in the 1998 Catalogue include our new PCI line of PCI-based modular instrumentation products, the latest version of LabVIEW graphical programming software, and our IMAQ imaging and analysis software and hardware.

CIRCLE 309

NATIONAL INSTRUMENTS

FREE EDA CD-ROM

OrCAD's new Desktop Solutions CD includes product overview, detailed data sheets and working demo versions of OrCAD's 32-bit Windows software- including new OrCAD Express and Capture Enterprise Edition. Order today by calling 1-800-671-9505 or visit our website at www.orcad.com

CIRCLE 310

ORCAD

GPIB DATA SHEET

The 1997 GPIB for PCMCIA and ISA data sheets from INES, Inc., are packed with the necessary information to help determine what type of GPIB card is best suited for all applications.

CIRCLE 311

INES, INC.

PLUG-N-PLAY CONTROLLER

Fairchild Semiconductor unveils a versatile Plug-n-Play controller that also supports Non-Plug-n-Play platforms like Windows-NT, DOS, Windows 3.1, UNIX, Novell and others. The NM95MS18 is the first PnP controller to allow several cards to share a single interrupt channel, consistent with the PC' 97 recommendations laid out by Microsoft Corporation. For more information and samples, call 1-800-272-9959

CIRCLE 312

FAIRCHILD SEMICONDUCTOR

APPLICATION SPECIFIC INTERCONNECT GUIDE

Samtec's Application Specific Product Group can quickly design modified and custom interconnects. This guide provides an overview of the capabilities, including contact and pin modifications, modified & custom insulator bodies& special services such as custom plating and packaging, and shows an extensive array of example interconnects. For information call 1-800-SAMTEC9. Fax: (812) 948-5047

CIRCLE 313

SAMTEC INC.

TRANSFORMER CATALOG

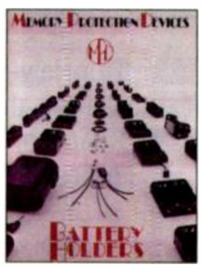
Signal Transformer Co., an operating unit of the Insilo Technologies Group, has just released a new 40-page, 4 color catalog that is an ideal reference source for engineers and buyers. signal Transformer offers the most extensive line of 50/60 Hz transformers available in a power range of 1 VA to 10 KVA.

CIRCLE 325

SIGNAL TRANSFORMER

BATTERY HOLDERS

Featured products: SMT button cell holders, battery snaps, case hardware, computer clock back-up holders, multi-cell holders with covers, auto cigarette lighter plugs. For computers, alarms, controls, instruments, toys, appliances, ect.



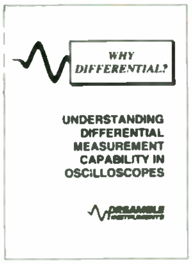
CIRCLE 315

MEMORY PROTECTION

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

DIFFERENTIAL MEASUREMENTS

A discussion of sing;e-ended and differential scope measurements on ground referenced and floating signals. differential amplifier characteristics such as common mode rejection ratio and commen mode range are covered. 1-800-376-7007



CIRCLE 316

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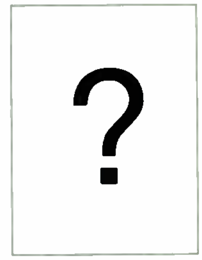

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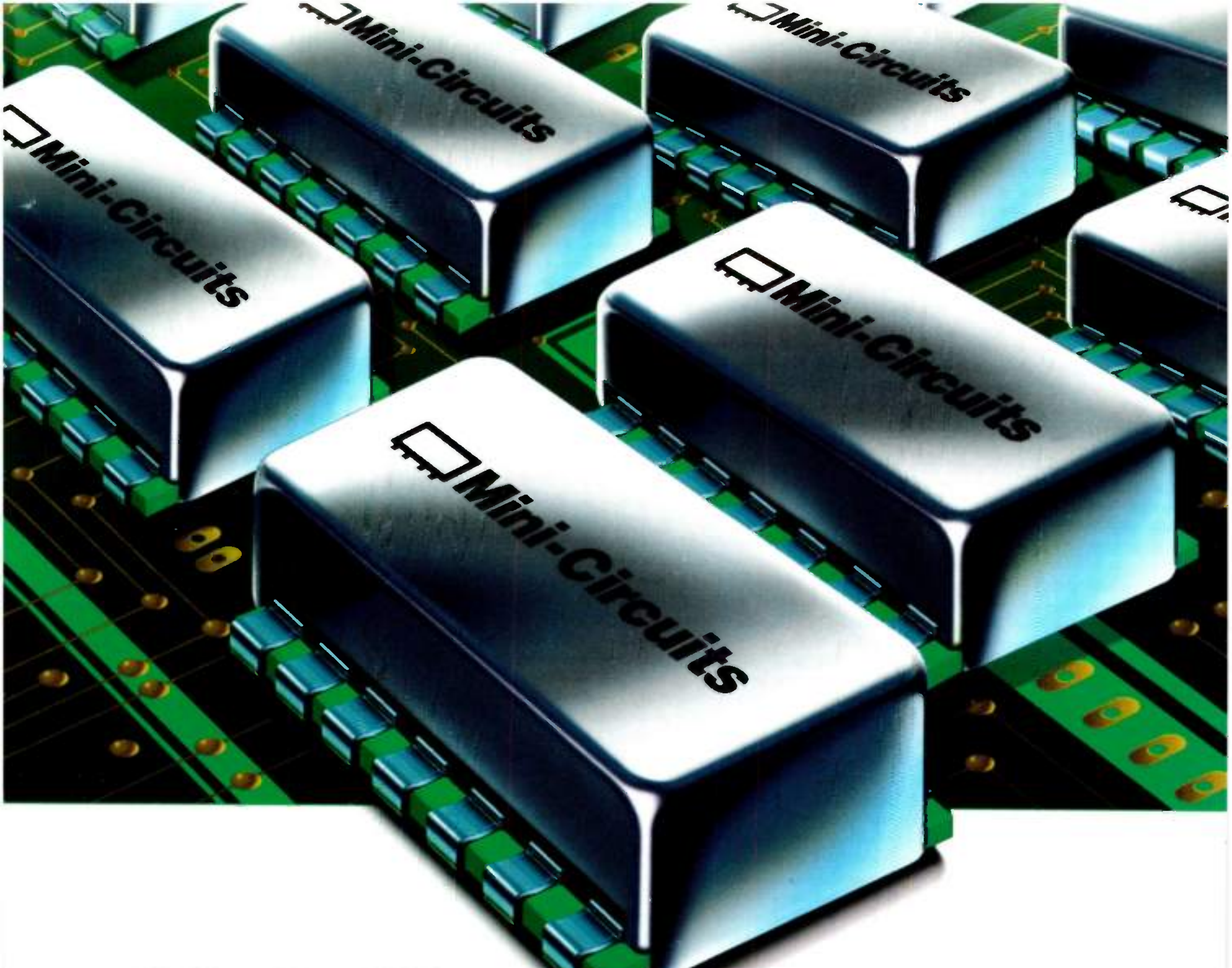

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