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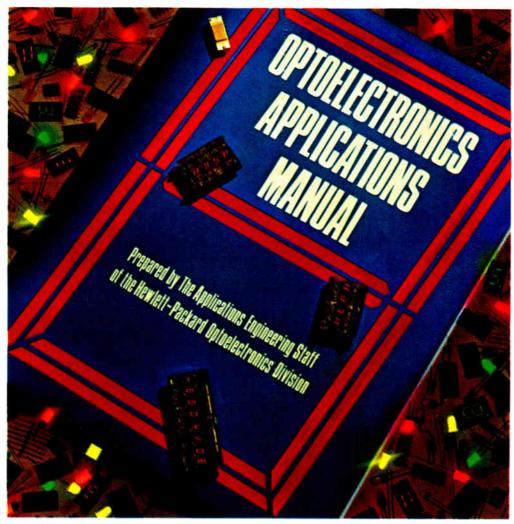
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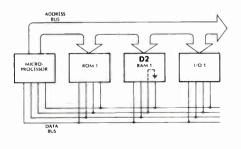
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Publisher's letter

The state of flux in the codec industry really became clear to Communications Editor Harvey Hindin when he was gathering the information for the summary chart of specifications shown on page 107. "The parameters quoted sometimes changed several times during the sixweek period I was getting them together," Hindin notes. "Many codecs are still developmental in nature and new versions and modifications are still being made.

"There's also the competitive pressure. As news breaks and people leak rumors and issue preliminary data sheets, others decide that they have to do as well or even better. It's like a market survey. Since some data, like power dissipation, is critical as far as telephone applications are concerned, no one wants to have the worst spec." But, Hindin asks, "How do you quote-conservatively? on the basis of how many samples and tests? And what supply voltage do you use and what temperature and what kind of operating conditions? Even though test procedures are usually well established, there's still room for variability in results."

To complicate matters, some reluctant companies submitted data after the deadline, and some were even too late to be included in the chart. And in other cases the manufacturers wouldn't release information at all. A few even went so far as to say they had never heard of codecs, and others wouldn't talk until they learned that the competition already had disclosed information. "It was a real chicken-and-egg situation. Rather than having a specific policy regarding release of

data, it seemed that all too often the policy was to act on the basis of what others were doing," says Hindin.

Hindin, who joined the staff of Electronics back in April, is not unacquainted with the vagaries of hightechnology companies. The 40-yearold editor, who holds BSEE and MSEE degrees from the Polytechnic Institute of Brooklyn (now New York). has worked at such companies as Sperry Gyroscope and Airborne Instrument Labs. He has also taught engineering science at the State University of New York at Stony Brook and is the author of 55 articles in refereed IEEE publications.

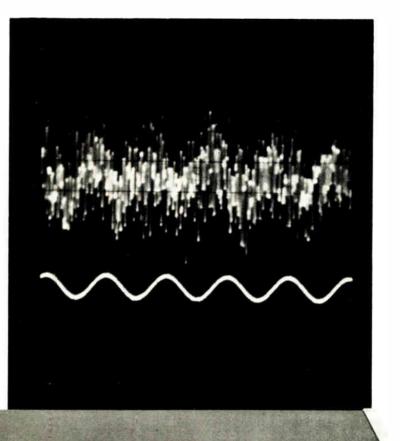
o paraphrase the TV commercial about the brokerage house, when Hewlett-Packard talks, everyone listens. So when the giant instrumentmaker turns out what Nick Pendergrass of its Loveland division calls "one of the most complex instruments ever built at the division," the rest of the world had better take notice. The product in question is the 3582 spectrum analyzer and, despite its complexity, development work was "surprisingly smooth," says Pendergrass, now a project manager. But it did take some time: the project was already under way when Pendergrass brought his expertise in digital signal processing (he has a doctorate from Cal-Berkeley) to HP in January 1976. For the results of the project, see the article on the 3582 on page 132.

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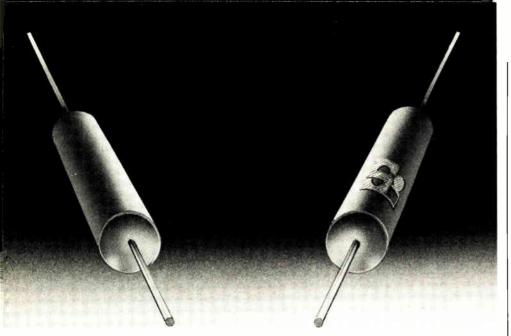
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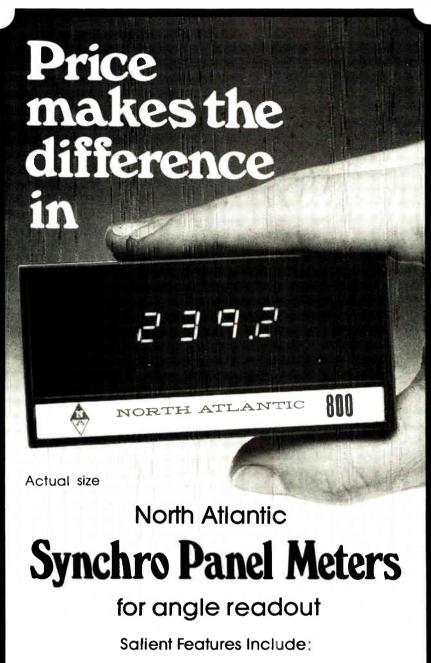


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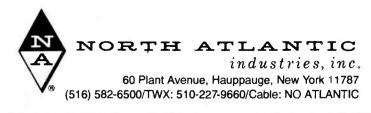
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News update

■ RCA Corp. is getting bullish on home computers, despite the prophecies of doom from several quarters. It plans to have two boards for its Video Interface Processor by mid-October—one that generates music and another that creates color video displays. The VIP computer, an outgrowth of the CDP1802 evaluation kit [*Electronics*, March 31, 1977, p. 94], was designed for hobbyists to create and play video games, generate graphics, and develop microprocessor control functions.

The VP-550 Super Sound Board will come with a computer program called PIN (for Play It Now) that permits users to easily transcribe sheet music or to compose their own music for playing on the VIP. The \$49 board generates a variety of sounds over a four-octave range, some of which resemble those of conventional musical instruments. Priced at \$69, the VP-590 Colorboard will allow the VIP to provide video displays in eight colors. A user can select one of three background colors for the display and then specify one of eight foreground colors for each of 64 areas on the screen.

■ The race to supply the U.S. Army's General Support Rocket System is heating up. Norden Systems of Norwalk, Conn., a division of United Technologies Corp., plans to deliver the first fire control system for Vought Corp.'s version of the rapid-fire artillery rocket system in late fall. Vought, which selected Norden to supply the system [*Electronics*, March 2, p. 84], heads a team that is pitted against a Boeing-Teledyne tandem.

Thus far, Norden has completed design of the fire control system and demonstrated a working brassboard. Norden also plans to deliver three additional GSRS systems in early 1979. The equipment will be tested in a series of competitive missile firings, operational tests, and environmental tests to determine who will win the prime contract to produce the rocket system, which is scheduled to enter service in the early 1980s. **Bruce LeBoss**

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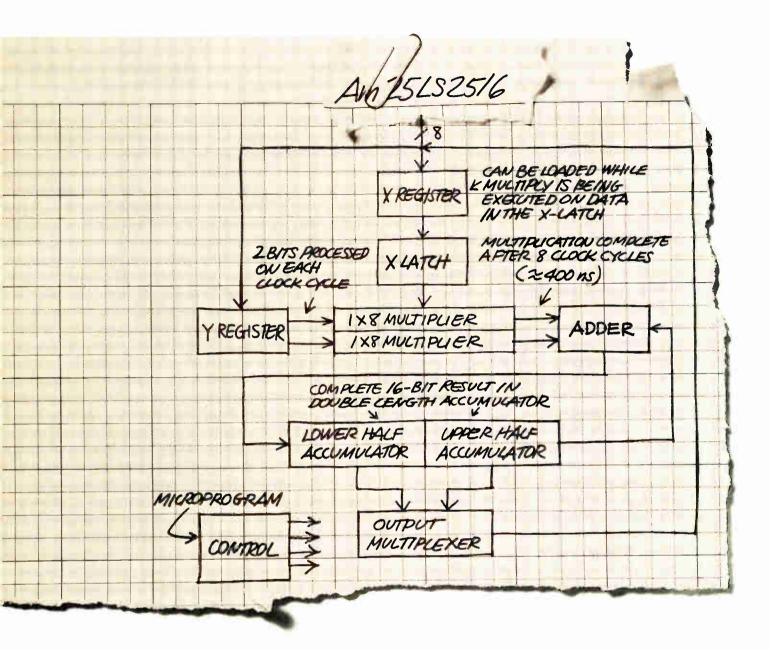
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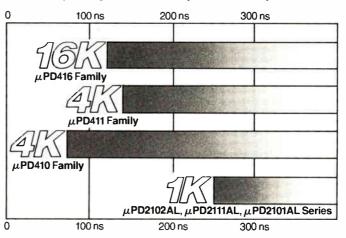
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P/N	^t RAC	^t RC	I _{DD1}	I _{DD2}
μΡ1)416-5 μΡ1)416-3 μΡ1)416-2 μΡ1)416-1 μΡ1)416	150 ns 200 ns 250 ns	375 ns 375 ns 430 ns	35 mA 35 mA 35 mA	1.5 mA 1.5 mA 1.5 mA
	$t_a = 0$	PC to + 2	70°C	

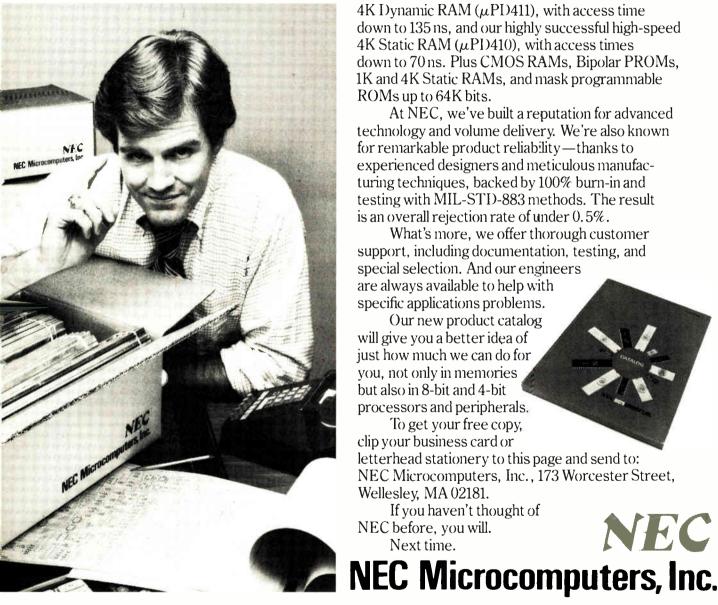
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Detailed information on the OPB 706 and OPB 707 reflective object sensors and other OPTRON optoelectronic products ... chips, discrete components, optically coupled isolators, and interrupter assemblies ... is available from your nearest OPTRON sales representative or the factory direct.



People

Cochran seeks standard digital recorder approach

Trade secrets are usually exchanged under the table. So why is Leroy C. Cochran broadcasting the fact that he is giving them away?

Because he is not talking just for his own benefit. The new general manager for audio products at Ampex Corp. in Redwood City, Calif., is willing to disclose proprietary techniques in the hope of spurring interest in a set of standards for digital audio-recording equipment. This new equipment area promises extreme noise immunity for broadcasters and recording houses.

"It's crucial that a sensible standard be adopted before we all go off and do things our own way," says the 39-year-old Cochran, who holds degrees in both electrical engineering and accounting and has spent the last 10 years specializing in accounting. "Unlike the mainframe computer industry, there is no single manufacturer who dominates the recording and broadcasting industry and whose recording scheme could become the tacit standard."

Revealing. What Cochran is doing is to reveal what would usually be considered sensitive and secret information at, for example, technical conferences, in the hope that others will see enough merit in the Ampex approach to copy it. "I've gone out on a limb already by detailing Ampex's method for editing digital recordings," Cochran says. "That scheme represents a lot of money's worth of research and analysis. But I would really hate to see a situation where a recording made on one manufacturer's machine could not be played on another's because of a lack of a standard.

The fight may be hard for Ampex. Another industry heavyweight, 3M Co., has already introduced a commercial digital recording system with its own recording format. At the same time, a second front is shaping up in the Far East, where Sony Corp. may be moving ahead with plans to market a commercial recorder that uses the same format



No secret. Ampex's Leroy Cochran hopes others will like his design enough to use it.

as its consumer digital recorder.

Cochran proposes a pair of standards: one for broadcasting and one for recording. "There are differences that need to be addressed," he explains, "the bit-rate and sampling frequencies for broadcasting must be consistent with efficient communications, whereas the standard for the recording industry must lend itself to maximum manipulation and creativity." Therefore, he thinks that the broadcast standard should have a faster bit rate than the recording industry standard.

Cochran, who joined Ampex in 1973 and now moves up from being controller of his division, sees second-generation prices dropping an order of magnitude from the present \$250,000 within three to five years. As would be expected, the firstgeneration gear is likely to be grabbed by the major broadcasting networks and recording houses. However, Cochran says some of the smaller independents may buy some just for the "notoriety."

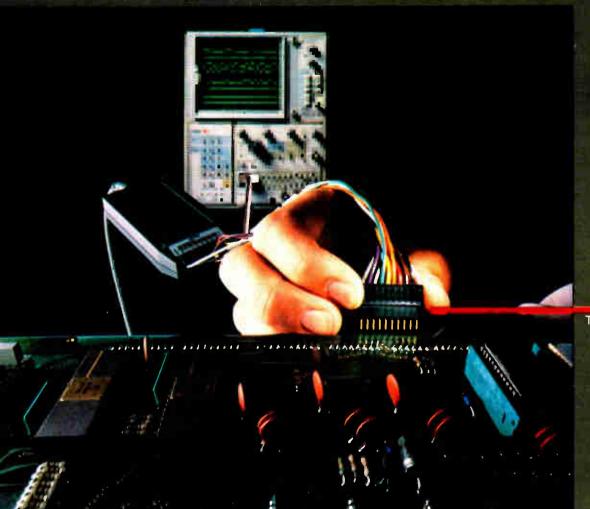
Swystun likes what he sees

in I²L and n-channel codecs

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THE VERSATILE ONES

People

Swystun, 36, the new vice president of development for BNR Inc., has some very strong ideas about coderdecoders. He believes that integrated injection logic and n-channel metaloxide-semiconductor technologies look best right now for codecs.

"I²L should be able to give the chip size you need as well as the speed," he says. "But n-channel is *the* technology. It's good for dynamic and static parts." Furthermore, "the vLSI thrust will produce the needed cost reduction. That will happen. There's no doubt about that at all." (Others disagree. (See story on p. 105). Swystun and his new employer, which is a wholly owned subsidiary



Once you've got your equipment designed, there's always the problem of what to do for an enclosure. You want to be sure that it gets just the right degree of protection and just the right degree of impressiveness at just the right price.

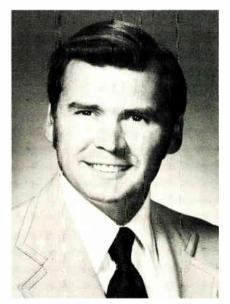
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View. Low power really means little in present codecs, says Gene Swystun.

of Bell-Northern Research Ltd., the jointly owned research arm of Northern Telecom Ltd. and Bell Canada, the Canadian phone company, are evaluating codecs from four chipmakers, he says. With a Ph.D. in electrical engineering, he formerly was director of advanced developments at Signetics Corp., which is developing an 1²L codec. Before that he was director of memory engineering at American Microsystems Inc. Altogether, he spent about seven years designing and developing semiconductors.

From where he sits, he sees a "critical mass of effort" being put into $1^{2}L$ and n-channel technologies. He does not see nearly the same amount of effort going into another codec contender—complementary MOS—and so tends to discount it.

"C-MOS is a candidate, but the penalty you pay is extra size," he declares. "There's no advantage to the low power consumption that C-MOS offers you in a codec. The edge is with n-channel because it's smaller and cheaper." The low power advantage of C-MOS is useless because telecommunications systems still have a lot of transformers and transistor-transistor-logic parts. "Why reduce power when you have all that junk still hanging around there?" he asks.

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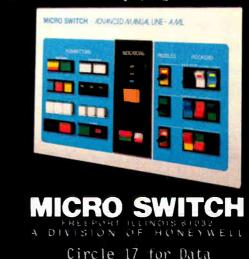
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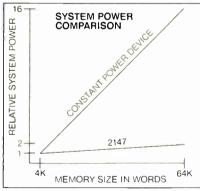
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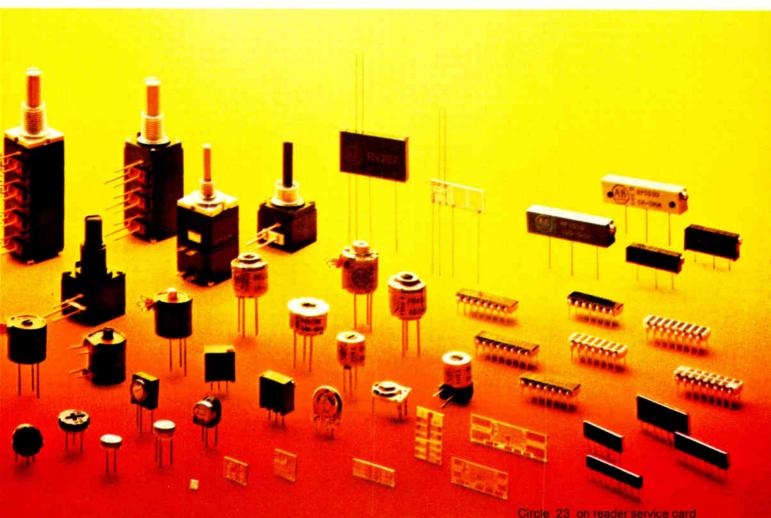
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Editorial

Will video-text systems travel well?

There is a sleeping giant lurking out there, and it would be well for Americans to start getting used to the idea that one day they may be asked to have it in their homes and offices. It goes by different names in different countries—the British call it Viewdata, the French have dubbed it Antiope, and, on this side of the Atlantic, the Canadians have yet to christen their upcoming system.

What all of them are is video-text information services, and the British and French, at least, are busily getting a jump on the rest of the world by industriously selling their approaches to other nations. The British Post Office to date has invested close to \$20 million in Viewdata and has sold the software—the guts of all the systems—to the West German and Dutch post offices. The French, who started later than the British and say that they therefore have benefited from their rivals' experience to produce a more flexible arrangement, are pushing to have Antiope adopted as the European standard teletext system.

All this is very well, but where does the U. S. — and, by the way, Japan — come into it? Right now, virtually nowhere. While it is possible to obtain some cable-television information about the stock market, weather, time, fruit and vegetable prices, and the like, such data presentation is archaic compared to video-text systems because the viewer cannot dial up for it.

Some watchers of the telecommunications industry are beginning to wonder nervously about the absence of technology giants like America and Japan, particularly now that Canada, too, has announced that it will dip its toe into the water next year with a pilot link using telephone lines. AT&T says it has no present plans to test such a system; it may be presumed that the Japanese, a people whose keen interest in mass circulation of facts has made facsimile a commonplace, are watching developments and seriously considering the options available to domestic telecommunications companies.

But does Ma Bell know something about the American market that the others don't? It is within the realm of possibility that Americans are getting just a bit oversold on and underinterested in magical technological systems for the home. Take, for example, video cassette recorders: sales this year will reach about two thirds of what was predicted — 500,000 units versus 750,00 — though the industry is hopeful that things will improve. Even video games seem to have settled quietly into a post-shakeout mode. And all the *Brave New World*-ish talk about home computers is little more than just that — talk.

The big question, then, revolves around the mood of the American consumer, the condition of the dollar, and inflation. Just how anxious is the average person to dial up for news, advertisements, and the like, most of which are found on commercial TV? Will Bell take the plunge, or will it be left for some hardy telecommunications pioneers to hitch their wagons to the concept of video-text information services and ride off in search of fame and fortune? Or is it back to newspapers?

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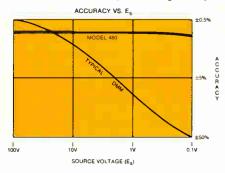
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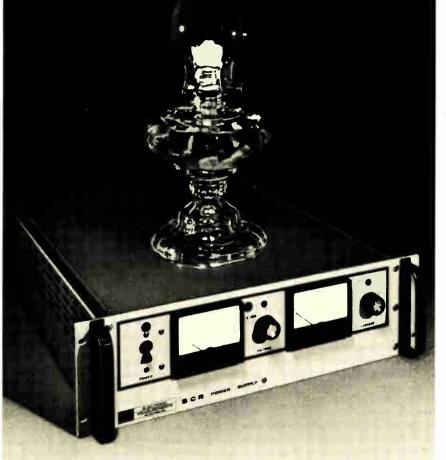
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Meetings

Eascon-Electronic and Aerospace Systems Convention, IEEE, Sheraton International Hotel, Arlington, Va., Sept. 24-27.

Distributed Data Processing, AIAA, Ramada Inn-Rosslyn, Washington, D. C., Sept. 25–26.

Convergence 78—International Conference on Automotive Electronics, Society of Automotive Engineers (Warrendale, Pa.), Hyatt Regency Hotel, Dearborn, Mich., Sept. 25-27.

ISHM 78, International Society for Hybrid Microelectronics (Montgomery, Ala.), Radisson Hotel, Minneapolis, Sept. 25–27.

International Electrical Electronics Conference and Exposition, IEEE, Automotive Building, Toronto, Sept. 26–28.

MEDE 78—Military Electronics Defense Exposition, Kiver Communications SA (Millbank House, Surbiton, Surrey, England), Rhein-Main Halle, Wiesbaden, West Germany, Oct. 4–6.

Land-Mobile Telecommunications Symposium, National Research Council (2100 C St. N.W.), Washington, D. C., Oct. 5.

ISA/78 International Conference and Exhibit, Instrument Society of America, Philadelphia Civic Center, Philadelphia, Oct. 15–19; with the Joint Automatic Control Conference, Oct. 18–20.

NCF-NEC/78—National Communications Forum and National Electronics Conference, National Engineering Consortium, Inc. (Oak Brook, Ill.), Hyatt Regency O'Hare Hotel, Chicago, Oct. 16–18.

1978 Design Automation Workshop, IEEE, Michigan State University, East Lansing, Mich., Oct. 18–21.

Engineering in Medicine and Biology, IEEE, Marriott Hotel, Atlanta, Oct. 21–25.

What the learning curve has done for Mostek's 16K RAM.

Learning curve experience has made Mostek the leader in dynamic RAM production, reliability and performance. Now, Mostek introduces the MK4116-2, industry's fastest

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MK4176-2	156KM	32045	-	Jumiy
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16K RAM, at just 150ns access time and 320ns cycle time.

The new 4116-2 offers all the features found in Mostek's industry standard 16K RAM family. In addition, for flexibility in system design, VBB power supply now operates over the range of -4.5 volts to -5.7volts allowing -5 volt operation with TTL, or -5.2 volt operation with ECC systems.

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AK4116-

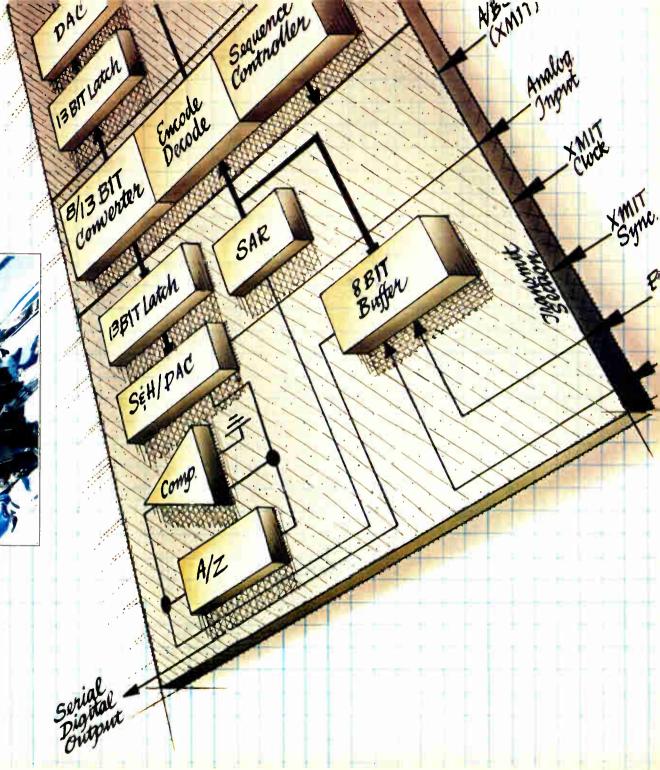


Electronics/September 14, 1978

tek's one-chip Codec inswer u NOS ţij Ē



A WAY



Designed to offer industry's lowest operating power, Mostek's new family of Codec integrated circuits is available now. This new CMOS family also features singlechip operation, a choice of 16 or 24-pin packages and a variety of on-chip functions.

30mW power dissipation

Operating power for Mostek's Codec family is a low 30mW (typ). Power supply operation of ±5V and the elimination of pull-up resistors through TTLcompatibility further enhance low power considerations. With the thousands of codecs required in applications like PCM Channel Banks and PBX Systems, the low power advantages of economy and reliability are essential.

Mostek's Codec family

	MK5150	MK5155	MK5116
Power (Active)	30mW typ	30mW typ	30mW typ
Pins	24	16	16
Туре	μ-Law	A-Law	#-Law
Full A/B Signalling	Yes	No	No
Asynchronous Operation	Yes	Yes	Yes
Supply Voltage	±5v	±5v	::5v
Reference Voltage	±2.5v	±2.5v	±2.5v
Signal to Quantizing Distortion @ 0dm0	40 dB typ	40 dB typ	40 dB typ
Idle Channel Noise	12 dBrn cO	-85 dBm Op	5 dBrn cO
Gain Tracking	±0.1 dB	±0.1 dB	±0.1 dB

It's easy to realize system savings with on-chip features like auto-zeroing, sample-and-hold capacitor and full A/B signalling. Operation is synchronous or asynchronous with serial data output of 128KHz-2.04MHz. Industry's smallest package Mostek's two newest codecs are available in space saving 16-pin packages. The MK5116 (µ-Law)

and the MK5155 (A-Law) meet domestic and international needs in applications like D3, T1 carrier, pair gain, PBX, C.O. and more. The 16-pin codecs-are especially suited for PBX applications that do not require signalling. To further reduce system complexity, compatible filters are coming soon

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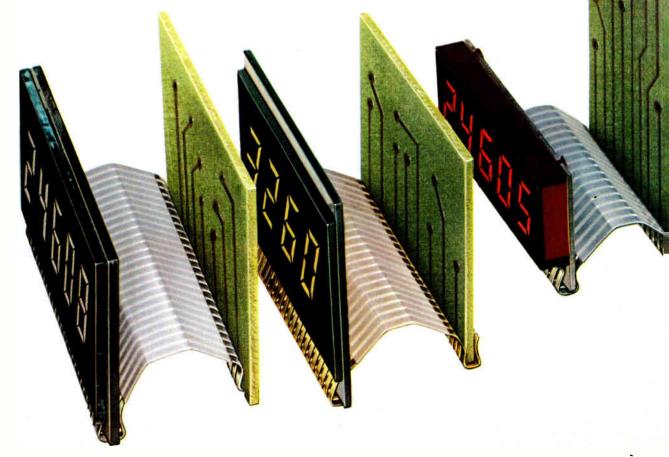
It's the reliable way to connect glass and ceramic substrate displays. By utilizing insulating film instead of molded housings, Laminar connectors eliminate mechanical stresses caused by display or housing warp. Each contact can track the display surface without applying any bending force, thereby reducing the likelihood of damage.

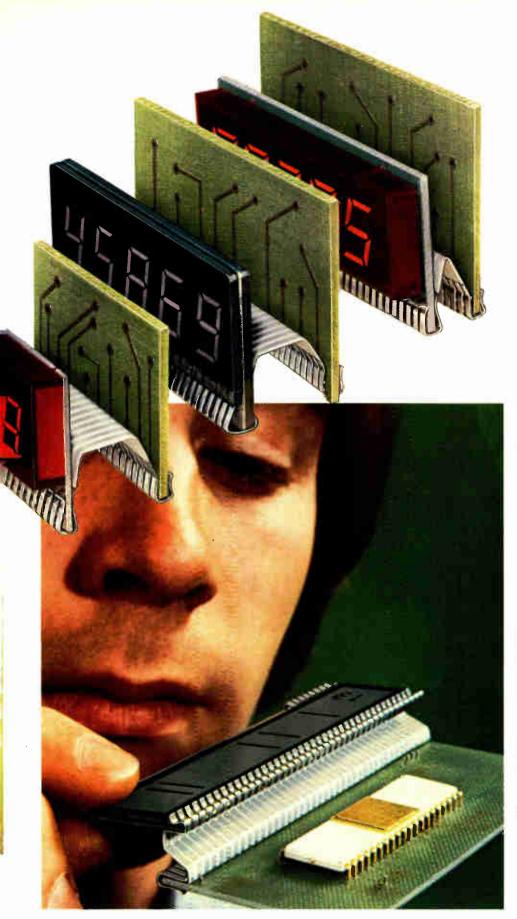
Laminar connectors match applications. There are clip-solder types for mounting angles of 0 to 90 degrees and clip-to-clip types for popular contact centerlines and board thicknesses. With many hundreds of configurations available, you won't have to compromise your design to fit the connector.

Wherever you use them, Laminar connectors mean extra economy. Since conventional molded housings are not necessary, costs are substantially reduced. In addition, they are available with economical tin-plated, as well as gold-plated contacts. Laminar connectors also mean superior reliability. Because their contact design provides proper normal force to assure good electrical connection, even with the deposited circuitry on glass displays.

There are more good reasons why you should try the AMP Laminar System, not the least of which is AMP engineering service and support. It means over 2,000 scientists, engineers and aides around the world are available to help you. In production. In quality control. In prototype sampling. And wherever you need higher performance products and lower installed costs.

AMP Laminar connectors are already available in a broad variety of pre-formed shapes, and custom designs can be made to your special order. For complete information on the entire line, just call Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.



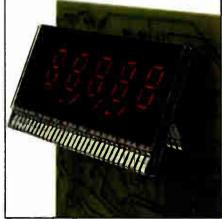


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Electronics newsletter

Hitachi working on plug-compatible EE-PROMs

American chip makers may have promised them, but it looks as if Hitachi Ltd. will be first to deliver EE-PROMS compatible with microprocessor systems. Already demonstrated in the lab is a 2,048-bit EE-PROM—electrically erasable programmable read-only memory—that has the attributes U. S. chip makers are looking for: single +5-v operation with E-PROM-compatible 25-v write and erase, blinding 100-ns access time, and a tiny cell size: 17.5 by 17 μ m. Next year, Hitachi plans to bring out a 16-K EE-PROM that, like its 16-K static random-access memory, is inter-changeable with the industry-standard 2716 E-PROM.

Intel produces one-chip fliter for codec

Already supplying customers with one-chip coder-decoders for the growing digital telecommunications market [*Electronics*, April 13, p. 77], Intel Corp. is now shipping monolithic filters made with n-channel MOS technology to customers (see p. 48). The 2912 pulse-code-modulation line device sits between the codec and the two-wire-four-wire hybrid, or subscriber-loop interface circuit (SLIC), which links the four-wire transmission circuitry to the two-wire connection to the telephone. The 16-pin 2912 has a transmitting filter with 50-Hz and 60-Hz rejection and a receiving filter, gain adjustment in both directions, and **compatibility with U. S. and European standards.** The Santa Clara, Calif., company claims low power consumption for the device: maximum ratings are 290 mW with an electronic SLIC, 440 mW with a hybrid, and 74 mW in power-down.

Codec from AMD to make debut Look for Advanced Micro Devices Inc. of Sunnyvale, Calif., to join the codec parade when it starts shipping samples of a two-chip codec within a month or two (see p. 105). "Our pin-programmable μ - or A-law codec is designed to handle two channels at a time," says Russ Apfel, linear systems and applications engineering manager. Both n-MOS and bipolar technologies are used. The n-MOS chip is 15,000 square mils and is made with five masks; the bipolar one measures 10,000 square mils and is made with seven masks. Both are in 24-pin packages.

Top IBM scientist asks for unregulated ACS service

In what is being viewed as a major policy statement, Lewis Branscomb, vice president and chief scientist at IBM Corp., has called for the deregulation of so-called value-added carriers. Specifically citing AT&T's recently proposed Advanced Communications Service [*Electronics*, Aug. 3, p. 79], Branscomb says the fact that Bell proposes to offer ACS over the existing regulated Data Phone Digital Service "indicates there is a line between regulated pure transmission services and value-added services. AT&T should be allowed to offer the value-added features of ACS on a competitive and unregulated basis." Branscomb was keynote speaker at the IEEE Compcon '78 fall meeting in Washington, D. C.

256-K bubble memory due from National

Not wanting to be left in the dust following announcements by Rockwell International Corp. (see p. 161) and Texas Instruments Inc. of 256-kilobit magnetic-bubble memories [*Electronics*, Aug. 17, p. 39], National Semiconductor Corp. is releasing details of its 256-kilobit part, due in sample quantities at the end of 1979. Called the NBM 2256, the 16-pin design follows current thinking in having a block-replicate approach with chevron patterns. But the part will have extra redundancy and an on-chip error

Electronics newsletter.

map to ensure 256 good loops of 1,024 bits each. Target specifications include $3-\mu m$ bubbles, access time of less than 7 ms, a shift rate of 100 kHz, and power dissipation of less than 1 w.

At the same time, Sperry Rand Corp.'s Sperry Univac division reports it has fabricated a 256- κ bubble-memory chip, housing a 2.7- μ m bubble. The chevron-shaped device will operate at 200 kHz and uses the blockreplicate architecture that greatly reduces memory cycle time over the major-minor-loop approach. The Blue Bell, Pa., computer maker is fabricating bubble devices to determine the architecture best suited for its purposes and to compare its costs and margins with what vendors offer. Sperry Univac is interested in bubbles for terminals, minicomputers, and communications processors.

HP pushes
GaAs FET into
18-to-26-GHz area
Hewlett-Packard Co. has raised the frequency ceiling on gallium-arsenide field-effect transistors to the K-band region of 18 to 26 GHz. Moreover, HP designers reported at this month's eighth European Microwave Conference in Paris that they believe that the 26-to-48-GHz band may be obtainable. The GaAs FET has a gain of 9.8 dB at 18 GHz and an extrapolated maximum frequency of 80 GHz in a broadband oscillator circuit. The 200-mw device is in pilot production in Santa Rosa, Calif., and is expected to offer a neat transistor solution to conventional circuitry built around Impatt or Gunn diodes for such applications as microwave sweep oscillators and signal generators. The device is made with silicon ion-implanted into a GaAs substrate to form both the channel and n⁺ contact layer.

New top capacity coming from CDC in large disks Using an enhanced version of what is frequently called IBM 3350-type technology, Control Data Corp.'s peripherals operation in Minneapolis is readying for introduction this week a fixed-media hard-disk drive with a capacity of 635 megabytes per spindle. When marketed as an IBMcompatible drive, the unit will be configured to appear to the system as two logical volumes of 317.5 megabytes each—the largest capacity currently offered by IBM on its 3350s.

Work under way at GI on 1980 microcomputer microcomputer microcomputer associated chips. The Hicksville, N. Y., group expects a decision before year's end on one of several choices: strike out on its own development program for a multichip set, second-source another firm's multichip microcomputer but add a little extra, or either develop or second-source a single-chip microcomputer. The first is the least likely option, notes Frank Jelenko, marketing manager.

Computer scientists to view technology of the Chinese of the Chinese Republic of China to view chinese computer technology. At the invitation of China's engineering society, the Institute of Electronic and Electrical Engineers is coordinating the tour. Its leader is Merlin Smith of IBM Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y., and president of the IEEE Computer Society.

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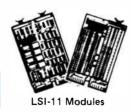
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Significant developments in technology and business

64-K RAM unveiled by U. S. chip maker outperforms 16-K units

Texas Instruments to offer samples in October for \$125; RAM operates from single 5-V supply, dissipates 3 μ W/bit

With other memory manufacturers expected soon to follow suit, Texas Instruments Inc. last week became the first U.S. chip maker to unveil a 64-K dynamic random-access memory. To be available in sample quantities at \$125 each in October, the new TMS 4164 is quite a performer, according to TI's specifications. It not only quadruples the density of the current generation of 16-K dynamic RAMS but it outperforms them in many important respects as well.

Perhaps most dramatic is the improvement in power dissipation. Operating from a single +5-volt supply, the new part dissipates only 200 milliwatts maximum, or 3 microwatts per bit. In contrast, TI's older 16-K device, the TMS 4116, uses three supplies (+5, -5, and +12 v) and dissipates more than twice as much power-462 mw, or 28 μ w per bit. Also improved are the access times, which range from 100 to 150 nanoseconds, and the minimum cycle times, which range from 250 down to 200 ns.

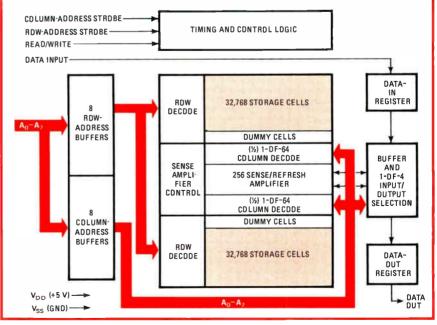
These parameters, coupled with a $64-\kappa$ -by-1-bit organization and a standard 16-pin package, make the part particularly well suited for use in minicomputers and mainframes. The potential for the part and others like it is enormous. Indeed, some industry analysts expect $64-\kappa$ dynamic RAM sales to reach 25% of the

predicted \$1 billion worldwide metal-oxide-semiconductor memory business by the early 1980s. As for TI, it "hopes to reach initial volume production levels of several thousand chips per month by the end of the first quarter of next year," says John Hewkin, strategic marketing manager for MOS memory in Houston.

Likely to follow soon with 64-K RAM announcements of their own are Motorola, Mostek, Intel, National Semiconductor, and Nippon Electric, Japan. The only semiconductor maker with a jump on TI is Fujitsu Ltd. of Japan, which announced its 64-K earlier this year and is now supplying samples. That memory, however, requires two power supplies +7 and -2 v. In achieving its single-supply operation, TI has made a significant development in MOS design. All 5-v MOS devices now on the market require a negative supply for reverse-biasing the substrate to make inputs and outputs compatible with transistor-transistor logic—onchip circuits called charge pumps generate the negative voltage. The new RAM, however, contains no onchip substrate-biasing circuit—TI designers have altogether eliminated the need for negative voltages.

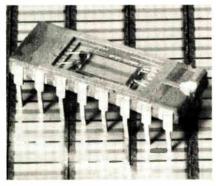
"Although it is TTL-compatible on the outside, the inside is geared more toward achieving an optimal speedpower product," says G. R. Mohan Rao, who headed the design team at TI.

He refuses to get more specific,



Twin arrays. Block diagram of TI's dynamic 64-K RAM shows it divided into two 32,768-bit storage areas. Cells are refreshed by 256 sense amplifiers every 4 milliseconds. The chip has no need for negative voltages, unlike current 4- and 16-K memories.

Electronics review



65,536 bits. Division of new RAM into two sections shows clearly in photo of 132-by-252-mil chip and its 16-pin package.

saying only, "People will be surprised when they see how we did it."

Long refresh period. In contrast to the 128-cycle/2-millisecond refresh used in current 4- κ and 16- κ dynamic RAM designs, the 4164 incorporates a 256-cycle/4-ms refresh period. This means that systems designed for the TI part can easily be modified to use 128-cycle 64- κ parts, should the upcoming parts be designed this way. But the reverse shift will not be possible.

"We saw no good reason to use a 128-cycle refresh," says John Hewkin. "The 256-cycle refresh period allows the same 64-kilohertz oscillator to be used when upgrading from the 16-K." Adds Rao, "The only savings [from using 128-cycle refresh] might be 1 bit in the row counter and multiplexer, but since these parts come in 4- and 8-bit multiples, no full packages can be dropped." And he asks, "When you sit down to design the 256-K RAM, how can you do it with 128-cycle refresh? It would take 1,024 more sense amplifiers."

Using only 256 sense amplifiers and scaled-down MOS n-channel double-level polysilicon-gate technology, TI has kept the bar size for the TMS 4164 down to 33,000 mil² (132 by 252 mils). "With 60% of the area taken up by the array, it's the first dynamic RAM not dominated by the peripheral circuitry," Rao says.

TI used test chips in parallel with computer-aided design to develop its design ideas. "The tricky part was to get 40 internal clocks on the chip to be timed together," Rao continues. "Using our approach, the major internal clocks are guaranteed not to have a timing skew—even if the row and column strobes from the user are nonperiodic." \Box

Fiber optics

Studio-quality TV looks OK in tests

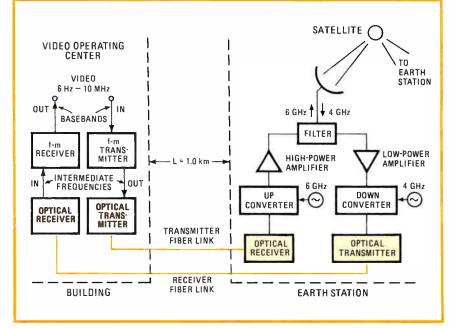
Tests of fiber-optic equipment carrying voice conversations are being carried out all over the country, mostly by telephone companies. But just how good is the gear for carrying television signals?

At Bell Laboratories in Holmdel, N. J., researchers Andres Albanese and Harry Lenzing are looking into this question, particularly whether fiber optics can carry studio-quality TV signals from a satellite earth station antenna to the video operating center that distributes the signals to individual receivers. With first test results starting to come in, the answer seems to be yes.

"We want to directly compare the capabilities of fiber optics and coaxial cable under the same set of conditions," says Albanese. "And we want information on transmission methods and picture-quality factors like signal-to-noise ratio, insertion loss, linearity requirements, and practical transmission distances."

Two systems. The fiber-coax comparison system links a 10-meter earth station antenna over a 1-kilometer run in Holmdel; it can handle both analog and digital signals. The coaxial cable and 12-fiber ribbon cable are laid side by side in a duct and have been functioning since last February. The fiber cable, made by Bell, is identical with the cable laid in a Chicago installation that has been successfully conveying telephone conversations for one year. A typical fiber has a core diameter of 55 micrometers, an outer diameter of 110 μ m, and a 0.23 numerical aperture and transmits light at 830 nanometers.

For most of the tests, the optical transmitter, shown in the figure, is modulated with a 70-megahertz intermediate-frequency signal that is frequency-modulated by the video signal. Results indicate that a color video channel can be transmitted with a 68-decibel signal-to-noise ratio, 0.1-dB differential gain, and 0.5° differential phase over a link 4.1 kilometers long. This well exceeds



Entrance link. Transmitter/receiver system in Bell's test can interchange the fiber-optics links (shown) with coaxial cable for comparing transmission and reception characteristics.

Computers

the noise figure for studio-quality requirements.

Frequency modulation at 70 MHz was chosen instead of other modulation techniques because it uses existing fm terminals and is compatible with existing radio equipment. Moreover, this fm technique relaxes the linearity requirement on the transmitter and receiver.

At the same time, the fiber-optic transmission line has been shown in the Bell tests to be superior to the coaxial cable in that no equalization circuits are needed and it is immune to electromagnetic interference. As an added and important bonus, the fiber cable is smaller than the coaxial cable and was easily run into an almost filled cable duct, into which more coax would not fit.

Supplemental tests. The 1-km link at Holmdel has been supplemented since July with a 0.5-km link at Bell's nearby Indian Hill site. The Indian Hill tests use only a fiberoptic link with a light-emitting-diode source whereas the Holmdel facility has both a diode and a laser, as well as the coax system. However, the new site will test more equipment combinations.

So far, results at Holmdel show a 25-dB link loss for the laser transmitter and 12 dB for the LED. For a signal-to-noise ratio of 68 dB and the fiber attenuation of 6 dB/km, the maximum link length is 4.1 km for the laser source and 2 km for the LED. But if the s/n ratio is lowered to 53, still a usable figure, the lengths are 6.3 km and 4.2 km, respectively. The s/n figure needed varies according to the system application and noise budget.

More work is planned in the coming months with different transmitters and receivers as well as modulation schemes at both sites. But for now, the Bell researchers are happy. Notes Albanese: "We have met the system objectives and feel optimistic. It's a matter of getting used to fibers—we had no unexpected problems." For example, the fiber-optic connectors developed in house by Bell proved as practical as commercial electrical connectors, he reports.

Air Force's SOS-based fault-tolerant unit going great, but budget bodes ill

There's both good news and bad news about the Air Force's faulttolerant spaceborne computer. On the plus side, researchers say they have whipped significant large-scaleintegration process problems, clearing the way to building the first working hardware.

No funds. However, "it looks like there's no money for prototypes until 1981," reports Capt. Roy L. Schmeising, who heads development for the service's Space and Missile Systems Organization in Los Angeles. Overall Samso budget pressures are the cause of the program stretch-out, he says.

The first LSI parts, logic circuits built of complementary metal oxide semiconductors on sapphire substrates are now being delivered by RCA Corp.'s Solid State Technology Center, Somerville, N. J. Others are expected from Hughes Aircraft Co.'s Microelectronic Products division, Newport Beach, Calif. The siliconon-sapphire structure was chosen because it is more resistant to radiation than circuitry on bulk silicon.

Started more than three years ago, the spaceborne computer is intended to be "self-healing" through an innovative architecture and system design, giving it up to five years of operating life. A selfhealing computer is one that can correct for failure of its components without outside help. Through a combination of architecture and software, the computer can switch automatically from a failed part to one that works, choosing from an array of standbys.

Customized. Rather than construct the central processing unit from a collection of standard logic chips, the Air Force partitioned its computer architecture to meet its self-healing requirement and then had each piece implemented in custom LSI chips. The result is some 22 types of chips, including a regis-

ter arithmetic/logic unit, a 1-K-byl-bit static random-access memory, a 2-K-by-4-bit read-only memory, and a ROM sequencer, to name the few standard kinds of chips. The other chips cannot be described so succinctly; because of the partitioning, they perform combinations of functions that are not standard.

The silicon-on-sapphire technology is deemed to be the only way to get radiation-resistant devices to survive space missions and to run at the needed rate of 200,000 operations per second. While the concept of the computer was proved in late 1977 by a brassboard model built with discrete parts by prime contractor Raytheon Co.'s Equipment division, Sudbury, Mass., none of the LSI chips have been built until now. Raytheon is proposing design simplification to reduce the 20 or so logic types to about 10.

The LSI devices have an average line width of 0.22 mil and between 2,500 and 3,000 devices per chip, with each chip measuring an average of 220 mils on a side, according to Arnold Van Doren, Raytheon's project manager. The chips have a speed of 7 nanoseconds per gate, he adds.

Survival. Completed, the computer is expected to occupy 1.3 cubic feet, weigh 50 pounds, and dissipate 35 watts. It will have a cycle time of 1 microsecond. Air Force studies estimate that continual reconfiguration to correct component failures will give a 95% chance of surviving a five-year mission. This compares with a 35% chance for three redundant computers and 44% for four machines.

Making the fabrication job rough is the number of pins required on some chip packages—up to 84 because of the complexity of providing interconnections between the working and backup modules. This number of leads is 20 more than the 64-pin packages now considered the

Electronics review

practical limit for production devices. "We tried configuring the computer with 64-pin packages, but ended up with more than 30 different logic types," Schmeising says.

With the first prototype chips in hand, "we have proved that C-MOS/SOS, which does not have a good reputation for driving a computer bus, can do the job." To reach its operating speed and throughput, the computer's logic circuits must drive a 700-to-1,000-picofarad bus capacitance, with a 100-ns rise time. "We got 60 ns at capacitance in the tests," he says.

Schmeising estimates that \$15 million to \$20 million is required to build prototypes for flight testing in the early 1980s. Even without full funding, a lower-level program is planned to push critical LSI work. By going ahead with device testing for radiation, reliability, and extended life, "we can refine out risks considerably in the meantime," he says.

Companies

GI to broaden its chip business

Having reached some significant milestones in the microcomputer and memory fields, General Instrument Corp.'s Microelectronics group in Hicksville, N. Y., is setting out on a new tack. Principally a supplier to

GI adds silicon-gate process for 64-K ROM

General Instrument Microelectronics not only is trying to shift its emphasis from consumer to nonconsumer markets but also is making a major change in process technology. In effect conceding that its traditional n-channel metal-gate process is not suited for building very dense read-only memories, the Hicksville, N. Y.-based group is going to a new silicon-gate process to fabricate its first 65,536-bit n-channel ROMs, due in sample quantities by January 1979.

Called the RO-3-9364, the edge-activated 64-K ROM will be pin-for-pincompatible with Mostek Corp.'s 24-pin MK36000 "in virtually every way," says Robert A. McDonald, general manager of GI's Industrial Business unit. A and B versions, having maximum access times of 850 and 450 nanoseconds, respectively, will list for \$10 to \$12 in lots of 1,000 and \$8 to \$10 at the 10,000-piece level. Meanwhile, a 9364C with a 350-ns access time will be priced at \$13 to \$14 and \$9.50 to \$11 in like quantities.

Having a chip area of about 38,000 square mils, the 9364 "is our initial push into high-density, silicon-gate n-channel ROMs," says McDonald. Right behind it will be a 28-pin edge-activated 64-K ROM, followed by 24- and 28-pin fully static 64-K ROMs, "all of which will hit the market by the first quarter of 1979," he adds.

There will be other new n-channel silicon-gate products, too, including an 8-bit microcomputer in late 1979. "These will basically be the same 8-bit parts we have now, but will take advantage of silicon-gate technology to offer bigger ROMs on board, faster speeds, and lower cost," McDonald says. Why go to silicon-gate processing now? McDonald answers, "We eventually would have had to do it for performance. We decided to bite the bullet now and use the 64-K ROM as the springboard for getting us into it."

producers of television and nonvideo games, as well as toys, the group is shifting its engineering resources toward nonconsumer markets that seem to offer even more lucrative business opportunities and greater stability.

"We are viewed as a manufacturer of large-scale integrated circuits for the consumer market, but we are beginning to see our niche defined more accurately by the words 'communication' and 'control,' " explains Edgar A. Sack, the senior vice president who runs the group.

Steady. "We are now beginning to deal with a different set of customers whose volume requirements are of higher orders of magnitude," says marketing manager Frank Jelenko. "Also," he continues, "they don't readily change designs from year to year, as do those in the games market." This means that engineering resources need not be expended annually to develop new software, he says.

Some of the non-game and nontoy applications for microcomputers and memories Jelenko identifies are in automobiles ("a few in the dashboard and a couple in the engine and elsewhere"), in digital tuning of radio and TV receivers, in ballasttype controls for lighting, and in

Widening. Though doing well selling their chips to toy and TV games makers, GI's Bob McDonald (seated) and Frank Jelenko are looking for other users—manufacturers of industrial controls and telecommunications.





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motor controls for air conditioners, refrigerators, and power tools. "These areas alone offer a potential market of 215 million microcomputers annually," he states.

However, GI is not about to abandon a good thing. It wants to expand it. GI shipped 1.1 million 16,384-bit read-only memories and more than 800,000 electrically alterable ROMs in its recent fiscal quarter ended Aug. 25. What's more, it shipped in excess of 100,000 8-bit microcomputers in August alone. In fact, "we will have shipped over 1 million single-chip 8-bit microcomputers in 1978," claims Robert A. McDonald, general manager for GI's Industrial Business unit, which encompasses microcomputers and memory.

Seasonal. McDonald notes that though the games market has served as "a good theater" for GI to introduce its microcomputers and provided the impetus behind getting the necessary design and production machinery in place, "it's not the kind of market we want to be dedicated to." A reason for this decision is that the games market is seasonal and "all visibility to the market is lost after Christmas," says Jelenko. Furthermore, "the games market has to be supported each year. . . . We will just spend a much smaller percentage of our engineering resources next year toward developing game software.'

An indication of GI's continuing commitment to the games market, Jelenko notes, is the planned introduction of the PIC 1655A, a singlechip 8-bit microcomputer with higher drive currents and lower cost than the existing 1655. It is designed to compete with 4-bit microcomputers, such as Texas Instruments Inc.'s TMS 1000, in toys and games using light-emitting-diode displays.

Samples of the 1655Å will be available in the fourth quarter of 1978, as will be samples of an 18-pin version of the 28-pin 1655. Called the PIC 1645, the latter will have less ROM (256 by 12 bits) than the 1655 and will be tailored for low-end motor-control applications. These will be followed in the first quarter of 1979 by the PIC 1670, which will have 1,024 lines of 12-bit ROM and 48 by 8 bits of random-access memory. The 1670 will be for high-end nonconsumer products and, Jelenko says, "allows us to do complex applications that we can't do with less ROM or RAM."

Military

Air Force wants more data on wind

The Air Force is going shopping for a system that will tell it more about the wind, especially in areas where it is difficult or impossible to place ground weather stations. This month the Electronic Systems division at Hanscom Air Force Base, Bedford, Mass., will ask for industry proposals to develop a wind-sounding system that will eventually go aboard both weather reconnaissance aircraft and cargo planes carrying troops and equipment to be dropped by parachute.

The system will use pressure, temperature, and humidity sensors in the parachute-borne radiosonde that will also carry an Omega navigation receiver to develop wind profiles between the plane that drops the sondes and the ground. Similar sensors have been used before by the National Oceanic and Atmospheric Administration to map winds. But they were sent aloft in balloons from ground weather stations.

Data produced by the NOAA radiosonde are usually telemetered to a large computer on the ground for data reduction. The Air Force, on the other hand, will put a minicomputer in the sonde-dropping aircraft to plot the wind profiles in real time. The plan is to put the system in 10 Military Airlift Command C-141 cargo ships and 20 Air Weather Service WC-130 weather reconnaissance planes.

MAC will use the system to calculate an optimum release point that considers wind direction and velocity changes for the aircraft that may follow. The Air Weather Service wants the wind-sounding system to better track hurricanes and typhoons, and to develop a better data base on wind speed and direction in areas such as the Western Pacific Ocean, where few ground weather stations exist.

Capt. William Bennett, manager for the wind-sounding program at the Electronic Systems division, says, "In combat drops, the C-141 equipped with the wind-sounding system goes in ahead of the strike force to show planes following where to drop." That is where the real-time requirement comes into play.

The wind-sounding program is in ESD's Global Atmospheric and Environmental Systems office. A typical combat airdrop mission would have an instrumented C-141 in the lead drop sondes at intervals as it approaches the target. The sensors, plus a small Omega receiver in each sonde, will get three signals every 10 seconds from the navigation-aid transmitters. The pressure, temperature, and humidity data will be telemetered with the Omega information over a band between 400 and 406 megahertz to a receiver aboard the mother ship.

There the data will be digitized and fed to the minicomputer that separates and processes the signals to provide the wind velocity, pressure, temperature, and humidity for display to an operator. The data is also printed out for later analysis on the ground, as well as used immediately to calculate the best release point for the mission.

Continuous position. The computer will use the phase data in the Omega signals to calculate the sonde's position continuously as it descends. That position is a function of the wind velocity and direction. Temperature, pressure, and humidity data assist here by reducing errors in determining the sonde's altitude. Bennett says the computer will probably be a 16-bit minicomputer with a memory of 32 kilobytes or less.

The development phase of the contract will call for two preproduction systems—one each for the C-141 and WC-130 aircraft. They will be very similar, Bennett says, except that the C-141 hardware will be

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Communications

SBS, facing legal snag, pushes on . . .

The future of Satellite Business Systems Corp. is up in the air because of a court battle regarding legality of its joint ownership by International Business Machines Corp., Communications Satellite Corp., and Aetna Life and Casualty Co.

Hearings. Ruling on a Justice Department challenge of the Federal Communications Commission decision that authorized the McLean, Va., firm to provide domestic satellite communications service, a U. S. appeals court late last month overturned the FCC authorization. The court said the FCC should have given more consideration to the antitrust questions and should have held hearings on those issues before granting a license to the company. The court's decision sends the case back to the FCC for such hearings.

The legal stumbling block comes a month after SBS reported the success of Project Prelude, a test of the technical feasibility and market potential of its planned service for integrated digital, voice, and television communications via satellite [*Electronics*, July 20, p. 48].

Despite the dispute over its ownership, SBS intends to continue installing equipment for a planned January 1981 opening. Although the company is disappointed, a spokesman says it does not expect the decision "to impede the establishment of our system."

Reconsideration. The question the FCC must reconsider is whether IBM and Comsat's partnership in SBS violates Section 7 of the Clayton Antitrust Act by lessening competi-

tion or creating a monopoly. Key is whether IBM and Comsat were likely to have entered the market separately. When it approved SBS in January 1977, the FCC said that the venture was not anticompetitive and that, even if it were, approval would be in the public interest because SBS would provide a service that could compete with AT&T.

Earlier this month, a spokesman for the commission's litigation division said it has not decided yet whether to appeal the decision or to accept it and hold the hearings.

If the FCC holds the hearings and finds SBS to be in violation of Section 7, it could cancel its license. But Calvert Crary, a litigation analyst at Bache Halsey Stuart Shields, New York, says, "A more likely outcome would be for the commission to decide after a hearing that SBS doesn't violate the statute. After all. the recent history of Section 7 in the courts indicates that it is violated only by the most blatant combinations, and I think a pretty radical change in the standard would be required before SBS could be considered in violation."

. . . as Sperry uses 5-m earth stations

While officials in Washington, D. C., play ping-pong with the fate of the planned Satellite Business System, one independent manufacturer has gone ahead and developed its own satellite communications network for the computer-to-computer transfer of data. Established by Sperry Rand Corp.'s Sperry Univac division in Blue Bell, Pa., the network is the first commercially licensed system for all-digital twoway transmission in the C band (6 gigahertz up, 4 GHz down) to use 5-meter-diameter antennas.

Provided by American Satellite Corp. of Germantown, Md., and linked to the Westar I synchronous satellite, the network's hardware currently consists of two earth stations—one each at development centers in Blue Bell and Roseville, Minn. Other earth stations are projected for installation at Univac centers in Salt Lake City and in Irvine and Cupertino, Calif.

Applications. Large Univac Series 1100 computers at Roseville and smaller Series 90 computers at Blue Bell supply processing power for developmental groups using the network. Principal applications will be the transfer of data related to hardware design, software development and applications programs, and the exchange of manufacturing and financial information. The system will also be used for technical conferences via freeze-frame television and for high-speed facsimile. says Nate Pearlman, a Univac systems engineer.

"The key objective in establishing this new network is to optimize datacommunications control procedures and formats for use over dedicated satellite links," says R. C. Phillips, vice president of Univac's Major Systems division. Most computer communications protocols designed for use over old analog telephone links "can't be applied intact over satellite links," adds Pearlman. This is because the long propagation delay of satellite communications would make the system inefficient with respect to speed and error rates, among other factors, he explains.

Compensating. The effect of propagation delay, Pearlman says, can be offset by developing digitally controlled techniques that make more efficient use of the link's wide bandwidth, excellent reliability, and high signal-to-noise ratios. The Univac network has a present capacity of 112 kilobits/second and a bit-error rate of 2×10^{-8} , and this rate is "at least two orders of magnitude better than what we've experienced with the [Bell System's] Digital Data Service," he claims.

Using Univac's Universal Data Link Control, a bit-oriented, fullduplex protocol, Pearlman says, "we are provided with peak performance for a mixed satellite-terrestrial communications network." Further, because the system has but one voice channel for supervisory functions, extensive voice circuitry is elimi-

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Electronics review

nated and, Pearlman says, "the cost of a communications facility such as this is comparable to that of high-quality, terrestrial lines of equivalent bandwidth."

Codecs

Interface relies on bipolar technology

Although only the coder-decoder chip has been fabricated in silicon so far, Motorola Inc. has released details of a three-chip subscriberchannel unit aimed at the market for central-office and PABX digital switching.

But surprisingly, the Communications group in Phoenix, Ariz., which designed the unit, is prouder of its interface circuit, called the subscriber-loop interface circuit, or SLIC, than of the codec and filter chips. It believes the SLIC (or hybrid, in Bell System vernacular), which takes decoded analog signals from the filter chip and conditions them for driving the noisy telephone lines, will withstand extremely tough environmental conditions.

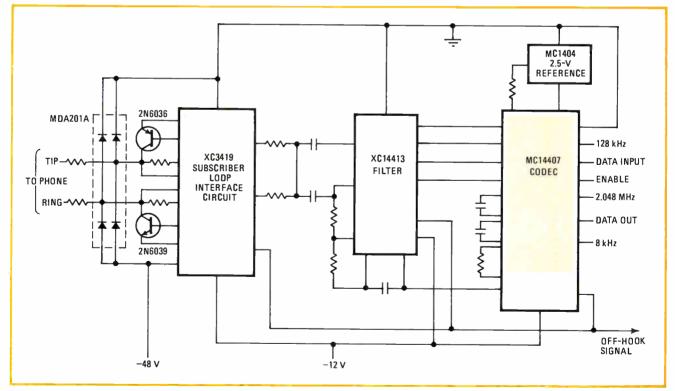
For example, the SLIC is specified to survive extreme voltages-like online transients as high as 1,500 volts caused by lightning-points out Steve Kelley, principal staff engineer for strategic marketing and product development at Motorola. Moreover, the chip must be powered by the 48-volt dc telephone line drive and be so well protected against 60-hertz signals that it can survive when it is inadvertently connected to the 120-v ac household line voltage. Technically, the SLIC, dubbed the XC3419 by Motorola, converts two-line differential talk-and-listen signals to four single-ended lines, generates the offhook signal, and provides line current to the telephone.

Tough technology. The SLIC is built with bipolar technology because MOS devices cannot withstand such extreme voltages, Kelley explains. As extra protection, Motorola adds transient-suppressing diodes to the chip, which must take a momentary surge of 50 amperes. A pair of power transistors is also added to supply the short-circuit current drive, which is 120 milliamperes in the worst case—too much power for an integrated circuit to dissipate.

Although Motorola uses bipolar technology for the SLIC, it builds its codec and filter chips with complementary-metal-oxide-semiconductor technology. Many manufacturers lean toward a similar three-chip approach, though the choices encompass n-channel and complementary MOS and bipolar.

C-MOS decisions. Motorola says it took a good long look at the various technologies it could have used for the codec and filter—and saw bipolar technology as a close contender before settling on C-MOS. "We never considered n-channel MOS, because C-MOS alone best serves all the various circuit functions needed in a codec and filter. C-MOS builds a better op amp; n-MOS, without active loads, can't give you as much gain, so you need more stages, and the resulting three-pole roll-offs are difficult to compensate," Kelley says.

The main reason for choosing



Trio. Motorola's three-chip subscriber channel unit uses C-MOS for its filter and codec and has a bipolar subscriber-loop interface circuit (SLIC). The SLIC's outboard components provide current drive for the telephone line and protect against transients.

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News briefs

Fairchild comes on FAST.

Fairchild Camera & Instrument Corp. will begin providing samples Oct. 1 of the first nine devices in a new digital logic family that combines the best of both Schottky worlds, high speed and low power. Called FAST (for Fairchild Advanced Schottky TTL), the family has typical gate delays of 3 nanoseconds and typical power consumption of 4 milliwatts per gate, about 25% that of conventional Schottky devices. Fairchild, in Mountain View, Calif., will announce later this year the introduction schedule for 57 members of the family, which is made with the company's established Isoplanar and Schottky technologies.

Hitachi to assemble RAMs in Texas

Hitachi Ltd. of Tokyo, is establishing a semiconductor manufacturing operation in Irving, Texas. To be called Hitachi Semiconductor America, the new company is expected to begin assembling metal-oxide-semiconductor memories next spring in an 11,000-square-foot plant now under construction.

LCDs predicted to take over as major display

Liquid-crystal displays will show a dramatic 25% compound annual growth through 1982, putting them in top position in the display industry by the mid-1980s, according to Creative Strategies International, a San Jose, Calif.-based research firm. Until that time, light-emitting diodes will remain as the display industry leader, primarily because of low prices and extensive use in consumer goods. Gas-discharge displays are expected to lose ground and end up third by 1982 in what will be a \$455 million worldwide optical-display market, but they will stay competitive in single-digit applications, with plasma panel displays a key growth area.

C-MOS, however, is low power consumption—the MC14407 codec and the XC14413 five-pole elliptic filter each draw less than 100 milliwatts and power down to less than 1 mw. Motorola has used that inherent quality of C-MOS to give its threechip system a telecommunications selling point—minimal power consumption when the phone is on the hook. Motorola's entire system, as it is now designed, will power down to less than 10 milliwatts—a tenth that of most other manufacturers' codecs alone.

Packaging & production

Varian machine slices 975 wafers at one go

There's more than one way to slice wafers from a silicon ingot. In the semiconductor industry, the wafers are usually cut with a diamondtipped blade that produces wafers up to 20 mils thick. However, the process wastes silicon because the kerf—the place where the cut is made—is wide. This wastage is one of the problems that researchers have begun to tackle at the Lexington (Mass.) Vacuum division of Varian Associates.

But Varian is not producing wafers for ordinary semiconductors. The division is funded by the Department of Energy to come up with cheaper methods of slicing wafers from silicon ingots for photovoltaic solar cells. The work is part of the low-cost solar array project administered for the DOE by the Jet Propulsion Laboratory, Pasadena, Calif.

Varian has developed a prototype machine that is expected to slice 975 wafers at a time. This is accomplished by widening the cutting head to handle ingots more than 19 inches wide, about a threefold increase. Moreover, the cutting head that holds each of the V_{4} -in.-high blades weighs about a ton—mostly because the blades must be held under a tension of about 200,000 pounds per square inch.

So far, the Varian machine's



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developers have sliced just two ingots, and these without too much success. But they are not at all fazed.

"We're as confident as we can be several years from the goal that we can meet the numbers DOE has set for us," says Robert G. Wolfson, manager for advanced materials at the division, which manufactures Czochralski crystal-pulling furnaces as well as wafering machines now used mainly to slice sapphire and quartz. From each cutting cycle, Varian must deliver 1,000 wafers that are 12 mils thick—with a kerf loss of just 6 mils-from a 4-in.diameter ingot at cutting rates of up to 9 millimeters per hour. By 1986, the cutting process should add no more than \$5.78 per square meter of silicon produced to the cost of the purchased ingot, taking into account material, labor, and equipment costs.

In contrast, a commercially available Varian wafering machine has cut 300 wafers per cycle. The kerf width was 10 mils for a 16-mil-thick wafer, and the cutting rate was 3.5 mm/hr. Wolfson says that works out to a cost for the cutting process of \$81.80 per square millimeter of silicon produced.

(Also funded by the DOE, Crystal Systems Inc., Salem, Mass., has cut silicon wafers 4 mils thick, with a 6-mil kerf, using a modified commercial machine from Varian and wires impregnated with diamonds on their cutting surfaces [*Electronics*, July 20, p. 44]. It is now working with a new slicing machine with 500 wires in a blade head that moves over the silicon.)

In the prototype machine, the secured ingot reciprocates back and forth over the 8-mil-thick carbonsteel blades. A silicon-carbide abrasive suspended in oil bathes the ingot and does the cutting.

Jonathan R. Fleming, project engineer for slicing equipment, says the first cut with the huge prototype produced no unbroken wafers because of problems, since solved, in evenly distributing the slurry and in applying the tension to the blades. The second cut resulted in a wafer yield between 40% and 50%, with 12-mil-thick wafers and 8-mil kerfs. Fleming says the yield would have been as high as 98%, except that many wafers broke after the cut because cement holding the ingot to the reciprocating head loosened. \Box

Microprocessors

AMD snubs Intel, chooses Zilog part

The race for dominance in the emerging 16-bit microprocessor market has hardly begun, but already things are heating up. Fueling the fire is an agreement signed last month between Advanced Micro Devices Inc. and Zilog Inc. The terms are for AMD to second-source Zilog's forthcoming Z8000 microprocessor and for the two to jointly develop a suite of peripheral devices under an exclusive five-year pact covering the U. S. market.

Industry marketers, who mostly refuse to go on the record, generally agree that the signing adds credibility to the Z8000 design. At the same time, one industry figure notes, the deal "takes luster away from the [Intel] 8086." After all, why should AMD, already a second source for Intel's 8048, 8080, and 8085 microprocessors, not line up behind the 8086, which is essentially compatible with the 8-bit products?

New line. "We can sell the Z8000 as a better part," answers Sven E. Simonsen, vice president and technical director for AMD in Sunnyvale, Calif. "It has up to 30% higher throughput at a lower clock rate, a more regular architecture, and a more powerful instruction set." Because the 8086 was made compatible with the 8080 family, it has limitations, he continues. "The 8086 is the end of a line—the Z8000 is the start of a new one. With the 8086, we could only compete on pricing and delivery."

The deal may also trigger some intense jockeying for second sourcing as other chip makers take turns lining up behind either of the two 16-bit machines. For example, Mostek Corp., which is a second source

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Electronics review

of Zilog's 8-bit Z80, is expected to cast its vote for a 16-bit microprocessor within the next 90 days. But with AMD's exclusive rights in the U. S., Mostek or anyone else would essentially have to pirate the part by designing a functionally compatible Z8000—a difficult task in view of the Z8000's complexity.

For Zilog, the deal allies it with an aggressive marketing organization of second-source products and furthers its intention of making the Z-bus, Zilog's bus protocol, the standard for 16-bit microprocessors, says Robert B. Field, vice president, marketing. Moreover, the Cupertino, Calif., company will continue the pressure by announcing "in the near future" second sources for the Z8000 in Europe and Japan as well as similar pacts for the Z8, a lower-end 8-bit microprocessor due out with the Z8000 [Electronics, Jan. 19, p. 42]. Field also hints that other deals may be coming for other Z8000-compatible devices.

Terms. Under the AMD-Zilog pact, AMD agrees to pay Zilog a \$200,000 "creativity fee" and develop an unspecified range of parts. In return, Zilog gives AMD the Z8000, a serial input/output device, a memorymanagement buffer, a parallel I/O chip, and a first-in-first-out memory buffer. AMD hopes to be providing samples of its Z8000 a few months after Zilog.

Because the next two years is a crucial design-in time for 16-bit devices, the joint effort will allow the two companies "to help each other to take as big a share of the market as we can," Simonsen says.

Although the 8086 is being shipped in small quantities, the Z8000 is not yet available. In fact, it has slipped its due date, and no samples are expected before December, according to Zilog. Simonsen acknowledges it is risky to second-source an unavailable part, but "it would be more risky and take more time if we were to develop our own versions of the 8086, for example."

Intel declines comment on the pact, but the industry expects a second source for the 8086 to materialize as early as next year.

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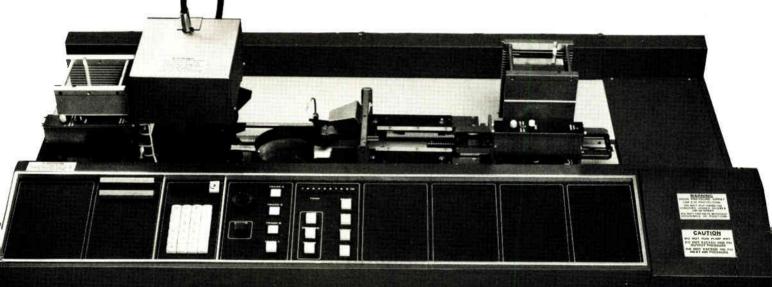
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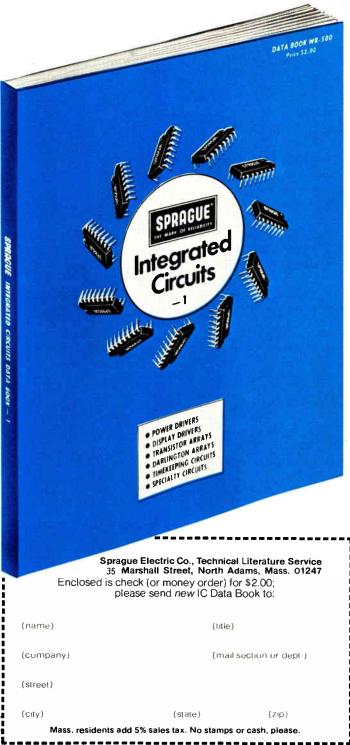
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Air Force awards Boeing \$129 million for B-52 digital avionics

By giving a \$129 million contract to Boeing Wichita Co., the Air Force has committed itself to full-scale development of a new digital Offensive Avionics System for its B-52G and H heavy bomber series. The OAS will control the Short-Range Attack Missile, the B-52's main armament, and the air-launched cruise missile now in development. Under the 36-month contract, Boeing will spend **two years equipping a B-52G test aircraft with the new avionics and the third year on flight tests.** The firm will use equipment provided by the Government, like the USAF strategic common doppler radar and Honeywell's Geans inertial navigation package, and has also picked the following subsystem contractors: IBM Federal Systems of Owego, N. Y., for avionics processors; Lear Siegler Instruments of Grand Rapids, Mich., for the attitude-heading reference system; Honeywell Avionics of Minneapolis for the radar altimeter; Sperry Flight Systems of Phoenix for controls and displays; and Norden Systems of Norwalk, Conn., for radar modifications.

Bendix gets \$2 million for microwave landing prototype from FAA

The Federal Aviation Administration is giving Bendix Corp. just under \$2 million for prototype development of the so-called "Basic Wide" microwave landing system to be used for precision all-weather approach and landing at large airports. Under the award, which runs about two years, the company's Baltimore-based Communications division will begin **delivering hardware in 10 months for installation and tests by the FAA next summer** at the National Aeronautics and Space Administration's test center in Wallops Island, Va. Texas Instruments, the other FAA-qualified competitor, initially entered the competition but did not remain in the bidding, an FAA official said. The MLS time-reference scanning-beam system developed by the U. S. and Australia was qualified as the next world standard this year by the International Civil Aviation Organization.

Japan still supplies 65% of U. S. color TV Imports

Imports accounted for nearly a quarter of the domestic supply of nearly 10.1 million color TV receivers in the U.S. market for the 12 months ended June, the first year in which Japanese exports were restrained by the Orderly Marketing Agreement. New Commerce Department data shows that nevertheless, out of nearly 2.5 million color TV imports, Japan shipped 1.63 million color receivers, or 65%. Taiwan was second with 458,000, followed by Korea with 182,000, Canada with 172,000, and Mexico with 22,600.

NBS seen blased In touting emi as 'pollution' problem

The electronics industries are unhappy about the National Bureau of Standards' publicity for its Nov. 2–3 Government, industry, and consumer conclave on electromagnetic interference—billed as "a major workshop on the growing problem of 'electromagnetic pollution.' "To be held at NBS's headquarters in Gaithersburg, Md., the meeting will deal with emi radiated by transportation, communications, medical, industrial and consumer products. Commerce Department sources say that a number of companies, which they decline to identify, have written Secretary Juanita Kreps and her staff challenging the validity and fairness of an NBS statement that reported "some observers believe emi may become one of the top environmental problems in the 1980s because of the proliferation of electronic products and components in American life."

Washington commentary.

The Pentagon's VHSI: will it fly in Monterey?

The newest piece of Pentagon jargon is VHSI, an abbreviation for the program in very-high-speed integration it will unveil Nov. 14 at Monterey, Calif. VHSI is likely to reverberate quickly up the peninsula into Silicon Valley when the microcircuit industry learns it is the name of the Defense Department's ambitious new six-year plan to spend an estimated \$200 million on advancing the state of the integrated-circuit art (see p. 81). It will differ from industrial VLSI efforts in emphasizing much higher speeds and uneconomically large die sizes.

Site of the unveiling will be Monterey's Del Monte Hyatt House, headquarters for the threeday Government Microcircuit Applications Conference sponsored by DOD, its military services, and the other Federal agencies that consider themselves heavily involved in high technology. Most semiconductor industry specialists have rated past Gomac gatherings as certainly informative, sometimes useful, but rarely profitable in terms of developing new business leads. This year, however, the VHSI premiere seems to guarantee that the conference will shed that not-for-profit, tutorial image.

Breakthroughs and breakdowns

In addition to DOD's detailed proposal on how to sponsor new breakthroughs in microcircuits, Gomac's audience will also get to hear a blistering critique of "the biggest single deficiency" in modernizing America's armed forces-the incredibly long and costly lead times between development of a technology and the delivery of production hardware to users. Leading his audience down that barrier-strewn pathway will be Rep. Richard Ichord, the plain-spoken Missouri Democrat who chairs the House Armed Services Committee's research and development subcommittee. Ichord's presentation will draw on the findings and present preliminary conclusions of an extensive investigation by his subcommittee that could prove newsworthy.

While Congressman Ichord's keynoter should appeal to the national interests of Gomac's audience, DOD's announcement of its major shift in policy on funding microcircuit technology is certain to generate major questions. Why is DOD reversing its *laissez-faire* approach to microcircuit development?

What each of the several different but equally

valid answers to the question have in common is economics. Or, more crudely, money. DOD has carefully monitored the hectic and expensive competition within the U.S. semiconductor industry during the past decade and a half. It has carefully plotted the advances in technology and noted that the rising U.S. curve is beginning to flatten out while other nations, capitalizing on prior American achievements, move to catch up.

Lack of capital

The pace of American technology has not slowed because it is running out of ideas but because it is short on investment capital in a high-risk market. The Pentagon has watched with quiet anxiety as America's most innovative microcircuit producers generally have remained unresponsive to the military's peculiar, lowvolume requirement, while cultivating larger, more responsive civilian markets. Military leaders believe they saw U.S. technological dominance eroding as manufacturers necessarily paused to profit from long production runs and recoup some of their heavy investments in capital equipment, rather than make existing hardware obsolete with more expensive innovation.

What appears to have broken the back of Government resistance to intervening in America's most successful example of a competitive free market at work, however, was the increasing number of capital-starved semiconductor manufacturers who turned to foreign sources.

Changes yet to come

Technological leadership is the keystone in the arch of U.S. defense policy. The eager response by foreign manufacturers to every opportunity to acquire American technology and access to its markets was more than policy makers could take. Thus the Government has responded through the Defense Department with its \$200 million program for developing the technology it calls VHSI.

There is no doubt that VHSI will influence the course of the American microcircuit industry. One clear consequence is that the Gomac-80 scheduled for Houston 26 months hence is sure to draw a record crowd. Beyond that, however, even Gomac's sophisticated audience can only guess at what other changes DOD's new market entry will bring. **Ray Connolly**

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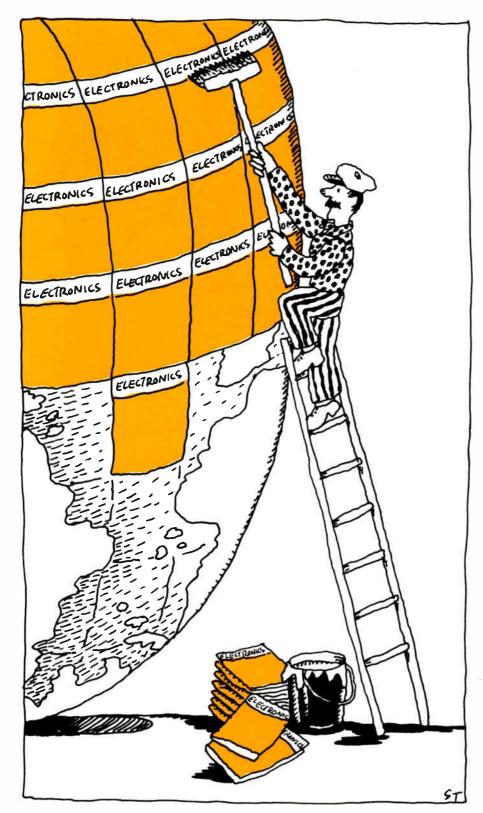
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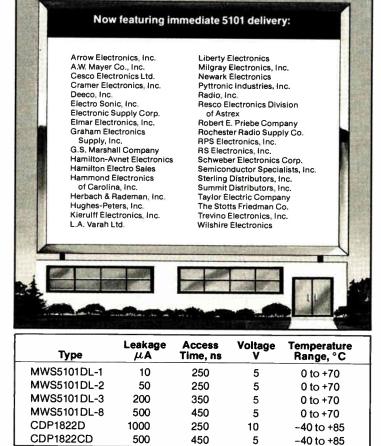
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Circle 62 on reader service card

International newsletter.

Japan's largest computer due at end of 1979

Deliveries of Japan's largest computer, the M-300H from Hitachi Ltd., will start in the fourth quarter of 1979 or first quarter of 1980. The new machine will be the largest so far of a line of software-compatible computers using completely different hardware and built by Hitachi and Fujitsu Ltd. with government financial aid. Hitachi claims that the average instruction execution time of its system will be 10% faster than that of the next largest machine in the line, Fujitsu's M-200-78 ns compared with 85 ns. It also claims that the M-200H is 1.7 times faster than IBM's top-of-the-line 3033.

The new computer will have bipolar emitter-coupled-logic circuits with 550 gates in its central processing unit and 16-K n-MOS dynamic randomaccess memories in its main memory. Main-memory size options range from 4 megabytes to 16 megabytes. Up to four CPUs may be used in multiprocessor arrangement, and Hitachi engineers say that the addition of an integrated-array processor to the CPU about quadruples its speed for complex scientific and technical computations. The company expects demand for 100 systems over five years, with rental starting at about \$190,000 a month.

Siemens spends \$250 million on two EDP plants

The drive of Siemens AG to become a bigger force in electronic data processing is shifting into high gear. The West German firm is spending \$250 million on a just-completed 115,000-square-meter facility and another of about 80,000 m² under construction. The outlay for the two Munich facilities amounts to **the biggest single investment the company has ever made**. As for its business, the Siemens Data Processing and Information Systems division did about \$600 million last year, and a 16% increase is expected in 1980. Even so the division will still be in the red, although it is West Germany's second biggest EDP supplier, commanding 20% of the computer market. IBM is first with 58% of the market.

Flat-screen display for Viewdata shows 960 characters

With an eye on the potential market for low-cost, portable business Viewdata terminals, General Electric Co. Ltd.'s Hirst Research Laboratory has developed a 960-character flat-screen display that accommodates a complete Viewdata/Teletext page. Based on dc electroluminescent technology, the display produces 24 lines of 40 bright yellow characters. Still **needed for the system and being developed by the** GEC **lab is an integrated-circuit display driver.**

Also under development is a 480-character display, and an 80-character module is now being evaluated by the British Post Office as a possible second source to the display made by Phosphor Products Ltd. for its automatic call-recording system. Meanwhile, Phosphor Products has received a contract from the Ministry of Defence to develop red, green, and blue dc electroluminescent displays in addition to the conventional yellow digits available.

Peripheral chips for microprocessors coming from NEC

Three LSI peripheral chips sought by users of microprocessors are about to become available simultaneously in Japan and the U.S. Nippon Electric Co. says it will ship samples of its μ PD765C programmable floppy-disk controller (see p. 202) and μ PD769C high-speed serial interface in October, and its μ PD3301C/D programmable cathode-ray-tube controller in November. All three parts will be available in production quantities in

International newsletter_

April. They are compatible with 8080 systems and also with NEC's μ COM1600 16-bit microprocessor. Using fine-pattern H-MOS technology, they will operate from a single + 5-v supply and use a high-frequency crystal for their clocks.

Thomson alms electronic PABX at low end Determined to become a factor in world PABX markets, the Société des Téléphones STE (Thomson Ericsson) has added two new and smaller electronic private automatic branch exchanges to the P line it launched last year. Thomson figures that the smaller of the two, the P10, could become a strong seller in the fast-growing low end of the market. Built around a Zilog Z80 microprocessor, the unit combines a switching circuit and an operator's console in a single cabinet about the same size as an oversized office typewriter. Capacity is up to six outside lines and up to 24 extensions. The unit, which offers most features of other electronic PABX systems, is highly modular.

 French working on 90-Mb/s
 At the behest of the government-run French telecommunications agency, Thomson-CSF has begun to develop what the two believe will be the fastest digital coaxial-cable telephone transmission system so far, one that operates at 900 Mb/s. Feasibility trials for the link are some 18 months off, but Thomson-CSF has already fabricated experimental versions of two crucial components for the system's repeaters. They are the comparator and signal regenerator circuits, both built around field-effect transistors integrated on gallium-arsenide chips to get switching speeds fast enough for 900-Mb/s transmission.

Sensor to enable Spacelab to study earth's surface Under contract to Bonn's ministry for research and technology, the West German aerospace firm Dornier System GmbH is working on a multimillion-dollar microwave measuring and remote sensing system that is to be tested during the first Spacelab mission. The system will be able to investigate the earth's surface in fine detail, whatever the weather and terrain, by using a side-looking radar. Sending out microwave pulses and measuring the radiation returned from the surface, the system will generate microwave pictures that give information on soil conditions, vegetation, harvest yields, and the like.

Addenda Now that they have designed a 1,024-bit static random-access memory that boasts 10-ns speed, engineers at Nippon Electric Co. are pushing into faster zones. Employing $3-\mu m$ design rules and positive photoresist with the company's diffusion self-aligned n-MOS technique, the designers are planning to use even finer lines to get faster devices... An experimental 13-bit monolithic analog-to-digital converter accurate to $\frac{1}{2}$ the least significant bit has been built by Matsushita Electric Industrial Co. It uses p-MOS analog switches in its sample-and-hold circuits, integrated injection logic, and two types of npn transistors; conversion time is 16 μ s. The devices are due at the end of next year... General Electric Co. Ltd. has followed its announcement of a silicon-on-sapphire capability with word that it is well advanced on a V-groove MOS process, selected for its high-voltage, high-current capability.



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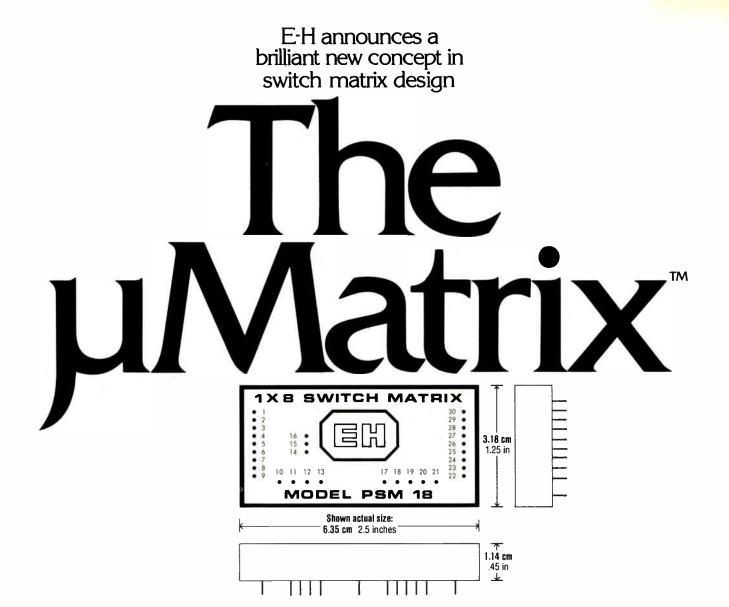
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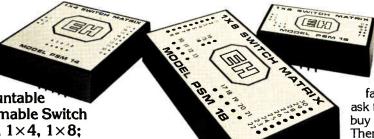
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Significant developments in technology and busines

Digital compensation technique in crystals yields ultrastability

Racal to develop IC version based on method developed at University of Bath that promises low production cost

By adopting a novel digital method of compensating for temperatureinduced frequency drifts in quartzcrystal frequency references, researchers at the University of Bath in England have achieved frequency stabilities of 5 parts in 10⁸ over a 40°C operating range. Only the best analog-compensated frequency references are as stable.

Moreover, the new technique has a tighter performance spread and promises lower production costs. It also rivals the stability of bottomrange oven-controlled crystals without high current drain or long warmup times.

According to Prof. William Gosling of the School of Electrical Engineering at Bath, the new crystal reference could be a key element in the development of future singlesideband mobile-radio receivers, where instant startup, low power consumption, controllable performance, and low production costs are all necessities. But the crystal reference could also find its way into instrumentation and distributed synchronous data nets.

IC coming. Now that the technique has proved feasible, Racal Dana Instruments Ltd. in Bracknell, Berks., is to develop an integratedcircuit version [*Electronics*, Aug. 31, p. 68]. If this succeeds, a cost-reduction program will aim at producing a frequency reference to be marketed alongside the company's range of oven-controlled crystals, says Keith P. Thrower, director of the Advanced Developments division.

Racal and the Science Research Council funded the work at Bath, and Racal holds patents on the technique. The decision to go ahead will depend on costs, says Thrower, who will be content to achieve initial accuracies of one part in 10⁷.

The technique rests on the use of two co-mounted crystals, one a conventional high-stability AT-cut and the second Y-cut to give it a large temperature coefficient of frequency. The two are in good thermal contact so that changes in the frequency of the Y-cut crystal can be used to represent the temperature of the crystal pair.

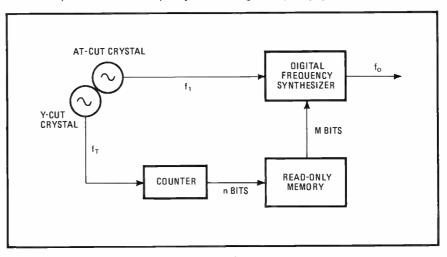
The high-stability crystal serves as a frequency reference in a phaselocked-loop frequency synthesizer capable of frequency increments of about 0.3 hertz over a range of about 75 Hz, sufficient to compensate for any likely frequency drifts over a 50°C range.

The frequency synthesizer output is adjusted by the second temperature-sensitive Y-cut crystal, whose output is counted against that of the high-stability AT crystal. The output word of the counter, held in a latch, represents the temperature of the crystal pair and is used to address a programmable read-only memory.

PROM data. The data stored in this 256-by-8-bit PROM corresponds to the temperature characteristics of the crystal pair employed. The output of the PROM is an 8-bit word, sufficient to define 256 frequency synthesizer increments. Thus, for each increment in the temperature register of the Y-cut crystal, the appropriate correction is made by an 8-bit-output word from this ROM.

Data stored in the PROM corre-

Cooperation. In a Bath University technique, two co-mounted quartz crystals, one with a high-stability cut and the other with a temperature-sensitive cut, work together to compensate for temperature-induced frequency drifts in a digital frequency synthesizer.



Electronics international

sponds only to that particular pair of crystals for which it was programmed. That, says researcher G. A. Warwick, is why an automatic programming system is a basic element in the concept. The circuit can then be calibrated rapidly on the production line, ensuring very high accuracies in the field. Warwick claims that individual testing and matching techniques are impossible with the rival analog temperaturecompensating techniques. Instead, he says, the manufacturer approximates a temperature-frequency curve for each crystal batch, so that there is a wide spread of the temperature coefficients resulting.

One big advantage of the automatic programming system for the Bath scheme is that no absolute measurement of temperature is required during cycling. All that is needed is in the dual-crystal setup to temperature-cycle the systems and load each read-only-memory address with the value that brings the actual frequency in line with the specified frequency.

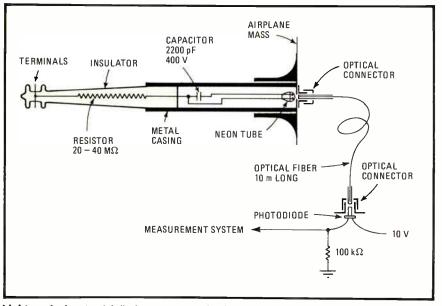
The technique developed at Bath University parallels work at the U.S. firm, Hewlett-Packard Co., which is using a single crystal made to vibrate in two modes simultaneously to produce temperaturestable and temperature-sensitive frequency pickups. But, says Gosling, this technique requires a complex crystal technology whereas the Bath approach uses well-proven crystalcutting techniques.

He says his technique could be reduced to two chips: one a custombuilt chip, the other a PROM, with a typical power consumption of around 30 milliwatts. It could provide an accurate frequency reference within 1 second of being switched on, as well as an excellent signalto-noise ratio.

France

Optical-fiber transmission featured in airborne current-measurement device

Flying over the wheat fields of France is a Falcon 10 business jet fitted out with a current-measuring device that transmits its digitized data over an optical fiber. The instrument easily outperforms air-



Light work. A potential discharger uses a circuit of a capacitor and a neon tube. The circuit discharges the potential and serves as an optoelectronic source at the same time.

borne devices employing the conventional measuring technique, says its developer, the government aerospace research outfit Onera.

Its function in the jet is to measure the current emitted by the discharge of electric potential. Such corona discharges can interfere with communications and navigation systems. Highly effective dischargers are needed, and accurate, rapid measurements of the currents they emit are necessary.

Parts. The experimental device from the Office National d'Etudes et de Recherches Aérospatiales is built around a neon tube intermittently illuminated as current is emitted, a Quartz et Silice QSF 600A monofiber, a photodiode, and a measuring system. There are no manufacturing plans afoot, but Onera does expect there will be commercial devices eventually.

The standard method of measuring the discharge is to isolate the discharger from the aircraft mass but connect it by an insulated wire to the measurement system and thus indirectly to the plane. Unfortunately, the wire can act as an antenna, picking up lots of interference. Moreover, if the data-collection system malfunctions, it may disconnect the discharger from the plane.

As the figure shows, the approach taken at the Onera laboratory in Chatillon is to make the discharger out of a ceramic capacitor in parallel with a miniature neon tube. This circuit converts the charge into optical digitized energy.

Discharge current passing through the capacitor increases the potential across its ends, causing the neon tube to light. As the tube lights, it discharges the current, and recharging begins. The process continues at a rate proportional to the current.

The neon tube acts as a light source for the 10-meter-long optical fiber, and its flashes are picked up by a photodiode at the end of the fiber. The diode is the front end of a preamplifier converting the light pulses representing the current into a digital format for transmission to the data-collection system.

The optical fiber is a good dielec-

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tric, guarding against the dangers of extremely high potentials. For example, it will protect the data-collection system against the high charges that may result from lightning strikes, says Pierre Durrenberger, an engineer on the project.

Less noise. Onera developed its transmission method as part of its program to reduce aircraft electrical noise. "We are aiming for an electrically clean aircraft," says Jean-Louis Boulay, an engineer at the Chatillon lab. The defense ministry backs its work, and Avions Marcel Dassault/Bréguet Aviation, the important military and civil aircraft maker that manufactures the Falcon 10, supplied the test plane and set up the discharger that it is carrying.

The Onera engineers envision an increasing role for optical fibers in all aspects of airborne data-transmission systems. "We will be using optical fibers, not only for protection systems, but also for functional devices such as control circuits," says Boulay. Work on such devices is also under way in the U. S.

One other application of the current-measuring device is under development. It will be used to detect dangerous levels of electrical charges in storage tanks containing explosive fuel or other chemicals. But this is only the beginning, say Onera engineers: many more applications are likely.

Japan

Directional couplers send TV signals down a single optical-fiber cable

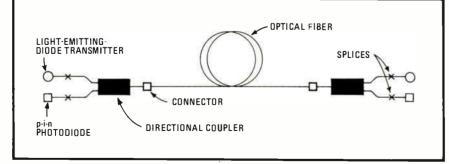
If optical fibers are to make it in show biz, then some way must be found to cut the costs of television transmission systems. Matsushita Electric Industrial Co. thinks it can do just this, with its experimental couplers for bidirectional TV transmission on a single optical fiber.

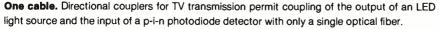
Engineers at Matsushita's Central Research Laboratories in Osaka have developed directional couplers that pass the output of a lightemitting-diode transmitter to the input of a p-i-n photodiode receiver over a single optical fiber. The directional couplers separate the transmit and receive channels by more than 44 decibels. Their loss is only 3.7 dB, including the 3 dB inherent in splitting the power equally among transmit and receive.

Operation. The directional coupler at the transmitter sends slightly less than half the power it receives down the line. The directional coupler at the receiver sends slightly less than half the incoming power to the photodiode, where it is detected.

The resulting system is flat within ± 0.5 dB over a frequency range extending from 20 hertz to 11 megahertz. Differential gain is less than 1%, differential phase is less than 1°, and sag is less than 2%.

For both transmit and receive, the largest source of interference is





reflection at the couplers from the opposite transmission direction. To reduce it as much as possible, Matsushita cuts the fiber ends at the directional couplers at an angle that causes most of the reflection to leak into the cladding. The company says that reflections are at most 0.05% of the transmitted signal, or 33 dB below the forward signal, and typically 0.03%, or more than 35 dB below. Reflections at splices measure less than 0.02%.

The components have not yet been translated into commercial products. Masakazu Fukai of the central labs says that such products are awaiting standardization among the fiber manufacturers because best results are obtained when the fibers in the components match those in the transmission lines.

Fibers. Typically, the experimental systems have used Nippon Sheet Glass Co. SI-100 optical fibers, which are of the type that has a step change in the index of refraction. Numerical aperture of these fibers is 0.27, core diameter is 100 micrometers, and cladding diameter is $150 \,\mu\text{m}$.

This optical cable is suitable for bidirectional circuits with 11-megahertz bandwidths and distances between repeaters of about 1 kilometer when used with an LED transmitter. Greater distances between repeaters are possible with higher-output LEDs or laser diodes.

In the experimental system, the light-emitting diode and p-i-n diode used in the transmitter and the receiver, respectively, have short lengths of optical fiber attached for best coupling to a transmission line. The actual output at the LED is 0.630 milliwatt; received power at the p-i-n diode is -24 dBm.

West Germany

Double-laser setup yields tiny scalpel

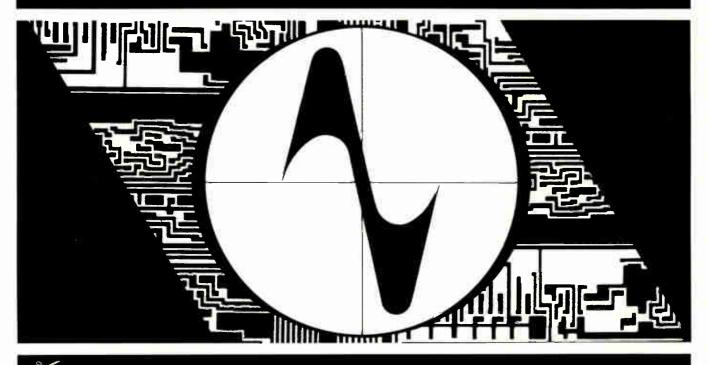
Neurobiologists have a new tool to work with: a laser beam used under a microscope as a scalpel. Research-

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ers at the Max Planck Institute for Psychiatry in Munich have already begun to apply this subminiature "cutting torch" to cell cultures of the nervous system grown outside the living organism. They have succeeded in severing minute extensions of living nerve cells without damaging the cells themselves.

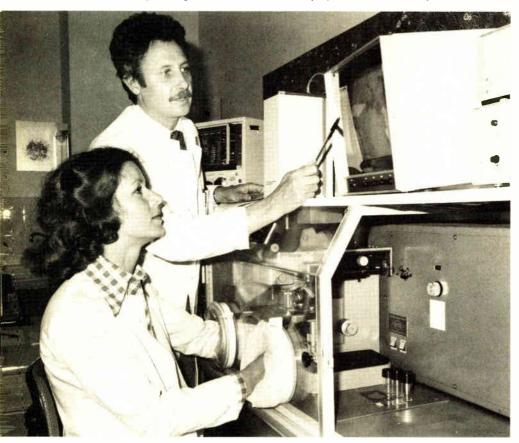
In the nervous system, axons, as these extensions are called, link one cell to another and transfer both electrical impulses and molecules between them. Finding out more about the transport of information over these intercellular communications networks is the ultimate aim of a group of institute researchers.

The precise microsurgery possible with the new laser microscope is already giving important clues to the regenerative ability of the intercellular networks. "We were able to cut the axons of individual cells by laser shots with high accuracy," says Ellen Rieske, a member of Georg Kreutzberg's group. "With mechanical means, such fine micromanipulations are impossible to perform without damaging or completely destroying the cell."

Two lasers. The new tool, developed at Munich-based Biotechnik GmbH, has two lasers whose light is colinearly fed into the microscope's lens system. One laser produces the cutting beam, and as many as 100 of its 8-nanosecond pulses of light may be fired in a second. This laser uses nitrogen as its active medium and generates light at a wavelength of 337.1 nanometers, in the invisible ultraviolet range. Its pulse output power may be set between 4 and 40 kilowatts.

The other laser, a helium-neon version, emits light in the red range. Its visible beam is used to steer the invisible cutting beam to its target. The light of the latter beam is deflected onto the object plane, where it is focused to a point less

Laser surgery. Neurobiologists Ellen Rieske and Georg Kreutzberg are looking at a monitor screen showing the target area of a laser microscope (in the sterilizable box).



than 1 micrometer in diameter. The red laser has a 632.8-nm wavelength and a 500-microwatt continuous output power.

Burn away. This focal point constitutes the "blade" of the laser scalpel, Rieske says. "Its power density gets up to 50 billion watts per square centimeter, high enough for biological material to evaporate instantly." By moving the microscope's stage relative to the laser focal point, minute operations on the cells can be performed. Ordinarily it takes but one laser shot to sever a cell's axon, she explains.

The microscope with its two lasers is contained in a box (see photograph) that can be sterilized to prevent contamination of the cell cultures. The temperature inside the box is a constant 36° C, which insures that heat will not expand the microscope's optical components and throw them out of alignment, impairing the laser's cutting accuracy. The cutting operations can be observed on a monitor by the researcher.

The institute's work thus far has shown that cells vary in their regenerative ability. Axons grow back to almost their original length within 3 to 12 hours, even after repeated severings. Cells with only two or three axons, called bi- or tripolar cells, regain almost their original shape. The group eventually hopes to find methods and substances that enhance and speed up the regenerative process.

More work. The Planck Institute specialists are also applying the laser microscope in another set of neurobiological experiments that they are carrying out with an American guest researcher, Guenter Gross. Usually, cells grow and interconnect in completely unpredictable fashion into highly complex networks, Rieske explains.

Such disorderly networks make investigating intercellular communications very difficult. "We are currently working on a technique to control the formation of cells and their axons by laser operations and thus to cultivate a two-dimensional model nervous system," she says.

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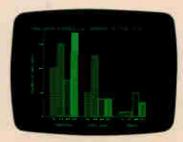
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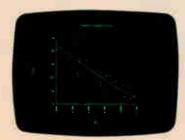
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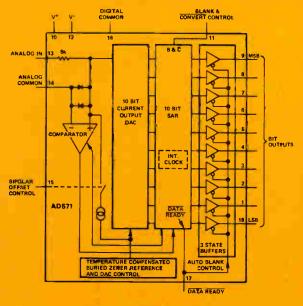
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For Technical Data circle #80 For Demonstration circle #81

Pentagon to fund major IC program

Six-year development of very-high-speed circuits with goal of increasing chip throughput 100 times could cost \$200 million

Troubled by intelligence estimates that other nations are rapidly eroding America's leadership in integrated circuits, the Department of Defense is moving to counter the challenge. After years of leaving IC development to the competitive marketplace, the Pentagon is executing an about-face with a six-year development program that industry leaders estimate will cost \$200 million. To be called VHSI-for very-highspeed integration-when it is launched in the fiscal 1979 year that begins Oct. 1, the program will involve all three military services, half a dozen of their newest weapons platforms, and all of the semiconductor companies that believe they can respond to the Defense Department's competitive goals.

For its investment the military expects to advance the technology of integrated circuits so that manufacturers can deliver circuits in production quantities—not just laboratory prototypes—that would measure 400 mils on a side and "provide 100 times the processing throughput of present ICs," says Larry W. Sumney, VHSI project leader. Sumney is a specialist for electronic devices and IC technology on the staff of the under secretary of defense for research and engineering.

Sumney and his boss, Leonard Weisberg, will unveil the VHSI program and goals on Nov. 14 at the Government Microcircuit Applications Conference near the heartland of America's semiconductor industry in Monterey, Calif. Weisberg is director of electronics and physical sciences in the office of Ruth M. Davis, deputy under secretary for research and advanced technology,

Application	Typical processing requirements (millions of instructions)	
	Current	Future
Weapons targeting control	0.1 - 1.0	10 - 100
Radar systems	1 - 10	100 — 500
Video / Imaging	10 - 20	200 - 1,000
Wideband data communications	10 - 30	500 - 2,000
Electronic warfare	25 - 100	1,000 - 10,000

by Ray Connolly, W	lashington bureau manager
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where the VHSI effort will be managed. Weisberg believes VHSI "can affect not only the future military capability of the United States but also the electronics industry."

Goals. While the Pentagon and the military services are still refining VHSI's technical goals and exact dollar requirements, its outlines are emerging. The program got its name, for example, because Defense officials want to stress speed over industry-oriented efforts to achieve density processing under very largescale-integration programs.

As for the competitive threat, classified intelligence data shows the U.S. technology lead has slipped from an estimated 5 to 10 years to 3 to 5 years and is continuing to diminish. However, the Defense Department declines to identify the direction of the threat on security grounds, even though industry sources are convinced that the VHSI effort is more a response to Japan's government-sponsored VLSI program [*Electronics*, June 9, 1977, p.99] than to any Soviet Bloc challenge.

But the Pentagon does admit it

can no longer remain aloof from the U.S. IC industry, using no more than 7% of its output, and waiting for reluctant manufacturers to qualify ICs to rigid military specifications and then produce a customized product in small quantities.

The VHSI program will move to focus industry interest on future military needs—and advance the state of the art—by establishing three committees reporting to a fourth overview committee headed by Sumney. The most important of the three will deal with VHSI delivery and have approximately half the program's budget to develop an industrial production capability for the circuits.

Feeding into this group will be a lithography committee, with an estimated 20% to 25% of the budget, to advance IC lithography beyond optical limits to submicrometer dimensions. Its emphasis will be on electron-beam or X-ray lithography "or some combination of the two," Sumney says, and perhaps deep ultraviolet technology.

The final feeder unit, with 25% to

Probing the news

30% of the program's fund, will be called DAST—for its mission of chip design, architecture, software, and testing. Each of the three committees reporting to Sumney will be headed by a representative of one of the three military services, he says, with the possibility of periodically rotating the chairmanships of the committees among the Air F orce, Army, and Navy.

Systems. In addition, each of the services will select at least two military systems areas at the start of the project for brassboard demonstrations of VHSI potential (see "Applications for very-high-speed ICs," p. 81). Ideally, Sumney says, a project's potential use of VHSI must be "essentially open-ended;" that is, capable of almost unlimited performance gains.

Of the two selected projects, he says, one will be used for "a shrink system demonstration" to show the advantages VHSI circuits can achieve through reduced size, weight, and power consumption. The second will be used to demonstrate a high-priority, highly advanced capability possible with one or more VHSI chips. Both approaches, to be funded separately as advanced technology demonstrations, will guide the eventual design of VHSI circuits.

The Pentagon's technical goals for deliverable circuits, while measured somewhat differently from industry's existing standards, are staggering. The product of the clock rate times the number of gates will be the overall figure of merit for VHSI devices, rather than the speed-power product, Sumney explains, since "in practice the power dissipation is roughly constant—realistically, less than 4 watts per square centimeter."

While specific numbers are still being massaged, the VHSI delivery committee and its subcontractors are expected to be charged with setting up in-plant pilot production lines capable of:

• Delivery of 1,000 2-megabit militarized random-access memories, with additional requirements for read-only memories, programmable logic arrays, and perhaps an analogto-digital converter.



Speedier electronics. The Pentagon's VHSI program would mean faster processing for radar, weapons control systems, and imaging systems aboard such craft as the F-16.

• Delivery of 1,000 specified militarized logic ICs with a clock period of at least 3×10^{12} times the number of gates. In bipolar technology, for example, this translates into 30,000 gates and a 200-megahertz clock, while the n-channel metaloxide-semiconductor goal would be 150,000 gates and a 30-MHz clock. Assuming appropriate memory, these figures "equate roughly to a processing throughput of 1 million instructions per second on a single chip," says the VHSI project office.

• Establishing a minimum-feature size of 0.5 micrometer, while escalating silicon chip sizes to 400 mils on a side. However, this goal will be approached cautiously with an interim milestone of 1.2 μ m compared to today's 2 to 5 μ m. All VHSI work will be done with silicon, Sumney says, although the Defense Advanced Research Projects Agency will continue to pursue its separate efforts with gallium arsenide, which could be ready for VHSI development in about three years.

• Delivering devices capable of mil spec performance, especially in the -55° C to $+125^{\circ}$ C range, with a failure rate equal to or less than 0.1% per thousand hours at 125°C. Offsetting these tough specs will be a softening of packaging requirements and elimination of a radiationhardening standard against nuclear blasts. The Defense Department will be satisfied if packaging comes up to "high-reliability commercial practice," while radiation-hard digital devices will not be required although technologies amenable to hardening will win a plus in proposal evaluations.

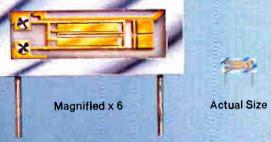
Backup. Critical to the VHSI delivery committee's achievement of these goals will be the feeder efforts of the support groups in advanced lithography and DAST, Sumney says. The lithographic unit will push for development of commercially available equipment with an alignment capability of 0.1 μ m in addition to a resolution of 0.5 μ m-both breakthroughs—plus a 15-minute exposure per 3-inch wafer or mask. However, it will support development of resists with at least three times present sensitivity levels that are capable of maintaining resolution under subsequent processing, and urge development of dry processing equipment for ICs to achieve high-yield precise resist removal.

Technical goals for the DAST committee will be equally challenging. It will be responsible for promoting commercial availability of hardware for automated chip testing; sponsoring new or improved chip architectures to minimize costly customization; developing on-chip test circuits and fault-tolerant designs, including redundancy; and pursuing parallel processing/multichannel architectures that would reduce random interconnects.

Orientation of the VHSI effort will be toward the single large chip, Sumney points out, since circuits on the same piece of silicon have obvious performance and life-cycle advantages over multiple chips that must be interconnected, making them vulnerable to malfunctions.

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Memories

Pinout standards causing grief

While rule for 32-K EPROMs appears settled with provisions for both one and two supplies, 64-K dynamic RAM knot is still tied

by Raymond P. Capece, Solid State Editor

That elusive ideal-standard pin designations in memory chips-is as slippery as ever, even though manufacturers and designers dread a repetition of the chaos that existed a few years ago in 4,096-bit dynamic random-access memories. While the dynamic RAM picture has settled down considerably, another new device-the 32,768-bit erasable programmable read-only memory-is causing paroxysms among would-be standards writers.

If so many people strive for standards, and so many others at least passively support them, why then are they so difficult to settle? A review of the progress, or lack of it, in big dynamic RAMS and erasable PROMS provides some answers-in parallel

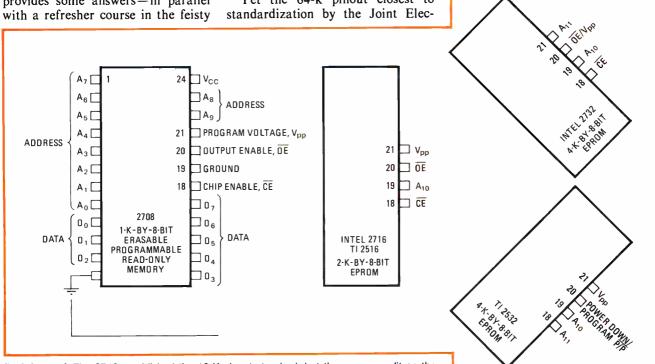
manufacturers' marketing rivalries. For dynamic RAMS, only two related questions have to be settled in the coming 65,536-bit devices: what to do with pin 1 and whether the standard should specify one power supply or two supplies.

Regarding the pin, the simplest approach is to do nothing, as Texas Instruments Inc. does in its TMS 4164 (see p. 39). Making the pin a no-connect, reasons TI, automatically makes the device plug-compatible with the 64-K RAMS of other manufacturers, several of which may use the pin for a negative supply voltage or a special function. Also, TI's part requires only a single +5volt supply.

Yet the 64-k pinout closest to

tron Device Engineering Council, the group that makes such decisions, is the two-supply 16-pin package. It has survived the first two steps in the Jedec procedure: the decision to conduct a letter ballot, and approval by 90% of the dues-paying committee members who receive the ballot. To become official, it now need only be approved by the council, says Jeff Schlageter. He is manager of the MOS RAM design department at Advanced Micro Devices Inc. in Sunnyvale, Calif., and chairman of Jedec's JC-42 subcommittee on semiconductor memories.

As for the single-supply standard



Fork in road. The 2716 established the 16-K pinout standard, but there was a split on the 32-K device. TI came first; Intel switched for compatibility with its microprocessors.

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Probing the news

(TI's), it is one step behind the twosupply measure on the Jedec ladder. Apparently, it will be approved, too. Explains Schlageter: "Some companies simply won't be able to make a single-supply part; Jedec can't shut them out of the market." As a result, both versions probably will be official, with the one-supply part probably becoming the industry's *de facto* standard. While the differences between the two 64-K RAMs will not be great, a look at the situation among the makers and standards-bearers of the 32-K EPROM reveals how complicated such things can become.

Intel ahead. At the 16-K level, Intel Corp. led the way; its single 5-v supply 2716 soon became the generally accepted industry standard erasable PROM. TI had made a go of it with a three-supply version; although it still ships many of them, it has become an Intel second source with its 2516.

In the next generation of parts, the 32-K level was reached first with a simple ROM because it is easier to build than an erasable PROM. Coming out with 32-K ROMs almost simultaneously just over a year ago were TI and Mostek Corp., the former with its TMS 4732, the latter with the now-discontinued MK 32000. The parts are identical in their single 5-v operation and 24-pin packages. Both also use pin 18 for A₁₁, the address line needed for the doubling of storage capacity.

The trouble started when Intel announced its 32-K ROM, the 2332, with the additional address line not on pin 18 but on pin 21. Larry Jordan, Intel's strategic marketing manager for MOS memories, reasoned: pin 18 had to be used for the chip-enable so that the ROM would operate properly with Intel's own microprocessors. What is done with the ROM is a commitment on the erasable PROM, so sure enough, when Intel announced its 32-K part, there was the A₁₁ address line on pin 21.

Meanwhile, back at JC-42, voting was already progressing on the TI-Mostek pinout, and a favorable decision appeared certain. On first ballot, 90% requirement was missed by a scant half percent; ultimately, though, a revote established the pinout as standard. Now Intel appealed, arguing that by this time it was committed to its own pinout. The committee, acknowledging Intel's importance, sent out another letter ballot—and Intel's layout was approved. Thus, 32-K erasable PROMs were blessed with two standards, a consummation greeted coolly by some members who wondered why the group had not been informed earlier of Intel's plans.

But Dave Ford, Motorola Semiconductor's strategic marketing manager and a member of the JC-42 committee, does not regard the dual standard as a serious problem, saying that two is better than four or five. "We meet only four times a year, and our function is not to plan products," Ford says.

Derrell Coker, Mostek's strategic marketing manager and voice on JC-42, says that while Jedec tries to be on top of the market, it can never solve the problem of getting competing technology leaders to talk about what they are planning.

Systems. In the case of the 32-K erasable PROM. Intel was designing a part to work with its microprocessors, explains Jim E. Coe, memory marketing manager at American Microsystems Inc., who was presenting Intel's case when working there before joining AMI. "The second standard is great for themthey need it for their microprocessors. With the 8048, 8085, and 8086 microprocessors, Intel went to a multiplexed-bus approach, so that the data and address are on the same pin. A systems-oriented house, Intel put the address latches on board the memory chips, which get the address-latch-enable signal from Intel microprocessors." Coe also thinks the output-enable pin, unique to Intel erasable PROMs, "is handy for problems of bus contingency."

In any event, the split is interesting. Mostek's Coker expects Signetics Corp. and Motorola to line up behind the TI pinout, as will Mostek. "These three are big price cutters, whereas Intel has traditionally been a high-price outfit, using the leverage of its microprocessors to keep memory prices up," and that could be a dangerous game in the case of the 32-K erasable PROM.

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Are plug-compatibles vulnerable?

Makers of mainframes that use IBM 370 software see good days, but some observers say leader will make moves to end the game

by Anthony Durniak, Computers Editor

Will the gold-paved ways of the IBM 370 plug-compatible market crumble with the introduction of IBM's E and H series in 1979-80? To gauge by the ever-thickening ranks of vendors of IBM-compatible mainframe computers, it would appear not. Some industry observers, though, question the market's longterm potential.

The most recent entry is add-on memory maker Cambridge Memories Inc. of Waltham, Mass., which late last month announced three processors compatible with the lowend IBM 370/115, 125, and 135 computers (see "Cambridge joins the marketing ranks"). Cambridge is joining other recent entrants, including Two-Pi Co. [*Electronics*, May 11, p. 228], Magnuson Systems Inc. [*Electronics*, May 25, p. 93], National Semiconductor Corp. [*Electronics*, May 11, p. 81], and Mitsubishi Electric Corp. [*Electronics*, Aug. 31, p. 48], in a market pioneered by Amdahl Corp., with early competition coming from plug-compatible

Cambridge joins the marketing ranks

The IBM-compatible computers from Cambridge Memories will offer 10% to 15% higher performance than their IBM counterparts yet will sell at approximately 80% of the IBM price, says product manager Kent E. Crombie. Although this is Cambridge's initial entry into the market as a direct marketer, the company has been involved for some time as the initial backer of and now 40% partner in IPL Systems Inc., Bedford, Mass. IPL is the firm that developed and manufactures the Omega 480-1 IBM 370/138- and 148-compatible mainframe marketed since 1977 by Control Data Corp., Minneapolis, Minn.

Built with a combination of emitter-coupled logic and transistor-transistor logic, Cambridge's Model 1 has a processor cycle time of 480 to 1,130 nanoseconds, equal to or slower than IBM's 115 cycle time of 480 ns. The Model 2 also comes in with speed equal to that of the IBM Model 125, but Cambridge's Model 3, with a cycle time between 180 and 850 ns, beats the speed of the IBM's 135, which has a cycle time that ranges from 275 to 1,485 ns.

In the matter of memory capacity, Cambridge offers up to 2 megabytes some four times the 524-kilobyte limit on the IBM 135. The MOS static random-access memory chips are now 4-K; Cambridge plans to move to 16-K chips as they become available. More input/output than IBM's is also offered by Cambridge. Cambridge has a standard byte-multiplexer channel and two block-multiplexer channels with two additional block channels optionally available on the Model 3. IBM supports one byte-multiplexer channel on the 115 and 125, and it, too, can have up to two block channels on the 135.

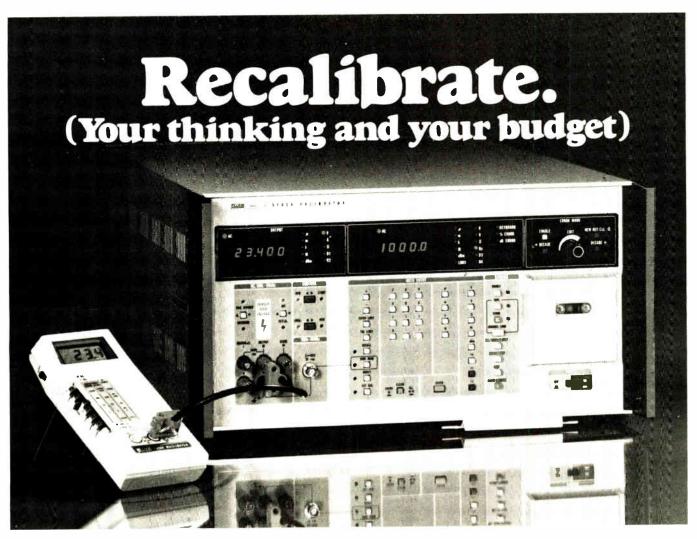
IBM's maximum I/O data rate on the 155 and 125 is 900,000 bytes per second, where Cambridge's is 2,600,000 bytes/s. On the IBM 135 the I/O rate is 2,400,000 bytes/s while Cambridge's Model 3 operates at up to 3,700,000 bytes/s.

manufacturers Itel Corp. and Control Data Corp.

Like most of his competitors, Cambridge executive vice president Richard Eagan says the large installed base of IBM mainframes and the tremendous amount of software written for them makes the market attractive. The impetus for many of the newer competitors, he says, is that "user acceptance has been indicated by Amdahl's success."

But Robert Fertig, director of the technology analysis group of Advanced Computer Techniques Corp. of New York, marketing consultants, says that "for all its competitiveness, the 370 plug-compatible business will likely be short-lived because of the anticipated introduction in early 1979–80 of new IBM hardware, particularly the E and H series [*Electronics*, Aug. 17, p. 44].

Complex. The debate over the future of the IBM-compatible concept revolves around a series of intertwined technical and business questions. The major attraction of the IBM-compatible units is their improvement on IBM's price/performance ratio, achieved by using stateof-the-art large-scale integration for logic and memory chips that use less power and run cooler. In addition, internal architectural changes provide higher rates of data input/output, improved diagnostics, and other features unavailable from the computer industry giant. Although the guts of their hardware are not identical with the internal hardware of the 370, most of the manufacturers have put machine-level software, called microcode or firmware, into their machines to interpret and emulate



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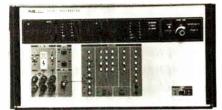
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Probing the news

the IBM instruction set—and thereby run all software written for the IBM computers.

"The makers exist in the mainframe business because the 370 exists with its largely technological weaknesses," Fertig agrees. "But the E and H series products will presumably incorporate technologies at state-of-the-art levels equal to, or ahead of, those currently used by 370-compatible machines," he warns. In addition, Fertig says that any changes made by IBM in the instruction set or microcode will not be announced until the new machines are delivered—often 12 to 18 months after they are announcedgiving IBM a head start in the market.

Paul Magnuson, president of Magnuson Systems, echoes the confidence of his competitors. "We have things in development to stay ahead of IBM with price/performance so I don't see a problem." As for the time lag between IBM's announcement of new products and the delivery of their details, Magnuson feels his company "can catch up quickly. We're a smaller company and we have a good feeling for what things make sense to build in with microcode changes."

Changeable. Eagan notes that because Cambridge's machine is microcoded and stores that microcode in electrically alterable read-only memories, any changes IBM makes can be copied and easily added to his machine to keep it compatible. And Jared Anderson, Two-Pi's president, says IBM will have to inform its rivals about changes-whether it wants to or not. "Changes in the operating system software or microcode appear to the programmer as a new instruction. And IBM will have to explain to him what that instruction does. That's all we need to know."

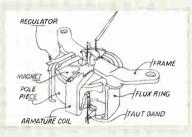
Despite the debate, increased activity is expected in the market for the near future. "There are a tremendous number of people with IBM plug-compatible peripherals and I wouldn't be surprised if those peripheral companies also entered the mainframe business," Anderson says.

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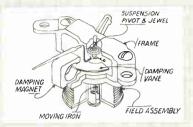
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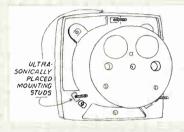
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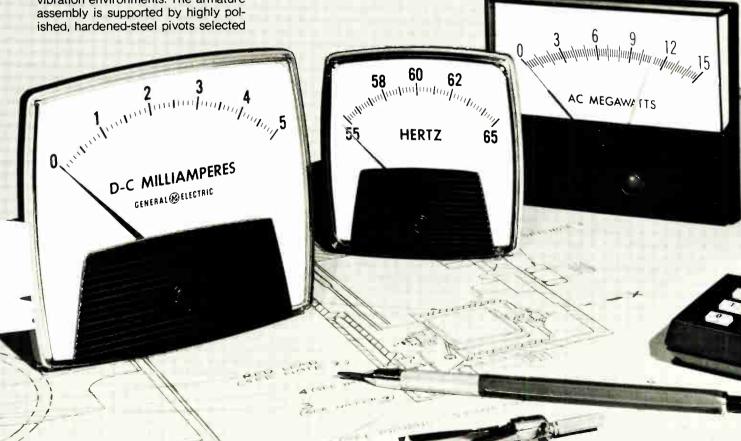


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Electronics abroad

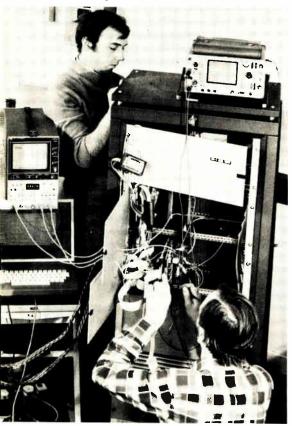
British work on multimicro systems

Major research effort is aimed at real-time use by such companies as airlines and brokerage houses

by Kevin Smith, London bureau manager

The growth in real-time computer systems like those used by airlines and banks or for process control is spurring a major research effort in British universities and research laboratories to tap the growing power of the microprocessor in the first generation of multi-microprocessor systems.

Most recently, Britain's National Physical Laboratory announced that it was teaming with Scicon Microsystems Ltd., a commercial software consultant, to develop a multimini/microcomputer system called Demos that could link up to 100 computers via an 8-million-word-



per-second parallel ring. This ambitious project is paralleled by several others.

These systems, say proponents, promise modularity that allows expansion, flexibility in matching microcomputers to a required response speed, and low cost when compared with the present generation of timeshared mainframe computers and minicomputers.

Significant. The concept could have a major impact on computing technology over the next decade. "Multiprocessor technology is one of the most important and difficult areas today," says Prof. J. E. Brignell of London's City University, a leading researcher in the field. "Computer programmers have been trained to analyze problems sequentially because that's the way computers have worked till now."

E. L. Dagless, who is establishing at University College, Swansea, Wales, an academic program for the subject with a general-purpose multi-microprocessor system based on six Intel 8080s, cites two reasons for the growing interest. First, the microprocessor allows the user to build his computing power in modular steps, and this can be important in specific industrial and commercial applications, since it allows a system to grow. Next, it lets an engineer tailor his system to a specific task so that it can be split into identifiable modules, each assigned to a processor. The partitioning can be accomplished by pipelining or paralleling processors.

Wired. At University College in Wales, researchers are working with a multimicrocomputer system of six Intel 8080s. Still a third reason for going to a multiple-microprocessor system could be to increase the microcomputer's brute computing power. It is by far the most difficult problem and one that raises the most skepticism among the industry's mainframe traditionalists.

However, few present-generation microprocessors are suitable for such close coupling. "We chose the F100-L because it was designed by computer systems engineers," says Brignell, "and has features like indivisible bit testing and setting, which you need for semaphore protection. However, newer-generation microprocessors could incorporate these features." In fact, one British company has a processor specifically for multiprocessor operation on the drawing board and is currently canvassing interested semiconductor manufacturers.

The power of multiprocessor technology has also been demonstrated in specialized sectors of the mainframe market. ICL's distributedarray processor, with its 100 million instructions per second, uses an array of simple processing elements distributed through the memory of a conventional mainframe computer. Also, Plessey Telecommunications Ltd. has gone to multiprocessor architecture to achieve a high-integrity exchange secure against the failure of any one element.

Finding places. Where will the systems make their first market impact? Demos, says Wilkinson, is especially suited to applications where large numbers of activities take place in parallel: interactive and financial-transaction processing, for one, where large data bases can be divided on a disk-per-computer basis to allow fast and efficient file access.

Interface control. Telecommunications is another major application area. In collaboration with Warwick University, Systems Reliability Ltd. in Luton is developing a closelycoupled multi-microprocessor system as a universal interface processor in data-communication systems. Its job is to switch together data terminals and data links having widely different data rates and lengths. The system, which should be ready for the end of this year, uses Texas Instruments Inc.'s 9900 16-bit microprocessor.

But problems crop up with increasing processor integration. As each calls on the other's resources, where memory and data channels are shared, contention between processors and administrative overhead can clog the system.

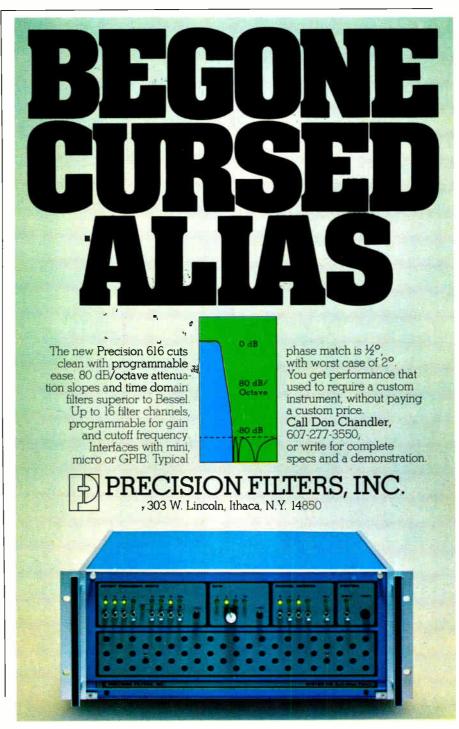
Loosely coupled systems present fewer problems than closely coupled ones. At the Royal Signals Research Establishment in Malvern, for example, researchers have gone for an asynchronous bus linking Intel 8080 microprocessors, each performing a specific function that is frozen into read-only memory. The team is using its Discus system to test Ptarmigan, a digital switch, for the British Army.

At the University of Kent in Canterbury a packet-switching protocol is being used by a team under F.K. Hanna to link a five-node network of Digital Equipment Corp. LSI-11s. The system, which could be employed in such applications as implementing a hospital data-collection system, uses no particular interconnection structure, because one processor broadcasts to all others simultaneously over all links. The system offers high integrity, modularity, and plasticity of programming since programs can readily be changed on line.

Difference. One big distinction between dedicated systems of multiple-microprocessor and general-purpose multi-microprocessor architectures comes at the software level. A dedicated multiple-processor system has little need of general-purpose software because it is directed to one application. However, multi-microcomputer systems require a highlevel operating system if they are to be sufficiently general.

The Royal Signals Research Establishment is using Coral high-level real-time language, and University College at Swansea is using a highlevel language developed at the University of Strathclyde in Glasgow by a group that pioneered the virtual-machine concept. At the Nationl Physical Laboratory, to cut software costs, workers are using Concurrent Pascal, a recently developed high-level language. All of these high-level operating systems have the kind of generality that allows them to be run on yet-tobe-invented multi-microprocessor systems.

Not everyone, though, is convinced that the first generation of multi-microprocessor systems coming out of the universities and research labs is architecturally sound. Brignell takes a jaundiced view and argues that some systems have been thrown together with far too little thought.



AMux in Linear Wonderland

PMI Takes the Nonsense Out of Analog Multiplexers



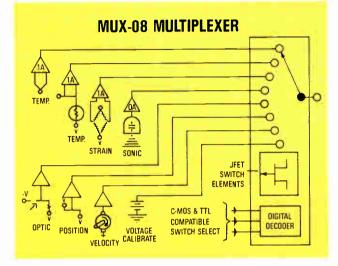
Alice's nonsensical Wonderland was full of things with strange sounding names no one would ever explain to her. Like the Gryphon, the half-bird/halfbeast that sat around saying things like, "Hjckrrh!" And the famous Jabberwock; Alice learned to beware of it, even though she never found out what it was, except that it had eyes of flame and burbled as it came whiffling through the tulgey woods.

In Linear Wonderland, engineers have a similar problem in trying to understand what a MUX means. They know that a lot of people make analog multiplexers. But they must get as confused as Alice when they try to compare PMI's Improved BIFET MUXes with other people's Standard BIFET or CMOS versions. It's like comparing slithy toves with borogoves.

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Itel thrives by taking on IBM

Leasing, service bureau, and mainframe business adds up to \$285 million of company's \$401 million in 1977 sales

by William F. Arnold, San Francisco regional bureau manager

Competing against IBM Corp. may not be the surest way to success, but for Itel Corp. it looks like the best of several worlds. The San Francisco-based company enjoys a thriving three-part business: leasing systems based on IBM computers, running a service bureau, and selling mainframes under its own name into the growing IBM-compatible marketplace. These activities yielded \$285.7 million of the corporation's \$401.8 million in 1977 revenues.

Although the company started 11 years ago by leasing IBM-based systems through its Financial Services group, its Data Products group attracts most attention because it serves the bustling IBM-compatible market. For this market, competitors build IBM-software-compatible machines but use more up-to-date architecture and technology, such as emitter-coupled logic and air cooling, to offer price or performance advantages over IBM System 370 and initial 303X series mainframes.

"Business couldn't be better," declares John H. Clark, president of the Data Products group. His staff sold 52 machines last year, expects to sell about 200 this year, and looks forward to a 300-machine business next year—not bad for a group that brought out its first machine only last year. That was the AS/6, which is equivalent to the 370/158, to which has been added the AS/4, which is 40% more powerful than IBM's 370/148, and the AS/6, which is equivalent to the 370/168 and newer 3032 machines. This month it extended the range downward by introducing the AS/3 in two models: the \$570,000 model 4, equivalent to the 370/148 and the \$490,000 model

3, which Clark says has 1.5 to 1.8 times the power of an IBM 370/138.

Of course, there is competition. Of course, there is competition. On the high end Itel's AS/6 encounters streaking Amdahl Corp.'s 470 V/5 machine. At the low end its machines face such newcomers as Magnuson Systems Inc.'s M80 [*Electronics*, May 25, p. 93], National Semiconductor Corp.'s System 400 [*Electronics*, May 11, p. 81], and Two Pi Co.'s V/32 [*Electronics*, May 11, p. 228]. But Clark says that it meets only IBM in the middle ranges.

Unique spot. "Itel is positioned uniquely in the market," observes Jean Michael Gabet, director of research in the computer division of Gnostic Concepts Inc., a Menlo Park, Calif., market-research firm. "For years as a computer-leasing company it was a go-between for IBM and the end user. This gave it a thorough understanding of the customer's needs for software, hardware, and maintenance, something

Happy days. John Clark, president of Itel's Data Products group, sees blue skies ahead.



special that the others don't have. I tend to look at Itel as somewhere between a commodity trader, where the commodity is CPU and hardware, and a service company."

Buyer. Also unique to Itel is the fact that it makes nothing it sells under its own name. Under exclusive licenses, the AS/6 comes from Japan's Hitachi Corp.; the other mainframes come from National. When the bids call for more extensive systems, Itel uses nonimpact printers from Siemens AG of West Germany, disk drives from Sperry Inc.'s ISS group, and main memories from Intersil Co. and National. Clark likes this arrangement because "there are so many people in the terminal and front-end business."

Clark also says that Itel is not interested in the stand-alone hardware or minicomputer business. Its market is hardware with specialapplications software, such as a general accounting package for businesses, because "the real add-on value is in applications packages," he says. Nevertheless, Itel also markets Data General's CS lines of business minicomputers [*Electronics*, May 25, p. 40] and is negotiating with National to offer its 400 series and Magnuson for its M80 line.

Still, sharing a market with IBM is like being a fly in a bear's cave. "Where will Itel's market be when IBM's E and H series computers appear?" asks Steven Cottrell, senior analyst with Creative Strategies International, a San Jose, Calif., market-research group. He expects the E series computers to have dramatically improved price/performance ratios, that could shrink the cost advantage of the plugcompatible market. "IBM won't let the [mainframe] market get away from it," says Gnostic's Gabet, who pegs it at "certainly less than 15,000 units over the next five or so years." He thinks that the new IBM machines will have 370 emulators so that IBM will be able to upgrade its customers' present machines.

Conceding that IBM is "damn tough competition," Clark says Itel plans "to penetrate their installed base by 5% a year over five years" and will announce competitive machines shortly after IBM introduces the E and H series. "We expect a 2-to-1 price/performance improvement from IBM," Clark says. "We're prepared to react to that."

Hard threat. Some believe another threat is IBM's attempt to protect its software through microcoding, or putting software into hardware, often called firmware. But, according to Clark, "firmware is no big deal if you understand software and hardware and have firmware machines," which Itel does. Its machines have twice as much reloadable control store as do IBM's, and it is developing enhancements to its rival's operating system in firmware, he says. Concurring, James Siehl, director of enduser products marketing for National's Computer Products group, says all his group's machines are in microcode, which is "easier to change than a hardwired architecture like Amdahl's."

Some problems may be more immediate, however. One example: the joint venture with Hitachi could be setting up a potentially powerful competitor. They are developing a computer that is 50% more powerful than IBM's 3033 for introduction in 1980, Clark says. "They have the technology, we have the understanding of IBM architecture, software, and diagnostics," he explains.

And what about the relationship with National, which is making more and more noise about becoming an independent computer company? "The relationship is a good one," according to Clark, who says the exclusive agreement on the AS/4 and 5 runs through 1980. "That gives us four years in the marketplace with one product," which he thinks is good.

As for National's potential threat,

Clark's answer is: "You have to have an established sales and service organization to be credible in the marketplace." He notes that, although Itel had been offering peripherals under its own name since 1971 when it brought out its mainframes, "we had to convince customers that we were in the central-processing-unit business and were a long-term player." Clark says that his 550 market representatives and 330 systemssupport engineers are split into three groups on a worldwide basis: microand minicomputer for special-applications software, general systems in the 138 and 148 class, and large systems in the IBM 3031 and 3032 equivalent machines.

National's basic assumption, according to Siehl, is that "we will continue to have an agreement with Itel." He says his company will actively market the System 400 as a mainframe processor for originalequipment manufacturers and intends to expand its products to OEMS "and to end users, if appropriate." But for any end-user business, Siehl says, National will select fairly narrow markets "where we feel comfortable-we'll stay in areas where our semiconductor technology affords us an advantage." However, Creative Strategies' Cottrell looks for the Itel-National relationship to be "at arm's length after 1980" and for National to go after the end-user market directly.

There is probably enough business for everyone. "The market is so vast that one would have a hard time even approximating how many people use IBM computers," observes Jared Anderson, president of Two Pi. "Itel should do really well so long as IBM doesn't change the rules, meaning changing the microcode extensively. Observing that "no company can service the entire market," Siehl says that IBM actually created two markets, the plug-compatible and the independent-service companies. "You look at the raw numbers and the market is huge," he says, but "you don't have to be a \$20 billion corporation to have a successful product. People overlook the fact that with 3% to 4% you can have a successful market share." But Clark says, "I'd love to see us get 10% of the monthly shipments."

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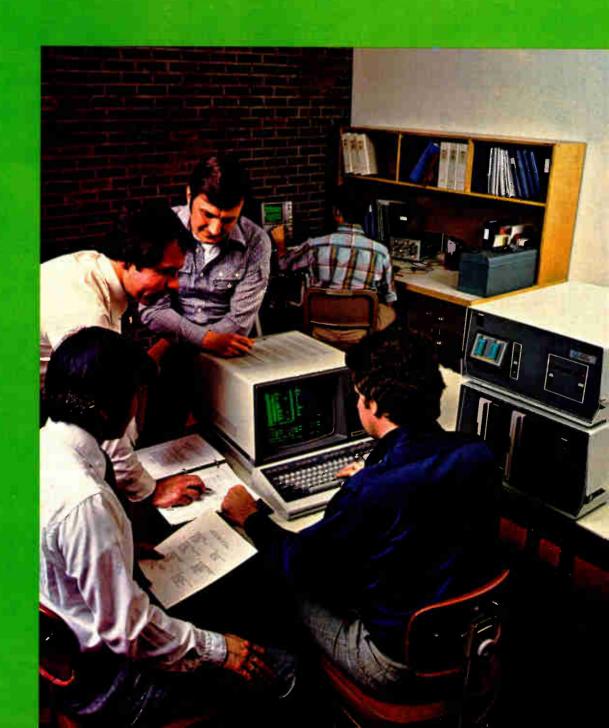
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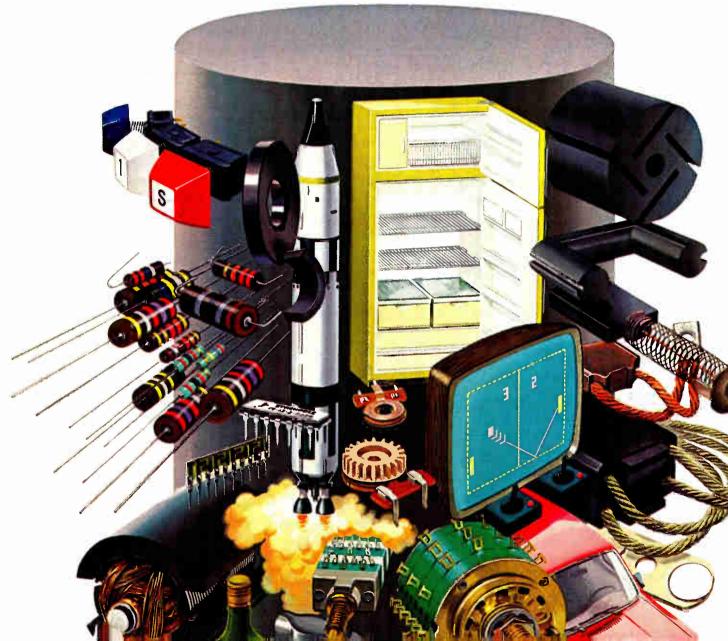
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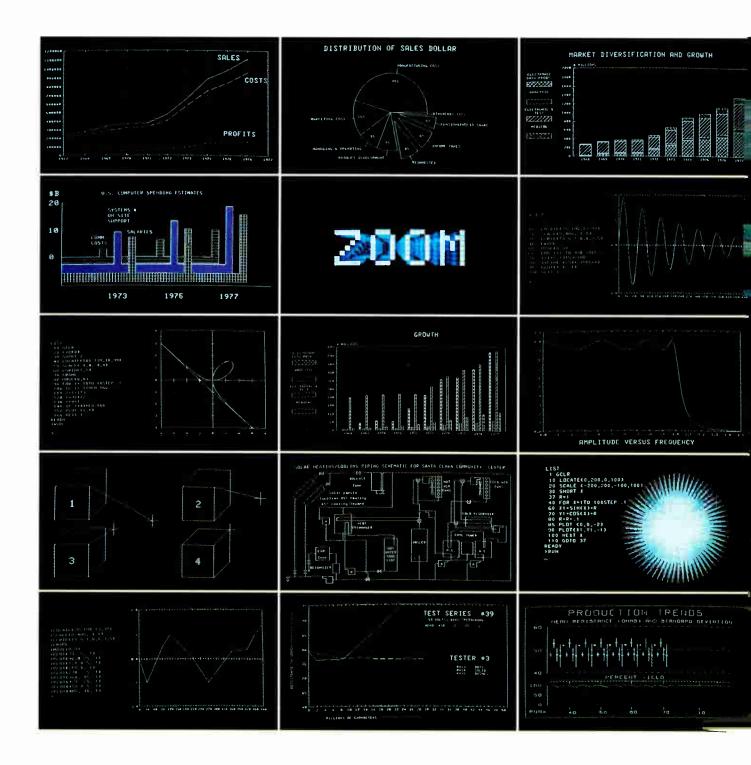
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Technical articles



Technologies, architectures compete for huge codec market

by Harvey J. Hindin, Communications and Microwave Editor

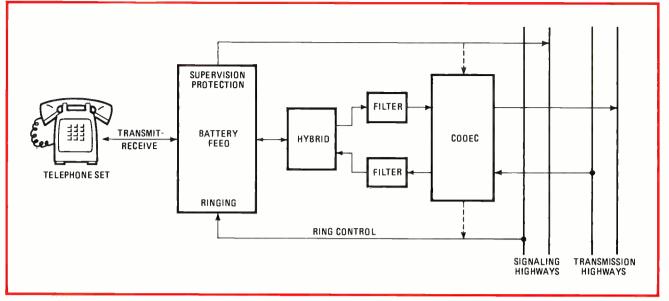
□ There's a new integrated circuit in town, and it's making quite a stir in both the semiconductor and communications industry. Dubbed the codec, it is already widely available from many manufacturers, and it promises to sell in million-unit quantities as a result of the telephone industry's worldwide turn to digital technology [*Electronics*, July 20, p. 88].

Codec is short for encoder-decoder. An encoder contains all the elements needed to convert analog voice into digital data for transmission over a telephone line. Conversely, a decoder contains the elements that perform the digital-to-analog conversion needed to restore the sound of the voice after transmission.

Previously, these conversions were achieved by highspeed a-d and d-a converters multiplexed over many analog channels. But now the advances in large-scale integration have made it economically feasible to encode each channel separately and multiplex the resulting digital signals (see "What the codec does").

Short-term applications of codecs are likely to be concentrated in central stations and in larger private exchanges. This market still represents millions of parts, according to forecasts from semiconductor manufacturers [*Electronics*, April 13, p. 77]. There is also that eventual possibility of one in each phone—and there are 398 million telephones in the world. But for the longer term, because codecs will take time to impact the fiscally and technologically conservative telephone industry, applications are expected in transmission systems, local and tandem (interoffice trunk switching) offices, private automatic branch exchanges, and ultimately, local subscriber loops and telephones. And, since codecs will sell for a few dollars each in large quantities, it is easy to see what is exciting the semiconductor industry.

The major telephone companies represent the largest portion of the potential market. It hardly comes as a surprise, then, that they are doing development work in this field themselves. The biggest of all, American Telephone & Telegraph Co., is thought by industry observers to be working on its own codec through Bell Laboratories. A spokesman notes a "vigorous codec program is going on, but no information is available yet." In



Placement. A one-chip codec without on-board filters would fit in a private branch exchange or central office switching system just before the so-called transmission highways. Ultimately it might interact with signal-line highways for ringing and other functions.

contrast, aggressive Northern Telecom of Canada has already released some information on a codec it has been working on. One feature is an on-chip filter, which alone is enough to set Northern's codec apart from most of the others that have been announced. Moreover, according to John Mahoney, division general manager of the company's Digital Switching division, the codec "will be used in the DMS-100 large digital local switch, which has a capacity of up to 100,000 conversations and will be shipped by the end of the year for service in 1979."

Among semiconductor manufacturers, only American Microsystems Inc. also claims an on-board filter. So it is interesting and perhaps strange, as one industry observer chose to put it, that Northern Telecom and AMI recently entered into a "custom fabrication" agreement for production of Northern Telecom-developed codecs over the next two years.

Doing it

The manufacturers now producing codecs use a diversity of approaches in building them. Still, the specifications the codecs must satisfy are well-defined by the telephone industry. Consequently, although the chip counts, processes, and architectures may vary widely, the results must satisfy certain performance requirements.

At present, one-chip and two-chip devices and totally discrete components are all available. Proponents of the one-chip approach claim that this is the way the codec will finally go, so "why not do it now?" They assert that the use of a single-process technology has not required compromise on any specifications.

Two-chip advocates disagree, saying that different functions are better served by different processes. They claim that the use of two separate processes has not only allowed them to far exceed telephone industry requirements but also lets them build smaller and therefore more reliable devices. The small die size also boosts the production yield and thus lowers final cost.

A third viewpoint is advocated by Precision Monolith-

ics, which is making parts available for so-called shared codecs. In this approach, discrete codec parts are simultaneously used by 8, 12, or more channels. The company believes this is the most efficient in cost and power when these factors are measured on a per-channel basis.

To further complicate matters, some manufacturers keep encoder and decoder separate. Among other advantages, they claim that they can meet requirements this way in a smaller package with fewer pins.

Actually, there is not even agreement as to how many functions a codec should perform in a complex telephone network. According to Ron Hlavinka, General Instrument Corp.'s telecommunications marketing manager, a "true codec performing all the required telephony functions has yet to be developed" on one or even two chips. GI, along with Motorola Inc., has chosen to produce one chip for both the μ and A laws (see "What the codec does"), leaving the user to pick the one he wants by pin selection.

As for process technologies, there is a variety being utilized in codecs. These include both n-channel and complementary metal oxide semiconductor, integrated injection logic, and charge-coupled devices. As industry observer Benjamin Rosen of Morgan Stanley & Co., a New York investment firm, points out, "The codec affords us a good example of how there can be reasoned difference as to what constitutes the right technological direction—in this case the optimal process and design."

Table 1 summarizes the approaches being followed by representative codec manufacturers. Key specifications are given where they are available for one- and two-chip approaches. Precision Monolithics' shared codec has too many components to be included here, but they are discussed in detail in the technical article on page 108.

Intersil Inc., Fairchild Camera & Instrument Corp., and Advanced Micro Devices Inc. are also working on codecs, but it is too early for any information to be available about them. In addition, industry giant Texas Instruments Inc. is playing it close to the chest and will

Manufacturer	intel	Mostek	Signetics	Motorola	American Microsystems	General Instruments	National Semiconductor	Siliconix
μ-law part (s)	2910	MK5150 MK5116'	ST100	MC14407 ⁴ MC14406 ⁷	S2900 coder S2901 decoder	AY3-9900⁴	MM58100 LF3700	DF331 coder DF332 decoder DF334 decoder
A-law part (s)	2911	MK5155	not available	MC144074	S2902 coder S2903 decoder	AY3-9900 ⁴	MM58150 LF3700	DF341 DF342
Process technology	n-MOS	C-MOS	l ² L	C-MOS	C-MOS	n-MOS	C-MOS bipolar	C-MOS
Die size (mil ²)	22,000	31,280	36,000	34,125	info not available	19,500	25,600 11,550	19,162 16,386
Mask count (with final coat)	9	10	10	7	8	6	info not available	info not available
Number of chips	1	1	1	1	1 ³	1	2	1 ³
Filter on chip?	no	no	no	no	yes	no	no	no
Number of power supplies (not including reference)	3	2	3	1	2	2	2	2
Voltage supply values	+12, ±5	± 5	± 12, + 5	10 - 16	± 5	+ 9, + 5	± 12	± 7.5
Mode of operation	asyn/syn	asyn/syn	asyn/syn	asyn/syn	asyn/syn	asyn/syn	asyn/syn	syn
Number of pins	24 22	24/16 16	24	28/24 28	18 coder 16 decoder	24	28/20 22/20	14
Voltage reference on chip?	yes	no	no	no	no	reference not needed	yes	no
Power dissipation (typ): active (mW) standby (mW)	220 110	30 not available as option	375 50 (max)	80 0.5	(includes filter) 200 25	300 not available as option	250 < 10	45 not available as option

not even say if work is in progress.

European companies, while not included on the chart, have not been napping. Siemens AG of Germany has taken a two-chip n-MOS and bipolar approach in its A-law codec but does not yet have a μ -law device. Sweden's Ellemtel is said to be cooperating with National Semiconductor's C-MOS and bipolar effort.

In England, General Instrument Microelectronics Ltd. is one of the first companies on the market with a pin-selectable μ - or A-law device with full CCITT compliance. It uses an off-chip delta-sigma modulator to convert data to pulse-code-modulated form. Pye Ltd., Ferranti Ltd., Plessey Co., and General Electric Co. Ltd. are also hard at work in this area. As in the U. S., there are probably too many potential suppliers, and a shakeout appears just as inevitable.

Strangely enough, no Japanese codec activity has been visible—a state of affairs that no one in the American semiconductor industry expects to last much longer.

What are the tradeoffs?

Obviously, manufacturers want a small chip, the fewest possible number of masks, and simple processing to maximize their yield. Users want a minimum number of standard power supplies with wide tolerances. Low active power dissipation and a possible standby mode are also desirable as may be a voltage reference on the chip, depending on the conversion method used. Microprocessor selection of time slots may be useful in certain cases, as may be various interfaces for phone ringing, dial pulse echoing, and other special codec functions. Also, where

timing cannot be derived from local clocks, asynchronous operation may be required.

None of the codecs available has all of these features or options simultaneously. Clearly, compromises have had to be made. Unfortunately, the various manufacturers disagree as to which of the codec requirements are more important.

However, power dissipation is accepted as one of the more critical characteristics, especially when codecs are installed in individual telephones. It is dogma that no external power can be connected to the telephone, so that all power must come from the relatively low-level line. In this regard, C-MOS parts are inherently superior to n-MOS and bipolar devices. For instance, Motorola's C-MOS part dissipates 80 milliwatts in its active mode and just 0.5 mw typical in standby. In contrast, the n-MOS parts dissipate 220 to 300 mw active and 110 mw standby. Moreover, three of the codecs, General Instrument's n-MOS, Mostek's C-MOS, and Siliconix' C-MOS do not have standby modes.

Codecs from Signetics Corp. are being tested by International Telephone and Telegraph Corp., and General Instrument's device was developed in conjunction with the British Post Office. In addition, National Semiconductor Corp. says it has shipped thousands to two telephone companies. But actually most manufacturers have made samples available to all comers, and it appears that "everyone is buying from everyone." Small-quantity prices seem to be rather arbitrary, and no one knows what a really large quantity would go for dollar-wise.

Industry observers and the semiconductor manufac-

turers themselves believe that there has to be a significant shakeout. Right now there are a dozen or so possible manufacturers, both domestic and foreign. Once the customers start making volume buys and the trends become clear, it is probable that the losers will abandon their own idiosyncratic designs and become second sources for the preferred approach, whatever that may be. Marketing clout, reproducibility, low cost, high performance, and early delivery as usual will determine who's who in codecs.

The two articles that follow offer a detailed account of the shared-codec approach and an n-MOS one-chip design. Articles on codecs implemented with C-MOS and I^2L processes will appear in subsequent issues.

What the codec does

In any telephone network, the input voice information is an analog time-varying signal. In a digital net of the timedivision-multiplexed kind, this voice-data input is digitally sampled by the codec at discrete, uniform intervals. These intervals are determined by the Nyquist sampling theorem, which states that any signal can be ultimately reconstructed if it is sampled at a rate equal to twice its highest frequency of interest. The universally accepted rate for a telephone conversation is 8,000 samples per second because voice data transmission up to 4,000 hertz has been found to have enough fidelity for practical purposes.

The voice signal must be band-limited at 4 kilohertz by a low-pass filter to prevent it from being distorted by the codec's analog-to-digital and digital-to-analog conversions. Ultimately semiconductor manufacturers will incorporate the filter in the codec itself, and there is some feeling that even the full-duplex hybrid, which allows twoway conversions, will end up in the codec.

The digitally encoded information is transmitted in bitserial form. This technique allows data transmission from 24 voice channels into 24 time slots on a single, serialtransmission highway or bus. One 8-bit code word from each voice channel is transmitted in its associated time slot, and the bus format groups the 24 8-bit time slots into a 192-bit block.

Overall synchronization is provided by adding 1 bit and the resulting 193 bits are designated a frame. This last frame synchronization bit defines the boundary between time slots 1 and 24 and serves to keep the time-slot counter of the far-end receiver synchronized with that of the near-end transmitter. The 8-kHz frame repetition rate then produces the characteristic 1.544-megabit-persecond data used in all AT&T T1 systems. The 8-bit data block corresponding to one sample of a given voice channel is demultiplexed by time-slot identification at the receiver. The critical step in the process of forming the digital pulse-code-modulation signal is the assignment of a binary code to each analog sample as it is presented to the codec. This is usually done by a system of nonlinear quantization referred to as companding and performed by a compander (compressor-expander).

In a typical companded transmission system, the analog signal is passed through the compressor part of the transmitting compander before being transmitted. At the receiver the analog signal is passed through the expander part of the receiver compander. The process boosts lowlevel signals, making them better able to compete with the system noise, and attenuates high-level signals, preventing them from saturating the system.

A digital realization of the desired companding law is obtained by segment or chord approximation to the curve shape. North American PCM systems use digitally realizable approximations to the so-called μ -255 law. For this encoding law, there is a total of 8 chords for each input polarity, with each chord having 16 equal steps. The step size within each chord is constant, but doubles in size from one chord to the next, starting with the chord nearest the origin.

European telephone systems also use a chord or segment approximation but in accordance with the socalled A law. A total of eight segments is again used for each polarity. For the four chords nearest the origin, however, the step size remains the same and the four chords about the origin are merged into a single chord. After the first two chords, the steps double in size from one chord to the next.

In practice, there is not much difference between the two laws. Controversy over which is "better" exists but involves various nontechnical arguments concerning the place of origin. In any case, most codec manufacturers are making both laws available for the two markets.

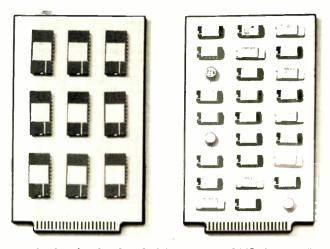
Multichannel shared codecs cost less and save on power

by Guido Pastorino, Precision Monolithics Inc., Santa Clara, Calif.

□ One option for the designer of pulse-code modulation systems is to assemble a coder-decoder from separate large-scale integrated circuits and share it among eight or more channels. Such a codec uses less power and costs less per line than the single-chip-per-channel approach advocated by most integrated-circuit manufacturers.

The idea has a long pedigree. The earliest codecs, which were built out of discrete transistors and passive components, were shared devices, and LSI shared codecs have been going strong for as much as two years. Such devices can be found, for instance, in carrier systems, digital private-branch exchanges, and remote terminals, including a number of systems that meet or exceed telephone system specifications. In a typical digital exchange, this kind of codec may be shared among 8, 12, or 24 lines. Such a design is at present being considered by AT&T for the D4 channel-bank codec.

A shared codec digitizes the signals from each channel in turn. It takes a sample from the first channel, assigns



1. Packaging density. Only 9 of the necessary 24 ICs for a per-line codec fit on the board at left, whereas all the ICs needed for a 24-line shared codec fit on a board on the same size at right. Packaging density is a prime factor favoring the shared-line codec approach.

it a digital value, puts it out on the PCM line, and starts over again with the second channel. This contrasts with the per-line approach in which each line requires its own codec and the time-slot interfacing is done digitally, usually by busing the codec outputs.

To share or not to share?

In a shared-codec system, the multiplexers, references, sample-and-hold circuits, digital-to-analog converters, and other devices are all implemented as separate LSI circuits. The multiplexers and sample-and-hold circuits, in particular, are manufactured to exhibit much lower crosstalk than their discrete counterparts, seriously weakening the argument that per-line codecs are necessary to eliminate interchannel crosstalk.

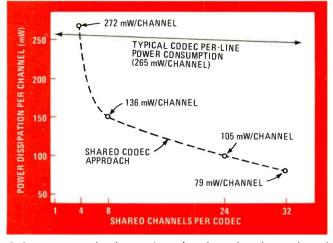
Moreover, the use of shared codecs allows the appropriate process technology to be used for the different codec functions. In the per-channel approach, it is not always practical to optimize all functions at the same time on the same chip, since different functions are sometimes best performed by different technologies.

The budget's the thing

As far as the engineer is concerned, however, the key reasons for going to shared codecs are the power and cost budgets and the package count (Fig. 1).

Figure 2 and the table show how low the power consumption can become with two distinct shared-codec configurations. The per-line 24-channel codec, which encodes with two d-a converters and decodes with one, has a total codec power consumption of 2,541 mw, which divided by 24 yields a per-channel power consumption of only 106 mw. The 32-channel codec has exactly the same component count as the 24-channel system and also exactly the same total power dissipation, but the per-channel power dissipation drops to 79 mw.

Then there is the cost factor. Estimates indicate that the per-channel cost of the Precision Monolithics devices used for an 8-channel system with one digital-to-analog converter each for the receiving and transmitting functions are \$3.92 per channel, in 100,000-piece quantities,



2. Less power. As the number of codecs shared per channel increases, the power dissipation per channel decreases rapidly. With the per-line codec approach, dissipation is constant, regardless of the number of channels. A curve comparing prices would be similar.

and the per-channel cost for the devices in the 24channel system is \$2.36 per channel for the same quantity. For the 32-channel system, cost shrinks to about \$2.00 per channel.

In terms of package count (a major size and reliability consideration), shared codecs are competitive with perline codecs if shared over eight or more channels. When the per-line device is contained on one chip, the package count for both systems is about the same. When the per-line system is a two-chip set, the package count favors the shared-codec system. For the 24-channel codec system in the table, the total package count would be 24 even with a generous 10-package allowance for the successive-approximation register and miscellaneous digital components. With a per-channel system, allowing two extra packages for reference supplies, the package count would be 26 for a one-chip system and 50 for a two-chip system.

Building a shared codec

A typical shared-codec system, such as a 24-channel D3/T1-type bank, may be built with a set of three 8-channel shared codecs (Fig. 3). This design is easy to construct and requires only noncritical layout techniques. It uses six d-a converters to encode and decode 24 channels. More advanced systems use two converters to encode two groups of 12 channels and one converter to decode 24. The theory of operation of those more advanced systems is the same as the one for the 8-channel systems.

Each input to the transmitting multiplexer is preceded by a transmitting filter, and each output of the receiving multiplexer is followed by a receiving filter. The receiving and transmitting filters are identical, except that the receiving filters have a frequency response peak between 3 and 4 kilohertz to correct for frequency rolloff caused by the zero-order-hold capacitors at the output of the receiving multiplexer.

In the next step, the transmitting filter outputs are applied to the transmitting multiplexer, which is the first of the two stages of the analog sampling system. The

	COST/POWER I	BUDGETS FOR TW	O SHARED CODEC	SYSTEMS						
System configuration	-	24-channel		32-channel						
System configuration	with one d-a converter for receiver, two for transmitter									
Device	Number required	Power dissipation (mW)	Unit cost in quantities of 100 (\$)	Number required	Power dissipation (mW)	Unit cost in quantities of 100 (\$)				
Digital-to-analog converter	3	423	27.00	3	423	27.00				
Sample-and-hold amplifier	2	320	19.00	2	320	19.00				
Reference	1	15	1.95	1	15	1.95				
Comparator	2	206	6.00	2	206	6.00				
High-speed operational amplifier	1	110	2.50	1	110	2.50				
Multiplexer	7	1,092	52.50	7	1,092	52.50				
Successive-approximation register and miscellaneous digital components	10	375	20.00	10	375	20.00				
TOTALS	26	2,541	128.95	26	2,541	128.95				
Per-channel	1.08	106	5.37	0.8	79	4.02				
Large-quantity per-channel cost			2.36			2.05				

multiplexer connects each of the channels, in sequence, to the sample-and-hold circuit, functioning as a single-pole, eight-throw switch that cycles through all eight channels at an 8-kHz rate.

After all the switching transients have died down, the output of the multiplexer is sampled by the sampleand-hold circuit, which becomes the second stage of the analog sampling system. The output of this circuit remains constant throughout the entire analog-to-digital conversion period. It is fed through a resistor into the comparator, which together with the a-d conversion logic and the digital-to-analog converter make up the codec's a-d converter.

The comparator has one resistor in series with its positive input terminal (through which the sample-and-hold output enters) and another resistor in series with its negative input terminal. The resistors' job is to convert the d-a converter output, currents $I_{\infty}(-)$ and $I_{\infty}(+)$, into voltages that can be compared with the one from the sample-and-hold output. Current $I_{\infty}(+)$ flows only for negative signals (indicated to the d-a converter by a binary 1), while $I_{\infty}(-)$ flows only for negative signals (indicated by a binary 0).

To satisfy the successive-approximation criterion used in this system, the input to the a-d conversion logic must be binary 1 whenever the magnitude of the analog voltage exceeds the product of R and either $I_{\infty}(-)$ or $I_{\infty}(+)$. For a positive analog signal, the output of the comparator is a binary 1 whenever the analog voltage exceeds $I_{\infty}(+)R$. For a negative voltage, however, the output of the comparator is a binary 0 whenever the analog voltage magnitude exceeds $I_{\infty}(+)R$. The exclusive-OR gate inverts the output of the comparator for a negative analog signal.

The a-d conversion logic, which consists of a successive-approximation register with supporting logic, operates in a standard manner. After the encode command is generated by the system timing and switching logic, the encode-decode pin of the converter is placed in the decode or binary 0 state forcing both $I_{oe}(+)$ and $I_{oe}(-)$ to zero. The comparator is then disconnected from the d-a converter and acts as a polarity detector. The signbit pin is forced to 0 during the first clock cycle to allow the result of the polarity detection to be clocked into the a-d conversion logic as the sign bit.

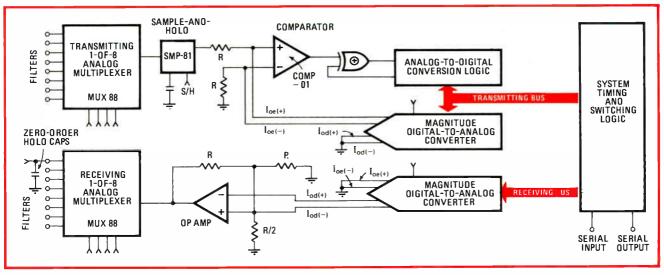
This sign-bit generation ends with the arrival of the next clock pulse. Following this, the input on the d-a converter's encode-decode pin is returned to binary 1 to reconnect the comparator. The bit adjacent to the sign bit, the most significant bit, is forced to 0 and all succeeding bits are forced to 1. The second input to the exclusive-OR gate resumes the inverse value of the sign bit, and the input analog voltage is again compared with the $I_{\infty}(+)R$ or $I_{\infty}(-)R$ product.

If the magnitude of the analog voltage exceeds $I_{oe}(+)$ or $I_{oe}(-)R$, the output of the exclusive-OR gate becomes a binary 1, indicating that the trial bit (the 0 on the MSB) should be a 1. The next clock pulse will then clock in the 1 for the MSB. Had the analog voltage magnitude been less than $I_{oe}(+)R$ or $I_{oe}(-)R$, then the output of the exclusive-OR gate would be 0 and a 0 would have been clocked into MSB on this clock pulse.

This successive-approximation procedure continues until all the binary bits have been determined, and the resulting binary number represents the best approximation to the analog input. Since two converters are used per codec, the system is completely asynchronous and decoding and encoding functions can be performed simultaneously.

Putting it together

In order to multiplex a large number of channels through the same codec with the least amount of distortion for low-level signals, both short acquisition time and superior accuracy (low zero-scale error) are required of the sample-and-hold circuit. The accuracy itself is severely affected by a secondary term that is designated the droop rate.



3. Typical system. A 24-channel D3/T1-type bank may be built with a set of three 8-channel shared codecs. Only a portion of the repetitive system is shown for simplicity. In this particular configuration, six d-a converters encode and decode all 24 channels of the system.

A suitably designed sample-and-hold amplifier, such as the SMP81, takes the codec's needs into account when addressing the acquisition and accuracy problems. Acquisition time is reduced by force-feeding current into the hold capacitor whenever there is a large difference between the input and the output voltages. Proper input characteristics are provided by zener-zap circuitry. This is trimmed at the wafer stage, so as to introduce input offset voltage of the proper polarity to null out any zero-scale error due to charge transfer.

Droop rate is minimized by the use of ion implantation. As a result, the sample-and-hold amplifier has rates comparable to those obtainable with field-effect-transistor versions, but without their severe temperature degradation. Where the droop rate of FET sample-and-hold circuits deteriorates with increasing temperature in the 0°C-to-70°C temperature range, the SMP-81 droop rate actually becomes better. Because of bias-current-canceling techniques, it actually goes through zero at approximately 70°C.

The multiplexers require very low crosstalk between channels and minimum susceptibility to damage from the inadvertent application of signal and power in the wrong sequence. This implies devices designed around a bipolar-FET approach. The MUX88 eight-channel multiplexer is a good example. It operates over a wide range of supply voltages, including single supply, and is pincompatible with most of the popular complementarymetal-oxide-semiconductor and FET multiplexers. Because operation is break-before-make, two channels can never be simultaneously applied to the output.

The companded 8-bit μ -law system, which has the equivalent resolution of a 12-bit system, makes heavy demands upon the comparator. For example, the input offset voltage should be small compared to 1.0 millivolt and the input offset current should be small compared to 200 nanoamperes. This requirement is satisfied by the CMP-01 precision comparator, which typically has 0.3-mv offset voltage and 25-nA offset current.

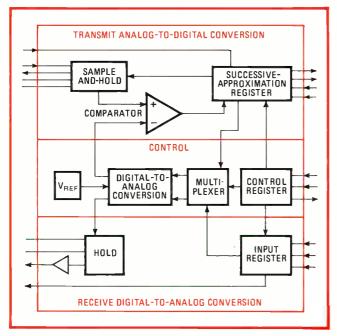
All codecs require precise references for the converters. The PMI REF-01 and REF-02 were designed for use with multiplying converters. A band-gap approach is used because the energy bandgap of silicon is a fundamental physical property and not a process variable. Compatible thin-film resistors and zener-zap trimming of the bandgap slope itself provide a stable, precise reference with a low temperature coefficient.

The companding converters required for d-a conversion have internal ladder networks that make them applicable in almost any codec configuration. They are capable of decoding up to 32 channels at the CCITT 2.048-megabit rate.

In conjunction with the sample-and hold amplifier, comparator, and successive-approximation register, the companders can easily encode 8 to 12 channels. In transceiver applications, the encode/decode pin may be sequenced so that the same device may be used for both encode and decode. $\hfill \Box$

N-MOS codec packs in analog and digital circuitry

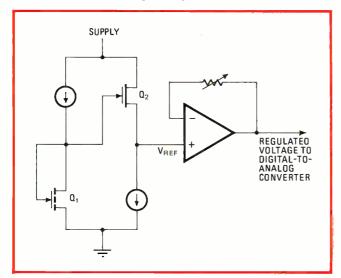
by Ben Warren, John Huggins, and Marcian Hoff, Intel Corp., Santa Clara, Calif. □ A single-chip coder-decoder can be an elegant, economical, and highly reliable integrated circuit, but it can be even more than that. The use of n-channel silicon-gate metal-oxide-semiconductor technology permits a versatile large-scale integrated codec that packs in many extra analog and digital functions. As well as enhanced capability, the n-MOS process allows a voltage reference on chip, and one that needs no precision components or external adjustments at that. The result is



Small and capable. The single-chip-per-channel 2910/11 meets the specifications of North American and European standards for PCM codecs. It performs all conversion functions and, when interfaced with a microcomputer, performs time-slot computations.

the 2910/11 pulse-code-modulation codec. The 2910 conforms to the North American PCM protocol, and the 2911 is designed for the European protocol. Each is a metal-mask option of a basic chip.

Use in the telephone system puts stringent requirements on this IC. It must perform analog-to-digital and d-a conversion of voice data while meeting strict gaintracking, stability, and noise standards. The telephone industry specifies PCM encoding for compatibility with existing transmission facilities, and it also specifies framing, signaling, and companding laws.



1. Stable reference. To meet the stringent requirements for loop gain in a codec design, the d-a converter must have a precision reference. By using the difference in threshold voltage between enhancement-mode and depletion-mode devices for this purpose, temperature and supply effects are greatly reduced.

However, in approaching the design of a telephone codec, there are many options to be considered, in functions as well as in process technology. For example, codecs have been used primarily for transmission between switching centers, but a properly configured device could be useful in the switching systems themselves. Once digitized, voice signals could be routed by logic gates, rather than by analog switches.

All PCM codecs are intended for use in timemultiplexed systems, and the 2910 is designed to digitize the voice signal before it is assigned its time slot in the data stream. Thus each incoming analog line or trunk must have access to a codec. In such a setup, significant power and hardware savings can be realized with this chip. Because the input lines typically operate with relatively low duty cycles, it is designed to be quiescent when its input is inactive, and thus it will not occupy a time slot in the voice data stream or draw power from the supply. More hardware is saved because any 2910 can be assigned to any open time slot. This capability permits switching in small systems without needing additional logic in the data stream.

Reducing the burden on the system controller is another asset made possible by the 2910 codec. The part incorporates circuitry that permits it to perform the PCM multiplexing and demultiplexing operations at the right instant with no more input than a time-slot assignment and two bits to select the desired operational mode. Since microprocessors are rapidly coming into use as controllers for telephone switching systems, the 2910 is designed to operate much as an intelligent peripheral chip does.

Why n-channel?

Although some analog functions are included in modern n-MOS microcomputer and memory devices, the codec analog circuitry has not been implemented in an n-channel process previously. However, meeting the rigorous codec requirements means that, by extension, any low- or medium-speed analog LSI problem can be solved with the process. Also, the superior n-channel density in logic applications allows numerous analog and digital functions on the same substrate.

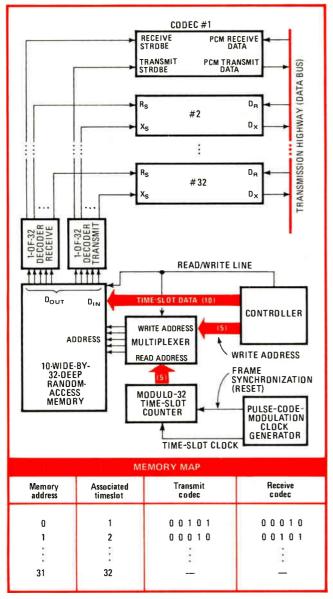
For example, with n-channel technology, chargetransfer devices and switched capacitors can be used to form economical filters. Furthermore, a random-access memory, a read-only memory, a programmable ROM, a-d and d-a circuitry, precision references, and additional codec logic are combined on the same substrate.

Buried-ion reference

All telephone networks need consistent gain in the transmission loop; therefore each codec-equipped line must perform its a-d or d-a conversion with a known stable insertion loss or gain. This requirement may be met by supplying the d-a converter with a stable reference voltage.

Such a reference may be added through the use of external precision components, but in this single-chip codec, the reference is built in. In any event, there are three key requirements that must be met.

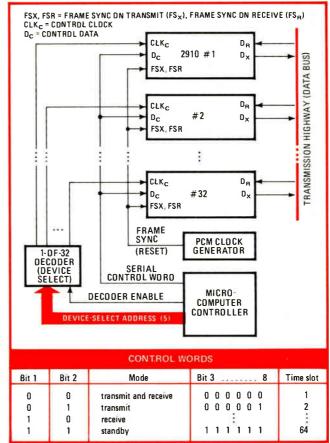
The first is initial accuracy at the device level. If each



2. External time slots. A common controller requires one RAM location for each time slot. Output and receive data are strobed concurrently. Two external memory words and time slots are required to establish a two-way conversation. The first two locations in the map indicate a call between codecs 5 and 2 in time slots 1 and 2.

block in the system is sufficiently accurate, no gain adjustment is necessary. Furthermore, the reference must not drift appreciably with age, for a change in gain over the 40-year normal life of a telephone system can cause its instability and failure. Reliable operation also requires low temperature and voltage coefficients. Finally, local generation of the reference is necessary. Verylow-level voice signals preclude designs that share the reference for many codecs (because system noise will interfere), as well as designs that distribute the reference signal any distance (because voltage drops accumulate).

To obtain the 2910's on-chip voltage reference, Intel uses its customary approach for standard two-layer polysilicon n-channel devices and two separate thresholdadjusting implants. These implants permanently lodge ions in the crystal-structure channel regions, which are



3. Local switching. A significant hardware reduction is achieved using the 2910 as a programmable switching element. Time slots for each direction are made independently over a single bit-serial input by shifting in an 8-bit control word specifying transmit, receive, neither, or both. The control words contain two fields: 2 bits to show the direction and 6 to define the time slot.

then sealed with a high-integrity thermal gate oxide. Diffusion of the ions is not measurable below 900°C, resulting in a very stable threshold. It is this stability that is the basis for the codec's reference.

The reference circuit (Fig. 1) generates a voltage equivalent to the difference in thresholds of devices Q_1 and Q_2 . Q_1 is an enhancement device, while Q_2 is a depletion device, and in such a configuration the temperature effects cancel and supply-voltage coefficients are greatly reduced. Thus V_{ref} variations over time, temperature, and supply can be held to less than 0.07 decibel.

Since the difference in the devices' thresholds, and hence V_{ref} , is a function of two separate implants, there is a chance for a mismatch that will lead to a stable but nonstandard voltage. Thus a trim circuit is included, which works by setting polysilicon fuses in an operational-amplifier feedback circuit. Manufacturing tolerance on this operation is ± 20 millivolts around a nominal 3.15 volts.

Time-slot assignment

A crucial function in any PCM system is assignment of the encoded voice to a time slot in the data stream. A codec that can take much of this responsibility can go a long way towards reducing system complexity and cost,

The quest for standardization

The vastness, complexity, and interdependence of telephone systems makes standardization an all-embracing rule, for economy as well as for successful operation. There are three basic aspects to this standardization, each of which bears upon the design of a successful coderdecoder chip.

First of all, there is component standardization, which benefits the device manufacturer, the system manufacturer, and the telephone company alike. There are two aspects: designing the codec as both a switching and a transmission device, and, as Intel has done, extending the versatility of software control to the codec.

The result is a part that can be used in all basic classes of telephone systems—not only transmission channel banks and central-office switching systems, but also remote line modules and concentrators, private automatic branch exchanges, key telephones, telemetry, secure communications, and other digital applications.

Secondly, there is system standardization. The manufacturer of telephone equipment generally seeks a production life cycle of 20 to 30 years in order to amortize the hefty costs of planning and developing systems that fit

improving reliability, and eliminating components in the circuitry common to all phones in the network. A comparison of systems will bring this out.

Figure 2 represents a small system with 32 codecs and a single transmission highway with 32 time slots (a system where the number of slots equals the number of phones is called nonblocking). For the sake of simplicity, only the select and data interfaces of the codecs are shown in the figure.

Local conversations in this system can be set up if the PCM transmit-data output of the caller's codec is strobed onto the bus at the same time that the PCM receive-data input of the listener's codec is strobed on. A common controller performs dynamic time-slot assignments with the help of a RAM that has an individual location associated with each time slot. Thus the memory must have enough locations to address or select all codecs in the system.

As the memory map in Fig. 2 indicates, there are two fields in each 10-bit word addressing the receiving codec. Of course, two memory words—and two time slots—are required to establish a two-way conversation.

The amount of hardware used is impressive. A pair of 1-of-32 decoders is required to select simultaneously one transmitting and one receiving codec in each time slot. The address multiplexer permits the controller to write new time-slot assignments into the RAM via the R/W line, and the 5-bit counter continuously sequences the memory through all 32 locations, once per time frame of the data stream. Moreover, the controller must maintain a record of all calls in progress, which generally requires a separate, more accessible memory (not shown).

In contrast, the same system built with 2910 codecs and a low-cost microprocessor or single-chip microcomputer (Fig. 3) can handle the time-slot assignment with a single 1-of-32 decoder for device selection. The controller can assign time slots for each direction of transmisinto their proper niches in the telephone network. Generally, his prices are based on such a life cycle, but he can be hurt badly if a basic system cannot be modified easily to follow the phone companies' changes in system architecture and service capabilities. Hence there is increasing emphasis on software control and microcomputers in new switching systems—and in the design of codecs.

Above all, there is network standardization. Here standards and practices exist so that wholesale modifications to the telephone network need not be made to accommodate new equipment. Since pulse-code modulation and time-division multiplexing are used for transmission between switching centers in most digital applications, network standardization benefits by the use of the PCM codec on the subscriber side of the switching system. Special interfaces and hybrids are therefore not necessary at the interfaces between systems.

In the long run, PCM and TDM standardization will extend to the other side of the switching system. Then interfaces will disappear as PCM switching-system highways are integrated with PCM span lines to satellite systems and with PCM trunk lines to other offices.

sion directly to each codec by shifting in an 8-bit control word over a single bit-serial input.

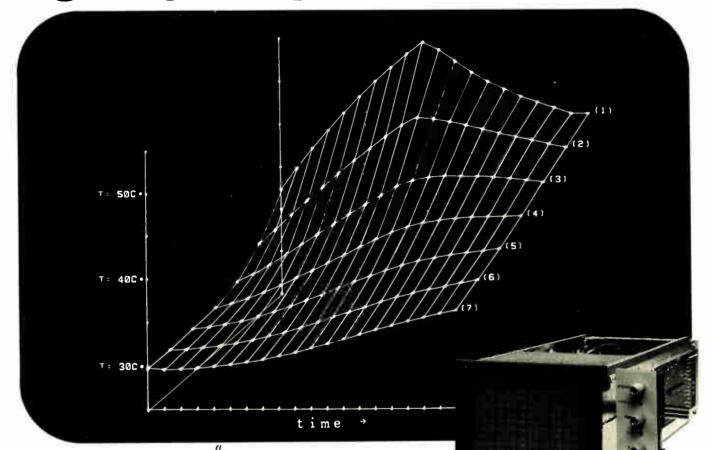
As the memory map in Fig. 3 shows, the control word contains two fields, the first specifying the mode of operation and the second specifying the time slot. If the mode field specifies neither transmit, nor receive, nor both, the codec enters a reduced-power standby state, and remains in it until another time-slot assignment forces it into activity. The only restriction in the clocking rate is that the 8-bit control word must shift in less than one frame, typically 125 microseconds. However, this shifting can be asynchronous with respect to all other 2910 clocks because the codec addressed will take care of any necessary synchronization.

These two system approaches demonstrate how onchip time-slot computation can reduce hardware and interface complexity. Similarly, reliability doubles with the on-chip interface. Since the time-slot logic is contained in each codec, the amount of critical common circuitry is reduced, thereby cutting the chances of a multiple-line failure.

The 2910 can be used as well in systems with 24 and 48 lines and also within the modules of larger systems. Nor is it restricted to nonblocking systems. In a blocking system, the number of codecs that can be handled is determined by the size of the requirement for simultaneous call handling. For example, blocking systems of 100 subscribers (and 100 codecs) may be served by a 24-channel network with dynamic time-slot assignment.

In addition to the savings in systems hardware, large savings in cabling can be realized. For example, a simple T1 line (a twisted pair in each direction) can link a central office with a remote line module, which may be blocking or nonblocking. A blocking module will act as a concentrator and may also have the capability to complete local calls, thus enhancing cabling and central-office equipment savings.

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Designer's casebook

Negative-output regulator tracks input voltage

by Gil Marosi Intech Function Modules Inc., Santa Clara, Calif.

By using an astable multivibrator in a flyback arrangement to develop negative voltages from positive ones, this regulator ensures that its output tracks the input, such that $V_0 = -V_{in}$. The voltage-controlled circuit requires only three active devices, all of them transistors.

 \dot{Q}_1 and Q_2 form the free-running oscillator, as shown in the figure. With Q_2 on, the V_{in} voltage is impressed across resistor L, causing the current through L to increase linearly. The peak value of current reached before Q_2 turns off will be directly proportional to the magnitude of the output voltage developed across capacitor C₄.

During the time the current through the inductor increases, no voltage can be developed across C_4 because diode D is back-biased. When Q_2 switches off, however, the collector voltage drops from V_{in} , and the capacitor charges to a negative voltage. This occurs because the charging current through the coil makes D turn on,

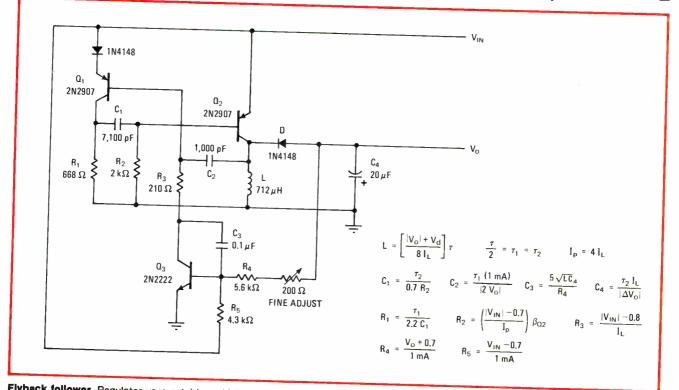
thereby causing a negative voltage at the output.

The field across L then begins to collapse and D is biased on, placing the output voltage $(V_o + V_d)$ across L, where V_d is the diode drop. The current through L must then fall linearly to zero. This completes one cycle of the flyback operation.

The input voltage is next compared with the output voltage at the summing node, at the base of Q_3 . This transistor amplifies the voltage difference and transforms it into a current that is used to control Q_2 's turn-on time. Thus if V_{out} should fall, the control current will act to increase the on time of Q_2 , thereby increasing the peak current through L and so raising the output voltage. This analysis assumes that V_{in} emanates from a stiff source—that is, an increased current demand will not cause a drop in V_{in} because of an increased voltage drop across the source's internal impedance.

Without Q₃, the load regulation would be directly proportional to a change in load current (I_L) and so a 10% change in I_L would cause a 10% change in load voltage V_L. Q₃ ensures that such a change in I_L causes only a 0.2% change.

Component values are given for a circuit that operates with an $I_L = 20$ milliamperes, a $V_o = -5$ volts, and an astable multivibrator operating at 50 kilohertz ($\tau = 20$ microseconds). Equations are given in order to facilitate the design of regulators for specific parameters.



Flyback follower. Regulator uses astable multivibrator $Q_1 - Q_2$ and inductor to generate negative output voltages from positive inputs while also ensuring that $V_{out} = -V_{in}$. Differential amplifier Q_3 serves to develop feedback control voltage to readjust on time of Q_2 and thus voltage developed across L and C₄ when $V_{out} \neq -V_{in}$. Component values are given for $I_L = 20$ mA, $V_o = -5$ V, and f = 50 kHz.

Controller selects mode for multiphase stepping motor

by Oldrich Podzimek Electrical Engineering Research Institute, Prague, Czechoslovakia

Offering a selection of the most common stepping modes, these circuits are an inexpensive solution to the problem of torque control in four- and five-phase motors. The mode can be changed simply by the flip of a switch.

The basic circuit is the same for either stepping motor. It consists of a 4-bit binary-coded-decimal counter, a BCD-to-decimal converter, and several gates that serve as phase detectors.

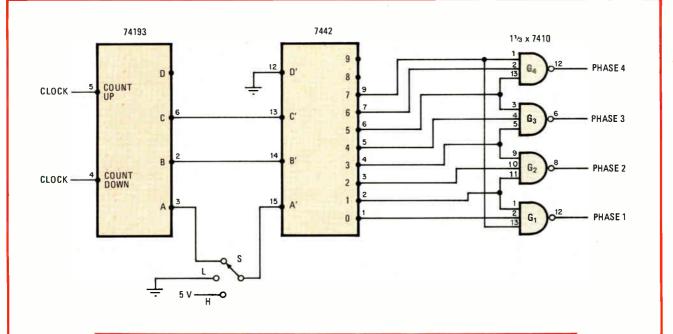
The four-phase controller is shown below. The 74193 counter advances with each input-clock pulse at a frequency determined by individual requirements. Note

that the 74193 can count up or down and so may be used to step the motor in the opposite direction if desired.

As the counter increments or decrements, the output of the 7442 4-to-10-line decoder switches in a manner dependent on switch S. If S connects port A' of the 7442 to the A port of the 74193, the decoder's output will move from 0 to 7 in sequence. Otherwise, the output will switch to even values every other count (S connected to logic 0) or switch to odd values (S connected to logic 1).

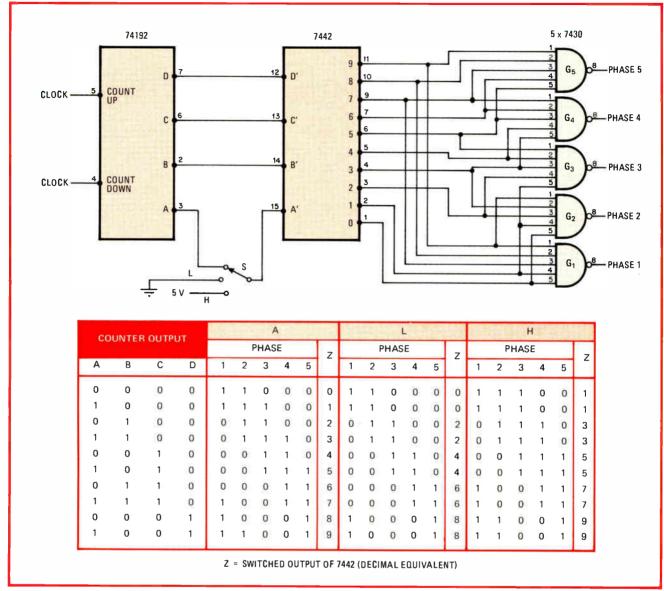
A combinational logic circuit using gates G_1 - G_4 converts the 7442's output to phase information in order to drive the motor. As can be seen in the truth table, either one or two windings of the motor will be active at any given time.

The motor will step most smoothly when S is connected to A. When S is connected to L, the step angle will be doubled, and only one of four motor windings will be excited at any given instant, thereby improving the efficiency of the step operation for a given torque. Note that when S is in the H position, the step angle will be the



	COUNTER OUTPUT						А	16				L.	H							
COUNTER COTFOT				РН/	ASE		z		PH/	ASE		z		PH/	ASE		z			
А	В	С	D			1	2	3	4	2	1	2	3	4	2	1	2	3	4	2
0	0	0	0	OR	1	1	0	0	0	0	1	0	0	0	0	1	1	0	0	1
1	0	0	0	OR	1	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1
0	1	0	0	OR	1	0	1	0	0	2	0	1	0	0	2	0	1	1	0	3
1	1	0	0	OR	1	0	1	1	0	3	0	1	0	0	2	0	1	1	0	3
0	0	1	0	OR	1	0	0	1	0	4	0	0	1	0	4	0	0	1	1	5
1	0	1	0	OR	1	0	0	1	1	5	0	0	1	0	4	0	0	1	1	5
0	1	1	0	OR	1	0	0	0	1	6	0	0	0	1	6	1	0	0	1	7
1	1	1	0	OR	1	1	0	0	1	7	0	0	0	1	6	1	0	0	1	7

1. Multimode. Step controller uses up-down counter, decoder, and logic to control excitation of four-phase motor windings. Switch S selects one of three possible operating modes, ranging from smooth-stepping to high-torque.



2. Multiphase. Controller for stepping five-phase motors is similar to that for four-phase case. Five 5-input NAND gates and some additional wiring are the only new changes required for enabling up to three phases of a motor to be excited simultaneously.

same as in the preceding case, but two motor windings will be active at any time, power input will be doubled, and 41% greater torque will be obtained.

A similar circuit suitable for stepping five-phase

motors is shown above. In this case, either two or three phases of the motor are excited simultaneously. This circuit can be extended to solve a general m-phase motor problem.

Op amps and counter form low-cost transistor curve tracer

by Forrest P. Clay Jr., Clarence E. Rash, and James M. Walden Old Dominion University, Department of Physics, Norfolk, Va.

For a curve tracer, this relatively simple circuit is unusually inexpensive. Used to test small-signal bipolar transistors as well as junction diodes, it generates the waveforms needed to display or plot their characteristic curves on an oscilloscope or X-Y plotter, interfacing directly with either. Operational amplifiers, one transistor, and a single binary counter are the only active devices needed.

Central to the circuit is a current generator made up of an op amp driven by the counter. It supplies eight levels of base current in sequence to the transistor under test. Op amps A_1 and A_2 , with the aid of the R_1 - R_2 - C_1 timing network, initially produce both square and triangular waves at test points A and C (TPA and TPC), respectively. S_1 selects the waveform frequency—either

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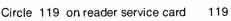
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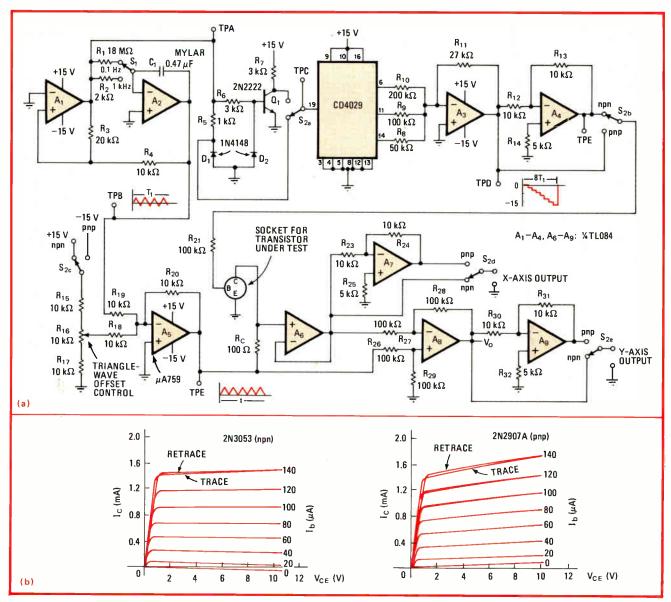
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Current family. Tracer produces set of eight curves of collector current vs collector voltage from npn or pnp transistor under test. Diodes may also be checked in circuit's pnp-transistor mode (a). Representative curves are plotted using X-Y recorder (b). Note temperature effects seen on the retrace portion of curves for higher values of I_b and I_c .

1 kilohertz for output onto an oscilloscope or 0.1 hertz for plotting with an X-Y recorder.

The waveform at TPA is then shaped by D_1-R_5 or D_2-R_6 into a clock pulse suitable for the 4029 binary counter. The signals emanating from the Q_a , Q_b , and Q_c ports of the counter, when fed into a binary-weighted summation network (R_8-R_{11}), produce an eight-step staircase waveform at the output of A_3 or A_4 , depending upon whether a pnp or npn transistor is under test. The actual base current value is determined by appropriate selection of R_{21} . The collector current can be calculated from $I_c = V_o/R_c$.

Both the collector-biasing voltage for the transistor under test and the linear-deflecting voltage for the X-axis output to the scope are derived from the triangle wave. The first voltage is obtained by using S_{2c} and R_{16} , which permit the proper dc component to be added to the triangle signal. Note that the Y axis is stepped at one eighth of the rate at which the X axis is scanned. Thus, if the sampling rate is 1 kHz, each of the eight current levels is swept at a rate 125 Hz, well above the rate at which flicker is detectable on a scope.

The circuit is easy to use. Simply place ganged switch S_2 into whichever position is correct for the type of transistor being measured (npn or pnp); place the transistor into the test socket; and apply circuit power. To test a diode, insert its anode and cathode leads into the emitter and collector sockets, respectively, and put S_2 in the pnp mode.

Figure lb shows two representative families of curves the circuit produced on an X-Y recorder for the two types of bipolar transistor. \Box

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$50 for each item published.

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MACRO-11 is an in-depth assembly language course.

Real Time Operating System (RT-11) teaches students to use RT-11 for program development.

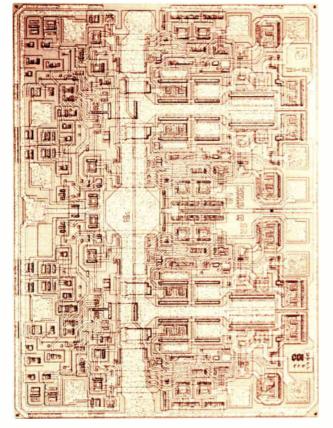
(3) On-site specialized training – reduces expenses and allows emphasis on points of particular value to your software needs.



Data goes faster, farther with chips for drivers, receivers

Family of Schottky devices meets new EIA electrical standards

> by David A. Laws and Roy J. Levy, Advanced Micro Devices Inc., Sunnyvale, Calif.



Typical die. The driver/receiver circuits in low-power Schottky technology are a cooperative effort of Advanced Micro Devices and National Semiconductor. This Am26LS29 die is 70 by 94 mils.

□ Hundreds of kilobauds, a mile of cable: today's highperformance data-processing systems can meet these demands with ease if their line drivers and receivers meet the Electronic Industries Association's new standards RS-422, -423, and -449. A designer turning to these in preference to RS-232-C will welcome a family of lowpower Schottky-technology quad receivers and drivers.

The new standards go far beyond the 20-kilobaud, 50-foot maximum requirements of the 10-year-old RS-232-C and move beyond its single-ended operation to include differential operation (see "What's the standard story?"). While they can be implemented with discrete circuitry and operational amplifiers, they are a natural for straightforward integration. However, the standards are sufficiently unfamiliar to warrant the discussion that follows of the new devices in terms of the requirements that spawned them.

These chips provide for unbalanced-transmission-line communications up to a 300-kilobaud rate or up to a distance of 4,000 ft with a 3-kilobaud rate, and balanced-line communication at a 10-megabaud rate up to 4,000 ft. Development of the dice was a joint effort between AMD and National Semiconductor Corp. Moreover, other manufacturers, including Texas Instruments Inc., are making members of the family.

Although these drivers and receivers were conceived for data communications applications, their performance makes them useful also for transmission among the various parts of a computer or central processing unit. So the EIA is considering the development of specifications covering their use in the party-line mode most favored in such applications.

The devices, labeled Am26LS29, -30, -31, and -32, are a family of quad drivers and receivers using Schottky transistor-transistor logic. Each chip incorporates four drivers or four receivers, together with control logic, in a standard 16-pin package.

RS-422 is implemented with a -31 driver and a -32 receiver. The single-ended RS-423 configuration is achieved with a -29 or -30 driver and the -32, which can be used as a single-ended or differential receiver.

Driving the lines

The -29 and -30 (Figs. 1a and 1b, respectively) consist of four single-ended line drivers designed to meet or exceed the requirements of RS-423. Buffered driver outputs are provided with sufficient source and sink current capability to drive 50-ohm transmission lines and large capacitive loads.

Each of the four driver inputs, as well as the enablemode control input, is a pnp Schottky input. Since there are two inverters between each input and output, the driver is noninverting. When operating in the RS-423 mode, the -29 and -30 require \pm 5-volt supplies. This setup allows the outputs to swing symmetrically about ground, producing a true bipolar output.

The -29 has a three-state output enable, while the -30 provides mode control, which permits operation as a dual differential driver. Each output of the -30 is designed to drive the RS-423 50- Ω load with an output voltage equal to or greater than + 3.6 v in the low state. Each output is also current-limited to 150 milliamperes in either state.

What's the standard story?

The most widely used standard for interfacing between data terminals and data communications equipment is the Electronics Industries Association's RS-232-C, which defines a single-ended, bipolar, unterminated circuit. It is intended for serial data interchange over less than 50 feet at rates under 20 kilobauds. A protocol as well as an electrical standard, it specifies handshaking signals between terminals and communications equipment.

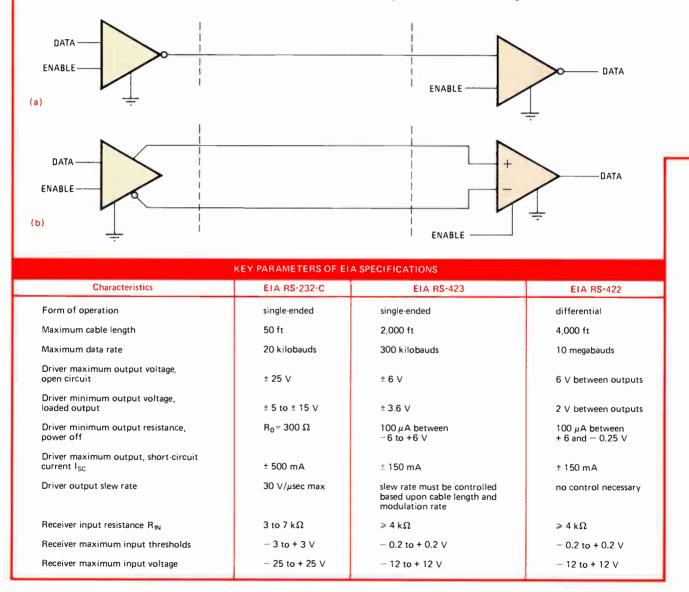
The single-ended circuit uses a single conductor to carry the signal with the voltage referenced to a single return conductor (part a of the figure). This conductor may also be the common return for other signal conductors. It is the simplest way to send data, as it requires only one signal line per circuit.

However, this simplicity is often offset by an inability to discriminate between a valid signal produced by the driver and the sum of the driver signal and externally induced noise signals, commonly called crosstalk. Also, operation in multiwire systems tends to produce radiated emission on neighboring circuits. These problems may be solved, but at the expense of circuit performance. Since noise and crosstalk are both directly proportional to transmission-line length and bandwidth, RS-232-C restricts both. To control radiated emission, it limits the slew rate of drivers to 30 volts per microsecond, which works with the length limitation to limit reflections on unterminated lines.

To allow the newer data communications systems to utilize their full performance capabilities, the EIA issued RS-422 and -423, two new electrical standards, in 1976. They define interface standards for higher data rates and longer distances than possible with RS-232-C.

RS-423 defines a single-ended, bipolar-voltage, unterminated circuit. It extends the distance and data-rate capabilities to 4,000 ft and 3 kilobauds. Higher rates of 300 kilobauds are permitted over a maximum of 40 ft.

RS-422 gives a balanced-voltage differential operation capable of significantly higher performance than are single-ended configurations. It can accommodate rates of 100 kilobauds over 4,000 ft or up to 10 megabauds over shorter distances. These improvements stem from the advantages of a balanced configuration, which is isolated



from common-mode currents among other pluses.

Differential operation (part b of the figure) is implemented by a differential driver (essentially two singleended drivers with one always producing the complementary output-signal level to the other), a terminated twistedpair transmission line, and a differential line receiver. The driver signal appears as a differential voltage to the line receiver, while the noise signals appear as a commonmode signal. A receiver with a sufficient common-mode voltage operating range can discriminate between them.

The adoption of these two standards made it necessary to fully specify the remaining functional and mechanical characteristics of the interface. Consequently, the EIA issued standard RS-449 in 1977. It describes a total of 30 interface circuits and defines 37-pin and 9-pin interface connectors and their pin assignments. The key features of the three new standards are shown in the accompanying table.

While these EIA standards define interfaces compatible with current integrated-circuit technology and provide significant performance advantages over the older standard, equipment designed to use these specifications can be made to operate with unmodified RS-232-C equipment.

A similar group of specifications has been defined by the international-standards groups of the CCITT (the International Telegraph and Telephone Consultative Committee). Recommendations V.10 and V.11 are essentially European equivalents of RS-422 and RS-423 respectively, and recommendations V.24 and V.54 are compatible with RS-449. In addition, the International Organization for Standardization's draft proposal DP-4902 describes the 37-pin and 9-pin interface connectors.

For both devices, a slew-rate control pin is brought out separately for each output to allow control of the output ramp rate (rise and fall time). This provides suppression of near-end crosstalk to other receivers in the cable.

Differential drivers

The -31 (Fig. 1c) is a quad differential line driver designed to meet RS-422 while operating with a +5-v supply. It has high-speed, skew-matched, differential outputs with typical propagation delays of 12 nanoseconds and residual skew of 2 ns. Both differential line outputs are designed for three-state operation to allow two-way half-duplex or multiplex party-line operation.

The -31's outputs are designed to source or sink 20 mA each, so that they can generate at least 2 v across a 100- Ω load, as required by the standard. It also meets the RS-422 requirement that the driver not load the line should its power supply fail.

Receivers

The -32 (Fig. 1d) is a quad line receiver operating from a +5-v supply, which can be used in differential or single-ended modes to satisfy RS-422 or -423 applications. The three-state outputs, which can sink 8 mA, incorporate a fail-safe input/output relationship that keeps the outputs high when the inputs are open.

The chip meets the required receiver input specification of a ± 200 -millivolt threshold sensitivity over a $\pm 7v$

common-mode range. The same circuitry assures excellent rejection of the power-supply ripples that can be troublesome when switching the high currents involved in a system's interfaces.

A typical hysteresis of 30 mv provides the -32 with differential noise immunity. This feature is important since signals received on long lines can have slow transition times; without hysteresis, a small amount of noise around the switching threshold can cause erroneous sensing in the receiver output.

A mask option—the Am26LS33—on the -32's input resistors modifies the receiver to improve operation in environments with high common-mode noise. An inputdifferential, or common-mode, voltage range of ± 15 v is achieved at the expense of a minor decrease in input threshold sensitivity (to ± 500 mv from ± 200 mv) over the common-mode range.

Implementing the circuits

Integrating these drivers and receivers did pose some special design challenges. A particular requirement of the -29 shown in the opening figure and the -30 was to provide a high output impedance in the power-off and disable mode over a wide common-mode range.

Output circuitry similar to a TTL totem pole meets these challenges. The chief modification is an added controlled current source to supply the high-current symmetrical drive required by the output transistors in both source and sink modes. The current source is designed around a pnp current mirror.

With the -31 balanced differential line driver, the challenge is the RS-422 requirement for very low residual skew between true and complementary outputs (typically 2 ns). An emitter-coupled differential amplifier and a symmetrical balanced drive are the answer.

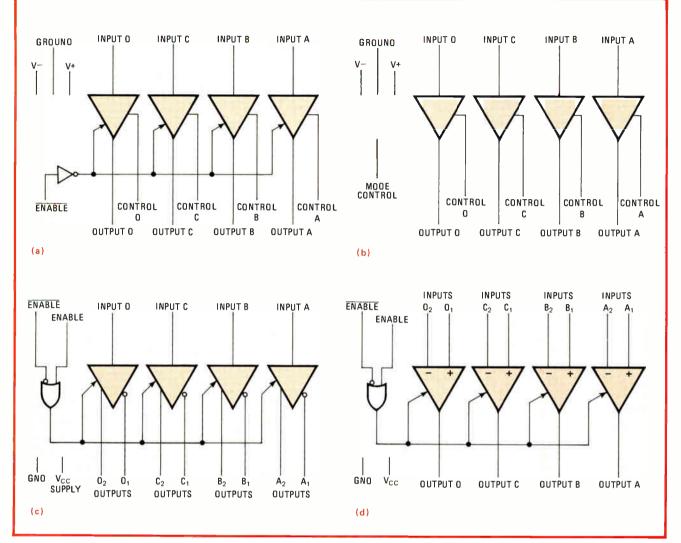
The -32 receiver must detect differential input signals of less than 200 mv over a 7-v common-mode range, difficult to achieve with a single 5-v supply. Providing the necessary hysteresis also is a consideration. A balanced pair of differential amplifiers with Darlington inputs and a very tightly matched resistor attenuation network meet these requirements. It is balanced so that the common-mode range is achieved outside of the operating V_{∞} range.

System applications

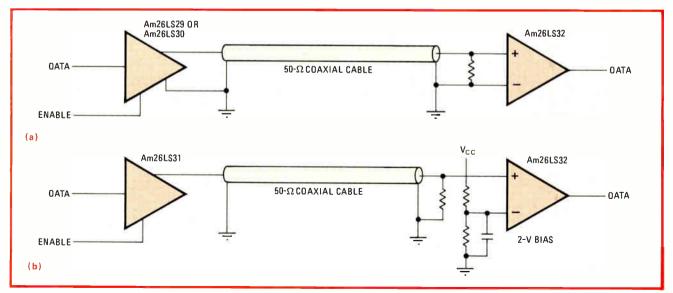
The Am26LS29-33 series can be combined in several configurations for data communications networks. A unidirectional RS-423 communication link can be constructed using the -29, -30, and -32 (Fig 2a). Either the -29 or -30 will meet bipolar signaling requirements.

If a single-ended line is needed without a bipolar requirement (Fig. 2b), the -31 can be used by biasing the reference terminal of the receiver to about 1.5 v. A balanced-line, single-direction RS-422 application uses the -31 and -32 (Fig. 3a). If bidirectionality is required, an extra termination should be added (Fig. 3b).

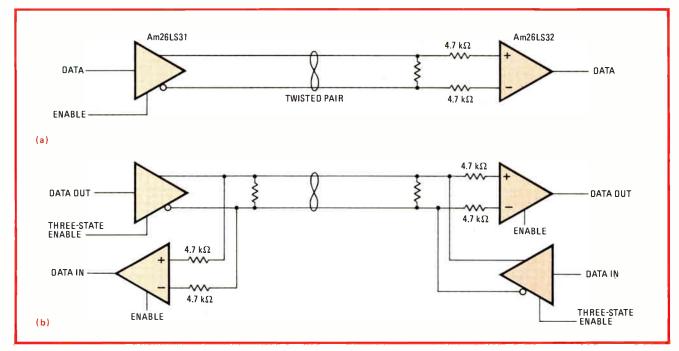
In the party-line mode found in intercomputer communications, the most common usage is that of a four-wire, full-duplex exchange system (Fig. 4). This mode involves two pairs of wires each handling a single direction of traffic. While this design is simple to imple-



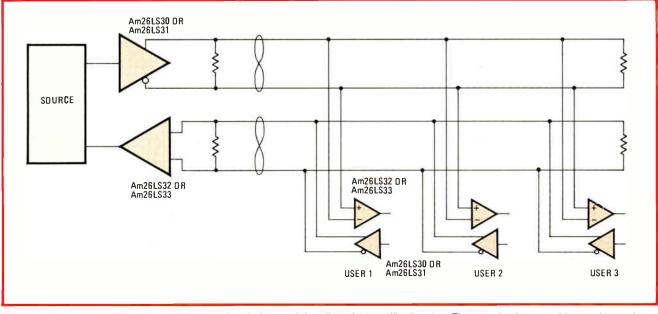
1. What's inside. The Am26LS29 driver (a) has a three-state output control, while the Am26LS30 driver (b) has a mode-control input that allows it to operate as a dual RS-422 driver or as a quad single-ended device. The Am26LS31 receiver (c) has common enable and disable functions while the Am26LS32 receiver (d) has complementary enable and disable functions.



2. Single-ended line. Unidirectional lines can be either bipolar (a) or nonbipolar (b): the configuration chosen depends on external circuit and system requirements. In either case, the line-driving and -receiving requirements of RS-423 can be satisfied.



3. Balanced line. Additional $4.7 + k\Omega$ resistors improve the fail-safe margin in both the single-direction (a) and bidirectional (b) RS-422 applications. The bidirectional connection requires twice as many components. Still other configurations are possible for special applications.



4. Party line. In this intercomputer mode, two pairs of wires each handle a single traffic direction. The outgoing has one driver and n receivers, and the incoming has one receiver and n drivers. As many as 12 users can be serviced. Most design problems involve system ground.

ment, problems arise with system ground. If the network of receivers and drivers spans a distance of a foot or more, ground-loop noise may develop. This noise changes the voltage that appears at the terminals of all receivers and drivers, referenced to the one driver that is active.

This induced, or system-developed, voltage is referred to as common-mode voltage (V_{CM}) and must be considered as a device parameter. RS-422 specifies the V_{CM} capability of receivers but not drivers. If the distances in the system are less than a fourth of the equivalent wavelength of the maximum data rise and fall times, the V_{CM} can be assumed to be minimal. Then drivers such as the -31 with single-voltage supply and limited negative V_{CM} can be used.

If the system dimensions are large, the V_{CM} will cause problems: the driver will clamp to ground the moment the line voltage swings below -0.5 v relative to any driver ground. This clamping will cause a short in the line and increase level shift and noise. It is caused in part by conduction of the integrated-circuit substrate diode. The problem can be avoided by using a driver such as the -30, which guarantees an output V_{CM} range of about ± 12 v about the driver ground reference.

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Integrated ac-dc-parametric capability does it. The L135 offers many analog force-and-measure functions through matrix connections, all completely integrated into system hardware and software. If these capabilities aren't integrated into the test system, they must often be added to accommodate the increasing analog content of LSI boards. That prolongs test time and slows diagnosis considerably.

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9. The L135 has enough clock-rate channel capacity for the big jobs.

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Immediate-response debug software does it. During testplan debugging, the L135 responds to the test engineer's commands and displays results immediately. Total debugging time is cut to a fraction because the test engineer is not distracted by system delays; he can concentrate on his circuit and his test plan.

12. The L135 readily assembles the many parts of LSI test plans.

<u>Structure-merge programming</u> does it. Test plans originate in many places: manual patterns and circuit models, learned data from known good boards, circuit and device simulators, automatic pattern generators, etc. The L135's structure-merge software and its straightforward protocol assembles them all into a coherent package, saving your engineers hours of tedious and costly work.

For more information on these and other L135 features, write Teradyne, Inc., 183 Essex Street, Boston, Massachusetts 02111.



Coherence function and averaging boost confidence in spectrum measurements

by N. A. Pendergrass, Hewlett-Packard Co., Loveland Instrument Division, Colo. Digital technology and the fast Fourier transform can do more for the low-frequency spectrum analyzer than just increase its speed. They can add an altogether new and extremely useful capability to the instrument—the ability to measure coherence—and they can also significantly enhance the accuracy of existing measurement techniques by the use of averaging.

Coherence, time averaging, and rms averaging are all complicated statistical functions that are difficult to perform with analog methods. Seeing how they are implemented on the HP-3582 dual-channel spectrum analyzer [*Electronics*, April 27, p. 170] will demonstrate the power of these new types of measurement.

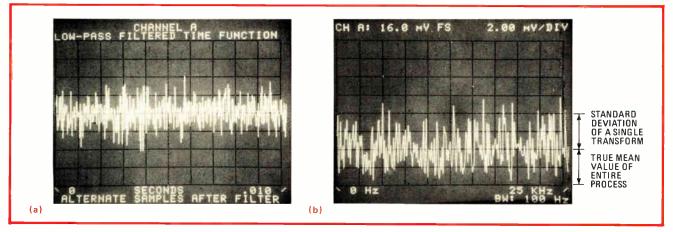
The need for averaging

In the real world, processes are often random or involve large random components. The evaluation of a signal spectrum containing random components requires averaging if the estimate is to be accurate. Indeed, to obtain a perfect model of the spectrum would require sampling the waveform for an infinite time, and the calculation from a single segment of a random process could never more than approximate the true spectrum.

The voltage waveform displayed in Fig. 1a is white Gaussian noise sampled for 10 milliseconds by the HP-3582 spectrum analyzer. Figure 1b shows a single record of the spectrum of the same sample over a 25-kilohertz range. The true spectrum would be flat, but the singlerecord spectrum has rather large deviations about its mean magnitude, and such a degree of uncertainty allows little information to be derived from it.

Root-mean-square averaging of many more samples reduces this uncertainty. For instance, if the source of the white Gaussian noise shown in Fig. 1 is sampled 256 times and rms-averaged, the result is a nearly flat spectrum that resembles the true, or expected, spectrum (Fig. 2).

Since averaging many spectra can take a long time, especially at very small bandwidths, it is desirable to average only the number of values required to obtain the necessary level of confidence and smoothing in the estimate. Table 1 relates the 90% confidence interval to the number of averages required for Gaussian random input signals. In other words, 90% of the measurements on



1. Gaussian sample. The waveform displayed (a) is a single 10-millisecond sample from a Gaussian white-noise source. The single-record spectrum of the same noise source (b) illustrates the magnitude of the deviation from the flat spectrum ideally expected.

Gaussian noise will be within the interval indicated. Since noise is generally Gaussian or nearly so, the table should have wide application.

To use the table, first decide on the allowable statistical tolerance in decibels. Then find the number of averages having 90% limits that are within the tolerance bounds. For instance, if a ± 2 -dB accuracy band can be tolerated, then the 16-average routine is what is needed. Remember that the limits given are statistical, not absolute; they state that, on the average, the true value of amplitude will lie within the stated bounds in 9 out of 10 measurements.

For example, suppose that a random-noise source has been measured, 32 spectra have been rms-averaged, and a marker at 1,000 hertz shows a signal level of -55 dBv.

TABLE 1: 90%	CONFIC	DENCE	LIMITS	FOR R		RAGIN	۱G
		1	Numb	per of av	erages		
	4	8	16	32	64	128	256
Upper limit(dB) Lower limit(dB)		+ 3.0 - 2.2				+ 0.7 - 0.6	+ 0.5 - 0.4

In this case the table can be interpreted to indicate that the true signal amplitude has a 90% probability of being in the range of -53.6 dBv to -56.2 dBv.

Time averaging

Another technique for enhancing an estimate is time averaging. Unlike rms averaging, it does not smooth the spectra but reduces the noise relative to a desired signal. It would be very difficult to do without a digital approach and the FFT.

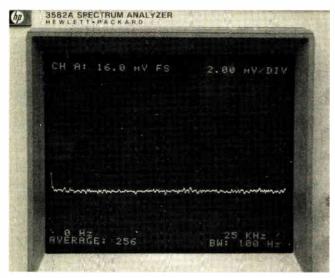
With this technique, input waveforms are first averaged as time records one after another. However, averaging several time records is exactly equivalent to vector-averaging the corresponding spectra one after another. This is done by taking the real and imaginary parts of the complex spectrum and averaging them over time (as opposed to rms averaging, in which the squared values of their magnitudes are averaged).

The noise-reducing action of time averaging is most easily understood in the frequency domain. Figure 3 illustrates how the resultant obtained by vector averaging at a given frequency causes the interfering signals' average to approach zero.

Time averaging is done with the aid of a synchronizing

Measure	t value of	Number of averages									
coherence function		16	32	64	128	256					
0.2	Η (dB)	+ 5.2, - 14.6	+ 3.8, -7.1	+ 2.8, - 4.2	+ 2.1, -2.7	+ 1.5, -1.8					
	φ (°)	± 54	± 34	± 23	± 16	± 11					
0.3	Η (dB)	+ 4.2, -8.4	+ 3.1, -4.8	+ 2.2, -3.0	+ 1.6, -2.0	+ 1.2, -1.4					
	φ (°)	± 38	± 25	± 17	± 12	± 8					
0.4	lΗl (dB)	+ 3.5, -6.0	+ 2.6, -3.6	+ 1.8, -2.3	+ 1.3, - 1.6	+ 1.0, - 1.1					
	φ(°)	± 30	± 20	± 14	± 10	± 7					
0.5	Η (dB)	+ 3.0, -4.5	+ 2.1, -2.8	+ 1.5, -1.9	+ 1.1, - 1.3	+ 0.8, -0.9					
	φ (°)	± 24	±16	± 11	± 8	± 5					
0.6	Η (dB)	+ 2.5, -3.5	+ 1.8, -2.2	+ 1.3, - 1.5	+ 0.9, - 1.0	+ 0.7, -0.7					
	φ (°)	± 19	± 13	± 9	± 6	± 4					
0.7	lΗl (dB)	+ 2.1, -2.7	+ 1.5, −1.7	+ 1.0, -1.2	+ 0.7, -0.8	+ 0.5, -0.6					
	φ (°)	± 15	± 10	± 7	± 5	± 4					
0.8	Η (dB)	+ 1.6, - 2.0	+ 1.1, - 1.3	+ 0.8, -0.9	+ 0.6, -0.6	+ 0.4, -0.4					
	φ (°)	± 12	± 8	± 6	± 4	± 3					
0.9	Η (dB)	+ 1.1, - 1.3	+ 0.8, -0.8	+ 0.5, -0.6	+0.4, -0.4	+0.3, -0.3					
	φ (°)	± 8	± 5	± 4	± 3	± 2					

Measured value of	Number of averages										
coherence function	<mark>16</mark>	32	64	128	256						
0.4	0.15, 0.59	0.23, 0.54	0.28, 0.50	0.32 <mark>,</mark> 0.47	0.34, <mark>0.45</mark>						
0.5	0.25, 0.67	0.33, 0.63	0.39, 0.59	0. <mark>42,</mark> 0.57	0.45, <mark>0.</mark> 55						
0.6	0.36, 0.74	0.45, 0.71	0.50, 0.68	0.53, 0.66	0.55, 0.64						
0.7	0.50, 0.81	0.57, 0.78	0.61, 0.76	0.64, 0.75	0.66, 0.73						
0.8	0.65, 0.88	0.70, 0.86	0.74, 0.84	0.76, 0.83	0.77, 0.82						
0.9	0.81, 0.94	0.85, 0.93	0.87, 0.92	0. <mark>88</mark> , 0.92	0. <mark>88</mark> , 0.91						



2. Smoothed spectrum. This spectrum of a Gaussian noise source is the result when 256 samples of the input are recorded and then rms-averaged. The spectrum resembles the ideal white-noise spectrum because of the smoothing action of rms averaging.

trigger signal. Assume that several time records of the same length, each starting at the trigger instant, have been taken and converted into the frequency domain by the FFT. The magnitude and phase of each time record then corresponds to a frequency component of the input spectrum.

At each frequency component, the signal can be separated into two parts: one that is at some fixed phase ϕ , relative to the trigger, and one that is not (Fig. 3a). The latter might be noise or an interfering signal, but its phase angle θ on successive samples is random relative to the trigger (Fig. 3b). Since the interfering signal is not fixed in phase from record to record, its vector average will approach zero (Fig. 3c). On the other hand, the signal component, being phase-synchronous vis-à-vis the trigger, is unaffected because it has the same phase at each sample.

An interfering signal or noise, therefore, can be reduced by time averaging if a suitable trigger is available. The magnitude in decibels of the improvement in the signal-to-noise ratio is approximately 10 \log_{10} (K), where K is the number of averages. For example, if 256

time records are averaged, the s/n ratio is improved by about 24 dB.

Notice that time averaging does not smooth the spectrum estimate—it only reduces the magnitude of an interfering waveform. The spectrum of any interfering noise that remains will be much smaller but decidedly ragged (Fig. 4).

The coherence function

The coherence function when used on a transfer function measurement is the fraction of output power attributable to an input signal. It is unique to digital implementations of network and spectrum analyzers and yields a lot of information about several hard-to-measure factors. It gives insight into the accuracy with which the transfer function of a noisy system is being measured at each frequency point. It can be used to compute s/n ratio at an output or to draw attention to nonlinearities in the system under test. It can also be used to study causeand-effect relationships between possible noise sources and the waveforms at other points in a system.

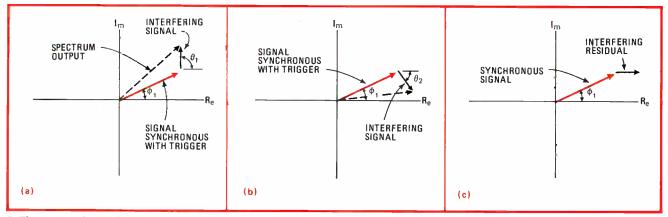
Perhaps the best way to see how the coherence function can do all of these things is first to examine how it is computed along with a transfer function in the HP-3582. Then the situations that do not involve the transfer function become more comprehensible.

Consider the transfer function measurement shown in Fig. 5. Notice that there is added noise that could interfere with the measurement accuracy. This is not unusual—the extra noise could be room sounds in loud-speaker testing, noise in measurement transducers such as accelerometers, or simply the noise that is produced by an amplifier.

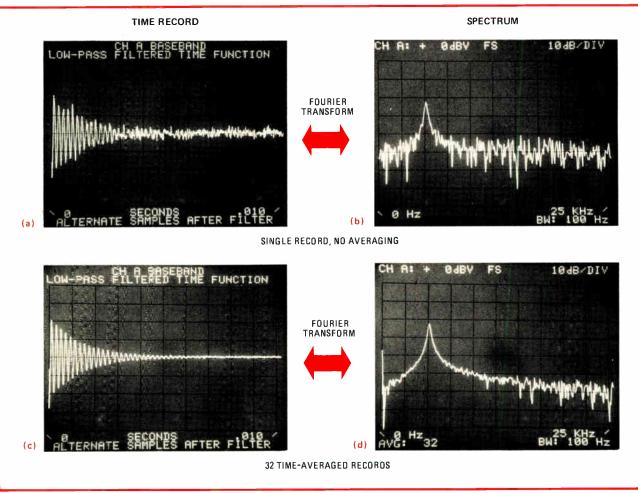
The usual approach for measuring the transfer function is to estimate the input $S_A(f)$ and the output $S_B(f)$ and then find the transfer function H(f) by dividing output by input spectra and subtracting their phase angles:

$$|\mathbf{H}(\mathbf{f})| = \frac{|\hat{\mathbf{s}}_{\mathbf{B}}(\mathbf{f})|}{|\hat{\mathbf{s}}_{\mathbf{A}}(\mathbf{f})|}$$

at angle $\phi_B - \phi_A$ where the symbol $\hat{}$ is used to indicate an estimate. But if the noise spectrum $S_N(f)$ is significant in any portion of the spectrum of the output $S_B(f)$, this traditional approach will give rise to errors because $S_B(f)$



3. Time-averaging action. The vector diagram above represents two (trigger-synchronized) FFT output samples and their vector-averaged resultant. Each signal contains random-noise components that approach zero when vector-averaged together.



4. Noisy damped sinusoid. The two sets of time and spectrum waveform displays illustrate the kind of improvement in s/n ratio possible when even as few as 32 samples are time-averaged. Only the contribution made by noise to the spectrum is reduced.

has energy in it that has not come from the input. For example, the noise spectrum could be masking a notch or some other irregularity in the transfer function.

In the digital approach there is a mechanism for reducing the effect of the interference. The technique involved is similar to the time averaging described previously. It uses the so-called cross-power spectrum $S_{AB}(f)$, which is estimated by taking the complex values of the $S_A(f)$ and $S_B(f)$ spectrums and forming the complex-conjugate product. The magnitude of this computation is simply the product of the $S_A(f)$ and $S_B(f)$ magnitudes. Since the complex-conjugate product is desired, the phase θ is the difference between the $S_B(f)$ and $S_A(f)$ phases as shown in Fig. 6.

Cross-power spectrum

The resulting complex values are vector-averaged over time as in time averaging. That is, the real parts are averaged and the imaginary parts are averaged. The estimate of the cross power spectrum is:

$$\hat{s}_{AB}(f) = \frac{1}{N} \sum_{i=1}^{N} \hat{s}_{Ai}^{*}(f) \cdot \hat{s}_{Bi}(f)$$

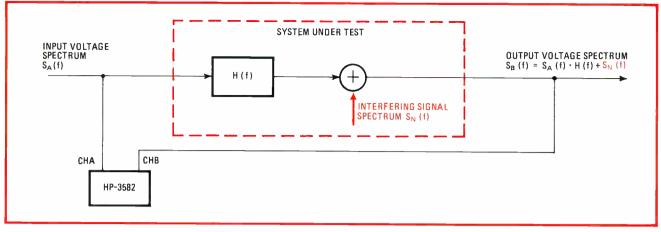
where the superscript * indicates the complex conjugate, N is the number of averages, and the subscript i refers to the results of the ith spectrum taken. If there is no noise present, the input and output spectral values are related in phase by the transfer function phase. Therefore, the phase of $S_{Ai}^*(f) S_{Bi}(f)$ is the same from record to record since there is no noise and the values of the complex-conjugate product simply accumulate without cancellation as additional records are taken as shown in Fig. 6c.

Noise-generated output

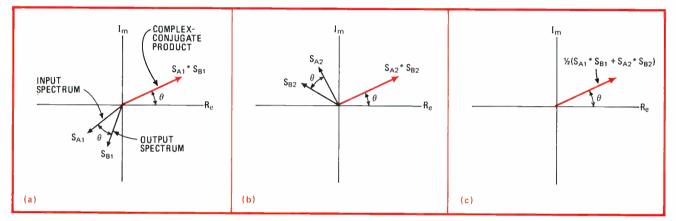
Now suppose that the input signal is not reaching the output at all, but only the noise spectrum is present there, so that $S_B(f) = S_N(f)$. The noise spectrum, or output in this case, has a random phase relative to the input (Fig. 7).

Therefore, the complex-conjugate product $S_{Ai}^*(f) \cdot S_{Bi}(f)$ has a different phase at each record taken and the vector average cancels, causing the magnitude of the resultant to approach zero.

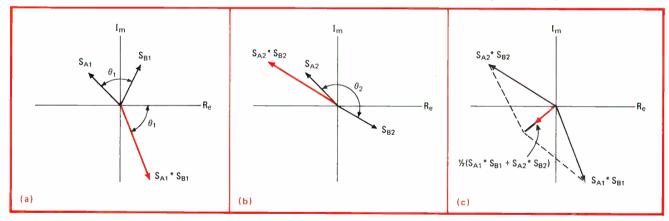
In a situation where noise is mixed with the desired signal, the noise cancels toward zero, as above, while the signal due to the input is undiminished. Therefore, the cross-power spectrum estimate converges with averaging to be just the product of the input spectrum and that part of the output spectrum that results from the input. It has the phase angle of the transfer function. Mathematically stated:



5. System measurements. Block diagram shows a typical transfer-function measurement setup using the HP-3582 dual-input spectrum analyzer. The output containing additional noise has been injected by a source somewhere in the system.



6. Noise-free. The complex-conjugate products of two records (a, b) are vector-averaged to yield the cross-power spectrum (c). Since no noise is present, they are all related by the transfer function's phase angle (θ) , and no cancellation in magnitude takes place.



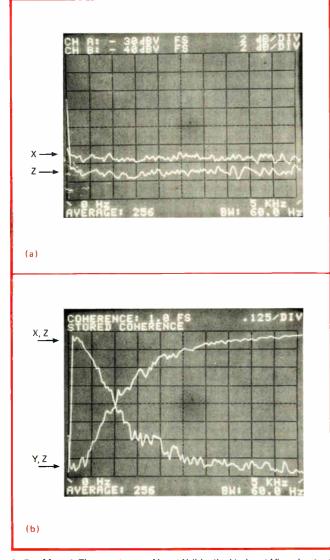
7. Input lost. With only noise generating the output, the magnitude of the cross-power spectrum resultant that will be formed (c) will approach zero because of the random phase relationship of each vector-averaged complex-conjugate product (a, b).

$$\lim_{A \to B} S_{AB}(f) = S_{A}^{*}(f)[S_{A}(f) \cdot H(f)] = |S_{A}(f)|^{2} \cdot H(f)$$

ave + ∞

The cross-power spectrum gives the handle needed to reduce the effect of noise in the measurement, since the transfer function estimate is easily obtained by dividing the cross-power spectrum estimate by the square of the magnitude of the input spectrum estimate. This is a much better estimate of the transfer function than the one described earlier and is used in the HP-3582. The coherence function also depends on the crosspower spectrum to remove the part of the output (noise) that is not consistently phase-related (or coherent) with the input. The coherence function γ^2 is defined as the squared magnitude of the cross-power spectrum divided by the magnitude squared of both the input and output spectrums, or:

$$\gamma^2 = \frac{|S_{AB}(f)|^2}{|S_A(f)|^2 |S_B(f)|^2}$$



8. Dual input. The spectrums of input X (identical to input Y) and output Z are shown in (a) but reveal little about X's and Y's contributions to output. The coherence functions between each input and output (b), however, show what each input contributes to the output.

The discussion of the cross-power spectrum should make one important property of the coherence function obvious. The function gives that fraction of the power at the output of a transfer function that came from the input. The cross-spectrum estimate converges to the product of the input and the output due to the input. Therefore, the numerator of the coherence does not have the noise in it, but the denominator does. Mathematically, then, this yields the ratio of power out due to input exclusive of noise to the total power out including noise:

$$\lim_{\text{ave } \neq \infty} \gamma^2 = \frac{|S_A(f)|^2 \cdot H(f)|^2}{|S_A(f)|^2 \cdot |S_B(f)|^2} = \frac{|S_A(f)|^4 \cdot H(f)|^2}{|S_A(f)|^2 \cdot |S_B(f)|^2}$$
$$= \frac{|S_A(f)|^2 \cdot |H(f)|^2}{|S_B(f)|^2}$$

This is an important interpretation of the coherence function. That is, over frequency it gives a measure of that fraction of output that came from the input only. The s/n ratio is then given by $\gamma^2/(1-\gamma^2)$ where $(1-\gamma^2)$ is the fraction of the output that is noise. Note that γ^2 always has a value between 0.0 and 1.0. A value of 1.0 indicates perfect coherence.

System nonlinearities

Nonlinearities in a transfer function measurement generate distortion products and cause portions of the input signal at one frequency to appear at others. If the input signal is not periodic, as is the case with noise, the phases of the distortion-produced signals will be random relative to the actual input at the distortion product frequencies. The distortion products are eliminated by the converging action of the cross-power spectrum computation in just the same way as the interfering noise is. The transfer function measurement when made with the cross-power computation and averaging reduces the nonlinear effects, whereas if done by the simple division method, it could again result in a significant error. The coherence function indicates the presence of nonlinearities by yielding values less than 1.0 at those frequencies where distortion products are present, assuming no interfering noise is present.

All along in this discussion, the term "estimate" has been used. In the face of significant noise or nonlinearity, averaging must be used to smooth the transfer function and coherence computations and reduce the errors.

If averaging is not used, the transfer function obtained by using the cross-power method may be inaccurate. The coherence will compute to 1.0 in this case even if interference is present. Of course, if nonlinearities or interference are not present, then the computations are accurate without averaging unless a random input is used (see Tables 2 and 3).

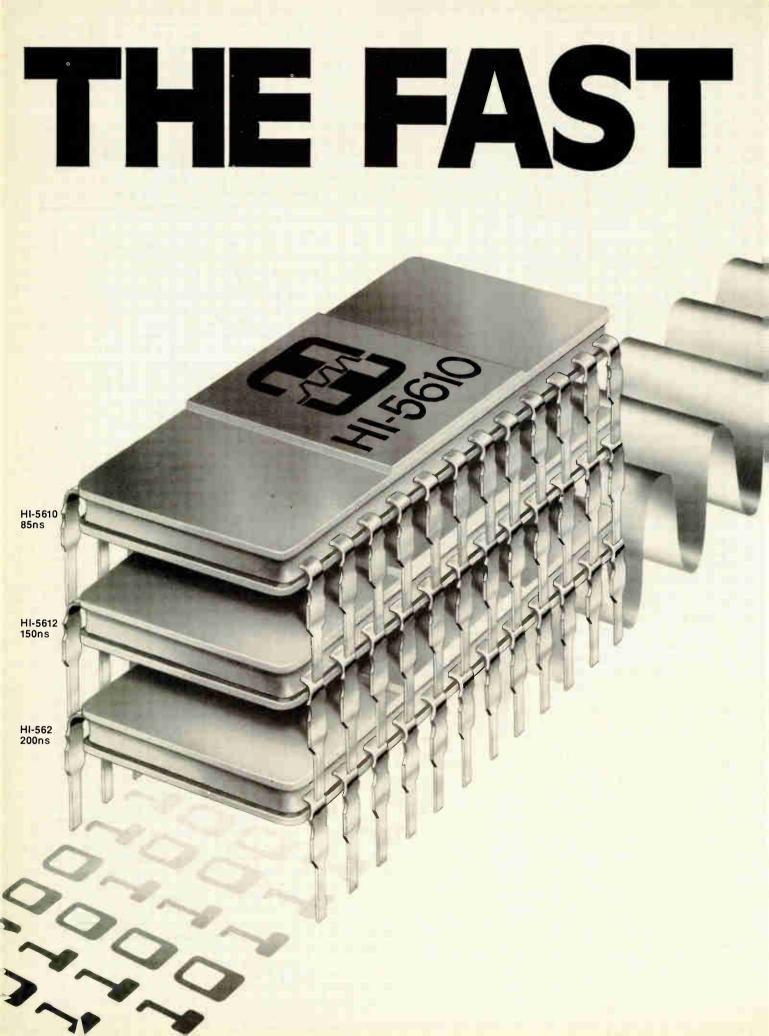
Multiple inputs

The coherence function is particularly useful when investigating cause-and-effect relationships in multipleinput systems. It gives a measure of how much output power (either desirable or undesirable) at a frequency can be attributed to each input source without modifying the operation of the system under test. (Mechanical vibration occurring at full throttle in a twin-engine plane is one example.)

Consider the system shown in Fig. 8, which has two possible sources of noise at the output. Usually some unknown transfer mechanism is involved and often the offending sources cannot be selectively turned off.

In this example, it is determined that source X is a white noise and so is source Y. The output spectrum at Z is also found to be nearly white, as shown in Fig. 8a. But which source is the offender?

Both the transfer and coherence functions can help answer the question. The coherence functions measured between X and Z and then Y and Z are shown in Fig. 8b, indicating that not one but both sources contribute to the output noise. The only difference between sources is in how much noise they contribute versus frequency. Note that each source accounts for a coherence of 0.5 or 50% of the output noise at the 1,000-Hz intersection. Thus the coherence function shows the transfer functions are balanced, giving the output a nearly flat spectrum.



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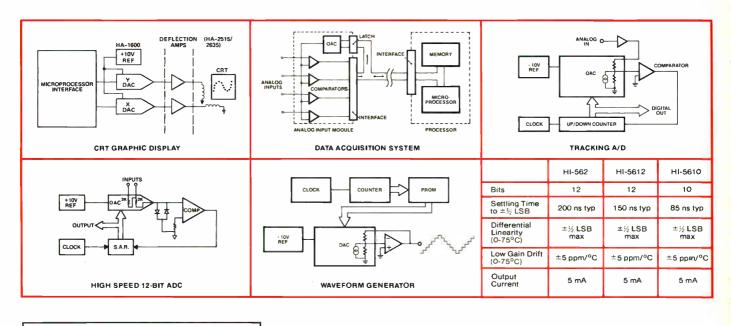
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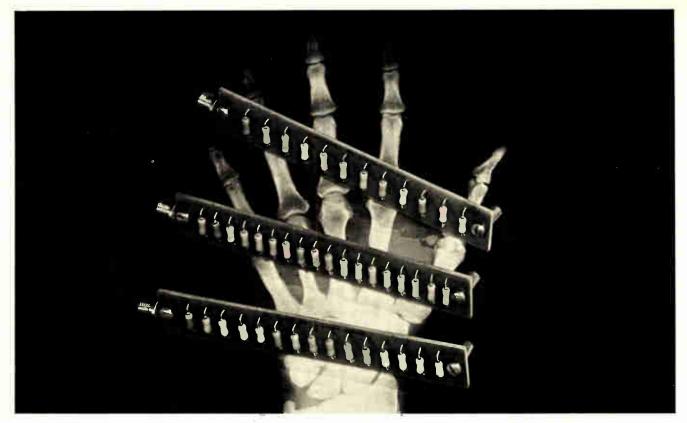


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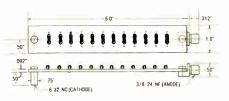




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Why switching power supplies are rivaling linears

Use of power transistors instead of a bulky transformer keeps efficiency high, size small, and power consumption low

by Malcolm Burchall, Gould Inc., Electronic Components Division, El Monte, Calif.

□ Today's switching regulated power supplies are beginning to compete with linear types for the system designer's vote. They certainly deserve it if efficiency, small size, and low power consumption are what he wants most. And sometimes, in the context of a particular system's overall requirements, they may still be the better choice despite their greater noise, slower transient response, higher ripple, and generally higher price.

The virtues of the switching power supply stem from its smaller size. Its vices, on the other hand, stem from what makes that smaller size possible: the substitution of a high-frequency switching system based on power transistors for the bulky 50-to-60-hertz input transformer of the linear supply.

Approximately 80% of the linear supply's bulk is accounted for by three components: the input transformer, the reservoir electrolytic capacitors, and the heat sinks (Fig. 1). The transformer provides input/output isolation and reduces the relatively high input voltage to a level more nearly matching the required dc output level. The reservoir electrolytic capacitors perform two functions: they store enough energy to keep the output in line with the specifications in the event of short interruptions in the input, and they filter the raw, rectified dc from the rectifiers to an acceptable level. The heat sinks are needed to cool the power-dissipating components (rectifiers and series-pass transistors).

In the switching regulated power supply, most of the bulky components are replaced by solid-state circuits (Fig. 2). The switching system uses power transistors that turn on and off at rates of 20 kilohertz or more, the ratio of their on to off time being determined by a detector-amplifier configuration. This high-frequency operation allows smaller components to be used for the energy-storage capacitor, rectifiers, and filtering network. Being small, all these elements dissipate less heat and therefore need less—sometimes nothing—in the way of heat sinking than their larger linear counterparts.

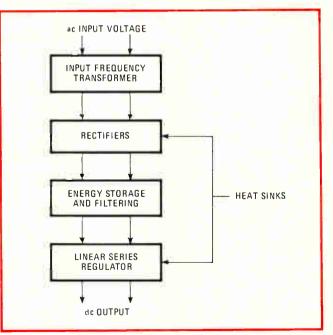
Efficiency, size and weight

All other things being equal, then, linear power supplies have lower efficiencies. The usual efficiency for a good linear under nominal operating conditions is about 50%, and even the best of the new high-efficiency linears achieve only 53% to 56%.

Switchers, on the other hand, typically have 75%

efficiencies, with some claims as high as 85%. To provide an output of 100 watts, a 133-w input is required of a switcher, while 200 w, at least, would be needed for a linear. The linear supply's efficiency is also highly dependent on the input line voltage, unlike the efficiency of the switcher, which is considered a theoretically lossless pulse-width-modulated device. As such, it acts as a dc-to-dc transformer that keeps output power constant by compensating for an increase in input voltage by a decrease in input current.

Another consideration is power loss density, or the power dissipation of a given group of components expressed in terms of their volume. For similar types of equipment, the maximum power loss density is determined by the temperature rating of the components used, the ambient temperature, and the method of heat extraction used (convection or forced cooling). Theoretically, this means that a switcher producing 100 w of output power with an internal loss of 33 w can be one third the size of a linear power supply that has an



1. Conventional. Sizeable linear power supply consists for the most part of large input transformer, bulky electrolytic capacitors, and large heat sinks for the rectifiers and regulator.

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ISO 1745-1975	Information processing—basic mode control procedures for data communications systems	
ISO 33 <mark>0</mark> 9-1976	Data communication—high-level data link control procedures— frame structure	

American National Standards Institute 11 standards, including...

X3.4	Code of information interchange
X3.24	Signal quality at interface between data processing technical equipment for synchronous data transmission
X3.36	Synchronous high-speed data signaling rates between data terminal equipment and data communications equipment
X3.44	Determination of performance of data communication systems
	al Standards

11 standards, including...

- FED-STD-1003 Bit oriented data link control procedures FED-STD-1010 ASCII bit sequencing for serial-by-bit transmission
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A subsidiary of Loral Corporation

Digital differentiator determines shaft acceleration

by N. Bhaskara Rao U. V. C. E., Electrical Engineering Department, Bangalore, India

Using standard logic elements to determine the derivative of an input signal digitally, this inexpensive circuit can find the acceleration or deceleration of elements in linear and rotating systems, such as those encountered in moving projectile problems or when measuring changes in shaft speed. The magnitude and sign of the derivative is expressed as a 5-bit word at the output, which makes interfacing with a microprocessor or other processing device in a data-acquisition system easy.

The rate of change of an input signal is measured with the circuit shown in the figure. The input signal, f(t), has been derived by a transducer that converts the speed of the shaft, etc. to a corresponding frequency. With the aid of gates $G_1 - G_3$, this signal is gated to an up-down counter. Clock signal x(t), which is low for approximately 100 nanoseconds, can be generated by a 555 timer in the astable mode.

Generally, the negative-going edge of x(t) clocks the flip-flop A₁, which operates in the toggle mode. When its

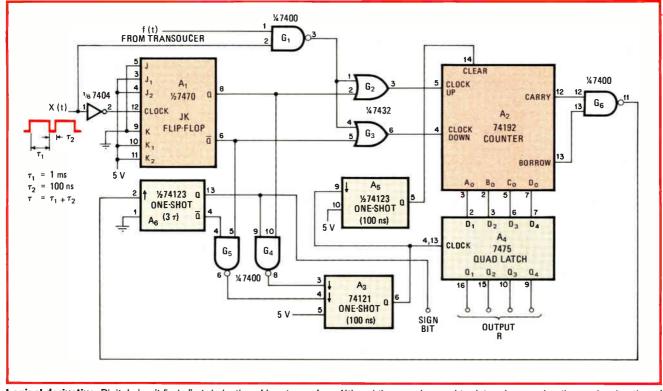
output is high (Q = 1), G₂ is disabled and G₃ is active; hence, the 74192 counter, A₂, counts down. Otherwise, A₂ is in the count-up mode. In either case the 74192 counts during the time T_1 .

Consider circuit operation when the change in f(t) is positive. A narrow positive-going pulse is generated by A_5 each time the Q output of A_1 moves high (at the start of the measuring cycle) and sets the counter to zero. The 74192 first counts down for the period T_1 . The Q output of A_1 then moves low as it is toggled by x(t), and the 74192 counts up during the next T_1 period. The net reading from the counter at this time is thus:

$$|\mathbf{R}| = (\mathbf{f}_{u} - \mathbf{f}_{d})\mathbf{T}_{1} \tag{1}$$

At the end of the counting cycle and at the start of a T_2 period, A_1 triggers A_3 and the one-shot generates a positive-going pulse. This signal clocks latch A_4 , so that the counter's contents appear at the output. The negative-going edge of the latching pulse then triggers A_5 , clearing the counter for the next measuring cycle.

During successive cycles, A_6 is retriggered continuously by the A_2 carry pulse, which is generated during the up-count interval. Continuous retriggering of A_6 ensures that circuit timing is maintained, for A_6 activates G_4 and enables A_3 to fire only at the start of every other T_2 period. Note that a carry pulse will be generated during each timing interval if f(t) is rising (R in Eq. 1 will be positive), because the number of pulses received during



Logical derivative. Digital circuit finds first derivative of input waveform f(t) and thus can be used to determine acceleration or deceleration of elements in linear and rotating systems. Output is expressed as a 5-bit word: 4 bits for magnitude and 1 bit to indicate sign.

the count-up interval must be greater than that encountered during the count-down time.

If the period between A₁'s toggling times, and thus the measuring cycle $t = (T_1 + T_2)$, are small, then the derivative of the input wave, f'(t), may be assumed to be constant over the measuring cycle, and f'(t) = K. Therefore the change in the average frequency with respect to time t is:

$$\frac{f_u - f_d}{t} \rightarrow f'(t) = K$$
(2)

Substituting for $f_u - f_d$ in Eq. 1 yields:

$$\mathbf{R} = \mathbf{K}\mathbf{T}_{1}\mathbf{t} \tag{3}$$

where R now represents acceleration and T_1 and t are known constants.

If the change in f(t) is negative (deceleration), the

Calculator notes

HP-25 finds thyristor's conduction angle, output power

by William D. Kraengel Jr. Valley Stream, N. Y.

Thyristors have enjoyed increased popularity ever since optocoupler and microprocessor drivers have made them convenient to use in such applications as traffic-light controllers and microwave ovens. A thyristor's most important parameter is generally considered to be its conduction angle for a specified power output, and these HP-25 programs aid in the design of power systems using thyristor controllers by finding the set angle required for proper circuit operation, or alternatively, the output power for a specified conduction angle. Either the average or root-mean-square values of current or voltage may be determined directly for thyristors operated in either the half-wave or full-wave modes.

Unfortunately, the conduction angle cannot be uniquely determined, but rather must be found using an iterative approach. The first program can solve two iterative equations that hold true for all thyristors operating in the half-wave case:

or:

$$\Theta_{\rm c} = 360^{\circ} \left(\frac{\sin 2\Theta_{\rm C}}{4\pi} + \frac{\rm P}{\rm P_{\rm L}} \right)$$

 $\Theta_{\rm c} = 360^{\circ} \left[\frac{\sin 2\Theta_{\rm c}}{4\pi} + \left(\frac{X_{\rm rms}}{X_{\rm L}} \right)^2 \right]$

where:

 Θ = the half-cycle conduction angle (that is, the number of electrical degrees during which the thyristor is in conduction for each half cycle of the applied ac input voltage)

 $X_{rms} = load voltage or thyristor current$

 X_L = rms line voltage or current (full conduction)

P = power dissipated by the load

number of pulses received during the first (down) counting interval will be greater than that received during the next (up) counting time. Hence, neither a carry nor a borrow pulse will appear at A_2 , and A_5 is not triggered. Therefore G_4 is disabled, G_5 is enabled, and A_3 is triggered at the end of every other T_1 period.

The end result of this operation is that A_2 first counts up during the initial T_1 period and down for the second T_1 period, at the end of which time the Q output of A_1 moves low and the next measuring cycle starts. Thus the latched output of A_2 is still given by Eq. 3, where K now represents the rate of decrease of f(t). The state of the retriggered A_5 indicates whether f(t) is accelerating or decelerating (Q = 1 or Q = 0, respectively).

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.

 P_L = power dissipated by the load at full conduction. The 360° in both equations becomes 180° for the full-wave case, and 4π becomes 2π .

The second program solves the inverse equations for voltage, current, and power when Θ_c is known:

$$X_{av} = \frac{(1 - \cos \Theta_c) X_L}{\pi 2^{1/2}}$$
$$X_{rms} = \left(\frac{\Theta_c}{180} - \frac{\sin 2\Theta_c}{2\pi}\right)^{1/2} \frac{X_L}{2^{1/2}}$$

where X_{rms} and X_L are as defined previously and X_{av} is the average voltage across a load or the average current through the thyristor when operating in the half-wave mode. These equations are also useful under full-wave conditions, where X_{av} is twice that of the half-wave case, and X_{rms} is $2^{1/2}$ times its former value. For the case where both E_{rms} and I_{rms} are known, the program also solves P = $E_{rms}I_{rms}$, which holds true for both the half- and full-wave conditions.

Because the first program solves for Θ_c using the iterative approach, an initial guess for Θ_c must be stored in one of the available registers. Unless the value can be predicted approximately, 90° is a reasonable choice. A step size for the program iteration must also be specified. Its value should be kept small—say about 10^{-5} —so that the program can converge toward a solution. The final value of Θ_c will be displayed in the same register in which the initial value was stored.

For initial guesses far from the actual value of Θ_c , convergence is slow and the program may take several minutes to run. A good guess will enable the program to converge on Θ_c in 20 to 25 seconds, or less if the initial guess is very good.

The second program displays 1.41 after performing the calculation for the various parameters. This number has no significance, but is rather a byproduct of the program's calculations. Additional register arithmetic is performed in accordance with the program instructions to unite the appropriate factors in order to display the desired parameter. Θ_c , E_L , and I_L are overwritten while the program is run and consequently must be stored again before each new run.

A numerical example illustrates the programming procedure. Two systems, one using a triac controller, the other a silicon controlled rectifier, require 450 watts of energy from a heater circuit that normally draws 10 amperes from a 120-volt line. What must the conduction angles be for the triac operating in a full-wave mode, and for the SCR operating in a half-wave mode? What are E_{rms} across the heater and I_{rms} through the heater for both? What is the average current (needed to determine the power the heat sink for the thyristors must be capable of dissipating)? Using the first program and placing power function 450, 120, 10 in R₀, 90 in R₁, and 10⁻⁵ in R₂ as instructed yields a Θ_c of 113.83° for the sCR and 78.60° for the triac. Note the total conduction angle for the triac is 2(78.60°) = 157.20°. Placing the value of 113.83 into the second program with the line voltage and current previously specified yields V_{rms} = 73.49 across the heater, I_{rms} = 6.12 and I_{av} = 3.16. Recalling the contents of R₄ yields P = 450.02 w. Repeating the process using Θ_c = 78.60° and the instructions peculiar to the triac operating in the full-wave mode yields V_{rms} = 73.48, I_{rms} = 6.12, and P = 449.49 when the contents of R₅ are recalled.

Program 1:		Program		Instructions for program 1				
	θ_{c} for specified		E, I, P, for sp		Key in program and enter RUN r		Imode	
ine	Code	Key	Code	Key	Specify equation's step size (tolerance)			
01	00	0	01	1	(δ) , STO 2			
02	23 07	STO 7	24 05	RCL 5	For half-wave case, store power function or voltage/current functio			r voltage/current function
03	24 01 13 15	RCL 1 GTO 15	14 05 41	f cos		(P), \uparrow , (E _L), \div , (I _L), \div , S	STOOOR	
04	21	x Z y	15 73			$(X_{rms}), \uparrow, (X_L), \div 2 f\sqrt{-1}$	÷g x² 2 X 5	STO 0
06	23 06	STO 6	02	g π 2	• For	full-wave case, store power		-
07	01	1	61	X		$(P), \uparrow, 2 \div (E_L) + (I_L) + $		
08	23 07	STO 7	71	+		$(X_{rms}), \dagger, (X_L), \div 2 f \sqrt{2}$	÷g x² STO	0
09	24 01	RCL 1	23 00	STOO	• Est	imate conduction angle		
10	24 01	RCL 1	02	2		(0 _{ci}), STO 1		
11	24 02	RCL 2	61	X	• Cal	culate half-cycle conduction	n angle	
12	61	x	23 01	STO 1	12-	f PRGM R/S		
13	23 05	STO 5	24 05	RCL 5	1/			
14	51	+	01	1				
15	31	Ť	08	8				
16	31	Ť	00	0		Instructio	ons for prog	iram 2
17	02	2	71	4	10		1	
18	61	×	24 05	RCL 5	• Ke	in program and enter RUN	Imode	
19	14 04	t sin	02	2	• Spe	cify half-cycle conduction a	angle	
20	15 73	gπ	61	Х	Sto	$(\theta_{\rm C})$, STO 5 re line voltage and current		
21	04	4	14 04	fsin	510	(EL), STO 6, (IL), STO 7	,	
22	61	X	15 73	g π	• Init	iate calculation		
23	71	1. 1.	02	2	• •	f PRGM R/S		
24	24 00	RCLO	61	X	1.4	1 is displayed after calculati	on is compl	eted
25	51	+	71	- 1				ated by load under half-wave
26	03	3	41	-		ull-wave conditions, respect		
27	06	6	14 02	f√	• To	display half-wave or full-way	ve value of I	E _{av} or E _{rms} , call out register
28	00	0	02	2		taining that function, multi		
29	61	×	71	+		display half-wave or full-way		av or I _{rms} , call out register
30	41	-	23 02	STO 2		taining that function, multi		
31	15 71	g x=0	02	2				heak) for the given conduction θ_c for 7, respectively, by sin θ_c
32 33	13 49	GTO 49 RCL 7	14 02 61	f√ X	ang	ie may be round by monthpi	ying register	o or 7, respectively, by sin oc
34	15 71	g x=0	23 03	STO 3		Carl Contractor of the second	11-1-1	
34	13 05	GTO 05	15 02	g x ²				
36	21	x ⊉ y	24 06	RCL 6				
37	24 06	RCL 6	61	X	Regis	sters for program 1	-	Registers for program 2
38	71	÷	24 07	RCL 7	Ro	f (P), f (E), and f (I)	8.	f (Eav), f (Iav) half-wave
39	01	1	61	X			Ro	
40	41	-	23 04	STO 4	R ₁	$\theta_{\rm c}$ (init) $\rightarrow \theta_{\rm c}$ (final)	R ₁	f (Eav), f (Iav) = full-wave
41	15 22	g 1/x	02	2	R ₂	δ	R ₂	f (E _{rms}), f (I _{rms}) : half-wave
42	24 05	RCL 5	61	×	$R_5 - R_7$	in use	R ₃	f (Erms), f (Irms) : full-wave
43	61	×	23 05	STO 5	- BARK		R ₄	P : half-wave
44	23 41 01	STO-1	02	2			R ₅	$\theta_{c} \rightarrow P$: full-wave
45	15 03	g ABS	14 02	f√			R ₆	E
46	24 02	RCL 2	23 61 06	STO x 6			R ₇	
47	14 41	f x < y	23 61 07	STOx7			L.,	
48	13 01	GTO 01	13 00	GTO 00				

Engineer's newsletter_

Electron-beam welding cuts connector production costs

Precious metals and base metals with widely different melting points have been hard to weld together in strips long enough for the economical production of connector contacts. But electron-beam welding can join metals that till now could never be welded together except under tightly controlled laboratory conditions.

Technical Materials Inc. of Lincoln, R. I., has developed such a welding process and refers to the product as Dual Metal Strip. Production of connector contacts is already benefiting at such places as Honeywell Inc.'s Micro Switch division in Freeport, Ill., where a change from hand-welded contacts to the electron-beam-welded type has so far saved \$164,000 in production time and material costs. The possible metal combinations are many-copper, nickel alloys, steels, and all precious metals all can be paired. Moreover, the process can join metals of different tempers.

Improving phototransistor pulse response

Murdock Taylor of Exide Power Systems division, ESB Inc., Raleigh, N. C., points out that the pulse response of a phototransistor can be greatly improved with much less circuitry than in Peter Kindlmann's combined transistor array and capacitor arranged in a bootstrap feedback configuration [*Electronics*, Aug. 17, p. 105]. Taylor says that a standard cascode configuration, in which a Litronix IL-CT6 optoisolator is coupled to the emitter of a 2N2222A transistor having a 1-k Ω load resistor, should result in rise and fall times of less than 0.5 μ s. (By itself with a 100- Ω load, the phototransistor of the IL-CT6 has typical rise and fall times of 5.0 and 25 μ s, respectively.) Naturally, rise and fall times of the circuit could be improved beyond 0.5 μ s by decreasing the 1-k Ω load resistor.

Why test at the bare-board level? Is the yield from your functional pc-board tester too low? Then a new Teradyne booklet called some "Hows and Whys of Testing Bare Boards" could cut your functional test time. The publication relates testing to the rest of the manufacturing process, emphasizing the reduced start-up times and rapid rise to high yield possible with automatic bare-board test equipment. Free copies of the booklet are available from the Publications Department, Teradyne Inc., 183 Essex St., Boston, Mass. 02111.

Battery storage continued

Al Schamel, a design engineer at Tektronix, wants to amplify Kenneth Kerwin's item on this page on July 20, "Simple switch saves battery during storage." He notes that although it is true that the battery-level meter in the Tektronix 1107 nickel-cadmium battery supply is connected across the battery output, it is not the only cause of battery discharge. The level of current drawn by the meter circuit from the battery is very low in relation to the ampere-hour rating of the battery, and in fact, even if the meter circuit is disconnected, the self-discharge characteristics of the nickelcadmium cell will discharge the battery.

Schamel points out that the 1106 operator's manual contains information on the battery's maintenance and extended storage, including a method of removing the load from the meter circuit without modifying the instrument. Jerry Lyman

The Birth of a Notion.

Robert H. F. Llovd President CONVER Corporation RCA Solid State Division, '57-60, R&D and Mfg.-Mgmut. IBM,'60-68, Product Development Mgmut. ADVANCED MEMORY SYSTEMS [now INTERSIL]'68-74, Founder and President NATIONAL, SEMI-CONDUCTOR,'75-77 Group Director, MOS/LSI

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Any voice message passing through this formidable process sounds to an eavesdropper like impenetrable static—but, of course, the police, with compatible DVP equipment, can hear each other clearly.

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FROM TUNING IN THE GOOD GUYS.

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We've come a long way from the time when we put radios into cars fifty years ago, and put TV sets into America's living rooms. Now we make hundreds of models of two-way radios, and although we no longer make home TV sets here at all, we do make some of the most advanced and durable TV cameras and monitors for industrial security systems.

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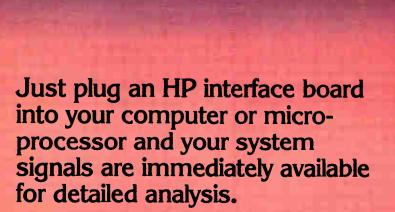


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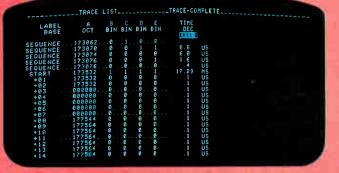
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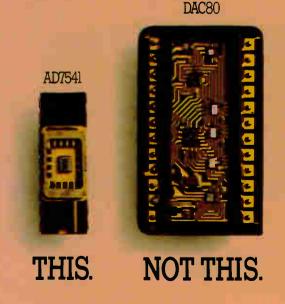
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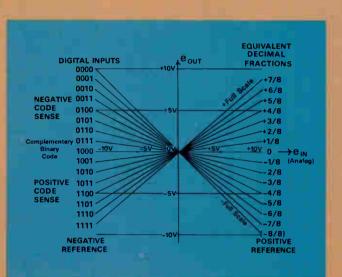
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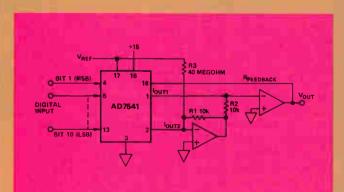
Below: unretouched photo of AD7541 and typical DAC80 with lids removed.





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New products.

Big bubble bows

Quarter-million-bit memory is supported by multichip module, controller board, and development system

by Raymond P. Capece, Solid State Editor

Rockwell International Corp.'s quarter-million-bit bubble memory, its first such commercial device, is making a grand entrance amid a crowd of supporting products, including a multichip module, a controller board, and even a bubblememory development system. And to follow through on its opening act, the company plans a big production number: delivery of small quantities on all items in 90 days.

Clearly, the race is on between Rockwell and Texas Instruments Inc., which announced its upcoming quarter-million-bit bubble memory last month [*Electronics*, Aug. 17, p. 39]. The bubble chips themselves are comparable in performance, similar in structure and appearance, and matched in price—\$500 each in unit quantities.

What, then, is Rockwell's strategy for one-upping the Texans? In the long term, Rockwell is selling reliability—a product that has been proven good enough for data recorders in space. In the short term, the selling point is a systems approach with various support products available now, so that designers can get acquainted with the idiosyncrasies of the device.

"We're giving the designer something he can use right now," explains John Archer, director of bubble memory products in Rockwell's Electronic Devices division in Anaheim, Calif. "The multichip module takes him right to TTL, and the controller board is bus-compatible with our 6500 microprocessors and Motorola's 6800."

The module is a printed-circuit board containing four bubble chips and the necessary linear circuits to reach the voltage swings of transistor-transistor logic. The $9\frac{3}{4}$ -by-6inch board, called the RLM658, thus has a million-bit capacity and is designed for 8-bit-wide operation with a data rate of 100 kilobytes per second. It is priced singly at \$2,500.

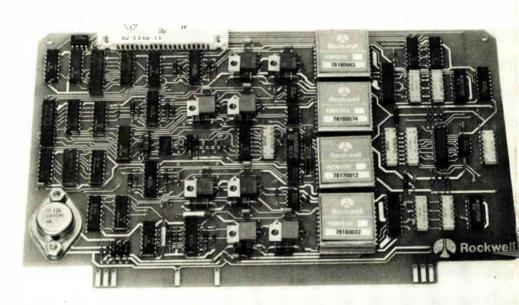
Built on a similar pc board, the RCM650 bubble-memory controller contains all the random logic and discrete components needed to interface the serial bubble operation to a parallel, byte-oriented bus structure. It can handle as many as 64 bubble chips—up to 16 megabits—and has a unit-quantity price of \$1,000.

Probably the most significant sup-

port product is Rockwell's development system. The \$11,400 system has essentially the same hardware as the System/65 that Rockwell offers for its 6500 microprocessor family, with the addition of a pair of million-bit bubble boards and a controller board. In fact, \$6,000 for the three boards is all those who already possess a System/65 need to get into bubbles.

"We've designed our bubble and control modules to plug right into the System/65," explains Archer. "They can even plug into Motorola's Exorciser development system."

The RBM256 bubble-memory



New products

chip itself has few distinct differences from Ti's part. The architecture of the two is the same—both use a dual-port block-replicate structure, and both divide the loops into even- and odd-bit halves. Whereas the 18-pin Rockwell device is organized into 1,025-bit loops, TI's loops contain 1,137 bits, or bubble positions. "We wanted to keep it as close as possible to a binary part, which TI's is not," says Archer. The data access in the Rockwell part, he explains, is by 1,024 blocks of 256 bits per block. "We felt that was extremely important in applications such as fixed-head-disk replacement," he maintains. TI says, however, that new markets, rather than replacement sales, are its chief targets.

Rockwell's chip has 282 loops in all, 260 of which are guaranteed fully functional. Redundancy has been the trend in bubble-memories, and some failed loops are permitted; they are simply masked out and not used, somewhat as bad tracks on a disk memory are avoided.

One striking difference between



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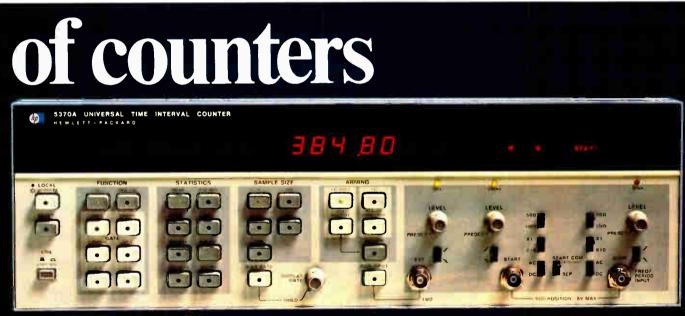


the two bubble chips, however, is that TI has chosen to provide a special loop that is dedicated to the masking out of bad loops, while Rockwell provides no such on-chip masking. It decided instead that mask data should not reside within the device. "For one, because of the circuits required, it's more costeffective to put the masking data in programmable read-only memory and since we will supply the PROM, the redundancy is transparent to the user," explains Archer. "More important, we expect that many users will be pushing the bubble devices to the operating limits, and masking data shouldn't be subject to the same error possibilities as the rest of the chip."

Rockwell is certain that reliability will become a major issue in bubble-memory devices, especially as temperature-range limits are pressed. It is specifying an operating-temperature range of -10° to 70° C for the RBM256 package and guaranteeing full data retention over a range of -50° C to 100° C. According to Archer, Rockwell is working on extending the operating specification to cover the temperature range from -25° C to 100° C.

The actual die size of the bubble chip is one square centimeter, and the structure is based on a 14-micrometer period with $3-\mu m$ bubbles. Archer says that in 1979, Rockwell will introduce a million-bit chip that can be used in parallel with and will be packaged identically to the quarter-million-bit device.

Rockwell International Corp., Electronic Devices Division, P. O. Box 3669, Anaheim, Calif. 92803. Phone (714) 632-3729 [338]



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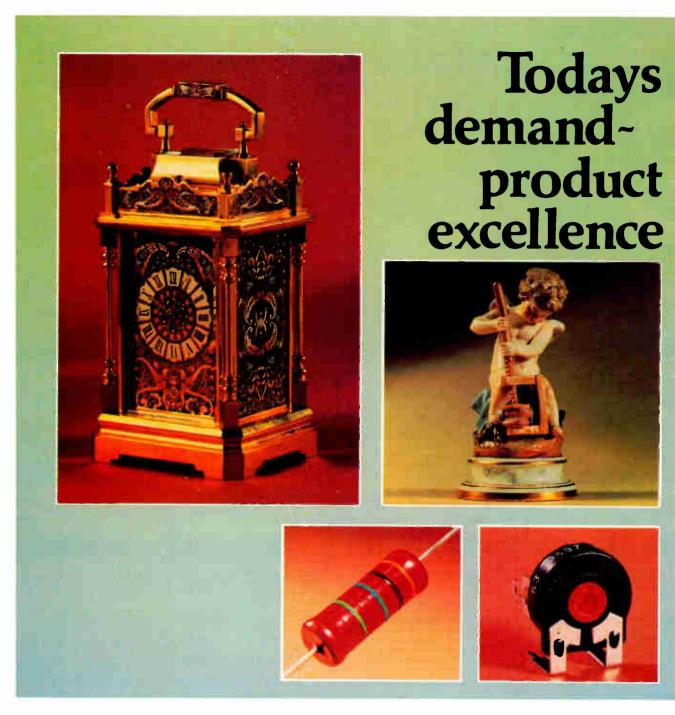
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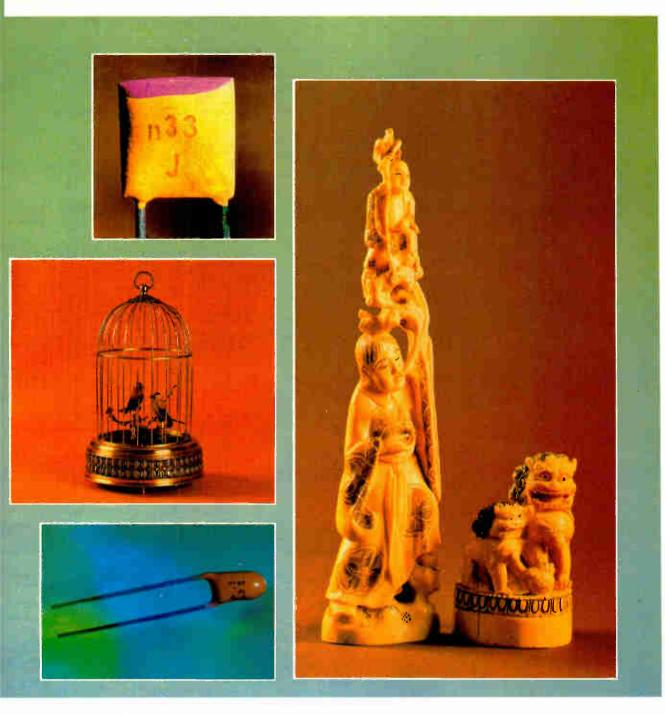
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Chip pair eases dynamic RAM refresh

Memory controller and memory-address multiplexer can be used with present 4-K and 16-K dynamic RAMs as well as future 64-K devices

System engineers eager to design with dynamic random-access memories soon find their eagerness dulled by the dozen or so medium-scale integrated circuits needed for all the RAMS' complex timing requirements. With Motorola's MC 3480 dynamicmemory controller chip, all the rowand column-address timing signals, as well as refresh controls, are generated on command from a compatible microprocessor, such as the company's own M6800.

"By combining the memory controller with our memory-address multiplexer and refresh address counter, the MC 3242A, we are able to save the design engineer 60% in printed-circuit board area," says Bill Carns, linear interface planner. "The

by Nicolas Mokhoff, Components Editor

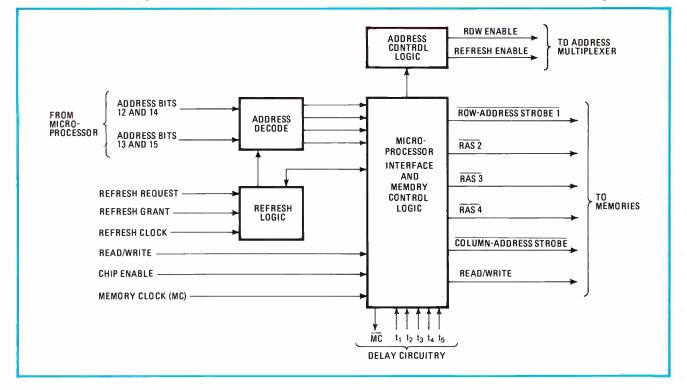
two-chip set can be used with presently available 4- κ and 16- κ dynamic RAMs that are housed in a standard 16-pin package. Consequently, future expansion into a 64- κ 16-pin configuration will be a simple matter, since the timing characteristics are identical."

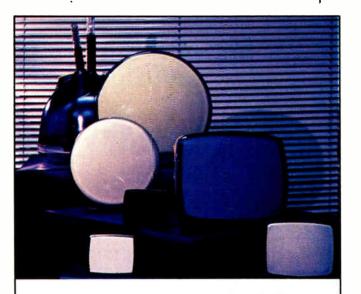
Instead of an on-board master clock, the controller operates off five general timing inputs that, upon command from the microprocessor, help generate all the required row and column address signals, as well as the read and write commands. The five timing inputs use external timing delays to sequentially select the proper output signals to be enabled. They generate up to four row-address control strobe signals for addressing a memory bank of up to $4-\kappa$ - or $8-\kappa$ -by-8 data blocks.

The RAS commands are encoded from two address lines $(A_{12} \text{ and } A_{13})$ from the microprocessor. A columnaddress strobe signal is also generated for all the data blocks, as is the read/write signal to the RAMs specifying whether data is being read out or written into the memories.

The timing signals may be generated from a number of sources: oneshots, high-frequency counters or shift registers, delay lines, or the basic microprocessor clock through the MC (memory clock) pin on the controller chip.

The controller, in conjunction with a separate oscillator, also generates all the refresh timing, needed to





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insure the retention of data in dynamic RAMS. The refresh cycle is initiated through the refresh grant line from the microprocessor system clock at the rate of the refresh clock from the outside oscillator. It is triggered by a refresh request from the controller to the processor. This, in turn, produces the enable signals for the address multiplex and refresh counter, signaling to this circuit that a refresh cycle is about to start and specifying which half of the multiplexed address is to be written into the memories.

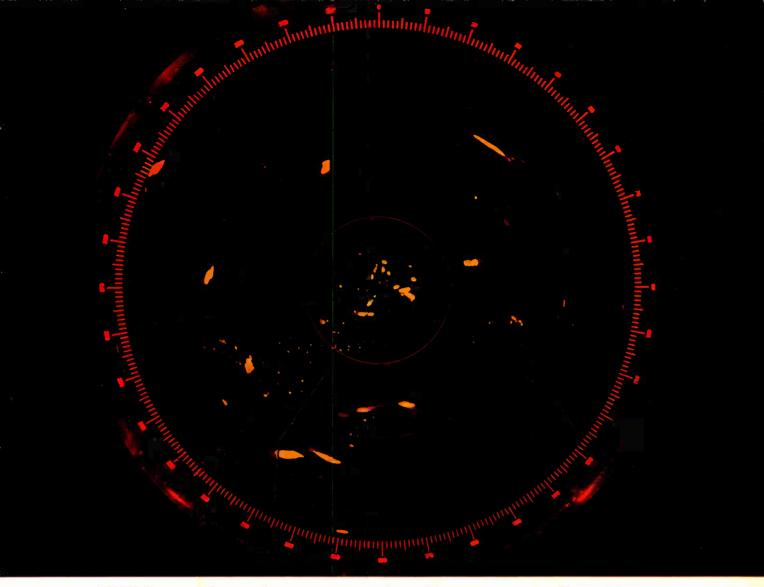
Also, the refresh-grant input signal from the system clock can be used to distinguish between a refresh command and a direct-memoryaccess command. This prevents a DMA from occurring during a refresh cycle thus ensuring that data is not lost.

The other half of this chip pair multiplexes 14 address bits from the microprocessor into the seven address inputs to the memory device. In addition, the MC 3242A has a 7-bit counter that generates the 128 sequential addresses required for the refresh cycle. "A unique feature of our memory-address multiplexer is the chip-enable control pin," says Carns. "If left disconnected, the chip can be used as a functional replacement for the Intel 3242, only without its detect-zero function. When the pin is grounded, the chip's outputs end up in a three-state condition. This feature adds flexibility for such conditions as the removal of power. The outputs at that time go to a three-state condition and subsequently, when power is returned, return to a known address." The address is all 1s; the outputs go there when the CE pin goes high.

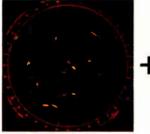
Both the 24-pin controller and 28pin address multiplexer are Schottky-transistor-transistor-logic parts and operate from a 5-v supply. Motorola is supplying samples of the 3480 this month and has parts available off the shelf at prices ranging from \$4.70 to \$6.85 in quantities of 100 for both chips, depending on the package desired by the user.

Motorola Semiconductor Products Inc., Box 20912, Phoenix, Ariz. 85036 [339]

5



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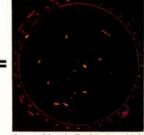


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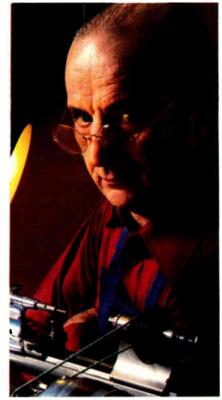
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FOTOCERAM. What the Swiss are seeing red about.

FOTOCERAM materials are replacing ruby wire-guides in high-speed, computer-controlled impact matrix printers. The printers operate by moving a single, vertical column of print wires across a horizontal line. Individual wires are activated in sequence to impact an inked ribbon against the paper, forming characters from patterns of dots. Those characters are generated at speeds up to 300 per second.

Precise vertical alignment of the print wires is extremely important. Up to now, many print-head manufacturers have used synthetic ruby wire guides because of their durability. Holes in the guide must be laboriously machined to less than 0.015 inch diameters, with a total tolerance within 0.001 inch. And the finished ruby guide must go through a polishing and assembly operation. It's an expensive

proposition!



FOTOCERAM materials by Corning compete on price and durability. Using a FOTO-CERAM brand glass-ceramic,

derived from Corning's unique photosensitive glass, extremely small holes can be chemically machined with precision. Manufacturers' tests show that FOTO-CERAM wire guides exhibit excellent

wear characteristics equal to ruby. They can withstand the constant motion of the wires through the guide holes. And they can be mass produced at significantly lower cost than ruby. The FOTOCERAM material is only one of a family of unique FOTOFORM materials that can be precision etched with holes of almost any shape and size. In excess of 50,000 holes per square inch, in pieces as thin as 0.010 inch. Holes, slots and channels, as small as 0.002 inch. And with tolerances within 0.001 inch. These photosensitive materials can be precision-etched, machined, cut, milled, chamfered, ground,

lapped, polished, sealed to glasses or ferrites, and even metalized. FOTOFORM materials offer you engineering flexibility –



the flexibility to do it your way. . We've given the Swiss

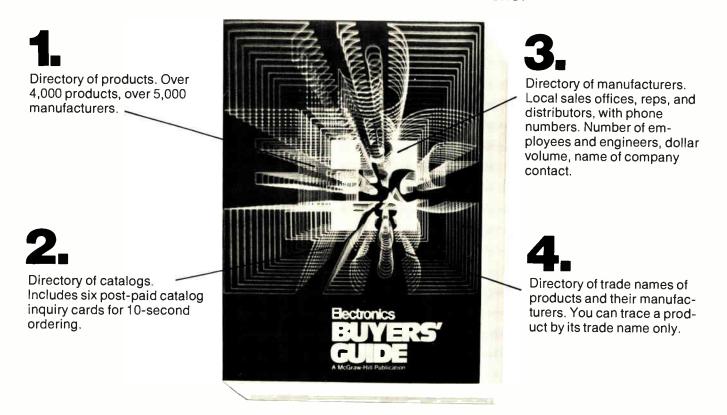
something to think about. Maybe we've given you an idea. FOTOFORM and FOTO-CERAM materials are being used to solve design problems for a wide variety of applications. Chances are they can solve a problem for you.

FOTOFORM and FOTO-CERAM materials by Fotoform Products Group, Corning Glass Works, Corning, New York 14830, (607) 974-4304.

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LCD driver saves space and money

C-MOS chip includes 32 latches to relieve microprocessors of display refresh chore, has on-board oscillator

by Larry Waller, Los Angeles bureau manager

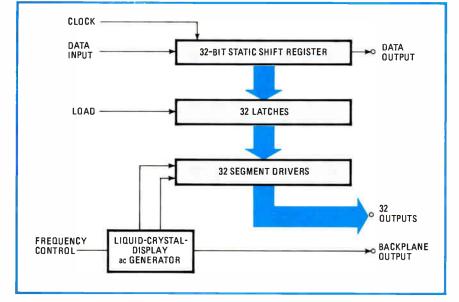
Large liquid-crystal displays, teamed with microprocessor control, are getting ready to move into such new areas as point-of-sale signs for retailing. They have been delayed until now by the cost of their drive circuits, mostly of the standard 4000 series, which are typically put together in expensive multichip configurations to accommodate the special symbols and nomenclature needed by different users.

To provide a single drive chip that can serve all LCDs, Hughes Aircraft Co.'s Microelectric Products Division has developed a complementary-metal-oxide-semiconductor circuit that handles any standard or custom display with up to 32 segments. Called the HLCD 0438, the part even works as a smart peripheral, relieving the microprocessor of the task of refreshing the display, according to Norman Moyer, manager of MOS design at the Newport, Calif., division.

"Our objective was a standard part for custom displays as simply the best way to interface with LCDs," he explains. The Hughes division has built up extensive capabilities in both LCD and C-MOS technologies from its participation in the digital watch business, and its experience is reflected in the new driver.

The HLCD 0438 handles both field-effect and dynamic-scattering displays. Because of its serial-input configuration, the driver needs only three input lines: one for the clock, one for the data, and one for the load command. Besides C-MOS, the inputs are compatible with n-MOS and transistor-transistor logic.

As a smart peripheral, the driver relieves the microprocessor of the task of generating the waveforms required to drive the display by latching the data to be displayed, Moyer says. The frequency of the ac



drive for the display can be set by a user-provided clock, or it may be generated internally by the driver. In the latter case, a frequency-determining capacitor must be connected to the frequency-control input of the circuit.

Another important feature of the 0438 is that several of the drivers may be cascaded by connecting the backplane output of one chip to the frequency-control input of the next, thus allowing one capacitor to provide frequency control for all. Alternatively, the frequency-control inputs may all be connected to a common driving signal. As far as load capacity is concerned, Moyer says that up to 100 displays can be driven at 10 kHz. "You will run out of money for displays before you run out of load capacity," he says.

The chip will run off supply voltages from 3 to 15 v dc. If the on-chip oscillator is used at a frequency of 15 kHz, the current requirement is 20 μ A. If the oscillator is not used, this drops to 5 μ A. Data setup time is 200 ns, data hold time is 100 ns, the load pulse width is 200 ns, and the dataoutput propagation delay is 300 ns. The operating temperature range is -40° to $+70^{\circ}$ C.

The unit, which sells for \$4.45 each in lots of 1,000 or more pieces, has a delivery time of 30 days. Since it replaces a number of 4000 series discrete devices (shift registers, gates, data latches, and oscillators), it will offer both lower cost and higher reliability, in addition to smaller size.

Microelectronic Products Division, Hughes Aircraft Co., 500 Superior Ave., Newport Beach, Calif. 92663. Phone (714) 759-2411 [340]



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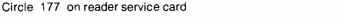
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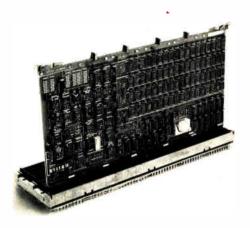
Contact GTE Sylvania, Connector Products Operation, Box 29, Titusville, PA 16354. Phone: 814-589-7071.

Remember, good connections run in our family.





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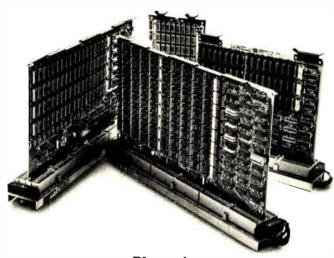


DEC's semiconductor memories:

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New products

Components

Floodgates open for large LCDs

0.5-in., 4-digit displays for clocks, instruments, available in big production quantities

For liquid-crystal displays to move as definitively into larger consumer products and instruments as they did into digital watches, what is needed is a marketing, rather than a technological, advance. The required next step, according to industry sources, is for a big, independent LCD producer to come out with a standard largedigit line, assuring customers of a stable supply. Accordingly, Beckman Instruments Inc., acknowledged kingpin of the noncaptive LCD makers, is introducing 0.5-inch, fourdigit, seven-segment displays, initially for use in portable clocks and instruments.

Beckman's strategy strongly confirms the market view just described, according to Rey Harju, marketing manager for LCDs at the company's Advanced Electro-Products division. "Major manufacturers need major suppliers," he states, adding that the Fullerton, Calif., division already has good-sized production orders in the bag. Earlier this year [Electronics, Feb. 3, p. 33], it discussed LCD plans, but awaited building up production capability sufficient to allow off-the-shelf delivery before announcing details at Wescon on Sept. 13.

Beckman is offering three types of displays in two packages, explains Harju. All of them have similar electrical specifications. The model 737-01 is intended for clocks; the 739-03, a $3\frac{1}{2}$ -digit unit with special symbols, is aimed at instruments; and the 739-04 is suitable for both applications. The 737-01 connects only on one side, while the others have connections on both sides for more flexibility.

The new displays typically draw

4.4 μ A from a supply voltage of 4.5 v rms. However, they may be operated at any voltage from 3 to 20 v and will draw less than 8 μ A. Both packages are offered in versions that allow operation in transmissive, reflective, and transflective modes, and have a polymer seal for humidity resistance.

The model 739-04 has three decimal points between digits and a colon in the center of the display. For clocks, the 737-01 adds a bell symbol, to show when the alarm is set, and a flag to indicate the passing seconds. All of the displays operate from -10° to $+55^{\circ}$ C ($+14^{\circ}$ to $+131^{\circ}$ F). At 25°C (77° F), segments typically turn on and off within 100 μ s. At 0°C, the turn-on time is typically 120 μ s and the turn-off time 180 μ s. The displays may be stored from -30° to $+70^{\circ}$ C.

In setting up a dedicated production line for the 0.5-in. displays, Beckman is making what it terms a significant investment in an important extended area of the LCD market. Building the new displays uses "the same expertise, but slightly different technology, as our watch LCD line," says Harju. The major difference is going to polymer sealing from the glass-frit sealing used in the watch units. This not only does away with the high temperatures needed to seal glass, but is easier to work with in the most critical process-alignment of segments.

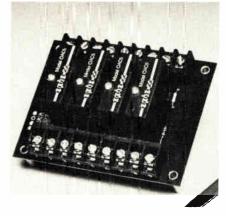
Prices of the three displays are similar. In quantities of 500 pieces or more, polarized units are \$7 each and nonpolarized displays go for \$5.45. When the quantities rise to 10,000, the prices drop to \$4.45 and \$3.50, respectively. All are available from stock.

Advanced Electro-Products Division, Beckman Instruments Inc., 2500 Harbor Blvd., Fullerton, Calif. 92634 [341]

Four-pole relays handle

ac and dc, isolate to 2,500 V

Composed of four individual input/output modules, Opto 22's fourpole solid-state relay can handle ac



loads of 120 or 240 v, dc loads of 60 or 200 v, or user-specified combinations of these voltages. The relays provide 2,500-v peak optical isolation, and each module is protected by its own plug-in fuse.

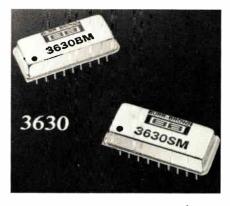
Control voltage for the relays can be 5, 15, or 24 v, and power terminations are made on a barrier strip at such distances as not to affect logiclevel terminals. Units are available from stock.

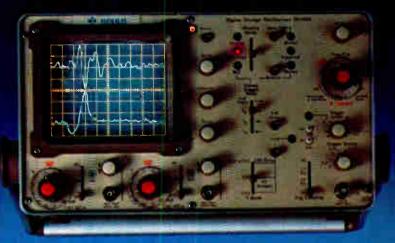
Opto 22, 5842 Research Dr., Huntington Beach, Calif. 92649. Phone (714) 892-3313 [344]

Instrumentation amplifier

has low voltage drift

Because of the sizable temperature variations commonly found in industrial environments, instrumentation amplifiers designed to work with such process-measuring devices as strain gauges, thermocouples, resistance-temperature detectors, and other remote sensors and transducers have to be insensitive to tempera-





Extend your storage

capabilities beyond the

conventio

Now Gould offers a range of digital storage oscilloscopes that offer a world of advantages over conventional tube storage technology, beginning with being able to capture transient or "one-time" events and

store them indefinitely for display or hardcopy printout. This makes them ideal for electronic, electromechanical, educational, and biophysical applications.

Both the OS4000 and the new OS4100 combine the capabilities of semi-conductor memory with a bright, stable,

flicker-free display. This technique allows analysis of signal build-up and decay characteristics through pre- and post-trigger viewing. Expansion of the display after storage permits detailed study of specific areas of the trace.

The new model-OS4100-also offers you stored X-Y displays, channel sum or difference and a maximum of 100 V per cm sensitivity with noise suppression. A unique trigger window circuit assures capture of transients of unknown polarity.

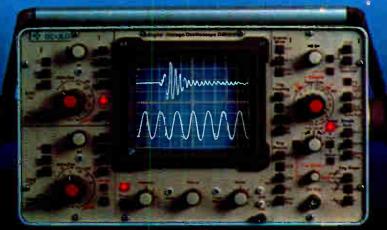
Other outstanding features include

automatic operation, display of stored and real time traces simultaously and hard copy memory output in digital or analog form. And IEEE488 is available for compatible interfacing.

If features like these aren't enough to lure you away from less sophisti-

cated instruments, remember that Gould scopes are backed by a two-year warranty of parts and labor, exclusive of fuses, minor maintenance and calibration. And application assistance, customer training and worldwide service centers are part of -> GOULD

Gould's customer support program.





Rugged environment? Routine trips through torture test prove out the reliability of typical inductive components selected at random from production runs. This sample is subjected to a series of high and low temperature extremes with performance characteristics verified for conformance to Military Specification MIL-C-15305. In addition, periodic samples are subjected to other torture tests:

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Cyclic
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New products

ture. That is why designers at Burr-Brown Research have developed a hybrid instrumentation amplifier, the model 3630, that has voltage drift of only $\pm 0.25 \ \mu v/^{\circ}C$ at a gain of 1,000.

The unit also features a nonlinearity within 0.01% maximum at that gain. At a lower gain of 100, voltage drift increases only slightly, while nonlinearity decreases to within a maximum of 0.003%. Initial offset voltage is a very low 25 μ v, which can be zeroed as required.

The 3630's 10^{10} - Ω input impedance preserves the unit's accuracy when amplifying low-level signals by minimizing the effects of source loading. Even in the presence of a source impedance imbalance of 1 k Ω , the common-mode rejection is a minimum of 106 dB with a gain of 100. The unit's noise level is 1.2 v, peak to peak, and bias current is a maximum of 20 nA.

To provide high initial accuracy, low temperature coefficient of resistance, and TCR matching, the resistor network is fabricated of Nichrome deposited on silicon. By laser-trimming the network, offset voltage is reduced, and the common-mode rejection and offset-voltage drift are optimized.

Packaged in an hermetically sealed 18-pin dual in-line package, the unit will operate from -25° to 85° C. In quantities of 100 and up, the 3630 is priced at \$25 each. Delivery is from stock to four weeks. Burr-Brown Research Corp., P. O. Box 11400, International Airport Industrial Park, Tucson, Ariz. 85734. Phone Dennis Haynes at (602) 746-1111 [343]

Power resistors slash

inductance with new twist

The models MS 260N, 310N, and 313N axial-lead power resistors are film resistors that have better performance characteristics than most wound-wire types. They employ patented resistance films fired onto a solid ceramic core in special serpentine patterns that reduce inductance, so that their inductance is about

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Like its proven and successful predecessor, the SS3 keyswitch is mechanically simple and contact-

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equal to that of a straight piece of wire as long as the actual resistor.

Resistors with power ratings to 12.5 w, resistance values to 30 M Ω and tolerances to 0.1% are available. They exhibit temperature coefficients of 50 ppm/°C or less in the temperature range from -15° to 105°C and can function at temperatures up to 275°C. Maximum operating voltages as high as 6,000 v are attainable.

For values up to $5M\Omega$ in quantities of 100 and up, unit prices are approximately \$2. Initial quantities of most resistors can be delivered from company stock, while production quantities require a delivery time of four to six weeks.

Caddock Electronics Inc., 3127 Chicago Ave., Riverside, Calif. 92507. Phone (714) 683-5361 [345]

Small push-button switch

responds to delicate touch

The J-B-T switch is a subminiature single-pole, double-throw push-button switch that responds to a touch lighter than that needed by any other push-button switch at present on the market, according to its manufacturer.

Rated for 0.4 vA at 20 v, ac or dc,



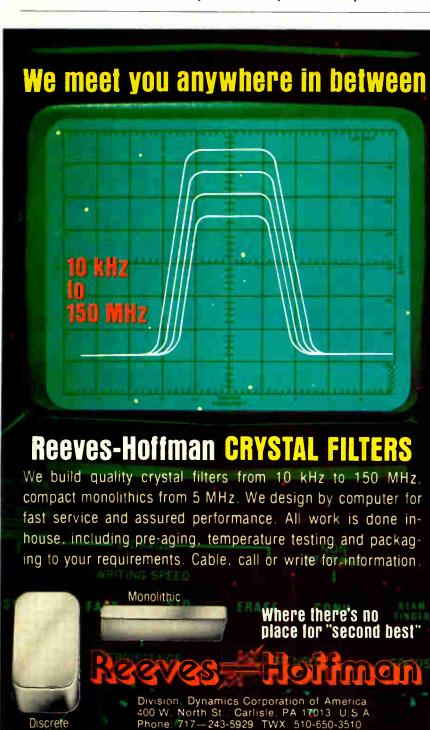
and for 1 A at 125 v ac, the switch has a life-under-load of 60,000 make-or-break cycles. Cutler-Hammer, 424 Chapel St., New Haven, Conn. 06509. Phone (203) 772-2220 [346]

Some potentiometers adjust

to user's preference . . .

Offered in the standard resistance range from 200 Ω to 500 M Ω with a power rating of 0.2w, the RVA-0911-313 line of subminiature trimming potentiometers can be adjusted from the front or through a funnel in the back with a standard screwdriver. Alternatively, they may be manually adjusted with a knurled knob.

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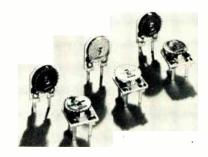
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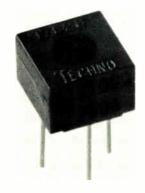
ment units are available with tolerances of either $\pm 30\%$ or $\pm 20\%$, a maximum working voltage of 250 v dc, linear taper, and a typical mechanical rotation of 260°. Murata Corp. of America, 1148 Franklin Rd., S. E., Marietta, Ga. 30067. Phone (404) 952-9777 [347]

. . . while others opt for

the rigors of military life

The model 714 nonwirewound trimming potentiometer is designed for military-grade applications where minimizing space is a key design criterion. A MIL-R-39035-qualified part, the 714 is housed in a ¹/₄-in.high, humidity-proof package of heat-resistant plastic. Potentiometers are available in the range from 10Ω to $1 M\Omega$, are rated for 0.25 w at operating temperatures of 85°C, and offer a maximum temperature coefficient of 100 ppm/°C. The units feature extremely high resolution and exhibit excellent characteristics in high-frequency circuits.

In quantities of 100 and up, each model 714 is priced at approximately \$6. They are available from stock. Techno Components Corp., 7803 Lemona Ave., Van Nuys, Calif. 91405. [348]



system for only \$2900*complete.

Standard Features:

- Dual 8" floppys store 500,000 characters on line
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The C3-OEM is an ultra-high performance microcomputer system. Its powerful 6502A microprocessor (now triple sourced) outbenchmarks all 6800- and 8080-based computers in BASIC and machine code using the BASIC and assembler provided standard with this system.

In fact, the C3-OEM executes standard BASIC language programs at speed comparable to small 16 bit minicomputers.

Ohio Scientific has a vast library of low cost software for the high performance 6502A including an on-line debugger, a disassembler, several specialized disk operating systems and applications programs such as our word processor package and a data base management system. However, the C3-OEM is not just limited to 6502 based software. This remarkable machine also has a 6800 and a Z-80 microprocessor.

The system includes a software switch so that machine operation can be switched from one processor to another under software control!

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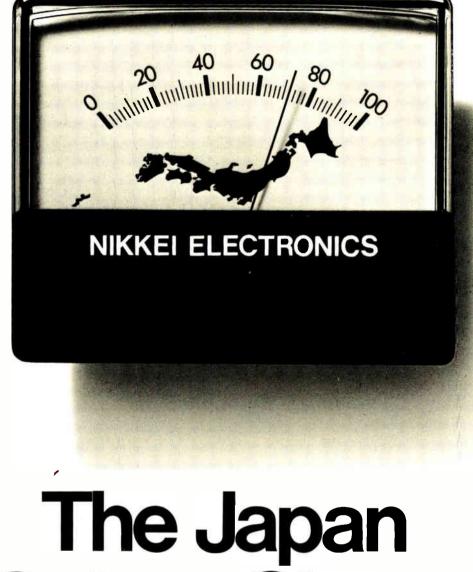
A full spectrum of add-ons are now available including more memory, up to 16 serial ports, 96 parallel I/O lines, a video display, a parallel line printer interface and a 74 million byte Winchester disk drive.

> * 25-49 unit price 1-4 \$3590. 5-9 \$3300. 10-24 \$3100.

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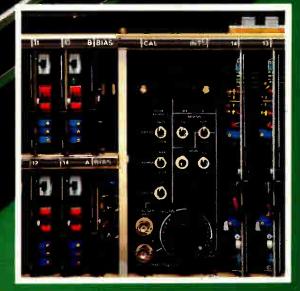
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Instruments

Network analyzer is sensitive

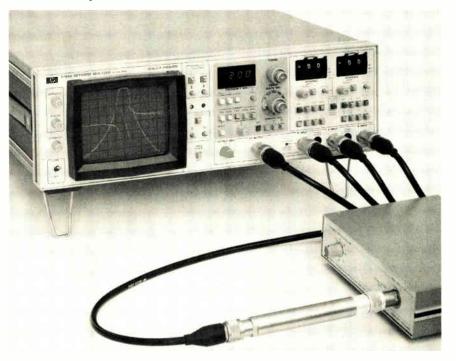
Costing only \$11,500, 4-to-1,300-MHz unit picks up - 80-dBm signals

To calculate the impedance and the transmission and reflection coefficients of radio-frequency transistors, filters, and amplifiers, the magnitude and phase of both incident and reflected signals must usually be measured. Until now, engineers had a choice of two approaches to the task: hook up a vector voltmeter and measure amplitude and phase at various frequencies, or use a \$25,000 automatic analyzer system. Lowcost systems built around diode detectors generally bottom out around -50 to -60 dBm and are therefore not of much use in measuring the values of small-signal transistors and amplifers.

Hewlett-Packard has changed this picture with its model 8754A rf network analyzer, an instrument

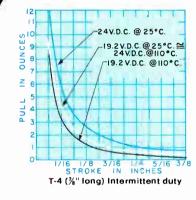
whose \$11,500 price is almost 3.4 dB below the \$25,000 level. With its 4-to-1,300-мнz swept-signal source and cathode-ray-tube display, the 8754A measures and displays the magnitude, phase, absolute power, and polar reflection coefficients of incident and reflected signals. Moreover, it is sensitive enough to detect signal levels down to -80 dBm, according to Larry C. Stratford, product manager for network analyzers. And its narrowband intermediate-frequency amplifier (20-kHz bandwidth centered at 1 MHz) is sharp enough to reduce spurious responses significantly. "For example," Stratford explains, "if you used а 100-мнz signal on a filter whose center frequency was 200 MHz, a diode-detector instrument would register a response to the signal generator's second harmonic. But the 8754A's tuned input would reject that harmonic."

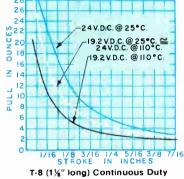
Clever design of the signal source and receiver front end is the key to the 8754A's low price/performance ratio. Instead of using precision phase-locked-loop oscillators, as is done in the company's higher-priced 8505A, the designers of the new analyzer employ a pair of open-loop, varactor-tuned oscillators. This de-



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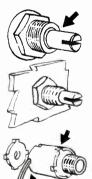
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New products

sign produces its swept output by beating the oscillator frequencies against each other as one oscillator slews from 3.6 to 3.0 GHz and the other goes from 3.6 to 4.3 GHz. The resulting difference frequency is kept at a constant 10-dBm level.

Another way in which HP keeps costs down is to use thin-film components for the receiver's three input mixers. In addition to saving space and money, these sampling mixers provide excellent broadband matching. "The return loss at the inputs is greater than 20 dB," says Doug Rytting, lab section manager for network analyzers. "This shows there is very little reflection due to mismatch."

The inputs to which Rytting refers receive signals from the outputs of the 11850A three-way power splitter, the 8502A transmission and reflection test set, the 8748A S-parameter test set, or a pair of high-impedance probes or other incircuit measuring accessories. Basically, the test sets inject the 8754A swept source's signal into a two-port device and then detect and deliver a reflected and transmitted version of that stimulus to the analyzer's A and B inputs. The receiver compares these two signals with a reference signal to develop the inputs for a display processor.

The user can switch between polar and rectangular displays at the touch of a button. Resolutions for the two are 2.5° or 0.25 dB per major division. When the polar mode is used, a slide-in Smith chart allows direct reading of impedances.

The 8754A is available eight weeks after receipt of order and can be configured to interface with the IEEE-488 general-purpose bus. Hewlett-Packard Co., 1507 Page Mill Rd.,

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New products



occasions does an engineer measure the actual operating temperature of individual circuit components. The reason for this is simple—until now, there has not been a quick, easy way to make exact measurements. So designers have had to be content with techniques like measuring the temperature of ambient or exhaust air.

The model 392 Heat-Prober changes that situation. The pocketsized, 6-by-3-by-1-in. temperature meter weighs a mere $10\frac{1}{2}$ oz and has a $4\frac{1}{2}$ -digit light-emitting-diode display that reads from -50° to 140° C with a resolution of 0.1 °C. From 140° to 500° C, it has a resolution of 1° C. When used with any one of a number of optional, applicationtailored, platinum resistance-temperature-detector probes, the unit takes readings that are accurate to within $\pm 0.5\%$ of full scale, ± 1 digit. Measurement repeatability is within $\pm 0.2\%$ of full scale.

Among the optional probes offered is the model 145, shown in the accompanying photograph. The spring-loaded sensing element provides positive-pressure feedback to the operator to ensure that good surface contact is maintained throughout the reading. Readings are updated three times a second, and the unit's response time is about a second or more depending on the temperature being measured. Another of the probes available is the model 123, which is intended for measuring the surface temperatures of dice and molds.

The Heat-Prober is available from stock and is priced at \$395 in single

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New products

quantities. Probe prices range from \$70 for a simple stick-on probe to \$225 for the model 145; the model 123 is priced at \$195. Also available is a \$75 calibrator, model 10382. which can check the meter's accuracy to within ± 0.1 °C at four points: 0°, 100°, 140°, and 400°C. Heat-Prober Division, William Wahl Corp., 12908 Panama St., Los Angeles, Calif. 90066. Phone (213) 822-6144 [353]

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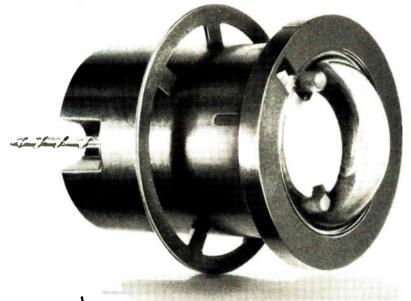
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measurements when it is necessary to insure that the probe is carefully placed. A switch on the probe lets the user initiate this mode of opera-

tion, make the measurement while watching the probe, and turn to the meter within about 3 minutes to take the reading.

The 9301A can be programmed using a parallel binary-coded-decimal word that is compatible with transistor-transistor-logic. Complete with probe, the millivoltmeter sells for a price of \$1,295 and is available from stock.

Racal-Dana Instruments Inc., 18912 Von Karmen Ave., Irvine, Calif. 92715. Phone (714) 833-1234 [354]

Generator modulates at preset

user-defined frequencies

When ordering the model 3003 signal generator, the user can specify any two modulation frequencies between 100 Hz and 10 kHz to which he or she has frequent recourse. The unit is then delivered with these internally generated, switch-selectable frequencies, in addition to the standard modulation frequencies of 400 Hz and 1 kHz.

Operating in the 1-to-520-MHz range, the 3003 also features an external modulation capability that, together with its internal capabilities, allows the operator to create a-m-a-m, fm-fm, and a-m-fm signals. Output levels may be varied continuously between 0.1 v and 1 v. Output level, as well as fm deviation and percent a-m modulation, can be displayed on the instrument's analog meter.

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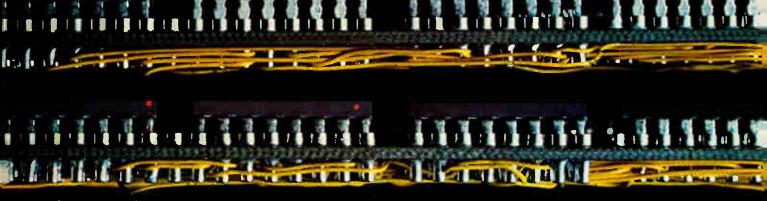
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Augat's stitchwire system works like this. After components are mounted on Planar boards, a stitchwire machine welds insulated wire to stainless steel pads.

Wiring instructions can be furnished using punched tape programs or wire lists. You can also do special wiring configurations including twisted pairs or wiring on the component side. Changes can also be made simply, either by stitch-wire machines or by

hand soldering. Adopting stitch-wire is easy, because Augat stocks the wiring machines and a wide range of general purpose Planar boards. Including boards compatible with most mini and microcomputers. These boards feature large etched power and ground planes.

The combination of large planes and low profile wiring makes them ideal for high speed logic. What's more, we can design and produce stitchwire boards to your specifications. Or we can provide the boards and equipment you need to do the job.

Augat stitch-wire offers density and flexibility advantages you can't get anywhere else. To find out how you can get started with stitch-wire, write Augat Planar Systems, Inc., 14751 Califa Street, Van Nuys, California 91411. Tel. (213) 786-3974.

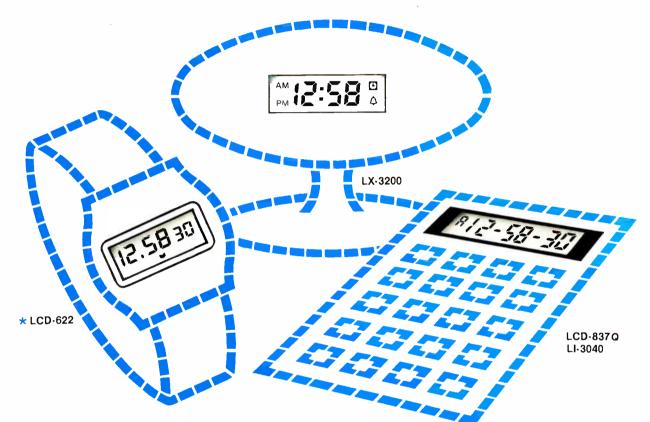
Augat stitch-wire machine



Augat interconnection products, Isotronics microcircuit packaging, and Alco subminiature switches.

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LCD Watch Displays

LCD-622

5-1/2 digits for numbers, symbols for colon (o) and ∑ (day display), and with Kit Supply available (LSI: LR-5105). Also displays with 24hour mode but without Kit Supply (LCD-609, LCD-611).

LCD Clock Modules

LX-3200/LX-3501G

Various sizes from slim type (0.2") with optional color and back light (LX-3200) to 0.5" number height with 24-hour mode on 3V operation (LX-3501G). Also models <u>LX-3403</u> (time correction, wake, sleep timer, audio timer, snooze), <u>LX-3405G</u> (slim type with 0.4" number height and PCW for both sidee) and

sides), and LX-3406H:

SHARP LCD DISPLAYS

See SHARP LCD displays at the: JAPAN ELECTRONICS SHOW '78 Tokyo Oct. 6-11 SHARP CORPORATION INTERNATIONAL DIVISION ELECTRONIC COMPONENTS DEPT. 22-22, Nagaike-cho, Abeno-ku, Osaka, Japan Tel: (06)621-1221 Telex: 5267286 (SHAPEC J)



* We regret to report the photo of Sharp's LCD-622 model on page 52 of the July 20th, 1978 issue appeared reversed due to a printing error

Clock-Calculator Kit

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For hour, minute, second/month.

date, day and 12/24 hour mode

and alarm for clock, or 8 digits

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(Low priced!)

calculator.

Rubber Connector



New products

Semiconductors

Chip controls floppy disks

MOS device can handle double-density, double-sided units, has three scan modes

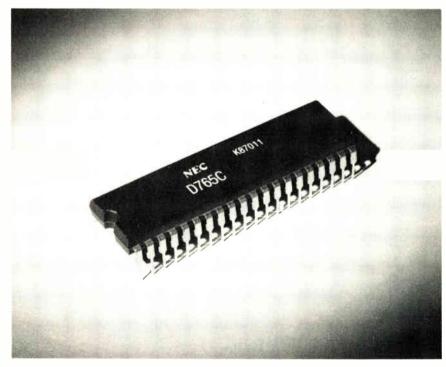
Most floppy-disk controllers have been designed for single- or doublesided, single-density disks. So, with the introduction of double-sided, double-density floppy disks earlier this year, interfacing the disk drives and the central processor has become a problem for most users. But NEC Microcomputers Inc. is offering a solution: the μ PD765C—a onechip n-channel metal-oxide-semiconductor device.

The 40-pin plastic-packaged chip is compatible with both single- and double-density disks. It allows four data record lengths -128, 256, 512, and 1,024 bytes per sector - for each of the two densities. Thus, the chip is fully compatible with standard IBM formats and is also capable of handling a variety of other standard and nonstandard arrangements.

Its multiple device-select lines allow the 765 to control up to four floppy-disk drives. Multiple headselect lines allow for double-sided recording, making possible a multitrack transfer capability in which the chip automatically transfers from a given track on one side of a disk to the corresponding track on the other side. Multisector transfer capability is also provided.

Three scan modes reduce both the time and the amount of main memorv required for handling transactions between the floppy disk and its host computer. One of them compares the entire data field on a disk, on a byteby-byte basis, with data in the processor's memory. This procedure, which is commonly used to verify correct writing onto a disk, needs only half as much main memory as it would if the chip lacked the comparison feature. The other two scan modes identify bytes that are, respectively, greater than or less than a computer-provided comparison word.

The 765 restores the head to track 00 with a seat command. "It's easier to have this command than to have to count steps," says Richard J. Weiner, a member of the micropro-



cessor technical staff. Other features include internal address mark detection circuitry, hand-shaking signals to a phase-locked loop, and programmable head-load time -2 to 256 ms in 2-ms increments. Head unload time can be programmed from 0 to 240 ms in 16-ms increments.

The chip is compatible with the IBM 3740 and System 34 and is designed to work with the 8080A, 8085, and Z80 microprocessors. It is also compatible with the industry-standard 8257 direct memory access chip. The 765 requires a single 5-v dc power supply. It will sell for \$38.10 in hundreds and have a delivery time of 60 days after Oct. 1. NEC Microcomputers Inc., 173 Worcester St., Wellesley, Mass. 02181. Phone Richard Weiner at (617) 237-1910 [411]

Monolithic codec

available commercially

Because it worked with several major manufacturers of telecommunications equipment, National Semiconductor Corp. is shipping the industry's first commercially available monolithic single-channel coder/decoder to meet both U.S. and CCITT specs. Labeled the TP3000, the part is available in both μ - and A-law companding versions.

The codec is fabricated with National's complementary-metal-oxide-semiconductor/bipolar technology and will be followed by a series of monolithic codec systems. It contains all that is needed for a singlechannel pulse-code-modulated codec: input and output sample-andhold circuits, nonlinear digital-toanalog converter, comparator, onchip voltage reference, successiveapproximation logic, digital input/output buffers, auto-zero circuitry, and control logic.

The TP3000 system samples a bandpass-filtered (300-Hz-to-3.4-kHz) analog signal at an 8 kHz rate. It converts the sampled voltage to an 8-bit companded digital code and loads the code into a high-speed serial output buffer that can operate between 64 and 2,100 kilobits per

second. Either system (TP3001 for μ law; TP3002 for A law) will also accept an incoming 8-bit PCM word and automatically interrupt the encode cycle to decode it and update the codec's output sample-and-hold. National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone Kurt Siem at (408) 737-5712 [413]

Baud-rate generator

uses single 5-V supply

A programmable divider, called the COM8046 baud-rate generator, uses depletion-mode loads to let it operate from a single 5-volt power supply. It produces a full spectrum of 16 asynchronous data-communication frequencies for $1 \times$, $16 \times$, and $32 \times$ UART/USRT/ASTRO/USYNRT devices.

Giving the user a choice of 32 output frequencies, the part is fabricated with Standard Microsystems' Coplamos and Clasp technologies. It



contains an on-chip crystal oscillator to provide the master reference frequency and can also accept an external reference. The COM8046 includes a reprogrammable readonly memory and an output disable. The part also may be used as a frequency shift keyer.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11787. Phone (516) 273-8898 [414]

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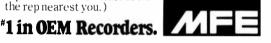
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New products

to within $\pm 1\%$ is available from Silicon General Inc. Designated the SG1503, -2503, and -3503, the devices are interchangeable with the MC1503 and AD580 voltage-reference ICs. They each require less than 2 mA of quiescent current and deliver in excess of 10 mA with total loadand line-induced tolerances of less than 0.5%. Input voltage may range from 4.5 to 40 v. The temperature coefficient of output voltage is less than 20 ppm/°C.

The new voltage references come in three types of packages: a hermetically sealed TO-39, three-pin metal can (T-package); eight-pin ceramic (Y-package); and plastic (M-package) miniDIP. The units can be specified over the full military temperature range of -55° C to $+125^{\circ}$ C, or for less stringent applications.

Price of the SG3503M, for example, is \$1.50 in 100-piece lots. All parts are available from distributor and factory stock.

Silicon General Inc., 11651 Monarch St., Garden Grove, Calif, 92641. Phone J. Castellano at (714) 892-5531 [416]

Fast turn-off SCRs use

compression assembly

Two lines of inverter silicon controlled rectifiers sport up to 20 times the thermal cycling life of conventional SCRs because of the way they are constructed. FMC Corp. compresses the silicon chip of the SCRs between a pair of molybdenum disks so that soldering, intermetallic bonding, and the high-temperature brazing of silicon to molybdenum are eliminated. The result is a compression assembly for the high-current devices, applicable to uninterruptible power supplies and induction heating equipment, that puts far less stress on the chip.

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Both lines are rated at 430 A rms and at 275 A average. The highvoltage 279 series comes in any of six blocking voltages from 700 v to 1,200 v in 100-v increments at turnoff times of 30 or 40 μ s maximum. The 309 series also has six blocking voltages but these are from 100 to **Off-The-Shelf Designs.** Standard Models... We've Got 'Em!

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Solid State Class C Protected Power Amplifiers

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Semiconductor Products Division, FMC Corp., Broomfield, Colo., 80020. Phone Art Connolly at (303) 469-2161 [418]

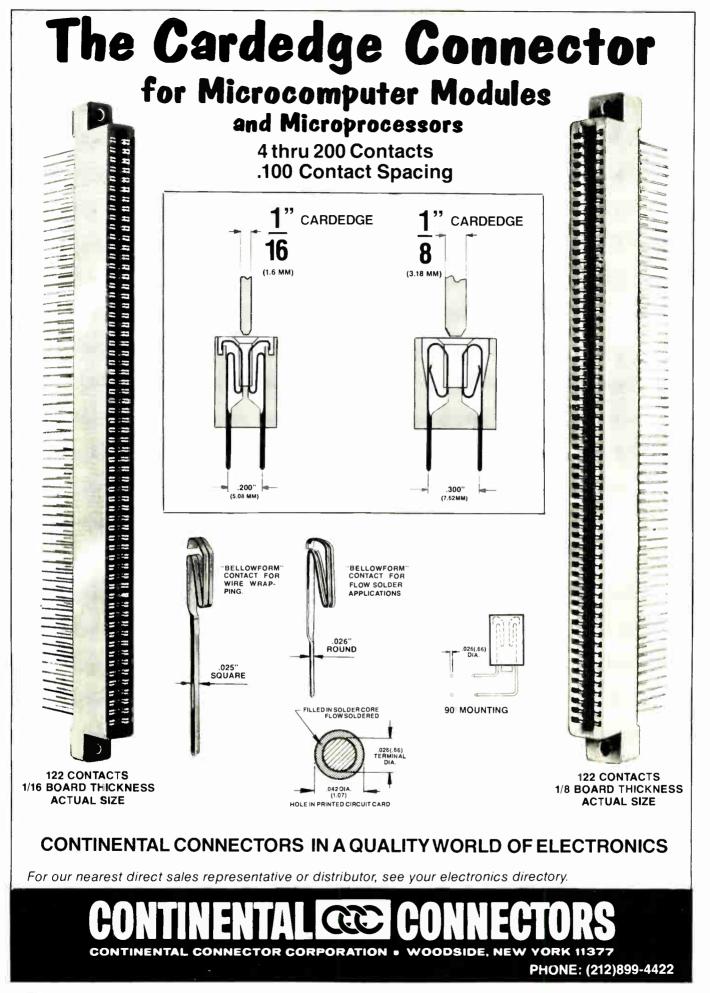
16-K RAM uses single

5-V power supply

Beginning in October, Intel Corp. plans to start supplying samples of a 16,384-bit dynamic random-access memory that operates from a single 5-v power supply. The part also features low power drain in both standby and operational modes and access times lower than 100 ns. "The applications we see for it are in the mainframe area as a replacement for cache buffer memories," declares James Oliphant, product manager for the memory components group. He also targets a market in small systems "where 64 kilobytes would be too much memory."

Dubbed the 2118, the device also offers designers an upgrade from Intel's 2117 16-K RAM, which requires three power supplies. On-chip substrate bias in the 2118 eliminates the need for the -5- and -12-v supplies. Noting that the 16-K market is "going up substantially," Oliphant says that the 2118 is targeted at the market segment that needs speeds normally associated with transistor-transistor logic.

Three speeds will be offered: 80-, 100-, and 120-ns access times. The maximum standby power is 22 mw and operating power is 99 mw for the 120-ns device and 190 mw for the 80-ns version. Prices will be competitive with the 150-ns 16-K devices—under \$15 in high volume. Intel Corp., 3065 Bowers Ave., Santa Clara, Calif. 95051 [419]



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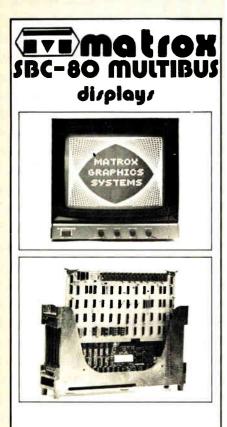
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In most systems that can program a variety of programmable read-only memories, a set of personality cards or modules plugs into a master unit. But E-H International's new model 4 substitutes software for these cards, which usually contain the sockets and electronic hardware required by a particular erasable PROM.

Moreover, the model 4's program accommodates the pinouts for all currently available triple- and singlepower-supply n-channel metal-oxidesemiconductor erasable PROMS, as well as those of the future, according to Jerry D. Rampelberg, program manager of the PROM programmer section. This is because Texas Instruments and Intel have already announced the pinout schemes for their future n-MOS erasable PROMS. "We've even got TI's 128-K part in there," he says.

The program involves more than just selecting the pins of the model 4's pair of zero-insertion-force sockets; it chooses the proper programming algorithm, as well. Triplesupply erasable PROMs use a looping algorithm, whereas the single-supply types program one address at a time, Rampelberg says. Hooked to a microprocessor development system, the model 4 will directly program any single-supply part. However, to program a triple-supply erasable PROM, it first passes the data through an internal buffer, which comprises 16,384 bits of randomaccess memory.

"I'm glad they stopped building the triple-supply EPROMS bigger than $16-\kappa$," says Rampelberg, "because we could get away with $16-\kappa$ of RAM buffer. There's no way we could have made so compact a unit if we had to put 128-K of RAM inside." The unit's designers put the 16-K RAM to other uses, too. For example, a user can store 16-kilobits of data from two 2708s in the RAM and then put it into one 2516 without powering down or changing modules.

Operation of the model 4 is easy. When it is turned on, the unit displays the letter D on its eightdigit readout, to remind the operator to enter the device type. He then presses the D key on the hexadecimal keyboard and follows it with a single hexadecimal number. D₁ through D₃ correspond to the 2704, 2708, and 2716 triple-supply erasable PROMS. D₄ through D_A set up the programmer for the 2508/2758, 2516/2716, 2532, 2732, 2564, 2764, and TI 128-K parts, respectively.

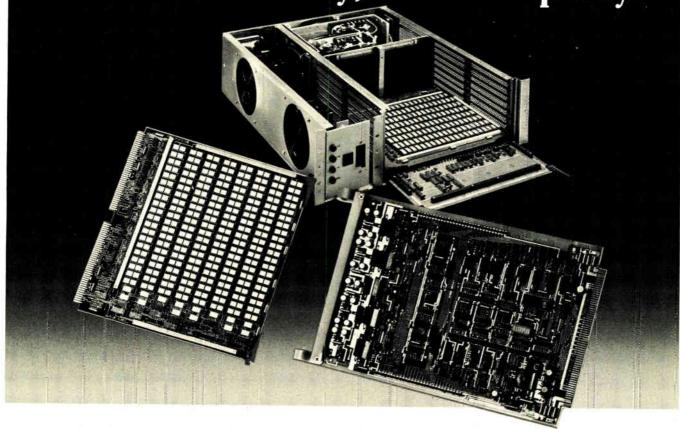
To interface the model 4 with a computer or microprocessor development system, there is an RS-232-C port or a standard 20-mA current-loop port. For in-circuit emulation, a master PROM may be loaded into RAM, removed and replaced with a 24-pin cable and plug, and then the address data stored in the RAM buffer altered to debug both software and hardware in the system being emulated.

The compact \$2,495 programmer is about the size of a desktop adding machine and weighs about 5 lbs. Along with the model 4, E-H is also introducing its model 16B, a gang programming version. In addition to the model 4's programming features, the gang system tests the copy PROMs for proper insertion, opens, shorts, and for adequate grounding and sufficient power-supply current. It also blank-checks them before programming and verifies them afterwards. The 16B's price is \$4,995. E-H International Inc., 650 Almanor Ave., Sunnyvale, Calif. 94086. Phone (408) 245-3900 [391]

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New products



ticed flex that results in endless hours of circuit testing. Thus the latest connector-adapters from Augat will be readily welcomed.

Called the Intra-Switch and the Intra-Connector, the two devices provide a means of thoroughly checking flat cables. The Intra-Switch, shown, allows line-by-line testing of flat cables. Positioned between a male and female connector, the device allows each conductor to be taken in and out of service by means of recessed sliding switches. The switches are pushed open or closed with a pointed implement, say a pen or probe.

When mated to a male header, the Intra-Connector forms a T connector to which two female connectors can be mated. Leaving one side of the T bar unmated provides pinaccess to each conductor in the flat cable, so that the cable can be tested while in circuit.

Both units are available in 20-, 26-, 34-, 40-, and 50-pin versions that mate with standard, dual-row male and female plugs. In quantities of less than 99, prices for the Intra-Connector begin at \$6.10 for a 20pin model. For a 20-pin Intra-Switch, the price is \$12.20.

Augat Inc., 33 Perry Ave., Attleboro, Mass. 02703. Phone (617) 222-2202 [392]

Bonding system automates

chip-to-substrate mounting

A microcomputer-controlled diebonding system, the HMC-1985, automates the mounting of chip

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Circle 212 on reader service card

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Circle 266 on reader service card

New products

components on hybrid substrates. It uses closed-circuit television to allow the operator to work out a bonding routine by interactively programming the system. Once programmed, the system automatically selects the appropriate die collet and positions the substrate for die mounting. Cycle rate is 3,600 cycles per hour, and the basic 200-position memory is expandable to 1,200 positions. With 200-position memory, the HMC-1985 is priced at \$27,500. Hughes Aircraft Co., Industrial Products Division, 6155 El Camino Real, Carlsbad, Calif. 92008. Phone (714) 438-9191 [396]

System tests RC networks for real-time process control

Manufacturers of hybrid circuits who want to gather data on individual resistor-capacitor networks at several production stages have been faced with a dilemma. Should they invest heavily in laser-trim systems, which are capable of providing realtime parameter measurements for process control but are most costeffective only at the trimming stage? Or should they use standard component test systems, which are considerably less expensive but lack the rapid data-reduction capabilities needed for real-time monitoring?

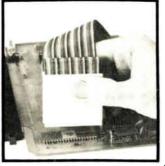
In introducing the model 2230H hybrid-circuit test system, GenRad feels it offers a new choice. The unit adds data-logging and -reduction capabilities, a data-output link, and 4 kilowords of additional randomaccess memory to the company's basic 2230 system. With these features, the system can test, gather data, and reduce it for 25 resistors per second. Moreover, it costs \$25,000, about one fourth the price of laser-trim systems.

The 2230H's data-reduction capabilities include continuous calculation of minimum, maximum, mean, standard deviation, and slope on each component in circuits containing as many as 35 elements. Each component is checked for shorts or opens, and a record maintained on the number passing or failing. A

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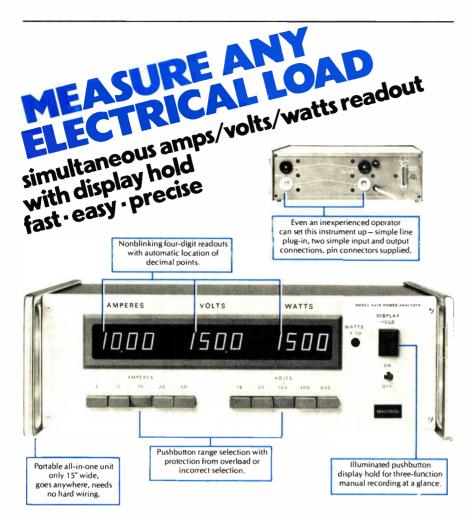
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macro-instruction keyboard lets users program specification limits. scanner connections, component types, and the frequency with which data is displayed.

In addition to the basic 16 scanning channels, 20-kiloword operating system software, 8-kiloword useraccessible RAM, and ohmmeter module, options such as channel expandability to 64 in groups of 16 and a capacitance-measuring bridge module are offered. Delivery is eight weeks after receipt of order. GenRad Inc., 300 Baker Ave., Concord,

Mass. 01742. Phone (617) 369-4400 [393]

Plasma etcher has new slant

on production processing

The MH-100 is a general-purpose production etcher that may make the whole dry-plasma-etching industry stand up and take note. The system is the first commercially available system to use a planar radial-flow reactor with a vertical, rather than horizontal, chamber [Electronics, Aug. 31, p. 117]. This makes loading more convenient and improves cleanliness and process observation.

The microprocessor-controlled unit can accommodate 50 2-in., 33 3-in., or 24 4-in. wafers. It costs about \$85.000.

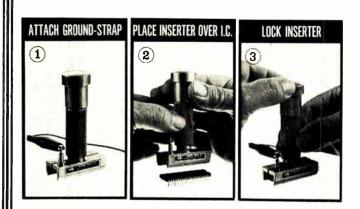
Materials Research Corp., Orangeburg, N.Y. 10962. Phone (914) 359-4200 [399]

Socket-carrier accepts

hard-to-handle packages

The SOT-23 socket-carrier is designed to facilitate testing of SOTpackaged devices, which are growing in popularity, especially among hybrid manufacturers. A three-lead SOT device is loaded into the socket, which snaps easily into the carrier and makes contact with an embedded lead frame. Once loaded, the device is protected and prepared for testing in either a standard flat-pack socket or an automatic handler.

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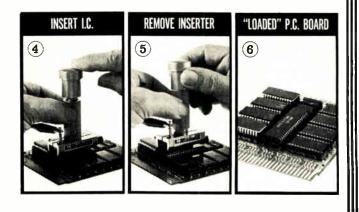


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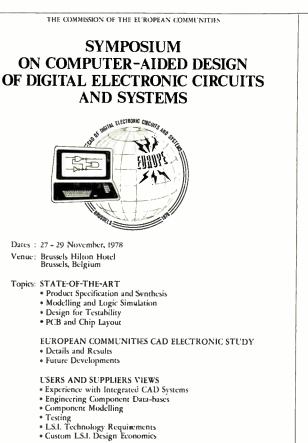
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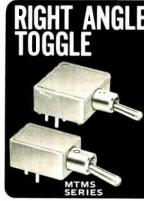


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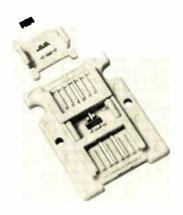
standard grigsby, inc. Dept. 14, 920 Rathbone Avenue Aurora, Illinois 60507

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New products



carriers are priced at \$1.43 in quantities of 1,000 and up and are available from stock.

Textool Products Inc., 1410 W. Pioneer Dr., Irving, Texas 75061. Phone (214) 259-2676 [395]

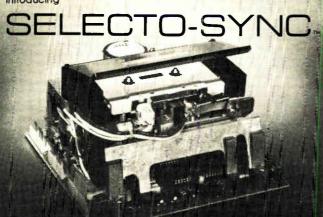
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New products

tions. The unit can either be purchased or leased.

Union Carbide Corp., Electronics Division Materials Group, 8888 Balboa Ave., San Diego, Calif. 92123. Phone (714) 279-4500 [394]

Backplane probes spring

to ensure pin contact

The "A" style spring-loaded probe is designed to provide firm contact with the pins on the back panels of wrapped-wire boards and other pindevices under going test. They are available in seven standard sizes from 0.035 to 0.156, so that they may be configured to accommodate different center-to-center pin spacings. They are priced from \$0.85 to \$1.50 in 100-up quantities and can be obtained from stock.

Everett/Charles Inc., 2867 Metropolitan Pl., Pomona, Calif. 91767. Phone (714) 593-7481 [397]

Tester checks turn-off times

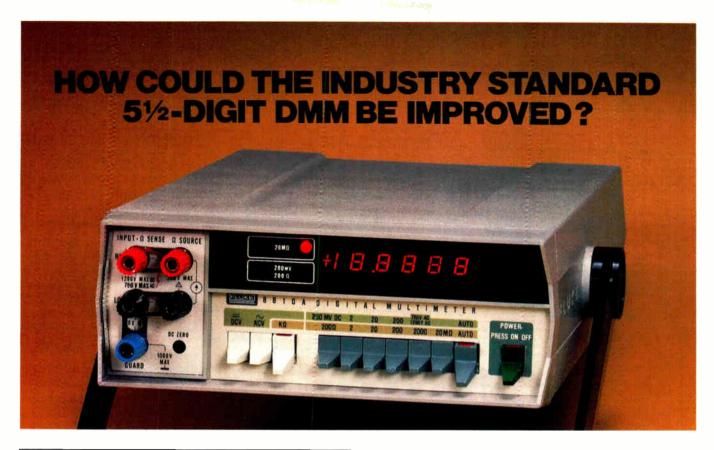
for SCRs and transistors

Capable of measuring silicon controlled rectifier or transistor turn-off times of 10 to 500 μ s, the SCR turnoff-time tester applies forward currents of 10 to 500 μ s and fall rates of 4 to 300 A/ μ s. It also offers reverse voltages of 5 to 50 v, reapplied voltage rise rates of 10 to 500 v/ μ s, and forward blocking voltages of 20 to 2,000 v.

Turn-off times are displayed on a digital readout, turn-off time ranges are continuously adjustable, and a go/no-go failure indicator is provided. An oscilloscope can be used with the unit to monitor all currents and voltages. No special training is required to operate the tester.

The 24-by-29-by-78-in. unit is priced at \$27,000; test fixtures are available at extra cost. Delivery is four to six months.

Semiconductor Division, Westinghouse Electric Corp., Youngwood, Pa. 15697. Phone (412) 925-7272 [401]





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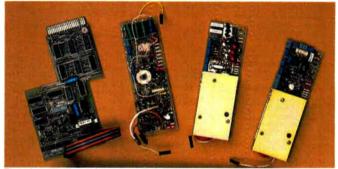
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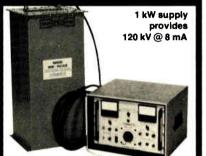
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Microcomputers & systems

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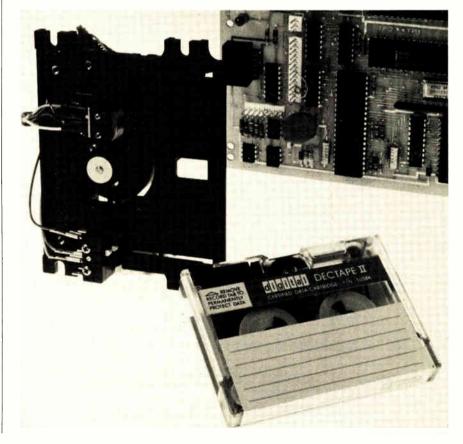
Fixed addresses plus microcomputer add up to easy accessing of data

Microcomputer users looking for mass storage in a microperipheral will be interested in the DECtape II, a magnetic-tape transport from Digital Equipment Corp., aimed at its own LSI-11 family and other plugcompatible microcomputers. Officials in DEC's Marlboro, Mass., components group are billing the unit as a random-access intelligent tape subsystem that can read and write 262 kilobytes of data on blockaddressable, preformatted magnetictape cartridges.

The unit consists of three parts: the DECtape II tape cartridge (which is based on the 3M Co.'s DC-100 cartridge), the tape drive, and a microprocessor controller card that provides the intelligence. Rolando Esteverena says that data is formatted in the unit "in a file-oriented directory, which allows addressing of 512 blocks each 52 bytes long, and it can go randomly to each of these blocks." Esteverena is LSI-11 market and product planning manager in the components group.

The system stores information at fixed positions like a floppy disk device, rather than at unknown or variable positions as in conventional magnetic-tape systems. Because it is a fixed-address device, the host computer does not need to know where the tape has stopped.

To locate a desired block, the host computer requests to read or write a numbered block. The address of the block currently passing over the head is read by the microprocessor, which then calculates the tape motion required to find the requested location and accomplish the requested task. James King, engi-



AN HONEST Our new S68047 Video Display Generator will emancipate you from TTL bondage. It's the easiest, thriftiest way yet to convert your digital data into colorful words and pictures for home computers, games, educational tools, annunciators and remote control indicators. Our singlechip circuit, compatible with the AMI 6800 microprocessor or any other 8-bit computer, saves you at least three times the cost of an equivalent TTL system. It ideas like this. Perhaps that's why AMI has conceived more MOS masterpieces than any other company in the business.

> You can get the picture 14 different ways with the S68047 Video Display Generator. These include six alphanumeric, four full graphics four-color and four full graphics two-color modes.

The 40-pin package, plus a minimal number of support components, connects directly with the TV or color monitor's video circuits, or to the antenna terminals via an external FCC approved RF modulator.

The on-chip ROM provides 64 ASCII 5 x 7 dot matrix characters on a 16 x 32 display matrix. The full graphics density can go up to a maximum of

192 x 256 dots.

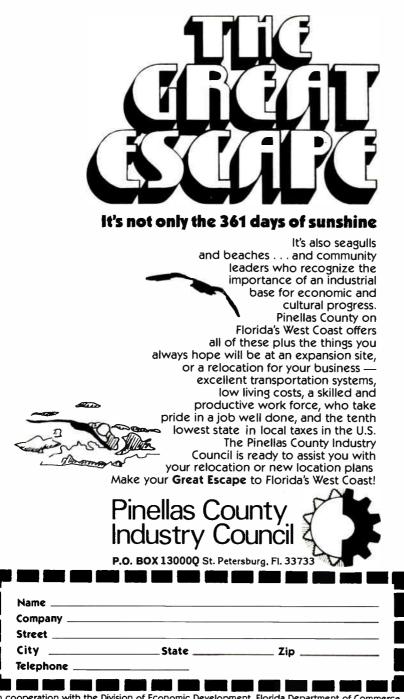
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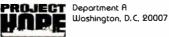
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neering manager, points out that this feature "allows you to go to the middle of the tape to block 37, for example, read and massage the data in that block and put it back into block 37 without disturbing any other information."

Cartridge life is specified at 5,000 passes, and tape length is 140 feet. Read-write speed is 30 inches per second, while speed in the search mode is 60 in./s. Each controller board can drive two cartridges, and average access time is 9.3 s. King is aware that the speed is not blazing minifloppy disks offer access times of 500 milliseconds, he notes, "but our emphasis is on low cost and medium performance."

He adds that DECtape II falls between standard serial cassettes and floppy disks, with faster access and storage—and better data integrity than cassettes—at "about half the cost of comparable products." DECtape II has an asynchronous fullduplex serial output compatible with RS-232-C, -422, and -423 interfaces, with the appropriate interface standard and baud rates selectable by jumpers on the control board. Transmission rates range from 150 to 38,400 bauds.

A single-drive unit has a price of \$620 singly or \$446 in hundreds; prices for the dual-drive model are \$780 and \$562 respectively. Evaluation units will be available in October, with volume production before the end of this year.

Components Group, Digital Equipment Corp., 1 Iron Way, Marlboro, Mass. 01752. Phone Rolando Esteverena at (617) 481-7400, Ext. 6650 [371]

Basic interpreter simplifies

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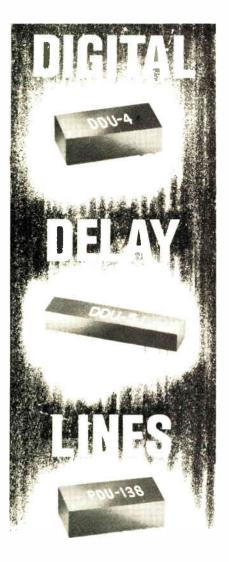
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control commands and the versatility to customize input/output features. The latter two give the power of assembly-language programming with¹ the ease of programming in Basic.

The language consists of a 7-kilobyte interpreter with built-in editor. It takes as little as 5 seconds to load XYBasic into a microcomputer or development system. With the read-only-memory version, XY-Basic appears instantly when the system is turned on. Powerful debugging commands, TRACE and BREAK, let the user follow the execution of the program. The first shows every line that is executed and prints all modified variables; the second interrupts the program at any variable or line number.

Control features include a unique software-interrupt command (ENABLE) that effectively multiplies the power of the user's computer. It allows external-device monitoring and program execution at the same time, and automatically checks to see if the specified condition is met before executing each program statement. A DELAY command builds real-time delays into the program without the addition of a real-time clock. In addition, XYBasic has a number of bit-manipulation commands, such as ROTATE. SHIFT, and TEST, usually found only in an assembler.

In conjunction with the interpreter, a Run-Time/Compiler package has also been developed. This package produces stand-alone systems that execute without special operator start-up commands. The Run-Time/Compiler compresses the XYBasic code, allows programs to run anywhere in memory, and increases execution speed—all in only 5 kilobytes of memory.

Versions are available for all environments. These include SBC/80, CP/M, and Isis-II, as well as the ROM and a ROM Squared version which allows user-generated code to reside in the same ROM as XYBasic. There is also a patchable I/O version that allows the user to tailor XYBasic to fit his system. An extended package includes transcen-

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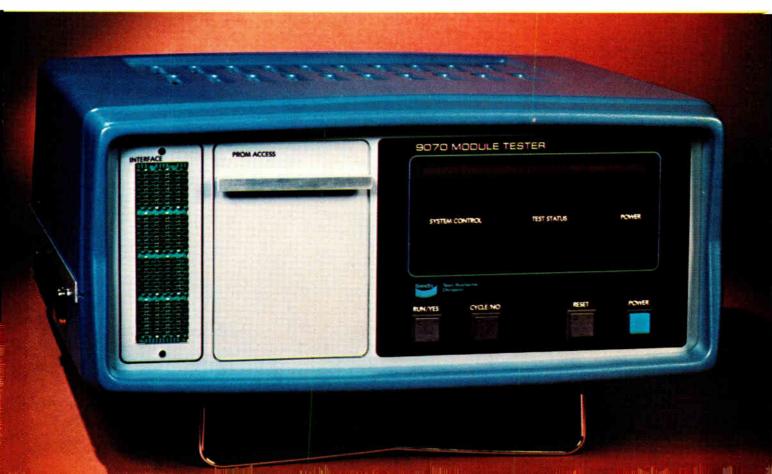
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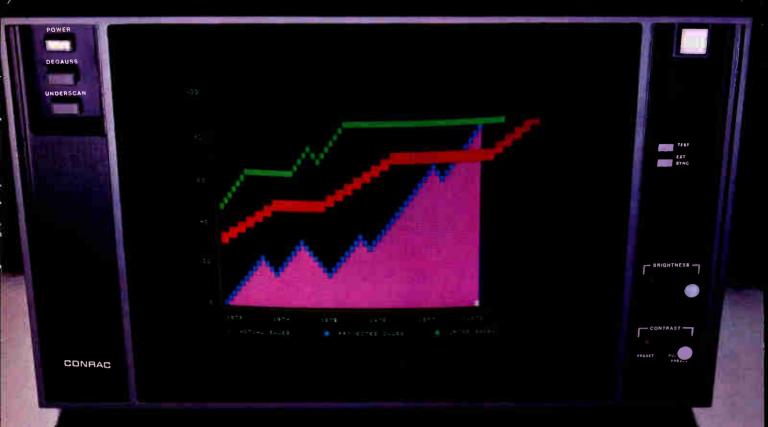


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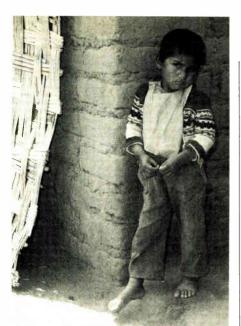
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IMEX Computers, 54 Middlesex Turnpike, Bedford, Mass. 01730. Phone (617) 275-

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On board the DR-115S is refresh circuitry as well as logic circuitry that allows the board to be equipped with a battery backup. Switches mounted in a dual in-line package provide address strapping. In addition, peripheral lockout can be set for the upper 4 kilobits or 2 kilobits of memory.

The DS-115S is priced at \$1,475 for the parity and \$1,400 for the nonparity version. Models with 16- κ and 8- κ memory capacity are also available in parity and nonparity versions. Delivery of the 32- κ DS-115S is 30 days.

Dataram Corp., Princeton-Hightstown Rd., Cranbury, N. J. 08512. Phone (609) 799-0071 [378]



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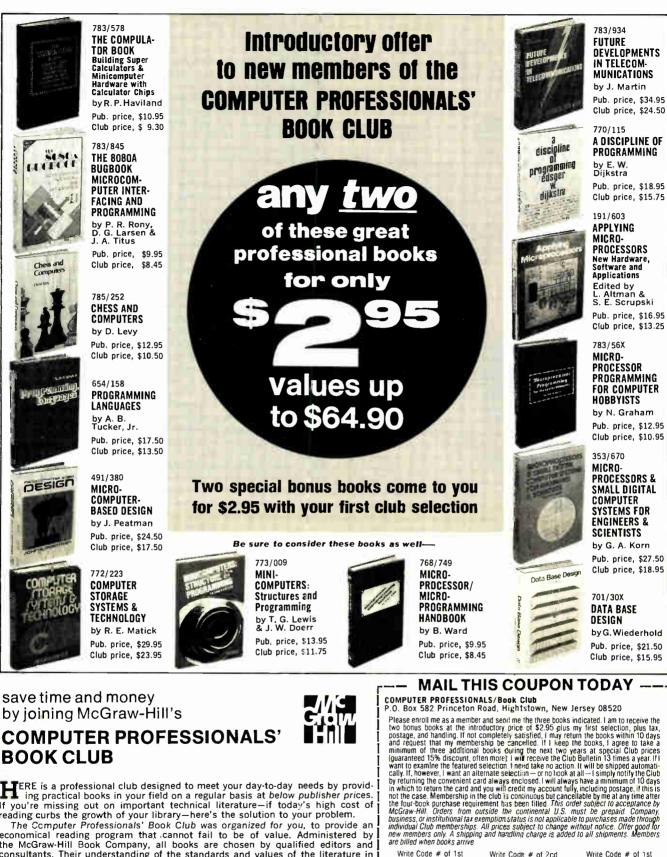
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Other laser-trimming systems adjust the resistances in the R-2R ladder network by cutting a metal link to lop off discrete resistor segments. Intersil's technique allows continuous active trimming of onchip thin-film resistors during wafer sorting. Trimming of the most critical resistors is done on a separate resistor in parallel with a small portion of the main body transistor. "This 'trim tab' technique desensitizes the laser-trimming effect," notes Osgood, "and retains nearly constant density in the main resistor, thus improving aging and reliability characteristics.'

The unit's other specifications also reflect the engineering effort that went into the device's development: maximum nonlinearity temperature coefficient is 2 ppm of full-scale resolution per °C, gain error is 0.3% of FSR, maximum gain error temper-

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ortes and K. Feher's book recently published on Digital Modulation Techniques provide state-ofthe-art material. For additional information, please write or call: **Dr. Kamilo FEHER, P. Eng. Assoc. Prof. Elect. Eng. University of Ottawa Ottawa, Ontario, Canada K1N 6N5 Tel: 613-231-2388** or: Mr. Rene LeHenaff **Tel: 613-231-2355**

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For complete information or a demonstration, contact your local Data Precision representative or Data Precision Corporation, Electronics Avenue, Danvers Industrial Park, Danvers, MA 01923, USA, (617) 246-1600, TELEX (0650) 921819.

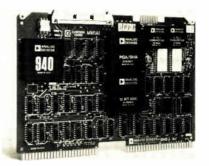
New products

ature coefficient is 5 ppm of FSR/°C, maximum power supply rejection is 20 ppm of FSR/%, and power dissipation is 20 mw.

Intersil Inc., 10710 N. Tantau Ave., Cupertino, Calif. 95014 [383]

System inputs analog data to MM1 microcomputer

Designed to interface analog signals with the Control Logic MM1 microcomputer, the MM1-AI/AO 32channel analog data-acquisition system plugs directly into a slot in that computer's Polybuss. The specific number of channels available depends on whether single-ended or differential inputs are required; up to 32 channels are available in the



former case and 16 in the latter.

The unit's analog-to-digital converter can be configured by users to accept any of three voltage input ranges: 0 to 10 v, -5 to +5 v, or -10 to +10 v. Adding a signalconditioning board allows the MM1-AI/AO board to accept 32 4-to-20mA current-loop signals for industrial and process-control applications. Two 12-bit d-a channels on the board provide output voltages of 0 to 5 v, 0 to 10 v, ± 2.5 v, ± 5 v, or ±10 v.

The system uses memory-mapped 1/O so that the board appears to the microcomputer as a memory block that uses the microcomputer's standard address, data, and control buses. As a result, program storage requirements are reduced and program execution time decreases. The unit is priced at \$1,050 and is deliverable in 30 days.

Control Logic Inc., Nine Tech Circle, Natick, Mass. 01760. Phone (617) 655-1170 [388]

The new DigiTec Datalogger 3000 takes an open-minded approach to data acquisition. Open-minded because it is a comprehensive microcomputer system dedicated to data acquisition; not just a microprocessor based, hardware-oriented datalogger.

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 You refree to define both open tables with any 16 points along any curve to linearize your specific in pouts. And since the Datalogger 3000 is truly a computer, it actually interpolates measurements that fall between points you've entered. The result: the most accurate measurements possible.
- the 3000 can be programmed from the front-panel, a remote CRT terminal or even a host computer.
- and of course an alphanumeric printer, alarm limits with relay outputs and English messages, scaling & offset factors, engineering units, composite video output and other features also come standard on the Datalogger 3000

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For brochure call toll free: (800) 325-6400, ext 77. In Missouri: (800) 324-6600.



Products newsletter_

HP quadruples memory of desktop computer	A new desktop computer from Hewlett-Packard will support up to 256 kilobytes of random-access memory—four times the memory limit of the top-of-the-line 9845 desktop unit. Dubbed the 9835, the microprocessor- based machine will reportedly run programs written in assembly language or Basic. It will be available with either a single-line readout or a full-blown cathode-ray-tube display. The computer will offer direct memo- ry access and 15 levels of interrupt to facilitate data input and output, especially in data-acquisition applications.
Protection, but not cost, added to power supply	ACDC Electronics of Oceanside, Calif., has just redesigned its popular 5-v, 3-A model EC5N3B open-frame power supply so that the unit now includes over-voltage protection as a standard feature. Previously, it was available as an option. The supply was granted UL recognition on Aug. 4.
Programmer ready for the blg PROMs	When 64- and 128-kilobit programmable read-only memories arrive on the scene, Data I/O's System 19 with its 128-kilobit random-access memory capacity will be ready to program them. The standard version of the Issaquah, Wash., company's programmer just made it through design in time for introduction at Wescon/78, according to Wayne M. Paulson, product marketing specialist. "The decision to bring it to the show was made on Aug. 15," he declares. The \$2,225 instrument features 32 kilobits of RAM and a dual serial data port for current-loop and RS-232-C interfaces. It will share booth space with the single-button \$1,495 produc- tion programmer, the System 17.
High-voltage capability added to test system	To satisfy the increasing need for full-voltage testing of high-power components, Teradyne Inc. of Boston is offering a high-voltage power supply that extends the capability of its J273B Linear Test System to 300 v —five times higher than its previous value. The M230 provides programmable current clamping at 30-mA intervals up to a maximum of 200 mA. The \$2,000 unit has a delivery time of 14 weeks.
Low-cost counter area gets more competitive	A pair of 100-MHz counters, scheduled for introduction early next month, seem to herald a shift in Hewlett-Packard's competitive emphasis from a strictly performance approach to a more balanced price and performance one. The counters, an \$800 microprocessor-based unit and a \$375 instrument built with Intersil's 7216 counter chip, are both two-channel types. The higher-priced HP 5315A uses HP's custom multiple-register counter chip and Mostek's 3870 4-bit microprocessor, whereas the less expensive HP 5314A is built with the 10-MHz Intersil IC preceded by a prescaler to reach 100 MHz.
Second sources	 Two equivalents to the Motorola MC1496 and MC1596 double-balanced modulator/demodulators have been announced by Plessey Semiconductors, Irvine, Calif. National Semiconductor Corp., Santa Clara, Calif., has introduced its MM 5257 4-kilobit static RAM—a pin-for-pin replacement for the TMS 4044 made by Texas Instruments.

New products/materials

Quartz materials available for use by original-equipment manufacturers include as-grown cultured quartz bars, lumbered bars, wafers, and dice. The materials are used in the



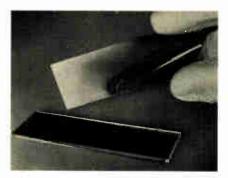
fabrication of microprocessors, channel elements, saws, and other applications requiring a frequency standard. These products come in a variety of sizes and orientations, and can be made to customer specification.

Motorola Inc., Communications Division, 1301 Algonquin Rd., Schaumburg, III. 60196 [479]

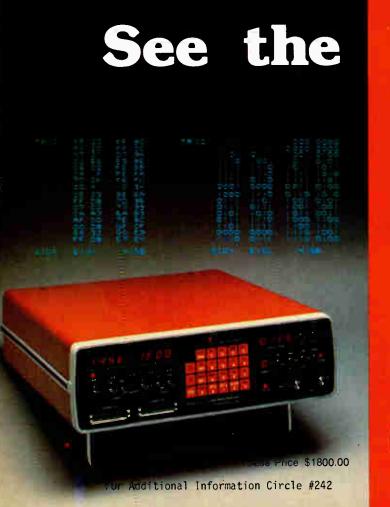
Two pelletized foam concentrates can be used with high-temperature thermoplastics to simplify the injection-molding process. Foam Kon 28 is recommended for use with Nylon 6, 6/10, 6/12, polyphenylene sulfide, polysulfone, polycarbonate, and amorphous nylon. Foam Kon 29 should be used with modified polyphenylene oxide and thermoplastic polyester. The foam concentrates can be handled more easily and offer more consistent shot-to-shot part weights than dry powder blending. In quantities of 1,000 pounds or more, Foam Kon 28 and 29 sell for \$2.05 per pound.

LNP Corp., 412 King St., Malvern, Pa. 19355 [480]

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ohms/sq, a 70% to 80% visible light transmission, and an operating temperature of -60° to 150° C. It sells for \$18 per ft. up to 24 ft. Technical Wire Products Inc., 129 Dermody St., Cranford, N. J. 07016 [475]



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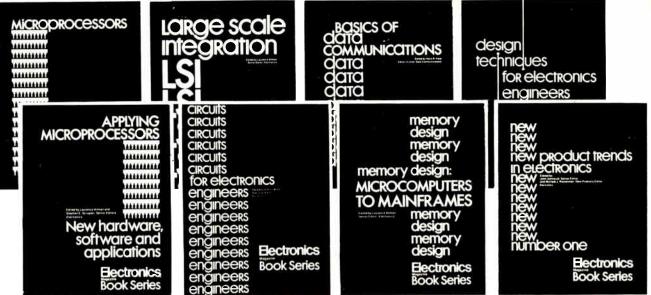
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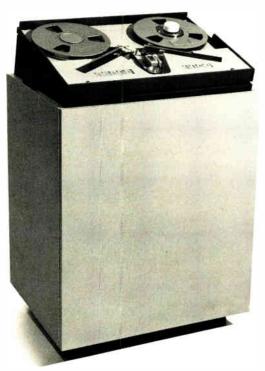
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New literature

Data-acquisition products. A 24page handbook gives detailed applications information for an 8-bit, 8channel data-distribution system; a 12-bit, 16-channel data-acquisition system; a 2-channel analog-output system; and a 2-channel analoginput system. All are tailored for microprocessor-based applications. Specifications are provided for amplifiers, converters, and generators. Micro Networks Corp., 324 Clark St., Worcester, Mass. 01606 [426]

Laminates. Information on preimpregnated materials and multilayer laminates is presented in a six-page brochure. Both single- and doublepressure prepregs, plus such physical properties as tolerance, glass construction, copper-cladding thickness, and dimensional stability, are listed. Graphs show thermal curves for both types when used in hot or cold presses. Included is a prepreg lay-up chart. Lamination Technology Inc., 2720 S. Main St., Santa Ana, Calif. 92707 [429]

Subminiature switches. A 16-page catalog of subminiature and microminiature toggle, rocker, and pushbutton switches containing specifications, mounting information, and



prices is being offered by C&K Components Inc., 103 Morse St., Watertown, Mass. 02172 [427]

Producing character graphics. A Fortran IV subroutine that allows the drawing of six styles of alphabetic characters, three styles of numbers, and 48 special mathematical symbols is described in a 57-page publication. Twenty-two symbols for graph plotting are also given. The program requires a computer that can accommodate a 30-bit word length. The booklet sells for \$2.30 each. Ask for Number 003-003-01921-6. Superintendent of Documents, U.S. Government Printing Office, Washington, D. C. 20402

Subassemblies. More than 200 products, including analog-to-digital and digital-to-analog converters, sampleand-hold amplifiers, analog multiplexers, operational amplifiers, voltage-to-frequency and frequency-tovoltage converters, and power supplies, are presented in a 184-page product guide. Specifications for each product are listed. Teledyne Philbrick, Allied Drive at Route 128, Dedham, Mass. 02026 [432]

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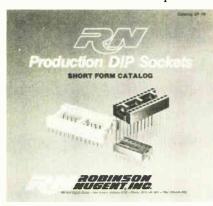
DUAL

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IC sockets. Specifications for the ICN/ICY series of sockets with pins for either soldering or wire wrapping and for the ICL series of low-profile sockets with solderable pins are



listed in a four-page pamphlet that is available from Robinson-Nugent Inc., 800 E. Eighth St., New Albany, Ind. 47150 [431]

Printers and plotters. "Total Output," a 28-page brochure, describes the applications and specifications of 47 printers, plotters, and printerplotters. It discusses how these units can be used in communications, computer-aided design, general data processing, mapping, scientific research, and word processing. Additionally, diagrams show the range of input sources and outputs available, interfacing schemes, Versaplot software organization, and remote and off-line systems. Listed are specifications for resolution, speed, and width, and the number of columns per line, character-set size, dotmatrix dimensions, and the standard available fonts for each unit. Versatec, A Xerox Company, 2805 Bowers Ave., Santa Clara, Calif. 95051 [434]

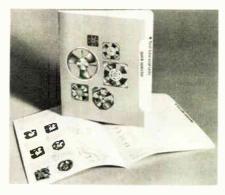
Tube-axial fans. A four-page catalog gives technical information on 11 models of cooling fans for electronic and computer hardware. Performance curves and specifications on

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dimensions, sound, power, and construction are provided. The fans range in size from 3.14 inches in diameter and 1.51 in. deep to 10 in. in diameter and 3.50 in. deep. Technology Services Inc., 16 Wilton Rd., Westport, Conn. 06880 [433]

Photocells. Intended for the design engineer, "Photoconductive Cell Application Design Handbook" discusses the photocell design, theory, and application for 89 types of cadmium-sulphide and cadmiumselenide bulk-effect photoconduc-

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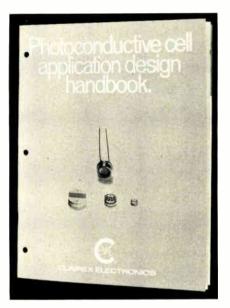


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New literature

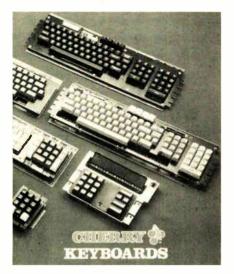


tors. An outline of the design considerations in selecting the appropriate cell is also given. The 24-page handbook also provides spectral response curves for the various photoconductive materials, along with data on temperature-and speed of response. Curves also indicate cell resistance, variation of conductance with hysteresis, color temperature response, and power derating at ambient temperature. A photometry nomograph relates candlepower, distance, and foot candles. Clairex Electronics, a division of Clairex Corp., 560 S. Third Ave., Mount Vernon, N. Y. 10550 [435]

Data communications. Secondhand modems for use with data communications equipment are featured in a 23-page brochure. Specifications and prices are provided for these modulator-demodulators, which operate at speeds from 2,400 to 9,600 bits/second. Also offered are adapters and accessories, and solid-state buffers, for use with the devices. Racal-Milgo Information Systems Inc., 8600 N. W. 41st St., Miami, Fla. 33166 [436] Radio-interference measurement. The International Special Committee on Radio Interference has released a 213-page document on radio-interference measuring apparatus and methods. This publication includes the texts of all related documents, recommendations, specifications, and reports. Information is provided on measurement apparatus, conduction and radiation measurement of radio interference, audiofrequency interference measurement, disturbance measurement due to switching operations, and the statistical considerations in determining the limits of radio interference. Ask for C.I.S.P.R. 16. International Electrotechnical Commission, 1 rue de Varembe, 1211 Geneva 20, Switzerland [437]

Keyboards. To make it as easy to order a custom keyboard as to buy a standard one, this 32-page catalog supplements information on five





standard keyboards and accessories with a designer's worksheet for those who need specialized boards. Several pages of diagrams point out the differences between these products. Additional aids are a keyboard timing and specifications chart. Ask for KBC-78. Cherry Electrical Products Corp., P. O. Box 718, Waukegan, Ill. 60085 [421]

Specification guide. "The Electro-Mechanical House," a 112-page catalog contains a wide assortment of Hollingsworth solderless terminals and connectors, Molex nylon connectors, Bivar printed-circuit board hardware, and Waldom Speedy-Tys spacers and electronic hardware. Specifications and dimensions are given for the items listed. Waldom Electronics Inc., 4301 W. 69th St., Chicago, Ill. 60629 [422]

Resistors. Electrical, environmental, and mechanical specifications for Cerbon and cermet trimmer resistors are given in a 16-page brochure. It is available from Centralab Electronics Division, Globe-Union Inc., 5757 N. Green Bay Ave., P. O. Box 591, Milwaukee, Wis. 53201 [423]







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New books

Energy Reference Handbook, 2nd ed., Thomas F. P. Sullivan, Government Institutes Inc. (Washington, D. C.), 344 pp., \$15.95.

Process and Device Modeling for Integrated Circuit Design, Fernand Van De Wiele, Walter L. Engl, and Paul G. Jespers, eds., Noordhoof International Publishing (Reading, Mass.) 867 pp., \$39.50.

Surface Wave Filters: Design, Construction and Use, Herbert Matthews, ed., Wiley, 521 pp., \$29.95.

Topics in Applied Physics, Vol. 19: Optical and Infrared Detectors, R. J. Keyes, ed., Springer-Verlag, 305 pp., \$39.60.

Handbook of Simplified Solid-State Circuit Design, 2nd ed., John D. Lenk, Prentice-Hall, 429 pp., \$16.95.

The Radio Amateur's Handbook: The Standard Manual of Amateur Radio Communication, Tony Dorbuck, ed., American Radio Relay League (Newington, Conn.), 711 pp., \$8.50 (paper).

The Assurance Sciences: An Introduction to Quality Control and Reliability, Siegmund Halpern, 431 pp., Prentice-Hall, \$16.95.

Electronics Dictionary, 4th ed., John Markus, McGraw-Hill, 864 pp., \$24.50.

Integrated Circuits Technology and Applications, F. F. Mazda, Cambridge University Press, 210 pp., \$24.95.

Thin Films: Interdiffusion & Reactions, J. M. Poate, K. N. Tu, and J. W. Mayer, eds., Wiley, 578 pp., \$35.00.

Telephony and Telegraphy, 3rd ed., Sydney F. Smith, Oxford University Press, 278 pp., \$16.50.

Take a Chance with Your Calculator: Probability Problems for Programmable Calculators, Lennart Rade,

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New books

Dilithium Press (distributed by ISBS), 163 pp., \$6.95 (paper).

Using Digital and Analog Integrated Circuits, L. W. Shacklette and H. A. Ashworth, Prentice-Hall, 303 pp., \$10.95 (paper).

Digital Image Processing, Rafael C. Gonzalez and Paul Wintz, Addison-Wesley Publishing, 431 pp., \$29.50 (hardcover), \$19.50 (paper).

The Theory of Information and Coding: A Mathematical Framework for Communication, Encyclopedia of Mathematics and its Applications, Vol. 3, Robert J. McEliece, Addison-Wesley, 302 pp., \$21.50.

Symmetry and Separation of Variables, Encyclopedia of Mathematics and its Applications, Vol. 4, Willard Miller, Addison-Wesley, 285 pp., \$21.50.

Analysis of Linear Dynamic Systems, John B. Lewis, Matrix Publishers, 862 pp., \$29.95.

Handbook of Practical CB Service, John D. Lenk, Prentice-Hall, 323 pp., \$14.95.

Computer Modeling of Gas Lasers, Kenneth Smith and R.M. Thomson, Plenum Press, 416 pp., \$42.50.

Current Interruption in High-Voltage Networks, Klaus Ragaller, ed., Plenum Press, 360 pp., \$37.50.

Data Processing Cost Reduction and Control, Dick H. Brandon, Van Nostrand Reinhold, 191 pp., \$17.95.

Passive and Active Microwave Circuits, J. Helszajn, John Wiley & Sons, 274 pp., \$27.50.

Handbook of Audio Circuit Design, Derek Cameron, Reston Publishing (a Prentice-Hall Co.), 255 pp., \$17.95.

Dictionary of Logical Terms and Symbols, Carol Horn Greenstein, Van Nostrand Reinhold, 188 pp., \$11.95.

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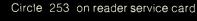
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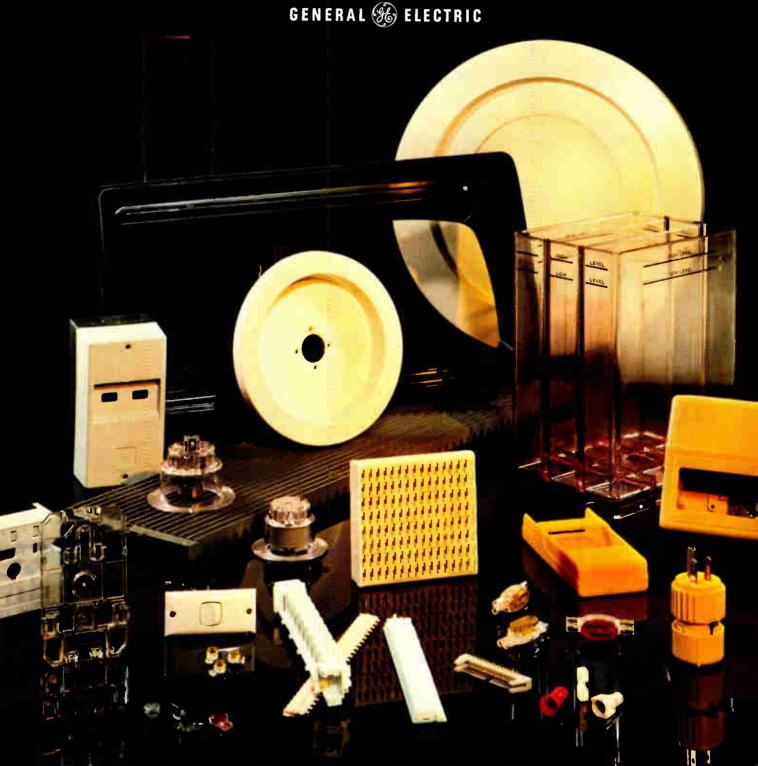
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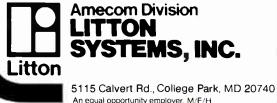
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Detection/estimation theory

- Advanced signal processing techniques
- Classical or modern control theory
- Target signature analysis
- Optical design/analysis
- Pattern recognition
- Real time software design
- Waveform analysis
 Kalman filter and estimation theory

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Experienced in microwave circuit design. Duties will involve Circuit Analysis/Design for automatic test station and writing programs for automatic test units and circuit subassemblies. A background on equipment operating at frequencies up to 16 CHz is desirable.

COMPUTERIZED TEST EQUIPMENT ENGINEERS

• Experience in digital/logic and analog circuit design. To perform digital and analog circuit analysis/design for an automatic test circuit cards. Power supply design/analysis experience desired for some positions.

• To design software/hardware for minicomputer-based automatic test equipment. Requires experience on digital systems. H.F. 21MK/RTE experience highly desirable.

SYSTEMS TEST & EVALUATION ENGINEERS

To perform developmental test of missiles at systems/subsystems level; plan tests and evaluate results. Experience desired in guided missiles, avionics, or airborne radar technology. Digital hardware and software helpful. BSEE desired.

CIRCUITS DESIGN ENGINEERS

With recent relevant experience in the design and development of RF/IF, digital, or analog circuits for missle guidance systems. MSEE, software/hardware integration experience also desirable. Must be familiar with applicable state-of-the-art components phase and frequence look loops, wide and narrow receivers, use of microprocessors.

SYSTEMS ENGINEERS

These positions require system engineering for missile systems using radar and electrooptical technologies. This includes defining design characteristics, interfaces, test requirements, and performing trade studies. Weapons experience not required, but previous systems engineering, servo analysis, or circuit or logic design experience in the above technologies is desirable.

SYSTEMS ANALYSTS

To perform design and anlaysis for state-of-the art electro-optical missile seekers. Job assignments require ability to develop mathematical models for missile guidance systems performance evaluation. Proficiency in advanced one and two-dimensional signal processing techniques desired.

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To participate in digital systems analysis and designer trade offs on RF components, subsystems and systems. Write design requirements, specifications and test requirements. Do RF modeling, hybrid missile flight simulation. Knowledge of Machine Languages, Basic and Fortran. Familiarity with microprocessor use in analytical and control systems. Interface equipment to systems.

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Several openings in our ROLAND Division for system test engineers with a background or interest in computer based automatic test equipment, for testing L band and K_u band radar units. Must be familiar with Basic or Atlas programming. Will be responsible for unit application software development, maintenance, and tasks related to production test stations.

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Experienced in CAD, including interactive graphics; ability to do product design for highrated production and knowledge of hybrid microelectronis and circuit partitioning required. Design experience in hybrids and electronic subassemblies desirable.

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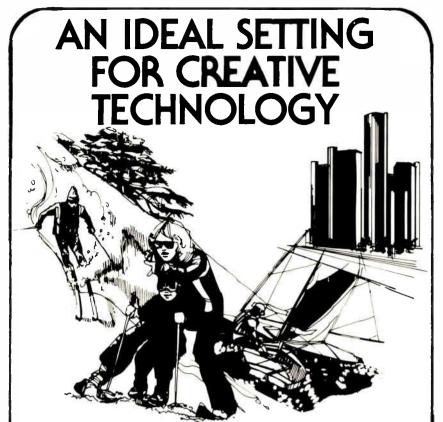
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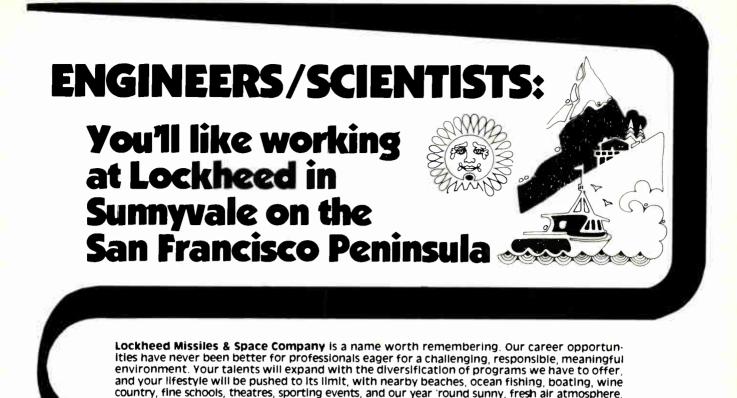
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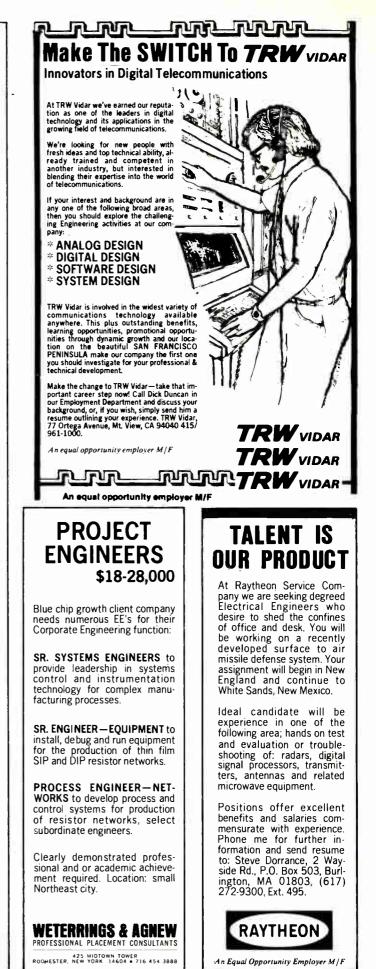
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HTL/CMOS

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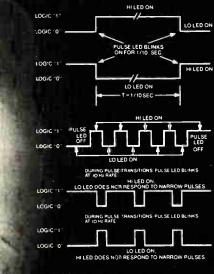
visible; in MEMORY position, first transition lights and latches LED

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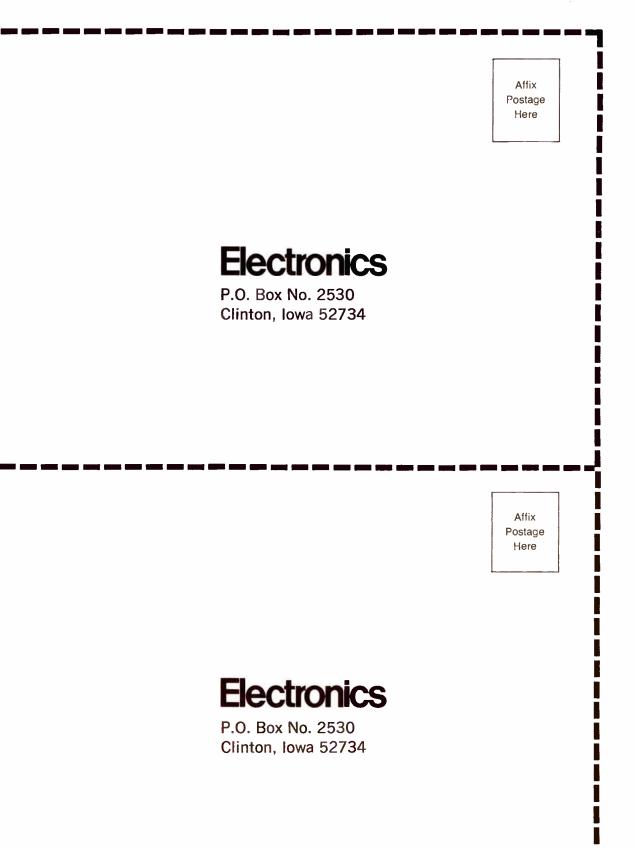
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