MAY 22, 1980

VOICE IS THE TALK OF THE INDUSTRY/95

32-bit minicomputer adopts a mainframe look / 130 What designers should know about power MOS FETs / 143



SPECIAL REPORT



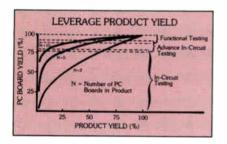
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circuit testing provides a relatively small increase in board yield. But as you can see from the accompanying diagram,

As you can see increasing cost of savings to be go ment such as substantial in or able break-everyou determine the 3060A work enough reductions.

To he for you

this small increase can mean a large improvement in product yield. For example, in a 5 PC board product, an increase in board yield of only 8% (from 90% to 98%) will leverage product turn-on rate from about 59% to 90%.

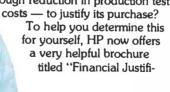
The impact of leveraging on production test costs.

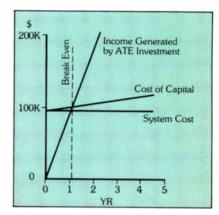
As you may have already discovered, production testing costs increase exponentially. In other words, a fault that costs 18¢ to find during in-circuit testing can easily cost \$20 or more if not detected until final product test. Why? Because of the additional time — and increased labor costs — associated with fault diagnosis and repair at this level.

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cation — Circuit Test Systems." It includes a production test model worksheet, and has guidelines for calculating the 3060A Automatic Board Test System's payback period, average return on investment and/or discounted cash flow. You can use this information to determine the rate of return offered by the HP 3060A in your facility, even in light of today's highinterest economy. For your free copy of "Financial Justification — Circuit Test Systems," or for more information on the HP 3060A, (Priced at \$85,000* for standard operational system) write to Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304, Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

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Electronics



The International Magazine of Electronic Technology

Vol. 53, No. 12 • May 22, 1980

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Highlights

Cover: 64-K RAMs trudge many rocky paths to production, 119

Picking their way among alpha-particle, lithographic, material, pinout, and power-supply obstacles, manufacturers of the coming generation of 64-K (and larger) dynamic random-access memories expect to have the big chips in volume production by 1983. A special report looks at the wide variety of cell and sense-amplifier designs, chip layouts, and alpha-proofing techniques being explored by the score of companies in serious contention for slices of this potentially huge market.

Cover illustration is by Sean Daly.

Speech technology spurred by consumer products, 95

Fledgling technologies for speech synthesis and recognition are due to see steep market-growth curves, according to observers. A comprehensive review of the field underlines the importance of large-scale ICs in bringing speech synthesis to the commercial sector—and speech recognition is not far behind.

When does a minicomputer become a mainframe? 130

A 32-bit computer designed for full compatibility with the Eclipse family of 16-bit minicomputers and existing software defies neat classification. Data General may view itself as a minicomputer maker, but the MV/8000's 4.3-gigabyte virtual memory space puts it in the big leagues, as does its hardware architecture: multiple buses and separate instruction and data caches serve a pipelined, microprogrammed central processor.

Power MOS FETs are taking over more bipolar turf, 143

MOS FETs made for power-switching jobs, which compare favorably with established bipolar parts in terms of switching speed, drive needs, multipledevice operation, and cost, are moving into higher-power areas. Designers used to working with bipolar devices should familiarize themselves with the techniques and tradeoffs involved in applying the three basic power FET structures currently built.

Japanese make serial communications chip for Intel line, 167

Nippon Electric Co. is marketing in the U.S. an MOS chip designed specifically as a two-channel serial communications controller for use with 8080s, 8085s, and 8086s—plugging a hole in the line. It supports bit- and byte-oriented protocols at programmable transmission rates.

. . . and in the next issue

A special report on LSI in communications . . . a chip pair for rf remote control of toys and models . . . changing manufacturer-customer relationships in the era of very large-scale integrated circuits . . . a two-chip 18-bit digital-to-analog converter with 16-bit linearity.

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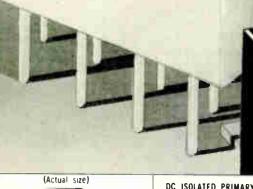
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T2.5-6	2.5	.01 100	\$3 95
TM02.5-6	2.5	.01 100	\$6 45
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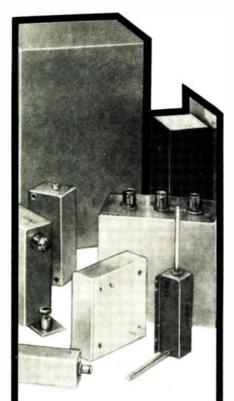
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Publisher's letter

Affordable speech-synthesis and recognition capability is just over the horizon. And as Bruce LeBoss, San Francisco regional bureau manager, points out in the Inside the News feature on this subject (p. 95), people will soon be surrounded by the chatter of hardware conversing in many languages.

Companies are already demonstrating equipment that converse audibly with other equipment. In one setup two terminals are able to tell those old "knock-knock" jokes and may soon be ready to deliver the famous Abbott and Costello "Who's on first?" routine.

In a more serious vein, Bruce reports that to some the arrival of speech input/output capability today is much like the development of the first microprocessors almost a decade ago. There is that same intense effort to find ways to exploit speech capability in products ranging from dolls to industrial process control systems. Also, as in the early days of microprocessors, many users will depend on advice and guidance from suppliers.

Still another aspect of speech I/O that impressed Bruce was the feeling of being on the brink of a new technology explosion—again quite like the early days of the microprocessor. This feeling was dramatized at a one-day seminar on speech synthesis and recognition sponsored by the Institute of Electrical and Electronics Engineers' Computer Society in the Bay Area. The meeting took place on a sunny Saturday, the kind of day most residents would be out playing golf or tennis.

"They expected about 75 to turn up, but I counted over 200," Bruce reports. "People were there not just out of curiosity, but in a serious effort to exchange information."

The crowd was too big to have lunch in the cafeteria at Hewlett-Packard where the sessions were held. Instead, everyone took to the outdoors and ate box lunches picnic-style. "I got the impression that sitting on the lawn in the warm sun was the core of people involved in the hottest technology for the next decade," Bruce observes.

It was not quite the case, since speech technology has quickly become an international bandwagon. As usual the Japanese appear to be a major factor in both synthesis and recognition, especially for consumer applications. In software, however, the U.S. has the edge, Bruce notes.

As for Europe, a large part of the speech effort is coming from government research. The British Post Office has a telephone directory service project and two French labs are working on communications applications.

This is a good time to take a look at dynamic random-access memories, especially 64-K RAMs. That's what solid state editor John Posa reasoned as he set out to prepare the special report on page 119.

"A lot of promises were made, but actual deliveries have been delayed," John points out. "Nevertheless, the 64-K RAMs will be produced and delivered."

More impressive still will be the 256-K RAMs, he adds. Building these will require real processing tricks. "The stored charge in the memory cell is diminishing, so it is harder to sense and store. And alpha particles are likely to create more and more problems."

But John stresses that, as for the 64-K memories, these problems will be overcome and the 256-K RAMs will be developed and produced. "Such devices are incredible, when you think about it," he says. "Four of them will equal a megabit of memory in a 2-square-inch space."

What's next? Dynamic RAMs are said to be composed of single cells but in fact each cell contains a storage capacitor and a switching transistor. According to John, down the road is a new class of cells that will combine the storage capacitor and the switching transistor. These will be truly single cells.



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Readers' comments

No more expansion

To the Editor: The editorial "Looking beyond the EE boom" [Feb. 14, p. 28] presented a needed reminder of the painful consequences of a boom-and-bust employment situation for electronics engineers. In contrast with the National Science Foundation's rationale for new spending programs described in the same issue ["Budget opens seller's market for EES," p. 95] is the Cassandra-like warning of an economist who predicts that "there's a serious recession coming." Some comments:

The National Science Foundation

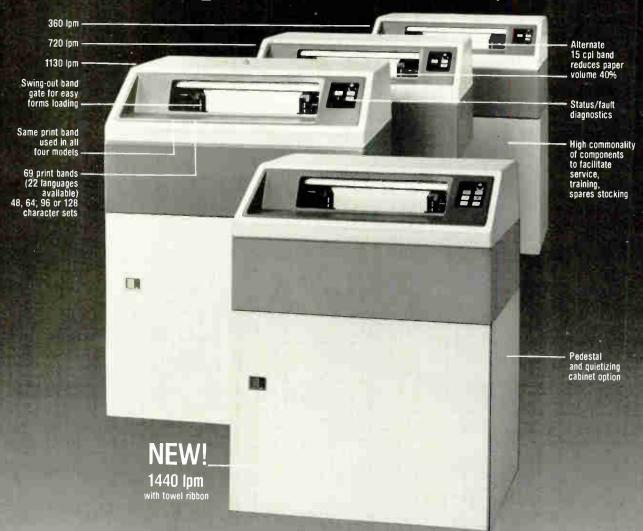
The National Science Foundation exists to serve the academic community, not the nation. By law, fully 99% of its research and development funds are reserved for the universities. The NSF has always predicted a shortage of engineers. Now its cry is "We need a broader national base for engineering education." Thus, with this single unproven allegation, the NSF has pulled off a remarkable feat. It has succeeded in obtaining a huge funding increase for its clients, the universities, and all this despite the sharp decrease in student enrollments

■ In contrast, the (also unproven) allegation of a serious recession to come is made by those who have no axes to grind.

In view of these points, what strategy should the American EE community adopt? To me, the answer is clear. Given the experiences of EEs who are now skilled taxicab drivers, employees of fast-food outlets, and gardeners; given the fact that, despite the alleged shortage, the real income of an EE is now less than it was in 1972 (the Institute of Electrical and Electronics Engineers' own figures); and given the self-serving nature of the academics and the corporate executives (both of whom benefit from an oversupply of EEs), the American EE cannot permit any expansion in the output from the engineering colleges. Nor can we permit any additional aliens to be trained or to work in the United States.

> Irwin Feerst Committee of Concerned EEs Massapequa Park, N. Y.

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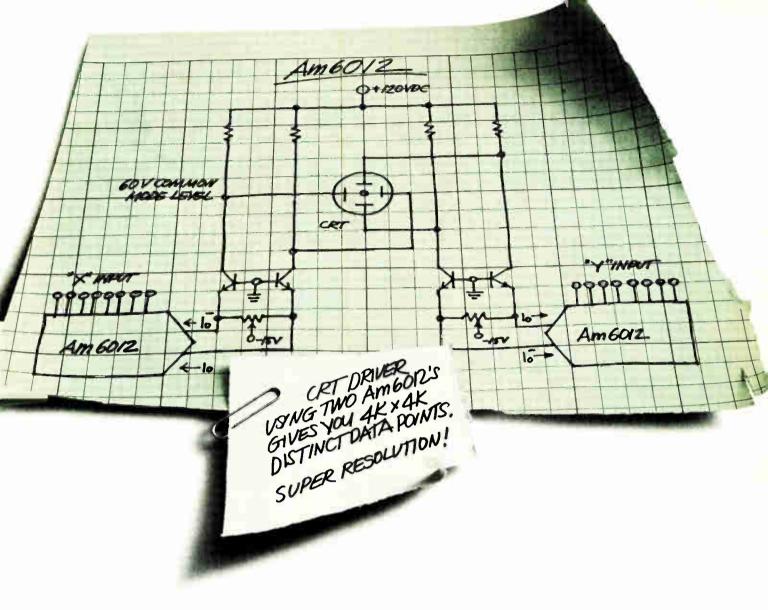
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News update

■ Competition is heating up in highspeed 4-K static random-access memories now that Hitachi Ltd.'s 6147 is available in quantity. The Japanese RAM is aimed straight at Intel Corp.'s pioneering 2147 fast static device.

The two parts have the same speed, with access times between 55 and 70 nanoseconds, and the same price range of \$30 to \$35, depending upon speed selection. However, the 6147 [Electronics, Dec. 20, 1979, p. 81] has complementary-MOS peripheral circuitry combined with an n-channel MOS storage array using doped polysilicon loads, whereas the Intel 2147 is strictly n-channel with depletion loads.

Power. As a result, Hitachi's part has an active power dissipation said to be five times better than the low-power 2147L's maximum of 700 milliwatts. It does not fare as well on standby dissipation because the chipenable line does not shut down the input address buffers upon deselection. Thus, if the address lines are allowed to toggle, power-down consumption shoots from a best case of 10 microwatts to a worst case of 60 mW, which the 2147L beats with 50 mW.

The price comparability staggers U.S. chip makers, for the 6147 requires 13 or 14 masking steps where Intel is said to get by with as few as 8. However, the much smaller cells and die size of the Hitachi part could improve its yield.

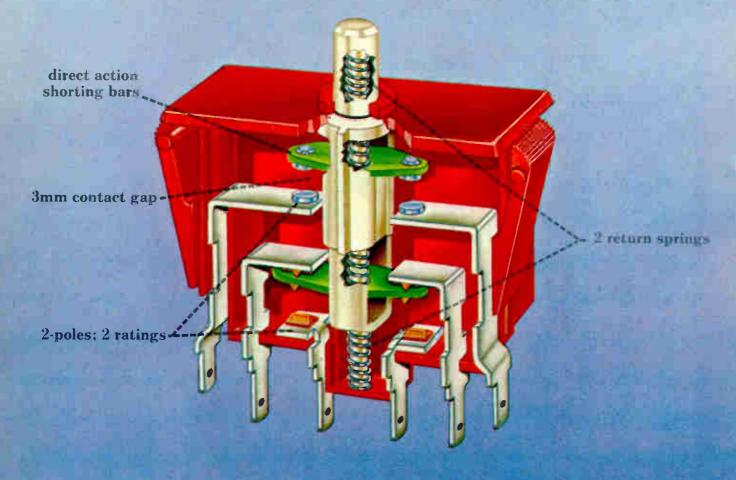
Also, Hitachi surrounds the memory matrix with an ubiquitous p well. The junction formed just below the storage nodes sweeps away carriers generated by an invading alpha particle, so that more parts may pass reliability tests.

Fighting back, Intel is using its leading-edge HMOS-II technology to produce the 2147H with 35-to-45-ns access times. Hitachi customers find that 6147s specified at 55 ns invariably perform at 45 ns, but some 2147H users find that their part can dip below 25 ns.

This gives Intel a clear-cut speed advantage because 25 ns is not just 20 ns faster than 45—it is 55% quicker.

-John G. Posa

LINE-INTERRUPT switch meets latest specs... WORLDWIDE



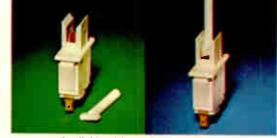
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Both devices are ideally suited for such non-contact sensing applications as paper or card edge detection, motor speed controls, EOT/BOT sensing,

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People

Wendt wants to place Sperry on technology's leading edge

Robert L. Wendt, the new president of the Sperry division of Sperry Corp., is going to push his military-oriented company to the technological edge. "I'm going to take a hard look at our technological position," he says, adding, "We've been doing state-of-the-art work in a limited number of areas; I'd like our reputation to be more noteworthy. We have a strong technical base for growth over the next 5 to 10 years. In five years, I want to double our present revenue size." That revenue was \$486.1 million in 1979.

Wendt, 59, is a 40-year veteran with Sperry. He joined the Great Neck, N. Y., division in 1940 after graduating from Harvard University with a bachelor's degree in physics and electrical engineering. He has held several engineering and managerial positions since then, including manager of the Polaris/Poseidon navigation subsystem program from 1964 to 1969; vice president and general manager of Sperry division's systems management unit from 1971 to 1975; and most recently, vice president and general manager of the Sperry Gyroscope unit from 1975 until his appointment as division president. Wendt succeeded the late Salvatore A. Conigliaro [Electronics, April 10, p. 46].

Wendt would like to see the Sperry division become more of a prime contractor and less of a subcontractor on military systems. "We've been moving toward the position of prime contractor in the last few years. We've been in the forefront among electronics—as opposed to aerospace-companies in taking responsibility," he says. "There are a couple of advantages to being the prime contractor. It enables us to tap our skills while providing a better product. In major program management we're able to capitalize on our strengths. I'd rather do the overall job than part of that job," he observes. Sperry is currently bidding on a Canadian patrol frigate contract, where it would be the contrac-



Moving up. If Sperry's Wendt has his way, the firm will do more prime contracting.

tor for the complete weapons systems and for the vessel itself.

Specifically, Wendt sees Sperry expanding into, among other areas, millimeter-wave devices, laser gyro field equipment, simulators and trainers for aircraft and ships, and software. "I want us to be better balanced as a military systems house," he sums up. "One of the thrusts I'll be pursuing is more Army, Air Force, and overseas business to balance our long-standing business with the Navy."

List sees close relations with buyers of speech chips

The ability to produce low-cost synthesized speech using semiconductor components will lead to new generations of talking products and equipment. But first there will be a great deal of talk between the chip vendors and their customers.

That's the opinion of Bernard H. List, vice president and corporate speech strategy manager for Texas Instruments Inc.'s new Speech Technology Center in Midland, Texas [Electronics, May 8, p. 33]. The 52-year-old List believes that selling speech chips will require much closer relationships with the original-equipment manufacturers that are the customers that semiconductor makers have been used to. Customers, of course, will be concerned with

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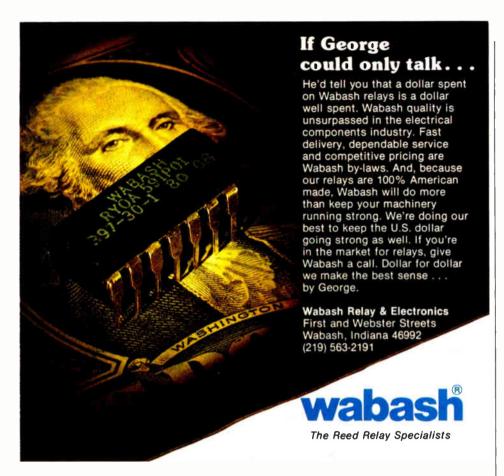


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People



Linguist. Tl's List believes establishment of regional centers is key to speech sales.

speech quality. As List puts it: "That's a very subjective and intangible kind of thing. Everybody hears sounds and interprets them differently. We've found that out just within TI."

As a result, the new speech chief feels that his company's commitment to establishing geographically dispersed regional technology centers "will be key in bringing speech technology to large numbers of customers." TI currently has centers open in Chicago and Boston that will provide a range of vocabulary development services to customers. List says that TI will aid customers in developing "personalized" voices for their products.

List has a background well suited to guiding an emerging technology such as speech synthesis. After receiving bachelor's and Ph.D. degrees from Johns Hopkins University in his native Baltimore, he worked in research and development at the Battelle Memorial Institute in Columbus, Ohio, before joining TI's research laboratories in 1957.

In 1970, he took a leave of absence to work at the Wright-Patterson Air Force Avionics laboratory as chief scientist. He eventually became lab director there and then returned to TI in 1976. Before being named last month to head the newly established speech organization, List was vice president for the firm's U. S. MOS operations in Houston.

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The CPU employs three microprocessors, the 6502, the Z-80 and the 6800. And the processor bus has been designed so new, more powerful micros (like 16 bit CPU's) can be added to the system later on.

There are also 10 open slots in the basic C3-C. The system supports up to 768K bytes of memory, in a multi user configuration.

The C3-B. 74 Megabytes. Under \$13,000.

For those who require even more hard disk storage, Ohio Scientific offers another microcomputer in the C3



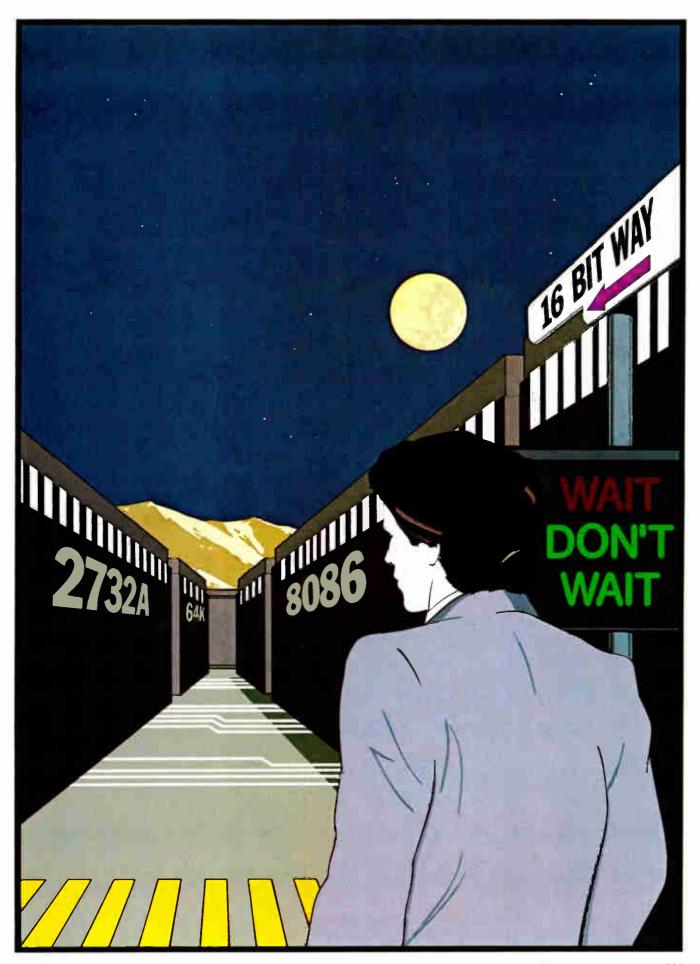
Series, the C3-B. Its specifications are the same as those of the C3-C. However, the C3-B offers a 74 Megabyte Winchester drive.

For those who do not need hard disk capacity now, but in all probability will need it in the future, Ohio Scientific offers the C3-A. It is like the C3-B and the C3-C in all respects but two. 48K RAM is standard in the C3-A, and it offers 12 open slots. When more storage is needed, the C3-A is easily expandable to either a 23 Megabyte or 74 Megabyte hard disk system. The C3-A is priced at less than \$6,000.

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2732A	64K
Pin Configuration	Pin Configuration
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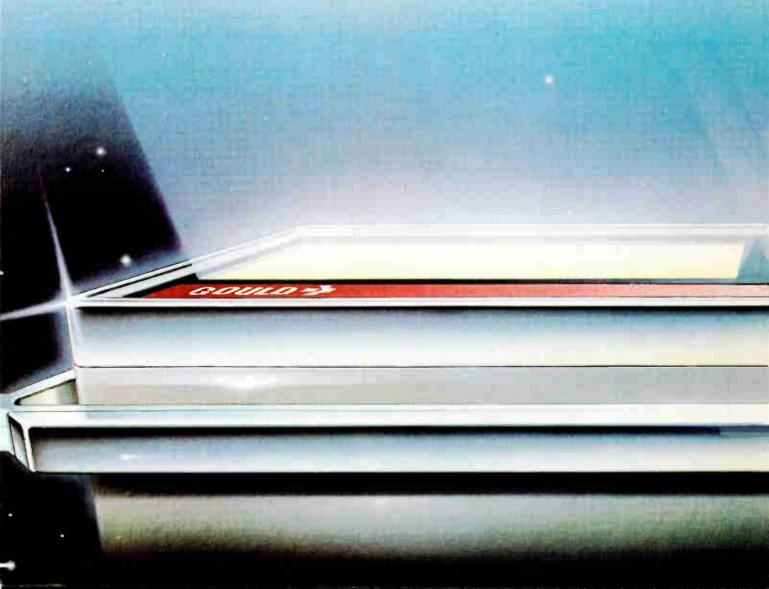
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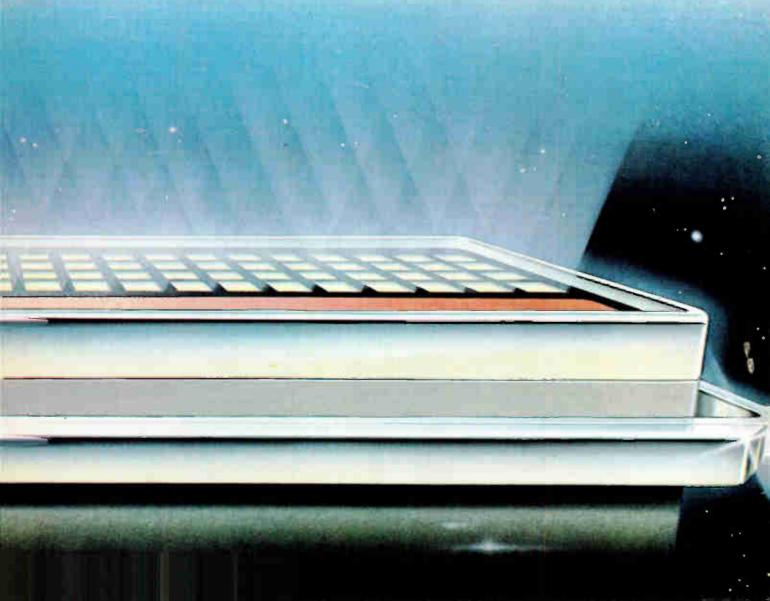
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Solutions at the touch of a button.

A good place to start the counterattack

The drumbeat grows louder: the U. S. is in danger of losing its preeminence as the world's leader in electronic technology and productivity. There is no doubt that there is a growing problem, but thus far solutions have been mostly of the shoot-from-the-hip variety generated by anger and frustration.

However, Leo Young, president of the Institute of Electrical and Electronics Engineers, has broached a plan that could be the first controlled step toward an orderly countereffort. Speaking last month at the IEEE 1980 Conference on U. S. Technological Policy, a meeting subtitled "Global Competition in the 1980s," Young urged a "holistic, long-term approach," starting with a presidential commission empaneled to study the engineering profession as a whole. Such a study would include the supply of engineers, the "quality and scope" of their education, innovation and productivity in industry, the professional needs of engineers, and, perhaps most important, "the possibility of a focal point

Working on America's weaknesses

At the same meeting, Hans M. Mark, secretary of the Air Force, lamented what he called a general retreat in the U.S. during 1945–1970 from the intensive development and application of new technology that characterized the nation from 1860 through World War II. "We had found a way to pass through the gate to a world where the 'quality of life' would be enshrined as the highest good and no entry fee would be required," he says. In the 1960s, Mark adds, the vogue words were "service economy" and "post-industrial society." The inevitable result was a weakening of America's productive ability. Now, it is time to "reindustrialize" the U.S. or become what Prof. Amitai Etzioni of Columbia

for engineering in government — perhaps even a cabinet-level position."

Technology must be recognized as a national priority, says Young, and after that, engineering must receive the kind of special consideration from the Federal government that is accorded medicine, law, science and agriculture. A White House request for an evaluation of engineering and science education, due in July from the Department of Education and the National Science Foundation, is not enough, Young says, for education is only part of the problem. The White House is expected to take no action on Young's program until it receives that evaluation [Electronics, May 8, p. 6].

Young's initiative is an idea whose time has come. He is on target when he says that technology too often has been used as a whipping boy, whereas "greatness will be restored to this country only as engineers transform the findings of scientists into technological solutions."

University characterizes as a "siesta society"—one in which basic productive industry gets short shrift, with the result that nothing works very well.

What must be done? Mark maintains that, to make a conscious national effort at technology development aimed at reindustrialization and modernization of the industrial plant, we first must start with people: make it attractive for young Americans to go into technical and engineering fields. Then, we must lead with our traditional technological strengths—aviation, electronics, synthetics, and so on—while striving to develop new ones where we have serious problems. Young's plan offers a good way.

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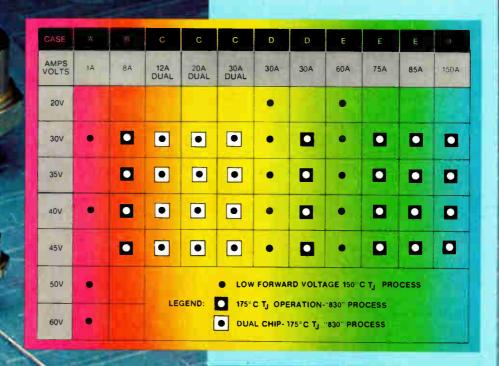
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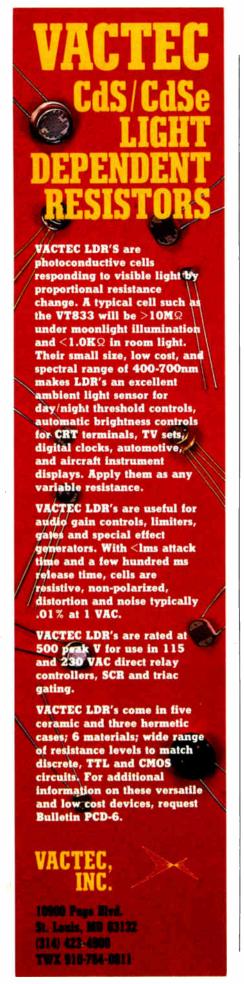


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Meetings

IEEE Computer Conference, NBS and IEEE (Frances Nielsen, B-212 Technology Building, National Bureau of Standards, Washington, D. C. 20234), NBS, Gaithersburg, Md., May 29.

North American Radio Science Meeting and Antenna International Symposium, IEEE et al. (1980 URSI/AP-S Meeting, Department of Electrical Engineering, Laval University, Quebec City, Quebec, Canada G1K 7P4), Laval University, June 2-6.

14th Pulse Power Modulator Symposium, IEEE et al. (Palisades Institute for Research Services, 201 Varick St., New York, N. Y. 10014), Orlando Marriott Inn, Orlando, Fla., June 3-5.

Eradcom Hybrid Microcircuit Symposium, U. S. Army Electronics Research and Development Command (Fort Monmouth, N. J. 07703), Fort Monmouth, June 4-6.

29th Power Sources Conference, U.S. Army Electronics Research and Development Command (Fort Monmouth, N.J. 07703) et al., Deauville Hotel, Atlantic City, N.J., June 9-12.

Automated Testing for Electronics Manufacturing Seminar/Exhibit, Benwill Publishing Corp. (1050 Commonwealth Ave., Boston, Mass. 02215), John B. Hynes Veterans Auditorium, Boston, June 16–18.

Automation for Safety International Symposium, International Federation for Information Processing et al. (ASSOPO '80, Studieadministrasjonen, The Norwegian Institute of Technology, N-7034 Trondheim-NTH, Norway), Norwegian Institute of Technology, Trondheim, Norway, June 16-18.

First Annual Conference of the National Computer Graphics Association Inc. (1129 20th St. N. W., Suite 512, Washington, D. C. 20036), Sheraton National Hotel, Arlington, Va., June 16–19.

1980 Power Electronics Specialists Conference, IEEE, Dunfey Atlanta Hotel, Atlanta, June 16-20.

International Microcomputers Minicomputers Microprocessors/DATA-COMM '80 Conference, Industrial and Scientific Conference Management Inc. (222 W. Adams St., Chicago, Ill. 60606), Palais des Expositions, Geneva, June 17-19.

19th Annual Technical Symposium, Association for Computing Machinery (1133 Avenue of the Americas, New York, N. Y. 10036) and National Bureau of Standards, NBS, Gaithersburg, Md., June 19.

17th Design Automation Conference, IEEE Computer Society et al., Radisson Hotel Downtown, Minneapolis, Minn. June 23-25

38th Annual Device Research Conference, IEEE et al., Cornell University, Ithaca, N. Y., June 23-25.

11th International Quantum Electronics Conference 1980, IEEE et al., Sheraton-Boston Hotel, Boston, June 23-26.

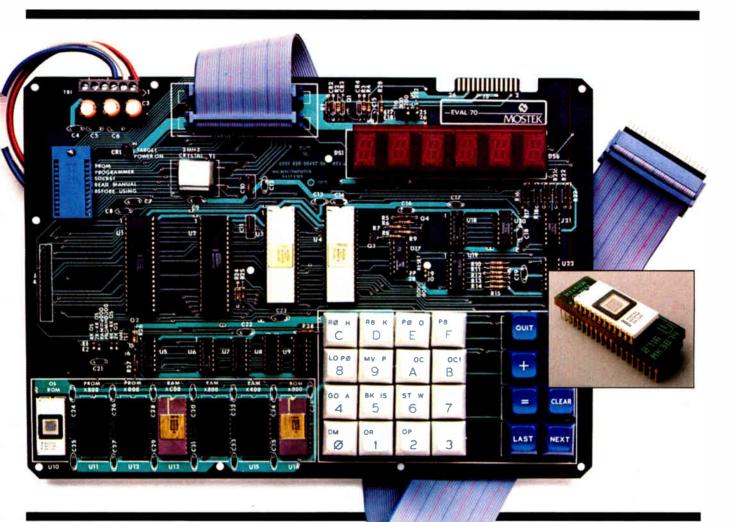
Conference on Precision Electromagnetic Measurements—CPEM 1980, IEEE et al., Stadthalle, Braunschweig, West Germany, June 23-27.

IBI World Conference on Transborder Data Flow Policies, Intergovernmental Bureau for Informatics (P. O. Box 10253, 00144 Rome, Italy), Auditorium della Tecnica, EUR, Rome, June 23-27.

Short courses_

Gordon Research Conferences (Alexander M. Cruickshank, director, University of Rhode Island, Kingston, R. I. 02881), Chemistry and Physics of Microstructure Fabrication, Colby-Sawyer College, S. New London, N. H., June 23–27, and Metal-Insulator-Semiconductor Systems, Tilton School, Tilton, N. H. July 21–25.

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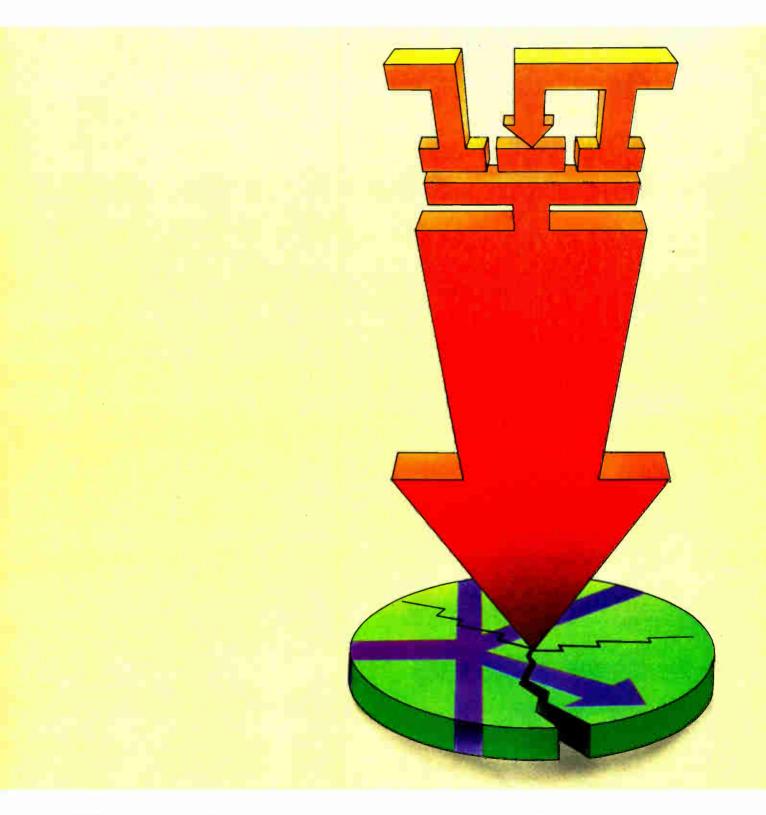
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VQ1000 Specifications

BV _{DDS}	60 volts
I _D (on)	0.3 amps
D (on) pulsed	1.0 amps
R _{DS (on)}	5.5 ohms
t(on) t(off)	10 ns
PD (max. total)	1.2 watts
Input Zener	yes
	ID (on) ID (on) pulsed RDS (on) t(on) t(off) PD (max. total)

Quads make production economy automatic.

Because they are packaged in a standard 14-pin DIP, VMOS Quads can be stuffed onto p.c. boards using automatic insertion equipment. This allows you to substantially reduce handling costs.

VMOS Quads multiply your savings.

When you use Siliconix VMOS Quads in place of bipolars, you can eliminate predrivers and the protective circuitry bipolars require. Your designs become smaller, more economical and space efficient. You use fewer parts so reliability is higher. Moreover, since VMOS Quads are simple one-stage power drivers, they're ideal for boosting the low current output of microprocessors to higher voltages and currents.

Put VMOS Quad economy to work for you.

For more information on VMOS Quads or any of the Siliconix family of VMOS power FETs, dial the Siliconix Hotline: (408) 496-6660. Or just write "VMOS Quads" on one of your business cards and send it to: Siliconix Inc., P.O. Box 4777, Dept. A, Santa Clara, CA 95054.

B Siliconix

VMOS power FETs

in power economy

PMI Creates a Rosy New Variety of Analog Switches

In the Linear Wonderland garden, one coat of BIFET covers a lot of CMOS whitewash



© PMI 1979

In Lewis Carroll's Wonderland, no one was more dreaded than the Queen. She dealt with anyone who crossed her path by ordering their beheading. The gardeners on her croquet court (the Two, Five and Seven from a deck of playing cards) were well aware of the risks.

"Would you tell me please," said Alice, a little timidly, "why you are painting those roses?"

Two began, in a low voice, "The fact is, Miss, this here ought to have been a red rose tree and we

put a white one in by mistake. If the Queen was to find out, we should all have our heads cut off."

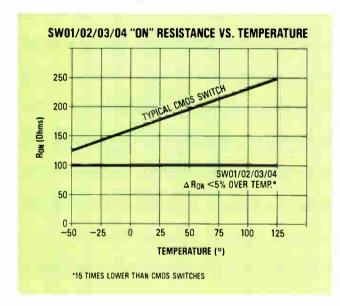
In Linear Wonderland, engineers who pick their analog switches from the CMOS tree are often tempted to yell, "Off with their heads!" just as the Queen did when she found out her red roses weren't really red. What brings out the executioner instinct in every engineer are the thorny problems with "ON" resistance and voltage overload typical of CMOS analog switches.

When PMI decided to get into the analog switch

market, we were determined not to lose our heads. So we looked at the best species of analog switches on the market and decided engineers would find them more attractive if they were grafted with PMI's proven BIFET technology, the same process used in our prized Multiplexer variety of circuits. It wasn't just a cover-up paint job, though; we started at the beginning and created something new: a family of Quad BIFET analog switches that fit the most popular CMOS pinouts but are more rugged electronically than CMOS can ever be.

Consider PMI's SW01/02/03/04. They're Quad BIFET analog switches with temperature-compensated R_{ON} coefficient (0.03%/°C), low R_{ON} vs. voltage (~4%) and a low absolute R_{ON} (100Ω maximum at 25°C). That's better performance than you get from CMOS, or even from the other BIFET switches on the market. In addition, you get low leakage (~0.2nA) and the protection against blowout that is inherent with PMI's BIFET technology.

ATTENTION DG201 USERS!



We didn't stop there, however. We know that most engineers are as forward-thinking as the White Queen in Through the Looking Glass, who told Alice her favorite things are those that happened the week after next. We kept going and developed the 7510/7511 analog switches which were designed to be pin-compatible with the well-known CMOS AD7510/11. These also eliminate the static discharge sensitivity in CMOS devices, improve leakage currents over temperature by two to five times, and there's no need for pull-up resistors to maintain TTL logic thresholds.

All in all, we think we've got the most beautiful Analog Switch Tree anywhere in Linear Wonderland. To prove it, we'd like you to use the coupon for your "BLOOMIN' SWITCH SAMPLE"

You'll find out that those CMOS guys don't have enough paint in their buckets to gloss over the advantages of PMI's Quad BIFET analog switches. The next time they try, you'll know what to say.

"Off with their heads!"

If someone beat you to the coupon, write to us for your sample. Or circle #199 for literature.

SW01	-Normally ON, no disable. (Pin compatible
	to both DG201 and LF11201.)

SW02 -Normally OFF, no disable. (Pin compatible to the LF11202.)

SW03 - Normally ON, with disable.

SW04 -Normally OFF, with disable.

SW7510 - Normally OFF. (Pin compatible with the AD7510.)

SW7511 - Normally ON. (Pin compatible with the AD7511.)



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SAMPLE	" you'd like to have.	

☐ SW01 — Normally ON, no disable.

□ SW02 - Normally OFF, no disable.

☐ SW03 – Normally ON, with disable.

☐ SW04 - Normally OFF, with disable.

☐ LF11202

☐ SW7510 - Normally OFF.

☐ SW7511 - Normally ON.

l am now using: ☐ 0G201

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Mail to: Precision Monolithics, Inc., 1500 Space Park Drive, Santa Clara, CA 95050

or: Precision Monolithics, Inc., c/o Bourns Ag Zugerstrasse 74, 6340 Baar, Switzerland

My name.

Company_

Our production LSI tester won't put the squeeze on your profits.

The cost of testing seems to be skyrocketing. Benchtops look cheap enough until you start adding up their program development and hardware interface costs. And systems designed for both production testing and engineering characterization force you to buy more than you need. So already narrow profits are squeezed even more.

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Sentinel is software-compatible with our Sentry® systems. So you can avoid high program development costs by using your Sentry programs for production testing on Sentinel. Which means you can get on line fast and for less money.

Unlike hardware based bench-



tops, Sentinel's general purpose architecture lets you test a wide variety of devices and technologies. Simple peripheral chips. Complex micro-processors. And just about anything up to 64 pins.

For production throughput, Sentinel is tough to beat. Its production-oriented operating system mini-

mizes test plan execution time. And its dual-level comparators eliminate the need for multiple passes on functional tests.

So relieve your profit squeeze. Look into Sentinel. Low cost hardware. Proven software. And the same worldwide field service team that gives Sentry the highest uptime record in the industry. Call us at (408) 998-0123. Or write Fairchild Test Systems Group, 1725 Technology Drive, San Jose, California 95110.

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Electronics newsletter.

New conversion method ups speed at which DVM reads accurately

Hewlett-Packard Co.'s Loveland (Colo.) Instrument division is set to introduce a new data-acquisition and -control unit that blankets applications from research to steel production. Called the 3497A, it features an optional high-speed digital voltmeter. The meter uses a new multiple-slope conversion technique that combines the speed of successive approximation with the accuracy of dual-slope integration; the new technique will also be used in other HP system DVMs. Adjustable for different integration times, the 3497A's DVM gives 50 readings per second with 5½-digit resolution and 300 with 3½-digit resolution.

Programming aid displays 'keyboards' for each decision

An aid to programmer productivity, in the form of a dedicated cathode-ray-tube terminal system called Proteus, will debut soon. Developed by Solid State Technology Inc. in Woburn, Mass., and the Massachusetts Institute of Technology in Cambridge, Mass., Proteus can generate and show on its screen specialized keyboardlike displays offering only the inputs necessary for each operator decision. **Programmers can design their own keyboards on the screen,** making individual symbols stand for whole subroutines or programs.

Automated tester sets speed mark

Researchers at Lockheed Missile and Space Co.'s Microelectronics Center in Sunnyvale, Calif., have put together an automated system for testing large-scale integrated wafers with signals in the gigahertz range, an order of magnitude above today's commercial systems. Almost the entire system has been built with off-the-shelf instruments.

Executives at Electro see strong 1980 and healthy 1981

A panel of industry chief executives and analysts predicts little important deterioration in electronics industry sales through year-end and sees a fairly healthy 1981—though its members agree that hard forecasting beyond about six months is risky. Such optimism runs counter to the opinions of some analysts who predict a slowdown in the third or fourth quarter of 1980. Meeting at Electro/80 in Boston, the group pointed to a number of positive signs: strong overseas sales and markets opening or expanding in digital communications, cable TV, automotive electronics, and automatic test and military equipment.

Signetics makes ECL move with Fairchild 100-K

Signetics Corp.'s Logic division, which has quietly built a multimillion-dollar business by second-sourcing Motorola Semiconductor's 10,000-gate (10-K) MECL devices, is about to launch a new offensive into the emitter-coupled-logic marketplace. Not only does the Sunnyvale, Calif., division plan to expand its 10-K emitter-coupled-logic offerings significantly, but it will soon make its move into the 100,000-gate (100-K) ECL arena by second-sourcing a majority of 100-K ECL parts offered by Fairchild Camera and Instrument Corp.

Nixdorf buys software firm, unveils computers

Smaller computers with bigger software capabilities will be the key to most user markets in the 1980s, according to Nixdorf Computer Corp. The Burlington, Mass., firm hopes to strengthen its hand in these areas with its acquisition of The Computer Software Co., a Richmond, Va., firm whose billings hit \$5 million in 1979, and with a spate of product introductions

Electronics newsletter.

aimed at personal-computer users and small to medium-sized corporate customers. Meanwhile, the parent firm, Nixdorf Computer AG of Paderborn, West Germany, is making its long-expected entrance into the mainframe business.

Slump causes Motorola to sell car radio lines

The auto and housing sales slumps are cutting into related electronics industries in the Midwest, and the first sell-offs and layoffs have begun. Motorola Inc. has sold most of its line of auto radios geared to the retail aftermarket. The reasons: car sales are sharply lower and an expensive retail inventory buildup stalled on high costs [Electronics, June 7, 1979, p. 48]. The ARA Manufacturing Co., Dallas, bought the operation.

Meanwhile, the precipitous increase in mortgage rates has led to a near halt in new-home sales, and Honeywell Inc.'s Residential Control Center has laid off more than 100 workers in its various lines. Competitor Pittway Corp. says that first-quarter revenues from its line of First Alert smoke detectors and burglar alarms were down 26%, with profits off 52%.

Converter boards offered by TRW for evaluation

TRW Inc.'s LSI Products division in El Segundo, Calif., is making available evaluation boards of its popular monolithic 6-bit 30-MHz flash-type analog-to-digital converter. By redesigning the TDC1007PCB evaluation board for its high-speed 8-bit digital-to-analog converter, the division has produced the TDC1014PCB 6-bit a-d converter evaluation board, which will sell for \$168 in 100-piece prices. The company also says that it could conceivably have a 10-bit 10-MHz a-d flash converter within a year and that the price of 6-bit 15-MHz a-d converters could drop to the \$20 level within three to four years. Meanwhile, TRW's Defense and Space Systems group is building a monolithic bipolar 10-bit 40-MHz a-d converter under a defense contract.

Systron-Donner and English firm offer response analyzer

SE Labs Ltd.'s Instrumentation division of Feltham, Middlesex, England, and Systron-Donner Corp. of Concord, Calif., are bringing to market their first joint product, the model 2450 frequency response analyzer. The under-\$20,000 unit provides virtually noise-free dynamic measurements of a system's transfer function in virtually any environment, performing with a precision approaching that of \$100,000 minicomputer-based systems.

Addenda

Look for Texas Instruments Inc. to announce a version of its TMS 1000 4-bit single-chip microcomputer housing an 8-bit digital-to-analog converter. . . . Beckman Instruments Inc. of Fullerton, Calif., will soon start selling its hybrid 12-bit complementary-MOS digital-to-analog converters through its distributors, the first time hybrid converters will be sold this way. . . . Precision Monolithics Inc. of Santa Clara, Calif., has set up a unit to custom-fabricate IC wafers. . . . TRW Electronics has formed a division called TRW Array Processors in Sunnyvale, Calif., to make high-speed digital array processing systems for commercial markets. . . . Digital Equipment Corp. and Intel Corp. will join Xerox Corp. to develop Xerox's Ethernet internal data-communications system for business offices. DEC will provide transceivers, Intel the interface circuitry, and Xerox the overall network design.

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MMI has grown to become a \$65 million company by consistently designing and delivering state-ofthe-art bipolar LSI products. And now

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Our tradition of excellence began with the industry's first IK PROM in 1971. This was followed by the first 2K, 4K and 8K bipolar PROMs, by the first fast 8x8 multiplier, and then the 15 MHz FIFO. Our latest innovation is PAL'* programmable array logic, the LSI circuit which allows you to program your own logic on a chip.

And we'll continue the tradition, working hard in the future to develop products which are denser, faster and more economical... the products you want!

Delivery that keeps pace with our designs.

MMI has made a commitment to deliver large volumes of bipolar products. We currently ship—and will continue to ship—more bipolar PROMs than anyone else in the world.

Our annual output has tripled during the last twelve months.



MMI was the first to install a 4-inch bipolar wafer fab line. And we will expand that line's capacity by another 80% before the end of 1980. At the same time, we have begun converting

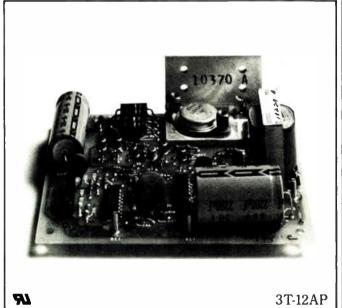
our 3-inch line to 4 inches and will double its output by mid-1981. We have also broken ground on a new assembly facility and expect it to be operational by September of this year. Over the next few years we'll spend 15-20% of every sales dollar on facilities and equipment to assure you volume delivery of MMI's bipolar LSI.

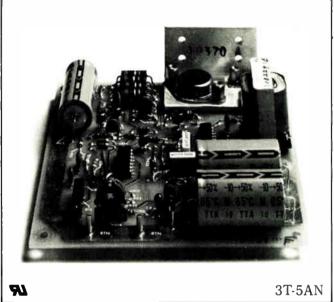
Let us prove it.

Send for a specially prepared report which details MMI's engineering and production capability and outlines our extensive line of digital bipolar LSI products. Please address your requests to Applications Department, Monolithic Memories, Inc., 1165 E. Arques Ave., Sunnyvale, California 94086.



People are switching to Boschert





because only Boschert offers a totally new concept in power regulation: 3T switching regulators.

Boschert 3T switching regulators can completely change the way you think about power regulation. See for yourself by answering true or false:

In a switching power regulator, input-output voltage differentials must be kept low.

False. With Boschert 3Ts, you can start with 10 to 40 volts and get 4.5 to 30 volts out, without a power penalty.

To get negative voltage out, you need negative voltage in.

False. Our 3T-5AN lets you take positive dc in and produce negative dc out.

Regulation is inherently inefficient.

False for 3Ts. They offer 70-90% efficiency over the entire operating range.

The magnitude of output voltage must be lower than the input.

False. Our 3T-5AN lets you set the output magnitude less than, equal to or greater than your input voltage.

	3T-12AP	3T-5AN			
Input Voltage	+10 to +40	+ 10 to + 40 volts			
Output Voltage	+4.5 to +30	-4.5 to -30 volts			
Output Current	0 to 12	0 to 5 amperes			
Efficiency	70.90%	70.90%			
Output voltage and current limits are					

adjustable.

Multiple output voltages require multiple tap transformers.

False. All 3T regulators can be powered from the same dc source.

Designing for a wide line voltage range means wasted power at normal line. False. Efficiency is virtually independent of the transformed line voltage input to 3Ts.

Battery backup of multiple voltages requires multiple batteries or a special UPS design. False. You can backup the input to multiple 3Ts, using one standard battery.

With Boschert 3Ts, you can build better power supplies, build battery backup or singlebattery multiple-voltage systems, even add extra voltages to an existing system without redesigning your supply. You see? Boschert 3Ts have already changed your ideas about power regulation. We've got 3Ts in stock, in volume, so you can put your ideas into practice today. For more information, contact your Boschert representative or write us: Boschert Inc.,

> 384 Santa Trinita Ave., Sunnyvale, CA 94086. Or phone (408) 732-2440.

Significant developments in technology and business

Three-chip mainframe to accompany other Intel processors

by John G. Posa, Solid State, and Richard Comerford, Measurement Editor

Advance announcements herald 32-bit computer on three chips with object-based architecture

Due for unveiling by Intel Corp., perhaps by year-end, is what amounts to a mainframe computer on silicon. The 32-bit three-chip machine joins a raft of new processors and board-level, development-system, and software-support products that the Santa Clara, Calif., company is announcing well in advance.

The announcements are part of a bold marketing scheme aimed at bolstering Intel's position in the high-performance microprocessor race. They reflect the company's vow to develop software-intensive machines [Electronics, Feb. 28, p. 89] to simplify program writing for the complex functions these processors will be called upon to perform.

The three chips that will make up the iAPX 432 silicon mainframe will be an interface processor, a data processor, and a storage module (see figure). Housed in 64-pin quad inline packages, these very large-scale integrated circuits may feature as many as 120,000 transistors per chip and geometries as tiny as 0.5 micrometer.

Architecture. The 432's architectural philosophy, with a computational style markedly different from ordinary microprocessors, was discussed earlier this month at the seventh annual Symposium on Computer Architecture in La Baule, France. "Our structure is based on objects rather than actions—on the 'what'

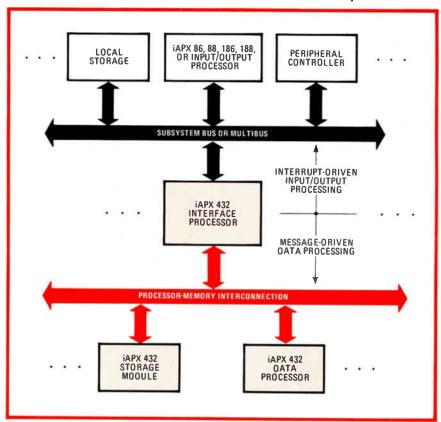
[like an array of data] rather than the 'how' [like move or add operations]," explains Justin R. Rattner, principal engineer for Intel's Special Systems operation in Aloha, Ore.

The approach is somewhat like that of IBM's System/38 [Electronics, March 15, 1979 p. 101]. In effect, the hardware embodies an understanding of the types of operations that can be associated with differing data structures (the objects) and thus relieves programmers of spelling out these operations.

To manipulate these objects, Intel

has given the machine two instruction sets. Both are based on highlevel languages with extensive data structures: one is Pascal, and the other is Pascal-based Ada. The architecture and language combination provides a framework wherein "software design methodology comes along for free," says Rattner.

16-bit arena. By 1981, Intel also will introduce three other new microprocessors: the iAPX 188 and 186 are 16-bit chips and the iAPX 286 has 32-bit attributes. (Also, the 8086 and 8088 microprocessors have



Step up. Intel's three-chip 32-bit microprocessor, the iAPX 432, integrates high-level-language and operating-system functions into a new architecture.

Electronics review

been renamed the iAPX 86 and iAPX 88). Unlike the iAPX 432 chips, these ICs are emerging from Santa Clara—not Aloha—and their instruction sets will be compatible with the iAPX 86's.

The iAPX 286 will offer five times the performance of a standard iAPX 86. Moving into the territory of much larger machines, it will support 10 to 200 tasks in multiprogramming environments and will address a 16-megabyte physical or a 1-gigabyte virtual space through onchip memory-management and protection logic.

Positions. The iAPX 188 will have a multiplexed 8-bit bus to provide an upgrade path for 8085 and iAPX 88 users. The iAPX 186, with its 16-bit interface, is targeted as a higher-performance iAPX 86 replacement.

Like the 432, these three processors take another bite out of software development costs because they will have access to kernel functions for an integrated operating system. These functions, which will first be offered in firmware for connection to a high-speed local bus, will create tasks, send messages, wait for semaphores, and so on.

Hot on the heels of its 8085A-2-based Intellec series II development system and mainframe link [Electronics, April 10, p. 165] comes the unveiling of the speedier 16-bit iAPX 86-based series III, which will support Pascal-86 and Fortran-86, both due later this year. In addition, Intel has opened up plans for a network that will use its present and future development systems in the form of a disk- and file-sharing system, D/FSS, due by year-end.

Network. D/FSS lets several users at different stations gain access to large programs. At the hub of the network is a central node and mass storage facility to which eight stations can be connected.

Any Intel development system—from the model 800 to the series III—may be connected to or disconnected from the network without logically or physically interfering with it. A model 240 or 245 hard-disk unit can be converted to a central node with an upgrade package.

Peripherals

Intelligent office telecommunications switch handles data and voice simultaneously

Bringing the fully integrated automated office a step closer, Exxon affiliate InteCom Inc. is unveiling a combined private-automated-branch-exchange telephone switch and a local data network. Its integrated business exchange, or IBX, will handle voice and data communications simultaneously, and it will perform protocol translation between the often incompatible pieces of automated office equipment.

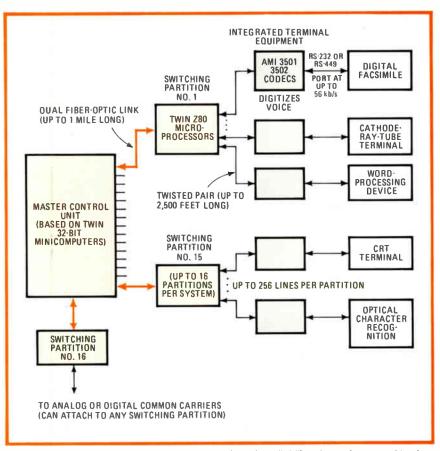
Thus IBX promises to tie together telephones, word-processing units, computers, and facsimile and other office equipment. "We want to be the common intrabuilding channel for all kinds of information," says C. Michael Bowen, president of the

Dallas company. "It gets rid of multiple wiring systems."

It is also another approach to the local network concept [Electronics, May 8, p. 40]. What's more, IBX will link its network with common carriers—analog or digital—for interfacility communications.

Switch. To accomplish this, Inte-Com has built a multiprocessor alldigital switch that performs a combination of functions not available in a single system today, Bowen says. Twin 32-bit minicomputers from Perkin-Elmer's Data Systems group equipped with up to 4 megabytes of main memory each and two 10megabyte disks form its heart.

To this master control unit are



Redundant switching. With redundancy throughout for reliability, the IBX integrated business exchange from Exxon's InteCom simultaneously handles digitized voice and data signals.

connected as many as 16 switching partitions, each of which can handle 256 lines. Each switching partition is built around two Z80 microprocessors from sister affiliate Zilog.

Instead of a conventional analog telephone. InteCom provides what it calls integrated terminal equipment—a tone-dialing phone that includes American Microsystems Inc.'s 3501/2 coder-decoder chips to digitize voice, an RS-232-C or RS-449 port to permit data-terminal attachment, and a controller that multiplexes the two signals onto a twisted-pair wire. The voice becomes a 64-kilobit-per-second signal and the data terminal can simultaneously operate synchronously or asynchronously at rates up to 56 Kb/s, leaving room on the 128-Kb/s line for 8 Kb/s of control signals.

For voice switching, the IBX acts just like a PABX switch, performing intrafacility switching with uniform alternate routing and queueing, calldetail recording, and other sophisticated functions. But its data-switching capabilities set it apart.

Data switch. The master control unit maintains a directory of all the equipment attached to its extensions and their characteristics. For incompatible equipment, IBX uses packet switching techniques and performs protocol and format translation. Bowen will not say what protocols will be handled, however, until first systems are ready for shipping early next year.

The company is the latest of a growing number of firms making electronic office equipment that are financed by Exxon Corp.'s Exxon Enterprises. These companies include facsimile maker Quip System, word-processing company Vydec, electronic typewriter producer Qyx, microprocessor manufacturer Zilog, and a host of others [Electronics, April 27, 1978, p. 88]. However, IBX is not limited to linking the products of the coaffiliate firms.

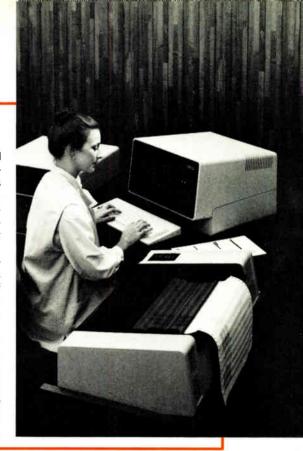
The InteCom offering will face competition from established PABX manufacturers that are adding data-handling capabilities. Rolm Corp. competes with its smaller 500 line Computerized Branch Exchange,

NCR goes desktop

Shrinking the minimum size and price of its I-8100 line of small-business computers, NCR Corp. is unveiling a new entry-level model, the I-8140. The desktop unit integrates the display with the microprocessor-based central processing unit that includes from 64 to 128 kilobytes of main memory. A separate cabinet holds two floppy-disk drives with as much as 4 megabytes of storage, and a 70-line-per minute matrix printer is also available, according to the company.

The unit is programmable in ANSIstandard Cobol or Basic, and optional software lets the unit simulate the popular NCR 299 accounting computer. Prices for the unit start at \$15,255, making it competitive with units like IBM Corp.'s desktop 5100 family.

-Anthony Durniak



and the Business Communications group of Northern Telecom Systems Inc. markets its digital SL-1 that can handle up to several thousand lines. But Bowen is confident that the IBX has a unique combination of features that will make it attractive even at its steep \$500,000 to \$4 million price range.

InteCom will also get a jump on future competition, says Dale Kutnick, director of research at the Boston-based Yankee group. "AT&T is developing a competitive product code-named Antelope, but that's at least two or three years away, and I suspect it will be at least two years before IBM enters this market," he reports.

-Anthony Durniak

Memories

4-Mb bubbles face propagation hurdle

A double-barreled bubble-memory development effort by Rockwell International Corp. aims straight at the major hurdle confronting the next generation of 4-megabit chips: can the familiar chevron-shaped propagation patterns be used, or will

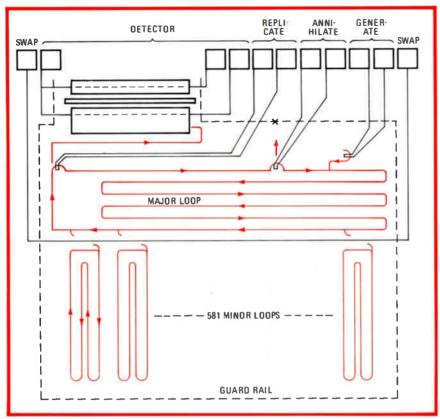
it be necessary to go to the more compact contiguous-disk pattern?

Rockwell's Anaheim, Calif., electronics research center is working on 4-Mb bubble chips using both approaches. It has a complete chevron chip, made with conventional lithographic techniques, and it is well on its way to fashioning a part with an ion-implanted contiguous-disk pattern.

Chevron. The 1.5-by-1.5-centimeter completed chip has bubbles 1 micrometer in diameter, so the gap between the Permalloy chevrons—the minimum lithographic feature—must be between 0.5 and 0.67 μ m. Rockwell is achieving its submicrometer dimensions with contact lithography.

The chevron chip uses a major/minor loop configuration much like those used in 256-K and 1-Mb bubble chips. The 6-by-6-µm minor loops are C-shaped, rather than simple elipses, facilitating the use of swap gates to move the bubbles from the storage minor loops into the sensing major loop. The design represents Rockwell's incorporation of the swap-gate transfer used by other bubble memory makers; the company has been limited to the block-replicate method. To synchronize

Electronics review



Follow the loop. In its 4-megabit bubble-memory design with Permalloy chevron propagation, Rockwell is using a major/minor loop configuration with C-shaped minor loops.

serial operation, the major loop and the minor loops (see figure) hold identical numbers of bits—8,146—says Isoris S. Gergis, principal designer on the project. Operating at 150 kilohertz at room temperature, it has a performance comparable with that of Rockwell's 1-Mb bubble.

Contiguous disk. However, achieving the required fine features by contact lithography may prove to be a stumbling block in production. So Rockwell and other bubble memory makers are looking at contiguous-disk propagation patterns, even though they are laid down by the much trickier ion implantation.

Because the propagation pattern is one contiguous track, there is no need to achieve the extremely fine minimum dimension that forms the gaps between chevrons. Also, the lack of gaps means that densities can be greater.

Rockwell has completed the minor loops of its contiguous-disk memory and is aiming for a 1.3-by-1.2-cm chip with 8- μ m periods (the length

of the basic element in the propagation pattern). The minimum feature size is $2 \mu m$, and the minor loops are G-shaped.

The researchers are working on a two-way switch to move bubbles between major and minor loops, since bubbles can move in either direction in contiguous-disk layouts. They also are devising hairpin loop conductors to stretch the bubbles for sensing.

Others. As with 1-Mb bubbles, the company appears well ahead of its competitors on the development trail. But when it came to 1-Mb production, Rockwell was overtaken by its rivals; in fact the company does not sell a part bigger than 256 K.

Other companies acknowledge Rockwell's head start but say they are coming on strong themselves. "I'm sure everybody is working on one," observes James Cunningham, director of National Semiconductor Corp.'s bubble program. His firm is likely to have 4-Mb engineering samples employing chevron propagation

later this year, but he is not sure "we will tell the world about them."

At Intel Magnetics Inc., first into 1-Mb production, vice president and general manager Richmond P. Clover would advance no timetable for the next generation. But he did say he sees no trouble in scaling the Intel Corp. subsidiary's 1-Mb part to higher densities, with some changes in loop lengths and dimensions.

The probability of a 4-Mb part "is pretty good . . . in a two-to-three-year time frame," observes H. Dean Toombs, the Texas Instruments vice president for bubble operations. He thinks it may work to build the parts with present technology by going to smaller geometries or by using such density improvements as folded loops—and TI is working on such advances.

-Larry Waller

Displays

Atoms add luster to electroluminescence

From a small Finnish research laboratory comes a thin-film deposition technique that promises to improve significantly the luminance of electroluminescent displays. Known as atomic-layer epitaxy, it deposits thin-film materials atom by atom, instead of at the coarser nucleated-structure level.

Attendees at the Society for Information Display's recent international symposium in San Diego, Calif., heard the method described by Tuomo Suntola and his associates at Oy Lohja Ab, an Espoo, Finland, research organization. Their approach immediately attracted the attention of leading researchers.

Brighter. The relatively low luminance of electroluminescent materials has restricted their use to some flat-panel displays, but interest pesists in them because of their inherently low cost. Suntola reports making a display with a luminance of about 1,500 candelas per square meter when driven at about 85 volts root-mean-square and 10 kilohertz. Under roughly comparable drive



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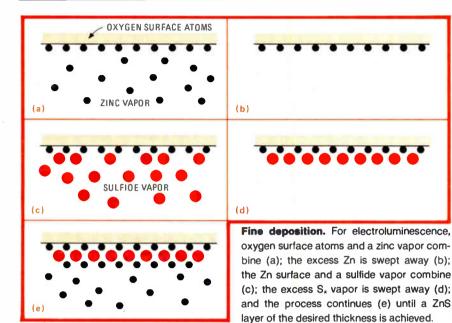
See EEM or GOLD BOOK power supply sections

abbott transistor

Circle 43 on reader service card

MILITARY PRODUCTS DIVISION

Electronics review



conditions, conventional electroluminescent panels give off about 500 candelas/m², so for adequate brightness they must be driven at much higher voltages or frequencies.

The other major problem with electroluminescent materials is susceptibility to voltage breakdown. Suntola expects that atomic layer epitaxy will reduce this sensitivity because it creates a thin film with fewer pinholes.

As with conventional electroluminescent techniques, the objective is to coat a glass substrate with a thin film of material that emits light when subjected to an electric field. The Finnish technique uses a typical material, zinc sulfide doped with manganese, but deposits it in much finer layers, as the figure shows.

A zinc vapor encounters a glass substrate containing an aluminumoxide insulating layer, so that oxygen-zinc chemical bonds are formed (a). The substrate's temperature is kept high enough to prevent any zinc from condensing above this monatomic layer (b).

Then a sulfide vapor is applied and another monatomic layer formed by a zinc-sulfide bond is built up (c). Again, the substrate's heat lets only one layer be formed (d). These steps repeat until the desired ZnS layer is formed, typically 3,000 angstroms thick. Alternatively, the ZnS can be derived from compound vapors laid down in the same manner. For example, zinc-chloride and hydrogen-sulfide vapor layers can be alternated, reacting to produce ZnS.

The secret behind the new process is the deposition equipment, but Suntola refused to release details at the symposium. He did say that, though the equipment is somewhat complex, it works in a low vacuum.

He also said that the equipment for each process step can handle larger substrates than with conventional thin-film deposition. Thus, although total processing time is longer, the throughput is at least as good, he claims.

-Roger Allan

Personal computers

Apple turns pro to aid professionals

Originally conceived as consumer products, microprocessor-based personal computers are positioning themselves as professional tools serving accountants, stockbrokers, very small businesses, and even engineers. It is not surprising then that the industry leaders are adding sophisticated options to their existing machines or unveiling entirely new

models to address these users.

This week's National Computer Conference, for instance, is seeing the unveiling of Apple Computer Inc.'s Apple III, designed around the 2-megahertz 6520A microprocessor, rather than the 1-MHz 6502 in the Apple II. "It is not intended to replace the Apple II, but is the next step in computing power," notes Apple III product marketing manager Don Bryson.

Features. As well as the speed hikes, Apple III also offers 96 kilobytes of random-access memory, with expansion to 128 kilobytes possible, where the Apple II has just 48 kilobytes. The new model adds as standard features a built-in 143-kilobyte mini-floppy-disk drive, a 13-key numeric keypad, and two printer interfaces, and it doubles the display size to 80 characters per line. It can emulate the older unit, however, to preserve the software base.

Along with this hardware, the Cupertino, Calif., company has added a new operating system that handles the memory management for the new larger memory and has file-management capabilities required by the applications' software packages. Also, it is partitioned so that software drivers for the peripherals are separate—a construction that facilitates adding peripherals to the system since the operating system does not have to be changed.

Offerings. Initially, the Apple III will be offered only in two packages. The first is an information analyst package, available in July, that costs \$4,400 without a printer and includes Visicalc III, an updated version of the popular Visicalc II chartbased mathematics and analytical mathematics software package written by Personal Software Inc. of Sunnyvale, Calif.

Visicalc III now features a datainterchange format, which can save the user's data on a diskette and then load it back. "A whole family of programs can operate on the same data," says Daniel Flystra, president of Personal Software.

Apple's second package is a wordprocessing configuration that will include a second floppy disk and





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New pro. The just introduced Apple III is an example of the upscale growth of personal computers into the category of professional tools by the addition of computing power.

either a thermal printer for a \$5,400 system price or a letter-quality printer for \$7,800 total. First deliveries will be in September.

Packages. Apple's competitors are also closing in on the word-processing and information-analysis market. Commodore Business Machines Inc., which in March unveiled a new business-oriented desktop computer, is announcing its Word-pro-IV word-processing package at NCC. It costs \$300 separately and will also come with a 32-kilobyte Pet computer, 250 kilobytes of dual mini-floppy disks, and an impact printer for about \$3,500. Commodore's minimum word processing system costs about \$2,500.

Earlier this year, Tandy Corp., the volume leader, announced its Scripsit word-processing package for the TRS-80 Model I. The user can buy a word processing package with printer for about \$3,300.

Commodore also is announcing a Visicalc package for its Pet computers at NCC. Tandy and Atari will follow suit this quarter.

At stake is a worldwide market estimated by International Data Corp. to be \$1.1 billion and growing at a compound annual rate of 30%—enough to make it reach \$4.35 billion by 1985. The Waltham, Mass., market research firm notes that business and professional users account for by far the largest portion. They already buy 47% of the units sold in the U.S. and will purchase 67% by 1985.—Martin Marshall

Components

New cutting angle keeps crystal calm

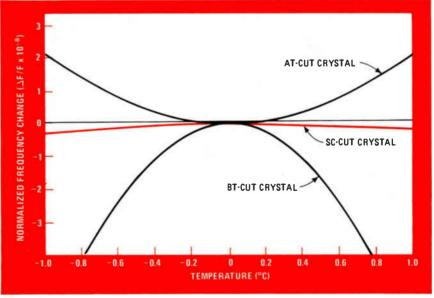
Entering full production at Hewlett-Packard Co. is an oscillator with a doubly rotated, stress-compensated quartz crystal. The new crystal greatly improves the temperature stability and warmup time of such oscillators, which are typically used in test instruments and in communications and navigation gear.

The improved characteristics of the SC-cut crystal come from cutting it at the angle obtained by precisely rotating the master crystal twice, once about its X axis (angle θ) and once about its Z axis (angle ϕ). Single-rotation cuts, such as the familiar AT and BT cuts, are sensitive to small rapid changes in temperature that occur without extremely tight control of oven temperature.

Compensation. These changes set up thermal gradients that stress the crystal, shifting its resonant frequency. Rotating the crystal through a second angle compensates for external stress (hence the SC designation), as well as for rapid temperature changes.

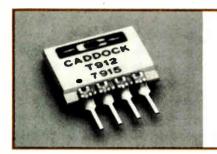
The double rotation means that the cut crystals have a lattice orientation with a zero elastic constant, which internally compensates for any thermal stress. Thus, at 55° ±0.8°C, the frequency shift experienced by SC crystals is less than 1 part in 10°, an improvement of 10 to 40 times over other crystal cuts (see figure).

Development. About half of the four-year development time was spent in defining the crystal orientation and geometry, says Charles Adams, production engineer for HP's crystal products. "The SC crystal's characteristics are approximately 10 to 20 times more sensitive to angular tolerance than the usual AT or BT cut," he explains. "Then too, getting [the final contour] right moves out the spurious response." The Santa Clara, Calif., company cuts the crystal with typical angles of 34° (θ and



Stable crystal. A double rotation before cutting oscillator crystals gives the SC-cut lattice orientation that compensates for thermal stresses, which can affect frequency stability.

Precision Resistance Ratios from Caddock



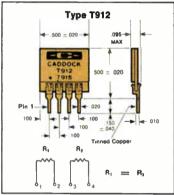
Caddock's Type T912
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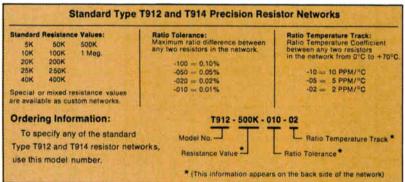
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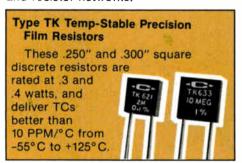
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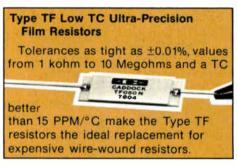
Caddock Electronics, Inc., 3127 Chicago Ave., Riverside, Calif. 92507 Tel: (714) 683-5361

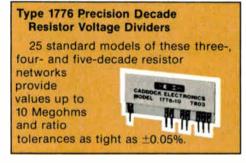


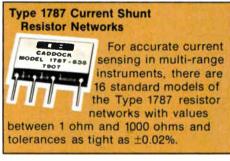
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Electronics review

22° (ϕ), finishing it to a planoconvex contour.

The remainder of the development time went to devising and perfecting special production equipment. HP uses the crystals in its new 10811 plug-in oscillator that can be substituted for the earlier 10544, which employed a single-rotation crystal.

Warmup. In addition to reducing the temperature sensitivity of the new oscillator, the crystal's thermal transient characteristics reduce its warmup time. Whereas the 10544's crystal oscillates about a nominal frequency during warmup and takes about 20 minutes to settle to within specification, the new oscillator approaches the nominal frequency asymptotically, thereby taking only 10 minutes to stabilize in spec.

The improvement in temperature performance is not due to the crystal alone; HP has also redesigned the oven that keeps the crystal at its 55°C operating temperature. The oven's gain—or change in ambient temperature versus change in crystal temperature—has been increased from about 300 to over 1,000 by switching to aluminum from copper for the oven cavity and lid for the former's lower thermal capacitance.

In addition, changes in oven design cut the overall power consumption of the new unit by more than half, from 4.5 to about 2 watts. The earlier unit used a resistive heater controlled by an external transistor in which almost half the consumed power was wasted. In the 10811, two Darlington transistors serve both to heat and control the oven, more than doubling its efficiency, the firm says.

-Richard W. Comerford

Communications

Codec filter chip jumps ahead of pack

As integrated-circuit makers push into telecommunications applications, they are finding new ways to exercise their expertise at putting systems on chip. A case in point is Motorola's new 14413 switched-

News briefs

Shockley receives IEEE award

William Shockley, coinventor of the transistor with John Bardeen and Walter H. Brattain, received the Institute of Electrical and Electronics Engineers medal of honor in a ceremony preceding Electro/80 last week in Boston. Bardeen received the IEEE's medal of honor in 1971. Other 1980 awards included: the Alexander Graham Bell medal to Richard R. Hough, executive vice president of American Telephone and Telegraph Co.; the Edison medal to Robert Adler, director of research for Extel Corp.; the founders' medal to Simon Ramo, vice chairman of the board of TRW Inc.; the Frederik Philips award to William M. Webster, vice president of RCA Laboratories; and the education medal to Aldert van der Ziel, electrical engineering professor at the University of Minnesota.

IBM expands entry-level 4331 mainframe

Neatly filling the gap between its latest entry-level model 4331 and medium-scale 4341 mainframes introduced over a year ago, IBM Corp. has introduced a new group of 4331 machines. Labeled the 4331 model Group 2 by the corporation's White Plains, N. Y., Data Processing group, the new units are technically similar to the 4331 model Group 1 machines [*Electronics*, Feb. 15, 1979, p. 85] but now include an 8-kilobyte cache memory and operate 1.8 to 2.3 times faster. The user pays about double the price of equivalent Group 1 machines—the Group 2 processor with 1 megabyte of memory sells for \$150,000. The Group 2 units are available with as much as 4 megabytes of memory—the previous limit was a single megabyte—with the biggest configuration selling for \$197,000.

Mohawk Data Sciences comes on strong

Bouncing back from financial reverses, Mohawk Data Sciences Corp., Parsippany, N. J., has introduced a communications service in conjunction with Wiltek Corp., Norwalk, Conn. Called WINC, for worldwide integrated communications, the electronic mail service will make use of Mohawk's series 21 family of microprocessor-based data terminals. It will also provide dataentry, distributed-processing, word-processing, and network-management capabilities. Earlier this month, the terminal manufacturer announced the imminent acquisition of Qantel Corp., the Hayward, Calif., small-computer maker for about \$36 million.

TRW, Fujitsu operations merge

TRW Inc.'s retail and financial systems business has been combined with computer offerings of Japan's Fujitsu Ltd. to establish a new joint venture that will market information-processing systems in the U. S. TRW-Fujitsu Co. will be based in Los Angeles. Except for manufacturing facilities, most of TRW's 450-strong communications systems and services division will be transferred to the joint venture, whose president will be TRW's vice chairman, J. S. Webb. Eventually the product lineup is likely to be all Fujitsu, with the same product lines the separate companies offer: retail systems, banking systems, small-business systems (Fujitsu's V-830 line), and general-purpose systems (Fujitsu's M-F mainframes).

Fire-control award goes to Norden

Norden Systems has won a \$97 million five-year contract for production of the U. S. Army's battery computer system. The Norwalk, Conn., subsidiary of United Technologies Corp. is scheduled to manufacture 687 systems for the Army Communications Research and Development Command, Fort Monmouth, N. J. The Army has options to buy some 2,000 systems worth more than \$250 million to Norden. The BCS, built around a military emulation of the Marconi Elliott 1800 computer, provides automated assistance in aiming and firing as many as 12 guns at the field-artillery battery level. It receives target information via a digital wire or radio link from forward observers, automatically computes firing data, and displays firing commands at each howitzer.

NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY.

HIGH QUALITY RAMS NOW AVAILABLE IN ALL SPEED RANGES.



Highly versatile fiber optic interface

Practical Wizardry for tomorrow

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Bubble Memory Optoelectronics Modules

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STARPLEX aids μ P system development.

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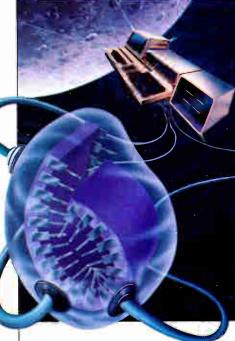
Using the STARPLEX development system with National's 8048 Emulator Package, designers of 8048 Family systems get the kind of sophisticated tool needed for efficient microcomputer development.

And with 8048 ISE (In-System Emulator), they get capabilities that up to now simply haven't been available in this type of instrument.

What is ISE? National's ISE is a separate STARPLEX module housing 32K bytes of real-time map memory, plus all the necessary logic for breakpoints, tracing, and memory mapping. These resources are available for the emulation of several different μ Ps. Because the individual emulator target cards are the only components dedicated to particular processors.

And since ISE doesn't share the STARPLEX BUS, the system doesn't have to compete for memory access with its STARPLEX host.

ROM display and disassembling. The 8048 emulator package provides capabilities which zero in on the problems of designing with single-chip microcomputers. The target card has its own 4K of RAM dedicated to the real-time emulation of the processor's program



ROM. So the designer has complete access to this memory throughout emulation.

He may examine and disassemble existing ROM contents, make changes, and execute the altered code. This gives him considerable flexibility in new

product design, as well as previously masked 8048.

Look into our ISE. National's easily-learned ISE software comes completely integrated into the STARPLEX system, including an "In-File" mode that will implement a predefined sequence of commands. And ISE can also record those results, so you can see exactly how each part of the system operated during the emulation sequence.

ISE's program control capability provides not only the usual breakpoint conditions, but also a "coast" command which allows you to continue executing a program after the breakpoint combination has been satisfied.

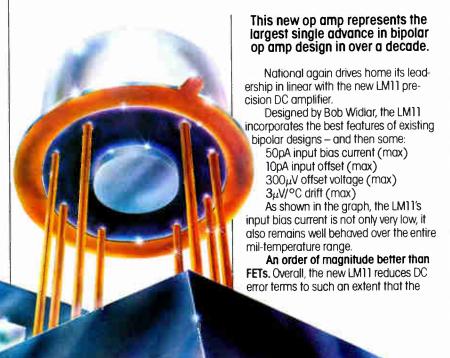
STARPLEX can not only develop and debug software for the 8048 Family, but also for 8080 and Z-80* microprocessors plus BLC/SBC Series 80 boards. NSC800, 8070 and other ISE packages will of course become available as these new processors are introduced.

When you get right down to it, National's STARPLEX with ISE offers features not available in any other development system on the market today. Yet it costs substantially less to own and operate than any system currently being sold.

Practical Wizardry strikes again.

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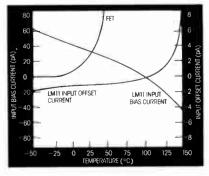
The LM11. A dramatic advance in op amps.



op amp is no longer the limiting factor in many practical designs. Especially over the mil-temp range.

Further, its offset voltage, drift and long-term stability are an order of magnitude better than FETs.

Although internally compensated with provision for offset balance, the new LM11 is pin-compatible with, and quite similar to, the well-known LM108A amplifier.



Leakage current only affects input current of the LM11 above +125°C

National's new BLC-8715 a more intelligent approach to data acquisition.

High-speed intelligent I/O board offloads analog pre-processing functions from the data acquisition system CPU.

National announces a bright new addition to its family of Series 80 Board Level Computers: the BLC-8715 Intelligent Analog Input Board.

The BLC-8715 was specifically designed for industrial data acquisition and process control systems. This new microprocessor-based interface offloads all of the analog data pre-processing functions normally performed by the host CPU.

And in doing so, the CPU may then devote more of its valuable resources to the rest of the control system.

Faster than a speeding digit. Besides freeing up host system resources for more demanding tasks, there are many reasons why the rugged BLC-8715 smooths out process control.

One of the most dramatic is its A/D conversion speed. Based on National's proven BIFET™ technology, the 8-bit BLC-8715 Analog Input Board performs the A-to-D conversion in a scant 8µsec.

Application Note
035 ☐ Additional Series/80

Information



More versatility than ever before.

The BLC-8715 performs "front end" measurement and control functions for 16 analog processes. But that's not all.

It also features 22 digital (TTL-compatible) lines for controlling simple on/off equipment functions, digital readouts, and even manual keyboard override systems.

And to further increase the board's versatility, the Practical Wizards at National designed it so that it may be configured in either of two ways.

By using its standard RS232C interface, the BLC-8715 becomes a remote "slave" to the CPU host.

However, the intelligent I/O board can also interface directly with the host system bus. One of the many benefits of this approach is the BLC-8715's Mailbox memory: 265 bytes of RAM that are directly addressable by any intelligent device on the bus.

It certainly comes as no surprise that National should be the first to take a more intelligent approach to data acquisition and process control.

After all, that's what Practical Wizardry is all about.

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NA 12

LH0082 fiber optic receiver amp lightens the load.



National now in fiber optics with versatile high-speed interface.

National has good news for anyone designing commercial fiber optic applications. Their new LH0082 general purpose receiver amp eliminates the cost and hassle of building your own highspeed amplifier. But there's more. The LH0082 not only expedites development,

it also improves performance while allowing an unprecedented degree of design flexibility.

All you need, all in one. The self-contained LH0082 requires only a single 5V to 12V power supply. So it can act as the interface between all of the most popular photodetectors and any standard logic family or any analog circuit.

The LH0082 transimpedance amp also features a 2GHz gain bandwidth, excellent sensitivity (to 30nW), data rates up to 50Mbps, and high immunity to noise in a fiber optic environment. All hermetically sealed for reliability in a standard 14-pin DIP.

The possibilities are endless.

National's new LH0082 lends itself perfectly to fiber optic communications both guided and broadcast. It can, for example, be used for computer interfaces with peripheral devices, word processing systems, remote graphic terminal data links, and point-of-sale data links.

The LH0082 is also ideal for industrial control devices, robotics, telecommunications on T1, T2, or T3 carriers, as well as airborne and shipboard multiplex communication and control systems.

And to top it off, all of this performance is now available at a surprisingly low cost.

When you come right down to it, it's no surprise that National would be the first to offer a truly versatile necessity to the fiber optic designers. After all, that's what Practical Wizardry is all about.

AF100 active filters-a universal solution to cost problems.

In the past, the easiest and least expensive means of active filtering was with discretes. But this is no longer the case thanks to National's new AF100 universal active filters.

The AF100s are internally adjusted to provide center frequency accuracies of $\pm 2.5\%$ (for the AF100-1CN model) and $\pm 1\%$ (for the AF100-2CN model).

And because of their small size and low external parts count, the AF100 active filters lend themselves perfectly for use in MODEMs and many other telecommunications applications that require lowpass, highpass, or bandpass filter configurations.

But there's more to the price/ performance story than just design versatility and decreased manufacturing costs. The AF100 universal active filters are attractively priced as well.

Just another example of Practical Wizardry cutting your costs to the bone. 2



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William Sanderson, Group Marketing Manager, Custom MOS/LSI.

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Practical Wizardrya means toward new beginnings.

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To answer these questions, consider some of the most outstanding personal examples of practical wizardry – the works of Sir Isaac Newton.

Newton's brilliance came from his uncanny insight into common, everyday phenomena. The swinging of a pendulum. Gravitational attraction. Terrestrial mechanics. The spectral properties of sunliaht.

And when he needed to go further than simple algebra could take him, he opened up a whole new realm of mathematics called calculus – one of the most fundamental beginnings of modern technology.

In fact, if it wasn't for Newton, today's technological renaissance may never have happened.

And when you think about it, today's practical wizards really aren't very different. Although their efforts are more specialized, their contributions to today's society are every bit as useful and significant as Newton's were to his.

At National Semiconductor, practical wizardry is much more than just a catchy phrase – it's our lifes' work. A means toward new beginnings.

By following the examples set by Newton and dozens of other practical wizards of the past, we're finding the most useful and workable solutions for today's needs.



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National's DP8350 Series of single-chip CRT controllers form the heart of over 60 terminal designs worldwide.

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Due in part to their bipolar (I²L) circuitry, the DP8350 Series is widely regarded as the ultimate in CRT display refresh circuits.

Single-chip versatility. The 40-pin DP8350 Series — which includes the DP8350, DP8352 and DP8353 controllers — offers a full range of features using internal mask programmable ROM.

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The versatility inherent in the DP8350 Series cannot be understated. In the character field, for example, both the total number of dots per character field and the number of scan lines per character may be specified (up to a 16 x 16 dot matrix). The number of characters per row (from 5 to 110) and character rows per video frame (from 1 to 64) may be specified as well.

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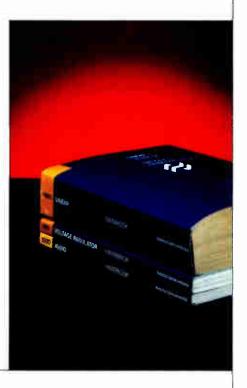
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Patent pending
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Don't miss the important news inside.

Electronics review

capacitor filter IC for coder-decoder chips: it adds an on-board high-pass filter to take care of both 20- and 60-hertz noise rejection.

The Austin, Texas, MOS Integrated Circuits division recently started production on a predecessor chip with two low-pass filters that meet most telephone-industry specifications for codec filters. The problem is that "systems using filters with different architectures [than the new 413] have to take care of the 20 Hz in the system, and that costs money," notes Steve Kelley, engineering manager for telecommunications products.

Others. Motorola is not alone in adding these new filtering functions, although it may be furthest along since it is at the sample stage. Mostek is working on a similar chip, which will also take care of the 20-Hz induced noise from ring signals on other lines and of the 60-Hz line noise. Intel has available a codec filter chip that uses a notch filter for 60-Hz rejection.

The complementary-MOS metalgate 4113 packs other added functions into its 175-by-113-mil area. To boost weak signals, the amps may be used to drive "any kind of a subscriber-line interface circuit, including hybrids," Kelley says.

What's more, the 413 can handle two codec signals at once, making conference calls possible. This feature is available with other codec filter approaches, but at the cost of adding some auxiliary circuitry.

Motorola has a patent on the 413's frequency compensation. Known as the (sine x)/x correction, its version is unusual in that "it does not increase the delay distortion that the filter introduces into the codec signal path," Kelley says.

Less crosstalk. The new filter IC has a typical 80-decibel crosstalk isolation, at least 20 dB better than some existing chips. The next step for Motorola is to integrate the IC with its codec chip, giving a system highly resistant to crosstalk.

"It is just bizarre how some people justify separate transmit and receive codecs because of the crosstalk problem," Kelley says. "Crosstalk should

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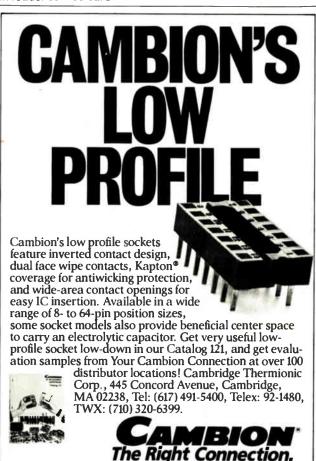
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Electronics review

not be a problem for either codecs or filters."

The chip draws but 25 milliwatts in the active mode. When it is used with the Motorola codec, it automatically powers itself down under the appropriate conditions. "That's the proper system concept—designing parts that work together," Kelley boasts.

The North American standard governing filter specifications does not call for the 20- and 60-Hz rejection. But, as Kelley notes, the problem has to be solved somewhere in the system, and doing it on chip is an elegant solution. -Harvey J. Hindin

Consumer

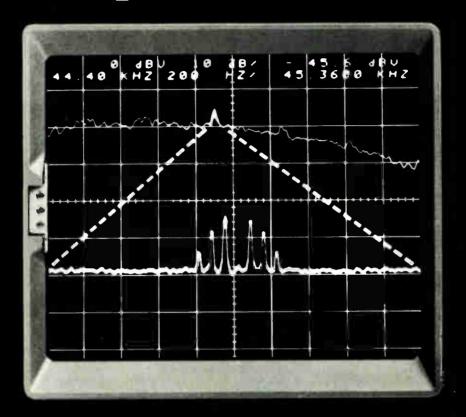
A-m stereo chips getting ready to play

Hard on the heels of the Federal Communications Commission's selection of the Magnavox a-m stereophonic broadcast system, Sprague Electric Co. and Signetics Corp. have disclosed a joint development program for a-m stereo decoder chips. Christened the ULN-3800, the integrated circuit is well into the breadboard stage and should be introduced later this year.

"We may have to go through one or two more design refinements, but essentially we're there," says Oliver L. Richards, design engineer at Sprague's Semiconductor division in Worcester, Mass. Because the design is compatible with both firms' semiconductor processes, it will be available simultaneously from both and will mate with each firm's front-end ICs for a two-chip a-m stereo radio.

Architecture. Though the decoder IC still needs work on its noise-detection and -processing sections, much of the design is firm. It will use a standard peak detector to demodulate the left-plus-right, or monaural, signal and a low-frequency phase-locked loop to acquire the interchannel-difference, or left-minus-right, signal. Algebraic addition of the two signals would take place in a matrix much like that used in pres-

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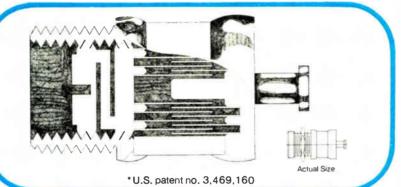
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Electronics review

ent-day fm stereo decoders.

"The design is compatible enough with existing systems that you could almost substitute it for the detector diode in the intermediate-frequency strips of existing a-m radios," says Richards. The ULN-3800 will fit an 18- or 20-pin dual-in-line package and will take up less than 10,000 square mils of silicon.

Pricing plans. "We want samples in the marketplace in the fourth quarter of 1980," says Peter R. Loconto, who is director of product development and marketing for the division. The price should be \$1.50 to \$2 in large quantities, dropping to less than \$1 by 1982 or 1983.

Loconto says the semiconductor division and Signetics, across the continent in Sunnyvale, Calif., began investigating each proposed a-m stereo system several years ago, so when the FCC decision was announced [Electronics, April 24, p. 48], they were ready to move. At stake is what is viewed as a major consumer market, mostly for automobile radios.

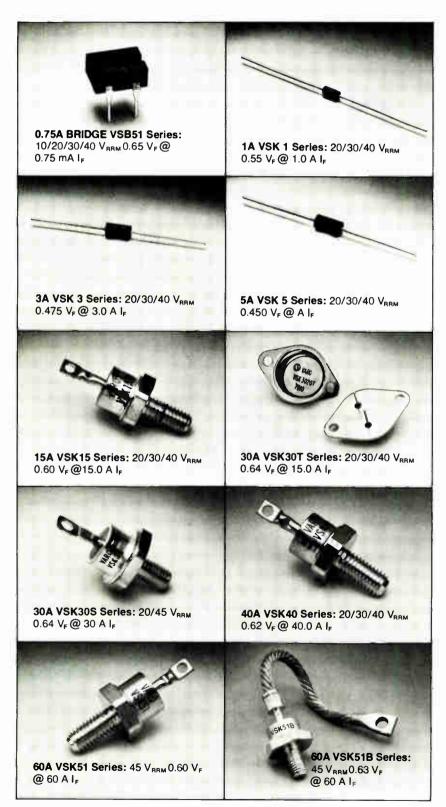
The attraction over fm stereo is expected to lie in the greater long-distance range and tolerance to urban interference inherent in a-m broadcast. "The U. S. soaks up eight million auto radios a year," says Robert F. Milewski, product manager for custom ICs. "By 1985, I expect that 50% to 70% of all auto radios will have a-m stero decoders, and by 1982, up to 90% of [other] fm/a-m radios will include a-m stereo."

Target areas. "The market we see includes the whole U. S., outside the heavily urbanized areas where there is almost a saturation level of fm stations," says marketing director Loconto. "And even in urban areas, a-m stereo's operating advantages should make it a strong competitor to fm."

Fm stereo is prone to interference from image frequencies and multipath; a-m stereo will not be. Also, a-m stereo should offer longer-range reception than fm; a-m stations already reach out 150 miles or more routinely, whereas some fm stations are difficult to receive in suburban locations.

-James B. Brinton

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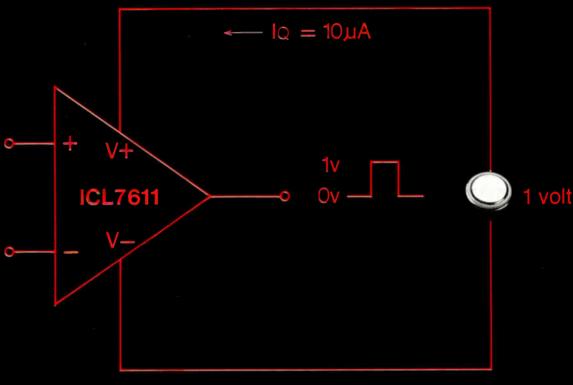


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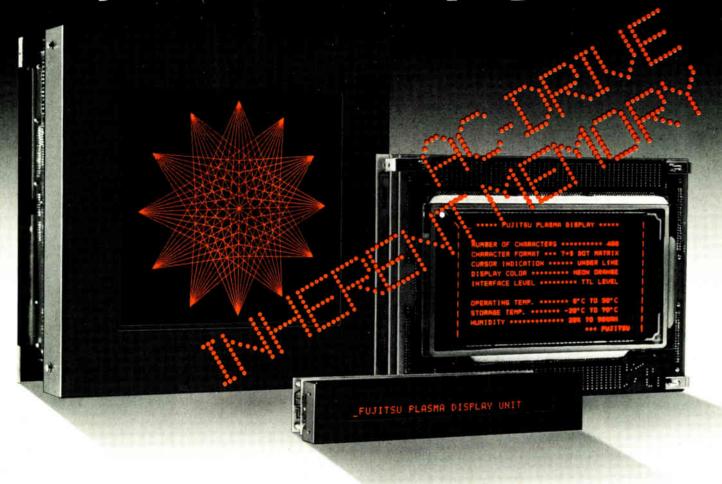
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FPC2004NRCA	80 (20 chars, x 4 rows)	5 x 7 dot matrix	40 50	
FPC3201NRCE	32 (32 chars. x 1 row)		4.0 x 5.6	
FPC3208HRCD	256 (32 chars. x 8 rows) 7 x 9 dot matrix		3.5 x 4.5	
FPC4002NRCD	80 (40 chars. x 2 rows)	5 x 7 dot matrix	3.1 x 4.4	
FPC4012HRCB	480 (40 chars, x 12 rows)		3.5 x 4.5	
FPC8001HRCB	80 (80 chars, x 1 row)		3.15 x 4.5	
FPC8002HRCB	160 (80 chars. x 2 rows)	7 0 4-4		
FPC8006HRCA	480 (80 chars. x 6 rows)	7 x 9 dot matrix		
FPC8012HRCA	960 (80 chars. x 12 rows)		2.8 x 4.5	
FPC8025HRCA	2,000 (80 chars. x 25 rows)			

GRAPHIC UNITS

Character color: neon orange

Model	Effective Display Area		No. of Effec- tive Lines		Dot Pitch
	D (mm)	W (mm)	D	W	1 (11011)
FPG7NRUC	78	78	128	128	0.6
FPG9HRUD	217	217	512	512	0.42
FPG0805NRUA	153	18.6	256	32	0.6

Character color: neon orange



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Washington newsletter_

SBS sees high-speed electronic mail by end of 1981 . . .

Satellite Business Systems expects to have high-speed electronic mail customers operating with its first domestic satellite by the end of 1981 using new AM International Inc. automatic digital copiers able to reproduce 70 pages per minute—more than 100 times faster than conventional facsimile devices. Where conventional fax costs now run to several dollars per page, an SBS official says the AM International prototypes developed for SBS show costs will be "substantially under \$1 a page," depending on a user's volume and if it employs simultaneous transmissions to multiple terminals. The first SBS satellite is to be launched in October, with operations to begin in January 1981.

. . as AM International unveils 70-page/min fax prototypes

The AM International prototypes developed by its Multigraphics division at Mount Prospect, Ill., achieve document resolution of 300 lines per inch, compared to 96 lines for a 6-minute facsimile machine, using a heliumneon laser under computer control for a 2-second page scan. Data is then condensed in the computer—by the elimination of white space between lines, for example—and digitized for transmission at rates up to 448 kb/s, almost 100 times the data-carrying capacity of a telephone line. Laser imaging is used for data reproduction in the system, which is linked to a document generator that electronically prints pages in sequence, and collates and staples them into sets automatically. The number of copies and addresses are specified by the sender, although SBS says each copy will show only the name and address of one recipient. AM International retains rights to manufacture and market the new system since SBS contracted only for prototype development and delivery of two systems.

Threat of changes in VHSIC timetable troubles contractors

Whether the military very high-speed integrated circuits program can maintain its tight timetable, plus the threat that some segments of the effort may be broken off and assigned to a single contractor, concerns some of the nine industry contractors. Timetable watchers are waiting to see if the Department of Defense's program office meets its Sept. 7 deadline for getting a VHSIC Phase One proposal instruction package to interested companies. The contractors are anxious to submit proposals by the end of December, when the ongoing Phase Zero nine-month studies are scheduled to be completed [Electronics, March 27, p. 41]. Contractors will need the proposal instruction package if the program is to stay on schedule with Phase One awards in June 1981. The possibility of breaking off segments of the program such as computer-aided design—instead of letting each competitor mount its own effort as part of a vertically integrated program—is reportedly being reviewed following receipt of a separate proposal from Sandia National Laboratories, Albuquerque, N. M., seeking to lead the CAD aspect of the program.

Carter pressured to extend controls on TV imports . . .

Unless President Carter extends color TV receiver import controls that expire June 30, a U. S. labor-industry coalition predicts, the remaining 65,000 American jobs in the industry will disappear. The group foresees a new invasion of the U. S. market led by South Korea, along with Taiwan and Japan. Carter received a mid-May recommendation from the International Trade Commission to continue import controls on Korea and Taiwan that went into effect last year, but to end the 1977 Orderly Marketing Agreement with Japan, which now has eight color TV manufac-

Washington newsletter.

turing operations in the U. S. The President can accept, reject, or modify the ITC recommendation. Compact—the Committee to Preserve American Color Television, made up of four companies and 11 unions—cites a recent Korean prediction that it expects to boost its color TV exports to the U. S. by 400% to 800,000 sets this year if import controls are lifted. If that occurs, Compact contends, "color TV manufacturing will simply follow all the other [domestic consumer electronics] procedures into the increasingly crowded graveyard of domestic industries."

. . . as court puts a hold on Commerce dumping settlement

Compact and the Electronic Industries Association's tube division got some good news this month when the U. S. Court of Appeals in Washington, D. C., granted their request for an injunction against implementation, by the Department of Commerce and the Customs Service, of the controversial settlement of television dumping claims against Japan [Electronics, May 8, p. 61]. But Compact and the EIA still have a long struggle ahead after winning that first battle in the dumping duty struggle that began in 1968. At issue is the amount of dumping duties that can be assessed against Japan for selling TVs to the U. S. below its home market price—Compact says \$700 million compared to the Commerce Department's estimate of \$128.7 million—and the department's negotiation to settle for about \$75 million, an action the petitioners claim is illegal. The appeals court must now rule on the validity of the claims.

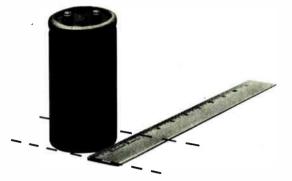
April TV sales show sharp drop as recession deepens

Sharp declines of more than 17% in April sales of both color and monochrome television receivers are convincing Washington economic observers that the domestic recession is likely to be deeper than earlier Federal forecasts. The April drop in total TV sales to less than 835,000 sets is well under the 1 million-plus sold by manufacturers to dealers of a year earlier and 44% below the nearly 1.5 million sets sold in March. The April figures put sales for 1980's first four months at 4.4 million units, down 8.2% from last year—a significant increase from the 5.8% decline posted for the first quarter. The recession has yet to cut into spending for high-priced video cassette recorders, however. The Electronic Industries Association figures show that April VCR sales of 3,400 units were 47% higher than last year, putting volume for the first four months 57% ahead of the 1979 level. Nevertheless, analysts note the growth rate for VCR sales is also slowing.

New hearings urged by Datapoint for 1934 Act rewrite

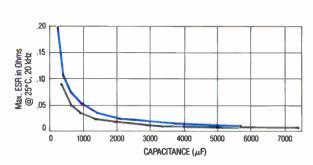
A new call for full public hearings on H. R. 6121—the congressional rewrite of the 1934 Communications Act—has come from Datapoint Corp. of San Antonio, Texas, which believes competitive telecommunications could be threatened by American Telephone & Telegraph Co.'s market dominance resulting from a hastily drafted, compromise bill. H. R. 6121 is still bogged down in the House Commerce subcommittee on communications, and observers doubt whether an acceptable compromise can be passed and coordinated with a Senate version before adjournment for the elections. "The present third-generation bill has never been the subject of hearings," says Datapoint chairman and chief executive Harold O'Kelley in his call on Capitol Hill for hearings on both House and Senate versions. Datapoint manufactures computers, electronic office products, and telephone management systems.

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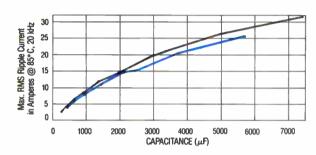
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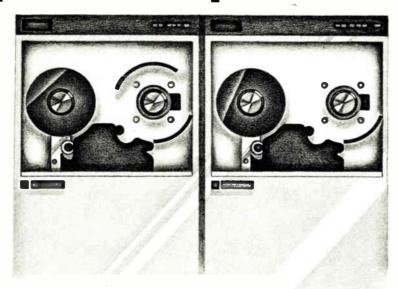
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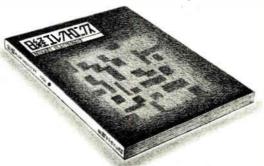
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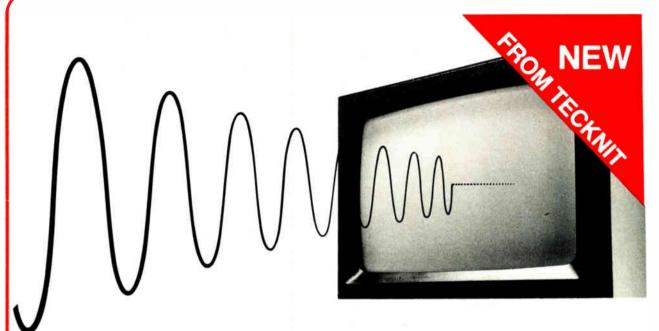
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International newsletter_

Matsushita microprocessor clocks at 13.3 MHz

Three companies in Japan's Osaka-based Matsushita group have announced the development of the fastest 16-bit n-MOS microprocessor yet. To be available in sample quantities next spring, it has a clock frequency of 13.3 MHz. The fastest execution time of any of the device's 100 different instructions—for addition and subtraction and logical operation—is 300 ns. Floating-point multiplication instructions can be executed in 58 ms. Known as the MN 1613, the new processor can address 512 kilobytes of main memory.

West Germans build small green-iight laser

Using a proprietary design, researchers at the Ruhr University in Bochum, West Germany, have developed a helium-selenium green-light laser whose power output is comparable to that of a helium-neon laser but that is considerably smaller. The air-cooled laser, which emits its light at wavelengths between 497 and 530 nm, has an output of 3 mW in multimode operation and 0.8 mW in single-mode operation. Its active length is 10 cm, about one third that of a helium-neon version. The small size and green light should make it a handy device as an adjustment tool and for providing a pilot light in laser surgery. Since green light is three times more perceptible than red light, laser outputs of about 1 mW are clearly discernible even in broad daylight.

Muliard gives viewdata terminal intelligence

With its third-generation viewdata chip set, code-named Lucy, Mullard Ltd., the London-based Philips subsidiary, is transforming the basically dumb viewdata terminal, which links television sets to a remote computer by telephone, into an intelligent terminal system with powerful message-handling capabilities. The system builds from a basic terminal for home applications to one addressing the professional market with interfaces for a full alphanumeric keyboard, data cassette storage, and data transfer between terminals. It incorporates a modem, a universal asynchronous receiver-transmitter, and an autodialer that interfaces via the telephone line with other terminals and with a keyboard. There are also interfaces for a teletext display and for a remote control. The heart of the system is a new custom large-scale integrated interface chip, designated the SAA 5010, that works with an Intel 8048 microcomputer. Mullard is supplying customers with developmental printed-circuit—board systems expandable from one to three boards. A production version would fit on one board.

France wants major increase in domestic ICs

The French government wants French-controlled semiconductor firms to boost their output of integrated circuits enough over the next five years to equal the country's needs by 1985. Last year, production was less than 20%, nearly all of it in bipolar circuits. Jean-Claude Pelissolo, who heads the government's Direction des Industries Electroniques et de l'Informatique, disclosed the goal at an electronics markets strategies conference held in Monte Carlo by London's Financial Times and the UK consultant firm, Mackintosh International Ltd., in early May. Pelissolo estimates that foreign firms will still have half of the French IC market in 1985, meaning the French semiconductor houses will have to export half the chips they turn out.

International newsletter.

Semiconductor moves made by GEC

Britain's General Electric Co. Ltd. is looking at ways of sharpening its semiconductor capability. For starters, it is bringing its microcircuit, hybrid, and power semiconductor activities together into one group with a \$40 million turnover. Future development will be concentrated at a new plant in Lincoln, headquarters for the power semiconductor group. The company is also negotiating with the Canadian company, Mitel Corp., for manufacturing rights to its high-density dielectrically isolated complementary-MOS process. More speculatively, the firm is interested in a stake in Inmos Ltd. and is awaiting a reply from the government's National Enterprise Board. A joint manufacturing operation with Fairchild Camera and Instrument Corp. [Electronics, Aug. 17, 1978, p. 63] is going ahead at the engineering level at least, despite rumors to the contrary, but the long-term intent of both companies—since Schlumberger Ltd.'s acquisition of Fairchild—will not be fully tested till a scheduled board meeting to finalize equipment investment for the jointly owned fabrication unit at Neston, Cheshire.

Cambridge Scientific instruments boosts E-beam unit's speed

One of the first products to benefit from the United Kingdom's joint electron-beam program embracing industry, government, and university research establishments is Cambridge Scientific Instruments Ltd.'s EBMF-6 electron-beam microfabricator. The vector-scanning machine is 10 times faster than its predecessor, thanks to an increase in the writing rate from 1 to 6 MHz and and increase in resolution from 13 to 15 bits. The latter allows the writing-beam diameter to be matched to the size of features within an individual frame that can be set from 0.5 to 3.2 mm on a side. Features down to $\frac{1}{32} \mu m$ have been produced. The writing speed is 6.4×10^6 picture elements per second. That means that a 4-inch wafer could be exposed in two hours using $1-\mu m$ design rules.

Philips' West German microcomputer plant now in full swing

The first European-made 8048 and 8021 single-chip microcomputers are now in full production at NV Philips Gloeilampenfabrieken's plant in Hamburg, West Germany. The new production facility, Philips says, should help alleviate the supply shortages in some areas that have resulted from the enormous worldwide demand for microcomputer products. "The facility will be a welcome additional source for such devices for many users," a company spokesman declares. The Dutch firm's 8048 family is fully interchangeable with that manufactured by Intel Corp. The production of other microcomputers of strictly European design is being planned.

Addenda

Hitachi Ltd. will start volume production of its 16-K electrically erasable programmable read-only memory, the world's first [Electronics, Feb. 15, 1979, p. 39], this fall in Japan and the U.S. Samples of the device, designated HN48016, are now available in the U.S. . . . Nippon Electric Co. has introduced Japan's first office computer with Japaneselanguage input/output that combines data and word processing. The N6300 model 50N will sell for about \$35,600, and deliveries will start in October. On another front, NEC has opened a 37,000-ft² plant in Ireland's County Meath to increase its production of integrated circuits for the European market. Sales of the company's Irish operations rose from about \$5 million in 1978 to more than \$11 million in 1979, with another doubling expected for 1980.

Inc. and ternational effort in semiconductor products.

X2201 FABRICATION FACILITIES

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(continued on next page)

Aicor announces a breakthrough

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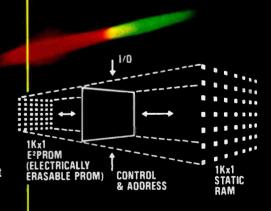
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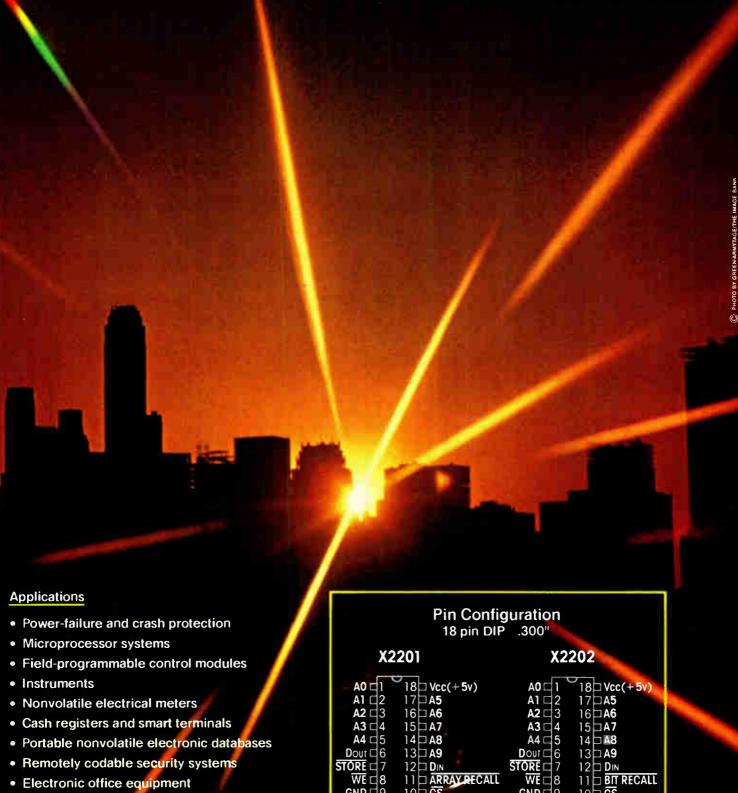
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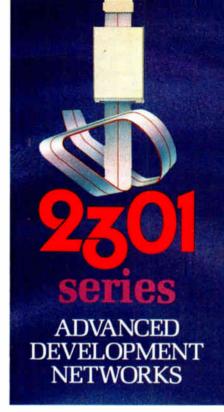
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THE LIGHTS FANTASTIC



Electret microphone's output is quiet and highly linear

by Kevin Smith, London bureau manager

One of three types to be evaluated by the BPO, it performs better than carbon-granule microphones

A thin electrically polarized plastic membrane vibrating in sympathy with the speaker's voice will soon replace the carbon-granule microphone in large-scale trials by the British Post Office. The new electret microphone is one of three technologies—the others are piezoelectric film and moving coil—to be evaluated in a first bulk purchase of high-quality linear microphones.

The speech quality of the electret microphone is far superior to that of the carbon-granule microphone, but it does need an amplifier, and this pushes the cost to \$6 for initial pilot production versus \$1 for its predecessor. In compensation, BPO researchers argue, the electret microphone's inherent reliability will cut service calls, lowering overall costs. Further out, future telephone generations performing many other functions and containing several integrated circuits could incorporate the amplifier as part of an existing chip at little or no extra cost.

Committed. The post office has now made a commitment in principle to high-speech-quality linear microphone designs. As one part of a \$110 million program to replace existing phones with more modern versions, it has placed a first, 150,000-piece order with five suppliers for telephones incorporating a variety of linear electronic amplifier designs. The bulk of these purchases

is for electret microphones to be supplied by A. P. Bessons Ltd., GEC Telecommunications Ltd., Pye-TMC Ltd., and Standard Telephones & Cables Ltd. Plessey Telecommunications Ltd. and STC are also supplying piezoelectric-film versions.

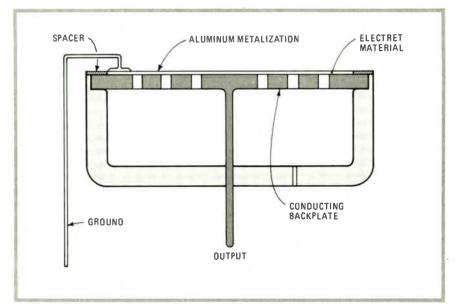
Electrets—a term coined by Oliver Heaviside to describe materials that permanently retain an electric charge—can now be made using polymer films such as fluorinated ethylene polymer Teflon aluminized on one surface and only 13 micrometers thick. A charge of up to 100 volts is imparted to the membrane during manufacture by one of four basic techniques—electron-beam, corona-discharge, thermocharging, or knife-edge.

Diaphragm. In a design originating at the BPO's Martlesham, Ipswich, research center, a metalized

film diaphragm is placed 70 μ m in front of a conducting back plate. It closely resembles a capacitive microphone in action but without the need for a polarizing voltage. Flexure of the diaphragm changes the microphone's capacitance and with it the charge-induced voltage. A back volume of air is also included to provide compliance, against which the diaphragm acts under the influence of a sound wave.

The resulting microphone structure provides a highly linear low-noise output. This performance is reliable, predictable, and stable with age, and the output is unvarying with line length. In all respects except cost, it is thus superior to the carbon-granule microphone.

Because of the electret microphone's low output, some 20 decibels below that of a typical carbon-gran-



On trial. The electret microphone above, one of three high-quality linear types the BPO is to evaluate, uses a metalized film diaphragm and acts much like a capacitive microphone.

Electronics international

ule microphone, a compensating amplifier with a high input impedance (10 megohms) must be provided. It is most readily achieved using a field-effect transistor in a hybrid configuration and could eventually be integrated. But for stand-alone applications, the research center has commissioned Ferranti Semiconductors Ltd. to develop a one-chip solution using its high-density collector-diffused-isolation, or CDI, process.

Integrated amplifier. The circuit, to be evaluated in the Besson transducer, incorporates a high-impedance Darlington front end together with a high-dissipation bridge used to rectify the supply. Designated the ZN470, the 72-by-75-mil chip is housed in a 14-pin dual in-line plastic package. To enable it to handle up to 2 watts at line currents of up to 100 milliamperes (or 200 ma for a 20-second overload), Ferranti uses a copper-alloy lead frame with the unused pins; shorted together. The amplifier's operating temperature

range is from -20° to $+80^{\circ}$ C.

Since electrets have an extremely high impedance, the amplifier has to match into it. To achieve this in bipolar technology, Ferranti engineers adopted a Darlington input configuration with its input impedance determined off chip by high-impedance biasing resistors. As a result, the chip can handle the electret's input current of 2 to 5 natio-amperes, providing a 20-dB current gain. Thus the resulting output is comparable to that of the carbon-granule microphone, for which it is a drop-in replacement.

But whereas the carbon-granule microphone's output varies with line length and hence current, the output voltage variation of Ferranti's chip is less than 1 dB for line currents of from 10 to 100 mA. In fact, the amplifier will operate down to a line current of 1 mA. Further, to match the chip to the transducer, the gain can be set during manufacture from 20 to 26 dB in 2-dB steps.

West Germany

Focusing system emulates human eye to yield clear, high-contrast pictures

A research team at the Technical University of Berlin has developed a system that focuses a video camera or other photographic device fully automatically. Called Biofocus, it allows clear, high-contrast pictures to be made that compare in quality with those taken by a professional photographer with a manually focused video camera.

The result of a five-year development effort by Ingo Rechenberg, Hans-Eberhard Koralewski, and Peter Bienert of the university's Institute for Measuring and Control Engineering, the new system is based on a phenomenon encountered in real life: the focusing mechanism of the human eye. Hence the name "Biofocus."

According to the researchers, who consider their system a milestone in photographic techniques, many others around the world are also work-

ing on self-focusing, but their efforts have thus far led to systems that provide only inadequate pictures. The reason, the team believes, is that others are approaching the problem from the wrong end. They all try to perfect highly precise distance-measuring devices based on either ultrasound or triangulation techniques and use the measured results as criteria for controlling the camera lens. The upshot: generally sharp objects in the near field, but poorly focused objects further away.

Instead, Koralewski says, "we set out to emulate the eye." He explains that, to focus, the eye evaluates contrast levels. In this process, the eye muscles are always in motion, shaping the eye's lens such that the sharpest light-dark contrast, and thus an image of the highest possible sharpness, is projected onto the retina.

At the retina, nerve cells collect

and sort the light information and convert it into electrical pulses. The latter are sent to the vision center in the brain. If the nerve cells transmit pulses denoting a poor-contrast, unsharp image, the brain tells the muscles to adjust the eye's lens for greater sharpness.

That, in principle, is what the Biofocus system does electronically. But of course the system is a far less sophisticated device than the human eye with its millions of nerve cells.

Implementation. In implementing their scheme, the team uses the photoconductive layer on the camera's vidicon tube to represent the eye's nerve cells. Taking the place of the eye muscles is an electric motor that continually adjusts the camera lens for optimum sharpness in accordance with the vidicon output.

The vidicon output, which consists of a stream of signals each representing the brightness of a picture dot, is evaluated signal by signal. Three signals are handled at a time. The first one is delayed by a certain period, typically 200 nanoseconds, the second one by half that time, and the third is undelayed, so that the three signals are simultaneous.

Next, half of the first and third signals is subtracted from the second signal, so that the result represents a brightness-difference signal of a certain level. The delay and subtraction process, taking place behind the vidicon tube, is a continuous one, with the last two signals of one three-signal combination constituting the first two signals of the succeeding combination.

In this manner, the brightness-difference signals for a whole "measuring window"—that is, the marked-off portion of the camera field in which the object to be photographed lies—are obtained. The difference signals are subsequently summed and integrated and the resulting difference signal represents the degree of image sharpness. Maximum sharpness is obtained when the lens is adjusted to its optimum position. As an aid, the degree of sharpness can be read off a meter calibrated in volts.

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summing and integrating circuits are fed to the camera-control unit, where they are temporarily stored in a sample-and-hold circuit. A comparator then compares each incoming signal with the previously stored one, determining whether the new value is bigger or smaller than the previous one. Depending on the result of this comparison, the motor is signaled to turn the camera lens in either the same or the opposite direction. If the new value is bigger than the old, the direction changes. Thus, the position of the lens is continually changed in search of the optimum sharpness of the image.

Koralewski sees a host of applications for the Biofocus system. Besides in video cameras, it could be used in slide projectors; there, an array of photocells would sense the brightness and sharpness level of the projected slide. The Berlin team has, in fact, already built an experimental model of a Biofocus-based slide projector. Other applications are in movie cameras, electron microscopes, and night-vision cameras. In amateur-type still cameras, however, the system will not be used soon because of its initial high cost.

Both industry and the military, Koralewski says, are already showing much interest. Negotiations with some firms wanting to commercially exploit the system are already under way.

-John Gosch

350 W or so necessary for the French satellite. Jean Boulange, export manager for microwave tubes and devices, says that the company's engineers think TWTs with a 400-W output could be designed. But he points out that it would be difficult at that power to get the reliability that is a must for space applications, where tubes must last for seven years or more.

Actually, the 3619 is the high-power version of a line of TWTs for TV satellites that Thomson started developing some four years ago. The amplifying technique is conventional—a microwave signal traveling along a helix interacts with an electron beam. Traveling-wave amplification can also be achieved using coupled cavities instead of a helix, but this makes for a much heavier tube. The 3619 weighs in at just over 3 kilograms; a coupled-cavity tube with the same output power would weigh 7 to 8 kg, says Boulange.

Although the amplification scheme is conventional, Thomson has its particular technology for building TWTs. For one thing, it brazes the copper helix to its beryllium oxide supports and the supports to the copper envelope of the tube as well. This structure boosts the thermal transfer to the outside by a factor of 10 or more compared with a mechanically fixed helix, Agniel maintains, adding that no other tube maker has mastered the Cu-BeO brazing technique. And, he insists. this will be the first time direct thermal radiation will be used in a satellite tube.

Impregnated. For another, the tube's collector, with electrodes of pyrolytic graphite, radiates directly into space, so that heat levels inside a satellite will remain reasonable even at high power. Like other tube makers, Thomson uses porous tungsten cathodes impregnated with calcium and barium aluminates; they have longer life than cathodes coated simply with oxides.

Despite its many merits, a single 3619 cannot provide the power needed for good reception all over France. Therefore the company, which is responsible for the electron-

France

Thomson-CSF going after market for broadcast-satellite TWTs

Like death and taxes, more television seems inevitable, and with terrestrial channel allocations already hard to come by, countries from Australia to Zaïre expect they will one day beam TV programs into their territories from geostationary satellites. That points to a solid market on the way for space-qualified broadcast tubes, and Thomson-CSF, the leading French firm in space electronics, has positioned itself for a solid share.

Flight models. Roger Agniel, marketing manager for Thomson's Electron Tube division, headquartered in the Paris suburb of Boulogne-Billancourt, says the company's effort to develop high-power traveling-wave tubes for TV broadcast satellites involves an outlay of about \$12 million. The firm already has a return in sight: it is producing 30 flight models of a 230-watt version of the tube, a dozen of which will power the preoperational satellite that France plans to launch early in 1984 as part of the Franco-West German directbroadcast satellite project [Electronics, Dec. 6, 1979, p. 66]. The order for the tubes, which operate in the 12-gigahertz region, is expected toward the end of this year.

Agniel is convinced this first batch will be just the beginning. Although AEG-Telefunken has a TWT in the works that will power the preoperational satellite that the West Germans have scheduled for a late 1983 launching, French tubes could possibly get the pick for follow-on satellites as the four main contractors— AEG-Telefunken and Messerschmitt-Bölkow-Blohm GmbH of West Germany and Société Nationale Industrielle Aérospatiale (SNIAS) and Thomson for France—apportion the procurement to get the near 50-50 balance the two governments have agreed on. Above all, Thomson is counting on the upcoming world market for TV broadcast satellites to make its investment a profitable one.

The tube that the firm is readying for this market is the TH 3619. It was first breadboarded last summer, and the engineering model should be ready by the end of the year, Agniel says. Despite its power rating of 200 to 230 w at 11.7 to 12.5 GHz, the tube all by itself cannot power a satellite-TV channel, so Thomson has worked out a way to operate two 3619s in parallel and thus get the



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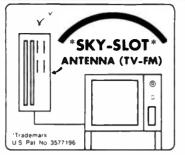
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ics package, will operate them in parallel to get the necessary 350 W per channel. TWTs have been paralleled before for satellite operation, but at much lower power and frequency levels.

The idea is to group the tubes by threes and run two of them at a time. To do this, the input signal is split into three approximately equal signals, each of which drives a TWT amplifier. Associated with the amplifiers are three remote-control switches. One selects single-tube or double-tube operation (a single tube will work for degraded reception), and the other two select the operat-

When two are working, the output signals are recombined by a hybrid coupler. The phase difference between the outputs of these TWTs usu-

ally runs no more than 30°, and the power loss is therefore not crucial. If closer matching is desired, it can be had by attenuating the input signals or by adjusting the helix operating voltages of the tube.

Twos and threes. For the preoperational satellite, Thomson now plans to use two groups of three tubes and three groups of two in parallel for a total of 12. Although the satellite will have only three broadcast channels, this setup will make it possible to try out a five-input multiplexer for the antenna.

The company says that the change was made to make the French and West German satellites more like each other. Thomson switched to a five-input multiplexer because the operational satellites will have five -Arthur Erikson channels.

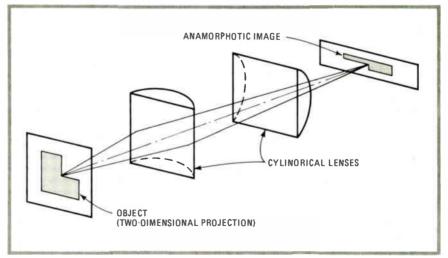
West Germany

Optoelectronic sensor makes images quasi-one-dimensional for fast processing

With automated production processes in mind, engineers at Siemens AG in Munich have perfected a fast, low-cost optoelectronic sensor that reduces a normal two-dimensional image of an object to a quasi-onedimensional image. This considerably reduces the amount of data that pattern evaluation circuits must sub-

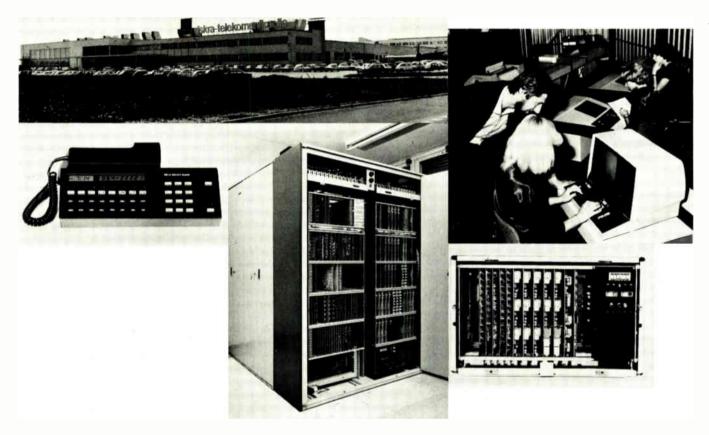
sequently cope with, thus allowing more patterns to be handled in a given time.

Called Optomat and developed by Norbert Roth and his associates, the sensor could be part of an industrial robot for recognizing the shapes of workpieces or part of a sorting system. In the latter application, the



Done with lenses. Optomat sensor converts two-dimensional image into quasi-onedimensional, or anamorphotic, one detected by just one row of photodiodes.

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Things are getting tougher all over.

Electronics international

device could be programmed to respond only to certain object patterns moving past it and to disregard all other shapes.

Lenses. The key to the sensor's operation, Roth explains, is a lens system consisting essentially of two half-cylinder lenses (see figure). From a normal two-dimensional image of an object, the lenses produce a laterally stretched and vertically highly compressed version, called quasi-one-dimensional, or anamorphotic. Because of the narrowness of that image, it can be projected onto just one row of photodiodes.

The Optomat uses 128 such diodes in a row. Their output is a video signal proportional to the brightness levels of the original object. An evaluation circuit external to the sensor digitizes the signal and compares it with the previously stored data of a reference image. A Siemens SKC85 microcomputer, which is built around an 8085 microprocessor, checks whether or not the signal and the reference image agree. In this way, the sensor detects the patterns of the workpieces that it is programmed to recognize.

Less data, more speed. Since only one row of photodiodes is used, the data to be handled is much less than would be involved if a two-dimensional image were projected onto a two-dimensional diode array. The number of patterns that can be compared in a given time is therefore high: up to 7,000 per second. This speed allows workpieces to be moved quickly past the sensor.

With the present sensor, image fields between 2 by 2.8 millimeters (79 by 110 mils) and 50 by 70 mm (2 by 2.8 inches) in size can be obtained. The workpieces need not move through the image field at a constant rate, so that they may be moved past the sensor along a transport system or down a slide.

The Optomat sensor could also be used to automatically detect flaws—in textiles, for example—to check the position of parts during automated assembly, to read characters and symbols, or to select electronic components according to their size and shape.

-J. G.

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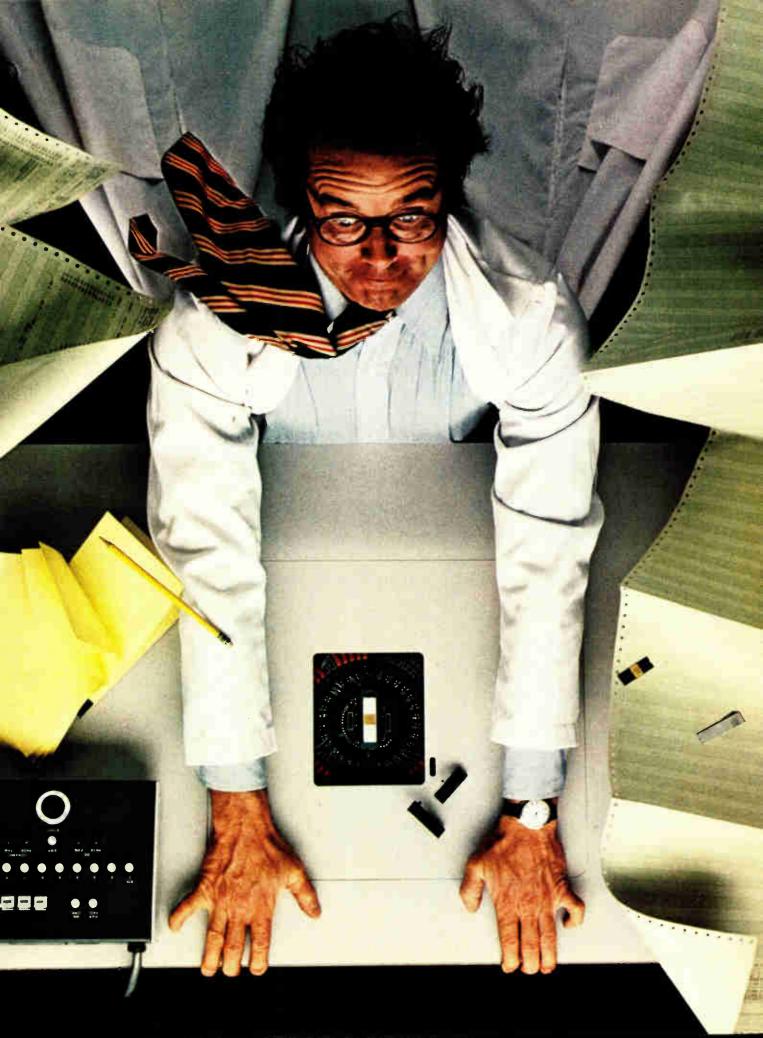
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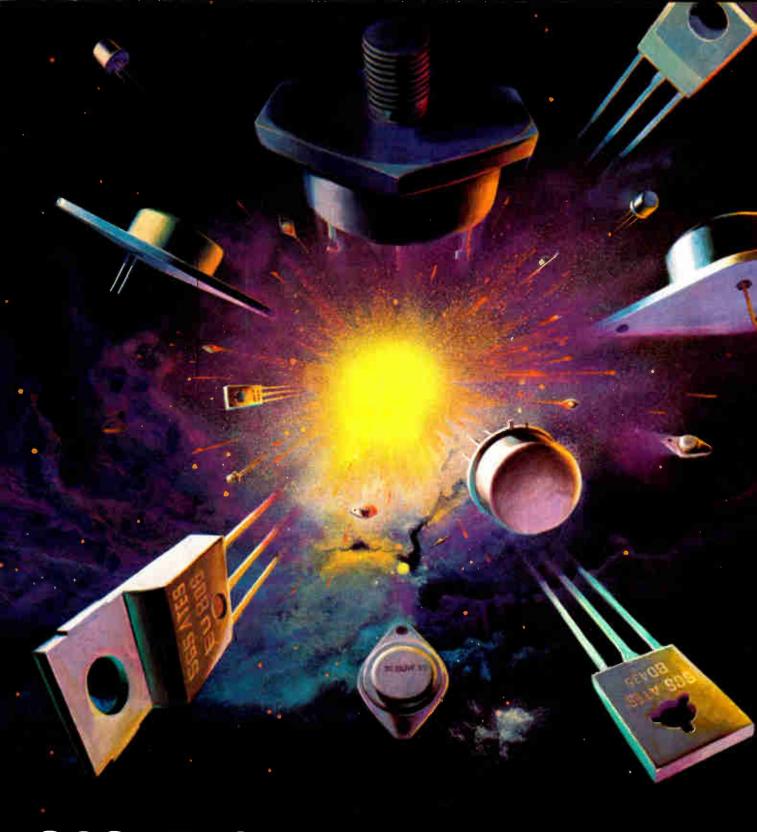
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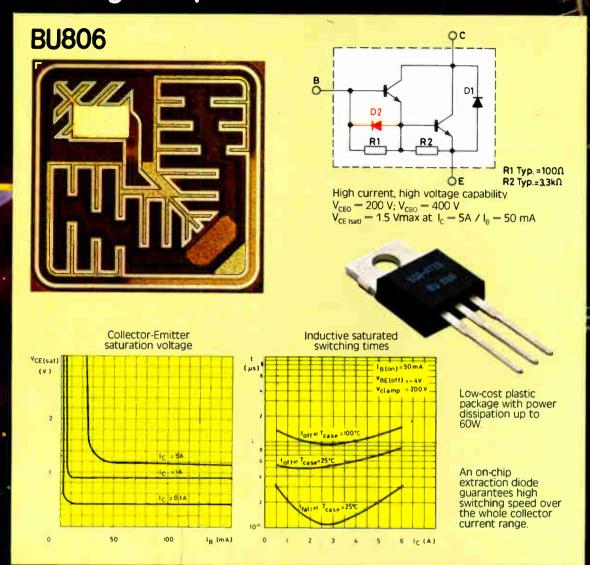
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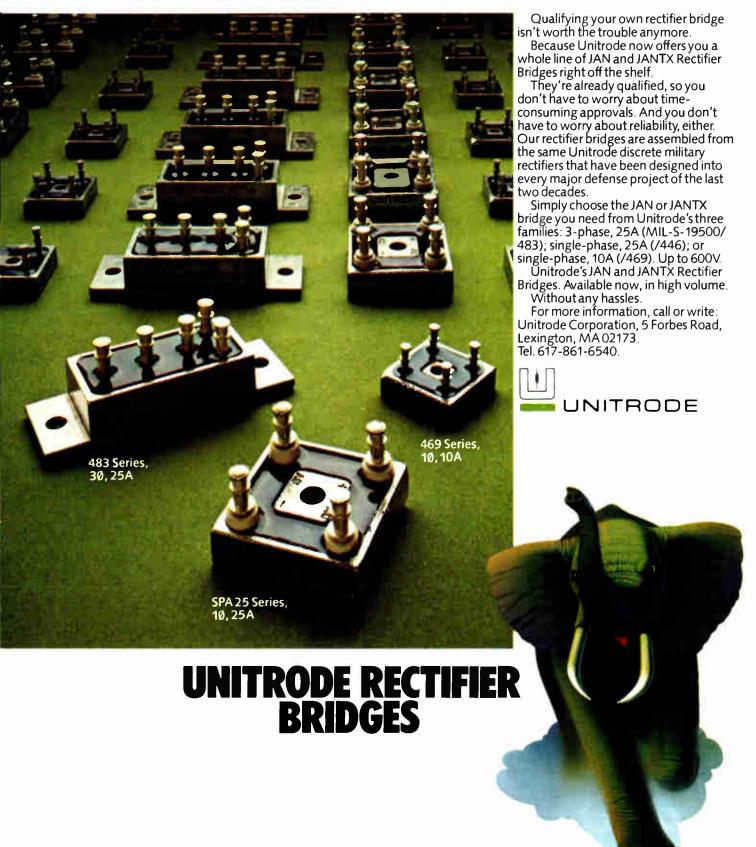
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Speech I/O is making itself heard

Popularized in recent consumer and commercial products, voice synthesis and recognition are set for a boom

by Bruce LeBoss, San Francisco regional bureau manager

Up to now, anyone listening to or talking to an automobile or a calculator, a microwave range or a television, might have been a candidate for the psychiatrist's couch. But thanks largely to advances in solid-state and computer-software technologies, such behavior seems destined to become commonplace as speech synthesis and voice recognition are perfected and applied in a wide variety of products.

Unquestionably, the latest developments in computer-controlled voice input/output devices herald a new era, when the chatter of hardware will be heard across the land.

Several suppliers and users of I/O devices, subsystems, and systems have embarked on a wide range of applications developments that use speech synthesis or recognition technologies and even a combination of the two. Although a number of voice

I/O products have surfaced over the last decade or so, most have been quite cumbersome, extremely costly, and of relatively poor performance.

New patterns. However, with the rapid advances of late in large-scale integrated circuits—both analog and digital—and in developing signalprocessing and pattern-recognition algorithms, it is now realistic to expect a rapid escalation in the development of speech devices, boards, and modules. These are likely to find their way into a large number of consumer, industrial, and commercial systems, ranging from talking games and appliances to automobile dashboards that deliver warning messages; from voiceactuated patient-support systems to computers, terminals, and dictation machines that recognize speech and respond to the voice input.

Interestingly, the total U.S. mar-

ket for speech I/O equipment in 1978, according to a recent report by SRI International, Menlo Park, Calif., was estimated to have been less than \$20 million. However, high equipment prices and technological constraints that have limited growth are being overcome, SRI points out.

Rapid growth. Today, not only have a number of companies made a strong commitment to the voice I/O

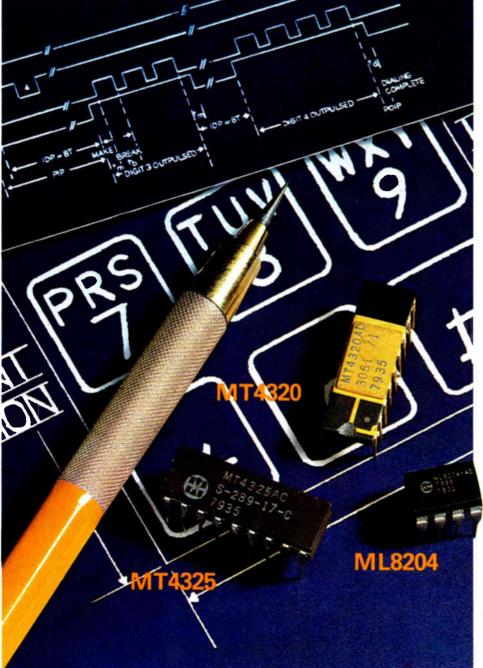


Chatterboxes. Soon homes will be filled with the voices of TV sets such as Toshiba's prototype (below, left), calculators such as Sharp's desktop CS-6500 (below, right), and microwave ovens such as Quasar's (right) dispensing information to the consumer.





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Inside the news

equipment field, but further, as SRI adds, economic incentives to increase productivity, growing consumer and business acceptance of electronic systems and devices, and dramatic improvements in price, performance, and flexibility "are spurring the interest of potential users and suppliers." In fact, SRI forecasts the market for U.S.-produced voice response and speech recognition "should experience high growth at an average annual rate of over 50%, reaching between \$1.265 and \$1.81 billion by 1988." What's more, SRI notes that the current aerospace and

defense market should add one quarter to one half again to the total for all other markets.

Voice-response systems, subsystems, and components, which by far dominate the total speech communications market at present, accounted for from \$14.5 to \$19 million in 1978 and will jump to \$100 million to \$145 million in 1983, SRI estimates. Five years later, voice-response equipment should increase to \$270 million to \$355 million.

Of particular note in SRI's report is the market growth projected for speech recognition equipment, which accounts for only about 10% (\$1.5 million to \$3.0 million) of the total speech communications equipment

market (\$16 million to \$22 million) estimated for 1978. SRI's forecast for 1983 puts speech-recognition equipment at \$151 million to \$192 million. By 1988, this segment is forecast to reach \$995 million to \$1.455 billion.

Whereas the major applications for speech communications equipment are expected to be in the industrial and commercial markets, it is the consumer market that is initially sparking user interest and paving the way for advances in technology. Texas Instruments Inc.'s Speak & Spell learning aid, introduced by the Dallas-based firm nearly two years ago [Electronics, June 22, 1978, p. 39], is largely responsible for consumer

Three ways to design speech synthesis

Each of the three methods of designing speech-synthesis circuits—formant synthesis, linear predictive coding, and waveform digitization with compression—has its supporters. The Votrax division of Federal Screw Works, Troy, Mich., uses formant synthesis; Texas Instruments Inc., Dallas, has been a leading exponent of linear predictive coding; and National Semiconductor Corp., Santa Clara, Calif., has come out for waveform digitization.

In the Votrax system, the process starts by partitioning the text into the basic sound elements, phonemes. But even phonemes are not specific enough for high-quality speech because used in different contexts the same phonemes may sound different. Therefore, the system selects so-called allophones from memory, according to the sound and context of what is to be said. These give the spoken words a lifelike sound.

Votrax machines have 128 allophones to select via either a keyboard or a computer. An advantage of this arrangement is that the vocabulary is unlimited—allophones are simply connected as needed to produce continuous speech. The allophones are generated by 12-bit control words acting on a hardwired phonemic synthesizer developed by Votrax.

The phonemic synthesizer generates speech from the 12-bit control word in two steps. First, the control word is decoded and processed into analog control signals specifying the pitch, duration, timing, amplitude, and overtone quality associated with each allophone. This technique is called synthesis by rule because the rules for extracting the word signals are stored in hardware; the word parameters are not extracted through a computer analysis of actual speech, as with the TI device.

The second step is implemented by a parametric synthesizer, which translates the parametric signals into speech sounds. As with the other techniques, the parametric signals act on an array of sound generators and programmable filters. Voiced sounds are created in the synthesizer by a variable-pitch generator and unvoiced sounds by a white-noise generator.

In the case of Texas Instruments, its trio of chips represents an integrated-circuit model of the vocal tract. Basic to a model is the linear predictive coding technique. LPC

provides the feedback values or coefficients for a secondorder digital lattice filter on the a synthesizer chip.

This multistage linear filter mimics the major resonant modes of the vocal cavity in the human vocal tract. A TMS 1000 microprocessor performs the calculations to derive the filter coefficients. The third chip is a word-storage read-only memory that holds the speech parts broken into four parameters—voicing, pitch, amplitude, and frequency. A complex software algorithm manipulates the sound parameters to create the speech synthesis.

The benefit of LPC is that it takes advantage of the slow time constants of the human vocal tract. These physiological constraints limit the range of formants (frequency ranges) that can follow a prior set. LPC predicts new filter characteristics based on prior sets. Predicting and generating the formant sets reduces memory requirements, as well as the overall system data rate, which is 1,200 bits per second.

National's synthesizer is based on the ability to perform an analog-to-digital conversion of the speech waveform and store it in memory for subsequent retrieval. That would suggest a tall sampling order and make this technique less appealing.

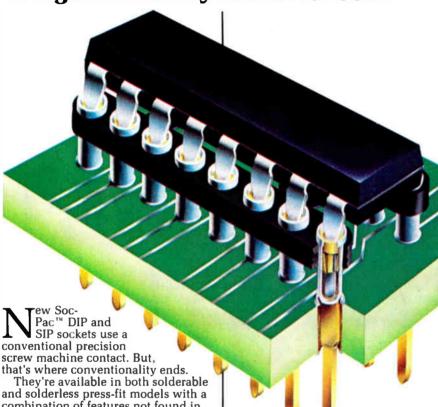
But National has gotten around the problem by combining data-compression techniques to offer a practical approach to chip-level speech synthesis in the time domain. A minicomputer performs the digitizing and compression on an audio tape recording of the original spoken phrases. The resulting data is stored in a ROM for retrieval by a speech-processor chip. Three compression techniques—phase-angle adjustment, delta modulation, and half-period zeroing—reduce the data rate to about 1,000 bits for one second of speech, so that 10 K of ROM stores about 10 words.

Compression is begun by digitizing the analog speech wave and forming the data into groups of 128 samples, called pitch periods. The phase angles are adjusted to produce a set of digitized samples analogous to the spoken phrase. Further compression is achieved by delta modulation, so that instead of digitizing and storing the absolute amplitude of each sample, only the amount of change from the last value is stored.

-Gil Bassak

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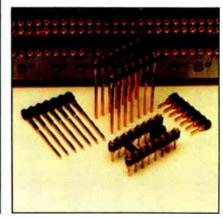
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Inside the news

awareness and interest in speech communications equipment. And, as evidenced at the Consumer Electronics Show in Las Vegas, Nev., earlier this year [Electronics, Jan. 17, p. 39], speech-synthesis and speech-recognition capabilities are proliferating in a variety of products.

Three ways. Thus far, most if not all of the voice-response products introduced or in development use one of three main techniques—formant synthesis, linear predictive coding (LPC), or waveform digitization with compression—to synthesize human speech (see "Three ways to design speech synthesis," p. 97). There are tradeoffs to be considered in the use of each of these techniques, for they vary considerably in the quality of speech provided, the data rate required to achieve acceptable quality, and the cost of the memory for storing speech data, among other factors. Usually, the technique chosen depends upon the application and the size of the vocabulary required for the application.

When Ti's Central Research Laboratories first became involved with the development of Speak & Spell in 1976, both the LPC and formant synthesis techniques were considered, says George R. Doddington, manager of speech synthesis research in the Systems and Information Laboratory. Major consideration was given to producing good-quality speech while linked with other phonemes accord-

keeping the data rate low to hold down storage cost, he notes.

According to Doddington, TI eventually settled on LPC despite the fact that the 1.200-bit-per-second data rate achieved with the technique was not sufficient to meet TI's original goal of at least a 500-word vocabulary. Thus, the original device has about a 230-word vocabulary, which was later expanded with the availability of read-only memory modules.

The 500-600-b/s data rate needed to achieve the original goal could have been accomplished with formant synthesis. But the architecture of such a chip, Doddington says, would have been "substantially more complicated" than that required for the LPC chip. "We were not convinced that the [voice] quality [of formant synthesis] would be sufficient," he says.

Talkies. Also enjoying a measure of success in the speech-synthesis arena is Federal Screw Works' Votrax division, Troy, Mich. Its phoneme-based speech-synthesis system has been incorporated into hobbyist computers, among them Radio Shack's TRS-80 and Commodore Business Machines' PET, as well as in many medical and business applications. IBM Corp.'s Office Products division, Franklin Lakes, N. J., for example, has introduced an audio typing unit for the blind based on the Votrax voice synthesizer. The unit translates each type character into a stored phoneme that, on playback, is ing to programmed rules of pronunciation. The audio typing unit verbalizes punctuation in addition to text and prompts the user through various typewriter functions.

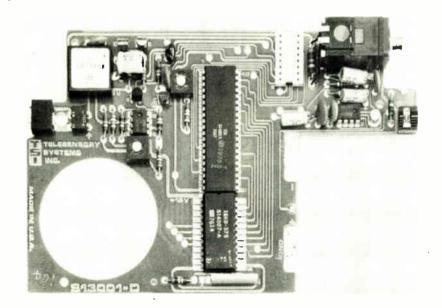
A somewhat similar aid for the handicapped has been developed by Kurzweil Computer Products Inc., Cambridge, Mass. The firm's Reading Machine for the blind uses computer software to convert ASCII-print images into synthesized speech. Conversion is done using a complex set of programming instructions that string phonemes together into whole words and sentences. It relies on Kurzweil's own specially designed analog formant synthesizer, said to be capable of speech rates faster than human speech.

Other aids for the handicapped developed or in various stages of design take advantage of speech-processing technology. For example, Telesensory Systems Inc. of Palo Alto, Calif., developed a talking calculator in 1976 and, more recently, a portable Braille and audio information center. These products and other modules use the LPC technique.

According to Barbara R. Glavish, the company's speech components manager, the LPC approach was chosen because "it is the most useful for the most number of applications." Although the LPC technique consumes more memory than other approaches, it provides an extremely high quality of natural-sounding speech, she states.

The science of speech interfacing

Speaking board. One of two speech-synthesis modules from Telesensory Systems Inc., this calculator unit has a 24-word vocabulary in English, German, or Arabic. It contains a voltage converter, audio filter. amplifier, volume control, and 2-in. speaker.



Inside the news

extends even to pinball machines. Williams Electronics Inc., a Chicago-based subsidiary of Xcor Corp., last year introduced Gorgar, a talking pinball machine that has a 15word vocabulary compressed in a 12-K n-channel MOS ROM.

According to Ward Ellis, engineering vice president, a continuously variable-slope delta-modulation (CVSD) detector chip from Harris Semiconductor, Melbourne, Fla., takes the ROM code and creates a facsimile of a sound waveform under the direction of an 8-bit Motorola 6808 microprocessor.

speech processing with its CVSD chip, introduced about five years ago and originally aimed at telecommunications speech and signal-process-

ing applications [Electronics, Oct. 13, 1977, p. 91]. Harris uses self-aligned silicon-gate complementary-MOS circuitry (for its low-power, high-speed advantages), along with dielectric isolation and on-chip resistors. Ordinarily no microprocessor control or external components are required for recovery of digitized speech; the chip does all its own data conversion and processing, says Harris senior scientist Norman C. Seiler.

In Gorgar, the 15-word vocabulary in ROM can be arranged into eight different phrases. "Substantially all our future machines will have speech," notes Ellis of Williams Electronics.

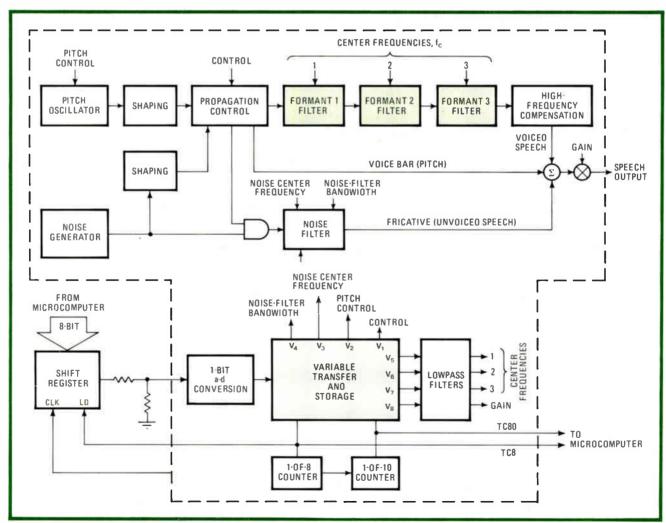
Voicing approval. Others are Harris Semiconductor backed into headed that way. At the recent consumer show, for example, TI introduced a speech synthesizer for its 99/4 home computer, while Atari Inc., Sunnyvale, Calif., showed the

prototype of a new video game. Home Run, with limited speech capability.

Also ready to plunge into the speech-game waters is Mattel Inc.'s Electronics division, Hawthorne, Calif., which unveiled its first voiceactuated game at the consumer show and plans to introduce several products with voice-synthesis capabili-

Mattel is currently working with suppliers of several kinds of speechsynthesis techniques. Director of product engineering David Chandler believes that there is room for each of the different approaches and that the choice of which one to use for a particular application is based on performance and cost tradeoffs, among other factors.

Already enjoying a measure of success with its voice-response games is Fidelity Electronics Ltd., a



Talkative. Intel's 2920 general-purpose signal-processing single chip microcomputer lends itself to speech-synthesis chores. The device is organized to handle format synthesis to lower the memory bit rate. Data rates as low as 100 to 150 b/s are possible.

Miami, Fla.-based firm that has introduced several chess and bridge games that communicate orally with the player. Fidelity's initial voice Chess Challenger, introduced last year, tells the player all its moves, repeats the player's moves, suggests moves and announces mate-in-two for the player to solve.

According to design engineer Robert N. Nelson, the basic chess game has a 50-word vocabulary housed in 8 K of ROM and is controlled by a Z80 8-bit microprocessor.

Attention. Voice response and recognition are also making a lot of noise in the military/aerospace market. One such system, developed by Sperry Univac's Defense Systems division, St. Paul, Minn., instead of creating speech by synthesis methods, prerecords voice responses that are first spoken by a trained announcer, then digitizes the words and phrases and stores them in memory. "We use some speech compression with adaptive differential pulsecode modulation," explains Timothy C. Diller, principal research engineer for speech communications technology. Using ADPCM, he notes, "the net result is much better than can be achieved with synthesis. It turns out just like a tape recording, only the signal hasn't been broken up into its parameters."

To produce speech output, a host computer first specifies the sequences of words and phrases that form the desired output message. A voice-response controller next retrieves the digitized speech from the Sperry Univac-developed VRU-401 voice-response unit. The controller is implemented with a programmable microprocessor, which provides "a great deal of flexibility and internal processing capability," Diller says.

Talk is chip. Perhaps the foremost reason for the acceptance of speech-response technology today is the general availability of speech-synthesizing components. Based on recently announced and ongoing developments from major U. S. and foreign semiconductor producers, it appears the several-hundred-million-dollar market forecast for the late 1980s is within reach. Until recently, TI's speech-synthesis chip set was not sold to outside manufacturers. But

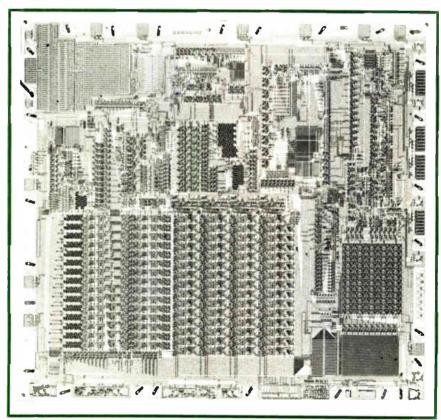
now that other major semiconductor houses are selling—or plan to make available—their LSI implementations of speech synthesis, TI will make its chip set available from a new facility in Midland, Texas [Electronics, May 8, p. 33].

Most likely, a factor in TI's decision to go to the original-equipmentmanufacturer market was the announcement by National Semiconductor Corp., Santa Clara, Calif., of plans to begin offering evaluation quantities in June of its speechprocessor chip (SPC) and a 16-K clocked or static ROM that contains both compressed word patterns and the frequency and amplitude information necessary for speech [Electronics, March 27, p. 39]. Rather than adopting LPC or formant synthesis techniques, National opted for waveform digitization, sampling at twice the highest frequency of interest, a technique used for pulse-code modulation. However, because standard PCM would produce far too many bits in proportion to the amount of talking, the firm uses a comprehensive data-compression scheme to condense the speech data.

Also about to be heard in the market is General Instrument Corp.'s Microelectronics division, Hicksville, N. Y., which is developing a single-chip speech processor, to be available in December. Designated the LISP-0256, the n-MOS chip draws on two techniques for encoding speech—synthesis by analysis like TI's LPC approach and synthesis by rule like Votrax' phoneme-based approach.

GI stores data in ROM on board the 0256 in two forms. One form is the parametric data needed to adjust filter and sound-generator characteristics. The other is the speech phoneme, called up as needed, to form words. Generally speaking, the LPC technique requires relatively large amounts of data, processed at a high rate, and simple hardware, says a GI spokesman. In contrast, speech generation using phonemes needs less data processed at a lower rate. However, he adds, the processing hardware is more complicated.

Equally interested in the prospects for speech-synthesis ICs is Harris Semiconductor's Seiler. He notes that Harris' R&D budget commit-



Japanese. The first effort to use LSI for speech synthesis in Japan used the Parcor(for partial correlation) technique developed by Nippon Telegraph and Telephone Public Corp.

Inside the news

ment to these areas is growing fast and that the firm is developing new products for both speech synthesis and recognition.

Higher calling. Certainly one development that highlights the importance of speech-generating algorithms, when coupled with advanced LSI devices, is the model 2920 general-purpose signal processor from Intel Corp., Santa Clara, Calif. Because of its analog input and output, plus high speed, this single-chip analog microcomputer readily lends itself to speech synthesis. By using appropriate software algorithms, it can implement a variety of speechsynthesis techniques. What's more, the 2920 also is being considered for use as a front end in a voice-recognition system, notes M. E. Hoff Jr., Intel's manager of applications research.

Among several signal-processing applications, Intel engineers have developed a formant speech synthe-

sizer based on the 2920. Although the chip can implement LPC and other speech-synthesizing techniques, Intel is concentrating its efforts on formant synthesis because this method has the potential for using the lowest memory bit rate.

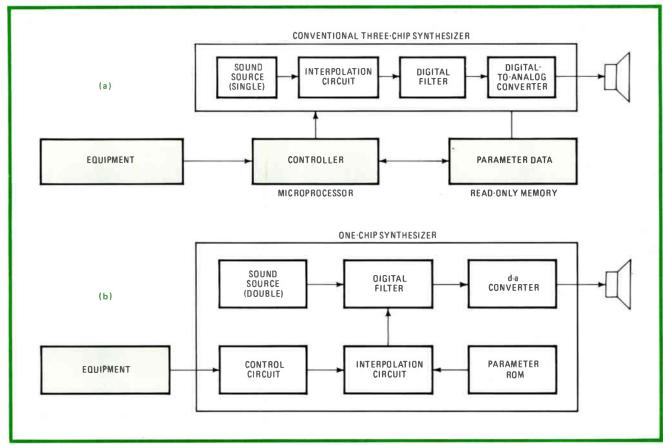
Undoubtedly, one company that is committed to getting speech synthesis off the ground even more than it already has, is Texas Instruments. In the wake of its plans to sell speech chips to outside manufacturers, TI is establishing a new organization within the company devoted primarily to speech and headed by Bernard H. List (see p. 14).

Although he will not talk specifics, List says TI plans to come out with a whole new line of speech chips, which are set to appear over the next 12 months. The first such addition was seen at Electro in Boston last week, where TI unveiled a new LPC synthesizer chip known as the TMS5200. Like the 5100, the new chip is fabricated in p-channel MOS metal-gate technology. Unlike the earlier device, however, the 5200

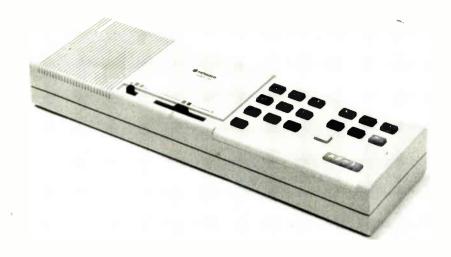
contains a 128-bit first in, first out buffer and other circuitry on board that will enable it to interface with any standard microprocessor having an 8-bit data bus. Speech code for the 5200 can also be stored in any type of standard memory, including n-channel ROMs, erasable programmable ROMs, random-access memories, or bubbles.

Speaking Japanese. As is true of many burgeoning market opportunities, where advanced technologies are making cost-effective and practical applications a reality, U.S. companies are by no means alone in their intensive development efforts. As demonstrated by the spectrum of speech communications equipment previewed this year, the Japanese are on the heels of U.S. speech-synthesis and -recognition developments and may even have taken the lead in some segments of the technology.

Japan's pioneering work in speech synthesis was done by Nippon Telegraph and Telephone Public Corp., which in 1968 announced development of its Parcor (partial correla-



Three to one. Compared with the conventional three-chip synthesizer (a), Matsushita's one-chip n-MOS version (b) has one third to one half the size, power consumption, and cost. It is headed for vending machines, facsimile equipment, calculators, and appliances.





Teaching and telling. Hitachi has put its three-chip speech synthesizer into a \$95 learning aid to teach students the use of the abacus, or soroban (left). Sharp's digital pocket watch (right) uses a C-MOS synthesizer IC that lacks only a 6-bit d-a converter.

tion) coefficients for speech analysis and synthesis. Parcor is a form of LPC, similar to TI's approach, and one that most Japanese companies are using.

NTT built its first experimental speech synthesizer—a large computer—in 1971. Two years ago, it finished a six-year effort to achieve acceptable sound quality at a 2.4 kb/s-to-9.6 kb/s data rate. NTT is synthesizing speech from phonemes stored in memory.

Meanwhile, Hitachi Ltd. has flexed its muscles in the speech communications arena by implementing Parcor on a three-chip set that is Japan's first commercial voice-synthesis LSI device [Electronics, Oct. 25, 1979, p. 63]. Since early February, the firm's Musashi plant has been producing about 1,000 sets daily for in-house use, with outside sales not expected to start for another two or three years. Hitachi's first speechsynthesis product, introduced last month, is an abacus (soroban) trainer that sells for about \$95 and is being produced at the rate of 5,000 monthly. The unit calls out digits and answers for students practicing on the abacus. This month, Hitachi took the wraps off a talking elevator that will go on sale next month. And in August, it will begin selling a talking clock.

The Hitachi chip set uses Parcor, which is a "very stable" form of LPC, says Kazuo Nakata, director of engineering and chief researcher at Hitachi's Central Research Laboratories

in Kokubunji. The speech-processing chip operates at a data rate of 2.4 kb/s and, when coupled with the set's 128-K ROM that stores whole words, can synthesize speech for 50 to 100 seconds. What's more, the set operates with a 4-bit single-chip microcomputer that can control up to 16 128-K ROMs.

Matsushita Electric Industrial Co.'s recent unveiling of a one-chip LSI synthesizer, generated considerable interest in voice communications equipment circles. The first voice-synthesis device from Japan that combines the synthesizer, d-a converter, ROM, and controller on one chip, the n-MOS device is expected to enter production next month and reach large-volume production by August, mainly for use in Matsushita products at first. The chip's 32-K ROM can hold up to 63 words, but external ROM coupled with an external controller can boost capacity. Speech length ranges from 10 seconds for high quality to 30 seconds for low quality. The firm expects to boost vocabulary eightfold within five years by quadrupling its memory and halving its bit rate.

Savings. Using Parcor, the Matsushita chip has a data rate of about 1.6 kb/s. Parcor was chosen because its analysis of sound can be easily processed mechanically and because it offers a low bit rate, explains Shinichi Yagi, assistant planning counselor in Matsushita's R&D center, engineering division.

On the heels of Matsushita's

announcement of a single-chip synthesizer, designed for consumer applications where very high quality is not necessary, Sharp Corp. of Osaka disclosed development of a similar C-MOS speech synthesizer, only without the d-a converter [Electronics, April 10, p. 64]. A new "talking time" pocket-sized digital watch whose components, except for an external 6-bit d-a converter, are contained on a 5.3-by-5.3-millimeter chip announces the time at the press of a key or automatically each half hour. It also makes elapsed time announcements as programmed and 5- and 10-minute audible warnings after its chime and melody alarm have sounded. The Japanese-language model contains 39 words spoken by a female voice, whereas the English-language version holds 43 words spoken by a male voice.

With a bit rate as low as 1.3 kb/s but averaging 2.4 kb/s, the Sharp chip can synthesize 13 to 22 seconds of speech. Capacity can be expanded by adding up to 10 100-K C-MOS ROMs.

Triple play. Just now being heard from in the voice-synthesis field is Nippon Electric Co., which has established itself in the voice-recognition segment of the industry. NEC's IC division is working simultaneously on three groups of synthesizers, the first of which uses ADPCM waveform coding. NEC has a prototype of its n-MOS synthesizer, which offers 10 seconds at 10 kb/s. The multichip device will be converted to C-MOS

Inside the news

next year, according to the company.

The second group of synthesizers NEC is developing include two basic products that use LPC techniques, among them Parcor. One product is a 10-to-12-chip n-MOS signal processor having a data rate of 1.4 kb/s and offering up to 90 seconds (60 to 120 words) of speech. It will be used internally for computer terminals.

The third group of synthesizers will use waveform phoneme synthesis, which Suzuki calls "the perfect one-chip system." It will contain a 32-bit ROM and have a data rate of 800 b/s to 2 kb/s. The device will not be available for several years, the major hurdle being voice analysis.

European tongue. Meanwhile, voice-synthesis developments are being pushed on the European front as well. For example, when Britain's System X made its debut at the Geneva Telecommunications Exhibition last year, one of its crowdpulling features was a voice that talked to the user and helped him to make use of available services. The voice-response system caters to each individual's requirements by acknowledging his push-button actions, offering guidance, and then confirm-

ing the actions taken.

Like many stored-program-control exchanges, System X provides more than a dozen services, among them repeat last call, bar incoming calls, and alarm call. British Post Office researchers determined that instruction books were inadequate and that a means was needed of guiding the caller through the control procedures and informing him how the exchange responded. In the production version, this is achieved by a microprocessor-controlled voice-response system with individual words and word segments stored in 64-millisecond speech segments housed in RAM. For the highest voice fidelity, BPO engineers use PCM techniques to compress digitized speech from 64 kb/s to 48 kb/s. The processor pulls out the needed words from the stored vocabulary and assembles them according to an announcement assembly table, interspersing periods of silence as needed.

France is also working on speech synthesis, but most of the buzzing is coming from two government laboratories. Using LPC techniques, researchers at the Centre National d'Etudes des Télécommunications in Lannion, Brittany, have designed a single-chip synthesizer very similar to that of TI. Corrected prototypes of

the chip are expected by year-end, says Jacques Majos, a researcher in CNET's Microelectronics Laboratory. The chip is fabricated in the multidrain MOS process developed by CNET, although actual production will be handled elsewhere.

Like the TI synthesizer, the CNET chip uses a 10-step lattice filter, but its data-compression scheme requires 6 kb/s of control input, 150% more than the TI device. The CNET chip is optimized for telecommunications applications and, as such, has two different digital outputs. Synthesis experiments at CNET are based on a library of all possible combinations of phonemes that are stored in 600,000 bits of ROM. Though CNET researchers have thus far used a minicomputer to process their data, they are confident a 16bit microprocessor can do the job.

Meanwhile, researchers in the electronics laboratories of the French atomic energy agency—the Commissariat à l'Energie Atomique (CEA)—in Saclay have developed a system based on a wave-function approach to synthesis [Electronics, Aug. 31, 1978, p. 71]. The system currently uses a d-a converter, with the synthesis performed through software, explains Benoit Dupeyrat, a CEA research engineer.

Hearing. As designers drive toward the next generation of synthesis systems, advancing the state of the art of speech recognition appears to be a much tougher task at present. Despite all the advances in LSI technology that make it possible to perform complex signal-processing functions on a single IC, researchers in the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory at the University of California at Berkeley suggest that much work has yet to be done on speechrecognition algorithms.

According to the university's Hy Murveit, "The most difficult problem is to understand a large vocabulary [greater than 1,000 words] of normally spoken, connected speech, without any special knowledge of the speaker. This task has proven to be extremely difficult, and," he adds, "the algorithms which would allow greater than 90% accuracy are not yet developed."

Words, words. One of IBM's speech-recognition projects emphasizes programmability so that users can maintain their own software. The intended use is for office equipment.



In contrast, for small vocabularies (less than 100 words), with each word spoken in isolation by a given speaker, Murveit notes, "it has been possible to obtain extremely high accuracy [greater than 99%] with a relatively straightforward feature-extraction approach."

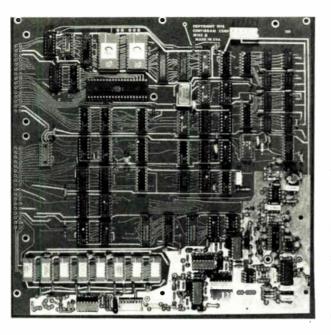
"Speech recognition is a funny kind of business. People paint a very rosy picture for the distant future. It's generally accepted that in 1990, in the data entry room of the office of the future, speech recognition will be an important, economically feasible technology," states Joel S. Birnbaum, director of computer sciences at IBM's Thomas J. Watson Research Center, Yorktown Heights, N. Y. The key question in patternrecognition systems, he says, is that it is hard to set price-performance goals. "Right now we have good ways of getting information into a computer using a keyboard."

Researchers at Bell Laboratories in Murray Hill, N. J., also have made significant strides toward enabling a large population of people to speak directly with a computer. One of the experimental systems they have devised can automatically provide directory assistance in response to a spoken request, rather than push-button entry, like the British Post Office's System X.

Capable of comprehending most American dialects and some foreign accents, the system's "ear" is based on an automatic word recognizer that was developed at Bell Labs several years ago and refined by researchers Larry Rabiner and Aaron Rosenberg to suit the directory assistance application.

A user-independent system for airline reservation and other applications is already available from Dialog Systems Inc., an Exxon Enterprises affiliate located in Belmont, Mass. The major application to date for the firm's model 1800 is for large-company telephone network access by employees in remote locations. They can dial the networkaccess line and give an identification number and the number they wish to call, explains chief engineer R. Robert Osborn, who says the system processes the verbal commands with better than 95% accuracy.

Although technical and market



Analyzer. Voice-recognition board made by Centigram for its Mike terminal learns and recognizes patterns derived from spectrum analysis data. When learning a word, the system stores patterns in memory and then compares the incoming pattern with each reference to make a match.

limitations remain a problem, there are signs that major high-volume applications for voice recognition are beginning to materialize, particularly in computers and terminals. For example, Control Data Corp., Minneapolis, says it is examining the option of adding speech recognition to its Plato computer-aided instruction system. Lear Siegler Inc.'s Data Products division in Anaheim, Calif., has gone a step further by contracting with an outside supplier to provide a speech-recognition system for its ADM-3A, a cathode-ray-tube terminal that has an installed base of about 100,000 units.

Supplied by Heuristics Corp., Sunnyvale, Calif., the speech-recognition module will add \$2,000 to the price tag of the \$895 terminal. However, Philip W. Shires, marketing and sales vice president at the Data Products division, says the disproportionate price for voice "doesn't bother me a bit. It's a matter of total price for the function."

Sharing the enthusiasm for potential applications is Carl L. Berney, engineering vice president at Centigram Corp. The firm, also based in Sunnyvale, has developed a combined voice-recognition and -response system, called Mike. The system learns and subsequently recognizes 16 isolated words or short phrases in any language. Its vocabulary can be segmented into two sets of 16 words in the internal memory, and with the addition of an expan-

sion module having 16 K of RAM, another 10 sets of 16 words can be added. The system responds with up to 8 seconds of speech recorded by the user.

Interstate Electronics Corp. in Anaheim, Calif., sees almost endless potential applications, such as in word-processing control, computeradded design of ICs, and telecommunications. Its voice-recognition offerings currently require 256 bits of memory for each reference pattern, with a 1.5-to-2-second delay in response time. Like Heuristics and Centigram, Interstate makes speechrecognition products available both as single-board modules and as selfcontained units. They are capable of recognizing up to 100 discrete words or phrases spoken by a trained user.

Getting speech-recognition systems to recognize more than isolated words or phrases has indeed proved to be a challenge for most firms in the business. In fact, Japan's NEC appears to be the only supplier that has built and is selling such systems. NEC's DP-100, developed more than two years ago, is capable of recognizing up to five words spoken continuously out of a basic 120-word vocabulary.

Reporting for this article was provided by James Brinton, Linda Lowe, Pamela Hamilton, Wesley Iversen, Larry Waller, Larry Marion, Kenneth Dreyfack, Kevin Smith, Robert Neff, and Charles Cohen.

Mainframe builders making more ICs

More turning to captive lines as semiconductor suppliers turn into competitors with VLSI-based systems

by Larry Marion, Chicago bureau manager

Pragmatic business practices and advancing technology are pulling mainframe makers and their semiconductor vendors away from the close collaborations of the past. A result of the new, more cautious arm's-length relationship is a crop of in-house IC production facilities started up by the computer firms.

One of the biggest stimulants is the introduction by traditional vendors such as Intel Corp. and Texas Instruments Inc. of very large-scale integrated-circuit components and systems that compete with mainframe product lines. Computer designers therefore feel constrained to protect distinctive product concepts expensive and awkward position of by burying them in silicon that they producing chips at the high and low

turn out themselves. "We see more and more vertical integration of the semiconductor industry, and we have to be careful about what we tell our vendors," explains Wallace W. Lindemann, vice president of the Computer Components division of Control Data Corp., Minneapolis. At the same time, IC makers are loathe to talk about their new competitors.

Meanwhile, the increasing expense of IC mass production forces the component vendors to abandon obsolete low-volume parts designed into ongoing peripheral product lines. One result is that the computer makers now find themselves in the ends of the spectrum.

Thus, the recent announcements that Sperry Univac and IBM are building dedicated VLSI production facilities are only the tip of the growing captive-IC production iceberg each mainframe maker in the U.S. now can or is gearing up to produce in house at least 20% of its needs. Though no manufacturer is ready to declare complete independence from the semiconductor vendors, NCR Corp. in Dayton, Ohio, is typical in expecting eventually to produce 60% of its component needs, including logic and memory (see chart).

Sperry Univac is the last of the computer firms to begin IC production. Explains Robert A. Erickson, recently appointed vice president and general manager of Sperry Univac's new Semiconductor division in St. Paul, Minn.: "We've observed that vendors are less and less interested in special work for the computers. We've had suppliers say no to requests to continue producing second-generation parts. They say, 'Using [scarce] silicon to make chips with six to eight gates is damned inefficient."

New needs. Erickson explains Sperry Univac's late entrance into the captive production parade by noting that until now it could get what it needed and that bipolar transistor-transistor logic, emitter-coupled logic, and gate-array production technologies had matured enough to avoid startup cost overruns. On the other hand, if the company had waited longer, the cost would have been prohibitive—beyond the \$50 million already committed.

Honeywell Inc.'s future investments are even bigger-a \$100 mil-

CAPTIVE INTEGRATED-CIRCUIT PRODUCTION: COMPANY PROFILES								
	Number of employees	Number of ICs produced (millions)	Product value (\$ million)	Percent of need	Technology			
IBM Corp.	30,000	-	1,600	80	Large- and medium- scale integrated bipolar logic and memory			
Honeywell Inc.	875	80 (1979)	55	10 – 20	80-90% bipolar integrated injection logic, direct-coupled logic, and low-power Schottky in MSI and LSI			
NCR Corp.	800	50 (1980)	60	40	LS microprocessors, p-MOS and n-MOS memory			
Burroughs Corp.	800	=	50	-	MOS, current-mode, complementary- transistor logic and memory in MSI and LSI			
Sperry Corp. (1982 projection)	less than 800	_	50	20	Very large-scale integrated TTL and emitter-coupled logic, perhaps also complementary-MOS and metal-nitride-oxide-semiconductor logic and memory			
Control Data Corp.	500	50 - 60	30	20 – 25	n-MOS memory, I ² L and ECL in MSI and LSI			
SOURCES: INTEGRATEO CIRCUITS ENGINEERING CORP., STATEMENTS TO ELECTRONICS, ESTIMATES								



Spender. Honeywell, under Carl Nomura, will spend \$100 million for ICs over five years.

lion, five-year capital spending program begun this year strictly for IC design and production, says K. C. (Carl) Nomura, vice president and general manager of the company's Solid State Electronics Center in Plymouth, Minn.

IBM, always a heavy producer of semiconductors, plans to add to its capacity with a 13,000-square-foot IC plant in Manassas, Va., about 60 miles from Washington, D. C. Part of IBM's Federal Systems division facility, the IC plant is keyed to the Defense Department's very high-speed integrated circuit (VHSIC) design competition. It already has 100 workers.

The operation initially will produce silicon-gate n-channel MOS chips with 2-µm features. Advanced bipolar and complementary-MOS technologies are being evaluated, says Ed Spall, manager of the division's advanced development program. Electron-beam direct-writing systems will be installed later as the program becomes operational this summer. Gallium arsenide technology will also be explored for use in VHSIC, in rf amplifiers and analogto-digital converters for radar, but the new operation will not produce standard components, such as random-access and read-only memories.

While VLSI and vertical integration of the vendors are the twin pistons behind the plunge into IC production, each firm has adopted a unique approach. Captive suppliers are usually the component source of last resort, but many are used as the

focal point of new end-product development. Explains Erich Bloch, general manager of IBM's East Fishkill, N. Y., logic facility, "Close coupling between semiconductor development and manufacturing results in better end products."

The contribution to the overall success or failure of the parent company is measured in a variety of ways. The performance of Honeywell's Solid State Electronics Center is measured by the value of the final products containing its components; the center's payback has been 300 to 1 from research through five years of system production, Nomura says. In contrast, James Van Tassel, NCR's new Component division vice president and former MOS product line manager at TI, and Lindemann of CDC both are responsible for a separate profit and loss center—components must meet internal and marketplace cost and price targets.

Other examples of the nature of the captive supplier are:

- Honeywell produces far more ICs for its Industrial Control division than for its computers. Currently it is a 2-to-1 ratio, but that will rapidly change as the Solid State Electronics Center becomes a key source of VLSI components, says Nomura.
- Most of the in-house production of NCR, Burroughs, and CDC are for peripherals, not mainframes, because of the price-performance premium at the printer, tape driver, and terminal level. Sperry Univac will focus on mainframes, though.
- Single-device production at the typical captive operation ranges from 1,000 to less than 10,000 parts per year, except for NCR, which has a 5,000-to-250,000 range.
- Better quality and reliability than are available from the vendors are required to be a successful captive supplier. "It's up to us to convince the purchasing agents in the divisions that we can do as well as or better than the vendors," says CDC's Lindemann. Van Tassel of NCR says, "Our goal is to be considered the most cooperative vendor of specialty devices, with quality and reliability above the merchant market at an acceptable price."

unique approach. Captive suppliers Fine geometries. In addition to the ductor brothers are usually the component source of low profile and "source of last makers are scran last resort, but many are used as the resort" humility at the captive tional specialists.



Gearing up. Sperry Univac is launching its ic division under Robert Erickson.

houses, there is expertise. For example, development chips at CDC and Sperry Univac feature 2-micrometer geometry. CDC has achieved 50,000 gates on a chip, and NCR has reached the 100,000-component level with 3-µm geometry. Sperry Univac, Honeywell, and Burroughs each have an electron-beam machine, and Honeywell has two more on order. "We're making 500- to 600-picosecond devices and have already reached 250 ps," claims Nomura.

In fact, Nomura is currently pondering whether Honeywell should reenter the merchant market with homegrown special-purpose "nuisance" devices that other companies have requested after failing to find vendors willing to provide the chips. "Two questions have to be answered first, though: which chips do we sell, and can we do it at a profit?"

Underneath the bravura of achievement, captive production also can leave the parent company vulnerable to production glitches that can disrupt the entire corporation—like last year's shortfall of MOS memory chips at NCR, due to a variety of yield problems.

But now production is under control, says Van Tassel, who adds that he is spending a significant amount of time on yield improvement. And several unnamed "weak areas" of NCR's Components division will be bolstered with an infusion of outside people, he says. Like their semiconductor brothers, the mainframe makers are scrambling to hire additional specialists.

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Supermarket scanners start to move

Point-of-sale systems make headway as customer resistance lessens and food chains complete equipment evaluations

by Wesley R. Iversen, Dallas bureau manager

The long-simmering market for supermarket point-of-sale scanning equipment may finally be heating up. Despite the looming recession, scanning-system suppliers are adding factory capacity aimed at keeping up with recent mounting backlogs for the laser-based equipment. And point-of-sale vendors at the annual Food Marketing Institute (FMI) convention this month in Dallas were touting new scanners and related hardware among their new product offerings as well as software packages for better utilization of scanner-captured data.

Despite the availability of the technology since 1973, when the

retail food industry adopted the Universal Product Code of vertical bars and spaces for marking grocery products, supermarket scanning has been slow to catch on. Only about 2,000, or 6%, of the nation's 33,000 food stores have scanning equipment in place, says Timothy M. Hammonds, FMI senior vice president. But that figure is about four times the 562 scanning installations reported by FMI at the end of 1978, and grocers now are adding scanners at a rate of about 100 installations per month.

Point-of-sale system vendors attribute the surge in scanner order rates during the past two years to several factors. Early consumer resistance related to the removal of prices from products on the shelf has softened, they say, and most large food chains have now had time to complete evaluation testing of the scanner equipment. An additional barrier fell during 1978, when the portion of products actually marked with the price symbol reached 75% to 80%, the level that industry sources say is necessary to make scanning cost-effective.

Figures for scanner-related savings vary widely by store. But many agree that improved checkstand productivity coupled with the so-called "soft" benefits that come with better inventory and labor management due to availability of scanner data in a variety of report forms can add 1% to a store's profit margin. In an industry that works with notoriously low margins to begin with, vendors are counting on this factor too.

NCR is leader. According to FMI figures, NCR Corp. of Dayton, Ohio, led the industry with 36.1% of the installed scanner base as of March this year, followed closely by IBM Corp. Armonk, N. Y., with 35.3% and National Semiconductor Corp. of Santa Clara, Calif., with 19%. Other vendors with smaller market shares include Sweda International Inc. of Pine Brook, N. J., a division of Litton Industries; Data Terminal Systems Inc. of Maynard, Mass.; and DataCash Systems Inc. of Clearwater, Fla.

As the supermarket-scanner business matures, production capacity of the respective competitors could play a role in ultimate market share. While IBM and National both manufacture their own scanners, several



Light reading. IBM's 3663 supermarket point-of-sale terminal shown in use. The laser-based system has helped IBM sell 35.3% of such installations, just behind leader NCR's 36.1%.

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Probing the news

other vendors purchase the heliumneon gas laser-based systems on an original-equipment-manufacturer basis from Spectra Physics Inc. of Mountain View, Calif. That firm began shipments early this year on a fourth-generation scanner known as the model F, which is being produced exclusively in a new Spectra Physics factory in Eugene, Ore.

The model F uses a design that takes advantage of a recent easing of Federal regulations governing allowable laser radiation output to reduce system component count by 66%, says Alfred P. Hildebrand, general manager of the company's Laser System division. Schottky TTL devices were notable among circuit types eliminated, he indicates.

As noted by Ralph E. Canada, food and drug systems marketing manager for NCR's Dayton, Ohio, Retail Systems division, the model F is "more manufacturable" than Spectra Physics' previous model E scanner. But officials from more

than one vendor at the Dallas show—including Data Terminal Systems and DataCash—complained that slower-than-expected startup deliveries of the model F have contributed to growing backlogs.

Top speed. NCR's Canada reckons that his company's 2552 POS system is currently in place in some 6,000 supermarkets, each of which can be upgraded to scanning. NCR is now "installing scanners as fast as we can" at the rate of about 20 to 30 per month, says Canada. In addition to purchasing Spectra Physics scanner systems, he adds, NCR has recently begun making its own and hopes to boost installation rates to 60 to 70 per month by summer.

National also recently increased its scanner manufacturing capability almost twofold, reports Systems division marketing director John Humphreys. This has enabled the Sunnyvale, Calif., division to cut scanner lead times for its Datachecker POS equipment line from about nine months last November to about four months currently, Humphreys says.

As the scanner technology catches on, more standard software can be expected from vendors that will enable grocers to take advantage of scanner-captured data. Illustrative of this trend are two new software packages from IBM called Merchandise Management and Resource Management. Designed for use on the IBM 3650 programmable store system, these programs are capable of providing more than 50 standard format reports to aid a store manager in controlling merchandise flow and labor and equipment scheduling.

Among new hardware at the Dallas show was the Eagle 1 scanner from DataCash. Pegged for availability in June, the Eagle 1 uses a 2900-type bit-slice processor that is 12 bits wide. The firm says it will significantly increase "first pass" reads of irregularly printed price symbols. Also new was the model 6100 scanner from Sweda, which is said to provide a 50% depth-of-field improvement over previous Sweda units

Out back. Most vendors of POS systems offer the supermarket scanning option within an architecture that includes checkstand terminals with limited intelligence that are tied into a backroom disk-based processor holding the store's inventory file. For an eight-lane store, the total cost of such a system—which sometimes includes dual, redundant processors—was typically quoted at the Dallas show between \$90,000 and \$120,000.

A maverick among vendors is Data Terminal Systems, which has configured its system using no central processor. Rather, the company has chosen to hold down system cost by employing semiconductor chip intelligence at each checkstand. William T. Emberton, food industry systems development manager, says this enables Data Terminal to offer systems at about 40% less than competitors. There are, however, disadvantages. One is that inventory files must be duplicated for each checkstand. No more than four terminals can work from the same file without degrading response time, and the 384-kilobyte capacity currently offered can handle only 15,000 items, which is not big enough for the largest stores.



Checking out. The Bar Double X scanner from National Semiconductor reads product codes at better than 100 inches per second. National ranks third with 19% of installed POS base.

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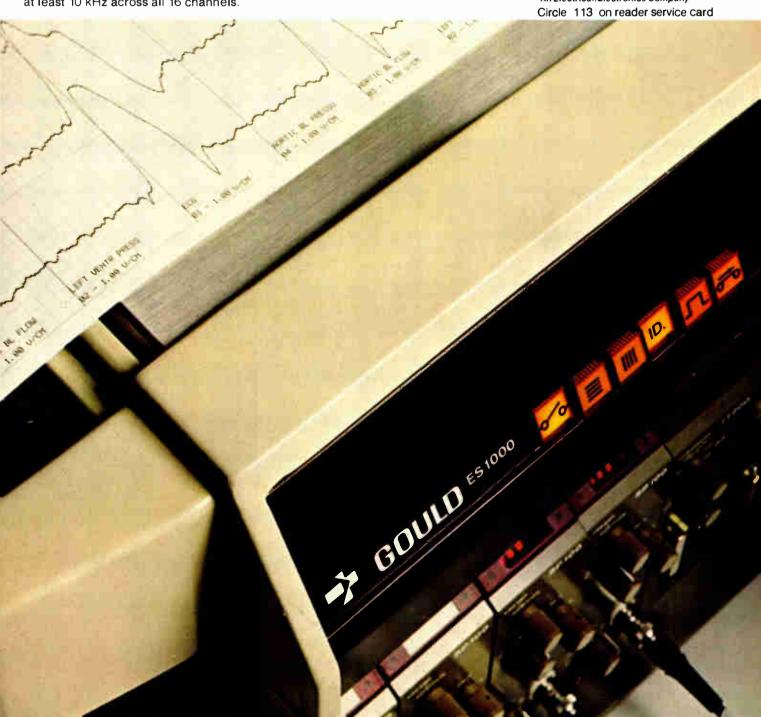
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Displays

World of displays is a wide one

Flat panels especially show the multiplicity of technologies and design talents that are needed to surmount barriers

by Roger Allan, Components Editor

It wasn't too long ago that information display meant cathode-ray tubes. Now, though CRTs are still a dominant force, the world of displays has become an interdisciplinary, multifaceted one involving specialists in a variety of technologies teaming up to solve problems.

Nowhere has this been brought home more clearly than at the Society for Information Display Seminar/Symposium/Exhibition earlier this month in San Diego, Calif. (see "The SID: many disciplines, more members," at bottom). There, circuit designers, software engineers, materials researchers, and interface specialists placed one another's achievements and problems under a magni-

fying glass, coming away with the impression that flat panels are making the kind of progress that will enable them to complement CRTs in the next decade. Born of a need to fulfill special form-factor requirements that the CRT cannot, these new technologies are now poised for market acceptance.

Make no mistake: the CRT will still be around long after other display technologies have matured. However, most display experts queried at the San Diego show, including some CRT stalwarts, felt that, given the rate of information-processing advancements and the greater pervasiveness of computer technology in everyday life, information-

display requirements will dictate more and more the use of new technologies compatible with future needs. These technologies will inevitably be non-CRT flat-panel displays.

Drivers needed. An example of how interdependent different disciplines are in information-display technology-and of a technological weak point that is holding it back is the critical need for more breakthroughs in flat-panel-display drive electronics. At a discussion on such displays, the call went out to semiconductor manufacturers to accelerate their development of driver chips for panels. It was pointed out that plasma, vacuum-fluorescent, and electroluminescent panel displays have reached the point where the remaining stumbling block is the availability of low-cost, high-voltage driver integrated circuits.

Confirming this, representatives of Texas Instruments Inc., Dallas, reported that demand for the company's 512-line plasma-panel driver chips that were on display was beyond expectations [Electronics, May 8, p. 33]. Yet as Laurence Tannas of Aerojet Electro-Systems, Azusa, Calif., a participant in the discussion and a well-known flatpanel display expert, points out, it is difficult to interest a semiconductor manufacturer selling millions of microprocessors and memories in producing more driver ICs with greater voltage and line-driving capabilities for flat-panel displays that are not even in production.

Still, someone has to have the courage to do it first, maintains Elliot Schlam of the U.S. Army Electronics Research and Development Command, Ft. Monmouth,

The SID: many disciplines, more members

The recent Society of Information Display Seminar/Symposium/Exhibition was the most successful in its history. Over 1,000 individuals attended, compared with some 700 last year in Chicago, with most of the technical presentations, panel sessions, and seminars drawing standing-room-only audiences. "Interest in the SID meeting has gone up dramatically, from 46 technical presentations last year to 89 this year," says Ifay Chang of IBM Corp.'s Thomas Watson Research Center, Yorktown Heights, N. Y., program chairman.

The large number of technical presentations reflects the multidisciplinary aspects of the conference, where physicists, electronics engineers, glass manufacturers, avionics experts, and TV broadcast engineers, among others all had something to say. In fact, it is also a reflection of the SID itself, a body that was founded in 1962.

"One of our society's successes has been its interdisciplinary broadness," explains Bernard Lechner of RCA Corp.'s David Sarnoff Laboratories, Princeton, N. J., who is the outgoing SID president. The next president is Tarricia DuPuis of Hughes Aircraft Co., El Segundo, Calif. Ms. DuPuis feels that the SID, with close to 2,000 members worldwide, has become large and well established enough to warrant greater attention from the electrical-electronics engineering communities at large. "We would like to grow at a reasonable rate, but we'd also like to keep the small-community feeling we now have," she says. "Because of the society's relative smallness, you'll find many renaissance SID individuals who are forced to deal with several aspects of information display," she adds.

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Probing the news

N. J. Schlam, also a participant in the session on flat-panel displays, says there is great demand for highvoltage driver ICs for flat panels.

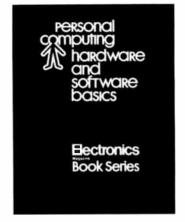
Complicating things is a debate raging among flat-panel experts about the feasibility of flat-panel technology with the use of highvoltage driver ICs. One school feels that flat-panel displays, to be successful, must be compatible with lower-voltage ICs like those made of TTL and emitter-coupled logic. Liquid-crystal and light-emitting diode displays are thus looked upon as more promising, since it may be possibile to integrate the display material and driver electronics on the same chip. On the other hand, LCDs and LEDs cannot compete with plasma, electroluminescent, and vacuum-fluorescent displays for large-screen and graphic applications even though the latter require higher-voltage driver ICs. There is also hope that further research into display materials could reduce the drive voltage needed.

Using the future. As though technology and circuit design were not providing enough barriers that must be surmounted, display experts also find themselves worrying about the human-machine interface. This is particularly true when they discuss the office of the future.

Thus, instead of discussing technologies, a group of experts at San Diego found itself embroiled with questions of how to get people in the office setting to accept the next generation of electronic aids. An emerging consensus is that a definition is needed of what those products will be and what they can do, shaped mainly by how they interact with the office worker.

Panelist Christopher Stockbridge of Bell Laboratories in Holmdel, N. J., summarized the participants' feelings by urging product designers to spell out more clearly what their designs hope to achieve and how these designs will stimulate office workers into accepting them. Such equipment must meet the needs of individuals to maintain or improve their perception of themselves and of others, he said.

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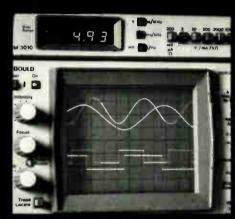
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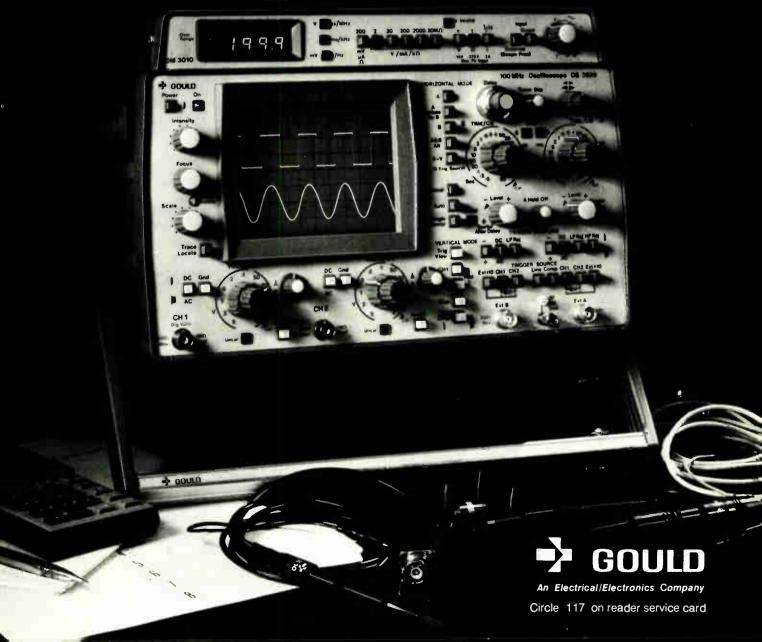
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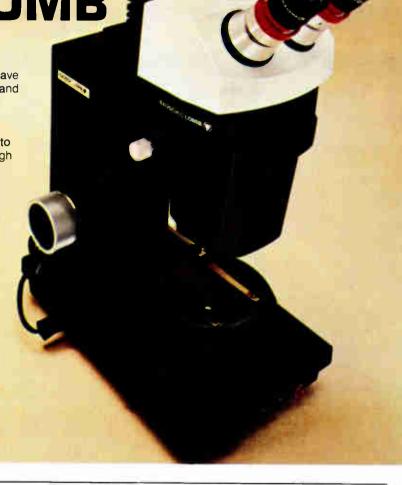
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18	.300	.896	703-5318-01-04-12	703-4218-01-04-10
20	.300	.996	_	703-4220-01-04-10
22	.400	1.096	703-5322-01-04-12	703-4222-01-04-10
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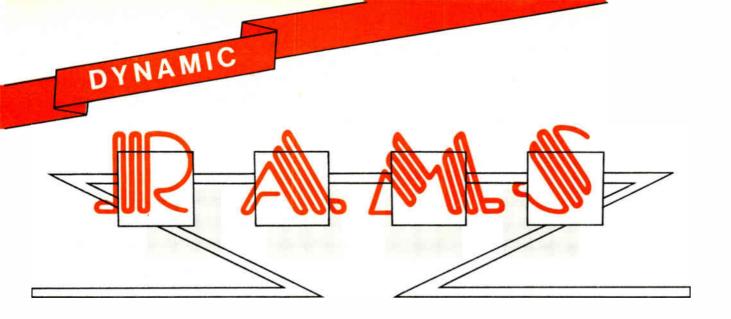
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What to expect next: a special report

64-K and larger dynamic memories struggle toward the market, trusting in a variety of technologies

by John G. Posa, Solid State Editor

☐ Early cost-per-bit studies projected that 64-K random-access memories would be competitive with 16-K RAMS in 1981. However, this prediction was predicated on a bad assumption: that semiconductor manufacturers possessed the resources and technical prowess necessary to mass-produce the parts. For this reason and others, that crossover point has been pushed back two years. While memory users will be denied their bits, this lull in volume production affords an excellent opportunity to compare and contrast 64-K and bigger dynamic RAMS in the offing.

Although the 16-K RAM demanded a second level of polysilicon, its device geometries were not significantly reduced from 5 micrometers, so in-place projection lithography equipment that exposed 4-K RAMs could be used for the new generation. In contrast, the 64-K RAM needs linewidths of 3.5 μ m or less, so the contestants must all learn the art of scaling. This minimum feature also taxes present lithography machines, yet the alternatives—deep-ultraviolet and direct-step-on-wafer exposure systems—are back-ordered.

To make matters worse, it was established that 64-K RAMS should generate their substrate bias internally for operation from a single 5-volt supply. This, in conjunc-

tion with roughly half-sized cells, lowered internal operating margins while at the same time increasing susceptibility to alpha radiation. Undeterred, at least 18 U. S., Japanese, and European chip makers say they will make 64-K RAMS (see table). The carrot being held in front of them is a market exceeding \$1 billion by 1983, according to some market research firms (see "A \$1 billion 64-K market by 1983," p. 121).

Many choices

With so many manufacturers poised to crowd the market, it is reasonable to expect that some or most of the chip designs will be identical or at least similar. Nothing could be further from the truth, however; indeed, the most fascinating aspect of the upcoming dynamic RAMs is the variation in their design. These differences—some subtle, others striking—are no longer just being debated at circuits conferences, but are being put into silicon. And each manufacturer feels strongly justified in choosing the architecture and manufacturing process that it will put into practice.

RAM storage areas are being partitioned into two, four, and eight array sections. Open and folded bit-sense lines will both be used, as will a unique sense amplifier

fed by four bit-sense lines—double the usual number. The chips will be refreshed in 2 milliseconds with 128 cycles or in 4 ms with 256 cycles, and at least three 64-K memories have or will be given counting circuitry for automatic refreshing, done on chip.

Redundancy will be used in some cases to improve yield, while new materials and implants are being tried to up the capacitance of the storage cells. Refractory silicides and laser annealing are being experimented with to lower the resistance of polysilicon wiring, and various coatings are being prepared as shields against ionizing alpha radiation. As a result of this diversity, access times and power dissipations for the latest generation of dynamic RAMs, too, will span a wide range.

A bit of history

The design of 64-K dynamic RAMs got off to an early start in Japan through an adjunct program of its recently concluded four-year, government-sponsored program for research and development of very large-scale integration. But at present the Japanese appear no closer than U. S. chip makers to volume production of 64-K RAMs, although they are regarded as the ultimate threat in the domestic and world dynamic RAM markets—Nippon Electric Corp. was second only to Mostek Corp. in global 16-K RAM shipments for 1979.

Specifically, Japan's initial 64-K RAM designs were targeted for Nippon Telegraph and Telephone Public Corp. equipment. NTT has a research arm—its Musashino Electrical Communication Laboratory—but no real production facilities. At the 1978 International Solid State Circuits Conference, NTT described a 64-K RAM

that was partitioned into 16 4-K arrays; later, in a paper coauthored by Nippon Electric Co., a 16-K-by-4-bit dynamic RAM was presented. Last year, it reported a 64-K chip with a 1- μ m molybdenum gates. None of these designs were slated for production.

Some more recent 64-K RAMS originally intended for NTT were, however, manufactured by NEC, Fujitsu Ltd., and Hitachi Ltd. All were two-supply parts. Between shipments to NTT, Fujitsu and NEC stock their own computers with these devices. Fujitsu also offers its part, the MB8164, commercially; if fact, the company claims to be the only company that can, today, supply 64-K RAMS "by the thousands per month." In the light of the single-supply precedent set by the U. S., Fujitsu plans to introduce a 5-V-only device this month, the MB8264. The fate of its older +7- and -2.5-V RAM depends on demand, says Fujitsu.

Fujitsu's 8164, considered by some to be the first 64-K RAM, was announced in 1978 along with devices from Texas Instruments Inc., International Business Machines Corp., and Motorola Inc., in that order. In 1979, Bell Laboratories and Mitsubishi Electric Corp. followed suit, as did Hitachi, now with a 5-V-only device. Since then, a great many other chip makers have promised 64-K RAMS. Also, 256-K memories have been described by NEC and the Musashino Lab. And the now defunct Kawasaki Cooperative Laboratories of Japan's VLSI Technology Research Association has laid the groundwork for half-megabit and even larger monolithic dynamic RAMS [Electronics, Feb. 14, p. 138].

It is interesting to note that two big names in the memory business—Intel Corp. and NEC—have so far been very close-mouthed about their 64-K devices. NEC will introduce a single-supply device this summer; Intel will do so shortly thereafter. In previous generations, NEC took pride in being the last to announce a device,

Manufacturer	Part number	Die size ¹ (mil ²)	Access time ¹ (ns)	Power dissipation ¹ (mW)	Voltages (V)	Refresh (cycles/ period)	B ²	W²	32·K partial ⁷	5∙V 16∙K
Fujitsu, Tokyo, Japan	MB8164 ³	34,250	150/200	385/n.a.	+7³, -2.5	128/2	FM	Р	N	М
Texas Instruments, Dallas, Texas	TMS4164	33,000	150/200	125/17.5	+5	256/4	D	М	N	Υ
IBM, Essex Junction, Vt.	internal	62,500	330-440	360/20	+8.5, +4.25, -2.2	256/2-3	D	М	Y4	N
Motorola, Phoenix, Ariz.	MCM6664 ⁵	39,000	150/200	275/30	+5	128/2	FM	Р	Y	Υ
Bells Labs, Murray Hill, N.J.	internal	61,800	170	440/n.a.	+8,5	128/4	Р	М	N	N
Hitachi, Tokyo, Japan	HM4864	45,460	150/200	330/20	+5	128/2	FM	Р	M	Υ
Mostek, Carrollton, Texas	MK4164	40,750	100/120	300/20	+5	128/2	Р	M	A _e	Y
Mitsubishi, Tokyo, Japan	M58764S	41,750	150/200	250/27.5	+5	256/4	D	M	N	Y
National, Santa Clara, Calif.	NMC4164	31,000	120/150/200	200/20	+5	256/4	M	Р	Y	Y
Toshiba, Tokyo, Japan	TMM4164C	38,600	120/150	250/20	+5	128/2	D	M	M	N
NEC, Tokyo, Japan	μPD4164	50,650	200	250/28	+5	128/2	D	M	N	Y
Intel, Santa Clara, Calif.	2164	n.a.	100/150/200	n.a.	+5	128/2	n.a.	n.a.	Y	Υ
Siemens, Munich, West Germany	HYB4164	39,000	150	250/n.a.	+5	256/4	n,a.	M	n.a.	n.a.
tTT, Freiburg, West Germany	1 TT 4564	36,000	150	250/25	+5	128/2	D	M	Y	n.a.
AMD, Sunnyvale, Calif.	Am9064	< 40,000	100/150/200	200/20	+5	128/2	n,a,	n.a.	M	Υ
Fairchild, Mountain View, Calif.	F64K	36,450	120	< 200	+5	256/4	М	Р	n.a.	n.a.
Inmos, Colorado Springs, Colo.	n.a.	< 40,000	n.a.	n.a.	+5	256/4	n,a,	n.a.	N	Υ
Signetics, Sunnyvale, Calif.	2164	40,700	60/80/120	300/15	+5	256/4	n.a.	n.a.	Υ	n.a.

1. Actual and speculative values are intermixed. 2. B = bit-line material, W = word-line material, M = metal, D = diffused (ion-implanted), P = polysilicon, F = folded bit line.
3. Newer 8246 is 5-V-only. 4. Not a partial. 5. Newer 6665 has no pin-1 refresh. 6. 4332 contains 2 16-K RAMS; 4532 is a 64-K partial. 7. Y = yes, N = no, M = maybe.

A \$1 billion 64-K market by 1983

Updating its outlook for the dynamic RAM marketplace, Dataquest Inc. now foresees 64-K RAMs crossing the \$1 billion threshold by 1983. As shown in the graph on the left, the Cupertino, Calif., research firm expects the market for 64-K chips to start a steep upward climb in 1981, gaining nearly \$4.5 million in market size per year at least to 1984, leaving the other device types in the dust just after 1982's onset.

The data it has compiled on the single-supply 16-K RAM, too, is optimistic, indicating that a linear upward ramping has already commenced, shooting to hit \$400 million by 1984. But, as underscored by current fluctuations in the cost of triple-supply RAMs due to a softening in demand, RAM pricing and market size are particularly sensitive to industry capacity and day-to-day economics. "If the market goes soft for the 16-K, it will provide the incentive to push wafer starts," states Dataquest's Daniel Klesken. This may close the window on the single-supply 16-K RAM, he cautions.

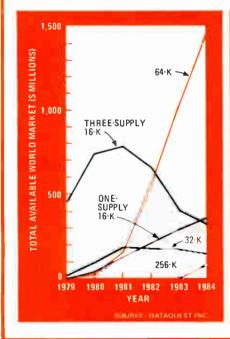
Based on Dataquest's average selling price curves (center graph), the single- and triple-supply 16-K RAMs will not compete on a cost-per-bit basis until the second half of 1981. The curve for the 64-K RAM crosses that for the three-supply 16-K in the second half of 1982 and that for the one-supply 16-K RAM in mid-1983 (right graph).

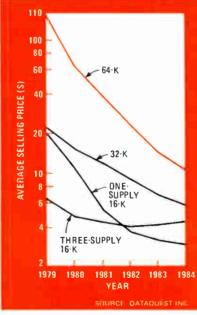
In a market study done by Hitachi Ltd., growth curves for the 16- and 64-K parts are more conservative; but for

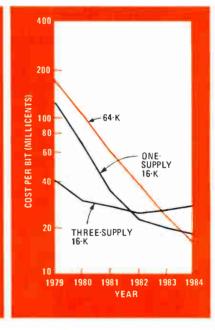
the 256-K RAM, it forecasts a \$0.5 billion market by 1985. Hitachi sees the same peak year for the 16-K RAM—1983—and although its curves resemble those of Dataquest's, Hitachi's combined total for both 16-K device types comes within only 60% of Dataquest's, on the average. With the 64-K RAM, Hitachi closely tracks Dataquest until 1983, at which point it predicts a market of only \$700 million, followed by a wait until 1985 to reach \$1 billion from a more moderate slope.

These market estimates are for worldwide consumption in noninflated, or constant, dollars. Dataquest's Klesken adds that of the total, the U. S. consumes about 55%, Europe about 25%, and Japan, about 20%. He feels that Japan might pick up 5 to 8 percentage points in the next five years for its own computers, subtracting from both European and U. S. shares. But much of this equipment will "get purchased in Europe and the U. S. anyway."

In terms of production, Dataquest says that about 16,000 64-RAMs were shipped in 1979, of which about 10,000 came from Motorola, about 2,400 from TI, and the rest from Fujitsu. Motorola does not repudiate these estimates; in fact it adds that though Dataquest quotes Hitachi as merely supplying samples of its 64-K RAM in 1979, it has "heard rumors that Hitachi may have shipped as many as 1,000 64-Ks last year." IBM and Western Electric (for Bell Labs) both claim to be in volume production of their devices, albeit for captive consumption.







but afterwards began production with a vengeance and quickly forged its way to the top of the pack. With the materialization of the market so distant, these two companies feel no compulsion to rush. After all, each is profiting from 16-K dynamic RAM sales—NEC from its three-supply device and Intel from its new, expensive, but fast single-supply 2118.

As the table shows, more than half of the companies planning 64-K RAMs are also considering single-supply

16-K memories. There will be diversity in these designs too. Some of the manufacturers will first build 64-K RAMs, then offer tiny 16-K chips incorporating the same scaled-down design rules. Others, like Intel, to beat the competition to the market, will first introduce 5-V-only 16-K parts with relaxed geometries. Single-supply 16-K RAMs will not be competitive with three-supply devices for at least another year, especially when 64-K RAM features are used. The parts therefore must—and do—

have something else to offer: speed. Intel's 2118 is twice as fast as the slower versions of its 64-K RAM.

The single-device cell used in modern dynamic RAMs actually contains a MOS FET in series with a storage capacitor. The drain of the transistor connects to a bit line that in turn feeds a sense amplifier for that column of cells. The gate of the transistor connects to a word (or row) line. The bit lines are perpendicular to the sense amplifiers. The word lines are parallel; thus, their number settles how many cells will hang on a sense amp, as well as the number of refreshing cycles.

Dynamic organizations

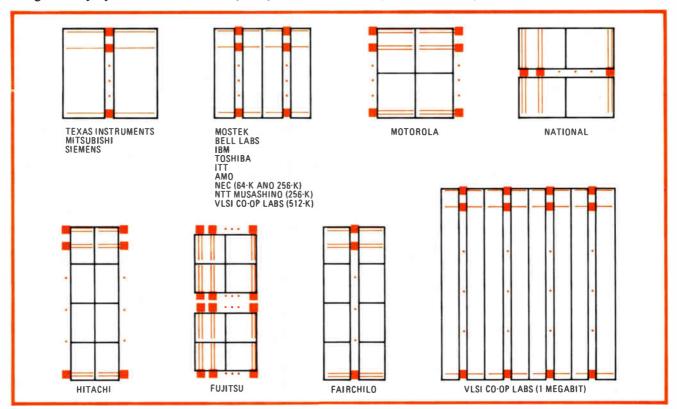
The most daring way to organize a dynamic RAM is to divide up the array the fewest number of times consonant with the requirements of such peripheral circuits as the sense amps and decoders. Large, solid arrays mean long, unbroken bit and column lines, and since metal is rarely used for both, the nonmetallic set of interconnections may exhibit long RC time delays and bog down access time. In addition, if large numbers of cells are attached to the bit lines, more sense amp sensitivity might be required or operating margins may suffer. Also, partitioned arrays may be more conducive to use as partial devices, and it is possible to shut down unused array sections to conserve active power.

No manufacturer has so far been bold enough to build a high-density dynamic RAM and not split up the array at least once. The degree to which 64-K and denser parts are divided is shown in Fig. 1. At the 64-K level, Texas Instruments, Mitsubishi Electric Corp., and Siemens AG begin with a 256-by-256-bit matrix and split it down the middle into two 32-K arrays. It is believed that Signetics Corp. is adopting the same plan for its 64-K chip.

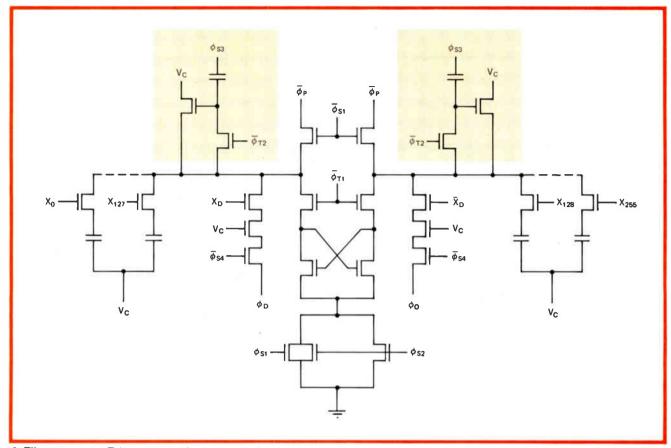
With two 128-by-256-bit arrays, there are 256 sense amps that connect to 256 cells each—128 on either of the two arms that emanate from every amplifier. Since in general the number of cycles required to refresh the array equals the number of cells serviced by each sense amp, TI, Mitsubishi, Siemens, and Signetics all specify a 256-cycle refresh.

Although every 16-K RAM is refreshed with 128 cycles, this 64-K departure from precedent has become a non-issue. As the 128 cycles must be supplied in 2 ms, 256-cycle RAM makers simply specify a 4-ms period. This means that the overhead—the percentage of time wasted on refreshing—is the same in both instances. A common method of refreshing 128-cycle devices is with 7 bits from an external binary counter. But counters have 8 bits if they have 7, so the previously unconnected line is simply brought over to the eighth address line—A₇—of a 256-cycle RAM.

However, with 256 cells attached to each sense amp and with 4 ms elapsing between refreshes, companies like Texas Instruments must take added precautions against leakage or the charge stored on the cells will fade away. Data loss is caused by a buildup of minority carriers underneath and around the storage region, degrading a stored 1 to a 0. Expressing minority carrier buildup mathematically, TI found that leakage currents



1. Array of arrays. Dynamic RAMs are partitioned into two, four, or eight subsections in accordance with sense amplifier and cell design. The sense amps (the small tinted boxes) usually have two bit-sense lines emanating from them. Folded bit-sense lines are adjacent.



2. Tl's sense amp. This sense amplifier is used by Texas Instruments in its 64-K RAM. The word lines, x_0-x_{255} are bootstrapped so full V_{00} potentials are written into the cells. The active load devices (shown tinted) restore this level after reading and refreshing.

are aggravated by increasing the negative substrate voltage, V_{BB}, so the Dallas, Texas, company straps the substrate of its 64-K RAM to the cold-water pipe—in other words, to ground, V_{SS}.

However, all other domestic 64-K RAM suppliers generate a negative substrate bias on chip—with the exception of IBM and Bell Labs, which forgo 5-V-only operation and bias the substrate externally. So TI's practice of making V_{BB} equal to 0 v certainly has given the rest of the industry something to talk about. For instance, the competition cannot fathom how TI achieves workable operating margins since the loss of V_{BB} truncates internal signal swings by at least 2 v.

Enough margin

To keep margins up in the 64-K RAM, most chip makers—TI included—bootstrap their word lines to a high voltage so that a full V_{DD} logical I level can be written into the cells. This bootstrapping offsets the threshold voltage of the cell's selection transistor, which must otherwise be subtracted from the potential stored on the cell. In addition, after a cell is written, state-of-the-art sense amps keep it at full V_{DD} level after read and refresh operations.

TI's sense amp is shown in Fig. 2. V_C is a regulated version of V_{DD} . The active loads (shown tinted) keep 0s equal to V_{SS} and 1s equal to V_{DD} . Until those pull-ups are clocked, however, operation is more or less as in 16-K parts. With a high-going row-address strobe, \overline{RAS} , indi-

cating a precharge mode, precharge clock ϕ_P is set to V_{DD} and sense amp clock $\overline{\phi}_{S4}$ is pulsed to establish a dummy-cell reference between V_{SS} and V_{DD} .

Whether to read it or refresh it, the desired cell is selected with an appropriate word line (x_0 through x_{255}) and, simultaneously, a dummy cell is selected on the opposite side of the sense amp. At this point the crosscouple flip-flop in the sense amp goes through its decision-making process on the basis of signals presented to it by the dummy cell and the memory cell. With clock ϕ_{T1} high, ϕ_{S1} and ϕ_{S2} are sequenced to amplify these voltages, now latched on opposite sides of the flip-flop.

Those active loads now swing into play. First, $\bar{0}_{T2}$ is raised; on the side of the sense amp that reads 0, this discharges the gate of the load transistor (the device across V_{DD} and the bit-sense line). On the high side of the sense amp, though, raising $\bar{\phi}_{T2}$ charges up the gate of that load device. Now ϕ_{S3} is brought higher than V_{DD} —this time to avoid the threshold of the load device—and a full V_{DD} level is restored to the cell. Had a cell been selected on the other side of the sense amp—the zero side—current would have been unable to flow between V_{DD} and the bit-sense line so that the cell would remain near ground.

Active loads and extra clock lines, in addition to bootstrapped lines—are they worth it? Il gives an unequivocal "yes." With the exception of National and Fairchild, for a reason that will be explained shortly, all of the designs with 128-cycle, 2-ms refreshing need

double TI's number of sense amplifiers, or 512. "About 80% of the power dissipation is in the sense amps," explains Dick Gossen, manager of MOS memory development at TI. He and A. C. D'Augustine, dynamic-RAM marketing manager, feel that the schemes using 512 sense amps "are going to have a tough time matching the TMS 4164's 200-mw specification" and parts now coming off the assembly line consume even less, they claim. The TI officials also like to observe that "every successful dynamic RAM to date—including the 1-K 1103, 4-K 4060, 4-K 4027, and 16-K 4116—has had a square organization with a single rail of sense amps running down the middle."

Double strength

In all other 64-K dynamic RAMs, the sense amps are loaded down with only 128 cells, essentially doubling the signal strength riding on the bit lines. This camp of manufacturers believes their almost doubled margins yield a more mass-producible part; after all, if the 64-K RAM cannot be manufactured, who cares about the 256-K RAM anyway? The only drawback with the 128-cycle refresh is that a slightly larger die area is required.

Mostek, Bell Labs, Toshiba, and the others listed in Fig. 1 divvy up the main array lengthwise into a pair of 128-by-256-bit subarrays, each with a row of sense amps running up the middle. They get 128-cycle refreshing, but with the extra row of sense amps. Toshiba feels that two 32-K arrays are just right in light of package restraints and 16-K compatability. It says that "further division [into more arrays] would only increase the amount of on-chip wiring." Also, while TI makes claims about low power consumption, Bell Labs interjects that with two arrays, active power and peak current are both

minimized because only one of the arrays need be selected at a time—in the other block, only row decoding and refreshing occur.

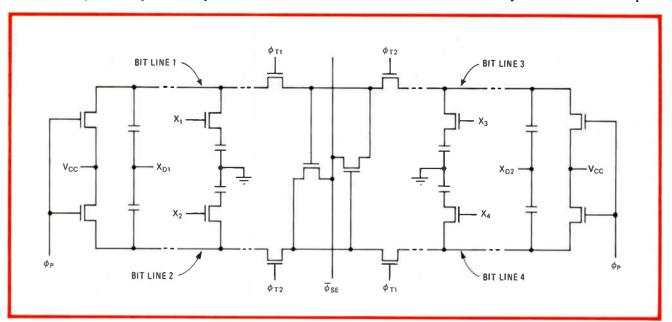
As mentioned briefly already, National and Fairchild use sense amps with double the refreshing power. In their 64-K RAMS, each sense amp is shared between two pairs of bit lines. Both chips use a 256-cycle, 4-ms refresh, need only 128 sense amps, and connect each bit line to only 64 cells.

National's sense amp is shown in Fig. 3 (Fairchild's is similar in principle). Note that it is symmetrical about the sense amp enable line, $\overline{\phi}_{SE}$. Bit lines 1 and 4 are balanced, as are bit lines 2 and 3. Clocks ϕ_{T1} and ϕ_{T2} select one of these pairs, while a memory cell is singled out with the appropriate word line, say X_1 . A dummy cell is also selected, but on the same side of the sense amp as the chosen memory cell.

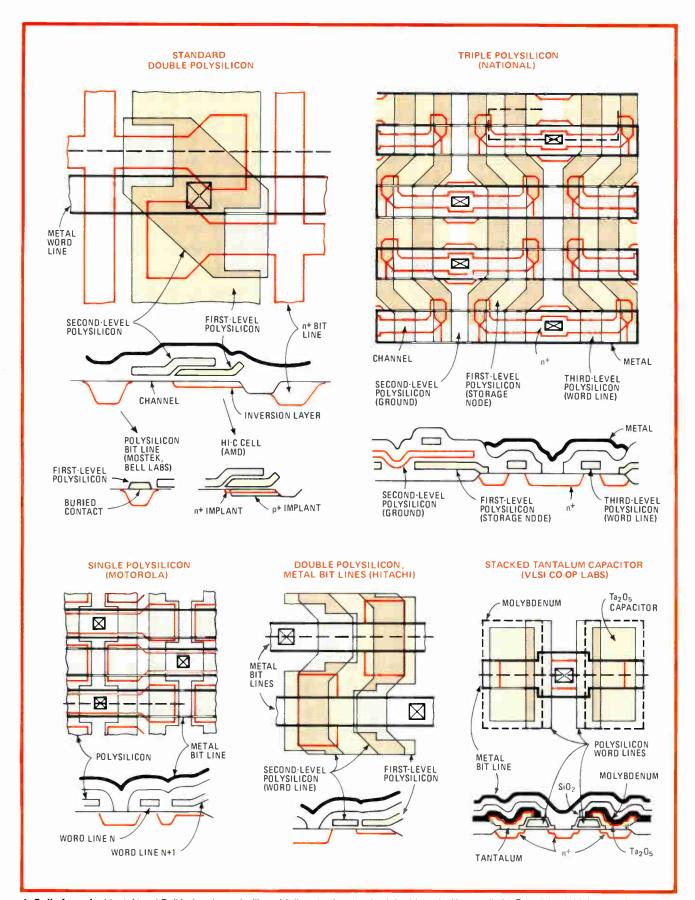
If the memory capacitor is charged to store a 1, the added charge from the dummy cell causes bit line 1 to be slightly more positive than bit line 4. If a zero is stored, the imbalance will go the other way. The difference is sensed and amplified as $\overline{\phi}_{SE}$ is lowered.

John Barnes, a senior staff member in Fairchild's dynamic-memory department, points to another distinct advantage of this scheme: "It allows a full-sized dummy-cell capacitor." The charge on such a capacitor can be divided between two bit lines, presenting each with a midpoint reference; this is exactly what a sense amp wants to see for its comparison. Older dynamic RAMs allowed half-sized dummy capacitors to be fashioned for this purpose, but new RAMs practically forbid it. "How can you make something with half the minimum feature?" asks Barnes.

The sense amps of National and Fairchild are optimally laid out with metal bit (not word) lines. This makes polysilicon the logical choice for the word lines, though now a greater distance must be traversed, forcing a further division of the array to circumvent the speed



3. Four for one. National uses this sense amp in its 64-K RAM and Fairchild will use a similar version. Each amplifier is responsible for four bit lines—twice the usual number—so these two companies are able to achieve 256-cycle refreshing with only 256 sense amps.



4. Cells for sale. Mostek and Bell Labs give polysilicon bit lines to the standard double-polysilicon cell. AMD is giving it high-capacity storage; Motorola has a single-poly process; National's cells have three; Hitachi folds its bit lines; and the VLSI Co-op Labs use tantalum.

problems inherent in polysilicon's high sheet resistance.

Metal bit lines are also helpful against alpha radiation, since diffused bit lines appear even better than the storage nodes at collecting the excess charge generated by the alpha particles. Further shielding is realized by folding the bit lines, which is what Motorola, Hitachi, and Fujitsu have done in their 64-K RAMS.

A twofold plus

Folded bit lines are nothing magical. Each sense amp is still connected to only one pair of bit lines, but instead of being aimed in opposite directions, the lines are laid out right next to each other. The rationale is that the carriers created from the alpha particle will now be coupled to both sides of the sense amp. Since the sense amp is designed to amplify a difference signal, the chance of alpha-generated soft errors will be significantly diminished.

At least one company says that folded bit lines also give layout advantages. Says Bill Martino, a Motorola circuit designer who helped on its 64-K RAM, "You can put the sense amps on one end of the pair of bit lines and you can put a decoder with an I/O section on the other. It saves running the bit lines across the decoder," which can foul up the signal. But, as with the designs of National and Fairchild, metal bit lines strongly suggest polysilicon word lines. As a result, Motorola, Hitachi, and Fujitsu were similarly forced to divide their array and place column decoders within it to decrease word-line propagation delay.

In sum, then, for the same performance that metal word lines provide, polysilicon word lines ask for a somewhat larger die. In addition, Mostek claims that folded bit lines do not permit bootstrapping of the word lines. But there is reason to believe that metal bit lines are a winning choice. Aside from some thick, organic coatings, folded metal bit lines seem to be the best protection against alpha particles. No U.S. 16-K RAMS

5. Burned out. IBM, Bell Labs, and the Musashino Lab of NTT have designed dynamic RAMs with redundant elements to improve yield. Each concern has a unique method of swapping in the extra circuitry. In Bell Labs' 64-K RAM, spare rows and columns are inserted with a laser at the time of wafer probing.

feature folded bit lines, but Fujitsu's 16-K RAM does. "Ask any user, and he'll tell you that the most reliable 16-K RAM is Fujitsu's. Its alpha particle error rate is practically three orders of magnitude less than Mostek's device's," says a senior memory designer at Inmos. "Folded bit lines are the only way to go."

It is no secret that the smart RAM makers are investigating methods to lower polysilicon's sheet resistance. This, in the industry, is referred to as "the low sheet rho problem," the Greek letter ρ symbolizing resistivity. Whereas some IC manufacturers think that the problem can be put off until the 256-K level, Mosaid Inc., the MOS memory analysts in Ottawa, Canada, maintain that low sheet ρ will be needed for the 64-K RAM.

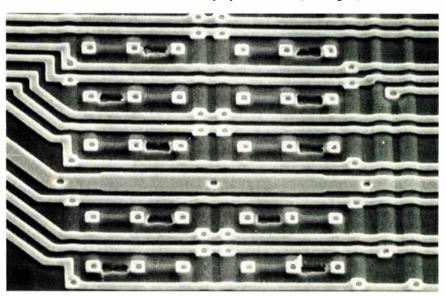
At the present time there are three techniques to heighten polysilicon's conductivity. These include the use of a second metal layer, refractory metal silicides, and laser annealing of the polysilicon itself. All three schemes are being tried. IBM uses two levels of metal in its 64-K RAM, NTT uses molybdenum disilicide word lines in its 256-K device, and memory makers are buying up laser annealing equipment at a fast pace.

As yet, no manufacturer will admit that it is using laser annealing, but there is reason to believe that at least one company—NEC—is using it in its 64-K RAM. Mosaid recently observed NEC's polysilicon interconnections and found them to exhibit large grains and a sheet resistance of about 22 ohms per square. Heavily doped polysilicon has a resistance of over double that. It has also been rumored that Intel Corp. intends to solve the low sheet ρ problem on its 64-K RAM; this decision may have contributed to the tardiness of its chip.

Cells on offer

Besides the variety of architectures and interconnection schemes in the new dynamic RAMs, there is variety in their cell designs. These are based on compact layout, to be sure, but because of the reduced stored charge resulting from scaled geometries, the primary focus is how to achieve more capacitance for the micrometer.

Commercial 16-K RAMs and some 64-K chips use the standard double-polysilicon cell (see Fig. 4). Bit lines are



diffused and staggered so that their hammerhead-shaped appendages, sometimes referred to as spades, interlock. Cell capacitors reside at the tips of these spades. First-level polysilicon field-plate lines meander between each bit line, forming the top capacitor plates and connecting them to $V_{\rm DD}$. Upper-level polysilicon is used as gate material, controlling current between bit lines and storage capacitors. To save room, this second polysilicon layer with its single contact via is shared between two cells from adjacent bit lines. Although two layers will be most common, dynamic RAM cells have been also given one or three layers of polysilicon.

Inversion layers

Actually the bit lines of modern RAMs are ion-implanted and not diffused, but the terminology has held on from the old days. Also, the polysilicon field-plate line has another role. Besides connecting upper capacitor plates to V_{DD} , it also inverts the surface of the silicon underneath it, and the resulting collection of charge becomes the bottom plate of a capacitor.

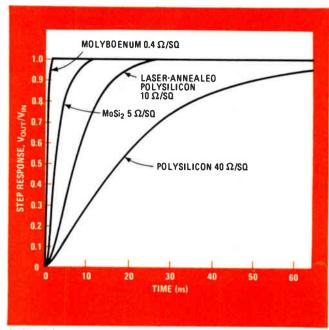
A logical 0 is represented by the electrons trapped in this inversion layer, and a 1 is established through the removal of some of these electrons via the MOS FET switch. The inversion layer can be augmented with a diffusion or implant and, if p-type, the field-plate line can be grounded yet retain electrons.

Evidently Mostek added such a p-type ion implantation (and its mask step) because the capacitors in its 64-K RAM are grounded and not attached to the supply. Sam Young, Mostek's strategic marketing manager of memory products, points out that this configuration eliminates the signal loss due to power supply excursions, commonly known as voltage bumps. Other companies, like TI, circumvent this problem by regulating V_{DD} right on the chip.

Mostek also switched from diffused to polysilicon bit lines for its 64-K RAM. This adds a mask for the buried contact between the diffused and polysilicon regions, but Young explains why the tradeoff is worthwhile: "It allows a larger cell without enlarging the die size. Diffused bit lines sit on the same physical plane as the capacitor, which means that a 4- μ m-wide bit line has to be 7 μ m away from the capacitor on each side.

"With the polysilicon bit line," Young continues, "the entire distance between both capacitors—with the 4- μ m-wide bit line in between—can be reduced to 7 μ m, thus saving 11 μ m" between the two capacitors. According to Bell Labs, which also chose polysilicon bit lines, the resulting ratio of storage cell to bit-line capacitance is 0.08 compared with 0.05 for diffused bit lines and the same layout rules.

To up the capacitance in their 64-K RAMS, Advanced Micro Devices Inc. and a major Japanese chip maker are going to use the high-capacity or Hi-C RAM cell. In this cell, first described by TI in late 1977, a deep p-type implant dramatically increases the otherwise negligible depletion-region component of the storage cell capacitance. Unfortunately the implant also raises the threshold necessary to form the inversion layer, so a second, shallow n-type implant is used to counteract this unwanted side-effect. Aside from the two implants and



6. Good, better, best. If polysilicon is to be used for long, unbroken interconnection paths in dynamic RAMs, its resistance will have to be lowered. This graph, from TI, shows the combined effects of laser annealing, molybdenum disilicide, and pure molybdenum.

their associated masking steps, the Hi-C cell need not be different from a standard double-polysilicon cell.

It takes guts to use the Hi-C cell, though, because alignment is of the essence. If the shallow n implant encroaches too far into the MOS FET's channel region, undesirable short-channel effects may occur. Worse still, if the p implant is allowed to completely engulf the n implant, a potential barrier might arise and prevent reading of the cell capacitor. Nonetheless, "we have taken care of that with our cell structure," boasts Jeff Schlageter, product manager of MOS dynamic RAMS at AMD. "Alignment [of the implants] is no more critical than anything else in the circuit." TI originally predicted that the storage capacity per unit area could be 50% to 100% greater with the Hi-C cell; in practice, AMD expects a 30% increase.

Motorola is the company that gets by with a single level of polysilicon in its 64-K RAM cells; the resulting six-mask process probably did not adversely affect the chip's manufacturability. Using a cell first discussed by Teletype Corp., it also makes every word line double as a field plate line for an adjacent row, as shown in the bottom-left drawing in Fig. 4. This space-saving trick has, however, been criticized from a reliability stand-point. Under certain test procedures and operating conditions such as refreshing, a capacitor's field plate line, being a word line, may be rapidly pulsed. This, say some, may induce built-in voltage-bump problems.

National's 64-K RAM cell adds a third level of polysilicon, allowing both capacitor plates to be made of polysilicon. This layering "allows us to double the amount of charge that can be stored," according to Gene Miles, director of memory components marketing for National. The capacitor is also of higher quality, with only one fifth of the storage node's total area subject to substrate

leakage. Although the third polysilicon level is said to be second in complexity only to epitaxy and the formation of buried n⁺ regions, Miles contends that National's 64-K RAM will use eight or fewer mask steps.

A better dielectric

All of the increases in cell capacitance described thus far have been achieved with silicon dioxide as the dielectric material. But capacitance is directly proportional to the dielectric constant of the insulator, so a change in this material provides another degree of freedom. At last February's ISSCC, Japan's Cooperative Laboratories presented experimental 512-K and 1-megabit dynamic RAMs that exploit tantalum oxide (Ta₂O₅).

Combining the stacked-capacitor RAM cells first described by Hitachi in 1978 with their own quadruply self-aligned MOS process, the lab members refer to their creation as the stacked-high capacitor RAM. With a basic design rule of 2 μ m, the team's 512-K RAM—at about 71,000 square mils—is roughly twice the size of an ordinary 64-K RAM. To build a megabit RAM, it essentially puts two 512-K RAMS onto a single 140,000-mil² die. The designers also state that with a 1- μ m process, chips of "several megabits" are possible.

If the area of the storage capacitor in a standard double-polysilicon cell were to be reduced to the dimensions of the ones in the Co-op Labs' megabit RAM, stored charge would drop from about 250 femtocoulombs to below 30 fc, assuming that cell voltages are restored to full $V_{\rm DD}$ levels. This works out to fewer than 200,000 electrons. Such a minute charge packet would demand almost constant replenishing, and an alpha particle would wreak havoc.

So the researchers opted for tantalum oxide, which has a dielectric constant of 22; SiO₂'s value, at 3.9, is less than a fifth of that. As shown in the cross section in Fig. 4, the tantalum makes direct contact to diffused regions. Next, to form Ta₂O₅, the tantalum is anodically oxidized, then covered with molybdenum.

The process requires 10 masks, but the reward is twofold. One benefit is more stored charge than in conventional double-polysilicon 64-K RAM cells. The second boon is low leakage through the Ta_2O_5 : it takes 3.7×10^4 seconds for a 5-V stored level to decay to 4 V—if the Ta_2O_5 plate is the only escape path, that is.

Adding extras

Tough as it is to squeeze thousands of cells and hundreds of sense amps and decoders onto one substrate, some companies are adding extra circuitry. Bell Labs, IBM, and the Musashino Lab of NTT add redundant cells to improve yield. Motorola and Mostek add to their 64-K RAMs self-refreshing logic, activated with a low signal applied to pin 1. AMD is studying the approaches taken by these two companies as it prepares to pick one of the techniques for a version of its upcoming 64-K RAM. And up Inmos' sleeve is a way to get refreshing without dedicating a pin to the function.

As the logistics of on-chip refreshing are ironed out, there will be a fusion of static and dynamic RAM technology. This will not really affect by-1-bit memory organizations, but it will have a profound impact on byteorganized pseudostatic RAMS, as they are often called. A majority of the 64-K RAM makers also have a self-refreshing 8-K by 8 bit version in the works. If on-chip refreshing can be perfected to the point where dynamic RAMS appear to be truly static—and many feel this probable—it may signal the demise of fully static RAMS beyond the 16-K level, says one TI memory designer.

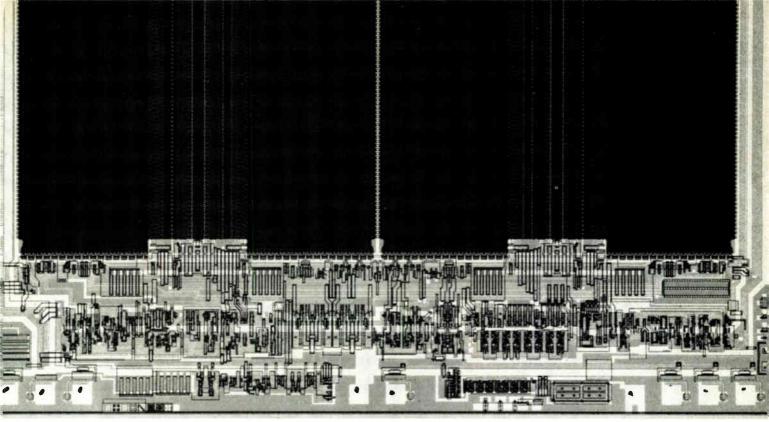
Interestingly, the three approaches to fault-tolerant yield are unique. NTT's 256-K RAM (probably another research vehicle) has four 128-by-512-bit sections, each with one spare word line and four spare bit lines, for a total of 4,096 spare bits; the superfluous cells are substituted with 15-V programming pulses applied at wafer probing. Bell Labs provides two spare rows and two spare columns for each of the four 64-by-256-bit arrays in its 64-K RAM, for a total of over 2,560 bits. Programming here, however, is done by opening 3-\mum-wide polysilicon links with a laser (see Fig. 5).

On IBM's 64-K chip, another device intended just for in-house use, redundant lines pinch-hit for cells, rows or columns that fail functional testing. Bad addresses are stored in an on-chip ROM programmed with the second metalization level; incoming addresses are compared and routed accordingly. IBM's chip contains over 2,000 bits of built-in redundancy, says Nicholas M. Donofrio, manager of systems and test at IBM's General Technology division's development laboratory in Essex Junction, Vt.

In these three examples, neither the percentage of redundant storage nor the method of swapping the extra circuitry is the same. Obviously, a standard form for dynamic RAM redundancy does not exist. Although opinions vary, the consensus is that spare circuitry will not be put into commercially available RAMs, even at the 256-K level. Even though Bell claims that a fault-tolerant memory occupying 62,000 mil² (the size of its chip) will yield better than a memory half that size (slightly smaller than all the others), semiconductor manufacturers are still too proud to anticipate imperfection. And besides, the sale of partially good devices is going well.

Even though on-chip refreshing techniques have been endorsed by some major chip manufacturers, it is the important users that have given the concept a lukewarm welcome. David Ford, Motorola's strategic marketing manager of MOS memories, estimates that "about 50% of our customers want it," but concedes that those customers are in the minority when it comes to sales. "The mainframe guys don't want to refresh," he admits. "That's why we're offering a part [the 6665] that doesn't have it."

Motorola's 6664, the version with refresh, features two internal modes initiated with a low-going signal applied to pin 1. These are self-refresh and automatic refresh. Mostek's pin-1 refresh cycle is a perfect subset of the latter, though there are two minor differences. One is that Mostek specifies that the refresh line be inactive (brought high) for a minimum of 125 nanoseconds within the refreshing cycle. And Motorola puts an upper bound of 2 microseconds on pin 1's low state.



7. New kid in town. It is nowhere near volume production, but the Nippon Electric Co. is actually fabricating this 256-K RAM with wafer steppers from GCA Corp. The chip is only about twice the size of 64-K devices; NEC fit it into a standard 16-pin DIP.

Motorola limits how long pin 1 can be low because after about 13 μ s the chip enters the self-refresh mode, a condition unique to Motorola's 64-K RAM. In this state, a new row is refreshed every 12 to 14 μ s; thus, even in the worst case, the entire memory will be refreshed in less than the 2 ms specified. Motorola says this mode is mainly intended for battery-backup applications.

Packaging problems

There is reason to believe that pin 1 will be used for the ninth address line, A₈, for the 256-K RAM. Such a decision would forgo pin-1 refreshing. This has not yet been standardized by the Joint Electron Device Engineering Council's JC-42 committee, but Intel for one has already announced that it will use this pin for that purpose.

One solution to this dilemma is being proposed by Inmos. When the column address strobe, \overline{CAS} , is pulled low before \overline{RAS} , the row address strobe, an internal refreshing sequence will be activated in its 64-K design. This should not conflict with normal read and write operations since all manufacturers specify that the row address be latched before the column address.

Another solution, being looked at by both Motorola and Mostek, is a package with more pins. Mostek, for example, through a so-called bit-wide concept, will use the same 18-pin package for its 32- and 128-K products. The pin designations have actually been established already with the MK4332, a 32-K RAM built with two 16-K chips. Next, when the 32-K partial of the 64-K RAM becomes available, it too will be put in this package, as will two fully functional 64-K chips for a 128-K device. One reason why Motorola and Mostek want to salvage dedicated-pin refreshing is that the newer microproces-

sors have refresh pins that, in cases, can be directly interfaced to pin 1 on their parts.

More pins are only one of the bitter pills that will be swallowed as higher-density random-access memories draw near; the medicine is being tasted already at the 64-K level. To make the 256-K RAM, IC manufacturers will want to increase sense amplifier sensitivity. For optimum performance and alpha particle hardening, respectively, capacitance will have to be stolen from on-chip wiring and given to the storage nodes while decreasing cell size. A routine method of lowering polysilicon's resistance is anxiously awaited—perhaps only perfection (see Fig. 6). Cells exploiting Hi-C-like concepts will tend to prevail; maybe the use of a higher-dielectric material such as tantalum oxide is the answer.

Alphas revisited

Many of these problems will have to be solved to confound alpha particles. Hitachi has been coating its chips with a proprietary version of the organic material polymide it calls PIQ. A thickness of 40 to 55 μ m diminishes soft errors by a factor of 1,000. Although invisible, alpha particles will still be heard from. But chip coatings, cells with high capacitance, and folded metal bit lines will sufficiently frustrate them.

There exists an entire other class of dynamic RAM cells that combine transfer and storage functions into a single unit. The taper-isolated cell and the stratified-charge memory are 2 of the 10 or so approaches that come to mind. Maybe the next generation of dynamic RAMs will be graced with the enormous density advantages that such concepts have the potential of offering.

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Minicomputer fills mainframe's shoes

Fully compatible with its 16-bit family, this 32-bit minicomputer has mainframe features: multiple-bus hardware with separate instruction and data caches, and a 4.3-gigabyte virtual memory

by Carl J. Alsing, Kenneth D. Holberger, Charles J. Holland, Edward J. Rasala, and Steven J. Wallach, Data General Corp., Westboro, Mass.

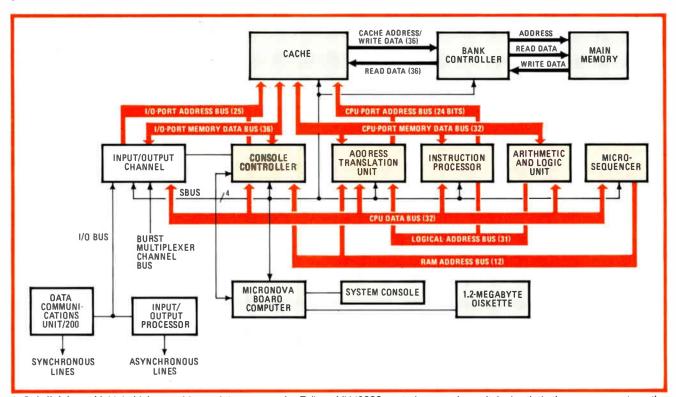
☐ The new head of the Eclipse minicomputer family, the fully compatible 32-bit MV/8000, has a hardware organization that is hard to distinguish from those used in mainframes. It also supports a mainframe-size virtual memory.

The MV/8000 can address a main store of 2 megabytes—as much as IBM's medium-scale 4341 main-frame—and a virtual memory space of 4.3 gigabytes—250 times that of the IBM machine. The new Advanced Operating System/Virtual Storage (AOS/VS) written for the MV/8000 lets users write programs up to 512 megabytes long—32 times the maximum program length for Digital Equipment Corp.'s 32-bit VAX-11/780.

The new Eclipse hardware features a novel cache memory arrangement that uses separate buffers for data and instructions; a pipelined, microprogrammed central processing unit; a separate system-control processor; a high-speed input/output subsystem that can transfer data at rates as high as 16 megabytes/second; and an independent I/O processor that can support up to 128 terminals. An eight-level hierarchical-ring protection scheme is also provided by the hardware.

The MV/8000 is unique in its complete compatibility with the existing 16-bit members of the Eclipse family. Whereas most other machines to date have accomplished this with dual operating modes—a native mode and one compatible with the existing machines—the MV/8000 has only one manner of operation.

To achieve compatibility without adding an operating mode, the MV/8000's instruction set was designed as a superset of the Eclipse instruction set—it includes all the 16-bit instructions as well as 250 new 32-bit instructions. There is no mode bit to distinguish them. This provides total binary compatibility with existing 16-bit Eclipse



1. Subdivisions. Multiple high-speed buses interconnect the Eclipse MV/8000 central processing unit (color tint), the memory system, the system-control processor, and the input/output system. The S bus has only four lines and handles diagnostic functions exclusively.

programs written under the current Advanced Operating System (AOS). They will not have to be recompiled or reassembled to run on the new machine.

In addition, the MV/8000 can concurrently execute existing 16-bit programs with new 32-bit programs and handle an intermingling of both 16- and 32-bit instructions in the same program with no loss in performance. The input/output system is both hardware- and software-compatible with that of the 16-bit Eclipse, as well.

State-of-the-art design concepts implemented in the MV/8000's hardware organization support these architectural features. The computer is divided into four functional portions: the memory system, the central processing unit, an input/output system, and the system-control processor (Fig. 1). Unlike traditional single-bus minicomputer designs, these subsystems are interconnected by several high-speed buses.

Loads of buses

The 36-line I/O-port memory data bus (IPM) carries 4 bytes with 1 bit each for parity checking between memory and the I/O system and the system-control processor. The 32-line CPU-port memory data bus (CPM) connects the CPU and the memory system; due to their physical proximity and the bus protocol, no error checking is used. Two buses for physical addresses, called the I/O-port address bus (IPA) and CPU-port address bus (CPA), connect the I/O system and system console to the memory and the CPU to the memory, respectively. A third data bus, the CPU data bus (CPD), connects the CPU, the system console, and the I/O system. These buses operate at a data-transfer rate of 18.2 megabytes per second.

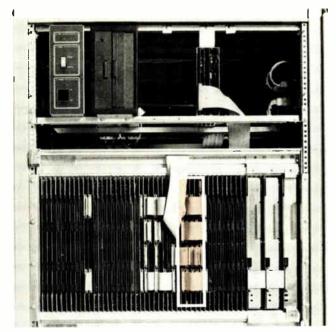
The four-line diagnostic-scan bus (S bus) is connected to all major elements of the computer to allow the system-control processor to perform its diagnostic functions.

The highly pipelined 32-bit central processing unit is built on five standard Data General 15-by-15-inch printed-circuit boards. Because of its compact size, this CPU and up to 2 megabytes of main memory, the 1/O system and the system-control processor (SCP) can fit into a single cabinet that measures 34.5 inches wide, 30.75 inches deep, and 60 inches high and includes the necessary front panel and power supplies (Fig. 2). Each board performs one major function. These boards are the arithmetic and logic unit, microsequencer, address translation unit, instruction processor, and console controller. The CPU has a minor cycle time of 110 nanoseconds and a major cycle time of 220 ns. Instructions typically execute in one or two 220-ns cycles.

The National Semiconductor 2901A-1 4-bit-slice processor is the basic building block for the ALU. This particular version of the 2901 was chosen primarily for its fast arithmetic times.

The ALU is divided into two separate sections, an 8-bit section that performs operations on floating-point exponents, and the 32-bit section that manipulates floating-point mantissas, fixed-point quantities, and 32-bit logical addresses (Fig. 3).

Like the previous top-of-the-line 16-bit Eclipse M/600, the MV/8000 contains four fixed-point accumulators, but in the MV/8000 these accumulators are 32



2. Squeeze play. The 34-inch-wide, 56-slot card cage holds the five 15-by-15-inch CPU boards (tint), along with eight memory boards holding 2 megabytes of memory, the I/O system, the system-control processor, and power supplies. The front panel is at upper left.

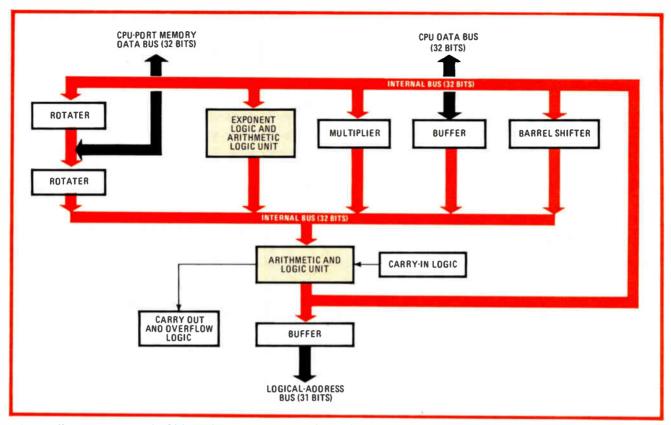
bits wide. Four 32-bit stack registers aid in the management of stacks in main memory and four floating-point accumulators, each 64 bits wide, contain single- or double-precision floating-point operands.

To direct this ALU, the microsequencer chips available in the 2900 family were considered too slow and lacking in flexibility in the generation of the next microinstruction address. But more importantly, the inability to easily dump the contents of the microsubroutine stack maintained within the chip encouraged a custom microsequencer design.

Using programmable-array logic (see "Logic arrays dominate design," p. 133) and a static-RAM control store with a fast (55-ns) access time, the microsequencer contains 4 kilowords of microcode that interpret the MV/8000's instruction set. Each microcode word is 74 bits long plus 1 bit for parity and generates the control signals required by the other processor elements. Because the control store is constructed from random-access memories, unlike previous Eclipse machines, the microcode is loaded from the SCP's diskette.

Feeding the microsequencer

Providing the input to the microsequencer is the instruction processor, which decodes instructions for subsequent execution. Unique among 32-bit minicomputers is the instruction processor's 1-kilobyte direct-mapped instruction cache. It is organized as a 64-block memory with 16 bytes per block and operates on a 110-ns cycle time. During program execution, the instruction cache provides a speed increase because of its look-ahead and look-behind potential. Program loops or backward jumps, in particular, can be executed faster because of this feature. Totally separate from the system cache, the instruction cache allows instructions to be fetched con-



3. Team effort. In addition to the 32-bit arithmetic and logic unit that performs the bulk of the data and address calculations, a second 8-bit ALU is included to handle the exponents of floating-point operands. These ALUs are built with 2901 4-bit-slice processors.

currently with data without interference.

The instruction cache provides the input for the pipelined instruction decoder (Fig. 4). The first stage of this process fetches an instruction from the cache. Then the op code of the instruction is decoded to obtain the starting microcode address (stage 2). In stage 3 the first microinstruction of the microcode program that interprets the instruction is read. In stage 4 the first microinstruction is executed. This four-stage pipeline makes it possible to fetch and decode the next instruction (stages 1 and 2) while the present instruction is executed (stages 3 and 4), increasing performance significantly.

Key to the MV/8000's virtual memory capabilities is the address translation unit (ATU) that converts the logical addresses used in the programs and by the ALU into the physical addresses needed by the main memory system. The ATU performs all the hardware checking required by the protection scheme described later.

To support compatibility with the 16-bit Eclipse, the ATU can also emulate the Eclipse memory management and protection unit, to handle the memory-mapping techniques used in the current systems.

Memory blocks

One of the keys to the high performance of the MV/8000 is its block-oriented memory system. Designed to provide optimum throughput with minimum cost, this block orientation extends throughout the entire MV/8000 and minimizes bus demand and cache fault resolution time. All processor and I/O transfers to main memory go through the cache in 16-byte blocks.

The block-oriented memory system is made up of three major elements. The system cache acts as a high-speed buffer between main memory and the rest of the system to significantly reduce effective memory-access time. The bank controller is the interface between the system cache and third system component, the memory modules themselves.

Between four and eight memory modules are supported by the MV/8000. Because each module stores 256 kilobytes of data, the maximum physical memory is 2 megabytes. A module is organized as 64-K double words of 4 bytes each (a single word being 2 bytes); a 7-bit modified Hamming code is appended to each double word. Each memory module is interleaved four ways, resulting in an extremely high data-transfer rate of 36.4 megabytes per second.

Selecting these memory modules is done by the bank controller when it receives a physical address from the system cache. This controller also performs complete error checking and single-bit error correction on transfers between itself and the memory modules. Byte parity checking is done between the system cache and controller. To further increase reliability the bank controller performs a novel "sniffing" operation. Each time a refresh operation begins, the bank controller reads one block from the memory row being refreshed. This block goes through a complete error check and correction and is written back to the memory module.

Because this operation occurs on a different block during each refresh operation, the entire contents of main memory are checked and, if need be, corrected

Logic arrays dominate design

The hardware design of the new Eclipse MV/8000 is as much a departure from previous designs as the 32-bit architecture is from the existing 16-bit processors.

Most obvious is the widespread use of fast static random-access memories in the various caches and the system's control store. But programmable-array logic chips (PALs), more than any other component, affected the design, performance, and personality of the MV/8000.

A PAL (manufactured by Monolithic Memories Inc. and National Semiconductor) is a programmable AND array providing inputs to a fixed NOR array. Three versions of the PAL family of devices (16R8, 16R4, and 16L8) were used, all of which were packaged in 20-pin, 0.3-inch dual in-line packages.

The use of PALs in the design began slowly, but when it started reducing parts count by a factor of 3 to 5 compared with off-the-shelf medium-scale integration, their use accelerated. Ultimately over 10% of all components used in the central processor were PALs.

Why use so many PALs? They are packaged in 20-pin DIPs, providing good board density; they offer the right functionality while reducing parts count; they permit design changes to be limited to fuse changes in PALs, avoiding board changes; and they are easy to use.

Software design tools developed under Data General's AOS operating system on an internal engineering time-sharing system permitted each logic designer to enter the PAL equations interactively. Then this system is used to create a file containing the fuse characteristics of the desired PAL. The logic designer then inserts a PAL into a Prolog M900 programmable read-only memory programmer connected to the engineering time-sharing system via a RS-232 adapter and personalizes the part. All these actions are done on line.

PALs were not used when an off-the-shelf MSI chip could do the job at a lower price or when a PAL was too slow. About 30% of the PALs used were 16L8s, which have a propagation delay of 40 nanoseconds. In many cases this was not sufficient to handle the worst-case circuit delay. If a PAL with a propagation delay of 20 ns had been available it would have been used.

Of course the decision to use PALs is not easy to make. In all cases, prudent use of PALs and its reduction in parts count must be balanced against their availability in volume and the cost of an equivalent MSI implementation. In some cases the tradeoffs are straightforward. In other cases, where board count, connectors, and system reliability are considered, the tradeoffs become more complicated.

every 4 seconds. Thus, single-bit memory errors do not accumulate undetected over time, which can result in their becoming uncorrectable double-bit errors.

A 16-kilobyte system-wide cache operates with a 110-ns cycle time and is dual-ported so that the CPU and 1/O system each have their own access path. The cache devotes alternate cycles to memory requests from the CPU and the 1/O system, thus reducing the time needed by each to access main memory and minimizing contention between the two ports. The system cache functions as both a look-ahead and look-behind buffer for the system. It contains 1,024 16-byte blocks, which are directly mapped to main memory locations. Simply, every block of main memory always maps into the same cache block. This saves retrieval time to the cache. Stores into the cache utilize the write-back instead of the less efficient write-through technique.

Moving data into and out of the CPU and memory system is the I/O system. It comprises three levels: a high-speed burst multiplexer channel (BMC), a data channel, and programmed I/O. All three are under control of the I/O channel board.

Access to cache

Both the BMC and the data channel transfer data to and from the system cache directly; data need not pass through the CPU. The BMC transfers a 16-byte block at a rate up to 16.16 megabytes per second. Even at this rate, the 32-bit central processing unit can continue unabated. Only when there is conflict over the system cache/bank controller bus does the processor pause.

As previously mentioned, a 16-bit Eclipse minicomputer functions as the 1/O processor (10P) that, connected to the data-channel bus, controls all asynchronous communications for up to 128 user terminals.

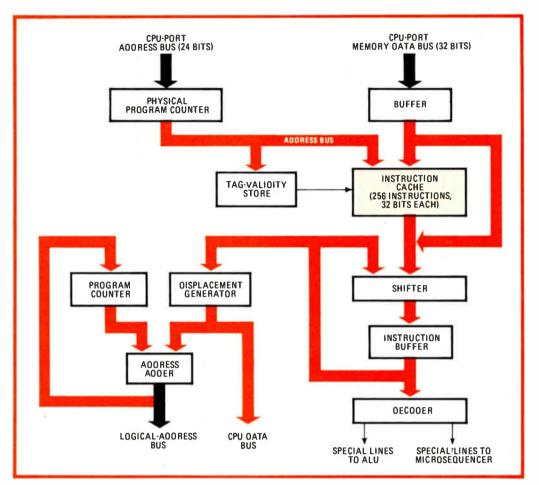
A second front-end communications processor, the Nova-based Data Communications Unit/200, is available for handling synchronous line protocols such as IBM's binary synchronous protocol. Using its 8 kilobytes of local memory, it provides extensive communications handling capability in distributed processing environments. Each DCU/200 can support up to 8 synchronous lines with an aggregate data rate up to 38,400 bits per second or a single 56,000-b/s line. Up to four DCU/200s can be attached to an MV/8000, but the number of synchronous lines on a system is limited to 16.

Managerial processor

Overseeing the operation of the other three elements is the system-control processor (SCP), a diagnostic and console-control monitor. Included in the SCP is the console controller board that provides all the system timing for the MV/8000 including the real-time clock and programmable interval timer. Based on a microNova with 32 kilobytes of RAM, 4 kilobytes of programmable read-only memory, and a 1.2-megabye diskette, the SCP connects to all the other elements of the computer through a diagnostic bus (S bus) driven by a universal asynchronous receiver/transmitter.

Besides providing the operator's console interface into the system, the SCP runs microdiagnostics that isolates faults to a logic board in minutes. Also under control of the SCP is the ability to logically disconnect the instruction cache, system cache, and the ATU address cache. Thus, processing can continue in a degraded mode of operation should one of these units fail.

A significant architectural feature supported by the MV/8000 hardware is its 4.3-gigabyte virtual memory. The MV/8000 operating system, called AOS/VS, provides the mechanisms that allow the virtual-memory



4. Unique cache. The instruction processor contains a 256-instruction cache—a unique feature among 32-bit minicomputers—that speeds instruction fetching. In addition, the decoding of the instruction is pipelined with the execution of the previous instructions.

hierarchy to be totally transparent to the computer's user.

The benefits of virtual memory in general are well established. To these the MV/8000's virtual memory system adds several architectural advantages including a large user-program size of 512 megabytes. Both one- and two-level page-table structures are available to optimize the logical-to-physical address translation for the size of the program being run.

In addition, it lets the operating system be imbedded in the user-addressable space. This significantly decreases processor and software overhead for operating-system call processing. These features make MV/8000's virtual memory system the most advanced virtual memory structure available on 32-bit minicomputers.

Efficient virtual addressing

As in any virtual memory system, data and instructions are moved between main memory and disk in pages. The size of MV/8000 page is 2 kilobytes. The area in main memory that a page occupies is called a page frame. An important characteristic of this memory management scheme is that the largest unit of continuous physical memory is the 2-kilobyte page frame. This makes the AOS/VS memory-management algorithms perform more efficiently.

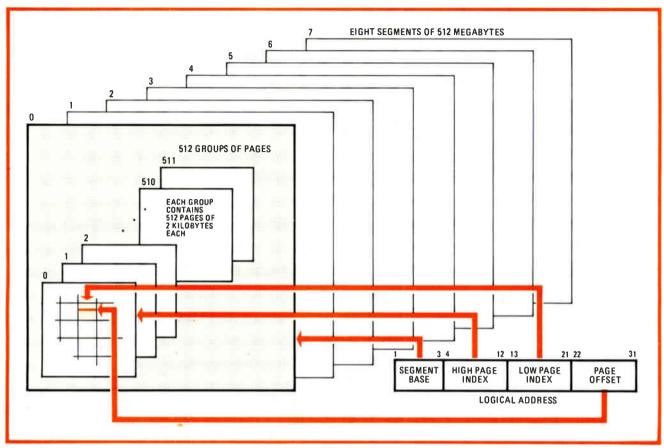
Managing the 4.3 gigabytes of virtual memory simply as 2-kilobyte pages would be a bit unwieldy, however, so the MV/8000 virtual address space is further partitioned

into eight segments. Each segment contains 512 megabytes of memory, or 256,000 pages. The pages within a segment are then divided into 512 groups, each of which contains 512 pages.

This division of the logical address space also reduces the amount of main memory needed to hold shared programs. The shared program is bound into one segment. This segment is used only for these features and the user programs occupy different segments. Then, all users have different user segments but the same run-time segment, only one copy of which need be kept in main memory. This decreases main memory requirements and, more importantly, virtual memory management. That is, only one copy of the shared program per system is managed, rather than one per user.

As shown in Fig. 5, the 31-bit virtual address is subdivided in a similar manner. The first 3 bits denote which of the eight segments are in use. The next 9 bits, called the high page index, indicate which group of pages is being referenced, and the next 9 bits, called the low page index, choose one of the 512 pages in the group. The final 10 bits, called the page offset, locate a 16-bit word within that page. Should the programmer use instructions that generate 32-bit virtual byte addresses, an extra bit is added to the logical word address. The address translation then proceeds as outlined below except that the last bit is saved by the ATU and appended to the final physical address.

The address translation unit hardware transforms this



5. Virtual segments. The 4.3-gigabyte virtual memory is divided into eight 512-megabyte segments, each containing 512 groups of 512 2-kilobyte pages. The 31-bit logical word address is similarly divided to facilitate the address-translation process.

logical address into the 29-bit physical address. It should be noted that while this 29-bit address provides for 536 million words or 1 gigabyte of physical main memory, only a 24-bit physical address is currently implemented in the hardware. And of these 24 bits only the least significant 20 are currently used by the MV/8000 to address its 2-megabyte main memory. The ATU uses page tables stored in main memory to provide the cross-references necessary to derive the physical address.

As shown in Fig. 6, the first 3 bits of the logical address are used by the ATU to pick one of eight segment base registers. These registers contain various flags associated with the security system and the starting address of the appropriate page table in main memory.

The high page index portion of the logical address (bits 4 to 12) is used to index one entry of that table. The contents of this page table entry are used by the ATU to point to 1 of the 512 page tables. Then, together with the low page index of the logical address (bits 13 to 21), it locates an entry in that table. This latter page entry includes flags for the security system, as well as a bit that tells the ATU if the next needed page table is resident in main memory. If not, the ATU signals the operating system to begin the page swap to bring the needed information from disk into main memory. The last 19 bits of the page table entry are appended to the page-offset portion of the logical address (bits 22 to 31) to create the 29-bit physical word address.

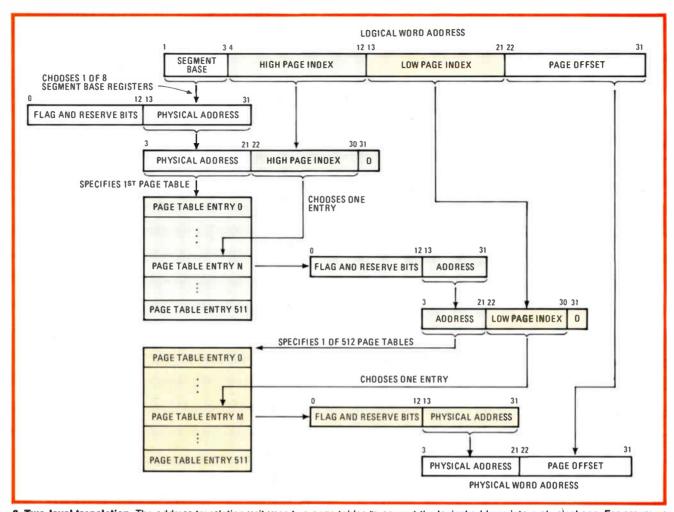
This novel two-level page table scheme provides the

operating system with a great deal of flexibility in managing virtual memory. For programs taking up to 1 megabyte, the operating system can use a single level of page tables, saving translation time. All the high page index bits must be zero in this case.

Dealing with 16-bit addresses

The MV/8000's ability to handle 16-bit direct memory references is crucial to its compatibility with its 16-bit predecessors. It converts the 16-bit byte address into a 32-bit logical byte address by placing it into the 16 low-order bits of the logical address, appending 3 bits from the program counter register, and filling the remaining bits with 0s. This logical address is of course only capable of addressing the first 64 kilobytes of the 512-megabyte segment. But the AOS/VS creates a single-level page table for the segment containing this 16-bit program, thereby minimizing the time for translating the logical address into the physical address and ensuring that existing 16-bit programs can be run without degradation of their memory-reference time.

Once an address translation is made, it is desirable that the association between the logical and physical address be remembered, since programs often reference the same memory locations more than once while executing. Thus the ATU includes a 256-entry direct-mapped address cache that operates with an access time of 45 ns. Because of the design of the translation mechanism, it is expected that more than 98% of the time the needed



6. Two-level translation. The address translation unit uses two page tables to convert the logical address into a physical one. For programs up to 1 megabyte in size, only the second page table (tinted) is used, and the high page index in the logical address (gray) is all 0s.

address translation will already be available in the cache memory, thus speeding memory access.

In addition to partitioning the virtual address space into pages and segments, the virtual address space is duplicated many times over. Each duplicate of the address space is called a process and contains the 8 segments of 512 megabytes each for a total of 4.3 gigabytes. The hardware does not limit the number of processes on the MV/8000 but the current version of the AOS/VS operating system limits it to 255 processes. Various portions of the logical address space of the segments can be shared between different processes, reducing the overall amount of main memory required to support the on-line interactive, multiprogrammed computational environment the MV/8000 is designed for.

Of the eight segments, segment 0 is system-wide—that is, all the processes have the same segment 0. This segment is reserved for the basic kernel of the AOS/VS.

This is one of the most important features of the MV/8000 because it integrates AOS/VS into the user's logical address space. Imbedding the operating system in the user's address context allows the user to view the operating system as a set of system-provided subroutines. The same MV/8000 instruction (CALL) that is used to invoke a user subroutine is also used to make an operat-

ing-system call. This totally hardware-supported structure results in more reliable, structured, and distributed software systems. Reduced hardware and software overhead for servicing operating-system calls is also a byproduct of this sophisticated structure, since a complete context switch does not have to be performed.

Additionally, the user address space is viewed by the operating system as an extension of its own address context. Thus data movement by the operating system between user and system data bases is direct, requires no remapping, and is very efficient.

But imbedding the operating system in the user's address space requires some form of protection against malicious or accidental encroachment by an user on operating-system data bases and programs. The basis of this protection is an eight-level hardware mechanism based on the concept of rings.

Ring around the memory

There are eight hardware-supported protection rings, that correspond to the eight segments of the virtual address space and are numbered 0 to 7 (Fig. 7). Ring 0 is the most privileged and so is where the AOS/VS kernel (the most secure and privileged segment of the operating system) executes. A special class of privileged instruc-

tions can only be executed in ring 0. Instructions which manipulate referenced bits and that perform context switching are examples of the privileged actions that can only be executed in ring 0.

The amount of privilege decreases as the ring number gets higher. Rings 1-3 typically contain outer layers of the operating system. These outer layers, though part of AOS/VS, do not have the same privileges of ring 0. The layering of the operating system in this manner, coupled with the hardware-supported ring structure, results in a highly maintainable and reliable software system.

Rings 4-7 have less privilege than rings 0-3; ring 7 has the least privilege. User programs are executed with the ring 7 privilege.

Hardware within the MV/8000 processor mediates all logical address references with respect to proper ring ordering. The eight-ring structure is tightly coupled with the eight-segment structure of the virtual memory mechanism. Segment 0 always executes with ring 0 privileges. Segment 1 executes with ring 1 privileges, and so on.

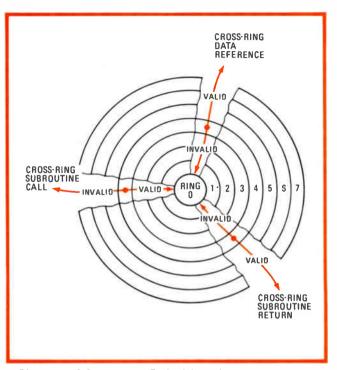
Completing the protection structure two are additional mechanisms: gates and access privileges for a page. Each page table entry contains three access privileges: read, write, and execute. As was mentioned earlier, upon every memory reference, the ATU validates that the correct page-access privileges are being used.

Gates are portals that mediate normally prohibited accesses from higher rings to lower-numbered rings. Gates force all system calls to branch to a known starting instruction location in the called program. If this hardware-enforced protocol were not present, the potential would exist for operating-system—call processing to initiate at an unknown instruction. This would result in unknown side effects, potentially leading to abnormal program or system termination.

The gates' function is analogous to a military security system's. If a person with only confidential clearance needs to have access to a confidential section of a top-secret document, it is clear that a security violation could occur if the entire top-secret document was made available. This problem is solved by requiring a person with the necessary top-secret clearance to screen the document and provide only the requested confidential information. A security violation is avoided and the appropriate information is transmitted.

The hardware-enforced screening is a two-step mechanism. The first step requires that the caller possess a minimum ring number. This is an example of the military principle of "need to know." The second step is the direct vectoring to a known starting instruction within the inner (callee's) ring. Then the inner-ring program beginning with this instruction provides the proper data-extraction service and returns the requested operands to the caller.

As previously described, all valid data references must be to the same or to an outer ring. All subroutine calls must be to the same or to inward rings (that is, toward ring 0). Inward calls to rings 0-3 are operating system calls. Inward calls to rings 4, 5, and 6 by the user are typically to common run-time support or to proprietary software packages provided by a system house. Subroutine returns are the inverse of subroutine calls. Valid



7. Ring around the memory. Each of the eight memory segments is associated with one of the eight protection rings. Ring 0 is the most secure and privileged and ring 7 is the least privileged. Accesses across ring boundaries are permitted only in certain directions.

returns are either to the same or to outward rings.

The MV/8000 protection mechanisms serve to enhance the reliability of the user and system software systems. Program debugging is made easier and runaway user programs are kept isolated to their own process. High-level operating-system services can be made available to the user without concern for system integrity.

Room to grow

As in other aspects, the MV/8000 leaves room for growth. In the initial releases of AOS/VS, certain rings are reserved for future system-software expansion. As these operating system functions are added, they can reliably be incorporated in the reserved rings.

With the exception of this virtual memory and protection mechanisms, the architecture of the MV/8000 is basically an extension of the 16-bit Eclipse machines.

The instruction set of the MV/8000 comprises 437 instructions of which over 250 are new. The rest are the same as the instructions of the 16-bit Eclipse processors. This comprehensive instruction set can manipulate several types of data, including fixed point bytes, 16-bit words, and 32-bit double words, single- and doubleprecision floating-point operands, byte strings, and bit strings. Furthermore, eight types of commercial variable-length byte strings and stacks are supported. New instructions handle 32-bit integers for the first time in an Eclipse, plus linked structures that can be manipulated as double-threaded queues or single-threaded linked lists. These instructions can be used with three types of addressing: absolute, program-counter-relative, and accumulator-relative, which can be performed with 16- or 32-bit displacement.

Designer's casebook

Fm decoder improves SCA subcarrier detection

by Robert F. Woody Christiansburg, Va.

The 67.5-kilohertz subcarrier required for subsidiary communications authorization (SCA) service in the fm band can be recovered by a decoder that needs only two chips and one discrete amplifier. And it can be built for less than \$10. Besides using fewer parts than existing designs, this circuit provides higher output and offers greater versatility.

As an illustration of its advantages, the 4046 phase-locked loop in the decoder provides an output level approximately equal to the fm level at its input, thereby generating adequate drive to succeeding stages. In addition, the PLL's filter also serves as the deemphasis filter, thus eliminating the need for a separate network. Finally, upon loss of the subcarrier, the circuit generates a signal that can cue a recorded message to the audience receiving SCA service.

The decoder is attached to an fm receiver at its ratio-detector output, ahead of the deemphasis filter. For best performance, it is recommended that the signal be

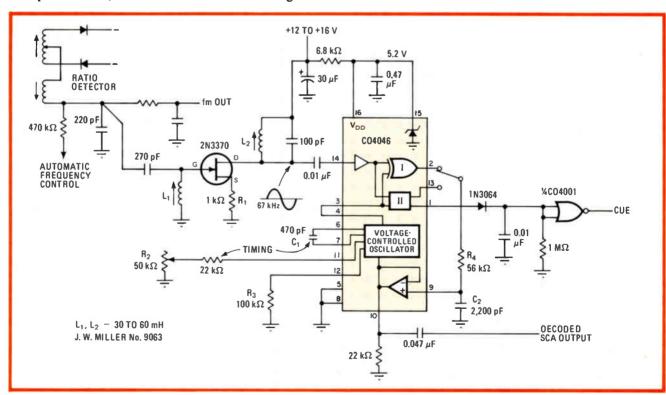
taken from a stereo receiver because its bandwidth, which is designed to be broad for the stereo carrier, provides good reception of the 67.5-kHz SCA signal.

The 2N3370 tuned field-effect-transistor amplifier separates the low-level subcarrier from the other program material, including the very strong stereo carrier. Resistor R_1 yields maximum amplifier gain at 1 kilohm. This resistance can be increased to reduce the amplifier's gain for fm receivers that deliver high-level output signals. Values to $5 \, k\Omega$ are within the amp's range.

The CD4046 PLL performs the decoding. C_1 and R_2 set the loop's center frequency. R_3 sets the conversion gain (volts/radian) of the PLL's voltage-controlled oscillator. Increasing R_3 makes the VCO less sensitive to input-voltage changes. Decreasing R_3 reduces the SCA output level.

 \tilde{C}_2 and R_4 comprise the low-pass filter. As placed in the circuit, these elements also deemphasize the SCA signal at high frequencies, the amount of deemphasis being about 3 decibels at 1.3 kHz.

A string of pulses is emitted from pin 1 of the 4046 when the PLL is in lock. The pulses are rectified by the 1N3064 diode and filtered by the 0.01-microfarad capacitor. Thus a dc level is derived. Should the subcarrier disappear, however, the level will fall and the CD4001 NOR gate will go high. This signal can be used to cue the playing of recorded messages, such as typical commercial advertisements.



Simple service. Improved fm decoder for detecting SCA subcarrier yields higher output, uses fewer parts, provides good selectivity and cue option. Requiring only two chips, and one tuned amplifier for separating the stereo from the SCA subcarrier, it costs less than \$10.

Low-cost logarithmic amp works over one decade

by Christopher S. Tocci
Becton-Dickinson Medical Systems, Westwood, Mass.

If extremely high precision is unnecessary and if the required dynamic range spans no more than one decade of input voltage, then this logarithmic amplifier will serve the application well. Use of a simple exponential generator, which is ultimately required to convert a voltage into its base-10 logarithmic equivalent, makes it possible to build the amp for a mere \$3 to \$4.

The overall system is shown in (a), with the schematic of the exponential generator shown in (b). Voltage divider R_1 - R_2 applies 0.5 volt to RC combination R_3C_1 through op amp A_2 on power-up in order to initialize the exponential growth process. As C_1 charges, the output of A_2 increases as shown in the curve until the Schmitt trigger, A_3 , which has a switching threshold of 10 V, fires, turning on field-effect transistor Q_1 and discharg-

ing C_1 to about 1.0 V. The process then repeats, with switching occurring at a rate, τ , determined by C_1 and R_2 . The op amp must have a minimum slew rate of:

$$dV_o(t)_{max}/dt = (1/\tau) e^{t/\tau}_{k-\tau}$$

= $(10 \log_e 10)/\tau = 23.03 f_s$

where f_s is the switching frequency. Thus at a switching frequency of 10 kilohertz ($C_1 = 0.01 \, \mu F$, $R_1 = 4.32 \, k\Omega$) the slew rate must be at least 0.23 V/microsecond.

During each switching cycle, the exponential output is compared at A_1 to the instantaneous input voltage, V_c , that is to be converted into its corresponding logarithm. A_1 's on time, D_{V_c} , is thus related to input voltage V_c by:

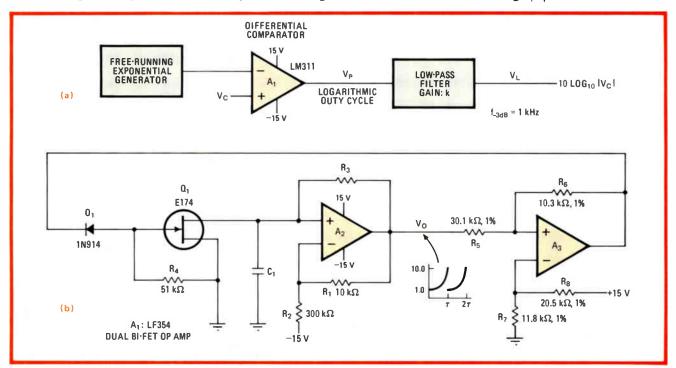
$$D_{V_e} = (t_{on}/\tau) \ 100 = \tau \log_e |V_c|/\tau = 0.434 \log_e |V_c|$$

where output voltage V_p corresponds directly to D_{ν_p} , ignoring a scale factor.

The active low-pass filter of gain k that follows, which should be at least a third-order type for the best results, then finds the average value of V_p from:

$$V_L = \overline{V}_p = k(0.434) \log_e |V_c|$$

Choosing k such that $k(0.434) = k(V_{p \text{ max}}/\log_e 10) = 4.34$, it is seen that $V_L = 10 \log_{10} |V_c|$ for $1 \le V_c \le 10$.



Naturally. Low-cost generator provides exponential waveform of sufficient accuracy in amplifier that takes logarithms over one decade of input voltage. Filter averages pulse-width-modulated equivalent of V_c produced by differential comparator, A_1 , for $V_L = 10 \log_{10} V_c$.

Hall sensors and flip-flop sustain pendulum's swing

by John Karasz Sperry Corp., Great Neck, N. Y. This circuit offers a simple way to control and sustain oscillatory motion in a simple pendulum and in many other types of mechanical oscillators. Using Hall-effect sensors to detect the instantaneous position of the pendulum and to call for delivery of an energy burst through a flip-flop to keep it swinging, the circuit is a good alternative to the complicated electromechanical arrangements frequently employed. The cost of the entire circuit is also

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relatively low, making it especially attractive.

When the small permanent alnico magnet that is part of the pendulum support rod comes into sufficiently close proximity to Hall sensor S_1 , the sensor generates a negative-going pulse. This pulse sets the R-S flip-flop formed by two cross-coupled 74LS00 NAND gates, A_1 and A_2 . The Q output of the flip-flop, now at logic 1, energizes electromagnet L_1 , thereby delivering energy to the pendulum via the field between the steel pendulum bob and L_1 .

When the pendulum bob reaches the lowest point in its trajectory, L_1 is deenergized by the negative-going pulse generated by sensor S_2 , which clears the flip-flop. Simultaneously, one-shot A_5 is triggered. Hence, as long as the Q output of A_5 remains active low, the flip-flop cannot be retriggered because gate A_4 cannot move to logic 0. This action prevents L_1 from energizing and thus creating any drag effect on the pendulum. Also, it conserves power by limiting the time L_1 is on.

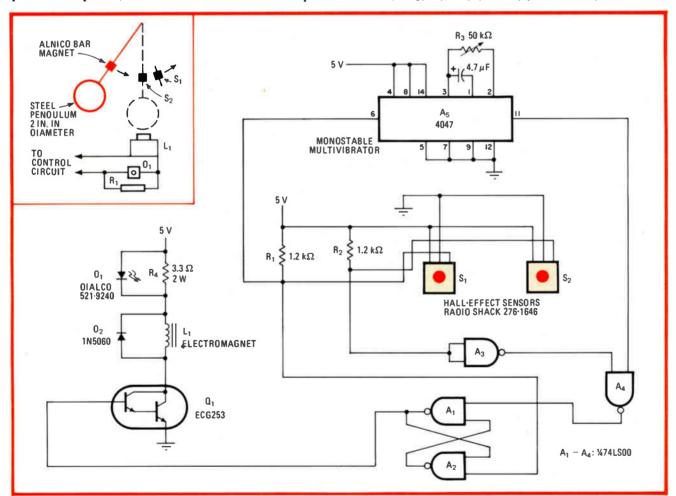
In order to initialize the circuit at a relatively small pendulum swing, the period of the one-shot should be set for t = T/4, where T is the natural period of the pendulum. Because the oscillation frequency of a simple pendulum is $\omega^2 = g/L$, where $\omega = 2\pi f$, g = 32.2 feet per second squared, and L = the distance from the point

of support to center of mass of the pendulum bob, it may be seen that $T = 2\pi (L/g)^{\nu_i}$, and so t should be in the range of 0.32 to 0.36 s in a practical configuration, for T = 1.44 s.

As for component considerations, L_1 is constructed from 100 feet of AWG 24 enameled wire wound on a steel core $1\frac{1}{16}$ inch long and $\frac{3}{8}$ in. in diameter. The alnico magnet is situated only about 0.45 in. above the top surface of the pendulum bob—in terms of metric units, approximately 12 millimeters away. The magnet is 3 mm wide, 3 mm high, and 8 mm long. The clearance between the magnet's pole face and the Hall-effect sensor's surface should be between $\frac{1}{32}$ in. and $\frac{1}{16}$ in. for best results. A small decoupling capacitor (0.033 μ F, disk ceramic) is connected between the supply lead and ground of the 74LS00 chip to keep circuit transients caused by S_1 or S_2 's firing from inadvertently setting the flip-flop to the wrong state.

Light-emitting diode D_1 serves as a visual monitor, being lit when L_1 is energized. When mounted at the base of the electromagnet, it facilitates a qualitative check on the performance of the system.

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$50 for each item published.



Keep swinging. Hall-effect sensors detect instantaneous position of pendulum, direct flip-flops A₁-A₄ to generate energy pulse via field between L₁ and alnico magnet in order to keep pendulum moving. One-shot A₅ prevents flip-flop refiring in any given cycle, thus stops pendulum drag, and conserves energy. Inset illustrates physical relation of bar magnet to pendulum and interface elements.

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8:00 a.m. Registration

8:30 a.m. Introduction of Intel's total solution approach

10:30 a.m.

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12:00 Noon—Lunch

1:00 p.m.

Microsystem architecture Discussion of new peripheral building blocks and system interconnects

2:30 p.m. Microsystem software Review of new operating systems, high level languages and development tools

3:45 p.m.

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MOS FETs rise to new levels of power

Boasting exciting performance advantages over bipolar transistors, they are moving into numerous applications and even creating new ones

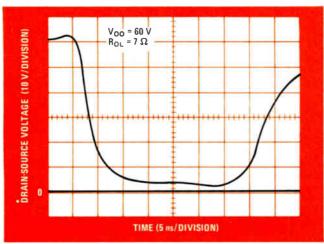
by Rudy Severns, Intersil Inc., Cupertino, Calif.

☐ Advances in the fabrication of MOS field-effect transistors have freed them and their users from their earlier power limitations. Now, designers can exploit to the full their performance and economic advantages over bipolar power transistors.

Besides costing less than bipolar types, power MOS FETS switch faster (typically in a few nanoseconds), offer higher input impedances with low drive requirements, simplify multiple-device operation, and greatly extend safe operating areas. Thus it is no surprise that they are beginning to replace bipolar transistors in many power-switching applications. Furthermore, they have created circuit opportunities that did not exist before.

Several different types of power MOS FET are available, each with its own strong and weak points, and all steadily increasing in performance levels. Despite the proliferation of a host of power MOS FET structures with similar-sounding and confusing names—like V-MOS, V-FET, HEX FET, T-MOS, D-MOS, and Z-MOS—they all break down into three basic structures: vertical-junction MOS FETS, V-groove MOS FETS, and vertical D-MOS FETS (see "Examining power FET structures," p. 144).

Although power MOS FETs compete favorably with bipolar transistors in performance, the different structures do not yield the same benefits. And beyond a good

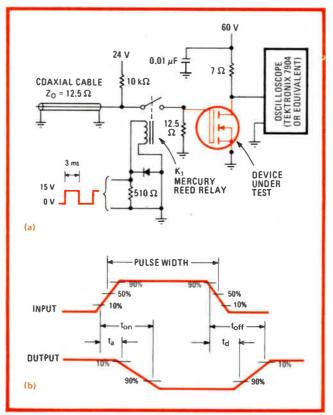


1. Switched. A power MOS FET like the Intersil IVN5200 can switch nearly 60 V at 8 A in a little more than 5 ns. The test circuit of Fig. 2 was used for switching. The slight voltage rise at turn on is caused by capacitive coupling of the drive pulse to the output.

understanding of how each type behaves lies the need for a basic understanding of how a power MOS FET in general differs in construction, operating characteristics, and application from a bipolar transistor. Such an understanding is a prerequisite for getting the most out of the device.

Breakdown voltage affects on-resistance

As the breakdown voltage rating of either a MOS FET or a bipolar transistor increases, the transistor's on-resistance goes up by an exponential factor of 2.3 to 2.7 for a given die area and process. If the breakdown voltage rating of a 1-ohm, 100-volt device, for example,



2. Test circuit. The test circuit (a) should be used to accurately measure the switching time of a power MOS FET. The resulting switching waveform is shown (b). Note that the actual switching waveform of Fig. 1 is different because of FET capacitance effects.

Examining power FET structures

A host of different structures for power field-effect transistors exist, each with its own advantages and drawbacks.

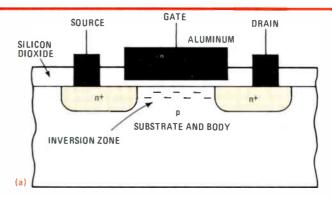
Planar MOS FET. Figure (a) is a cross section of a conventional planar n-channel enhancement-mode MOS FET. Fabrication begins with a p substrate into which n⁺ regions are diffused. A silicon dioxide layer is then grown and etched for later deposition of aluminum. The aluminum forms the source, gate, and drain connections. When no bias voltage is applied to the gate, the device acts as two back-to-back pn diodes and no conduction occurs. When the gate is made positive with respect to the source, an electrostatic field draws electrons near the surface of the p region, inverting it to an n region. A channel is thus formed, allowing conduction between source and drain.

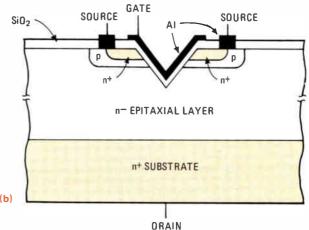
Since the MOS FET is a majority carrier device, it acts as an extremely fast switch with no storage time effects. However, a number of drawbacks eliminate this structure from practical consideration for high-power use. For one, the length of the channel is controlled by the mask spacing of the n+ regions; because of the degree of accuracy of photomask technology, relatively wide spacing is needed. The wide spacing produces long channel lengths that increase the resistance for a given area of silicon. For another, source, gate, and drain conductors are on the same surface, and their metalizations take up a major portion of the die area, further increasing the onresistance. Finally, the planar structure has large inherent capacitance, especially between gate and drain. These capacitances reduce the gain-bandwidth product and increase the drive power in repetitive pulse applications.

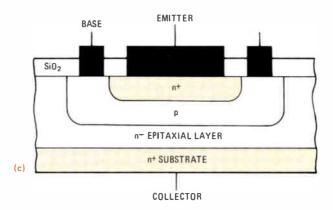
V-MOS. Most of the deficiences of the planar MOS FET can be overcome by a structure that allows the current to flow vertically and in which the channel length is controlled by diffusion processes rather than by mask spacing. The V-MOS structure shown in (b) is a particularly good solution. The fabrication process starts with an n+ substrate and an n- epitaxial layer. A p region is diffused in, followed by an n+ layer that is diffused within the p region. Up to this point, this process is very similar to that for a double-diffused non transistor, shown in (c). Instead of applying base and emitter metal layers, a V groove is anisotropically etched in the surface of the device. Then a silicon dioxide insulating layer is grown, and finally source and gate metal is deposited. Note that the source metal overlaps the p and n+ regions so that the base and emitter of the transistor are connected together.

By applying a positive potential between the gate and source, the p region close to the gate can be electrostatically inverted to n-type material and a conducting channel formed. Thus the source and gate connections are on the upper surface, the drain is on the bottom, and current flow is essentially vertical. In addition, the channel lengths are controlled by the diffusion processes and can be made very short. This structure allows very efficient utilization of the silicon and fabrication of high-power MOS FETs.

The structure in (b) has some drawbacks. The sharp bottom of the V groove produces a strong field concentra-







tion between the gate and drain. In addition, a tendency exists for the gate oxide layer to thin down around the tip of the V. The result is limited high-voltage capability because of gate-oxide breakdown, even though the gate does not see the full drain-source voltage.

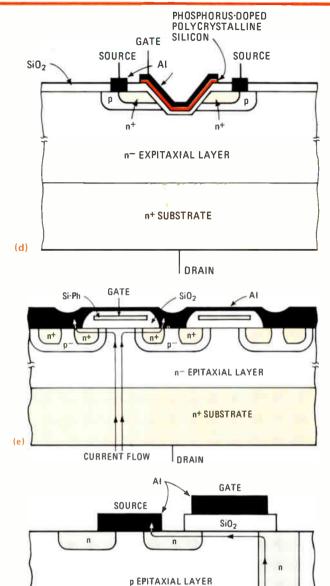
Another problem is the use of an aluminum gate, which can cause long-term reliability problems as a result of ion migration (principally sodium) through the gate oxide. Ion migration leads to variations in the device threshold voltage. Still another drawback is the channel formation. If the channel's groove does not penetrate well past the p region into the epitaxial layer, excessive current densities

is increased to 200 V, the device's die area would have to be at least five times larger for the transistor to maintain the same on-resistance.

There are two basic reasons for the exponential increase in on-resistance: the resistivity of the transistor's

epitaxial layer must be increased for higher avalanchebreakdown capability, and its thickness must be increased to ensure that the transistor's depletion region remains totally within the layer.

In a 400-v transistor, the resistivity of the epitaxial



can cause current-injected avalanche breakdowns.

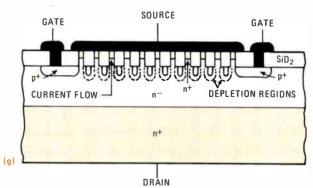
Most of these problems can be relieved by a structure with a flat-bottomed groove and a combined silicon and aluminum gate structure as shown in (d). Fabrication is very similar to that for V-MOS, except that the etching is halted while the bottom of the groove is relatively wide. A layer of oxide is then grown and overlaid with a layer of polycrystalline silicon doped with phosphorus.

n+ SUBSTRATE

DRAIN

CURRENT FLOW

Phosphorus-doped polysilicon is an effective ion-migra-



tion barrier but not a particularly good conductor, having a resistance about 3,000 times that of aluminum. In a large device, this resistance could lead to a slow turn-on time and reduced dV/dt capability. Therefore a layer of aluminum is applied over the silicon gate for high conductivity. The silicon-gate process, which Intersil uses for V-MOS, also increases yield, lowering the device cost.

Vertical D-MOS. Although the modified V-MOS process of (d) is very effective for voltages under 150 volts, voltage-gradient problems still exist, and the groove spacing requirements increase the die area. A vertical D-MOS (double-diffused MOS) structure, shown in (e), alleviates these problems. The process begins as for an n-channel device, with an n⁻ epitaxial layer grown on an n⁺ substrate. P⁻ regions are then diffused; and inside these, n⁺ regions. Next, a silicon gate is imbedded in silicon dioxide and the source and gate metalization are then added. The current flow is at first vertical and then horizontal, with the drain on the n⁺ substrate.

This structure has a number of different names, among them, D-MOS, T-MOS, Z-MOS, and HEX FET. The processes used to make them are basically the same, the primary differences being in the geometry of the p and n regions and the interconnections. The HEX FET, for example, uses hexagonal p regions, which allow a very low on-resistance by maximizing the channel perimeter. Unfortunately, as currently implemented, the silicon-gate structure has a relatively high series resistance, which increases the switching time significantly. An alternative geometry used in Intersil's power devices retains the low on-resistance but reduces the gate resistance.

Hitachi Ltd. has developed a MOS FET in which the gate structure overlays a checkerboard of n and p regions to form the channels, and the n regions connect to the n+ substrate so that the drain is on the back side of the die (f). To date, devices using this structure display a restricted gain-bandwidth product of 0.6 to 1.5 megahertz and a relatively high r_{DS(on)} for a given die area.

Sony Corp. makes a vertical depletion-mode junction FET that it calls a V-FET. It has a square-law transfer characteristic (g). Its disadvantages are a relatively low stage gain, substantial gate current if the gate is driven positive, and relatively high gate resistance and input capacitance that reduce the gain-bandwidth product.

layer is typically 1,500 to 2,000 times greater than that of the n⁺ substrate. At high voltages, therefore, the transistor's on-resistance is dominated by the resistance of the epitaxial layer. Thus for a given MOS or bipolar transistor die area, an increase in the transistor's break-

down voltage means a decrease in the device's powerhandling capability. If the power capability is to be retained for a higher breakdown-voltage rating, a large die area is needed.

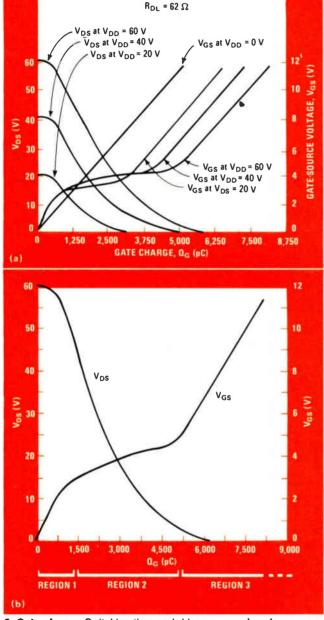
The large die area is a double-edged sword. The larger

it is, the lower the on-resistance, since the latter is inversely proportional to the die area. However, that also means fewer dice per wafer. This last fact, combined with dice losses due to inherent wafer defects and an increased scrap zone around the wafer's center and periphery (for a given larger die), means lower wafer yields and therefore higher costs. The yield can typically be represented by the relationship:

$$Y = K(n) (1 - e^{AD})^2 / AD$$

where:

A = the die area



3. Gate charge. Switching-time and drive-power values for a power MOS FET are accurately calculated from a knowledge of the FET's gate charge as a function of its gate-source voltage (a). For simplicity, the curves for a drain supply of 60 V are reproduced (b).

D = the defect density

n = the number of process steps

K= an exponential factor that varies inversely with n For small die dimensions of less than 0.050 by 0.050 inch, yields are usually very high and die costs low. As die dimensions exceed 0.100 by 0.100 in., yields decrease rapidly and die costs escalate. Many power-transistor die dimensions are usually larger than those mentioned, accentuating the yield and subsequent cost problems as devices with a lower on-resistance are made. A 450-v transistor with $1-\Omega$ on-resistance, for example, may cost four to six times as much as a transistor with 2.5- Ω on-resistance and the same breakdown-voltage rating.

Most MOS power transistors are n-channel devices. Although p-channel devices can be built just as easily as n-channel ones by the simple interchanging of n- and p-channel regions, there is a difference in their performance compared with n-channel MOS FETs.

In n-channel MOS FETs, the majority carriers are electrons, while in p-channel devices the majority carriers are holes. Since holes have about one half the mobility of electrons, p-channel on-resistance for a given device is about twice as high as that of an n-channel structure, unless about twice the n-channel's area is used in a p-channel structure. A larger p-channel structure means more capacitance and a higher cost than does an equivalent on-resistance n-channel one.

MOS FETs-ultrafast switches

A major advantage of a power MOS FET over a bipolar power transistor is its ultrafast switching speed. If the gate capacitance of a MOS FET could be charged instantaneously, switching times of 50 to 200 picoseconds would be possible. That is the time it takes for the transistor's majority carriers to travel from the device's source to its drain terminal. In fact, production MOS FETs can be switched in less than 1 nanosecond, provided a suitable pulse source is used to drive the transistor's gate terminal. Such a pulse source can include a mercury-wetted relay and a transmission line.

In practice, switching times of 10 ns or more are fairly easy to accomplish, limited primarily by the source resistance of the drive circuit. For shorter switching times, the transistor's package inductance, the internal gate resistance, and the pulse-generator source's connections become more limiting factors. It is difficult, for example, to attain switching times under 2 to 3 ns for power transistors packaged in commonly used TO-3 cases.

Switching waveforms

Figure 1 shows the switched waveform for an Intersil IVN5200 power MOS FET switching 60 v at 8 amperes and using the test circuit and waveform shown in Fig. 2. The slightly positive voltage rise at turn on is due to the coupling of the drive pulse to the output by the reverse transfer capacitance, C_{rss} , during the turn-on delay time. A similar negative pulse can occur during the turn-off delay time.

The delay at turn on is due to the length of time it takes for the gate voltage to rise to $V_{GS(th)}$, where the device begins to conduct. In most switching applications,

sufficient gate drive will be supplied to obtain the minimum $r_{DS(on)}$. (This corresponds to the area in Fig. (e) ("Linear characteristics—a closer look," p. 151, where r_{DS} changes relatively slowly with V_{GS} .) The result is a turn-off time delay where V_{GS} has to drop significantly before r_{DS} begins to rise.

Gate capacitance is nonlinear

Switching-time and drive-power calculations for power MOS FETs tend to be inaccurate when computed from small-signal input capacitance and source-resistance values. That is because gate input capacitance is highly nonlinear. A more accurate method of calculating a MOS FET's switching-time and drive-power values can be derived from a knowledge of the MOS FET's gate-charge behavior as a function of the transistor's gate-source voltage. Fig. 3 shows this behavior for an IVN5200 MOS FET, which is driven from a current source whose output is integrated to derive the charge.

As can be seen, the MOS FET's dynamic input capacitance is different for three distinct gate-source voltage regions. Take the curve where the drain supply voltage is 60 V. The first region exists between a gate-source voltage of 0 V to a threshold value (a charge of about 1,100 picocoulombs). In this region, the MOS FET is essentially off. The relative linearity of the gate-source voltage's rise indicates that the capacitance is fairly constant.

Regions two and three

As the gate-source voltage is increased, the curve enters the second region, in which a large increase in capacitance occurs. In this region, the drain-source voltage is falling and the Miller effect takes place, being bounded by charge values of approximately 1,100 to 4,800 pC.

In the third region, above 4,800 pC, the slope of the gate-source voltage curve begins to increase again, although not quite as much as in the first region. Again, the slope is relatively linear. In this region, the MOS FET is on and the transistor's drain-source voltage is no longer changing. No Miller effect is present here.

A knowledge of gate-source voltage and capacitance values for each of the MOS FET's three regions allows the circuit designer to calculate the input capacitance for each of these regions.

As for drive-power requirements, the energy, W, needed to turn the MOS FET on is defined as:

$W = \frac{1}{2}V_GQ_G$ watt-seconds

where V_G is the gate voltage and Q_G is the gate charge.

If the MOS FET's gate is driven on and off repetitively from a resistance source at a rate f_0 , then the drive power is:

$$P = Q_G V_{GS} f_0$$

At a V_{GS} of 10 v and a switching rate of 100 kilohertz, 7.5 milliwatts of drive power would be required for an INV5200. That is a vast improvement over a comparable bipolar transistor.

For a power semiconductor device to perform satisfactorily, the circuit designer must make sure that the

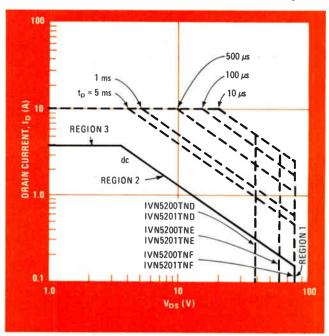
device is operated within its voltage, current, and thermal ratings. Generally, power-device manufacturers provide the device's maximum ratings, a safe-operating-area rating (SOAR) curve, and a thermal-impedance curve. However, a maximum-rating table of values by itself is insufficient, and unfortunately, that is all that some manufacturers supply.

More than the ratings

As can be seen in Fig. 4, the SOAR curve for a MOS FET has three boundary regions. Region 1 is defined by the MOS FET's breakdown-voltage capability. Region 2 is defined by the device's thermal capability, where a junction temperature of 150°C maximum is normally specified. This limits the power dissipation to a peak junction temperature of 150°C. Higher peak powers can be defined from a family of thermal curves for shorter pulse widths. Region 3 is defined by the device's current-handling capability.

The current-handling capability of a MOS FET is limited by the diameter of its bond wire, the area of the bonding pad on the die, and the metalization on the die surface. Although breakdown-voltage and junction-temperature limitations for a power transistor can be determined readily by direct measurement, current limitations are derived empirically from life testing. The maximum current is limited to a value that has been found to give an acceptable service life.

In a bipolar transistor, there is a rapid decrease in h_{FE} —the transistor's common-emitter static forward current-transfer ratio—above its current ratings. In a MOS FET, however, the gain is not reduced at high currents. For fast-pulse applications where a high drain-source voltage is acceptable, the temptation may exist to operate the transistor with very short high-current pulses



4. Safe operation. To adequately define a power transistor's safe operation conditions, a safe-operating-area rating (SOAR) curve is necessary. For a MOS FET, this curve has three boundary regions: for breakdown voltage, thermal capability, and current capability.

in excess of the ratings. Doing so is inadvisable for two reasons, even if the device's power dissipation is low. First, the device's reliability or service life is likely to be shortened. Second, for sufficient increases in current densities, it is possible that current-injected avalanche breakdown could occur and cause the destruction of the transistor.

For a bipolar transistor, the SOAR curves include a fourth boundary region, defined by the thermally induced secondary breakdown characteristics of the transistor. There are several ways of inducing secondary breakdown in a bipolar transistor. One way is by lateral thermal instability. When the temperature of a hot spot on the transistor is sufficiently high, the transistor's impedance is reduced drastically, funneling the collector current through a small area. This leads to eventual destruction of the device.

Another way is by avalanching. When the transistor's collector voltage is raised to the breakdown point of the collector-base junction, a very large current flows, causing the device to go into secondary breakdown.

MOS FETs have wider breakdown regions

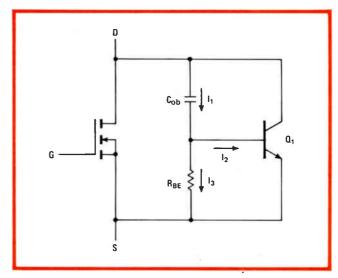
It has been widely advertised that MOS FETs do not exhibit secondary breakdown. This claim is not true. It is true that the thermally induced secondary breakdown phenomena so prevalent in bipolar devices is *not* present in MOS FETs, but avalanche-induced secondary breakdown is.

A MOS FET structure contains an npn transistor. The voltage limit of the this transistor is its base-collector junction breakdown voltage. Its base-emitter resistance, temperature, and h_{FE} all determine the current level at which primary breakdown becomes secondary breakdown.

In a MOS FET, the npn transistor's base and emitter terminals are shorted together on the die, so as to yield the least base-emitter resistance. Minimizing this resistance improves the MOS FET's drain-source dV/dt characteristics. Furthermore, the $h_{\rm FE}$ of a MOS FET's parasitic bipolar transistor is much lower than that of a conventional bipolar transistor. The net result is a higher current level at which secondary breakdown occurs compared with a bipolar transistor.

MOS FETS have maximum drain-source voltage ratings that are well below the actual breakdown point, so that voltage avalanche breakdown is not usually a problem. Theoretically, the current-injected avalanche breakdown present in bipolar transistors during reversed-bias operation can also lead to secondary breakdown in MOS FETs. For a given field gradient within a transistor, a maximum current-density threshold exists above which selfsustaining avalanche breakdown occurs. That threshold is the basic current-handling limitation of any power transistor. For MOS FETs, internal current densities are limited by design, so that the junction-temperature thermal limit is reached well before any current-injected avalanching is present. Since the thermally induced and avalanche-induced breakdown limits lie well outside the published SOAR curves, neither one is of direct interest to a user.

Typically, the SOAR curve for a bipolar transistor or a



5. Equivalent. A MOS FET contains an inherent bipolar transistor whose equivalent circuit and switching performance are shown above. This parasitic structure can impose a limit, through switchback effects, on the rate of rise of the FET's drain-source voltage.

MOS FET is plotted for a transistor case temperature of 25°C, for either dc or single-pulse operation. In reality, case temperatures often exceed 25°C and operation is often by repetitive pulsing. Therefore a user must modify the standard MOS FET SOAR curves to conform to the application at hand. Modification can be done by using the transient thermal-impedance, or $Z_{(th)}$, curve normally supplied by the MOS FET manufacturer.

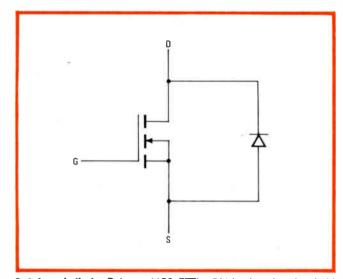
Bipolar structure limits MOS FETs

The bipolar transistor structure within a MOS FET can impose a limit on the rate of rise of the MOS FET's drain-source voltage, V_{DS} . Figure 5 shows an equivalent circuit of a parasitic bipolar transistor, Q_1 , in parallel with a MOS FET. Even though the MOS FET's source metalization connects the n^+ and the base p regions at the die's surface, a significant amount of base-emitter resistance, R_{BE} , exists due to the bulk resistance of the n and p regions. Furthermore, there is capacitance C_{ob} caused by the collector-base junction.

When the drain-source voltage undergoes a positive transition, a current flows through C_{ob} equal to $C_{ob}(dV_{DS}/dt)$. As V_{DS} rises more rapidly, more current flows through C_{ob} until a point is reached where the voltage across R_{BE} is sufficient to turn on Q_1 . This undesirable turn on, or switchback, interferes with the normal circuit operation of a MOS FET and can possibly destroy it.

The threshold for switchback varies from one MOS FET device type and manufacturer to another. Maximum dV_{DS}/dt information is not yet a standard item of information on most MOS FET data sheets. Thus a user must consult with the device's manufacturer or test the device to determine his parameter. For Intersil's IVN 5000 and 5200 MOS FETs, dV_{DS}/dt ratings are at least 20 V/ns.

The dV_{DS}/dt rating for a MOS FET can be improved by designing the FET's die layout for minimum R_{BE} and by controlling the doping of the p region to produce a bipolar transistor with low h_{FE}. In any parasitic bipolar



6. Internal diode. Below a MOS FET's dV/dt triggering threshold level, the internal bipolar npn structure is inactive and acts as a device with shorted emitter and base terminals—an equivalent circuit is shown above—allowing an FET to be used as a diode.

structure, h_{FE} is a function of the transistor's temperature. The dV_{DS}/dt switchback threshold decreases with increasing temperatures.

Using the internal diode

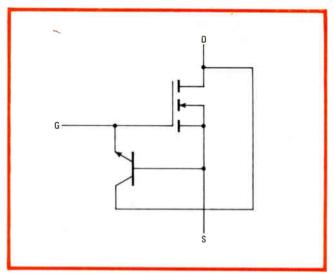
When the MOS FET's V_{DS} rise time is below the threshold of the switchback level, the internal parasitic npn bipolar transistor is inactive and acts as a transistor whose base is shorted to its emitter. The equivalent circuit shown in Fig. 6 is that of a diode in parallel with an ideal MOS FET. If V_{DS} is reversed, the diode conducts and can thus be used as a rectifier or as an inductive energy clamp in switching circuits. The diode's forward-current and breakdown-voltage ratings are equal to those of its parent MOS FET.

Reverse-recovery time for the diode can be very fast. For example, in the IVN5000 and the 5200 MOS FETS, it is typically 60 to 70 ns. This rapid reverse-recovery time is a function of the MOS FET's fabrication process and can vary widely from manufacturer to manufacturer. During fabrication, lightly doped epitaxial diodes with sharply defined doping gradients are produced. In addition, when a p region is formed by ion implantation, dislocations are caused in the semiconductor's crystal structure. These dislocations act as recombination centers for the stored junction charge and speed up reverse-recovery time.

Like maximum dV_{DS}/dt values, reverse-recovery time data is not normally found on MOS FET data sheets. Again, users are advised to seek this information from the device's manufacturer.

Synchronous rectification

A MOS FET can also be used as a synchronous rectifier. When the gate-source voltage, V_{GS} , is positive, current will flow through the FET in either direction with equal facility. For synchronous rectifier operation, V_{GS} is zero when the drain is positive with respect to the source. When V_{DS} reverses, the FET's gate is energized and



7. Protection. The first V-MOS power devices on the market included an on-chip zener diode from gate to source terminals, to prevent gate breakdowns caused by static charging. Newer MOS FET power devices are more rugged and do not require this on-chip diode.

current flows through it in the reverse direction. The forward voltage drop is proportional to the FET's r_{DS(on)} and the current flowing. When the threshold level of the parallel diode is reached, current bypasses the FET channel and the rectifier acts like a conventional pn junction diode.

For currents that keep V_{DS} under the 0.6-V diode threshold, the FET acts as an ultrafast high-voltage and low-capacitance rectifier with no minimum offset voltage. Such behavior is useful for employing the device as a power rectifier up to 15 megahertz. Currently available MOS FETs can be used in this manner, with the only drawback being a relatively high $r_{DS(0n)}$ value that restricts the amount of useful current. Future MOS FETs are likely with low-voltage and low- $r_{DS(0n)}$ characteristics, specifically designed for this type of service. Such characteristics will make possible the switching of large amounts of power efficiently for 2- to 5-V loads.

Internal zeners are no longer needed

The first MOS FETs on the market using V-groove structures included on-chip zener diodes connected from gate to source terminals. The diodes prevented gate breakdowns due to static charging. Each diode was formed by diffusing in an additional npn transistor, with the zener action being accomplished by the reverse breakdown of the npn bipolar transistor's base-emitter junction (Fig. 6).

The on-chip diode has a number of drawbacks. For one thing, its ability to handle no more typically than 2 milliamperes severely limits the FET's power dissipation. In addition, when the FET's gate is pulled negative to -0.6 V or more, the npn transistor turns on and draws current from the drain circuit, which can destroy the transistor. The result is poor device reliability.

On the other hand, experience has shown that the gate structure of a discrete power MOS FET is much more rugged than that of a small-signal MOS integrated circuit. Given reasonable care in packaging, handling,

Linear characteristics—a closer look

The output characteristics of MOS field-effect transistors differ from those of bipolar power devices. For a given die area, the total power loss of a MOS FET is greater than that of a bipolar transistor at frequencies below 20 kilohertz. Above 20 kHz, the power loss of the latter becomes much greater than that of the former. The differences can be seen, for example, from the behavior of an Intersil IVN5200 power MOS FET, where the on drain current, Io, is shown as a function of the drain-source voltage, VDS, in (a) and (b).

Two distinct regions of operation are apparent, a linear region and a saturated one (for bipolar devices, the definitions of these regions are almost exactly opposite). In the linear region (where V_{DS} is approximately equal to 0 to 5 volts), the voltage across a MOS FET's channel is not sufficient for the carriers to reach their maximum drift velocity or their maximum current density. In this region, the FET operates as a square-law device; the static drain-source resistance, $r_{\text{DS}(on)}$, is equal to V_{DS}/I_0 at each point, and the small-signal drain-source resistance, $r_{\text{ds}(on)}$, is the slope of the transfer curve.

Ås V_{OS} is increased, the carriers reach their maximum drift velocity and the device enters the saturation region, where the output impedance is high (the curves are relatively flat) and the equal spacing between the curves for the gate-source voltage, V_{OS} , is an indication of constant transconductance, g_m . In this region, the transfer function is linear.

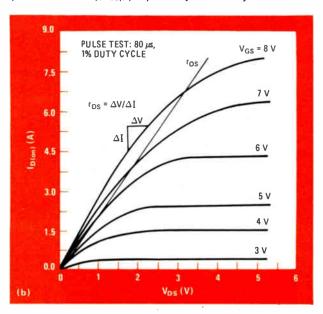
The output conductance, g_{os} , of an INV5200 is relatively independent of temperature. Its transfer characteristic is shown in (c).

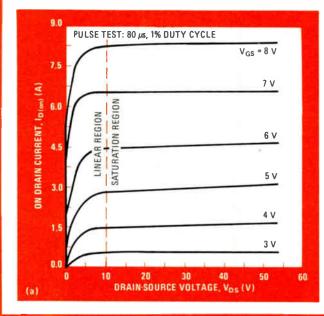
V_{GS(th)} is defined as the gate voltage at which some small current, usually 1 to 10 milliamperes, depending on device size, begins to flow. It varies as a function of temperature. Typically, an IVN5200 exhibits a temperature coefficient of 6 millivolts/°C.

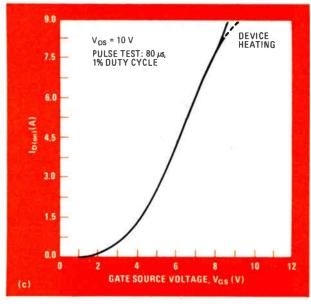
For switching applications, the temperature dependence of $V_{\text{GS(th)}}$ is not very significant. However, for linear applications, the MOS FET's bias point may need to be stabilized by the use of a source resistance or other negative-feedback scheme in order to keep this temperature dependence at a minimum.

A characteristic of short-channel MOS FETs is that, for a given V_{DS} , transconductance increases with I_{DS} until a point is reached where it becomes constant.

Drain-source on-resistance. A MOS FET's r_{DS(on)} is made up of two components: the channel on-resistance and the bulk device resistance. In low-voltage devices (less than 100 V), r_{DS(on)} is primarily caused by the channel







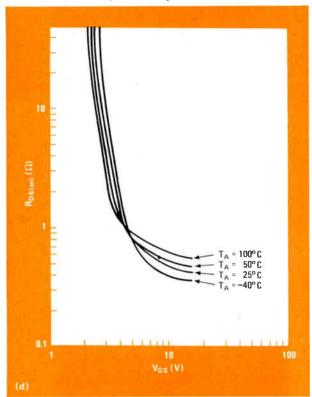
and installation, there is no need for an internal zener diode in most applications.

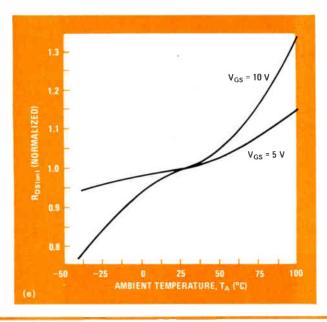
The positive temperature coefficient of a MOS FET's

r_{DS(on)} is useful when these devices are operated in parallel with each other. It is possible to parallel MOS FETs, without any matching, in dc applications; the device that

resistance. In higher-voltage devices, however, the minimum $r_{\text{DS(on)}}$ value is domimated by the resistance of the epitaxial layer.

Figure (d) shows how channel resistance is controlled by the degree of device gate enhancement. On-resistance can be decreased by increasing V_{cs} to about 15 V.





A point of diminishing returns, however, sets in, so that little is gained by increasing the gate-source voltage much above 15 V. It is also important not to approach the gate breakdown voltage in the quest for a low $r_{DS(on)}$. For MOS devices with higher $V_{GS(th)}$ levels, the curve in (d) will be displaced to the right, but the shape remains essentially the same.

The effect of temperature on $r_{DS(on)}$ at different values of V_{CS} is shown in (e). Note that the temperature coefficient of $r_{DS(on)}$ is positive, which is a major reason why a power MOS FET has an improved safe operating area over bipolar power transistors and can be easily paralleled. This positive coefficient, which is caused by the competitive effects of a positive temperature coefficient of silicon and a negative temperature coefficient of $V_{CS(th)}$, varies in value between +0.2% and +0.7%.

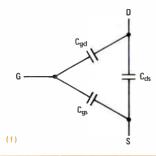
As shown for $V_{GS}=5$ V, when V_{GS} is close to $V_{GS(ph)}$, threshold effects predominate. As V_{GS} is increased, the temperature coefficient begins to take on the positive characteristics of silicon. In devices with voltages of more than 80 V, r_{DS} is dominated by the device's bulk resistance and the temperature coefficient is more nearly linear, with typical values being +0.6% to +0.9%.

Capacitance effects. Like the bipolar power transistor, the power MOS FET has significant input, output, and transfer capacitances that vary with voltage. For example, capacitances exist between the gate structure and both the source and drain structures, known as C_{gs} and C_{gd} .

Also, the base-collector junction of the inherent npn transistor in the MOS device, a reverse-biased pn junction, contributes capacitance between the drain and source structures (C_{ds}). C_{ds} shunts the series combination of C_{gd} and C_{ds} as shown in (f).

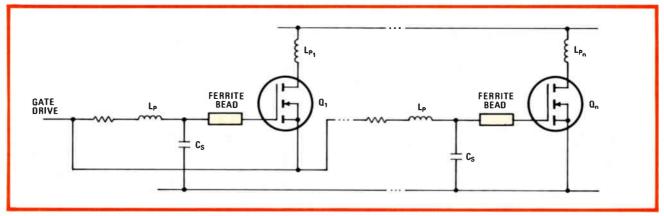
These three capacitances in turn result in C_{lse} , C_{rse} , and C_{ose} capacitances. C_{lse} is the parallel combination of C_{gd} and C_{gs} , C_{ose} is the parallel combination of C_{ds} and C_{gd} , and C_{rse} is the same as C_{gd} . Each of these varies with changing V_{DS} for a MOS FET, increasing very rapidly for V_{DS} under 10 V. For V_{DS} greater than 10 V, each of these capacitances decreases slowly at a nearly constant rate.

Since a MOS FET uses an insulated gate structure, its input current, I_{oss}, is normally very small—on the order of a few picoamperes—at room temperature. This current is made up of the leakage current through the gate structure and surface leakage current between the package terminals. Like any leakage current, I_{oss} increases exponentially with increasing temperatures.



initially draws the most current and consequently heats up shifts the current to other FETs, thereby distributing the current among the paralleled devices more equally.

Unmatched paralleling of MOS FETs is not recommended for dc applications, however, because a higher than necessary power dissipation level may occur. Mismatch-



8. In parallel. When power MOS FETs are operated in parallel, they tend to oscillate at very high frequencies, particularly if large numbers of them are paralleled. This tendency can be greatly reduced by inserting ferrite beads or resistors in series with the gate leads.

ing will also cause one FET to turn on or off before or after the other parallel FETs in switching applications and consequently one device may have to accept the full-load current. The FET may therefore function outside its SOAR and fail.

MOS FETs can operate in parallel

By matching the V_{GS(th)} levels of MOS FETs to within 5% of each other, paralleled operation is much more effective. This matching ensures that the turn-on and turn-off delays, due to the gate-voltage rise and fall time relative to V_{GS(th)}, are nearly equal. This will also ensure the matching of each FET's r_{DS(on)}, eliminating excessive differential heating of the FETs. By providing a higher V_{GS} drive potential so that all of the paralleled FETs operate at their minimum r_{DS(on)} values, the effects of mismatching are further reduced.

Keep in mind that many MOS FETs have gain-bandwidth products in excess of 500 MHz and therefore can oscillate at very high frequencies, particularly when many of them are paralleled. Such oscillations are often unsuspected causes of device failures. These oscillations can be reduced significantly by the insertion of low-value resistors (50 to 100 Ω) or ferrite beads in series with the gate leads of the FETs as shown in Fig. 8.

Symmetry needed for fast pulses

For MOS FET applications in fast-pulse circuitry, simply matching the transistors for parallel operation is inadequate. The circuit must also be reasonably symmetrical, so that identical drive voltages are applied to each FET gate. At high speeds, inductive as well as resistive effects of circuit components must be considered. For example, for proper circuit operation, the drain leads of FETs Q_1 and Q_n in Fig. 8 must have parasitic inductance values that are close to each other. If the parasitic inductance value for Q_1 is much smaller than that of Q_n , then most of the current will flow through Q_1 when the FETs are first turned on, even though the gate drive and threshold voltages of both may be identical.

Variations in the gate-circuit stray capacitance and the FET's input capacitance can also cause uneven FET turn on in this type of application. For switching times of less than 10 ns, it may be necessary to match FET capacitances. Nevertheless, in most applications, switching occurs well above 10 ns, where simple matching of FET threshold voltages is all that is needed for proper parallel operation.

For bipolar transistors, paralleling more than two devices can become a complex and expensive affair. It is for this reason that manufacturers are developing single-device bipolar transistors (as well as silicon controlled rectifiers) that handle more power. Obviously, making a device larger means increasing its die size. And as the die size increases, a point is reached where either the thermal capabilities of the case or the available mounting area for the die become limiting factors, so that a more expensive package may be necessary. These combined effects result in very expensive high-power bipolar devices.

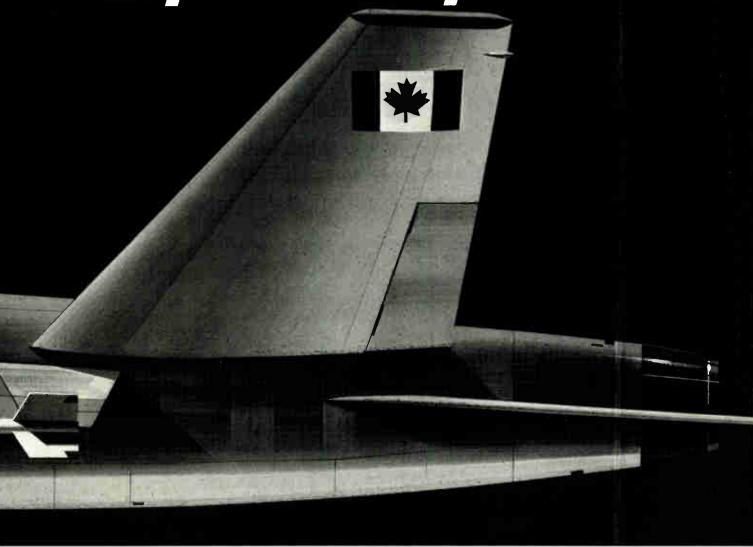
Multiple power devices or just one?

There are well-founded arguments for the use of a single bipolar power transistor instead of a number lower-power bipolar transistors that add up to the same power level. These arguments however, do not necessarily follow for power MOS FETS, since they do not behave as bipolar devices.

The tradeoff for MOS FETs may well be between multiple low-power devices with low die and package, as well as moderate heat-sink, costs and single high-power devices with high die, package, and heat-sink costs. But just where the crossover point between single and multiple devices lies has yet to be determined, and this calculation is complicated by the fact that larger-size MOS FET chips are expected to undergo substantial price reductions.

When using MOS power devices in series, other considerations are important. All power devices operating in series with each other should turn on simultaneously, with V_{GS(th)} and the gate drive for each device being matched closely. For applications where the maximum voltage capability is needed, it may be necesary to match the gate-source voltages closely, to ensure equal voltage distribution during switching transitions. The effect of parasitic capacitances for series-connected power devices is analogous to that of parasitic inductances for paralleled devices. Differential drain-source capacitances, either in a device or in a series of devices, leads to unequal sharing of transient voltages.

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Estimating the power coupled into an optical fiber

Nomograph yields values for butt joint using parameters supplied on data sheet

by Steven L. Storozum, McDonnell Aircraft Co., St. Louis, Mo.

Many engineers in communications, industrial control, and computers are thinking of including fiber optics in their designs. Initial evaluation is soon followed by the first attempt at a working system, which is often thrown together as quickly and inexpensively as possible. At this breadboard stage, light is usually fed into a fiber by simply butting the fiber up against a light-emitting or laser diode and clamping it there.

Here is a nomograph (Fig. 1) that provides a quick, easy way to determine graphically the coupling loss in a butt joint, from which the power coupled into the fiber may be calculated. The estimate relies only on specifications commonly made available on manufacturers' data sheets fordliodes and fibers.

The data sheet for a given diode lists its light-power output, but the manufacturer cannot specify the power coupled into a fiber because of the wide variety of fibers available. To get the coupled power, designers generally resort to measurements made with an optical power meter. The nomograph, however, can be used before the parts are over in hand.

Safety factor

The engineering assumptions made in the nomograph's derivation lead to conservative estimates of coupled power. These estimates in turn promote conservative preliminary system design. In a final design, techniques more sophisticated than simple butting are used to couple more power into the fiber.

These ttechniques include the use of lenses, indexmatching fluid, and antireflective coatings to enhance coupling efficiency. All are used in the final packaging of light-sources and fibers. The nomograph does not take final-design techniques into account: it is meant only for a worst-case analysis.

Using the light-power output figure quoted on the diode manufacturer's data sheet, experience shows, is reasonable in practice—deviations have little effect on the nomograph's accuracy. It is assumed that all the power specified is emitted from the front of the diode where the butt is made. Any other assumption would involve takking into account too many unknown or uncontrollable factors.

It is also assumed that the diode is perfectly butted to

the fiber so that the air gap between them is infinitesimal. Again, assuming otherwise is impractical; in any case, a gap variation makes little difference as long as it is small.

It should be noted, however, that the nomograph assumes the use of step-index optical fiber. If dimensionally similar graded-index fiber is used, the power loss will be about 1 decibel greater than the nomograph indicates.

A geometry problem

It is also assumed that the fiber core is centered on the emitting area of the light source. Centering is easy to do in practice. It is then an exercise in plane geometry to calculate the area of overlap between fiber and diode in the three cases of interest.

The first two cases are elementary. If the fiber core area encloses the emitter's active area (A_e) , the shape of the emitter is of no consequence and the overlap area (A) is equal to A_e . Conversely, when the emitter's active area encloses the fiber core area (A_f) , the emitter's shape is still of no concern, and the overlap area equals A_f .

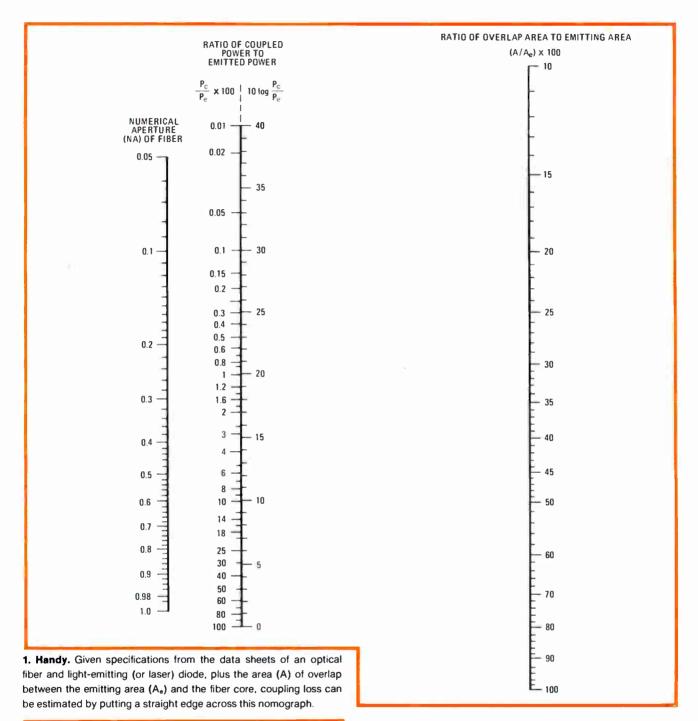
The third case arises with a rectangular emitter area (which most diodes have) that is longer than the fiber's diameter. The overlap area A, in this case, is found by calculating the approximate area of the intersection of the emitting rectangle and the circular cross section of the fiber (Fig. 2):

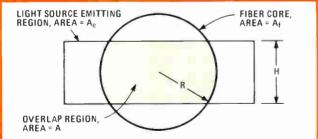
$$A = (H/2)(4R^2 - H^2)^{1/2} + 2R^2 \arcsin[H/(2R)]$$

wnere R is the fiber's radius and H is the height of the active emitting area. As the ratio of H to R grows very small, A approaches 2HR.

All of these dimensions are readily available from the manufacturers, as is the numerical aperture (NA) of the fiber used in the nomograph estimation. After overlap area A is calculated, the ratio of A to A_e is determined and the point on the nomograph's right-hand scale found. A straight line through this point and the point on the numerical aperture scale at left crosses the center scale at a point indicating the ratio of coupled power (P_e) to emitted power (P_e).

The results are helpful in computing tradeoffs in an optical fiber system. For example, trading numerical





2. Overlap. The portion of the light source's active emitting area that actually butts up against the fiber must be found to use the nomograph. The emitter is often rectangular; if it is longer than the fiber's diameter, overlap area (A) must be calculated by plane geometry.

aperture for fiber core diameter can be done to find the optimum fiber from the standpoint of coupling loss.

Suppose a step-index fiber with 0.25 NA and an A/A_c ratio of 0.4 is assumed as the first guess for some system. The nomograph indicates that a coupling efficiency of about 1.2% (19 dB loss) can be obtained. This may be satisfactory, but a fiber with a 0.3 NA can achieve the same efficiency with a more practical A/A_c ratio of 0.28.

This example illustrates the usefulness of fibers with large numerical apertures given a specific coupling-efficiency requirement. Of course, the bandwidth of source and fiber must also be considered during preliminary design, but these factors can also be estimated rapidly [Electronics, Nov. 23, 1978, p. 135].

Engineer's notebook

Micromapped control system jumps on multiple flags

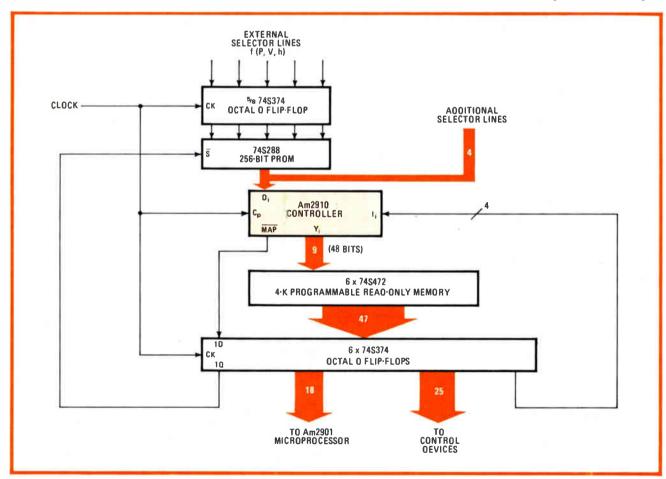
by Sorin Larnescu Teledyne Systems Co., Northridge, Calif.

Not even the most versatile of controllers, such as Advanced Micro Devices' Am2910, provides a microprogrammed system with the specific ability to select its next microinstruction as a function of more than one input variable. A viable system can be implemented, however, if programmable read-only memories and a few latches are added to the basic configuration, thus making it possible, for example, for the program to jump to any desired location for any given set of input conditions. Utilizing the input variables in this PROM-mapping scheme achieves the objective at minimum cost and without complex circuitry.

The hardware technique is illustrated for a 48-bit thermodynamic control system in which any of 32 combinational conditions of temperature, pressure, and humidity, as detected by the five address (external selector) lines, direct a microprogrammed routine to jump to a corresponding location. Thus the system is a barometer of real-time conditions, determining when the input variables constitute a serious but not hazardous state of affairs or, alternatively, when to shut down.

The states of the five external inputs are periodically latched into the 74S374 octal flip-flop by the system clock. This set of signals makes up the command address for the 74S288 PROM, whose 8-bit output drives the direct inputs of the Am2910 controller. The output of the controller represents the corresponding start address of the microprogram instruction cycle that is executed by the 74S472 operating memories.

If, under program control, any of the aforementioned 32 danger conditions should be detected by the controller, the corresponding microprogram will be run. By using the Am2910's arithmetic capabilities, the pre-



Expansion. PROMs and latches supply controller with the ability to select its next microinstruction as a function of a multiple set of input conditions. Monitored variables map input PROM for controller, whose output represents starting microinstruction address for 74S472 operating memory. Result of computation is passed on to the microprocessor, thus making possible program jumps or transfer of contents.

scribed actions may then be taken immediately.

An 18-line bus for controlling the microprocessor is required between the latches and the microprocessor to transfer 48-bit data. Four lines are dedicated to controlling the Am2910. Twenty-five control lines are made

available for closing mechanical relays, activating lamps, and so on. Execution time for each microinstruction is shortened by applying the map line of the controller, which bypasses the Am2910's internal pipeline register, to the 74S288's enable port via one output latch.

SCR controller keeps motor speed constant

by William Linkowski Copier Systems Division, Pitney Bowes Inc., Danbury, Conn.

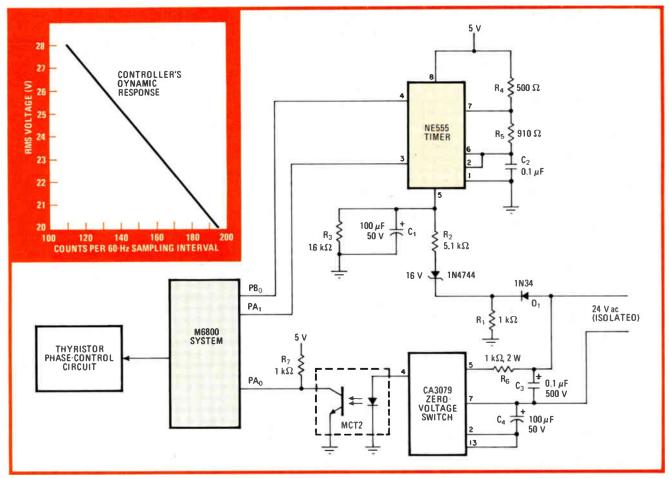
This microprocessor-based controller is a compact and relatively low-cost solution to the problem of adjusting a silicon controlled rectifier's firing angle to conform with variations in rms driving voltage in order to hold motor speed or light intensity constant. Use of an open-loop system also simplifies the circuitry considerably.

The technique is shown implemented in a standard SCR circuit driven with a 24-volt, 60-hertz ac line. Diode D₁ passes each positive half cycle of the line voltage to

pin 5 of the 555 timer through the zener, which fires when the incoming signal exceeds 16 V. Low-pass filter R₂-R₃-C₁ thus develops a dc voltage proportional to V_{in} for driving the timer, which operates as a voltage-to-frequency converter running at a center frequency of about 10.8 kilohertz.

Meanwhile, the CA3079 switch delivers a pulse to the PA_0 line of the 6800 microprocessor via the MCT2 optocoupler each time the input voltage passes through zero. This pulse initiates a counting interval of 16.6 milliseconds (one 60-Hz period) during which the 555's transitions at PA_1 are summed. The total count is thus proportional to the actual rms line voltage.

The typical rms voltage-to-count response is shown at the upper left (inset). The software relates this information to an internal look-up table that indicates the time increment correction needed to delay or advance the firing of the SCR to maintain motor speed.



Invariant. From monitored line voltage, microprocessor-based controller determines delay or advance-triggering time required for firing SCR in order to hold motor speed constant—independent of line variations. Software relates trigger time to a count that is proportional to the rms line voltage. Open-loop system, made possible by processor's look-up tables, simplifies circuitry considerably.

Sampling filters simplify converter's offset measurement

by Dennis Knowlton, National Center for Atmospheric Research, Research Aviation Facility, Boulder, Colo.

A microprocessor-based data-acquisition system has difficulty in making corrections for input offset and gain drift when it uses active filters to remove the effects of aliasing, or system noise. In such circumstances, the filters' frequency response and settling time vary as a function of the sampling rate and the magnitude of the input signal. However, the difficulties encountered with these sampled-data systems may be overcome by means of a switched aliasing filter, so that the anomalies in filter response may be virtually neglected and the offset and gain drift may be readily determined under software control.

In the typical input stage leading to the system's a-d converter, the noninverting ports of op amps A_1 and A_2 are periodically switched to ground and to a reference voltage so that the circuit can be isolated from all external stimuli and its inherent offset and gain determined. This scheme eliminates potentiometers and the requirement for precision components. It also leaves the measuring task to the software routine, where time and temperature have no effect on system accuracy, and where the data can be corrected for actual gain and

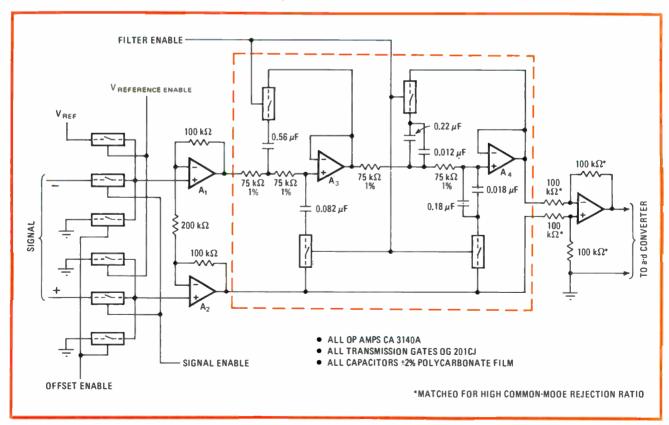
offset by means of look-up tables.

Because of sampling, however, the filter's frequency-domain response becomes a factor and thus a significant amount of signal data can be lost during the filter's settling time. Switching the filter out at a very slow rate compared with the signal sampling rate, and doing so at a low duty cycle, eliminates the problem.

The key to the success of the circuit lies in the fact that in the standard active filter, the only energy-storage elements are capacitors. Switching these elements out of the circuit periodically transforms the filter into one that has a very high cutoff frequency; thus the filter is essentially out of the circuit and its op amps' offset and gain drift can be easily measured. When the capacitors, which store the instantaneous value of the driving signal, are switched back into the circuit, they perform their basic filtering function. Thus, assuming the use of fast op amps, a high-speed a-d converter, and low-leakage capacitors in the filter, the signal-path response of the filter is unchanged; yet, offset and gain drift can be determined.

Shown in the circuit example is a simple four-pole filter built around A₃ and A₄ whose components are selected to reject aliasing noise at 10 hertz. Signal-path sampling is done at 50 Hz and capacitor switching at 0.1 Hz for a duration of 12 microseconds. The input and output stages of the circuit all utilize standard differential amplifiers.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.



Indeterminate. Aliasing filter A_3 - A_4 for data-acquisition system makes it impossible to ascertain input offset and gain drift unless it is itself of the sampling type. Filter's signal-path response will be unchanged, but stages' inherent imperfections can then be measured.

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Engineer's newsletter.

High-level math software for TRS-80 now available

Microsoft Consumer Products of Bellevue, Wash., has announced the availability of mumath, a symbolic math package that for the first time enables the popular TRS-80 microcomputer to do sophisticated mathematics. Developed by the Software Warehouse of Honolulu, Hawaii, it gives the TRS-80 the power to perform algebraic, trigonometric, calculus, and other symbolic math operations accurately and efficiently.

muMATH's capabilities include exact rational arithmetic and automatic algebraic simplification. Other talents include logarithmic simplifications and symbolic differentiation and integration. All operations are performed with a precision to 611 digits. The package requires a TRS-80 having a minimum of 32 kilobytes of RAM and a single disk drive. To take full advantage of its capabilities a 48-K system is needed. The muMATH package includes the muMATH diskette and complete instruction manual. Suggested retail price is \$74.95. For the name of the nearest dealer, contact MCP at 10800 Northeast Eighth, Suite 507, Bellevue, Wash. 98004, or telephone (206) 454-1315.

more electronic symbols . . .

Keeping engineers all over the world abreast of current electronic symbology, the International Electrotechnical Commission has recently issued Publication 148B, which contains the latest letter symbols agreed to internationally for semiconductor devices and microcircuits. The second supplement to Publication Standard 148, this manual contains over 100 letter symbols that apply to bipolar transistors, low-power signal diodes, voltage-reference and voltage-regulator diodes, thyristors, digital and analog integrated microcircuits, and current-regulator diodes.

. . . and receiver measurement methods, too

Also released is Publication 489-5, the fifth supplement to the standard used to specify measurement methods for radio equipment used in the mobile services, IEC Publication 489. IEC 489-5 deals specifically with radio receivers having audio-frequency bandwidths generally not exceeding 10 kHz for the reception of single-sideband signals. The new standards makes it possible to compare the measurements made by other observers on other equipment. The cost of Publication 148B is 32 Swiss francs, and that for 489-5 is 70 Swiss francs. Write the Information Officer, Central Office of the IEC, Geneva, Switzerland.

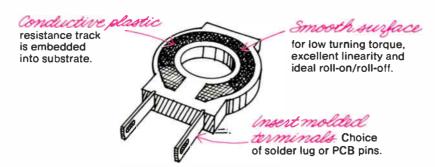
Op amp Integrator needs no capacitor

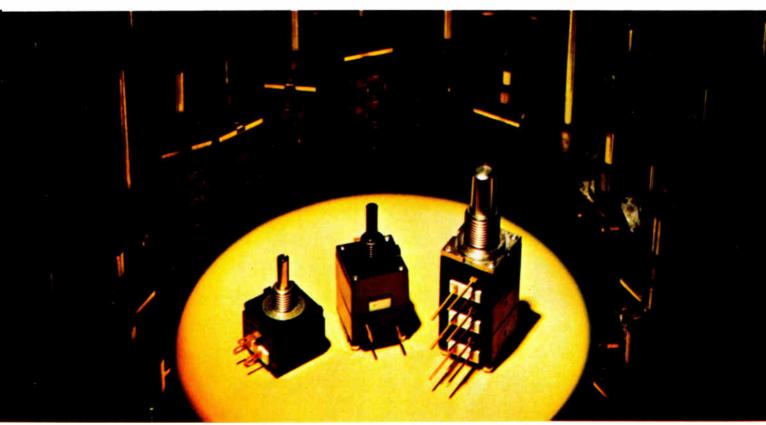
It's easier to utilize the inherent rolloff characteristics of an op amp to make an adjustable integrator than it is to adjust the values of the typical RC integrator's capacitor or to simultaneously vary its feedback and input resistor combination, says Angelo Pariani of Milan, Italy. Besides, he adds, the relatively high cost of the external capacitor can be saved.

The response of the typical inverting op amp integrator is $F(\omega) = (-R_f/R_i)/(1+j\omega CR_f)$, where R_f is the feedback resistor, R_i is the input resistor, and C is the integrating capacitor. But the frequency-dependent gain of the op amp itself is $A(\omega) = K/(1+j\omega/\omega_T)$ where K is a constant and ω_T the inherent cutoff radian frequency. As a consequence, an integrator can be formed with only R_f and R_i —no capacitor is needed. For if a potentiometer R_x is placed between the inverting input of the op amp and ground to select the cutoff frequency, the circuit's response will be $F(\omega) = (-R_f/R_i)/\{1+j\omega[(R_i+R_x)R_f+R_iR_x]/(R_iR_xBW)\}$, where the gain-bandwidth product, BW, is equal to $K\omega_T$.

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	434	25 MHz @ 10 mV/div	yes		20 ns/dlv	Split-screen storage
	314	10 MHz @ 1 mV/dlv	yes		100 ns/div	Only 10.5 lbs (4.8 kg)
	214	500 kHz @ 10 mV/dlv	yes		1 µs/div	Only 3.5 lbs (1.8 kg)
	T912	10 MHz @ 2 mV/div	yes		50 ns/div	Low-cost bistable storage
Nonstorage Models	485	350 MHz @ 5 mV/div	yes.	yes	1 ns/div	Widest bw in a portable
	475A	250 MHz @ 5 mV/dlv	yes	yes	1 ns/div	High-performance 250-MHz portable
	475	200 MHz @ 2 mV/div	yes	yes	1 ns/div	Highest gain-bw in a portable
	465B	100 MHz @ 5 mV/dlv	yes	yes	2 ns/div	Cost effective for 100-MHz bw
	465M	100 MHz @ 5 mV/dlv	yes	yes	5 ns/dlv	Triservice standard 100-MHz scope
	455	50 MHz @ 5 mV/div	yes	yes	5 ns/div	Cost effective for 50-MHz bw
	335	35 MHz @ 10 mV/dlv	yes	yes	20 ns/div	Only 10.5 lbs (4.8 kg)
	305	5 MHz @ 5 mV/dlv	yes		0.1 #s/dlv	Autoranging DMM
	221	5 MHz @ 5 mV/div			100 ns/div	Only 3.5 lbs (1.8 kg)
	213	1 MHz @ 20 mV/div			400 ns/dlv	DMM/Oscilloscope @ 3.7 lbs (1.7 kg)
	212	500 kHz @ 10 mV/dlv	yes		1 μs/div	Low cost for dual trace & battery
	T935A	35 MHz @ 2 mV/dlv	yes	yes	10 ns/div	Variable trigger-holdoff and differential
	T932A	35 MHz @ 2 mV/dlv	yes		10 ns/dlv	Delayed sweep and differential
	T922	15 MHz @ 2mV/dlv	yes		20 ns/div	Low-cost dual-trace scope
	T922R	15 MHz @ 2mV/dlv	yes		20 ns/div	Rackmount version of T922
	T921	15 MHz @ 2mV/div			20 ns/dlv	Lowest-cost TEKTRONIX Portable
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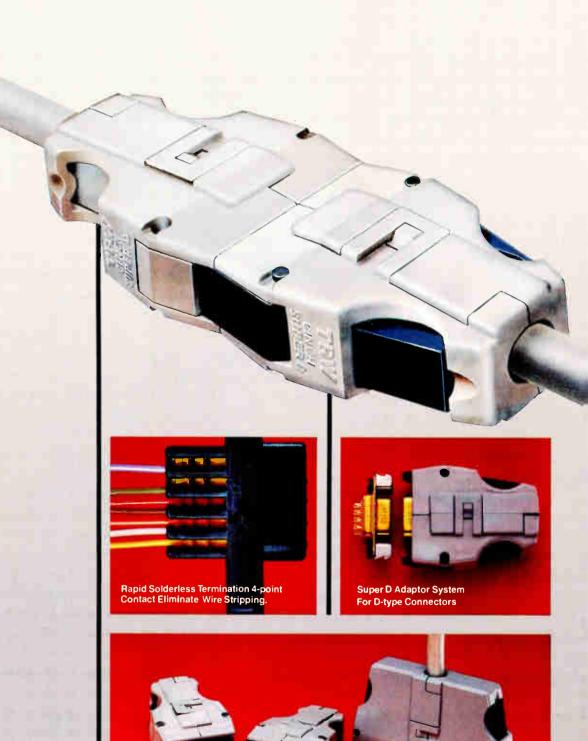
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Chip gives processors protocols

Two-channel communications controller presents 8080, 8085, and 8086 systems with bit- and byte-oriented protocols

by John G. Posa, Solid State Editor

The 8080, 8085, and 8086 microprocesors have, so far, been deprived of comprehensive, easily interfaced multiple-protocol serial communications. "There is basically a hole in these families of microprocessors for a high-performance multiprotocol chip," says Henryk Szejnwald, product marketing engineer at NEC Microcomputers.

The μPD7201, designed and manufactured by parent company Nippon Electric Co. of Tokyo, is a two-channel serial communications controller that supports asynchronous and synchronous byte-oriented data communications protocols like IBM's Bisync, as well as such synchronous bit-oriented protocols as HDLC and IBM's SDLC. Its data rate is software-programmable up to a 660-kb/s rate (with a 3-MHz clock) and, as expected, is intended to meet the needs of 8080-style and most other microprocessor systems.

Szejnwald is quick to admit that, with these qualifications, NEC's new 40-pin chip is not unlike Zilog Inc.'s SIO controller chip for the 8-bit Z80

microprocessor. But to use the Zilog part in an 8080, 8085, or 8086 system means an undesirable amount of superfluous hardware design and software programming. "Intel did a study and I think they concluded that it requires six extra ICs besides the large software overhead," says Szejnwald. He adds that the converse is a much different situation, however: "For somebody who has a driver written for the SIO, the switch [to the 7201] will be easy." This easy swap was taken into consideration when the 7201 was designed.

To achieve 8080 system compatibility, the new 5-V-only n-channel chip has different interrupt and direct-memory-access modes and read and write timing requirements than Zilog's SIO. Interrupt vector addresses and priorities are software-programmable, as is a flag that allows the device to meet the specifications of the 16-bit 8086 microprocessor. There are many other attributes under program control, too; indeed, NEC likes to say that the chip's "personality" can be opti-

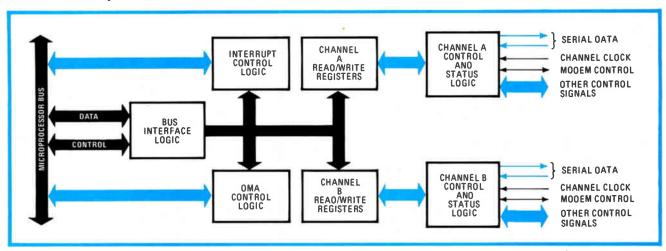
mized for the task at hand.

In fact, the chip can be used in applications beyond straight data communications. It can support virtually any serial protocol, according to NEC, and although both channels have built-in modem controls, these can be used for general-purpose input and output in applications without modems. For added faith in transmission, the 7201 can generate and test cyclic-redundancy-check codes in any synchronous mode and it can be directed to scrutinize data integrity in various modes.

Besides the two fully independent duplex serial channels the controller has four DMA channels. Transmitter data is double buffered and received data is quadruply buffered. The user may select between interrupt, DMA, or polling modes of operation.

The μ PD7201, samples of which are now being offered, will be available in the fourth quarter for \$40.00 each in quantities of 100.

NEC Microcomputers Inc. 173 Worcester St., Wellesley, Mass. 02181. Phone (617) 237-1910 [338]



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As soon as a new IC is introduced, GenRad writes new software for it. So when you're ready to use it, your tester is ready to test it.

We're also constantly

updating our component test systems. The minute a company introduces a new component, we start to work on the software. So by the time you're ready to use the new component, your GenRad tester is ready to test it. And that's true for both linear and LSI digital IC's.

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GenRad's Futuredata microprocessor development system is capable of programming and emulating—at full speed—all the popular microprocessors.

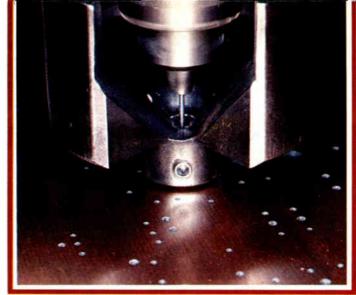
processors. And as new chips become popular, we'll have the new software to handle them.

Software-based testing. It's one reason GenRad's ATE systems don't get older. They get better.

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THE HOLE TRUTH

New GE Engineered FR-4. An advanced laminate designed to reduce drilling abrasion, improve thru-hole quality, and lower processing costs.

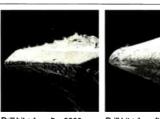
Now there's a PC board laminate with even better processing qualities than conventional FR-4. It's the new *Engineered* FR-4 epoxy-woven glass laminate from General Electric.

You can process Engineered FR-4 in exactly the same way as conventional FR-4, and tests by PC manufacturers have shown that you can enjoy improved yields and substantial productivity benefits.

The key to these benefits is a GE discovery: an exclusive epoxy adhesion promoter that greatly enhances the 3-D bonding of the epoxy resin to itself, and to the woven glass layers. The resulting uniform matrix gives the laminate much greater integrity than possible before.

As a result you can expect greater thermal shock resistance and reduced tendency toward delamination during processing. But the

opportunity for cost reduction is greatest in the drilling and plating-thru operations. Less abrasion encountered during drilling means reduced heat generation and longer drill life. This is illustrated in the 260X photomicrographs below. Note differences in tip sharpness and wear.



Drill bit edge after 9300 holes in Engineered FR-4

Driff bit edge after 9300 holes in conventional FR-4

Because there is less drilling abrasion and less heat generated, the quality of thru-holes is greatly improved. With Engineered FR-4, there is less resin smear, rifling, void formation; and fewer torn glass bundles. This in turn provides a superior, more uniform surface for electroless copper plating.

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GE LAMINATES: THE DIFFERENCE IS TECHNOLOGY



DEC introduces color terminals

Marking DEC's entry into color graphics, these display consoles cost under \$15,000 and operate with the PDP-11 and LSI-11 computers

by James B. Brinton, Boston bureau manager

The recent burst of activity among manufacturers of color cathode-ray tube monitors [Electronics, April 10, p. 153] was a warming-up exercise for the general movement toward color graphics among terminal and computer manufacturers. Current product introductions confirm a growing commitment to providing color for business and industrial uses at a reasonable price.

A family of display consoles from Digital Equipment Corp.'s Computer Special Systems group marks the firm's entry into color graphics. With its color displays priced under \$15,000, DEC's market strategy is clear, says product manager James E. Carroll. "We are pricing ourselves aggressively relative to the Ramteks and others in the market, and we are trying to offer more."

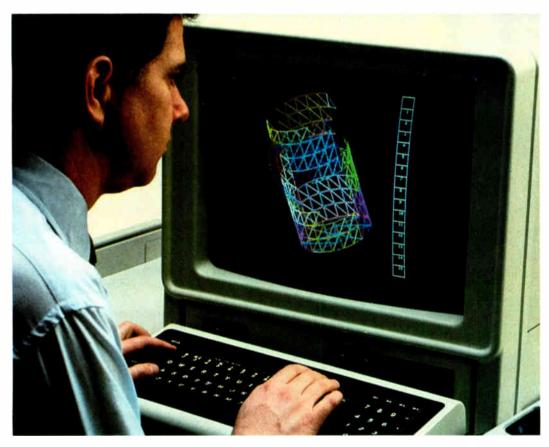
"Some vendors' products really offer little for their base price," he continues. "Users must add interfacing and color—sometimes at twice the original investment. We want to offer units a buyer can go on line with now, without hidden charges."

The model VS11 is designed to operate with DEC's PDP-11 series and VAX-11/780 Unibus-oriented

computers; the companion VSV11 works with the firm's LSI-11 computers. Both display types accept data from their host mainframes via direct memory access (the VS11 through a bus-converter subsystem), storing it in up to 1 megabit of image-buffer memory.

Software control. The monochrome versions of these displays yield 16 shades of gray on their 12-in. monitors; the color units offer 16 basic colors on 19-in. displays. Software control allows mixing the 16 colors to produce up to 256 tints.

To minimize host-processor over-



Graphics. Stress of complex cylindrical elements is displayed in full color on the DEC VS11 graphics subsystem using Patran-G software on the VAX-11/780.

New products

head, DEC has made the units almost self-sufficient. Aside from DMA requests and the consequent flow of data to the terminals, the host has little to do with display operation. Its role is limited to control over graphics parameters, gray scale, and color—much of it through software.

Running the displays is a 2901type bit-slice processor capable of executing 64-bit instructions in 160 ns. The display can thus be altered swiftly, a must for dynamic graphics applications. The display changes at about 640 ns per picture element. According to Carroll, this rate is "significantly faster than is possible with the serial-line graphics terminals on the market."

The speed comes partly from the units' DMA, bit-parallel input and partly from the fast processor control. At present, the limit is imposed by memory speed and the several modes that the memory must cycle through during operations, he says. The units use long-persistance phosphors, both in the color and the monochrome models, to eliminate fatigue-inducing flicker.

Resolution is good; the raster-scan systems generate more than 512 resolvable picture elements (pixels) per line across the face of the 19-in. color cathode-ray tube, and the CRT's spot size is about 0.7 mm. Resolution of the monochrome monitor also is 512 pixels per line. Convergence adjustments are unnecessary in the custom color unit, which has a three-gun, in-line design.

The VSV11 with a color-terminal option is base-priced at \$13,600; its monochrome counterpart costs \$7,900. The minimum-configuration price for the VS11 is \$14,200 for color and \$8,600 for monochrome. Deliveries begin in October.

Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754. Phone (617) 897-5111 [338]

Desktop computer has color display

HP's new computer system comes with a graphics monitor that offers 4,913 shades of color and a light pen that moves objects on the CRT display

by Bruce LeBoss, San Francisco regional bureau manager

Hewlett-Packard Co.'s system 45C is the latest and most powerful addition to the series 9800 family produced by HP's Fort Collins, Colo., Desktop Computer division. It constitutes a complete work station designed for engineers and scientists who must solve complex design and analytical problems. In addition to

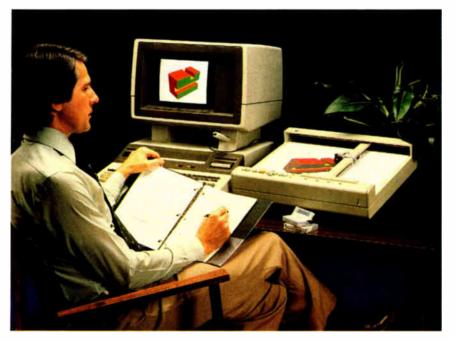
its operating system, read/write memory, Enhanced Basic language, keyboard, mass-storage system, and thermal line printer, the 45C integrates into a single desktop unit a sophisticated color graphics cathoderay-tube display and a novel light pen that enables the user to pick, move, and draw objects on the cath-

ode-ray tube interactively.

The system 45C's display features a 13-in. high-resolution shadow-mask CRT (560 by 455 picture elements, or pixels) that uses three electron-beam guns to activate triads of phosphor dots with red, green, and blue emissions. This technique provides the system 45C's eight basic colors—white, red, yellow, green, cyan, blue, magenta, and black (the eighth "color").

To provide 4,913 shades of color on the System 45C, HP engineers use a technique called dithering, Hale notes. Here the raster-scanned CRT is divided into four-by-four arrays of pixels. In every array, each of the 16 pixels can be turned either on or off, and the combinations of pixels being turned on and off in three different memory planes yields the 4,913 shades.

HP engineers developed a software-assisted color-convergence system that allows a user—with key-



Work station. Hewlett-Packard's system 450 desktop computer includes a high-resolution color CRT display and a light pen and offers the 9872 plotter as an option.

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New products

board commands, indicators on the CRT display, and 39 independent controls—to align the three electron-beam guns sequentially in 13 different areas of the CRT display and thus provide sharp colors across the entire display. Once convergence is adjusted, Hale says, the display can remain untouched for weeks to even months, depending on the operating environment.

The system 45C has eight "soft" keys located along the bottom of the display-screen bezel, each of which can be user-defined to show printed messages on the CRT display or to specify a color. The color commands allow the user to display alphanumerics and geometric figures simultaneously.

The light pen supplied with the standard system 45C is a graphics

tool that, using the system's tracking cursor, makes possible resolution down to the pixel level. The cursor can move at the same speed and direction as the pen.

Also, the system 45C's graphics statements—based on HP's Advanced Graphics Language—include, in addition to the 35 commands of prior system 45 machines, 35 new or enhanced commands to ease both the use of color and the light pen in graphics computation and interaction. With a single command, for example, the internal printer replicates the image in gray scale, or a color graphics package combined with HP's microprocessor-based 9872 plotter can provide the user with color hard copy.

The price for the standard system 45°C configuration is \$39,500 and includes the color CRT display and color graphics firmware, interactive light pen, 187 kilobytes expandable

to 499 kilobytes of user-available read/write memory, and two 217-kilobyte cartridge-tape drives and the internal (80-column, 480-line-per-minute) thermal printer. The operating system, as well as the functions for display, graphics, and control, is contained in 152 kilobytes of read-only memory, to leave the read/write memory entirely available to the user. Other ROMs are available for 1/O, mass-storage, advanced-programming, data-communications, and data-base management functions.

A streamlined entry-level configuration with only 56 kilobytes of read/write memory, one tape drive, and no light pen or internal printer is available for \$31,500. Delivery of either configuration takes 8 to 10 weeks after receipt of the order.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif., 94304. Phone (415) 857-1501 (339)

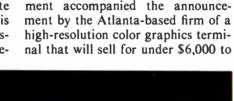
OEM color terminal costs under \$6,000

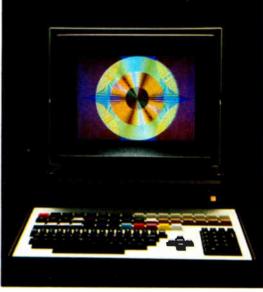
Microprocessor-based graphics terminal offers noninterlaced operation, 512-by-512-dot resolution, and a 60-Hz refresh rate for eight colors

by Ana L. Bishop, Assistant New Products Editor

"We intend to make black-and-white terminals wholly obsolete in this decade," says Terence Hughey, president of Chromatics Inc. His state-

Noninterlaced. Chromatic's CG 3999 terminal uses a Z80 microprocessor to achieve a 60-Hz refresh rate and noninterlaced operation on its 19-in. cathode-ray tube.





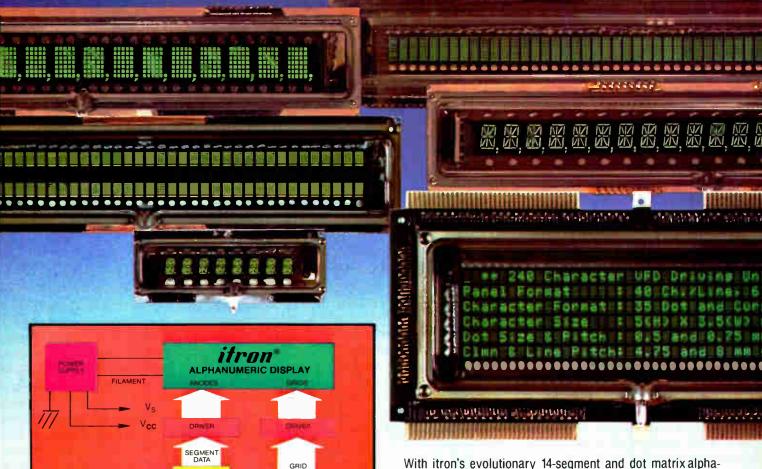
original-equipment manufacturers. It is on display this week at the National Computer Conference.

The terminal, model CG 3999, is a stand-alone computer "in its own right"—a basic machine also made to be integrated into a larger system by the system builder, says Don McKinney, director of marketing and sales. The unit contains a Z80 microprocessor with 128 kilobytes of random-access memory to refresh the colors on every dot on the screen at a 60-Hz rate.

"In this price range, no one else can offer noninterlaced operation," claims McKinney. Chromatics uses a standard 19-in. low-resolution television tube made by Panasonic but adds circuitry designed within the company to achieve a fairly high, 512-by-512-dot resolution.

"This is a significant price and quality breakthrough for process control applications in the OEM mar-

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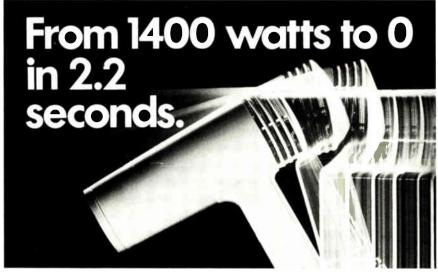
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Veteran tough guy meets his match.

See page 205

New products

ket," says Hughey. "Until now, comparable quality anywhere in the color field has cost at least \$2,000 more." Hughey forecasts a marked trend over the next few years toward lower prices and greater sophistication in the color segment of the graphics terminal market. "My goal for Chromatics is that by the mid-1980s there will be no reason for a user not to choose color."

The 3999 offers eight colors, achieved by making the red, green, and blue beams of three in-line guns converge through the holes of the shadow-mask screen. "By ANDing and ORing the colors, we get magenta, cyan, yellow, and white," explains McKinney. Black is the eighth "color." Sector convergence is done manually and, as long as there is no electromagnetic interference, it lasts for months.

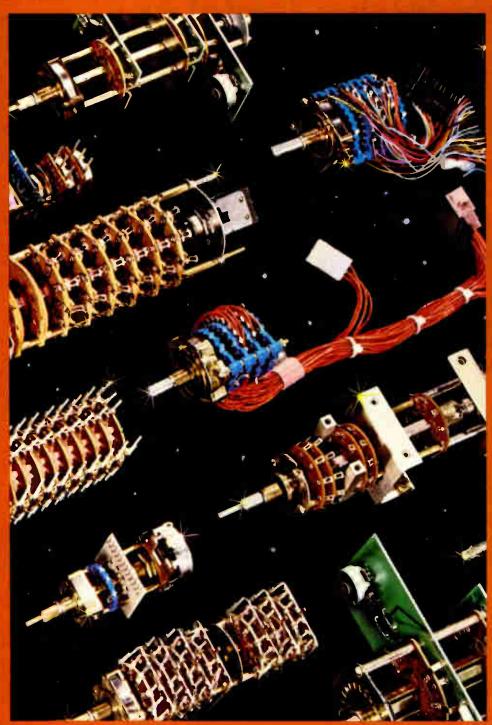
Memory. The 3999 uses the CP/M operating system. User memory is 128 kilobytes and can be upgraded in increments of 32 kilobytes by replacing a board and chip. In addition, it has 32 kilobytes of erasable-programmable read-only memory. The graphics capability is programmed in firmware. Errors can be diagnosed and corrected down to the chip level.

The terminal offers several digital and analog interfaces, including the RS-179 and RS-232-C, as well as a direct-memory-access interface. It has no interfaces for external buses. The stand-alone unit is not a large-scale computer, but it can store data on a disk, massage, and display it. It offers such general computer functions as input/output and storage.

The basic terminal with RS-232 port, Z80 microprocessor, random-access memory and graphics firmware measures 19.8 by 24.2 by 24 in. The base price for a single unit will be \$7,995, but drops to \$5,995 when ordered in lots of 100 units by the OEM. This summer Chromatics will double the size of its manufacturing facilities—built when the company was founded in 1976—in order to handle a six-month backlog.

Chromatics Inc., 3923 Oakcliff Industrial Court, Atlanta, Ga. 30340. Phone (404) 447-8797 [340]

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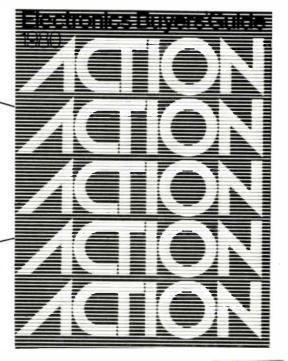
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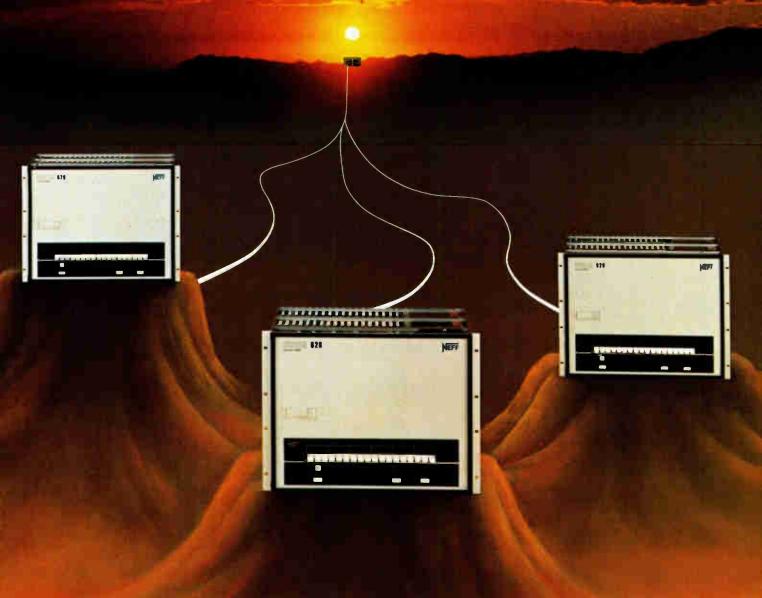
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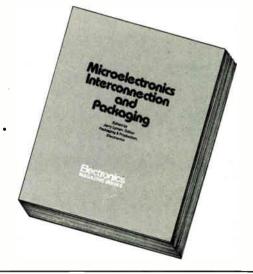
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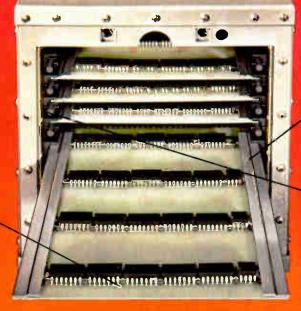
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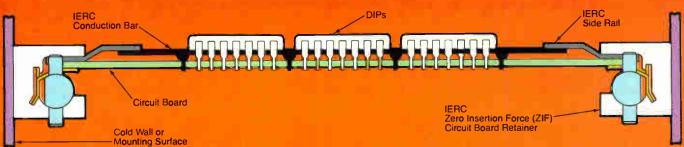
HERC's new 3-component conduction system matches—and in many cases exceeds—the cooling capabilities of forced-air systems, yet costs less and is easier to assemble.

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between the side rails and the
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transfer path.



These three off-the-shelf components are easy to assemble, allowing quick fabrication of a custom heat dissipation system. Conduction bars can be flow-soldered into any configuration along with other board components and place no restriction on the number of DIPs, distance between DIPs, or even the number of rows of DIPs. Standoffs raise the conduction bars .020" above the board to accommodate circuit traces.

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copper while the exclusive new ZIF circuit board retainers feature a unique locking action that provides an excellent thermal interface. These revolutionary retainers are the key reasons IERC's conduction bar system is so superior. They allow true zero insertion force installation to protect expensive circuit boards, then lock with a simple 90° turn of a cam actuator to provide both positive mechanical integrity and a highly efficient thermal interface.

All components in the new IERC conduction heat dissipation system come

in a variety of lengths so that the system can be adapted to virtually any circuit board design.

For more information, contact IERC or your nearest IERC Sales Representative.



Microcomputers & systems

Chip addresses 1 megabyte

Latest generation of microcomputer uses 8-in. Winchester disk for RAM

The jump from a Z80-based microcomputer system containing an 8-in. Winchester disk to a Z8000-based microcomputer system with an 8-in. Winchester disk may seem only evolutionary, but it reveals the great difference in power between the two generations of microprocessors. The first of these systems—the C8001 introduced at the National Computer Conference last year-addresses the 65 kilobytes of random-access memory allowed by its Z80A processor. The second, the C8002 computer system, which will be shown at this year's NCC, directly addresses up to 1 megabyte of RAM.

The C8002 is among the first microcomputer systems to be built

around Zilog's 16-bit Z8000 processor. It addresses 128 kilobytes of parity-checked RAM in its basic configuration, but that configuration can be expanded to 256-, 512-, and 1,024-kilobyte configurations. The mainframe also includes a 10-megabyte 8-in. Winchester disk and a 12-megabyte cartridge tape drive for backup. The C8002 retains the C8000's Z80A processor but, instead of using it as the central processing unit, has it handle direct memory access to the disk and tape drives.

Software. With initial shipments scheduled for July, Onyx Systems will support the Unix version 7 software, as well as a C language compiler, with additions in August of Basic, Cobol, and an IBM 2780 emulator for its communications package. A provision for Fortran comes with the Unix operating system, and Onyx should have it retargeted for the Z8000 and available in the third quarter. A data-base management software package developed by Micro-Soft of Bellevue, Wash., will also become available at the same time as the Fortran introduc-

According to Onyx president,

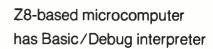
Robert Marsh, "The power of the C8002 lies between that of the DEC PDP-11/34 and the PDP-11/45." At a \$16,000 base price for a unit with 128 kilobytes of RAM, that represents a significant price-performance improvement, he adds.

The C8002 can be accessed by 10 serial ports, including nine RS-232 ports and one RS-422 high-speed interface. The serial ports allow the unit to support up to eight terminals and a modem, plus a bidirectional parallel port for a Centronics-type printer. The RS-422 port will be used in a local networking option that Onyx plans to introduce in the middle of next year. The C8002 can also support up to 15 similar drives.

Rather than using the Zilog memory management unit, Onyx has designed its own, which Marsh describes as "a cross between that used for the DEC PDP-11/45 and that used for the IBM Series/1." It segments the memory into two areas of 64 kilobytes each for instructions and for data. Within those segments, the memory is allocated in 2-kilobyte pages. The memory management unit has 16 sets of maps to keep track of its memory allocations.

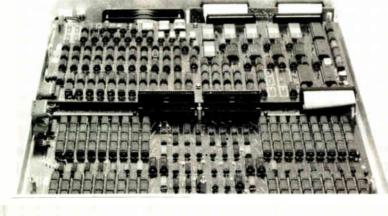
To handle the heavy number crunching, the C8002 also has a 64-bit arithmetic processing unit based on AMD 9512 floating-point processor chips.

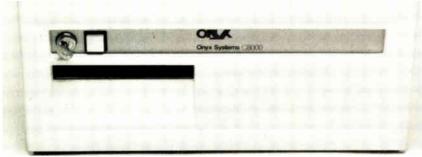
Onyx Systems Inc., 73 E. Trimble Rd., San Jose, Calif. 95131. Phone (408) 946-6330. [391]



The Z8-SBC single-board microcomputer features a Z8 Basic/Debug interpreter that is masked onto the 2-kilobyte internal read-only memory in the Z8 central processing unit. The microcomputer is designed for a variety of data-processing and data-acquisition applications. The language is a subset of the original Dartmouth Basic.

The 3.94-in.-by-6.3-in. board can accommodate up to 8 kilobytes of random-access memory, read-only





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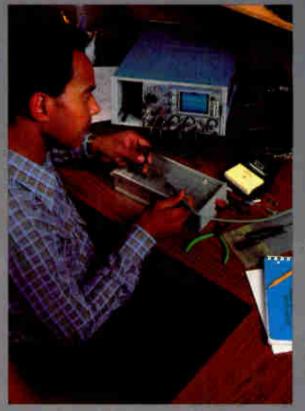
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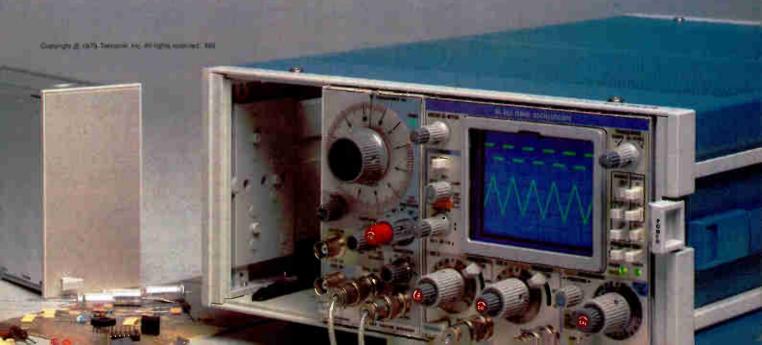
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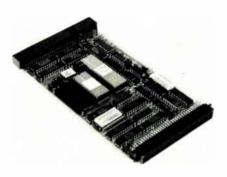


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See page **205**

New products



memory, or erasable programmable ROM. It has two counter-timers, five 8-bit parallel input/output ports, a programmable asynchronous serial channel that supports RS-422 or RS-423 interfaces, 124 general-purpose registers, and three levels of interrupts. The board has an effective instruction speed of 3.72 MHz and operates from a single +5-v power supply. Priced at \$695, or \$795 with an additional 4 kilobytes of RAM memory, the Z8-SBC will be available in July of this year.

Zilog Inc., 10340 Bubb Rd., Cupertino, Calif. 95014. Phone Mel Thomsen at (408) 446-4666 [376]

1-megabit bubble memory operates to 70°C

The 7110-1 is the first commercial 1-megabit magnetic bubble memory specified for operation to 70°C. A design enhancement of the 7110, it permits the operation of microcomputer systems at temperatures above 50°C. Another advantage of the 7110-1, says the manufacturer, is that bubbles can be used at temperatures at which tape and disk memories cannot operate.

Rated for operation from 0° to 70°C ambient temperature, the 7110-1 differs from its predecessor, the 0°-to-50°C-range 7110, in that it extends the temperature range of the module's storage and bootstrap loops. Also, the 7110-1 has a lower-amplitude current-pulse requirement for writing. The one-piece, U.S. price of the 7110-1 is \$1,985.

Intel Magnetics, 300 Oakmead Village Dr., Santa Clara, Calif. 95051. Phone Stew Sando at (408) 987-6046 [379]



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"We were looking for large program capacity. And VAX ran circles around the competition."



Skip Little,
Supervisor of Systems Analysis and
Systems Programming,
VAX Computer Group,
Woods Hole Oceanographic Institution,
Woods Hole, Massachusetts

Scientists at the Woods Hole Oceanographic Institution gather massive amounts of data about the earth's oceans. But until recently the only way they could analyze much of that data was by sending magtapes to and from a giant Cray 1 computer located 1800 miles away.

So the Institution decided to buy its own VAX from Digital.

Here's what Skip Little, Supervisor of Woods Hole's VAX Computer Group, has to say about VAX program capacity: "Some of the smaller versions of Cray modelling programs can actually be run on VAX. That's remarkable because the Cray 1 computer is the world's most powerful commercially-available system."

Now the problems they had in doing large data analysis and timesharing simultaneously are a thing of the past. Says Little, "We're able to lock our biggest jobs—like synthetic seismogram generation and fluid dynamical modelling—into VAX's main memory, while other timesharing users can be handled by the virtual memory system."

And Little has found that program conversion is a breeze: "We've converted programs from practically every kind of computer you can imagine with great ease."

"With VAX's virtual memory, there isn't a PC board around that's too large for LASAR to handle."





Teradyne, Inc. makes a wide range of automatic test equipment including computer-based systems for testing printed circuit boards. To help their customers program the most complex of these PC board test systems, Teradyne developed a sophisticated software package called LASAR."

But until Teradyne looked at Digital's VAX-11/780, LASAR was only available to customers through a timesharing service on a large batchoriented mainframe. The software package was just too big for anything less.

Now with LASAR running on VAX, Teradyne will have the program capacity they need, in a system their customers can afford to purchase.

"When you reach the limit of main memory, VAX automatically puts the program into virtual memory," Grant says. "That's a key factor in our LASAR development work. Test programmers can develop more complete programs without being limited by memory size."

Has Teradyne sacrificed performance by

switching from the mainframe?

"Definitely not," says Grant. "In our benchmarks, VAX matched up one-to-one with the mainframe. That really impressed us."

And VAX's interactive capability should be a big plus for Teradyne's customers: "Several people can program on VAX simultaneously, and they can monitor the progress of their programs as they work.

"There's more programmer involvement with VAX, and more efficiency too."

"Without Digital's VAX, our specialized design work just wouldn't be as cost effective."

Stephen Tritter, Senior Principal Engineer, Engineering Computer Facilities, E-Systems, Inc., ECI-Division St. Petersburg, Florida

The ECI Division of E-Systems, Inc., designs high-technology electronics and communications equipment for the U.S. Government. And that requires huge computer programming space.

So virtual memory capability was an important factor in the E-System decision to buy a VAX.

"We're doing a lot of work now that we couldn't have done without Digital's VAX," says Steve Tritter, Senior Principal Engineer.

"For example, we use the VAX to help us design our own LSI integrated circuit chips. That means keeping track of thousands of points, each with several different characteristics. It's a big job.

"And while that analysis is running, other people are performing high-frequency radio propagation studies using as many as 210,000 memory locations, or running Fast Fourier Transforms with up to 8,000 points."

Tritter says that ECI regularly has 10 to 12 engineers working interactively on VAX at a given time.

"We're very happy with VAX system performance," he adds. "We expect to add more memory, and eventually service 50 to 60 simultaneous users."

Digital's VAX-11/780, with its 4 billion bytes of virtual memory, has set a new standard for program capacity. This means you can run large programs easily on VAX, with a potential for growth that's unmatched in the industry.

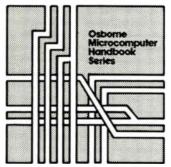
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Reference ICs gain in accuracy

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A series of precision hybrid voltagereference integrated circuits developed by Motorola Semiconductor is said to improve output voltage accuracy by nearly an order of magnitude and temperature stability by a factor of four. Maximum initial tolerances are $\pm 0.2\%$ for the family. according to Roger Janikowski, product planner, linear ICs, at Motorola's IC division.

The devices come in standard (0° to 70° C) and military (-55° to +125°C) temperature ranges. The commercial MC1400 series and the military MC1500 units are both intended for applications in data acquisition and conversion and instrumentation.

Two production process improvements combine to permit the higher-

performance references, Janikowski says. "A series of advances in thinfilm resistive network deposition is the basic one, and that has been enhanced by active laser trimming of the resistor networks themselves." The deposition techniques, which place thin-film networks on the silicon substrate carrying the active devices, make possible volume production of monolithic thin-film devices. And laser trimming helps raise overall specifications, "while adding only a small premium to the price of the devices," says the Motorola engi-

The Motorola devices are available in four output voltages: -2.5, 5, 6.25, and 10 v. The input range should be 1.0 to 40 v above the output voltage. The output voltage temperature coefficients are typically 2.5 ppm/° C, or a voltage change of 0.0175% over the commercial temperature range.

Moreover, the output reference is externally adjustable over a ±6% range using the output trim terminal. This allows, for example, the 10-v reference to be adjusted to 10.24 v for binary applications, such as digital-to-analog conversions. For data conversions, the initial ±0.2% accuracy opens use of these devices

to most 8-bit applications, without external adjustment, and to up to 12-bit uses by employing the trimming feature.

Another important feature is that "they can either source or sink greater than 10 mA of load current with excellent regulation," according to Janikowski. As a result, the devices have other advantages: they can be used as negative or positive voltage references; they can also act as a floating (ungrounded) reference when hooked up for two-terminal operation; and the buffer amplifiers and current sources normally needed for zener references can be eliminated.

Other specifications include:

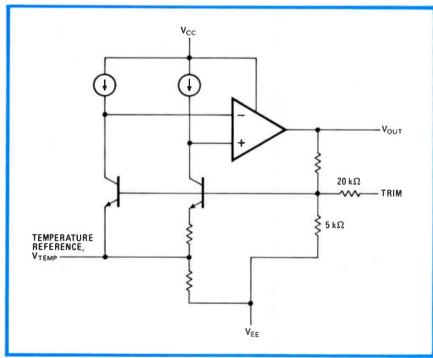
- Low-current consumption, 1.0 mA typical.
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- Long-term stability of 25 ppm/1,000 hours typical.
- Line regulation of 0.5 mv typical and 3.0 mv maximum.

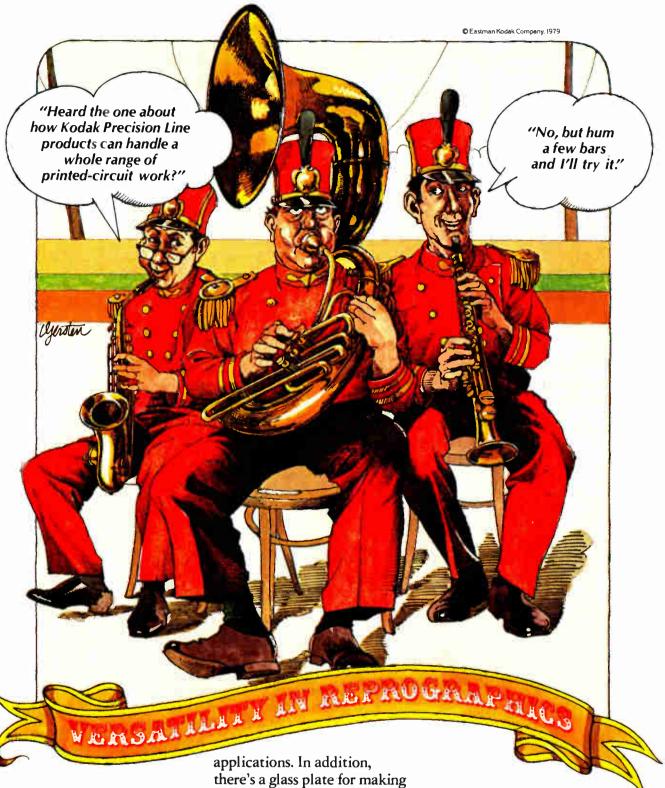
The MC1400 commercial series sells for \$3.25 per unit for 100 or more, the MC1500 military unit (with a typical temperature coefficient of 4.0 ppm/°C) for \$8.50. The units come in ceramic dual in-line packages, case model 693. All are available through Motorola originalequipment manufacturer sales or through distributors.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85202. Phone Roger Janikowski at (602) 962-2124 [411]

16-K C-MOS ROM draws Vout only 7 mA of current

The SCM5316 is a complementary-MOS read-only memory intended as a low-power replacement for the industry-standard 2316 n-channel MOS ROMs and 2716 and 2516 electrically programmable ROMs. Drawing only 7 mA of current, the static device has a maximum access time of 55 ns. Organized as 2,048 8-bit words, it incorporates a storage cell with control circuitry that automatically reduces current drain to 0.1 mA upon chip deselection for a C-MOS





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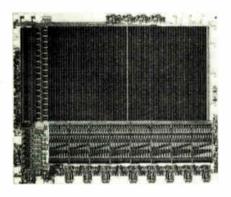
New products

interface or to 1 mA for a TTL interface. The ROM needs only one 5v $\pm 10\%$ supply and operates over -55° to $+125^{\circ}$ C.

Solid State Scientific Inc., Montgomeryville, Pa. 18936. Phone (215) 855-8400 [413]

8-K bipolar PROMs can be accessed in 60 ns maximum

The Am27S180 and Am27S181 high-speed electrically programmable read-only memories have a maximum access time of 60 ns over the commercial temperature range. The Schottky devices are organized as 1,024 by 8 bits and are available with open-collector (the 180) and three-state (the 181) outputs. Requiring only a single +5-v supply,



the units have a typical power dissipation of 600 mw.

The bipolar devices incorporate a platinum silicide fusible link at each memory location. An intact fuse represents a logic 0; Is are selectively programmed to a logic high by applying appropriate voltages to the circuit.

Prices for the units start at \$33.35 each in 100-unit lots.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, Calif. 94086. Phone (408) 732-2400 [414]

Dual 12-A Schottkys come in TO-220 plastic package

International Rectifier offers the first line of U. S.-made 12-A dual Schottky devices for power supplies

in TO-220AB plastic packages. Designated the 12CTQ series, each of the devices has two 6-A diode chips connected by a common cathode but with electrically separate anodes.

Manufactured using the company's 830 process, the circuits have a reverse leakage that changes little with changes in junction temperature and does not degrade in terms of voltage with increased temperature. The reverse leakage is 6 ma at 125°C; the junction temperature rating is 175°C for nonrepetitive operation and 150°C for repetitive. There are four devices in the family, with working peak reverse voltage ratings of 30, 35, 40, and 45 v, respectively. The maximum 45-v rating is better than that of competitive units, the company says.

The price is \$3.50 each for the 30-v unit in quantities of 1 to 49; for 100 to 999, the price is \$2.62 each. The 45-v dual Schottky sells for \$7.25 each in quantities of 1 to 49; for 100 to 999, the price is \$4.90. International Rectifier, Semiconductor Division, 233 Kansas St., El Segundo, Calif. 90245. Phone (213) 772-2000 [415]

Optoelectronic IC drives up to 8 TTL loads directly

The OPL 550 optoelectronic integrated circuit has a buffer with a totem-pole output that drives up to eight TTL loads directly without additional interface or signal processing circuitry. The discrete monolithic photosensor also includes a photodiode, a linear amplifier, and a Schmitt trigger. The device is encapsulated in a molded plastic package that has an integral lens for optical coupling to a compatible infraredlight-emitting diode. Typical propagation delay times are 2 µs and typical rise and fall times are 25 ns. The chip operates within the temperature range of -40° to $+70^{\circ}$ C. A buffer with open collector output, the OPL 550-OC, is also available. For 1,000 units, the price is \$2.50 each. Delivery is from stock.

Optron Inc., 1201 Tappan Circle, Carrollton, Texas 75006. Phone (214) 242-6571 [416]

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Shown 2/3 actual size



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Computers & peripherals

Printers sell for about \$1,000

Two matrix printers print 80 and 250 characters/s and have standard interfaces

With two new matrix-type units being shown at the National Computer Conference, Pertec Computer Corp. is expanding its peripherals line into the lower end of the printer business. The new units are manufactured in West Germany by Triumphwerke, Nuremberg, AG, parent company of Triumph Adler Inc., a U. S. subsidiary that acquired Pertec in 1979. Los Angeles-based Pertec plans to sell the printers worldwide.

Of the two matrix units, model P250 is the faster performer, turning out 250 characters per second. Although it will be priced above \$1,000, it is billed by the company as "a low-cost alternative to a line printer." Weighing about 55 lb, the printer is light enough to be portable and is designed for most distributed data-processing and multiterminal systems. With industry standard interfaces (serial RS-232 and teletypewriter), it transmits at 50 to

19,200 b/s. A 2-K character buffer (512 bits are included) and synchronous data transfer are optional.

The other printer, the P80, aims at low-speed data processing; it prints at 80 c/s. With simple construction intended to ease maintenance and add reliability, the P80 costs less than \$1,000. It provides up to three copies, with underlining and true character descenders, according to the company.

Other P80 characteristics include bidirectional logic that provides the ability to change print direction at any position and to process continuous forms, single sheets, or roll paper. It has transmission speeds of 110 to 9,600 b/s and a 256-character buffer. Weight is approximately 16.5 lb.

The P250 printer has a 7-by-9-dot matrix size, with a 9-by-9-dot size available as an option. It offers also a selection of character sets, numerous typefaces, and variable character spacing for up to 198 characters per line. For paper handling and fast ribbon replacement, the printer offers a bidirectional tractor-feed device, as well as self-test routines.

Voltages for the P250 are 100 to 240 v (\pm 10%) at 47 to 63 Hz. Power rating is 50 w standby and 150 w in operation. Temperature is 10° to 35°C.

For the P80, which also incorporates industry-standard parallel and

serial interfaces, self-diagnostic functions are provided, along with multiple character sets with either 80 or 120 characters per line. Voltage and power requirements are similar to the higher-priced model, except for ready state, which takes 15 w.

The printers will be available by late summer.

Pertec Computer Corp., Peripherals Division, 21111 Erwin St., Woodland Hills, Calif. 91367. Phone (213) 999-2020 [361]

Typewriter-sized printers use new head mechanism

A pair of typewriter-sized impact matrix printers capable of "office-quiet" operation is being added by General Electric to its family of TermiNet printers. The printers, part of the new TermiNet 2000 multimicroprocessor-based product line, are the 2020, which prints 30 characters per second, and the 2120, with a print rate of 120 characters per second.

The units rely on a newly designed blade print head, whose print dots, or pins, are each attached to a metal arm emerging from the side of a flat wire coil. The print head, placed in the field of a samarium-cobalt magnet, is 9 pins high and 7 wide; conventional matrix printers employ 7-by-7-dot matrixes.

Quiet operation. An injection-molded enclosure 22 in. wide, 18.5 in. deep, and 5.5 in. high, along with the new print head design, contributes to the quiet operation. GE rates operation noise at about 58 dBa. Each printer weighs 22 pounds.

The TermiNet model 2030 prints bidirectionally at 60 characters/s and a 150-character/s rate is provided by the model 2120. Print density is selectable at 10, 13.2, and 16.5 characters per inch along a 13.2-in. print line.

The keyboard is microprocessorscanned and employs capacitive key switches. For American models, an ANSI typewriter-paired arrangement is standard and an ANSI/APL layout is optional, as are layouts for inter-





Walter Benzing (right) pioneered work in epitaxial silicon deposition in the late '50s. In 1970, he and Michael McNeilly (left) coinvented the use of radiant heating in epitaxial reactors—the most widely used epitaxial technology in the semiconductor industry today.

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SEMI Presents... Great Moments in Semiconductor History

It was the work on bulk silicon growth done in the late '50s at the research labs of Merck and Company which led to the technology of growing epitaxial films on silicon single crystals. By vapor phase growing the film, and doping it as you go, Walter Benzing and his team discovered, one could achieve a plurality of layers having different conductivities. Direct preparation of P/N diodes and the more important n+/n structure from this method were usable in high frequency transistors.

Benzing, George Krsek and others received a patent for their method and a multiwafer reactor to achieve this breakthrough in the early '60s.

From the early Radio Frequency reactors, Benzing and Mike McNeilly (one of the founders of Applied Materials) worked on a radiant reactor which would ensure more wafer uniformity, handle larger wafers and more wafers per load. Their radiant heating reactor, most widely used today, yielded them a patent in the early '70s. Their greatest breakthrough was in being able to produce a wafer free of crystallographic slip. In more recent years, the same radiant heating has been applied in a reduced-pressure reactor which reduces autodoping.

SEMI is "breaking through" in 1980 too. This is the year of our Tenth Anniversary Celebration and the first year SEMICON will be managing the SEMICON/Southwest Trade Show at Market Hall in Dallas, October 8–9. Prior to that, we will gather for another "Great Moment" at SEMICON/East in Boston, September 23–25. Hope to see you then . . .

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Semiconductor Equipment and Materials Institute 625 Ellis Street, Suite 212, Mountain View, CA 94043 (415) 964-5111, Telex: 171-977 SEMI-MNTV

New products



national use. A numeric cluster also is available as an option.

The new printers, employing switching-type regulators, require 30 w (the 2030) and 50 w (the 2120). The units use dual 8085 microprocessors, offer a received-data buffer, and feature nonvolatile configuration memory. In addition, the printers incorporate modular software and provide a full RS-232 data interface.

The new product line will be sold directly to original-equipment manufacturers and through a new network of distributors. Full-scale production will begin in September for the TermiNet 2030 and by the end of the year for the TermiNet 2120.

Price for a single 30-character/s model will range from \$1,400 (receive-only) to \$2,300 for a send/receive unit with a keyboard and all options. Price for a single 120-character/s unit will range from \$2,100 (receive-only) to \$3,000 for a unit with all available features. OEMquantity discounts will be available. Data Communication Products Business Dept., General Electric Co., Waynesboro, Va. 22980. Phone (703) 949-1000 [362]

High-resolution color terminal refreshes at 30 Hz

The Whizzard model 7250 parallel raster terminal, the first member of a 7200 family, offers an average pixel writing time of better than 160 nanoseconds. That allows updating of complex pictures at standard 30-Hz frame rates on a 512-by-512-pixel color or monochrome raster monitor.

The unit supports multiple monitor setups, with up to four 16-color monitors or up to 16 monochrome monitors. It is completely compati-

ble with the firm's existing vector graphic refresh systems but differs from them in its use of a digital vector generator rather than an analog vector generator.

Explains Peter J. Shaw, vice president and director of marketing at Megatek Corp., "this gives OEMs the flexibility to address a much wider range of applications, while maintaining device independence of their software." The 7250 has a capacity of 196 kilobytes of memory, with each 32-bit word holding up to two vectors or four characters. Combined with the 4,076-by-4,096 virtual vector space, this provides detail in real-time steps from 512 by 512 to 4,096 by 4,096.

Prices for black-and-white monitor systems start at \$20,000, and those for color systems start at less than \$25,000. Deliveries are slated for late summer.

Megatek Corp., 3931 Sorrento Valley Rd., San Diego, Calif. 92121. Phone (714) 455-5590 [363]

Modular system includes up to 32 peripherals

A modular computer system from Infotecs—Control Center 2—consists of a terminal with a cathode-ray tube, a 150-character/s impact printer, and a control cabinet for a high-speed floppy-disk dual drive, two plug-in processor boards, and a power supply. The system can be expanded to include 32 peripheral devices. Software developed for earlier Infotecs systems can be run on the new system.

One unusual aspect of the system is the use of multiple dedicated processing units instead of the more conventional central processing units. This allows simultaneous multiprocessing. As devices—CRTs or printers, for example—are added to the system, additional DPUs are added also to eliminate the processing bottleneck. The basic hardware price is \$11,500 and delivery time is quoted as 30 days.

Infotecs, One Perimeter Rd., Manchester, N. H. 03103. Phone (603)624-2700 [365]

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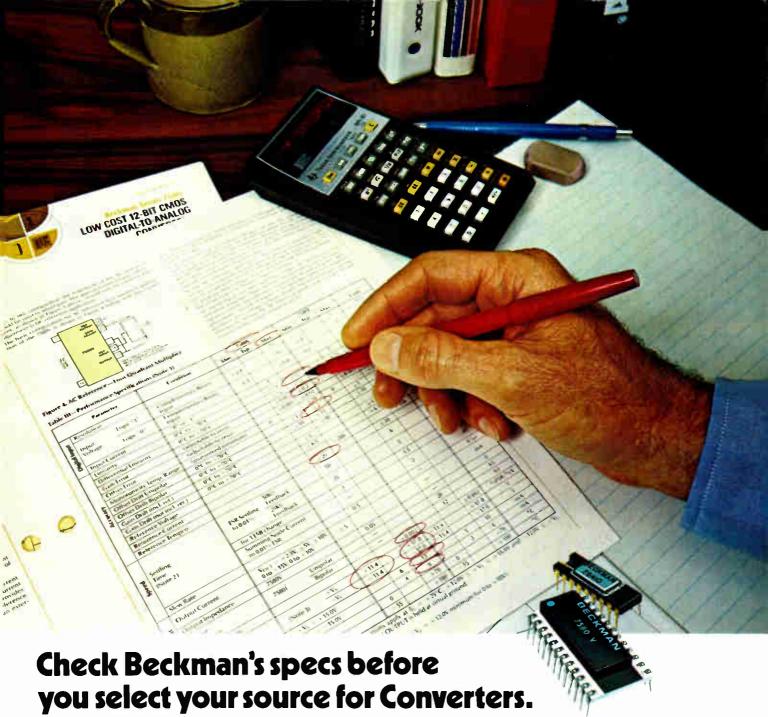
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Circle 197 on reader service card

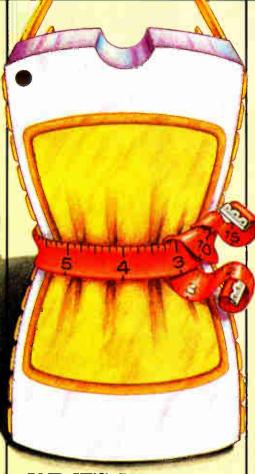
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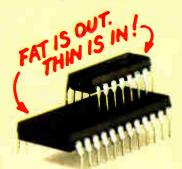
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For the full story on this lean, new DAC, contact Doug Grant or Don Travers at (617) 935-5565, or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062





WAYOUT IN FRONT

Instruments

Position indicator with LED display goes commercial

Size reduction has always been a way of life for those designing solid-state components. And where harsh service was demanded, few of the more advanced designs saw service beyond military applications such as ground-based radar antenna equipment. But all that may be changing, if a recent product introduction by Natel Engineering Co. is any indication.

The device—model SD4071 dualangle two-speed position indicator reads angular displacement in two axes and has several features that could be useful in such demanding applications as industrial robot production measurements, construction gear, oil drilling rigs, and vehicle testing.

As a two-speed device, it offers 0.01° resolution (for a five-digit version) or 0.001° resolution (for a six-digit version). Light-emitting diodes display angle measurement for each axis. Each axis has two synchros; one yields rapid coarse data, whereas the other produces fine data for high accuracy.

In operation, on-board processors convert the synchros' angular displacement into digital signals; plugin modules adapt the converter electronics to the synchro gear ratios used (those ratios range typically from 1:16 to 1:72, with 1:36 being the most common). The choice of ratios is determined by the accuracy needed.

Moreover, replacement converter modules are precalibrated as a condition of purchase. Five-digit resolution is provided by a converter with 16-bit capacity and six-digit by one having 20-bit capacity. Most customers, says the company. like to have one or two on hand.

Besides the flexibility permitted by the replacement converter modules, Natel's angle indicator can also be set up to operate with a variety of synchro input and reference voltages by adjustment of internal switches. Also provided are switchable voltages that permit up to 360° angle offset.

In addition to displaying angle position in two axis, the device provides other outputs for data storage and other uses. For one, it converts synchro or resolver inputs into a linear dc output proportional to the angle input. The output may also be in the form of binary or angle logic, the company reports.

Other options include binary angle offset controls to provide both, a 0° to 360° offset between synchro input and output, and a linear dc output proportional to the angle input. A ±180° bipolar input is also available.

Prices start at \$1,995 and delivery is from stock.

Natel Engineering Co., 8954 Mason Ave., Canoga Park, Calif., 91306. Phone (213) 882-9620 [352]

17-lb oscilloscope features 5-in. CRT

A small 17-lb, 25-MHz dual-trace oscilloscope has a large screen for its size. It measures 5.25 by 12 by 16.25 in., yet has a 5-in. rectangular cathode-ray tube with an internal

graticule for optimum accuracy. The portable model OS1200 has been designed for analog and digital uses in laboratory and field service.

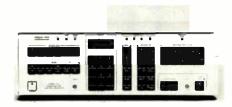
The unit's 14-ns rise time, 6-kv accelerating potential, and built-in signal delay make it a good choice for measuring narrow digital pulses with fast rise times and low repetition frequencies. A 1-v dc-coupled Z-modulation input eases its use with logic analyzer outputs. Time-base speeds range from 200 ns/cm to 1 s/cm with vernier control over a range of 2.5:1. The dual input channels have a maximum sensitivity of 2 mv/cm over the full 25-MHz bandwidth.

The oscilloscope with probes sells for \$1,299. Delivery is 30 days after receipt of order.

Gould Inc., Instruments Division, Marketing Services, 3631 Perkins Ave., Cleveland, Ohio 44114. Phone (216) 361-3315 [353]

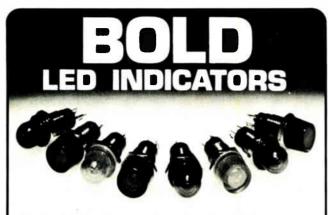
GPIB function generator has intelligence

The model 5900 may be the first intelligent programmable-function generator intended for use with the



general-purpose interface bus (GPIB). The microprocessor-based unit has a built-in automatic programmer that can learn a procedure and repeat up to 200 of the steps at any given rate. This capacity eliminates the need for a controller in low-level systems and reduces the demands on a central processor's time in larger systems. The feature, combined with the unit's arithmetic and automatic-incrementing and decrementing, makes possible precise linear sweeps over a 10,000:1 range, log sweeps over the unit's entire 100- μ Hz-to-5-MHz range, and nested





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New products

loops that can intermix log and linear sweeps as well as operate on frequency, period, pulse width, duty cycle, amplitude, dc offset, or burst cycle. Nine storage registers are available.

The 5900 produces sine, square, triangle, pulse, and sawtooth waveforms in continuous, gated, triggered, digital sin/log sweep, and triggered-burst modes. Its 30-v peak-to-peak output has a 10-mv resolution. The unit has a front-panel attenuator that will provide attenuation ratios of 20, 40 or 60 dB. The price is \$3,000 and delivery is in 90 days.

Krohn-Hite Corp., Avon Industrial Park, 255 Bodwell St., Avon, Mass. 02322. Phone (617) 580-1660 [354]

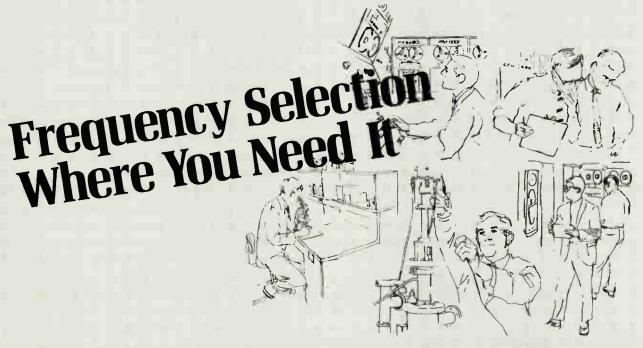
Multichannel FFT analyzer links to computer terminals

The model 6080 multichannel fast-Fourier-transform analyzer can be used as such or combined with peripherals and computers to operate as a 128-channel real-time analyzer, high-speed data-acquisition system, or modal analysis system. A proprietary bus concept allows a large number of data-acquisition cards, each with its own auto gain stage, a 12-bit analog-to-digital converter, and anti-aliasing filters to be connected to common signal-processing and central-processing-unit buses.

The instrument can be used with a Zonic 6081 or Tektronix terminal to perform a variety of functions, including 30-ms, 400-line FFT, and with a DEC minicomputer to perform advanced modal analysis. Twentytwo sample rates, from 20 Hz to 102.4 kHz, can be selected internally, and frequencies to 40 kHz can be analyzed. Two optional modules are available; one provides bandselectable frequency analysis, and the other provides transfer functions from swept sine excitation and order analysis of rotating machinery. The instrument sells for \$19.950.

Zonic Technical Laboratories Inc., 2000 Ford Circle, Milford, Ohio 45150 [356]

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25 Locust Street, Haverhill, MA 01830 Tel: 617-374-0761 TWX: 710-347-0314 Communications

Codec partitioned into encoder and decoder chips

A two-chip complementary-MOS codec set has been partitioned into an encoder with filters on one chip and a decoder with filters on the other. The model S3501 encoder and model S3502 decoder have been designed to handle voice frequencies in each channel of pulse-code-modulation channel banks.

The separate chips are said to eliminate any possibility of crosstalk between transmit and receive channels. Also, they enable users of only transmit or receive devices to buy chips highly suited to their specific purposes.

Each chip contains a bank-limiting filter and an analog-to-digital or digital-to-analog converter that conforms to the transfer characteristics specified in the μ -255 law. The filter consists of a sixth-order low-pass elliptical filter followed

by a third-order Chebyshev high-pass filter. Rejection below 65 Hz is at least 25 dB, which minimizes noise induced by power frequencies. The analog-to-digital converter uses charge redistribution techniques to perform the conversion.

The units receive and transmit 8 bit data words containing analog information and do so at up to 3.2 Mb/s, with analog sampling at a nominal 8-kHz rate. The 8-kHz strobe signal also generates all internal timing signals in a phase-locked loop so the device's pin count can be reduced.

The 18-pin encoder has control logic for common-channel interoffice systems and D3 signaling, a loop that nulls long-term offsets, and an uncommitted operational amplifier for gain trimming and anti-aliasing. The filter on the 16-pin decoder has sin X/X correction, and the op amp is for directly driving a $600\text{-}\Omega$ load. In addition, it has optional TTL or relay drive from the A or B signaling output.

Each chip needs one reference voltage and two noncritical power supplies (typically ±5 v dc). In the absence of

the 8-kHz strobe, the units power down. They also do this when the phase-locked loops sense unlocking. Standby power dissipation is 15 mW per chip; the typical operating power dissipation is specified at 70 mW for the S3501 and 55 mW for the S3502.

The chips come in ceramic dual inline packages. Each set sells for \$37.50 when ordered in quantities of 100 sets. American Microsystems Inc., 3800 Homestead Rd., Santa Clara, Calif. 95051. Phone (408) 246-0330 [401]

Processor transmits speech and 1,200-b/s data together

Until recently, simultaneous transmission of speech and full-duplex data over a single, four-wire voice circuit was limited to 600 b/s, and even then the quality of the voice, with its 1,800-Hz bandwidth, was marginal. Now a speech and data processor, the model 6860, allows transmission of high-quality speech simultaneously with a 1,200-b/s data rate.

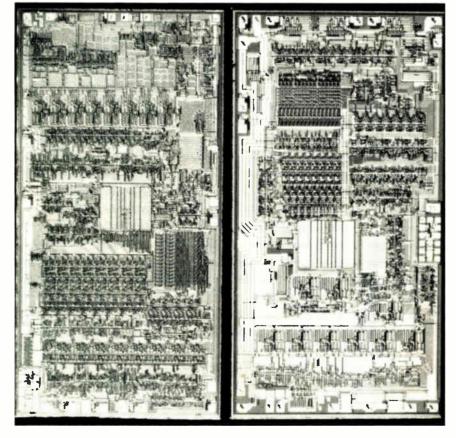
The speech-processor portion of the system uses a voice compandor to provide a low-noise circuit and includes ear and mouth (E&M) signaling to interface PBX and PABX terminals. The modem portion features data distortion of less than 1%, a modem-loopback switch, and light-emitting-diode displays that aid in the supervision of digital functions. Digital interfaces include an RS-232 connection or one that meets the Consultative Committee of International Telephony and Telegraphy standard V.24.

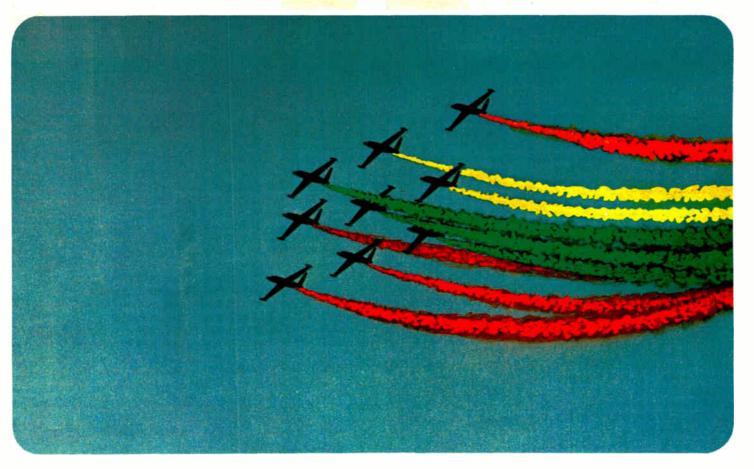
The communications processor sells for \$3,264 per terminal end and can be delivered in 60 days.

RFL Industries Inc., Boonton, N. J. 07005. Phone Al Jordon at (201) 334-3100 [403]

Optical transmittive coupler has insertion loss of 0.6 dB

A two-port-by-two-port optical transmittive coupler has an insertion loss of 0.6 dB and directivity of -30





Fly by color!

The Electron Tube Division is now readying a range of specially ruggedized, extremely high brightness, high-resolution, multicolor CRT's, destined for the head-down display (HDD) systems of the new generations of civilian and military aircraft that are being developed for the 1980's. The use of these tubes in HDD's permits displaying several different parameters simultaneously on a single screen, by using different combinations of scanning standard (TV or stroke-writing) and color. This reduces total display area. simplifies data assimilation, and reduces recognition errors. All of these new tubes will use the penetration screen principle, pioneered by THOMSON-CSF. Typical of

these new tubes is a 5" x 5", 3-color, high-resolution tube with a contrast-enhancing directional filter. Primarily destined for the MIRAGE 2000. the new French combat aircraft, this tube, or a derivative thereof, is suitable for any military aircraft in which high readability is required under the intense lighting commonly found in cockpits. Similar tubes have been developed for civilian aircraft where environmental conditions are slightly less severe. In addition, because the copilot must have access to the same information as the pilot, these tubes use wide-viewing-angle, neutral-density filters for contrast enhancement, instead of directional filters.





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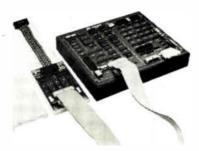
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DB/65



If you were designing the ideal 6500 development system, what would it contain?

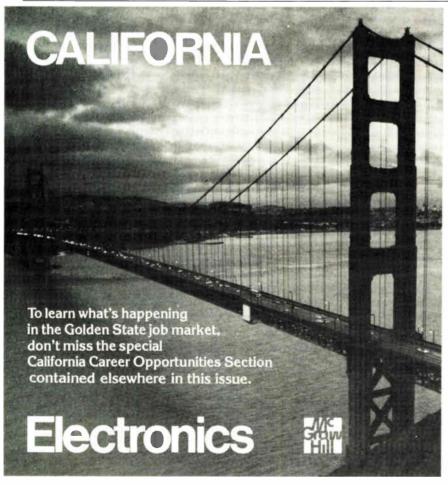
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Circle 218 on reader service card



New products

dB. The Maxlight model C2X2-200 has an 0.38 numerical aperture and works well with plastic-clad silica optical waveguides with a $200-\mu m$ core. It allows the user to design a wide variety of single-fiber configurations that he could not design in the past. For example, duplexing, branching, monitoring, and mixing are now feasible applications.

The coupler operates passively and requires no external connections other than to the waveguides. The core diameter is 208 μ m. The units operate from -30° to 80° C. Four cabled fiber leads may be varied in length by the user. Each lead is terminated using a semirigid connector adapter sleeve whose inner surface provides an optical cladding with a high-strength molecular bond to the silica core.

The coupler may be ordered with the adapter sleeve only or with optional AMP or Amphenol 905series connectors installed. Singleunit prices start at \$198 with delivery from stock to four weeks.

Maxlight Optical Waveguides Inc., 3035 N. 33rd Dr., Phoenix, Ariz. 85017. Phone Gary Nelson at (602) 269-8387 [405]

Selective call receiver is field-programmable

The model 7924 is a programmable call receiver designed for use in all types of secure combinatorial switch selectors, which include mobile radios and remote telephone answering systems. Contained in a multiple dual in-line package, this dual-tone multifrequency (DTMF) device can correlate a sequential code of digits in a preselected time interval. When it is used with the TC-100 DTMF encoded keyswitch, one or more 7924 receivers may be placed at various locations along a two-wire system up to several kilometers long.

In quantities of 1 to 49, the 7924 sells for \$150 apiece; 50 to 99 units sell for \$125 each; and 100 to 499 units sell for \$100 apiece. Delivery is from stock to four weeks.

Telaris Telecommunications Inc., 2772 Main St., Irvine, Calif. 92714 [406]

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Tell them you want to see how tough they are"



Circle 219 on reader service card

Data acquisition

D-a converters aid raster-scan CRTs

Fast-settling d-a converters offer small size and low-glitch performance

Fast-settling, low-glitch digital-toanalog converters have been a boost to raster-scanning cathode-ray-tube display terminals. Though such displays may have lower resolution than vector-scanning systems, they usually are brighter, offer a wide range of colors, and cost less.

Until now, d-a converters for raster-scanning applications have fallen into two categories: they have been either relatively large, power-hungry modules or monolithic devices prone to random output spikes, or glitches. The typical monolithic unit also needs a number of outboard passive components.

The HDD d-a devices from Analog Devices Inc.'s Computer Labs division, Greensboro, N. C., are not only fast, but also small—they come in dual-width, dual in-line packages. They require no outboard parts and need relatively little power.

The 8-bit HDD0810C and 10-bit HDD1015C are emitter-coupled-logic-compatible for speed and use 125-MHz input registers to store display data. The C suffix indicates that the units offer digital control of the composite signal, sync, and blanking at packaging pins. The composite blanking output is 1 v with the units terminated in a 75- Ω load. Companion units without digital composite control, that is, without the C suffix, are available at lower cost.

All four units settle in 10 to 15 ns to within 0.2% and 0.1% of full scale for the 8- and 10-bit versions respectively. The slew rate is 200 V/ μ s; the rise time is 4 ns. The update rates are 100 MHz for the 8-bit converter and 67 MHz for the 10-bit.

The units offer low-glitch output as well: 200 pV-s, maximum. With so-called deskewing capacitors added between the input registers and the initial converter stage, glitch output then reaches a maximum level of only 100 pV-s.

These are current-output devices and their output format meets EIA performance standards RS-170 and RS-373 for video even though television applications are expected to account for only 5% to 30% of sales.

The units come complete with internal voltage reference, and both the 8- and 10-bit versions are guar-

anteed to be monotonic and are accurate to within $\pm 0.1\%$ and $\pm 0.5\%$ of full scale, respectively.

Linearity and the zero-offset temperature coefficient are 5 and 1 ppm/°C, respectively. The gain temperature coefficient is 80 ppm/°C for both converters.

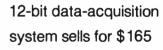
The converters have a unipolar output-current range, or gray scale, of 0 to -17 mA and ±1.1 v output-voltage compliance. For applications requiring a wider output-current range, the two units that come without a video composite output—the HDD0810 and HDD1015—offer a range of from 0 to more than 27 mA.

The HDDs require only a single -5.2-V supply, with the 8-bit model drawing only about 380 mA and its 10-bit companion drawing only about 450 mA.

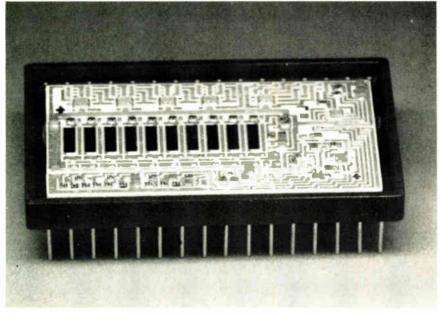
The devices are designed for a zero to $\pm 70^{\circ}$ C commercial temperature range and are packaged in a ceramic dual in-line package; for industrial applications, hermetically packaged versions operate over a -30° to $+85^{\circ}$ C range.

In 100-unit lots, prices are \$135 for the HDD0810C and \$151 for the HDD1015C. For the units without composite video output, prices fall to \$129 and \$143, respectively. The HDD d-a converters are available from stock.

Analog Devices Inc., Computer Labs Division, 505 Edwardia Dr., Greensboro, N. C. 27409. Phone Arnold Williams at (919) 292-6427 [381]



This 16-channel, 12-bit data-acquisition system accepts analog inputs over a \pm 10-v range. The SDM854 operates from -25° to $+85^{\circ}\text{C}$, has 12-bit, $\pm0.01\%$ or $\pm0.025\%$ linearity, throughput sampling rates of up to 27 kHz, and high input impedance of $5\times10^{9}~\Omega$. Its internal circuitry is protected when input signals range up to 20 v higher than the unit's positive or negative supply. This protection is a special advantage when the system is used in electrically





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DAX500-2H

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SPECIFICATION

Model	DA50-IH	DA200-1H	DAX200-1H	DAX300-1H	DAX300-2H	DAX500-2H
Output Power	50VA	200 VA	200VA	300 VA	300 VA	500 VA
Input Voltage	DC11~16V	DC11~16V	DC11~16V	DC11~16V	DC22~32V	DC22~32V
Output Voltage	AC115 (230) V	AC115 (230) V	AC115 (230) V	AC115(230) V	AC115 (230) V	AC115 (230) V
Output Regulation	Less than ±5%	Less than ±5%	Less than ±5%	Less than ±5%	Less than ±3%	Less than ±3%
Output Distorsion	Less than 10%	Less than 10%	Less than 5 %			
Dimension (mm)	178×110×233	178×153×213	180×183×261	180×183×391	180×183×391	220×350×300
Weight (kg)	6.0	6,5	7.0	12.0	12.0	15.0

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New products

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Included in the SDM854's 54.6by-43.3-by-5.6-mm package are an analog multiplexer, address register, sample-and-hold circuit, 12-bit analog-to-digital converter, delay timer, clock, voltage reference, and threestate output buffers that simplify 4-, 8-, and 16-bit data-bus interfacing. Chips are mounted on an 80-pin quad in-line ceramic substrate that offers total isolation and an effective heat sink, says the company.

Prices are \$165 for the SDM854AG (0.025% linearity), \$185 for the SDM854BG (0.01% linearity). Delivery is from stock. Burr-Brown, P. O. Box 11400, Tucson, Ariz. 85734. Phone (602) 756-1111 [383]

10-bit a-d converter samples at 20-MHz rate

Perhaps the first 10-bit, 20-MHz analog-to-digital converter, the model MOD-1020 allows the user to double sampling rates for radar digitizers, digitize baseband signals in communications applications, and extend spectrum analysis bandwidths, says the manufacturer. Its root-mean-square signal-to-noise ratio is 56 dB, minimum; and the peak signal-to-rms noise ratio is 65 dB, minimum.

On a printed-circuit board, the MOD-1020 includes all the circuitry necessary for a complete 10-bit accurate conversion, such as trackand-hold, encoder, timing logic, references, and output latches. It also features pin-selectable analog inputs of 1 V peak to peak or 2 V p-p at 500 Ω or 1 k Ω ; a noise-power ratio of 45 dB, minimum; a 15-MHz largesignal input bandwidth; a 30-MHz small-signal input bandwidth; and transient response and overvoltage recovery times of 50 ns.

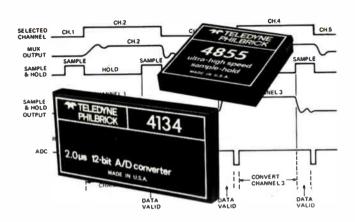
Packaged on a printed-circuit card, the MOD-1020 a-d converter sells for \$1,795 when ordered in quantities of 100. Delivery is from stock.

Analog Devices, Computer Labs Division, 505 Edwardia Dr., Greensboro, N. C. 27409. Phone Ed Graves at (919) 292-6427 [384]

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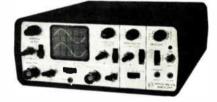
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- Line synchronization mode.
- Power usage—<15 W.
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MS-230 \$598.15 30 MHz — Dual-Trace

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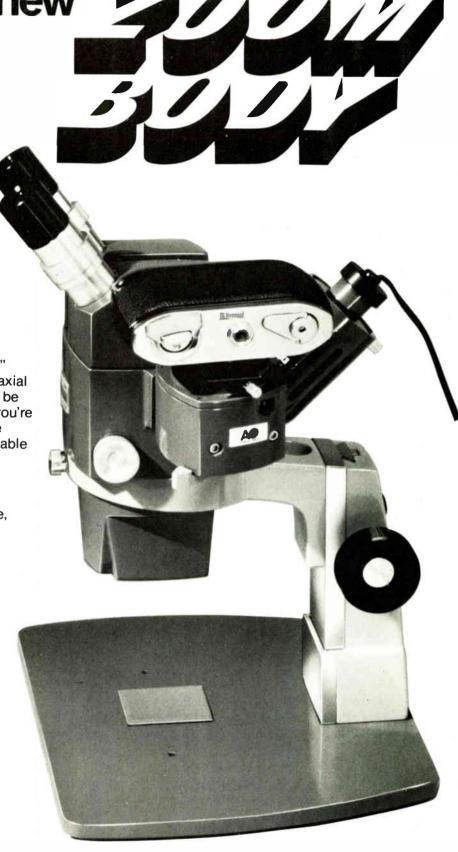
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Products newsletter.

Minicomputers drive Protos development system

The National Computer Conference this week will see the 4/95 and 4/97 minicomputers from Computer Automation Inc. that form the basis for the Irvine, Calif., company's new Protos software development system. Key to the new design is a memory management unit that makes it possible to convert 16-bit logical addressing into a 22-bit physical address format, allowing 8-megabyte capacity. Access time has been cut to about 125 ns. The price of the 4/95, which is offered with central processing unit, memory management, and cache (with up to 128 kilobytes of random-access memory), starts at \$8,500 and goes up to \$30,000 for a full megabyte of capacity. The 4/97 Protos, built around the 4/95, is scheduled for delivery in October and will be priced between \$80,000 and \$120,000.

HP adds IEEE-488

This week at the National Computer Conference, Hewlett-Packard Co. is introducing the first enhancements to its HP 85 personal computer. The HP 85, which was itself introduced earlier this year, has a built-in 40-character-wide thermal printer. However, with a new IEEE-488 interface, it will be able to feed printers with 80- and 130-character widths, as well as handle forms. The model 82937A interface fits into one of the four rear slots in the HP 85 and costs \$385.

The Palo Alto, Calif., company is also showing a read-only memory that performs the necessary input/output functions to make the computer into an instrumentation controller. The \$295 ROM gives the HP 85 I/O statements similar to those used on the HP 9835A desktop computer.

Winchester disk to HP 250 computers

Hewlett-Packard has put a standard 12.1-megabyte Winchester disk in its HP 250 computer, replacing the options for dual and triple flexible disks. The new disk system has four times the capacity but the same \$23,000 price tag as the discontinued triple-floppy system. Its average seek time is 70 ms, with a maximum transfer rate of 526.7 kilobytes/s. A single 1.2-megabyte flexible disk is included for backup and data loading. Three additional capabilities offered by the Palo Alto manufacturer are a larger add-on memory priced at under \$20,000/megabyte; an intelligent network processor and remote-job-entry software for data communication to HP, IBM, and other computer systems; and a facility to read and write IBM 3741-formatted flexible disks.

Scope calibrator module for TM500 is programmable

Tektronix Inc. is offering an oscilloscope calibration generator that plugs into the TM500 series of instruments. But that's not all: the model CG-551AP module is programmable. The microprocessor-based scope calibrator can be used to verify vertical gain, horizontal timing and gain, vertical bandwidth and pulse characteristics, probe accuracy and compensation, and current probe as well as calibrator output accuracy. The Beaverton, Ore., firm expects the IEEE-488 programmable unit to be used as part of an automated system that would include a controller and a printer. Besides governing operator actions and calibration signals, software for the system also compares test results from the CG-551AP with the user's permissible standards and is included in the \$12,000 price.

The biographies of 5,240 of your colleagues...

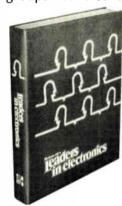
Profiles the Top Management of Major Electronics Firms throughout the World —and more

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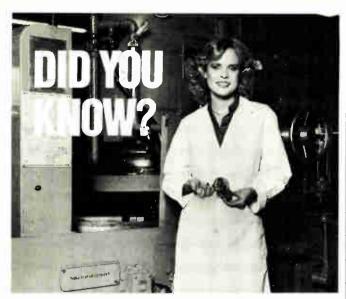
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New literature

Computer software and related reports. The "1980 Directory of Computer Software and Related Technical Reports" contains a listing of machine-readable software used by the Federal government, along with technical reports about the software. More than 350 programs are divided into 27 subjects on social sciences, economics, science, and technology. Report topics include modeling and simulation, statistical analyses and evaluation, data base management systems, and search and retrieval systems. Software programs include the Cobol Compiler Validation System, Version 3; Fortran Compiler Validation System, Version 1; and Table Producing Language (TPL), Version 3. Ask for order number PB80-110232. The publication sells for \$40. U.S. Department of Commerce, National Technical Information Service, 5285 Port Royal Rd., Springfield, Va. 22161.

Relays. A 60-page catalog presents detailed information on various lines of relays, including the line of QPL relays for high-reliability applications, a wide variety of industrial, commercial, and computer-grade relays, and a number of radio-frequency relays. The catalog also has a cross reference chart listing the Hi-G devices and their equivalent military parts. Engineering data on performance, electrical parameters, and mechanical and mounting specifications is presented for each relay series. Hi-G Inc., 580 Spring St., Windsor Locks, Conn. 06096. Circle reader service number 422.

Knobs. Machined aluminum and molded plastic knobs for electronic, medical, and audio equipment and instrumentation are illustrated in a 16-page catalog. Fourteen series of machined aluminium knobs are shown in 58 sizes; another 14 series of plastic knobs are shown in 59 sizes. The knobs come in regular, bar-pointer, double-bar-pointer, two-tone, and concentric configurations. Prices and complete ordering information are given. Front Panel Devices Inc., 530 Burnside Ave., Inwood, N. Y. 11696 [423]



When you need more than off-the-shelf magnets,

PERMAG HAS THE ANSWER!

...PERMAG has computer controlled machines for honing, slicing and dicing magnets to extremely close tolerances. And PERMAG has specially designed EDM machines that can put precision holes in magnets. Combined with our cutting, grinding and fabricating facilities, we can produce any magnetic assembly to your design. Each of our 9 modern plants is stocked, staffed and equipped to meet your every requirement.

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Consult Yellow Pages for address & phone number of PERMAG near you

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with HIGH THERMAL CONDUCTIVITY

16.7 x 10 4 cal/sec cm° C, min.)

NEW SILICONE FREE PQ Heat Sink Compound is ideal for electronic assemblies & circuit applications where excessive heat can reduce service life.

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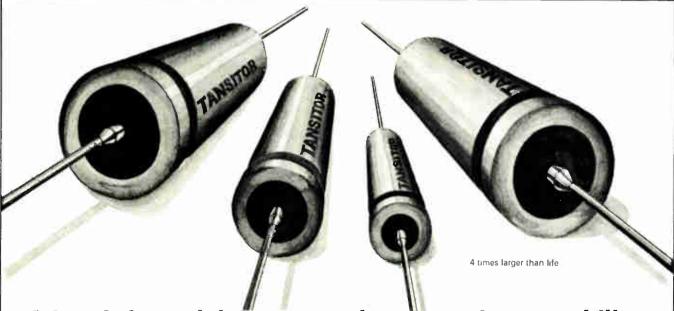
• EXCELLENT LUBRICITY means easier, more efficient applications

Meets Western Electric Spec KS-21343 Available in 4 oz applicator tip tubes. 1 lb cans. 40 lb pails, 250 lb drum

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Circle 228 on reader service card



A breakthrough in wet tantalum capacitor capability

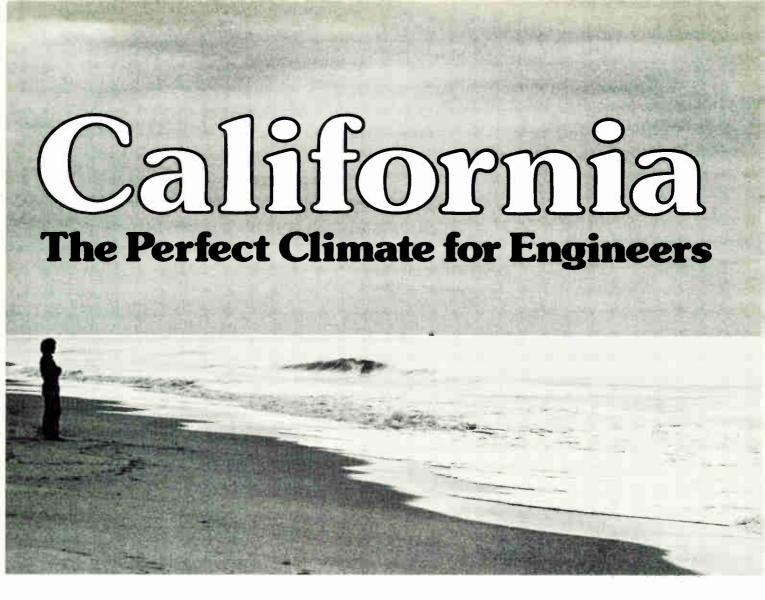
This unique product eliminates the primary problem inherent in silver cased wet tantalum capacitors namely, the interaction between the silver case and the electrolyte. The Puritan Type AT all tantalum capacitor offers a far better capacitance stability and lower

E.S.R., and a higher ripple current handling capability than its silver cased counterpart. Moreover, Puritan has a reverse voltage capability of 3 V. d.c. at 85°C. Capacitance range 2.5 to 1200 mfd; 6 to 100 Volt. Write or 'phone for further data.

Tansitor PuriTan capacitors

Tansitor Electronics, Inc.

West Road, P.O. Box 230, Bennington, Vermont 05201 Phone: (802) 442-5473 TWX: (710) 360-1782 Tansitor - reliable in so many ways



Engineers seeking a career with a future, above-average working conditions, high starting salaries, some of the best technical schools in the country for career advancement, plus a pleasant climate and lifestyle should seriously consider California.

The Golden Gate State offers great employment opportunities for engineers, especially those with EE and aerospace/aeronautical disciplines. To give you an idea of the state's tremendous demand for engineers, in 1978 schools in the United States graduated 54,740 engineers. At that time, companies in Southern California were seeking 30,000 engineers to fill their various and vital job requirements. The growth of this sector of the California economy has been phenomenal. The demand for engineering talent in the 1980s and beyond is essential for the state, for industry and for government needs.

Electronics represents a significant portion of California's manufacturing activity. This high-technology area

employs over 400,000 residents who receive some \$6 billion in wages on an annual basis.

According to Census estimates, California has:

- Over 200 computer-production parents or subsidiaries—30% of the nation's total.
- Over 400 producers of electronic equipment and systems—about 22% of the U.S. total.
- About 750 electronic component production operations—30% of the U.S. total.

There are more than 3,700 separate business locations in California that are classified as part of the electronic/electric equipment market.

The significance of California's rapidly-growing electronics industry is particularly evident in certain geographical areas of the state, mainly the metropolitan areas of Anaheim-Santa Ana; Los Angeles, Long Beach; San Jose; and San Diego. These four areas account for more than 89% of the industry's

employment and 82% of the number of electronic/electric products firms.

A close look at employment trends in these metropolitan areas reveals that the electronics industry has been a dominant factor in each area's economic growth. In San Jose's famed Silicon Valley, for example, total manufacturing activity increased by 25,200 workers during the 1973-1977 period, with the electronics industry contributing 14,800 workers, or 59% of the growth.

Though Silicon Valley is now overcrowded, *Electronics* magazine (Feb. 20, 1980) reports "... even the established companies expect that this area will continue to be the jumping-off point for new companies excited about taking electronic technology to new applications.

"That is the key. To a large extent the new companies in the VLSI area will be those that apply microcomputers in new ways and develop new markets. Examples of this trend are already around us. Look at the toy and game industry,







Photo by Joel Gordon, DPI

which until a few years ago was basically a cardboard and plastics business. Today all the major concerns are up to their elbows in electronics.

"Yes, the stakes are high in VLSI. But the outlook is for a decade of expansion. The migration of engineers to new industries will continue."

The result is a growing number of jobs for engineers in California.

The aerospace/aeronautical and the electrical/electronic industries are intricately related. Enrollment for aerospace/aeronautical engineers is about 50% below that of 10 years ago as a result of the cutback in the space program. This is one of the reasons for the great demand for engineers now and in the future.

In an effort to encourage engineers to work in California, many companies are offering incentives. Housing, for example, is a problem in California. To ease this problem, some companies are helping engineers and their families find

suitable housing. This includes paying lodging costs until a house is found and also the closing costs on the house in some instances. In other cases, engineers recruited to work in California are offered companyowned condominiums at reasonable rents.

In addition, some companies are offering engineers who want to pursue their careers in California sign-up bonuses that can amount to several thousand dollars. They may also provide experts to solve tax problems at no extra cost.

Once on the job, the engineer is encouraged to upgrade his or her skills. Many companies pay full tuition costs for engineers who want to obtain a master's or PhD degree. In-house training to update one's skills or to learn new skills is provided by cassette on the company premises. Another method used for engineers' on-the-job education consists of closed-circuit television, with programs beamed from colleges and universities to the company classroom. This is an excellent way to upgrade skills at no cost or inconvenience to the engineer.

California's lifestyle is famous. The engineer who chooses to live and work in this beautiful 1,000-mile-long



California's Lt. Governor, Mike Curb. Engineers are in great demand in the 1980s.

state bordering the Pacific Ocean can enjoy every type of cultural and recreational activity available any place in the world. The ocean, lakes, desert and mountains—California has them all.

Let's look at the state on an areaby-area basis where both EEs and aerospace/aeronautical engineers are in demand. In Los Angeles
County's Los Angeles-Long Beach Metropolitan Area, according to a recent forecast by the United California Bank, "Aerospace will again be a key sector generating new job opportunities, with demand for workers strong in aircraft manufacturing and electrical machinery."

In Orange County's Anaheim-Santa Ana-Garden Grove
Metropolitan Area, the forecast says,
"Aerospace should continue to be
responsible for a large share of job
gains, including substantial increases
among various electronic firms."

And in The San Diego Metropolitan Area the forecast is that "... aerospace will provide a major thrust to economic activity in 1980. Employment gains will thus be sizable among firms involved in aircraft, missiles, instruments and electronics."

The outlook for Santa Clara
County's San Jose Metropolitan Area
is: "Employment gains will be
bolstered by the dominance of hightechnology industries, including
electronics and instruments. The
slower growth in capital spending
expected nationally is likely to have
some moderating impact, but the
strong momentum of the aerospace
industry, together with sizable export
demand, should lead to substantial
gains."

That's the optimistic outlook for engineers seeking employment in EE and aerospace/aeronautical.
California is the uncontested leader when it comes to hiring engineering talent. It hires more engineering graduates, more engineers with master's degrees and more engineers with PhDs than any other state. And the trend will continue.

In short, California is the perfect climate for engineers. If you are graduating from engineering school this year, are a recent graduate or a veteran engineer looking for a virtually guaranteed career with a future, don't miss the following California Career Opportunities Section that features specific companies seeking EE and aerospace/aeronautical engineers with your talents.

Our most important resource is OUR PEOPLE

Founded in 1888 on the invention of the first adding machine, Burroughs has grown to become a major corporation serving all the aspects of the recording, computation, editing, processing and communication areas.

Our philosophy is to encourage and maintain strong resources for continued product invention, development, manufacturing and marketing.

Right now, we have leadership positions open involving the development of a state-of-the-art optical computer memory.

LEAD CIRCUIT DESIGN ENGINEER Optical Computer Memories

Your job responsibilities include the design of analog and digital signal processing circuits for control systems and data storage. These functions will be implemented with monolithic integrated circuits as well as thick and thin film hybrid circuits. It is required that you have a strong background in worst case circuit design theory, transistors and OP amp design. Experience with wide bandwidth (20mhz) low noise analog circuits is desirable.

You will be working with several engineers on this project. A minimum of five to seven years applicable experience and a B.S.E.E. are required.

Burroughs Westlake is located away from traffic and noise in a beautiful country setting, yet just a short drive to downtown Los Angeles and our beaches

We offer an excellent compensation and benefits package as well as company paid holidays, sick leave, life and family health insurance plus a stock plan.

Please send your resume or call collect:

Burroughs Corporation Optical Engineering Dept. E 5411 N. Lindero Canyon Road Westlake Village, CA 91361 (213) 889-1010

Affirmative Action/Equal Opportunity Employer

Burroughs

Circle A on the Resume Forwarding Page

Field Sales Engineers Field Applications Engineers

"Intel's success affords our people many opportunities for rapid growth and advancement."

--Bill O'Brien, Western Regional Sales Manager

"There are 8086 reasons why you should call us today to pursue a sales career at Intel."

-- Gerry Lawrence, Northwest Regional Sales Manager

Is profitability important? You bet it is -- because our success is based on reinvesting these earnings in continued research and development -- all in leading edge technology. This concentration on proprietary products lets us command and develop key market segments to minimize our vulnerability to economic cycles.

As you can see, we take success seriously. So if you are an aggressive, innovative individual with a BSEE or equivalent and at least 3 years' microcomputer design experience, please call Bill O'Brien at (714) 835-9642, or Gerry Lawrence (408) 987-8086 collect for further information.

Join Us At NCC. Stop by our booth and speak with Bill O'Brien and others about how Intel delivers career solutions by offering new and complex challenges.

If you are unable to call or see us at NCC, please send your resume or call Joyce Cordi at Intel Corporation, Dept. 19BD, P.O. Box 3078, Santa Clara, CA 95051; (408) 987-6298. An equal opportunity employer m/f/h.



Circle 8 on the Resume Forwarding Page

Telecommunications

15 Years Profitability And Technological Innovation... A Winning Combination

Siliconix is the world's leading manufacturer of FET's and analog switch IC's. Our innovative technology has generated a variety of new products, including IC's for telecommunications and analog-to-digital conversion.

Share this winning combination with us. Our salaries are competitive, and our outstanding employee benefits include profit sharing stock purchase plan, and our own discount gas station!

Telecommunications Applications Engineer

You will define and specify new telecommunications IC's, creating new designs and generating applications literature. This position entails heavy customer interface, requiring some travel. You should have a minimum of a BSEE plus 3 or more years in telecommunications hardware development (digital PCM switches, PCM line circuits, channel banks, or telephone sets). Other requirements include familiarity with design techniques and terminology, and writing ability. Experience with microprocessor hardware/firmware would be a plus.

Please send your resume in confidence to Jean Sullivan, M/S 55-105, 2201 Laurelwood Road, Santa Clara, California 95054. Or call (408) 988-8000, extension 215.



An Equal Opportunity, People-Oriented Employer

ENGINEERS & COMPUTER SCIENCE PROFESSIONALS

Join Lockheed on the San Francisco Peninsula

Lockheed Missiles & Space Company is a name worth remembering. Our career opportunities have never been better for professionals eager for a challenging, responsible, meaningful environment. Your talents will expand with the diversification of programs we have to offer, and your lifestyle will be pushed to its limit with nearby beaches, ocean fishing, boating, wine country, fine schools, theatres, sporting events, and our year 'round sunny, fresh air atmosphere.

ELECTRONICS

SYSTEMS ENGINEERING

Development and analysis of advanced communication command and control systems in support of satellite missions and tactical and strategic operations. Will include application of advanced ECM/ECCM techniques.

MICROELECTRONICS

Develop wafer fabrication processes for fabrication of GaAs, SOS, TTL, and MOS integrated circuits.

COMMUNICATIONS

Wideband/Secure Communications systems. We need engineers to design systems involving spread spectrum, frequency hopping, and error correcting coding.

RADAR SYSTEMS

Positions available in systems and signal processor design involving SAR and other sophisticated concepts.

COMPUTER SCIENCE

ADMINISTRATIVE PROGRAMMERS

Experienced Administrative Programmers to work on large scale applications. Requires a Degree and two years experience in Administrative Applications.

SYSTEMS PROGRAMMERS

Requires experience at assembly language level with knowledge in any one of the following systems software areas: Operating Systems; Communications; Teleprocessing; Interactive Systems, Associated Languages, and N/C APT and Graphics..

SOFTWARE

Conduct research to establish effective hardware/software tradeoffs. Develop methodology for and coordinate development of software design specifications using state-of-the-art mini and microcomputers.

DATA BASE SYSTEMS

Design and development of an integrated corporate data base for Financial, Manufacturing, Engineering, Procurement, and Logistics Systems.

CADAM IMPLEMENTATION

Perform overall coordination of CADAM implementation of all Space Systems Manufacturing applications. Utilize CADAM in support of initial Numerical Control and Tool Design inputs for Space Systems Division.

Most of these positions require an appropriate degree and U.S. citizenship. Several positions offer opportunities at all levels. Interested?

For immediate consideration, please forward your resume to Professional Employment, Dept. EL-522, P.O. Box 504, Sunnyvale, CA 94086. We are an equal opportunity affirmative action employer.

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MISSILES & SPACE COMPANY



Engineering Development And Applied Energy Research

Technically Challenging Work in Multi-Disciplinary Teams

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WITH

... Extensive equipment, technical personnel and facilities support ... On-site advanced degree and non-degree programs ... Three weeks' vacation

... Quick access to San Francisco Bay Area, ocean, mountains

DISCUSS YOUR INTERESTS WITH AN ENGINEERING MANAGER

Resumes may be sent in strict confidence to George Kumparak, Professional Employment Division, LAWRENCE LIVERMORE LABORATORY, P.O. Box 808, Dept. KET-050, Livermore, CA 94550. Or call Ed Lafranchi, Department Head, collect at (415) 422-8373, for more information. U.S. Citizenship is required. We are an equal opportunity employer M/F.



An Equal Opportunity Employer M F

Software Engineering Professionals A New Era...

...has begun at Advanced Micro Computers. Our engineers and programmers are involved in projects that will make an impact on the future of the entire industry.

Our atmosphere, our energy, our outlook reflect our youth. Our stability, our maturity, and our resourcefulness reflect the support of Advanced Micro Devices.

Join us at the onset of a new age in microcomputer design and development. We have the following opportunities for software engineers:

Operating Systems

Sr. Software Engineer Software Engineer

These positions include responsibility for the design and implementation of operating systems components. Both require a BSCS or BSEE along with appropriate program design and development experience in operating systems. Your background must include multi-user/multi-tasking systems, related peripheral equipment handling, file management and task scheduling, preferably in a mini computer environment. Exposure to systems implementation language would be beneficial.

Language Development

Sr. Software Engineer Software Engineer

As members of the implementation team, your responsibilities will entail implementation of systems program languages. A BSCS or BSEE is required (MS preferred), along with at least 3 years' experience in compiler design (particularly code generation) for block structured languages such as Pascal or C.

Quality Assurance/Reliability Software QA Engineers All Levels

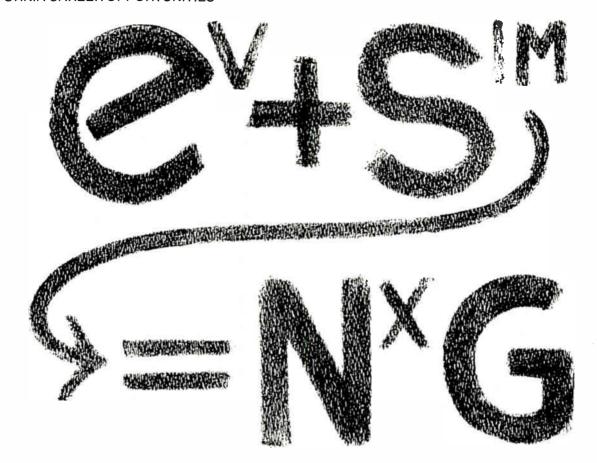
Positions exist at various levels for individuals to assist in developing QA methods and test procedures for our existing software projects. In addition, you will be involved with the development team for future software products. Requires a BSCS, BSEE or equivalent. Programming experience with mini or micro computers, 8080, Z8000, CP/M, Pascal or C is desired.

To learn more about how you can become a part of the new stage of development at Advanced Micro Computers, call **Shirley Boyer COLLECT** at **(408) 988-7777**, or send your resume to her at **3340 Scott Blvd., Santa Clara, California 95051.** An equal opportunity employer m/f/h.



ADVANCED MICRO COMPUTERS

Circle F on the Resume Forwarding Page



Evolution + Simulation = The Next Generation

At Link's Advanced Products Operation in Sunnyvale, CA, on the scenic San Francisco Peninsula, we're involved with developing the next generation of real-time computer graphics for ever-expanding applications of out-the-window scene and radar simulation technology utilized primarily for, but not limited to, total flight crew training for commercial, military and space end users.

Recent developments in the high technology field of simulation have virtually tripled our personnel needs for highcaliber, creative individuals with degrees or equivalent training, and background in the following areas:



A DIVISION OF THE SINGER COMPANY

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At Link you will enjoy continued opportunity for career enhancement, a competitive salary that includes a professional overtime payment plan, and a comprehensive benefits plan including 100 percent advance tuition payment ... plus much more! Interested? We hope so and we invite you to respond with letter or resume, or for immediate consideration call us toll free or fill in and mail the coupon below to: Personnel Office, LINK, 1077 E. Arques Avenue, Sunnyvale, CA 94086. At Link, we're proud to be an equal opportunity employer M/F/V/H.

Nam <i>e</i>				
Name Address				
Phone (Home)	(Work)			
Position Applying For:				
Education & Expe	rience:			
Present Salary:				
	anent Resident?			



Join us at nuglies.

Come join our engineers working on advanced test systems for airborne and spaceborne radar avionics; tactical systems guided by lasers, TV, and infrared control; and computer-controlled trainers and simulators.

At Hughes Support Systems, our role is the design and development of these systems, as well as training of customer personnel, maintenance and operation worldwide. We need your know-how, and we'll reward you well if you can handle one of these responsible jobs:

 Design of automatic test systems ● Digital hardware development ● Electro-optical equipment design ● Field system engineering ● Maintainability analysis ● Product support engineering ● Real-time software ● RF circuit design

Hughes offers you a home base in the easy-living climate of southern California, near LA International Airport and beach communities; excellent salary and benefits; and this unique brand of stability:

Our company has a backlog of over \$4½ billion in contracts comprising 1,500 different projects. When we complete one, there are a lot more challenges waiting, at Hughes.

Let's talk about what you and Hughes can do for each other. Call collect to (213) 641-6691, or send your resume to:

Hughes Aircraft Company Support Systems Department 046, Professional Employment, P.O. Box 90515, Los Angeles, CA 90009.

HUGHES

Creating a new world with electronics An equal opportunity employer, M/F/HC U.S. Citizenship required



Looking for a go-ahead career? Start where GROWTH OFFERS OPPORTUNITY.

General Dynamics is the nation's largest defense contractor. The Pomona Division is the Free World's leading producer and developer of tactical missiles and advanced weapons systems including Standard Missile-1, Standard Missile-2, Stinger, DIVAD, RAM, Viper, Sparrow AIM 7-F, Phalanx, Assault Breaker and more. These programs provide a continuing challenge for creative engineers in a growing company that is meeting America's defense needs for tactical systems.

At Pomona, advancing and applying state-of-the-art in engineering is a way of life.

The Pomona location offers a wide variety of lifestyles where every conceivable form of recreation is readily available year-round, with major entertainment offerings in nearby Los Angeles. General Dynamics offers you a chance to move to a company where growth does indeed mean career opportunities.

Professional openings range from entry level for recent college graduates to highly experienced employees in a wide spectrum of engineering disciplines:

Digital & Analog Circuit Design **Guidance & Control** Systems Engineering EMI/EMC **Test Equipment Design Electro-Optical Telemetry Systems** Microwave/Antenna Fire Control Design **Microelectronics** Microprocessor Design **Engineering Writers** Hydraulic Design Reliability **Power Supply Electronic Packaging Test Systems Radar Systems** Signal Processing

Components
Stress Analysis
Electro-Mechanical Design
Auto Pilot Design
Servo Design
Logistics
ATE Design
Propulsion
Manufacturing Engineering
Industrial Engineering

Send your letter or resume for prompt technical review. You'll hear from us soon.

R.M. Kemp Vice President, Research & Engineering GENERAL DYNAMICS Pomona Division, Dept. 426 P.O. Box 3011, Pomona, CA 91766

An Equal Opportunity Employer M/F/H' U.S. Citizenship Required

GENERAL DYNAMICS

Pomona Division

Circle I on the Resume Forwarding Page

ENGINEERS AND ELECTRONIC TECHNICIANS

Today Magnavox Advanced Products and Systems Company is playing a key role in the most revolutionary advance in the history of navigation and position determination — the Navstar Global Positioning System. Navstar is an anti-jam, real-time determination of position, time and velocity, even under severe dynamic conditions.

Meeting the great challenges of the future depends entirely on the people employed at **Magnavox** ... people like you — who are provided the opportunity to grow with **Magnavox** and pursue areas of technology among the most advanced in the electronics field

"NO OTHER COMPANY IN THE WORLD COMES CLOSE TO pride ourselves on having the people who can create and develop these resources into superior products.

Magnavox has outstanding resources for engineering, research, design, and manufacturing and we pride ourselves on having the people who can create and develop these resources into superior products.

This represents an enormous advance for both military and commercial positioning. It is made possible by Navstar's successful marriage of satellite navigation and spread-spectrum technologies: fields in which **Magnavox** exercises undisputed leadership.

If you are seeking a future where there is a diversity of technological challenges, complete involvement with projects, a strong management team and a stimulating work environment conducive to your professional growth, this is your opportunity to join a very successful electronics team . . . MAGNAVOX!

Current Career Opportunities:

ENGINEERS

- Analog Engineers
- LSI Engineers
- Power Supply Engineers
- Systems Mechanical Engineers
- Components Engineers
- Digital Design Engineers
- Systems Test Engineers
- Hybrid Engineers
- RF Design Engineers
- Sr. Communication System Analysts

ELECTRONIC TECHNICIANS

- System Test Technicians
- Power Supply Technicians
- RF/IF/L Band Technicians
- Components Technicians
- Calibration Technicians
- Analog Technicians
- Digital Technicians
- Electronics Failure Analysis

Join the Leader . . . Challenging Careers Now and for the Future!

We are an equal opportunity employer. Women, minorities

Professional Placement, Dept. ELEC-522 2829 Maricopa Street Torrance, CA 90503

and handicapped individuals are encouraged to apply



ELECTRONICS' FREE RESUME FORWARDING SERVICE

for California employment advertisements only

If you're interested in any of the companies advertising in the preceding California Career Opportunities Section, but you don't have your resume ready and/ or up-to-date, why not fill out and return the handy form below?

Then, as a free service, ELECTRONICS will xerox and send copies of same to as many companies as you indicate interest in by circling in the box at right.

After that, it's up to you and them—and good luck!

RESUME FORWARDING SERVICE BOX

To have ELECTRONICS xerox and forward a copy of your completed and returned resume form to any of the companies advertising in the preceding California Career Opportunities Section, just circle the letter below that corresponds to the letter listed under their ad.

ABCDEFGHIJKLM NOPQRSTUVWXYZ

Also, if you're actively job-seeking and willing to work anywhere in this wide world, why not consider placing this same resume in the Electronics Manpower Register, a computerized system which matches your qualifications to the requirements of industry employers.

To do so, just check off the box at the top of the form below. Remember, it's completely confidential, you'll be called before your name is placed on computer, and there's no charge to you.

☐ Check this box if you want this resume to be included in the Electronics Manpower Register	REE RESUME ALIFORNIA E	MPLOYMI	DING SERVI ENT ADVER ete and that you type or print	TISERS ONL	Y sun	Check this box it want this re- ne to be included the Electronics appower Register
IDENTITY			PRESENT OR MOST RECE	NT EMPLOYER		,
Name		Date	Parent company			
Home address			Your division or subsidiary			
City	State	Zip	Location (City/State)			
Home phone (Include Area Code)			Business Phone (If OK to	use)		
Education: List Degrees		Major Field	Year Degree Earned	Colle	ge or University	
Employment Information Position Desired	on:			-		
Industry of Current Employer						
Present or Most Recent Position From	To Title					
Duties & Accomplishments						
Reason for Change						
Previous Position Employer		City/State		From	То	
Division		Type Industry		Salary		
Duties & Accomplishments						
General Information: s	ummarize your overall qualificati	ons and experience in you	ır field.			
Salary Desired						
Min Salary						
Current Annual Base Salary						
Bonus	Total Years Experience	Date Available	Employed □	Unemployed □	Self Employed □	Married □ Single □
Level of Security Clearance		US Citizen □	Non US Citizen □	l will travel:	light □ moderate	□ heavy □

MAIL TO: ELECTRONICS, P.O. BOX 900, NEW YORK 10020

Manufacturing Test Development Manager

Take the lead in a key function in telecommunications technology

With an international reputation in telecommunications, this well established research center in Shelton, Connecticut is pushing the state-of-the art in telephone technology for new generations of service worldwide. Work now underway in advance systems and equipment provides new opportunity for a technical leader with pronounced talents in manufacturing test development.

You'll be heading a group responsible for product testability and for developing new test techniques for these new systems including new versions of ITT's highly innovative System 12 digital switching facility, and for liaison functions with U.S. and overseas manufacturing plants. To qualify, you should have good working knowledge in the following areas:

- Digital LSI Board testing, ATE and Programming
- Line and trunk circuit testing
- Microprocessor and memory testing
- Functional unit testing of digital switching equipment
- Systems testing of digital switches

Our Shelton location in famed Fairfield County, Connecticut offers bountiful opportunities for the good life. Flexible housing to suit all tastes in areas free from urban pressures and pollution. Water sports on Long Island Sound. Facilities for year-round recreation. The cultural attractions of readily accessible metropolitan cities. No State tax on earned income. And to put it all within your reach, full ranging ITT benefits include a home purchasing program and mortgage assistance.

For further details, send resume with salary requirements to Mr. Eugene Edwards, ITT Telecommunications Technology Center, One Research Drive, Shelton, Conn. 06484.

TITE Telecommunications Technology Center

An Equal Opportunity Employer, M/F

rstems Engineers

There will never be another opportunity like this... an opportunity to choose from such a broad range of disciplines and responsibilities.

Be a part of the largest systems program ever undertaken. The Strategic Systems Division of GTE's Sylvania Systems Group has embarked on the largest and most complex C3 system ever conceived. The challenges and opportunities presented by this long-term program are mind-boggling.

The MX C3 program will involve the world's largest fiber optic cable network, over 15,000 Kilometers; a radio communications systems incorporating over 600 VLF, MF, HF, VHF, UHF, and SHF radios; a hierarchy of over 5000 computers; and one of the largest software communications networks ever developed.

Although the design, development and implementation of this system will extend far into this decade, the real challenges AFARO FABER MONGOL AF and opportunities exist now, at the beginning. The capability demonstrated by Strategic Systems Division in winning this program will be applied to future major programs. We are committed to being the major strategic systems organization of the future.

Opportunities for Systems Engineers exist at every level of experience up to managerial in the broadest range of disciplines available anywhere. There will never be another opportunity like this...an opportunity to choose from such a broad range of disciplines and responsibilities.

You Have Everything To Gain and Nothing To Lose.

For immediate information, please phone Kevin J. Cronin at (617)449-2000, Ext. 3275, or just check off the level of responsibility and technical areas of interest to you. Give us a brief summary of your background. Mail this ad back to us. And we'll do the rest.

Address City Phone

Or, if you prefer, forward your resume indicating position(s) of interest to Kevin J. Cronin, Sylvania Systems Group, Strategic Systems Division 189 "B" Street, Needham, MA 02194.

Desired Level of Responsibility

- Engineer
- Sr. Engineer
- Principal Engineer
- □ Project Engineer
- □ Engineering Supervisor
- □ Engineering Manager

SYSTEMS ENGINEERING **Systems Analysis**

Concept Development

- C3 Operational Concept Development
- □ Command and Control Analyses
- Trade Studies and Analyses
- □ Definition of Communication Interfaces

Simulation and Modeling

- ☐ Network Traffic Modeling
- ☐ Math Modeling and Simulation to Validate Systems Performance
- □ Trade Studies and Analyses
- □ C⁴ Simulation Requirements

Systems Architecture

- Nodal Integration Multi-Subsystems Activities and Trade Studies Coordination
- Development of Nodal Equipment Block Diagrams
- Trade Studies and Analyses ☐ Interface Design

SRA and Integration

Operational Analysis — Cable Systems

- ☐ Cable Architecture Requirements
- Cable System Requirements
- Data and Voice Terminal Requirements
- ☐ Timing and Synchronization
- ☐ HW/SW Partitioning
- Secure Interfaces
- □ BIT/BITE Requirements

Operational Analysis — Radio Systems

- □ Radio Architecture Requirements
- Radio Systems Requirements
- П Radio Terminal Requirements Antenna Requirements
- Timing and Synchronization
- HW/SW Partitioning
- **BIT/BITE Requirements**
- Secure Interfaces
- □ Airborne Radio Requirements

Operational Analysis — Command & Control

- □ Nodal Considerations/Integration
- Commands
- Status/Maintenance Requirements
- □ Processors/Memory
- Displays
- Security
- Secure Equipment and Interfaces
- □ Sub-system Interface Definition
- Communication Integration/Interface and Controls
- ☐ System Simulation Requirements

Operational Software

- ☐ Higher Order Language
- PDP 11 Architecture
- Computer Security
- Remote Software Change
- Communication Processing Real Time Command/Control Processing
- Compiler Development Support
- Bench Marking Performance Trade Offs
- ☐ Airborne Unique Software Requirements

Systems Integration

- □ Test Planning Analyses
- Logistic Support Analyses A & CO Technical Analyses
- Operational Analyses
- Maintenance Analyses

System Requirements Development

- □ Functional Flow Diagrams
- □ Forms B Functional Requirements B-1 Prime Item Development Specifications
- **B-5 Computer Program Development**
- Specifications
- □ Operational/Maintenance Time Lines

Command and Control

Communication and Control Software

- □ Operating Systems Including Secure Operating
- Communications Software
 - Command Generation and Operational Status
- Monitoring Software
- **CAMMS Software**
- Code Processing Software
- Personnel Authentication Software
- Auxiliary Software
- Diagnostic Software



	Requirements Definition
Systems Operability	Ground-Based Antenna Systems
Systems Operability Concept Man-Machine Interface Displays and Controls	 □ Wideband MF Broadcast Antennas □ UHF/SHF Satellite Terminal Antennas □ VLE HE VHF and UHF Antennas
Processors and Interfaces	☐ VHF Mobile Radio Antennas
 □ Processors □ Bulk Store Technology □ Processor Interfaces □ Performance Trade Offs 	Airborne Antennas MF Trailing Wire Antennas MF Ferrite Luop Antennas UHF/SHF Satellite Antennas
C ² Subsystem	□ VLE HE VHE UHE and SHF Antennas
☐ Data Network Architecture Requirements	Cable Systems
 ☐ MF Radio Protocols ☐ Fiber Optic Cable Protocols 	Voice Communication
☐ Communications Protocols ☐ Message Formats ☐ Message Responses	 □ Secure Voice Order Wire Communic □ Secure Voice Switched Network □ VHF Mobile Radio Communication
Radio Systems	Data Communication Section
radio systems	Data Communication Section
Communications Measurements and Analysis Wideband Atmospheric Noise Measurements Rough Terrain Surface Wave Propagation	Cable Data Network Architecture Cable Nate Noting Protocol Network Traffic Modeling Survivable Cable Communication Network
Communications Measurements and Analysis Wideband Atmospheric Noise Measurements	☐ Cable Data Network Architecture☐ Cable Network Routing Protocol☐ Network Traffic Modeling
Communications Measurements and Analysis Wideband Atmospheric Noise Measurements Rough Terrain Surface Wave Propagation Measurements	□ Cable Data Network Architecture □ Cable Network Routing Protocol □ Network Traffic Modeling □ Survivable Cable Communication Network Traffic Modeling □ Survivable Cable Communication Syste □ Fiber Optic Cable Connectivity □ Fiber Optic Modem Design
Communications Measurements and Analysis Wideband Atmospheric Noise Measurements Rough Terrain Surface Wave Propagation Measurements Propagation Analysis Mobile VHF System Analysis/Design	Cable Data Network Architecture Cable Network Routing Protocol Network Traffic Modeling Survivable Cable Communication Ne Fiber Optic Cable Connectivity Fiber Optic Modem Design Fiber Optic Cable Plant Design
Communications Measurements and Analysis Wideband Atmospheric Noise Measurements Rough Terrain Surface Wave Propagation Measurements Propagation Analysis Mobile VHF System Analysis/Design Communications System Testing Concepts/Analysis Radio System Design Higher Order Modulating Technology Error Detection and Correction Spread Spectrum Communications	□ Cable Data Network Architecture □ Cable Network Routing Protocol □ Network Traffic Modeling □ Survivable Cable Communication Network Traffic Modeling □ Survivable Cable Communication Syste □ Fiber Optic Cable Connectivity □ Fiber Optic Modem Design
Communications Measurements and Analysis Wideband Atmospheric Noise Measurements Rough Terrain Surface Wave Propagation Measurements Propagation Analysis Mobile VHF System Analysis/Design Communications System Testing Concepts/Analysis Radio System Design Higher Order Modulating Technology Error Detection and Correction	Cable Data Network Architecture Cable Network Routing Protocol Network Traffic Modeling Survivable Cable Communication Ne Fiber Optic Communication Syste Fiber Optic Cable Connectivity Fiber Optic Cable Plant Design Fiber Optic Component Evaluation Mechanical Systems of Interfaces Environmental Constraints Analysis NH & S (Mechanical)
Communications Measurements and Analysis Wideband Atmospheric Noise Measurements Rough Terrain Surface Wave Propagation Measurements Propagation Analysis Mobile VHF System Analysis/ Design Communications System Testing Concepts/ Analysis Radio System Design Higher Order Modulating Technology Error Detection and Correction Spread Spectrum Communications Modeling and Performance Estimation Implementation Feasibility Considerations	Cable Data Network Architecture Cable Network Routing Protocol Network Traffic Modeling Survivable Cable Communication Ne Fiber Optic Cable Connectivity Fiber Optic Cable Connectivity Fiber Optic Cable Plant Design Fiber Optic Component Evaluation Mechanical Systems of Interfaces Environmental Constraints Analysis NH & S (Mechanical) Packaging Concepts
Communications Measurements and Analysis Wideband Atmospheric Noise Measurements Rough Terrain Surface Wave Propagation Measurements Propagation Analysis Mobile VHF System Analysis/Design Communications System Testing Concepts/ Analysis Radio System Design Higher Order Modulating Technology Error Detection and Correction Spread Spectrum Communications Modeling and Performance Estimation Implementation Feasibility Considerations MF Radio Conceptual Design	Cable Data Network Architecture Cable Network Routing Protocol Network Traffic Modeling Survivable Cable Communication No Fiber Optic Communication Syste Fiber Optic Cable Connectivity Fiber Optic Cable Plant Design Fiber Optic Cable Plant Design Fiber Optic Component Evaluation Mechanical Systems of Interfaces Environmental Constraints Analysis NH & S (Mechanical)

Antenna Systems Hardened Antenna Development	 □ Secure Communications Equipment Integration □ Computer Security □ Code Processing □ Security Studies
□ VLF/MF/HF Buried Antennas	Hardness and Survivability
☐ Triplexer Development ☐ Erectable HF Antennas	EMP Analysis and Test
UHF/SHF Satellite Terminal Antennas EMP Mitigation Techniques and ESA Requirements Definition Ground-Based Antenna Systems	EMP Analysis SGEMP Analysis EMP Test Requirements Analysis
Wideband MF Broadcast Antennas	☐ Allocations Analysis ☐ EMI/TEMPEST
□ UHF/SHF Satellite Terminal Antennas	Radiation Analysis and Test
□ VLE HE VHF and UHF Antennas □ VHF Mobile Radio Antennas	☐ Analysis
Airborne Antennas	☐ Requirements Analysis ☐ Test
☐ MF Trailing Wire Antennas ☐ MF Ferrite Loop Antennas	Special Studies
☐ L'HF/SHF Satellite Antennas ☐ VLE HE VHE UHE and SHF Antennas	☐ Hardness Assurance/Maintenance ☐ Subcontractor Support ☐ Thermal/Mechanical
Cable Systems	☐ Fiber Optics
Voice Communication	Maintenance Systems
 □ Secure Voice Order Wire Communication □ Secure Voice Switched Network 	On-Line Maintenance Subsystem
□ VHF Mobile Radio Communication	Subsystem Design
Data Communication Section	 □ Nodal Requirements Allocation □ Maintenance Management (CAMMS)
Cable Data Network Architecture Cable Network Routing Protocol Network Traffic Modeling Survivable Cable Communication Network	Maintenance Monitoring and Control BITE, BIT, SELF TEST Requirements Fault Error Requirements Man-Machine Interface Functions HW/SW Allocations
Fiber Optic Communication System	SW Architecture
☐ Fiber Optic Cable Connectivity ☐ Fiber Optic Modem Design	Off-Line Maintenance Subsystem
☐ Fiber Optic Cable Plant Design ☐ Fiber Optic Component Evaluation	☐ Intermediate Level/Depot Level MSE ☐ ATE Subsystem Design ☐ Integration of IL/DL Functions
Mechanical Systems and Inte rf aces	IL/DL Repairable Items IL/DL Repairable Items IL/DL Test Requirements Test Station Requirements
C Project montal Constraints Analysis	in the common recommendation in the commendation in the commendati

Security Systems

Operating and Diagnostic SW Requirements
 Test Applications SW Requirements

☐ Test Equipment — Fiber Optic, Antenna, ESA
☐ B-3 Portable Tester Specs

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Organizational MSE

□ Requirements

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☐ Cable System Requirements
☐ Site and Facility Interface Requirements

□ Requirements Specification

□ ICD Requirements

□ A & CO Requirements



Systems

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Survivability

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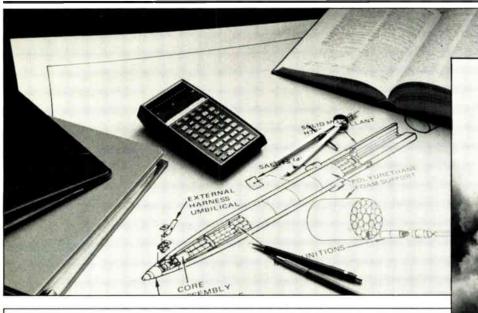
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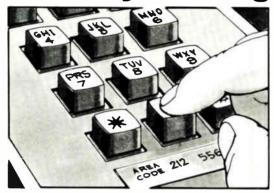
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