JULY 17, 1980

#### **SMART MEMORIES ADDRESS THEMSELVES TO MICROPROCESSORS/92**

Shielding chip and board shipments against static discharge / 115 One-chip microcomputer exposes buses for easy emulation / 126





#### HOW DEPENDENT SHOULD YOU BE ON THE ATE SUPPLIER?

Automatic board test equipment can provide a powerful solution to today's testing needs. But choosing the right system can be a complex and bewildering task, because of all the non-hardware factors to be assessed.

#### Purchase alternatives.

One factor is the question of system responsibility. At one end of this spectrum is a turnkey system. Here the ATE manufacturer assumes total responsibility and the user is dependent upon the supplier for hardware, software and system implementation. At the other end is the do-it-yourself system tailored to your exact application, in which case the user is almost self sufficient. Other alternatives also exist. So how can you choose the right one?

#### Some helpful criteria.

The three most important criteria are: your environment, departmental resources, and the system supplier.

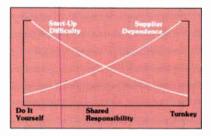
Production environment is critical. How high is the PC board volume? Are the boards extremely complex? How many new products are anticipated? For example, if you have fairly simple boards and few requirements for changes, a turnkey solution may be your answer. But for highly complex boards and a stream of new products, you

may wish to keep expansion and revision control in-house. What about departmental resources? Do you have the technical people to assemble and program a do-it-vourself system? Finally, the

system supplier should be evaluated. Does the company have knowledge of your business and applications engineers familiar with your needs? Will service and support personnel be available when and where you need them?

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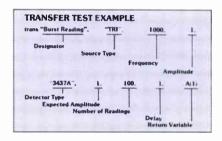
Program Generator (IPG) does the rest, selecting appropriate test methods, determining uncertainty, generating the test program and more. Then, your technical people can easily master BTL (Board Test Language),

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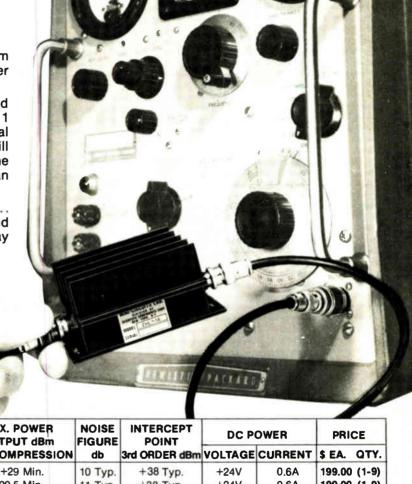
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#### **Highlights**

#### Special report examines the art of data conversion, 101

Data-conversion electronics is getting a healthy shove forward from the success of microprocessors in process control, automotive, and digital signalprocessing applications. Growth in these areas is returning to pique the interest of the big semiconductor houses that make the microprocessors, so that these firms are now increasing the performance, self-sufficiency, and versatility of their monolithic converters. And growing cooperation with the IC makers is proving beneficial to companies building hybrids and modules for high-speed and high-precision conversion applications.

Cover construction is by Robert Strimban.

#### Bell System announces big plans for fiber optics, 89

AT&T's recently disclosed plans for a Boston-to-Washington fiber-optic link represent a milestone. For fiber-optic transmission's long evaluation phase, it marks the beginning of the end. For the technology's serious implementation, the 44.7-megabit/second data highway marks the start.

#### Shielding MOS chips from static-discharge damage, 115

People are among the worst offenders, carrying with them electrostatic charges that can easily damage sensitive MOS circuits. Extra care in handling and board-assembly techniques is not enough: highly conductive materials are needed to serve as shields in the bags, tubes, and boxes in which the devices are transported.

#### **Emulation version bares microcomputer's hidden functions, 126**

The latest generation of microcomputers and microprocessors present testequipment designers with devilish problems: the states of internal registers, buses, even whole sections of logic may not be discernible on the chip's pins. Though costly, one way for chip makers to meet these test troubles head on is to develop special chip versions with additional pads for access to the hidden computer operations.

#### LSI trio calls the tunes in fast, flexible CPU, 130

Large-scale integration of processor logic makes provision for future enhancements difficult at best. A three-chip microcomputer partitioning gives the 16-bit machine an easily expandable microinstruction store—carte blanche for specialized or expanded capabilities.

#### . . . and in the next issue

A complementary-MOS electrically erasable programmable read-only memory . . . a coder-decoder pair with zero crosstalk . . . thermoelectric pumps move heat electronically . . . Multi-ICE software aids dual-processor system development.

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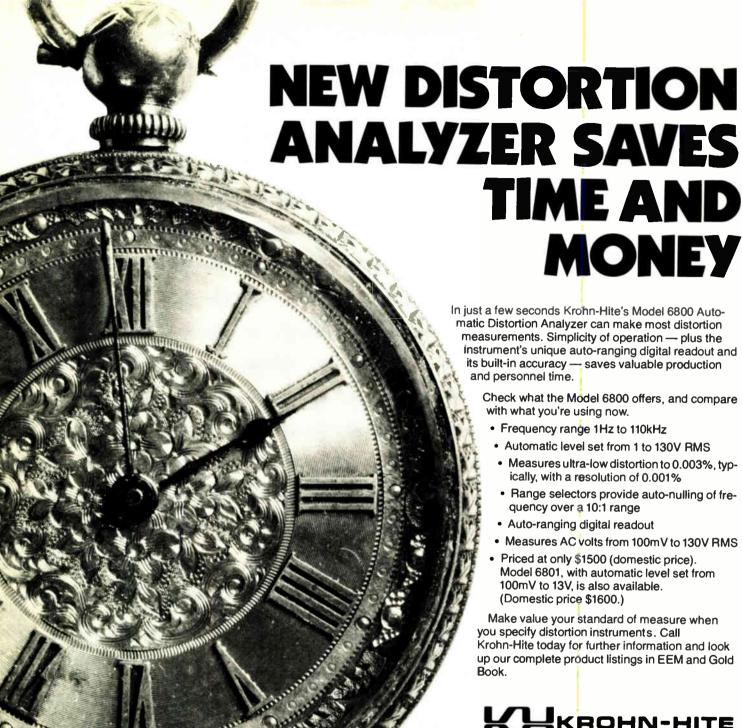
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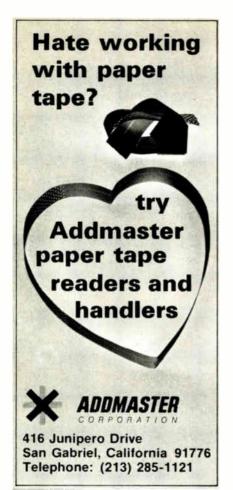




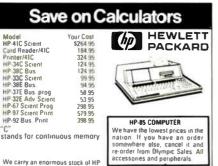
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#### Publisher's letter

Business is good for the manufacturers of data converters, components editor Roger Allan determined as the result of his research done for the special report that begins on page 101. But for the long term, there is an ominous cloud gathering on the horizon for strictly hybrid and modular converter makers.

Giant semiconductor manufacturers that made some monolithic data converters were content to view the data converter market with halfhearted interest at best, but now they have a new outlook. They are convinced that the emergence of the microprocessor has opened very large data-acquisition markets that are capable of supporting volume sales of analog-to-digital and digitalto-analog converters. The result, Allan says, is that for those firms making strictly hybrid and modular units, the impact of monolithic data converters on their business is bound to be noticeable.

As a result, says Allan, the whole converter arena is beginning to lose its neat compartments. Most discussions of data converters have tended to segregate monolithic a-d and d-a devices from those made by hybrid and modular means. Although this demarcation still exists today, the lines are much fuzzier. Monolithic and hybrid and modular converter makers are poaching on each other's territory.

Some makers of monolithic data converters have purchased hybridconverter houses, and companies that once devoted themselves exclusively to hybrids are rushing to master the intricacies of at least integrated-circuit chip design and layout. All sides involved, says Allan, recognize that for the foreseeable future no one technology will predominate and that their interests are best served by a strong hand in both hybrid and monolithic technologies.

It can blow \$50 chips, push costs sky high, and cause much tooth gnashing and consternation. What is this bane of the electronics manufacturer, this phenomenon that has been with semiconductors since Day One? It's electrostatic discharge, a fact of life that no one enjoys living with.

One of the difficulties in combatting the problem is that it crosses the boundaries between disciplines with such ease that it has never been addressed by one technology area never, that is, until two researchers at the 3M Co. in St. Paul came along (see p. 115).

As packaging and production editor Jerry Lyman puts it, "Before Donald Yenni and James Huntsman did their work, there weren't any studies of electrostatic discharge from a scientific viewpoint that included materials and all the other facets of the subject. Yet at every meeting and convention, there are sessions about it and anxious engineers picking one another's brains about what to do.'

What makes the Yenni-Huntsman data so timely is the fact that the problem is exacerbated by the advent of smaller and smaller very large-scale integrated circuits. Because these devices use thinner oxide layers than their predecessors—by almost a third—they have lower voltage breakdown and thus are more sensitive to static discharge. At the same time, the Department of Defense has issued a new specification requiring protection from static electricity when shipping printed-circuit boards, an important change from previous practice.

So it appears that static is finally beginning to be attacked with scientific methodology. As summed up by Roy Walker of the Air Force's Reliability Analysis Center at the Rome Air Development Center in Rome, N. Y., who is in charge of a seminar on the subject to be held in San Diego, Calif., beginning Sept. 9, "We are trying to get more papers documenting this area so that we can alleviate the problem of electrostatic discharge. It is becoming more and more of a problem as parts get smaller."

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#### Readers' comments

#### Interpreting effective bandwidth

To the Editor: "100-MHz oscilloscope displays innovations in digital storage" by Thomas P. Dagostino and Michael R. Turner (May 8, p. 161) contains innovations in information theory and other matters with which we disagree.

First, the authors have assigned a "useful storage bandwidth" far lower than their actual bandwidth to digital scopes, discouraging potential users. No oscilloscope, analog or digital, can accurately show the waveform of a periodic signal to be sinusoidal without a bandwidth far beyond the signal's frequency. Theoretically, to show it as sinusoidal requires infinite bandwidth, but in real situations a factor of 10 or 20 excess bandwidth usually suffices.

The authors have chosen a factor of 12.5 and applied it to digital oscilloscopes unilaterally, indicating that the "effective storage bandwidth" of a 10-MHz digital scope is therefore 800 kHz. The implication here is that only digital scopes are handicapped, which is simply not so.

A 10-MHz digital scope looking at an unknown signal of fundamental frequency 800 kHz will clearly show it as a sine wave if it is, as a triangular wave if it is, and so on. This requires an effective bandwidth that is far beyond the fundamental frequency.

Also, it is not "impossible," despite the claim of the authors, to understand a digital oscilloscope's display when slightly more than two points per cycle are shown. It is easy if there is prior knowledge that it is a sine wave. Without that knowledge, the scope is being misused. Experienced analog scope users avoid looking at signals known to be sine waves near the bandwidth limit, for the only information available without gross error is fundamental frequency. Digital scope operators avoid it for convenience only.

Sine interpolation, which the authors enthusiastically promote, eliminates the inconvenience but in no way enhances "effective" bandwidth. And why should sine interpolation be included in a hybrid scope that is fully capable of displaying

# Interested in higher performance software?

The Mark Williams Company announces COHERENT.™ a state of the art. third generation operating system. The design of COHERENT begins with the basic technology of the highly-acclaimed Western Electric UNIX operating system. From this starting point, it goes on to include further substantial software innovation. The primary goal of COHERENT is to provide a friendly environment for program development. The intent is to provide the user with a wide range of software building blocks from which he can select programs and utilities to solve his problems in the most straightforward manner.

COHERENT and all of its associated software are written totally in the high-level programming language C. Using C as the primary implementation language yields a high degree of reliability, portability, and ease of modification with no noticeable performance penalty.

#### **FEATURES**

COHERENT provides C language source compatibility with programs written to run under Seventh Edition UNIX. enabling the large base of existing UNIX software (from numerous sources) to be available to the COHERENT user. The system design is based on a number of fundamental concepts. Central to this design is the unified structure of i/o with respect to ordinary files, external devices, and interprocess communication (pipes). At the same time, a great deal of attention has been paid to system performance so that the machine's resources are used in the most efficient way. The major features of COHERENT include:

- · multiuser and multi-tasking facilities,
- running processes in foreground and background,
- compatible mechanisms for file, device, and interprocess i/o facilities,
- the shell command interpreter—modifiable for particular applications,
- distributed file system with tree-structured, hierarchical design,
- pipes and multiplexed channels for interprocess communication.
- asynchronous software interrupts,
- generalized segmentation (shared data, writeable instruction spaces),
- ability to lock processes in memory for real-time applications,
- · fast swapping with swap storage cache,

- minimal interrupt lockout time for realtime applications,
- reliable power failure recovery facilities.
- fast disc accesses through disc buffer cache,
- · loadable device drivers.
- process timing, profiling and debugging trace features.

#### **SOFTWARE TOOLS**

In addition to the standard commands for manipulating processes, files, and the like, in its initial release COHERENT will include the following major software components: SHELL, the command interpreter; STDIO, a portable, standard i/o library plus run-time support routines; AS, an assembler for the host machine: CROSS, a number of cross-assemblers for other machines with compatible object format with 'AS' above; DB, a symbolic debugger for C, Pascal, Fortran, and assembler; ED, a context-oriented text editor with regular expression patterns; SED, a stream editor (used in filters) fashioned after 'ED'; GREP, a pattern matching filter; AWK, a pattern scanning and processing language; LEX, a lexical analyzer generator; YACC, an advanced parser generator language; NROFF, an Nroff-compatible text formatter; LEARN. computer-aided instruction about computers; DC, a desk calculator; QUOTA. a package of accounting programs to control filespace and processor use; and MAIL, an electronic personal message

Of course, **COHERENT** will have an ever-expanding number of programming and language tools and basic commands in future releases.

#### LANGUAGE SUPPORT

The realm of language support is one of the major strengths of **COHERENT**. The following language processors will be supported initially:

a portable compiler for the language C, including stricter type enforcement

in the manner of LINT.
 FORTRAN portable compiler supporting the full ANS Fortran 77

PASCAL standard.
portable implementation of the complete ISO standard.

XYBASIC™ a state of the art Basic compiler with the interactive features of an interpreter.

The unified design philosophy underlying the implementation of these languages has contributed significantly to the ease of their portability. In particular, the existence of a generalized code generator is such that with a minimal effort (about one man-month) all of the above language processors can be made to run on a new machine. The net result is that the compilers running under COHERENT produce extremely tight code very closely rivaling that produced by an experienced assembler programmer. Finally, the unified coder and conformable calling sequences permit the intermixture of these languages in a single program.

#### THE OPERATING SYSTEM

In part because of the language portability discussed above, and in part because of a substantial effort in achieving a greater degree of machine-independence in the design and implementation of the COHERENT operating system, only a small effort need be invested to port the whole system to a new machine. Because of this, an investment in COHERENT software is not tied to a single processor. Applications can move with the entire system to a new processor with about two man months of effort.

The initial version of **COHERENT** is available for the Digital Equipment Corporation PDP-11 computers with memory-mapping, such as the PDP 11/34. Machines which will be supported in the coming months are the Intel 8086, Zilog Z8000, and Motorola 68000. Machines for which ports are being considered are the DEC VAX 11/780 and the IBM 370, among others.

Because COHERENT has been developed independently, the pricing is exceptionally attractive. Of course COHERENT is completely supported by its developer. To get more information about COHERENT contact us today.



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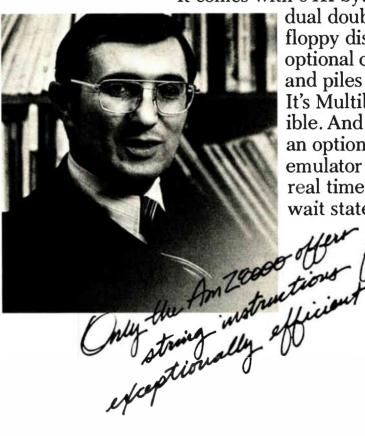
Rick McCarthy Manager, Field Applications, Engineering move a data item every 2.5  $\mu$ sec. And you can interrupt the instruction to take care of other business.

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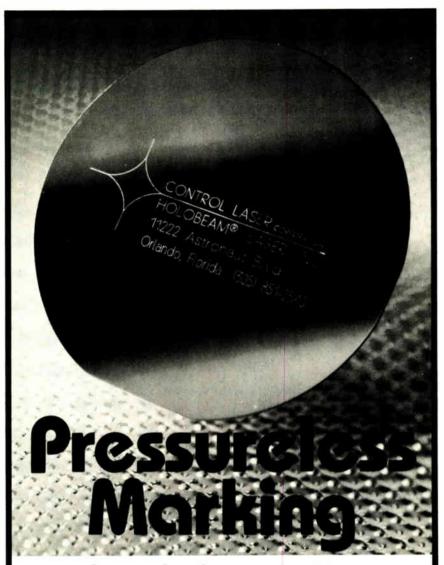
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#### Readers' comments

10-MHz sine waves directly, by virtue of the Tektronix model 468's 100-MHz analog section? Direct display makes it possible to disclose "distortion," if it exists, and show amplitude correctly.

The authors also state that display jitter has plagued every commercial digital scope except the 468. This is not the case. Nicolet's digital scopes eliminate the timing errors that cause jitter. This is the preferred way, because in averaging, a major bandwidth loss will occur if the display, but not the timing, errors are corrected.

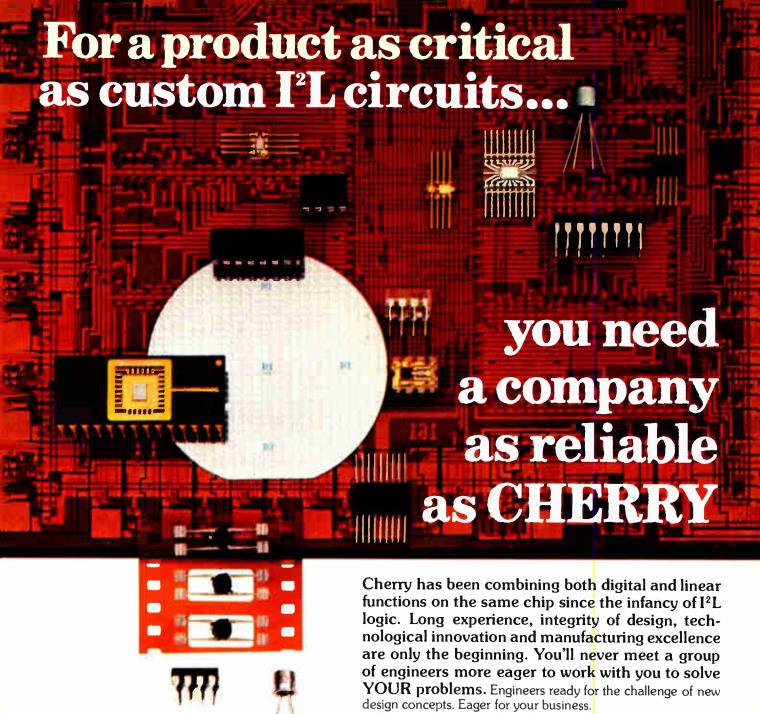
Robert W. Schumann Nicolet Instrument Corp. Madison, Wis.

The authors reply: Regarding useful storage bandwidth, our view of the oscilloscope's role as a general-purpose test and measurement instrument is somewhat different from that of Mr. Schumann.

At Tektronix, the oscilloscope is regarded as a tool for making waveform measurements such as amplitude, phase, and frequency that require a good visual representation. Useful storage bandwidth merely addresses the number of samples per cycle needed for a good visual representation: that is, 25 samples per cycle if a dot display is used, 10 per cycle for dots joined by vectors, and 2.5 for the 468 interpolated display.

Theoretically at least, all the information of a signal is present if there are only 2+ samples per cycle as the Nyquist criterion states. But amplitude, frequency, and phase measurements are extremely difficult, if not impossible, when a waveform is represented by only two-plus dots per cycle.

As for the jitter-correction circuit in the 468, the article addressed digitizing circuits that use the trigger point as a memory location, making possible pretrigger viewing. In this type of system,  $\pm \frac{1}{2}$  sample trigger uncertainty is inherent, but is corrected by the 468. But if the trigger is used to begin the sweep, a restart oscillator can be used to correct trigger uncertainty. This feature gives performance comparable to that of an analog oscilloscope, but cannot work when pretrigger information is desired.



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#### **People**

### West, McDougall won't run from Japanese competitors

"Who invented the notion that technological competition between the U.S. and Japan is a war?" demands J. Thomas West, Data General Corp.'s engineering manager for Japanese business development. That view has U.S. companies running scared, he complains, begging for Government protection, "when running away from competition is the most self-defeating course we could take."

West, 40, who led the team that developed Data General's new MV/8000 32-bit minicomputer [Electronics, May 8, p. 185], believes his company is taking a wiser course. Last fall, he became technical liaison between Data General and a Japanese minicomputer firm, Nippon Mini-Computer Corp.

Nippon Mini-Computer, a licensee of Data General since 1971, built and marketed the firm's Nova computers in Japan. Last year, it traded 50% of its stock to Data General in exchange for licensing rights to the American company's entire product line over the next 10 years. Renamed Nippon-Data General Corp., the firm is now "a full and equal partnership," says Donald L. McDou-

gall, West's counterpart for the business side of the arrangement. He hopes to see its annual sales growth rate exceed Data General's own in the coming decade.

McDougall, 37, a Canadian "who was never much interested in travel" before he embarked on developing a string of subsidiaries in the Netherlands, Belgium, Switzerland, Italy, and France, figures he has spent nearly four of the last nine months in Japan working with the Japanese firm's management during the period of adjustment to its U.S. marriage or on planes between there and the Westboro, Mass., corporate headquarters of Data General.

He has come away convinced that "the Japanese are quite capable of taking over the world economy." He agrees with West, however, that the prospect is better viewed as a challenge and an opportunity than as a threat, and he stresses the advantages his company looks for in making friends with such talented foreign competitors.

Rich soil. Japanese firms, coming on strong in mainframes, are not so active in minicomputers, McDougall notes, "so we see a fertile market there for our products." The Nippon connection means Data General machines, made in Japan, do not run into Japanese trade restrictions ap-





**Partners.** J. Thomas West, left, Data General's engineering manager for Japanese business, and Donald McDougall, his business counterpart, see Japanese as partners.

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#### **People**

plied to imports. And, McDougall says, "Nippon-DG's engineering expertise helps us offer Japanese-specific products, instead of Americanbuilt ones requiring the customer to do all the adjusting."

The Japanese-language input-and-display system developed last year by Nippon-DG for use on Data General's Eclipse computers [Electronics, Jan. 3, p. 213] "could not have been built by Americans," McDougall believes. He adds that the benefits of such cooperation should mean a significant competitive edge over other U.S. minicomputer makers, whose homegrown machines go into the Japanese market via sales offices or distributors.

Commonality a goal. Another goal is standardization of Data General's product line. Any improvements the Japanese make will be incorporated into the line, eventually resulting in a commonality of parts, servicing, and technical support wherever Data General minicomputers are built and sold. Tom West, the man in charge of bringing back technological fruits of the alliance, expects to see longrange benefits from Nippon-DG's access to Japanese advances in custom very large-scale integrated circuits, voice recognition, fiber optics; and copier technologies.

From their respective managerial and technical orientations, the two agree that the most profitable Japanese-American effort will be one that successfully balances Japan's highly disciplined, team-player work ethic and the U.S.'s individualistic brand of entrepreneurial energy. McDougall particularly feels that his role-interfacing with Nippon-DG's management, product development, and marketing people—calls on him continually to strike such a balance. "Deciding whether to do it their way, our way, or by compromise takes a lot of flexibility," he says. "I think developing a high degree of cultural sensitivity is the prime requisite of this job."

"Followed closely by a high degree of stamina," adds West, whose travel schedule is as rugged as McDougall's. "Jet lag is getting to be an old friend."

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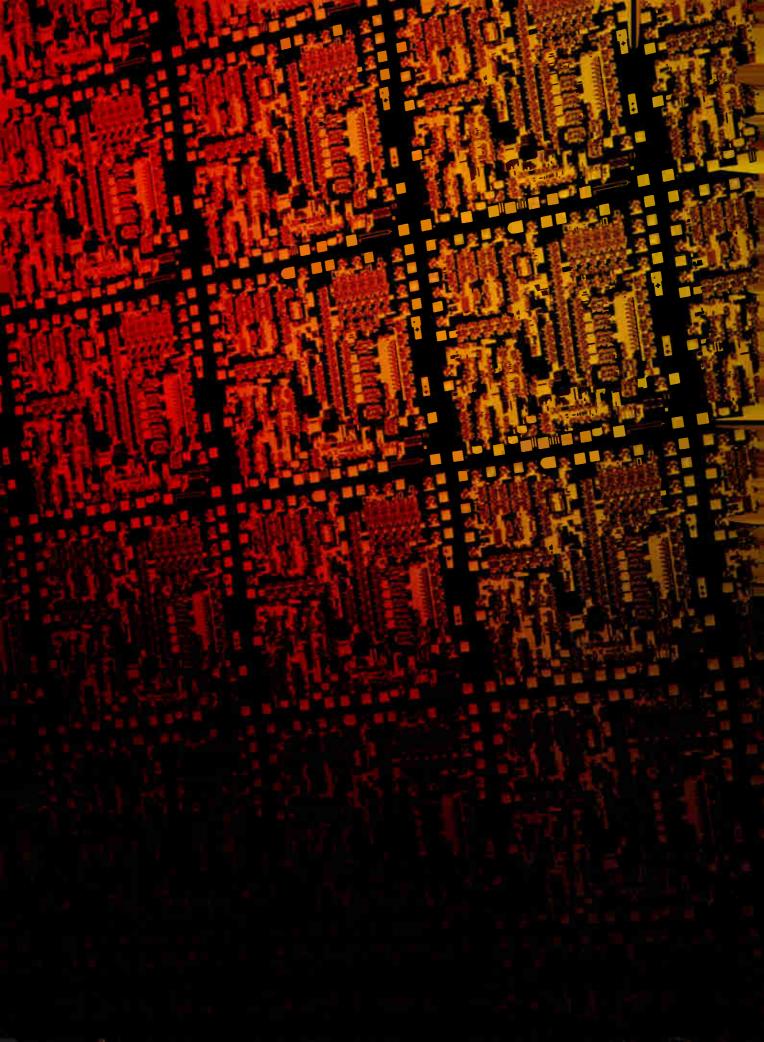
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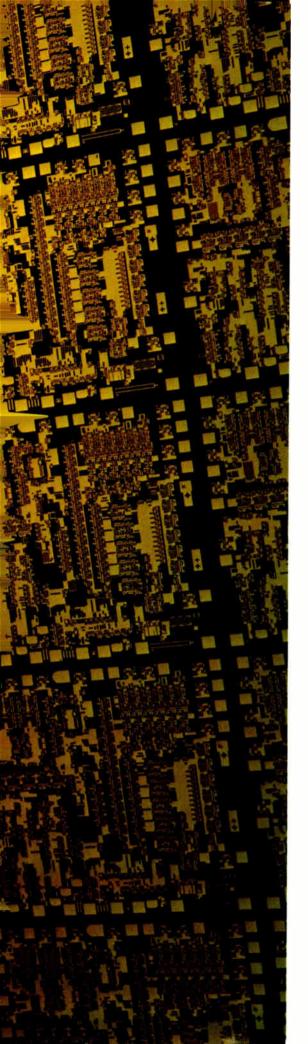
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#### Making the FAA straighten up and fly right

The United States can be proud of its commercial air transportation system, if not the Federal Aviation Administration that is charged with running it. Much of the success the system has had is more a tribute to the engineering competence of the aircraft and avionics manufacturers and operators than to the FAA. Now those private judgments that have long ranked the FAA near the bottom of the Federal bureaucracy in professional competence and efficiency are out in the open, thanks to a devastating special report issued by the National Research Council at the end of June.

Titled "Improving Aircraft Safety" and dealing with FAA aircraft certification, the study is the product of a 13-member blue-ribbon panel headed by George M. Low, president of Rensselaer Polytechnic Institute at Troy, N. Y. He is better known in Washington for his former job as the National Aeronautics and Space Administration's second in command and, earlier, as manager of the Apollo spacecraft program. The 118-page analysis was undertaken to allay public fears after 271 people were killed when an American Airlines DC-10 lost an engine and crashed on takeoff at Chicago's O'Hare Airport on May 25, 1979.

If the FAA is to improve and keep up with the industries and technologies it monitors, the Low committee concludes, it needs "highly competent, dynamic leadership, with terms of sufficient duration to provide stability and continuity," plus "improved technical staff of greater competence." To achieve better leadership, the appointments of the FAA administrator and deputy administrator should be removed from politics and selected from a slate of candidates recommended by a new, independent aviation safety policy board that would be set up to counsel the Secretary of Transportation on major issues

and FAA oversight. The FAA administrator, who could be reappointed, would also get a technology advisory group.

To counter the FAA's "inadequate level of technical currency and competence," which the report says means that industry engineers have greater competence than the FAA staff members who must judge their work, the FAA is urged to establish a central engineering organization to replace the 12 regional staffs that now report to Washington. Such a move could reduce or eliminate "inadequate and ambiguous direction, supervision, and support of staff, resulting in confusion about priorities, reluctance to assert government prerogatives, and low morale."

Beyond management and staff policy changes, the FAA is also urged to speed up the "leisurely pace" of its five-year effort to develop a comprehensive information-gathering and data-processing system for staff access to records of aircraft manufacturers and carriers. The Low committee also calls for stringent accreditation standards for aircraft mechanics—like those for flight crews—including separate standards for avionics maintenance staffs.

The analysis deserves high marks for its depth, knowledgeability, and clarity of presentation. It is long overdue in an era when a passenger airliner takes off or lands somewhere in the United States on an average of every three seconds around the clock, every day of the year. The worst thing that could happen to the study is that it be forgotten or discarded in an election year. The best thing that could happen is that these excellent recommendations be implemented and that the other key element of the nation's air transportation system—the one dealing with air traffic control, airports, and airways—be the subject of another analysis by an equally expert group as that headed by George Low.

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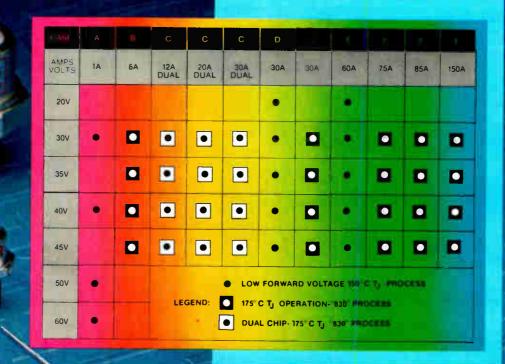
To create this definitive "Full Spectrum" Line we developed 7 new series, each characterized to effectively cover a specific area of common usage.

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#### **Automatic Precision** Screen Printing Machine **MODEL: LS-15GT**

#### **SPECIFICATIONS**

Printing size: 6 × 6 in.

 $(150 \times 150 \,\mathrm{m/m})$  $12.6 \times 12.6$  in. Screen frame:

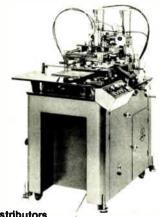
 $(320 \times 320 \text{m/m})$ 

Squeegee stroke: 2 ~ 8 in.

 $(50 \sim 200 \,\text{m/m})$ (variable speed)

Squeegee speed: 0 ~ 4 in./sec.

 $(0 \sim 100 \,\text{m/m/sec.})$ 



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#### **Meetings**

Electromagnetic Interference Metrology Seminar, National Bureau of Standards (M. Gerald Arthur, EMI/Radiation Hazards Group, Electromagnetic Fields Division, NBS, Boulder, Colo. 80303), NBS, Gaithersburg, Md., July 22-24.

1980 Microcomputer Show, Online Conferences (Cleveland Road, Uxbridge JB8 2DD, England), Wembley Conference Center, London, July 22-24.

Second Telecommunications Conference, IEEE (Umid Nejib, Engineering Department, Wilkes College, Wilkes-Barre, Pa. 18766), Best Western Motel, Wilkes-Barre, July 28 - 31.

SPIE's 24th International Symposium and Instrument Display, Society of Photo-Optical Instrumentation Engineers (Box 10, Bellingham, Wash. 98225), Town and Country Hotel, San Diego, Calif., July 28-Aug. 1.

23rd Midwest Symposium on Circuits and Systems, University of Toledo (A. R. Thorbjornsen, Electrical Engineering Department, University of Toledo, Toledo, Ohio 43606), Toledo, Aug. 4-5.

Fifth Annual Conference on Innovation and Regulatory Issues and Technical Seminar on Solar Energy and Energy Conservation, National Bureau of Standards (Sandra A. Berry, B-226, Building Technology, NBS, Washington, D. C. 20234), Plaza Cosmopolitan Hotel, Denver, Colo., Aug. 6.

Impact of the AT&T Business Unregulated Subsidiary and the Restructuring of the Computer/Communications Industry, The Yankee Group (Box 43, Harvard Square Station, Cambridge, Mass. 02138), Meadowlands Hilton, Secaucus, N. J., Aug. 5-6, and Palo Alto Hyatt, Palo Alto, Calif., Aug. 12-13.

1980 Joint Automatic Control Conference, IEEE, Instrument Society of America, et al., Sheraton-Palace Hotel, San Francisco, Aug. 12–15.

Electronics/China 80, U.S.-China Trade Consultants Inc. (Clapp & Poliak Inc., P. O. Box 277, Princeton Junction, N. J. 08550), Canton, China, Aug. 14-24.

First Annual National Conference on Artificial Intelligence, American Association for Artificial Intelligence (AAAI 1980 Conference, Stanford University, P.O. Box 3036, Stanford, Calif. 94305), Stanford University, Aug. 19-21.

International High-Fidelity Trade Fair with Festival, Nowea (D-4000 Düsseldorf 30, P.O. Box 320203, West Germany), Fairgrounds, Düsseldorf, Aug. 22-28.

First Annual Hewlett-Packard 1000 International Users Group Conference (Glen A. Mortensen, Intermountain Technologies Inc., P.O. Box 1604, Idaho Falls, Idaho 83401), San Jose Hyatt House, San Jose, Calif., Aug. 25-27.

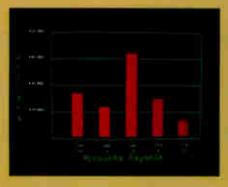
The 12th Conference on Solid-State **Devices**, The Japan Society of Applied Physics (3-5-8 Shiba Koen, Minato-ku, Tokyo 105), Tokyo Chamber of Commerce & Industry Building, Aug. 26-27.

10th Symposium on Electromagnetic Theory, Verband Deutscher Elektrotechniker (D-6000 Frankfurt 70, Stresemannallee 21, West Germany), Munich Technical University, Aug. 26-29.

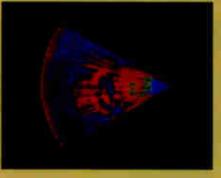
The 15th International Conference on the Physics of Semiconductors, Physical Society of Japan (Hiroshi Kamimura, Department of Physics, Tokyo University), Tokyo, Kyoto International Conference Hall, Kyoto, Sept. 1-5.

#### Short courses\_

Implementing Cryptography in Data **Processing and Communications** Systems, University of Southern California Continuing Engineering Education, Powell Hall 216, University Park, Los Angeles, Calif. 90007), USC, Aug. 25-28.



Management Information Display



Ultrasonic heart sector scan



High-resolution display with alphanumerics

## Get the professional color display that has BASIC/FORTRAN simplicity

#### **LOW-PRICED, TOO**

Here's a color display that has everything: professional-level resolution, enormous color range, easy software, NTSC conformance, and low price.

Basically, this new Cromemco Model SDI\* is a two-board interface that plugs into any Cromemco computer.

The SDI then maps computer display memory content onto a convenient color monitor to give high-quality, high-resolution displays (756 H x 482 V pixels).

When we say the SDI results in a highquality professional display, we mean you can't get higher resolution than this system offers in an NTSC-conforming display.

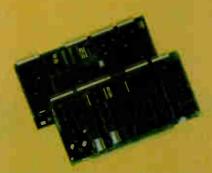
The resolution surpasses that of a color TV picture.

#### **BASIC/FORTRAN** programming

Besides its high resolution and low price, the new SDI lets you control with optional Cromemco software packages that use simple BASIC- and FORTRAN-like commands.

Pick any of 16 colors (from a 4096-color palette) with instructions like DEFCLR (c, R, G, B). Or obtain a circle of specified size, location, and color with XCIRC (x, y, r, c).

\*U.S. Pat. No. 4121283



Model SDI High-Resolution Color Graphics Interface

#### **HIGH RESOLUTION**

The SDI's high resolution gives a professional-quality display that strictly meets NTSC requirements. You get 756 pixels on every visible line of the NTSC standard display of 482 image lines. Vertical line spacing is 1 pixel.

To achieve the high-quality display, a separate output signal is produced for each of the three component colors (red, green, blue). This yields a sharper image than is possible using an NTSC-composite video signal and color TV set. Full image quality is readily realized with our high-quality RGB Monitor or any conventional red/green/blue monitor common in TV work.



Model SDI plugs into Z-2H 11-megabyte hard disk computer or any Cromemco computer

#### **DISPLAY MEMORY**

Along with the SDI we also offer an optional fast and novel two-port memory that gives independent high-speed access to the computer memory. The two-port memory stores one full display, permitting fast computer operation even during display.

#### **CONTACT YOUR REP NOW**

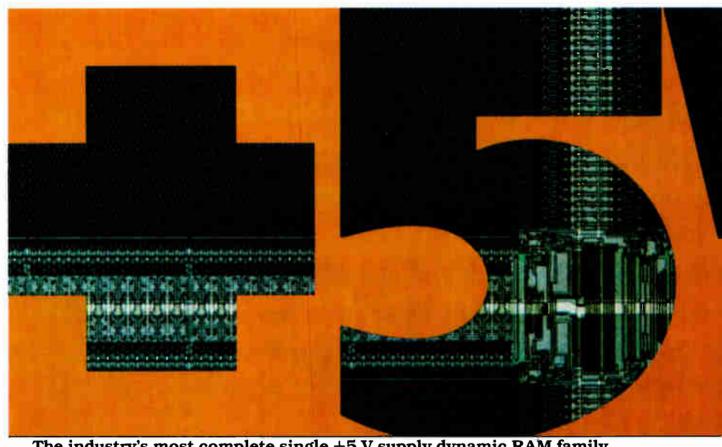
The Model SDI has been used in scientific work, engineering, business, TV, color graphics, and other areas. It's a good example of how Cromemco keeps computers in the field up to date, since it turns any Cromemco computer into an up-to-date color display computer.

The SDI has still more features that you should be informed about. So contact your Cromemco representative now and see all that the SDI will do for you.

Circle 27 on reader service card



## The world's broadest +5 is available in volume

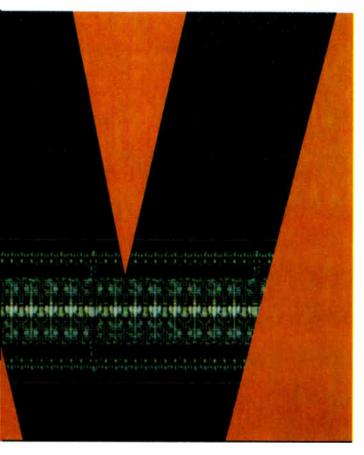


The industry's most complete single +5 V supply dynamic RAM family

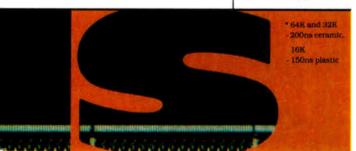
Density	Device	Self/Auto Refresh	Power Supply	Access tim <del>es</del> (ns)	
64K 64K	MCM6664 MCM6665	_	+5 V. ±10%	150, 200	
32K 32K	MCM6632 MCM6633	-	+5 V. ±10%	150, 200	
16K 16K	MCM4516 MCM4517	<b>V</b> –	+5 V. ±10%	120. 150, 200	



## V dynamic RAM family today, from Motorola.



V CC Supply Current-Max Active/Standby mA*	Price* 100/pc.
50/5	\$124.00 113.00
50/5	62.00 56.65
23/2.5	18.00 15.00



For the first time, a complete family of single-supply +5 V dynamic RAMs from 16K through 64K is available in production quantities. You can get them now, from Motorola.

The dynamic RAM family leaders are the 64Ks. These "memories of the future" are available *today* from Motorola, and from authorized Motorola distributors.

The single-supply 16K RAMs also are available now in production quantities from the factory and distributors. Completing this family of totally upward-compatible 16-pin RAMs are the +5 V 32Ks, for intermediate memory system densities between 16K and 64K. They're also available now direct from the factory.

The entire family uses industry-standard pinouts and has the high speed and low power you expect from our HMOS technology. Systems designed with our 16K RAM can double or quadruple their memory capacity as demand warrants by simply plugging in our 32K or 64K family members.

#### The pin that refreshes

Motorola's +5 V 64K RAM was the first in volume production. Now, two versions are available. The original MCM6664 has the leadership Pin 1 self-refresh and auto-refresh functions. The MCM6665, without Pin 1 refresh, is now also in volume production.

Our 16K and 32K single-supply dynamic RAMs are designed with and without Pin 1 refresh, too. The 32K MCM6632 (with Pin 1 refresh) and MCM6633 (without) are both in production, as is the 16K MCM4517 (without). The 16K with Pin 1 refresh, MCM4516, will be available later this year.

Not only is Motorola first with the broad line of fully-pin-compatible 16K - 64K +5 V dynamic RAMs, but first with 16K - 64K +5 V families of fully pin-compatible 24-pin ROMs and EPROMs as well. Look to Motorola leadership in MOS Memories for designing

Innovative systems through silicon.



## BIOMATION A COO-D



## Compare this general purpose logic analyzer with the currently accepted industry standard.

#### The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer



ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

#### Compare clocking speed.

With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—five times better than the 1615A's. Use the K100-D's latch

mode to catch gliches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, mainframe and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

#### Compare capacity.

The K100-D's 1024 word memory is four times as deep as the 1615A's. This dramatically extends the length of data you can trap from your system at any one time. And that means faster, more accurate debugging. In addition, the K100-D's standard 16 channel format can be expanded to 32 channels for work on the new generation of 16-bit microprocessors.

#### Compare your productivity.

Finally, the K100-D makes designers more productive with convenience features superior to those of the 1615A. The K100-D has a larger keyboard, plus an interactive video display. Comprehensive status menu. Data domain readout in hexadecimal, octal,

binary or ASCII. And the list goes on and on.

#### The final analysis.

To help you evaluate these two fine instruments before you buy, we've prepared a point-by-point competitive comparison of the two. If you're designing and debugging high-performance digital systems, you'll want to read this document carefully. To get your free copy, just use the reader service number or write Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.



Hewlett-Packard 1615A A very good logic analyzer



Speed: 10 20 MHz
Speed: 10 20 ms
Speed: 10 250 ms
Resolution: 256 mords
Memory: 256 mords
Memory: 8 iming 8 18
Shannels: 8 or 24 data

Biomation K100-D

The industry's finest logic analyzer



Speed: to 100 MHz

Speed: to 100 ms

Resolution: 10 ns

Resolution: 10 ns

Resolution: 10 ns

Channels: 16 timing or 16 data

Channels: 16 timing or 32 data



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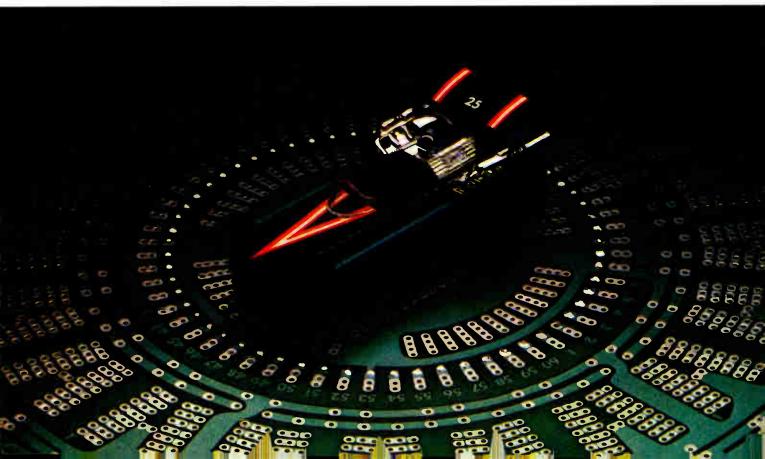
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#### **Electronics newsletter**

## Word generator delivers bytes at 100 MHz

To provide digital signals for testing high-speed integrated circuits, Interface Technology Inc. of San Dimas, Calif., is about to offer the first commercial word generator able to supply bit-parallel bytes at a 100-MHz rate. Also able to generate 16-bit-parallel bytes at 50 MHz, the \$15,000 unit has been dubbed a digital waveform generator because, unlike other word generators, it permits the clocking rate for each output channel to be varied independently. Thus the unit (model RS-680) can be programmed to provide seemingly asynchronous digital waveforms with 10 ns resolution for testing ICs with complex timing requirements.

### Light-pipe imager yields 240 dots/in.

A low-cost light-pipe method of imaging at high resolution, one that yields 240 dots/in.—compared with the figure of 60 dots/in. so far available—has been developed by Static Systems Inc. of New York. Using either liquid-crystal or electroluminescent multiplexed displays, the technique involves laying down on a display multiple layers of specially prepared glass in which staggered holes 1/240 in. in diameter are etched. The glass can be concave to match the curvature of photocopier drums, allowing direct imaging and sharp focus without additional optics. Several display and copier makers are looking at the development. The Minolta Corp. of Ramsey, N. J., owns the rights for use with flat-bed copiers.

## Microwave oscillator provides 100 times more energy

Varian Associates of Palo Alto, Calif., has built a gyrotron oscillator able to provide 212 kw of continuous operating power at a frequency of 28 GHz, 100 times more energy than previous devices. Designed to provide microwave heating of fusion plasmas in nuclear experiments at the Oak Ridge National Laboratory, the tube has a beam-conversion efficiency of 40% at that power level, higher at lower levels. Although designed for continuous operation, the unit is useful for pulsed operation in mirror and Tokamak-type fusion devices. The company claims that the new gyrotron oscillator will also be useful in communications, giving "unprecedented" bandwidth capability to increase the information carried, and in radar systems to increase long-distance resolution.

## Standard Unix operating system due from Microsoft

Designers who fear that the tremendous investment in software will tie them to their microprocessor choice forever may be reassured by a new version of the Unix operating system now being readied by Microsoft. Bellevue, Wash. Because Unix itself is written in the high-level C language, it is portable and can be made to work on any number of microprocessors, says company president William Gates, and can take all the other software along with it. Current plans call for versions for the 8086, 68000, and Z8000 microprocessors. Developed by Bell Laboratories for minicomputers, Unix is in Gates' view the best choice for a standard operating system for the 16-bit microprocessors that now have the instruction sets and larger memory-addressing capabilities necessary to take advantage of it. And where the standard Bell licensing fee of \$28,000 has made Unix too expensive up to now, Microsoft hopes to charge about one tenth that when it is introduced this fall and will provide support to boot. However, it will have to compete with several other Unix versions reported to be under development [*Electronics*, Feb. 28, p. 33].

#### **Electronics newsletter**

## Sears to train its personnel to sell computers

After nearly two years of test marketing the Atari 400 and 800 personal computers, Sears Roebuck & Co., Chicago, has decided that its sales personnel are not sufficiently knowledgeable to market computers. "This does not mean, though, that we are dropping the Atari 400 and 800 lines," notes a Sears spokesman. What it does mean is that, at about half the sites where test marketing took place, Sears will upgrade its sales personnel with specialized training in computer marketing. The computer lines will be dropped at the remaining sites. The company would not say which sites had been tested or which stores would drop the computer line, but a company spokesman confirmed that California was a prime test area.

## Hybrids to aim at geothermal research work

The first members of a line of very high-temperature hybrid devices due this fall from Teledyne Philbrick aim at applications in geothermal energy research and drilling operations. The model 2115 15-v voltage regulator can operate in temperatures of up to 275°C, and the model 4160 12-bit analog-to-digital converter is guaranteed to operate with no missing codes at up to 200°C. The Dedham, Mass., firm plans to start marketing the devices after their formal debut at Wescon, Sept. 16–18, and says more such heat-beating hybrids are on the way.

#### Mostek to shift ROM assembly to Texas plant

Mostek Corp. is planning to set up an integrated-circuit assembly operation at its Carrollton, Texas, headquarters wth an eye toward shortening customer lead times on mask-programmed read-only memory parts. The target for bringing the new operation on line is late first quarter next year, when the firm expects to transfer all ROM package assembly to Carrollton. Coincidentally, the late first quarter startup goal for the new packaging line coincides with the anticipated start of order taking for Mostek's planned 256-K ROM device—the MK38000. Mostek currently ships ROM dice to Malaysia for package assembly, which lengthens lead times by two to three weeks or more.

## Signetics to expand controller family for bit-stream jobs

Look for Signetics Corp., Sunnyvale, Calif., to begin expanding its 8X300 microcontroller family targeted at high-speed bit-stream management applications. The firm's bipolar LSI division plans to add several peripheral devices, including host interfaces and a floppy-disk controller, among others, as well as new development systems hardware, by year-end. The new chips are expected to allow the implementation of specific applications, such as floppy- and hard-disk controllers, as well as data-terminal and communications controllers, with typically one fourth the component count of prior designs.

#### Addenda

Another sign of the recession: sales of TV receivers to dealers in June dropped another 6.9% to 1.45 million sets. Total sales for the first six months of 1980 were off 9.1% to 6.71 million units, from last year's first half. . . . Ralph Simon, who has been heading the power device and electro-optic operations of RCA Corp.'s Solid State division will now be division vice president for special assignments, reporting to Robert S. Pepper, general manager of the Somerville, N. J.-based facility. Succeeding Simon will be Eric Burlefinger, formerly managing director of ITT's semiconductor operations in the United Kingdom.

# SO YOU NEED ROMs. WHY STAND IN LINE AT THE SUPERMARKET?

No need to wait for the big semiconductor com-

panies to schedule your ROM production among their RAMs and EPROMs and Microprocessors.

Come to Electronic Arrays, with an N-channel silicon gate fabrication facility 100% dedicated to ROMs. With sort and final test 100% dedicated to ROMs. With in-house ROM program verification and in-house mask making for fast-turn tooling . . . 100% dedicated to ROMs!

Face it. When you specialize in one thing, you get very good at it. And very fast. At EA, we think, live and breathe 8K, 16K and 32K ROMs. Electronic Arrays, 550 East Middlefield Rd., Mountain View, CA 94043. (415) 964-4321; Philadelphia (215) 643-1447; Chicago (312) 858-8508.

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And our future.

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#### Continued leadership in bipolar technology.

MMI has grown to become a \$65 million company by consistently designing and delivering state-ofthe-art bipolar LSI products. And now

we're growing faster than ever.

Our tradition of excellence began with the industry's first lK PROM in 1971. This was followed by the first 2K, 4K and 8K bipolar PROMs, by the first fast 8x8 multiplier, and then the 15 MHz FIFO. Our latest innovation is PAL<sup>14</sup> programmable array logic, the LSI circuit which allows you to program your own logic on a chip.

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#### Delivery that keeps pace with our designs.

MMI has made a commitment to deliver large volumes of bipolar products. We currently ship—and will continue to ship—more bipolar PROMs than anyone else in the world.

Our annual output has tripled during the last twelve months.



MMI was the first to install a 4-inch bipolar wafer fab line. And we will expand that line's capacity by another 80% before the end of 1980. At the same time, we have begun converting

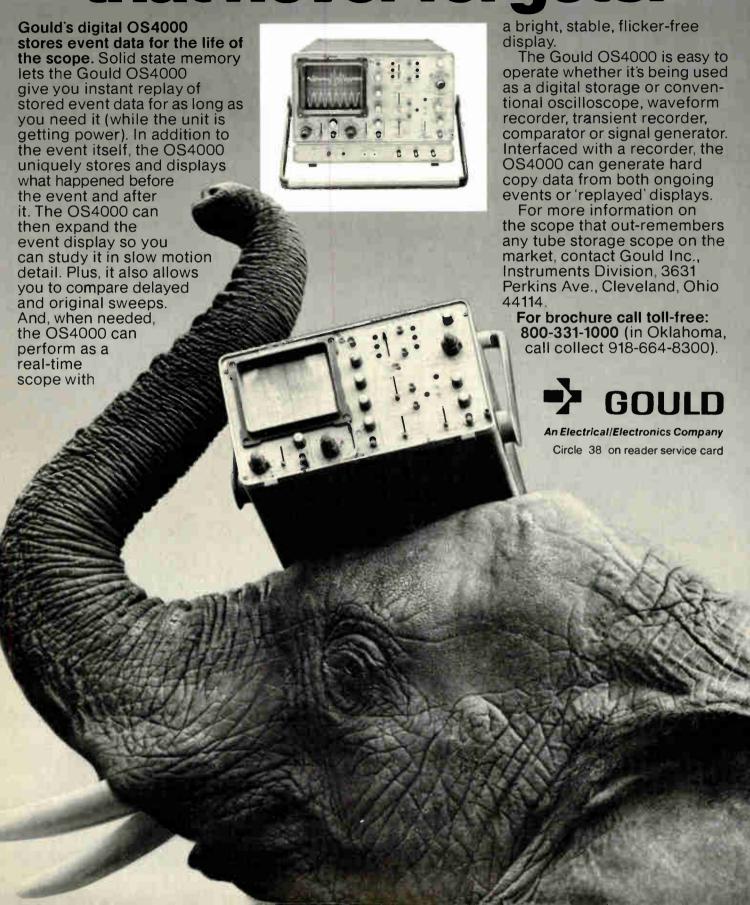
our 3-inch line to 4 inches and will double its output by mid-1981. We have also broken ground on a new assembly facility and expect it to be operational by September of this year. Over the next few years we'll spend 15-20% of every sales dollar on facilities and equipment to assure you volume delivery of MMI's bipolar LSI.

#### Let us prove it.

Send for a specially prepared report which details MMI's engineering and production capability and outlines our extensive line of digital bipolar LSI products. Please address your requests to Applications Department, Monolithic Memories, Inc., 1165 E. Arques Ave., Sunnyvale, California 94086.







Significant developments in technology and business

# Harris mobilizes for tough C-MOS processor battle

by Raymond P. Capece, Managing Editor, Technical

Company plans campaign to scale down its process for C-MOS memories and 8086, 8748 versions

Long a contender in the complementary-MOS ranks, Harris Corp. has plans to take a command position. The company's Melbourne, Fla., semiconductor division is mounting an ambitious design program in C-MOS memories and microprocessors, drafting Intel's n-channel processors as the basis for its designs.

Even now, Harris designers are fighting through the painstaking reengineering of Intel's popular 16-bit 8086 into C-MOS, for what could be the leading-edge 80C86 [Electronics, June 19, p. 35]. They also are working on a C-MOS version of Intel's widely used 8-bit single-chip microcomputer, the 8748. Neither move has the support of Intel, however.

SAJI. Of course, C-MOS memories are prominent in Harris' plans as well. Regarded by Dataquest Inc., the Cupertino, Calif., market research firm, as the leading supplier of 4-K C-MOS static random-access memories, Harris has used memories to establish its SAJI (for self-aligned, junction-isolated) process.

It plans to execute a 16-K RAM with SAJI IV for volume production next year. Also in the works are read-only memories and erasable programmable ROMs to support the microprocessor families.

In microprocessors, Harris has been slogging along for five years with the 6100. This 12-bit low-technology device was developed by Intersil Inc. to emulate the instruction set of Digital Equipment Corp.'s PDP-8/E minicomputer.

Whereas Harris' 6100 used the original SAJI process, a single-level self-aligning polysilicon-gate process with 5-to-6-micrometer features, the company has adopted the SAJI II process, currently in production for its 1-K-by-4-bit static RAMs, to build a new 6100 for DEC.

SAJI II, first developed in 1977, adds another level of polysilicon, as well as buried and self-aligned contacts, and shrinks some features down to 4  $\mu$ m. The results are impressive: the 6100(R), which thus far is available only to DEC, drops the cycle time from 2.5 to 1.4 microseconds (running off an 8-megahertz clock) and boosts the addressing range to a full 16-bit capability, or 65 kilobytes.

The new processor also adds some instructions to the repertoire of the 6100. What's more, Harris is reportedly working on a C-MOS version of the LSI-11 for DEC.

After the new 12-bit device, the

company's plans are Intel all the way (see "C-MOS challenges n-MOS"). According to E. J. D'Escoubet, director for digital research and development, Harris conservatively forecasts production volumes of the C-MOS 87C48 for 1982, built using the SAJI IV process, which will be planar (similar to Fairchild's Isoplanar oxide-isolated bipolar process), adding self-aligned guard bands and shrinking minimum features to 3.5 µm, comparable to minimum channel lengths in Intel's HMOS process.

Others. In terms of complexity and density, National Semiconductor Corp.'s current double-polysilicon P'C-MOS process falls between SAJI II and SAJI III, and Mitel Corp.'s ISO'C-MOS is roughly between SAJI III and IV. The SAJI III process marked the addition of planar structures and has been reserved for Harris's memories.

"The guard bands, for which we received a patent over two years ago, will be critical in reducing parasitic effects, especially latch-up," D'Escoubet claims. Latch-up is a condition in which paper structures that

#### C-MOS challenges n-MOS

It has long been said that n-channel MOS is not inherently faster than complementary-MOS—it just got a head start. According to Harris, its 4.0-micrometer SAJI II process, first developed in 1977, compares favorably with Intel's 3.5- $\mu$ m HMOS process in speed, yielding the same gate delay of 1 nanosecond. But it is at the finer geometries that C-MOS will truly challenge n-MOS: with the scaled-down SAJI II process in preproduction of memories this year, Harris is claiming 500-ns gate delays, comparable with those of Intel's 400-ns HMOS II, which the Santa Clara, Calif., company is applying to fast static random-access memories. Intel's process uses some devices with channels as short as 2.0  $\mu$ m, and Harris' will descend to 2.5  $\mu$ m. Of course, C-MOS's 1,000:1 advantage in power dissipation will only improve with further scaling, Harris says.

#### **Electronics review**

are part of the usual C-MOS process show thyristorlike behavior and conduct current in the same way as do silicon controlled rectifiers. The anticipated instruction cycle time of the 87C48 will be  $1.35~\mu s$ —comparable to that of the HMOS version of Intel's 8748

Another interesting point about Harris' C-MOS microprocessors is the goal of small dice through careful circuit design as well as scaling. The 87C48 will reportedly come in at 50,000 square mils—about the same as the original 8748 and far less than the 87C48 planned by Intersil, which initially occupied a whopping 90,000 mil<sup>2</sup>.

What's more, Harris' 80C86— which will use a scaled SAJI IV process for features down to  $2.5~\mu m$ — will have a die size of  $55,000~\text{mil}^2$ — about the same as Intel's initial n-channel MOS offering of the 8086. "We expect not only performance equal to that on n-MOS, but equivalent chip packing densities as well," D'Escoubet says.

Different route. Harris takes an approach to C-MOS rendering of n-channel processes that differs from that of other manufacturers like National, which is also building the 87C48 [Electronics, March 27, p. 44]; Intersil; and Mitel in Kanata, Ontario, Canada, which is building Motorola's 6802 in C-MOS. Harris sets specific goals for die sizes and uses a predominance of space-saving n-channel devices in the design effort.

"It keeps the dice from blowing up," explains D'Escoubet. "Seventyor ninety-thousand-mil<sup>2</sup> dice just aren't producible." By using polysilicon-load n-channel static RAMs (rather than C-MOS static RAMs) for on-chip memory, for example, Harris is able to conserve silicon.

Also, rather than entirely static C-MOS circuits, Harris uses n-channel dynamic logic circuits and runs them off clocks independent of the system clock. Motorola is also believed to be pursuing similar space-saving techniques on its forthcoming C-MOS version of the 6805 single-chip microcomputer, due out later this year.

#### **Memories**

## TI going to market in standardization struggle over pinouts for 8-bit-wide parts

Texas Instruments Inc.'s contest to win standardization for its pinout scheme for high-density 8-bit-wide MOS memories is turning into a real cliff-hanger. Nevertheless, the combelow). In this way they hope to capture so many sockets that the pinout will become established, even without Jedec recognition.

TI will not have the field to itself,

TI'S E PROM PLANS					
Memory type	Current die size (mil <sup>2</sup> ), maximum access time (ns)	X-series die size (mil <sup>2</sup> ), maximum access time (ns)			
TMS 2516 (16-K)	23,700, 350/450	15,000, 250/350			
TMS 2532 (32-K)	28,300, 450	21,500, 250/300	16,500 <sup>1</sup> , 100 (typical)		
TMS 2564 (64-K)	40,800, 450	33,000, 300/350			
128-K		41,500 <sup>2</sup> , 350/450			
Note:— All chips employ 4.5-µm design rules except: 1. 3-µm design rules 2. 3.5-µm design rules					

pany is pushing ahead with marketing plans for the parts, hoping to establish a *de facto* standard.

TI has been seeking approval from the JC-42.3 MOS memory standardization committee of the Joint Electron Device Council for its pinout for 64-K parts only [Electronics, March 13, p. 46]. This move follows an earlier JC-42 rejection in favor of Intel Corp.'s pinout for 8-bit wide readonly memories, erasable programmable ROMs, static random-access memories, and pseudostatic RAMs at the 64-, 128-, and 256-K levels.

The two approaches differ in the placement of address and control signals. This results in six discrepancies in pin assignments.

No matter what the JC-42 committee does, TI memory marketing officials in Houston are vowing to go ahead with plans to supply E-PROMS at 64-K density levels and beyond that use the firm's pinout (see table

however. Its chief rival in the game, Intel Corp., is ready to offer samples of its 64-K E-PROM with the JC-42-approved pinout. No pinout for the 64-K and higher density levels has yet received full Jedec approval.

Members of the JC-42 group will not talk for publication, but apparently TI's request for a dual standard at the 64-K level received approval at a recent meeting—though only by a one-vote margin. An Intel representative promptly challenged the vote on procedural grounds, and a reballoting will take place in September.

To market. With approval hanging fire—if not in real doubt—T1 has launched an aggressive campaign aimed at some 1,000 potential E-PROM customers. In addition to samples of the 64-K TMS2564 E-PROM, the company is showing samples of a 128-K part slated for introduction in the first half of 1981.

The 128-K and smaller next-gen-

eration parts will be what TI is calling its X series, based on an X-shaped cell design that uses such techniques as a virtual ground approach with bit lines and ground interlaced to improve density. As well as allowing significantly smaller die sizes, the design will provide performance improvements.

The 64-K and smaller X series parts could come late this year, says Frank B. Hrobak, TI's strategic marketing manager for static RAMs and E-PROMs. The 128-K part, with tighter design rules, will have a die size only a quarter larger than the X series 64-K's 33,000 square mils.

Intel samples. The X series is coming just in time to meet the competition. Intel's 2764 64-K E-PROM, available as samples this month, features a die size of 32,400 square mils and an access speed ranging from 200 to 300 nanoseconds, topping off just where the X series 2564 starts out. According to Larry T. Jordan, strategic marketing manager for the Special Products division, the Intel

part uses an E-PROM version of the Santa Clara, Calif., firm's HMOS II process, HMOS-E. Both processes have 2-micrometer channel lengths.

More than one competitor is now predicting that TI will be forced to redesign its 28-pin package to comply with Intel's pinout. The latter will be the choice for major memory makers once Jedec approval is gained, the reasoning goes, leaving TI high and dry without a major second source for its pinout.

TI officials say that no active second-source discussions are under way. They note, however, that Motorola's 24-pin 64-K E-PROM programmed off board would be addressed in a board laid out for TI's 28-pin scheme.

The real question is how fast Intel will move with its part. Mostek Corp. is also working on a 64-K E-PROM with the approved pinout, so the battle that began at the JC-42 standardization meetings will soon spread to potential customers' offices.

-Wesley R. Iversen

fully configured unit can perform at a maximum rate of 160 million instructions per second on 64-bit words and hold a staggering 1 billion bytes of memory. The key to its high throughput and to Denelcor's claims is the HEP's unusual multiple-instruction-stream, multiple-data-stream architecture.

Architecture. As the term implies, this form of parallel processing lets more than one program run on the system simultaneously, each operating on its own set of data (see figure). It is not widely used in the central processors themselves.

Most other supercomputers on the market use what it called a vector approach—they process just a single stream of instructions at a time, although they simultaneously perform those instructions on multiple streams of data. Denelcor, a tiny 12-year-old Denver maker of analog and hybrid analog-and-digital computers, put a six-year, Government-funded effort into its architecture.

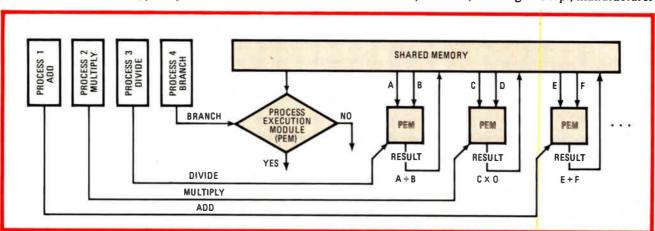
It will face some stiff competition from the established supercomputer makers, such as Cray Research Inc., whose Cray-1 performs at 80 million to 100 million floating-point operations per second and sells for between \$4.5 million and \$16 million, and Control Data Corp. which recently announced its Cyber 205 that can perform a breathtaking 800 million floating-point operations per second and sells for between \$7.9 million and \$16.5 million. In addition, Burroughs Corp., manufacturer

#### **Computers**

## Supercomputer handles multiple instruction streams with parallel-processing architecture

A brash upstart is challenging an elite circle of manufacturers of digital supercomputers. The Heterogeneous Element Processor, or HEP, from Denelcor Inc. is a type of paral-

lel processor that can be built with 1 to 16 process-execution modules—essentially central processing units—and as many as 128 data banks of 1 million words each. As a result, a



**Versatile juggler.** The Heterogeneous Element Processor can juggle multiple instruction streams, or processes, as they operate on separate streams of data, unlike conventional computer architectures, which let just one set of instructions operate on a single group of data.

#### **Eiectronics review**

of the famous Illiac IV supercomputer, is preparing to ship its first Burroughs Scientific Processor, which will perform 50 million floating-point operations per second, in the third quarter of this year.

Built from standard 10000 series emitter-coupled-logic parts, each HEP process-execution module occupies between 100 and 150 14- by-18-inch printed-circuit cards. Each module includes 2,048 general-purpose registers, 4,096 constant registers, and up to 1 million words of dedicated program memory.

Tying multiple processing modules to the memory modules is a digital switch that uses packetswitching techniques to manage oneword packets of information, according to Burton J. Smith, technical director at the company. Unlike switches that store data until it can be routed to its destination, the HEP switch continually reroutes data around the system until it eventually arrives at its destination.

Managing activity is the HEP operating system, a copy of which resides in every processor module. Operating in a batch mode, it allocates the system's resources to the various processes. Programming is in Fortran or assembly language.

Contract. The publicly held company grossed just \$2.7 million in revenue last year and has high hopes for HEP. Earlier this month it held a press conference to unveil the system and announce that in May it was awarded a \$2.4 million contract to build a four-processor system for the Army's Ballistics Research Laboratory in Aberdeen, Md. It says it demonstrated its prototype to the Army last November.

The company also wants to market the system to the lower end of the supercomputer market, "for people who want performance on a budget" according to David Miller, Denelcor chairman and president. A starter set with a single process-execution module that performs 10 million instructions per second, one memory module, the switch, and a few peripherals will sell for about \$1.5 million.

-Deborah Williams

McGraw-Hill Publications Co.

#### Communications

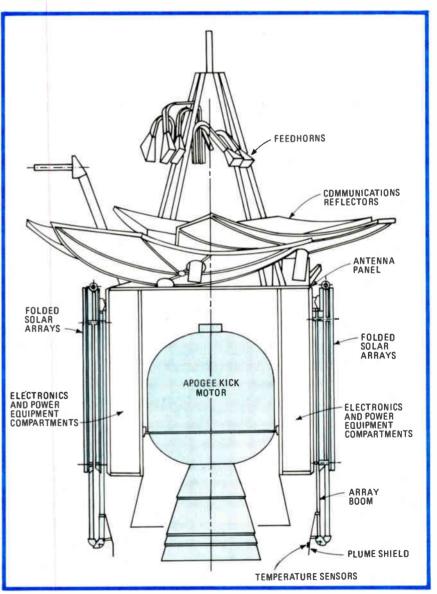
## Satellite loss laid to motor or solar array

All RCA Corp. wanted for Christmas last year was its missing Satcom III communications satellite. The spacecraft is still missing, but RCA has an idea of what happened.

A study concluded recently suggests two likely scenarios that would have led to its disabling and probable destruction. In the first and most likely, the apogee kick motor starts and then the exhaust cone breaks, letting hot gases melt the back portions of the satellite. Loss of communications equipment would have resulted (see figure).

In the second version, the motor ignites normally, but at the same time the solar arrays deploy prematurely. Because of the spacecraft's spinning and the motor thrust, the arrays suffer rapid structural damage, leading to complete failure of the on-board power system.

Headed by consultant J. Preston Layton and consisting of engineers



What happened. An RCA study group thinks that the missing Satcom III suffered problems with either its motor or its solar array panels (tinted), leading to its probable destruction.

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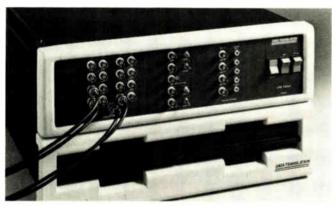
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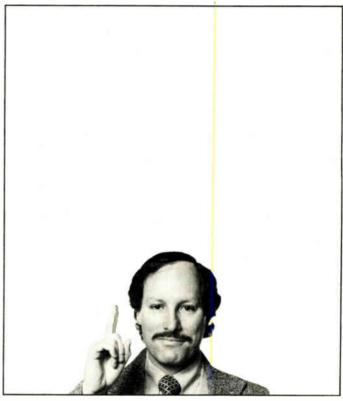
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#### **Electronics review**

and scientists from the National Aeronautics and Space Administration, the Jet Propulsion Laboratory, the Charles Stark Draper Laboratory, and RCA, a review board determined that those two scenarios were the most consistent with the known data:

- Satcom's departure from its transfer orbit.
- Its failure to achieve geosynchronous orbit.
- The loss of communications.
- A too-high exhaust temperature from the apogee kick motor.

The review board noted that all communications ceased 14.5 seconds into a 28-second motor burn intended to change the transfer orbit into the planned geosynchronous orbit. Then, too, the exhaust temperature sensors indicated overheating.

The sensor indication led the board to prefer the first scenario. However, power failure stemming from premature array deployment could take place within the 14.5-second time span.

The loss of Satcom III cost RCA \$48 million in launch and hardware expenses and another \$20 million or so in lost revenues [Electronics, Jan. 3, p. 46]; it had insurance for \$77 million. The company has since leased 11 preemptable transponders on AT&T's Comstar D-2 satellite at a cost of \$70,000 per month per transponder and will be charging its customers only the \$40,000 per transponder it was to charge for Satcom III usage. It will launch a replacement satellite next June.

Preventives. The review board made a number of recommendations to RCA to prevent recurrence of such a loss. For example, it recommended additional testing that would more closely approximate the combined effects of vibration, acceleration, and motor operation.

The board also suggested more stringent procedures for constructing, handling, installing, and inspecting the apogee kick motor. Perhaps fatalistically, it also recommended radar tracking of future Satcoms from launch until orbit—so if the bird stops talking, RCA will at least know where it is. -Pamela Hamilton

#### Components

## Photodetector climb may lure IC makers

The market for silicon photodetectors is going to climb, and with this will come a change in the makeup of the industry. So says Lawrence A. Murray, a market researcher and semiconductor industry consultant who sees a push into integrated parts that will require a level of solid-state expertise lacking among most suppliers in the field.

Increasing numbers of photodetectors will be required in fiber-optic equipment, new consumer products like video disks and sensors for home computers, electronics in the automobile, and even more applications, according to Murray. Smoke detectors and automatic cameras have already given the parts an impetus away from the industrial and military applications they have long served.



**Expansive.** Industry researcher Lawrence A. Murray foresees a boom in silicon photodetectors and an industry shakeup.

All of this will "put zing into a market for what has been, basically, a simple-to-produce device," Murray says. "It has sold for a lot of money because volume has not been high enough to attract mass producers." His firm, Murray Consultants of St. Louis, Mo., recently completed a survey of the field.

Three masks. A standard discrete p-i-n silicon photodetector, for example, is made with a three-mask process on a 50-by-50-mil substrate and sells for an average of \$7, Murray points out. "This is twice the

#### At last, the System/38 emerges

After a delay of almost a year, IBM Corp.'s General Systems division is finally making production shipments of its System/38 small-scale computer system. Heralded when it was introduced in November 1978 as having IBM's first new computer architecture in almost a decade, the unit featured a sophisticated new operating system that offered a more powerful data-management scheme than any other offering from the company.

Much to the company's chagrin, however, problems with this sophisticated software last year forced it to delay first shipments of the machines to customers [*Electronics*, Aug. 30, 1979, p. 88]. At first, IBM was not talking, and industry observers conjectured that the System/38's advanced virtual memory management system that referenced 281 trillion bytes of memory was making too many swaps between the main and peripheral stores—thrashing, in computer jargon.

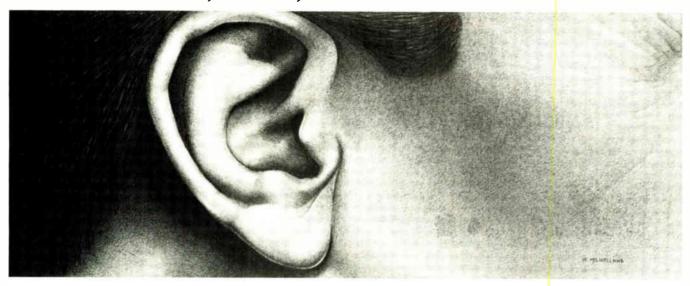
But at a briefing last January, the company reported significant progress in solving the problems and gave hints as to their cause. Brian Utley, project manager at IBM's factory in Rochester, Minn., where the System/38 is built, said it was necessary to improve the batch operations of the interactive operations-oriented operating system. This is critical if users of the older, batch-oriented System/3 were to move on to the new machine.

In addition, he said, interfaces between the various software modules had to be tested and cleaned up before the machines could be shipped. Thrashing was not the problem, he added.

At the beginning of July, IBM said it was satisfied that everything was working, and the first units began rolling out the door. In fact, three customers—United Merchants and Manufacturers Inc., New York, Road Machinery & Suppliers of Minneapolis Inc., and St. Olaf College, Northfield, Minn.—have been testing the System/38 since February to ensure that all is well with the new machine.

-Anthony Durniak

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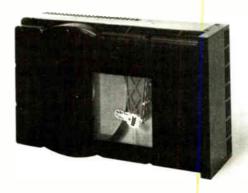
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#### **Electronics review**

selling price of a 200-by-200-mil integrated chip with thousands of transistors, for example, that requires eight masks to much tighter tolerances and is produced at a lower yield. So there is certainly room for photodetector prices to fall."

With the higher volume will come a move toward integrating the photodetectors, either the p-i-n device or the more expensive avalanche diode, on an integrated circuit containing circuitry that could amplify, multiplex, decode, or reconfigure the output to interface with the rest of a system, Murray continues.

Change. Here is where he sees the supplier makeup changing. "Only six companies out of the 72 now making photodetectors also have IC production and assembly capability. These six companies are likely to play a major if not dominant role as the market expands."

These companies are Texas Instruments Inc., RCA Corp., Spectronics Inc., Hughes Aircraft Co., Motorola Inc.'s Semiconductor Group, and Hewlett-Packard Co., he says. Texas Instruments is the largest supplier of the detectors, having between \$5 million and \$10 million in sales in 1979.

Next come companies like Spectronics, RCA (from a plant in Montreal, Canada), TRW/Optron, Clairex Corp., and EG&G Inc. But total sales for any one company are minuscule by the standards of the semiconductor industry.

Of the 72 companies in the field, some 65 had sales last year of less than \$3 million each, Murray estimates. Indeed, until 1978, the market increased by about 5% yearly, when new consumer applications started things moving.

Over the next decade, he projects a growth rate for silicon photodetectors of 38% per year. This would take it from an anticipated \$75 million in 1980, which includes phototransistor and photo-Darlington devices in optical couplers, to \$400 million in 1990. "These are numbers that could certainly entice companies used to high-volume production into the business," Murray concludes.

-Alfred Rosenblatt

#### **Military**

## Controller promises more fight per flight

Faced with the need to get more bang per aircraft, the U.S. Air Force is about to test a new system that combines flight- and fire-control computers with electro-optic target designation. If the concept works as well as its developer says it will, fighter-bombers could carry out airto-air combat and ground missions and survive antiaircraft attacks far more effectively than in the past.

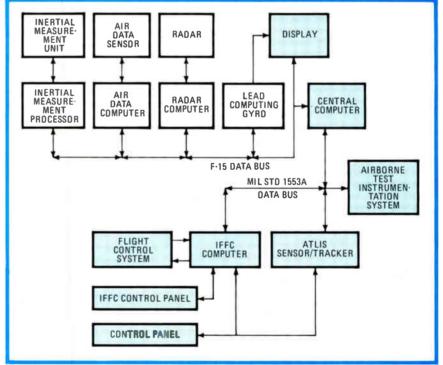
Called Integrated Flight and Fire Control (IFFC), the concept has been under study and in simulation at General Electric Co.'s Aircraft Equipment division in Binghamton, N. Y. Essentially IFFC mates the new generation of digital flight and weapons control computers with airborne tracking and designation systems like the Atlis II television/laser target tracker that has been developed by Martin Marietta Corp.'s Orlando, Fla., division.

As such, the system does more than relieve the pilot of the need to track a target on a head-up display. It also directs weapons release or gunnery for maximum accuracy during the aircraft's maneuvers. An IFFC will even take over automatic flight of the plane momentarily during these maneuvers.

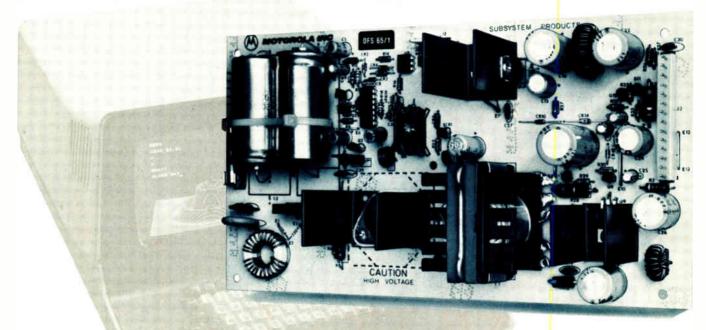
The payoff. GE's computer simulations indicate that the results of the IFFC system would be enormous. In air-to-air combat, for example, compared with today's manual gunnery, the system promises three times more hits; four times as many firing opportunities; four times longer firing time; and the potential for getting into firing position twice as fast.

In air-to-ground missions, compared with manual attack techniques, the new system yields up to twice the bombing accuracy, 10 times less vulnerability to ground fire, and bombing accuracy during wild maneuvering at least equal to that possible with a straight-line, wing-level approach.

The potential has excited the Air Force in part because much of the system is already developed and



**Fire away.** Automated weapons and gunnery control for USAF planes would use essentially off-the-shelf components, integrating flight- and fire-control systems with target tracker.



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#### **Electronics review**

could become operational fast. "If this thing works as well as we think it will, it'll be like having the Red Baron in every cockpit, and with the numbers of potential enemy aircraft we face, we'll need it," quips an Air Force officer stationed at the USAF Wright Aeronautical Laboratory in Dayton, Ohio.

Test flights. The Air Force will flight-test IFFC next year. GE and McDonnell Douglas Corp., St. Louis, Mo., will equip an F-15 fighter bomber with a Martin Atlis II target tracking pod, plus some new hardware and software, for trials at Edwards Air Force Base, Calif.

Output from the Atlis pod-data on target range and relative bearing plus the rate and direction of change of both-will be fed to a GEdesigned computer. A variation of GE's off-the-shelf design for an F-18 flight control computer, the unit will translate this tracking data, feeding it to the F-15's flight- and firecontrol computers. These two computers would be coupled, according to William J. Murphy, who is a senior staff engineer at McDonnell Douglas. Using the Atlis data, the computers would either fly the aircraft or semi-automatically assist the pilot by blending commands from the IFFC system with the pilot's man--James B. Brinton ual ones.

#### Consumer

## Compact VCR raises standards queries

It looks like an 8-millimeter movie camera, but it is really a TV camera with a microcassette that can record 20 minutes of picture and sound. Sony Corp. says that it is showing the prototype to convince the industry to start work on standardization of a cassette and tape format—preferably the one it developed—for these extraordinarily compact combinations of video-cassette recorder and camera.

Sony president Kazuo Iwama says that the company has no intention of producing the product unless there is

#### **News briefs**

#### Harris forms unit for GaAs semiconductors

Harris Corp. plans to form a new semiconductor manufacturing subsidiary in the San Francisco Bay area. Harris Microwave Semiconductor Inc. will manufacture state-of-the-art high-frequency microwave circuits, built with gallium arsenide technology, for use in telecommunications applications. It will be headed by vice president and general manager Richard W. Soshea, formerly engineering manager for the Components Group of Hewlett-Packard Co. and one-time general manager of HP's Microwave Semiconductor division. Initially, the new subsidiary will operate from the San Mateo, Calif., facility of Harris's Farinon division, but the firm is looking for a facility of its own to lease in Silicon Valley.

#### Fairchild, GEC end joint MOS venture

Schlumberger Ltd.'s Fairchild Camera & Instrument Corp. subsidiary in Mountain View, Calif., and Britain's General Electric Co. Ltd. have agreed to terminate their joint venture in MOS semiconductor products. GEC will assume Fairchild's interest in the joint venture located in Neston, England. No reason for the termination was given, but the joint venture agreement did predate Schlumberger's acquisition of Fairchild last year.

#### STC nixes merger with Amdahl

Objecting to various proposed modifications of agreements between computer manufacturer Amdahl Corp. of Sunnyvale, Calif., and its principal shareholder, Fujitsu Ltd. of Japan, Storage Technology Corp. has decided not to merge with Amdahl. Fujitsu and Amdahl have complex and comprehensive cross-licensing accords covering certain future technologies, and the Japanese firm requested that these be modified in order to clarify its relationship in the new company that would have come about from the merger [*Electronics*, April 10, p. 46]. A Louisville, Colo., producer of IBM-compatible disk and tape data-storage peripherals, STC would not agree to such modifications.

an industrywide standard. However, some of his competitors question the firm's intentions.

The competing Japanese consumer electronics makers wonder why the firm started by showing the prototypes to the press and has not yet approached them. They say many companies are doing similar work in the laboratory, but the start of sales is probably four or five years off.

In addition to the slow process of reaching an industry consensus on standards, it may take that long for development of suitable tape. Also, low-cost charge-coupled-device or MOS color sensors are needed, and the Sony prototype includes a new CCD sensor.

Sony and its competitors seem to have reached a consensus on price, though, without ever conferring. They agree that a camera-recorder combination plus a tabletop unit that converts the camera into a playback machine will have to sell for less

than \$900 in Japan to be viable.

Perhaps one reason Sony unveiled its package in New York recently was to show off its single-chip narrow-channel frame-transfer CCD color sensor with 570 by 490 picture elements. The 10.1-by-12.1-mm chip has an active surface equivalent in size to a <sup>2</sup>/<sub>3</sub>-inch vidicon tube. Pictures are taken through a 14-to-42-mm 3 × zoom lens.

Tape. The demonstration unit uses a microcassette measuring 56 by 35 by 13 mm with 25 meters of 8-mm-wide high-coercivity metal tape. The tape is 14 micrometers thick, but Iwama says that thinner tape could be used to extend recording time to 30 minutes.

Two recording heads rotate inside a drum half the size of the 75-mm one used in the company's Betamax recorders. Since the recording often will be dubbed onto a conventional VCR with some degradation of picture quality, a high signal-to-noise

## NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY.

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Linear bestsellers for 1980

TO-237 transistors last up to 8 times longer than TO-5s

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#### NATIONAL ANTHEM

## New COPS<sup>™</sup>Family member puts V.F. on display.

The new COP470 multiplexes four 8-segment vacuum fluorescent displays with no external resistors.

The new COP470 vacuum fluorescent display driver brings the economy and practicality of the COPS microcontroller family to applications using V.F. displays.

The Microwire™- compatible COP470 offloads the system controller by interfacing directly to a multiplexed four-digit by eight-segment V.F. display. In addition, it can be cascaded and/or stacked to drive more digits, more segments, or both.

The outputs on the COP470 switch 35V to drive either large or small displays. Yet it requires absolutely no external resistors to

Versatility in 20 pins. The 20-pin COP470 operates from 4.5V to 9.5V and offers 15 programmable brightness levels. With the addition of an entermologies means of interfacing a microcontroller to a large-digit LED display.

The tamily approach saves you money. The COPS design philosophy is a very practical one—create a powerful family of architecturally compatible devices that combines a common instruction set with a multi-dimensional array of product capabilities.

By optimizing the family's instruction set, each COPS device makes much more efficient use of its on-chip program and data memory than do other microcontrollers. The simpler task-oriented COPS instructions not only take up less memory space, they also accomplish each task in less time.

 temperature ranges. Mask selectable I/O characteristics. Even a MICROBUS™ option.

So now the engineer can choose the COPS controller that most closely matches the requirements of the application.

This family approach therefore results in significant cost savings in three ways. First, the engineer can apply all of the knowledge he has gained using any single COPS device to any application addressable by the entire COPS Family. Second, the entire COPS Family is supparted by a single product development system (the COP400-PDS). And third, COPS devices provide the lowest cost microcontroller solution to your application problems.

And now the COP470 brings vacuum fluorescent display capability to the entire COPS Family of low-cost microcontrollers.

For complishe information on the DCP470 VF display driver and the entire DCP5 Family, check this saum coupon.

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#### Economical IC pressure transducers from National.

Ever since National introduced the first hybrid IC pressure transducer in 1973, engineers have "robotized" a wide variety of electromechanical applications.

Today National offers the broadest line of IC pressure transducers on the market. Their line encompasses not only hybrids, but a full range of monolithic devices as well. All of which offer pressure systems engineers much greater design flexibility than ever before. At much lower design costs than ever before.

These IC pressure transducers are compact and easily interfaced with other integrated circuits. And because National processes silicon in large volume, they can offer these products at very low costs.

In fact, their LX05XX and LX06XX monolithics are the lowest cost IC pressure sensors available. They offer high accuracy and  $\pm 5$  to  $\pm 100$  psi pressure ranges. Their compact T05 and ceramic packages allow easy PC board installation which cuts costs of OEM pressure systems even further.

Of course, the LX16XX hybrid is also available in a ceramic package. This fully signal-conditioned pressure transducer features built-in temperature compensation, high-level output and full voltage regulation.

The LX16XX, in a nylon or diecast zinc housing with NPT fittings and a snap-on connector, becomes an LX18XX. The LX18XX

is ideal for plug-in operation with pressure ranges from  $\pm 5$  to 300 psi.

Far high pressure applications – 100 to 5000 psia – National offers the LX14XX hybrid series. Housed in rugged cylindrical brass or stainless steel, the LX14XX is available with flying leads and an optional fluid isolator. This device is perfectly suited for submersion or tough industrial environments.

Far additional information, check the coupon for the Pressure Transducer Data Packets — including the handbook, data sheets and application notes. Everything you need to get in on the "robotic" revolution from the Practical Wizards of Silicon Valley. 22



# National turns up the volume on their RAM production line.

National has the technical expertise and manufacturing muscle to produce the industry's most popular high performance RAMs.

It takes a great deal of manufacturing and technical know-how to satisfy the ever-increasing demand for static and dynamic RAMs. And National Semiconductor has a lot of both.

In fact, National offers a broad line of the most popular high performance MOS RAMs in the business.

Having just stepped up their production capacity even further, National is able to ship more parts in one month than most suppliers can ship in six. At volumes like these, you can be sure that their prices are competitive.

Vastly superior test facilities. Between the production and shipment of each RAM order come National's high-caliber test procedures.

In addition to their use of conventional component level electrical testing from wafers to tested packages, many dynamic RAM customers request National's unique

MST™ (Memory Systems Test) program.\*

MST eliminates or greatly reduces your own requirements for internal testing. So your incoming test, board test, and system rework costs are substantially reduced. Because MST parts have already been debugged in a 9 megabyte memory system.

The future looks even brighter. In the months to come, National's MOS RAM product line will grow even broader. They will soon add new low-power XMOS™ static RAMs and dynamic RAMs incorporationg their new and exclusive TRI-POLY™ process.\*

The new TRI-POLY RAMs will feature

The new TRI-POLY RAMs will feature (among other things) improved refresh characteristics and a high immunity to soft errors.

To find out just how competitive National really is, contact your local distributor or NSC sales rep.

Between their technical expertise, their high-quality RAMs and their unmatched volume production capacity, it's easy to see that the Practical Wizards are taking random access out of RAM supply.

\*Patent Pending MST, XMOS, and TRI POLY are trademarks of National Semiconductor

## National's TO-237 puts heat on ice.

TO-237 transistors run cooler to last up to eight times longer than metal cans. Yet they cost 40% less.

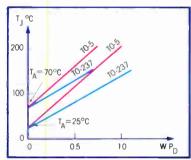
The Practical Wizards from National Semiconductor are offering a refreshing alternative to the TO-5 and TO-39 transistors: the pin-compatible TO-237.†

The TO-237 transistor – encased in National's patented Epoxy B\* plastic – runs so much cooler that it can last eight times longer than the metal cans. As if that wasn't enough, National has priced it 40% less than the short-lived competition.

The key to the TO-237's cool disposition is an exclusive combination of the Epoxy B used in conjunction with an efficient heat dissipating thermal tab. The result, as shown in the graph, is a reliable workhorse component that can last 8 times longer than the cans (at 0.5W dissipation).

National sorts them out. The TO-237s are currently available off-the-shelf in 65 standard part types and pin configurations. However, should a special selection be





JUNCTION TEMPERATURES TO 237 vs TO 5

required, National would be more than willing to supply it.

This kind of design and production versatility comes from over 20 years in the transistor business. So it's no surprise that only National can offer this cool, low-cost alternative to metal can transistors.

For additional information about the Epoxy B transistors, be sure to check this issue's National Archives coupon or contact your local distributor or National sales rep. 22

\*U.S. Patent Number 3838094

tNSC originally applied for JEDEC package registration (1979)

## The totally self-contained precision instrumentation amp with fast settling to 12-bit accuracy.

With a low-noise input stage and a complete thin-film resistor network in a single package, the LH0038 allows precise gains ranging from 100 to 2000.

National, the recognized leader in linear circuitry, is offering their LH0038 precision instrumentation amplifier to design engineers working on data acquisition and related systems.

The LH0038 is the most complete single package instrumentation amp available because it requires no external resistors. In fact, the LH0038 contains four amplifiers, a low-noise input stage and a precision thin-film resistor network – all in a single 16-pin metal DIP.

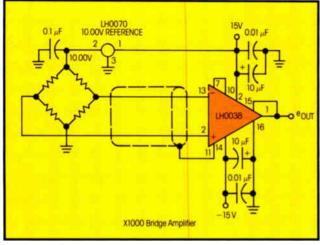
The pin-strap gain options on the LH0038 range from 100 to 2000, which makes it ideal for amplifying very low-level signals (such as thermocouples, low impedance strain gauges, etc.).

**High-performance specifications.** A large part of the LH0038's success in the industry is reflected in some of its key specs.

The LH0038 exhibits an excellent common-mode rejection ratio (114dB at a gain of 1000) and a closed loop gain error of only 0.5% (also at a gain of 1000).

In addition, the LH0038's input offset voltage is an ultralow  $0.25\,\mu\text{V/}{}^{\circ}\text{C}$ . The settling time to 0.01% is typically between 60 and 120  $\mu\text{sec}$ .

Also available in mil-spec version. In addition to National's own stringent REL and QA standards and procedures, a version of the LH0038 amp is also available that meets military standard 883 level B specifications.



For more information on the LH0038 precision instrumentation amp, check the National Archives coupon below for the Special Functions Data Book and the free LH0038 data sheet.

The LH0038 single package instrumentation amp – another minor miracle from the Practical Wizards of Silicon Valley.

#### Special Linear Data Book offer.

National announces the new 1980 Linear, Data Acquisition, Voltage Regulator and Audio data books. And until Labor Day, they're yours for \$20° complete.

National's new 1980 Linear Data Book, the analog designer's "right-hand man," gives you over 1200 pages packed with useful, up-to-date information on the industry's broadest line of Linear components. And until Labor Day, you can add this perennial bestseller to your reference library for only \$6.00 (\$3.00 off the regular price).

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The 1980 Voltage Regulator Hand-

The 1980 Voltage Regulator Handbook covers power supply and regulator design all the way from the transformer to the heat sinks.

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The Practical Wizards of Silicon Valley

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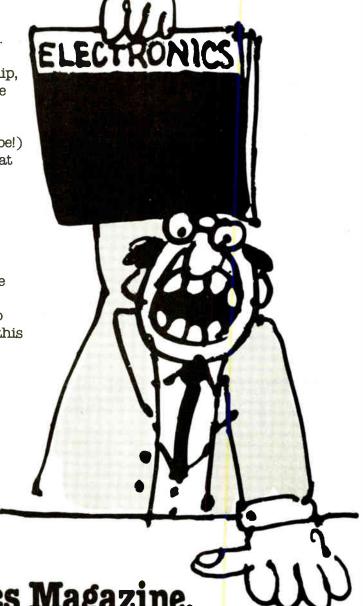
# Who stole page 39?

This whodunit happens all the time. By the time the office copy of Electronics Magazine gets to your name on the routing slip, a page is missing. Or maybe the reader service cards. Or an entire article has been clipped. Sometimes you never get the magazine at all.

Other times the magazine is (glory be!) intact. But dogeared. Or otherwise abused. Or at the very least, you get it late.

O.K., we'll grant that a second-hand, third-hand, or maybe seventh-hand copy of Electronics is better than none. But it's no substitute for the copy that comes directly to you—to your home if you wish—with up-to-the-minute news and information of the technology in this fast-moving field.

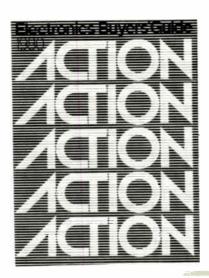
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#### **Electronics review**

ratio is important in this unit. Therefore another two heads on the drum are used for playback.

The demonstration unit weighs only 1.6 kilograms for a small package measuring 191 by 171 by 60 mm. A handle weighing another 0.4 kg incorporates a 9-volt rechargeable silver oxide battery.

For playback the handle is detached and the unit placed in the tabletop unit that includes playback circuits, a power supply, and remote controls for a conventional VCR. The microcassette can be dubbed onto a Betamax or VHS recorder or played directly over a TV. -Charles Cohen

## FCC may reverse a-m stereo decision

The Magnavox stereophonic a-m broadcasting technology favored by the Federal Communications Commission may be dropped by the FCC as a result of intense pressure from proponents of other approaches and from broadcasting station executives. An Aug. 1 FCC meeting is expected to result in a reopened comment period on its acceptance.

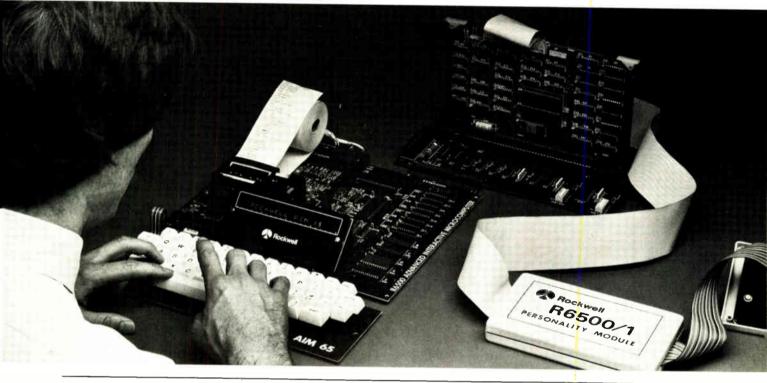
As late as June 25, the FCC was saying only that it planned to delay final acceptance of the Magnavox scheme. But the reopened comment period is a step beyond that delay.

"It is virtually certainty that Magnavox will not get it," avows one competitor. Responds Kenneth C. Meinken Jr., president of Magnavox Consumer Electronics Co., Fort Wayne, Ind., "We are deeply concerned that pressure placed on the FCC staff by other parties to this proceeding may deprive us of a fair hearing."

Furor. Broadcasters are raising a furor over the alleged range limitations and costs of the Magnavox approach [Electronics, April 24, p. 48]. They have mounted a large-scale letter-writing campaign, prodded by proponents of competing technologies such as Motorola Inc. and Harris Corp.

Independent observers estimate a negative modulation limit of 85% for

# Rockwell announces in-circuit emulation at evaluation board prices.



## AIM 65-based Desktop Development Center cuts cost of R6500/1 family software and hardware design.

Pools well Internal

Rockwell International announces a microcomputer development system with in-circuit emulation at the price of most evaluation boards. The heart of this Desktop Development Center is the AIM 65 Advanced Interactive Microcomputer with full alphanumeric keyboard, printer and display.

AIM 65 connects to Rockwell's System 65-bus-compatible Motherboard\* R6500/1 Personality Module and additional RAM card to achieve in-circuit emulation of Rockwell's R6500/1 single-chip microcomputer.
The result: economical microprocessor evaluation, development, debugging and more.
That's Rockwell Micropower!

AIM 65's resident Text and Symbolic Assembler Editor speed program development. And the Debug provides trace, edit, and breakpoint to trouble-shoot software and hardware. An optional high level design language, PL/65, is available.

But the AIM 65 Desktop Development Center is more than just a development tool. Engineers use it as a selfstudyeducational microcomputer, as a professional printing microcomputer using BASIC, and as an OEM standard board computer.

The AIM 65 expands to include additional Rockwell RAM, PROM and ROM cards, and Rockwell Bubble Memory, as well as bus-compatible analog and solid state relay products from Burr-Brown, Compas Microsystems and others.

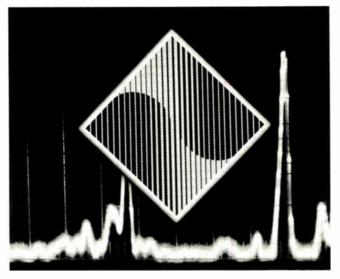
For more information contact your local distributor or write or call AIM 65 Marketing, Electronic Devices Division, Rockwell International, P.O. BOX 3669, RC55, Anaheim, CA 92803, (714) 632-3729.

\*Compatible with EXORciser\* and Micromodule bus. EXORcisor\* and Micromodule are trademarks of Motorola. Inc.



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#### **Electronics review**

the Magnavox design, which would reduce the range of the a-m stereo more severely than competing concepts. "The 15% decrease from the current 100% negative modulation is not insignificant," one consultant says. "The change would decrease signal range."

However, Magnavox disagrees with that evaluation. "The range of broadcast will remain the same. The Magnavox proposal to restrict negative modulation to 95% [will result] in a change so small that it will not mean a discernible loss of range," the company says.

Costs. Magnavox also rejects other claims that its approach would require larger hardware expenditures and more complex interconnection to existing monophonic transmitters. It says an exciter to convert existing transmitters could cost \$3,000 to \$5,000, plus a \$1,000-to-\$2,000 monitor for verifying the quality of the broadcast signal.

Electronics designers at National Semiconductor, Sprague, Signetics, and elsewhere are biting their nails over the confusion and changes in direction. "We've already committed our design to silicon," notes Charles Smaltz, marketing manager for consumer linear products at National.

The National chip, with about the same 10,000-square-mil size and less-than-\$2 price as the previously announced design of Signetics and Sprague [Electronics, May 22, p. 56], will have 8 to 10 proprietary differences, he promises.

Similar. Others do not expect significant variation in chip design, though. "Everybody will get ICs with virtually the same performance," says Jerry Lebow, vice president for receiver consultant Frank Barth Inc., New York.

However, the promised September delivery dates for Magnavox-compatible receiver chips may slide because of the second thoughts at the FCC. If the agency selects another technology, then look for an additional six weeks to three months delay for chip delivery, estimates Peter Loconto, Sprague Semiconductor's director of product development and marketing. -Larry Marion

To:

S. Printz, VP/Planning & Product Development

From:

C. Keith, Components Engineering

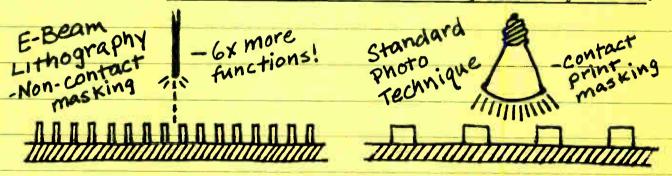
Subject:

What off-the-shelf delivery of OKI's 16K VLSI static RAM

implies for our marketplace.

Evaluation of OKI's new 16K NMOS static RAM (2128-1) turned into more than a performance check. We think the following points are important in considering the implications—and potential—of VISI technology to our future products and memory requirements.

- 1. On-line production of sophisticated 16K static RAMs signals a crossover into a new memory state-of-art. The VISI era is here, now that 100,000 components per chip are available for current product designs. We should consider the implications for our next generation of terminals, printers, minicomputers, and add-on memory products.
- 2. We expect industry interest in VLSI to focus on this 16K static. As one of the first products designed using new electron beam lithography, the OKI 2128-1 squeezes all those functions on a single chip about half the size possible using standard processes. The very close geometries that E-Beam can produce yield a 16K static memory equivalent in density to a 64K dynamic RAM.



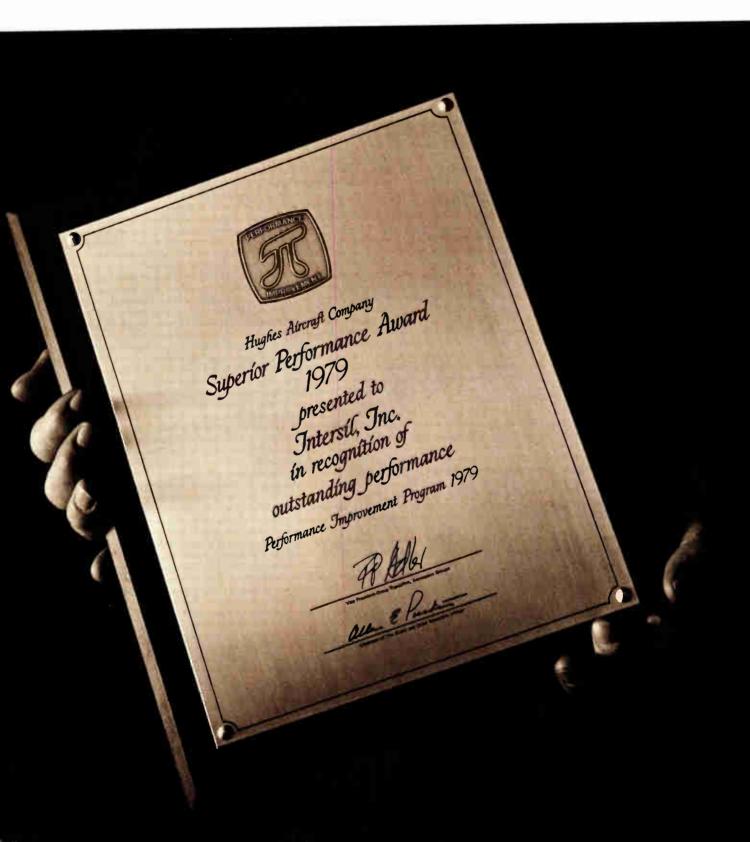
- 3. In our opinion, E-Beam VLSI will shakedown the memory-supplier ranks. It's so complex that tremendous time, manpower and capital investments are required: an order of magnitude over previous technology. Few manufacturers can match the financial and technical resources of billion-dollar OKI corporate—who committed to E-Beam back in '77-'78. A long headstart that will be hard (and expensive) to catch. Especially with most sources just beginning to install/trial-run E-Beam machines.
- 4. The attached Ad Coupon backs up our view that OKI is far past the seminar/
  sampling stage. And any company that can produce, market and deliver 16K VLSI
  static RAMs from distributor stock has to be considered a major memory source.

C. Keith

- P.S. If you'd like to explore these implications with OKI, contact Sales Director Ron Engelbrecht, OKI Semiconductor, 1333 Lawrence Expressway, Santa Clara, California 95051. (408) 984-4842.
- P.P.S. With their 2128-1 launched, ask OKI how soon they expect availability of 64K dynamics!

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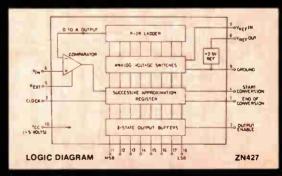


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#### Washington newsletter\_

#### SIA persuades U. S. to break out IC Import data

New details on imports will be broken out of semiconductor trade statistics under a modification of the U. S. Tariff Schedules. Separate statistical subdivisions for microprocessors and memory integrated circuits are being established this month under an agreement among the Departments of Commerce and Treasury and the U. S. International Trade Commission, following a request from the Semiconductor Industry Association. The SIA will be asked to aid the U. S. Customs Service by supplying technical information to ensure that the reported statistics are accurate, says Robert E. Herztein, under secretary of commerce for international trade.

## Fujitsu's computer success at home establishes pattern . . .

Though Fujitsu Ltd. has become the first Japanese computer maker to top IBM Japan Ltd. in domestic sales [Electronics, June 5, p. 64], four other companies there outdid Fujitsu in posting percentage gains. The U. S.—Japan Trade Council, Japan's industrial lobby in Washington, says that Fujitsu had domestic sales of about \$1.513 billion in the fiscal year that ended in March, up 8% from the year before. At the same time, IBM Corp.'s manufacturing and marketing subsidiary reported \$1.501 billion in Japanese sales for calendar 1979, its comparable fiscal year.

It says the other Japanese computer makers that had even larger percentage gains than Fujitsu in fiscal 1979 sales were Hitachi Ltd. with \$1 billion (up 14%), Nippon Electric Co. with \$929 million (up 20%), Mitsubishi Electric Corp. with \$245 million (up 18%), and Toshiba Corp. with \$233 million (up 17%). Japanese production of computers and peripherals overall in 1979 rose 23% to \$5.185 billion, says the trade council, including \$2.083 billion in mainframes (up 22%) and \$1.257 billion in terminals (up 56%).

## . . . but U. S. exports soar by 33% in last quarter

American exporters of computers and related equipment seem nonetheless undeterred by rising competition from Japan as they reported a record \$1.4 billion positive trade balance with all foreign competition for the first 1980 quarter. Exports rose by one third over the first 1979 quarter, to \$1.66 billion, while imports climbed just 12% to \$259.3 million, according to Census Bureau data compiled by the Computer and Business Equipment Manufacturers Association. The bad news for the U.S. industry in the first quarter came in other business equipment, including word processors and automatic typewriters, where imports jumped 23% to \$478.6 million, thus exceeding exports of \$332.9 million, which rose only 13% from the 1979 level.

## NASA names four firms to define oceanic satellite

The National Aeronautics and Space Administration has picked four contractors from six who submitted proposals to negotiate Phase 1 system definition studies for the National Oceanic Satellite System (NOSS). Named to negotiate for the \$750,000 nine-month studies leading to selection of a single Phase 2 hardware development contractor in fiscal 1981 are: General Electric Co.'s Space division, Valley Forge, Pa.; Lockheed Missiles and Space Co., Sunnyvale, Calif.; RCA Corp.'s Astro-Electronics division, Princeton, N. J.; and Rockwell International Corp.'s Satellite Systems division, Seal Beach, Calif. Dropped from the competition were Hughes Space and Communications Group, El Segundo, Calif., and McDonnell Douglas Astronautics Co., St. Louis, Mo.

#### Washington commentary.

#### Postponing action on the Communications Act

The 96th Congress is proving no different from its predecessors as it rushes to adjournment in an election year. Anxiety, if not hysteria, is evident as legislators strain either to pass or to vote down the bills that remain on the calendar. The pending rewrites of the Communications Act of 1934—H. R.6121 in the House and S.2827 in the Senate—are perfect examples.

Since the initial introduction nearly five years ago of the so-called Bell bill, this legislation has gone through numerous rewrites, revisions, and hearings. These have been almost ignored by most members of the Congress, many of the affected communications companies, and much of the press. Now, however, with deregulation the current popular cause in Washington, it seems everyone is becoming involved, demanding passage or postponement, depending on individual biases. And these demands are getting lots of press.

#### Momentum versus bad law

Among those driving for passage is a new ad hoc group. Called the Coalition for Telecommunications Reform Legislation, it is made up principally of three large independent telephone companies, two communications labor unions, and a handful of trade associations [Electronics, July 3, p. 65]. Chairman Paul Benson of United Telecommunications Inc. believes that "if we miss this opportunity, it may be another two to four years before we can get up the momentum again." Nevertheless, he concedes that passage of a bad bill would be worse than no bill at all.

Former Attorney General William R. Saxbe, who brought the pending antitrust suit against AT&T in 1974, believes H. R.6121 is a bad bill. Despite legislative language that would protect the ongoing litigation, Saxbe is convinced the bill will in effect gut the Government's antitrust case. "It would be ridiculous," he contends, "to go ahead and try the case when they [AT&T] already have a whitewash before it starts" under a law that would let AT&T and other dominant carriers compete in new markets through arm's-length subsidiaries.

Saxbe believes the 1956 consent decree that settled an earlier AT&T antitrust action by prohibiting it from competing in other than telephone markets should be modified by the court before which it was negotiated, not by Congress. A legislative "end run" of the courts is a mockery of the law, he says. A former Ohio Senator, Saxbe now speaks on behalf of a half-dozen Ohio interconnect companies that his law firm represents. Asked why some leading legislators

support the bill, he replies, "I don't think they have read it."

#### A second look at antitrust

Two Senators who have read the tougher S.2827 and are concerned about its antitrust implications are Edward M. Kennedy (D., Mass.), chairman of the Judiciary Committee, and Howard Metzenbaum (D., Ohio), chairman of the antitrust subcommittee. They want Sen. Howard Cannon (D., Nev.), whose Commerce Committee has jurisdiction over the bill, to let their staffs review the antitrust implications of deregulation. Cannon and key members of his committee have consented.

Following that Senate action, House Judiciary Committee chairman Peter W. Rodino (D., N. J.) wrote Commerce Committee chairman Harley O. Staggers (D., W. Va.) warning that notwithstanding H. R.6121's antitrust neutrality language, the bill's substantial restructuring of the communications industry "will have a dramatic effect on the bargaining positions of the parties in the pending litigation, perhaps impairing the chances of a settlement, or drastically altering the terms that could be attained."

The electronic mail portion of S.2827 is but one more unsatisfactorily resolved issue, according to Government Affairs Committee chairman Abraham Ribicoff (D., Conn.). He believes the issue should be either deleted from the bill or referred to his committee.

Guarantees for the protection of the research capabilities of Bell Laboratories in their present form is another concern expressed in a joint letter to the Senate by Frank Press, the President's science and technology advisor, and by Jerome B. Wiesner, president of the Massachusetts Institute of Technology.

#### No rush to judgment

No bill can satisfy all interests, of course, for law making is the art of compromise. But good law making stems from thoughtful compromise, something that cannot be achieved during the current rush to adjourn. Too many important changes to the bills have come in committee and not been the subject of hearings.

Suspension of further action on the measure until the next Congress seems the best step at this point. For—as a proponent of passage, Paul Henson of United Telecommunications, admits—a bad bill is worse than no bill at all. And the House version of this bill, despite its multiple revisions, is still essentially a bad bill [Electronics, Jan. 31, p. 50]. -Ray Connolly

#### **HIGH CAPACITANCE PER CASE SIZE**



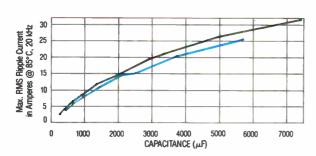
**LOW ESR** x. ESR in Ohms 25°C, 20 kHz 2000 4000 CAPACITANCE (µF)

Curve plotted in gray represents capacitors rated at 200 VDC. Curve plotted in blue represents capacitors rated at 250 VDC.

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Values as high as 7,400 μF @ 200 VDC in a 3" x 5.625" case.

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## Three very good reasons why you should give TI four hours of your time.



## TI's newAdvanced Bipolar Logic seminars start Monday, August 11.

On Monday, August 11, TI is kicking off a new series of seminars that will examine the role of bipolar logic design. A series of seminars that will provide an in-depth look at performance, power and reliability improvements with AS/ALS — for better systems solutions.

It's a different kind of seminar. Learning-intensive. For system designers who need to know what the future holds for Advanced Schottky, Advanced Low-Power Schottky and Low-Power Schottky.

The agenda will fill you in

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Information that could give you the competitive edge today for leading state-of-the-art products tomorrow.

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For complete information and to guarantee yourself a seat (sorry, only preregistered attendees are eligible to win the calculator) call your local TI field sales office or authorized distributor at least one week prior to the semi-

nar in your area.

The dates, locations, names of contacts and phone numbers are listed on the right.



84618

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#### TEXAS INSTRUMENTS

#### Agenda

• TI's Schottky Families for the '80s... characteristics, applications and compatibility:

Low-Power Schottky

- High-performance Schottky
- Second Generation Families:

· Advanced Schottky

Advanced Low-Power Schottky

• New product previews

Quality/reliability improvements

High-density packaging innovations:

• Chip carrier packages

New 24-pin DIPs

#### **Dates, Locations, Contacts**

Date	Location	Contact	Phone	Date	Location	Contact	Phone
August 13 August 15 August 18 August 20 August 22 August 25	Boston (Waltharn) New York (Melville) New Jersey (Clark) Philadelphia (Ft. Washington) Washington (Arlington, VA) Florida (Ft. Lauderdale) Minneapolis (Edina) Chicago (Arlington Heights)	Jack Edick Chuck Messmer Terry Manton Ken O'Connor Jim Myers Hank Keuhler Roger Scott Dave Nesbitt	(617) 890-7400 (516) 454-6616 (201) 574-9800 (215) 643-6450 (703) 553-2200 (305) 973-8502 (612) 830-1600 (312) 640-3000	August 29 Sept. 8 Sept. 10 Sept. 12 Sept. 15 Sept. 16 Sept. 17 Sept. 19	Dallas Denver Seattle (Bellevue) San Francisco (Sunnyvale) Phoenix Los Angeles (El Segundo) Orange County (Costa Mesa) San Diego	Jim Roundtree Ken Mudge Dave Burkhart Tom Addie Bill Tanner Jim Davi Joe Favela John Lucas	(214) 995-6531 (303) 695-2800 (206) 881-3080 (408) 732-1840 (602) 249-1313 (213) 973-2571 (714) 540-7311 (714) 278-9600

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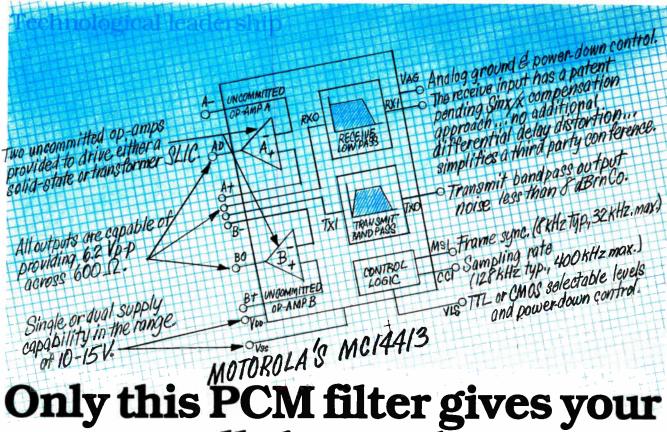
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## systems all these advantages

There's no better way than Motorola's new MC14413 for using an LSI PCM filter to meet the goals of saving time, space and cost in telecommunications systems while maintaining or improving performance.

Motorola's MC14413 is the one outstanding PCM filter that is loaded with unique features, offers the low power, producibility and reliability of standard metal gate CMOS, and meets all Bell System D3 and CCITT specs. The MC14413 is in full volume production, and arrangements have been made with RCA as a mask- provided second source.

The MC14413 operates from either a single or split power supply, with a single supply from 10 V to 15 V, or a range of  $\pm 5$  V to  $\pm 7.5$  V with 5% tolerance for split supplies. Therefore, in addition to the natural CMOS compatibility, it's also TTL compatible.

Our patent-pending method for universal Sinx/x compensation introduces no additional differential delay distortion, allows three-party conferencing without external circuitry and provides for a variety of other system savings we'd like to discuss with you.

Power supply rejection is excellent at better than 40 dB, and cross talk is superior at 80dB or better. Temperature performance is excellent, too. Gain and ripple stability over a 0 to 70°C temperature range is .0007 dB °/C. The naturally low-power characteristic of CMOS permits the filter to dissipate a very low 25 mW in operation and a miniscule  $125 \mu W$  while in the power-down state, all without design tradeoffs. When this filter is used on a single supply with

Motorola's MC14404/6/7 codecs, the filter powers down automatically with the codec.

Each filter output (AO, BO, RXO) is capable of providing 6.2 V p-p across  $600 \Omega$ . This means that in the push-pull configuration, 600  $\Omega$  and 900  $\Omega$ loads can be driven to +18 dBm.

Last year, Motorola put the industry's first lowpower, switched-capacitor, sampled data PCM filter, the MC14414, into volume production. All the advantages of this innovative circuit have been retained in the 14413, and more have been added. Where required, the MC14413 is an excellent drop-in improvement for the MC14414. The receive sections of both filters are the same, with a 5-pole elliptic filter operating at a sampling rate of 128 kHz. In the transmit sections, where both also have the 5-pole elliptic low-pass filter, the MC14413 incorporates a 3-pole Chebychev high-pass filter for 50/60 Hz and 15 Hz rejection.

Motorola's matched codecs and filters together meet all required system specs for subscriber line interface units. As integral segments of Motorola's LSI approach to total telecommunications systems, they show the way to

Innovative systems through silicon.



#### International newsletter

## 13 Japanese companies adopt Pascal language

Look for Pascal to come to Japanese microcomputers in a big way soon. Since February, 13 Japanese companies have received licenses from Softech Microsystems in San Diego, Calif. The thirteenth—Japan Business Automation Co., a software subsidiary of Toshiba Corp.—will also be the last, having been granted the rights to offer sublicenses to others. A spokesman at the firm says that Softech has licensed its structured analysis and design technique software to Toshiba since 1973 and thus had sufficient confidence to make Toshiba's subsidiary its sole agent. He expects Pascal to replace Basic in many applications over the next few years. The other 12 Pascal licensees are: At Electronics, Fujitsu, Hitachi, Matsushita, Nikko Telecommunication, Nippon Electric, Oki Electric, Sanyo Electric, Sharp, Sony, and Sord Computer Systems.

## UK logic tester detects faults in feedback loops

The Locator, a field test instrument developed by Solartron Electronics Group specifically for microprocessor-based products, brings a battery of eight test and measurement techniques to bear on tracking down an obstinate fault. Most notably, it has a signature analysis capability complemented by trace analysis, a technique borrowed from the world of automatic testing. According to Brian Kett, digital instrument product manager at the Farnborough, Hants., Schlumberger subsidiary, the new technique succeeds where signature analysis fails—in feedback loops, where a faulty node can ultimately cause all the other nodes to display fault signatures. Trace analysis, on the other hand, lets the engineer trace a fault back to the earliest time frame and the first node in which it occurs. Itself microprocessor-based, the Locator weighs 15 lb in a 17-by-12-by-4-in. case and sells in the UK for \$3,250 without options.

## Vhf direction finder from West Germany has only ±0.1° error

West Germany's Rohde & Schwarz, the Munich-based instruments and communications equipment maker, has developed a precision, very-high-frequency direction finder featuring an accuracy of within  $\pm 0.1^{\circ}$ , five times better than conventional vhf equipment, according to the company. Developed under contract to German maritime authorities for spotting ships in narrow channels, the PA 001 picks up ships carrying vhf radio systems at ranges of up to 80 km (about 50 miles), fixing their position on a radar screen to within 20 to 30 meters. Readings are shown on a four-digit display and can be fed to external processing equipment.

## Hermetic fiber-optic transmitter module targeted at telecoms

Though there are several epoxy-sealed fiber-optic transmitter modules on the market, fully hermetic packages capable of meeting stringent post office requirements are not yet established. One of the first comes from the Paignton, England-based Microwave and Electro-Optic division of the ITT Components Group. A metalization layer is applied to the cladding of the fiber-optic pigtail so that it can be hermetically sealed into the feed-through. The resulting 10-pin dual in-line package accommodates a submount for the laser diode and an integral power output monitor that allows for the temperature stabilization of the diode output. There is also space within the package for two hybrid circuits accommodating any needed driver circuitry in high-bit-rate (560-Mb/s) applications. Currently ITT uses a gallium arsenide and gallium aluminum arsenide double-heterostructure laser diode with 6-mw output and 180-mA threshold that has been proven in operation for two years on a 140-Mb/s link.

#### International newsletter\_

## Monomode fiber for high data rates waits in wings

Standard Elektrik Lorenz AG, the Stuttgart subsidiary of ITT, will not start producing its new monomode optical fiber until it has lined up some buyers. But the wait may be a long one, even though the fiber has an average attenuation of less than 1 dB/km. The reason is that the current price for connectors for the 4- $\mu$ m-diameter fiber is \$570. SEL engineers believe monomode fibers are the only fibers capable of handling very high data rates of 140 to 560 Mb/s.

## West German P. O. starts fax-based mail service

Using a combination of classical postal service and modern communications technology, West Germany's post office started an experimental scheme for letter transmissions last month. Called Telebrief—German for teleletter—it transmits information on standard-format pages by facsimile equipment between any of 600 post offices in West Germany. At the destination station, the letter is put in an envelope and delivered to the addressee the same day. At the transmitting station, the sender has his original letter either handed back to him or, on request, mailed to him later. The fee is about \$6 for the first page, roughly \$2.30 for each additional page. Telebrief's big advantage is that it can transmit not just text, like telegrams, but also diagrams and other graphics.

The French telecommunications administration started public facsimile service some three years ago and now offers it in about 40 cities. However, the addressee has to pick up his letter at the receiving end.

## Apple computers establish beachhead in Japan

Japan's present 6% share of Apple Computer Inc.'s worldwide sales of personal computers should double in the next 18 months, predicts sales vice president Gene Carter, now that Cupertino, Calif., firm has an official import representative in Toray Industries Inc. (For the reverse trend, see story on p. 85). Toray will provide full support for the Apple computers, including servicing. Short-range plans call for first-year sales of 10,000 of the new Japanese version of Apple II, due out next month. Major differences include a Japanese katakana syllabary pattern generator and key tops and a one-year guarantee to show the quality-conscious Japanese market that the company stands behind its products. Long-range plans include the establishment of Apple Japan Ltd.

## Two 850-nm signals pass each other in French optical fiber

An optical-wavelength multiplexer and coupler capable of sending and receiving video transmissions simultaneously and at the same 850-nm wavelength along a single multimode optical fiber is being developed by TRT (Télécommunications Radioélectriques et Téléphoniques), a French subsidiary of the Netherlands' Philips group. Each signal follows its own path, spiraling around the signal headed in the opposite direction. While the system, developed as part of a military contract, now handles only 20 kb/s, megabit rates are expected soon.

#### Addenda

According to an agreement between the two companies, West Germany's BASF AG this fall will start marketing under its own label in Europe, Brazil, and Argentina Hitachi Ltd.'s large computer systems. . . . The National Aeronautics and Space Administration has ordered a \$17 million instrument pointing system for its space shuttle from West Germany's Dornier System GmbH.



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Our second-generation JFET Input Op Amp, now known as QUADRAFET." features precise input matching without the use of laser trimming. So you're getting an inherently superior design.

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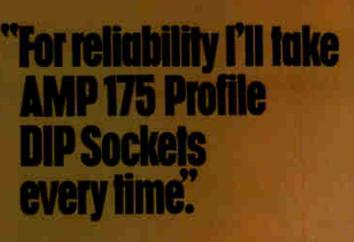
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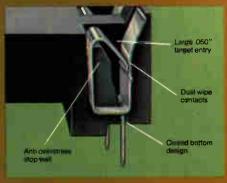


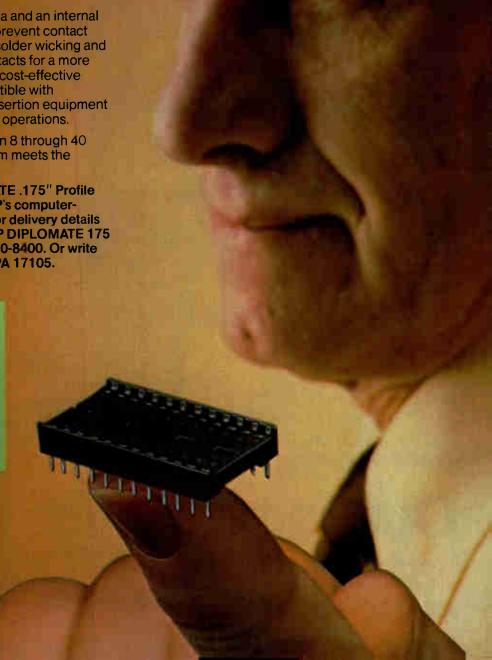
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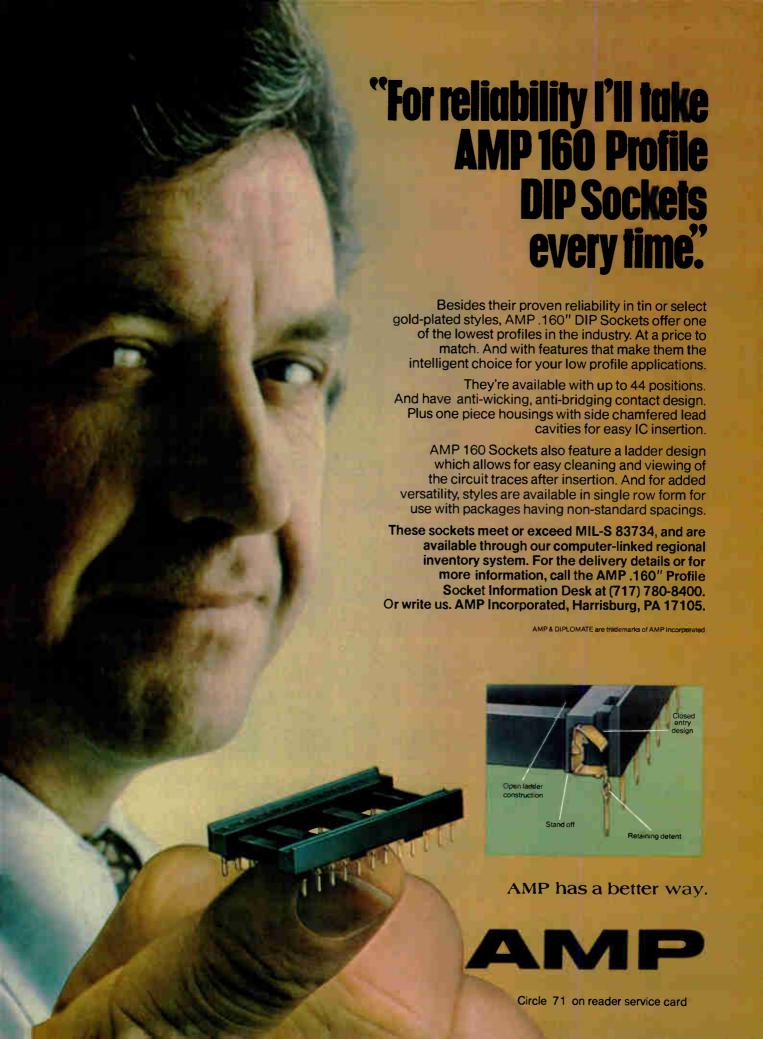
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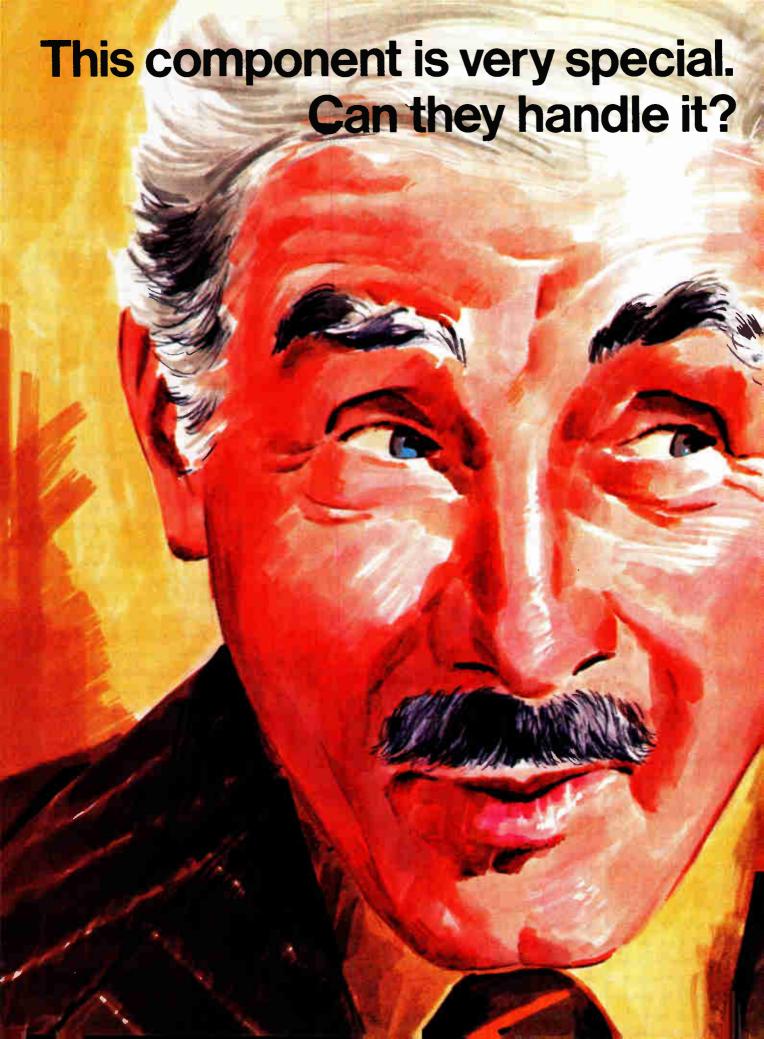
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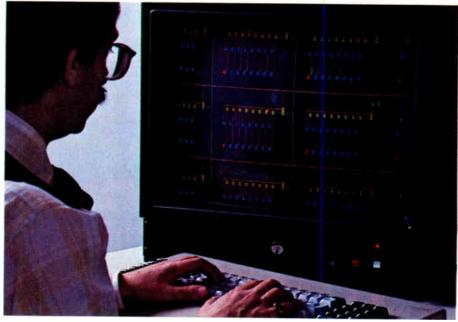
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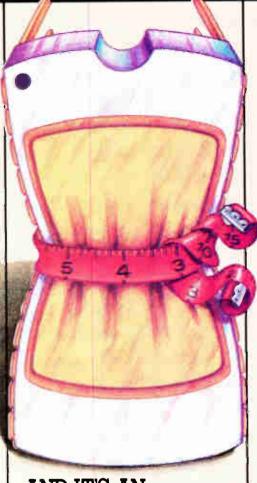
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Significant developments in technology and business

### Lowered i-f shrinks fm radio onto one chip

by John Gosch, Frankfurt bureau manager

Key to its design are an intermediate frequency of 70 kHz, a reduced i-f swing, and 'correlation' muting

Virtually an entire frequency-modulation receiver has been integrated, all the way from the antenna input to the audio output, on an experimental 3.5-square-millimeter chip. Only a tunable resonant circuit and 14 ceramic capacitors are external to the chip, report its developers, the Philips Research Laboratories in Eindhoven, the Netherlands.

The result of a three-year effort, the advance is expected to have a big impact on fm radio design over and above the obvious diminution in equipment size. The number of receiver adjustments made at the factory will drop from the normal 10 to 14 to only 2. "Besides, it is reasonable to expect a substantial decrease of circuit costs as well as receiver assembly time," notes research team head Dieter Kasperovitz.

To be sure, efforts to integrate fm receivers are being made at other labs. But these aim simply at replacing the receiver's transistors with integrated circuits and little is gained in cutting circuit costs and improving receiver performance.

Radical. The Philips concept, on the other hand, radically alters receiver design in two ways. First, it lowers the intermediate frequency from the normal 10.7 megahertz to only 70 kilohertz, so that the critical tuned inductance-capacitance filters can be replaced by simple untuned resistance-capacitance types. Thus, coils with a Q of less than 1 can be used instead of the hard-to-integrate high-Q coils needed with LC filters. Also, all receiver adjustments are eliminated except the two made to the external resonant circuit, to define the fm band limits at 87.5 and 108 MHz.

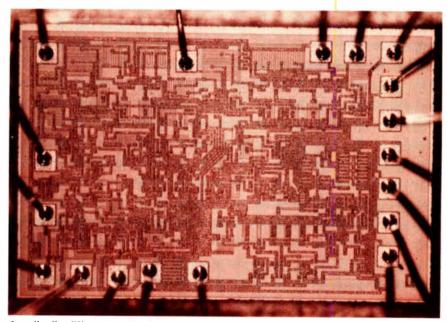
Second, frequency feedback is employed to eliminate the audio distortion that, with the ±75-kHz fm receiver i-f swing common in Europe, would otherwise occur at a 70-kHz i-f. The feedback reduces the swing to ±15 kHz, a value at which harmonic distortion is all but absent.

Correlation. On top of this, the Philips receiver incorporates a new muting system. Based on the correlation between the i-f signal and a delayed and inverted version of it, it suppresses audio signals at improper

tuning or at input signals comparable to the input noise. Thus it combines the features of an ordinary muting system and a deviation muting system based on automatic frequency control principles.

Under proper tuning, the two i-f signals used in the mute system are identical, and that results in large correlation. The demodulated audio signal is then switched to the audio output. Under detuning, one half of the period of the original i-f signal no longer corresponds to the delay time between the original and the delayed i-f signals. The correlation is then small or negative, and the demodulated audio signal is squelched. This way, tuning to image frequencies is suppressed.

Using standard bipolar technology, the experimental chip integrates



A radically different radio. Experimental 3.5-mm<sup>2</sup> chip contains entire fm radio. The only external components needed are 14 ceramic capacitors and a tunable resonant circuit.

#### **Electronics international**

about 280 circuit elements (see photo). The cutoff frequency of the transistors is around 800 MHz. The supply voltage range extends from 3 to 18 volts, and current consumption at 6 V checks in at 9 milliamperes. Continued work at Philips could decrease chip area to 3 mm<sup>2</sup>.

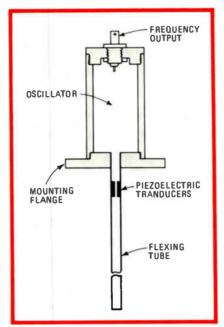
#### **Great Britain**

## Vibrating transducer has digital output

The ideal interface between the analog world and a digital system would be a transducer with a digital rather than an analog output. But few such devices have made the leap from the laboratory bench to the production floor.

One of the latest to do so is a vibratory transducer probe developed by Marconi Research Laboratories for a sister company that plans to use it in fuel management systems. The device can be adapted to measure liquid level, density, or viscosity or combinations of these parameters. In its first application, it gives a direct reading of the mass of fuel in an aircraft's tanks—the critical parameter in assessing the number of flying hours at a pilot's disposal-from the product of simultaneous depth and density measurements.

The probe is a cylindrical metal tube that is made to vibrate and. when inserted in a liquid, does so at a frequency determined by the liquid's level. The tube is typically 30 centimeters long and has a 2-millimeter-thick wall. Epoxy-bonded inside it are two piezoelectric transducers, to one of which a tracking oscillator applies a sinusoidal voltage, causing it to expand and contract lengthwise. As a result, the tube undergoes a sinusoidal flexural vibration. The frequency of this vibration is detected by the other piezoelectric device, which feeds a phase-locked loop that adjusts the oscillator frequency. The squaredoff signal is interpreted by being counted against a reference clock.



**Simple.** Oscillator keeps tube vibrating at rate set by characteristics of surrounding liquid. Output frequency is squared off.

According to Roger M. Langdon, who heads up the project at the laboratories in Great Baddow, Essex, a lot of calculation is required to generate the output parameter from the input frequency. But, he says, the low cost of digital processing makes the approach economically feasible.

Ruggedness and an output frequency dependent mainly on the probe's mechanical characteristics are its major attractions, adds Langdon. Most transducers used in industrial measurement need extra circuitry to digitize their output. But converting at source to digital signals eliminates converter errors as well as the effects of electrical noise in the transmission path. The approach also allows the use of multiplexing techniques, with consequent savings in cabling costs, and squares well with microprocessor technology.

Though not the first in the field a vibratory density transducer is already commercially available—the Marconi researchers have extended and refined the technique.

Refinements. For example, when applied as a fluid depth gauge, a vibratory transducer has an output only approximately linear with depth, because standing waves at

various intervals produce vibrational nodes along the length of the rod with corresponding fluctuations in output. The group therefore uses two sets of transducers to establish orthogonal flexural vibrations, longitudinally displaced from each other by a quarter wavelength, so that their outputs, when added electronically, yield a linear relationship between frequency and liquid level.

Again, the group has devised techniques of measuring several parameters simultaneously. One of the most sophisticated is a submarine battery meter, developed under a Ministry of Defence contract, that checks the electrolyte's density and liquid level. The sensing element in the meter is a glass tube with a small, four-bladed paddle wheel at one end and a pair of transducers at its upper end. One transducer produces torsional vibration of the paddle wheel, reflecting the electrolyte density, and the other produces flexural vibration of the glass tube, measuring the product of liquid level and density.

So far, the transducer manufacturers Langdon has talked to have been wary of the new techniques, but with a first production application due to be proved, that situation could change.

-Kevin Smith

#### Italy

## Single IC regulates car battery voltage

Spikes as high as 100 volts can develop on the 12-V supply line connected to an automobile's battery, and 24 V may appear there under hot-shot cranking using an extra battery in series. Then there is always the risk that accidentally reversed battery connections will reverse the polarity of the supply.

The only integrated circuits certain to survive such harrowing conditions would have to be fabricated with a high-voltage technology on large and therefore expensive chips. But cost-conscious auto makers need not worry—according to Aldo Ro-

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#### **Electronics international**

mano, the applications and product marketing manager of SGS-ATES Componenti Elettronici, only one such chip is necessary, a voltage regulator that protects the car's entire electrical system.

The Italian semiconductor house, based in the Milan region at Agrate-Brianza, has gone to market with three terminal regulators for this system approach. The L 2600 series delivers a closely regulated voltage for ICs and also suppresses the spikes that plague an automobile's electrical circuits. "We have started deliveries of a 5-V version to a major automobile manufacturer and are supplying samples of 8.5-v and 10-v versions," Romano reports. The regulators are the first members of an extensive family of automotive linear ICs, he adds.

Current concerns. In the quantities auto makers buy, the regulators sell for roughly \$1 each. To manage a price that low, SGS-ATES kept the units' current capability to 500 milliamperes, enough to power a car's dashboard instrumentation, for example. When more current is needed, a specially designed pass transistor can be added. It is a pnp device, with a very low voltage drop at saturation and a very high base-emitter breakdown voltage, that can handle up to 20 amperes. It will sell in volume for about \$1.45.

A block diagram of the L 2600 looks much like that of a conventional IC three-terminal regulator, explains Giordano Seragnoli, SGS-ATES' marketing manager for linear ICs. But, he goes on, considerable innovation was needed in the protection circuits for the output stage and for the reference generator to achieve an IC that can withstand the automotive electrical environment. Its key maximum ratings: input voltage to +30 V, with reverse inputs to -18 V; positive spikes to 120 V, negative ones to -90 V; drop-out voltage of 1.7 V; and operating temperatures of -55° to 150°C.

For the chip, SGS-ATES uses a high-voltage diffusion technology that has a collector-emitter (with base open) breakdown voltage (V<sub>CEO</sub>) of 80 v minimum and a col-

lector-base (emitter open) breakdown voltage ( $V_{\text{CBO}}$ ) of 130 v minimum. The overvoltage protective circuit in the output stage is arranged so that the base of the output transistor is grounded when a positive transient occurs. That way the transistor can handle voltages up to the  $V_{\text{CBO}}$  level. A pair of integrated diodes protects against negative transients and polarity reversal.

For safe operation, the chip temperature was to be held to 150°C at most. When that limit is reached, the internal dissipation is lowered by diverting the output transistor base current to ground. The control is through a pair of temperature-sensing transistors located close to the output transistor.

For current limiting, the voltage drop across a sensing resistor is amplified. At the maximum permissible current of 0.5 A, the amplified drop switches on a transistor that bypasses the base current.

The reference voltage is held to within  $\pm 1\%$  of the nominal 1.2-v

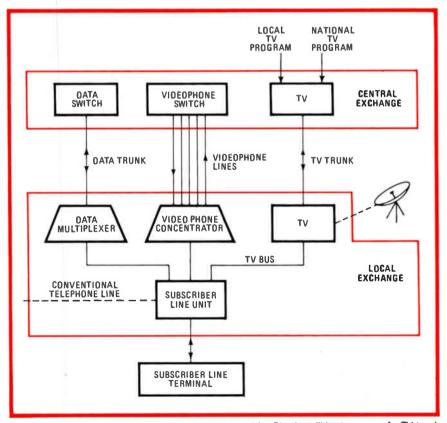
level despite a dispersion of ±3% or so in production. The means is a pair of zener diodes in the voltage divider that multiplies the basic 60-millivolt level obtained from two transistors biased at the same current level but having a 10:1 emitter-area ratio. To adjust the reference voltage, 7 v across one of the zeners short-circuits it and changes the voltage divider ratio.

-Art Erikson

#### France

## Fiber-optic net to link thousands of homes

Best known for its bikinis and beaches, Biarritz is now about to acquire an experimental network of fiber-optic cables. And though the contracts for the French government's \$75 million project will not be announced for another month or so, a fairly clear picture of who and and what is involved has emerged.



**Wired city.** All services in the fiber-optic net planned for Biarritz will be two-way. As TV trunk can handle only three programs, subscriber will signal central exchange which he wants.

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#### **Eiectronics international**

The two post office ministry agencies involved, the Direction Générale des Télécommunications and Télédiffusion de France, have not yet said how many households in the southwestern French city (population 27,700) will be hooked up once the experimental network starts operating early in 1983; informed estimates run from 2,000 to 5,000. Bell Canada's net in Toronto links 35 [Electronics, Jan. 18, 1979, p. 41]. The network will pipe into subscribers' homes programs from France's three national television stations, a color videophone (or picturephone) service, and interactive videotext, as well as a conventional telephone service (which will not replace subscribers' existing phones).

Hierarchical. With transmissions expected to be at a 1.3- or 1.55-micrometer wavelength, the network will be built with conventional 50
µm-diameter multimode fibers. It will be organized in a hierarchical, starlike architecture—much like a telephone network—with several local exchanges feeding into a central one (see figure on p. 80). Each local exchange will contain scores of subscriber line units, one for each subscriber.

The early subscribers will probably be tied into their local exchange by a pair of fibers, one each for outgoing and incoming transmissions. The links will not be longer than 1 kilometer. Later, a more economical single-fiber link can be expected, once the necessary optical-wavelength multiplexers come down far enough in price.

Besides the three national TV programs, some extra programs will be provided. However, the multimode fiber can handle no more than three at one time, each occupying 6 megahertz of bandwidth, the equivalent of 34 megabits per second. So subscribers will choose their programming through a small control unit whose digital signal from the unit will be carried along either the trunk used for TV transmission or an adjacent, low-capacity line. Eventually, national programs may be fed into local exchanges through directbroadcast TV satellite.

The data-transmission service is expected to be fully interactive, with multiplexing done at the local exchange. Videotext will be transmitted via the data line, which may also be used for fully digital telephone service. Otherwise, each subscriber-line unit in a local fiber-optic exchange will probably be linked, via a conventional analog line, to a local telephone exchange.

Quality. The most costly and the most controversial service to be provided is the switched color videophone. The DGT has so far insisted on a high-quality (34-Mb/s) service, giving each fiber a three-signal capacity, as for TV programming. But some of those involved with the project see a 2- or 8-Mb/s videophone service as more realistic, given the project's overall budget.

As far as who will supply which part of the network, French industry officials are betting that contracts will be shared among the four companies that have already received about \$150 thousand each for preliminary studies. They are Thomson-CSF and its transmission subsidiary LTT, ITT'S LCT and CGCT subsidiaries, the Compagnie Générale d'Electricité's CIT-Alcatel and Cables de Lyon subsidiaries, and the SAT.

-Kenneth Dreyfack

#### Japan

## 2-mil lines condense multilayer hybrids

For the country's commuters, the new ticket-dispensing machines that Japanese National Railways started putting into service in late April are nothing special—just another kind of vending machine. But for the hybrid functional circuits development department of Toshiba Corp., they signify a solid achievement. The thermal printing heads of the dispensers are built around high-density multilayer hybrid circuits having 2-mil (50-micrometer) line widths and sometimes 1.2-mil spacings.

Tamio Saito, leader of the group that developed the interconnection

method around a combination of thin- and thick-film technology, says the new hybrids pack in 20 to 30 times as much circuitry as conventional printed-circuit boards carrying dual in-line packages. For the 352-dot ticket printing head, a serial-to-parallel converter and driver circuits are built in, eliminating a large external parallel signal source and the bulky 352-conductor cable needed for earlier heads.

Saito's paper on how these hybrids are fabricated was delivered at the International Microelectronics Conference held in Tokyo in late May. It attracted attention because his firm appears to be the first in the world to use multiple-layered thin film between thick-film layers that are fired after the thin film.

The high-density hybrids use conductive epoxy die bonding and ultrasonic thermal wire bonding along with conventional chips. Though the chips cannot be pretested, Toshiba engineers say that 60% of the circuits work as initially fabricated and essentially all the remainder after one repair cycle.

Films on films. Each layer of the 2-mil-wide conductors is formed by evaporating multiple thin metal films over the ceramic substrate surface and then defining the conductor pattern by photolithography. The use of multiple films ensures good conductivity and adhesion to the substrate and survival of the firing of the dielectric thick film below and above.

Vias between the metal layers are 4 mils square, to make sure they overlap both lines. They are formed after deposition but before firing of the overlying thick-film dielectric. The dielectric is coated first with a photoresist, then with photosensitive film. Via holes are etched through all this, and thick-film conductive paste forced into them and trimmed off with a squeegee. The film is lifted off, removing any excess conductive paste, and the upper surface of the via conductors shaved level with the dielectric. The thick-film dielectrics and via conductors are then fired, at which time the photoresist is also -Charles Cohen burned off.



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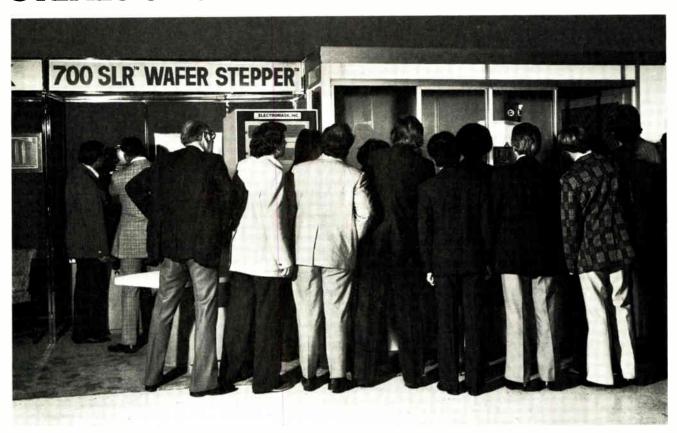
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Circle 83 on reader service card

## AUTOMATIC WAFER ALIGNMENT STEALS SHOW AT SEMICON WEST



SAN MATEO, CA.—Out of the 481 exhibitors who displayed their equipment in 733 booths at the recent SEMICON WEST convention—none drew larger more interested crowds than Electromask. Why? Because, of the four exhibitors who were displaying systems for printing circuits directly on wafers, only the Electromask Model 700SLR Wafer Stepper™ was actually exposing wafers during the show under the most adverse conditions. And this incredible machine was doing it all automatically with only the human attendance of the curious visitors.

Just exactly what was going on here in booth 967? Very simply—the Electromask 700SLR was doing its thing...and doing it very well. It not only demonstrated fully automatic reticle loading, alignment, and masking, as well as fully automatic wafer loading, prealignment, leveling, and unloading—but it also clearly demonstrated the superiority of its system for fully automatic wafer-to-reticle alignment.

In the demonstration at SEMICON, the automatic alignment of the first die was absolutely perfect, and so was the 2nd, the 3rd, the 4th, the 5th, the 6th, etc., etc., etc. Never did the machine exceed its registration specifications. So much for one wafer, but the 700SLR was designed for continuous production, and so it continued through the next wafer, and the next, and the next ... continuing its fully automatic performance throughout the three days of the show.



In a comment to a customer, Ralph Miller, Electromask president, said: "If that's what the Electromask 700SLR Wafer Stepper can do in the middle of a trade show, just think what it could do for you under your control in your own production shop."

Continuing his comment, Mr. Miller noted: "This SEMICON WEST

show includes scores of other advanced equipment for semiconductor manufacturing but probably no other piece of equipment holds a more urgent claim on the immediate future of semiconductor production than does the Wafer Stepper."

Several hundred visitors to the Electromask booth apparently agreed with the president as they placed requests for descriptive literature on the system. Literature packages fully describing the system are now available. For more information, or to arrange for a product demonstration, contact: Electromask, Inc., a subsidiary of TRE Corporation, 6109 DeSoto Avenue, Woodland Hills, California 91367. Phone: (213) 884-5050, Telex 67-7143.



### Personal computer: Japan's next plum?

Some predict that the Japanese will have 30% of U. S. sales in two years, though only Hitachi is at present committed to the market

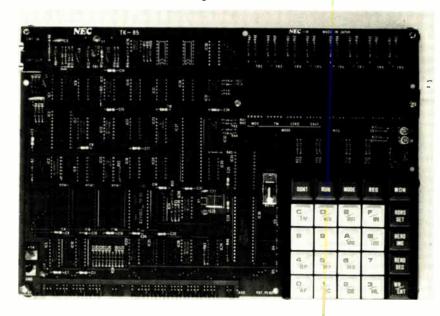
by Charles Cohen, Tokyo bureau manager

Do Japanese manufacturers agree with the prediction of some of their American rivals that in the next two years they will capture 30% of the U.S. market for personal computers? Most of the Japanese, wary of creating the type of waves generated by their auto and television successes, will not say. But Jun Maruyama, manager of the microcomputer instruments project at Hitachi Ltd.'s Consumer Electronics division, is not reticent: he agrees. And on the American side, some observers even see that share reaching as much as 50% [Electronics. June 19, p. 48].

Part of the reason for the reticence of all save Hitachi is that the firm appears to be the only Japanese producer to have formulated its U.S. marketing strategy. The two leading sellers of personal computers in Japan, Nippon Electric Co. and Sharp Corp., say they have not yet made a decision.

Some Americans in the business profess to be unruffled by the prospect of a Japanese invasion of their domestic market. They see the major Japanese influence as a positive one: expansion of the market with the introduction of hand-held computers. Sy Lipper, president of New York's APF Electronics Inc., believes that the Japanese will find software development an obstacle.

But at Ohio Scientific Inc. in Aurora, Ohio, president Charity Cheiky considers the Japanese formidable foes but also likely allies in the competition with other computer makers. She says her \$30 million company is negotiating a technology exchange "with one of the foremost Japanese companies." Ohio Scien-



**Learning to microcompute.** This training microcomputer from Nippon Electric Co., the TK-85, is on one board and sells for \$200. The market is mostly industry and schools.

tific will contribute final product designs in exchange for very largescale integrated logic and memory chips.

The under-\$1,000 hand-held model introduced at the Summer Consumer Electronics Show by Matsushita Electric Industrial Co. [Electronics, June 19, p. 46] is viewed as a stepping-stone as well as a system in its own right. The way Sakae Fukushima, general manager of the handheld computer department at Matsushita's Radio division, sees it, persons who start with a hand-held machine will go on to buy a desktop unit, and those with a desktop computer may buy a hand-held computer for use when traveling. Sharp will start selling two models, available in Japan since March, in the U.S. this

In the personal or home computer field, Hitachi's Maruyama has great expectations for the company's socalled Basic Master Level 3 MB-6809, which features Microsoft Basic in read-only memory. It is built around the firm's licensed 6809 chip. Maruyama characterizes the Level 3 machine as a super-Apple because, he says, its capabilities exceed those of the Apple II. Furthermore, he claims that it is the first consumeroriented computer available in Japan with internal space for up to six optional input/output boards. Another feature not duplicated by other manufacturers is a 14-inch color monitor with a high-resolution color tube that can display 2,000 characters as 25 lines of 80 characters each.

The Level 3 comes with 24 kilo-

#### Probing the news



**Looking Sharp.** PC-3000 system from Sharp is part of line that includes both hobby computers and models for small businesses.

bytes of read-only memory, including a monitor and extended Basic, and 32 kilobytes of dynamic random-access memory. RAM capacity can be increased to 60 kilobytes, which automatically disconnects all ROM except 4 kilobytes of monitor firmware and allows the user to supply his own language or work in machine language. The display provides six colors plus white. An interlaced display with 640 dots horizontally by 400 vertically provides fine detail in both upper- and lower-case letters.

For graphics, a noninterlaced 640-by-200-dot format is used. Floppy-disk drives and printers will enable the system to operate as a word processor. Maruyama thinks that a reasonable price for the basic machine in the U. S. will be about \$1,500 and that the high-resolution monitor should go for about \$900.

According to plan. Kazuya Watanabe, general manager of the Microcomputer Application division at Nippon Electric, says that his company is now selling about 3,000 to 4,000 units of its PC-8000 series computers a month. That puts him right on budget for domestic sales because he expects to sell 30,000 systems during the current fiscal year that started April 1. The average selling price for each system is \$1.800, including \$760 for the PC-8001 computer and at least another \$220 for a black and white monitor. Most users also want a cassette recorder or disk for storage. Although the system was demonstrated at the recent National Computer Conference, Nippon Electric has not yet made any decision about exports.

The PC-8001 is built around the company's 4-megahertz PD780C, which is compatible with the Z80A. It was chosen for ease in using dynamic memories and features 24 kilobytes of ROM that stores both the monitor firmware and N-Basic, NEC's version of Microsoft's disk Basic. There are 16 kilobytes of RAM, and both ROM and RAM can be increased to a maximum of 32 kilobytes each. Included are a 600bit/second tape interface, a parallel printer (Centronics) interface, and a TTI-level serial interface that will work at selected data-transfer rates. An external expansion unit is available for RS-232 interfaces, additional ROM and RAM, and extra I/O

Nippon Electric also has a oneboard training microcomputer that it sells for \$200. The company sold its more expensive predecessor, which was a kit, mostly to individuals when it first came out, but the market has changed to mainly industry, schools, and other institutions.

Two series. Sharp Corp. has two divisions each making a series of Z80-based microprocessors. One, which has been on the market for some time, is for hobbyists. The newer series is for business applications and is sold through business machine dealers.

Sharp's hobby computers, the MZ-80K2 at \$900 and the MZ-80C at \$1,200, differ mainly in the more expensive model's having a standard typewriter keyboard (rather than the less expensive model's calculatorlike keyboard, in the Pet tradition) and 48 rather than 32 kilobytes of RAM. In both, ROM has been kept to the practical minimum of 4 kilobytes and all languages are loaded from tape before use. This approach has kept the price low-in fact, the computers include both a built-in cathode-ray-tube monitor and a built-in cassette recorder, whereas Nippon Electric's similarly priced unit has neither. It probably also kept the price of fixes low because errors in the early version of Basic could be corrected by cassette substitution. To make up for the need to load



**Out of pocket.** Sharp's PC-1210 pocket computer is shown linked to cassette player via its CE-121 cassette interface device.

programs from cassette, the relatively high data-transfer rate of 1,200 b/s is used. Sharp's nonbusiness Basic uses floating-point calculation for science-oriented applications.

Expandable. Sharp's business-oriented personal computer, which includes the main processor and a separate 10-inch CRT monitor on an adjustable tube frame for \$1,125, has its business Basic alongside the display in a total of 24 kilobytes of ROM. An additional 8 kilobytes can be used to expand the language. The RAM space is initially 16 kilobytes, but up to 32 kilobytes can be installed. The business Basic used in this machine does binary-coded decimal computation, which is more suited to business applications than floating-point calculation.

Among other manufacturers, Toshiba Corp. sells a one-board uncased machine with a full keyboard and Basic capabilities. Though it is not a major factor in Japan, Toshiba could become a factor in the export market. However, it says it has no plans at present for that segment. Also, Sanyo Electric Co. may get into the business in the future. It sells nothing of this sort in Japan now, although it has displayed prototypes at shows. And Casio Computer Co.-the calculator company-has shown a prototype computer but has not billed it as a sample of a future product. The firm could also obviously jump into the hand-held computer market if it desired.



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M2115AL	1Kx1	75	75
M2125A	1Kx1	55	125
M2125AL	1Kx1	75	75
M2114AL-3	1Kx4	150	50
M2114AL-4	1Kx4	200	50
M2114A-4	1Kx4	200	70
M2114A-5	1Kx4	250	70
M2148H	1Kx4	70	180/30
M2147H-3	4Kx1	55	180/30
M2147H	4Kx1	70	180/30
Dynamic <sup>2</sup>			
M2118-4	16Kx1	120	25/2
M2118-7	16Kx1	150	23/2

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#### Communications

### Decade dawns brightly for fiber optics

1970s saw experimental work in optical communications, but commercial market could grow to \$1 billion in the 1980s

by Bruce LeBoss, San Francisco regional bureau manager

The just completed International Conference on Communications in Seattle, Wash., did not plan to commemorate the centennial of the birth of light-wave communications—Alexander Graham Bell's so-called photo phone. In fact, the major technology coverage was reserved for digital communications. Nevertheless, the ICC might have wound up marking the start of the decade in which communication by light finally comes to life commercially.

To date, most fiber-optic systems installations have been for prototype and field-evaluation applications, with a few operational systems installed for small military applications. The total market is only about \$50 million. But forecasts at the Seattle meeting were that it may grow tenfold by 1985 and reach \$1 billion by the end of the decade.

Through the first half of this year, "business has been super, better than anticipated," notes James A. Cole, sales manager at Siecor Optical Cables Inc., Horseheads, N. Y. What's more, he points out, "the systems houses are talking about the second half of this year being better

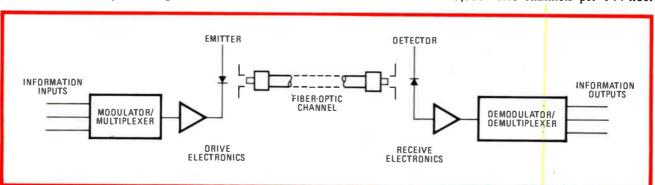
yet, and they're very optimistic about the first half of 1981."

Perhaps the single most important factor responsible for the buoyancy in the fiber-optic business, Cole notes, was the Bell System's announcement of its decision to install a 1,000-kilometer link between Washington, D. C., and Boston—the so-called Northeast Corridor. "As a result of that decision, a lot of telephone companies are beginning to believe that fiber optics makes sense for them. It tells them that Bell is committed to the technology and that it is not to be just a test installation but a fully operational system," he says.

Hank Maas, marketing manager for telephone transmission products at Harris Corp., Melbourne, Fla., concurs. He says, "Two years ago everyone wanted to experiment with fiber optics, and last year was a lull period while they evaluated the technology. Now, it is an accepted thing. The Northeast Corridor decision reinforced Bell's position and endorsed fiber-optic technology. Now the other telcos are getting ready to commit."

The fiber-optic system that Bell will install in the Northeast Corridor is its new FT3 Lightwave Digital Transmission System, built by Western Electric. The first standard FT3 system is slated to be placed in service by Southern Bell Telephone Co. this December in Atlanta. The link will carry both business and residential traffic and is the first of many standard systems scheduled for installation by various Bell operating companies over the next four years. The light-guide cable route of the Southern Bell system will include three telephone switching offices and one repeater point, with the maximum distance between offices about 5 miles.

According to a Western Electric spokesman, the FT3 has a transmission rate of 44.7 megabits per second, "equivalent to sending 5,000 pages of information at 350 words per minute in 1 second." The transmission medium is graded-index glass fibers (12 to 144 fibers per light-guide cable), and the system's capacity is 672 two-way voice channels per pair of fibers, "or more than 40,000 voice channels per 144-fiber



How it's done. Fiber-optic communications avoids all of the electromagnetic interference to which wire systems are susceptible because of the dielectric nature of optical fibers. Data is converted into modified infrared light, transmitted, then reconverted into electronic signals.

#### Probing the news

cable," the spokesman notes. Repeater spacing is 4 miles, he adds, compared with typically every mile for standard copper cable.

A prestandard FT3 system was installed last October by Southern New England Telephone Co. over a 3.9-mile stretch between Trumbull and Monroe, Conn. Having an initial capacity of 192 voice circuits, it has been serving residential customers since mid-November, and so far, according to phone company associate staff manager Deane B. Olsen, there have been "no service interruptions, no equipment failures, and no switch to the automatic protection arrangement."

Bell operating companies are by no means the only ones anteing up for operational fiber-optic systems. Alberta Government Telephones in Canada has awarded Harris a \$7 million contract-perhaps the largest yet awarded for an operational system of this kind—to design, build, and install a high-capacity system that will transmit telephone messages through a 32-mile cable containing 12 glass fibers. To begin service tests next month, it operates at the T4 rate of 4,032 phone conversations per fiber, which is six times the rate of Bell's FT3 system, Maas points out.

Lots of talk. At the T4 rate, the Harris system will transmit 274 million bits of digital information per second, "the highest rate in use today by the North American telephone industry," Maas claims. What's more, he continues, when the system in Alberta reaches its ultimate capacity, it will be able to handle over 20,000 telephone calls simultaneously.

NEC America Inc.'s Radio and Transmission division in Dallas is also installing some noteworthy fiberoptic systems. One is for Central Telephone Co. of Texas and covers an 8.6-km (5.2-mile) link between Humble and South Humble, Texas. The system, going through cable tests this month and scheduled to become operational in September, is the first to transmit at 90 Mb/s, as well as boasting the longest nonrepeater length, claims Alan B. Mann,

#### Fiber and cable pick up speed

Contrary to the situation that existed several years ago, when electronic technology was waiting for fiber and cable technologies to develop, notes James A. Cole, sales manager at Siecor Optical Cables Inc., Horseheads, N. Y., the more recent fiber and cable advances are outpacing the electronics needed for practical, viable commercial systems. "The fiber is here and the cable can be produced. It's now simply a matter of waiting for the electronics, waiting for the systems houses to come up with a broad offering of the necessary sources, detectors, and other equipment."

Indeed, many of the systems houses are busy developing such equipment. Harris Corp. in Melbourne, Fla., for example, has in its laboratory both a 1,300-nanometer system and a wavelength-division-multiplexing system that are expected to surface commercially in 1982. Also in development is a T3C system featuring a 90-megabit/second transmission rate and a capacity of 1,344 channels, to be introduced next year.

The development of ultralow-loss optical fibers operating in the wavelength range of 1.2 to 1.6 micrometers, together with the realization of suitable, high-power high-speed light-emitting-diode sources, "will permit the fabrication of long-haul high-data-rate links using LEDs instead of lasers, which have traditionally been viewed as essential sources for such systems," states Andrew C. Carter, research engineer at Plessey Co.'s Allen Clark Research Centre in Caswell, Northants., England. Plessey has developed a high-radiance LED using gallium indium arsenide phosphide and indium phosphide layers [*Electronics*, May 24, 1979, p. 73]. This system allows lattice-matched double heterostructures to be grown over the wavelength range of 0.95 to 1.7 μm, he adds, "covering most wavelengths of current interest."

Carter notes that GalnAs detectors, combined with GaAs field-effect transistors, "make very effective, high-performance front ends" for optical communications systems. Within the next few months, Plessey plans to release commercially such an integrated unit. Carter believes that the long-wavelength high-speed LEDs are "suitable for systems up to 280 Mb/s, maybe even higher." In fact, transmitter and receiver equipment for 800-Mb/s single-mode optical-fiber transmission at 1.3  $\mu$ m have been built and tested by researchers at Fujitsu Laboratories Ltd. in Kawasaki, Japan.

Major implementations of fiber-optic communications systems are under way in several foreign countries, among them West Germany, Italy, and the UK. "Optical-fiber systems have undoubtedly arrived in the United Kingdom and are being used widely," states John E. Midwinter, program manager at the British Post Office's research center in Ipswich. The user reaction, he adds, "has been enthusiastic, recognizing the great advantages in performance offered." However, though the first installations offer negligible savings over conventional systems, he notes that once the development costs have been written off, substantial cost reductions will be possible.

-B. LeB.

senior systems engineer. Mann neither confirms nor denies reports that NEC America also has received an order from Mountain Bell Telephone Co. in Denver for a 32-km (19-mile) military defense system that will feature the first domestic use of manhole repeaters.

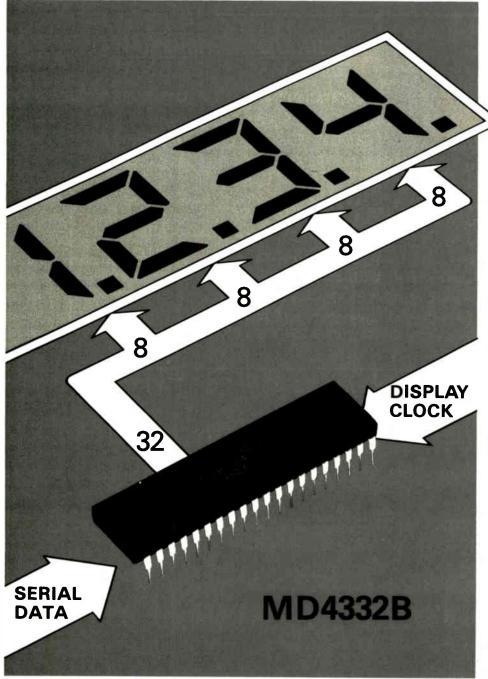
Perhaps the most significant of NEC America's recent orders, and one indicative of changing lightwave communications technology, was placed by Continental Telephone Co. of Virginia in Vienna, Va. The system makes use of a recently developed fiber from Corning Glass Works' telecommunications products department in Corning, N. Y., and is expected to use a novel multi-

plexing scheme for increased capacity.

Best of both. The new Corning fiber, called DWF (for double-window fiber), has two different attenuation characteristics that allow for operation at wavelengths of 850 to 1.300 nanometers [Electronics, April 10, p. 176]. "The fiber enables telcos to make a decision now, but upgrade their systems in the future," says William L. Babcock, a Corning sales manager. Because "change is painful to many," he says, "Corning developed DWF so that users could reap the economic benefits that fiber optics provide today and still get the performance or capacity benefits yet to come."

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#### Memories

### Microcomputer memories get smart

8-bit-wide dynamic RAMs and EE-PROMs will be about as easy to use as static random-access and programmable devices

by John G. Posa, Solid State Editor

It has been hard for the microcomputer system designer to exploit the low cost per bit of dynamic random-access memories and the in-circuit alteration possible with electrically erasable programmable read-only memories. But these devices are literally wising up: emerging from the semiconductor companies are both intelligent dynamic RAMs—pseudostatics, as they are generally called—and EE-PROMs that will be almost as easy to use as fully static devices.

Dynamic RAMs and currently available EE-PROMs require considerable support electronics to be useful in microcomputer systems. Dynamic RAMs need to be refreshed, so

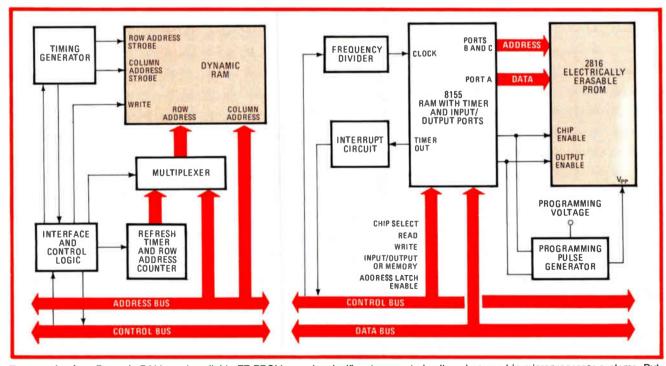
if the design cannot guarantee a minimum number of memory accesses within the refresh period, a row address counter, multiplexer, and miscellaneous control logic must be added to the system (see figure). Even the pseudostatic RAMs now on the market need some logical glue to make them work.

Because they take so long to program, today's EE-PROMs need external latches to hold addresses and data stable. They also require a high-voltage (17 to 25 volts) programming-pulse generator and a circuit to tell the central processing unit when read and write operations have been completed. The block diagram on the right in the figure shows

how Intel Corp.'s 2-K-by-8-bit 2816 EE-PROM might be connected to a system bus. Other EE-PROMs would require a RAM buffer because they lack the 2816's byte-erase feature.

The intelligent pseudostatics and EE-PROMs now in design will simply incorporate the peripheral circuitry on chip needed for smooth interconnection and operation. Byte erasure is one of the first such enhancements for EE-PROMs, and many if not all of the firms promising electrically erasable devices will follow Intel's lead.

Address and data latching will be the next function to be integrated on the memory chip, says Larry Jordan, strategic marketing and applications manager for Intel's Special Products



**Too much glue.** Dynamic RAMs and available EE-PROMs require significant support circuitry when used in microprocessor systems. But future 8-bit-wide dynamic RAMs—pseudostatic RAMs, as they are called—and EE-PROMs will be smart and easy to use.

division in Santa Clara, Calif. Beyond that, he says, EE-PROMS will be able automatically to time out their own erasing and writing operations and to alert the microprocessor through a ready signal when such operations have been completed.

"If you've got all of this integrated on chip, you will simply be able to tell it [the EE-PROM] that you want to do a write operation," says Jordan. "It then accepts the data, performs a false write automatically to clear the intended location, and does a regular write operation."

Challenge ahead. The internal timing of erase and write operations will be one of the most challenging features to be bestowed on an EE-PROM. There are two ways to accomplish this timing. In one, called the worstcase method, the chip waits just longer than the longest time within which the operations are guaranteed to finish. This worst-case period is found by testing numerous devices and adding an allowance to balance processing variations.

Better than the worst-case approach, an alternative arrangement is to design the EE-PROM so that it can accurately and continuously monitor the erase and write operations at the cell level, signaling the CPU precisely when they have been completed. "The timing network can be set up so that whenever an individual cell is programmed, the ready line says 'I'm done,' "comments Jordan. "Then the device doesn't run on maximums anymore," he adds, "it runs on typicals."

So far, only Intel and Motorola Inc.'s Semiconductor Group in Phoenix have intimated that they will develop smart EE-PROMs. But it seems that the widespread acceptance of these devices will at least partially hinge on the inclusion of the ease-of-use features. This can also be said of pseudostatic RAMs. which have not really been economically practical in the past because bit densities have not been high enough to overshadow the added circuitry.

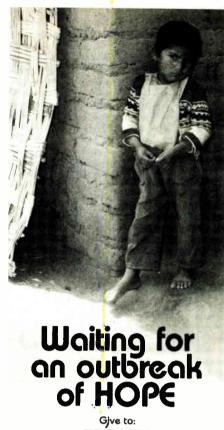
This helps to explain why Intel. Motorola, National, Texas Instruments, Toshiba, and others have waited for the 64-K level to bring out a pseudostatic RAM. Each will offer an 8-K-by-8-bit pseudostatic memory, and each company will have its

own scheme for making the refreshing appear invisible to the user. Mostek Corp. of Carrollton, Texas, already offers a pseudostatic, the 4816. So does Zilog Inc. in Cupertino, Calif.: the Z6132. Both will go on to produce 64-K devices; Zilog may do so as an alternate source to National Semiconductor.

For a pseudostatic memory to recognize when it can best hide its internal refresh operations, it helps to know which microprocessor is in use. Motorola's device, due next year, will be able to ascertain which processor it is connected to "by looking at the edges of the address, data. and control signals," states Al Bormann, design manager for MOS memories at Motorola's 1C division in Austin, Texas. From the timing of those signals, "the memory will be able to distinguish among an 8080, 8085, 8086, 6800, 6805, 6809, 68000, and Z8000."

Static look. Motorola's refresh pin will be connected to different signals from different processors, so "refreshing will occur at different times. depending upon the processor," Bormann says. In this way, the RAM "will look totally static." Motorola has already designed a circuit called Motel-for Motorola and Intelthat can tell the difference between a 6800 and an 8080.

Motorola cannot guarantee that its pseudostatic will work with its 6801 single-chip microcomputer, because when the 6801 is halted, there is no signal from the processor to tell the memory when to refresh. Ti agrees that this is one of the obstacles that it had to overcome for its pseudostatic device. "If the microprocessor goes into a hold state, the memory must go asynchronous and control its own refresh," says Peyton M. Cole, strategic marketing manager at TI's MOS memory division in Houston, Texas. He adds that "it would be nice if the microprocessor could supply a synchronization signal." A complaint about Zilog's device is that it refreshes on every cycle, consuming power. "Through the refresh pin, you should be able to configure the part to look just like a dynamic RAM," says TI's Cole. "If the memory is being accessed enough, it does not have to be refreshed separately," he explains.



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#### Office systems

### Tailor terminals to people, makers told

Word-processor manufacturers warned that they ignore strained eyes, frazzled nerves, and aching backs at their peril

Unless designers of automated office equipment start mixing psychology with their electronics, they may increase users' problems instead of their productivity—and ultimately lose their business.

Customers today are demanding ease of use, ease of upgrading, and ease of training, judging from the comments at Syntopican, the eighth annual convention of the International Word Processing Association, held last month in Minneapolis.

The ease-of-use issue was pushed into the spotlight by a report from the National Institute for Occupational Safety and Health, released just before the convention. The report stated that cathode-ray-tube terminals common to word- and data-processing equipment can cause problems ranging from eyestrain and blurred vision to unexpected complaints such as sore shoulders, anxiety, and depression.

The causes may be electronic, like the flicker rate or color of the CRT, or may be traced to the system's mechanical design. Here, features such as detachable keyboards, tilting and rotating displays, and nonglare screens were found to reduce the operators' complaints significantly.

Now that such cause-and-effect relationships have been established, attention to human engineering—or ergonomics, as that branch of psychology is called—will become more critical in the future of the industry [Electronics, March 27, p. 102]. For example, one life insurance company recently discontinued use of a particular word-processing system because it caused eyestrain. A key point was that the old units had a green CRT display. Newer displays at the com-

pany have either black and white or amber displays.

To reduce the problem with glare, the Duke Power and Light Co., Durham, N. C., relocated lights in the work area when word-processing gear was installed. Now it is sound-proofing the equipment.

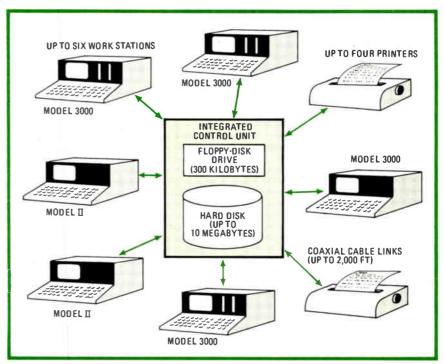
Vendors are responding to buyers' needs in these areas. The Industrial Products division of Hazeltine Corp., Greenlawn, N. Y., was demonstrating for the first time its recently developed Opus 80, a shared-resource system [Electronics, April 24, p. 44] that incorporates most of the user-friendly features in evidence at Syntopican.

CPT Corp., showed a terminal

whose screen is white with a bluish tint and dark characters so that the operator can avoid the eye fatigue that might result from constant refocusing between high-contrast screen and paper, the Minneapolis company says. Dictaphone Corp., Rye, N. Y., has a tilting screen with a nylon coating to reduce glare.

Nor is software being neglected. Many tedious or repetitive tasks, such as footnote tie-ins, spacing and repagination, tabulation or creation of contents, and indexing, are now done automatically by the software in many systems.

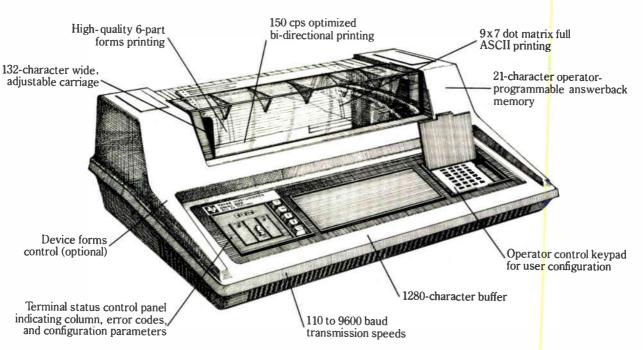
But all the current attention to human engineering in the United States pales in comparison with



**Sharing resources.** A typical office system featuring shared resources ties stand-alone units to a central controller containing hard-disk memory for archival storage.

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#### Probing the news

European efforts, particularly in West Germany. Many companies noted that ergonomic features are becoming standard requirements in European markets, and most feel it is only a matter of time before American products follow suit. Still, there is some foot-dragging about specific European requirements. Typically, one vendor is adopting a wait-and-see attitude about reports of health problems. Another markets two models of the same unit-one that will satisfy the more stringent European requirements, the other with fewer user-friendly features for the U.S. market.

Room to grow. Answering another user demand—for upgradability—is a new series of shared-resource systems. But unlike the traditional versions of these systems, which share the entire computer as well as the various peripherals among several work stations, the new units let existing stand-alone word-processing units expand. The stand-alone stations, each already with a microcomputer and floppy-disk storage, tie over communications links to a controller that houses larger hard disks for archival storage and for faster printers.

The Office Automation Systems developed by NBI Inc., Boulder, Colo., enable the buyer to go from the firm's system 3000 independent work station to any combination of stand-alones, peripheral systems, and printers driven by the eight-port integrated control unit of the new system 8, or the 64-port system 64.

These join a similar system called Netword from Vydec Inc., Florham Park, N. J., a subsidiary of Exxon Information Systems [Electronics, July 3, p. 95]. The Netword controllers communicate with the Vydec 1400, 1800, 2000, and 4000 standalone work stations as well as with the Qyx intelligent typewriter.

Similar announcements were made by CPT, which has developed the 8000 W/P system with expanded storage, and by Micom Data Systems Inc. of Montreal for its new 2001 word-processing system.

Reporting for this story was provided by Pamela White, McGraw-Hill World News, Minneapolis.

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#### **Probing the news**

Software

## Microcomputers adding data-base management

Sales of DBMS packages for small-business systems expected to rise 177% a year through 1983

by Martin Marshall, West Coast Computers & Instruments Editor

The exploding sales of microcomputers in the small-business market have triggered a parallel need for data-base management systems, or DBMSs, as software modules. In the words of a report from Creative Strategies Inc., "By 1983, the average vendor will have to offer a DBMS package if it expects to remain com-

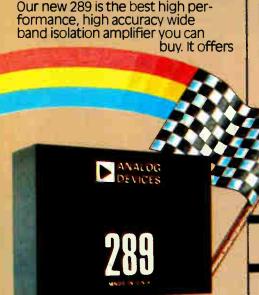
petitive." Thus, the San Jose, Calif., market research firm projects a dramatic 177% compound annual growth rate through 1983 for shipment of these packages to the small-business-computer market.

In response to the growing need, various companies are offering such packages as Microseed, MDBS, and

Info 80, with others such as Harvest to follow soon. The most recent of these offerings is the Info 80, which will be released at the end of this month by Data Train Inc. of Grants Pass, Ore. Initially it will be marketed for Radio Shack's TRS-80 model 2, but since it is written in Microsoft Basic to be run on a CP/M operating system, it can be used with other computers running under CP/M. Info 80 allows the user to feed in data as characters, binary values, logical variables, double-precision values, or special calendar variables. It also can write reports by taking information from as many as seven files at one time. The user may derive data based upon several key parameters used together or may use a unique key.

Data Train has developed its own data-base language, text editor, and a method of processing for Info 80 that allows it to perform partial batch operations, even on systems based on minisloppy disks. The pro-

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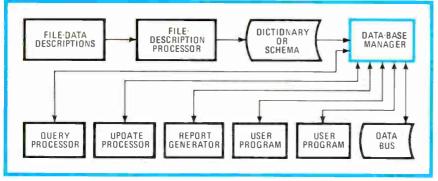
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For further technical information, contact James Conant, Applications Engineer, Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062. Telephone 617/329-4700, Ext. 1304.



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Angles. Typical management system provides many ways of viewing same data base.

gram is distributed, however, on single-density 8-inch floppy diskettes. A key feature of the package is its price: \$99 for a license for the database manager program, with options for one of three data bases at \$99. \$299, or \$499.

Representing the next step up the ladder are two Codasyl-compatible network packages, Microseed and MDBS. Microseed, developed by International Data Base Systems Inc. of Philadelphia, and marketed by

Microsoft Inc. of Bellevue, Wash., was introduced in January at a single-copy end-user price of \$900. Following the Codasyl format, it allows the user to establish both records, which contain the actual data, and sets, which contain the interrelationships of the data.

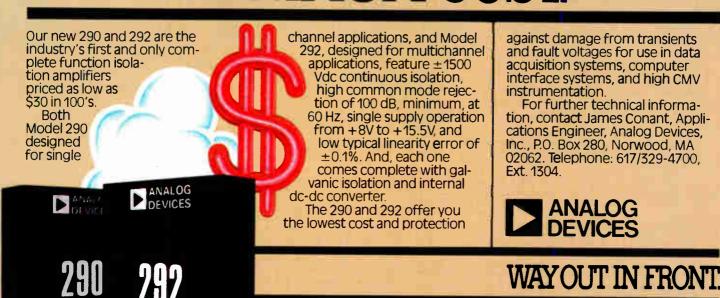
Since it is a network system, Microseed also has password security designed into its schema definitions. The program currently uses 64 kilobytes of the user's random-access

memory, but in mid-August it will have a load-to-disk feature that will alleviate the strain on the user's main memory. The program is written in Fortran and can be used on systems running under CP/M.

Also coming for 16-bit systems is Harvest, a high-level interactive query language and report writer that can be used with Microseed. Due next January, it requires 60 kilobytes of memory and allows the user to make up search criteria for pursuing the data base.

Running with somewhat fewer features than Microseed but much more compact coding is MDBS, a Codasyl-compatible program from Micro Data Base Systems Inc. of Lafayette, Ind. "We were able to get it down to 18 kilobytes by writing it in Z80 assembly language," says president Andrew Winston. The program, whose U. S. price will increase to \$900 from \$750 on Aug. 1, can be run with CP/M, North Star-DOS, Apple-DOS, and TRS-DOS.

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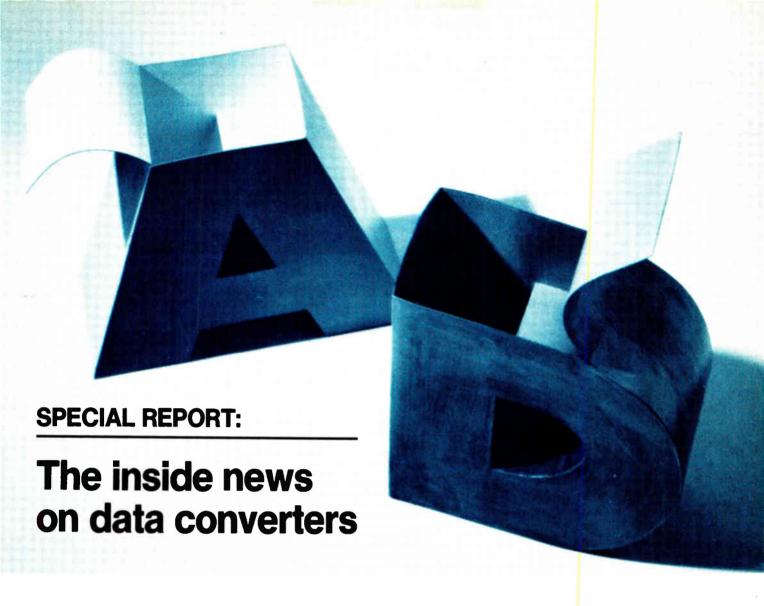
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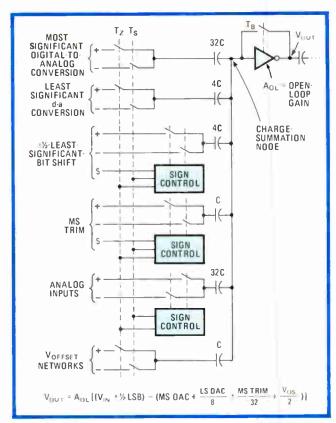
Progress in monolithic technology is pepping up the performance of all types of data converters and putting entire data-acquisition systems on a chip

by Roger Allan, Components Editor

☐ Great strides are being made in data converters, where the emphasis continues to be on upward system integration, higher speeds, and better accuracies. Monolithic 12-bit digital-to-analog and 10-bit analog-to-digital converters are now available. These same integrated circuits, while replacing some hybrid converters at the low end of 8 bits, are being eagerly gobbled up by the hybrid manufacturers for ever more accurate, stable, and high-speed products.

But despite all this activity in monolithic and hybrid d-a and a-d converters, modular data converters employing monolithic, hybrid, and discrete components continue to achieve the highest performance levels. Even the most sophisticated hybrid designs cannot offer, for example, true 12-bit a-d conversion over a converter's entire operating-temperature range and operating lifetime—at least not yet. Only modular converters are at present capable of this.

A principal driving force in the growth of d-a and a-d converters is the proliferation of microprocessors and digital signal processing. And though progress is continuous in integrating more converter functions onto the same chip, the going is getting harder as IC manufacturers approach the 12-bit level and beyond. More fundamental limitations like the stability of a converter's resistor-ladder network and the voltage reference are coming into play. As a result, monolithic converter manufacturers are concentrating on improving their present 8- and 10-bit designs by adding more functions and by improving performance. That includes buffering to inter-



**1. Sampled.** This comparator makes it possible for National Semi-conductor to build a C-MOS version of a 12-bit (plus sign) successive-approximation analog-to-digital converter. The capacitors scale the differential voltages and convert them into charges.

face with microprocessor buses, lower power dissipation, single-supply operation, and higher conversion speeds. Many of the formerly external functions, such as references, output amplifiers, clocks, registers, ladder networks, and data latches, are being integrated onto the chip. Still, there are quite a few monolithic converters that are far from self-sufficient.

Single-chip data converters have been coming down steadily in price, to the point where many 8-bit d-a units can be purchased for less than \$5 in single quantities. Even 12-bit monolithic d-a converters can be bought for under \$10 in unit quantities.

#### Systems on the chip

As more functionally complete monolithic data converters evolve, entire single-chip data-acquisition systems are emerging. Single- and multiple-channel data-acquisition ICs typically contain an a-d converter, input multiplexer (for multiple input channels), output buffer, and address latch and decoder. Monolithic 8- and 16-channel data-acquisition ICs are readily available.

Typical is the ADC0808 from Texas Instruments Inc. of Dallas. It is an eight-channel successive-approximation monolithic data-acquisition IC with  $\pm \frac{1}{2}$ -least-significant-bit linearity error, 100-microsecond conversion time, latched address input, and three-state output for easy microprocessor interfacing.

The data-acquisition market is a lucrative one for makers of monolithic converters, who see in it ample opportunity for the volume sales of a-d converters that can support low prices. Many of them see the automotive market as a major one for these ICs. According to one important manufacturer's estimate, the data-acquisition market is a \$40 million one, with a-d converters having over one-half of the market share.

#### The right choice of technology

Most of the earlier monolithic data converters were of the complementary-MOS variety. These integrating-type a-d converters were typically slower in response than successive-approximation units, but were more accurate, used less power, and, most importantly, could be made at low cost, since C-MOS is an inherently low-cost process. And, for portable digital instruments—digital panel meters and voltmeters—C-MOS a-d converters continue to be ideal.

But C-MOS has its drawbacks. For example, C-MOS voltage references are difficult to integrate on chip so that there is a host of multiplying MOS d-a converters for which references have to be supplied externally. Bipolar processing, on the other hand, has made possible higher-speed converters with stable buried-zener and bandgap references and high-gain, low-offset-voltage amplifiers on the chip, overcoming another C-MOS deficiency. Of course, bipolar transistors, which are larger than C-MOS ones, are more expensive and hence unlikely to make it in a big way in data-acquisition applications.

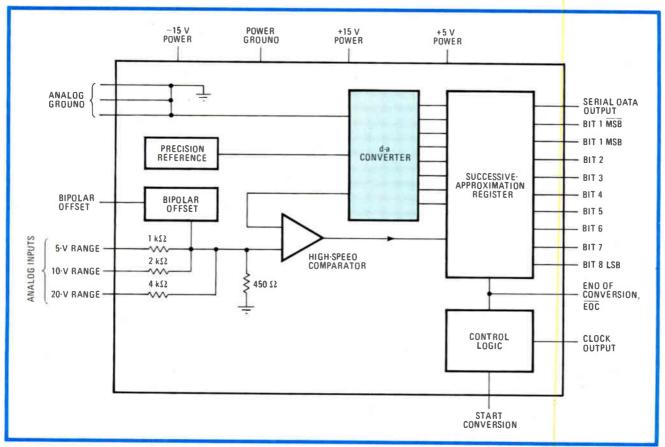
For instance, at this year's International Solid State Circuits Conference evening panel session on "Data Acquisition Peripherals," Jim Solomon, director of linear engineering for National Semiconductor Corp., Santa Clara, Calif., told how his firm started out heavily in bipolar processing for data-acquisition ICs, but has since switched to MOS, which constitutes about 85% of National's processing for data-acquisition ICs. "Large bipolar die sizes result in very poor process yields and higher device costs," he explained.

Still, some of the most important performance advances in data converters have come from bipolar technology. Besides the many 8-bit bipolar d-a converters on the market, 10- and even 12-bit ones have begun to surface. Bipolar 10-bit monolithic d-a converters are, for example, available from Precision Monolithics Inc., Sunnyvale, Calif.; Harris Semiconductor Corp., Melbourne, Fla.; and Signetics Corp., Sunnyvale, Calif. The Signetics NE5020 converter, besides being microprocessor-compatible, is a self-sufficient unit, complete with resistor ladder, voltage reference, output amplifier, data latches, and buffers.

An example of how far monolithic d-a converters have progressed in performance is Precision Monolithics' bipolar DAC-210. Containing both a voltage reference and an output amplifier, the device settles in 1.5  $\mu$ s and is monotonic and linear for 10 bits plus sign (the equivalent of 11 bits) over both commercial (0° to 70°C) and military (-55° to +125°C) temperature ranges.

At the 12-bit level, bipolar d-a chips are available from Precision Monolithics; Teledyne Philbrick, Dedham, Mass.; Harris Semiconductor; Analog Devices, Wilmington, Mass.; and Advanced Micro Devices.

The Advanced Micro Devices model 6012 is signifi-



**2. Fast.** Hybrid technology allows the making of high-speed successive-approximation analog-to-digital converters. An example is this 8-bit ADC-815 from Datel-Intersil with a 600-nanosecond conversion time within  $\pm \frac{1}{2}$  least significant bit. The converter requires no external parts.

cant because it is manufactured by a standard bipolar process. It has a segmented resistor-ladder network whose resistors are diffused boron types that require no trimming. The converter is inherently monotonic and yields 0.01% differential nonlinearity [Electronics, Dec. 6, 1979, p. 152]. The firm feels confident enough in its design approach to predict 14- and 16-bit versions.

#### Other processes flourish

One bipolar process that rises superior to the others' limitations for data-converter designs is integrated injection logic. That's what Analog Devices used for its model AD565 12-bit d-a converter, which should become available shortly. The converter settles in just 150 nanoseconds in the current-output mode. To circumvent damaging the silicon substrate during resistor-ladder laser trimming, Analog Devices employs silicon-chromium thin-film resistors in the resistor-ladder network.

I<sup>2</sup>L processing combines the high-speed advantages of other bipolar technologies with the low power dissipation advantages of C-MOS. It is linear-compatible and makes practical the fabrication of high-speed data latches for d-a converters as well as small successive-approximation registers for a-d converters

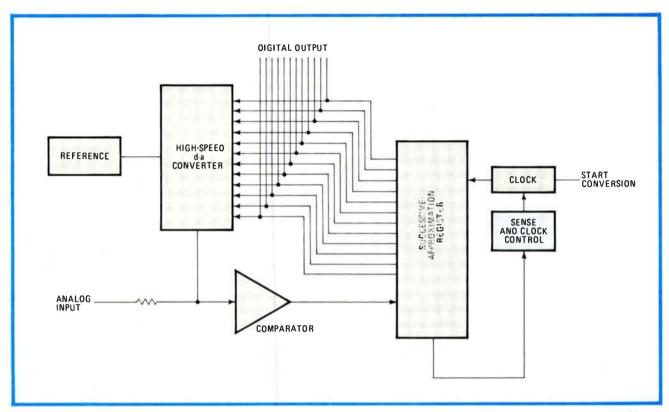
Analog Devices discussed the advantages of 1<sup>2</sup>L processing for data converters at this year's ISSCC, where it introduced an 8-bit d-a unit that also uses siliconchromium thin-film resistors in the ladder network. The AD558 operates from a single power supply of 5 to 15

volts, settles in less than 1  $\mu$ s for a 2.5-V output and under 2.5  $\mu$ s for a 10-V output, and is within  $\pm \frac{1}{4}$ -LSB accuracy. The converter is self-sufficient, containing  $1^2$ L data latches, a merged bandgap reference, pnp current sources, the silicon-chromium resistor-ladder network, an emitter-coupled-logic control gate, and an output amplifier [Electronics, Feb. 28, 1980, p. 125].

A different process that allows optimization of high speed and low power dissipation is dielectric isolation as employed by Harris Corp. The firm uses it to make a monolithic 12-bit d-a converter that features an output settling time of 300 ns for a current-output mode (there is no output amplifier on the chip). The laser-trimmed device features maximum nonlinearity (at 25°C) of  $\pm \frac{1}{4}$  LSB and a gain-temperature coefficient of  $\pm 5$  parts per million per °C maximum. Although this converter lacks an internal reference, Harris is working on supplying one—the model HI-565—that will include a buried-zener 10-v 5-ppm/°C reference. The HI-565 will settle in 200 ns and be within  $\pm \frac{1}{4}$  LSB over its operating-temperature range.

Collector-diffusion isolation is still another process used by Ferranti Electric Inc., Commack, N. Y., to make monolithic d-a and a-d converters. Similar to an I<sup>2</sup>L process, CDI requires fewer masking steps than bipolar or C-MOS processes and allows on-chip diffusion of resistors without laser trimming. It is, however, a low-voltage process, being limited to less than 10 v.

There are other processes under development for data



3. Speeding up. The successive-approximation a-d conversion scheme has been speeded up with sense and clock control circuitry. Used in the 4134 hybrid 1.9-µs 12-bit a-d converter from Teledyne Philbrick, the technique is dubbed progressive approximation.

converters. These include n-channel MOS and bipolar—C-MOS. Texas Instruments Inc. of Dallas points to the bid-FET (bipolar, double-diffused, field-effect-transistor) process it has employed successfully for high-voltage plasma-panel driver ICs as a mixed technology that could be useful for future data converters. With bid-FET processing, the high speed of bipolar technology, the high input impedance of bi-FET technology, the low power dissipation of C-MOS, and the high-voltage capability of DMOS can all be tapped within a monolithic structure.

#### Bipolar a-d converters reach new plateaus

The availability of high-performance bipolar d-a converters has enabled monolithic IC converter manufacturers to use them as a basis for high-performance a-d converters. These have now reached the 10-bit level and should hit the 12-bit level next year.

Analog Devices has the only 10-bit a-d converter chip on the market. Its model AD571 is made with  $1^2L$  technology and contains a successive-approximation register, a reference, a laser-trimmed d-a converter, three-state outputs, and a clock. It has a maximum conversion time of  $40 \mu s$ .

By next year, Advanced Micro Devices hopes to have a 12-bit a-d version of its monolithic 8-bit model 6108. To be introduced shortly, the 6108 has a maximum conversion time of 1  $\mu$ s and maximum nonlinearity and differential nonlinearity of  $\pm \frac{1}{2}$  LSB. The 8-bit accuracy level will apply over the unit's entire operating temperature range, both commercial and military. The microprocessor-compatible converter is complete, containing a successive-approximation register, reference, data

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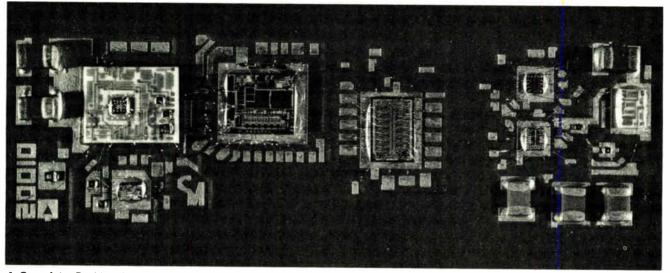
latches, and so on. Available in a 28-pin dual in-line package, the  $\pm 5$ -v unit will be priced at less than \$20 for 100-lot quantities.

The 12-bit version of the 8-bit 6108 a-d converter is a difficult part to manufacture and is pushing the bipolar converter state of the art. Colin Barry, linear IC design manager for Advanced Micro Devices, feels the challenge of using bipolar technology to go to higher resolutions in order to achieve higher accuracy (that is, using 14- and 16-bit resolutions to obtain 12-bit accuracy levels): chip size and hence costs increase as a result, testing a designer's ingenuity. Nevertheless, he feels that the emergence of high-speed microprocessors demands equally fast as well as high-performance a-d and d-a converters, and bipolar technology is compatible with such data-converter requirements.

#### C-MOS converters coming on strong

Several companies now offer monolithic 8- and 10-bit C-MOS d-a converters. Ten-bit devices are available from Analog Devices; National Semiconductor Corp.; Intersil, Cupertino, Calif.; Micro Power Systems Inc., Santa Clara, Calif.; and Motorola Inc., Austin, Texas. All of them except Motorola also offer multiplying 12-bit C-MOS monolithic d-a converters.

Hybrid Systems Corp., Bedford, Mass., a hybrid converter manufacturer, has gone still farther and designed a 14-bit C-MOS d-a converter chip to be manufactured by a monolithic IC maker under a joint development in which Hybrid Systems assisted in the chip's layout. The four-quadrant multiplying IC has a settling time of 1  $\mu$ s (current output), dissipates less than 50 milliwatts, and



**4. Complete.** Rapid and accurate 12-bit a-d conversion will soon become available from this multichip product from Analog Devices. The successive-approximation unit has 4-µs conversion and ±0.012% maximum nonlinearity. No external components are needed.

features stability of 2 ppm/°C. Decoder functions are included on the chip, which will have 14-bit accuracy as well as resolution at room temperature.

To quote Dan Hauer, product general manager for Micro Power Systems: "Circuit designers usually think of their input/output sections last, and as a result leave little room for error margins, thus requiring the use of high-accuracy and very stable a-d and d-a converters. This is why hybrid and modular data converters are needed. Our line of multiplying C-MOS 12-bit d-a converters with accuracy over temperature is an example of what monolithic C-MOS technology is now capable of achieving and which formerly required hybrid and modular converters."

Micro Power Systems was the first to produce a monolithic C-MOS data converter back in 1973. The company also makes bipolar ICs and is investigating mixed bipolar and C-MOS processes.

Speeds are also up in monolithic C-MOS d-a converters. For example, take Motorola's 10-bit MC3510/3410 d-a C-MOS converter. Its conversion time of 250 ns was hardly believable for C-MOS just a few years back. Later this year, Micro Power Systems hopes to introduce a 500-ns 12-bit monolithic C-MOS d-a unit.

As was mentioned earlier, it is not possible to put an accurate voltage reference on a C-MOS converter chip. This is why all available C-MOS d-a converters are multiplying types that require external references. Some also require other external components, such as an output amplifier.

The lack of a reference is not a total disadvantage for C-MOS d-a converters. A multiplying-type d-a converter, for example, can be used with an external reference voltage for ratiometric conversion and for digitally controlled attenuation.

It has long been conventional wisdom within the monolithic data converter industry that the C-MOS process is not useful for the fabrication of high-speed successive-approximation a-d converters. National Semiconductor, in a paper at this year's ISSCC, laid that myth to rest. It unveiled a 12-bit-plus-sign successive-approxi-

mation C-MOS a-d converter chip that should be available later this year. Until the unveiling of National's converter, all monolithic a-d converters available were of the slower integrating types, since the C-MOS comparators used in successive-approximation conversion schemes tend to perform poorly and be slow, not very accurate, and noisy.

#### An accurate C-MOS comparator

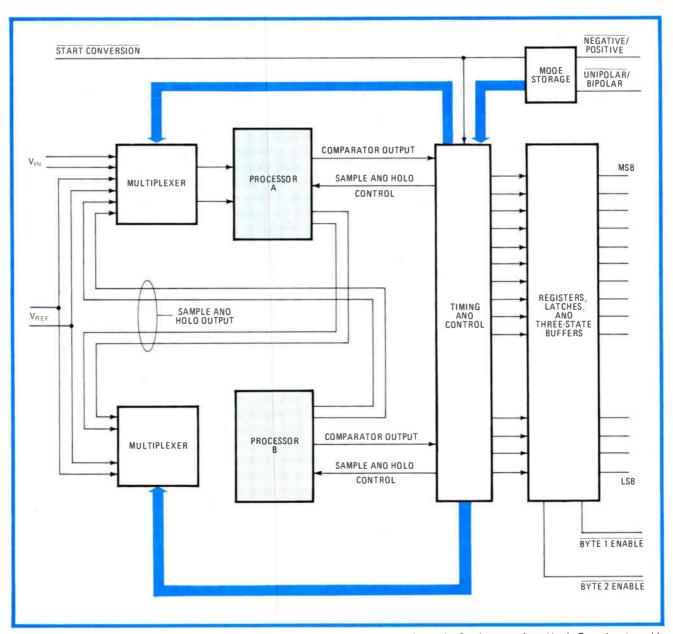
National licked the comparator performance problem by the use of a multiple-input comparator that accepts an arbitrary number of differential input voltages (Fig. 1). As a result, conversion speed is  $50 \mu s$  and yet power dissipation is only 25 mW.

A unique feature of the converter's design is how it achieves its 12-bit linearity—by laser-cutting fuse links within its on-chip programmable read-only memory. The National 12-bit C-MOS a-d converter, like all C-MOS converters, has no voltage reference.

To put things in perspective, National's is not the only monolithic 12-bit C-MOS a-d converter. Intersil also has one. Its model ICL7109 is compatible with microprocessor buses and with universal asynchronous receiver/transmitters, but it is a slower, integrating type, intended for data-acquisition systems. The chip features a conversion time that ranges from 20 to 50 ms.

Integrating-type monolithic C-MOS a-d converters with resolutions and accuracies greater than 12 bits have been readily available for a number of years from several manufacturers, including Intersil, Analog Devices, and TI. An entire generation of low-power-dissipation, handheld digital panel meters and digital voltmeters has been made possible by these 3½- and 4½-digit a-d integrating converters, which are used in their front ends. When compared with successive-approximation a-d converters, however, they are slow, with conversion speeds being milliseconds at best.

NEC Microcomputers Inc. of Lexington, Mass., has a 12-bit C-MOS a-d device that achieves 5-millisecond conversions by combining an integrating technique the company calls simultaneous integration with voltage-to-



5. Two-chip. Hybrid converter makers are using fewer chips for higher accuracies and speeds. Coming soon from Harris Corp. is a two-chip 30-μs 12-bit a-d converter with an advanced microprocessor interface. The quantizing unit is accurate to 12 bits over -55° to + 125°C.

current front-end conversion. The  $\mu PD7002$  is microprocessor-bus-oriented and includes a multiplexer that accommodates four analog inputs.

Despite all the fanfare about monolithic data-converter technology, the market for hybrid data converters continues to show steady growth. These hybrid units are generally complete converters, containing all of the converter elements necessary. Furthermore, they achieve better accuracy and stability levels over time and temperature, as well as faster d-a settling times and a-d conversion speeds.

#### How hybrid converters stay one step ahead

The principal advantage of hybrid converter technology is that it allows the mixing and matching of individual chip functions, regardless of the IC technology, for optimum performance levels. The drawback is that too many

chips in a hybrid circuit create a costly complexity and reduce reliability because of the number of chip interconnections.

Somewhat paradoxically, hybrid converter manufacturers are becoming more involved in the design of the ICs they are using to make their products, as evidenced by the Hybrid Systems 14-bit d-a converter chip mentioned earlier. Hybrid Systems president Wayne Peacock explains that "if hybrid converter makers don't get involved with monolithic IC design, the way monolithic converters are advancing will leave hybrid converter makers holding the bag." Of course, some hybrid converter leaders like Burr-Brown Research Corp., Tucson, Ariz., and Analog Devices have monolithic as well as hybrid capabilities. Others, like Datel-Intersil Inc., Mansfield, Mass., are part of large semiconductor companies. National Semiconductor, on the other hand, a

leading monolithic data-converter manufacturer, is also pushing its hybrid expertise.

One of the most significant hybrid converter developments is an 18-bit d-a converter from Hybrid Systems. On its alumina substrate the DAC-370-18 has two chips—a custom C-MOS switch network and a laser-trimmed thin-film resistor network. It is the first d-a converter in a double-width DIP to offer 16-bit linearity, input latches, and 50-mw power dissipation [Electronics, March 27, 1980, p. 199]. An equally important feature of the DAC-370-18 is its very low price—just \$210 in 100-unit quantities.

Samuel Wilensky, Hybrid Systems' vice president of engineering and one of the company's founders, says modestly that "the design of the custom chip at the heart of the DAC-370-18 is something any good designer should be able to accomplish once sound engineering principles are employed." The company had earlier in the year introduced a two-chip 16-bit d-a converter guaranteed to be 16-bit linear to within  $\pm \frac{1}{2}$  LSB (0.008% of full scale). Settling to within  $\frac{1}{2}$  LSB in 1  $\mu$ s, the 9331-16 surprised many with a price of just \$99 in 100-piece quantities. It also is available in a double-width DIP [Electronics, Jan. 31, 1980, p. 124].

Burr-Brown also has a 16-bit hybrid d-a converter. Its DAC73 has a maximum linearity error of 0.0008% of full scale and has the all converter functions necessary within its DIP. Settling time ranges from 8 to 40  $\mu$ s. A faster-settling version is the 16-bit DAC71 with a settling time range of 1 to 10  $\mu$ s. This one has less linearity though, with a maximum linearity error of  $\pm 0.003\%$  of full scale. It also comes in a DIP.

Also Burr-Brown's is the 16-bit ADC71 hybrid a-d converter, a  $50-\mu s$  device available in two versions: one 14 bits and the other 13 bits accurate.

Micro Networks Corp. of Worcester, Mass., is working on a truly challenging device—a 16-bit d-a converter that is accurate to all 16 bits over the military temperature range of -55° to +125°C. Such a project may, however, take two to three years to complete. The firm has been selling high-performance data converters to the military market for a number of years.

In its MN3348 12-bit hybrid d-a converter [Electronics, March 13, 1980, p. 174], the firm has managed to produce a truly high-performance part in a hermetically sealed 24-pin package. Requiring no user adjustments. the converter is guaranteed to have a maximum total error (including those of gain offset and nonlinearity) of ±0.075% of full-scale over the operating temperature range of  $0^{\circ}$  to  $70^{\circ}$ C. A military version (-55° to +125°C) has combined errors of ±0.1% of full scale over the military temperature range. Linearity for both versions is to within  $\pm 0.024\%$  and  $\pm 0.048\%$  of full scale, respectively. Equally important is the availability of optionally adjustable versions for even higher accuracy levels. The fully monotonic converter has an internal 10-V reference, an output amplifier, a C-MOS switch network, and a laser-trimmed thin-film resistor-ladder network. Maximum power dissipation is 375 mw.

In the works from National Semiconductor is a family of three-chip hybrid d-a converters that are pin-for-pin-compatible with the popular DAC80 d-a converters.

To be introduced by the end of this year, the converters contain voltage references and output amplifiers. Settling time is about 3  $\mu$ s (200 to 300 ns for current output).

Several manufacturers are racing the clock in trying to come up with 12-bit hybrid a-d converters that combine high speed with high performance. Some of these products have already surfaced, and others are likely to hit the market this year.

High speeds have already been attained in hybrid a-d converters at lower accuracies. A good example is the ADC-815 hybrid 8-bit a-d converter from Datel-Intersil with a 600-ns conversion time to  $\pm \frac{1}{2}$  LSB. The successive-approximation a-d converter includes a precision reference, clock, comparators, registers, and a current-output d-a converter (Fig. 2).

### High-speed 12-bit a-d converters coming

In the 12-bit a-d hybrid converter area, Teledyne Philbrick took the successive-approximation technique and modified it to what it calls progressive approximation to achieve still faster conversion speeds. In its model 4134, conversion typically occurs in 1.9  $\mu$ s. Faster conversion times are achieved by the use of a sense-and-clock circuit that speeds up the converter's clock rate for all bits after the third bit (Fig. 3).

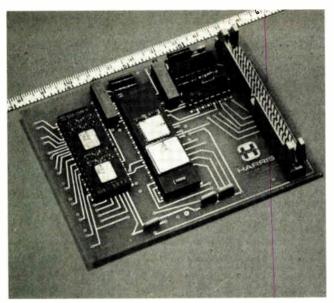
Analog Devices will shortly introduce a 12-bit successive-approximation hybrid a-d converter with 4- $\mu$ s conversion and  $\pm 0.012\%$  maximum nonlinearity. The AD578 is a multichip device (Fig. 4) with all the necessary components in a DIP—a comparator, reference, clock, etc.—to make it a complete converter.

Another firm with plans to introduce a hybrid 12-bit  $4-\mu s$  a-d converter is Harris Corp. The company is getting ready to announce a 30- $\mu s$  hybrid a-d unit accurate to 12 bits over the military temperature range of  $-55^{\circ}$  to  $+125^{\circ}$ C. An important feature of the 5812 is that it uses only two chips. Offering an advanced microprocessor interface and an internal sample-and-hold amplifier, the converter operates by a quantizing scheme that involves the use of two analog processors on the chip (Fig. 5).

### From hybrid to data-acquisition system

Hybrid converter technology has been particularly suitable for integrating upwards into complete single-channel and multichannel data-acquisition systems. Some of these systems are now available in small DIPs. Systems like the 12-bit eight-channel MN7140 from Micro Networks, which operates at a 20-kilohertz rate from a 40-pin double-DIP-width (2.1-by-0.83-by-0.17-inch) package are setting high-performance small-size standards. Another high-performance small-size 12-bit eight-channel (differential) data-acquisition system is the SDM857 from Burr-Brown, which operates at a throughput rate of 18 to 25 kHz. It fits into a ceramic package 2.2 by 1.7 by 0.22 in. Still, the highest-performance hybrid data-acquisition systems require slightly larger modular packages.

This year, Harris Corp. took an unconventional approach in a hybrid data-acquisition system with its two-DIP eight-channel differential 12-bit data-acquisition system [*Electronics*, June 5, 1980, p. 40]. Each DIP



**6. Data acquisition.** Harris Corp. uses leadless chip-carrier integrated circuits in dual in-line packages for a two-DIP eight-channel differential 12-bit data-acquisition system. On the left is the HI-5900 signal processor, on the right the HI-5712 a-d converter.

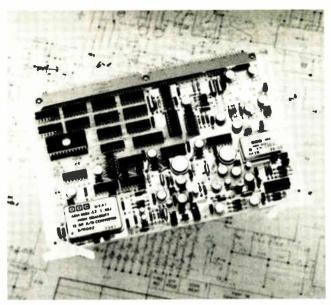
holds several leadless chip-carrier ICs. One DIP is the HI-5900 analog signal processor and the other is the HI-5712 8- $\mu$ s successive-approximation a-d converter. The HI-5900 has software-programmable gain and sample-and-hold amplifiers (Fig. 6).

Just as increasing levels of accuracy in monolithic converters are bringing their manufacturers up against fundamental limits like resistor-ladder network and voltage-reference stabilities, so hybrid converter makers are being confronted by increasing labor, materials, and packaging costs as hybrid circuit complexity increases. There is only so much performance that can be squeezed into a hybrid package before the product becomes too expensive to manufacture.

This is one reason why hybrid converter manufacturers without monolithic facilities are getting more involved with designing and laying out their own ICs for custom production by semiconductor manufacturers. They are also investigating a variety of innovative manufacturing methods and acceptable packaging materials to meet rising labor costs and increase functional densities. In addition, most of them are switching over from manual to automatic wire-bonding machines. Automatic laser trimmers and in-process testers are now more commonly used.

How a hybrid circuit is laid out and the layout's effect on testing and reworking are becoming as important to hybrid manufacturers as the circuit's design. The Harris leadless chip-carrier approach (cited earlier in relation to the firm's two-DIP data-acquisition system) was chosen because it allows economical in-house testing of the individual chips used and facilitates reworking through simple reflow soldering.

Nevertheless, certain applications like medical imaging, seismographic measurements, and audio digitizing require the use of very high-resolution data converters that are accurate to the same resolution and that can



**7. High performance.** Modular data converters provide the highest performance levels. This 16-bit a-d converter from ILC Data Device Corp. has a 4-μs conversion time. The DDC-5497 performs automatic corrections with an on-board programmable read-only memory.

hold that accuracy over time and temperature conditions. As has been the case for the last several years, modular data converters using discrete components mounted on printed-circuit boards continue to be the only type of converter to meet those needs (Fig. 7).

#### Modular converters are alive and well

According to Bernard Gordon, chairman of the board and technical director of Analogic Corp., Wakefield, Mass., a leading modular converter manufacturer, data-converter power-dissipation levels, sizes, and prices may have been dropping throughout the last two decades, but the disparity between what is being offered on the market and what the user discovers he or she really needs is growing wider.

"In 1969, we offered a 12-bit a-d converter module that sold for about \$800," he observes. "But it was built with ultrastable wirewound resistors, had a certified reference stable to within 0.01% for a year, and exhibited total stabilities of a few parts per million per °C. In short, it was 12 bits accurate over all operating time and temperature conditions. "Today, one can buy a 12-bit a-d converter for under \$20 that is certainly much smaller than the 1969 module and dissipates quite a bit less power. But will it be 12 bits accurate over time and temperature six months or a year later? Probably not, since the basic components used in monolithic and hybrid data converters such as resistors and references are fundamentally limited in performance."

Gordon points to the fact that laboratory standard wirewound discrete resistors typically used in Analogic's modular converters exhibit better long-term stability and accuracy than bulk, precision and laser-trimmed thinfilm as well as thick-film resistors typically used in hybrid and monolithic data converters. He cautions that "for a data converter to work properly, it should be designed and built with much better specifications than

### **Breaking the data-conversion speed barriers**

Applications for which data conversion speeds must be high are increasing. Radar, medical imaging, telecommunications, broadcast and video uses, and instrumentation all require very high-speed d-a and a-d converters capable of working at speeds of a few to tens of nanoseconds.

Two of the pioneers in high-speed data conversion are TRW LSI Products of El Segundo, Calif., and the Computer Labs division of Analog Devices, Greensboro, N. C. The former has pioneered monolithic high-speed d-a and a-d converters, while the latter has been in the forefront of developing hybrid and modular high-speed d-a and a-d converters.

At present, a number of monolithic and hybrid data converter companies are either actively in or clamoring to get into this lucrative high-speed data-conversion field.

TRW LSI Products has succeeded in reaching the 30-megahertz speed plateau with its monolithic 8-bit TDC1007J a-d converter. The company has 6- and 4-bit 30-MHz monolithic a-d converters (TDC1014J and TDC1021J) as well as 8-, 9-, and 10-bit monolithic 20-MHz d-a converters (TDC-1016J-8, TDC1016J-9 and TDC1016J-10). It hopes to have within a year a 10-bit 10-MHz monolithic a-d converter that makes use of the flash technique the firm employs in its line of high-speed a-d converters [*Electronics*, May 22, 1980, p. 34].

The flash, or parallel processing, technique involves the use of voltage comparators. The analog input signal for an a-d converter is applied simultaneously to several voltage comparators that are in parallel with each other. Each comparator is biased to operate at a unique voltage level. However, the number of comparators gets inordinately large with increasing converter resolutions, going up to the binary power. For an a-d converter, (2<sup>n</sup> – 1) comparators are needed, where n is the converter's resolution in bits. Thus for 8 bits, 255 comparators are needed. On the other hand, going from 8 to 10 bits means going from 255 to 1,023 comparators, and for 12 bits, 2,047 comparators would be needed. This sheer number of comparators, besides increasing an IC's complexity and manufacturing cost tremendously, increases the chip's power dissipation.

It thus remains doubtful that 10-bit and higher-resolution monolithic a-d converters could be made to operate at speeds like 30 MHz, at least for commercial markets.

TRW's Defense and Space Systems division in Redondo Beach, Calif., on the other hand, need not worry as much about the price constraints of the commercial market. Under development there, for example, is a 40-MHz monolithic 10-bit a-d converter for a defense contract. The division also hopes to integrate an 8-bit 25-MHz a-d converter and a sample-and-hold amplifier on the same chip. Even 10-bit 100-MHz a-d conversion is being looked at.

Motorola, which last year introduced a 10-ns 8-bit monolithic d-a converter [*Electronics*, Nov. 22, 1979, p. 140], the 10318, is getting ready to supply samples of a 7-bit a-d version (10317) using the flash conversion technique and operating at 30 MHz. Aimed at video processing in broadcast markets, the device will be priced in the \$100 range for 100-unit quantities.

Harris has also entered the high-speed d-a converter field with an 8-bit monolithic d-a converter. Its HI-5618 settles in 50 ns and is within  $\pm 1/4$  LSB accuracy over the commercial and military temperature ranges.

A number of other monolithic data converter manufac-

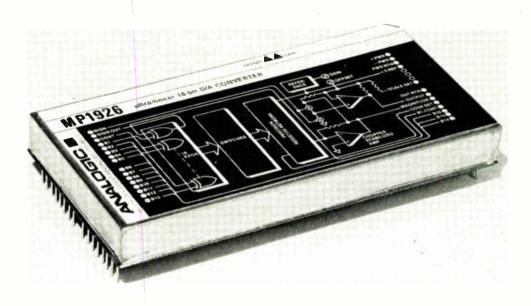
turers have plans for video converters. Ferranti Electric Inc. of Commack, N. Y., for example, is working on a bipolar 4-bit a-d converter with a conversion speed in the nanosecond range. The converter uses four 1-bit a-d converters in parallel. At this year's ISSCC, Plessey Semiconductor Corp., Irvine, Calif., discussed a 5-ns 8-bit monolithic d-a converter subsystem that the firm hopes to have ready shortly. Intended as a building-block component for a successive-approximation monolithic 15-MHz a-d converter, the 8-bit chip has a precision reference, a reference amplifier, and a latched comparator with a propagation delay of 1.3 ns. Also expected soon is the monolithic (SDA-5010) 6-bit 10-ns a-d converter from Siemens Corp., Iselin, N. J.

In line with the trend by hybrid converter manufacturers to get more involved with monolithic designs, ILC Data Device Corp. of Bohemia, N. Y., has designed and laid out two 14-bit monolithic d-a converter video-speed chips. The devices are being made by a semiconductor IC manufacturer and will feature low-glitch outputs. One of the 143-bit d-a chips has a current-output settling time of 30 ns, is ECL-compatible, contains an on-chip reference, and reportedly has an extremely low-glitch output. The other 14-bit d-a converter chip is a low-power device that also has an on-chip reference, settles in 100 ns (current output), and is TTL-compatible. It is classified by ILC as a low-glitch-output converter, whose glitch level is slightly higher than the first chip's.

There is only so much monolithic data-converter designers can squeeze out of chips for video-speed performances before hybrid designs take over for even higher performance levels. Take the DAC-HF series of high-speed hybrid a-d converters from Datel-Intersil Inc. of Mansfield, Mass. Available in current-output 8-, 10-, and 12-bit versions, they are specified with maximum settling times to a full-scale change within 1 LSB of 25, 25, and 50 ns maximum. Each unit has a voltage reference, ladder network, and current switches. Stability is typified by a maximum gain temperature coefficient of 20 ppm/°C.

An innovator in high-speed video data converters is Computer Labs. The firm makes the fastest hybrid and modular a-d and d-a converters in the 4-to-13-bit resolution range. Its 9000 series "Bare Bones" CLB1310, for example, is a 13-bit a-d converter with a word-encoding rate of 10 MHz. In the firm's MOD family of a-d converters, a line of high-speed video converters spans 4 bits at 100-MHz (MOD4100) to 12 bits at 5 MHz (MOD1205). Some of the devices are on small single printed-circuit cards. The 10-bit 20-MHz MOD1020, for example, is housed on a small card only 35 square inches in area. The card also holds a track-and-hold amplifier with a 25picosecond aperture time. Large-signal bandwidth for the MOD-1020 is 15 MHz. The firm also makes equally fast hybrid d-a converters like the 10-bit 5-MHz 4120E and the 13-bit 10-MHz model 1310.

Recently, Computer Labs entered the raster-scanning cathode-ray-tube market with the 8- and 10-bit HDD0810C and HDD1015C hybrid d-a converters that feature rapid settling times and low-glitch outputs in dual-width dual in-line packages [Electronics, May 22, 1980, p. 206]. Offering composite-blanking 1-V outputs and terminated in 75-ohm impedances, the converters feature a settling time of 10 ns (to 0.2% of full-scale value). The maximum output glitch energy is 200 picovolt-seconds.



8. Ultralinear. For digital audio, a data converter must be highly linear. This modular 16-bit d-a converter from Analogic Corp. (MP1926) has a total drift of less than 1 ppm/°C and less than 0.005% total harmonic distortion. Offering the equivalent of 18-bit linearity, it has ±1/4-LSB maximum midrange nonlinearity.

the system's rating, so that the laws of probability will see to it that, say, a 12-bit converter is truly a 12-bit converter. It is generally counterproductive to attempt to just barely make it with a design."

Although many data-converter designers agree with Gordon on the superior performance of discrete components used in modular converters, they disagree on the extent of limitations he cites for the types of resistors used in monolithic and hybrid converters. The fact that there are 10-bit monolithic and 12-bit hybrid data converters that pass the time and temperature test indicates how much progress has been made in monolithic converter technology—it is only a few years since 8-bit monolithic data converters were 8 bits accurate at room temperature only.

Quite a few applications do not demand high levels of accuracy over time and temperature. In many such cases, users are content with, for instance, a 12-bit converter that gives them 10 bits of accuracy. Furthermore, the sensors with which an a-d converter is interfacing are often accurate only to within 1% to 2%.

On the other hand, for many large process-control applications, high levels of converter stability and accuracy can translate into high processing efficiencies and savings of millions of dollars in improved productivities.

### Ultralinearities for digital audio

One application for which data converters must be ultralinear is in digitizing audio, where a wide dynamic range of 96 decibels (16 bits) is needed. A drift of just 1 bit out of 16 can foul up the digitized audio's quality with crosstalk and render the digitizing process useless.

Analogic recently introduced an ultralinear 16-bit modular d-a converter with the analog equivalent of 18-bit linearity to address this problem (Fig. 8): the MP1926, which settles under 3  $\mu$ s (MP1962A), has total drift from all error sources of less than 1 ppm/°C

(MP1926S). Its total harmonic distortion is under 0.005%, measured with a deglitched amplifier. It is ultralinear, having  $\pm \frac{1}{4}$  LSB maximum midrange nonlinearity. The converter is designed specifically for reconstructing dynamic complex waveforms from digital data, particularly audio, acoustic, and sonar signals that have substantial information content in the vicinity of the midrange of 0 V. At 0 V, the converter has the equivalent of 18 bits of linearity.

The MP1926 achieves its high performance levels thanks to a proprietary sign-magnitude internal architecture that improves the converter's performance as the signal approaches zero level from either direction. Although the sign/magnitude conversion scheme is a known one, it has formerly been limited in high-speed and high-accuracy performances.

### The microprocessor: to have or have not

A debate is on within the data converter industry as to whether or not a microprocessor and a data converter ought to be integrated together on the same chip. Proponents of this approach argue that, though such an approach would make the chip more dedicated, in applications like those in the automotive field it makes sense to combine a microprocessor and a data converter on the same chip. Opponents, on the other hand, point out that such a level of integration would not only make the IC more specialized, but would also make it so complex as to be uneconomical to manufacture.

The debate is taking on more urgency because a number of microprocessor manufacturers have already put data converters on the microprocessor chip. The most notable of these is Intel's model 2920 so-called analog microprocessor [Electronics, March 1, 1979, p. 105], which has an a-d converter at its input and a d-a converter at its output. Other microcomputers with data converters on them are Intel's two-input 8022,

Motorola's 146805R2, and TI's TMS2100.

Explains Gene Pucket, manager of automotive systems engineering of Motorola Inc., Mesa, Ariz.: "Although putting an a-d converter on the same chip as the microprocessor makes the chip more dedicated for automotive and similar applications, such a chip could serve other uses, like industrial control. Besides, a dedicated chip containing both the microprocessor and an a-d converter is more reliable than two separate chips." Motorola and other big data-converter chip makers have large automotive programs in which their data-converter products are being used.

One thing everyone agrees on is that many monolithic and hybrid data converters on the market are not truly microprocessor-compatible, often requiring additional external components. As a result, some manufacturers are trying to offer products that are totally microprocessor-compatible, like the double-buffered series of Micro-Dac C-MOS d-a converters from National Semiconductor [Electronics, June 19, 1980, p. 140] and the Beckman 7581 double-buffered 12-bit hybrid d-a unit that is pin-for-pin-compatible with the popular DAC-80.

The issue of microprocessor compatibility is gaining in importance because a growing number of data converter users know little about the intricacies of analog-to-digital interfacing. However, with so many microprocessor buses out there, which one should be picked as the standard interface?

Leroy Little, senior development project engineer for

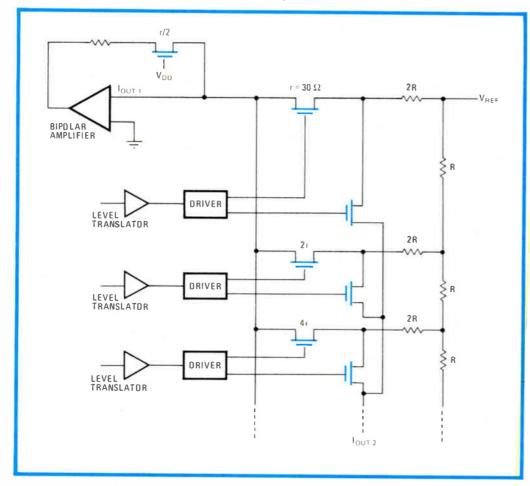
Beckman Instruments Inc., Fullerton, Calif., says that "if a standard microprocessor bus could be achieved for peripherals—and that could be very difficult—it would make the converter designer's job quite a bit easier. Certainly the 6800 and 8080 microprocessor families are two well-known and popular buses that are well worth standard bus interface."

Another microprocessor-interface issue stems from the emergence of high-speed microprocessors. Converter manufacturers are now finding that their products have to keep pace with faster microprocessors and that the right amount of input and output buffering is one way of tackling this problem.

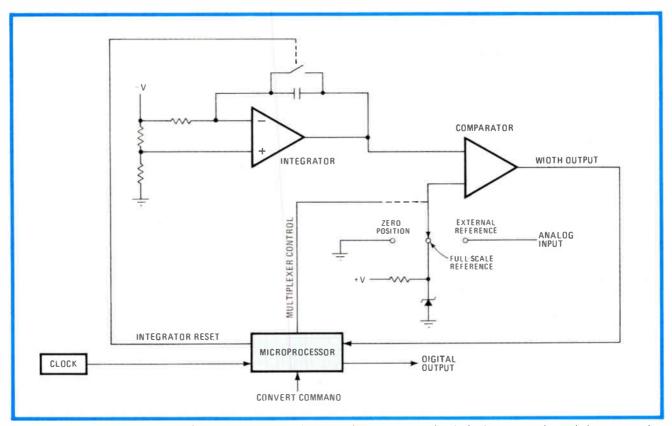
### Innovations in design

Many a converter designer is finding out that old circuit ideas never die. Some of these once discarded circuit concepts are being brought back to life with a new twist. Designers are discovering that totally new circuit designs are not always needed to surpass certain performance barriers.

Take the sign/magnitude conversion scheme mentioned earlier for Analogic's MP1926 ultralinear 16-bit d-a converter with 18-bit accuracy. That conversion technique is an older one whose previous limitations have been improved by Analogic with an innovative circuit design. Analogic claims that its implementation of the sign/magnitude conversion method is superior in performance to older offset-binary and other bipolar



9. Stable. Beckman Instruments achieves high stability with this current-switch and resistor-ladder network used in its family of 12-bit hybrid data converters. The amplifier-based feedback loop provides better gain stabilities and power-supply sensitivities than conventional R-2R resistor networks and allows better linearity compensation.



**20-bit a-d.** In this experimental circuit from National Semiconductor, a microprocessor and a single-slope conversion technique are used to get 20-bit (1-ppm) a-d conversion linearities. Conversion accuracy is limited only by the absolute accuracy of the reference used.

sign/magnitude techniques. Judging from the MP1926's specifications, that claim is modest.

In Teledyne's model 4134 12-bit hybrid a-d converter, an adaptation of the traditional successive-approximation conversion circuit is used to increase conversion speeds. Called progressive approximation, it involves adding sense control functions to a conventional successive-approximation circuit (Fig. 3).

Often, the most innovative and far-reaching circuit designs result from simple circuit ideas. Such is the case of the segmented resistor ladder network conceived by John Schoeff, project manager for Advanced Micro Devices. The network is used in AMD's monolithic 12-bit model 6012 d-a converter.

In all of Beckman Instruments' hybrid 12-bit data converters, a modification of a current-switched resistor ladder used by H. H. Schmid of General Electric Co., Syracuse, N. Y., results in a ladder network with better performance than conventional designs. The circuit (Fig. 9) offers better gain temperature coefficients, more linearity due to its compensation technique, and less power-supply sensitivity.

At this year's 38th Annual Device Research Conference, researchers from the Japanese Musashino Electrical Communication Laboratory, Tokyo, described a novel resistor-trimming technique that can be used to make high-resolution d-a converters. The technique involves applying current pulses to arsenic-doped polycrystalline silicon. The current pulses cause the polysilicon resistors to decrease in resistance and thus be trimmed. The resistance can also be increased by following a current-

decreasing pulse with one slightly lower in value. The trimming technique described was applied successfully to the fabrication of a monolithic 14-bit d-a converter with a linearity error of less than 1/4 LSB. Settling time is 200 ns. Full-scale drift of 3 ppm/°C was claimed.

### Rehashing some old principles

Remember the single-slope a-d conversion technique of some 20 years ago? It might be coming back with a new twist.

At National Semiconductor Corp., Jim Williams, linear applications engineer, is experimenting with a microprocessor-based circuit using the single-slope conversion technique for extremely high-linearity a-d converters (Fig. 10). In fact, he has demonstrated 20-bit (1-ppm) linearities in an a-d circuit whose absolute accuracy is limited by the accuracy of the voltage reference used. One of Williams' colleagues, the venerable Robert Pease, staff scientist, is also working with an 18-bit a-d conversion scheme using the well-known voltage-to-frequency conversion principles.

There may very well be dozens of other examples like the ones mentioned here on circuit-design ingenuity. The point worth noting is that perhaps the answer to future high-performance monolithic data converters lies more in the past. It could be that the era of radically new circuit ideas has reached saturation point and that innovative thinking may benefit more from a closer look at older basics.

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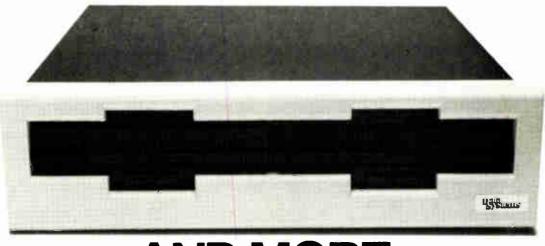
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# Guarding ICs against static discharge

Individual devices and loaded circuit boards should be handled and transported in laminated or carbon-loaded containers

by Donald R. Yenni Jr. and James R. Huntsman, 3M Co., St. Paul, Minn.

☐ Major advances in processing are already resulting in very large-scale MOS integrated circuits with increased packing density, higher operating speed, and lower operating power. However, the finer lines and thinner oxide layers of these new superchips will aggravate a problem that has plagued MOS manufacturers and users since the emergence of these devices—device failure from electrostatic damage.

Fortunately, effective methods and materials for handling and packaging static-sensitive devices have been developed. For MOS devices—whether individual parts or mounted on printed-circuit boards—transportation in bags, tote boxes, or storage tubes made of special metalized film laminates or carbon-loaded plastics serving as static-protective materials is required. The use of older, military-specified materials has resulted in device damage and failure.

Today's MOS ICs can be damaged by electrostatic discharge as low as 100 to 200 volts. Electrostatic dam-

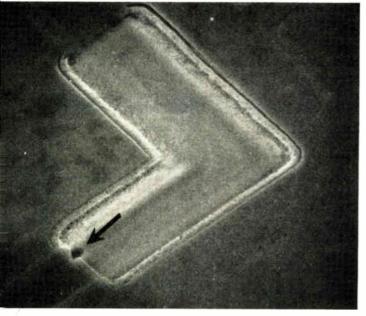
1. Zapped. Protective devices for MOS ICs are often ineffective in preventing field-induced static damage. Here a direct discharge from a person has damaged the input-protective diode of a p-MOS character-generator chip, damaging the entire circuit in the process.

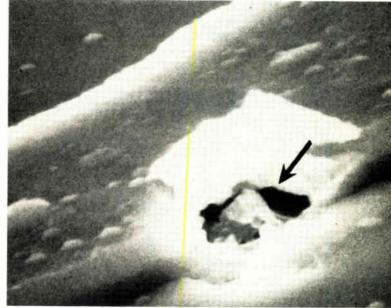
age to complementary-MOS devices occurs from 250 to 3,000 v. And although MOS circuits are the most susceptible to electrostatic discharge, large numbers of bipolar ICs, diodes, and even film resistors have been damaged or even completely destroyed by static charge in various stages of board assembly. The danger is evident when it is realized that a person merely walking across a tile floor can generate an electrostatic charge upwards of 25,000 v.

The single most important characteristic of a static-protective packaging material is its electrical resistance. The lower the resistance of the package, the greater the static protection. In fact, to characterize a material as being static-protective, a resistivity measurement may be all that is needed, as will be seen.

In any discussion of packaging materials, two elements must be considered: the ability of the material to protect devices from damage due to triboelectrically (frictionally) generated charge and its ability to shield

2. In the bag. This 3N157 MOS FET was damaged by static charge generated while inside a MIL-B-81705 Type I film bag. Type I material consists of an opaque aluminum foil laminated to a polyethylene film. Static is created inside bag as parts rub together.





Paulaning films	Number of damaged devices after shipment test							
Packaging films	3N157 (10 tested)	SM110CJ (5 tested)						
MIL-8-81705 Type I	9	4						
MIL-B-81705 Type II	9	4						
Metalized film laminate	0	0						
Carbon-loaded film	0	0						

its contents from external electrostatic charge.

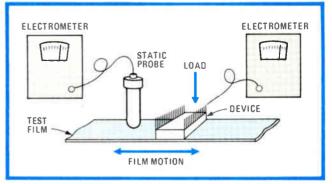
Triboelectric charge generation between materials is independent of electrical resistivity. It results whenever two materials contact one another and then separate, and rubbing enhances the effect. Triboelectric charge can damage semiconductor devices, particularly as they are inserted or removed from a bag and during shipment.

External static fields may also present a problem, a factor often overlooked in selecting a packaging material. The electric fields from nonconductors such as foam packing material and tape and from conductors such as charged employees all have been shown to cause electrostatic damage to semiconductors unless the proper steps are taken to shield the devices.

### Charged personnel

Electrostatic damage occurs most commonly when a person charged with static electricity touches a semi-conductor device, causing a transient voltage discharge to pass through it. This discharge produces such a high current density at the junction interface in the device that overheating and melting result. An example of static-induced damage is shown in Fig. 1.

Many semiconductor devices also can be damaged without direct contact. One of the most basic semiconductor structures, consisting of an insulating layer between two relatively conductive layers (essentially a capacitor), can be destroyed by exposure to a voltage field. When such a field exceeds the insulating layer's dielectric strength (about 100 v on current MOS chips), dielectric breakdown occurs. These field-sensitive capacitive elements are present in all MOS devices. A similar capacitive element is often found in non-MOS semicon-



3. Triboelectric screening. A test apparatus of this type is used for triboelectric screening of bag materials. In a typical test, the material in question is rubbed against pc boards and devices and monitored for charge buildup by means of electrometers.

ductors—for example, as a discrete capacitor in linear ICs or hybrids and inherently in bipolar ICs between insulated metal crossovers.

Faraday established that field-induced effects can be prevented by enclosing an object in a highly conductive material. This creates an electrostatic shield, or Faraday cage. The degree of shielding of the Faraday cage is a function of the conductivity of the shield material: the higher the conductivity, the better the shielding.

### Bagging it

One of the most widely applied methods of protecting static-sensitive ICs is static-protective bags. These bags should protect their contents both from frictionally generated static and from a handler's static charge.

Basically, four types of bag material are available. Two are materials specified by MIL-B-81705, the major military standard for protective packaging materials. The others are a low-resistivity carbon-loaded film and a metalized laminate film. Tests done at 3M Co. show both military-specified films to be ineffective in preventing static damage. On the other hand, the two commercial types worked well.

Type I mil-spec material is an opaque-foil film laminate composed of aluminum foil on polyethylene film. This material can act as a shield against electromagnetic interference. Also, it has an extremely low moisture-vapor transmission rate, which enhances its use for long-term storage. However, although Type I film is an

		Z . 7.	Number of devices damaged (out of 10)				
Bag material	Tendency to charge	Resistivity of bag material	Devices on printed-circuit boards	Loose devices			
Plain polyethylene	high	10 <sup>16</sup> Ω/sq	10	9			
MIL-B-81705 Type I	híġh	10 <sup>16</sup> Ω/sq	6	10			
MIL-B-81705 Type II	low	10 <sup>12</sup> Ω/sq	none	none			
Carbon-loaded plastic	low	300 Ω·cm	none	none			
Metalized film laminate (antistatic side)	low	10 <sup>13</sup> Ω/sq	none	none			

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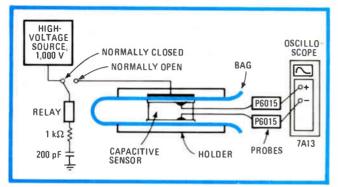
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**4. Shield testing.** This apparatus tests the shielding capability of various types of protective bags. A capacitive sensor detects the amount of static voltage coupled from a simulated static discharge. The sensor's voltage is displayed on an oscilloscope.

excellent electrostatic shield, it is not electrostatic-free. Because the inside, black, heat-sealable surface of the film is an insulator having a surface resistivity in excess of 10<sup>16</sup> ohms per square, it will not dissipate static electricity and will easily create static when parts rub against it.

Type II materials are transparent extruded antistatic films. Typically, they are composed of polyethylene plus an antistatic agent; the latter is an organic compound dispersed throughout the volume of the polyethylene or coated onto the completed film's surface. Type II bags do not effectively protect their contents from external fields of static charge.

As noted, two other types of film are also commercially available for protecting static-sensitive devices. One is a carbon-impregnated volume-conductive film. The other is composed of an outer metalized layer forming a Faraday cage and an inner antistatic film preventing the generation of triboelectric charge [Electronics, Feb. 16, 1978, p. 167]. It combines the best feature of the Type I and II films.

All four bag materials were tested for static protectivity by placing 3N157 MOS field-effect transistors and SM11OCJ linear ICs, which contain both bipolar and p-channel MOS devices, on pc boards and sealing them in various bag materials. Each semiconductor was tested before being inserted onto a board. The results showed conclusively that the two commercial bags were more effective than their military counterparts.

The bagged boards were placed in a cardboard box with a foam packing material commonly used for protecting components. In low humidity, this insulating foam can accumulate a high static charge through triboelectric charging during shipment. It was used to determine whether its charge could damage devices through the walls of the protective bags.

### How they did

The box was sealed and placed on a truck bed vibrator and run at 250 revolutions per minute for one hour. Relative humidity was held to 30%. The box was then unpacked and the devices retested. As expected, the foam had developed from 3 to 8 kilovolts of electrostatic charge due to vibration.

Significant failure levels were found in the two mili-

Bag material	Resistivity	Pulse amplitude (V)
MIL-B-81705 Type II	1 x 10 <sup>12</sup> Ω/sq	450
Carbon-loaded	1 × 10 30/34	450
plastic	3 x 10 <sup>2</sup> Ω-cm	310
Carbon-loaded	5.6 x 10 <sup>3</sup> Ω-cm	500
prostro	3.0 x 10 32 cm	300

tary-specified films (see Table 1). Devices in the Type I material bag were well shielded from the external effects of the charged foam packing but were damaged by frictionally generated charge on the pc boards and on the semiconductors themselves inside the bag. Figure 2 is a scanning electron photomicrograph of one of the 3N157s damaged while inside the Type I material bag.

Devices in the Type II material resisted triboelectric charging because of the bag's antistatic inner surface. However, they were damaged by the voltage field from the charged foam.

The highly conductive carbon-loaded film and the metalized film laminate with an antistatic interior minimized the effect of triboelectric charge and provided sufficient shielding from the voltage generated on the charged foam. No devices were damaged in bags made of these films.

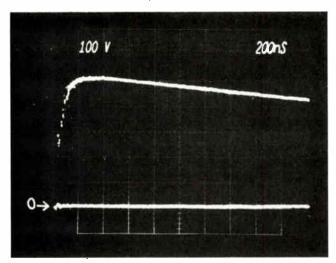
### Static testing

Relatively simple setups were devised to test whether a material is suitable for controlling triboelectric charge generation and providing electrostatic shielding. To test its resistance to triboelectric charging, the material is rubbed against electronic devices and pc boards and monitored for charge buildup as shown in Fig. 3. This test gives a reasonable indication of whether a damaging static charge might be produced on a device, a pc board, or the film itself.

Voltages on ICs with metal, ceramic, and plastic lids were monitored by attaching a single lead to the pins along one side of each dual in-line package. The voltage induced on the lead frame resulting from rubbing the DIP lid against each test film was monitored by electrometer. In the case of the boards, a single wire soldered into one of the terminal holes was used to indicate the voltage on the device lead located on the board. Both the film samples and the devices were electrically isolated from ground during these tests.

Films causing residual voltages in excess of 25 V on either the device it was being rubbed against or on the film itself were rated as having a high propensity for such charge generation. Those films charging to less than 5 V were considered to have a low propensity for charge generation.

Surprisingly, there did not seem to be any middle



5. Type II bag. Lack of an electrostatic shield and high surface resistance result in a long-duration, 450-volt pulse coupled to the interior of a Type II bag. As this voltage is sufficient to damage most MOS devices, this bag is an ineffective electrostatic shield.

ground for the films being tested. At most speeds and loads, a film charged either rapidly or hardly at all.

Because of their antistatic surfaces, the metalized film laminate and Type II materials did not charge themselves or the parts during the charging tests (see Table 2). Similarly, the conductive carbon-loaded film produced less than 5 V on itself and on the parts.

#### **More results**

Plain polyethylene tended to generate rather high localized charges on itself. Because of its high resistivity, it could not dissipate these charges. Spot voltages on a sample typically varied from +200 to -1,000 V.

Type I material, like plain polyethylene, exhibited high charging tendencies. The highest measured voltages occurred on the devices' lead frames and on the pc boards and not on the film itself, as had been the case with plain polyethylene. It is suspected that the highly conductive aluminum sublayer in the Type I film suppressed the voltage field surrounding the charges on the

film, making accurate measurement difficult.

According to these results, both conductive and antistatic films are capable of controlling triboelectrically generated charges. Table 2 indicates that a correlation does exist between resistivity and a film's ability to deal with frictional charge generation. Antistatic films having a surface resistivity of  $10^{13}$   $\Omega/\text{sq}$  or less are capable of retarding triboelectric charge generation. Although the experiments conducted at 3M have not been extended to these limits, volume-conductive materials having a resistivity of even as high as  $10^{11}$   $\Omega$ -cm are capable of distributing charge rapidly enough to prevent the damaging effect of triboelectrically generated charge.

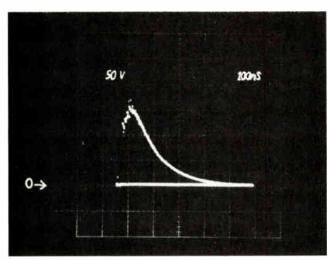
### Resistivity versus charge

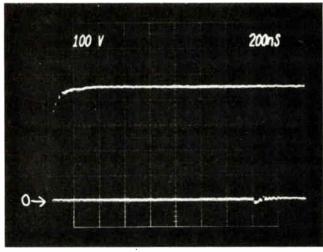
A test was run to determine whether the results shown in column 1 of Table 2 could be correlated with the problems that could occur if a static-sensitive device or board was placed into a package of the material and shipped. This was done by sealing several 3N157 MOS FETs (in metal-can packages) mounted on pc boards in bags made of various materials, shaking them for a few seconds, and then retesting them. In addition, loose 3N157s were placed singly in bags and shaken for 1 minute. Columns 3 and 4 of Table 2 show the results of these tests, along with the triboelectric screening data and material resistivity for each.

As expected, no device failures occurred in the bags having antistatic inner surfaces or made of the conductive carbon-loaded film. The tendency of plain polyethylene to generate and sustain isolated voltage differences was the likely cause of failure for all the MOS FETs that were mounted on pc boards and the 9 out of 10 loose devices that were damaged in bags of this material.

Voltages triboelectrically created by the Type I material resulted in the destruction of 6 out of 10 of the devices mounted on pc boards and all 10 of the loose devices. Therefore neither the Type I material nor plain polyethylene should be used as intimate wraps for static-sensitive devices.

The amount of electrostatic shielding a material provides is directly related to its conductivity. The question





**6. Carbon-loaded.** Variations in the resistivity of carbon-loaded bags result in variations in the coupled pulse's height. A carbon-loaded sample with a resistivity of 300  $\Omega$ -cm (left) has a 20% lower pulse height than a 5,600- $\Omega$ -cm sample (right).

### The continuing threat of electrostatic damage

Electrostatic damage to printed-circuit boards loaded with MOS integrated circuits continues to plague both commercial and military users of complex electronic equipment. In fact, the concern is so great that the Department of Defense has come out with a new standard, DOD Standard 1686, on electrostatic discharge control [Electronics, July 3, 1980, p. 39] that among other things calls for the use of a combined antistatic and conductive wrap for electronic items shipped on Government contracts.

Prime examples of industry's concern are the experiences of the Unitech Products division of Radian Corp., Austin, Texas, and the McDonnell Aircraft Co., St. Louis, Mo. Unitech, a producer of programmable batch terminals, recently had a near disaster when a rash of IC failures was directly traceable to a change in static-protective bag material. As for McDonnell, it has initiated an extremely stringent program to protect static-sensitive semiconductor components on the F-18 fighter's electronic subsystem. Part of the program consists of insisting that all vendors ship boards and components in static-shielding bags or risk return of the material.

Unitech manufactures a microprocessor-controlled communications system that contains a considerable number of MOS components requiring special protective measures. Under Bob Morton, then a senior engineer with the company, precautions were taken to eliminate every source of static electricity. Manufacturing operations were conducted at static-safe work stations and test station benches were grounded. Loaded pc boards were moved from station to station and shipped in opaque carbon-loaded bags. These precautions proved effective.

However, to be able to see and identify the type of board inside each bag, Unitech engineers substituted transparent antistatic-coated pink polyethylene bags for the opaque carbon-loaded types that had been used. The results were nearly catastrophic. The number of boards with damaged or destroyed ICs zoomed, particularly at the customer's end.

"We were having to ship almost twice as much stuff out to the field as replacements, since about half of the boards shipped were turning up dead on arrival," says Morton. Unitech's fix was first to return to the original bag type and then to switch to bags of a new transparent material from 3M Co. combining a nickel coating, polyester, and antistatic polyethylene.

Morton is now manager of digital electronics at Esquire Inc.'s Wide-Lite division, San Marcos, Texas, in charge of a program to develop microprocessor-based lighting controls. His first move on his new job, he says, was to order carbon-loaded bags, conductive mats, and wrist straps.

"At McDonnell," says Glen Fisher, a specialist in electronics support technology, "failure analysis has shown that many electronic failures of linear and MOS ICs in this program were caused by electrostatic discharge. In view of this fact, we are in the process of educating 3,500 people in static control, and we feel we are way ahead of other airframe firms in attacking the problem."

McDonnell has written stiff process specifications, installed conductive benches, and even made training films on electrostatic protection. It uses only bags made of the 3M metalized laminate internally and specifies that all boards and components shipped in bags from vendors must use a similar material or be returned.

The importance of electrostatic damage to electronic components is underscored by the fact that the Air Force's Reliability Analysis Center, Rome Air Development Center, Rome, N. Y., is going to devote an entire seminar to the subject on Sept. 9–11 at the Town and Country Hotel in San Diego, Calif. The seminar's 30 to 35 papers will cover all phases of electrostatic damage, including such topics as problems and techniques, failure mechanisms, and protective networks.

is, how conductive must it be to provide adequate shielding protection?

In order to answer this question, a special test was designed to measure how much of a specified external static discharge is coupled into the interior of a bag. The test setup is pictured in Fig. 4.

### **Shielding tests**

A special sensor consisting of two conductive plates separated by an insulator monitored the voltage difference between the top and bottom of the inside of the bag. Each capacitive plate was connected to an input of the differential amplifier of a fast storage oscilloscope. A metal disk was positioned against the top of the bag and held there between two parallel nonconductive holders.

A static discharge was then applied to the top of the bag through the metal disk. All discharges were at 1,000 V from a charged 200-picofarad capacitor through a 1,000- $\Omega$  resistor. Table 3 shows the resulting transient voltage observed across the sensor in several commercially available bags.

Because of its intermediate metal-foil layer, the Type I bag is an excellent static shield. (It cannot, however, be considered completely protective, because of the tribo-

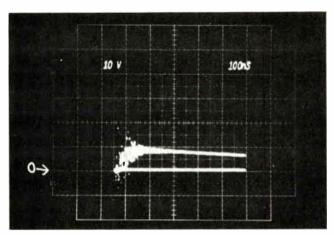
electric charging propensity of its nonconductive inner surface.)

Type II material showed poor shielding because of its extremely high surface resistance (Fig. 5). A measurement of the entire pulse duration in this bag could not be made using this equipment. Charge equalization across the sensor occurred faster through the probes ( $10^8 \Omega$  to ground) than around the bag ( $10^{12} \Omega$ ). Type II material, like plain polyethylene, does not offer Faraday-cage static protection.

### Increasing the resistivity

A tremendous difference in the shielding effectiveness of volume-conductive materials having a resistivity in the range of  $10^2$  to  $10^3$   $\Omega$ -cm was illustrated with two carbon-loaded plastic bags (Fig. 6). Increasing the film resistivity from 300 to 5,600  $\Omega$ -cm resulted in a 20% increase in pulse amplitude.

As important as the amplitude of the pulse, however, is its duration. The increase from 300 to  $5,600~\Omega$ -cm yielded a thirtyfold increase in pulse length. Higher voltages can be tolerated by a device for shorter times. The lower the resistance around the bag, the shorter the pulse duration and the less the opportunity for damage



7. Metal laminate. A bag composed of a metallic coating over a polyester film followed by a layer of antistatic film effectively stops capacitive pulse coupling, resulting in a short-duration 15-volt pulse. The coating acts as an effective Faraday cage against external fields.

to the device.

The surface resistivity of the metalized film laminate was found to be 100  $\Omega/\text{sq}$ , and only a barely observable pulse was produced (Fig. 7).

Although this pulse-shielding test does predict relative material behavior well, it must be noted that it uses a step-function voltage excitation. In an actual person's touch discharge, though, the excitation is not a step function. The reason is that as the person's hand nears the bag, the electric field causes induced charge redistribution in the material before contact actually occurs. The pulse amplitude, or voltage difference, actually occurring across the bag is therefore reduced proportionally to the conductivity of the bag.

The advantage of the pulse test is that it allows the relative effects of the electrical properties of a material on static protection to be determined quickly and easily. Once the basic electrical parameters enhancing static protection are identified, their effects on devices may be observed by means of a practical in-use test.

### **Personal tests**

A 3N157 was used to evaluate the effects of material resistivity on actual device protection when a person is touching the bag. The MOS FET's actual level of static sensitivity was determined by alternately connecting a 200-pF capacitor in series with a 1-kilohm resistor to a variable dc supply and to the gate lead of the FET. The pulse-forming network was alternately charged by the power supply and discharged through the FET in rising 25-V increments until damage occurred, with damage defined as a shift out of manufacturer's specification in the gate-threshold voltage (V<sub>T</sub>) or gate-leakage current (I<sub>GSS</sub>). The 90% failure level was determined to be 200 V.

A 3N157 that had been tested and found good was placed in one of a variety of bags. A charged person then touched the outside of the bag directly adjacent to the device. After removal from the bag, the FET was retested to see if it had been damaged. If not, the voltage on the person was increased and the experiment repeated until either the device failed or the test equipment maximum of 25 kilovolts was reached. This test was performed on

10 different devices in each bag sample. The average level of voltage on the person at which device failure occurred in various volume- and surface-conductive bags is shown in Fig. 8.

### Lowering the resistivity

For volume-conductive materials (4 mils thick), a sudden drop in shielding effectiveness occurs in bags made from films exhibiting a resistivity of between 102 and  $10^3 \Omega$ -cm. The 5,600- $\Omega$ -cm bag, exhibiting the higher, longer pulse in the oscilloscope testing, protected the devices to only one third the voltage of the  $300-\Omega$ -cm material. At lower resistivities, the shielding effectiveness increased very rapidly. This relationship is an important consideration in selecting packaging materials that will provide effective static protection. The effect of increasing the thickness of a volume-conductive material is that of raising the level of protection afforded by film of a given resistivity. Thus, whereas a thin-walled bag made from a material having a resistivity 10<sup>2</sup> to 10<sup>3</sup>  $\Omega$ -cm might allow static damage, tote boxes or DIP tubes of a very thick volume-conductive material would be highly protective.

A similar relationship of protective efficacy to increasing conductivity was noted with surface-conductive materials, as shown by the curve on the right of Fig. 8. In this case, however, the effects of conductivity were not so abrupt. The maximum surface resistivity that offered 25-kV protection to the MOS FETs was found to be about  $10^4~\Omega/\text{sq}$ . For surface-conductive materials, variations in film thickness were found to have very little effect on shielding. Consequently, tote boxes and DIP tubes of such materials provide little more shielding than the thinwalled bags.

### **Protective tote boxes**

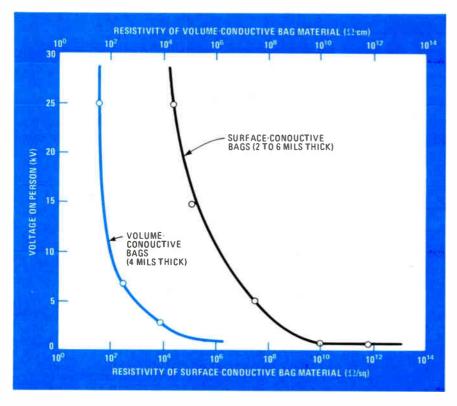
The primary use for tote boxes is for in-plant transportation of devices and pc boards to and from controlled-static work stations. As with bags, low-resistivity material is best for electrostatic protection.

The shielding effectiveness of two types of tote boxes—a volume-conductive, carbon-loaded plastic box with a resistivity of 300  $\Omega$ -cm and a surface-conductive antistatic plastic box having a resistivity of  $10^{11}$   $\Omega/\text{sq}$ —were examined experimentally. A test apparatus similar to that of Fig. 4 was used to measure the amplitude and length of the pulse coupled into the two types of box. The transient discharge was applied from a human-body equivalent consisting of a 200-pF capacitor discharged through a  $1,000-\Omega$  resistor. The transient voltage across the boxes was monitored with the probes and oscilloscope used in the pulse tests for bag materials.

### **Thicker walls**

For volume-conductive boxes, increasing the wall thickness decreases the resistance around the box. This in turn enhances the shielding ability of the box over that of a thin-walled bag made from a material having the same resistivity.

The 75-mil thickness of the material from which this tote box was made cut the amplitude of the pulse in the tote box to a twentieth of that of the comparable bag



8. Shielding effectiveness. This composite graph compares the shielding effectiveness of both volume-conductive and surface-conductive bags. Note that for volume-conductive bags, shielding effectiveness increases rapidly at low values of resistivity.

(see Fig. 6 again). More important, the duration of the voltage transient in the tote box was extremely short (under 200 nanoseconds).

The surface-conductive antistatic tote box also had a much thicker wall than the comparable bag, but that did not appreciably improve its shielding ability. The increase in wall thickness from 6 mils for a bag to 75 mils for a box increased the shielding ability by only 30%.

The tote boxes were also functionally tested for their static protection. A pc board containing a static-sensitive MOS FET was placed in each box. The foil pattern of the board was designed so that each lead was terminated at the card edge, and the board was large enough to span the box from one side to the other.

The voltage on the experimenter was increased in steps starting at 1 kV up to a maximum of 25 kV. At each step, the charged person touched one end of the box. This test was run with the box on a conductive table top and on a nonconductive table top.

Ten devices were tested in each tote box. One device at a time was mounted on the pc board and tested. The high, low, and average values of the voltage on the person touching the box when the device was no longer within manufacturer's specifications were recorded in the test.

All 20 devices placed inside the antistatic plastic tote box (10 on a conductive table top and 10 on a nonconductive top) were damaged at from 1 to 4 kv. The devices on the pc boards in the carbon-loaded plastic tote box all were protected to voltages in excess of 20 kv.

Perhaps the most common carrier used for shipment, storage, and automatic handling is the storage rail, or tube, designed for holding dual in-line packages. These DIP tubes are fabricated from a variety of materials,

including aluminum, plain plastic, carbon-loaded plastic, and antistatic plastic.

Because of the odd shape and small size of these tubes, it was difficult to make many meaningful measurements of the pulse inside using the high-speed oscilloscope technique previously described. Therefore, the shielding ability of each type of DIP tube was examined by placing a SM110CJ integrated circuit inside. This 14-pin IC was tested using a 200-pF capacitor discharged through a  $1,000-\Omega$  resistor.

### Static protection in DIP tubes

The tube containing the IC was placed on an uncharged surface and touched by a person at a potential of 2,000 v. The device was then tested for damage. If it was still good, the voltage was increased and the test repeated until damage occurred. The voltage at which the device was damaged was recorded for five different devices in each DIP tube. This test was performed on both grounded conductive and uncharged nonconductive table tops.

A comparison of the data on device damage for plain plastic and antistatic DIP tubes shows that there is virtually no difference in their shielding characteristics. Devices contained in these plastic tubes were destroyed at an average voltage on a person of 4,000 v. Although the nonconductive package materials used to provide physical protection for these tubes in shipment are often charged far in excess of 4,000 v, the biggest hazard is people, who commonly attain potentials of as high as 10,000 v in the manufacturing environment. The devices packaged inside the DIP tubes made from carbon-loaded plastic (300-Ω-cm resistivity) and those packaged in the aluminum tube all were protected to the maximum test voltage of 25 kv.

### **Designer's casebook**

### Dynamic logic probe displays five states

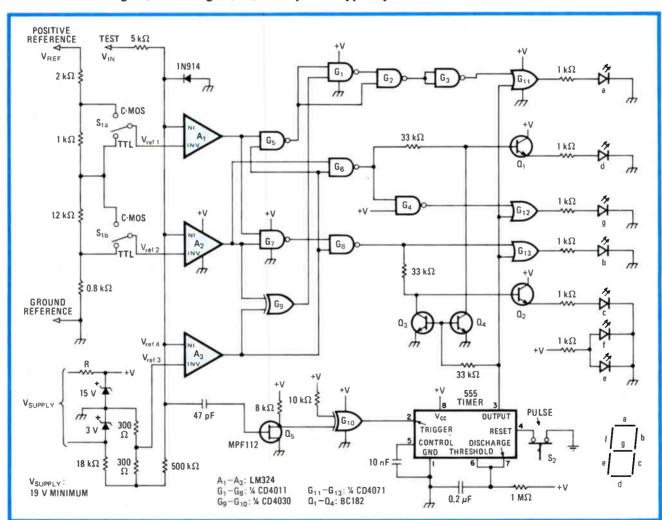
by Mihai Antonescu Federal Institute of Technology, Lausanne, Switzerland

Providing the convenience of the logic probe proposed by Prasad and Muralidharan<sup>1</sup>, which utilizes a seven-segment display readout rather than discrete LEDs or lamps, this five-state detector also senses the presence of pulses and differentiates between the logic 0 and open-circuit conditions. Furthermore, provision has been made to bias the probe via its external-reference inputs, permitting it to check logic levels in circuits built with either TTL or complimentary-MOS devices.

As shown in the figure, the test signal, V<sub>in</sub>, is compared

with reference voltages  $V_{ref1}$  to  $V_{ref2}$  at comparators  $A_1$  to  $A_3$ . Voltages  $V_{ref1}$  to  $V_{ref2}$  are derived from the supply that powers the circuit under test, with  $V_{ref3}$  (developed from the probe's power source) and  $V_{ref4}$  at approximately 0.05 volt and 0.1 V below ground, respectively. Switches  $S_{1a}$  and  $S_{1b}$  at the voltage divider are used to set the required logic-level references at  $A_1$  and  $A_2$  in order to check either TTL or C-MOS circuits.

Gates  $G_1$ – $G_{13}$ , comprising the combinational-logic detector, determine  $V_{in}$ 's relation to  $V_{ref1}$ – $V_{ref4}$  and activate the appropriate segments of the display (see table).  $A_1$  and  $A_2$  are used to check for the logic I, 0, and guard-band conditions.  $A_3$  is used to detect the noconnection, or open-circuit, condition, which can be differentiated from the logic 0 state because  $V_{ref4}$  is maintained at 0.1 V below ground. Note that the logic 0 state for TTL will typically be 0.4 V and is hardly ever below 0.2 V, whereas the logic 0 state for C-MOS will be typically 0.01 V.



All-state. Logic probe having seven-segment display detects logic 1 and guard-band conditions, can differentiate between logic 0 state and open circuit, and senses a pulse train. Unit can check logic levels in circuits built with the two most popular families, C-MOS and TTL.

RESPONSE OF FIVE-STATE LOGIC PROBE																
Test vol	Itage	Display	Display Comparator						Display segments							
C-MOS*	TTL	Letter	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	а	b	С	d	g	e f					
V <sub>in</sub> < 40%	V <sub>in</sub> < 0.8	L	L	L	Н				on							
40% < V <sub>10</sub> < 60%	0.8 < V <sub>in</sub> < 2	F	L	н	Н	on				on	on					
V <sub>in</sub> > 60%	V <sub>in</sub> > 2	н	Н	Н	Н		on	on		on	permanently					
NC	NC	0	L	L	L	on	on	on	on							
pulse	pulse	Р	-	-	-	on	on			on	*% of V <sub>ref</sub>					

Switch S<sub>2</sub> must be depressed to catch any expected input pulses having a width down to 15 nanoseconds. This action resets the 555 one-shot, enabling it to override the displayed symbol with the letter P when the pulse arrives. If a train of pulses having a repetition rate greater than about 0.2 seconds (the time constant of the 555) is detected, the P will be displayed indefinitely.

With faster one-shots, pulses of 5 ns can be snared.

The probe can be powered by any dc source having a minimum voltage of 19 V. Resistor R should be selected to pass about 30 mA to the probe circuit.

#### References

1. S. Jayasimha Prasad and M. R. Muralidharan, "Logic tester has unambiguous display," Electronics, March 3, 1977, p. 117.

### Adjustable e<sup>x</sup> generator colors synthesizer's sounds

by Randall K. Kirschman Mountain View, Calif.

Providing the control signals for voltage-controlled amplifiers, oscillators and filters in order to modulate sound parameters such as loudness, pitch and timbre, this adjustable e<sup>x</sup> generator is the indispensable ingredient required to attain superior performance in a music synthesizer. Only four integrated circuits and a few

passive components are needed in the inexpensive unit, which costs under \$6.

When gated or triggered, the generator produces a waveform that passes through four states:

- An exponential attack.
- An initial decay, or fallback.
- A sustain, or steady dc level.
- A final decay, or release.

Each of these four parameters is continuously variable, so that waveforms having a large variety of shapes can be generated.

The waveforms are generated by the sequential charging and discharging of capacitor  $C_1$  (see figure). In general operation,  $C_1$  is connected to a current source or sink as required, through the 4016 complementary-MOS

12 V 12 V 12 V  $R_3$  $R_4$ LF356 WAVEFORM 10 kΩ QUITPUT R. C<sub>1</sub> 0.47 -12 V  $1 k\Omega$ R<sub>5</sub>  $R_6$ SUSTAIN  $R_2$ 12 V 10 kΩ (10 V) R<sub>7</sub>  $R_8$ M31 FINAL 10 kΩ %4001 4016 **GATE INPUT** R<sub>3</sub>, R<sub>5</sub>, R<sub>7</sub>: 1 MΩ LOG TAPER %4001 RS FLIP-FLOP 1/4 4001 (2)

Musical tint. Four-state generator provides myriad control waveforms for modulating voltage-controlled amplifiers, oscillators, and filters in a music synthesizer, and thus is useful for coloring loudness, pitch, and timbre. Attack and decay times are variable from 5 to 500 milliseconds; sustain level is adjustable from 0 to 10 volts.

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analog switches. These switches are controlled by simple logic set into action by the gate-input pulse. Triggered operation is made possible by adding a monostable multivibrator to the circuit.

In the dormant state (gate input low), analog switch C is on, switches A and B are off and the RS flip-flop formed by two 4001 NOR gates is reset. The onset of a gate pulse turns on switch A and turns C off. Consequently,  $C_1$  charges through  $R_3$  and  $R_4$ , producing the attack segment of the waveform. Note that the LM356 buffer protects  $C_1$  from excessive loading.

When the voltage across C<sub>1</sub> reaches V<sub>max</sub> (determined

by voltage divider  $R_1-R_2$ ), the LM311 comparator sets the RS flip-flop. This action in turn switches B on and A off. Thus the initial decay segment is generated as  $C_1$  discharges through  $R_5$  and  $R_6$  to reach the sustain voltage, the level of which is determined by the setting of potentiometer  $R_2$ .

Concurrently, the comparator's output has gone low, but the RS flip-flop remains set until the gate pulse moves to logic 0, at which time switch C turns on. Thus C<sub>1</sub> discharges through R<sub>7</sub> and R<sub>8</sub> to produce the final-decay portion of the wave, after which the circuit reverts to its dormant state.

### Low-loss shunt protects high-current supplies

by Roy Hartkopf and Ron Kilgour Alphington, Victoria, Australia

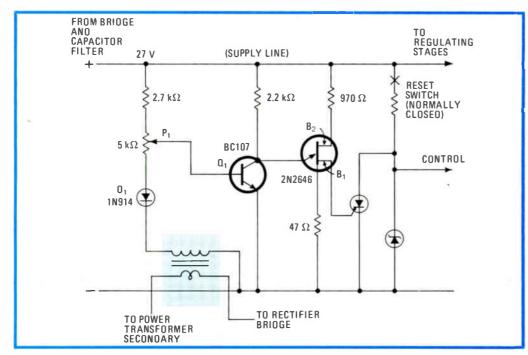
The usual method for providing short-circuit protection in low-voltage, high-current power supplies is to employ a current-sensing resistor in series with the load. Unfortunately, this scheme develops an appreciable voltage drop across the resistor when large currents flow and may consequently reduce the available output voltage to a great degree. The voltage drop can be virtually eliminated with an alternative method, shown here, which uses an audio transformer and a single-turn winding to sense the overcurrent condition at the secondary of the supply's power input transformer. Besides being inexpensive, the current sensor will react faster to overloads than some of the more conventional circuits.

As shown in the figure, current protection may be

secured for a typical 27-volt, 20-ampere supply by winding a single turn of 10-gauge wire, which is placed in series with the power transformer's secondary and the supply's rectifier bridge, onto a small audio transformer connected in the control section of the supply. During normal operation, transistor  $Q_1$  will be saturated because current is delivered to its base from the 27-v supply line. Note that the secondary of the audio transformer, in conjunction with diode  $D_1$ , will contribute a relatively small negative voltage at the summing junction of  $P_1$ .

Should the current demands increase, however, the magnitude of the negative voltage developed at the audio transformer's secondary will increase and, consistent with the setting of potentiometer  $P_1$ , pull the base-to-emitter voltage down to cut off  $Q_1$ . The 2N2646 unijunction transistor will then turn on and trigger the silicon controlled rectifier, and the control signal will be brought low. Thus this signal can be used to cut off the supply. This action will be instantaneous, occurring on the first overload cycle.

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$50 for each item published.



Current gauge. An audio transformer and a single turn of heavy-gauge wire, placed between input transformer's secondary and rectifier, give high-current supplies overload protection without introducing input-to-output voltage drop that occurs with units employing current-sensing resistors. Potentiometer P1 sets the overload point. Overload detection is instantaneous, occurring on the first positive cycle of input voltage.

# Microcomputer for emulation bares hidden buses, functions

Internal states and data paths not visible on standard pins call for special bond-out versions of modern MOS machines

by Jim Moon, Intel Corp., Santa Clara, Calif.

☐ Integration on large and very large scales is presently ushering in an era of systems on chips. Although this trend may make microprocessor users smile, it is giving headaches to some test equipment designers. What happens when the internal workings of a processor can no longer be viewed through its pins? How will it be tested? How will it be emulated?

These questions loom larger as microprocessors and single-chip microcomputers are stoked with instruction prefetch units and look-ahead queues, asynchronous communications controllers, analog converters, and hidden buses. One solution is specialized chips that provide access to these internal subsystems and buses and allow memory normally accessed internally to be located off chip. On such devices, special test and monitoring points are made available via extra bonding pads; for this reason such components are termed bond-out chips.

In early microprocessors such as the 8080, only one function or process is performed during any time period. Today's processors, however, as well as virtually all foreseeable designs provide for multiple parallel asynchronous functions (see Fig. 1). Although these functions vary according to the intended use of a particular microprocessor, they all communicate with, and alter the sequence of, operations of the central processing unit in a

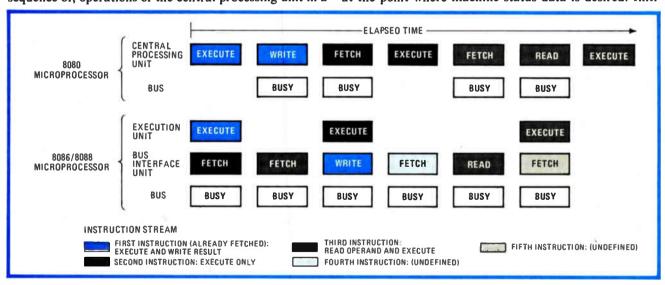
way that cannot be determined from the device's pins.

Other problems are encountered when an attempt is made to interrupt the processor's operating sequence to gather information about its state. Processor functions that either do not respond directly to a sequence of operation codes or may change state as a result of an interrogation of their status pose complex problems to the designer of the test instrumentation so essential to their successful application.

### **Architectures contrast the problems**

A relatively simple example can be put forth using the 16-bit 8086. In this microprocessor, a central processing unit communicates with program memory, data memory, and input/output ports over a well-defined bus structure. Each operation begins with the fetching of an operation code, or op code. This may be followed by additional bus cycles, depending upon the decoded instruction. Each bus cycle is accompanied by status information that, together with address and data values, fully describes the step-by-step operation of the microprocessor.

The most common way to emulate a device of this type involves a forced sequence of instructions, inserted at the point where machine-status data is desired. Initi-



1. All at once. In older microprocessors like the 8080, only one process is performed during a time interval. With today's machines and all foreseeable designs, many asynchronous functions are performed in parallel, so the chip's state cannot be read from its pins.

ated by the first op-code fetch cycle after this point has been reached, the interjected instructions place the contents of the various registers and flags on the data bus.

The transition out of the emulation mode consists of loading desired values back into each of the registers and performing an unconditional jump to the address of the next user instruction to be executed. Proper handling of the device's interrupt functions and its hold/hold-acknowledge and ready/wait signals makes proper emulation something more than trivial; but it can be accomplished with a moderate amount of external logic.

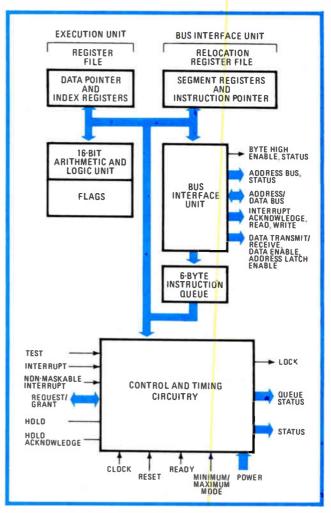
One architectural feature of the 8086, while enhancing performance significantly, also happens to create considerable difficulty in implementing an accurate real-time emulator. As shown in Fig. 2, the microprocessor consists of three asynchronous functional blocks, only one of which communicates with the external world. The execution unit takes its instructions out of the instruction queue, and the bus interface unit determines the priority of the bus activity and synchronizes the other two blocks with the outside world. Such an arrangement improves performance by optimizing the use of available bus and memory bandwidth. However, the activity at the pins of the device no longer reflects the execution unit's sequence of operations.

Instruction-prefetch bus cycles load the instruction queue a word at a time, irrespective of the address of the first byte of an op code (the only exception is the first address fetched after a jump, call, or return instruction to an odd address). Any nonsequential code execution, however, causes the queue to be emptied so that the bus cycles associated with the prefetched instructions must somehow be disregarded in determining the machine's state. The implementation of breakpoints and conditional-trace routines becomes a major problem. Although queue-status information is available on the pins while operating in the maximum mode (used in larger systems with multiple master processors), either the queue must be duplicated in external hardware or the execution address must be regenerated as each byte is taken from the queue. In either case, accurate emulation requires a substantial amount of external hardware.

### A single-chipper's needs

The 8051 single-chip microcomputer provides another point of reference. This device includes a read-only program memory, a random-access memory, an asynchronous serial port, two timer-counters, four parallel input/output ports, and a vectored interrupt structure (see "Inside the 8051 single-chip microcomputer," p. 128). All of this is on chip. The device functions either in a single-chip mode, in which all program and data memory transfers are performed internally, or in memory-intensive applications, where up to 65-K bytes of program memory and the same amount of data memory may be addressed off chip.

Even in the 8051's most basic single-chip mode of operation, several emulation problems become immediately apparent. First, software debugging demands the use of external random-access memory for code storage. With the 8051 two I/O ports (0 and 2) are used to implement the external memory bus, which means that



2. Three in one. The 8086 microprocessor is composed of three independent function blocks: the execution unit, instruction queue, and bus interface unit. This partitioning makes emulation difficult because only one of the sections talks to the outside world.

these may not be referenced in the user's program. Second, an instruction sequence to gain control of the 8051 for emulation must limit its use of interrupts to the low-priority level, reserving the higher level and one of the external interrupt inputs for emulator use. Finally, the inability to control timers and serial-port functions during an emulation break would be severely restrictive.

The inability to readily determine device operation at the pins of modern components like the 8051 points to a need for extraordinary solutions to the problems of advanced microprocessor system testing. At the same time, the increased complexity of system applications suggests a reevaluation of those capabilities considered to be essential for effective microprocessor diagnosis.

The functions to be provided through in-circuit emulation show where microprocessor system testing is headed. First of all, the instrument will provide accurate, real-time emulation, where real-time means an exact duplication of the operation of the target processor.

The ability to predict and control the operation of asynchronous functions such as serial ports, timers, and counters during an emulation break is possible at the discretion of the user, since the desired mode of opera-

### Inside the 8051 single-chip microcomputer

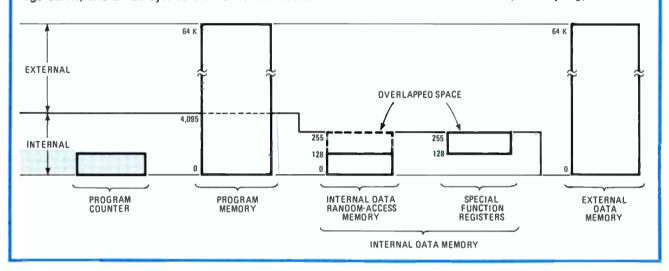
The 8051 contains 4-K bytes of program read-only memory, a 128-byte random-access memory, 32 I/O lines, two 16-bit counter/timers, a five-source, two-priority interrupt structure, a serial communications port that can handle multiprocessing, and an on-chip clock and oscillator. An 8051 system can be expanded with external memories and peripheral chips. In the 8051 series, the 8751 replaces the 8051's mask-programmable ROM with an erasable programmable ROM, and the 8031 contains no internal program memory.

The architecture of the 8051 is based on the 8048's, but enhanced with direct addressing, four eight-register storage banks, and a 128-byte stack. Instructions added to

the 8048's repertoire include those for nonpaged jumps and those to multiply, divide, subtract, and compare. Most instructions occupy 1 or 2 bytes and, with a 12-megahertz crystal, execute in 1 microsecond.

Operands for the 8051 can reside in four spaces: the 64-K bytes each of program memory and external data memory, a 384-byte internal data memory, or a 16-bit program counter. Internal data memory is further split into a RAM and special function registers that contain the memory-mapped I/O ports, timers, etc.

The 8051 has extensive bit-manipulation capabilities through an internal Boolean processor. It has its own instruction set and accumulator (the carry flag).



tion will depend upon the application and the test.

Finally, the user is relieved of the tedium of translating addresses and data into program listings. Symbolic references are used and programs and data are displayed in symbolic form to save engineering time.

These goals require a special version of the processor to be emulated; the 8051 bond-out chip is such a device. Housed in a 64-pin leadless carrier, the bond-out chip has no internal read-only memory. Addresses and data are transferred between the processor and external memory by way of a specialized bus that is brought out via the extra bonding pads. The need for off-chip buffering of this bus required close attention to a number of timing parameters to insure that the bond-out version does not differ from the way a normal 8051 accesses its program ROM. As shown in Fig. 3, the bond-out chip includes special-purpose inputs and registers to control the serial port, timers, and interrupts during an emulation break.

Two special-purpose registers provide a means to determine the processor's state without compromising data integrity. A general-purpose communication register located at address 9E<sub>16</sub>, unused in the 8051, permits the contents of the accumulator, flags, and registers to be read from the processor without affecting the I/O-port pins. The second register, at address 9F<sub>16</sub>, supplies the status of interrupts in progress, the specific interrupting device, and its priority level. These registers are accessed via special control pins that permit their contents to

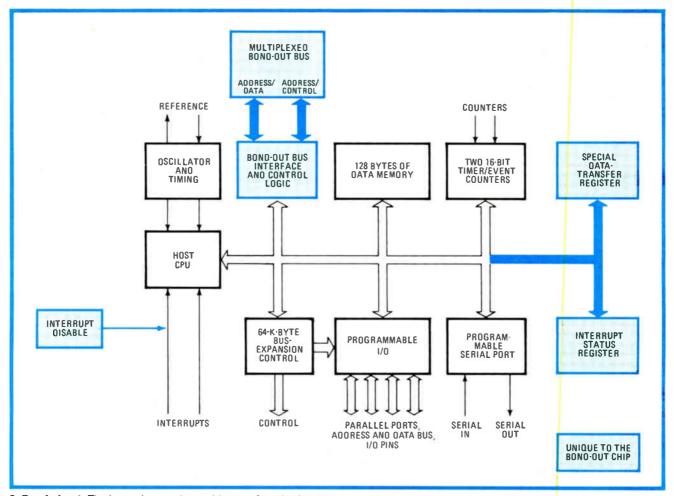
appear on the bond-out address and data buses.

Control inputs are provided to stop the timer-counters and to inhibit the normal response to an interrupt request. Memory-mapping features of the in-circuit emulator are supported through a control input that functions in accordance with the normal internal-to-external address boundary at 4-K bytes. This feature permits the mapping of program memory that would normally be accessed via  $P_0$  and  $P_2$  port pins into the emulator via the bond-out address and data buses.

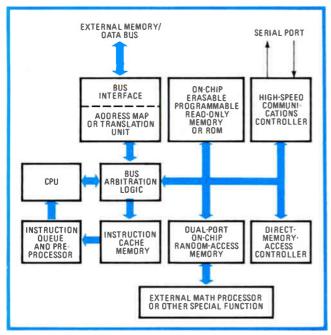
Bond-out techniques, although costly to develop, provide a diagnostic tool that emulates the target processor and circumvents the functional problems associated with emulation breaks. The pins of the bond-out chip that are identical in function and timing to those of the target processor interface directly with the system designed around the part. No additional timing or buffer elements need be used, so the speed degradation inherent with such devices is avoided, and load and drive requirements are identical.

### What the future holds

Future microprocessors will garner more on-chip functions (Fig. 4). In addition to asynchronous functions such as direct-memory-access channel controllers, serial-I/O interfaces, and arithmetic processors, more on-chip hardware will be dedicated to specialized operating system and algorithmic requirements.



3. Bonded out. The internal memories and buses of single-chip microcomputers are especially difficult to get at for test purposes. For full emulation of the 8051, a special version was developed. It has inputs and registers to control I/O ports, timers, and interrupts.



**4. Chip of the future.** In future processors, particularly single-chip units, added functions such as cache memories, preprocessors, and I/O controllers will compound the problems of in-circuit emulation, making bond-out versions necessary for system development.

Single-chip processors will continue to expand their on-chip memory. I/O functions will grow in scope and complexity; analog-to-digital and digital-to-analog converters as well as serial communications controllers are among the more obvious additions. The 8022 single-chip microcomputer, with its on-chip a-d converter and its inability to address external memory, also warranted a bond-out version, which will be introduced soon. Time-critical relationships between I/O functions and software execution require test systems that can provide the necessary stimulus and measurement capabilities.

Processors with 16-bit and wider buses will undergo the architectural evolution that has already taken place in the minicomputer and mainframe domain. On-chip cache memories, instruction preprocessors, and protection hardware for multitasking environments will create problems in the design of instrumentation to support hardware and software integration, with the result that software diagnostic aids alone will not suffice.

The chip maker should address the testing and diagnostic needs of a processor from concept through volume production. Many problems will only be solved from within the component. Many of the necessary diagnostic features will serve little or no purpose in applications and, in fact, would only create another level of testing complexity if used in the applications.

# LSI trio calls the tunes in microcomputer's CPU

Bus duo and chip combining programmable logic and read-only memory give LSI-11/23 speed and expandable microinstruction store

by Duane Dickhut, Burt Hashizume, and William N. Johnson, Digital Equipment Corp., Maynard, Mass.

☐ How best to apply large-scale integration to an existing computer architecture is a continuing challenge in the industry. Reduced size, power consumption, and costs are the rewards, but the designer faces the risks of reduced flexibilty to make future enhancements.

The LSI-11/23, the latest microcomputer member of the PDP-11 family, resolves the problem by using a multiple-chip central processing unit. Rather than include the microinstructions and the bus that transports them on a single chip as one-chip CPUs do, this multichip approach makes the bus accessible and the number of microinstructions expandable.

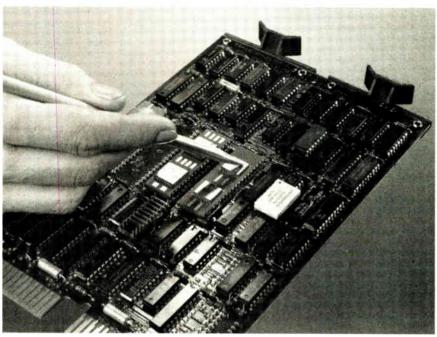
The flexibility inherent in an expandable number of microinstructions makes microprogramming easier and makes it possible for these chips to be used also for other PDP-11 machines and such non-PDP-11 products as input/output controllers.

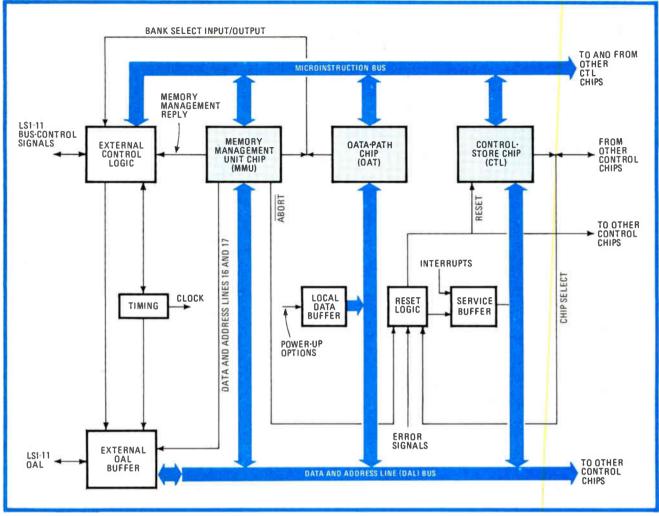
In addition to its flexibility, the LSI-11/23 is powerful. Though it costs about as much as the entry-level LSI-11 microcomputer, the LSI-11/23 has about two and a half times the execution speed and offers the functions and performance of the PDP-11/34 mid-range minicomputer [Electronics, March 15, 1979, p. 88].

1. Side by side. The three chip types that form the heart of the LSI-11/23 microcomputer are packaged in a novel manner: the data-path chip is mounted on the same DIP as the control-store chip, to which the pen points, and immediately to the left of this package two additional control-store chips share another DIP. The memory management unit (hidden) resides by itself.

The multichip processor keeps the LSI-11/23 fully software-compatible with the other members of the PDP-11 family, ranging from the LSI-11 at the low end to the PDP-11/70 at the top. In particular, the LSI-11/23 uses the same electrical bus structure as the LSI-11. Therefore it can directly replace the centralprocessing-unit module in the LSI-11-based PDP-11/03 microcomputer and operate with the same associated hardware. Furthermore, it implements the entire basic PDP-11 instruction set. It uses PDP-11/34-type memory management and its hardware supports a physical address up to 18 bits long. This compatibility permits the RSX-11M timesharing operating system and PDP-11 application software to run unchanged on the LSI-11/23 microcomputer. And because its microcode is expandable, other PDP-11 instruction sets such as the FP-11 floating-point operations and business-oriented features like string and decimal operations can be added.

The central processing unit of the LSI-11/23 is mounted on a single 5-by-8-inch printed-circuit board (Fig. 1). At its heart is a set of three custom n-channel MOS LSI chips: a data-path (DAT) chip, a control-store (CTL) chip, and a memory management unit (MMU).





2. Accessible communications. A major advantage of the multiple-chip approach is the accessibility of the microinstruction bus (MIB), which lets up to 32 control-store chips be used. The data- and address-line (DAL) bus also handles the interrupt and abort information.

The data-path chip handles math and logic functions, address and data-bus transfers, and most interchip communications. It contains 16-bit PDP-11 registers, 16-bit temporary (scratch-pad) registers, the arithmetic and logic unit (ALU), and conditional branching logic.

The memory management unit provides memory management registers and memory relocation logic that are functionally identical to those on the PDP-11/34. It also holds the FP-11 floating-point register set that is functionally identical to those on the PDP-11/34, PDP-11/60, and PDP-11/70 minicomputers.

The control-store chip contains a unique combination of mask-programmable read-only memory that stores the control microcode (also known as microstore) and programmable logic arrays that act as the microprogram sequence logic. It holds 552 25-bit words. These chips can be cascaded up to an architectural maximum of 32, each containing entirely independent microprograms. The LSI-11/23's maximum microstore capacity is thus 552×32, or 17,664 words.

Each CTL chip is responsible for accessing only its local microstorage. Only one CTL chip may be active at any given time, and jump microinstructions transfer microprogram control between CTL chips. With all nec-

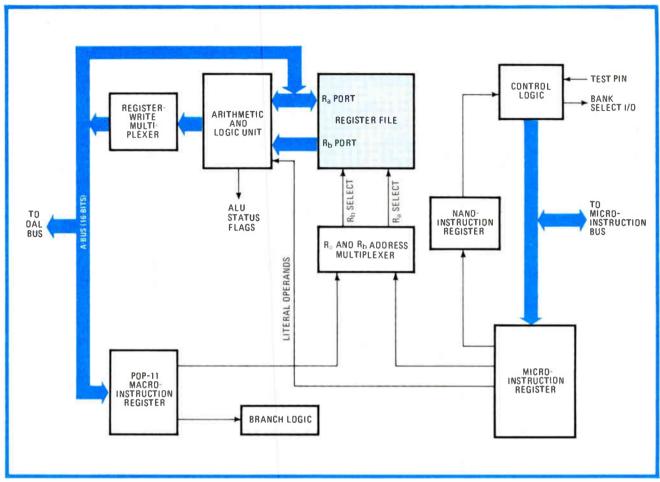
essary control functions on these self-contained chips, microstore extension can be achieved without any change to the DAT and MMU chips or to CTL chips already on the board.

#### **Packaging**

As seen in Fig. 1, the DAT and the first CTL chip are mounted side by side on a 40-pin hybrid dual in-line package located at the center of the CPU board. The MMU chip is mounted by itself in a single DIP at the left side of the board. Just to the left of the DAT-CTL package, a similar dual-chip DIP houses two more CTL chips that contain the optional FP-11 floating-point instructions.

These chips communicate with each other and with surrounding logic on the CPU board over two buses—a 16-bit microinstruction bus (MIB) and a 16-bit data- and address-line (DAL) bus, as shown in Fig. 2. The microinstruction bus transfers the 16-bit microinstruction portion of the 25-bit microcode word and control information. The DAL bus communicates interrupt and abort information, as well as data and addresses.

Both the MIB and the DAL bus are bidirectional and time-division multiplexed. Transmission of different



3. Two paths are better than one. The data-path chip is built around a 16-bit arithmetic and logic unit and a dual-ported register bank. Because of the two ports, any register can be either the source or the destination of operands, thus cutting execution time.

types of information is assigned to particular half cycles, either the positive phase  $(\phi)$  or the negative phase  $(\phi)$  of the 288-nanosecond LSI-11/23 microcycle. The MIB uses the  $\overline{\phi}$  half cycle to transfer a microinstruction from the active CTL chip to all other chips. Then, during the  $\phi$  half of the microcycle, the MIB transfers control signals associated with this microinstruction from the DAT to the MMU and other CTL chips, as well as to the other logic on the CPU board, and to the hardware that interfaces to the outside world.

The DAL bus can be used for a variety of data transfers during the  $\phi$  half-cycle. Floating-point data can be transferred either way between the DAT and the MMU, microprogram subroutine return data can be moved from the DAT to the CTL, or data from the local buffer can be moved into the DAT. In addition, the DAL bus can be called upon during this half-cycle to transport virtual addresses from the DAT to the MMU and the outside world, to accept macroinstructions from the outside world, or to move data between the outside world and the chips.

In the  $\overline{\phi}$  half-cycle, however, the DAL bus restricts itself either to transferring physical addresses from the MMU to the outside world or to moving service data from the outside world into the CTL. The service data includes synchronous interrupts (such as those generated by peripherals, the ac power-failure monitor, a halt switch,

and the real-time clock), as well as asynchronous events like memory management abort, parity error, bus time-out trap, and illegal macroinstruction trap.

When handling macroinstructions during the  $\phi$  half-cycle, the DAL bus gives copies of the current macroinstruction to the DAT, MMU, and every CTL—not just the currently active CTL. Each chip then executes its particular functions, decoding the necessary data from its PDP-11 macroinstruction register. This technique of transferring the macroinstruction initially to all chips, whether they need it or not, is used because it is less time-consuming than the alternative approach of transferring a single copy of the PDP-11 macroinstruction into the DAT and then sending copies of that to other chips in sequence as needed. This design tradeoff in the LSI-11/23 has reduced execution time but added to each chip the hardware needed to eliminate sequential transfer of macroinstructions.

### Multiplexing and LSI packaging

The purpose of time-division-multiplexing two types of function on both the MIB and the DAL bus was to make the size of the microstore extendible in a compact, convenient, and economical fashion—that is, fitting the chips into a 40-pin DIP, the familiar hardware configuration of single-chip processors.

Without time-division multiplexing, the DAT and CTL

chips would each have had to have four 16-bit buses—one for microinstructions, another for control signals, a third for data and address transmission, and one more for service signals—and 64 pins. Moreover, additional pins would have been needed for extra control signals, plus power and ground, bringing the total to more than the 64 pins that is the current maximum for DIPs.

Reduction of the pin count from what would have been more than 64 to fewer than 40 through time-division multiplexing reduced the cost of both the integrated circuits and the chip packages. It was possible to mount two 40-pad chips on a single ceramic substrate forming a 40-pin dual-in-line package, whereas it is not practicable at present to mount and connect two 64-pad ICs on a 64-pin DIP.

#### Microinstruction set

Key to the operation of these chips are the microinstructions that perform the tasks indicated by the macroinstructions coming from the program. Each 25-bit microcode word consists of 16 bits of microinstruction and 9 bits of sequencing data, commonly called a next address. The currently active CTL chip transmits the 16-bit microinstructions to the DAT, MMU, and other CTL chips via the MIB. Each chip decodes certain fields within the 16-bit microinstruction to determine its operation, if any.

There are 63 LS1-11/23 microinstructions that fall into seven major classes. One of the most commonly used classes is operate, which consists of an 8-bit operation code (op code) field, a 4-bit operand-source specifier, and a 4-bit operand-source or -destination specifier. Each of the 4-bit operand specifier fields can select any one of 16 registers in the DAT register file. Each of the 31 operate instructions has four variations that act on different types of data, and 22 of the instructions are identical to PDP-11 macroinstructions in symmetry, operation, and condition-flag setting. These microinstructions include such operations as logical shifts and rotates, arithmetic shifts, arithmetic and Boolean operations, byte-word moves, and bit testing and setting.

The six literal microinstructions, each of which contains 8 bits of immediate data that are used as the source operand, include such operations as load, compare, and add. The nine address instructions specify the type of bus cycle—for example, read-only or read-modify-write—and select the source register in the DAT for the virtual address.

The four input-control microinstructions receive macroinstructions, peripheral interrupt vectors, and operand data from the outside world and transfer floating-point data from the MMU to the DAT chip. On the other hand, the four output-control microinstructions transmit data from the DAT to the CTL, the MMU, and the outside world. These transfers include floating-point data from the DAT to the MMU and microprogram subroutine return information from the DAT to the CTL.

There is only one unconditional-jump microinstruction, and it transfers control from the currently active CTL to any other of the up to 32 chips. Finally, the eight conditional jumps make decisions on the basis of ALU output data or PDP-11 condition flags. The 8-bit jump

address field contains the branch target address within the currently active CTL chip.

Built around a 16-bit ALU and a dual-ported register bank (Fig. 3), the data-path chip is central to the LSI-11/23. This register bank contains 10 PDP-11 general-purpose registers, including registers R0 to R5, a kernel-mode stack pointer (KSP), a supervisor-mode stack pointer (SSP), a user-mode stack pointer (USP), and a program counter (PC). In addition, there are the processor status-word (PSW) register and five working registers for scratch-pad storage for microprogramming complex operations.

Since the register file in the DAT is dual-ported, data in a given register can be considered as either a source or a destination operand. Whereas the R<sub>b</sub> port can be used only as a read path (source), the bidirectional R<sub>a</sub> port can be used for both read and write (source and destination) access. In implementing the PDP-11 instruction set, this dual-ported arrangement cuts execution time and simplifies chip design by reducing the number of registers in the data path needed for emulating macroinstructions.

The microinstruction register in the DAT receives the active inicroinstruction over the MIB from the CTL. The PDP-11 macroinstruction register (at the bottom right of Fig. 3) receives the macroinstruction from the currently executing PDP-11 macroprogram over the DAL bus from the main memory. When the current macroinstruction is a PDP-11 branch instruction, this register is used by the special branch logic to test the PSW pondition codes in the DAT register file.

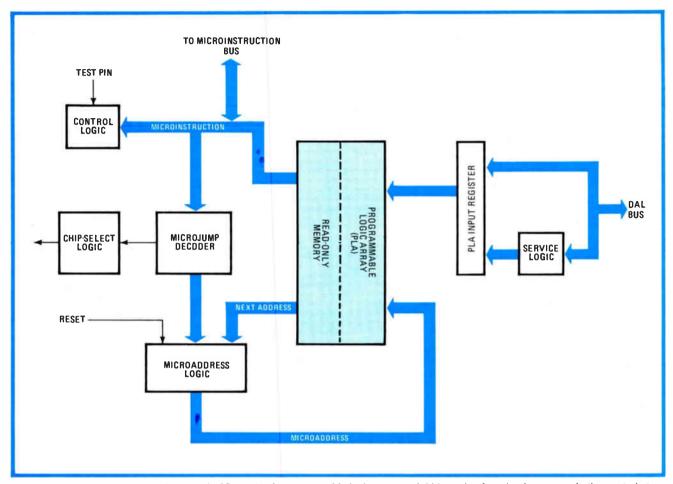
### In control

The contents of the microinstruction register are used by the control logic to generate control signals. These signals are then transmitted over the MIB during the  $\phi$  half-cycle to the CTL, the MMU, and the outside world. In this process, the vertically encoded microinstruction received from the CTL microstore is translated into horizontal microinstructions, called nanoinstructions, that can be used directly to control the data paths and logical functions.

The R<sub>a</sub> and R<sub>b</sub> address multiplexer permits the register specifier portions of the microinstruction to access directly any one of the 16 registers in the DAT register file. These specifier portions of an instruction can be set to select particular registers by means of 3-bit source-register and destination-register specifiers included in the macroinstruction. The ability to specify source and destination addresses for the microprogram avoids the need for additional chip hardware and extra execution time to calculate the address. The older LSI-11 microprocessor, for example, uses an additional microcycle to perform this task.

The 16-bit outputs of the R<sub>a</sub> and R<sub>b</sub> ports, as well as literal operands from the microinstruction register, enter the ALU. The ALU performs binary and binary-coded-decimal arithmetic and Boolean operations as determined by the microinstruction op codes. A set of status flags in the ALU are updated every microcycle and can be tested by conditional-jump microinstructions.

From the ALU the 16-bit output goes into a register-



4. New combo. The novel combination of 138 words of programmable logic array and 414 words of read-only memory in the control-store chip increases the performance of the LSI-11/23 over the LSI-11, since the CTL directly handles the microcomputer's microcode sequencing.

write multiplexer, which selects either the ALU results or data from outside the CPU for transfer to the R<sub>a</sub> port over the bidirectional A-bus. The data is then written back into the register file at the location indicated by the destination specifier in the microinstruction. The A-bus connection to the R<sub>a</sub> port is also used to transmit data from the register file to the outside world and to load the PDP-11 macroinstruction register.

Operands are read out of the DAT register file and latched into the ALU during the  $\phi$  half-cycle. The ALU operation is completed and the result is written back into the register file through the  $R_a$  port during the  $\overline{\phi}$  half-cycle. Therefore, two 16-bit numbers can be fetched, added, and placed back into the destination register file within one microcycle.

### The CTL chip

The control-store chip holds the microcode that directs the operation of the data-path chip. The microstore in this chip (Fig. 4) is a novel combination of 138 words of a programmable logic array (PLA) and 414 words of read-only memory (ROM). The PLA structure is designed for efficient decoding of PDP-11 macroinstructions, and the ROM is used for efficient storage of in-line microcode. Input data into the PLA consists of 16 bits from the PLA input register, which can be either a macroinstruction or any type of microsequencing information, plus

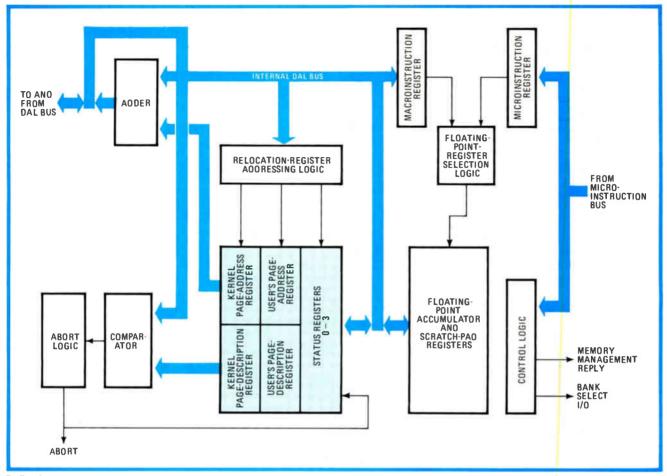
the 9-bit-long next address. The next address can invoke either PLA locations for decision making or ROM locations for in-line microinstructions.

Integration of the PLA and ROM into a single semiconductor microstore provides two valuable characteristics. First, the output of the PLA is itself an executable microinstruction, rather than simply an address. Second, PLA terms and ROM words may be mixed in any order because the next-address fields permit transferring within and between PLA and ROM without a time penalty. In the customary two-tier control-store structure in many microprocessor designs, on the other hand, the macroinstruction is decoded in the PLA in order to generate the starting address of the instruction's execution microcode stored in a separate control store. There may be several stages of mapping PLA or ROM for deciding addressing modes in addition to the op codes.

An outstanding advantage of these characteristics is the elimination of the need to wait for dispatching. The first microinstruction in the appropriate addressing or emulation sequence is immediately executed. And since most of the PDP-11 arithmetic and logic macroinstructions are emulated by matching microinstructions, they can be executed in a single microcycle following macroinstruction fetching without any decoding overhead.

System interrupts, line-clock interrupts, bus errors, and memory management aborts occur asynchronously,

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5. Registers and memory. Two sets of registers in the memory management unit keep the user and system modes of operation separate when translating virtual-memory to real-memory addresses. Also on the chip are the unrelated floating-point accumulators.

but many of them must be tested at the end of each puter's memory management mechanism. instruction execution. The LSI-11/23 uses the PLA structure to test for these interrupts, again without a time penalty. While the last microinstruction of a macroinstruction routine is being executed, the PLA input register is loaded with the interrupt information. If interrupts are pending, the PLA decodes the interrupt requests and generates the first service microinstruction in the next microcycle. If none is pending, the PLA translation instead generates the first microinstruction in the next macroinstruction routine.

In fact, the major reason for the increased performance of the LSI-11/23 over the LSI-11 is the saving in execution time within the integrated PLA and ROM microstore in the CTL.

### The MMU chip

The virtual address translation and memory management function of the MMU chip (Fig. 5) is based on information contained in two sets of page-address registers (PARs) and page-description registers (PDRs). One. called the kernel set, is for the exclusive use of the operating system and has unrestricted access to all CPU functions. The user's set, however, has restricted access and is for the application program. In addition, there are four status registers (SR0-SR3) that are functionally equivalent to those used in the PDP-11/34 minicom-

The active MMU register set—user PAR and user PDR or kernel PAR and kernel PDR—is defined by the 2-bit mode specifier in the PSW in the DAT's register file. The top 3 bits of the virtual address received over the DAL bus determine which one of eight PARs or PDRs for each mode is to be used.

### Addresses

The contents of the selected PAR is one input to an adder; the remaining bits of the virtual address from the DAL bus are the other. The adder combines bits 6 to 12 of the virtual address to the 12-bit PAR term to form bits 6 to 17 of the physical address. Bits 0 to 5 of the physical address are identical to bits 0 to 5 of the virtual address. The address translation takes just one microcycle—the virtual address is transmitted back to the DAL bus by the adder during  $\phi$  in the same microcycle.

Information in the PDRs, together with the comparator, is used to implement memory protection features. The four status registers capture information when there is an abort caused by violation of the protection rules.

Although they are unrelated to its basic function, the MMU also provides storage space for eight 64-bit floating-point accumulators. A particular accumulator is selected by a combination of the input and output microinstructions and by the PDP-11 macroinstruction.

### **Engineer's notebook**

### MOS FETs sequence power to sensitive op amps

by J. E. Buchanan
Westinghouse Electric Corp., Baltimore, Md.

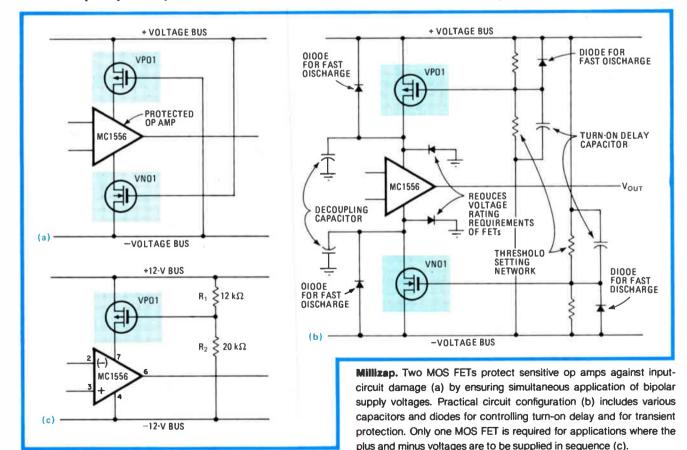
Though hardly mentioned, even in application notes, operational amplifiers with double-diffused input devices often require—like many other integrated circuits powered by bipolar supplies—the simultaneous or sequential application of positive and negative voltage. This is to prevent device degradation or burnout due to forward biasing of various input-circuit diodes and transistors. One simple and low-cost means to meet these requirements can be achieved by using MOS field-effect transistors, which have high input impedance and low output impedance, to apply power to one terminal of the op amp after sensing the presence of power at the opposite terminal. Such an arrangement is not only more reliable than any using double-pole relays, but uses less power and takes up less space as well.

The basic circuit shown in (a) ensures the simultaneous application of plus and minus voltage to a MC1556 op amp. The p-channel, enhancement-mode

MOS FET in the positive supply line requires a negative gate voltage to turn on and the n-channel unit in the negative supply line requires a positive gate voltage to turn on. Therefore, this cross-coupled configuration does not allow the application of positive voltage unless a negative voltage is present, and vice versa. If one supply fails, power applied from the other supply is removed. The FETs are selected such that the threshold, or turn-on, voltage is roughly equal to the difference between the positive and negative supply rails. Thus both supplies must be near their rated values before either FET can turn on.

In actual operation, the gates of the FETs will have to be biased via resistive voltage dividers in order to match their individual threshold requirements, and other supporting circuitry is needed as well, as shown in (b). The addition of a capacitor at the divider will allow the turn-on time to be selected. The capacitor can also be used to compensate for a relatively slower FET in one leg or for differences in supply turn-on times.

The delay in applying the voltages to the op amp is determined by the RC time constant formed by the equivalent resistance of the divider and the turn-on delay. The decoupling capacitor is also useful for noise suppression and in supplying peak (transient) load currents. A diode may be required across the MOS switch, as shown, to ensure the rapid discharge of the switched



nodes when the system's supplies are turned off.

A basic circuit that will apply bipolar voltages in sequence is shown in (c). This circuit ensures that the positive supply is not turned on unless the negative supply is established. A similar arrangement is used for positive-supply predominance, except that an n-channel device is placed in the negative-supply lead.

Use of the Supertex VP01 p-channel MOS FET (and the n-channel VN01) is ideal for all applications. They have a specified on-resistance of about 10 ohms, which is

low enough to ensure that there is little voltage drop across them when they are on; in this case, the drop is only 50 mV for a supply current of 0.5 mA, and it will not increase greatly despite rather heavy current flow.

Again, voltage divider  $R_1$ - $R_2$  is selected so that the VP01 will be fully on with minimum operational supply levels. Circuitry as seen in (b) is also needed.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.

### Calculator notes

### TI-59 MOS FET program aids LSI designers

by Ray Pinkham Texas Instruments Inc., Houston

Designers of large-scale integrated circuits who use this TI-59 program to find the dc response of many simple networks built with MOS transistors can avoid having to wait for a computer-aided design system that is down or has long job-turnaround times. The program is fast and easy to use.

Given the modeled devices' semiconductor constants, operating potentials, and the circuit's configuration, the program finds the drain current through each MOS FET operating in the linear region from:

$$I_{D} = \frac{k_{P}W_{\text{eff}}\alpha[2(V_{GS} - V_{T})V_{DS} - \alpha(V_{DS})^{2}]}{L_{\text{eff}}[1 + \theta(V_{GS} - V_{T})]}$$

or, for saturated operation, where  $V_{DS} \ge (V_{GS} - V_T)/\alpha$ , it automatically selects:

$$I_{D} = \frac{k_{P}W_{\text{eff}}(V_{GS} - V_{T})^{2}\{1 + \lambda \left[V_{DS} - (V_{GS} - V_{T})/\alpha\right]\}}{L_{\text{eff}}\left[1 + \theta(V_{GS} - V_{T})\right]}$$

to calculate drain current, where:

 $V_{DS}$  = average drain-source voltage

 $V_{GS}$  = average gate-source voltage

 $k_P = gain factor$ 

W<sub>eff</sub> = effective channel width

L<sub>eff</sub> = effective channel length

 $\theta$  = mobility reduction factor due to normal field

 $\alpha$  = pinch-off modulation value due to normal field

 $\lambda$  = channel-length modulation value due to drain potential

 $V_T$  = threshold voltage, which is given by:

$$V_T = V_{T0} + BE[(2\phi_F - V_{BS})^{1/2} - (2\phi_F)^{1/2}]$$

where

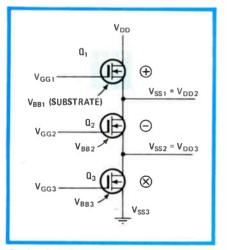
V<sub>BS</sub> = substrate-to-source voltage

 $V_{T0}$  = threshold voltage with  $V_{BS}$  = 0

BE = body-effect or back gate-bias coefficient

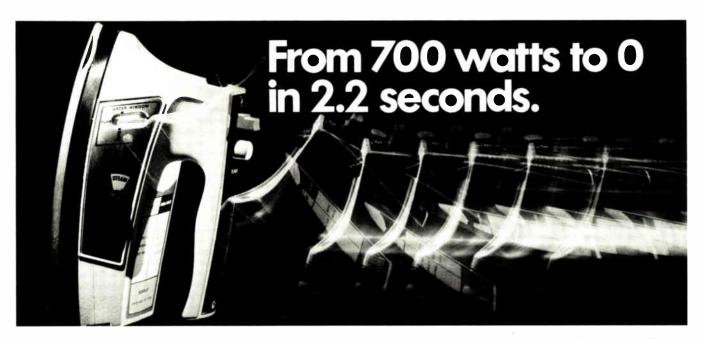
 $\phi_{\rm F}$  = Fermi potential of substrate at equilibrium

The device parameters for up to three separate modeled MOS FETs can be loaded into memory locations 30 through 60 (see table) and recorded on a magnetic card using memory bank three. Later, any one of the three models can be called and loaded back into memory with three keystrokes. Numerous NOP (no operation) instructions also appear throughout the program to provide for future program expansion. Parameters can be added to describe the behavior of devices with ever-decreasing channel widths and lengths. DO loops can also be inserted to iterate executions of the  $I_{DS}$  calculation to achieve a given  $I_{D}$  for specified gate, source, and drain supply voltages ( $V_{GG}$ ,  $V_{SS}$ , and  $V_{DD}$ ) or channel width W or length L, where  $W_{eff} = W - WR$ , where WR is the channel-width reduction value. Similarly, LR is the



THE STATE OF	MEMORY LOCATIONS OF MOS FET PARAMETERS												
Parameter	Q <sub>1</sub> (label: +)	Q₂ (label: −)	Q <sub>3</sub> (label: X)										
L eff	30	38	46										
Кp	31	39	47										
V <sub>TO</sub>	32	40	48										
λ	33	41	49										
α	34	42	50										
θ	35	43	51										
BE	36	44	52										
* Ø F	54	54	54										
*WR	55	55	55										
*LR	56	56	56										
		*assumed the	e same for all devices										

**Drained.** TI-59 program finds current flowing through each of up to three MOS transistor stages, given their semiconductor constants and operating potentials. Device parameters may be stored in memory (see table) in order to quickly expedite design changes.



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Circle 139 on reader service card

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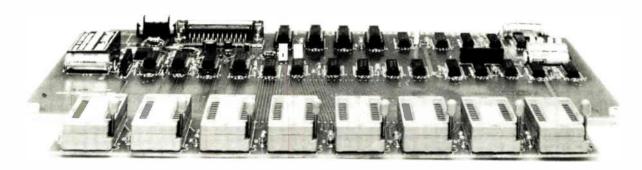


## THE ZENDEX Model ZX-908 PROGRAMMER FOR MDS or SBC OPERATION

Hardware compatible to MDS-UPP-103 via 25 pin cable. Software compatible to ISIS-UPM

Multibus\* edge connector allows use in SBC-80 systems. Simple I/O port interface with examples in Manual provided.

For 2716, 2732 or 2732A model EPROMs, the ZX-908 can program up to 16K Bytes of storage in one operation. Zero-Insertion-Force sockets are provided for quick insertion/withdrawal.



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#### TI 59 PRINTER LISTING MOS FET STAGE ANALYSIS

Loc	Key	Loc	Key	1.00	Kou	Loo	Key	Loc	Kov	Lon	Kou	Loo	Kon	Lon	Key	1.00	Key
		_	NOP	Loc	Key 09	153	_	204	Key	Loc	Key	Loc	Key	Loc	Key	Loc	
000	LBL A	051 052	RTN	102 103	RTN	154	NOP LBL	204	NOP	255 256	NOP	306 307	RCL	357 358	SBR GTO	408 409	STO 06
002	STO	053	LBL	104	LBL	155	IXI	206	RCL	257	NOP	308	23	359	RTN	410	RCL
003	00	054	E	105	X <sup>2</sup>	156	RCL	207	09	258	NOP	309	÷.	360	NOP	411	48
004	RCL 00	055 056	STO 04	106 107	STO	157	07	208	STO 21	259	X≑T	310 311	RCL	361	LBL	412 413	SBR
006	-	057	SBR	108	10 RTN	158 159	RCL	209 210	NOP	260 261	RCL 18	312	21 1	362 363	RCL	414	C' RCL
007	RCL	058	00	109	LBL	160	11	211	NOP	262	ĞĒ	313	ĺ	364	38	415	49
800	13	059	29	110	√X	161	X	212	RCL	263	)	314	)	365	STO	416	STO
009	≂ RTN	060	SBR 00	111	STO 11	162	(	213	06	264	2	315	=	366	01	417	08
011	LBL	061 062	42	112 113	SBR	163 164	2	214 215	X	265 266	X RCL	316 317	NOP NOP	367 368	RCL 39	418	RCL 50
012	В	063	SBR	114	IXI	165	X	216	RCL	267	23	318	NOP	369	STO	420	STO
013	STO	064	00	115	RTN	166	RCL	217	00	268	×	319	NOP	370	06	421	09
014	01	065	71	116.	LBL	167	12	218	-	269	RCL	320	RTN	371	RCL	422	RCL
015	RCL 01	066 067	RTN	117 118	1/X STO	168 169	RCL	219 220	RCL 13	270 271	18	321 322	LBL +	372 373	40 SBR	423 424	51 STO
017		068	A'	119	12	170	20	221	ا ز	272	RCL	323	RCL	374	C'	425	10
018	RCL	069	STO	120	SBR	171	)	222	÷	273	21	324	30	375	RCL	426	RCL
019	14	070 071	05	121 122	IXI	172	√× _	223	(	274	X	325	STO	376	41	427	52
020	RTN	071	RCL 05	123	RTN	173 174	(	224 225	RCL 01	275 276	RCL 18	326 327	01 RCL	377 378	STO 08	428 429	SBR √X
022	NOP	073	-	124	RCL	175	2	226	_	277	X <sup>2</sup>	328	31	379	RCL	430	NÔP
023	NOP	074	RCL	125	STO	176	X	227	RCL	278	= 1	329	STO	380	42	431	NOP
024	NOP LBL	075 076	04	126 127	13 SBR	177 178	RCL 12	228 229	14	279	X	330	06	381	STO	432	NOP
026	C	077	STO	128	00	179	)	230	NOP	280 281	RCL 21	331 332	RCL 32	382 383	09 RCL	433 434	NOP SBR
027	STO	078	20	129	04	180	ýχ	231	NOP	282	X	333	SBR	384	43	435	GTO
028	02	079	SBR	130	RTN	181	)	232	NOP	283	RCL	334	C'	385	STO	436	RTN
029	RCL 02	080 081	IXI RTN	131 132	LBL	182 183	STO	233 234	÷ (	284 285	24	335 336	RCL 33	386 387	10 NOP	437 438	NOP
031	-	082	LBL	133	STO	184	22	235	ì	286	RTN	337	STO	388	RCL	438	LBL GTO
032	RCL	083	B'	134	14	185	RTN	236	+	287	LBL	338	08	389	44	440	RCL
033	04	084 085	STO 06	135	SBR	186	NOP	237	RCL	288	)	339	RCL	390	SBR	441	54
035	STO	086	RTN	136 137	00 15	187 188	NOP NOP	238 239	10 X	289 290	RCL 24	340 341	34 STO	391 392	√X NOP	442 443	SBR 1/X
036	17	087	LBL	138	RTN	189	NOP	240	RCL	291	X	342	09	393	NOP	444	RCL
037	RTN	088	C,	139	NOP	190	NOP	241	23	292	RCL	343	RCL	394	NOP	445	55
038	LBL D	089 090	STO 07	140 141	NOP NOP	191 192	NOP	242	)	293 294	23 X <sup>2</sup>	344	35	395	NOP	446	STO
040	STO	090	SBR	142	NOP	193	NOP NOP	243 244	STO	294	X	345 346	STO 10	396 397	SBR GTO	447 448	13 RCL
041	03	092	IXI	143	NOP	194	LBL	245	24	296	- î	347	RCL	398	RTN	449	56
042	RCL	093	RTN	144	NOP	195	CLR	246	RCL	297	1	348	36	<b>39</b> 9	NOP	450	STO
043	03	094	LBL D'	145	NOP	196	RCL .	247	23	29B	+	349	SBR	400	LBL	451	14
044	RCL	095 096	STO	146 147	NOP NOP	197 198	17	248 249	RCL	299 300	RCL	350 351	√X NOP	401 402	X RCL	452	RTN
046	04	097	08	148	NOP	199	RCL	250	09	300	08	352	NOP	402	46		-
047	=	098	RTN	149	NOP	200	22	251	=	302	X	353	NOP	404	STO		
048	STO	099	LBL	150	NOP	201	=	252	NOP	303	(	354	NOP	405	01		
049 050	18 NOP	100	E' STO	151 152	NOP NOP	202 203	STO	253	NOP	304	RCL	355	NOP	406	RCL		
030	NOP	101	310	152	NOP	203	23	254	NOP	305	18	356	NOP	407	47		

#### Instructions

- Key in program
- Enter device's desired channel width and length (W), A, (L), B
- Specify device's operating voltages
   (V<sub>GG</sub>), C, (V<sub>DD</sub>), D, (V<sub>SS</sub>), E, (V<sub>BB</sub>), A'
- State device's semiconductor constants
   (k<sub>P</sub>), B', (V<sub>TO</sub>), C', (λ), D', (α), E', (θ), GTO x<sup>2</sup> R/S, (BE), GTO √x R/S, (φ<sub>F</sub>), GTO 1/x, R/S, (WR), GTO RCL R/S (LR), GTO SUM R/S
- Press GTO CLR R/S to find drain current, I<sub>D</sub>.

length reduction value resulting from lateral diffusion.

The general procedure for using the program is:

- Choose the desired drain current, I<sub>d</sub>.
- Call up the Q<sub>1</sub> parameters by pressing GTO + R/S.
- Specify W<sub>1</sub>, L<sub>1</sub>, and supply voltages.
- Find I<sub>D</sub> by keying GTO CLR R/S.
- If  $I_D \neq I_d$ , provide new W, L, such that W/L =  $W_1I_d/(L_1I_D)$ .
- Call up the stored Q<sub>2</sub> parameters by pressing GTO -

R/S and repeat the two steps preceding this one.

■ Call up the  $Q_3$  parameters by pressing GTO × R/S and repeat the third, fourth, and fifth steps.

Consider the simple case where a single MOS FET stage,  $Q_1$ , has W = 50 micrometers,  $L = 5 \mu m$ ,  $V_{T0} = 0.7 \text{ volt}$ ,  $k_p = 10(10^{-6})$  ampere/ $V^2$ , BE = 0.25,  $\lambda = 0.1$ ,  $\theta = 0.15$ ,  $V_{GG} = 2.5 \text{ v}$ ,  $V_{DD} = 5 \text{ v}$ ,  $V_{SS} = 0$ ;  $V_{BB} = -2 \text{ v}$ ,  $\alpha = 1$ ,  $\phi_F = 0.3$ , WR =  $1(10^{-6}) \mu m$ , and LR =  $0.1(10^{-6}) \mu m$ . The program yields  $I_D = 273.8885 \mu A$ .  $\square$ 

### Engineer's newsletter.

# Fooling the TRS-80 on LPRINT through software

Cass Lewart's hardware suggestion for fooling the TRS-80 into thinking it has a printer connected to it [Electronics, June 19, p. 62] is sound but unnecessary, says Philip M. Haskell of Datel-Intersil Inc. in Mansfield, Mass. "Outputs to both the screen and the printer are controlled by pointers in the 4000<sub>16</sub> page of random-access memory," he notes. "If desired, printer data may be diverted to the screen or screen data may be sent to the printer. All this can be done under software control. To divert LPRINT from the printer to the screen for analysis, enter POKE 16422, 88 and POKE 16423, 04. In this mode, normal PRINT will work as expected. ASCII codes above 128 will appear on the screen as graphics, since the character read-only memory is designed to do just this. To return to the normal mode, enter POKE 16422, 141 and POKE 16423, 05.

"If you wish to send the screen data to the printer for a hard copy of a program display, enter POKE 16414, 141 and POKE 16415, 04. The printer will respond with all outputs that would normally appear on the screen. It actually echoes the keyboard. To return to normal from this situation, enter POKE 16414, 88 and POKE 16415, 04. When the printer is ready, PEEK 14312 will equal 63; if it is out of paper, PEEK 14312 will equal 127. Use of these memory locations and their contents will avoid getting a program HUNG."

### NASA and Boeing aim to increase your productivity

Want to use a computer to increase productivity in your company? A national symposium, set for Sept. 17–19 at the Brown Palace in Denver, Colo., will tell you how. The first of its type, it is sponsored by the National Aeronautics and Space Administration and a technical advisory board from industry. The theme: "IPAD—A National Resource for Increased Productivity." IPAD is an acronym for "Integrated Programs for Aerospace-Vehicle Design," but IPAD concepts, even though spawned in the aerospace field, apply to technical problem solving throughout the electronics industries. Ralph E. Miller, director of the IPAD program for the Boeing Co., says that "the primary goal of the meeting is for companies to increase productivity through the application of an integrated computer system to support both management and engineering activities in the design process, to manage all the data required for these activities, and to provide a smooth link between the design process and manufacturing."

For more information, write to the NASA IPAD Project Office, Mail Stop 246, NASA Langley Research Center, Hampton, Va. 23665, or to Ralph E. Miller, Boeing IPAD Manager, Box 3707 (M. S. 73-03), Seattle, Wash. 98124.

# EIA reports on optical cable, connector tests and standards

If you feel that your fiber-optic cable or connectors, or both, might be run over by a truck or tank—not a farfetched idea for mobile communications and military applications—get a copy of the Electronic Industries Association's "Standard Test Procedures for Fiber Optic Fibers, Cables, Transducers, Connecting and Terminating Devices—Addendum No. 2." This report is the latest word concerning fiber and connector air-leakage and crush-resistance tests and standards. It was formulated by the EIA's Working Group on Fiber Optics Test Methods and Instrumentation under Jim Wittmann of Hughes Aircraft Co. A copy of RS-455-2 costs \$4.50. It is available from the association at 2001 Eye St. N. W., Washington, D. C. 20006.

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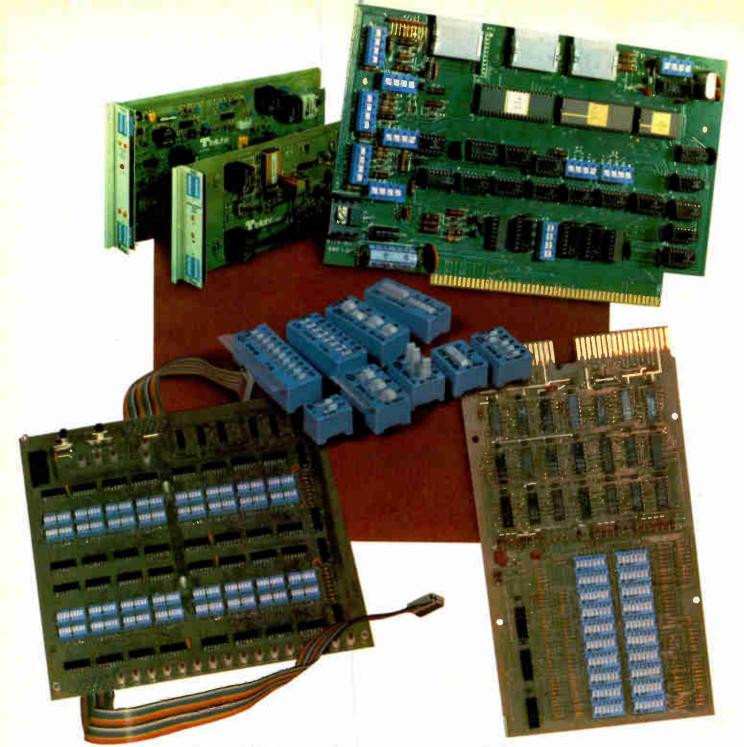
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### Microcomputer draws only 3 $\mu$ A

Unpackaged chip, based on programmable logic arrays, needs minimal external circuitry for timing and control uses

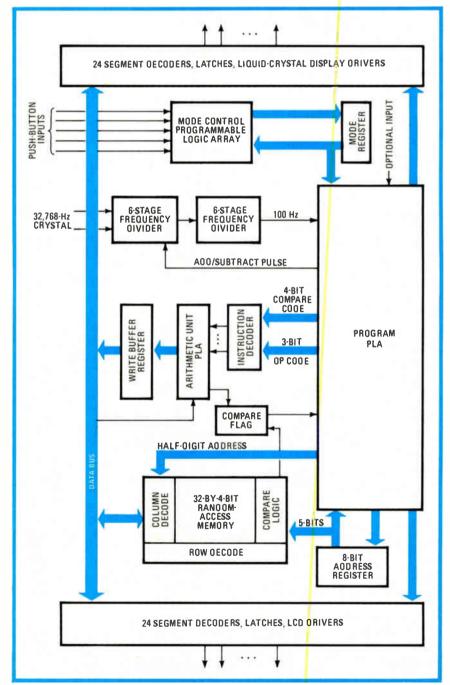
by John G. Posa, Solid State Editor

The AMCC 1259 complementary-MOS 4-bit single-chip microcomputer is heavy on input and output capability and light on the amount of external circuitry required to build a working system. Though the device was intended primarily for timekeeping applications, its unique architecture—based on programmable logic arrays—gives it many other timing and control applications. The 1259's low cost also makes it attractive for the rapidly expanding range of electronic consumer products such as toys and games.

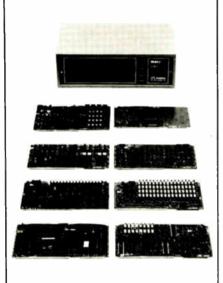
The C-MOS chip does not come packaged; it is delivered in die form. This allows the user the flexibility of selecting the most appropriate package for the device's intended use or for mounting the microcomputer on a hybrid substrate. The 170-by-199-mil chip is fabricated with a standard metal-gate C-MOS process, ionimplanted for 1.5-V operation from a single battery. At this voltage, the chip draws only 3  $\mu$ A.

Of the chip's 64 bonding pads, 5 accept inputs from push buttons and 48 can directly drive liquid-crystal-display (LCD) segments. A 32-kHz crystal is connected across two other pads. These feed an oscillator and a chain of frequency dividers from which all internal timing is derived. An alarm output pad, when coupled to a single external transistor amplifier, drives a piezoelectric or magnetic speaker to provide audible tones.

A separate pad called  $V_{DIS}$  controls the voltage delivered by the 48 output lines. In general, to drive an LCD display,  $V_{DIS}$  is equal to the battery voltage and the output lines are toggled at about 32 Hz. How-



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#### **New products**

ever, the V<sub>DIS</sub> level can be raised to be compatible with standard C-MOS and the output drivers can be electrically switched between V<sub>DIS</sub> and the battery voltage. In this configuration, the 48 output lines can drive standard C-MOS loads. The remaining pads are assigned miscellaneous functions.

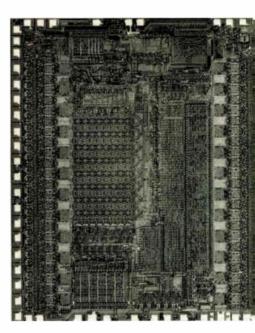
As can be seen in the block diagram of the chip shown on page 143, the microcomputer has programmable logic arrays for program storage, mode control, and arithmeticand-logic-unit operations. The architecture also includes a 32-by-4-bit random-access memory and output decoders and drivers, in addition to miscellaneous timing and control circuitry.

The program PLA's address is stored during each microcycle in an 8-bit address register. This makes it possible to address 256 program steps, though only 136 are implemented on the chip. Five of the bits are simultaneously used to address the on-chip RAM. A compare flag allows branching in the form of conditional IF statements in the microprogram.

The mode control PLA determines the next state of the machine based upon the present state, the contents of the mode control buffer, and the status of the five external pushbuttons. For each valid switch closure, the outputs of this array are strobed and stored in the mode register's latches. This present state is then used as a portion of the program PLA's address.

RAM data is referenced via a 5-bit row address and a 2-bit half-digit address. Such partitioning allows access to a full 4-bit word, the most significant bit of a word, or the 3 least significant bits. Also, RAM addresses are part of the microinstruction word and are therefore under program control. The number of assigned memory locations is stored in the program PLA. Up to 64 uniquely addressable RAM locations can be referenced.

The chip's arithmetic unit is another PLA. Its incrementer and decrementer use programmable lookup tables. An internal compare-



flag generator, with 4-bit inputs from the data bus and the program PLA, performs standard comparisons such as A < B and A = B and also allows for customer-specific comparisons.

The instruction set of the 1259 is structured for maximum efficiency in timing applications. A machinecode instruction is composed of a 3-bit operation code, a 4-bit compare code, and a 2-bit RAM control code. The programmer is allowed to deal with binary, octal, decimal, and hexidecimal numbers in the same pro-

Programming is done by the manufacturer by generating a metal mask pattern for the program PLA. A one-time mask fee costs from \$12,000 to \$16,000, and this price includes 25 prototypes of the chip. In production quantities, the microcomputer's cost ranges from about \$3.50 in 100,000-piece quantities to about \$6.00 apiece when fewer than 1,000 parts are ordered. Delivery is from 8 to 10 weeks after settling on a working program.

A preprogrammed multifunction chronograph version with alarm is also available at the same per-unit costs. However, there is no mask fee for this version.

Applied Micro Circuits Corp., P. O. Box 552, Cupertino, Calif. 95014. Phone (408) 257-4030 [338]



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#### BECKMAN

Circle 145 on reader service card

### FETs used in 200-W supply

New FET-based design cuts size and weight; autoranging feature provides variable current and voltage combination

by Pamela Hamilton, New York bureau manager

Single-output power supplies have traditionally been capable of providing maximum power output at only one combination of voltage and current. In addition, they have tended to be bulky and unsuited to use in both systems and laboratory operations. However, by applying advanced technology to those problems, Hewlett-Packard Co.'s New Jersey division has implemented an innovative design concept involving autoranging and the use of power MOS field-effect transistors for dc power supplies.

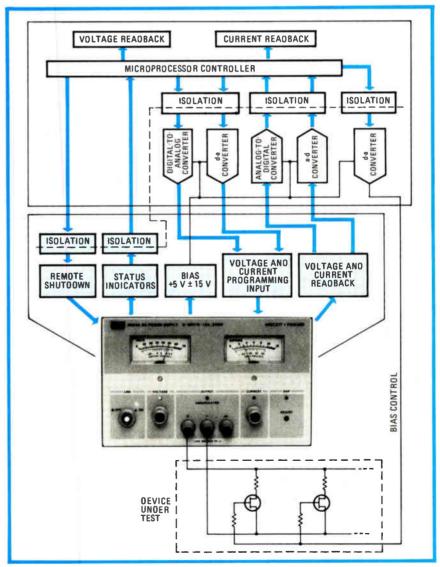
The most noteworthy feature of the 6024A dc power supply is its autoranging capability. In contrast to the conventional constant-voltage, constant-current units, HP's supply provides maximum output power over a broad and continuous range of voltage and current combinations it supplies up to 60 V and up to 10 A, the particular combination being limited to a total of 200 W. Both voltage and current outputs can be manipulated by using front-panel controls, through analog programming, or by an optional system interface. Front-panel controls are 10turn potentiometers; minimum adjustment for voltage is 20 mV, and for current 5 mA.

Up to eight units can be connected in parallel while using a single master power supply to increase current output to a maximum of 80 A. The total output voltage may also be increased—to 240 V—by connecting four units in series with the master supply. When operating the 6024A in the constant-voltage mode, the user may set a maximum current limit; if operating in the constant-current mode, a maximum compli-

ance voltage may be set. A trip voltage setting on the front panel, adjustable from 2 to 64 V with a maximum of 1.5 V above output voltage, avoids false tripping.

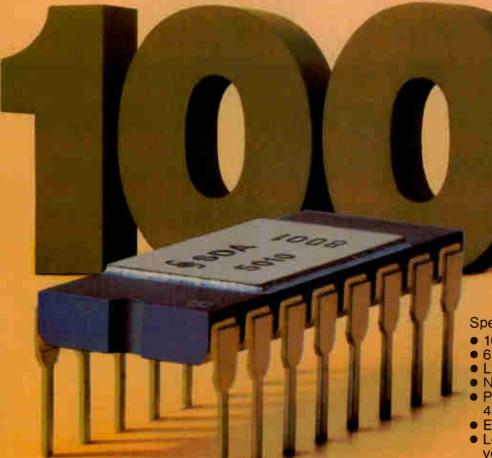
As noted, the 6024A includes

power MOS FETs. Although the switching frequency of 20 kHz is not unusual, the use of power MOS FETs in the 12-lb supply permits the use of substantially smaller power-handling components and filter capacitors—



Applied. Configured in a system, H-P's supply can help test devices.

## In Ten Nanoseconds from Analog to Digital



In only 10 billionths of a second it converts analog signals into digital 6-bit words. This is the new extraordinary device from Siemens—the SDA 5010.

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- Logic-compatible supply voltage.

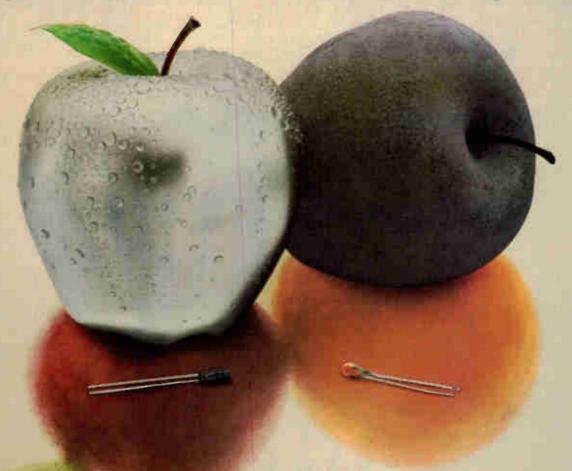
An evaluation board to the SDA 5010 is, of course, available.

And that's only half of it. This device has many other technical refinements. To find out contact: Al Liebich, (201) 494-1000 ext: 2563 or Bob Bruckstein (408) 255-4721. Siemens Corporation, 186 Wood Avenue South Iselin, New Jersey 08830.

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#### **New products**

a design approach similar to the one used with HP's recently introduced modular supply [Electronics, July 3, p. 46].

"The FETs are easy to control," notes Dennis Gyma, section manager of engineering for the Rockaway, N. J., facility. "They go on precisely, and when you tell them to go off, they go off," he observes. The HP design also meets the European radio-frequency-interference suppression criteria of VDE 0871/6.78, level A, and VDE 0411.

In a system. Most system designers need more than one power supply for equipment testing. They must also anticipate future systems needs when considering new supplies. The 6024A, because of its autoranging capability, answers many of these needs, says Bob Taylor, marketing engineer. "Most ATE guys end up with four to eight power supplies around them. Wherever they turn they run into a power supply," he says, but "with the 6024A only three or four units may be needed."

The 6024A provides an amplified current monitor to track those current shunts that are often lost in noisy systems. This amplified current monitor feature provides a voltage referred to the negative output terminal that is proportional to the output current. This voltage varies from 0 to 5 V for output currents between 0 and 10 A. This reading is accurate to within 0.9% + 7 mV, and the output impedance is  $10~\mathrm{k}\Omega$  nominally.

With a remote-control feature on the 6024A, the output voltage or current can be programmed by an external voltage input or resistors connected to programming terminals. A voltage input of 0 to 5 V produces a full-scale output of either 0 to 60 V or 0 to 10 A. A maximum resistance of 2.5 k $\Omega$  produces a full-scale output of either 60 V or 10 A.

Using input resistance programming, an output voltage accurate to within 0.7% + 1 mV or an output current accurate to within 2.3% + 1 mA is possible. With a voltage input signal, an output voltage accurate to within 0.2% + 1 mV or an output current accurate to within 0.9% + 1

mA can be produced by the input.

By means of an optional interface (option 002), the user may integrate the 6024A into a system. The interface ensures up to ±600-v isolation for status and control lines. Six isolated status lines give a digital readout of constant voltage, constant current, unregulated output, ac-line fault, overtemperature, and overvoltage. The open-collector outputs from these lines can be connected directly to TTL or complementary-MOS devices. Remote shutdown and outputbias supplies of +5, +15, and -15V are also part of the optional interface package.

Current input programming, in addition to the voltage and resistance programming, is available with this interface option. By supplying a 0-to-2-mA current sink, the user may obtain a zero-to-full-scale voltage or current output. The output voltage is accurate to within 0.3% + 7 mv and the output current is accurate to within 1% + 2 mA.

"Current programming is starting to come on in systems programming," says Taylor. "It provides systems with noise immunity."

Load regulation for voltage is 0.01% + 3 mV and 0.01% + 3 mAfor current, both under any load. Ripple and noise (listed as PARD, or periodic and random deviation) between 20 Hz and 20 MHz are specified in root-mean-square and peakto-peak terms: voltage PARD is 3 mV and 30 mV, respectively; current PARD is 5 mA rms. Also, when operated in the constant-current mode. output-voltage recovery time is less than 1 ms to regain 75% of the nominal output following a change in output current of 90% to 100% of maximum current.

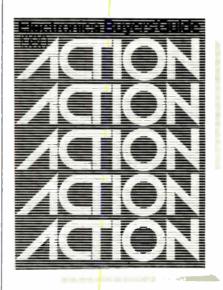
The fan-cooled supply operates from 0° to 55°C. It accepts an ac input from 104 to 127 V ac at 48 to 63 Hz, 5.3 A rms maximum.

The supply sells for \$875, with the system interface option adding another \$300. Delivery is within two to four weeks.

Hewlett-Packard Co., New Jersey Division, Green Pond Rd., Rockaway, N. J. 17886, or 1501 Page Mill Rd., Palo Alto, Calif. 94304 [339]

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Microcomputers & systems

## Unit controls tapes, hard disks

Multibus-compatible controller handles up to four hard-disk and four tape drives

The latest of the new wave of disk controllers for Winchester disk drives in small-computer systems handles both hard-disk drives and the tape drives that are so necessary for backup memory storage. The Rimfire 38, a single-board controller that is manufactured by Computer Products Corp., handles up to four disk and four tape drives and operates on the Intel Multibus.

Like the recently introduced Shugart Associates floppy- and fixed-disk and tape controller [Electronics, April 24, p. 208], the Rimfire saves the system designer the expense and trouble of designing his own controller and at the same time saves space. But, emphasizes Computer Products president Ronald B. Thomas, "unlike the Shugart controller, which operates on a general-purpose interface bus, the new controller works on

the widely used Multibus."

The Rimfire 38 can run any of Priam Corp.'s 8- and 14-in. disk drives, handling disks that store from 10 to 150 megabytes. For backup, the unit interfaces with as many as four Cipher Data Microstreamer tape drives, for a maximum of 46 megabytes of tape storage.

The core of the Rimfire 38 board is an Intel 8089 input/output processor that communicates with programmable read-only memory and random-access memory over its own 16-bit local bus. The controller is software-programmable to run with either an 8- or a 16-bit host system. It has 20-bit addressing to access memory directly and can function in a single- or multiple-processor environment. It also has software-programmable interrupts and contains full-sector buffering on board. It formats and detects errors using a cyclic-redundancy-checking technique across 16 bits (CRC-16).

The disk- and tape-drive controller operates in two modes—incremental and backup. Tape files may be read, written, and edited incrementally in real time, as in disk operation. This mode is useful for file reconstruction, says the manufacturer, "where fragmented portions of a disk file are reconstructed sequentially in system memory and

then stored on tape or later reloaded onto the disk." In the non-real-time backup mode, the controller locks the system bus and bypasses local buffers to save large portions of a disk on tape. As a buffer area for this mode, system memory must offer a minimum of 4 kilobytes; the ontimum-size buffer is a full track of data (about 19 kilobytes for a Priam Diskos 3350 with 1-kilobyte sectors). With enough host-system memory, the Rimfire can transfer data from a disk at a rate of up to 1.3 MHz, and a 30-megabyte disk can be loaded onto tape in 10 minutes.

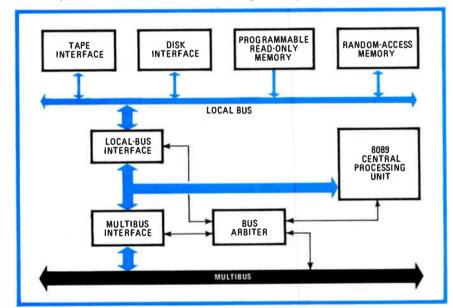
Prices for the disk and tape controller range from \$1,795 apiece for orders of 50 units or more to \$2,295 each for up to 9. The Rimfire 38 is also available in disk-only (38D) and tape-only (38T) versions. These are priced at from \$1,895 for single units to \$1,485 apiece in 50-unit quantities. The controllers can be delivered within 45 days after an order is placed.

A second member of the Rimstre family will follow shortly, says company vice president Michael L. Quealy. Instead of the interface with the Microstreamer, the forthcoming controller will include a Data Electronics Inc. <sup>1</sup>/<sub>4</sub>-in. tape-cartridge interface, he says. "We anticipate that this controller will appeal to the designer of smaller systems using 8-in. disks."

Computer Products Corp., 2415 Annapolis Lane, Plymouth, Minn. 55441. Phone (612) 559-2034 [371]

## AmZ8000 gets emulator, development systems

To provide support for the AmZ8000 microprocessor family, Advanced Micro Computers has introduced two development systems and a real-time emulator for the 16-bit processors. The AmSYS8/8012 is a double-density floppy-disk-based system that offers complete hardware and software development for the AmZ8000s, and the AmSYS8/8014 is a 10-megabyte enhancement of the 8012. Both sys-



**On-board.** At the heart of the Rimfire 38 controller is an Intel 8089 I/O processor that communicates with PROM and ROM over its 16-bit local bus.

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Whenever you want to record data, retain it, or change it in system...that's when you will want to consider General Instrument EAROM.

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#### **New products**

tems are based on the AmSYS8/8 development system, except that the 8012 uses an Am8085A-based 3-MHz central processing unit and doubles the amount of mass storage to one megabyte, and the 8014 has a cartridge-disk subsystem with 5 megabytes each of fixed and removable storage. The 8012 is priced at

\$10,900; the 8014 is \$22,400.

The model RTE16/8050 16-bit emulator provides real-time emulation for both the nonsegmented AmZ8002 and segmented AmZ8001 microprocessors. It includes an emulator, real-time trace, breakpoint, and control and program memory boards. The emulator has a dual-bus

structure and 8-K bytes of static random-access memory that can be expanded to 256-K bytes with standard dynamic RAM. With an AmZ8002 emulator pod, the RTE16/8050 card set is priced at \$7,250; with an AmZ8001 pod, its cost is \$8,250.

The emulator and the development systems are all available 120 days after the placement of an order. Advanced Micro Computers, 3340 Scott Blvd., Santa Clara, Calif. 95051. Phone (408) 988-7777 [373]

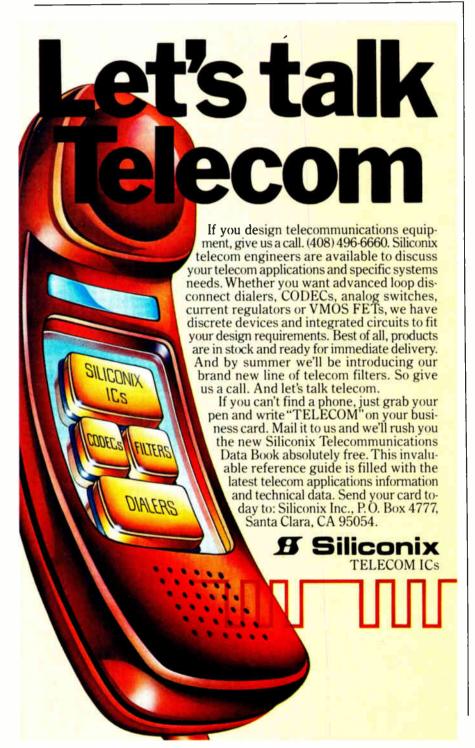
Apple III computer has up to 128-K bytes of memory

The most powerful of the Apple personal computers, Apple III, has up to 128-K bytes of memory and includes a built-in disk drive, color and black-and-white video capability, and a 6-bit digital-to-analog converter for voice or music generation. The computer uses a superset of the 6502 instruction set.

The first two application packages available for use on the Apple III are Information Analyst software for forecasting, planning, and scheduling, and a word-processor software package. The \$4,340 Information Analyst consists of an Apple III with 96-K bytes of random-access memory, a built-in 5<sup>1</sup>/<sub>4</sub>-in. floppy-disk drive, keyboard, two printer interfaces, and a 12-in. black-and-white monitor. Software includes Apple's Sophisticated Operating System (SOS) and assorted management tools

The word-processor system consists of the same basic configuration except that it includes two disk drives—one built in and one external. These can store about 60 pages of text per removable diskette. With a thermal printer the word processor sells for \$5,330; with a daisy-wheel printer it is \$7,800. A variety of peripherals is available, including up to 32-K bytes of additional RAM and up to four 51/4-in. floppy-disk drives. Shipments begin this month.

Apple Computer Inc., 10260 Bandley Dr., Cupertino, Calif. 95014 [375]



HIS is not a dream.
You are heading toward Hong
Kong harbour on an avenue
paved in Italian stone. You pass a
fountain, its plume as tall as a giant
palm. You stop, very nearly at the
shoreline itself.

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Your registration form is filled out for you instantly, by a computer. You are shown to your room and discover that your luggage has already arrived by a special express lift.

Alone, you pause to survey the spectacular view.

You scan the modern cargo ships, the ancient junks, the distant hills. And you begin to doubt that any of the room's future occupants will ever actually turn on the colour TV.

You look around the room, finding much to your liking. A full-sized desk. Telephones in all the right places. A door that isolates your foyer from the bedroom itself.

In the spacious bathroom, you note

# Once every generation Hong Kong acquires a great hotel



the marble tiling. The enormous tub. The separate shower.

You search for the mini-bar, and are a bit surprised not to find one. But of course. One tends to forget that 24-hour room service can still exist. At The Regent each floor has its own private butler. When you ring for service, he's there in a matter of seconds.

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Before dinner you stop at the Mezzanine Lounge. You order and the waiter pours your drinks right at the table, just as they do at your private club.

You glance across to the lobby below. A limousine pulls up to the hotel entrance and its elegant passengers vanish up a sweeping marble staircase. This leads to the Regent Ballroom, largest ever built in Hong Kong and destined to be the room where the city will celebrate its great events of the 1980s.

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The better you know hotels in Hong Kong, the more you will appreciate The Regent's huge octagonal pool and its exotic garden setting. It is a true resort, in the very heart of the city.

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#### **New products**

Computers & peripherals

## TRS-80 gets voice recognition

Second-generation voice-entry terminal has 40-word vocabulary

With the market for voice-recognition equipment expected to soar to as much as \$1 billion or more by the late 1980s [Electronics, May 22, p. 95], the field is spawning a number of new competitors, all eager to cash in on the emerging technology.

One of the latest entrants is Scott Instruments Corp. In February, the firm introduced the Vet-1 voice-entry terminal priced at \$495. Now, five months later, the two-year-old company has unveiled a second-generation unit priced at \$895 that offers extended vocabulary capabilities as well as some performance improvements.

Known as the Vet-2, this voiceentry terminal comes with a 41/2-by-101/2-by-101/2-in. preprocessor cabinet that contains digitizing and associated circuits; other components include a noise-canceling microphone and a 4-kilobyte operating system housed on a 51/4-in. minidiskette that also provides space for storing the vocabulary templates. Like the Vet-1 - now discontinued - the Vet-2 has been designed to work with Tandy Corp.'s TRS-80 model 1 personal computer. It is being adapted to work with Pet and Apple machines as well.

A speaker-dependent system, the Vet-2 requires operator training in that each person using the machine must repeatedly say the words of the desired operating vocabulary to create the voice-pattern templates; the templates are then used for the comparisons that make possible word recognition. Though this procedure is similar in many respects to that of competitive systems, Vet-2 employs some software techniques to aid recognition accuracy and system flexibility that are believed to be unique.

In one such technique, the system does a first-pass analysis of the number of syllables in an utterance before performing template comparisons for word recognition. This approach improves speed and cuts potential error by automatically bypassing from one third to one half of the word templates in a typical 40-word vocabulary that do not contain the proper number of syllables, explains Brian L. Scott, the company's president.

Another technique—Scott calls it variance weighting—applies more stringent recognition criteria to those portions of a word that are least subject to pronunciation differences from person to person; other portions are permitted greater variation. In some cases, this feature allows the Vet-2 to be used by two different individuals using the same set of templates, Scott officals say.

The Vet-2's recognition accuracy is specified as better than 98%. Response time using a 40-word vocabulary is pegged at less than 200 ms typically.

The Vet-2 goes beyond the single 40-word vocabulary provided on the earlier Vet-1, however. It employs a software overlay feature that allows an unlimited vocabulary by linking multiple 40-word template sets, though response time may be degraded, the company says. The minidiskette provides an 89-kilobyte memory. With 4 kilobytes devoted to the operation of the system and each 40-word vocabulary requiring 5 kilobytes, the unit has a potential capacity for 17 vocabularies.

Vet-2 units for use with the TRS-80 model 1 are available now. Versions designed to work with Pet and Apple personal computers are expected in about six weeks.

Scott Instruments, 815 North Elm, Denton, Texas 76201 [361]

## Intelligent terminal has custom emulation firmware

A stand-alone intelligent terminal for distributed processing comes in two versions: a desktop and a pipe-



You may never need the extreme-value engineering of our Snap-Lock metal circulars. They're made for the exceptionally tough environmental job. where failure is out of the question.

But our polycarbonate Thorkom circulars take over from there. And still, there's no skimping on quality. High impact housing, high contact density, high reliability—everything is high, but the price.

So. cut costs? Why sure. But skimp on Viking quality? Certainly not.

## We don't think skimping on the connector ever makes sense.





Test drive our high performance compact.

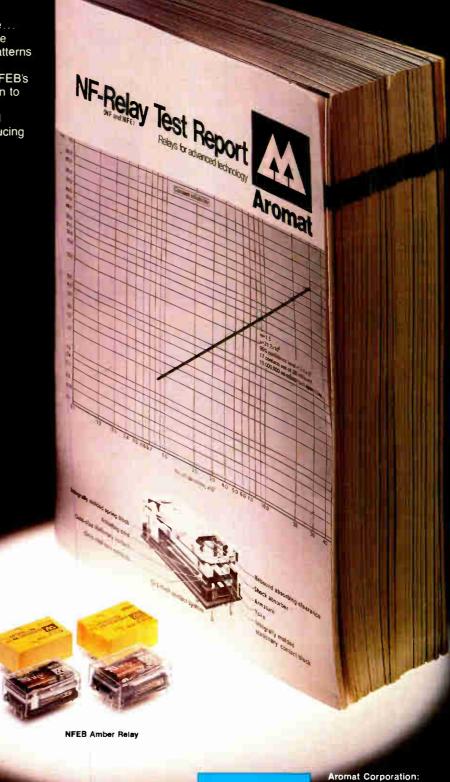
Over 20 million Aromat NF relays in use... built for high performance, with a low profile

that's perfectly suited for the busy traffic patterns of today's high density PC boards.

Responsive handling is the key to the NFEB's reliability, with shock absorbing construction to assure smooth long lasting performance.

Aromat was the pioneer in plastic sealed relays over 10 years ago, and is now producing the NFEB in the U.S. Extensive test data, gathered here and abroad, prove the dependability of these relays.

SPECIFICATIONS
Contacts
Arrangement
Rating resistive load
Max. switching power 60W 100VA
Max. voltage 220V AC/DC
Max. current2A
Max. current.         2A           UL rating.         0.5A 125V AC, 2A 30V DC           VDE rating.         1A 65V AC, 2A 30V DC
VDE rating
Expected life, min. operations
Mechanical
Electrical (2A 30V DC Resistive) 106
(1A 30V DC Resistive) 5 x 10 <sup>6</sup>
Initial contact pressure approx. 8.5g (0.3 oz)
Contact bounce approx. 1.5 msec.
Contact material
Movable contact
Stationary contact Gold-clad silver
For telephone circuit applications
gold-clad silver-palladium type is available
rated 0.1A 50V DC 10 x 10 <sup>6</sup> operations
Initial contact resistance
Maximum50 mΩ
Typical
Coll
Min. operating power (at 25°C) approx. NF2.150mW,
NF4 240mW
Nominal operating power (at 25°C) approx.
NF2/300mW,
NF4/480mW
Max. operating power approx.
for continuous duty
Max. operating speed
Operate time
Release time
Electro static capacitance
Contact/Contact approx. 4 pF
Contact/Coilapprox. 7 pF
Contact/Groundapprox. 6 pF
Breakdown voltage
Between open contacts
Between contact sets
Between live parts and ground 1,000Vrms
Between contacts and coil1,000Vrms
Initial insulation resistance1,000MΩ at 500VDC
Ambient temperature40 to +65°C
-40 to +149°F
Shock/Vibration resistance
Deenergized condition 8G 8G 55 cps.
Energized condition 20G 20G 55 cps.
Unit weight approx. NF2/14g (0.5 oz.) NF4/16g (0.6 oz.)
Specifications for MBB contact types
Expected life, min. operations
Electrical (1A 30V DC Resistive)106
Breakdown voltage
Between open contacts 200Vrms
All other characteristics are the same as those of
standard types.



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#### **New products**

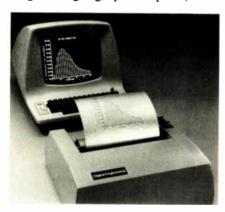
column model. As many as four cathode-ray-tube display stations and four input/output devices (plotter. printer, floppy disk, and modem) can be operated from one model 427 terminal. The manufacturer of the terminal will customize the firmware at no extra charge for special applications and for the emulation of any existing terminal.

The basic 427 includes a light pen, a Z80 microprocessor, a 256-byte random-access memory, a 1-kilobyte read-only memory, and a CRT display and keyboard. The CRT monitor has a screen capacity of up to 2.048 7-by-12-dot matrix alphanumeric characters. It displays 20 lines and buffers 12 lines on its 12-in. rasterscan screen. The keyboard has a full 128-character upper- and lower-case ASCII set. The terminal transmits full- or half-duplex asynchronous data at rates of up to 9,600 b/s via its RS-232-C interface. Options for the 427 include memory expansion to 65 kilobytes, synchronous protocol, and choice of parity and number of stop bits.

The desktop model sells for \$3,680; the pipe-column model is \$3,910. Delivery takes 60 to 90 days. Computer Talk, P.O. Box 100, Idledale. Colo. 80453. Phone Joan Henann at (303) 697-5485 [363]

#### Electrosensitive unit prints graphics from dumb terminal

An electrosensitive graphics printer fits Lear Siegler Inc.'s ADM-3A dumb terminals that have Digital Engineering's graphics option, Ret-



ro-Graphics. Retro-Graphics is a printed-circuit board (model RG-512) that makes the ADM-3A compatible with Tektronix software so it can perform such complicated computer graphics as point plotting and automatic vector generation. The Graphx-Printer, model GP-100, plugs into the RG-512 pc card.

The GP-100 can print a hard copy of the graphics within a 6.7-by-5-in. area in under 20 seconds. It prints alphanumerics at a rate of 170 lines/minute.

The suggested list price is \$1,995. Digital Engineering Inc., 1775-C, Tribute Rd., Sacramento, Calif. 95815. [365]



#### Higher accuracy, better resolution, and lower cost with Newport's Series 230/260.

Measurements of temperature, pressure, flow, speed, voltage and current can now be easily made with Newport's new meter relay line by selecting a plug-in signal conditioner tailored for a particular sensor and measurement range. A thermocouple conditioner will provide reference junction. μV preamp and linearizer, while a pressure cell conditioner Istrainometer) will provide bridge excitation,  $\mu V$  preamp and offsetting.

In addition, the basic ACpowered meter provides an analog output for strip chart recorders.

DC Voltmeter or Ammeter **Process Monitor Tachometer** 

Optional single or dual set point relay control is provided with 1500V isolated form C relav contacts rated at 5A for each set point. A dual set point controller can be logic level programmed for 3-position or hysteresis control. External control of latching and resetting of relay coils is provided. For each set point a pushbutton switch, when depressed, displays the set point value stored in a multiturn potentiometer. An LED lamp lights when the relay coil is energized.

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#### Components

## IC amplifier puts out 5 W at 1 kHz

SIP-cased dual-power audio amplifiers deliver 70 dB gain into 8-ohm load

The heat is on for manufacturers of audio power-amplifier integrated circuits to develop products that deliver more power from smaller packages, without sacrificing high performance levels. The LM2878P high-voltage dual audio-amplifier IC from National Semiconductor Corp. is one example of industry's response.

Packaged in an 11-lead single inline case, the IC amplifier operates into 8-Ω loads over an operating temperature range from 0° to 70°C. Despite its price of \$1.50 each (in 100-unit quantities), the IC delivers impressive performance. For example, it operates over a voltage range of from 6 to 32 volts. Ripple-rejection and channel-separation performances are also excellent for

MW 006 LM2878P

devices in such a price range: they are 60 and 70 dB, respectively, referred to the output.

The output-power rating of 5 W/channel is taken at a frequency of 1 kHz and at a total harmonic distortion of 10%. At that frequency, distortion is typically 0.20%, 0.15%, and 0.14% for output-power levels of 0.05, 0.5 and 2 W, respectively. The amplifier delivers an output-voltage swing of 6 V peak-to-peak into an  $8-\Omega$  load. Open-loop gain is typically 70 dB and open-loop input impedance is typically 4 M $\Omega$ .

The IC's maximum junction-temperature rating is 150°C. To operate at ambient temperatures of over 25°C, it must be derated using thermal resistance curves that depend on the device-mounting method used.

Included in an 11-pin SIP are current-limiting, short-circuit-protection, and thermal-shutdown features. Typical current limit is 1.5 A. The amplifier's slewing rate is typically 2  $V/\mu s$ . Its 3-dB power bandwidth (at 2.5 W) is 65 kHz.

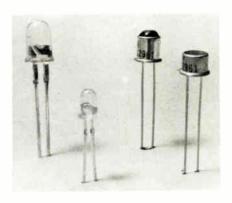
The LM2878P is internally compensated for gains greater than 10 and operates from a 22-v supply.

Applications include stereo phonographs, radio and TV receivers, tape recorders, power comparators, and servo amplifiers. Delivery is from stock.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. (408) 737-5000 [341]

#### Infrared device emits 10.5 mW at 100 mA

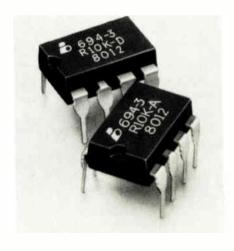
The XC-88-PC infrared emitter provides a minimum output of 10.5 mW at 100 mA. Power conversion efficiencies for the packaged devices can reach 20%, so according to the manufacturer the devices typically deliver twice the optical power of the best gallium arsenide emitters that are commercially available. These diodes have a typical output wavelength of 880 nm, which allows for improved coupling efficiency to silicon phototransistors.



The IR emitters are useful for applications in solid-state photoelectric controls, optical switches, reflective transducers, and encoders. They are available in TO-46 hermetic, T-1¾ plastic, and T-1 plastic packages. For 1 to 24 pieces, each component sells for \$3.06; they are \$2.35 each for 25 to 99 pieces; and in lots of 100 to 999 the devices sell for \$2.14 apiece. Delivery is from stock. Xciton Corp., 5 Hemlock St., Shaker Park, Latham, N. Y. 12110. Phone (518) 783-7726 [344]

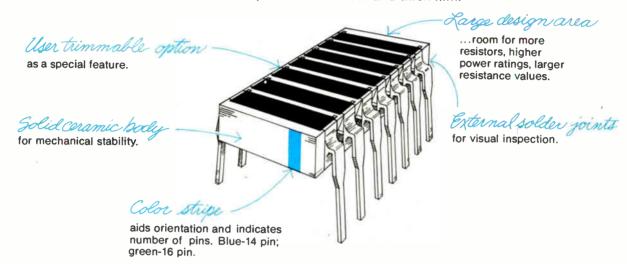
## 8-pin DIP thin-film resistors sell for under \$1.60

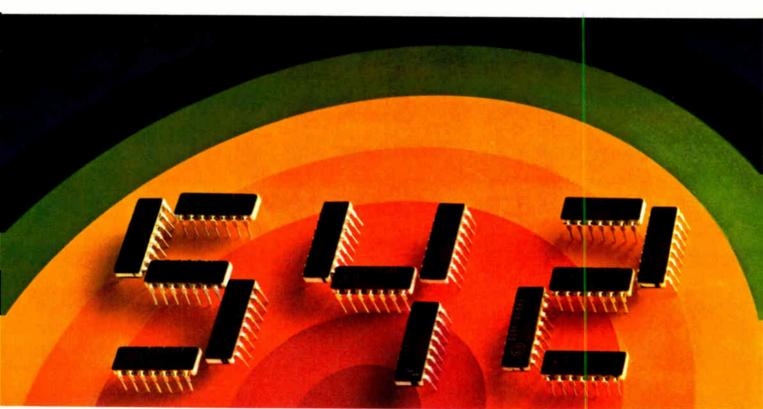
Selling for under \$1.60, the model 694 is a thin-film eight-pin dual inline package that contains four isolated precision resistors. The resistors can be connected in parallel and in series to create ratios for voltage dividers and current summing units. The thin-film resistor network allows the ratios to track within 5 ppm/°C



## Interested in network variety? Select from a spectrum of 542 standards.

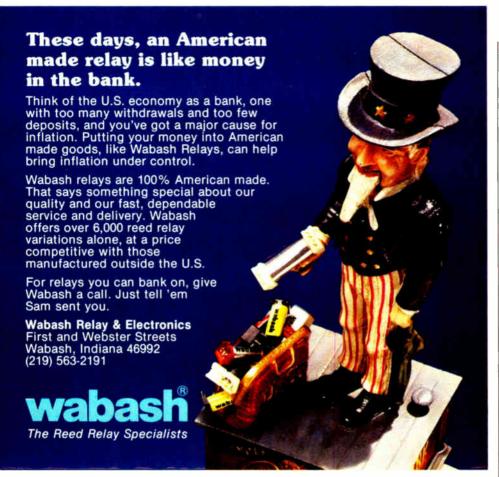
Allen-Bradley has the popular configurations you need. Pull-ups, Pull-downs. Line Terminators. Networks to complement Core Memory Sense Amplifiers. TTL to ECL Translators. O-Pad Attenuators. R/2R Ladders. Interconnect Networks. All styles available from your Allen-Bradley *Electronic Distributor*. Call for specs or check your EEM Catalog. If you need specials, contact your local Allen-Bradley district office for fast turnaround. Ask for Publication 5840. A-B is an experienced twin-film manufacturer, i.e. precision thin film and thick film.



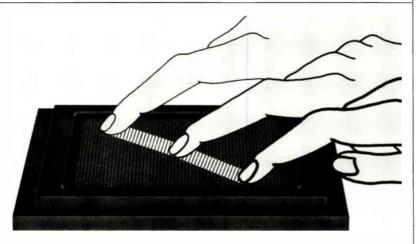


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#### **New products**

over the temperature range from  $-55^{\circ}$  to  $+125^{\circ}$ C. The absolute temperature coefficient is 50 ppm/°C or better. The units sell for \$1 to \$1.50 each in lots of 1,000.

Beckman Instruments Inc., Network Products Operations, 2500 Harbor Blvd., Fullerton, Calif. 92634. Phone (714) 773-8326 [346]

#### 100-A rectifiers

recover within 75 ns

The SER 8050, 8100, and 8150 100-A rectifiers are rated from 50 to 150 V. They exhibit a reverse-recovery time of 50 ns typically and of 75 ns maximum. The Epion ion-implanted devices have an average forward voltage drop of 450 mV and an average reverse current of 5 mA. The packaging uses metallurgically bonded construction with modified DO-5 case. The peak repetitive forward current is 400 A and the peak surge current is 1,000 A. The operating temperature range is  $-65^{\circ}$  to +175°C. In quantities of 100, the rectifiers sell for from \$14.95 each to \$20.95 each, depending upon the peak inverse-voltage rating. Delivery is from stock to 30 days.

Solid State Devices Inc., 14830 Valley View Ave., La Mirada, Calif. 90638 [347]

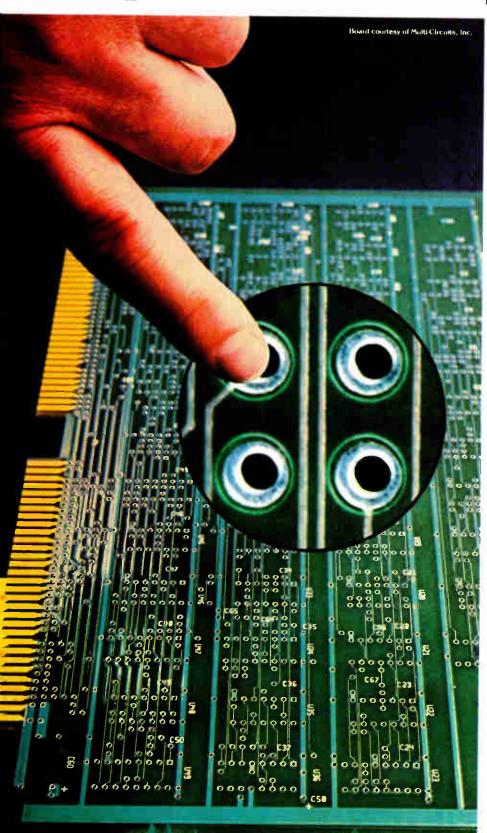
#### Scott T transformer

has 0.3-in. profile

The 52910 Scott T transformer, measuring 0.5 by 0.85 by 0.3 in. ±0.035 in., converts three-wire synchro information into four-wire resolver information. The 0.3-in. height allows for minimal board-to-board spacing and is also compatible with average integrated-circuit-board heights and spacing. Weighing only 0.25 oz., the transformer operates over the temperature range of from -55° to +125°C. In quantities of 1,000, it sells for \$27. Delivery time is approximately eight weeks.

Magnetico Inc., 182 Morris Ave., Holtsville, N. Y. 11742. Phone (516) 654-1166 [348]

# When you design circuitry this tight, you need the protection of VACREL.

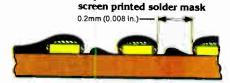


Fine line printed circuit board designs call for tight conductor spacing. And with spacing tolerances of less than 0.3mm (0.012 inch), you need circuitry protection beyond the capability of ordinary screen printed solder mask. You need VACREL dry film solder mask.

In the cross sectional illustration below, VACREL uniformly covers the circuitry with no skips. It provides *maximum protection* of fine line circuitry, even below 0.2mm (0.008 inch) conductor spacings, resulting in electrical, environmental and mechanical protection.

with VACREL Solder Mask
0.2mm (0.008 in.)

Skips with conventional



Conventional screen printed solder mask has limited utility in the protection of fine line circuitry.

Interested? Ask us to show you how VACREL dry film solder mask can protect your tightest circuitry designs. Write: VACREL Solder Mask, RISTON® Products, DuPont Company, Rm. 38014, Wilmington, DE 19898.

#### Innovations for Electronics



Circle 161 on reader service card

#### **New products**

Packaging & production

#### E-beam measures chip voltages, cuts probe capacitance

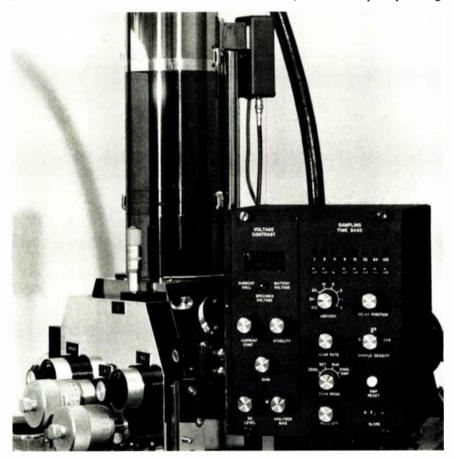
Normally, circuit voltages on a bare integrated-circuit chip or wafer are measured using fine tungsten-wire mechanical probes. However, for fine-geometry very large-scale integrated circuits and high-speed devices, the stray capacitance from a probe's contacts can change the characteristics of the device being examined. A new technique may overcome that problem.

Those using scanning electron microscopes (SEM) for detailed chip examination have long been aware of the difference in appearance between static IC sites with positive charges and those carrying a negative charge. Now Perkin-Elmer has introduced its Etec Autoscan

VC 200, which employs electronbeam technology to make precise measurements without the stray capacitance problem. The submicrometer beams also provide greater resolution than the mechanical probes.

The new system is actually an SEM, modified to provide quantitative characterization of time-variable voltage within an IC. It bombards the chip or wafer with electrons, which cause secondary emissions from the device surface. Also, the electron-beam pulse rate is synchronized to the device's operating frequency. An electron energy analyzer - part of the VC 200 system measures the secondary energy from the device surface and generates a signal that in turn can be calibrated to measure circuit voltage. Normally, SEM beam excitation is on the order of 30 kV. In the VC 200, it ranges between 10 and 20 kV, in order not to damage the device.

By locking the electron-beam pulses to the operating frequency of the circuit, a stroboscopic operating



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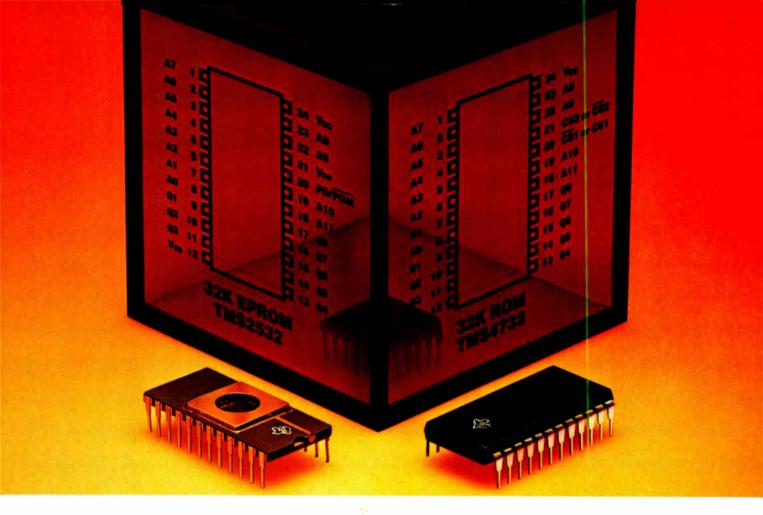
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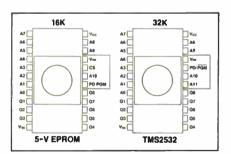
#### ROM compatibility

TMS2532 is pin compatible with 32K ROMs supplied by ten sources. So, when your programming is finalized and you're ready for volume production, the switch from EPROM to ROM is quick, easy and cost-effective.

#### **Upgradability**

From 16K or to 64K. Easy. TI's TMS2532 is plug-in compatible with the industry-standard 16K 5-V EPROM. All you need to do is include the signal to PD in the address decoder. Minimal modification for upgrade to 64K, too.

And the trend is continuing. Two other EPROM suppliers now provide this JEDEC-approved pinout.



#### Low power and lower power

The standard TMS2532 comes in at 400 mW typical active power (worst case —  $T_A = 0$ °C). When deselected, TMS2532 automatically assumes a low power mode — 50 mW typical.

The even lower power TMS25L32 actively dissipates 325 mW typical, while offering  $\pm 10\%$  power supply tolerance.

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If you're thinking 32K EPROM, think TMS2532. For new systems design. For upgrading existing systems. Or for eventually switching to 32K ROM.

Production is up and distributor stocks are in good supply, ready to move.

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authorized distributor. For more information on the entire TI 5-V EPROM Family, write to Texas Instruments, P. O. Box 1443, M/S 6965, Houston, Texas 77001.



#### Texas Instruments

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#### **New products**

mode is created, and that permits sampling over a large number of operating cycles for precise voltage measurements. Small, discrete changes in the sampling point within the duty cycle can result in a time-voltage profile with resolution on the order of 1 ns and 20 mv. Voltage readout may be through either an

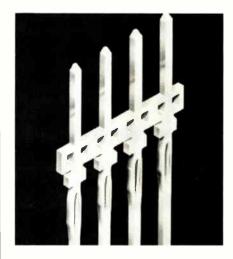
oscilloscope or a graphic recorder.

The final prototype of this machine was exhibited at the recent Semicon West in San Mateo, Calif., but delivery will not start until this fall. The prices will be between \$160,000 and \$170,000.

Perkin-Elmer Etec Inc., 3392 Investment Blvd., Hayward, Calif. 94545 [391]

## Compliant contact allows 0.035-to-0.041-in. tolerance

A compliant contact for multilayered printed-circuit boards overcomes relaxation, or creep, effects and has hole tolerances of from 0.035 to 0.041 in. It is designed for use with complex multilayer printedcircuit and heavy copper back panels, providing an efficient interface between plated-through holes and interconnections with other areas of



an electronic system.

The Reli-Afit contact supplies a high retention force that does not damage the plated-through holes of expansive multilayer back panels. The contacts are available on continuous reels in either feed-through or cantilever form. Application tooling is available. For the gold-plated version, each contact costs  $3\phi$  in production quantities. Delivery time is from 12 to 14 weeks.

Methode Electronics Inc., Connector Division, 7447 W. Wilson Ave., Chicago, Ill. 60656. Phone (312) 867-9600 [393]

## Clip-on bus bar lessens assembly and installation time

A clip-on bus bar system for prototyping and for custom and production assembly of backplane power and signal buses should lower termination costs by at least 60% by les-



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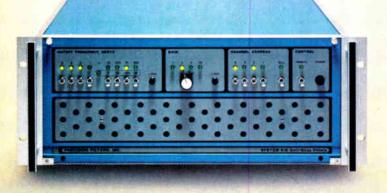
phase match is ½°, with worst case of 2°. You get performance that used to require a custom instrument, without paying a custom price.

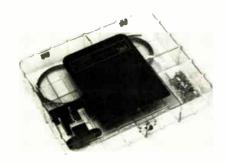
Call Don Chandler, 607-277-3550, or write for complete specs and a demonstration.



#### PRECISION FILTERS, INC

303 W. Lincoln, Ithaca, N.Y. 14850





has nickel or copper-nickel-gold alloy conductors 0.5 mil thick laminated to a silicone rubber substrate. These conductors wrap around the substrate and connect the edge-connector pattern of one pc board to that of another. Because the connector's conductors are very narrow—0.010 in. wide and on 0.020-in. cen-

ters—they provide redundant contacts. In fact, the connectors are self-aligning and therefore lend themselves to automatic positioning. In quantities of 10,000, each costs 25¢ per inch of length. Delivery takes four weeks.

Hulltronics Inc., 333 Byberry Rd., Hatboro, Pa. 19040. Phone (215) 672-0787 [397]

sening the time spent in assembly and installation, says 3M. The bar, a conductive copper alloy (CDA 110), is coated with Scotchcast electrical resin, a tough epoxy that will not crack when the bar is bent to mate with nonaligned rows of pins. Contacts are available with either gold or tin-lead plating. Kits come with two 6-ft lengths of bus bar (with 0.100-in. or with 0.125-in. spacing) that can be cut to desired lengths, 150 contacts, a contact-to-bar assembly tool, and a bar-to-pin field-insertion tool.

Preassembled and pretested 12-in. units with 24 tin contacts spaced 0.100 in. apart sell for \$2.70 in quantities of 500 or \$3.95 with gold contacts. A unassembled bus bar sells for 83¢/ft. The price of 1,000 gold-plated contacts is \$111 and \$76 for those with tin. Delivery time is three to four weeks.

3M Co., P. O. Box 33600, St. Paul, Minn. 55133. Phone Richard Barker at (612) 733-9214 [394]

## Self-aligning elastomeric connector mates pc boards

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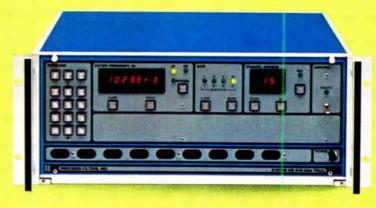
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Semiconductors

## MOS FETs have 450-V breakdown

Power MOS transistors, built with Z-MOS process, operate from ac line

Using its new process for producing vertical double-diffused MOS field-effect transistors, Intersil has developed a family of vertical power MOS FETs that guarantees freedom from breakdown below 450 v. The company expects them to be the first such devices capable of operating directly from ac line voltages while staying within industry-accepted safety margins.

Several suppliers offer power MOS FETS specified for 350-to-400-V breakdown, and so will Intersil. But the firm expects the 450-V breakdown provided in its IVN6000 series

to give it a big edge in designs for switching power supplies, ac motor controls, and other applications calling for operation from an ac line. What's more, their 10-ns switching speeds make units of the series an order of magnitude faster than competitive MOS FETS (100 ns typically) and several orders of magnitude faster than conventional bipolar power transistors (several microseconds typically), claims Jerry Zis, Intersil's director of analog and power products marketing.

According to Zis, the additional 50-to-100-v breakdown specification of the IVN6000 series "makes a big difference" to the circuit or system designer calculating safety margins. That is because line voltage in the United States, for example, ranges from 105 v to 132 v, which means that peak voltage (1.414 × line voltage) can be as high as 186.65 v, he explains. Though standard practices of doubling the peak voltage would suggest that a breakdown voltage of 375 v or more would be sufficient, Zis says, "that's not good enough."

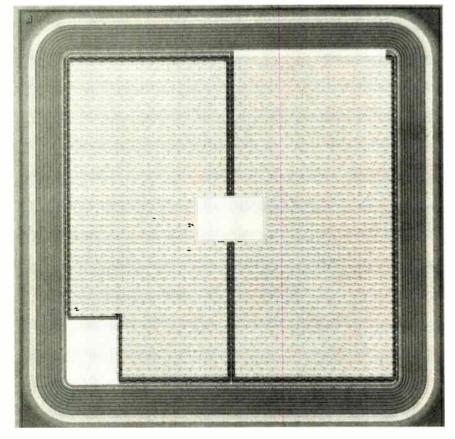
The Intersil marketer notes that there are other factors to be considered when determining safety margins. Among these are the stray inductances associated with transformers, lead wires, and other circuit elements that subtract about 10 v from the safety margin. Allowance also must be made for momentary line surges that could reach several volts for a few microseconds and cause a breakdown, he cautions.

Perhaps most significantly, Zis notes that because of the inherent characteristics of power MOS FETs, their breakdown voltage "is a function of junction temperatures, in turn affected by the ambient temperature. Specifically, at the low end of their temperature range, breakdown voltage is reduced. So when operating in cold environments, you don't have the breakdown voltage you thought you had."

At 0°C, for example, the breakdown voltage is derated to 97% of what it is at 25°C; at -40°C, it is derated to 92%. Under these conditions, a power MOS FET rated for 400-v breakdown at 25°C must be derated to 388 v for operation at 0°C and to 368 v at -40°C, or "well below safety margins, with a failure almost guaranteed," in Zis's words. At these temperatures, a similar device rated for 450-v breakdown at 25°C would be derated to 436.5 v and 414 v, respectively.

Initially, the new power MOS FET. devices will be made available with three voltage ratings—450 V for the IVN6000KNT, 400 V for the IVN6000KNS, and 350 V for the IVN6000KNR—and will come packaged in a standard TO-3 can, with a TO-220 package to come at a later date. On-resistance for the units at 1.0 A is 2.5  $\Omega$  typically and 3.0  $\Omega$  maximum. Continuous current is 2.25 A maximum, and peak current is 7.5 A.

Thanks largely to the Z-MOS process [Electronics, July 3, p. 46], which yields density improvements on the order of 20% to 25%, the power MOS devices are believed to be priced below competitive MOS FETs, although still more costly than bipolar power transistors. However, that



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#### **New products**

could be offset to some extent by the bipolar units' slower speed and need for more complex and costlier drive circuitry.

Delivery extends from stock availability to 30 days. Units in the series cost \$10.95 (450 V), \$10.25 (400 V), and \$9.50 (350 V) each in quantities of 100 to 999.

Intersil Inc., 10710 Tantau Ave., Cupertino, Calif. 95014. Phone (408) 996-5000 [411]

### Telephone speech chip interfaces 2 to 4 wires

A monolithic speech circuit in a 14lead dual in-line plastic package, replaces the hybrid circuit in telephone handsets. The LS285A interfaces two wires with four, so that the sending signal from the handset's microphone does not reach the receiving capsule except as a controlled amount of sidetone. The chip lets the same type of transducer serve sending and receiving circuits. Upon sensing the line current, the LS285A adjusts the gain on both sending and receiving amplifiers to compensate for the line attenuation. In lots of 1 to 99, the circuits sell for \$9 apiece and are available now from stock.

SGS-ATES Semiconductor Corp., 240 Bear Hill Rd., Waltham, Mass. 02154. Phone (617) 890-6688 [414]

## Counter with MNOS memory generates own voltage

To ease interfacing with TTL or complementary-MOS logic, a six-decade up-counter generates its own voltage for a nonvolatile metal-nitride-oxide-semiconductor memory. The integrated circuit comes in three versions: a batch counter and two lapsed-time indicators. The MN9106 batch counter has an overflow latch that is activated when the counter hits 999999; the MN9107 lapsed-time indicator will display up to 99 hours, 59 minutes, and 59 seconds; the MN9108 displays 10,000 hours less 1 minute.

The counters operate off a standard 12-V or a dual power supply. The manufacturer guarantees data retention for one year without external power. The synchronous six-decade counter operates from dc to 100 kHz and has 64 bits of MNOS memory, a self-scanning multiplexer, seven-segment display drivers, and an on-board voltage generator. All three versions are in stock and sell for \$15 apiece if purchased in quantities of 100.

Plessey Semiconductors, 1641 Kaiser Ave., Irvine, Calif. 92714. Phone (714) 540-9979 [415]

#### E-beam lithography fits 16-K static RAM on one chip

A 16-K very large-scale integrated static random-access memory has been fabricated with electron-beam lithography. The 16-kilobit static memory on a single chip is equivalent to a 64-K dynamic memory, says the manufacturer, but fits on a chip only about half the size. The RAM has a maximum access time of 200 ns and maximum power dissipation of 600 mw. It is organized as 2,048 by 8 bits and uses fully static circuitry that requires no clocks or refreshing. N-channel silicon-gate MOS technology allows for directly TTL-compatible inputs and outputs, as well as operation from a single +5-V power supply.

The model MSM 2128 comes in a 24-pin dual in-line ceramic package. It sells for \$105.60 apiece in quantities of one to 24, \$87 for 25 to 99, and \$72 for 100 to 999.

OKI Semiconductor, 1333 Lawrence Expressway, Suite 401, Santa Clara, Calif. 95051. Phone (408) 984-4840 [417]

### Memory management unit for Z8000 sells for \$187

Zilog's recently announced Z8010 Memory Management Unit for the Z8000 microprocessors family [Electronics, April 10, p. 134] is available in sample quantities for \$187 apiece.

# Motorola's unique multi-million dollar facility in Joplin...



a meaningful new factor in your CRT Display decisions.

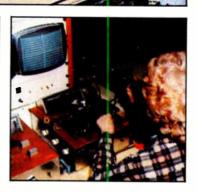
Make; buy; where to buy? If you are involved with CRT Display decisions, the new Motorola facility in Joplin, MO, is of vital interest to you. It houses the most inventive and exacting production and in-line testing equipment ever designed to achieve the ultimate in consistent quality conformance for CRT display systems.

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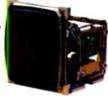
Beginning with basic components manufacturing, the Joplin plant is equipped with the latest in programmed sequencing and automatic insertion. New production line techniques keep handling to a minimum as circuit panels move through assembly and self-soldering stations. Verified at every stage, the panels must then pass testing on Motorola's futuristic Video Display Analyzers. No faulty focus or resolution; no blemish; no linear or geometric flaw can escape detection. Finally, samples of every

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#### **New products**

The Z8010 MMU offers dynamic segment relocation and memory protection for each of the Z8001's 8megabyte address spaces. Each unit has 64 randomly accessible segments that range in size from 256 bytes to 64 kilobytes. These can be mapped into a total physical address space of 16 megabytes. The logical structure with which the device provides the memory space is largely independent of the data's physical location. It prevents such errors as attempts to execute data and the unauthorized access to memory resources of data. It also protects the operating system from unexpected access by the user.

The Z8010 MMU also supports high-level language requirements crucial to the selection of 16-bit microproessors. Multiple MMUs can be used to support several translation tables.

Zilog, 10340 Bubb Rd., Cupertino, Calif. 95014. Phone (408) 446-4666 [416]

Single-chip quad op amp uses 0.38 mW per channel at 5 V

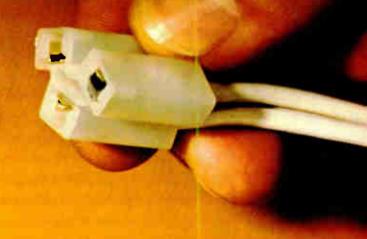
The OP-420 single-chip, bipolar quad operational amplifiers [Electronics, July 3, p. 166] can be used with either single or dual power supplies having voltages as low as +3 V, ±1.5 v. Maximum power consumption is 0.38 mW per op amp when the unit is operated off a 5-V supply. The device has an open-loop gain of 800 V/mV (110 dB) minimum on each channel and consumes a total of 220  $\mu$ A at  $\pm 15$  V. Input offset voltage is typically 500  $\mu$ V, with a drift of less than 5  $\mu$ V/°C. Two versions of the device have maximum offset voltages of 3.5 mv.

In 14-pin hermetic dual in-line packages, the OP-420 op amps are rated at -55° to +125°C for military applications (suffix BY and CY); -25° to +85°C for industrial (FY and GY); and 0° to 70°C for commercial (HY). All versions are available from stock and range in price from \$18.50 to \$5.25 apiece in 100-piece quantities.

Precision Monolithics Inc., 1500 Space Park Drive, Santa Clara, Calif. 95050 [413]

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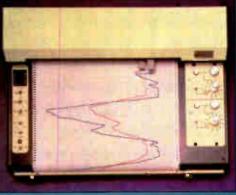
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#### **Products newsletter.**

## One more local carrier joins the Ethernet competition

A packet-switching coaxial-cable network—the Alphanet from Alpha Professional Systems Inc. of Beverly Hills, Calif.—joins the swelling ranks of local networks that aspire to compete with Xerox's Ethernet [Electronics, June 5, p. 89]. Although not a passive network like Ethernet, Alphanet will be made compatible with the combined Digital Equipment Corp., Intel, and Xerox specifications for Ethernet when those are released later this year. The Alphanet controller that is at the core of the new network will link to a keyboard, a video display, an 8085 microprocessor with 64 K of random-access memory, dual minifloppy-disk drives, and software to form a word and data processing network for under \$6,000 per station. The network, which is slated for delivery in the third quarter of this year, transmits data at 1 Mb/s.

## Josephson junction simulator operates at room temperature

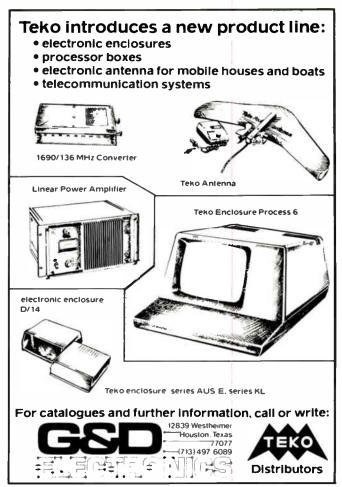
A newly formed Beaverton, Ore., company—Philipp Gillette and Associates—has created a \$245 Josephson junction simulator based on conventional circuitry. The Josephson Junction Analog allows the user to design circuitry around Josephson junctions, then observe simulated junction oscillations and transient-switching behavior without having to create the near-absolute-zero temperature environment in which a real Josephson junction device would operate. The unit provides simulation at lower speeds and higher voltages than such a device: it operates at 100 ms and 1 v, not at the usual 15 ps and 10 mv of a typical Josephson junction circuit. The simulator lets the user adjust the critical current and monitor the junction supercurrent on its own separate terminal.

#### TI second-sources RS-422 and RS-423 Schottky diodes

With the intention of blanketing the market for data-communications line circuits that meet the Electronic Industries Association's RS-422 and RS-423 standards, Texas Instruments Inc. has introduced a variety of low-power Schottky chips that second-source circuits built by other manufacturers. Among the quadruple- and dual-line drivers and receivers to be second-sourced are the AM26LS31 and -32 from Advanced Micro Devices, the MC3486 and -87 from Motorola, and the  $\mu$ A9636 and -37 from Fairchild. It will also provide an alternative version of the N8T26, a quadruple bus transceiver from Signetics. The new chips are available now, priced at between \$1 and \$2.30 each. They supplement the Dallas company's own line of SN75172 through -175 family, which also provides party-line capabilities that go beyond the RS-422 standard.

### AMI enters military market with S6800s

American Microsystems Inc. of Santa Clara, Calif., is offering 10 military versions of the S6800 microprocessor and memory products, each screened to MIL-STD-833, method 5004. The chips, which operate over a -55° to +125°C temperature range, include the S6800, S6802, and S6808 microprocessors and microcomputers; the S6810 1-K static random-access memory; the S6821 peripheral interface adaptor; the S6840 programmable timer; the S6852 synchronous serial data adapter; the S6831B 16-K read-only memory; the S5101 (256-by-4-bit) complementary-MOS static RAM; and the S6508 (1,024-by-1-bit) static C-MOS RAM. The chips come in two class B versions, one for method 5004 and one for method 5004.0, and in a class C version. The class B, method 5004 version of the S6800 costs \$42.60 each in quantities of 1,000 or more.



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#### **New literature**

Transducer interfacing. "Transducer Interfacing Handbook—A Guide to Analog Signal Conditioning" tells how to connect transducers to systems for sensing temperature, pressure, force, level, and flow. The 100-page book contains nearly 100 application examples illustrating transducer principles and shows the user how to apply them in electronic circuits for measurement and control. It sells for \$14.50 and is available postpaid from Analog Devices Inc., P. O. Box 796, Norwood, Mass. 02062.

Bus bars. "Mini/Bus," a 24-page brochure, describes the design and applications of the series Mini/Bus printed-circuit-board bus bars. The brochure gives alternative uses for the bars under and between the rows of integrated circuits on the pc board. It also includes a short article on how to assemble a complex breadboard and an in-depth discussion of electrical characteristics. Standard specifications, ordering information, and mounting guidelines for each configuration are also given. Rogers Corp., Bus Products Division, Circuit Systems Group, P.O. Box 700, Williams Field and Dobson Road, Chandler, Ariz. 85224. Circle reader service number 422.

Peripherals. A 12-page catalog describes computer peripheral equipment that can be rented, leased, or purchased. The equipment available includes cathode-ray-tube terminals, storage devices, data-communications systems, desktop computers, controllers, calculators, and logic analyzers. Manufacturers represented in the catalog include Digital Equipment Corp., Hazeltine, Hewlett-Packard, Lear Siegler, Diablo, Texas Instruments, Fluke, Biomation, and Tektronix. Prices quoted are for a one-month rental and a one-year operating lease. U.S. Instrument Rentals, 2121 South El Camino Real, San Mateo, Calif. 94403 [423]

Pulse transformers. A 14-page engineering handbook on pulse transformers provides a short introduction to these parts, as well as to their

## Ask yourself some loaded questions about bare board testing.

As loaded PC boards become more complex and more costly, ask yourself some questions about owning an electrical test system for bare boards. A system that insures fault-free boards before they're loaded.

Why should I consider electrical testing at the bare board rather than the loaded board stage?

Faults at the loaded board stage are more costly, time-consuming and impractical. And visual inspection is often not enough. Electrical testing at the bare board stage is designed to detect faults early to increase yield, reduce cost. The Everett/Charles Test Equipment, Inc. Series 50 evaluates a 120 square-inch reference circuit board with .015-inch lines and spaces and 28,672 test points in less than 15 seconds. Yield is 240 boards per hour. Visual inspection of the same board takes 10 minutes, yield is 6 boards per hour.

Electrical testing sounds great, but would it be too much of a financial load for my

present operation?

That depends on the volume of your production. But chances are that you'll more than break even with a reasonable total capital investment in fixturing and test equipment. At the current factory labor rate for visual versus electrical inspection, compare a 10-minute visual inspection that costs \$1.50 per board to a 15-second electrical, one-minute visual inspection that costs just 29¢ per board. Electrical testing represents a savings of over \$1,200 per 1,000 boards. And there's no comparison in accuracy between the two test methods.

3 Is the Series 50 loaded with test options?

There's a variety of efficient ways to do electrical bare board testing with the Series 50. From the simple red light/green light for bad board/good board testing to the fully

translated output on an alphanumeric printer for specific failure information. With any test method, the Series 50 gives high-speed

scanning for fast programming, fast test times.

### Will i be overloaded with programming problems?

Not at all. Programming is automatic from a known good board. There's no complex or expensive programming needed, no specially trained personnel required.

## What's so special about the Everett/Charles Test Equipment Series 50?

The highest test speeds available for shorts and continuity. And it resolves high resistance shorts. Not to mention the Series 50's "Dwell Time," modifiable for abnormally high capacitance found in highly complex, multi-

layer assemblies. In fact, the Series 50 can modify systems default settings to accommodate a number of open and short threshold limits.

#### Will the Everett/Charles Test Equipment Series 50 take a load off my mind for bare board testing?

Definitely. It's reliable, cost effective and fast. The Series 50 is a well designed, well integrated system that's easy to program, easy to fixture and modifiable to meet future needs. Don't wait until the loaded board stage to test. For fault-free testing at the bare board stage, there's no question about it. The Everett/Charles Test Equipment, Inc. Series 50.



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#### New literature

specifications. The handbook, which also contains diagrams for the various case sizes of the transformers, is available from Hans Schaffner's U. S. representative, Power Dynamics Inc., 177 Valley St., South Orange, N. J. 07079 [424]

Power supplies. A power-supply wall chart features 21 ac-dc and dc-dc product families and lists input and output voltages as well as package size. The chart includes off-line switchers, switched-mode regulated dc-dc converters, uninterruptible power-supply systems, and several new products—among them a universal, supply for 51/4-in. floppy-disk drives. The reference chart includes a reply card for ordering a free 64page power source engineering guide and reference material on such topics as testing procedures and thermal management. Semiconductor Circuits Inc., 218 River St., Haverhill, Mass., 01830 [425]

Communications products. A 36page product guide, OPT-115, provides tabulated data and outline configurations for a line of optical communications products. The guide includes infrared-light-emitting diodes and injection lasers, single element p-i-n photodiodes, avalanche photodiodes, hybrid photodiodepreamplifier modules, and optical communications systems. It delves into device and system characteristics and includes a selection guide and a section on optical communications terms and definitions. RCA, Box 3200, Somerville, N. J. 08876 [426]

Active filter applications. A 20-page guide presents tables and graphs of the theoretical frequency and phase response for the 700 series family of fixed-frequency, bandpass and bandreject active filters. Besides electrical and mechanical specifications, the booklet gives the working center frequency equations and discusses their interrelationship with Q—the circuit sensitivity—in terms of realizable values. Frequency Devices Inc., 25 Locust St., Haverhill, Mass. 01830 [427]

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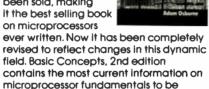
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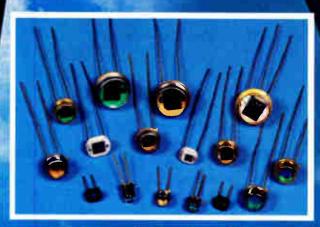
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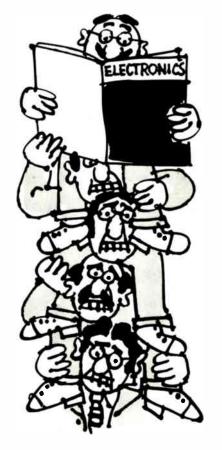
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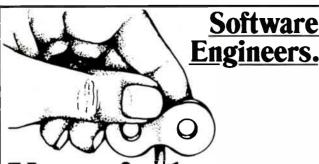
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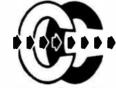
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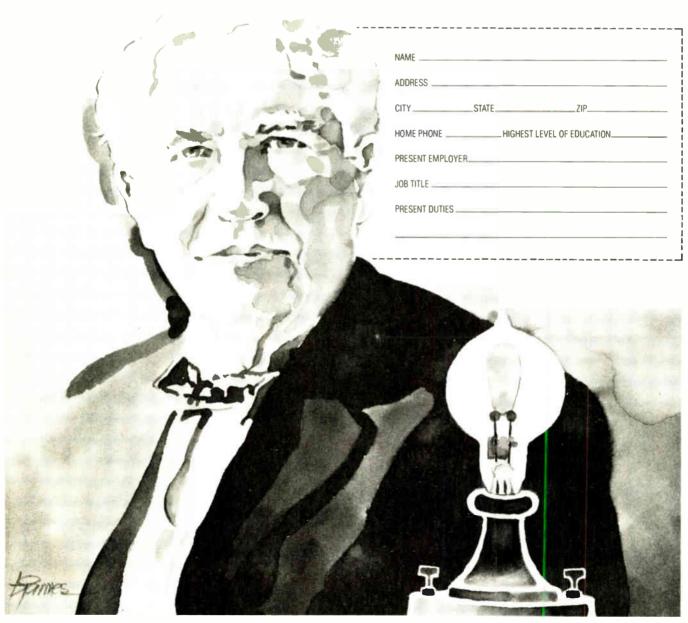
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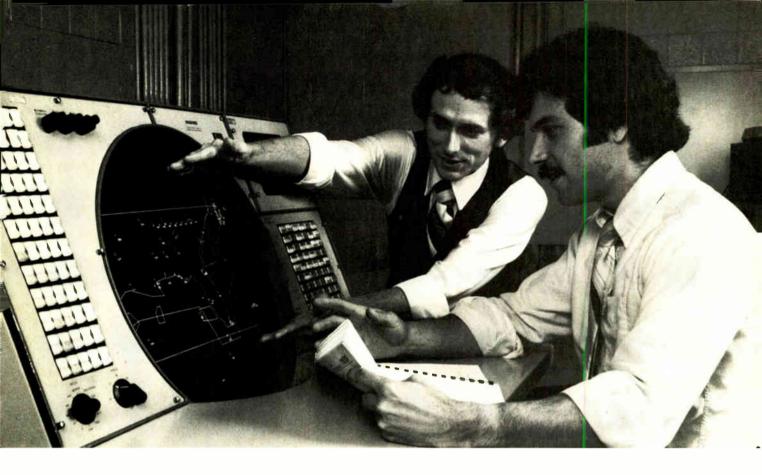
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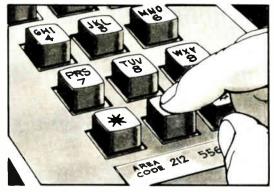
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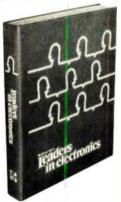
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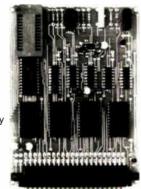
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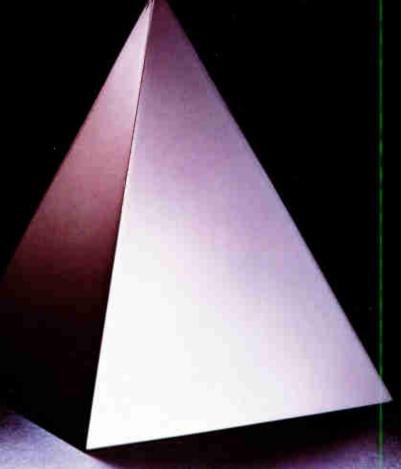
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