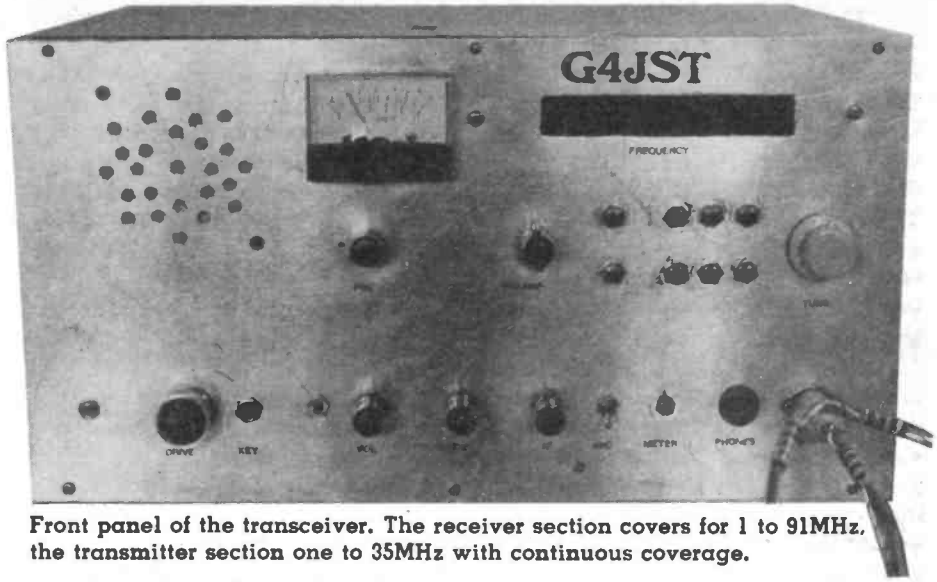
Sufficient to say that you can do a lot more than I have done with these particular systhesiser chips. For instance a VHF or UHF synthesised transceiver would be an easy task to manage. If you have any interest in adapting this type of circuit, I suggest that you write to Mullard Ltd at Mullard House, Torrington Place, London for the application note entitiled 'Versatile LSI frequency synthesiser system' M8I-0023.

Figs 2 and **3** offer just a hint of what is in the chip set. The HEF4750 combines a reference divider, set up in this circuit to provide a 10 kHz frequency from a 5MHz crystal, a crystal oscillator circuit to produce the input to this divider, a phase modulator (not used) and two phase comparators.

The chip provides two phase comparators to enable a fast locking speed combined with a very high frequency stability. It achieves this by running the first comparator, an edge triggered flip-flop arrangement, at ten times the final comparison frequency. This raw comparator input is the FF signal from the universal divider IC (HEF4751) obtained by programmable division from the VCO. Once a rough type of lock is obtained, the edge triggered flip-flop comparator is disconnected and the high accuracy, low noise



Front panel of the transceiver. The receiver section covers for 1 to 91MHz, the transmitter section one to 35MHz with continuous coverage.

comparator (PCI) takes over. Although this circuit is also driven from the basic 10 kHz reference, the 1 kHz FS signal from the universal divider also derived from the VCO division strobes PCI into an active state on every tenth reference pulse using the edge of the reference signal (derived from the crystal oscillator) as the absolute timing reference.

Although the system is as complicated as it sounds, it works exceptionally well. The real strength lies in the analogue comparator section (PCI). It provides incredibly high phase comparator gains — the output voltage of the section as a funtion of the phase shift between the divided VCO signal phase and the reference signal phase — enabling high stability at low reference frequencies. The initial transceiver design uses a channel spacing of 1 kHz with interpolation provided by a fine tuning control. The addition of two CMOS 4000 series ICs will enable the unit to operate at 100Hz spacing with no sacrifices in performance. A commercial communications receiver manufactured by Redifon uses the same chip set down to 10 Hz spacing with professional standards of synthesiser performance. Details

FIG. 3

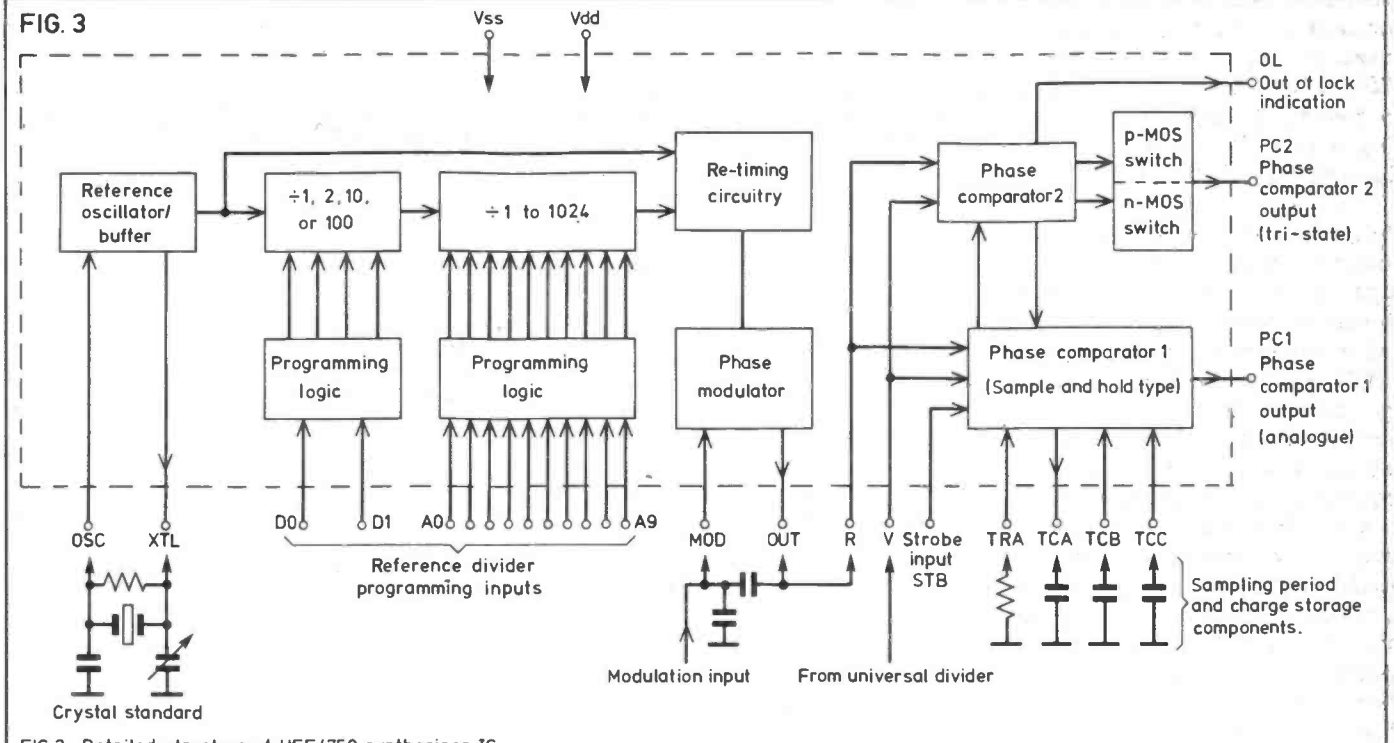


FIG. 3. Detailed structure of HEF4750 synthesiser IC