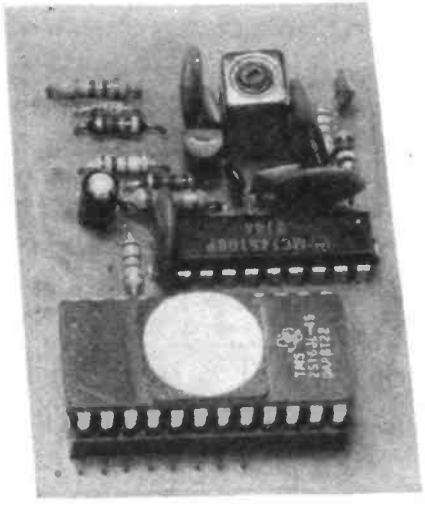
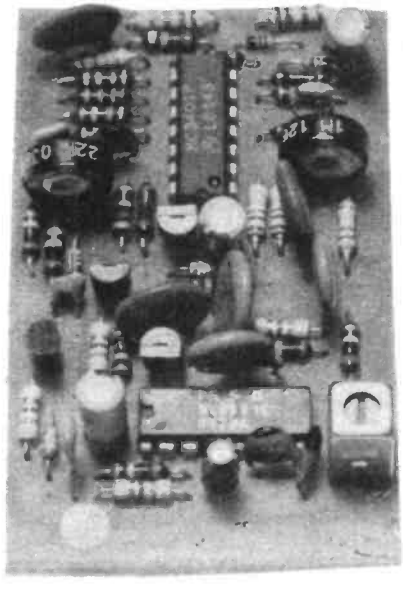
circuit to operate at any required frequency within the capabilities of the counter and the VCO. To remove the gaps on the FCC sets, suitably programmed EPROMs could be used as follows. In the case of the sets using the straight binary input PLL where the original synthesiser can remain in situ, the technique adopted is to cut the tracks from the switch to the device, and feed the program lines from the switch to the input lines of the EPROM via the address lines, remembering to keep the lines in the correct order. See **Fig. 9.**

In the EPROM used on the board shown in **Fig.4** the least significant digit is fed to address line 8 and the most significant to address line 3 in the case of 6 bit BCD. Address line 2 is used as the T/R line





to introduce the offset of 455kHz in the specific program on this EPROM but in the case of straight binary, address lines 8 — 1 are used as inputs. A suitable board layout for the code transfer is shown (**Fig.9**). This provides a facility for introducing a 5V regulated supply. It will be found in many cases that the leakage at the input of the EPROM address lines is so low that static charges can build up. It is therefore advisable to install pull-down resistors (50K — 500K 1/8 watt), across the wide earth line in the centre of the board. (Shown in **Fig.9.**

The loop filter shown in the diagram of the 145106 devices is important and due to its critical nature, when the system is being used as an alternative to dedicated device it is important to completely isolate the original loop filter to avoid incompatibility problems.

In order to explain the technique still further perhaps a look at a typical binary indication would help. In view of space restrictions only certain channels will be shown but the sequence, being additive should be easily followed as indicated in **Table 1.** (For further information on binary codes see appendix 3).

In the first example a difference offset frequency in which the VCO would be operating in the 36MHz region is shown. The offset frequency could be derived from a crystal oscillator operating around 37MHz or the circuit could use a 17MHz VCO with the 10.240 crystal oscillator being doubled to 20.48MHz if mixed with the 17MHz VCO this would give a down count for an increase in VCO frequency. Both techniques are used.

Table 1

Frequency	Code Sum	256 7	128 8	64 9	32 10	16 11	8 12	4 13	2 14	1 15	Powers of 2 Pin Number
27.601 9-15 only with	74	0	0	1	0	0	1	0	1	0	Using pins
27.701 technique	64	0	0	1	0	0	0	0	0	0	down count
27.801	54	0	0	0	1	1	0	1	1	0	
	256	1	0	0	0	0	0	0	0	0	Using all pins 7-15
	257	1	0	0	0	0	0	0	0	0	and up count
	260	1	0	0	0	0	0	0	0	0	
	511	1	1	1	1	1	1	1	1	1	
26.965	136	0	1	0	0	0	1	0	0	0	Pins 8-15
27.605	200	0	1	1	0	0	1	0	0	0	" "
27.995	239	0	1	1	1	0	1	1	1	1	" "
29.605	400	1	1	0	0	1	0	0	0	0	Pins 7-15