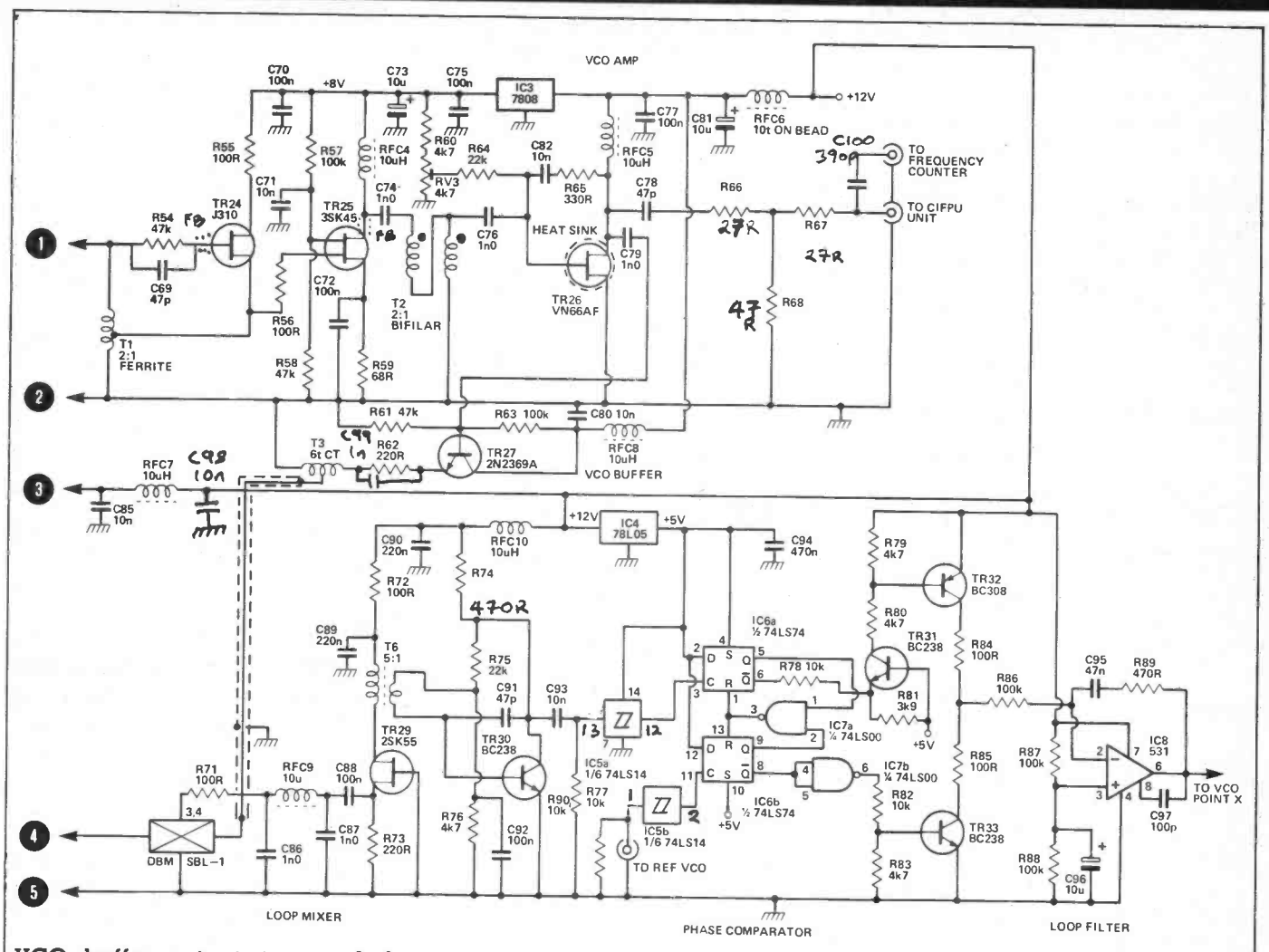


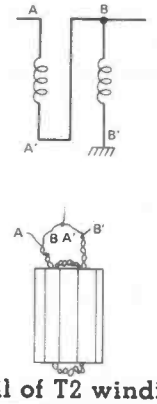
VCO, buffer, output stage and phase comparator

pcb surface.

5. Insert and solder IC1 and 2, observing orientation.

Operation of the VFO can be checked by temporarily connecting up the air spaced capacitor and applying +12v to point E. If a counter is available, attach it to point F and verify that the coverage is under 1.0MHz to over 2.0MHz. The exact limits can be set with VC1 and VC3, which should be adjusted together, and with the core of L1. The inductor sets the lower frequency limit, and the capacitors the upper — the adjustments interact and will need to be repeated a few times. We suggest +/— 50kHz extra coverage each side of nominal.

The RIT circuit adjustments should now be checked by connecting up the potentiometer and switch as shown inthe diagram. With +12v applied to point C, and the switch open, there should be no effect on the frequency as the pot is varied. Closing the switch should bring the circuit into operation, with the pot varying the frequency as it is rotated — near its central position it should agree with the switch open frequency. The actual RIT swing available will vary depending on the frequency to which the VFO is tuned. Near the low end it will be about +/— 5kHz, and at the top end about +/— 9kHz.



Detail of T2 winding

The alternative switch positions are for allowing ITT (Incremental Transmitter Tuning (or TIT (!) if you follow the RIT convention, rather than IRT) ie allowing the control to vary the frequency in the Transmit mode rather than the receive mode, and IRTT, where the control sets the frequency both in Transmit AND receive. These variations can be quite useful when working Dx-peditions, or keeping up with fellow 'Net' operators. The control voltages are derived from the Logic Control Unit, to be detailed next month.

Mechanical Construction

The photographs and drawings should be self explanatory in this respect. They suit the air-spaced variable capacitor which is supplied with the kits, but other capacitors can be use. The important point is that the spindle should be in the position shown if the final case layout to be given is used. The VFO