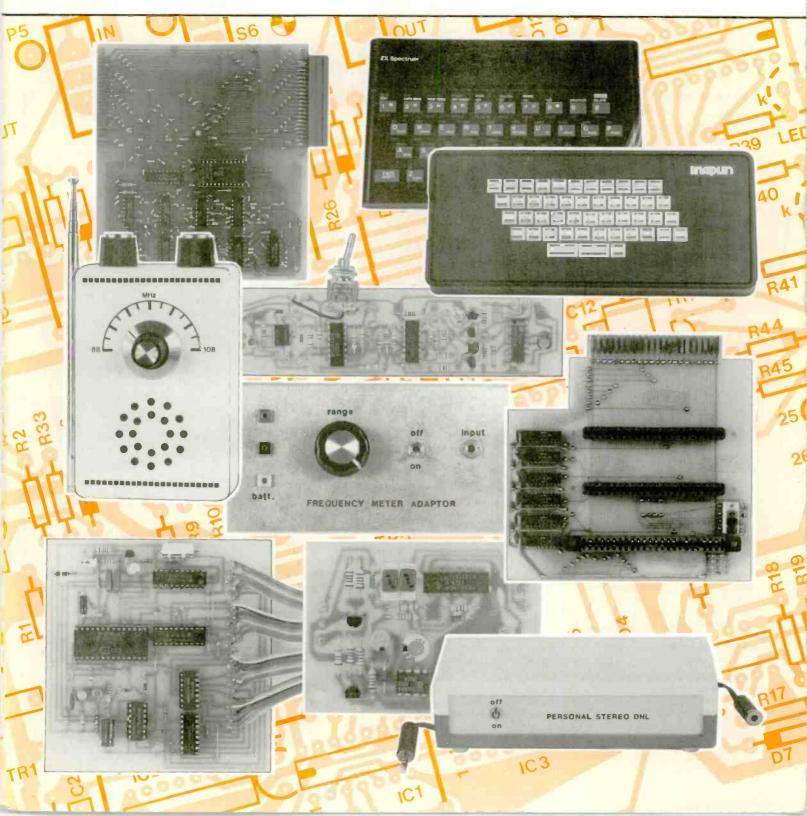
MAPLIN PROJECTS BOOK NINE

KEYBOARD FOR ZX SPÉCTRUM FREQUENCY METER ADAPTOR TTL/R5232 CONVERTER ORIC 1 TALKBACK TDA7000 RADIO 5 BOB'S WORTH PERSONAL STEREO DNL LOGIC PULSER HI-RES GRAPHICS FOR ZX81 VIC 20 EXTENDIBOARD



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PROJECT BOOK NINE

This Project Book replaces issue 9 of 'Electronics' which is now out of print. Other issues of 'Electronics' will also be replaced by Project Books once they are cut of print. For current prices of kits, please consult the latest Maplin price list, order as XF08J, available free of charge.

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Editor Production Manager Technical Editors Doug Simmons Gordon Andrews Robert Kirsch, Dave Goodman Art Director Technical Artists Peter Blackmore Roy Smith John Dudley Published byMa
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KEYBOARD

By Dave Goodman

* Full size, Full travel, 47 Keys

- * Multi colour legend for keys
- Single key mode selection
- * Plugs directly into expansion port
- Absolutely no soldering or dismantling of the Spectrum is required
- * Can accept Atari-type Joysticks

A full size keyboard with positive action mechanical keys, which simply plugs into the Spectrum expansion socket. Additional single key mode' selection is featured for GRAPHICS, SHIFT LOCK, CAPS LOCK, DELETE and EXTended keyboard; also a spare key is fitted which can be wired for personal requirements, such as system reset or interrupts. Atari type 'joysticks' can be fitted, with the addition of one or two (left/right) PCB plugs, thus allowing faster control of your programs and high speed games.

The keyboard connects to the Spectrum using a moulded cable and adaptor unit, which has an extension 2 x 28 way edge connector. Peripheral devices can still be fitted and all Maplin Spectrum projects will function normally with this system.

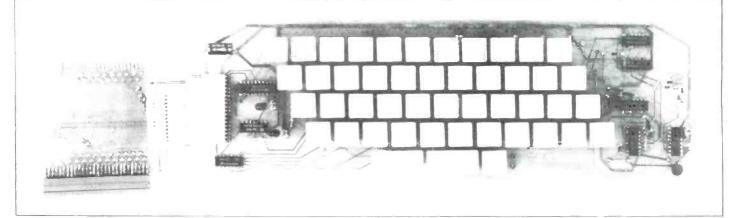
Circuit Description

Keyboard scanning is initiated with an I/O request from the Spectrum ULA I/C during a Z80 READ cycle and occurs when address line AO is low OV.

IC2 A, B decode this condition and enable both Address and Data line Buffers IC1, 6. The keyboard is scanned horizontally and vertically to register keys pressed at the cross points of the matrix. To simulate correct multi-key operations for the five 'mode' select keys, a tri-state buffer IC8 and open collector output buffer IC7 are used, which make the appropriate cross connections when active.

Caps lock mode is set by operating flip-flop IC4A. Pic 7 latches low and IC8A is enabled by D1. Scanning pulses presented by IC1A pin 14 appear at IC7 pin 12 and hence data line D0,via IC6 pin 9. Pull up resistor R5 supplies a high impedance +5V for positive going signals as IC7 can only sink current and not source it. SHIFT LOCK, functions in a similar manner by enabling IC8D from D2 and IC4B. LED 2 operating shows this mode is selected and also holds 'CAPS LOCK' key high from IC4B Pin 10, thereby preventing selection of CAPS LOCK when SHIFT LOCK is active. Spectrum owners will realise that extended keyboard mode is selected when operating both these keys together.IC4A Pin 6 also prevents 'SHIFT LOCK' from being selected when 'CAPS LOCK' is active

IC5A and B are both monostables which apply a single negative going, 75ms pulse, when keyed, 'GRAPHICS 2' momentarily operates IC8A,C or CAPS SHIFT and 9 keys, setting [G] mode, while 'EXTEND' momentarily operates



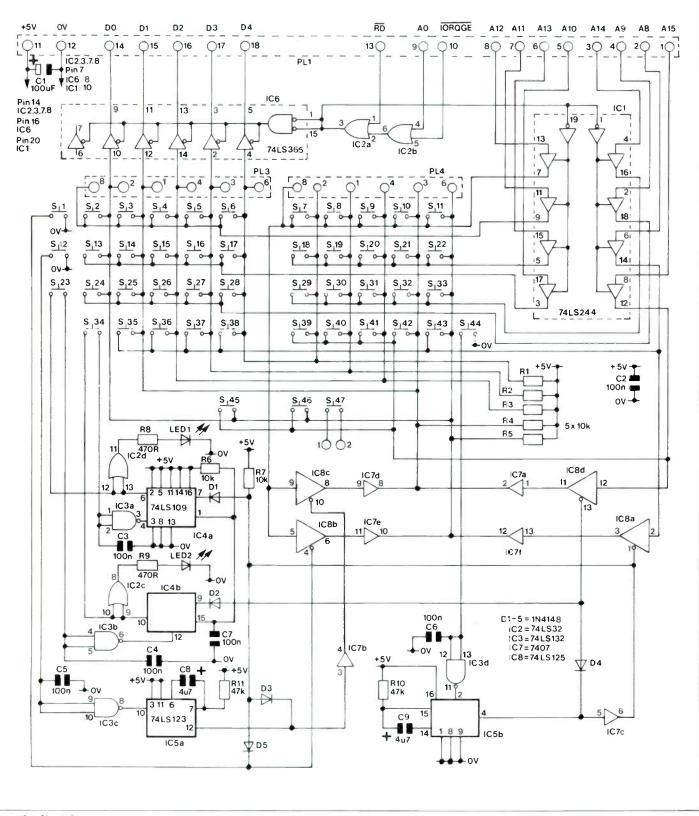


Figure 1. Circuit Diagram

IC8A and IC8D setting [E] mode. Construction (Keyboard)

Begin construction by fitting resistors R1 to 11 on the board. Diodes D1 to 5 are now bent to shape and inserted into their respective positions. A white line drawn on the legend represents the cathode band, printed at one end of the diode which must be fitted correctly. Next insert IC's 1 to 8. Sockets are not necessary here although they can be fitted if so desired. Fit capacitors C1 to 9 noting that C1, 8 and 9 are polarized and must be orientated correctly. Solder all components onto the PCB - side 2 and remove excess wire etc. This board is double faced and all holes are plated through joining tracks together on both sides so ensure that components are correct before soldering, otherwise they can be difficult to remove afterwards.

Now insert PL1, with right-angled

terminals facing out towards the end of the PCB, and mount all 47 keys. Fit 45 single and 2 double key tops (SPACE BAR), which may need slight readjustment if they appear twisted, and finally fit LEDS 1 and 2. Solder remaining components, clean excess flux or solder from the board using suitable solvents, and make a good inspection looking for poor joints and track shorts. This is well worthwhile and may help to prevent damage when power is applied.

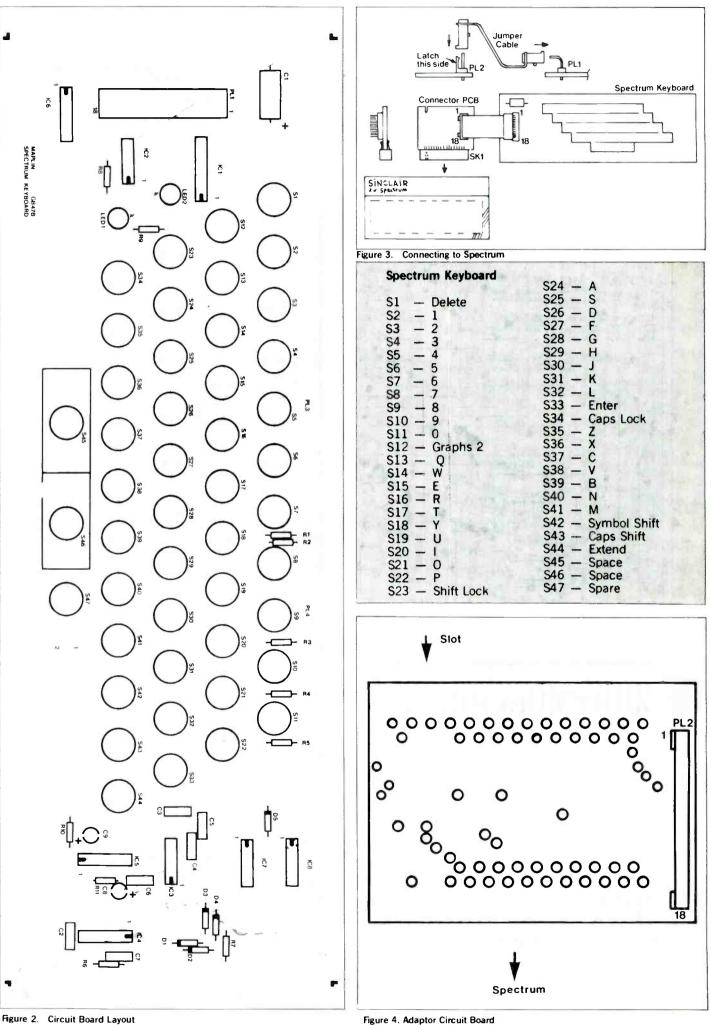


Figure 2. Circuit Board Layout

Construction (Adaptor PCB)

There are sixty four track pins to be inserted into all holes marked with a circle, and they must be soldered onto both sides of the PCB. Push them down onto the pads with a soldering iron to ensure they protude through the other side before soldering. Position a 2 x 28 way socket over the edge connector without a slot cut in position five. A blank pad exists in this position, which aligns with the socket locating peg. Solder all fifty four terminals onto the edge pads very carefully and avoid solder shorts between them. Finally, insert the 18 way vertical Minicon socket and solder in position. Check for shorts etc. on the board and insert into the Spectrum expansion socket on the back panel.

Testing

With only an adaptor unit in place, apply power to the computer and television. Check that the Spectrum keyboard functions normally. Switch off and fit the connecting cable between adaptor and remote keyboard PCB. Reapply power. The Sinclair copyright notice should appear, as usual, but the Spectrum keyboard will now be inoperative. Try all keys in every mode to ensure correct operation, see TABLE 1.

SPEC	TRUM	KEY	BOARD

Resistors - All	0.4W 1% metal film		
R1-7 inc	10k	(7 off)	(M10K)
R8,9	470R	(2 off)	(M470R)
R10,11	47k	(2 off)	(M47K)
Capacitors			
Cl	100uF 10V Axial Electrolytic		(FB48C)
C2-7 inc	100nF Disc Ceramic	(6 off)	(BX03D)
C8,9	4u7F 16V Tantalum	(2 off)	(WW64U)
Semiconductor	5		
D1-5 Inc	1N4148	(5 off)	(QL80B)
IC1	74LS244		(QQ56L)
IC2	74LS32		(YF21X)
IC3	74LS132		(YF51F)
IC4	74LS109		(YF44X)
IC5	74LS123		(YF48C)
IC6	74LS365		(YH11M)
IC7	7407		(QX76H)
IC8	74LS125		(YF49D)
LED1,2	Red LED	(2 off)	(WL27E)
Miscellaneous			
\$1-47 inc	Keyboard Switch	(47 off)	(FF61R)
	Keytop 1	(45 off)	(FF62S)
	Keytop 2	(2 off)	(FF63T)
	Spectrum Keytop Print		(YK77J)
·PL1	18 way R.A Minicon Plug		(BK84F)
	Spectrum Keyboard P.C.B.		(GB47B).
Optional			
	20 pin DIL Skt		(HQ77J)
	16 pin DIL Skt	(3 off)	(BL19V)
	14 pin DIL Skt	(4 off)	(BL18U)
PL3,4	R.A. D-Range 9-Way Plug	(2 off)	(FG66W)

KEY		OPERATION
Delete		Erases previous character
Graphics 2		Cursor [G], Graphic symbols
Shift Lock	_	Red 'On Key' symbols
Caps Lock		Upper case characters
Extend	_	Cursor [E], Green 'Off Key' functions

Table 1. Modes of operation for the Keyboard.

The Extend mode remains until a function is selected, whereafter the keyboard returns to normal operation. Graphics 2, Shift Lock and Caps Lock remain in the mode selected until reoperated and Delete can be either single or repeated operation.

Joystick Ports

Plugs 3 and 4 are wired to suit Atari type joysticks and can be fitted into the PCB as an optional extra. PL3 simulates keys 1 to 5 and PL4 simulates keys 6 to 0 as shown in TABLE 2.

PL3 - (4)	KEY
Pin 1	2 (7)
Pin 2	1 (6)
Pin 3	4 (9)
Pin 4	3 (8)
Pin 6	5 (0) Fire Button

Table 2. Key Sim

Case Details

The keyboard can be fitted into a case, designed specifically for the purpose, and held in place with six plastic snap rivets. If plugs 3 and 4 are fitted, slots will need to be cut into the back panels allowing clearance for joystick plugs, otherwise the PCB will not fit!

Finally, for the less adventurous, a complete keyboard, minus plugs 3 and 4, is available from us (see Parts List for details).

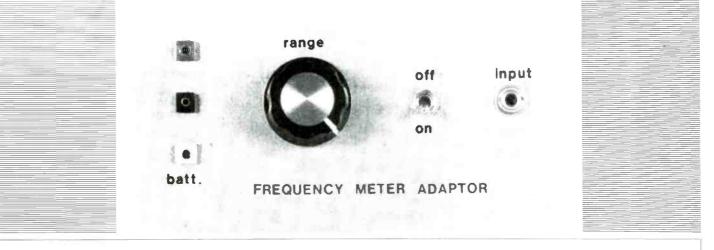
	2 (7) 1 (6)	and the second se	
	4 (9)		
	3 (8)	1 C	
	5 (0) Fire Button		
mulation	s on PL3 and PL4.		and an
		1.	COR.
OK)		augest a	100 gr
OR) 7K)		· · · · ·	
	- Contraction of the Contraction	and and	
8C)	21.3	and the	
3D)			
4U)	and the second		and a second
0B)		and an	
6L)			1 2 3 1 2 1
1X)			-
1F) 4X)			
8C)			
IM)	ADDREAD ADDREAD	Calle	
6H)	and the	11222	
9D)			
7E)			
1R)		the discount of the	
25)			
3T)	the second se		
7J)~~			
4F) ~ 7B)~	SPECTRUM CASE		
	Case		(XG35Q)
	* Snap Rivet	1 pkt	(BK87U)
7J)	* Velcromount	(2 off)	(HB21X)
9V) 8U)	* Stick on feet	(2 off)	(FW38R)
5W)			
	* These items are inc	luded in the Case (XG35(<i>)).</i>
	A complete kit of all parts to build	the Keyboard (excluding a	optional parts)
	is a	As LK29G	
	Urder	A3 LK230	
5 G) 3A)	A complete kit of all part	s for the adaptor is avail	lable
6T)		As LK30H	

A ready-built Keyboard is available, including adaptor and case Order As XG36P

ADAPTOR PL2 SK1

2	18 Way Latch Minicon Plug 2 x 28 way P.C. Edgecon 18 Way Jumper Cable	(BK85G) (FG23A) (BK86T)		
	Spectrum Keyboard Connector P.C.B. Track pin	(2 pkts)	(GB48C) (FL82D)	

Frequency Meter Adaptor



★ Turns Your Digital Multimeter into an Accurate Frequency Counter ★ Ideal For Measuring Audio Frequencies and Beyond ★ Battery Operated ★ Easy To Use

by Robert Penfold

A sophisticated frequency meter capable of highly accurate measurements at frequencies into the VHF range is extremely useful for anyone who is involved in radio communications, or certain specialised fields of audio frequency electronics. However, for most audio frequency work a relatively simple frequency meter is adequate, and costs substantially less than a high specification DFM.

This simple and inexpensive project is a frequency to voltage converter, which can be used with a digital multimeter switched to the 0 to 1.999 volts range to give a four range frequency meter having full scale values of 199.9Hz, 1999kHz, 19.99kHz, and 199.9kHz. The unit will also operate with an analogue multimeter having a suitably low D.C. voltage range, but if the full scale voltage is less than 1.999 volts the full scale value of each frequency range will be reduced accor dingly. The accuracy of the unit is largely dependent on the quality of the multimeter with which it is employed, and the accuracy with which the unit is calibrated, but results should be more than adequate for most audio frequency testing.

LM2917N

The LM2917N is a frequency to voltage converter IC which has a dual purpose comparator/amplifier output stage which enables the device to activate a relay or similar load if the input frequency exceeds or falls below a certain level, or to act as a straightforward converter. In this application it is just a simple frequency to voltage conversion that is required Figure 1 gives pinout details of the LM2917N and shows the internal stages of the device.

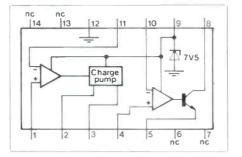
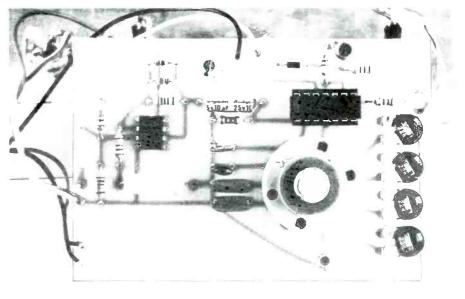


Figure 1. The LM2917 pinouts and internal circuit blocks.

An operational amplifier is used at the input, and this stage has built-in hysteresis which gives the circuit excellent immunity to noise on the input signal. The frequency to voltage conversion is carried out by a charge pump circuit which requires only three discrete components. This stage offers frequency doubling which enables a fast response time and a low ripple output to be obtained. The output operational amplifier has both inputs accessible and drives an npn transistor which can be used in either the common collector or emitter follower mode. A 75 volt zener diode enables the supply to be stabilised in critical applications.



The Circuit

Figure 2 shows the circuit diagram of the adaptor. IC1 is used as a simple non-inverting amplifier which boosts the sensitivity of the circuit by a factor of 11 times, and enables the unit to operate with an input as low as 2 millivolts RMS. This stage also gives the unit a reasonably high input impedance of about 500k Ω . D1 and D2 clip the output signal of IC1 to prevent an excessive input signal being applied to IC2.

R5 is used to bias the input of IC2 to the negative supply rail. Four switched timing capacitors (C4 to C7) give the unit its four measuring ranges, and a separate calibration preset for each range (RV1 to RV4) ensures good accuracy on all ranges. The third discrete component in the charge pump circuit is filter capacitor C8, and the value of this component is chosen to give a suitable compromise between response time and output ripple. 100pF is the lowest acceptable value for the timing capacitor, and $10k\Omega$ is about the lowest usable value for the filter (calibration) resistor, and this limits the maximum operating frequency of the unit to about 200kHz. If the input signal level is inadequate to operate the input stage and charge pump circuit properly the later fails to give an output voltage. This makes it obvious that an inadequate input level is present and prevents misleading readings from being obtained

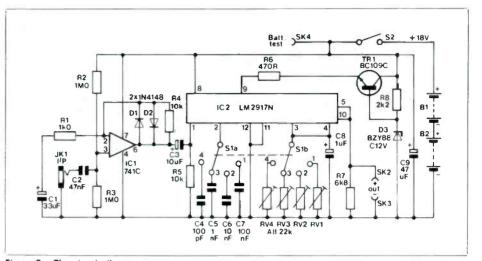
The output from the charge pump circuit is connected to the non-inverting input of the operational amplifier at the output of IC2, and this is used as a buffer amplifier having the npn transistor as an emitter follower output stage. At SK2 and SK3 this gives a low impedance output voltage which is proportional to the input frequency.

In this application a well regulated supply voltage is essential if accurate and consistent results are to be obtained. A single 9 volt battery is inadequate to give such a supply since the internal zener diode of IC2 is a 7.5 volt type, and for this to operate efficiently the supply input potential must always be at least one volt or so higher than this zener voltage. The circuit is therefore powered from two 9 volt batteries in series giving a nominal 18 volt supply, but this is fed to IC2 via a simple series regulator which is comprised of TR1, R8 and D3. The use of this regulator plus the internal zener diode of IC2 gives excellent stability with no discernable change in frequency reading if the supply is varied from 14 to 20 volts. SK4 enables the total battery voltage to be checked easily by providing an external test point. The current consumption of the circuit is about 12 milliamps.

Construction

Most of the components, including S1, are mounted on the printed circuit board, as illustrated in Figure 3. Assuming S2 is an ordinary rotary switch having tags rather than the printed circuit pins, the ends of the tags must be trimmed off using a pair of side cutters to leave what are effectively printed circuit pins that will fit into the board without too much difficulty. However, be careful to leave these pins as long as possible by trimming away no more than is absolutely necessary. In other respects construction of the board is quite normal.

An aluminium box measuring about 133 by 70 by 38mm makes a neat but inexpensive housing for the unit. The front panel layout can be seen by referring to the photographs, but from the electrical point of view the layout is not critical. However, it is advisable not to radically depart from this layout unless you





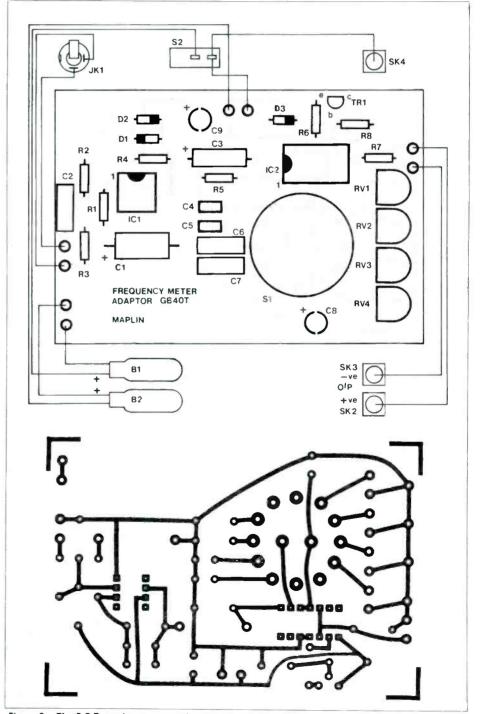


Figure 3. The P.C.B. track, component layout and wiring diagram.



by Dave Goodman

The current crop of low price home micro-computers has created a large market for peripheral devices, designed to expand the capabilities of these machines. Telephone links, via modems, make intercommunication between micros possible by using the RS232 standard, but unfortunately not all micros have the necessary +/- 12V levels available for data transmission. A method of converting 5V TTL signals to RS232 levels (or vice versa) is needed, and the converter module does just this.

Description

Regulator 1 produces +5V from the +9 to +12V input pin 1, to supply IC2. Regulator 2, which has its common input referenced to +5V, develops approximately a +10V output (dependent on the connected supply). IC1 generates a voltage, exactly opposite to its supply voltage, across C4; this being approx. -10V. Both +/-10V are present at the output stage TR1.

TTL signals are input at pin 3, and inverted by IC2. A second inverter reverts the signal back to the original and both outputs can be selected by S2. TR2 buffers the 5V signal which drives TR1 and outputs on pin 6. RS232 signals on pin 5 have negative voltages removed by D2, and R7 and D3 clamp the positive signals to +5V maximum. Two inverters then connect both input signals to S1 and output on pin 4.

Construction

Bend the leads and insert resistors R1 to R9. D1 to D3. Note that D3 is a zener, and will be a different colour. Fit the black band end to the white bar on the legend. Insert IC1, 2 and TR1,2, Regs 1 and 2 look similar to the transistors, so read the case markings carefully. Finally, fit C1 to C4, S1 and 2, and the 7 vero pins. Both switches may be inserted either way round, but C1, 2 and 4 must be fitted according to the legend. Carefully solder all components to the track, then cut excess leads and clean flux, etc, off the PCB. Inspect all components and joints before proceeding

Testing

Connect the +12V supply to pin 1, and OV to pin 2. Place a voltmeter across pin 6 and OV, and set S1 and S2 to 'NORM'. Switch on the supply, and you should read approximately +10V. 8

Converts 5V TTL to RS232, or vice versa Makes modem use possible on all micros Simple to construct

By connecting a length of wire to OV and touching input pin 3 the output should swing from +10V to -10V. Set S2 to 'INV' and repeat; this time the output should swing from -10V to +10V. Set S1 to 'NORM'.

Remove your meter from pin 6, and reconnect between OV and pin 4. The reading should be low, around +100mV. Remove the test wire from OV

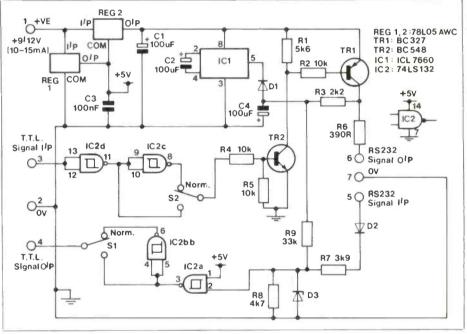
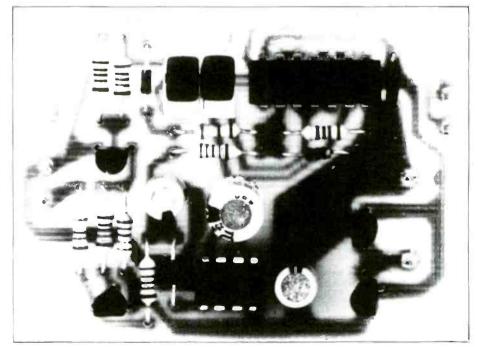


Figure 1. Circuit diagram



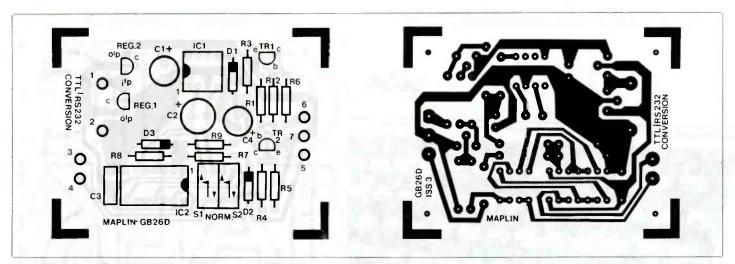


Figure 2. PCB layout and overlay

and pin 3, and connect it to +12V (pin 1). Touch the wire to pin 5 and the output should swing up to +4V. Operate S1 and the meter should read +4V. Touching the test wire to pin 5 again will produce a swing from +4V down to +100mV. Return S1 to 'NORM' position. If all is well the module is ready for use. Connect your computer TTL signal output to pin 3 and TTL signal input to pin 4. The outgoing RS232 line connects to pin 6 and the incoming RS232 line connects to pin 5. Pin 7 can be used as an OV reference or a screen, if required.

Resistors - A	II 0.4W 1% metal film unless specifi	ed		D1,2	1N4148	(2 off)	QL80B
R1	5k6		M5K6	D3	BZY88C4V7		QH06G
R2,4,5	10k	(3 off)	M10K	TR1	BC327		QB66W
R3	2k2		M2K2	TR2	BC548		QB730
R6	390R		M390R	REG1.2	78L05AWC	(2 off)	QL26D
R7	3k9		M3K9	IC1	ICL7660		YY755
R8	4k7		M4K7	IC2	74LS132		YF51F
R9	33k		M33K	Miscellaneous			
					P.C. board		GB26D
Capacitors				S1.2	DIL SPDT Single	(2 off)	XX28F
C1,4	100uF 10V P.C. electrolytic	(2 off)	FF10L		Veropin 2145	(1 pkt)	FL24B
C2 C3	100uF 25V, P.C. electrolytic FF11M 100nF Disc BX03D		A complete kit o Order				
						Contraction of the local distance of the loc	

FREQUENCY METER ADAPTOR Continued from page 7.

are quite sure that everything will physically fit into place properly. The board is fixed in place inside the case when S1 is fitted onto the front panel, and no additional mounting is required, but wire the board to the rest of the unit before finally fitting it in place. There is sufficient room for the two batteries to fit in the space beneath the board, and a piece of foam material can be used to hold them in position.

Calibration

Ideally the unit should be calibrated with the aid of a crystal calibrator having output fre-

quencies of 100Hz, 1kHz, 10kHz and 100kHz so that RV1 to RV4 can be adjusted to give the correct readings from the multimeter which is fed from SK2 and SK3. This is not essential though, and any signal source which provides known frequencies can be used as a calibration source. For optimum accuracy the calibration frequencies should represent
about 50% or more of the full scale reading of the range concerned. A good quality A.F.
signal generator should have adequate scale
accuracy, or an alternative is to use a
synthesiser or other musical instrument as
the signal source. For example, the 'A' above
middle C is at a frequency of 440Hz, with

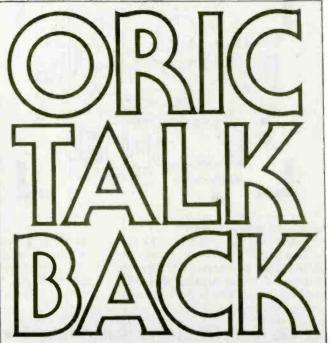
every octave increase in pitch giving a doubling of frequency, and each fall of one octave giving a halving of frequency.

Readings obtained using the unit are not significantly affected by the input waveform, and accurate results should be obtained with both symetrical and pulse signals. The circuit is also largely unaffected by the amplitude of the input signal with the output falling to zero in the unlikely event of an inadequate input signal level, but signals of more than about 10 volts peak to peak will overload the unit and could give erroneous results. It would therefore be advisable to use an attenuator probe when measuring very high level signals.

	LIST FOR FREQUEI	NCY		Semiconductors D1,2 D3	1N4148 BZY88C12V	2 off	(QL80B) (OH16S)
Resistors -	All 0.4W 1% metal film unless sp	ecified.		TR1	BC109C		(QB33L)
R1 R2,3	1k0 1M0	2 off	(M1KO) (M1MO)	IC1 IC2	uA741C LM2917N		(QL22Y) (WQ38R)
R4,5 R6	10k 470R	2 off	(M10K) (M470R)	Miscellaneous			
R7	6k8		(M470R)	S1	Switchpot 2 pole 6 way		(FH43W)
R8	2k2		(M2K2)	S2	SPST ultra min toggle		(FH97F)
RV1-4	22k hor preset	4 off		JK1	Jk SKT 3.5mm		(HF82D)
NV1-4	ZZK nor preset	4 Off	(WR59P)	SK2	2mm skt red		(HF47B)
Capacitors				SK3	2mm skt black		(HF44X)
C1	33uF 16V axial electrolytic		(FB350)	SK4	2mm skt yellow		(HF49D)
C2	47nF polyester		(BX74R)		PC Board		(GB40T)
C3	10uF 25V axial electrolytic		(FB22Y)		PP3 battery clip	2 off	(HF28F)
C4	100pf ceramic				Control Knob		(YX02C)
C5	100pr ceramic		(WX56L)		Wire		(BLOOA)
			(WW22Y)		Veropin 2145	1 pkt	(FL24B)
C6 C7	10nF polycarbonate		(WW29G)		Box type AB7		(LFO8J)
C8	100nF polycarbonate 1uF 100V PC electrolytic		(WW42V)	A	As the state to see a second state		
C9	47uF 25V PC electrolytic		(FF01B) (FF08J)	A comple	te kit of all parts, excluding Order As LK20W		ivailable.
03	and and to electrolytic		(1:00)		Under AS LK20W		



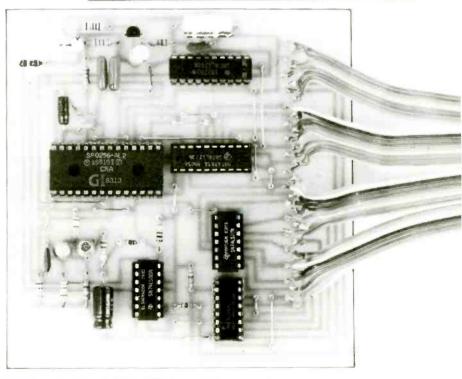


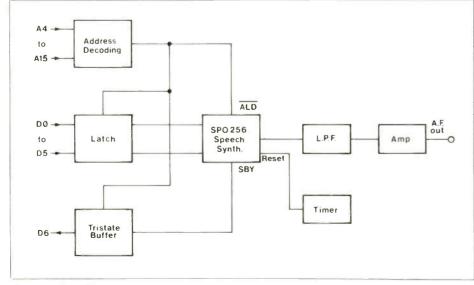


by Robert Penfold

his speech synthesiser for the Oric 1 computer, like the previous Maplin "Talkback" projects. is based on the GI SP0256 speech chip. Rather than a vocabulary of complete words, this chip provides a set of short sounds known as "allophones" which are strung together to produce the required words. This system is slightly more difficult to use than one which uses whole words, and the speech quality is not quite as good, but it has the advantage of what is effectively an unlimited vocabulary. The required phrases can be produced using a short program which takes up very little memory space.

The Oric Talkback connects to the expansion and cassette ports at the rear of the machine. Power is obtained from the Oric and the speech is reproduced through the machine's internal loudspeaker





Block Diagram

Figure 1 shows a simplified block diagram for the unit. The twelve most significant address lines are decoded to place the circuit at addresses #BFF0 to #BFFF inclusive, and this is within the unused memory area (#BFE0 to #BFFF) of the Oric 1 48k, and is also free on the 16k version where the upper 32k of memory area is unused.

Data lines D0 to D5 are fed to the six address inputs of the SP0256 chip via a latch. The SP0256 has a set of 64 allophones (including pauses), and the required allophone is obtained by POKEing the appropriate figure to any address in the range #BFF0 to #BFFF. The address decoding circuit provides a negative pulse to the Address Load input of the SP0256, and the selected allophone is then produced. The circuitry within the speech chip is very

Figure 1. Simplified block diagram.

complex, and includes a digital filter followed by a pulse width modulator which supplies the audio output signal. The output from this modulator is in the form of a signal of fixed (ultrasonic) frequency, with the pulse length being varied from a short duration, to give a low average output voltage, to a comparatively long duration to give a high average output potential. It is the average output level that constitutes the audio output signal, and a lowpass filter is used to filter the ultrasonic content of the signal to leave just the required audio signal.

As the output from the filter is at a fairly low level an amplifier is used to boost the signal to an adequate amplitude to drive the audio input of the Oric. In fact the Oric does not have an audio input, and the "SOUND" input on the cassette interface socket is intended as an audio output for use with a hi-fi amplifier. However, it also seems to work perfectly well as an audio input, and a good quality audio output is obtained. The Oric's sound generator still functions properly when the speech synthesiser is in use.

Even a programme written in a relatively slow language, such as BASIC, is capable of supply allophone addresses to the circuit far faster than the allophones can be executed. The speech chip must therefore signal to the computer when it is ready to receive another address. In this case the STANDBY output of the SP0256 is used, and this goes to logic 1 when the chip is inactive. This output is connected to the D6 line of the computer via a tristate buffer which ensures that the STANDBY output only connects through to the data bus when an address between #BFF0 and #BFFF is PEEKed. A software loop is used to read D6 and to hold up the program until this bit goes high.

The Oric 1 48k computer has 64k of RAM with the 16k at the top of the address range overlaid by ROM. At switch-on there is an initialisation period of about two or three seconds, and towards the end of this the speech synthesiser would be activated. This is overcome by using a simple timer circuit to delay the reset pulse for the speech chip until the initialisation has been completed.

The Circuit

Figure 2 shows the full circuit diagram of the Oric Talkback project.

IC1 and IC2 provide the address decoding. IC1 is a 3 to 8 line decoder, but by utilising the enable input the four most significant address lines are decoded. IC2 is an 8 input NAND gate and this is used to decode the middle eight address lines. Its output drives one of the negative enable inputs of IC1. A negative pulse is produced at pin 10 of IC1 when an address in the range #BFF0 to #BFFF is PEEKed or POKEd.

IC3 is the latch, and only six of the D type flop/flops in this device are used here. D1,D2, and R1 gate the output of

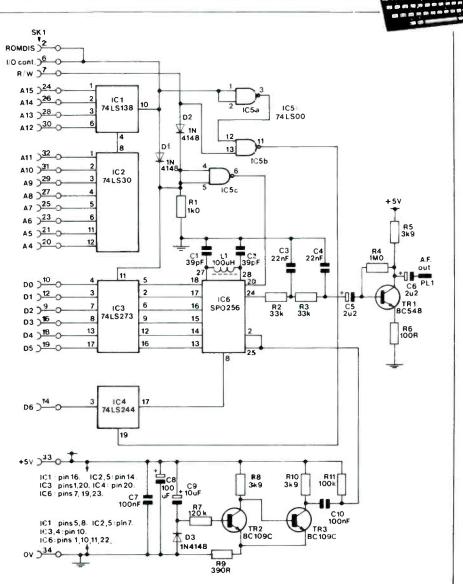


Figure 2. Oric Talkback circuit diagram.

IC1 with the Read/Write output of the computer so that the latch is only operated during a write operation to the unit. IC4 is the tristate buffer, and only one section of this octal device is used in this circuit. IC5a/b gate the output of IC1 with the Read/Write line so that IC4 is only enabled during read operations to the circuit.

IC6 is the SP0256 speech chip, and this requires a nominal 3.12MHz clock signal. This device has a built-in clock oscillator which can be used with a crystal having a resonant frequency of around 3.12MHz, but in this circuit the inexpensive alternative of a simple inductor (L1) is used. However, a crystal can be used in place of L1 if desired, and no other modifications to the circuit would be needed.

The lowpass filtering at the audio output of IC6 is provided by R2, C3, R3, and C4. TR1 is used as a common emitter amplifier which boosts the audio output of the circuit to an adequate level. The volume obtained should be perfectly satisfactory, but if desired a higher output can be produced by making R6 a little lower in value, or a higher value can be used to reduce the output level.

The negative pulse which is used to operate the latch is inverted by IC5c

and fed to the Address Load terminal (pin 20) of IC6. The speech chip Is activated at the end of the address pulse when the output of IC5c goes negative. While it might seem more logical to drive the Address Load input without the inverter stage, this method does not work properly in practice. A minor drawback with this method of activating the chip is that it does not switch off when an allophone has been completed. However, this is overcome in the software by finishing each phrase with a pause which effectively switches off the chip.

TR2 and TR3 are used as a conventional Scmitt Trigger circuit, and in conjunction with timing components C9 and R7 this provides the delayed reset pulse for IC6.

As the Oric 1 48k computer has 64k RAM chips all the addresses (including the spare ones between #BFEO and #BFFF) are occupied by RAM. When reading from an external device it is therefore necessary to disconnect from the data bus the RAM plus any other internal devices which might place an output onto the data bus. This is achieved by connecting the I/O control and ROMDIS lines to the output of IC1 so that they are taken low during read operations of the circuit.

Construction

All the components are fitted on the printed circuit board, as detailed in Figure 3. Start by fitting the link wires, diodes and resistors, and then fit the capacitors, inductor, transistors and finally the integrated circuits. It is not essential to mount IC1 to IC5 in sockets, but as IC6 is a rather expensive MOS device a (28 pin DIL) socket should certainly be used for this component. Other normal MOS handling precautions should also be observed when dealing with IC6. Be careful to fit the integrated circuits with the correct orientation.

PL1 is a 7 way DIN connector, and pin 4 or 5 of this is connected to the printed circuit board via an insulated lead about half a metre to a metre in length. It is not necessary for this lead to be a screened type. If preferred the output of the unit can be coupled to headphones or an amplifier instead of the cassette interface socket of the Oric. SK1 is a 34 way IDC header socket and this connects to the board by way of a 34 way ribbon cable, again about half a metre to a metre in length. Make quite sure that it is connected the right way round. If you are uncertain about the correct method of connection for either SK1 or PL1 refer to Appendix F on page 151 of the Oric manual.

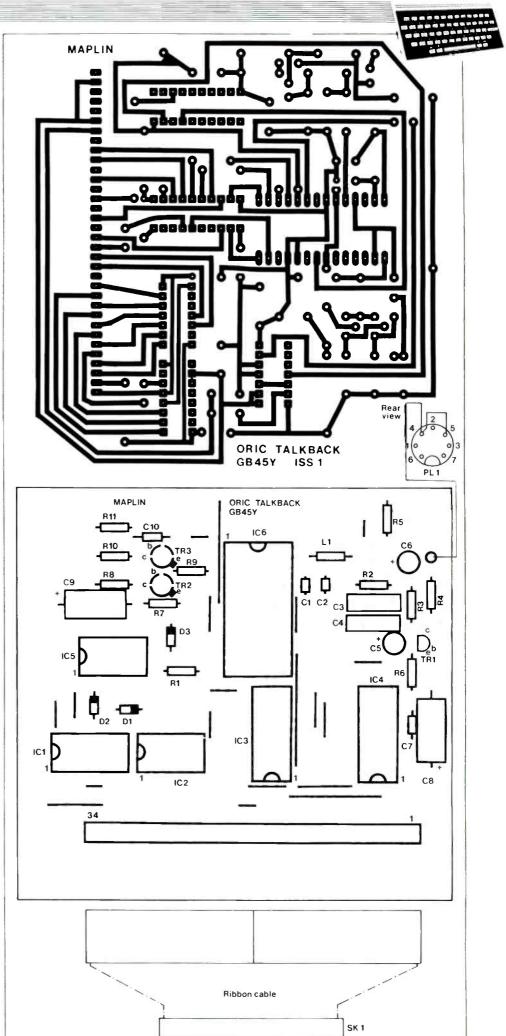
Testing

Connect the unit to the expansion port before applying power to the computer. Connecting or disconnecting the unit while the computer is operating will almost certainly cause it to "hang up", and could conceivably result in damage to one or other of the units. If the synthesiser is operating properly a quiet "click" should be heard from the loudspeaker a few seconds after switch on when the SP0256 is reset. Using the command POKE #BFFF,55 should give a noise sound from speaker, and POKE #BFFF,2 should switch off the noise. Assuming all is well, one of the test programs can then be tried.

Software

More information about speech synthesis and the use of allophones can be found in issue 6 of this magazine. Please note a copy of the article on Allophones is supplied with the kits.

As the number of allophones will vary from one phrase to another it is awkward to use FOR. NEXT loops since the number of steps must be matched to the number of allophones. A REPEAT...UNTIL loop as in listing 1 is a better solution. A value of 130 is used at the end of the DATA to terminate the loop, and the lower six bits are read by the speech synthesiser as 2 so that the pause to switch off the synthesiser is obtained. 65 could be used as the terminator, but a three digit number stands out better and this is helpful when debugging or altering a program with more than one phrase. Line 40 12



Pcb Layout for The Oric Talkback

180 UNTIL SPEECH(S~1,PHRASE)>128 190 UNTIL FALSE	
170 S=S+1	
160 REPERT: UNTIL(PEEK(#BEFE)AND64)	
(50 POKE #BFFF,SPEECH(S,PHRASE)	
140 REPERT	
130 5≖0	
120 GET PHRASE	
110 REPEAT	
100 UNTIL N>3	
90 N=N+1	SØ DATA 16.6.2.63.24.41.55.130
SØ UNTIL ALPHN>63	70 DATA 45,7,17,2,16,19,2,32,17,2,24,35,2
70 PHRASE≍PHRASE+1	60 DATA 46.7.11.2.59.2.49.22.2.61.53.19.56.2.13.22.2
50 SPEECH(PHRASE,N)=ALPHN	50 UNTIL A>63
50 READ ALPHN	40 REPEAT:UNTIL (PEEK(#BFFF)AND64)
40 REPEAT	30 POKE #BFFF,A
	20 READ A
20 REPEAT	10 REPEAT
0 DIM SPEECH(20/3)	5 REM listing 1

Listings 1 and 2

reads input line D6 and provides the delay until the SP0256 signals that it is ready to receive another allophone. Although it may appear that "=64" has been omitted from this line, due to the way in which Oric BASIC works this is unnecessary and would simply slow things down. The program includes a sample phrase in lines 60 to 80.

A problem with Oric BASIC is that it is not possible to RESTORE to a particular line number - only to the start of a DATA list. This makes it difficult to hold phrases in a long program where data statements may also be used for other purposes, such as redefining characters and for SOUND statements. The most elegant way around this is to READ the DATA into arrays at the start of the program, as in listing 2. The first part (10 - 100)READs the data into the array SPEECH. This can hold four phrases of up to 21 allophones (remember that element 0 is valued in Oric BASIC).

The second part produces the speech, and line 120 lets you choose a phrase by pressing a number key (0 to 3). Lines 110 to 190 could be made subroutines in a large program, with RETURN added at the end. Line 120 should then be omitted, and PHRASE passed as a variable when calling the subroutine (e.g. PHRASE = 3 : GOSUB 100). With the example phrases pressing keys 0 to 3 in that order produces a message from MAPLIN.

ORIC TALKBACK

URIC IA	LNDAUN		
Resistors - All	0.4W 1% metal film		
R1	160		(MIKO)
R2,3	33k	(2 off)	(M33K)
R4	1MO		(M1M0)
R5,8.10	3k9	(3 off)	(M3K9)
R6	10CR		(M100R)
R7	120k		(M120K)
R9	390R		(M390R)
R11	100k		(M100K)
Capacitors			
C1.2	39pF ceramic	(2 off)	(WX51F)
C3.4	22nF polyester	(2 off)	(BX72P)
C5.6	2u2F63V PC electrolytic	(2 off)	(FF02C)
C7.10	100nF Disc	(2 off)	(BX03D)
C8	100uF10V axial electrolytic		(FB48C)
C9	10uF25V axial electrolytic		(FB22Y)
Serni conducto			,
	74LS138		(YF53H)
IC2	74LS30		(YF20W)
IC3	74LS273		(YHOOA)
IC4	7415244		(0056L)
IC5	74LS00		(YFOOA)
IC6	SP0256		(QY50E)
D1.2.3	1N4148	(3 off)	(OL80B)
TR1	BC548	(5 01)	(08730)
TR2.3	BC109C	(2 off)	(0B33L)
	DC109C	(2 011)	(40502)
Miscellaneous	24 IDC		(BK96E)
SK1	34 way IDC socket & cable		(HH30H)
PL1	7 way DIN connector		(GB45Y)
	Printed circuit board	(2 off)	(BL18U)
	14 pin DIL socket	(2 011)	(BL19V)
	16 pin DIL socket	12 -40	(HQ77J)
	20 pin DIL socket	(2 off)	(BL21X)
	28 pin DIL socket	1 -14	(BLOOA)
	Cable hook up	1 pkt	(BLUUA)
Optional			
	Minicon latch plug 17 way	(2 off)	(BH61R)
	Minicon latch housing. 17 way	(2 off)	(RK69A)
	Minicon terminal	(34 off)	(YW25C)
	A complete kit of parts is avai	lable	

A complete kit of parts is available. Order As LK28F



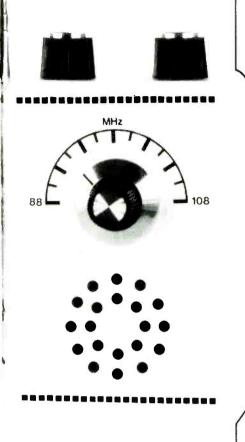
★ USES IMAGINATIVE MULLARD IC ★ NO ALIGNMENT EQUIPMENT NEEDED ★ EASY TO BUILD

onventional Band II VHF superhet radios use a large number of tuned circuits as these are needed for filtering in the RF, mixer, oscillator, IF, and detector stages. Ceramic filters have become very popular in recent years, but these can only replace one or two IF transformers, and only marginally ease problems with alignment of the finished receiver. The TDA7000 is a new and imaginative integrated circuit from Mullard which employs novel techniques that enable a good quality FM broadcast receiver having just two tuned circuits to be built. The reason for this device being developed is that it offers radio manufacturers the advantages of reduced costs, both in terms of components and the setting up time for the For the home finished receiver. constructor it similarly gives the advantages of low cost and ease of alignment. In fact the finished receiver only needs to have the core of one tuned circuit adjusted to give the correct frequency coverage, and no test gear is required. A TDA7000 FM radio is actually no more difficult to align than a simple SN414 based AM radio!

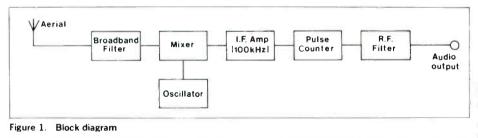
Low IF

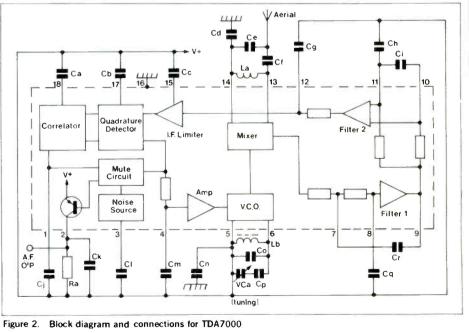
Strictly speaking the basic system used in the TDA7000 is not a new one, and is essentially the same as that used in the so called "pulse counting" FM tuner designs that were popular amonst home constructors around twenty years ago (the original designs used valves)! The block diagram of Figure 1 shows the way in which these operate. The RF, mixer, and osciallator stages are fairly conventional, but usually quite simple with just a broadband (preset tuning) filter ahead of the mixer, but a more complex arrangement could be used if preferred. It is at the IF and demodulator stages where the real departures from a conventional superhet arrangement occur. The IF amplifiers are virtually ordinary high gain audio amplifiers, but filter capacitors are used to roll-off the response above about 200kHz and the coupling capacitors only need to be effective at frequencies above the audio range. This gives an IF centred at around 100kHz or so, and not tuned circuits to

provide IF filtering are required. The low IF enables simple C-R filtering to give adequate results, and thre is no lack of performance in this respect. A pulse counting circuit plus an RF filter provides the demodulation, and the pulse counter is merely a diode-pump frequency-to-voltage converter. Other types of circuit such as a phase locked loop or even just a monostable multivibrator can be used here to convert the frequency variations into the corresponding audio signal. While this system has obvious attractions, it is not without its drawbacks as well. The main one is the lack of any image rejection, due to the very low IF and the spacing of only a few tens of Kilohertz between what would normally be the main and image responses. Thus, when tuning a receiver



of this type there are two very closely spaced points on the tuning dial where each station can be received satisfactorily, with a very narrow gap between these where the station is received, but is





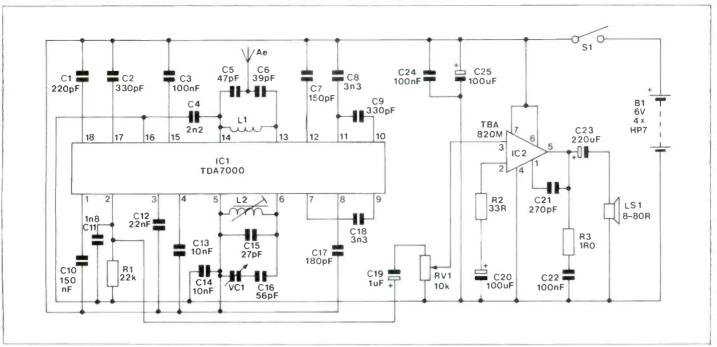


Figure 3. Circuit diagram of TDA7000 radio

very severely distorted. As Band II FM broadcast stations tend to be well spread out this is unlikely to give problems with co-channel interference, but does make tuning the set a little awkward.

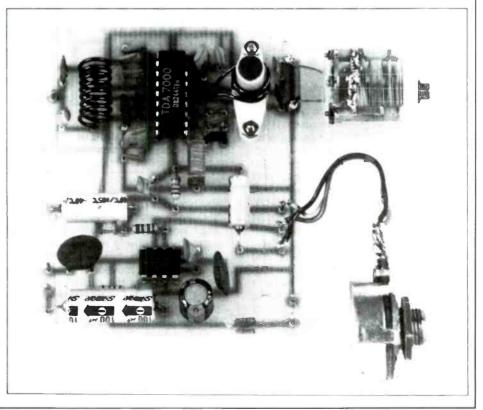
TDA7000

Although pulse counting tuners were originally conceived as simple alternatives to conventional circuits, it would not be accurate to think of the TDA 7000 as providing an inferior alternative to a conventional design. It uses a highly refined version of the pulse counting type of circuit, and in some respects it is superior to more conventional designs. Figure 2 shows the arrangement used in this device, plus basic details of the discrete components required. The standard TDA7000 has an 18 pin DIL plastic package, but there is also a minature 16 pin version, the TDA7000T. The input tuned circuit is formed by La, Ce, and Cf. Internal resistors of the TDA7000 heavily damp this filter so that it has a very wide bandwidth and no RF tuning is needed. La can in fact be a zig-zag of printed circuit track, but in the design featured here it is a simple home-made coil. The aerial, which is a simple wire or telescopic type, is coupled to the input tuned circuit by way of a capacitive tapping. A voltage controlled oscillator feeds the other input of the mixer stage. This VCO is a straight forward L-C type which achieves voltage control using a couple of variable capacitance diodes. There are three IF filter stages, and the first of these uses a second-order low pass Sallen-Key circuit, which is the type of filter used in scratch filters and similar applications. Cq and Cr are the filter capacitors, but the filter resistors and other components are part of the TDA7000. The second filter is a simple bandpass type, and again, the only discrete components are two capacitors. The final filter stage is a straight forward passive first-order lowpass type which uses discrete capacitor Cg. The

reason for using discrete rather than onchip filter capacitors is simply that it is difficult and expensive to include even low value capacitors in an integrated circuit. The -60dB bandwidth of the filters is approximately 500kHz, which is perfectly acequate for an FM broadcast receiver.

After filtering the signal is amplified and limited in the usual way, and demodulated by a quadrature detector. Unlike a standard 10.7MHz quadrature detector, no tuned circuit is required, just on phase shift capacitor (Cb). The intermediate frequency can be set at any reasonable figure by using the appropriate filter capacitor values, but a frequency of 70kHz would normally be used. Such a low IF eliminates any problems with the image signal of one channel interfering with reception of a transmission on the next channel. With

the set tuned to one channel the image response falls roughly half-way between this channel and the next. The problem of using such a low JF is that it would result in severe distortion with signals having something approaching the full plus and minus 75kHz deviation. This problem is overcome by amplifying the audio output signal and feeding it to the VCO. This gives a form of negative feedback with the VCO following the input signal up and down in frequency. The deviation of the VCO is not quite equal to that of the input signal so that there is some variation in the frequency of the IF signal, but this is only about plus and minus 15kHz. The typical total harmonic distortion on the audio output is 2.3% at maximum deviation, which is satisfactory for portable radios and similar applications. A useful "byproduct" of the feedback to



the VCO is that it gives a sort of automatic frequency control. Apart from counteracting any tuning drift, this effectively gives slow-motion tuning once the receiver has locked onto a transmission, and makes the set easy to tune even if only a small tuning knob is used.

Correlator

The correlator and mute circuits of the TDA7000 are used to suppress the image response as well as giving a conventional "squelch" action. The correlator operates by delaying the IF signal by an amount equal to the duration of one IF half cycle. This signal is then inverted and compared with the unprocessed IF signal. If the tuning is correct, the two signals will be virtually identical and will have a high degree of correlation. However, if the tuning is not very accurate the IF signal will be displaced from its normal 70kHz figure, and the delaying circuit will not give a one half cycle delay. This introduces a phase difference and poor correlation, with the mute circuit switching vf the audio in consequence. If the IF signal is noise, or largely consists of noise, this also gives very little correlation between the two signals and mutes the audio output. An interesting effect of this system of muting is that it eliminates the side responses that are normally found on FM radios. These are caused by the signal being "slope" detected by the skirt responses of the IF filtering, and they can make accurate tuning a little difficult. Many FM radios have a tuning indicator to assist proper tuning. The TDA7000 muting system eliminates the side responses, and together with the frequency locking tuning system makes tuning very easy indeed. A detuning indicator can be driven from pin 1 of the TDA7000, but in practice it would be pointless to do so

On its own the correlator does not eliminate the image response, but it does so in conjunction with the feedback to the VCO which was described above (the frequency locked loop or FLL) as the IC manufacturer terms it). This locking system only operates with the set tuned to the main response, and not when it is tuned to the image, due to the inversion of the signal that occurs. If we take a simple mathematical example to demonstrate this point, let us suppose that the receiver is tuned to a transmission which deviates between 100 and 101MHz, and that the oscillator is at 99MHz. This gives an IF range of 1 to 2MHz (100 - 99MHz and 101 - 99MHz). Of course, these figures have been chosen for their mathematical simplicity, and are not meant to be practical examples. As the IF signal moves up and down in frequency the audio output voltage also rises and falls, feeding a control voltage to the oscillator that shifts its frequency in the same direction as the input signal. The image response would occur with the oscillator at 102MHz, giving an IF range of 2 to 1MHz (102 - 100MHz and 102 - 101MHz). This frequency inversion of the if signal appears as a phase inversion of the

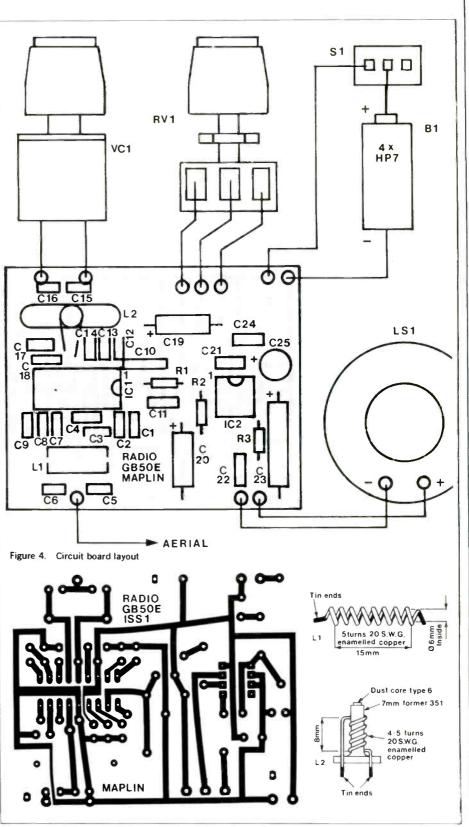


Figure 5. Coil details

audio output signal. Where the oscillator frequency was previously taken high er and lower in sympathy with the received signal to effectively reduce the level of deviation, when tuned to the image response it is moved in the opposite direction so that the deviation is effectively increased. For example, with the input signal at 100MHz the IF signal is at 2MHz, giving the maximum audio output voltage. This sends the oscillator higher in frequency, giving an even greater IF signal frequency, greater audio voltage, and positive rather than negative feedback. When tuned to the image the IF signal does repeatedly pass through the acceptable IF range, but the value of Cj is chosen to give the muting circuit a slow response time so that it ignores these transients, and the image is suppressed. Ra is the load resistor for the audio output stage, and Ck is the deemphasis capacitor. A slightly bizarre feature of the TDA7000 is a noise generator which gives a quiet noise signal at the audio output when the main audio signal is muted! This is included because it is otherwise very easy to tune over a station without realising it is there. The null in the noise signal as the set is tuned through a station helps to avoid this. However, if desired the noise can be eliminated by omitting C1.

The Circuit

Figure 3 shows the circuit of a practical radio built around the TDA7000, and the circuitry associated with IC1 exactly follows the arrangement shown in Figure 2 and discussed earlier.

An audio output stage using a TBA820M (IC2) is included, and this will operate with any loudspeaker having an impedance in the range 8 to 80 ohms. An output power of about 300 milliwatts RMS into an 8 ohm loudspeaker is available, and this is adequate for a portable radio. The output stage will also drive any normal type of earphone or headphones. VR1 is an ordinary volume control.

Construction

A suitable printed circuit layout for the radio appears in Figure 4. The TDA7000 is not one of the many radio ICs that tend to be unstable at every opportunity, and the low IF eliminates problems with harmonics of the clipped IF signal being picked up at the input of the circuit. However, with frequencies in the region of 100MHz involved it is not advisable to use a different layout unless you are familiar with radio projects and know exactly what you are doing. The only unusual aspects of construction are the two home-wound coils. L1 is the more simple of the two, and consists of 5 turns of 20 swg enamelled copper wire wound on a temporary former about 6 to 6.5mm in diameter. A twist drill of about this size or a potentiometer spindle can be used as the former. The coil is about 15mm in length, but as it is used in a broadband filter its exact characteristics are not critical. L2 is wound on a 7mm diameter coil former which is bolted to the board using M2 fixings. It consists of about 4.5 turns of 20 swg enamelled copper wire and the winding should be approximately 8mm in length. Again, the precise characteristics of the coil are not highly critical, and in this case it is because the former is fitted with an iron dust core that enable the inductance to be adjusted over a fairly wide range. An important point to bear in mind is that the leads which connect VC1 to the board must be very short, and should preferably be only about 10 to 30mm long. Be careful to connect VC1 the right way round or hand-capacity effects will make tuning practically impossible. (See Figure 6 for details on connecting VC1). Power is obtained from four HP7 size cells fitted in a plastic battery holder. The holder connects to the board by way of an ordinary PP3 style battery connector.

For best volume from the set it is advisable to use an 8 ohm impedance loudspeaker of reasonable size, and a 76mm diameter type is ideal. The unit can be fitted in a metal or plastic case, but a plastic type is probably the best choice as it will not have a detuning effect on the two tuned circuits. Also, with a plastic type there is no need to insulate the telescopic aerial from the case. Ideally the aerial should be a fairly long type having a swivel base, but satisfactory results can be achieved using a small non-swivel type, or even just a piece of wire about 0.5 to 1 metre long.

Adjustment

Only the core of L2 needs to be adjusted before the set is ready for use. This is just a matter of finding by empirical means a setting that enables the entire VHF Band Il to be tuned using VC1. In fact any setting that enables all the desired stations to be received is acceptable. It is a good idea to glue the winding and core to the former so that this coil is as rigid as possible. This helps to avoid problems with microphony, and prevents vibration from gradually detuning L2. It is possible to peak the sensitivity of the set by bunching the turns on L1 together, or spreading them apart, to alter its inductance. Due to the very wide bandwidth of this tuned circuit it is unlikely that this would produce a significant boost in performance though.

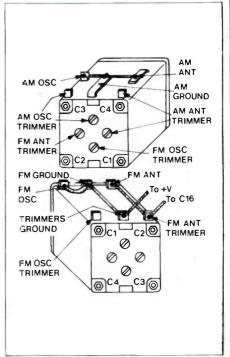
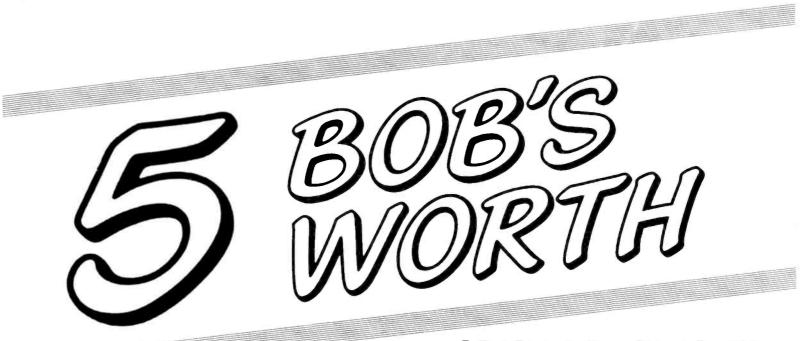


Figure 6. Connections made on VC1

Resistors - A	II 0.4W 1% metal film		
R1	22k		(M22K)
22	33R		(M33R)
3	1R0		(M1R0)
RV1	10k Pot log		(FW22Y)
Capacitors			
21	220pF ceramic		(WX60Q)
2,9	330pF ceramic	(2 off)	(WX62S)
3,22,24	100nF minidisc	(3 off)	(YR755)
24	2n2F ceramic		(WX72P)
25	47pF ceramic		(WX52G)
26	39pF ceramic		(WX51F)
27	150pF ceramic		(WX58N)
28,18	3n3F ceramic	(2 off)	(WX74R)
C10	15CnF Polycarbonate		(WW43W)
211	1n8F ceramic		(WX71N)
212	22nF ceramic		(WX78K)
213,14	10rF ceramic	(2 off)	(WX77J)
215	27pF ceramic		(WX490)
216	56pF ceramic		(WX53H)
217	18CpF ceramic		(WX59P)
219	1uF63V axial electrolytic		(FB12N)
20	10CuF10V axial electrolytic		(FB48C)
21	270pF ceramic		(WX61R)
23	220uF10V axial electrolytic		(FB60Q)
C25 /C1	10CuF10V P.C. electrolytic AM/FM Varitune		(FF10L) (FG75S)
emiconducto			
C1	TDA7000		(YH87U)
C2	TBA820M		(W063T)
			(#Q031)
Miscellaneous			and the first of the
51	SPST Ultra min toggle		(FH97F)
31	Four HP7 cells		distant for the
.S1	8R L/S LO-Z 768		(YW53H)
	Printed circuit board		(GB50E)
	Control knob K7B	(2 off)	(YX02C)
	20 swg enamelied copper		(BL26D)
	Wire (½ metre)		
	Former 351		(LB17T)
	Core type 6		(L842V)
	Bot M2 x 6mm	1 pkt	(BF41U)
	Nut M2	1 pkt	(LR59P)
	Veropins 2145	1 pkt	(FL24B)
	Wire		(BL00A)
optional			and the second second
	Battery holder		(HF29G)
	Battery clip		(HF28F)
	Case (as required)		
	Aerial (as required)		



5 Fun Projects From Robert Penfold

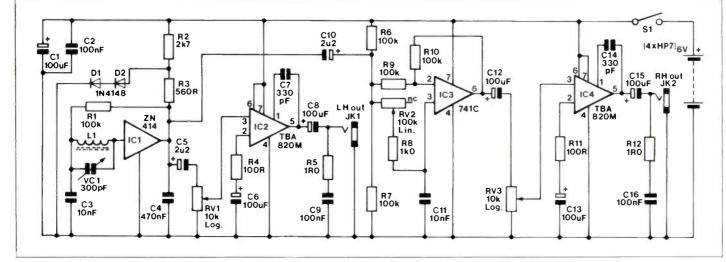


Figure 1. Pseudo stereo AM radio block diagram

PSEUDO STEREO AM RADIO

This simple radio receiver has been designed to drive a pair of medium impedance (personal stereo type) headphones, but it also gives quite good results when used with low or high impedance loudspeaker if a conventional portable radio is all that is required. Although several AM stereo radio systems are in existence, none of these are currently in use in the U.K., and a simple phase shifting system is used in this circuit to give a pseudo stereo effect.

The R.F., detector, and A.G.C. sections of the circuit are based on the ZN414 used in the standard configuration. L1 can be the tuned winding of any normal MW ferrite aerial, such as a Denco MW5FR. This type of aerial coil invariably seems to have a small coupling winding which is not needed in this application, and it is either removed or just ignored. Some of the audio output from IC1 is coupled by C5 to volume control RV1, and then to the input of an audio power amplifier which is based on IC2. The use of a power amplifier may seem to be unnecessary, but medium impedance (about 35 ohms) headphones require a higher drive current than could be provided by an operational amplifier or similar stage. The TBA820M can readily provide the required voltage gain of about 35dB and has a low quiescent current consumption of only about 4 milliamps which helps to give good battery life.

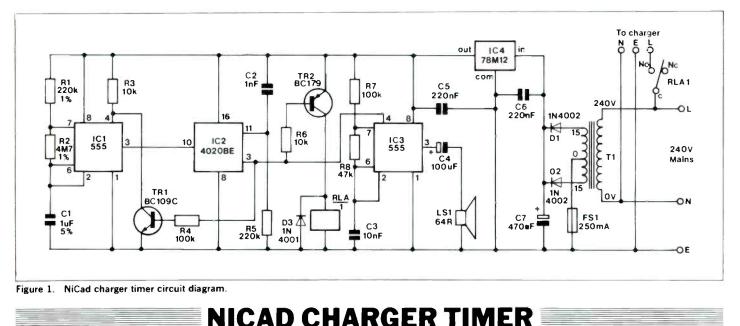
If mono reproduction is required the phones can be fed from the output of IC2 using series connection for low or medium impedance types, or parallel connection for high impedance headphones. A high impedance (about 64 ohms) loudspeaker can also be driven from IC2. If the pseudo stereo effect is required the phase shifter built around IC3 and the extra audio output stage which uses IC4 must be included. The two most common methods of producing a quasi stereo effect from a mono signal are to introduce anomalies in the frequency response or phasing of the two audio outputs. In this case one output is just the normal audio signal, and the other is phase shifted through IC3 by an amount which varies from

zero at low frequencies to 180 degrees at high frequencies.

With the two signals in-phase a strong central stereo image is produced, but with a significant phase difference between the signals the sounds seem to emanate from the sides of the sound stage. The effect of the phase shifter is to give a strong central image at low frequencies, with a spreading of the image at high frequencies. This does not give a true stereo effect, but does give somewhat more satisfactory and realistic results. RV2 controls the frequency at which a significant phase shift is introduced, and effectively acts as a stereo width control (maximum resistance corresponding to maximum separation).

Volume controls RV1 and RV3 must be separate (i.e. single gang) types so that they can also be used to balance the two channels. The only alignment the finished receiver requires is to fix L1 in a position on the ferrite rod that gives full coverage of the MW band. Note that the unit must not be fitted in a metal case as this would screen the aerial.

FIVE BOB'S WORTH



When recharging NiCad cells it is very easy to forget them so that they are left charging for a considerable length of time. This timer can be used to automatically switch off the charger after the normal 15 hour charging time and it also produces an audio alarm signal which indicates to the user that charging has been completed. The unit is connected in the mains supply to the charger which consequently does not require any modification. The circuit can easily be modified to provide a switch-on of other than 15 hours if desired.

The long timing pulse duration required in this application precludes the use of a simple C-R timer circuit. Instead an oscillator and divider chain are used, and with this type of circuit the pulse length is equal to a certain number of clock oscillator cycles. The clock signal is generated by a standard 555 astable (IC1) and the divider is a CMOS 4020BE 14 stage binary type (IC2). C2 and R5 produce a positive

reset pulse at switch-on so that IC2 starts with all outputs low. After 8192 clock cycles the Q14 output at pin 3 goes high, and TR1 plus the relay which forms TR1's collector load are both switched off. A pair of normally open relay contacts then cut off the mains supply to the charger. TR1 is switched on when IC2's Q14 output goes high, and it takes the reset input of IC1 low so that the clock oscillator ceases to operate. Thus, once the charger has been cut off from the mains supply it remains switched off until the unit is used again. The circuit is reset ready for reuse by simply disconnecting it from the mains and reconnecting it again, but in practice it is likely that the unit would only be used occasionally and would be disconnected after each recharge anyway

A second 555 (IC3) astable driving a high impedance loudspeaker is used to generate the audio alarm signal. The reset terminal of IC3 is normally held

low by the Q14 output of IC2 so that oscillation is blocked, but at the end of the timing pulse when IC2's Q14 output goes high the alarm generator is able to function normally.

A conventional 12 vclt stabilised power supply is used to power the unit. T1 can be any 15-0-15 volt type or twin 15 volt component having a secondary current rating of 100 milliamps or more. It is unlikely that IC4 will need a heatsink.

A switch-on time of 15 hours (54000 seconds) requires a clock cycle period of about 6.59 seconds, and the specified values for R1, R2 and C1 give a suitable clock cycle time. For other charging times the value of R2 and or C1 can be changed. Any change in the value of either component gives a proportional change in the charge time. When initially testing the unit a component of 1nF value can be used for C1, and the relay should then be energised for about 54 seconds after switch-on.

It can often be helpful to compare the input and output signals of an audio amplifier or other audio circuit using an oscilloscope with the two traces adjusted so that they overlap one another as precisely as possible. However, this will only clearly show up quite large changes in the processed signal, and a better method is to use a differential amplifier which shows the difference between the two signals as a single trace. For example, if the signal is subjected to strong second harmonic distortion by the amplifier (or whatever) the difference signal would show a strong content at double the frequency of the input signals. Some oscilloscopes have a built-in differential facility, but it is guite easy to add a simple external adder/subtracter to an instrument which does not.

The circuit is little more than an operational amplifier summing circuit based on IC1a, and a unity gain

ADDER/SUBTRACTOR

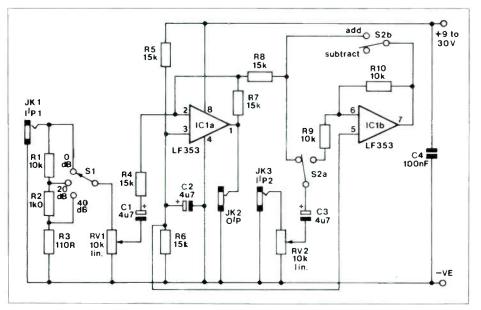


Figure 1. Adder/Subtracter circuit diagram.

inverting amplifier based on IC1b. In the adding mode IC1b is not used, and the two signals are applied to the inputs of IC1a. This mode is used where the processed signal has undergone an inversion, and the two input signals are therefore in antiphase so that the required cancelling effect is produced. RV1 and RV2 are used to balance the two input signals for

FIVE BOB'S WORTH

optimum cancelling, and, if necessary, to prevent the summing circuit from being overloaded. In many cases one input signal will be at a much higher level than the other, and the stronger signal is then applied to input 1 so that the attenuator (S1 plus R1 to R3) can be used to reduce it to a satisfactory level. This makes adjustment of RV1 much easier. In the subtracting mode IC1b is used to invert one of the signals so that the phasing out of the two signals is still obtained even though they are inphase. Obviously IC1b introduces a certain amount of phasing and amplitude distortion, but at audio frequencies, provided the circuit is not overloaded, both types of distortion will be too small to be of significance.

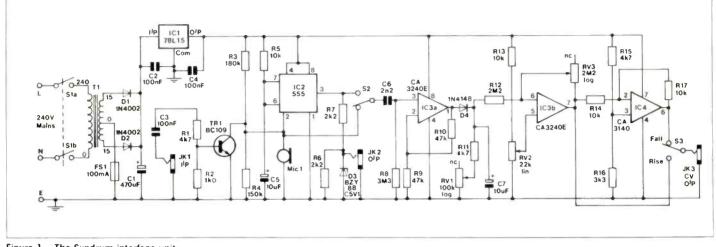


Figure 1. The Syndrum interface unit.

SYNDRUM INTERFACE

This circuit can be used in conjunction with a monophonic synthesiser having gate and CV inputs to effectively form a sophisticated syndrum capable of producing a wide range of interesting effects. The main function of the circuit is to generate a trigger pulse when thepickup is activated. The latter is a crystal microphone insert or a 27mm piezo transducer which is mounted on a drum, pad of rubber, or whatever. When operated, the first negative output half cycle from the transducer triggers the 555 monostable circuit based on IC2, and this gives a positive 5 volt trigger pulse of about 100ms in duration at JK2 (a nominal 15 volt pulse can be obtained from pin 3 of IC2). This pulse length should be satisfactory, but practically any desired figure can be obtained by altering the value of R5 and/

or C5. The circuit can be triggered using a positive trigger pulse of between about 5 and 15 volts applied to JK1, and this permits manual and automatic triggering to be employed together.

With some synthesisers it may be possible to obtain rising and falling pitch syndrum sounds without the use of an external control voltage circuit, but in many cases this would be difficult or impossible. The unit therefore incorporates a rising/falling control voltage generator. IC3a amplifies the trigger signal to produce a strong positive output pulse that charges C7 to a potential of several volts. The exact charge potential depends on how hard the transducer is struck, and the unit is to a degree touchsensitive in this respect. However, if S2 is set to the other position IC3a is fed

with the output of IC2 and C7 then charges to about 10 volts or so each time the unit is operated. D3 prevents C7 from discharging into the output stage of IC3a, and the decay time of the voltage is therefore largely controlled by RV1. IC3b is a level shifter and inverting amplifier, but it really acts as an attenuator since its voltage gain is never more than unity. RV2 acts as the pitch control while RV3 is used to control the sweep width. IC4 is a straight forward unity gain inverter, and this enables a rising or falling voltage (pitch) to be selected using S3.

The circuit is powered from a simple 15 volt stabilised mains power supply unit which can comfortably provide the supply current of only about 20 to 25 milliamps.

MICROPHONE PREAMP/LIMITER

Although this microphone preamplifier and limiter is very simple it provides a useful level of performance. It is primarily intended for use ahead of a mixer and tape deck, but it could, no doubt, be used in other, similar applications. Many tape decks have a built-in limiter, but there is a drawback in using a single limiter with several signal sources in that an overload from one source can effectively reduce the signal level provided by the other sources. Using a separate limiter for each input signal totally eliminates this problem.

The preamplifier is quite straight forward and uses IC1 as a non-inverting amplifier having a voltage gain of 20 about 22 times, and IC2 as an inverting amplifier having a voltage gain of approximately 26 times. The circuit is intended for use with a high impedance microphone, and the total voltage gain is sufficient to give an output in excess of 1 volt RMS with most microphones of this type. RV1 can be used to give a lower level of gain if necessary. An excellent signal to noise ratio is obtained by using a low noise bipolar operational amplifier in the IC1 position and a biFET type in the IC2 position.

an LM13700N dual transconductance operational amplifier is used as the basis of the limiter. IC3a is used as a straight forward current controlled amplifier and under quiescent conditions this is biased by R15 so that it has approximately unity voltage gain. R14 biases the linearising diodes of IC3a and gives improved distortion and large signal handling performance.

IC3b is used as a straight forward amplifier, and the gain of this stage can be varied by means of RV2. C8 couples the output of this amplifier t the input of the Darlington Pair emitter follower output stage of IC3b. This drives TR1 via R23 and R24, but under quiescent conditions TR1 is cut off due to the low bias level supplied to the emitter follower buffer stage by R21 and R22.

FIVE BOB'S WORTH

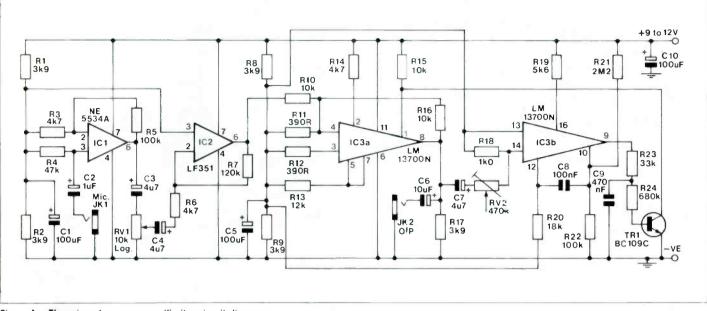


Figure 1. The microphone pre-amp/limiter circuit diagram.

However, on positive output half cycles from IC3b, provided the signal level is high enough, TR1 will be biased into conduction. It then reduces the bias current to IC3a so that its gain is reduced and the required limiting action is obtained. C9 integrates the pulses from IC3b, but the values of C9, R23 and R24 have been chosen to give fast attack and decay times so that the limiting action is unlikely to be noticed unless a very severe overload occurs.

RV2 is adjusted to give the desired limiting level, and this can be any practical value above about 20 millivolts RMS. Raising the input signal 20dB above the limiting threshold gives an increase of less than 2dB at the output. A substantial overload could result in the signal at the output of IC2 being clipped, but such an overload is unlikely to occur in normal use. An 18 volt supply gives the greatest overload margin, but in practice a 9 volt supply will usually be perfectly adequate.

PSEUDO S	STEREO AM RADIO			Capacitors			
).4W 1% metal film			C1	1uF 5% Polycarbonate		(WW53H)
R1,6,7,9,10	100k	(5 off)	(M100K)	C2	InF Polycarbonate		(WW22Y)
		(5 01)		C3	10nF Polyester		(BX70M)
R2	2k7		(M2K7)	C4	100uF 25V P.C. electrolytic		(FF11M)
R3	560R		(M560R)	C5,6	220nF Polyester	(2 off)	(BX78K)
R4.11	100R	(2 off)	(M100R)	C7	470uF 25V P.C. electrolytic	(2 011)	
R5.12	180	(2 off)	(M1R0)	C/	4700F 25V P.C. electrolytic		(FF16S)
R8	1k0	(/	(M1KO)	in the state of the second			
RV1.3	Pot log. 10k	(2 off)	(FW22Y)	Semiconductors			
		(2 011)		D1.2	1N 4002	(2 off)	(OL74R)
RV2	Pot lin. 100k		(FW05F)	D3	1N 4001	· · ·	(OL730)
				TR1	BC109C		(OB33L)
Capacitors				TR2	BC179		(Q854J)
C1,6,8,12,13,15	100uF 25V P.C. electrolytic	(6 off)	(FF11M)	IC1.3	555	10 10	
C2,9,16	100nF Polyester	(3 off)	(BX76H)			(2 off)	(QH66W)
C3.11	10nF Polyester	(2 off)	(BX70M)	IC2	4020BE		(QX11M)
C4	470nF Polyester	(2 011)	(BX80B)	IC4	uA78M12UC		(QL29G)
		12.40					
C5.10	2u2F 63V P.C.electrolytic	(2 off)	(FF02C)	Miscellaneous			
C7, 14	330pF ceramic	(2 off)	(WX62S)	RLA	Relay flat 12V		(HY20W)
VC1	AM Varitune 500pF		(~Q24B)	TI	Min Tr 15V		
	and the second second second second						(WB15R)
Semiconductors				LS1	Loudspeaker 64R		(WF57M)
D1.2	1N4148	(2 off)	(QL80B)	FS1	Fuse 20mm 250mA		(WRO1B)
		(2 011)	(OL41U)		Safuseholder 20		(RX96E)
IC1	ZN414	10 10					
IC2,4	TBA 820M	(2 off)	(WQ63T)				
IC3	741C		(QL22Y)	PARTS LI	ST ADD/SUBTR	ACTER	
Miscellaneous					0.4W 1% Metal film		
JK1,2	1/4" Jack socket	(2 off)	(HF90X)			2.41	(11101/)
	Jack plugs	(2 off)	(HF85G)	R1,9,10	10k	3 off	(M10K)
SI	Sub-min toggle A	(2 01.)	(FHOOA)	R2	1k0		(M1KO)
			(LB12N)	R3	110R		(M110R)
L1	MW/LW Aerial		(LOIZN)	R4-8	15k	5 off	(M15K)
	HP7 Batteries	(4 off)		RV1.2	Pot lin. 10k	2 off	(FWO2C)
				RV1.2	FOR INT. TOX	2 011	(111020)
				Capacitors		2 -4	(FF03D)
				C1-3	4u7F 63V P.C. electrolytic	3 off	
				C4	100nF polyester		(BX76H)
NI CAD CI				Semiconductors			
				IC1	LF353		(WQ31J)
	0.4W 1% metal film	10 10		the line of the li			
R1,5	220k	(2 off)	(M220K)	Miscellaneous			
R2	4M7		(M4M7)	S1	Switch rotary SW3B		(FF76H)
R3.6	10k	(2 off)	(M10K)	\$2	Switch sub-min toggle E		(FH04E)
R4.7	100k	(2 off)	(M100K)	JK1-3	1/4" jack socket	3 off	(HF90X)
R8	47k	(2 011)	(M47K)	301-3	Jack plugs	3 off	(HF85G)
10	3/0		(inite) (1)		Jack hinks	3 011	(11050)

★ SMALL AND PORTABLE ★ IMPROVES SOUND QUALITY ★ EASY TO BUILD

by Robert Penfold

Most personal stereo cassette players are capable of a creditable level of performance, but a weakness of all but a few of the more recent and expensive machines is a lack of any proper form of noise reduction circuit. Most units simply have a high/low tone switch which gives a certain amount of treble cut in the "low" position and helps to keep down the amount of tape noise.

This add on noise reduction unit simply plugs between the personal stereo unit and the headphones. It is a dynamic noise limiter, which is merely a form of lowpass filter. However, the cut-off frequency of the filter is not fixed, and it varies in sympathy with the dynamic level of the input signal. With little or no input to the unit the cuf off frequency would be quite low at about 4 or 5kHz, but at higher input levels the cutoff frequency would be forced upwards, reaching perhaps 15 or 20kHz, with the input at its maximum level.

This gives a large amount of noise reduction at low volume levels, but at high volume levels the amount of noise reduction is negligible. In practice the ineffectiveness of the system at high dynamic levels does not matter since the noise will be masked by the main signal and will not be noticeable anyway. In fact the lack of filtering is an advantage since it avoids an unneces-

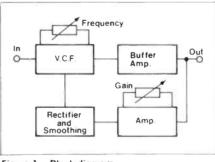


Figure 1. Block diagram.

sary reduction in the high frequency performance of the system. The weakness of a Single-ended noise reduction system of this type is that it does reduce the treble response at low dynamic levels, and to a lesser extent at medium signal levels, but it is nevertheless a great improvement in comparison to a simple top-cut filter.

Circuit Operation

The arrangement used in the DNL unit is outlined in the block diagram of figure 1. This is for one channel only, but with units of this type the two stereo channels are processed by separate but identical circuits.

The lowpass filter is a voltage controlled type, and a preset control enables the cutoff frequency (under quiescent conditions) to be set at a suitable figure. The filter cannot directly drive the headphones which typically require a maximum input voltage of about 1 volt RMS into an impedance of only about 35 ohms. A

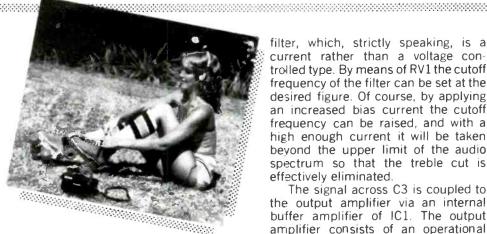


buffer amplifier which provides a suitably low output impedance and drive current capability is therefore used at the output of the filter.

Some of the output of the unit is coupled to an amplifier. The amplified signal is rectified and smoothed to produce a control voltage for the VCF. With low level input signals the control voltage is too small to have any significant effect on the VCF, but at higher input levels there is a roughly proportional increase in the control voltage, and the cutoff frequency of the filter is moved higher, giving the desired effect. The gain of the amplifier has been made variable so that the unit can be adjusted to only fully remove the treble cut when the input signal reaches its maximum level.

Figure 2 shows the circuit diagram for one channel of the unit. Most of the components are duplicated in the other channel. As is standard practice, these components have the same identification numbers in the components list and printed circuit overlay, but with one hundred added (e.g. what is R8 in one channel is R108 in the other). Note that IC1 is a dual device which has one section used in each channel of the unit (the pin numbers in brackets are those for the second channel). The battery, on/off switch S1, and supply decoupling capacitor C8 are common to both channels.

IC1 is a transconductance operational amplifier which is used as the basis of the VCF. This is a straightforward 6dB per octave circuit with the values of bias and feedback resistors R3 to R6 chosen to give approximately unity voltage gain. However, the circuit will have less than unity gain if the bias current fed to the amplifier bias input (pin 1) is inadequate in relation to the load impedance from the output of the amplifier to the earth rail. This impedance is largely formed by C3, and as the impedance of a capacitor decreases as signal frequency is increased, at some point the impedance of C3 must become so low that the gain of the circuit is rolled-off. RV1 and R7 supply a quiescent bias current to the







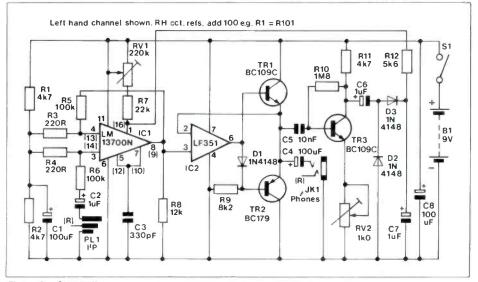


Figure 2. Circuit diagram

filter, which, strictly speaking, is a current rather than a voltage controlled type. By means of RV1 the cutoff frequency of the filter can be set at the desired figure. Of course, by applying an increased bias current the cutoff frequency can be raised, and with a high enough current it will be taken beyond the upper limit of the audio spectrum so that the treble cut is effectively eliminated.

The signal across C3 is coupled to the output amplifier via an internal buffer amplifier of IC1. The output amplifier consists of an operational amplifier (IC2) plus a discrete complimentary emitter follower output stage to boost the output current capability of the circuit to an acceptable level of high frequency distortion. D1 and R9 were therefore added to give a small quiescent bias voltage across the bases of the output transistors, and this leaves no significant crossover distortion.

TR3 is used as a simple common emitter amplifier which amplifies the output signal prior to rectification and smoothing by D2, D3 and C7. RV2 gives a controlled amount of negative feedback to the amplifier and enables the voltage gain to be varied between about 14 and 40dB. The bias voltage developed across C7 is fed to the amplifier bias input of IC1 via R12, and the current that flows through R12 in the presence of a strong bias voltage gives the required modification of the filter's cutoff frequency. The value of C7 and other components in the control voltage circuit produce rapid attack and decay times, and this is essential if the unit is to operate efficiently, and the changes in frequency response are not to be apparent to the user. As the circuit only processes high frequency signals it is possible to have attack and decay times of only a few milliseconds without introducing significant distortion.

Coupling capacitor C5 has been given quite a low value so that bass and lower middle frequencies are not efficiently coupled to TR3. This avoids having strong low frequency signals, which would not mask the noise, from operating the VCF and lifting the treble cut.

The current consumption of the circuit is only about 9 milliamps under quiescent conditions, and does not increase dramatically at high volume levels. A PP3 size battery is therefore adequate as the power source, although a higher capacity battery such as six HP7 (AA) size cells would probably be a better choice if the unit is likely to receive a great deal of use.

Construction

Refer to figure 3 for details of the printed circuit board. Construction of the board should not be difficult provided the resistors and diodes are fitted first, followed by the capacitors, presets, Veropins, and remaining semiconductors. Do not overlook the single link wire. Also, note that IC2 has the opposite orientation to the other two ICs.

PERSONAL STEREO D.N.L.

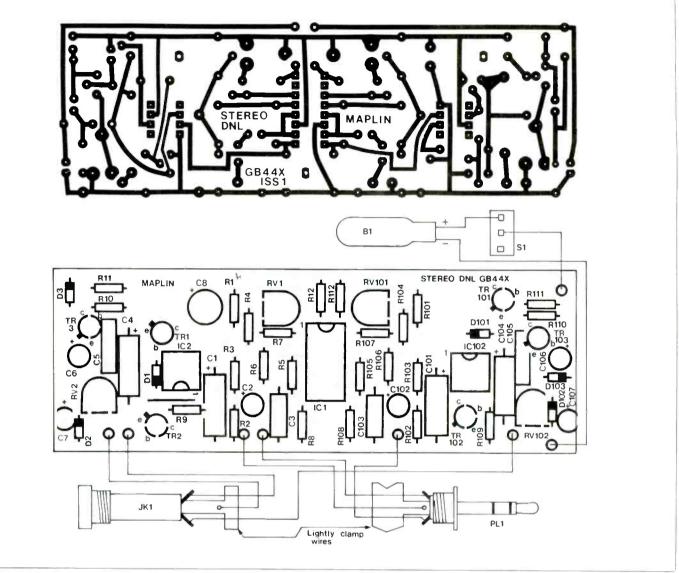


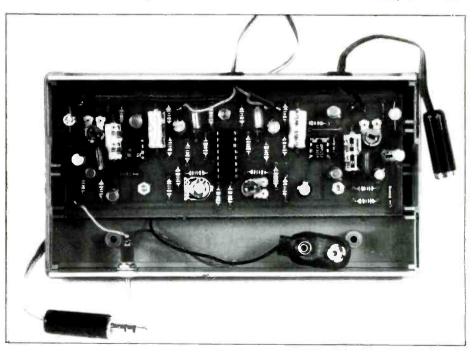
Figure 3. PCB artwork.

A verocase having approximate outside dimensions of 153 by 84 by 39.5mm makes a neat and practical housing for the unit, but it should be possible to utilise any plastic or metal box of around the same size. The printed circuit board is mounted on the base panel of the case using 6BA fixings. S1 is mounted towards the left hand end of the front panel, and holes for the input and output leads are drilled at the centre and right hand ends of the rear panel. The connection to the headphones is made by way of a short 3 way cable fitted with a 3.5mm stereo line socket. Use of a chassis mounting socket might be a neater solution, but sockets of this type do not seem to be available. The connection to the personal stereo unit is made via a 3 way lead about half a metre or so in length, and terminated in a 3.5mm stereo jack plug. As these leads carry high level, low impedance signals it is not essential to use screened types.

Setting Up

If suitable test gear is to hand, RV1 and RV101 can be adjusted to give a -6dB point a suitable frequency. With this type of equipment a cutoff frequency of somewhere between 4 and 10kHz is normally used, depending on the degree of noise reduction that is required, and 6kHz should be a suitable figure. However, either one leadout wire of D3 and D103 should be temporarily disconnected, or a temporary shorting links should be wired across D2 and D102 so that the test signal does not alter the cutoff frequency of the filter.

Again, if suitable test gear is available RV2 and RV102 can be adjusted to give the desired frequency response with an input signal level that roughly corresponds with maximum volume (about 1 volt RMS). use a test



Personal Stereo DNL

signal at a frequency of a few kilohertz.

It is not essential to have any test equipment in order to set up the unit satisfactorily, and RV1/101 can simply be adjusted to give the desired amount of noise reduction, being careful to keep the two stereo channels well balanced in this respect. Do not be tempted to set these controls for a very high level of noise reduction as this would give a very poor frequency response at low signal levels, and the changes in frequency response would be so large that they would probably be clearly audible to the user.

RV2 and RV102 can simply be set by trial and error. If these are set at or near minimum resistance the filtering will be

PERSONAL STEREO DNL

lifted even at quite low dynamic levels, and this will be heard as a rise and fall in the noise level as the input signal rises and falls in amplitude. RV2 and RV102 should be advanced to the point where this effect is no longer apparent on their respective channels, but not significantly further than this.

The setting of the volume control on the personal stereo unit obviously has an effect on the way in which the DNL performs. When setting up the unit the volume control should be at a fairly high setting. The DNL will then function properly when the system is used at fairly high volume levels, but will function more or less as a straight forward top cut filter if the system is used at low volume settings. In practice tape noise is generally only objectionable when listening at high volume levels, and it would not be worthwhile using the unit at low volume settings anyway. The DNL has nominally unity voltage gain, and there should not be any appreciable change in volume when it is used.

The unit will work with the tone switch on the personal stereo unit in either the "high" setting or the "low" one, but results will probably be best with this control in the "high" position. If this gives excessive treble at high signal levels backing off RV2 and RV102 slightly should clear the problem.

Resistor - All O	4W 1% metal film			Semiconductors IC1,	LM13700N		(YH64U)
R1,2,11,101,102 111	4k7	(6 off)	(M4K7)	IC2,102 TR1,3,101,103	LF351 BC109C	(2 off) (4 off)	(WQ 30H) (QB33L)
R3,4,103,104 R5,6,105,106	220R 100k	(4 off) (4 off)	(M220R) (M100K)	TR2,102 D1,2,3,101,102,	BC179	(2 off)	(QB54J)
R7,107 R8,108	22k 12k	(2 off) (2 off)	(M22K) (M12K)	103 Miscellaneous	1N4148	(6 off)	(QL80B)
R9,109 R10,110	8k2 1M8	(2 off) (2 off)	(M8K2) (B1M8)	S1	SPST Ultra min toggle		(FH97F)
R12,112 RV1,101	5k6 220k hor. preset	(2 off) (2 off)	(M5K6) (WR62S)	PL1 JK1 B1	3.5mm sterec plug 3.5mm sterec line skt. PP3 9V		(HF98G) (RK51F)
RV2,102	1k0 hor. preset	(2 off)	(WR55K)	5.	Printed circui, board		(G844X)
Capacitors					Verop ns 2145	1 Pkt	(FL24B)
C1,4,101,104	100uF 10V axial electrolytic	(4 off)	(FB48C)	The March	Ribbon cable 10-way PP3 c ip	1 mtre	(XR06G) (HF28F)
C2,6,7,102 106,107	1uF 100V P.C. electrolytic	(6 off)	(FF01B)	Optional	Case		(LL08J)
C3,103 C5,105	330pF polystyrene 10nF polyester	(2 off) (2 off)	(BX31J) (BX70M)	A	kit of parts (excluding case) is	available.	
C8	100uF 10V P.C. electrolytic		(FF10L)		Order As LK27E		

FIVE BOB'S WORTH Continued from page 21.

THE SYNDRUM INTERFACE PARTS LIST

Resistor	s - All 0.4W 1% Metal film					UTED	
R1.11.1	5 4k7	3 off	(M4K7)	MICROP	HONE PRE-AMP/LIN	ILLER	
R2	tkO	0 011	(M1KO)		I 0.4W 1% metal film		
R3	180k		(M180K)	R1.2.8.9.17	3k9	(5 off)	(M3K9)
R4	150k		(M150K)	R3,6,14	4k7	(3 off)	(M4K7)
R5.13.1		4 off	(M10K)	R4	47k	(0 0)	(M47K)
R6.7	2k2	2 off	(M2K2)	R5.22	100k	(2 off)	(M100K)
R8	3M3 %W 5% carbon film	2 011	(B3M3)	R7	120k	(2 011)	(M120K)
R9.10	47k	2 off	(M47K)	R10.15.16	10k	(3 off)	(M10K)
R12	2M2 KW 5% carbon film	2 011	(B2M2)	R11.12	390R	(2 off)	(M390R)
R16	3k3		(M3K3)	R13	12k	(2 011)	(M12K)
RV1	Pot log 100k		(FW25C)	R18			(M1KO)
RV2	Pot lin 22k		(FW03D)		1k0		(M5K6)
				R19	5k6		
RV3	Pot log 2M2		(FW29G)	R20 ·	18k		(M18K)
0	section of that when a data the			R21	2M2 1/2W5% Carbon film		(B2M2)
Capacit			(25) (0)	R23	33k		(M33K)
C1	470uF 25V PC electrolytic		(FF16S)	R24	680k		(M680K)
C2,3,4	100nF polyester	3 off	(BX76H)	RV1	Pot log. 10k		(FW22Y)
C5,7	10uF 35V PC electrolytic	2 off	(FFO4E)	RV2	Hor. Preset S- vin 470k		(WR63T)
C6	2n2 polycarbonate		(WW24B)				
Semico	ductors			Capacitors			
D1.2	1N4002	2 off	(OL74R)	C1.5.10	100uF 25V P.C. electrolutic	(3 off)	(FF11M)
D3	BZY88C5V1		(QH07H)	C2	1uF 1 DOV P.C electrolytic		(FF01B)
D4	1N4148		(QL80B)	C3.4.7	4u7F 53V P.C. electrolytic	(3 off)	(FF03D)
TR1	BC109C		(OB33L)	C6	10uF 35V P.C. electrolytic	(0 0)	(FF04E)
IC1	uA78L15AWC		(OL27E)	C8	100nF Polyes er		(BX76H)
IC2	555		(OH66W)	C9	470nF Polyes er		(BX80B)
IC3	CA3240E		(WO21X)	69	470hr roiges ei		(0,000)
IC4	CA3140		(OH29G)				
104	ONSITO		(41230)	Miscellaneous			
Miscella	220116			TR1	BC109C		(OB33L)
T1	Min Tr. 15v		(WB15R)	IC1	NE5534A		(YY68Y)
FS1	Fuse 20mm 100mA		(WROOA)	IC2	LF351		(WO30H)
131	Satuseholder 20		(RX96E)	IC3	LM13700N		(YH64U)
S 1	Switch rocker DP		(YR69A)			17 .00	(HF90X)
		2 off	(FHOOA)	JK1,2	%" Jack socket	(2 off) (2 off)	
\$2,3 JK1-3	Switch sub-min toggle A	3 off			Jack plugs	(Z OII)	(HF85G)
	%" jack socket	3 011	(HF90X)				
Mic 1	Crystal earpiece		(LB25C)				
	Jack Plug	3 off	(HF85G)				

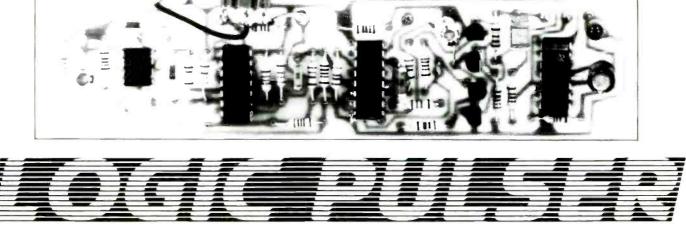
For anyone who builds or services circuitry incorporating TTL logic, a pulser is an invaluable piece of test equipment. This device enables the user to stimulate logic gate inputs when they are already connected into a circuit. This way it is often possible to test an I.C. which otherwise would have had to be removed with the associated trouble and possibility of damage. A logic pulser is usually used in conjunction with a logic probe which will locate and display the signal produced. The TTL pulser has the advantage of already having a pulse detector circuit built into it, thus making it versatile and easy to use.

The first half of the 7400 is used to de-bounce the biased toggle switch. Output pin 11 applies a negative edge to pin 5 of the 4049 via C1. The signal now travels in two different paths. Firstly, inverter output pin 6 switches on the transistors TR2 and TR4, so pulling down the output to logic '0'. The same signal from inverter output pin 4 eventually switches on transistors TR1 and TR3 as well, but this is delayed by the extra inverter, (pins 9 and 10) and capacitor C5. By the time that these two transistors conduct to take the output high, the output low condition has

Chris Bearman

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all to be mounted onto a single etched printed circuit board with the exception of the LED and the toggle switch which should be fitted into the housing. The resistors should be soldered in first, followed by the capacitors. Ensure that the correct polarity is observed when fitting the tantalum and electrolytic types. Solder in the four links on the board with pieces of wire. Putting aside the 4049 CMOS inverter, solder in the rest of the semiconductors. Careless handling of MOS devices can cause device destruction due to static buildup so care should be taken when the 4049 is soldered in. Try to handle the I.C. as little as possible without touch-



★ Makes checking IC functions much simpler ★ Inexpensive addition to your test gear ★ Easy-to-use

The pulser supplies a very short, but powerful, pulse each time the switch is depressed, the current of which will exceed half an Amp. This current is more than enough to overcome any TTL output, but could normally damage the I.C. being overridden, and therefore the pulse width is deliberately limited to a very short period. When the switch is depressed, the output will firstly fall to a logic low, and will then rise to give a logic high, so as to toggle the gate input regardless of the state it was previously being held at. When the pulse is completed the pulser's output will return to it's former high impedance state. By holding down the switch, a stream of pulses will be clocked out at around fifty hertz, which can be very useful when checking counting circuits, etc.

Circuit Description

A total of four I.C.'s and four transistors are used in the circuit, which is built on an etched printed circuit board. Around twenty-five milliamps at five volts is required from the host equipment's power supply for operation.

terminated. On completion of the high going pulse, the second pair of transistors are turned off, therefore allowing the output to return to it's high impedance state.

If the switch is held down for more than half a second, the clock generator IC3 will come into operation. Firstly C2 is allowed to charge up via resistor R9 until the 555 triggers. When this happens, its output (pin 3) will golow, so changing the state of output pin 6 of the R.S. flip-flop. This will now allow the 555 to oscillate in the astable mode, acting on inverter pin 5 via 1K ohm resistor R5. It will be noticed that two of the inverters in the 4049 package are not used but their inputs must be tied down to prevent any damage to the I.C. due to static build up.

The pulse detector part of the circuit is designed around a 74121 I.C. This I.C. is a monostable multivibrator which is used to extend the pulse detected to a length which may be observed on an LED. Each time a pulse is detected the LED will flash on.

Construction

The components for the pulser are

ing the pins once it has been removed from it's protective casing. Solder it in carefully using an earthed soldering iron. Lastly fit the vero pins to the board and connect up the LED and the switch. The cathode of the LED will be found to be adjacent to the flat on the body. The normally closed connection to the switch is that which is furthest from the toggle when in the biased position, the common connection is that in the centre.

Testing

Before applying power, check the circuit carefully for possible mistakes which could have been made in the assembly. Check in particular that the I.C.'s and the transistors are the right way round. If all appears well, connect a five-volt supply to the pulser with a milli-ammeter in series, observing that the current consumption should be in the order of 25-30mA. If it is very much higher than this, remove the power and look for any errors. Assuming that the consumption is correct, switch off, remove the meter and temporarily connect a wire from the pulse 'in' pin to the pulse 'out' pin. Reconnect the

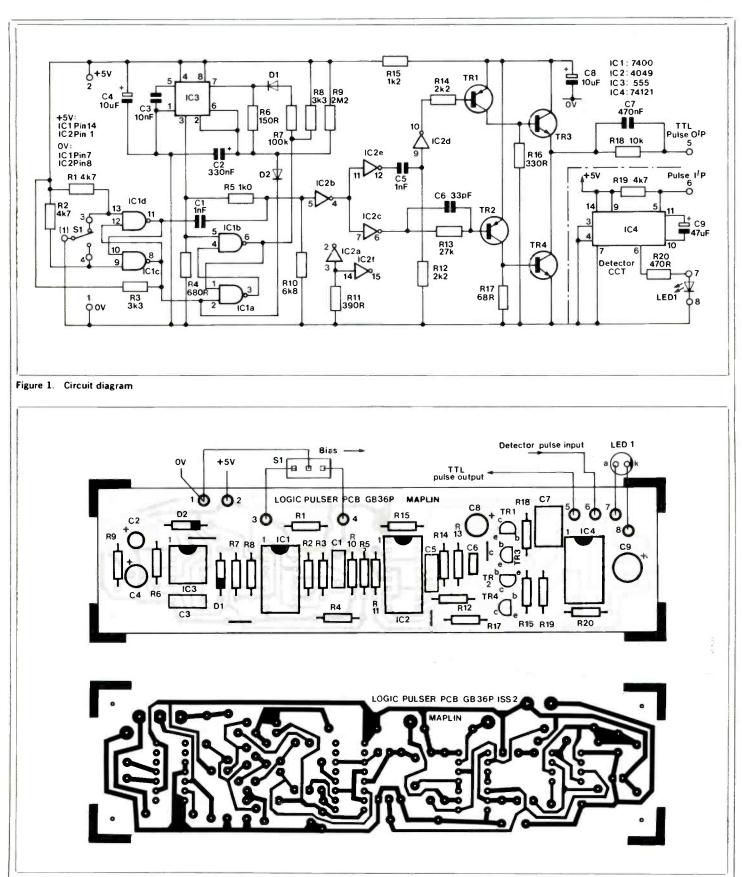


Figure 2. PCB layout and wiring diagram

supply and toggle the switch once. The LED should flash on once and go out. Now hold the switch in the 'on' position. The LED should flash once, then after half a second delay a stream of continuous pulses should be seen. Now temporarily connect a 10 ohm resistor firstly between the output of the pulser and ground, and then between the output and the +5V rail. Toggling the switch with the resistor in both of these positions should give the same results as found without it connected. This test shows the ability of the pulser to force both logic states sinking a current of over half an Amp. Now remove the 10 ohm resistor and the wire between the pulse in and out. The pulser is now ready for use.

Using The Pulser

Connect the supply from the circuit under test to the pulser. Now connect the pulse 'in' to the output of the gate to be tested and the pulse 'out' to the gate input. If the gate is working correctly, the LED will flash as the switch is toggled. To test a counter, connect the pulse 'in' to one of the counter outputs and the pulse 'out' to the counter input. When the switch is held down, the stream of pulses will keep clocking the counter enabling the pulse 'in' to be moved to the other outputs to check that they are all active. Alternatively each state of the counter may be checked by stepping through at the rate of one pulse at a time.

Continued on page 33.

EXTRA HIGH RESOLUTION GRAPHICS For the ZX81

- ★ Full 256 x 192 fine pixel display with normal/inverted video
- ***** Draws lines, circles and triangles, fills and textures.
- ★ Up to 32 user defined graphics

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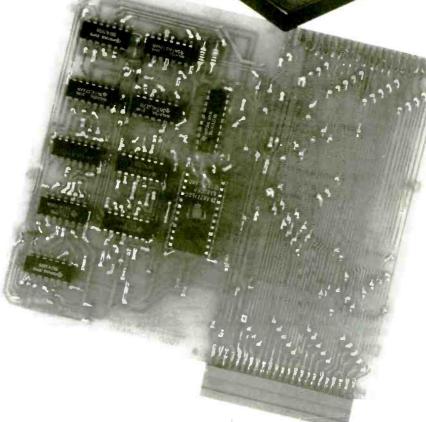
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* Operates directly from extended Basic

high resolution graphics module designed for the ZX81 with 16K-64K RAM availability. Access to the HI RES screen is made from extended basic commands such as SLOW n, FAST n, CLS n, and PLOT n,x,y which produce a 256 x 192 pixel display and keeps programming very simple for the operator. PRINTing to any pixel on the High Res screen enables characters, numbers or letters to be placed at will on the display, and both HI/LO RES screen's can be SAVED, LOADED or COPYed from BASIC.

How It Works

The module requires a minimum of 8K RAM connected externally (see Fig. 3) and also, the Sinclair 1 K RAM is used to store variables used by graphics routines and user defined character tables. The RAM is made to appear twice in memory map from 8K to 10K and IC 4,5,7 and 8K. ICII provides 2K of ROM containing graphics routines, which are pre-programmed, and appear in memory between 10K and 12K. A list of new variables appears further on, along with "routine" entry points and RAM areas useful for storing machine-code programs. The HI-RES display file is stored in a Basic program line at the end-of-program area. Being set up automatically, it moves around in memory as Basic lines are added or deleted, but is ignored by the computer as two newline characters (118) immediately follow the line number. Each row of pixels, are mapped from 34 bytes in the display file and 8 bits of each byte, map to 8 successive pixels on the screen (left most significant). Rows follow straight on from one another (top to bottom of the display) without any newline characters



at the end of each row.

Note that these variables are initialised only after the first HI-RES statement. Those marked * should not be poked at any time

Construction

Refer to the parts list for component designations

The module is quite easy to construct and track "throu" pins are used instead of wire links. These pins join tracks together on both sides of the PCB, and therefore should be soldered to each side. Insert track pins into all holes, marked with a circle on side A, 226 are required so keep count as you go. Push the head of each pin firmly down to the board with a soldering iron before applying solder. It is important to watch out for solder splashes and bridging across

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SYSTEM	VARIABLES		BYTES	ADDRESS	CONTENTS
BYTES	ADDRESS	CONTENTS	1	8983	"READ-POINT" BYTE, NOT ZERO IF PIXEL IS
2	8960	OFF-SET OF HI-RES DISPLAY FILE	-		SET
		ADDRESS, LESS 9, FROM THE "D-FILE"	1 *	8984	DISPLAY HEIGHT (NORM 192)
		VARIABLE	1	8985	FLAGS
2	8962	NOT USED	7	8986	TEMPORARY VARIABLES FOR PLOT
2	8964	START ADDRESS OF LAST LINE OF LO-RES			ROUTINE
		DISPLAY FILE	1	8993	PLOT OUT OF RANGE FLAT. BIT 7 = LATEST
2	8966	START ADDRESS OF HI-RES DISPLAY FILE,			STATEMENT
		LESS 9 (Used for video)	1	8994	NOT USED
2	8968	START ADDRESS OF HI-RES DISPLAY FILE	2	8995	X-COORDINATE FOR PLOT (SIGNED 16 BIT
2	8970	BYTES DEFINING TRIANGLE TEXTURE			NUMBER)
2	8972	CHARACTER TABLE ADDRESS FOR CHR8	2	8997	Y-COORDINATE
		0-63	8	8999	X AND Y COORDINATES FOR PREVIOUS 2
2	8974	CHARACTER TABLE ADDRESS FOR CHR8			PLOT STATEMENTS
		128-159	1	9007	FLAGS
2	8976	VECTOR FOR ADDITIONAL PLOT ROUTINES	4	9008	X AND Y COORDINATES OF GRAPHICS
3 🛪	8978	FLAGS			ORIGIN
2	8981	ADDRESS OF USER-DEFINED-CHR8 TABLE	4	9012	BYTES DEFINING 4 LINE TYPES
		(LESS 256)	2	9016	TEMPORARY VARIABLES FOR PLOT

System Variables

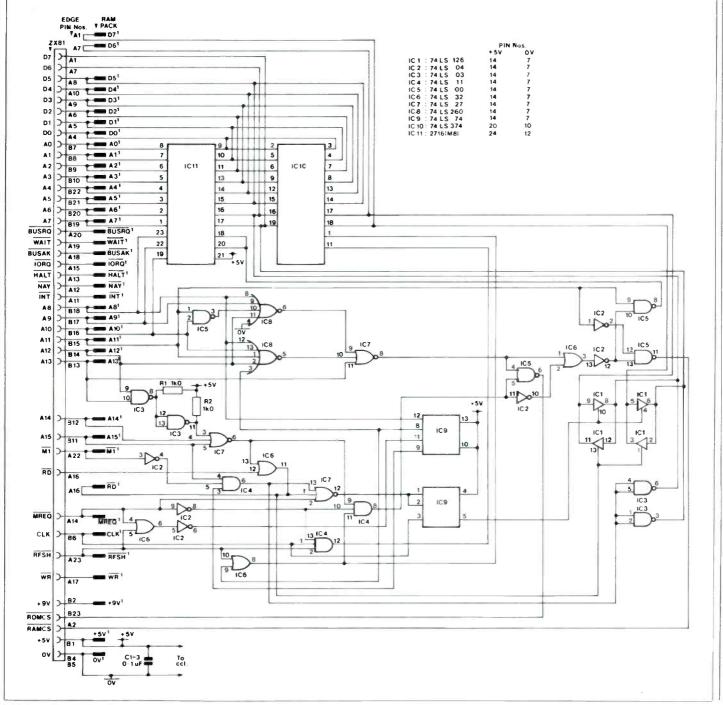


Figure 1. Circuit Diagram.

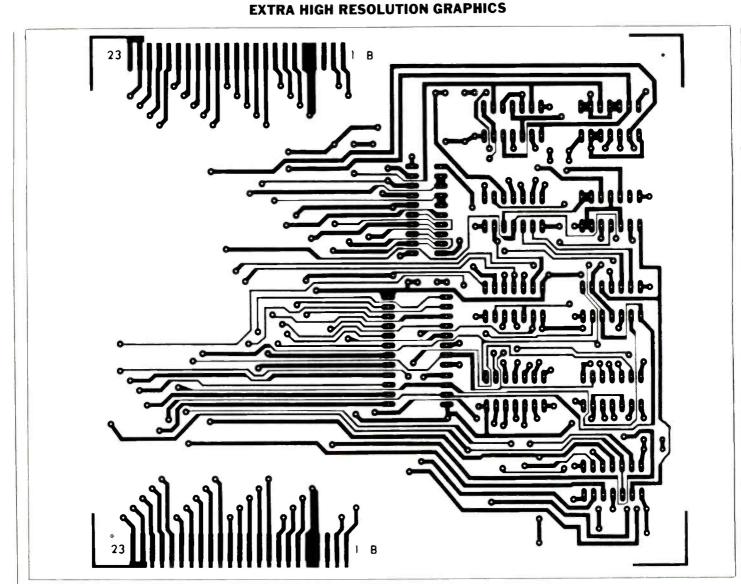


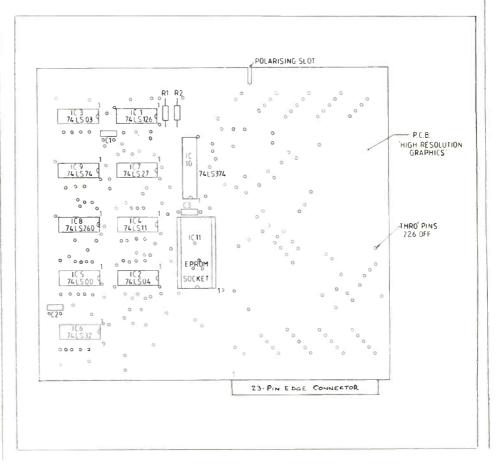
Figure 2. Artwork and Legend

track surfaces, as any mistakes introduced can be extremely difficult to find afterwards! Insert R1, R2 and C1 to C3. Fit the 24 pin dil Skt. (IC11) and mount all IC's. Solder each component lead, remove excess wire etc. and fit Eprom IC 11.

Two edge connectors are apparent on the PCB. One end has a slot cut in position three; the ram pack fits here. The other end requires a 2 x 23 way socket to be fitted which will insert into the ZX81 expansion port (or printer/ keyboard adaptor). Pins A3 and B3 are not used as the socket has a locating peg fitted in this position. Slot the socket terminals over the pads, and solder each one - they may need bending down to the board first! Clean both track faces with a suitable solvent and stiff brush, then closely inspect all joints. Special attention to detail may prevent damage to both module and ZX81 from occuring.

Testing and Using the Module

Connect module, ZX81 and RAM pack as shown in FIG. 3. If you wish to use a printer or external keyboard, connect these to the computer first, then fit the graphics module and RAM pack.



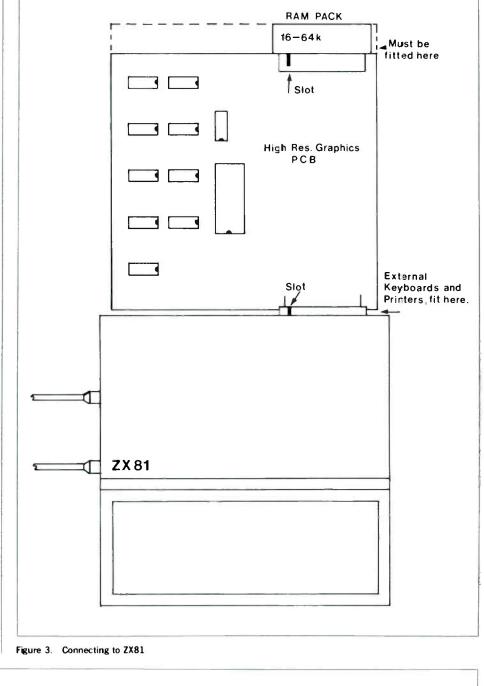
Connect up the computer and switch on. After several seconds, the [K] cursor will appear as normal (the actual time taken is dependant on the size of RAM used) if not, switch off and remove the module. Try running the computer and RAM pack only to make sure it still functions, then check the module for construction faults. One common fault when using PCB track pins, lies with not pushing them far enough through the board, but still applying solder, thereby hiding the fault. Other points to check are IC orientation and correct values in appropriate positions. Type SLOW 2 NEWLINE and if all is well, the statement Ø/GØØ7 will appear in the bottom left corner. Now type CLS 3 NEWLINE and the HI-RES screen will appear inverted in black with a white border. Of course, single key commands should be used - not individual letters! Type CLS 3 NEWLINE again and the HI-RES screen will revert to white. Type in a simple program line e.g. 10 REM NEWLINE. The [K] cursor appears but not the program, this is because SLOW 2 is a HI-RES mode command and program lines are not displayed in this mode. Now type SLOW NEWLINE and NEWLINE again. The screen is now back to LO-RES mode and line 10 will be displayed followed by G007 which is the start of HI-RES display area. By now, you can feel reasonably confident that the module is working, so type in PROGRAM 1 just to get an idea of what to expect.

PROGRAM 1

10 CLS 2 20 SLOW 3 For I = Ø to 255 30 PLOT 12, I, 191 40 50 PLOT 3, 255-1, 191 NEXT I 60 For I = Ø to 191 7Ø PLOT 12, Ø, I 80 90 PLOT 3, 255, 191 - 1 NEXT I 100 CLS 3 110 GOTO 30 120 **RUN NEWLINE**

SUMMARY OF BASIC STATEMENTSSTATEMENTOPERATIONPLOT 13@, X, YREPOSITIONS THE GRAPHICS ORIGINSLOW or SLOW ØSETS LO-RES MODEPLOT 13@, X, YHAS THE FOLLOWING EFFECTS FOR THESLOW 1 to 6SETS HI-RES MODE AND PRINT MODE AS FOLLOWS:n = 1DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN WHITESLOW 1PRINT CHRS, REVERSED VIDEOn = 2DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN BLACKSLOW 2PRINT NORMALord DINATES IN BLACKSLOW 3PRINT AT PLOT POSITION, TEXT FORE- GROUND, WHITEn = 4AS 3. BUT MISSING LAST POINT ON LINE TO ABSOLUTE CO- ORDINATES INVERTEDSLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3. BUT MISSING LAST POINT ON LINE n = 5.8SLOW 5PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 65-72AS 1 TO 4, BUT RELATIVE COORDINATES INFERSLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINESLOW 6CLEARS LO-RES DISPLAY CLS 1CLEARS LO-RES DISPLAY WITH BLACK CLS 2n = 97.104AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 1CLEARS HI-RES DISPLAY WITH BLACK CLS 2INVERTS HI-RES DISPLAY UST H-RES DISPLAYn = 9.16AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 1CLEARS HI-RES DISPLAY CLS1 and 2 also reset PLOT position and graphics origin to bettom leftPLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.				
STATEMENTOPERATIONPLOT n, X, YHAS THE FOLLOWING EFFECTS FOR THESLOW or SLOW ØSETS LO-RES MODEDIFFERENT VALUES OF n:-DIFFERENT VALUES OF n:-SLOW 1 to 6SETS HI-RES MODE AND PRINT MODE AS FOLLOWS:-n = 1DRAWS A LINE TO ABSOLUTE CO-SLOW 1PRINT CHR8, REVERSED VIDEOn = 2DRAWS A LINE TO ABSOLUTE CO-SLOW 2PRINT NORMALN = 3DRAWS A LINE TO ABSOLUTE CO-SLOW 3PRINT AT PLOT POSITION, TEXT FORE- GROUND, WHITEn = 4AS 3. BUT MISSING LAST POINT ON LINESLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3. BUT MISSING LAST POINT ON LINESLOW 5PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 5-8AS 1 TO 4, BUT RELATIVE COORDINATESSLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A COARSE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINECLS OR CLSØCLEARS HI-RES DISPLAY IN CLEARS HI-RES DISPLAY WITH BLACK CLS 2n = 97-1@4AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 1CLEARS HI-RES DISPLAY WITH BLACK CLS 2INVERTS HI-RES DISPLAY WITH WHITE CLS 1 INVERTS HI-RES DISPLAYn = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT Position.CLS1 and 2 also reset PLOT position and graphics origin to bottom leftposition.Position.	SUMMARY OF BASIC	STATEMENTS		
SLOW or SLOW ØSETS LO-RES MODEPRINT MODE ASPROT II, X, TPRAS THE POLLOWING EFFECTOR THESLOW 1 to 6SETS HI-RES MODE AND PRINT MODE AS FOLLOWS:n = 1DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN WHITESLOW 1PRINT CHR8, REVERSED VIDEOn = 2DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN BLACKSLOW 2PRINT NORMALor = 3DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN BLACKSLOW 3PRINT AT PLOT POSITION, TEXT FORE- GROUND, WHITEn = 3DRAWS A LINE TO ABSOLUTE CO- ORDINATES INVERTEDSLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3, BUT MISSING LAST POINT ON LINE n = 5-8SLOW 5PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 4AS 1 TO 4, BUT RELATIVE COORDINATESSLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A COARSE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINECLS OR CLSØCLEARS HI-RES DISPLAY CLS1 and CLEARS HI-RES DISPLAY WITH BLACK CLS 2n = 97-1@4AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT Position.CLS1 and 2 also reset PLOT position and graphics origin to bottom left Dosition.PLOT 16 miss out the Pixel and simply move the PLOT	STATEMENT	OPERATION		
SLOW 1SETS HI-RES MODE AND PRINT MODE AS FOLLOWS:n = 1DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN WHITESLOW 1PRINT CHR8, REVERSED VIDEOn = 2DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN BLACKSLOW 2PRINT NORMALn = 3DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN BLACKSLOW 3PRINT AT PLOT POSITION, TEXT FORE- GROUND, WHITEn = 3DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN BLACKSLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3, BUT MISSING LAST POINT ON LINE n = 5-8SLOW 5PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 4AS 1 TO 4, BUT RELATIVE COORDINATES INFSLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A COARSE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINESLOW 6CLEARS HI-RES DISPLAY FOREGROUND INVERTEDn = 97-1@4AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 0R CLSØCLEARS HI-RES DISPLAY WITH BLACK CLS 2CLEARS HI-RES DISPLAY WITH WHITE DISPLAY WITH WHITE CLS 1 INVERTS HI-RES DISPLAYn = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.	STATEMENT	OFERATION	PLOT n, X, Y	
FOLLOWS:ORDINATES IN WHITESLOW 1PRINT CHR\$, REVERSED VIDEOn = 2DRAWS A LINE TO ABSOLUTE CO-SLOW 2PRINT AT PLOT POSITION, TEXT FORE- GROUND, WHITEn = 3DRAWS A LINE TO ABSOLUTE CO-SLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3, BUT MISSING LAST POINT ON LINE ORDINATES INVERTEDSLOW 5PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 4AS 1 TO 4, BUT RELATIVE COORDINATESSLOW 6PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 33-40AS 1 TO 8, BUT WITH A COARSE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINESLOW 6CLEARS LO-RES DISPLAY FOREGROUND INVERTEDn = 97-104AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 0R CLSØCLEARS HI-RES DISPLAY WITH BLACK CLS 1CLEARS HI-RES DISPLAY WITH WHITE PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT Position.CLS1 and 2 also reset PLOT position and graphics origin to bettom leftposition.	SLOW or SLOW Ø	SETS LO-RES MODE		
SLOW 1PRINT CHR8, REVERSED VIDEOn = 2DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN BLACKSLOW 2PRINT NORMALn = 3DRAWS A LINE TO ABSOLUTE CO- ORDINATES IN BLACKSLOW 3PRINT AT PLOT POSITION, TEXT FORE- GROUND, WHITEn = 3DRAWS A LINE TO ABSOLUTE CO- ORDINATES INVERTEDSLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3. BUT MISSING LAST POINT ON LINE n = 5-8SLOW 5PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 4AS 1 TO 4, BUT RELATIVE COORDINATES DRAWS A LINE TO ABSOLUTE CO- ORDINATES INVERTEDSLOW 6PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 5-8AS 1 TO 8, BUT WITH A COARSE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINECLS 0R CLSØCLEARS LO-RES DISPLAY CLS1CLEARS HI-RES DISPLAYn = 97-1@4AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 1CLEARS HI-RES DISPLAY INVERTS HI-RES DISPLAYn = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.	SLOW 1 to 6	SETS HI-RES MODE AND PRINT MODE AS	n = 1	
SLOW 2PRINT AT PLOT POSITION, TEXT FORE- GROUND, WHITEn = 3ORDINATES IN BLACKSLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3. BUT MISSING LAST POINT ON LINE ORDINATES INVERTEDSLOW 5PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 5.8AS 1 TO 4, BUT RELATIVE COORDINATESSLOW 5PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 65.72AS 1 TO 8, BUT WITH A COARSE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINESLOW 6CLEARS LO-RES DISPLAY CLS 1CLEARS HI-RES DISPLAY INVERTS HI-RES DISPLAY WITH BLACK CLS 3n = 97-104AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 3INVERTS HI-RES DISPLAY INVERTS HI-RES DISPLAYn = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.		FOLLOWS:-		
SLOW 3PRINT AT PLOT POSITION, TEXT FORE- GROUND, WHITEn = 3DRAWS A LINE TO ABSOLUTE CO- ORDINATES INVERTEDSLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3. BUT MISSING LAST POINT ON LINE n = 5.8SLOW 5PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 4AS 1 TO 4, BUT RELATIVE COORDINATES n = 33.40SLOW 6PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 65.8AS 1 TO 8, BUT WITH A COARSE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65.72AS 1 TO 8, BUT WITH A FINE DOTTED LINECLS OR CLSØCLEARS LO-RES DISPLAY CLS 1CLEARS HI-RES DISPLAY INVERTS HI-RES DISPLAY WITH BLACK CLS 2n = 97-104AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 3INVERTS HI-RES DISPLAY INVERTS HI-RES DISPLAYn = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.	SLOW 1	PRINT CHR8, REVERSED VIDEO	n = 2	
SLOW 3INITIAL PLOT POSITION, TEXTn = 4ORDINATES INVERTEDSLOW 4PRINT AT PLOT POSITION, TEXTn = 4AS 3, BUT MISSING LAST POINT ON LINEFOREGROUND BLACKn = 5.8AS 1 TO 4, BUT RELATIVE COORDINATESSLOW 5PRINT AT PLOT POSITION, TEXTn = 33.40AS 1 TO 8, BUT WITH A COARSE DOTTEDBACKGROUND INVERTEDINVERTEDLINESLOW 6PRINT AT PLOT POSITION, TEXTn = 65.72AS 1 TO 8, BUT WITH A FINE DOTTEDCLS 0R CLSØCLEARS LO-RES DISPLAYn = 97.1@4AS 1 TO 8, BUT WITH A CHAIN DOTTEDCLS 1CLEARS HI-RES DISPLAY WITH BLACKn = 9.16AS 1 TO 8, BUT PLOTS A SINGLE PIXELCLS 3INVERTS HI-RES DISPLAYPLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOTCLS1 and 2 also reset PLOT position and graphics origin to bettom leftposition.	SLOW 2	PRINT NORMAL		
SLOW 4PRINT AT PLOT POSITION, TEXT FOREGROUND BLACKn = 4AS 3, BUT MISSING LAST POINT ON LINE n = 5-8SLOW 5PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 33-40AS 1 TO 4, BUT RELATIVE COORDINATES n = 33-40SLOW 6PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINECLS 0R CLSØCLEARS LO-RES DISPLAY CLS 1n = 97-1@4AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 2CLEARS HI-RES DISPLAY WITH BLACK CLS 3n = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.	SLOW 3	PRINT AT PLOT POSITION, TEXT FORE	n = 3	DRAWS A LINE TO ABSOLUTE CO-
SLOW 5FOREGROUND BLACKn = 5-8AS 1 TO 4, BUT RELATIVE COORDINATESSLOW 5PRINT AT PLOT POSITION, TEXTn = 33-40AS 1 TO 8, BUT WITH A COARSE DOTTEDSLOW 6PRINT AT PLOT POSITION, TEXTn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTEDSLOW 6PRINT AT PLOT POSITION, TEXTn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTEDCLS 0R CLSØCLEARS LO-RES DISPLAYn = 97-1@4AS 1 TO 8, BUT WITH A CHAIN DOTTEDCLS 1CLEARS HI-RES DISPLAY WITH BLACKLINECLS 2CLEARS HI-RES DISPLAY WITH WHITEn = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXELCLS 3INVERTS HI-RES DISPLAYPLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOTCLS1 and 2 also reset PLOT position and graphics origin to bottom leftposition.		GROUND, WHITE		ORDINATES INVERTED
SLOW 5PRINT AT PLOT POSITION, TEXT BACKGROUND INVERTEDn = 33.40AS 1 TO 8, BUT WITH A COARSE DOTTED LINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65.72AS 1 TO 8, BUT WITH A FINE DOTTED LINECLS OR CLSØCLEARS LO-RES DISPLAY CLS 1n = 97.104AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 2CLEARS HI-RES DISPLAY WITH BLACK CLS 3n = 97.104AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 3INVERTS HI-RES DISPLAY INVERTS HI-RES DISPLAYn = 9.16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.	SLOW 4	PRINT AT PLOT POSITION, TEXT		
BACKGROUND INVERTEDLINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINECLS OR CLSØCLEARS LO-RES DISPLAYn = 97-1@4AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 1CLEARS HI-RES DISPLAY WITH BLACK CLS 2CLEARS HI-RES DISPLAY WITH WHITE DISPLAY WITH WHITE CLS 3n = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.		FOREGROUND BLACK	n = 5-8	AS 1 TO 4, BUT RELATIVE COORDINATES
BACKGROUND INVERTEDLINESLOW 6PRINT AT PLOT POSITION, TEXT FOREGROUND INVERTEDn = 65-72AS 1 TO 8, BUT WITH A FINE DOTTED LINECLS OR CLSØCLEARS LO-RES DISPLAYn = 97-1@4AS 1 TO 8, BUT WITH A CHAIN DOTTED LINECLS 1CLEARS HI-RES DISPLAY WITH BLACK CLS 2CLEARS HI-RES DISPLAY WITH WHITE DISPLAY WITH WHITE CLS 3n = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXEL PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT position.	SLOW 5	PRINT AT PLOT POSITION, TEXT	n = 33-40	AS 1 TO 8, BUT WITH A COARSE DOTTED
FOREGROUND INVERTEDLINECLS OR CLSØCLEARS LO-RES DISPLAYn = 97-1@4AS 1 TO 8, BUT WITH A CHAIN DOTTEDCLS 1CLEARS HI-RES DISPLAY WITH BLACKLINECLS 2CLEARS HI-RES DISPLAY WITH WHITEn = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXELCLS 3INVERTS HI-RES DISPLAYPLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOTCLS1 and 2 also reset PLOT position and graphics origin to bettom leftposition.		BACKGROUND INVERTED		
FOREGROUND INVERTEDLINECLS OR CLSØCLEARS LO-RES DISPLAYn = 97-104AS 1 TO 8, BUT WITH A CHAIN DOTTEDCLS 1CLEARS HI-RES DISPLAY WITH BLACKLINECLS 2CLEARS HI-RES DISPLAY WITH WHITEn = 9-16AS 1 TO 8, BUT PLOTS A SINGLE PIXELCLS 3INVERTS HI-RES DISPLAYPLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOTCLS1 and 2 also reset PLOT position and graphics origin to bettom leftposition.	SLOW 6	PRINT AT PLOT POSITION, TEXT	n = 65-72	AS 1 TO 8. BUT WITH A FINE DOTTED
CLS 1 CLEARS HI-RES DISPLAY WITH BLACK LINE CLS 2 CLEARS HI-RES DISPLAY WITH WHITE n = 9-16 AS 1 TO 8, BUT PLOTS A SINGLE PIXEL CLS 3 INVERTS HI-RES DISPLAY PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT CLS1 and 2 also reset PLOT position and graphics origin to bettom left position.		FOREGROUND INVERTED		
CLS 1 CLEARS HI-RES DISPLAY WITH BLACK LINE CLS 2 CLEARS HI-RES DISPLAY WITH WHITE n = 9-16 AS 1 TO 8, BUT PLOTS A SINGLE PIXEL CLS 3 INVERTS HI-RES DISPLAY PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT CLS1 and 2 also reset PLOT position and graphics origin to bettom left position.	CLS OR CLSØ	CLEARS LO-RES DISPLAY	n = 97-104	AS 1 TO 8. BUT WITH A CHAIN DOTTED
CLS 3 INVERTS HI-RES DISPLAY PLOT 12 and PLOT 16 miss out the Pixel and simply move the PLOT CLS1 and 2 also reset PLOT position and graphics origin to bottom left position.	CLS 1	CLEARS HI-RES DISPLAY WITH BLACK		LINE
CLS1 and 2 also reset PLOT position and graphics origin to bettom left position.	CLS 2	CLEARS HI RES DISPLAY WITH WHITE	n = 9-16	AS 1 TO 8, BUT PLOTS A SINGLE PIXEL
CLS1 and 2 also reset PLOT position and graphics origin to bettom left position.	CLS 3	INVERTS HI-RES DISPLAY	PLOT 12 and PLOT	16 miss out the Pixel and simply move the PLOT
	CLS1 and 2 also reset	t PLOT position and graphics origin to bettom left		, , , , , , , , , , , , , , , , , , ,
side of the screen. In = 41-48 AS LIU & BUI DRAWS AND FILLS	side of the screen.		n = 41-48 -	AS 1 TO 8. BUT DRAWS AND FILLS
COPY OR COPY Ø COPIES LO RES DISPLAY TO PRINTER A TRIANGLE BETWEEN CURRENT AND	COPY OR COPY Ø	COPIES LO-RES DISPLAY TO PRINTER		A TRIANGLE BETWEEN CURRENT AND
COPY 1 COPIES HI-RES DISPLAY TO PRINTER PREVIOUS TWO PLOT POSITIONS	COPY 1	COPIES HI-RES DISPLAY TO PRINTER		PREVIOUS TWO PLOT POSITIONS
PLOT – 1, X, Y SAME EFFECT AS ORIGINAL PLOT X, Y n = 73-80 AS 41 TO 48, BUT THE TRIANGLE	PLOT - 1, X, Y	SAME EFFECT AS ORIGINAL PLOT X, Y	n = 73-80	AS 41 TO 48. BUT THE TRIANGLE
PLOT Ø, X, Y SAME EFFECT AS ORIGINAL UNPLOT X, Y IS TEXTURED, EXCEPT IN INVERT MODES	PLOT Ø, X, Y	SAME EFFECT AS ORIGINAL UNPLOT X, Y		





Program 1 produces a MOIRE PATTERN in both normal and inverted HI-RES MODES and is continual. Use BREAK to stop the program running.

The texture is defined by bytes 8970 and 8971. Useful values to POKE here are 0, 1, 17 and 85. If 16 is added to the above values for n, the "previous" PLOT position is unchanged once the PLOT statement is completed.

The 'READ POINT' byte at 8983 contains a non-zero number after a PLOT 12 statement, if the pixel is black.

Graphics Routines

5 routines can be called from machine code and the entry points are as follows:-

- 1. DELETE DISPLAY FILE. CALL ADDRESS 11737. Temporarily sets FAST mode and should be followed by CALL 519.
- 2. CHECK AND SET UP DISPLAY FILE. CALL ADDRESS 11807. Checks if a HI-RES display exists and sets up a new one if necessary. Also checks if system variables have been initialised.
- 3. CLEAR THE SCREEN. CALL ADDRESS 11858. Equivalent to CLS n in Basic and should be entered with REG A containing the required value of n.

 PLOT ROUTINES CALL ADDRESS 10566. ALL PLOT statement facilities are available by calling this routine. On entry, REG A must hold the appropriate PLOT number and REG's BC and DE must hold the X and

Y coordinates respectively. These coordinates are signed 16 BIT numbers.
5. SETTING HI/LO RES MODE. Display modes can be switched by changing the value held in the Z80 — I REG. Values of 30 and 31 in I set LO and HI-RES modes respectively.

An area of memory between addresses 8448 and 8703 is reserved for USER DEFINED CHARACTER definitions, but could be used for storing machine code etc. This area is protected from NEW. Also, 100 bytes of RAM are free from 9018 to 9117 which are safe from NEW, but will be cleared upon initialisation of the system variables. POKEing addresses outside of these ranges may cause a crash and is not recommended.

Point Plotting. Plot n, X, Y

The parameter n used in this statement behaves differently to the original PLOT and lies in the range — 1 to 130. Co-ordinates X and Y specify a position on the screen, which may be either absolute or relative. With absolute co-ordinates, the new PLOT position is given as X pixels to the right and Y pixels up from the Graphics origin, whereas with relative co-ordinates, the new PLOT position is given as X pixels right and Y pixels up from the previous PLOT position. The HI-RES screen has 256 pixels across and 192 pixels high with graphics origin located at the bottom left hand corner. Hence points on the screen have an X co-ordinate in the range \emptyset to 255 and Y co-ordinate in the range \emptyset to 191.

Drawing Lines

Lines are drawn from the previous PLOT position to the current PLOT position. If the current position is off the screen, it is interesting to note that lines will still be drawn to the edge of the display area. Various types of solid, dotted or dashed lines can be drawn as listed in the Basic statements, Also, note that broken line types can be obtained by adding 32, 64 or 96 to values of n that give solid lines.

Filling Triangles

Statements that will draw and fill in triangles are similar to those for drawing lines. Vertices of the triangle consist of the current PLOT position and the previous two PLOT positions. The triangle will only be filled if it lies completely within the screen. If any of the vertices lie off the screen, then error B will result. In invert mode, a triangle can be plotted, missing out the last edge or the edge between current and previous PLOT positions. This enables adjacent triangles to join up properly. Textured triangle fill is available for shading, cross-hatching etc. and is user definable. Two bytes 8970 and 8971 are rotated, respectively, by 1 and 3 bits to the right for each new row of the triangle. They are then ORed together, and the resultant pattern used to fill that row of the triangle.

PATTERN	897Ø	8971
Grey Left Diagonal Shading Right Diagonal Shading Right Diagonal Shading	85 Ø 17	0 17 0
(Coarse) Cross Hatching Fine Dots	1 17 Ø	Ø 17 1

Line Types

Four standard line types are determined by bytes 9012 — 9015 respectively. They can be re-defined by POKEing, the line pattern being an inverse of the bit pattern.

Read Point

The state of any pixel, on the screen, is determined by moving the PLOT position to that pixel, (USE PLOT 12) and then PEEK 8983. If number = 0 the pixel is white, otherwise a single bit of the number will be set, and the pixel black.

HI-RES Printing

The module provides six different modes of operation for the PRINT statement. A "PRINT mode set" number is given by the value of parameter n in the statement SLOW n or FAST n, used to set HI-RES mode. Text can be printed right down to the bottom of a HI-RES screen in all PRINT modes, but only as string results. If numeric results need to be printed, they should be converted to

strings by preceeding with STR8. (Note that SCROLL is inoperative in HI-RES mode). PRINT modes 1 and 2 are as for LO-RES, except mode 1 which is inverted. PRINT modes 3-6 are tied to the PLOT position which MOVES as characters are printed. Characters begin printing at the top left corner of the screen. A semi-colon, if used, holds the PLOT position at the end of the last character printed, otherwise the PLOT position goes to the start of a new line. As PRINT AT and TAB do not work, the PRINT statement is usually preceeded by a statement to move the current PLOT position (eg. PLOT 12 or PLOT 16).

User Defined Graphics

A section of the character set can be re-defined as required and PROGRAM 2 enables this to be done. CHRS 160 to 191 (inverse 4 to Z) are used for this purpose, allowing 32 characters to be stored in 256 bytes of RAM, starting at address 8448 and protected from NEW. Each character definition consists of 8 bytes corresponding to 8 rows of pixels in the CHR. 8 pixels in each row correspond to the 8 bits of each byte, with left most significance. To redefine a character, the 8 binary numbers for each row must be worked out as shown in Fig 4 and each number should then be POKEd into 8 consecutive memory locations of the first CHR table. The first address for the table will be 8448 + 8 * (character code -160) the character code being a number between 160 and 191. Memory locations outside of 8448 to 8703 must not be POKEd.

No.	ROW	TOTAL	CHARACTER							
			1	2	4	8	1	32	64	128
24	1	8+16								
24	2	8+16								
16	3	16								
120	4	8+16+32+64								
16	5	16								
28	6	4+8+16	Γ							
20	7	4+16				17				
36	8	4+32					- 7			

Figure 4. Re-defining CHRS

If CHR\$ 160 is to be re-defined, then from above formula; address = 8448 + 8 * (160) or 8448:

PROGRAM 2

- 10 SLOW 20 LET C = 160 30 FOR I = 0 TO 7
- 40 PRINT AT Ø, Ø; "GIVE ROW"; I + 1 50 INPUT N
- 50 INPUT N 60 POKE (8448 + 8 ***** (C - 160) + I), N
- 70 NEXT |
- 80 CLS 2
- 90 SLOW 2
- 100 PRINT CHR\$ 160

The program prompts for lines 1 to 8 so enter each number associated with that row from FIG 4. If other characters (161 to 191) are to be re-defined then LINE 20 and LINE 100 should be changed accordingly. Note that inverse CHR\$ 160 - 191 will be printed as normal in LO-RES mode, and the re-defined version printed only in HI-RES mode.

SAVEing HI-RES Pictures

Normally, the HI-RES display file is deleted automatically by the SAVE command. However a direct call to the save routine - RAND USR 764 - in FAST mode allows the HI-RES display to be saved with a name, or empty string (SAVE " ") Before loading, ensure the display is set or type CLS 2 otherwise it will be deleted by the first HI-RES statement in the program.

Finally, the command POKE 8833, Ø (or 237) will correct a display that bends at the top of a picture, and should be done after a HI-RES display file is set up. Following, are three programs showing circle plotting and three-dimensional effects and are worth entering.

PROGRAM 3 "CIRCLES" 10 LET D = 0.099 LET X = 90 20 3Ø LET Y = Ø 4Ø CLS₂ 50 SLOW 4 PLOT 130, 127, 95 6Ø 7Ø PLOT 12, X, Y 80 FOR I = Ø TO 63 LET $X = X + D \star Y$ LET $Y = Y - D \star X$ 90 100 PLOT 2, X, Y + X + D/2 110 120 NEXT I 130 PLOT 9, 127, 95 14Ø LET X = X - 10CLS 3 GOTO 70 150 160 RUN NEWLINE

PROGRAM 4 "CONTOURS" 10 CLS 2 2Ø SLOW 2 3Ø PLOT 130, 127, 10 FOR $P = \emptyset$ TO 12 40 LET X 1 = P + 10 50 LET Y $1 = P \pm 7$ 60 FOR Q = Ø TO 12 70 8Ø LET $Z = -20 \pm SIN(P/2) \pm SIN(Q/2)$ LET $X2 = (P-Q) \pm 10$ 90 LET $Y_2 = Z + (P+Q) + 7$ 100 PLOT 12, - X1, Y1 PLOT 2, - X2, Y2 PLOT 12, X1, Y1 110 120 130 140 PLOT 2, X2, Y2 LET X1 = X2150 160 LET Y1 = Y2170 NEXT O NEXT P 180 190 CLS 3 RUN NEWLINE

PROGRAM 5

1Ø C_S 1 FAST 2 2Ø PLOT 130, 127, 100 30 40 FOR X = 1 TO 120 STEP 2 LET $U = X \star X$ 50 LET L = INT (0.5 + SQR (14400 - U)/4)60 70 LET M = -10080 FOR Y = -L TO LLET R = (U + Y + Y + 16) / 1000 LET Z = 2.5 + Y - 150 / R + SIN R 90 100 IF Z < M THEN GOTO 150 110 120 LET M = Z1.30 PLOT 9, X, Z PLOT 9. - X. Z 140 150 NEXTY 160 NEXT X **RUN NEWLINE** This program takes about four minutes to run, but the result is quite spectacular.

PARTS LIST FOR **ZX81 HI-RES GRAPHICS** Resistors - All 0.41 R1.2

Capacitors

Semiconductors

C1-3

IC1 1C2

IC3

IC4

105

106

Lo unin			IC7	141521		(YF18U)
).4W 1% meta 1k0	il film 2 off	(M1KO)	IC8 IC9 IC10 IC11	74LS260 74LS74 74LS374 2716(M8)		(QY59P) (YF31J) (YH16S) (QY58N)
10nF disc	3 off	(BXOOA)	Miscellaneous	P.C. Board Track pin	5 pkts	(GB43W) (FL82D)
74LS 126 74LS04 74LS03 74LS11		(YF50E) (YF04E) (YF03D) (YF09K)		Socket 24 Pin DIL Socket 2x23 way P.C. Edgecon		(BL20W) (RK35Q)
74LS00 74LS32		(YF00A) (YF21X)	A Kit containi	ng all the parts listed Order As LK23A	above is	avail able

LOGIC PULSER Continued from page 27.

PARTS LIST FOR LOCIC DIII CED

FARISL	IST FOR LOGIC PULSE	.п		C4,8	10uF 35V PC electrolytic	2 off	(FFO4E)	
Resistors - All	10.4W 1% metal film unless specified.			C6	33pF ceramic		(WX50E)	
R1,2.19	4k7	3 off	(M4K7)	C7 C9	470nF polycarbonate 47uF 25V PC alectrolytic		(WW49D) (FF08J)	
R3,8	3k3	2 off	(M3K3)	0,	that cot no dectrolytic		(11005)	
R4	680R		(M680R)	Semiconductors				
R5	1k0		(M1KO)	D1.2	1N4148	2 off	(OL80B)	
R6	150R		(M150R)	TR12	2N3703	2 off	(OR27E)	
R7 R9	100k 2M2 0.3W 5% carbon film		(M100K)	TR3,4	2N3704	2 cff	(QR28F)	
RIO	6k8		(E2M2) (M6K8)	IC1	7400		(QX37S)	
R11	390R		(M390R)	IC2	4049UBE		(QX21X)	
R12.14	2k2	2 off	(M2K2)	1C3	NE555		(QH66W)	
R13	27k		(M27K)	IC4	74121		(QX73Q)	
R15	1k2		(M1K2)	Miscellaneous				
R16	330R		(M330R)	Miscellaneous	PC board		(GB36P)	
R17	68R		(M68R)		Veropin 2141	1 Pit	(FL21X)	
R18	10k		(M10K)	S1	SPCO (Biasec) Sub-min toggle	I I M	(FF70M)	
R20	470R		(M470R)	LED1	LED red		(WL27E)	
O					LED clip		(YY40T)	
Capacitors -	1eF only anybarate	0 - 44	(MANDOW)					
C1,5 C2	1nF polycarbonate 330nF tantalum	2 off	(WW22Y) (WW57M)		A complete kit of all parts is av	ailable.		
C3	10nF polycarbonate		(WW29G)		Order As LK19V.			
	tom porjear bondie		(111230)				an loong	

by Mark Brighton

- Allows the VIC to be fully expanded
- Three expansion sockets, one switchable
- * Optional 3K RAM on board
- Cheaper than conventional **3K RAM cartridge**

ne problem frequently experienced by the author when programming the VIC20, especially when using hi-res graphics, is lack of memory (within the computer, usually!) This may, of course, be easily overcome by plugging a RAM pack into the expansion socket, but this creates a new problem. No longer is it possible to use a Superexpander/Machine Code Monitor/Forth cartridge etc., because the socket is occupied.

Therefore the subject of this article is an extension board which plugs into the memory expansion connector on the VIC20, and provides three sockets into which any combination of RAM/ ROM cartridges may be plugged (within reason, of course, - two games cartridges at once would give your VIC a severe headache).

In addition to these expansion sockets it was considered worthwhile to include a built-in 3K RAM extension on the board, thus freeing a socket from carrying the 3K RAM cartridge. This is optional, however, and may be omitted. if desired, by leaving out ICs 1 to 6 and capacitors 1 to 5 inclusive.

For those who wish to experiment with switching blocks of memory in or out, during initialisation for example. the block select lines on the rear socket are switchable

Construction

Referring to the circuit diagram and parts list, locate and fit all capacitors. switches, and IC sockets, then solder

them to the board. Observing normal

The second second

NDPBC

precautions for CMOS devices, plug ICs 1 to 6 into their sockets. Clean the board and inspect for short circuits, dry joints, etc

Testing

Plug the extension board into the memory expansion connector on the rear of the VIC, and switch the computer on. If all is well, the VIC should initialise and display the message 6655 BYTES FREE', (if ICs 1 to 6 are

included). Now try entering and running a small BASIC program from the keyboard to check the operation of the 3K RAM extension. Program 1 would be suitable. Lastly, try a game cartridge, or similar, in each of the three sockets of the board in turn. Remember to switch the computer off before attempting to remove or replace a cartridge or the extendiboard

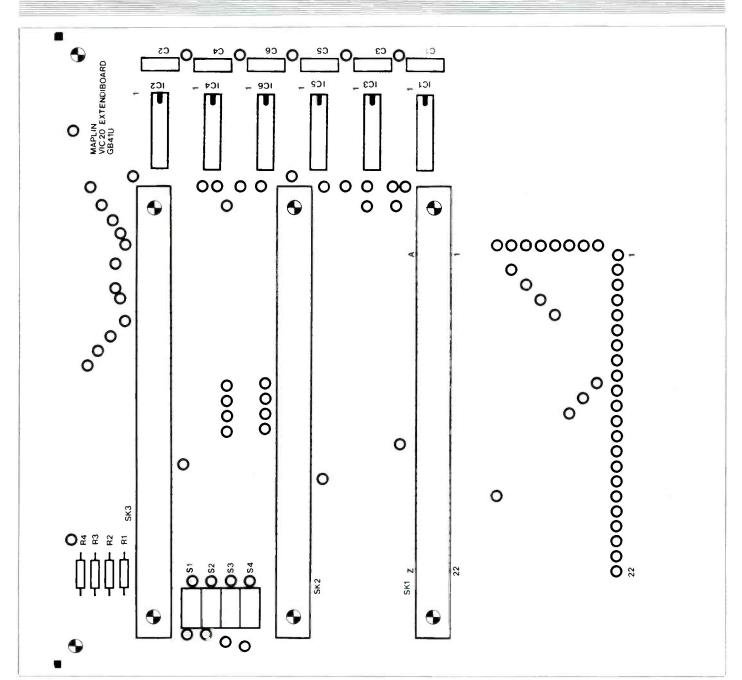


Figure 2. PCB layout.

Usage

As there are many possible uses for an extension board such as this, they could not all be covered in this article. However, I shall attempt to outline a few:

One 16K RAM cartridge and one 8K RAM cartridge, for those who write very long programs or wish to handle large amounts of data. This is the maximum memory extension available to BASIC on the VIC20.

The machine code monitor cartridge is not normally usable in the fully expanded VIC, as its address area lies within the top 8K RAM area. It could, however, be used in place of the 8K RAM cartridge, which still leaves a very considerable area for machine code program storage.

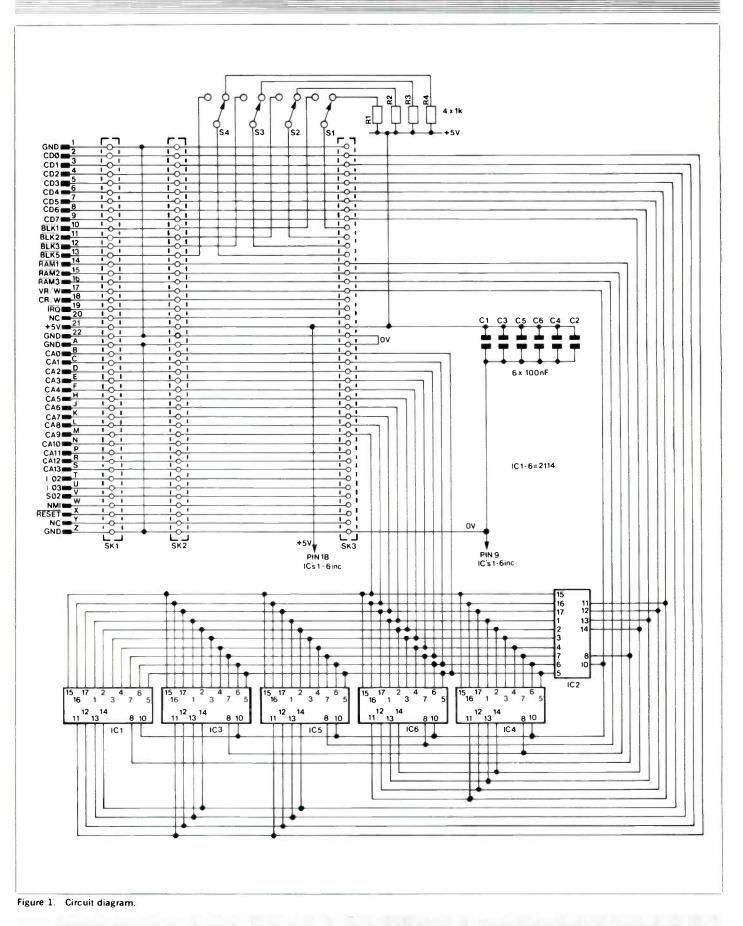
Maplin Talkback, or similar addons, plus extra RAM if required, can now be used together. Programs can be written using hi-res graphics, complex sound effects, and speech synthesis in BASIC or machine code. Your pro-



gramming abilities and imagination can come into full play — the possibilities are limitless.

It should be remembered that if 8K or 16K RAM cartridges are used, then the board 3K expansion, or 3K RAM cartridge, are not available for BASIC

program storage, due to the way the operating system arranges screen memory during initialisation. This area (decimal 1024 to 4095) is still useful for data storage using PEEK and POKE from BASIC, or may hold machine code to be executed using 'SYS' or 'USR'.



PARTS LIST FOR VIC20 EXTENDIBOARD

Resistors — All O	4W 1% Metal Film.		
R1-4 inc.	1k	4 off	(M1K)
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Switch SPDT Quad 0.156" 2 x 22 Way P.C. Edgecon VIC20 extendiboard Track pin

(XX29G) 3 off (BK79L) (GB41U) 2 pkts (FL82D)

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S1-4

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