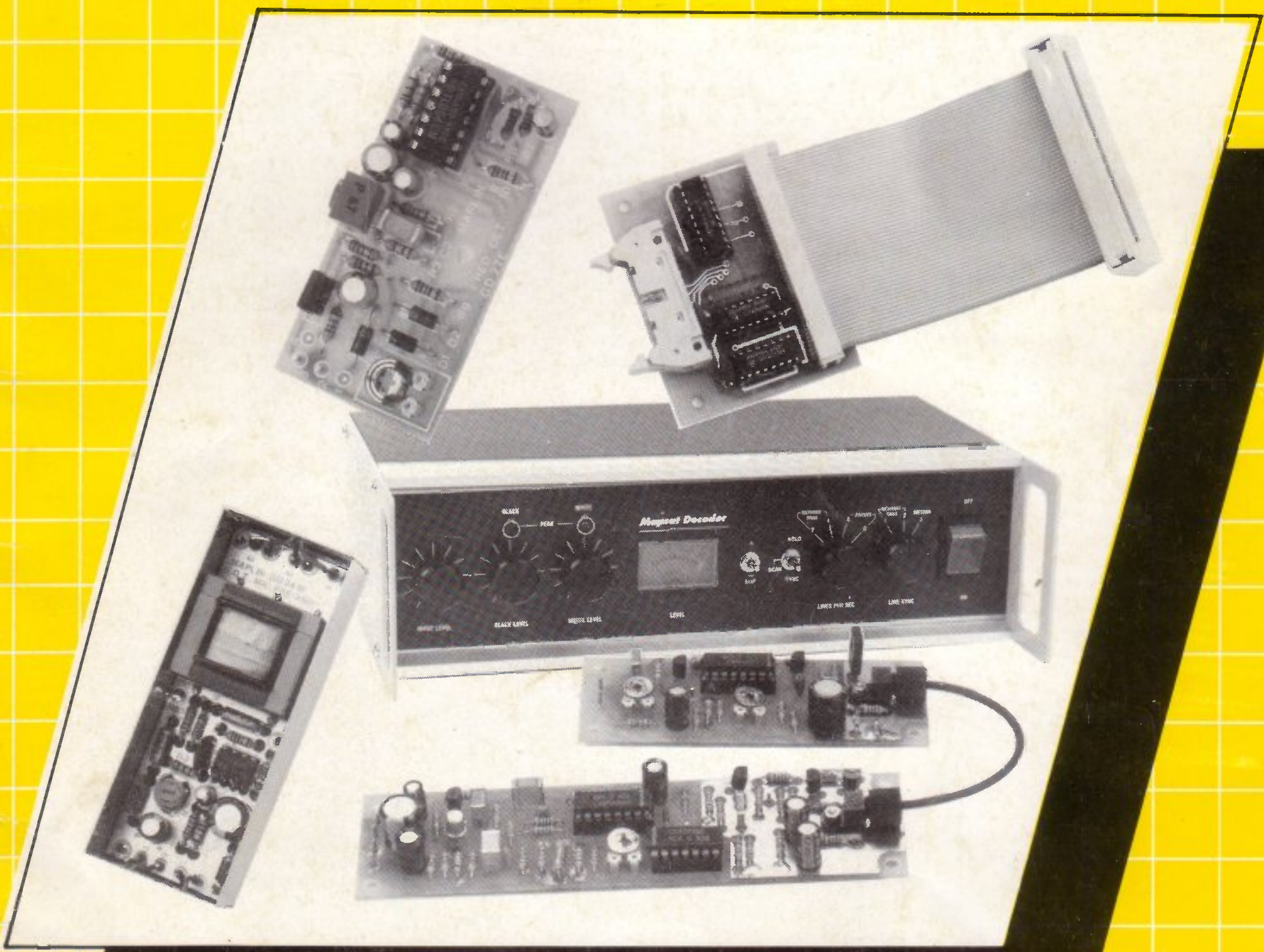
PROJECTS BOOK 20

Maplin Maplin Maplin



FIBRE-OPTIC AUDIO LINK
WEATHER SATELLITE DECODER
LOW-Z MICROPHONE PREAMPLIFIER
INFRA-RED PROXIMITY DETECTOR
AMSTRAD 8-BIT PORT

Electronics
THE MAPLIN MAGAZINE

PROJECT BOOK TWENTY

This Project Book replaces issue 20 of 'Electronics' which is now out of print. Other issues of 'Electronics' will also be replaced by Project Books once they are out of print. For current prices of kits, please consult the latest Maplin price list, order as XF08J, available free of charge.

CONTENTS

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The Fibre Optic Audio Link serves as an interesting alternative to the traditional pair of wires carrying audio signals from one point to another. Fibre optics are used extensively these days in the fields of communications, TV and Radio, computer data transmission, medicine and even motor vehicles – to name but a few!

Optical Fibre

The light guide itself may consist of many strands of fine, drawn, glass fibres or a single, solid fibre made from polymethyl-methacrylate and enclosed with a polymer cladding and protective sheath. Unlike cables and wires, the fibres do not carry an electric current, but instead reflect light waves along their length.

Therefore electrical signals must be converted into light and sent along the guide. At the far end, the light waves are re-converted back into electrical signals, closely resembling the original. Unfortunately, fibres exhibit the luminal equivalent of resistance which increases proportionately with length and limits the maximum length of guide which can be used in any particular system. Attenuation effects can be measured at 1.2dB per metre, or approximately a 20% reduction with the light guide recommended for use with this project (XR56L).

The maximum useable range of these modules is limited to 20 metres (65 feet approx) provided that the fibre ends are 'polished' for optimum light transfer.

Characteristics

Frequency Response	– 50Hz to 20kHz (−6dB) Flat from 150Hz to 3kHz
Max I/P and O/P Levels	– 0dB (775mV rms) @ 1kHz
Minimum I/P Level	– −28dB (30mV rms) for rated O/P
Noise Level	– 10mV
Signal to Noise Ratio	– 35dB
T.H.D. @ 1kHz	– 1.0%
P.L.L. Carrier Frequency	– 95 to 120kHz (110kHz nom)
PSU (Tx)	4.8 to 6V DC @ 30 to 50mA (Average) Recommended, +5V DC @ 38mA
PSU (Rx)	4.8 to 12V DC @ 5 to 12mA Recommended, +9V DC @ 8mA

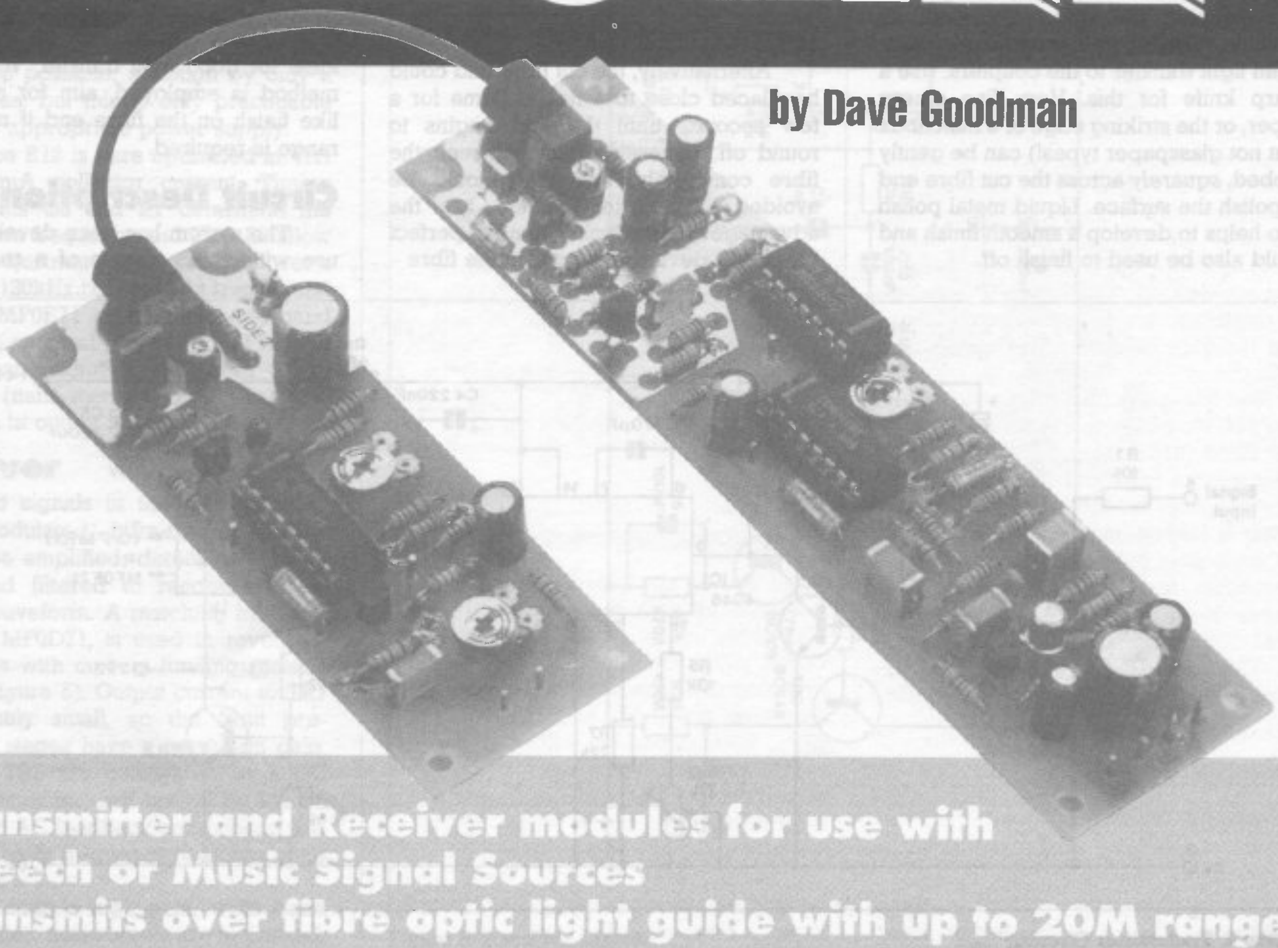
All specifications apply to the prototypes and may vary between different modules. Use recommended supplies for optimum performance.

Fibre Optic Couplers

A simple system for connecting the light guide to each module is shown in Figure 1. Both Emitter and Detector units contain an Infra Red PIN Diode and lens contained in the FLCS housing. Prepared light guide ends are inserted through the cap, which is then screwed onto the housing, up to finger tightness. The cap contains a compression ring which grips the light guide tightly and prevents it from being easily pulled out, see Figure 2.

FIBRE OPTIC AUDIO LINK

by Dave Goodman



★ Transmitter and Receiver modules for use with Speech or Music Signal Sources
★ Transmits over fibre optic light guide with up to 20M range

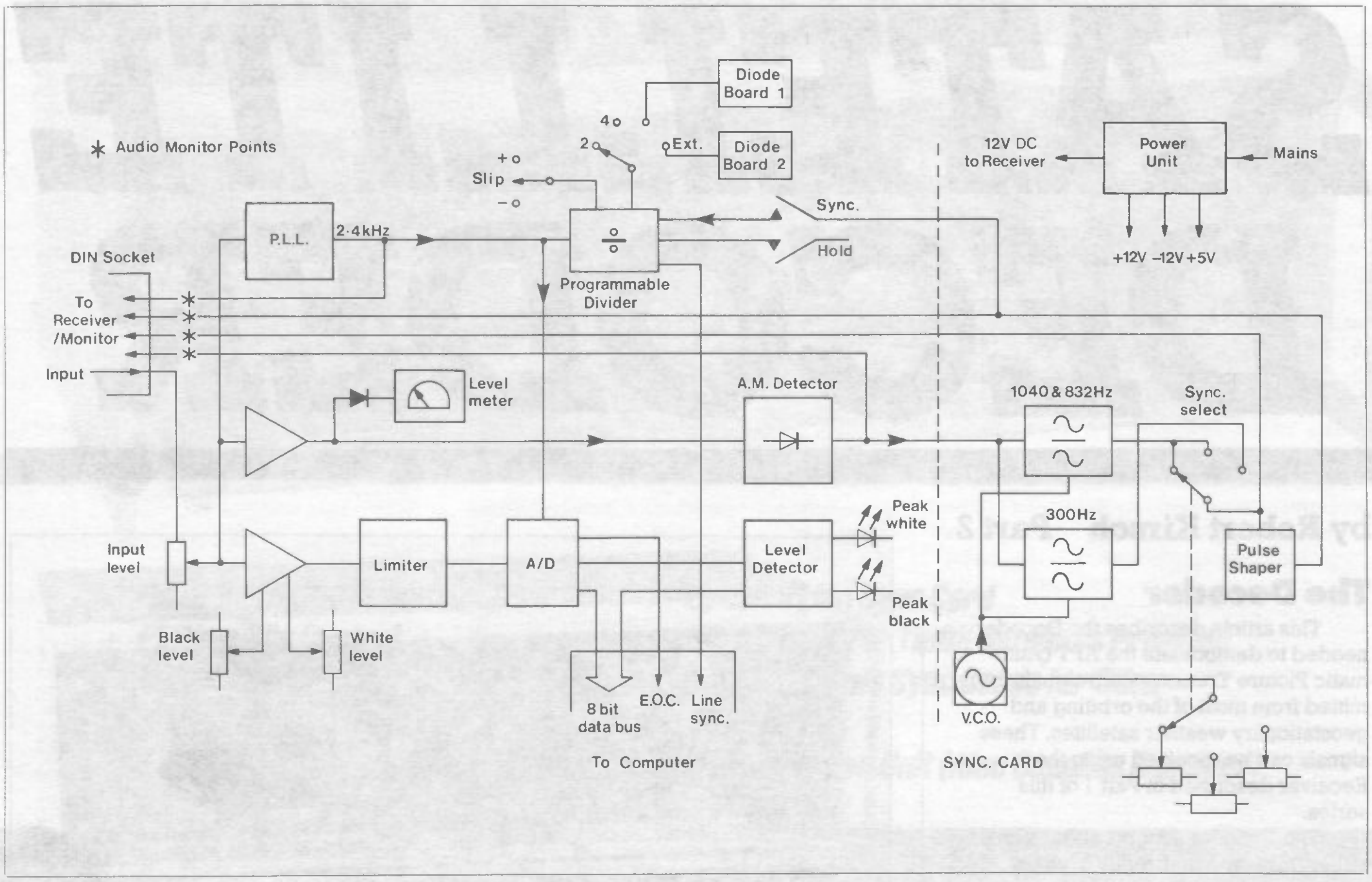


Figure 2. Decoder Block Schematic.

The conversion from the analogue subcarrier level to a digital code is accomplished by IC2, an 8-bit A/D converter. This device requires two inputs, one is the analogue information, and the other is a 'start conversion pulse'. The analogue input range of IC2 is from 0 to 2.5 volts to give codes from black to peak white. It is therefore important to adjust the level of the incoming signal in order to obtain correct contrast on the displayed picture. This function is provided by the op-amp IC1a. The gain of this device is adjusted by RV5 in the feedback circuit, this sets the white level. The output from IC1a is about ±2.5 volts but only the positive half cycle is fed to the A/D converter. RV4 sets the DC reference of the op-amp, and this offset is used to adjust the black level of the picture. Note, there is always a small amount of carrier at black level for synchronising purposes, so this circuit enables this level to produce true black on the display. The black and white level controls may also be used to enhance pictures particularly when only a few grey levels are available from the computer or frame store used.

The two light emitting diodes LED1 and LED2 are used to obtain the correct setting for the black and white level controls. The most significant bit from the output of the A/D converter is monitored and, when this bit goes high, TR2 turns on and causes LED2 to light, this indicates a level approaching peak white. All 8 bits are fed to the NOR gate IC5. When all 8-bits are low the output of this gate turns TR1 on, causing LED1 to light and indicate black level.

The second op-amp, IC1b, is fed with the incoming signal via the input level control. The output from IC1b is rectified by D3 and D4 to drive the level meter which should read full scale on a peak white signal. The AM detector formed by D1 and D2 is also fed from the output of IC1b and this audio signal is fed to the sync tone decoder card.

The phase locked loop, IC3, is fed with the incoming modulated signal and locks to the 2.4kHz subcarrier. The clean square wave output produced is used to generate the 'start conversion' pulse for the A/D converter and it is also fed to the programmable divider to produce line synchronising pulses.

The three counters IC6, 7 and 8 form the programmable divider whose division ratio is set by the data on pins 3, 4, 5 and 6 of each IC. The rotary switch S2 selects one of two preset ratios (1200 for 2 lines per second and 600 for 4 lines per second) and also two ratios that may be set by programming the optional diode cards, the circuit of which is shown in Figure 4. The SLIP control, S3, temporarily raises or lowers the division ratio to enable the picture to be moved in relation to the line sync pulse thus shifting the display left or right in relation to the television screen. The phase locked loop will produce an output even when no input is present, and therefore line sync pulses will also occur. For this reason the HOLD switch is provided to stop the

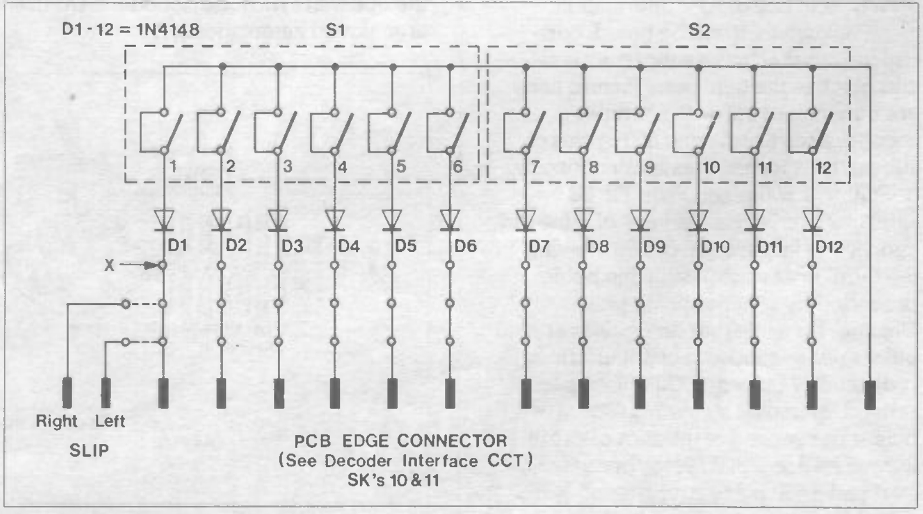


Figure 4. Diode Card Circuit.

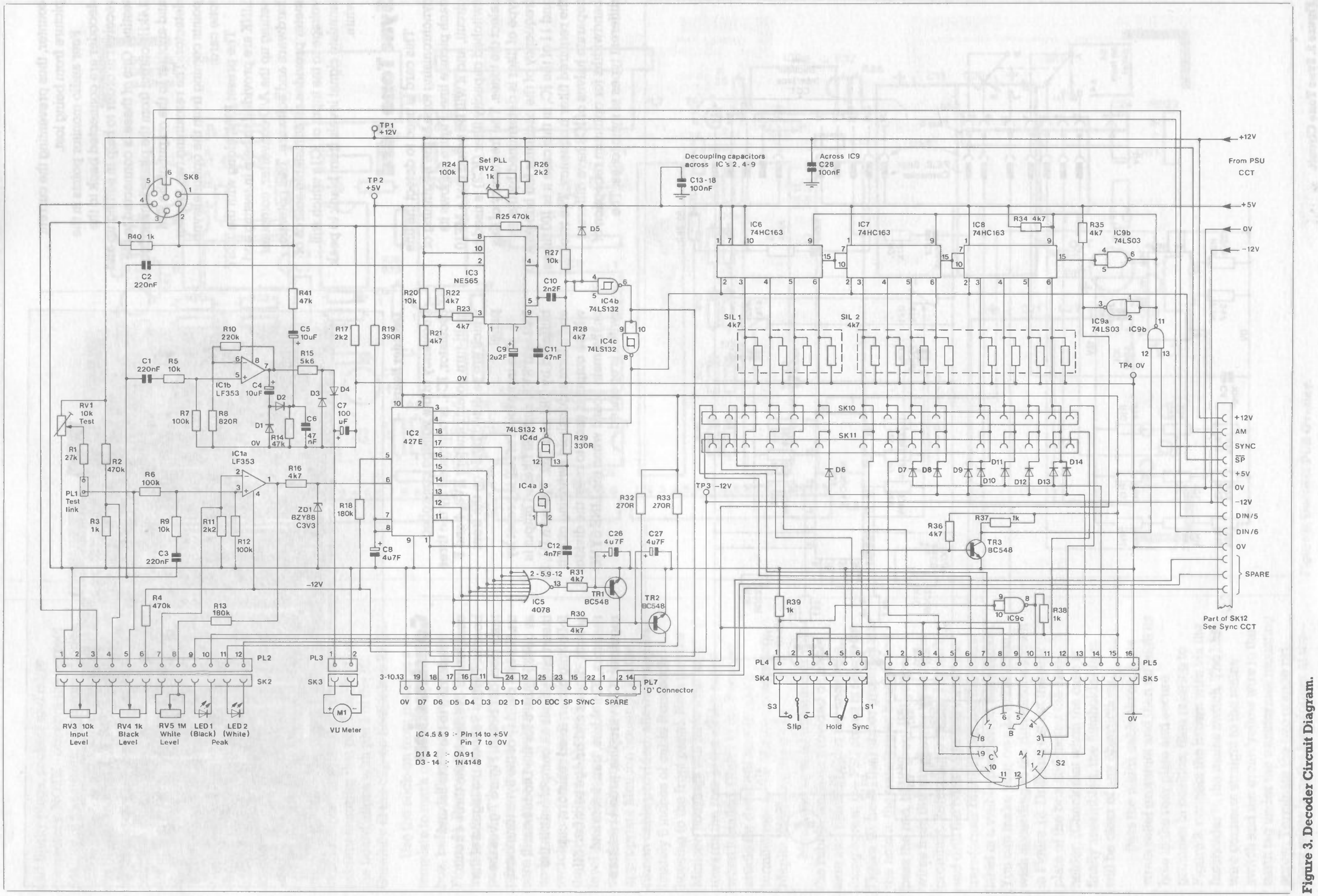
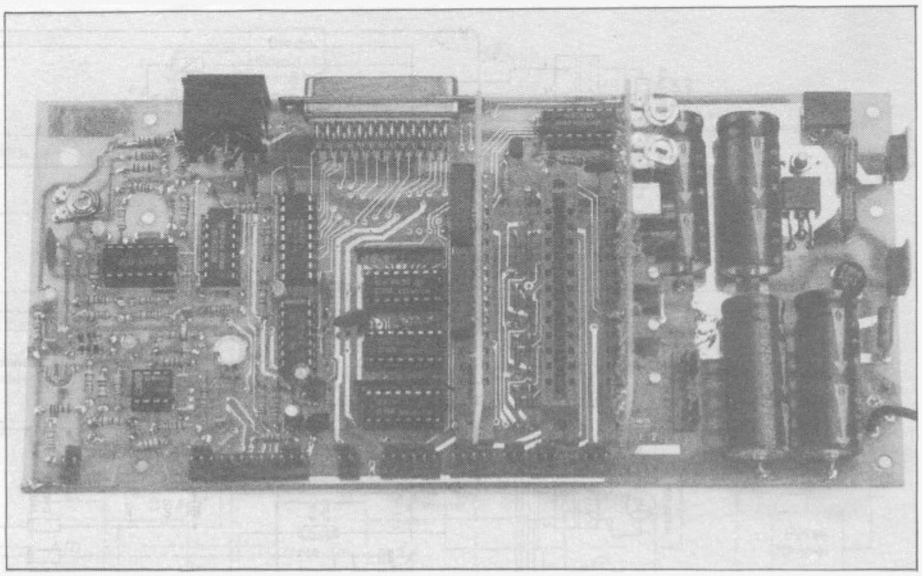


Figure 3. Decoder Circuit Diagram.

counter, thus preventing the current picture from being lost.

Four audio monitor points in the decoder are connected back to the receiver in order to help in setting up and testing. One of these is connected to the 2.4kHz output from the phase locked loop and another to the output of the AM detector. The remaining two monitor points coming from the optional sync tone card.

The preset RV1, along with the TEST LINK are provided to help in testing and setting up the A/D converter, computer hardware and software. This potentiometer provides an adjustable source of voltage to the input of IC1a which will simulate signal levels from black to peak white.



Decoder Board

Sync Tone Card

This card is used to detect the line synchronising tone at the beginning of each picture line. Figure 5 shows its circuit, and it will be noted that a MF10 switched capacity filter (IC2) is used to select the tones. The frequency of this type of filter is determined by the frequency of the oscillator fed into pins 10 and 11 of the IC, in this case it is 100 times the required filter frequency. The two separate halves of IC2 have different bandwidths for optimum reception of different types of sync tones. The frequency of the voltage controlled oscillator, IC1, is controlled by the three multi-turn potentiometers RV3, 4 and 5 which are selected by S4 on the front panel.

The input level of IC2 is preset by RV1 and RV2, and the filtered output is buffered by TR1 and TR2. TR3 with D1, 2 and 3 form a threshold switching circuit whose output is used to reset the divider on the main board when the LINE SYNC switch is operated.

Construction

Referring to the Parts list and component overlay on the three circuit boards, Figure 6 shows the legend of the main decoder board, Figure 7 gives the tracks and overlay of the Sync tone card, as does Figure 8 for the Diode board; insert and solder all components in the following order: fixed resistors, capacitors, diodes and bridge rectifier, SIL resistors, IC holders, transistors and regulator IC's; veropins, preset resistors

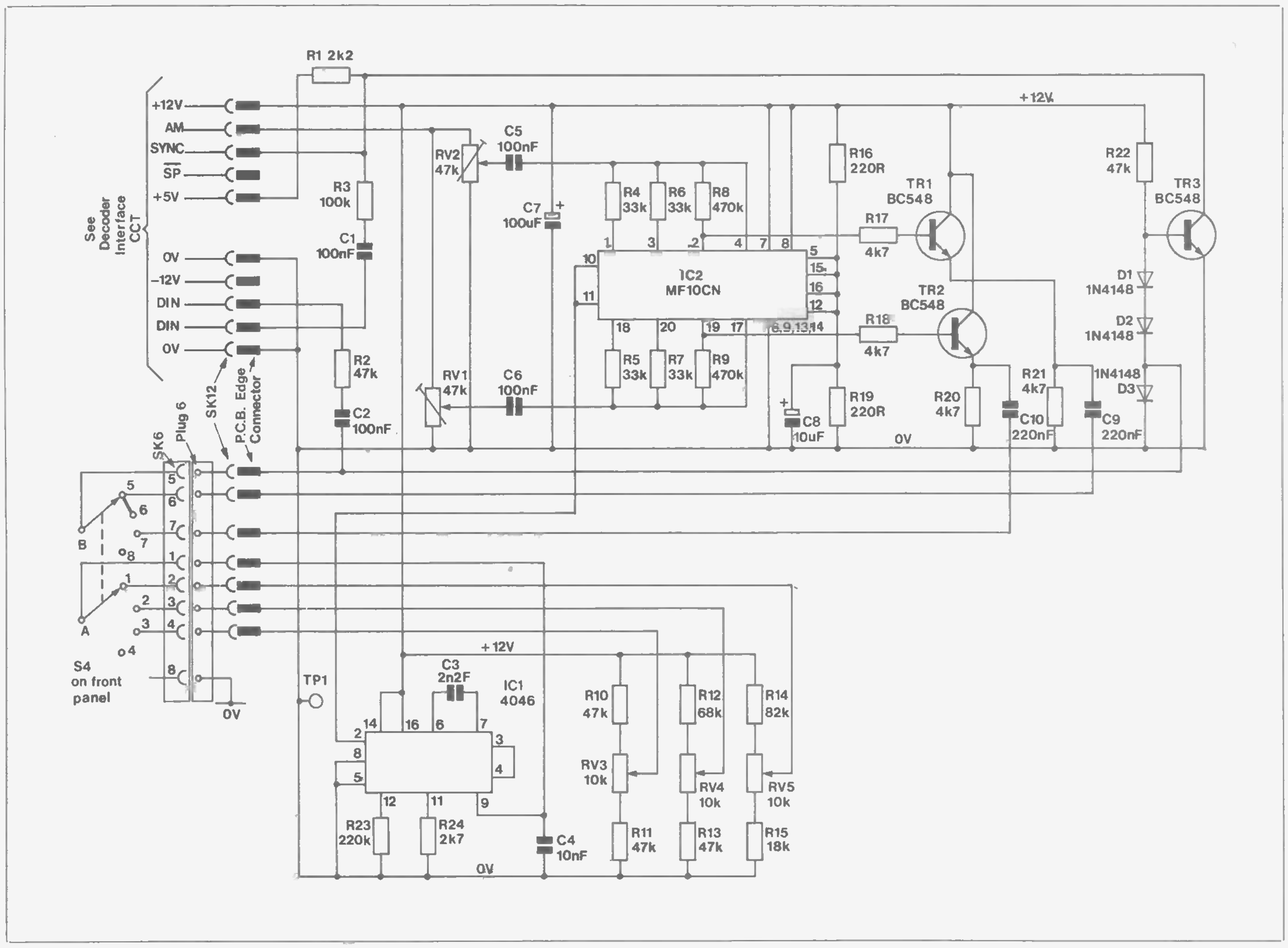


Figure 5. Sync Tone Circuit.

and finally plugs, sockets and edge connectors. **NOTE** - observe the correct polarity of transistors, regulators, diodes, LED's, meter, electrolytic capacitors and the bridge rectifier. The white dot marked at one end of the SIL resistor package should correspond to the white dot on the board overlay. The tags of the Minicon plugs should be to the rear of the circuit board. The white rings on the overlays indicate where the boards should be soldered on *both* sides; in addition TR1 on the sync card should be soldered on both sides also.

Insert the keys into the edge connectors, referring to the wiring diagram Figure 9. Carefully insert all integrated circuits into their correct holders ensuring that pin 1 marked on the board aligns with pin 1 of the IC. Carefully fit the clip-on heatsink to REG2.

Use the stick-on front panel as a template to mark out the front plate of the box, before drilling and cutting out, see Figure 11. Remove the protective backing from the front panel and carefully position it on the prepared front plate, pressing down evenly all over, making sure there are no air bubbles trapped underneath. Mount all controls and switches on the front panel. Referring to the wiring diagram Figure 9, connect all level controls, toggle and rotary switches, LED's and the meter to their appropriate Minicon housings via the ribbon cable provided, allowing approximately 5 inches of cable from each housing to the front panel. Note that the Minicon housings will have their lugs towards the rear of the circuit board when installed. (Refer to the Receiver article for details of how to make terminations to the Minicon connectors, Maplin Magazine Issue 18.)

Mount the toroidal transformer with the rubber washers provided on either side and place a solder tag under the fixing screw, the PSU circuit is shown in Figure 10. Insert the rubber grommet into the hole in the transformer bracket and pass the red, blue, grey, and yellow wires from the transformer through the grommet. Referring to Figure 11, mark and drill the base plate and mount the transformer bracket, placing the mains label in a visible position on this bracket. You can make your own bracket if you wish according to the dimensions shown in Figure 12. Drill and cut out the rear plate of the box and mount the fuseholder. (Check that when the case is finally assembled, the fuseholder tags will be clear of any obstructions.)

Pass the mains cable through the strain relief grommet and then through its hole in the rear plate and secure grommet in position, then refering to Figure 9, connect the brown wire via the fuseholder to the mains switch. The blue wire connects straight to the mains switch and the green/yellow wire to the earth tag under the transformer mounting screw. Terminate the two orange primary wires from the transformer at the

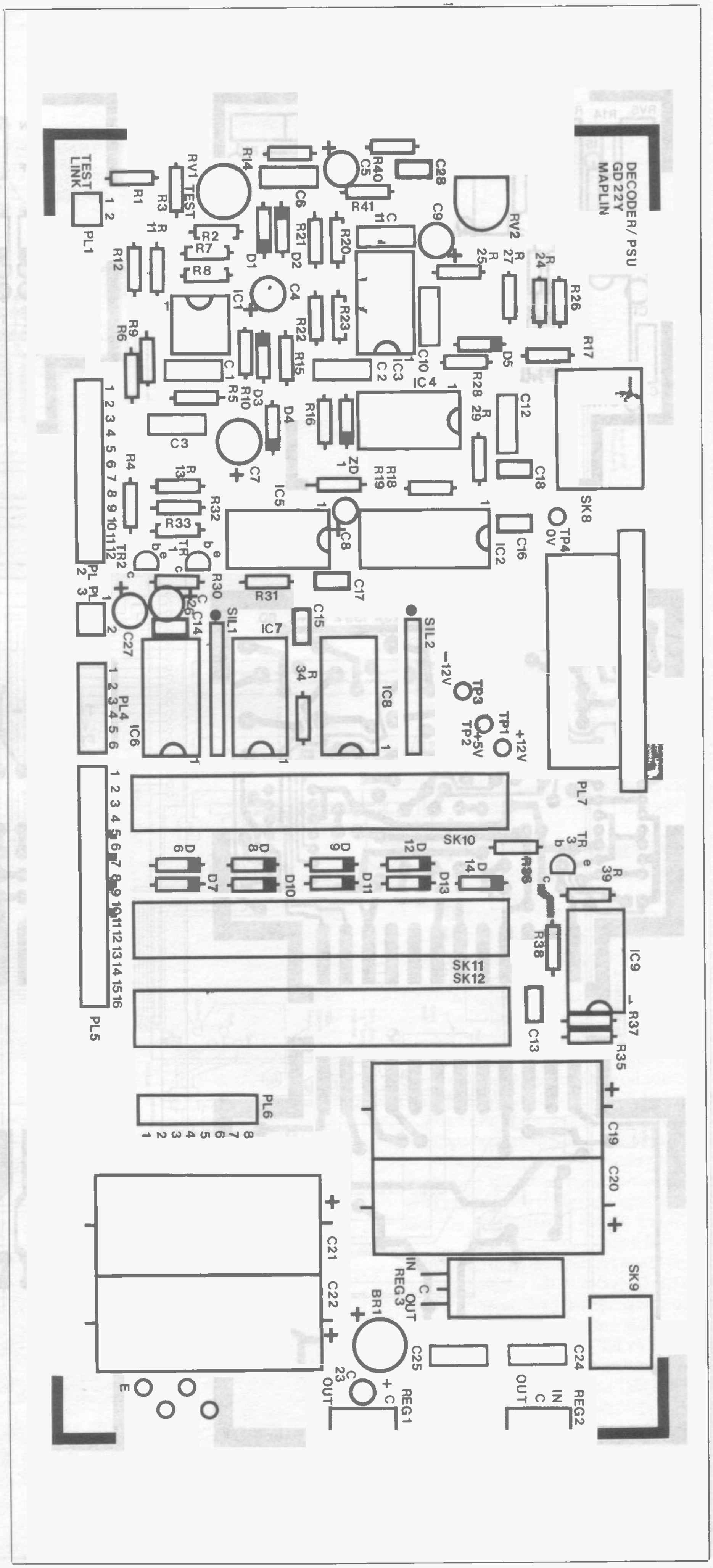


Figure 6. Decoder PCB Overlay.

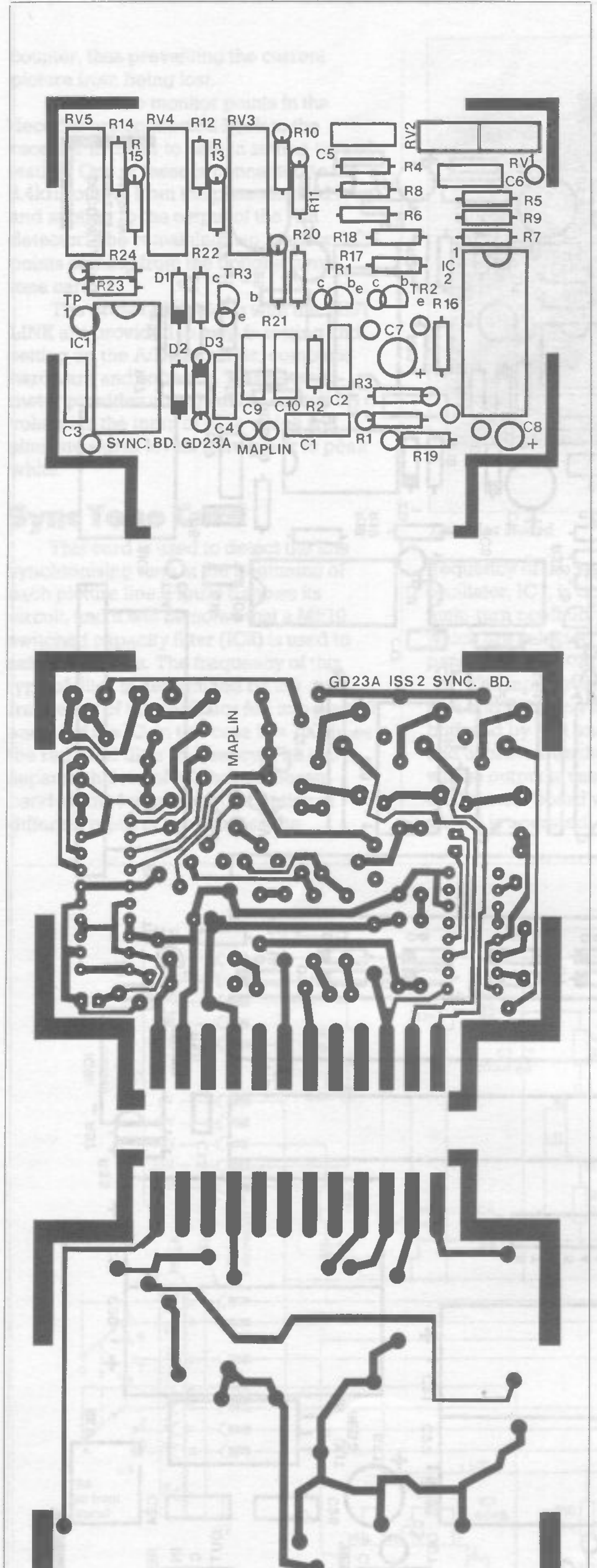


Figure 7. Sync Tone Tracks and Overlay.

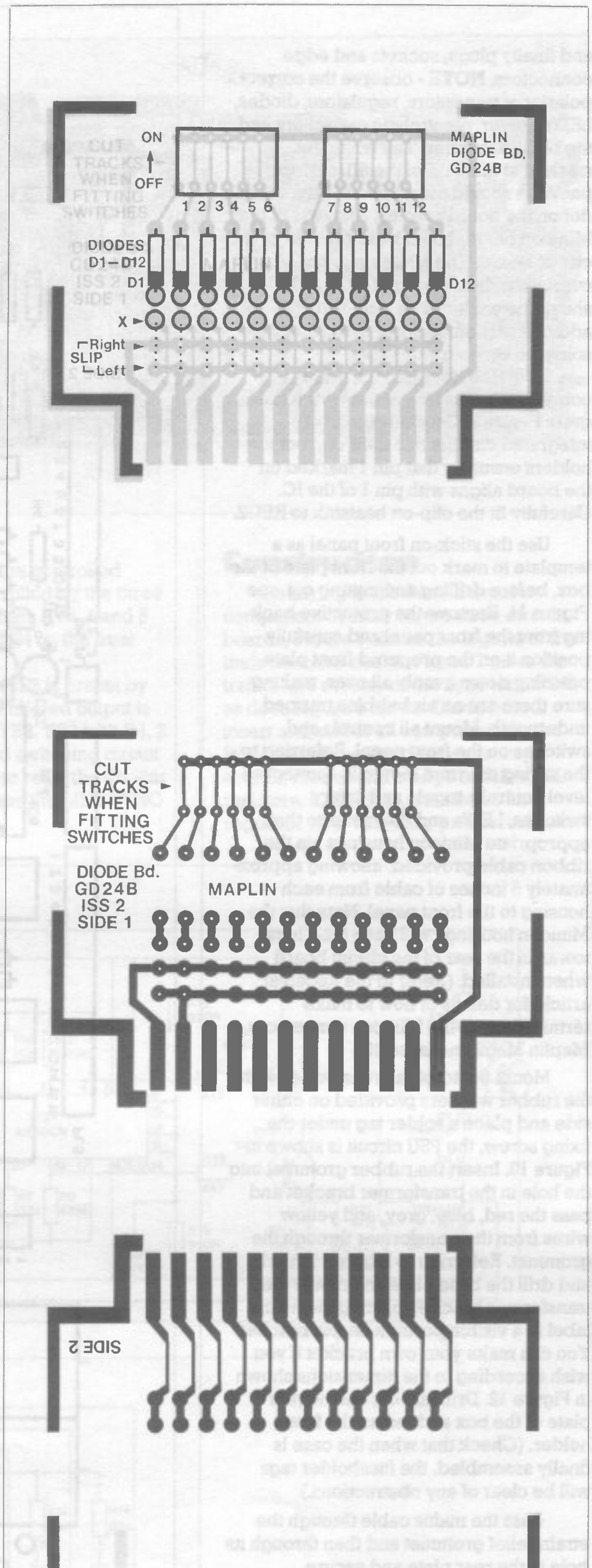


Figure 8. Diode Board Tracks and Overlay.

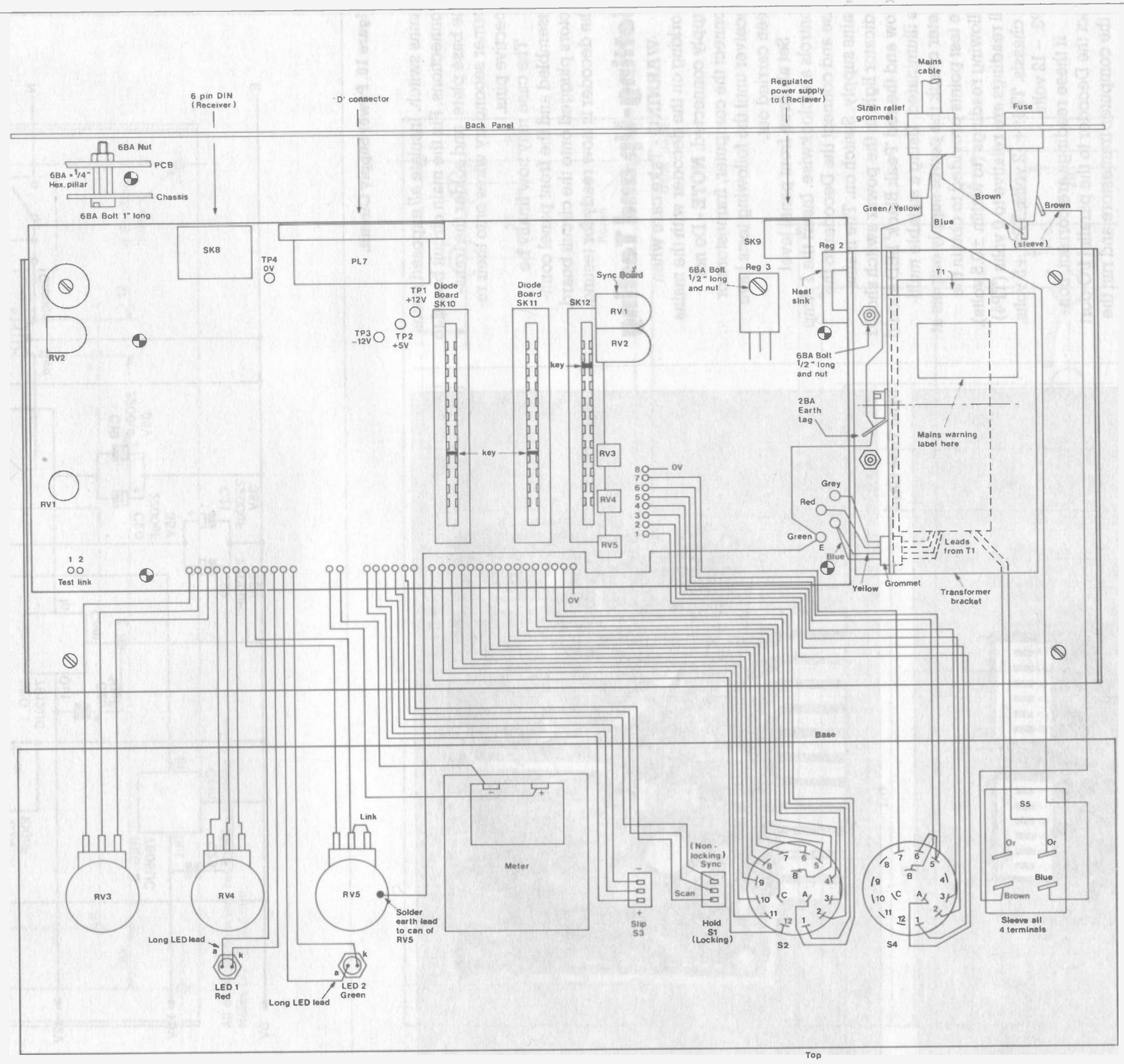


Figure 9. Wiring Diagram.

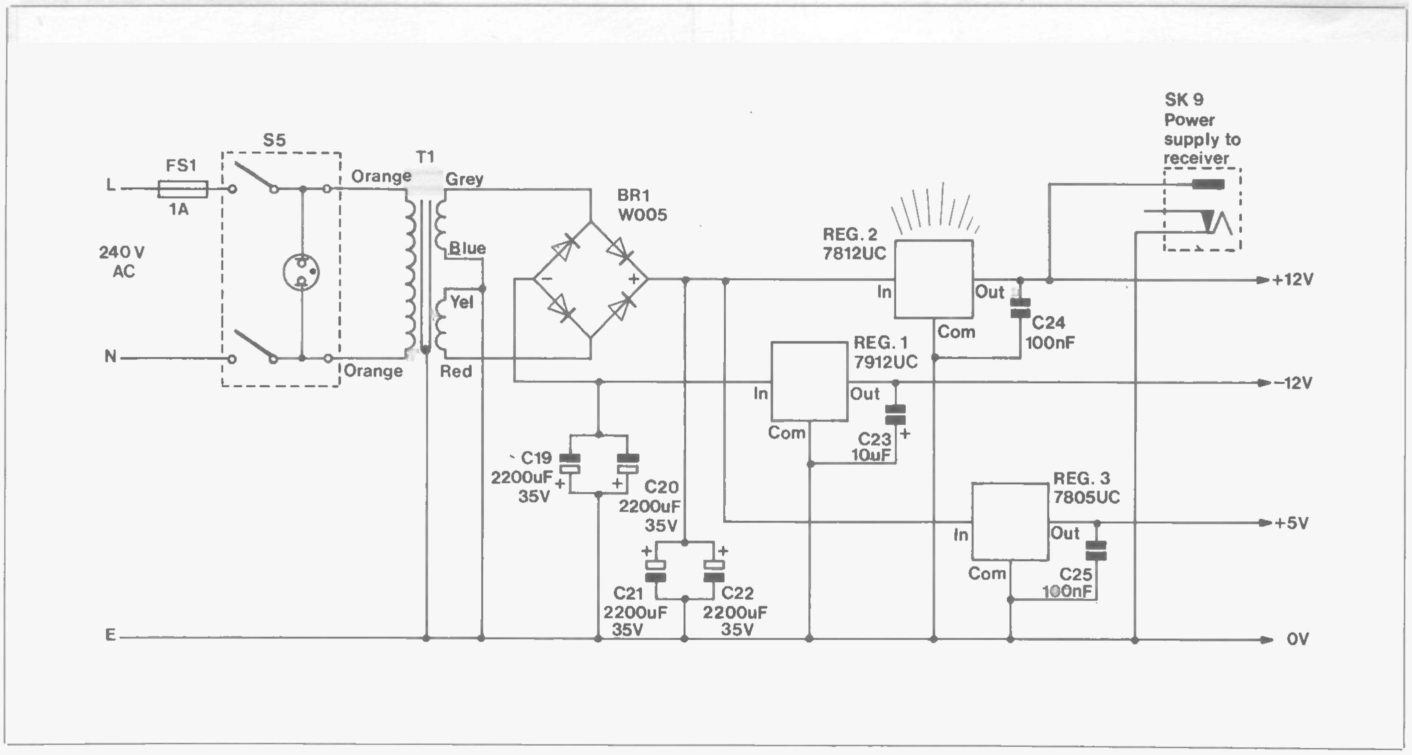


Figure 10. Power Supply Circuit.

mains switch. Insulate *all* exposed mains connections. Fix the main circuit board to the base plate, and solder the transformer secondary wires onto their respective pins.

The case may now finally be assembled and the front panel connectors plugged onto the circuit board. The decoder is now ready for testing.

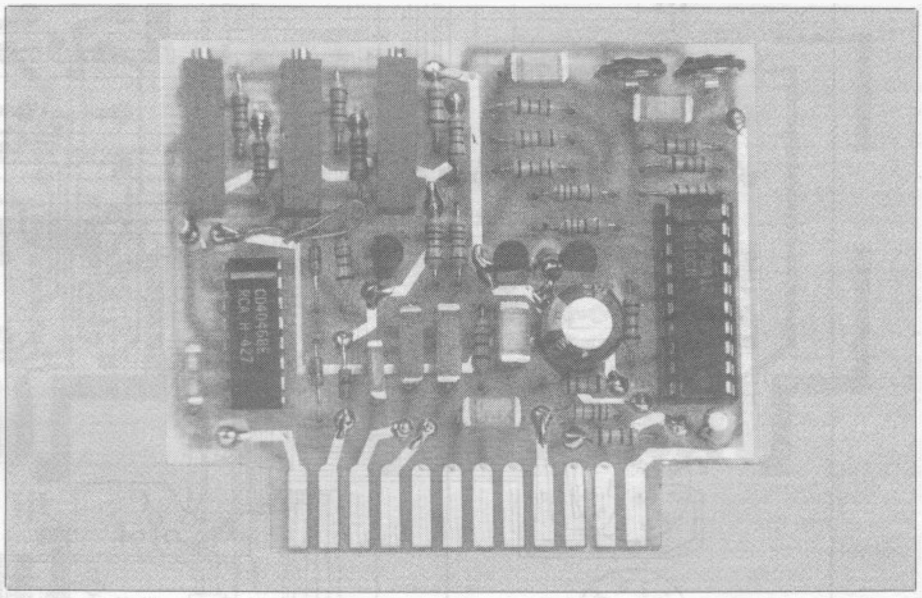
Setting-Up and Testing

WARNING - Take care when working on the decoder with the mains supply connected. **NOTE** - Do *not* connect the computer, framestore or receiver until the following tests have been carried out.

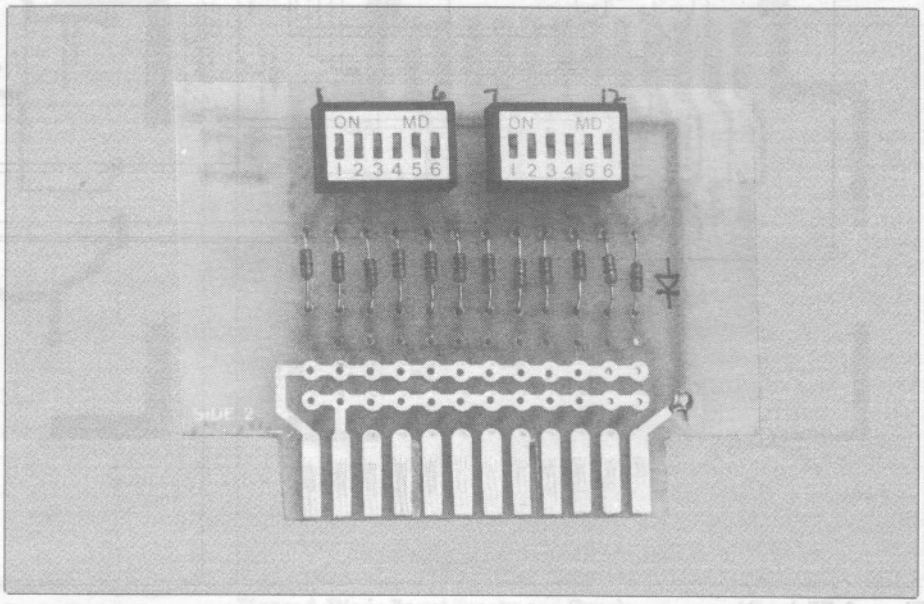
Set all three front panel level controls anticlockwise. Insert the 1 Amp fuse and connect the Decoder to the mains supply. Switch on. The mains indicator light in the power switch should glow and the red 'Peak Black' LED should be illuminated. Using a suitable multimeter check the power supply outputs at the test points provided to obtain the following readings (to within ±0.5 volts). All readings are relative to 0 volts (TP4) or chassis. TP1: +12 volts, TP2: +5 volts, TP3: −12 volts.

If these readings are correct, connect the Decoder to the parallel I/O port of the computer/framestore and run the appropriate software. (When using the Amstrad or BBC software provided in this article, set the horizontal resolution to 4.) Set the TEST preset (RV1) fully clockwise and the sync switch to SCAN. The lines per second switch should be set to 2. Join the two TEST LINK pins (PL1) together and note that the 'Black Peak' LED remains alight.

Slowly rotate the TEST preset anticlockwise whilst observing the monitor screen. The brightness of the scan lines moving up the screen should be seen to



Sync Tone Card



Diode Board

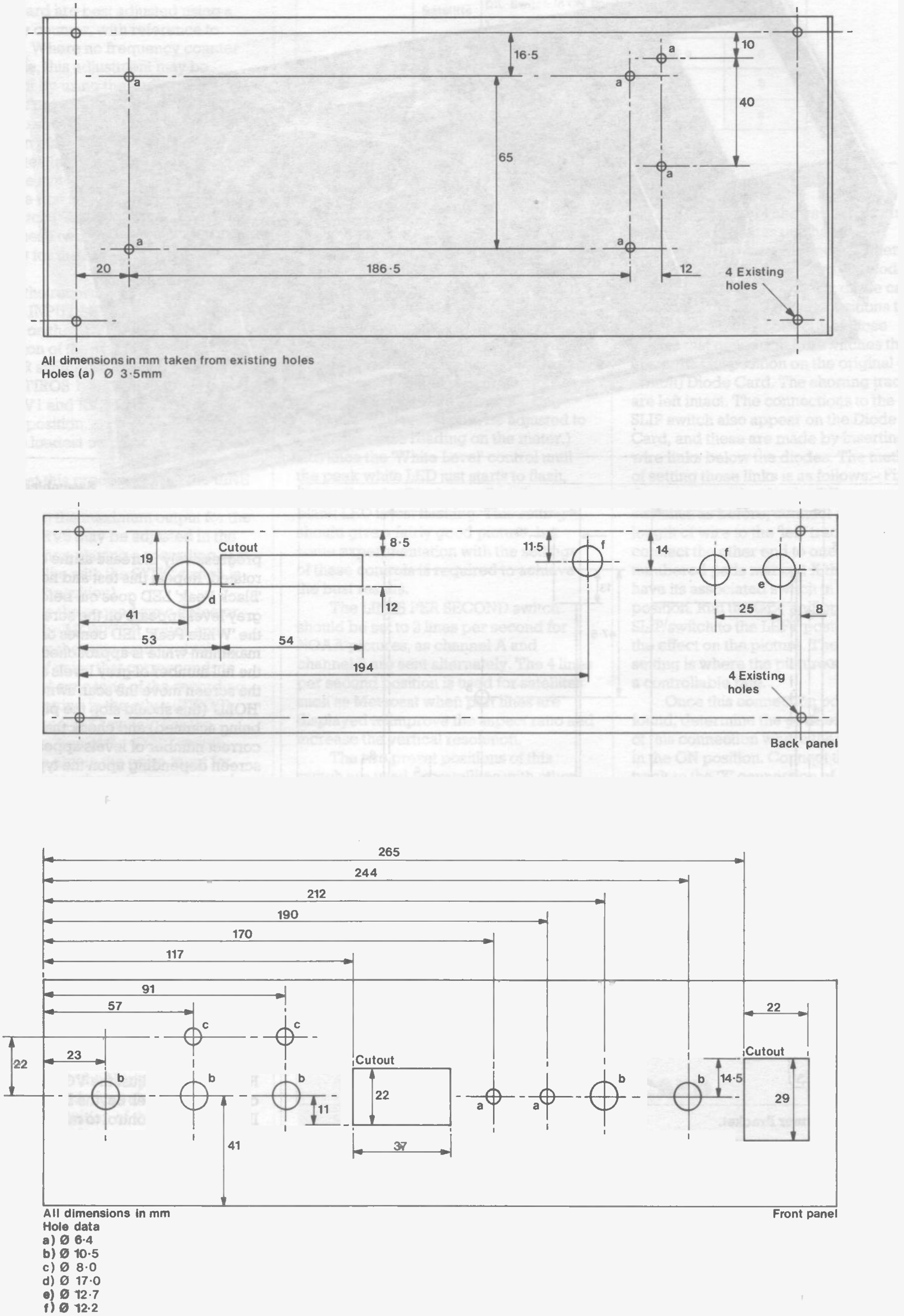
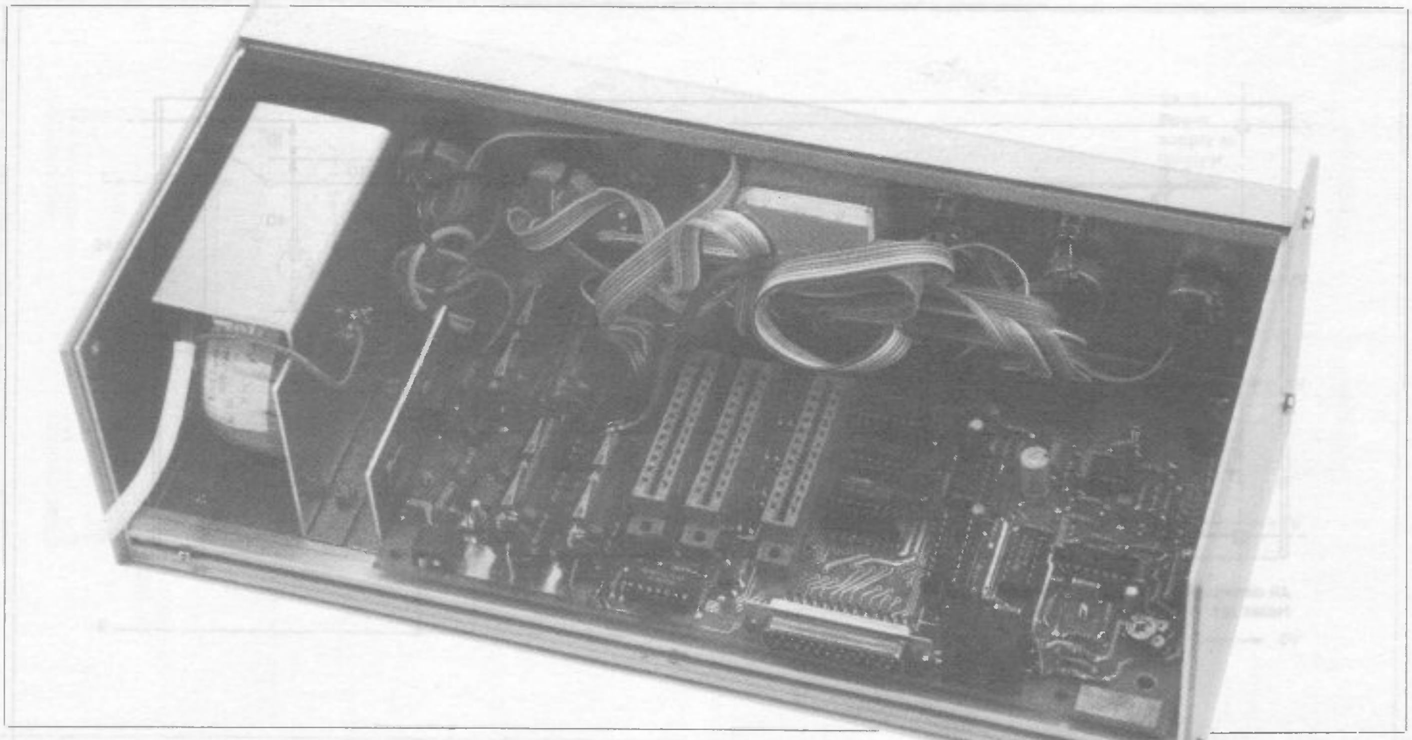


Figure 11. Case Cut-out Details.



Assembled Decoder

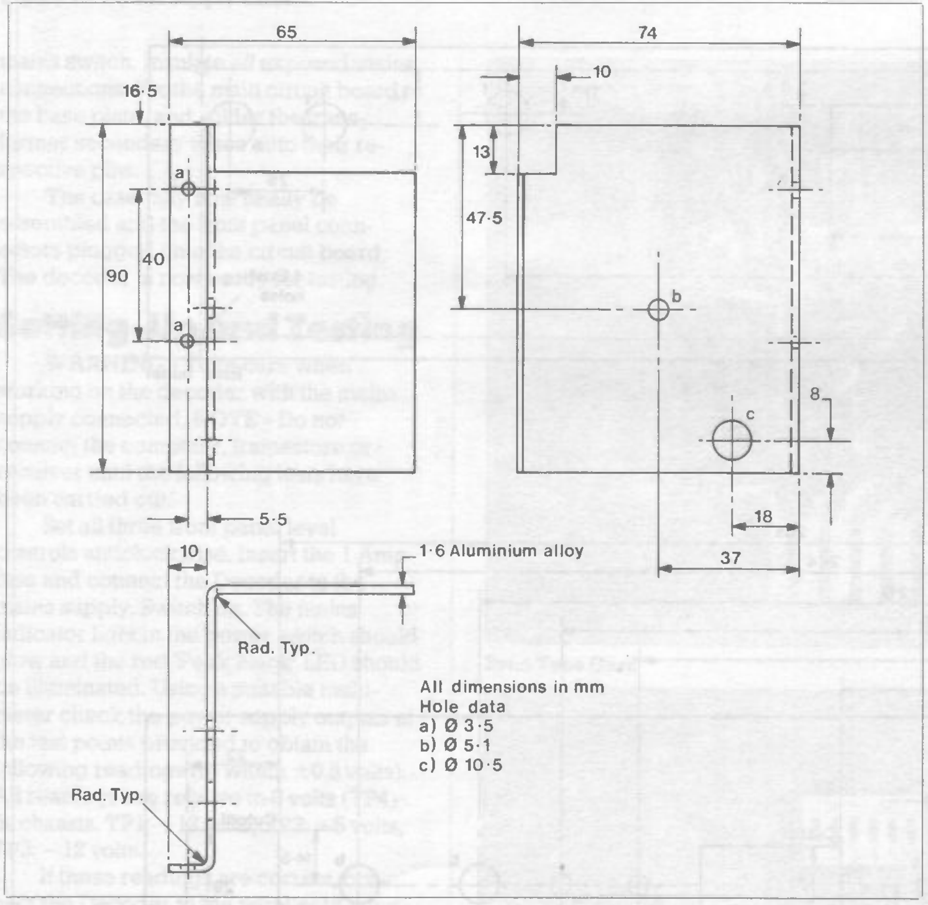


Figure 12. Transformer Bracket.

Sync Tone Switch Position	Frequency of Tone	Frequency at TP1 of Sync Tone Card
TIROS 1 (Channel A)	1040Hz	104 kHz
TIROS 2 (Channel B)	832Hz	83·2 kHz
METEOR	300Hz	30 kHz

Figure 13. Sync Card Frequency Settings.

progressively increase as the control is rotated. Repeat this test and note that the 'Black Peak' LED goes out before the first grey level appears on the screen and that the 'White Peak' LED comes on as the maximum white is approached. When the full number of grey levels appear on the screen move the scan switch to 'HOLD' (this should stop the picture being scanned) and check that the correct number of levels appear on the screen depending upon the type of display system in use. (The Amstrad and the framestore should produce 16 levels including black and white, and the BBC 8 levels including black and white). The 'TEST' link pins may now be disconnected.

The following tests should be carried out by using a good quality recording of the NOAA 6 or NOAA 9 satellites. Connect the Decoder to the Receiver via the 6-way audio DIN lead and the power lead. Connect the tape recorder to the Receiver, referring to the previous article (Issue 18). Play the recording of the satellite. Select TAPE OUT on the MONITOR switch of the Receiver and adjust the VOLUME to a comfortable level. Set the Decoder INPUT LEVEL control to minimum. Switch between TAPE OUT and PLL on the MONITOR switch, and adjust the preset RV2 on the Decoder board until the tone from the PLL is the same as that of the satellite's subcarrier.

To check this setting, the INPUT LEVEL may now be increased and the 'Black Level' LED should now flash or go out. Check that the LEVEL meter responds as the INPUT LEVEL control is increased.

The basic Decoder is now ready for use but if the sync tone card has been installed the following setting-up is

Satellite	DIL Switch in ON Position 1	2	3	4	5	6	7	8	9	10	11	12	Slip Switch Connections Left	Right
# 1	√		√	√		√						√	9	8
# 2	√		√	√					√	√	√		8	6
# 3	√		√	√		√							9	8

Figure 14. Settings for Russian Satellites.

required. The three multi-turn presets on the tone card are best adjusted using a frequency counter, with reference to Figure 13. Where no frequency counter is available, this adjustment may be carried out by using the audio monitor test points provided in the Receiver unit in the following manner.

When playing a recording of the NOAA satellites, the characteristic 'clip-clop' of the synchronising tones will be noted. The first two positions of the LINE SYNC switch ('TIROS') select one or other of these two tones, the third position is for the Russian Meteor satellites.

Play the recording as before and adjust the INPUT LEVEL to give about half scale on the LEVEL meter. Select the first position of the sync detector on the MONITOR switch. Switch the LINE SYNC switch to TIROS 1, and set the two presets RV1 and RV2 on the sync card to their mid-position, and adjust RV3 to obtain the loudest output for the *higher* tone.

Repeat this procedure with the LINE SYNC switch set to TIROS 2, and adjust RV4 to obtain the maximum output for the *lower* tone (RV5 may be adjusted in the same way when playing a recording of a Meteor satellite with the SYNC switch in the METEOR position).

Switch to the second sync detector position on the MONITOR switch and adjust RV2 on the sync card to obtain a short burst of noise that corresponds to every second sync tone of the recording. Check this setting in the other (TIROS) position of the SYNC switch. For the METEOR position of the SYNC switch, adjust RV1 to obtain the noise burst for every sync tone when playing a recording of the satellite.

Decoder in Use

The following information refers to the use of the decoder with the BBC B and Amstrad computers. (Information for using the Frame Store will be published later).

Program 1 is for the BBC model B, Program 2 is the machine code created by the GENA 3 assembly program from Amsoft. From Program 2 you can create your object file which can then be loaded by Program 3. When loaded and run, these will ask for the Horizontal Resolution to be entered; this value determines not only the definition of the displayed picture, but also the proportion of the total picture width displayed across the screen. The first time a recording is run, select full width (4), and then any interesting parts may be re-run with a lower setting to obtain greater detail. The SHIFT switch may be used to move the picture to the desired position at the beginning of the run, and if required, the full scan may be re-started by holding the space bar. (The sync when set is not lost until the tape is stopped or the signal fails.) Synchronisation to the start of a line is provided by the Sync Tone Card. The LINE SYNC switch selects the type of satellite and channel to be synchronised. With the recording running and the appropriate position of the LINE SYNC switch set, synchronisation is achieved by a short operation of the non-locking SYNC toggle switch.

The INPUT LEVEL control should be set to give an average reading of about half scale on the LEVEL meter. (Note that if a known peak white signal is being received, the level should be adjusted to give a full scale reading on the meter.) Advance the 'White Level' control until the peak white LED just starts to flash, then adjust the 'Black Level' until the black LED is just flashing. This setting should give a fairly good picture, but some experimentation with the settings of these controls is required to achieve the best results.

The LINES PER SECOND switch should be set to 2 lines per second for NOAA pictures, as channel A and channel B are sent alternately. The 4 lines per second position is used for satellites such as Meteosat when part lines are displayed to improve the aspect ratio and increase the vertical resolution.

The two preset positions of this switch are used for satellites with other line rates, and are programmed by using the diode cards. The Diode Card may either be fitted with DIL switches, or with diodes in a pre-selected matrix. When the DIL switches are fitted, cut the shorting tracks under the switches, and fit all diodes. The correct setting for a satellite is found by switching the LINES PER SECOND switch to the A position, inserting a diode card, with DIL switches installed, in position (nearest to the sync card) and trying different settings of the switches until a synchronised picture is obtained. Figure 14 shows some settings for Russian satellites that have been found to synchronise correctly. When the setting has been determined, the code may be 'copied' onto a blank diode card by inserting diodes *only* in positions that correspond to the positions of those diodes that connect to the switches that are in the ON position on the original (DIL switch) Diode Card. The shorting tracks are left intact. The connections to the SLIP switch also appear on the Diode Card, and these are made by inserting wire links below the diodes. The method of setting these links is as follows:– Find the correct setting for the DIL switches as before, connect a short length of wire to the 'left' track and connect the other end to one of higher numbered pads marked X that does not have its associated switch in the ON (up) position. Run the tape and operate the SLIP switch to the LEFT position and note the effect on the picture. The correct setting is where the picture moves left at a controllable rate.

Once this connection point has been found, determine the position to the left of this connection where there is a switch in the ON position. Connect the RIGHT track to the 'X' connection of this position, and turn the switch OFF. Try running the recording again and check that when the SLIP switch is held in the RIGHT position, the picture moves to the right at a comfortable rate.

When the correct positions for the two connections have been found, permanent wire links may be fitted.

The picture scanning may be stopped at any time by using the HOLD switch. (This does not lose synchronisation if the incoming signal is uninterrupted.)

DECODER DIODE BOARD PARTS LIST

SEMICONDUCTORS			
D1-12	1N4148	12	(QL80B)
MISCELLANEOUS			
S1,2	DIL Switch SPST 6-Way	2	(FV44X)
	Diode PCB	1	(GD24B)

A complete kit of all parts is available for this project:
Order As LM09K (Decoder Diode Board Kit)
The following item in the above kit list is also available separately, but is not shown in the 1986 catalogue:
Decoder Diode PCB **Order As GD24B**

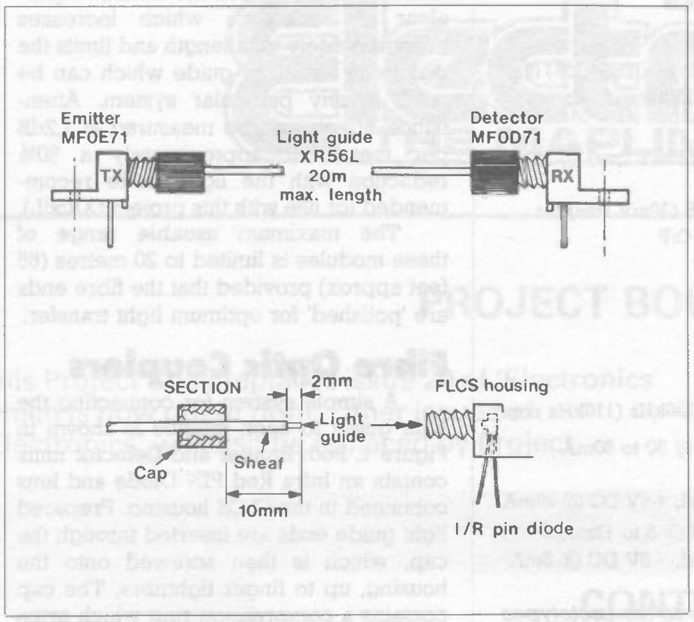


Figure 1. Connecting Light Guide.

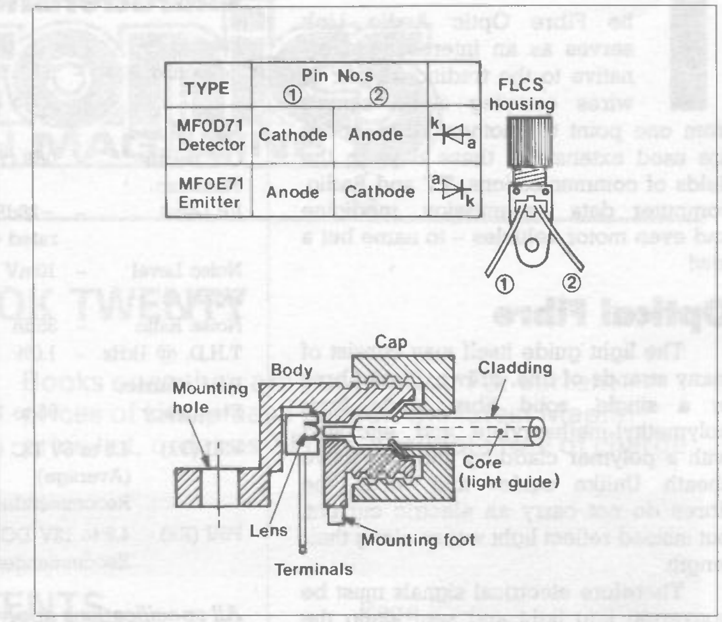


Figure 2. Emitter and Detector Pin-out and Construction.

Preparation of Light Guide

Both FLCS couplers are designed for use with 1000 micron (1mm) core plastic fibre, which can be found in our catalogue or parts list (XR56L). Remove a short piece of sleeving from one end of the light guide, as shown in Figure 3, by gently cutting around the circumference, or by using 18 gauge wire strippers. Great care should be taken when cutting through the covering sheath, to prevent scoring the fibre core inside!

Remove the end covering and cleanly cut the fibre core two millimetres long. Try to make a single, straight cut thus keeping the end as smooth as possible, this being important for maximum light transfer to the couplers. Use a sharp knife for this. Very fine emery paper, or the striking edge of a matchbox (but not glasspaper types!) can be gently rubbed, *squarely* across the cut fibre end to polish the surface. Liquid metal polish also helps to develop a smooth finish and could also be used to finish off.

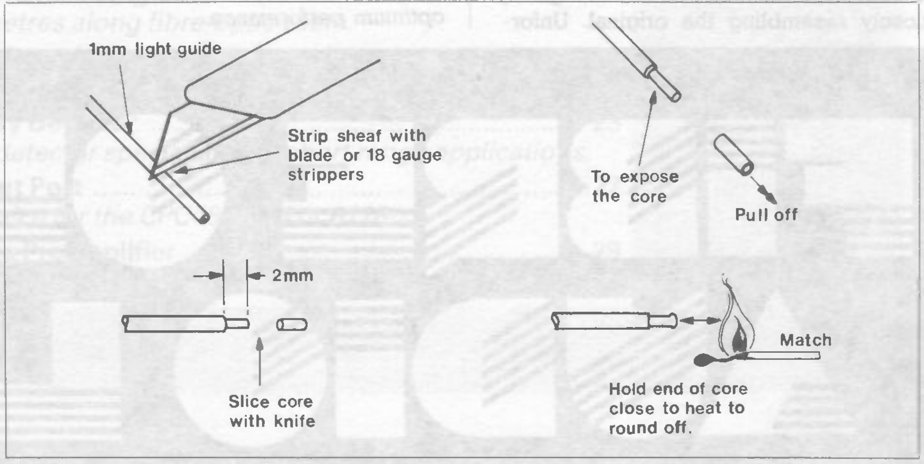


Figure 3. Preparing the Light Guide.

Alternatively, the cut fibre end could be placed close to a naked flame for a few seconds until the end begins to round off. Excessive heat will melt the fibre completely, and this should be avoided. This latter method has the advantage of producing a near perfect finish and develops a 'lens' in the fibre – ideal for good light transfer. Whichever method is employed, aim for a mirror-like finish on the fibre end if maximum range is required.

Circuit Description

The system has been developed for use with audio signals of a reasonably

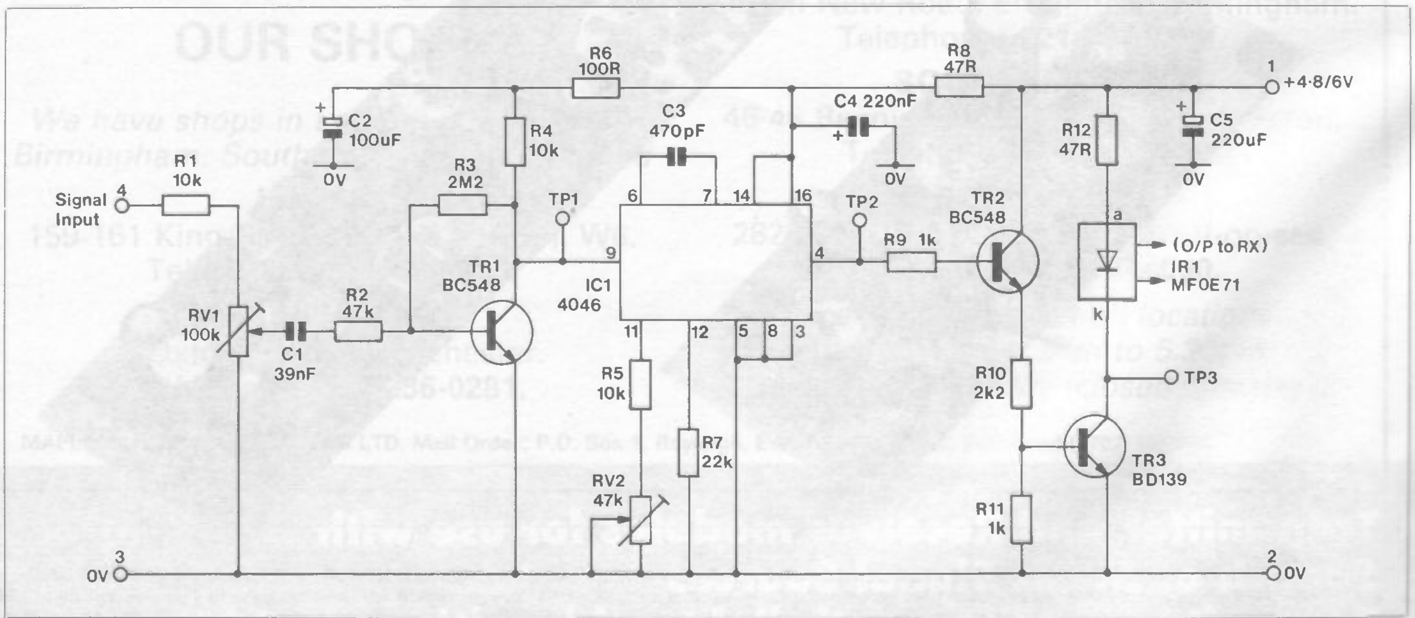


Figure 4. Transmitter Circuit.

Program 1.

```
10 MODE 7
20 CLS:PRINT:PRINT
30 PRINT"INPUT HORIZONTAL RESOLUTION (1-4)";
40 INPUT HRES
50 MODE 2
60 VDU 23;8202;0;0;0
70 PRINT
80 DIM CODE% 500
90 ROWBSE=&70
100 ?ROWBSE=((HIMEM+20479) MOD 256)
110 ?(ROWBSE+1)=((HIMEM+20479) DIV 256)
120 DOTBSE=&72
130 ?DOTBSE=((HIMEM+20479)MOD 256)
140 ?(DOTBSE+1)=((HIMEM+20479)DIV 256)
150 SMPL=&74
160 TEMP=&75
170 RWBSSH=&76
180 FINSCN=&78
190 OVBRT=&7A
200 ?FINSCN=((HIMEM)MOD 256)
210 ?(FINSCN+1)=((HIMEM)DIV 256)
220 PORT=&FE60
230 FOR P=0TO2 STEP 2
240 P%=CODE%
250 [OPT P
260 LDA #&02
270 LDX #&00
280 JSR &FFF4
290 .INIT LDA #&00
300 LDX #&00
310 LDY #&00
320 SEI
330 CLD
340 STA &FE62
350 STA SMPL
360 STA TEMP
370 .WTSYNC
380 LDA PORT
390 AND #64
400 BEQ WTSYNC
410 .FINSYNC
420 LDA PORT
430 AND #64
440 BNE FINSYNC
450 .WASTE BIT PORT
460 BMI WASTE
470 .PING BIT PORT
480 BPL PING
490 INX
500 CPX#01
510 BNE WASTE
520 LDX #&00
530 .WTBUSY
540  BIT PORT
550 BMI WTBUSY
560 .WTSMPL
570 BIT PORT
580 BPL WTSMPL
590 INX
600 .RESH CPX #&02
610 BNE WTBUSY
620 LDA PORT
630 AND #&0F
640 LDX #&00
650 STX TEMP
660 LSR A
670 ROL TEMP
680 ROL TEMP
690 ROL A
700 ROL A
710 ROL A
720 ROL A
730 ROL A
740 ROL A
750 ROL OVBRT
760 ROL A
770 ROL TEMP
780 ROL TEMP
790 ROL A
800 ROL TEMP
810 LSR OVBRT
820 BCC TEST
830 LDA#21
840 STA TEMP
850 .TEST  LDA SMPL
860 LSR A
870 BCC ODD
880 ASL TEMP
890 LDA TEMP
900 ORA (DOTBSE,X)
910 STA (DOTBSE,X)
920 JMP NEWDOT
930 .ODD
940 LDA TEMP
950 STA (DOTBSE,X)
960 .NEWDOT
970 LSR SMPL
980 BCS UNE
990 INC SMPL
1000 JMP WTBUSY
1010 .UNE
1020 LDA DOTBSE
1030 SEC
1040 SBC #&08
1050 BCS TWO
1060 DEC DOTBSE+1
1070 .TWO
1080 STA DOTBSE
1090 LDA ROWBSE+1
1100 STA RWBSSH+1
1110 LDA ROWBSE
1120 STA RWBSSH
1130 SEC
1140 SBC #128
1150 BCS THREE
1160 DEC RWBSSH+1
1170 .THREE
1180 STA RWBSSH
1190 DEC RWBSSH+1
1200 DEC RWBSSH+1
1210 LDA DOTBSE+1
1220 CMP RWBSSH+1
1230 BNE WTBUSY
1240 LDA DOTBSE
1250 CMP RWBSSH
1260 BNE WTBUSY
1270 TYA
1280 PHA
1290 TXA
1300 PHA
1310 LDA #&81
1320 LDX #&00
1330 LDY #&00
1340 JSR &FFF4
1350 TYA
1360 BNE NEWLNE
1370 PLA:PLA:JMP EIGHT
1380 .NEWLNE PLA
1390 TAX
1400 PLA
1410 TAY
1420 LDA ROWBSE
1430 SEC
1440 SBC #&01
1450 INY
1460 BCS FOUR
1470 DEC ROWBSE+1
1480 .FOUR
1490 STA ROWBSE
1500 STA DOTBSE
1510 LDA ROWBSE+1
1520 STA DOTBSE+1
1530 CPY #&08
1540 BEQ SIX
1550 JMP WTSYNC
1560 .SIX
1570 LDA ROWBSE
1580 LDY #&00
1590 SEC
1600 SBC# 120
1610 BCS FIVE
1620 DEC ROWBSE+1
1630 DEC DOTBSE+1
1640 .FIVE
1650 STA ROWBSE
1660 STA DOTBSE
1670 DEC ROWBSE+1
1680 DEC ROWBSE+1
1690 DEC DOTBSE+1
1700 DEC DOTBSE+1
1710 STY SMPL
1720 LDA ROWBSE+1
1730 CMP FINSCN+1
1740 BEQ SEVEN
1750 BCC SEVEN
1760 JMP WTSYNC
1770 .SEVEN
1780 JMP EIGHT
1790 LDA ROWBSE
1800 CMP FINSCN
1810 BEQ EIGHT
1820 BCC EIGHT
1830 JMP WTSYNC
1840 .EIGHT
1850 CLI
1860 RTS
1870 ]
1880 NEXT P
1890 IF HRES>0 AND HRES<5 THEN ?(RESH+1)=HRES
1900 CALL CODE%
1910 GOTO 90
```

Program 2.

```
Hisoft GENA3.1 Assembler.

A028              10         ORG  41000
A028              20         ENT  $
F8F0              30 PORT:   EQU  #F8F0
9C40              40 TEMP:   EQU  40000
9C41              50 LUM:    EQU  40001
9C42              60 XREG:   EQU  40002
9C44              70 YREG:   EQU  40004
9C46              80 HXREG:  EQU  40006
9C48              90 BLKADD: EQU  40008
A028  3E00       100         LD   A,#00
A02A  32479C     110         LD   (HXREG+1),A
A02D  CD0EBC     120         CALL #BC0E
A030  219F00     130 RERUN:  LD   HL,159
A033  22429C     140         LD   (XREG),HL
A036  21C700     150         LD   HL,199
A039  22449C     160         LD   (YREG),HL
A03C  DD2142A1   170         LD   IX,BYTEAD+15
A040  3E0F       180         LD   A,#0F
A042  32409C     190         LD   (TEMP),A
A045  DD7E00     200 COLSET: LD   A,(IX+0)
A048  47         210         LD   B,A
A049  4F         220         LD   C,A
A04A  3A409C     230         LD   A,(TEMP)
A04D  CD32BC     240         CALL #BC32
A050  21409C     250         LD   HL,TEMP
A053  35         260         DEC  (HL)
A054  FA5CA0     270         JP   M,WTFRM
A057  DD2B       280         DEC  IX
A059  C345A0     290         JP   COLSET
A05C  CD19BD     300 WTFRM:  CALL #BD19
A05F  CD19BD     310         CALL #BD19
A062  F3         320 LOOP1:  DI
A063  01F0F8     330         LD   BC,#F8F0
A066  ED78       340 LINE:   IN   A,(C)
A068  CB77       350         BIT  6,A
A06A  28FA       360         JR   Z,LINE
A06C  ED78       370 ENLIN:  IN   A,(C)
A06E  CB77       380         BIT  6,A
A070  20FA       390         JR   NZ,ENLIN
A072  160A       400         LD   D,10
A074  15         410 DELAY:  DEC  D
A075  20FD       420         JR   NZ,DELAY
A077  F3         430 LOOP2:  DI
A078  1602       440         LD   D,2
A07A  01F0F8     450         LD   BC,#F8F0
A07D  ED78       460 SMPL:   IN   A,(C)
A07F  CB7F       470         BIT  7,A
A081  20FA       480         JR   NZ,SMPL
A083  ED78       490 ENSMP:  IN   A,(C)
A085  CB7F       500         BIT  7,A
A087  28FA       510         JR   Z,ENSMP
A089  15         520         DEC  D
A08A  20F1       530         JR   NZ,SMPL
A08C             540 GETLUM:
A08C  ED78       550         IN   A,(C)
A08E  E60F       560         AND  #0F
A090  32419C     570         LD   (LUM),A
A093  1F         580         RRA
A094  CB18       590         RR   B
A096  1F         600         RRA
A097  CB18       610         RR   B
A099  1F         620         RRA
A09A  CB19       630         RR   C
A09C  1F         640         RRA
A09D  CB18       650         RR   B
A09F  1600       660         LD   D,0
A0A1  CB00       670         RLC  B
A0A3  CB1A       680         RR   D
A0A5  CB1A       690         RR   D
A0A7  CB00       700         RLC  B
A0A9  CB1A       710         RR   D
A0AB  CB1A       720         RR   D
A0AD  CB01       730         RLC  C
A0AF  CB1A       740         RR   D
A0B1  CB1A       750         RR   D
A0B3  CB00       760         RLC  B
A0B5  CB1A       770         RR   D
A0B7  3A429C     780         LD   A,(XREG)
A0BA  1F         790         RRA
A0BB  3003       800         JR   NC,NOLFT
A0BD  B7         810         OR   A
A0BE  CB1A       820         RR   D
A0C0  32469C     830 NOLFT:  LD   (HXREG),A
A0C3  7A         840         LD   A,D
A0C4  32409C     850         LD   (TEMP),A
A0C7  210050     860         LD   HL,#5000
A0CA  3A449C     870         LD   A,(YREG)
A0CD  CB3F       880         SRL  A
A0CF  CB3F       890         SRL  A
A0D1  CB3F       900         SRL  A
A0D3  5F         910         LD   E,A
A0D4  1600       920         LD   D,0
A0D6  0608       930         LD   B,8
A0D8  29         940 MULT:   ADD  HL,HL
A0D9  3001       950         JR   NC,NOADD
A0DB  19         960         ADD  HL,DE
A0DC  10FA       970 NOADD:  DJNZ MULT
A0DE  22489C     980         LD   (BLKADD),HL
A0E1  3A449C     990         LD   A,(YREG)
A0E4  CB27      1000         SLA  A
A0E6  CB27      1010         SLA  A
A0E8  CB27      1020         SLA  A
A0EA  E638      1030         AND  56
A0EC  67        1040         LD   H,A
A0ED  2E00      1050         LD   L,0
A0EF  ED4B489C  1060         LD   BC,(BLKADD)
A0F3  09        1070         ADD  HL,BC
A0F4  0100C0    1080         LD   BC,#C000
A0F7  09        1090         ADD  HL,BC
A0F8  ED4B469C  1100         LD   BC,(HXREG)
A0FC  09        1110         ADD  HL,BC
A0FD  3A409C    1120         LD   A,(TEMP)
A100  DD21429C  1130         LD   IX,XREG
A104  DDCB0046  1140         BIT  0,(IX+0)
A108  2001      1150         JR   NZ,PLOT
A10A  B6        1160         OR   (HL)
A10B  77        1170 PLOT:   LD   (HL),A
A10C  010100    1180         LD   BC,#0001
A10F  2A429C    1190         LD   HL,(XREG)
A112  B7        1200         OR   A
A113  ED42      1210         SBC  HL,BC
A115  3806      1220         JR   C,NEXY
A117  22429C    1230         LD   (XREG),HL
A11A  C377A0    1240         JP   LOOP2
A11D  219F00    1250 NEXY:   LD   HL,159
A120  22429C    1260         LD   (XREG),HL
A123  2A449C    1270         LD   HL,(YREG)
A126  B7        1280         OR   A
A127  ED42      1290         SBC  HL,BC
A129  3002      1300         JR   NC,NEWLIN
A12B  FB        1310         EI
A12C  C9        1320         RET
A12D  22449C    1330 NEWLIN: LD   (YREG),HL
A130  C362A0    1340         JP   LOOP1
A133            1350 BYTEAD:
A133  00010204  1360         DEFB 0,1,2,4
A137  0506080A  1370         DEFB 5,6,8,10
A13B  0C0E1012  1380         DEFB 12,14,16,18
A13F  14161B1A  1390         DEFB 20,22,24,26

BLKADD 9C48   BYTEAD A133   COLSET A045
DELAY  A074   ENLIN  A06C   ENSMP  A083
GETLUM A08C   HXREG  9C46   LINE   A066
LOOP1  A062   LOOP2  A077   LUM    9C41
MULT   A0D8   NEWLIN A12D   NEXY   A11D
NOADD  A0DC   NOLFT  A0C0   PLOT   A10B
PORT   F8F0   RERUN  A030   SMPL   A07D
TEMP   9C40   WTFRM  A05C   XREG   9C42
YREG   9C44

Table used:    307  from   350
Executes: 41000
```

Program 3.

```
5 MEMORY 30000:MODE 2
10 LOAD"wefax1.obj"
20 INPUT"enter horizontal resolution 1-4";resh
30 IF resh>0 AND resh<5 THEN POKE &A079,
resh ELSE CLS:GOTO 20
40 CALL 41000
50 CALL &A030
60 GOTO 50
```

SATELLITE DECODER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1	27k	1	(M27K)
R2,4,25	470k	3	(M470K)
R3,37,38,39,40	1k	5	(M1K)
R5,9,20,27	10k	4	(M10K)
R6,7,12,24	100k	4	(M100K)
R8	820Ω	1	(M820R)
R10	220k	1	(M220K)
R11,17,26	2k2	3	(M2K2)
R13	180k	1	(M180K)
R14,41	47k	2	(M47K)
R15	5k6	1	(M5K6)
R16,21,22,23,28, 30,31,34,35,36	4k7	10	(M4K7)
R18	180k	1	(M180K)
R19	390Ω	1	(M390R)
R29	330Ω	1	(M330R)
R32,33	270Ω	2	(M270R)
SIL 1,2	SIL 4k7	2	(RA29G)
RV1	10k Cermet	1	(WR42V)
RV2	1k Hor. S-Min Preset	1	(WR55K)
RV3	10k Pot Lin	1	(FW02C)
RV4	1k Pot Lin	1	(FW00A)
RV5	1M Pot Lin	1	(FW08J)

CAPACITORS

C1-3	220nF Poly Layer	3	(WW45Y)
C4,5	10µF 16V Minelect	2	(YY34M)
C6,11	47nF Poly Layer	2	(WW37S)
C7	100µF 25V P.C. Electrolytic	1	(FF11M)
C8,26,27	4µ7F 35V Minelect	3	(YY33L)
C9	2µ2F 63V Minelect	1	(YY32K)
C10	2n2F Poly Layer	1	(WW24B)
C12	4n7F Poly Layer	1	(WW26D)
C13-18,28	100nF Minidisc	7	(YR75S)
C19-22	2200µF 35V Axial Electrolytic	4	(FB90X)
C23	10µF 16V Tantalum	1	(WW68Y)
C24,25	100nF Polyester	2	(BX76H)

SEMICONDUCTORS

D1,2	OA91	2	(QH72P)
D3-14	1N4148	12	(QL80B)
ZD1	BZY88C3V3	1	(QH02C)
LED 1	Red LED Chrome large	1	(YY60Q)
LED 2	Green LED Chrome large	1	(QY47B)
TR1-3	BC548	3	(QB73Q)
BR1	W005	1	(QL37S)
REG1	µA7912UC	1	(WQ93B)
REG2	µA7812UC	1	(QL32K)
REG3	µA7805UC	1	(QL31J)
IC1	LF353	1	(WQ31J)
IC2	ZN427E	1	(UF40T)
IC3	NE565	1	(WQ56L)
IC4	74LS132	1	(YF51F)
IC5	4078	1	(QX26F)
IC6-8	74HC163	3	(UB42V)
IC9	74LS03	1	(YF03D)

MISCELLANEOUS

M1	Signal Meter	1	(LB80B)
T1	Transformer Toroidal 30VA 15V	1	(YK11M)
S1	Switch Sub. Min. Toggle SPDT (C)	1	(FH02C)
S2,4	Switch Rotary 3-pole 4-way	2	(FF75S)
S3	Switch Sub-Min Toggle SPDT (D)	1	(FH03D)
S5	Switch Dual Rocker Neon	1	(YR70M)
FS1	Fuse 1A A/S	1	(WR19V)
PL1,3	Minicon latch Plg 2-Way	2	(RK65V)
PL2	Minicon latch Plg 12-Way	1	(YW14Q)
PL4	Minicon latch Plg 6-Way	1	(YW12N)
PL5,6	Minicon latch Plg 8-Way	3	(YW13P)
PL7	R.A. 'D' Range 25-Way PCB Plg	1	(FG68Y)
SK1,3	Minicon latch Housing 2-Way	2	(HB59P)
SK2	Mincon latch Housing 12-Way	1	(YW24B)
SK4	Minicon latch Housing 6-Way	1	(BH65V)
SK5,6	Minicon latch Housing 8-Way	3	(YW23A)
	Minicon Terminal	46	(YW25C)
SK8	6-Pin PCB DIN Socket	1	(FA90X)
SK9	Power Socket D.C. 2.5mm	1	(FK06G)
SK10-12	2x12-Way P.C. Edgeconn	3	(BK74R)
	Polarising Key 0.156in	3	(FD08J)
	Bolt 6BA x 1in	1 Pkt	(BF07H)
	6BA x ¼in Threaded Spacer	1 Pkt	(FD10L)
	Nut 6BA	1 Pkt	(BF18U)
	Tag 2BA	1 Pkt	(BF27E)
	Bolt 6BA x ½in	1 Pkt	(BF06G)
	Mains Warning Label	1	(WH48C)
	Cable Min Mains White	1 mtr	(XR02C)
	Ribbon Cable 20-Way	1 mtr	(XR07H)
	Grommet Small	1	(FW59P)
	S.R. Grommet 6W-1	1	(LR49D)
	Sleeving Heatshrink CP95	1 mtr	(YR17T)
	Clip-on TO220 Heatsink	1	(FG52G)
	Decoder PCB	1	(GD22Y)
	Veropin 2141	1 Pkt	(FL21X)
	DIL Socket 8-pin	1	(BL17T)
	DIL Socket 14-pin	4	(BL18U)
	DIL Socket 16-pin	3	(BL19V)
	DIL Socket 18-pin	1	(HQ76H)
	Safuseholder 20	1	(RX96E)
	Knob K10B	5	(RK90X)
	Transformer Mounting Bracket	1	(FD09K)
	Constructor's Guide	1	(XH79L)

OPTIONAL

	Instrument Case NM2H	1	(YM51F)
	Decoder Front Panel	1	(FD05F)
	Araldite	1	(FL44X)
	DIN Plug 6-pin	2	(HH29G)
	Standard Power Plug 2.5	2	(HH62S)
	Cable Single Core Screened Grey	1 mtr	(XR13P)
	Multi-Core 6-Way	1 mtr	(XR26D)
	Decoder Interface Cable	1	(FD17T)

A complete kit of all parts, excluding optional items, is available for this project:
Order As LM07H (MAPSAT Decoder Kit)
The following items included in the above kit list are also available separately, but are not shown in the 1986 catalogue:
Sub-Min Toggle SPDT **Order As FH02C**
6-Pin PCB DIN Socket **Order As FA90X**
0.156in Edgeconn Polarising Key **Order As FD08J**
¼in x 6BA Threaded Spacer **Order As FD10L**
Decoder PCB **Order As GD22Y**
MAPSAT Decoder Front Panel **Order As FD05F**
Transformer Mounting Bracket **Order As FD09K**
Instrument Case NM2H **Order As YM51F**
Decoder Interface Cable **Order As FD17T**
Constructor's Guide **Order As XH79L**

DECODER SYNC TONE BOARD PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1	2k2	1	(M2K2)
R2,10,11,13,22	47k	5	(M47K)
R3	100k	1	(M100K)
R4-7	33k	4	(M33K)
R8,9	470k	2	(M470K)
R12	68k	1	(M68K)
R14	82k	1	(M82K)
R15	18k	1	(M18K)
R16,19	220Ω	2	(M220R)
R17,18,20,21	4k7	4	(M4K7)
R23	220k	1	(M220K)
R24	2k7	1	(M2K7)
RV1,2	47k Vert S. Preset	2	(WR70Q)
RV3-5	10k 23-Turn Cermet	3	(WR49D)

CAPACITORS

C1,2,5,6	100nF Poly Layer	4	(WW41U)
C3	2n2F Poly Layer	1	(WW24B)
C4	10nF Poly Layer	1	(WW29G)
C7	100µF 16V Minelect	1	(RA55K)
C8	10µF 16V Minelect	1	(YY34M)
C9,10	220nF Poly Layer	2	(WW45Y)

SEMICONDUCTORS

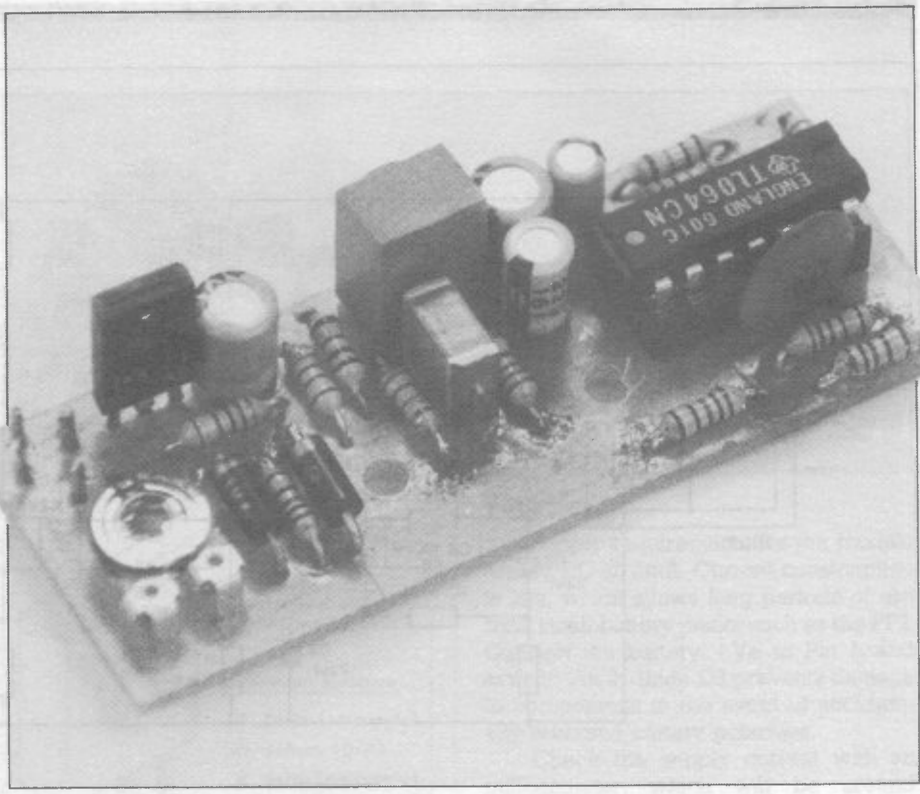
D1-3	1N4148	3	(QL80B)
TR1-3	BC548	3	(QB73Q)
IC1	4046BE	1	(QW32K)
IC2	MF10CN	1	(QY35Q)

MISCELLANEOUS

	Veropin 2145	1 Pkt	(FL24B)
	Sync 1 PCB	1	(GD23A)
	Track pin	1 Pkt	(FL82D)
	DIL Socket 20-Pin	1	(HQ77J)

A complete kit of all parts is available for this project:
Order As LM08J (Decoder Sync Tone Kit)
The following item in the above kit list is also available separately, but is not shown in the 1986 catalogue:
Sync 1 PCB **Order As GD23A**

INFRA RED PROXIMITY DETECTOR



- ★ ***Low Cost, Short Range, Heat/Movement Detector.***
- ★ ***Ideal for Doorways, Stairs and Proximity Systems.***
- ★ ***Low Power Consumption for Long Battery Life.***

by Dave Goodman

Commercially available body heat, movement detection systems, although very sophisticated in their operation, can be rather expensive for use in limited applications where short range coverage is required. This I/R proximity detector has been designed as a simple low cost system for detecting heat changes, movement of a warm body, etc., such as those emitted from the human body. The unit responds to a definite change or disturbance in ambient – or background – heat levels and could be placed across a doorway or stairs to indicate movement in those areas.

Pyroelectrics

The F001P sensor uses a ceramic, ferroelectric element made from Lead Zirconate Titanate (PZT), which has the property of producing an electrical change at its surface when the temperature changes, due to a change in polarization intensity. If a moving object enters the field of view of this sensor, changes in infra red energy levels occur due to a difference in temperature between this object and the background. Infra red energy is converted into heat by the surface electrode of the element, thus causing a change in temperature within the element itself, and a small electric charge is created as a result (see Figure 1).

This small charge appears across the gate resistance Rg in Figure 2, and is impedance buffered by the FET source follower, where a change in voltage appears across source resistance Rs. A small DC bias voltage (IDRs) is produced by the quiescent current (ID) flowing through the FET while no signal is present, as Figure 3, and output signals from the source terminal overlap this level with a +Ve voltage swing.

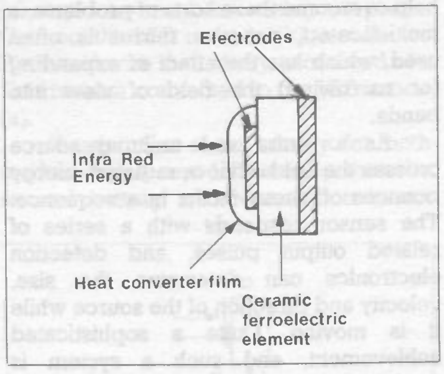


Figure 1. Pyroelectric Element.

In use, the voltage swing is very small, its amplitude being determined by the amount of incident energy available, which becomes smaller with increasing distance.

Done with Mirrors!

A negligible amount of energy is emitted from the human body which limits the effective working range of the module down to four feet or so. This range could be extended by increasing the sensitivity of the amplifier and developing velocity related filter circuits which would determine a given range of movement speeds and size of body.

An even more effective method is employed on commercial systems, in the form of collecting lenses and optical

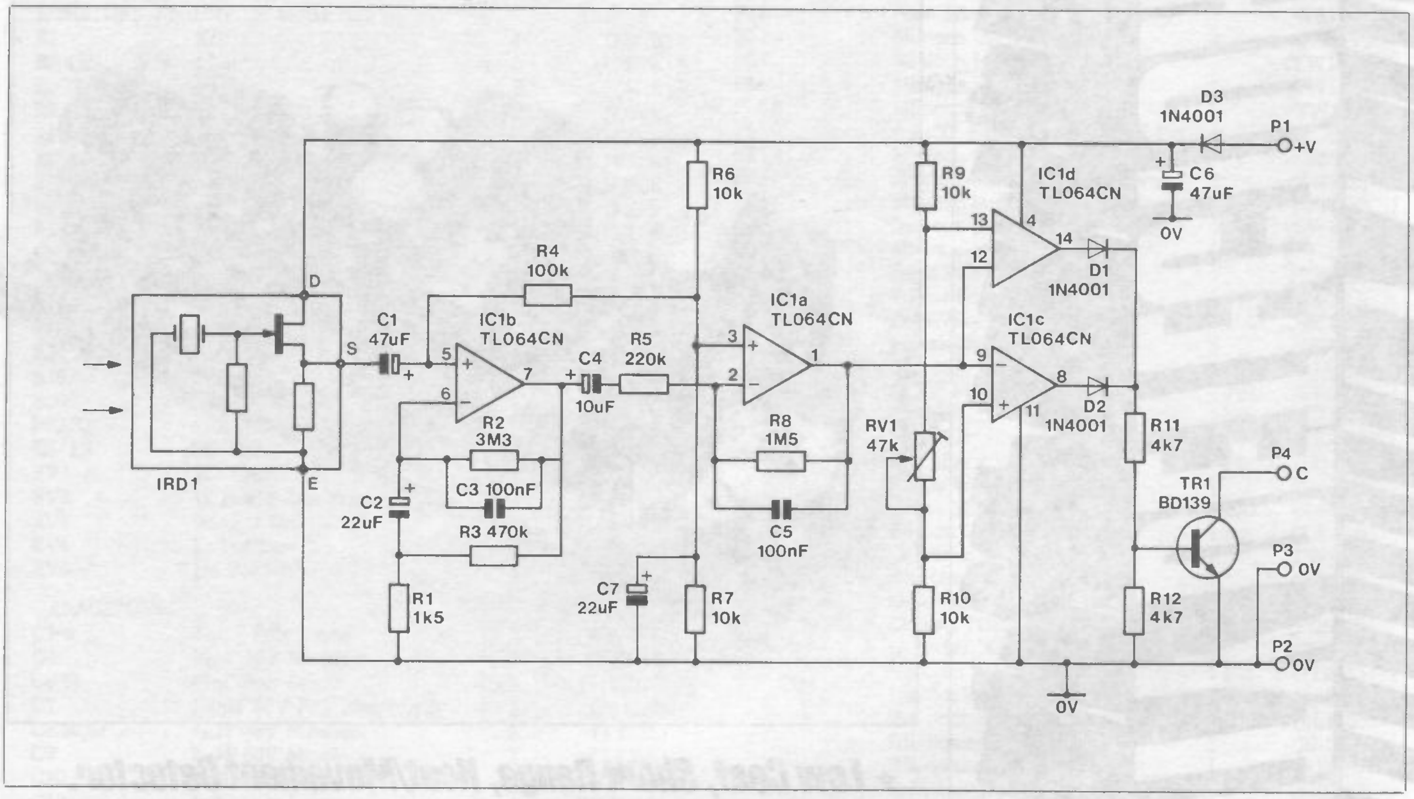


Figure 2. Sensor Circuit.

amplifying concave mirrors. Problems associated with energy collecting systems are: movements in the air, sunlight 'modulated' through curtains and even small animals generating fluctuations in the infra red energy background. To help overcome these sorts of problems, a multi-faceted, concave mirror is often used, which has the effect of expanding (or narrowing) the field of view into bands.

As an infra red emitting source crosses the field of view, radiated energy bounces off these facets in a sequence. The sensor responds with a series of related output pulses, and detection electronics can determine the size, velocity and direction of the source while it is moving. Quite a sophisticated achievement, and such a system is available in our catalogue, being more suitable for security and alarm uses than this particular system.

However, many applications exist where a simpler system is called for, especially for the home constructor!

Circuit Description

The circuit, shown in Figure 4, consists of two amplifying stages, with low pass filtering and a comparator threshold stage. Output voltage swings from the IRD are amplified by IC1b, which is configured as a non-inverting amplifier. The IRD receives energy from many sources, and a mixed waveform would be produced at IC1b output, therefore C3 integrates continuous low level signals and acts as a low pass filter.

The somewhat unusual arrangement of resistors R1 and R4 allow C2 to charge slowly during initial power up. C2 is necessary for isolating IC1b –Ve input from the 0V supply rail. With single supply op-amps, it is common to gen-

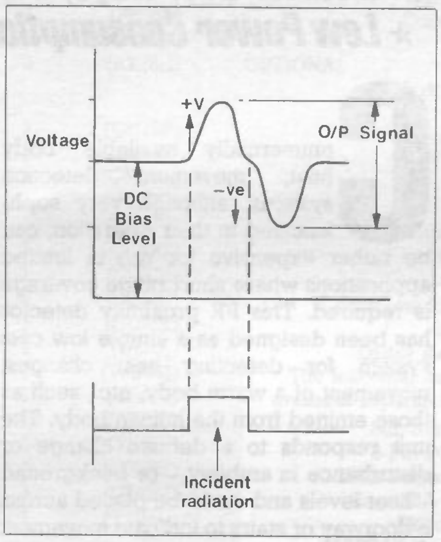


Figure 3. Source Output Voltage Swing.

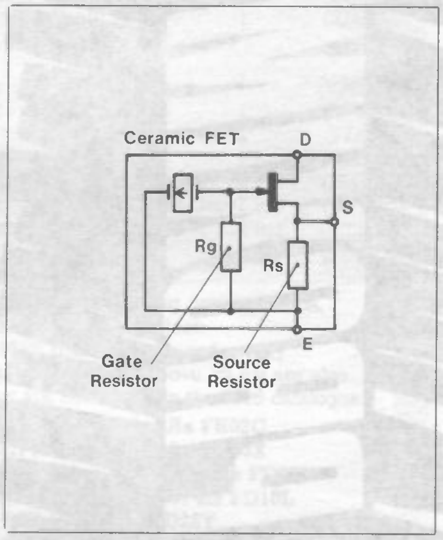


Figure 4. Proximity detector Circuit.

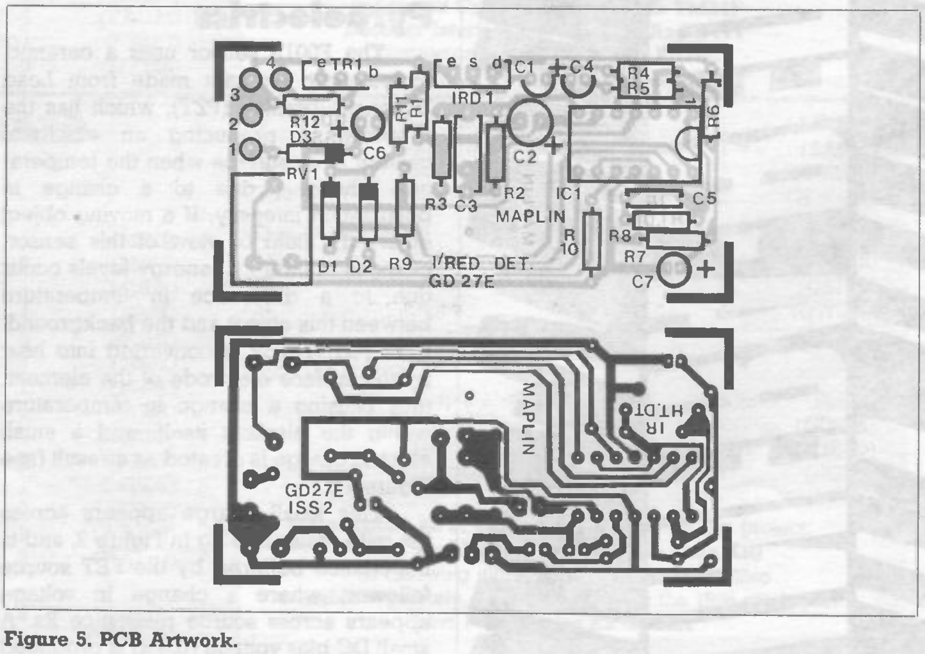


Figure 5. PCB Artwork.

erate a half supply DC voltage reference to bias the differential inputs, thus allowing output voltage swings about this level. The effect of integration on the continuous input signals produces a very low frequency output signal, which is applied to C2.

The charge across C2 varies with the magnitude of the output signal (from pin 7), and limits heavy transients from saturating this stage.

IC1a is a standard inverting amplifier, again voltage referenced to half supply by R6 and R7. C7 decouples the reference voltage to prevent comparator supply spikes from being introduced into the stage. IC1d and IC1c serve as a simple comparator. The threshold voltage reference, determining when the comparators will trigger, is set by RV1 in the potential divider chain R9 and R10.

Positive voltage swings from IC1a trigger the IC1d comparator causing D1 to conduct, while negative swings trigger IC1c causing D2 to conduct. From Figure 3 it can be seen that the output voltage swing from the IRD is, firstly, in a positive direction and then secondly in a negative direction. The ultimate effect from the comparator output at R11 is therefore not one but two pulses turning on transistor TR1.

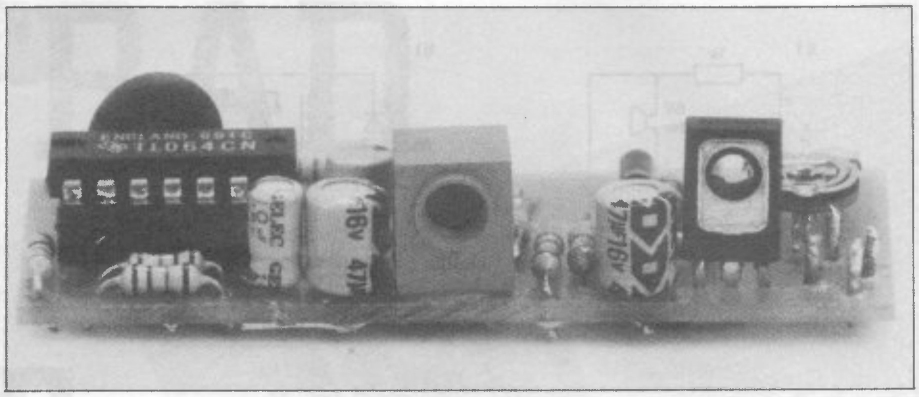
Either one of diodes D1 or D2 could be removed for single pulse output and which particular one to remove must be decided under full operational conditions. TR1 is an open collector switch, and will sink external loads (sourced from their own external +V supply) to the 0V common rail when conducting.

Construction

For information on building details and components, refer to Figure 5 for the board layout and to the 'Constructor's Guide' supplied with this kit (if you do not intend to purchase the complete kit then see the Parts List for the order code of the Constructor's Guide, price 25p). Identify and insert resistors R1 to R12. Solder these components and remove excess wire before continuing.

Mount diodes D1 to D3, and insert veropins at Pin 1 to Pin 4 in the holes marked with white circles. Next, insert a 14-pin IC socket in position IC1, and bend a few legs over the track pads to hold it in position. The PCB is quite small with tracks running close together, so care must be taken whilst soldering, as short circuits between tracks can easily occur.

Identify and insert capacitors C1 to C7. Polylayer type C3 should be fitted carefully to prevent breaking the lead out wires from each end of the package. Fit preset RV1, and solder all components in position. Again, cut off all excess leads, then fit TR1 and the sensor IRD1 shown in Figure 6. One side of TR1 has a metal, heat transfer mounting plate fitted. Insert TR1 with this plate facing outward towards the edge of the pcb. The sensor IRD1, shown in Figure 7, could be mounted vertically from the pcb, or horizontally off the pcb as detailed. Mount the sensor as close as possible – in both cases – to the pcb in order to reduce noise induced into this area.



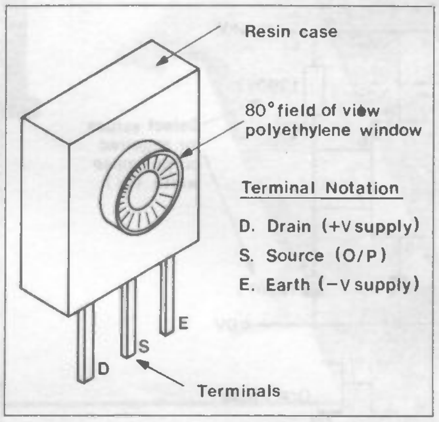


Figure 6. Sensor pin-outs.

Either mounting position will have to take into account the boxing (case) requirements, and this is left to the fitting as required by the constructor. Solder any remaining components, cut off all excess wires and clean up the track area to facilitate inspection.

Testing

Supply requirements for the module are 9V DC @ 2mA. Current consumption is low, which allows long periods of use from small battery packs such as the PP3. Connect the battery +Ve to Pin 1, and −Ve to Pin 2; diode D3 prevents damage to components in the event of accidentally reversed battery polarities.

Check the supply current with an milliammeter, which will be around 2.5mA for a minute or so, dropping to 1 – 1.5mA after this period. Current consumption increases by approximately 1mA while the comparator stages are operating.

The output transistor TR1 does not *source* current, but being open collector will sink current from an external supply load. Figure 8 suggests various methods of switching external loads, and diagram (a) could be used for testing purposes. Connect the LED cathode (k) to collector Pin 4, and wire the battery to one end of a 1kΩ resistor connected to the LED anode (a).

If using the same battery for both module supply and LED supply, then the second battery −Ve connection is not

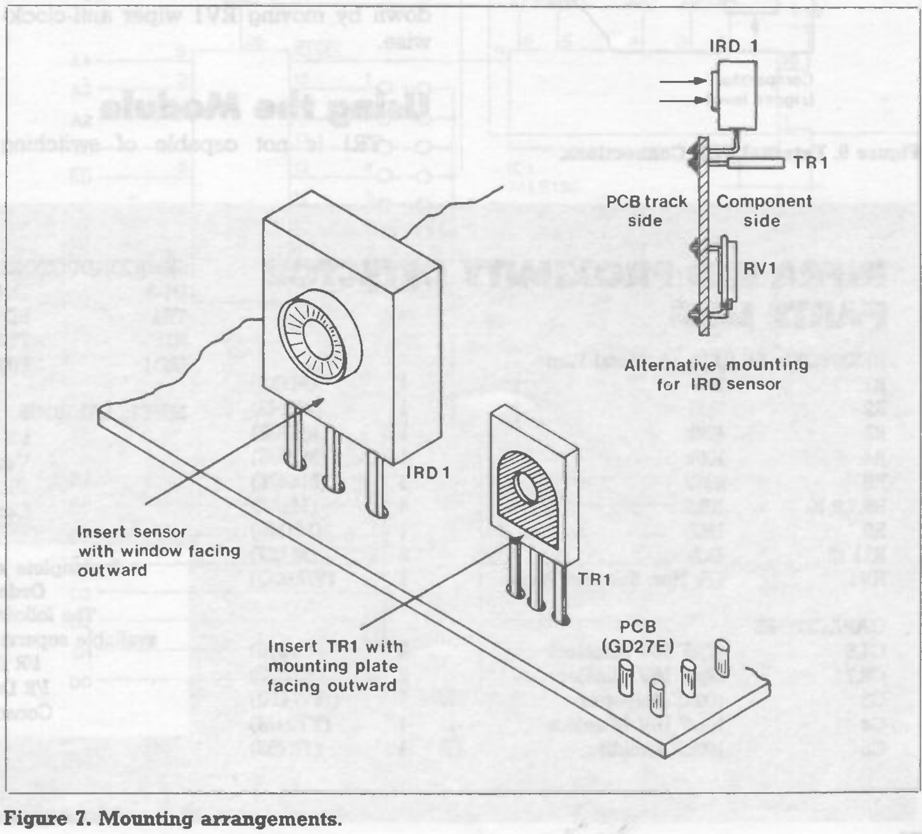


Figure 7. Mounting arrangements.

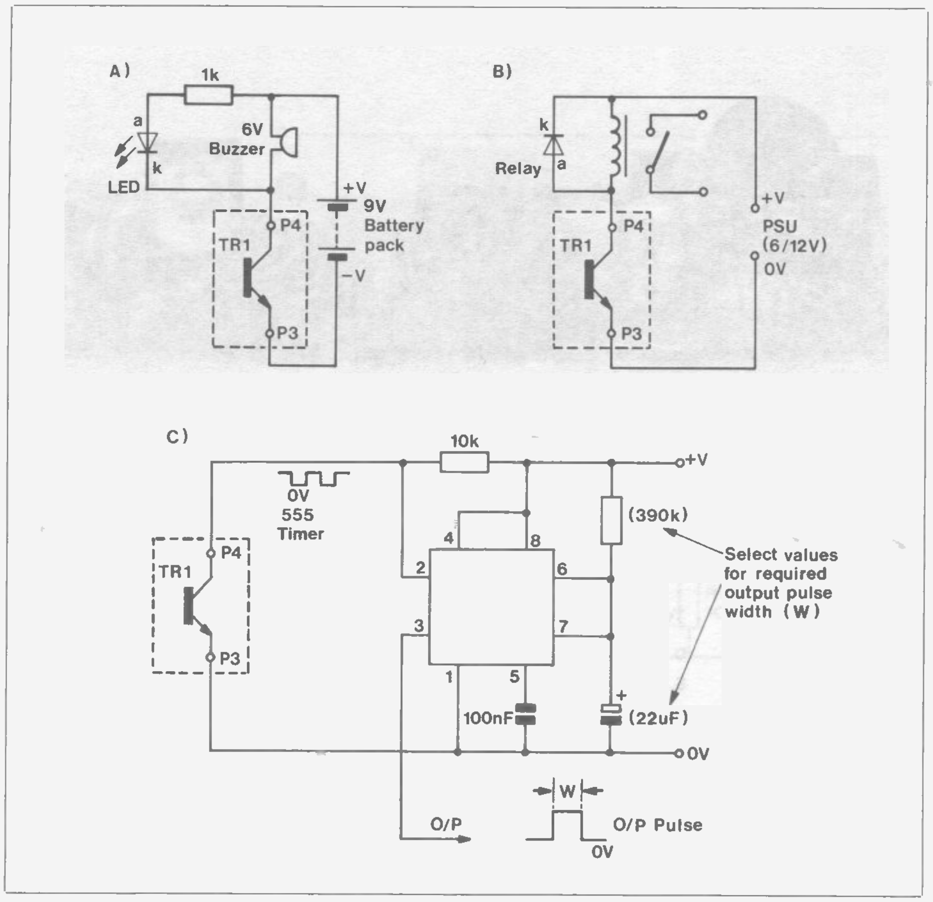


Figure 8. External Circuit Connections.

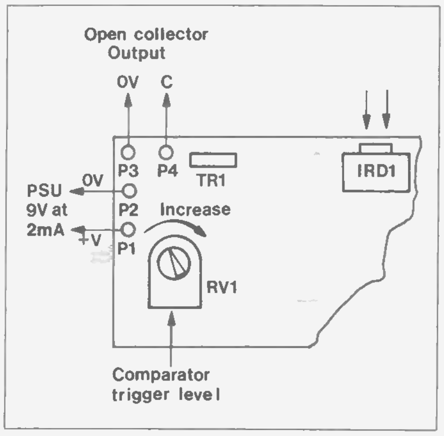


Figure 9. External PCB Connections.

required. Turn the comparator threshold control, RV1, to half travel (Figure 9), and after the initial 'warming up' period, move your hand across the sensor window. Do not poke the window with fingers as grease deposited will reduce sensitivity and may prevent operation completely! Figure 10 shows the spectral response expected in the window. The LED will light for a few seconds. If the LED is permanently aglow, turn the trigger level down by moving RV1 wiper anti-clockwise.

Using the Module

TR1 is not capable of switching heavy loads and should be used on external systems up to 12V DC, and current levels below 100mA. Relays could be used for controlling larger voltage/current devices (Figure 8b), or a timer could be employed to generate long operating periods once triggered (Figure 8c). On the prototype, a 6V @ 35mA buzzer was used, on a separate supply, to good effect. Any battery supplying the electronics should not be used for supplying the external devices as well, if more than a simple LED arrangement is to be used. Battery connections to Pin 1 and 2 should be kept short – a PP3 clip lead is ideal for this – and mount both module and battery together in the same housing with a suitable ON/OFF switch.

Sensing range is 4 to 5 feet, depending upon the sensor's field of view and variations in the light/heat background levels. A whole room, for instance, could not adequately be covered by this system, but doorways, narrow hallways and corridors are suitable areas. Another use for the module could be in a shower cubicle, using a timer circuit for controlling the water pump. Obviously, low voltage switching systems are important in this application.

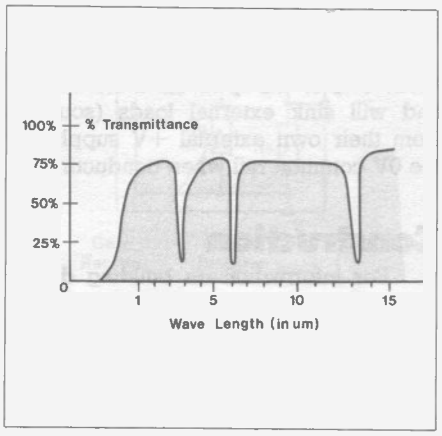


Figure 10. Window Spectral response.

INFRA RED PROXIMITY DETECTOR PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1	1k5	1	(M1K5)
R2	3M3	1	(M3M3)
R3	470k	1	(M470K)
R4	100k	1	(M100K)
R5	220k	1	(M220K)
R6,7,9,10	10k	4	(M10K)
R8	1M5	1	(M1M5)
R11,12	4k7	2	(M4K7)
RV1	47k Hor. Sub-min Preset	1	(WR60Q)

CAPACITORS

C1,6	47μF 16V Minelect	2	(YY37S)
C2,7	22μF 16V Minelect	2	(YY36P)
C3	100nF Polyester	1	(WW41U)
C4	10μF 16V Minelect	1	(YY34M)
C5	100nF Minidisc	1	(YR75S)

SEMICONDUCTORS

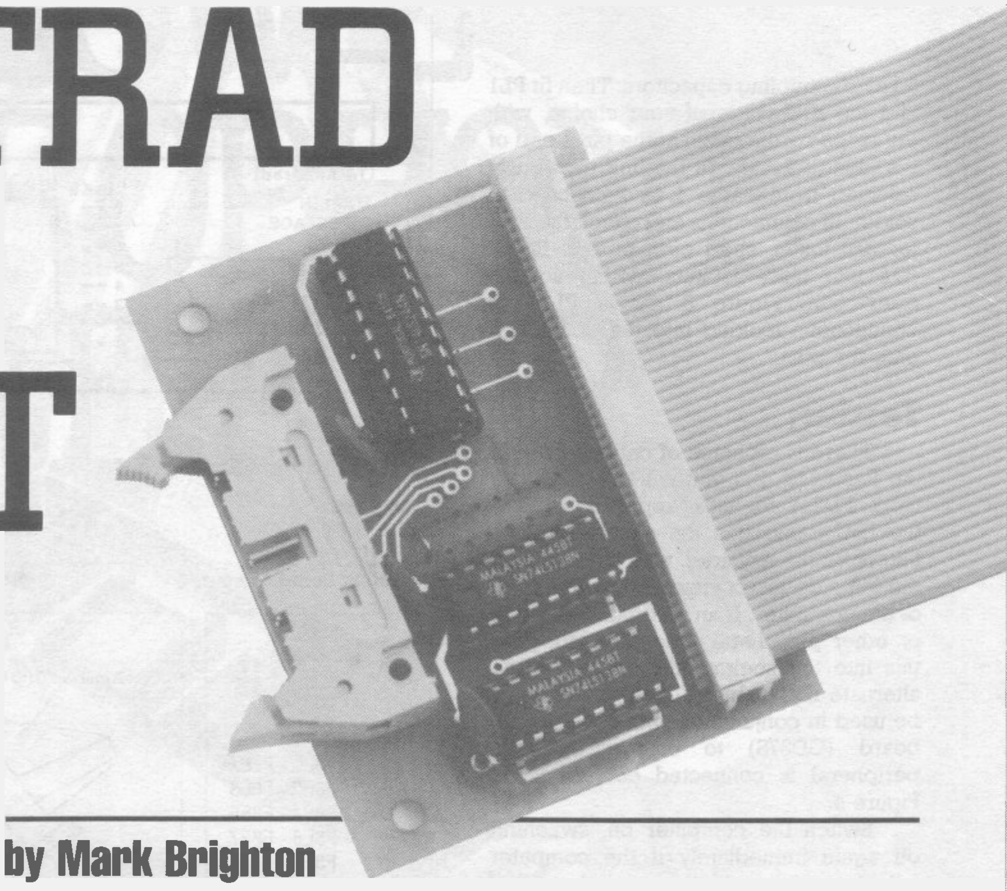
D1-3	1N4001	3	(QL73Q)
TR1	BD139	1	(QF07H)
IC1	TL064CN	1	(RA66W)
IRD1	F001P	1	(FD13P)

MISCELLANEOUS

	I/R Detector PCB	1	(GD27E)
	Veropins 2145	1 Pkt	(FL24B)
	DIL Socket 14-Pin	1	(BL18U)
	Constructor's Guide	1	(XH79L)

A complete kit of all parts is available for this project:
Order As LM13P (I/R Detector Kit)
The following items in the above kit list are also available separately, but are not shown in the 1986 catalogue:
I/R Detector PCB **Order As GD27E**
I/R Detector F001P **Order As FD13P**
Constructor's Guide **Order As XH79L**

AMSTRAD 8 BIT INPUT PORT



by Mark Brighton

★ **Inexpensive - Easy to Build and Fit**
★ **Compatible with BBC User Port Socket**

This article describes a simple 8-bit input port which plugs into the expansion connector on the rear of the Amstrad CPC 464/664/6128 range of computers and allows information from the outside world to be read and stored by the computer. It may be used, for example, to interface the weather satellite decoder described elsewhere in this issue with the Amstrad computers.

Circuit Description

In Figure 1, IC1 decodes $\overline{IORQ}$ and A5 - A7 to produce $\overline{IOSEL}$, which is active for any valid external I/O address, enabling IC2 when $\overline{RD}$ is active and A4 is high.

This locates the port within the second block of 16 addresses in the valid external I/O area starting at $F8E0, although the constraints imposed on the design complexity by the low cost specification precluded complete address decoding, so there are 'ghost images' of the port in the other I/O areas. For this reason, the port address may also be located at any two addresses within the block of sixteen by fitting one of the eight links as shown in Table 1.

By carefully choosing the link required, it should be possible to avoid overlapping the port with any other external I/O mapped device used within the system.

Finally, IC3, when enabled via the link fitted, gates any data present on P_0 - P_7 onto the data bus to be read by the processor.

Construction

Referring to the Parts List and the legend, as shown in Figure 2, fit and solder the IC sockets, ensuring that the notch on each socket aligns with the legend. Locate and solder the three

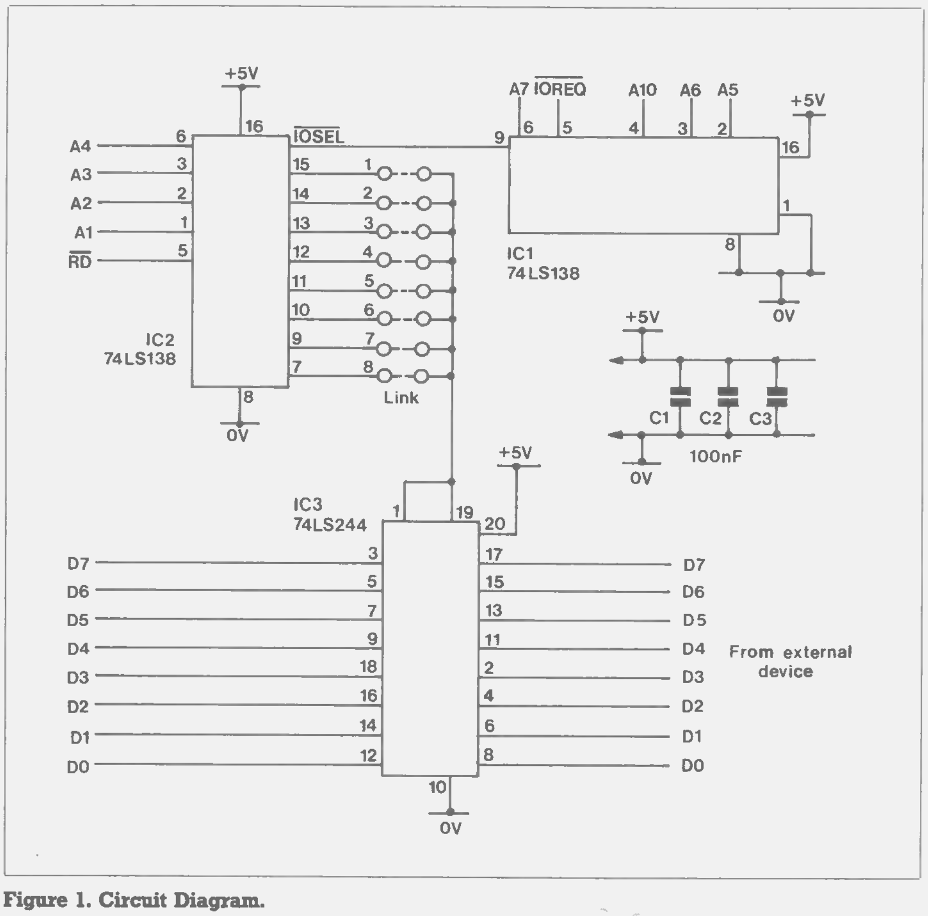


Figure 1. Circuit Diagram.

0.1μF decoupling capacitors. Then fit PL1 and the IDC cable of your choice, with the stripe on the cable at the pin 1 end of the legend! Lastly, fit the link previously selected from Table 1, and proceed to solder all connections and check the PCB for dry joints, short circuits, etc. Fit all IC's into their sockets, noting correct orientation. Figure 3 shows PL1 pin connections looking into the connector, onto the pins.

Testing

There is a choice of cables given in the Parts List, but you will probably use cable FD22Y for most applications. Plug the IDC cable into the expansion connector on the Amstrad, with the stripe on the left side when viewed from the *front* of the computer. If an external disk drive or other peripheral is to be used, plug this into the socket mid-way along the alternate IDC cable (FD24B) which must be used in conjunction with our Reversiboard (GD37S) to ensure that the peripheral is connected correctly, see Figure 4.

Switch the computer on, switching off again immediately if the computer fails to initialise in the normal way of displaying the 'ready' prompt.

If all is well, reading the address chosen with an 'INP' command should return the number set-up on the port inputs (if nothing is connected to the port, 255 will be read).

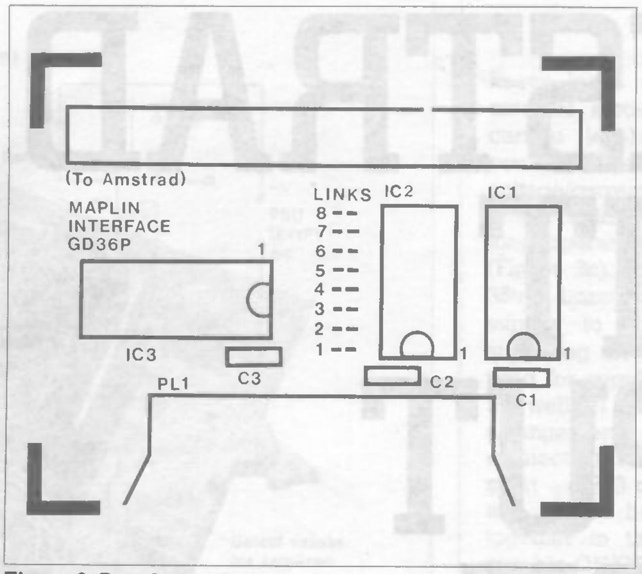


Figure 2. Board Layout.

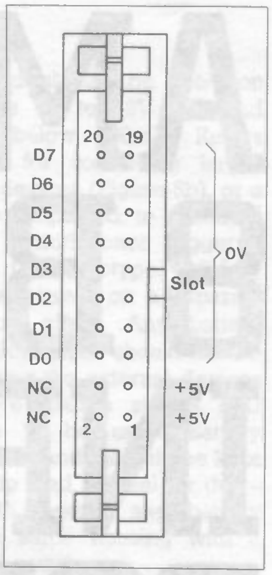


Figure 3. Header Plug.

LINK	ADDRESS
1	F8E0 - F8E1
2	F8E2 - F8E3
3	F8E4 - F8E5
4	F8E6 - F8E7
5	F8E8 - F8E9
6	F8EA - F8EB
7	F8EC - F8ED
8	F8EE - F8EF

Table 1.

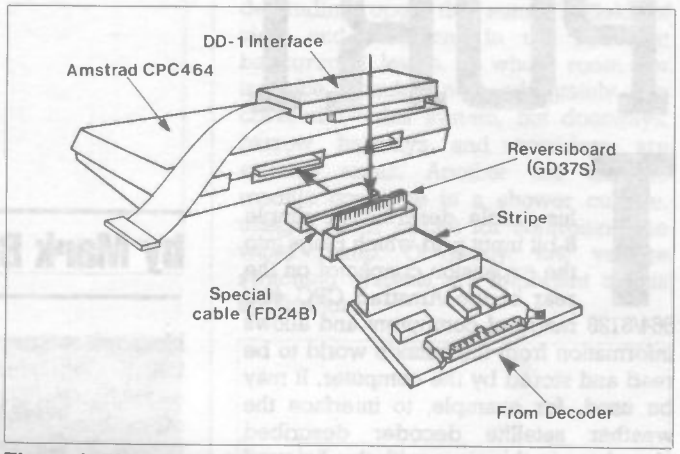
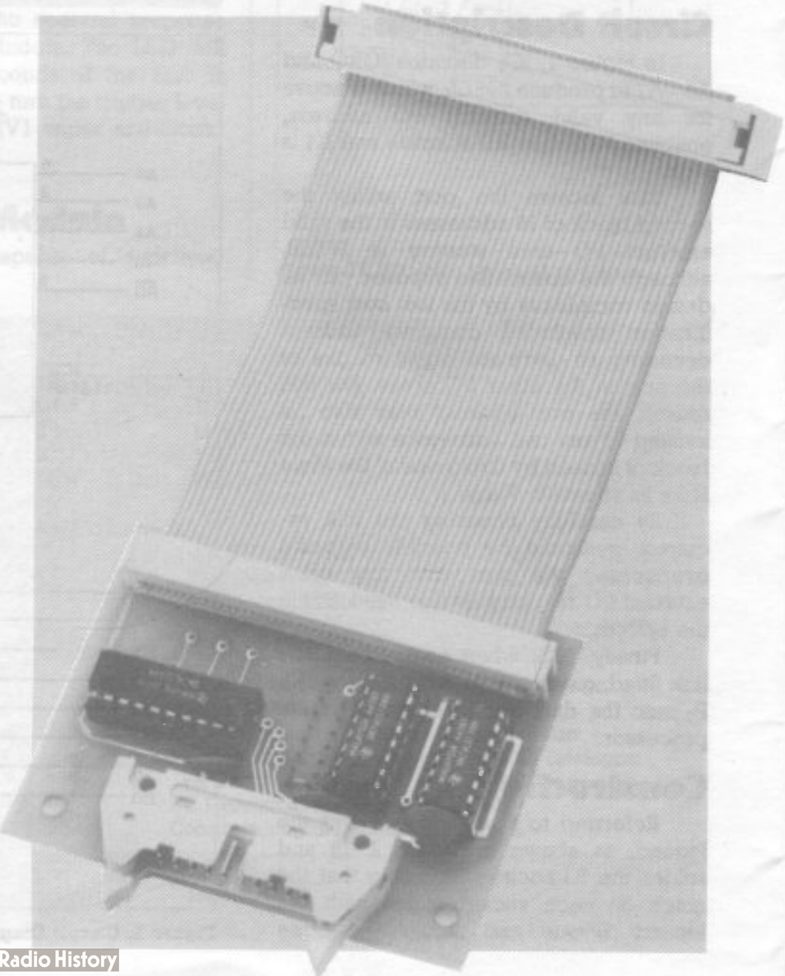


Figure 4. Alternate cable.

AMSTRAD 8-BIT I/P PORT PARTS LIST

CAPACITORS			
C1-3	100nF Minidisc	3	(YR75S)
SEMICONDUCTORS			
IC1,2	74LS138	2	(YF53H)
IC3	74LS244	1	(QQ56L)
MISCELLANEOUS			
	Amstrad Interface PCB	1	(GD36P)
PL1	20-way IDC Header R/A	1	(FT72P)
	DIL Socket 16-way	2	(BL19V)
	DIL Socket 20-way	1	(HQ77J)
	Bolt 6BA x ½"	1 Pkt	(BF06G)
	Nut 6BA	1 Pkt	(BF18U)
OPTIONAL			
	Cableform Amstrad/Interface	1	(FD22Y)
	Cableform Amstrad/Disc/Interface	1	(FD24B)

A complete kit of all parts, excluding optional items, is available for this project:
Order As LM14Q (Amstrad 8-bit I/P Port Kit)
The following items included in the above kit list are also available separately, but are not shown in the 1986 catalogue:
Amstrad Interface PCB **Order As GD36P**
Amstrad/Interface Cable **Order As FD22Y**
Amstrad/Disk/Interface Cable **Order As FD24B**
Reversiboard **Order As GD37S**



LOW Z MICROPHONE PRE-AMP

by Dave Goodman

- ★ ***Use with Balanced and Unbalanced Microphones***
- ★ ***300 - 600Ω Low Level Input, High Level Output***
- ★ ***Very Low Noise and Distortion***
- ★ ***Low Supply Current Drain***

General purpose microphones are usually supplied as either high impedance or low impedance versions and occasionally, both. In the past, high Z (where 'Z' represents 'impedance') microphones have been the most commonly used in non-studio applications, especially for stage mixing and PA amplification. Modern technology has allowed for very high quality Low Z microphones to be more readily available at much lower prices.

Matching these devices to High Z system inputs poses a problem, due to the inherent low signal levels, and resulting lack of high frequency response. In the absence of Low Z input facilities on amplification equipment, a pre-amplifier is required to match the mic' output impedance and amplify signals to a level suitable for driving into high Z inputs.

The Low Z mic' pre-amp module is intended for this purpose, and is available either in kit form, for home constructors, or as a ready-built module complete with its own screening case.

Impedance

The term impedance, abbreviated to 'Z', is commonly used in electronics and the expression describes the joint opposition to the flow of current, caused by the presence of resistance and reactance, in the circuit. With microphones, be they dynamic or condenser types, it is necessary to know the capabilities of the transducer, under specific operating conditions.

For instance, if a microphone output is designed to deliver 10mV of signal into a 47kΩ load, then decreasing the load to 100kΩ or more (remembering that a larger resistance is a lighter load) would allow a higher signal voltage, greater than 10mV, to be developed. Alternatively, increasing the load to 600Ω or less would greatly reduce the signal level developed.

To standardise these variations, microphone specifications typically state voltage (signal) levels with a particular impedance value; usually 47kΩ for high Z mic's and 600Ω for low Z mic's. With high impedance microphones, frequency is important when driving into a *reactive* circuit. Inductive and capacitive reactances effect the microphone signal level dramatically, and specifications often apply to voltage and impedance values at a frequency of 1kHz.

Low Z Mic Pre-amp Module

MODULE SPECIFICATIONS

Input Impedance	–	600Ω Balanced (300 – 0 – 300Ω)
Typical Signal Levels	–	1.25V out for 1mV in
Maximum Output Level	–	2V r.m.s (5.6V Pk)
Input/Output Gain	–	30 to 50dB Variable
Signal to Noise Ratio	–	80dB
Distortion (@ 1kHz)	–	0.02%
Frequency Response	–	50Hz to 30kHz (– 1dB)
PSU Requirement	–	9V @ 3mA

Low Z Balanced Lines

Figure 1 shows two typical configurations for balanced and unbalanced line connections to this module. Because Low Z mic signal levels are very low, in the order of 100 to 500μV, induced noise and hum becomes a very real problem especially where long connecting cables are used. Not all microphones have the facility for balanced line connection high level to begin with. High impedance microphones could be coupled directly to the input of the Tx module, as could cassette or amplifier line outputs.

TR1 on the transmitter module (Figure 4) pre-amplifies the incoming signal and RV1 is adjusted to suit the input signal level from Pin 4. Because a low voltage supply is used here (4.8 – 6V) the input range dynamics are somewhat limited and C1 has been chosen to roll off low frequency signals, which would otherwise produce distortion from the receiver output.

The low power, CMOS, Phase Locked Loop device, IC1, is used as a voltage controlled oscillator, operating at a centre frequency of 110kHz. Audio signals from TR1 collector swing the VCO each side of the 110kHz centre frequency, thus frequency modulating the 'carrier' signal. At test point TP2, a 5V square wave representing the modulated carrier is available, this being buffered by an emitter follower TR2 to the current switch TR3.

The Light Guide Emitter MF0E71 is an infra-red PIN diode, which is switched on and off, at the carrier frequency, by transistor TR3. R12, of 47Ω, limits current through the PIN diode at an average 40mA. The diode is capable of taking up to 100mA, made possible by reducing the value of R12 down to 22Ω or so, but power supply demands are then greater. If using a 4 cell nicad pack (5.2V) then the lower 40mA current drain is preferable for longer battery life. The advantage of increasing current through the PIN-diode comes from an increased light output; the signal to noise ratio is improved and greater transmission distances are possible, although by only a few metres, but this is only practicable given the appropriate power supply.

Hence R12 is here optimised at 47Ω for a 40mA collector current. Timing components C3 and R7 determine the VCO centre frequency and RV2, R5 allow a 25kHz adjustment approximately over a 95kHz to 120kHz range. Light transmitted from the MF0E71 is in the infra-red band at a peak, spectral wavelength of 820nM; the full bandwidth extends from 400 to 1000nM (nano-metres) with an 80% reduction in output power.

Receiver

Audio signals in the form of frequency modulated, infra-red light now have to be amplified, detected, demodulated and filtered to reconstitute the original waveform. A matching infra-red detector, MF0D71, is used in reversed-bias mode with current limiting resistor R1 (see Figure 5). Output current to TR1 is extremely small, so the front pre-amplifying stages have a very high gain. TR1 and TR2 are configured as a DC coupled amplifier, self biased by R2. C3 is the main AC feedback component, and this stage has a frequency response of up to 0.5MHz.

With such a high gain, wide band pre-amplifier, noise levels are increased,

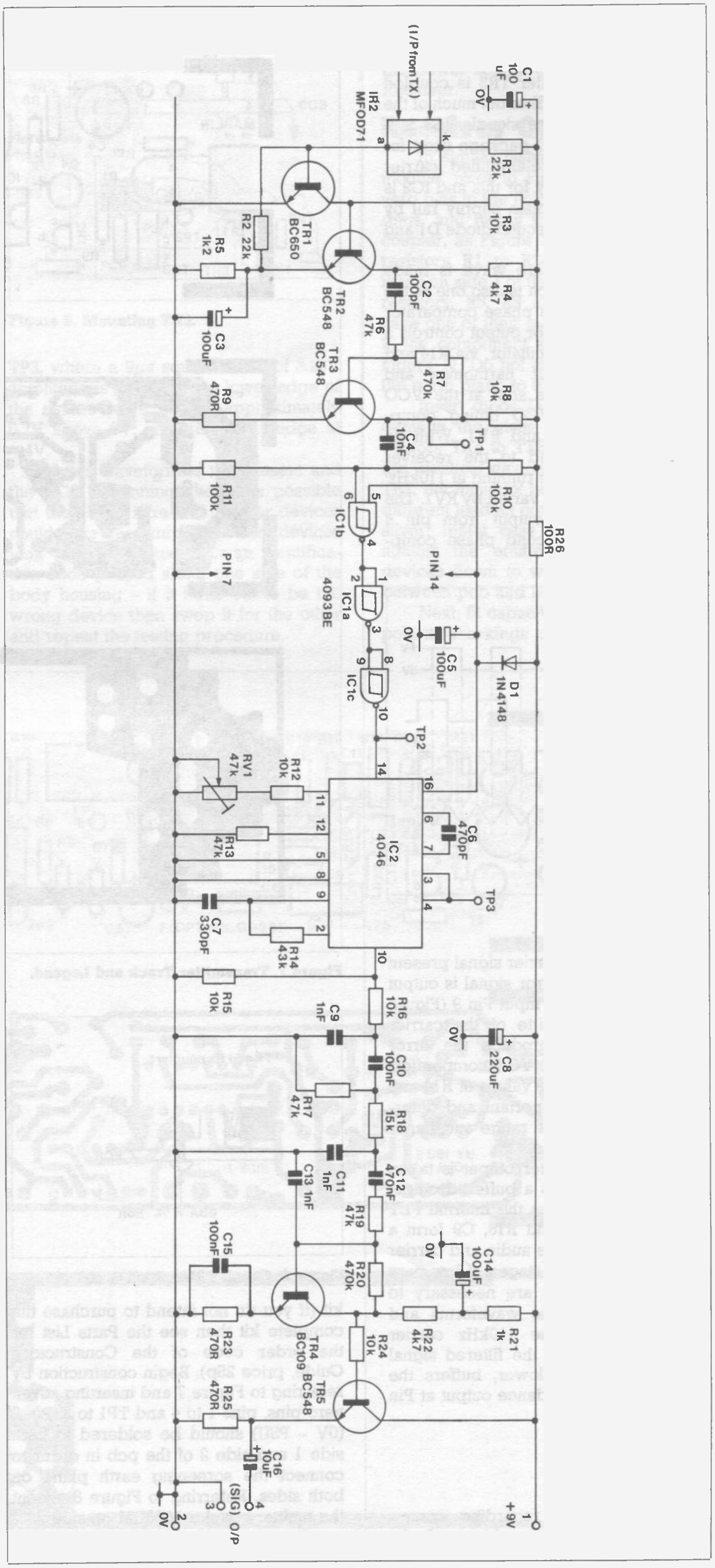


Figure 5. Receiver Circuit.

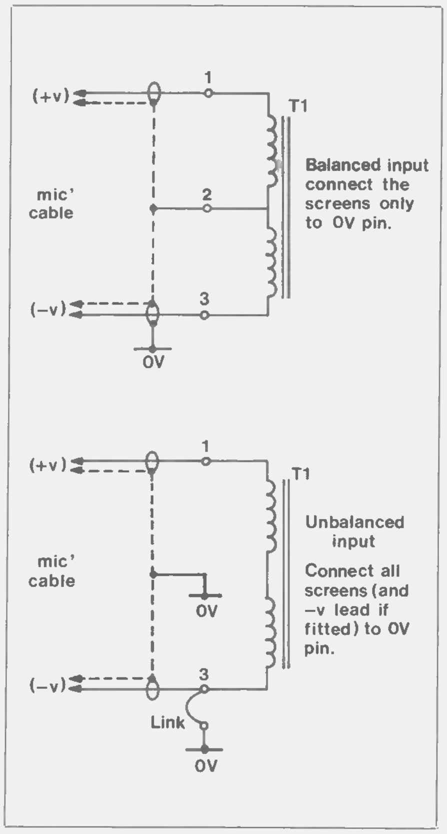


Figure 1. Balanced and Unbalanced Lines.

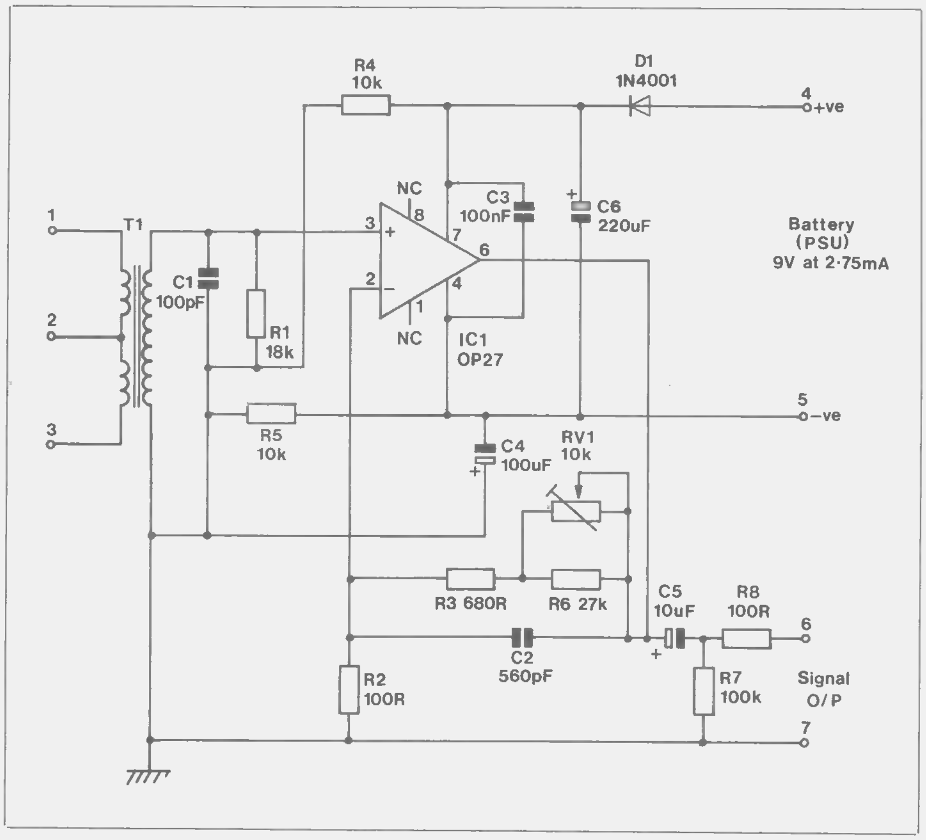


Figure 2. Circuit Diagram.

however, and in this case the unbalanced system must be adopted, although with degraded noise performance. The step up transformer, T1, can be used in either balanced or unbalanced systems with 600 and 300Ω microphones. 200Ω unbalanced lines can also be used, although output signal levels will be reduced by a few dB.

Circuit Description

Figure 2 shows IC1 which is a very low noise, instrument grade op-amp offering wide bandwidth, high slew rates and reduced low frequency noise performance.

For improved component noise figures, gain determining components, R2 and R3, have low values of resistance and C2 prevents RF breakthrough problems associated with local radio transmissions. Capacitor C1 limits HF response and R1 with T1 secondary determine the input impedance for optimum performance of IC1.

The preset potentiometer RV1 allows gain adjustment over a 20dB range, with resistor R6 selected at 27kΩ. The signal output impedance is approximately 600Ω, but at a much amplified level, making for compatibility with high impedance equipment inputs, and DC isolation is maintained by C5. Diode D1 prevents circuit damage in the event that the power supply connections may be reversed, and the divider made up from R4, R5 provides a local '0V' central to the positive/negative supply rails, for the purpose of biasing the inputs of IC1. Input and output signals are consequently referenced to this 0V tap, and *not* the negative rail, which is connected to a top earth plane of the PCB to ensure stability.

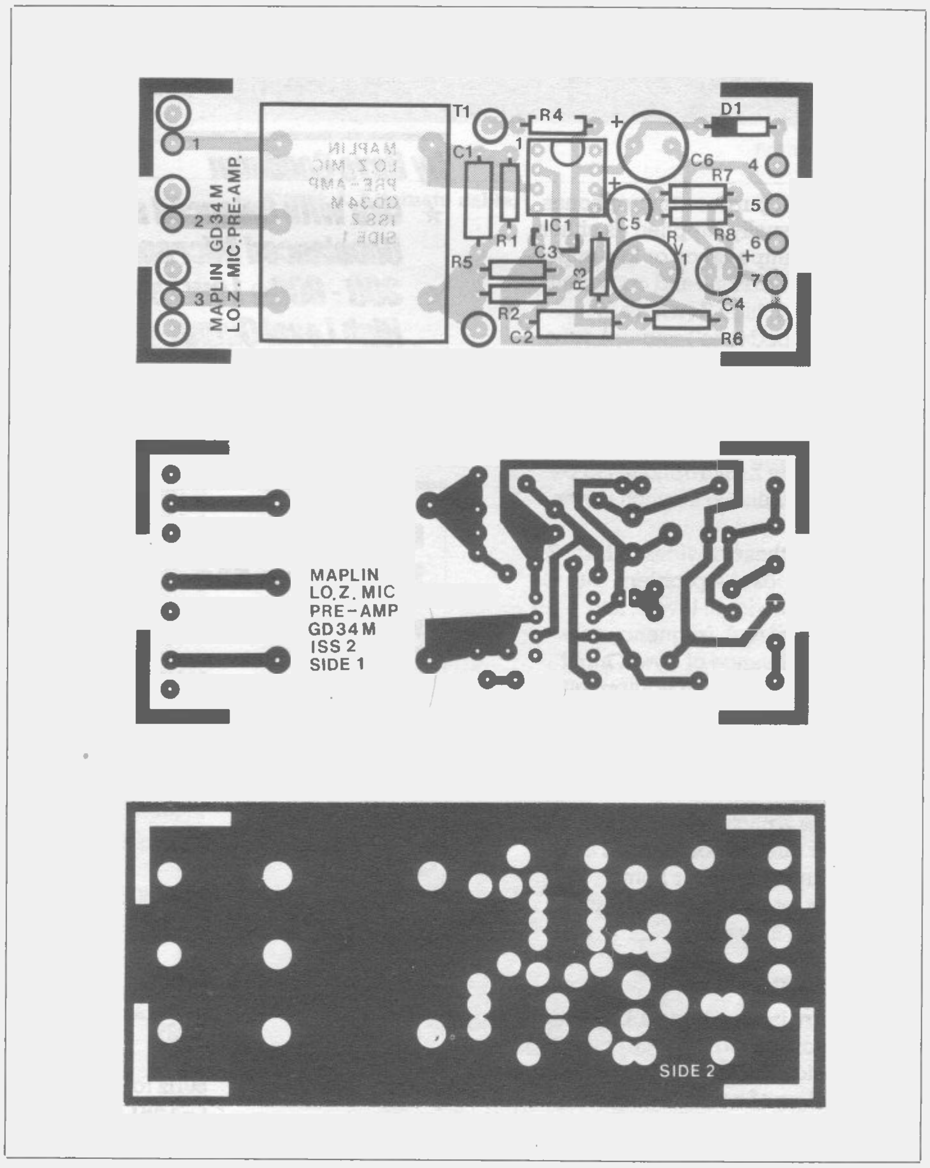


Figure 3. Track and Overlay.

Construction

Reference should be made to the 'Constructor's Guide' supplied with this kit (if you do not intend to purchase the complete kit then see the Parts List for the order code of the Constructor's Guide, price 25p), and Figure 3 which shows the PCB track and legend.

Component assembly is quite straight forward and is best begun by inserting 14 vero pins as detailed in Figure 4. Fit each pin into holes marked with a circle, from track side 1 and solder all pin heads. Seven of these pins require to be soldered on *both* sides of the PCB for connection to the earth plane.

Identify and insert resistors R1 to R8, and capacitors C1 to C6. Observe the polarity rules with electrolytics, and ensure there is adequate clearance between the leads of these components and the earth plane areas on top of the PCB.

Fit diode D1 and solder these components in position, removing excess wires. Mount IC1 directly into position on the board and insert RV1. Carefully solder these components and mount transformer T1 firmly onto the board and solder in place. Do ensure that the five terminating posts on T1 do not touch the earth plane or short across to any components. Clean the track areas and inspect all joints, looking for short circuits, etc.

Testing

A signal source is required, such as a microphone or AF signal generator, and also an amplifier or oscilloscope for monitoring the module output. Power supply requirements are low so a 9V battery, such as a PP3 can be used for this project. Connect the negative supply to Pin 5 (Figure 4) and positive supply via a milliammeter to Pin 4. With 9V applied, the current consumption is approximately 3mA; any large deviation from this figure will point to a fault condition such as D1 or IC1 fitted incorrectly, so switch off immediately and recheck. If all is well, connect a signal source across Pins 1 and 3, and wire Pin 3 to an adjacent 0V terminal.

Take the signal output from Pin 6 to a 'scope, or to an amplifier. Pin 7, connected to 0V, is the ground return connection for the 'scope or amp' cable screen/earth return. When using a signal generator, keep the peak-to-peak signal level at 5 to 10mV maximum, to avoid excessive distortion of the audio output. Turn RV1 clockwise for increased output signal or anticlockwise to decrease. When satisfied that the module is working, fit the screening case as follows.

Case Mounting Details

With reference to Figure 5 place a layer of insulating material cut to the size of the PCB (85 x 33mm) over the inside

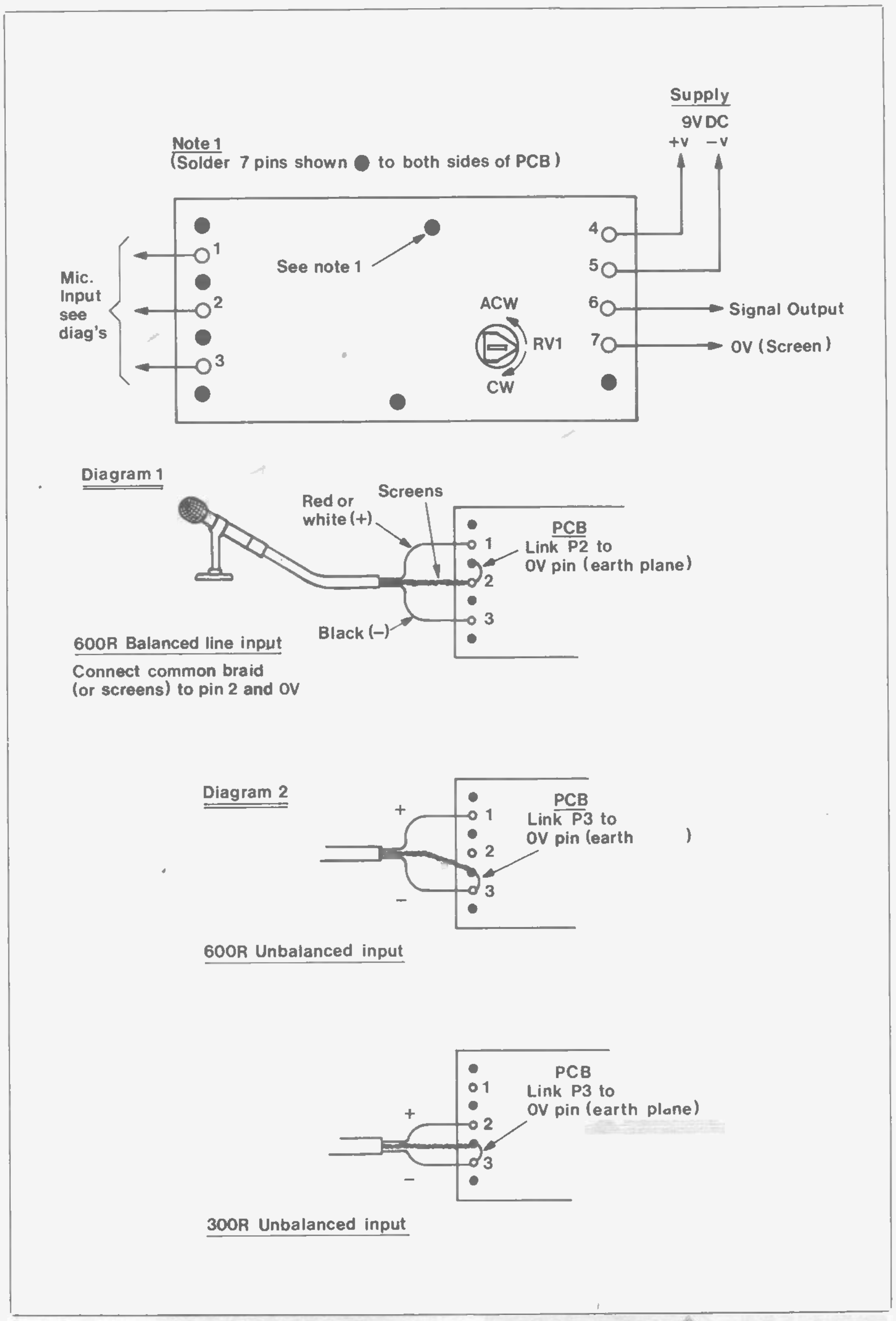
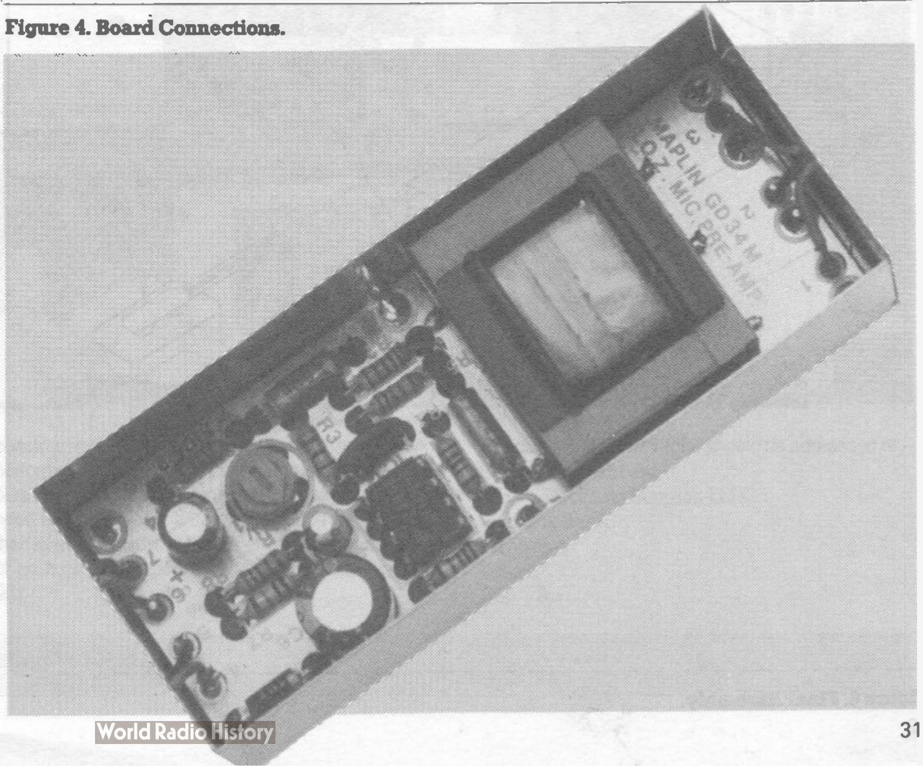


Figure 4. Board Connections.



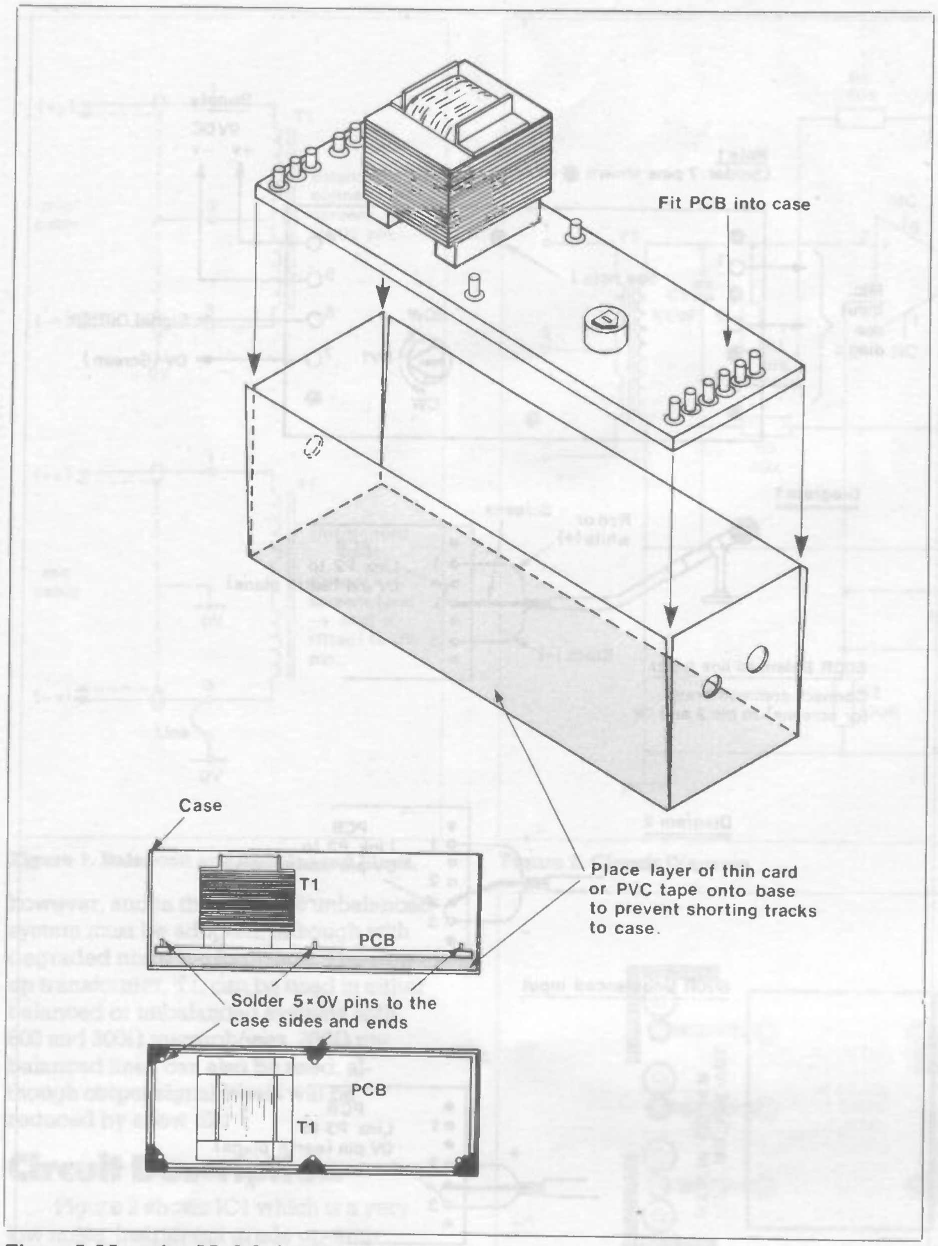


Figure 5. Mounting Module into Case.

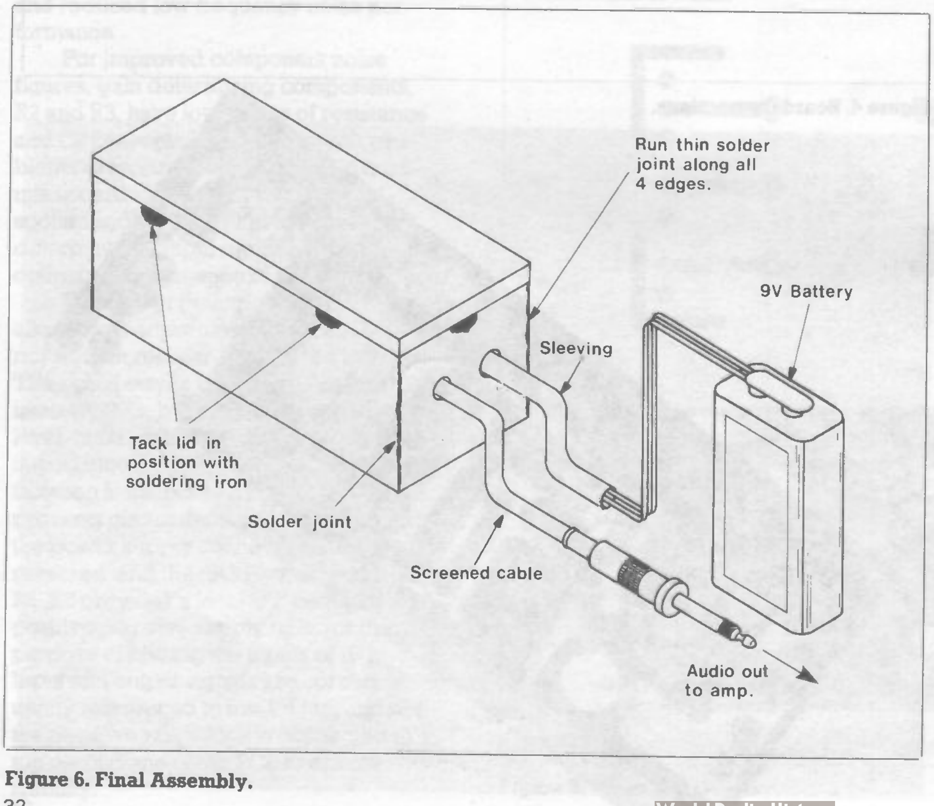


Figure 6. Final Assembly.

base area of the case. The material could be thin card, polythene or a few layers of PVC insulating tape. This insulation prevents the PCB tracks and joints from shorting to the case bottom. Insert the working module into the case with Pins 1 to 3 facing the case end panel that is drilled with a single hole only. If the module is a tight fit then the side plates can be spread apart or the PCB sides may be filed slightly to remove high spots, to help with this operation.

Push the module down towards the base until the transformer T1 just clears the top of the case, and does not obstruct the lid. Test that the module is still working correctly, and then apply small solder joints between all the 0V pins and the case sides as shown. *Do not* overheat the earth plane area, *or* put excessive amounts of solder onto the board. All that's required is a few small joints connecting the case to 0V, and to hold the PCB in position. The four corner edges can have a thin film of solder run along them, but electrically, this should not be necessary, especially if the module is required to be removed from the case later on.

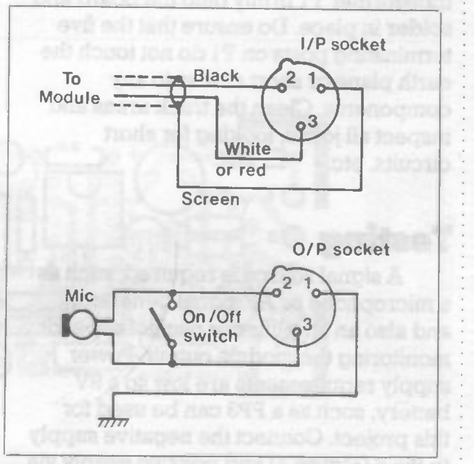


Figure 7. Wiring XLR Connectors.

Final Assembly

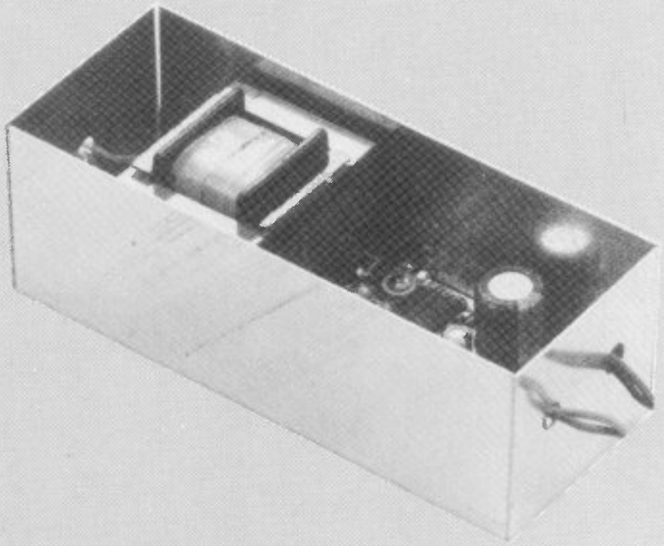
Input/output cables and battery/PSU connections can be made through the end panel holes of the case. Heat shrink sleeving can be fitted over thin wires to prevent them from chafing on the hole edges. Be careful when soldering wires to the PCB pins, as solder can run down onto the earth plane and cause a short circuit.

The input cable (from the microphone) screening braid can conveniently be soldered directly to the outside of the case as can the screened output cable from module to amplifier. Once wiring has been completed, fit the lid in position and distribute a few solder joints around the edges to seal the case, see Figure 6.

Figure 7 details various XLR plug and socket wiring arrangements for reference purposes; the terminals shown are standardised for most microphone/mixer systems, and these connectors are recommended where small signal, low noise terminations are required.

LOW-Z MIC PRE-AMP PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1	18k	1	(M18K)
R2,8	100Ω	2	(M100R)
R3	680Ω	1	(M680R)
R4,5	10k	2	(M10K)
R6	27k	1	(M27K)
R7	100k	1	(M100K)
RV1	10k Cermet	1	(WR42V)
CAPACITORS			
C1	100pF Polystyrene	1	(BX28F)
C2	560pF 1% Polystyrene	1	(BX54J)
C3	100nF Minidisc	1	(YR75S)
C4	100μF 10V PC Electrolytic	1	(FF10L)
C5	10μF 16V Minelect	1	(YY34M)
C6	220μF 16V PC Electrolytic	1	(FF13P)
SEMICONDUCTORS			
IC1	OP-27GNB	1	(RA74R)
D1	1N4001	1	(QL73Q)
MISCELLANEOUS			
T1	Mic Transformer 600/20	1	(FD23A)
	Low-Z Mic Pre-amp PCB	1	(GD34M)
	Low-Z Mic Pre-amp Case	1	(FD20W)
	Veropins 2145	1 Pkt	(FL24B)
	Constructor's Guide	1	(XH79L)
OPTIONAL			
	2mm Systoflex Black	As req	(BH06G)
	PP3 Battery Clip	1	(HF28F)



A complete kit of all parts, excluding optional items,
is available for this project:
Order As LK80B (Low-Z Mic Pre-amp Kit)
The following items included in the above kit list are also available separately, but are not shown in the 1986 catalogue:
Low-Z Mic Pre-amp PCB **Order As GD34M**
Low-Z Mic Pre-amp Case **Order As FD20W**
Mic Transformer 600/20 **Order As FD23A**
Constructor's Guide **Order As XH79L**
A ready-built version of this Kit is available:
Order As YM14Q (Low-Z Mic Pre-amp Assem)

MAPLIN SERVICE

With most electronic projects, performance will depend on the conditions of use. Recommendations and suggestions made in the articles in this magazine are for guidance only, since conditions of use are beyond our control.

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Our 'Get-You-Working Service' is available for any of the projects published in this magazine, *provided* they are constructed on our ready-etched printed circuit boards, and that they use a majority of components supplied by us. We regret we *cannot* extend this service to the 'interest' circuits, for which we do not provide ready-made boards, or supply as projects or kits; nor for projects or kits that have been *customised or modified by the constructor.*

We cannot enter into correspondence with regards to fault-finding, and recommend you return the unit to us for servicing if you are unable to rectify the fault yourself.

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If the problem has been caused by a faulty component supplied by us, then there will be no charge for the work performed or the components used. If the fault has been caused by error(s) in

construction, then there will be a charge for the work performed at a rate of £10 per hour, or part of an hour plus the cost of any damaged components which need to be replaced. If *no fault* is found on the unit, then there will still be a charge of £10 per hour or part of an hour *for the time involved in establishing this fact.*

Projects returned for repair should be addressed to:–
Service Department
Maplin Electronic Supplies Ltd
P.O. Box 3
Rayleigh
Essex
SS6 8LR

originating from the optical fibre itself, in addition to self-generated noise – therefore buffering amplifier TR3 is coupled by C2 and R6, which filter out much of the lower frequency noise signals. IC1 is a schmitt trigger-NAND package used for 'cleaning up' the pre-amplified carrier signal, and the supply for this and IC2 is separated from the main supply rail by reversed supply protection diode D1 and C5.

The carrier square wave is made available at TP2, which is also one of the Phase Locked Loop's phase comparator inputs. The comparator output controls a voltage controlled oscillator, via R14 and C7 which filter out harmonics and maintain a 90° phase shift at the VCO centre frequency. VCO timing components are C6, R13 and RV1. With no carrier signal applied to the receiver input, the VCO is free running at 110kHz; this frequency can be varied by RV1. The VCO square wave output from pin 4 feeds back to a second phase comparator input at pin 3.

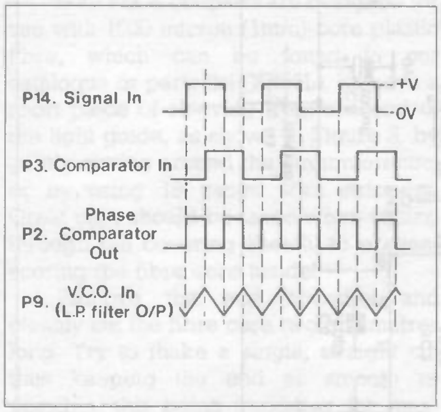


Figure 6. Waveforms.

With a 110kHz carrier signal present on Pin 14, a digital error signal is output to the filter and VCO input Pin 9 (Figure 6). Signals well outside of the carrier frequency do not produce the error signal, and the loop (VCO-comparator) does not 'lock on'. The values of R14 and C7, therefore, are important and determine the loop capture range and bandwidth.

The low pass filter output is taken from Pin 10, which is a buffered output from Pin 9. R15 serves the internal FET buffer source load and R16, C9 form a first stage filter for the audio and carrier output. A further two stages of low pass and high pass filters are necessary to reconstitute the audio waveforms and remove much of the 110kHz carrier signal. TR4 amplifies the filtered signal and TR5, emitter follower, buffers the signal for a low impedance output at Pin 4.

Transmitter Construction

For information regarding component identification, assembly methods and soldering, please refer to the 'Constructors Guide' supplied with this kit (if you do not intend to purchase the complete kit then see the Parts List for the order code of the Constructor's Guide, price 25p). Begin construction by referring to Figure 7 and inserting seven vero pins, pins 1 to 4 and TP1 to 3. Pin 2 (0V – PSU) should be soldered to both side 1 and side 2 of the pcb in order to connect the screening earth plane on both sides. Referring to Figure 8, mount the emitter coupler MF0E71 on side 2.

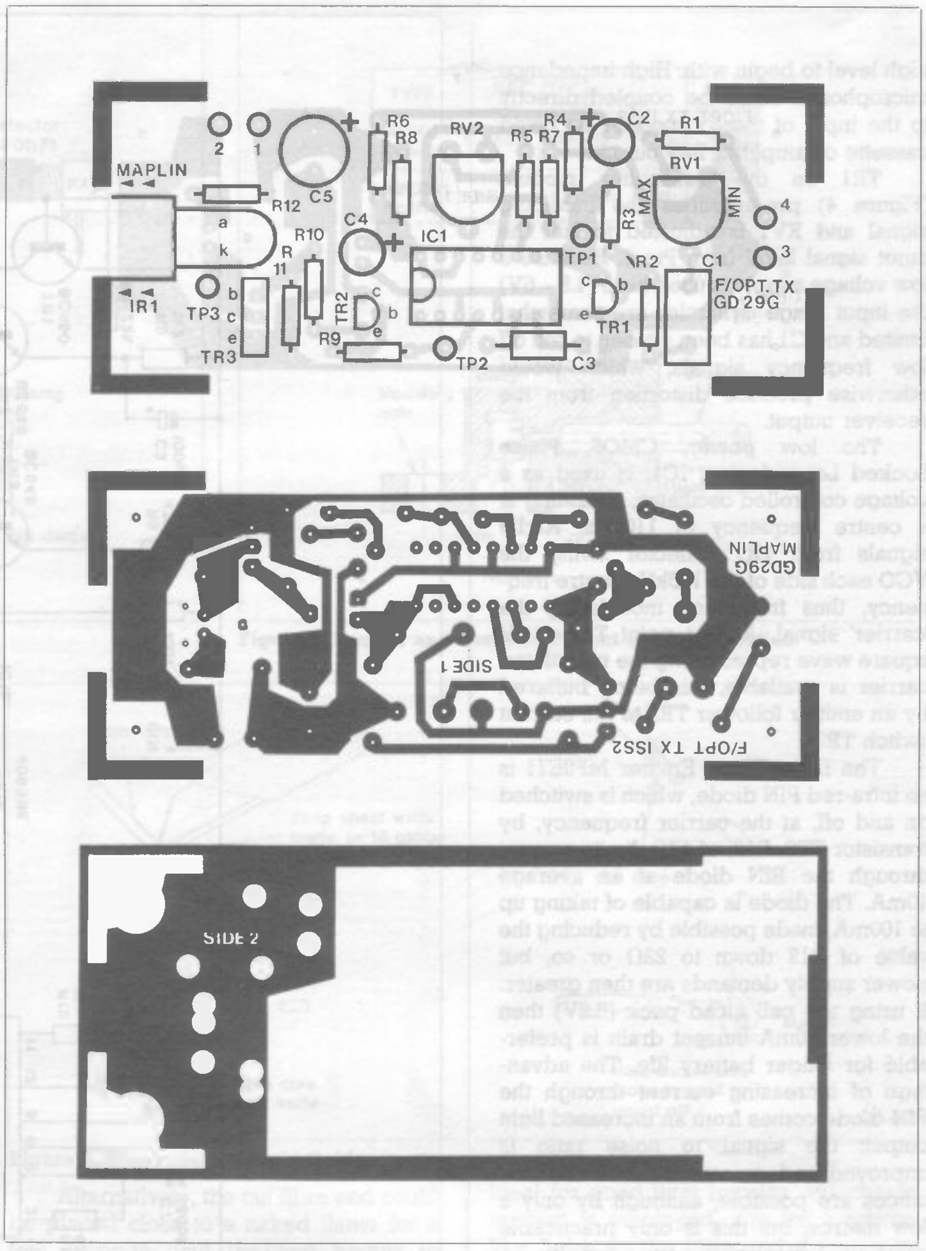


Figure 7. Transmitter Track and Legend.

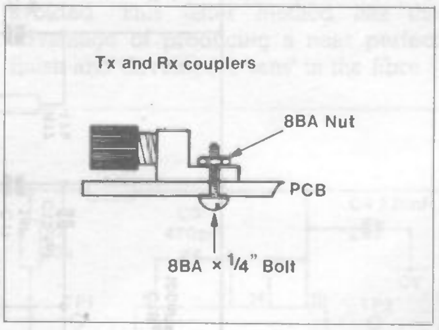


Figure 8. Coupler Mounting.

Ensure both terminal leads pass completely through the pcb and both locating pegs enter their holes. Insert an 8BA x ¼in bolt through the tab provided and tighten down with an 8BA nut. *Do not* overtighten, as excessive force is not necessary and the plastic body may be damaged.

Refer to Figure 9 and fit power transistor TR3 (BD139). This device must be fitted correctly, with the metal heatsink mounting surface facing toward TP3 and the front edge of the pcb. Push all three leads down into the holes leaving a clearance of 3mm between pcb and the base of the package of TR3. Solder all these five leads in place and cut off excess ends.

Now identify and insert resistors R1 to R12, and capacitors C1 to C5. When fitting C1, take care not to damage the leads on each end of the device, as they are very easily broken off. Note polarity markings on electrolytic and tantalum capacitors and insert correctly (consult the Constructor's Guide if in difficulty). Solder these components and again, remove excess wire ends.

Mount the 16-pin IC socket and TR1, TR2. Bend a few legs of the socket over beneath the pcb to prevent it from falling out. Mount RV1 and RV2 – note that their values are not identical so be sure to put the correct value in the required position – finally solder all remaining component leads, remove excess wire ends and clean the pcb tracks, before inserting the P.L.L. device, IC1.

Transmitter Testing

A few checks can be made at this stage to ensure that the transmitter module is operating properly. Connect a 5V power source to Pin 2 (0V) and +Ve via a milliammeter to Pin 1. Set the wiper of RV2 to approximately half travel, and turn on the power source.

A current reading of approximately 30 to 40mA should be obtained. Any readings well outside of this may well point to a fault, unless the test meter is not connected properly or the wrong range selected; double check and repeat the procedure. If the error is genuine and a frequency counter or oscilloscope is available, connect either to test point TP2. Adjust RV2 for 110kHz, which will be some 45° displacement of the wiper of RV2 from its central position. The output stage can be monitored with a 'scope on

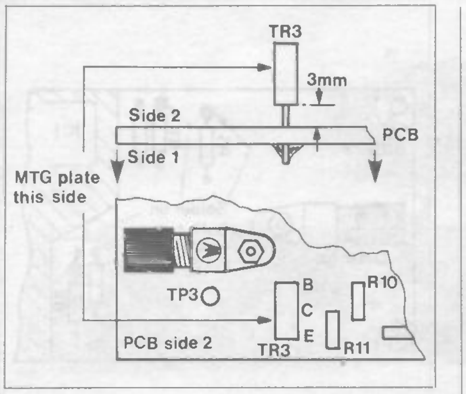


Figure 9. Mounting TR3.

TP3, where a 9μs square wave of 3.25V amplitude is present. The lower edge of the square wave will be approximately 0.7V above 0V, and the upper edge at +4V.

If this waveform is not present and the VCO *is* running, then it is possible that the actual infra-red coupler devices could have been mixed up! Both devices look the same, except for an identification code printed along one side of the body housing – if it turns out to be the wrong device then swop it for the other and repeat the testing procedure.

With testing completed switch off the power source and continue with the Receiver.

Receiver Construction

In similar fashion to the transmitter module, refer to Figure 10 and insert 7 vero pins in the holes marked with white rings, and mount the infra-red detector coupler, as Figure 8. Identify and insert resistors R1 to R26, then solder their leads on side 1 of the pcb. Three of these resistors, R5, R9 and R11, additionally have one of their leads soldered on side 2, the component side, of the pcb, see Figure 11. Do not omit this as it extends the earth plane to 0V.

Insert diode D1, taking care *not* to damage the glass case, and semiconductors TR1 to TR5. TR2, TR3 and TR5 are identical devices and look similar to TR1, but *must not* be mixed as TR1 has a different leadout configuration. TR4 has a silver, metal case with a marker tab against the emitter lead; push these devices down to within 3mm clearance between pcb and base of the package.

Next, fit capacitors C1 to C16, noting polarity markings on electrolytic types.

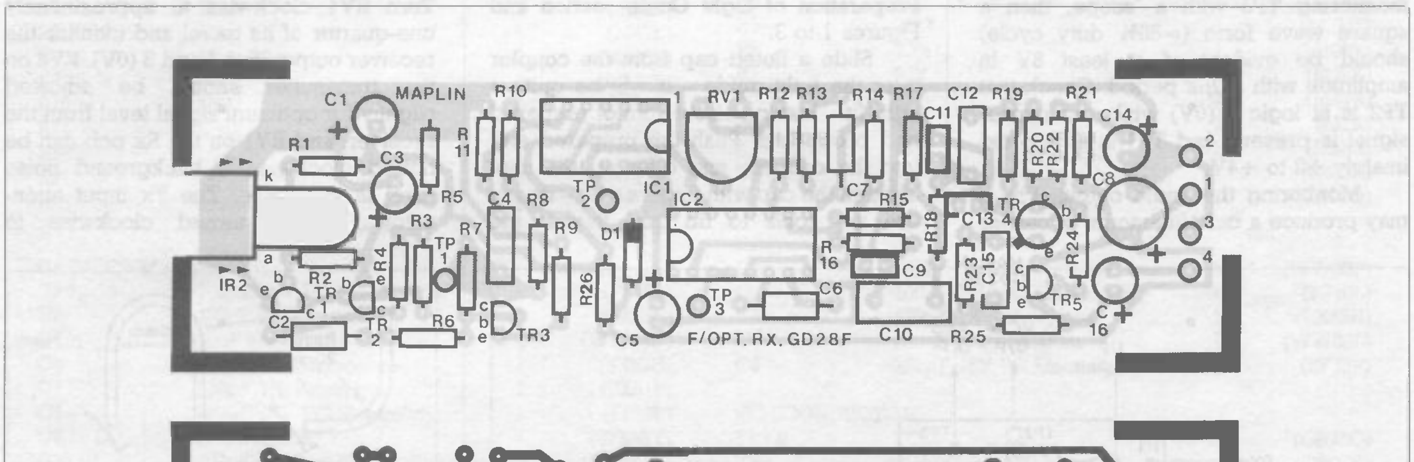


Figure 10. Receiver Track and Legend.

Poly-layer capacitors should be handled carefully to avoid their leads breaking off, as this is easily done.

Mount preset RV1 and a 14-pin IC socket at IC1 position, and 16-pin socket at IC2 position. Solder all components and leads and remove excess wire ends before inserting IC1 and IC2 into their sockets.

A careful inspection of all resistors and track areas is advisable at this stage, and cleaning side 1 of the pcb is recommended.

Receiver Testing

Basic checks and adjustments can now be made on the receiver module. Connect a 9V power source with 0V to Pin 2 and +V via a milliammeter to Pin 1. A PP6 9V battery pack is useful for this. Set the wiper of RV1 to approximately half travel, and turn on the power source.

A current reading of 7 to 9mA should be obtained. With a frequency counter or oscilloscope, monitor the test point TP3, and adjust RV1 for a frequency of approximately 110kHz. The exact setting is not that critical, since the PLL will lock onto the transmitter signal (once detected) and pull the VCO within range. If monitoring TP3 with a 'scope, then a square wave form (≃50% duty cycle) should be evident of at least 8V in amplitude with a 9μs period. Check that TP2 is at logic 0 (0V) whilst no carrier signal is present, and TP1 is at approximately +2 to +4V.

Monitoring the audio output, Pin 4, may produce a certain amount of carrier

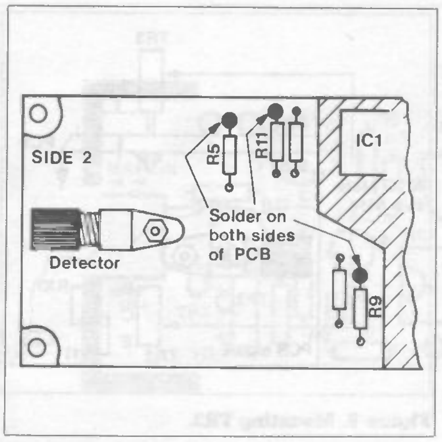


Figure 11. Some resistors are soldered both sides.

'breakthrough' signal (at 110kHz) which can be reduced by turning RV1 clockwise. The signal is present due to a lack of input carrier to the receiver and is removed when the PLL locks onto the incoming signal. Remove the 9V test power source.

Connecting the System

Figure 12 details both modules and should be referred to for the following. If the Fibre Optic Light Guide has not yet been prepared, then refer back to the Preparation of Light Guide section and Figures 1 to 3.

Slide a fluted cap from the coupler over the light guide – it will be quite a tight fit – leaving about 1cm of prepared end protruding. Push the prepared end into the coupler, and offer up the cap. Tighten the cap with fingers only – do *not* use any tools to do this! Repeat the procedure on the opposite end so that both Tx and Rx modules are secured to the light guide. It must be emphasised that careful preparation of the light guide core end is of vital importance if maximum range is required. Poorly prepared ends will produce noisy Rx output and may well limit useable cable length to below 10 metres or less!

When installing fibre optic light guide in a permanent position, be careful with bends, see Figure 13. The absolute minimum *radius* of any bend in the fibre should not be less than 20mm. Exceeding this limit will result in cracking of the fibre, which will completely refract light and result in zero throughput. If using clips to hold the guide in position, be careful not to pinch or damage the outer sheath in any way. Light will escape and/or enter from pierced sheathing and again poor results are inevitable. Excessive heat and some chemical solvents will also damage the guide and should be avoided.

Final Testing

Apply power sources to both modules and connect a suitable signal source to the transmitter input Pins 4 and 3 (0V). Turn RV1 clockwise to approximately one-quarter of its travel and monitor the receiver output Pins 4 and 3 (0V). RV2 on the transmitter should be adjusted slightly for optimum signal level from the receiver, and RV1 on the Rx pcb can be turned clockwise if background noise level is excessive. The Tx input attenuator can be turned clockwise to

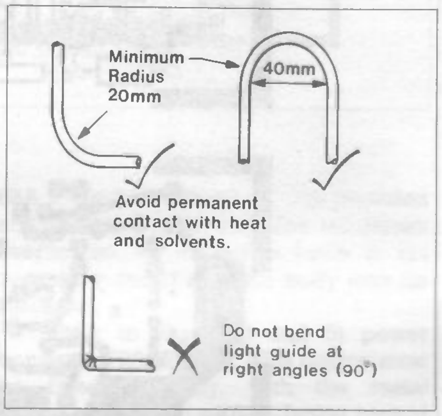


Figure 13. Bending the Light Guide.

increase the audio signal level through the system, but too high a level will produce a distorted audio output from the receiver.

Input signal levels to the transmitter should be kept as high as possible (at least 250mV to 500mV) for best signal to noise performance if using long (20 metre) lengths of light guide, although a fair amount of gain is available from the Tx input pre-amp.

Tests on the prototype produced quite good results using a Hi-Fi cassette player line output as the signal source, and the line/Aux input of a Hi-Fi tuner amp for the output of the receiver, with approximately 500mV average signal

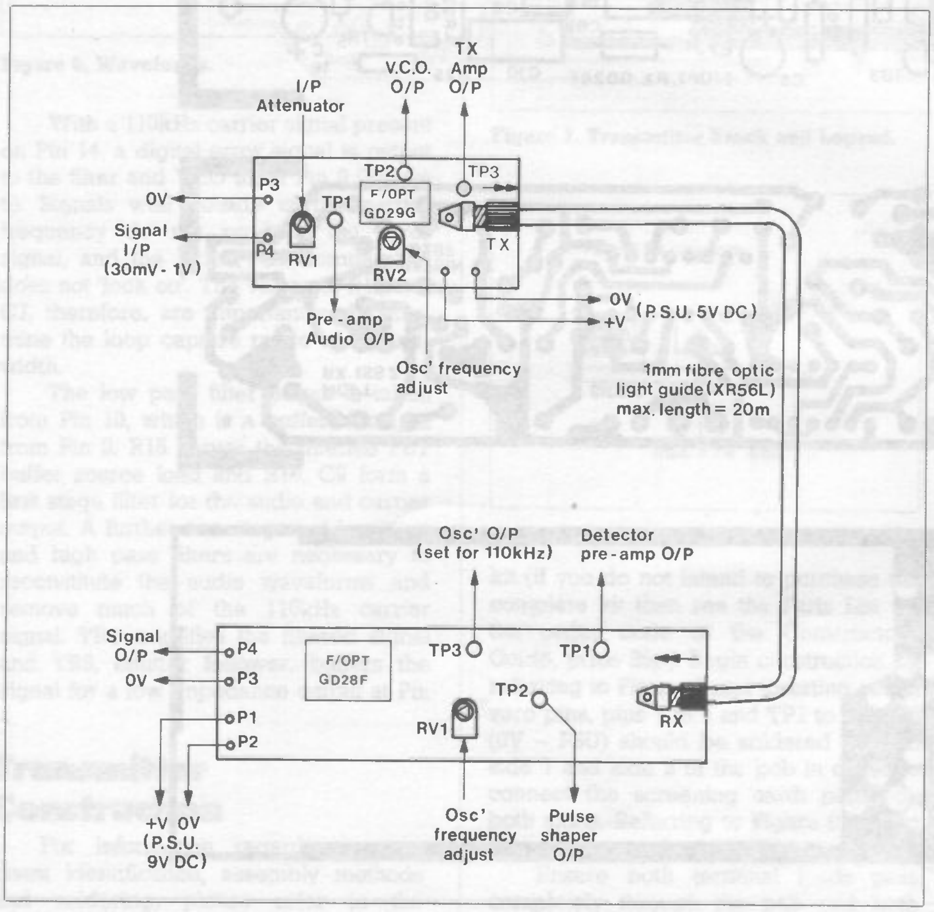
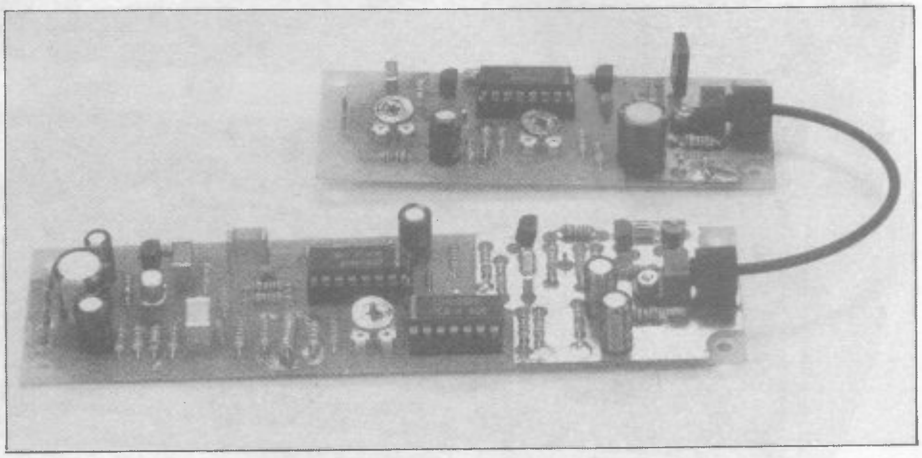


Figure 12. Connecting up the System.

level applied. Very low frequency transients are limited by the input stage filtering, middle and upper ranges are reproduced very well.

The modules are not designed to Hi-Fi standards, but as a fairly low cost introduction to fibre optics for personal and educational uses. Really useful practical applications would be in communications through environments plagued with electrical noise and powerful electro-magnetic fields to which conventionally carried screened signals cannot remain immune. Much scope exists for the enthusiast to improve on the basic system. For example, an audio compressor could be used to limit and average-out applied signals to the transmitter. The pre-amp gain could then be increased for better signal to noise performance, especially if an expander is used at the receiver output.



Another application could include computer data transmission. The system bandwidth will not allow very high baud rates, but this could be improved on by removing much of the receiver output filtering components as required, and is a matter for some further experimentation by the enthusiast.

FIBRE OPTIC LINK Rx PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,2	22k	2	(M22K)
R3,8,12,15,16,24	10k	6	(M10K)
R4,22	4k7	2	(M4K7)
R5	1k2	1	(M1K2)
R6,13,17,19	47k	4	(M47K)
R7,20	470k	2	(M470K)
R9,23,25	470Ω	3	(M470R)
R10,11	100k	2	(M100K)
R14	43k	1	(M43K)
R18	15k	1	(M15K)
R21	1k	1	(M1K)
R26	100Ω	1	(M100R)
RV1	47k Hor S-min Preset	1	(WR60Q)
CAPACITORS			
C1,3,5,14	100µF 10V PC Electrolytic	4	(FF10L)
C2	100pF Polystyrene	1	(BX28F)
C4	10nF Polylayer	1	(WW29G)
C6	470pF 1% Polystyrene	1	(BX53H)
C7	330pF 1% Polystyrene	1	(BX51F)
C8	220µF 16V PC Electrolytic	1	(FF13P)
C9,11,13	1nF Ceramic	3	(WX68Y)
C10,15	100nF Polylayer	2	(WW41U)
C12	470nF Polylayer	1	(WW49D)
C16	10µF 50V PC Electrolytic	1	(FF04E)
SEMICONDUCTORS			
D1	1N4148	1	(QL80B)
TR1	BC650	1	(QB74R)
TR2,3,5	BC548	3	(QB73Q)
TR4	BC109C	1	(QB33L)
IC1	4093BE	1	(QW53H)
IC2	4046BE	1	(QW32K)
IR2	F/Optic Detector MFOD71	1	(FD12N)
MISCELLANEOUS			
	F/Optic Rx PCB	1	(GD28F)
	Veropins 2145	1 Pkt	(FL24B)
	DIL Socket 14-pin	1	(BL18U)
	DIL Socket 16-pin	1	(BL19V)
	8BA x ¼in Bolt	1 Pkt	(BF08J)
	8BA Nut	1 Pkt	(BF19V)

A complete kit of all parts is available for this project:
Order As LM11M (Fibre Optic Rx Kit)
The following items in the above kit list are also available separately, but are not shown in the 1986 catalogue:
Fibre Optic Detector MFOD71 **Order As FD12N**
Fibre Optic Rx PCB **Order As GD28F**

FIBRE OPTIC LINK Tx PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,4,5	10k	3	(M10K)
R2	47k	1	(M47K)
R3	2M2	1	(M2M2)
R6	100Ω	1	(M100R)
R7	22k	1	(M22K)
R8,12	47Ω	2	(M47R)
R9,11	1k	2	(M1K)
R10	2k2	1	(M2K2)
RV1	100k Hor S-min Preset	1	(WR61R)
RV2	47k Hor S-min Preset	1	(WR60Q)
CAPACITORS			
C1	39nF Polylayer	1	(WW36P)
C2	100µF 10V PC Electrolytic	1	(FF10L)
C3	470pF 1% Polystyrene	1	(BX53H)
C4	220nF 35V Tantalum	1	(WW56L)
C5	220µF 16V PC Electrolytic	1	(FF13P)
SEMICONDUCTORS			
TR1,2	BC548	2	(QB73Q)
TR3	BD139	1	(QF07H)
IR1	F/Optic Emitter MFOE71	1	(FD14Q)
IC1	4046BE	1	(QW32K)
MISCELLANEOUS			
	F/Optic Tx PCB	1	(GD29G)
	DIL Socket 16-pin	1	(BL19V)
	Veropins 2145	1 Pkt	(FL24B)
	8BA x ¼in Bolt	1 Pkt	(BF08J)
	8BA Nut	1 Pkt	(BF19V)
	Constructor's Guide	1	(XH79L)
OPTIONAL			
	F/Optic Light Guide	As req	(XR56L)

A complete kit of all parts, excluding optional item, is available for this project:
Order As LM12N (Fibre Optic Tx Kit)
The following items included in the above kit list are also available separately, but are not shown in the 1986 catalogue:
Fibre Optic Emitter MFOE71 **Order As FD14Q**
Fibre Optic Tx PCB **Order As GD29G**
Constructor's Guide **Order As XH79L**

- ★ Full 8-bit Digital Output
- ★ Picture Slip Control
- ★ Black and White Level Controls
- ★ Input Level Meter
- ★ Peak White and Black Indicators
- ★ Optional Line Sync Card
- ★ Sync Timing for TIROS Satellites Provided
- ★ Programmable Sync Cards for Other Satellites
- ★ Built-in Power Unit (Also Supplies Receiver)

SATELLITE DECODER

by Robert Kirsch Part 2

The Decoder

This article describes the Decoder needed to demodulate the APT (Automatic Picture Transmission) signals transmitted from most of the orbiting and geostationary weather satellites. These signals can be received using the Receiver described in Part 1 of this series.

The Decoder accepts audio signals either from tape or directly from the receiver and converts them into an 8-bit digital format with necessary synchronising pulses for connection to a suitable computer or frame store for display on a television or monitor. Controls are provided to enable the contrast of the picture to be adjusted and various types of synchronisation may be selected to suit different satellites. Power for the decoder comes from an internal power unit which will also supply the receiver.

The APT Format

Pictures transmitted by most VHF American and Russian orbiting weather satellites, as well as WEFAX transmissions from the GOES series satellites (e.g. ESA METEOSAT 2), use the APT format. The radio frequency carrier is frequency modulated by a 2.4kHz subcarrier whose amplitude is modulated by the picture information and synchronising signals. Figure 1 shows the subcarrier envelope for a typical line of APT information.

Peak white, it will be noted, corresponds to maximum subcarrier level, and black to the minimum. Picture lines are transmitted either 2 or 4 times a second, each line having 600 cycles of subcarrier, thus the maximum horizontal definition is 600 pixels. The TIROS satellites send alternate lines of infra-red and visible information (when viewing the Earth in daylight) each line being preceded by synchronising pulses. Channel 1 (visible) sends 7 pulses at 1040 pulses per second and channel 2 (infra-red) sends 7 pulses at 832 pulses per second. Meteosat sends 7 pulses at 840 pulses per second at the start of every line, as well as a 300 pulses per second start and a 450 pulses per second stop signal for frame synchronisation.

Decoder with the Receiver

The Russian Meteor satellites send approximately 2 lines per second with a synchronising tone of 300Hz for every line. The decoder described in this article produces line synchronising pulses by dividing the 2.4kHz subcarrier digitally, using a programmable divider to obtain the correct periods for various types of satellites. These pulses may be manually adjusted to correctly position the picture on the screen. (When using the optional sync tone decoder card this is achieved automatically.)

Circuit Description

Figure 2 shows a block diagram of the decoder, synchronising unit and power supply. Figure 3 shows the circuit diagram for the main circuit board. Live or recorded signals, selected by the receiver, enter via the 6-pin DIN socket and are first fed to a master level control. The signal at this point splits into three paths; the first goes to the A/D converter, the second to the Level Meter and AM detector circuit, and the third to the Phase Locked Loop carrier regeneration circuit.

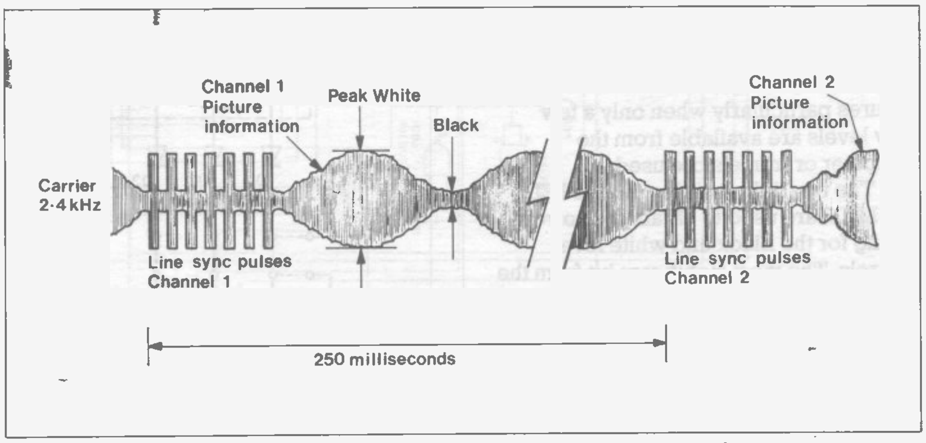


Figure 1. Typical APT information.

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