

Low-price robots from POWERTRAN - hydraulically powered - microprocessor controlled

The UK-designed and manufactured range of Genesis general purpose robots provides a first-rate introduction to robotics for both education and industry. With prices from as low as £425, even the home enthusiast can aspire to his or her own robot.

Each robot in the Genesis range has a self-contained hydraulic power source operated from single phase 240 or 120v AC or from a 12v DC supply. Up to six independent

axes are capable of simultaneous operation and all except the grip axis have sensing devices fitted to provide positional control by a closed loop system based on a dedicated microprocessor. Movement sequences can be programmed by means of a hand-held controller or the systems can be interfaced with an external computer via a standard RS232C link.

The top-of-the-range P102 has dual speed control, enhanced memory and double acting cylinders for increased torque on the wrist and arm joints. There is position interrogation via the RS232C interface, increasing the versatility of computer control and inputs are provided for machine tool interfacing.

All Genesis robots are available either ready-built or in kit form. The latter provides not only

GENESIS

P102

extra economy but also valuable additional training as an assembly project.



For under £100, Hebot II takes programming off the VDU and into the reai world. Each wheel is independently controlled by a computer, enabling the robot to perform an almost infinite number of moves. It has blinking eyes, a two-tone bleep and a solenoid-operated pen to chart its moves. Touch sensors, coupled to its shell return data about its environment to the computer enabling evasive or exploratory action to be calculated.

The robot connects directly to an I/O port or, via the interface board, to the expansion bus of a ZX81 or other microcomputer.

HEBOT II

GENESIS

GENESIS

P101

S101



A real, programmable robot for under £200! Micrograsp has an articulated arm jointed at shoulder, elbow and wrist positions. The entire arm rotates about its base and there is a motor driven gripper. All five axes are motor driven and four of these are servo controlled giving positive positioning. The robot can be controlled by any microcomputer with an expansion bus – the Sinclair ZX81 being particularly suitable.

MICROGRASP

Weight 8.7kg, max. lif	ting	board kit	£48.50
capacity 100g	0	23 way edge conne	
Robot kit with power supply	£145.00	AX81 peripheral/R splitter board	AM pack £3.00

GENESIS S101

Weight 29kg, max. lifting capacity 1.5kg 4-axis model (kit form) **£425** 5-axis model (kît form) 5-axis complete system (kit form) £737

GENESIS P101

Weight 34kg, max lifting capacity 1.8kg 6-axis model (kit form) 6-axis complete system (kit form) \$2945 GENESIS P102

Weight 36kg, max lifting capacity 2kg 6-axis system (kit form) £113

£1175.00

r interface

Powertran Cortex microcomputer self-assembly kit £



cybernetics Ita





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OUR APRIL ISSUE WILL BE ON SALE FRIDAY, MARCH 2nd, 1984

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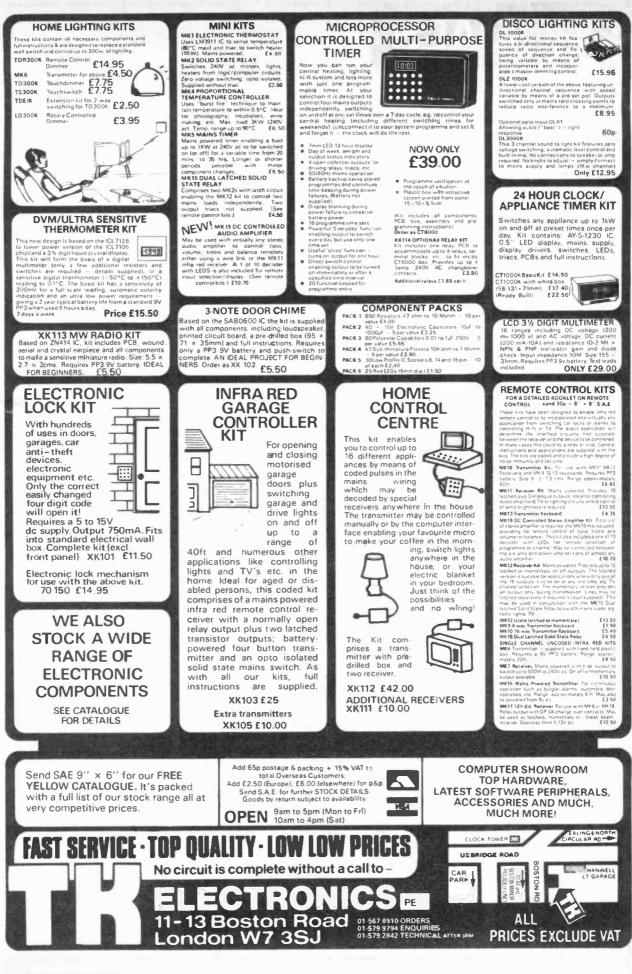
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220n 10p; 330n, 470n 15p; 680n 19p; 1µ 23p; 1µ5 40p; 2µ2 46p; ELECTROLYTIC, CAPACITORS (Values in µF), 500V; 10µF 52p; 4 9p; 10 10p; 15, 22 12p; 33 15p; 47 12p; 68 16p; 100 19p; 220 26 17p; 220 24p; 40V; 68 15p; 22 9p; 33 12p; 330, 470 32p; 100 100 11p; 150 12p; 220 15p; 330 22p; 470 25p; 680, 1000 34 92p; 16V; 25, 40 8p; 47, 68, 100 9p; 125 12p; 220 13p; 330 16p	778p; 63V:047,10,15,22,33,8p;47 ;100070p;220099p; 50V:6820p;100 45p;22090p; 25V:47,10,22,478p; ;150042p;22050p; 50p;330076p;4700	BC109 12 BD1 BC109B 14 BD1 BC109C 14 BD1 BC147B 9 BD2 BC147B 10 BD6 BC148C 10 BD6 BC149 9 BT1	38/9 40 40 40 45 45 95A 150 96A 150 94/5 12	MPSU06 55 MPSU52 65 MPSU55 60 MPSU56 60 OC23 170 OC28/36 220 OC41/42 75	ZTX109 12 ZTX212 28 ZTX300 13 ZTX301/2 16 ZTX303 25 ZTX304 17 ZTX320/26 30	-2N3820 38 2N3822/3 45 2N3866 90 2N3903/4 15 2N3906/5 15 2N4906/5 15 2N4859 78	2SJ85 225 3N128 112 3N140 112 40251 150 40311 60 40313 130 40361/62 70
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3300, 4700 60p each 11p; 220n 13p; 330n 18p; 470n 23p;680n 30p;1µF34p;2µ250p.	RESISTORS Hi-stab, Miniature, 5% Carbon. RANGE Val. 1-99 100+ 0 25W 202-4-M7 E24 3p 1p	BC213L 10 BFY BC214 10 BFY BC214L 10 BRY	36 32 '90 80 '39 40	TIP35C 128 TIP36A 130 TIP36C 140 TIP41A 50	2N1613 30 2N1671B 160 2N2160 295 2N2219A/20A/	2SC1162 30 2SC1172 125 2SC1173 125	WE DO THE REST. 0923 50234
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80, 0 3W, 2"; 2-25", 2-5", OPTO CRY	STAL PLAYS VOLTAGE REGULATO	SOCK		BEEBFONT ROM
0 3W, 2.5° 40Ω; 64Ω or 80Ω TL211 Green 3mm 14 4 dig	git 495 5V 7805 40p 79 git 530 12V 7812 40p 79	12 45p 16 pin	tob web	This is a character FONT ROM that gives you 5 16×16 predefined FONT. The ROM is ideal for high quality demonstration on screen and when
DIODES AA119 15 RECTIFIERS 02" Yel, Grn, Amber 14 BPX	25 250 24V 7818 40p 79	18 45p 20 pin 22 pin	20p 60p 22p 65p	used in conjunction with EPSON printer, allows printing of letters etc. in mixed type faces. The
AAY30 15 1A/50V 18 two part clip. R. G & Y 45 BPX BA100 15 1A/100V 20 Rectangl. Stackable IL74	65 320 5V 78L05 30p 79 65 6V 78L62 30p	L05 50p 28 pin - 40 pin	20p 80p	package is complete, including an Editor to de- sign your own Fonts and several spare Fonts
BAX13 20 1A/400V 25 LEDS BY100 24 1A/600V 34 Triangular LEDs R&G 18 ILO7 BY106 12 2A/60V 34 Criangular LEDs R&G 56 ILC7	4 115 8V 78L82 30p 4 220 12V 78L12 30p 79	12 500	LSOCKET	which could not be fitted in the ROM can still be run from RAM. Supplied complete with ROM, software on DISC/tape and Manual. Price £45
BY127 14 2A/200V 40 0-2* Bi colour LEDs Isola CR033 250 2A/400V 46 Red/Green 65 TL1	tor 135 11 70 KCL7660 248 LM317M	250 28 way	750p	
0A47 12 6A/100V 83 02" Tri colour LEDs ORP 0A70 12 6A/600V 126 Red/Green/Yellow 85 2N5"	12 78 78H12 12V/5A 640 LM323k 777 50 78HG +5 to LM3371	500 175 DIL	PLUGS (Headers)	IDC CONNECTORS (Speed block type) PCB Male Female Female with latch Header Card-Edge
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OA90 8 25A/600V 396 LD2/1 Infra Red (emit) 46 Recc OA91 8 BY164 56 TIL32 Infra Red (emit) 52 OP1 OA96 9 K440 56 SFH205 (detector) 118 OP1	Elver 715 LM309K 120 RC4195	160 24 28 40	88p 138p 185p 290p 195p 218p	10 way 90p 99p 85p 120p 16 way 130p 150p 110p 195p 20 way 145p 166p 125p 240p
0A200 8 0A202 8 ZENERS TIL 78 (detector) 55 SWI TIL 78 (detector) 55 SWI TIL 78 (detector) 55 Refu TIL 78 (detector) 50 Refu	TCH SWITCHES active 39 225 SLIDE 250V TOGGI		N CABLE (price per foot)	26 way 175p 200p 150p 320p 34 way 205p 236p 169p 340p 40 way 220p 250p 190p 420p
1N916 5 39V 400mW 7 Segment Displays to R	S 186 1A DPDT 14 SPST 1A DPDT C/OFF 15 DPDT	35 Ways 48 10	Grey Colour 15p 28p 25p 40p	50 way 235p 270p 200p 470p
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1N5401 15 1N5404 16 VARICAPS 3 Green C.A. 140 5x2	x2' 105 Latching or SPST o 1x1'' 90 Momentary 6A SPDT o		60p £5p 70p 90p 100p 135p	DIN 41612 2×32 way 275p 320p 220p 285p DIN 41612 2-3×32 way 295p 340p 240p 300p
1N5408 19 BA102 30 Bargraph 10 seg. Red 250 5x4 1S44 9 BB105B 40 Bargraph NSM3914 500 5x4	x 2i 130 SPDT c/over 110 SPDT B x 1i 99 DPDT c/over 160 DPDT 6 x 2i 120 DPDT c/over 160 DPDT 6	iased 105 tags 75 'D' CO	NNECTORS:	DIN 41612 3×32 way 360p 385p 260p 395p TRANSFORMERS (mains Prim. 220-240V) 3-0-3V, 6-0-6V 100mA; 9-0-9V 75mA;
15921 9 88106 40 FERRIC CHLORIDE 6×4 6×4000 40 TRIACE	×2 120 MINIATURE DPDT of ×3 150 Non Locking DPDT 6	n/on/on 185 Pins iased 145	9 15 25 way way way	37 30-30,
6A/800V 65 3A/100V 48 195p + 50p p&p 10x 3A/400V 56 195p + 50p p&p 10x		Solder Angle	150n 210o 250o	240p 12VA: 2x4V5-1-3A; 2x6V-1-2A; 2x12V-5A; 355p 2x15V-4A 345p (35p p&p)
SCR's 8A/100V 60 DALO ETCH RESIST 12x SCR's 8A/400V 69 Pen plus spare tip 100p 12x	5x3* 260 ROTARY: {Adjustable Stop 8x3* 295 1 pole/2 to 12 way, 2p/2 to 6 v 2 to 4 way, 4 pole/2 to 3 way		E	310p 24VA: 6V-15A 6V-15A; 9V-12A 9V-12A; 12V-1A 12V-1A; 15-8A 15-8A: 20V-6A 20V-6A 285p (60p p&p) 338p 50VA 2x6V-4A 2x9V-25A 2x12V-2A 2x15V-
08A-100V 32 12A/100V 78 COPPER CLAD BOARDS 5A/300V 38 12A/400V 82 Fibre Single Double	SRBP 9-5" x8-5"	Angle	165p 215p 290p	440p 1-5A; 2×20V-1-2A; 2×25V-2A; 2×30V-0.8A 420p 520p (60p p&p)
5A/600V 48 I6A/100V 103 6"×6" 100p 125p 8A/300V 80 16A/400V 105 6"×12" 175p 225p	110p DIP SWITCHES: (SPST) 4 wa 6 way 80p; 8 way 87p; 10 wa (SPDT) 4 way 190p.	y 100p;		90p 100VA: 2×12V-4A; 2×15V-3A; 2×20V-2·5A; 2×30V-1·5A; 2×40V-1·25A; 2×50V-1A 965p (60p p&p)
BA/600V 95 16A/800V 220 12A/100V 78 25A/400V 185 VEROBOARDS 0.1" 12A/400V 95 25A/800V 295 Clad Plain 'VO' Board	180	DC 25	way Pig. 385p, Skt. 450	DIL Plug (Headers)
12A/800V 188 25A/1000V 21×31 ^a 85-95 DIP Board BT106 150 30A/400V 525 31×31 ^a 100-110 Vero Strip BT116 180 30A/400V 525 31×31 ^a 100-110 Vero Strip	144 24 way IEEE 475p	Solder 450p 485p SIL	EDGE CONNECT	24" 145n 165n 240n 325n
C106D 38 T2800D 120 31×5° 115-125 95p PROTO-D TIC44 24 Strong 275p Veroblock TIC45 29 SOLDERCON 41×18° 495p - S-Dec	405 395 ASTEC LINE MODILI ATOPS	•osp Socke 0.1" 20 way	2×23 way 170p	6" 185p 205p 300p 465p
TiC47 35 PINS Pit. of 100 pins 55p Eurobread 2N5064 38 100 75p Spot Face Cutter 150p Binboard Spot Face Cutter 150p Binboard Spot Face Cutter 150p Spo	695 6MHz Standard	325p 85p 450p 32 way 95p	2×30 way 245p	24" > 210p 235p 345p 540p 36" > 230p 250p 375p 595p
DIAC VERO WIRING PEN and Spool Spare Wire (Spool) 75p; Co	350p Telephone orders by Access mbs 6p ea. phone your order through 092		2×36 way 295g 2×40 way 315g 2×43 way 395g 2×75 way 550g	10C FEMALE NECEPTACLE Jumper Leads 36 20pin 26pin 34pin 40pin 1 end 160p 200p 260p 300p
Wire Wrapping Stakes 100	250p we do the rest.	COVETALS	-	2 ends 290p 370p 480p 525p
COMPUTER CORNER	BROTHER HR-15	CRYSTALS	DDC	MICROCOMPLITER
SEIKOSHA GP100A – Unihammer Printer, nor-	DAISEY-WHEEL PRINTER/	32-768KHz 10 100KHz 23 200KHz 26	Model A £299:	MICROCOMPUTER Model B £399 (incl. VAT). We stock the
 SEIKOSHA GP100A – Unihammer Printer, nor- mal & double width characters, dot resolution graphics 10" Tractor feed, parallel interface stan- 	DAISEY-WHEEL PRINTER/ An exceptionally high quali Daisy Wheel printer at the prio	32-768KHz 10 100KHz 23 200KHz 26 455KHz 37 1MHz 27 1008M 27	Model A £299; full range of Bi ware like, Disc	, Model B £399 (incl. VAT). We stock the 8C Micro peripherals, Hardware & Soft- Drives (Top quality Cumana & Mitsubi-
SEIKOSHA GP100A – Unihammer Printer, nor- mal & double width characters, dot resolution graphics 10" Tractor feed, parallel interface stan- dard. FREE 500 Sheets £155 SEIKOSHA GP 250X Printer £199	DAISEY-WHEEL PRINTER/ An exceptionally high quali Daisy Wheel printer at the pric of a Dot matrix printer. 18CPS Bi-directional, has 3K of Buffe	32-768KHz 10 100KHz 23 200KHz 26 455KHz 37 1-008M 27 1-008M 27 1-50MHz 39 1-5MHz 42 1-6MHz 42	Model A £299 ; full range of Bi ware like, Disc shi), Diskettes, Dust Covers, C	Model B £399 (incl. VAT). We stock the C Micro peripherals, Hardware & Soft- Drives (Top quality Cumana & Mitsubi- Printers, Printer Paper, Interface Cable, assette Recorder & Cassettes, Monitors,
 SEIKOSHA GP100A – Unihammer Printer, normal & double width characters, dot resolution graphics 10' Tractor feed, parallel interface standard. FREE 500 Sheets SEIKOSHA GP 250X Printer EPSON FX80 PRINTER 160 CPS, 11×9 matrix, proportional spacing, superscript, subscript, dot 	DAISEY-WHEEL PRINTER/ An exceptionally high quali Daisy Wheel printer at the prio of a Dot matrix printer. 18CPB Bi-directional, has 3K of Buffe has clear buffer facility, Carriag skip movement, Proportion	32-768KHz 10 100KHz 23 200KHz 26 200KHz 26 200KHz 27 11MHz 27 5, 128MHz 39 6, 15MHz 39 6, 16MHz 39 16, 18432M 20 2, 20MHz 22	Model A £299 full range of Bi ware like, Disc shi), Diskettes, Dust Covers, C Connectors (Re- ter (Graphic Ta	Model B £399 (incl. VAT). We stock the C Micro peripherals, Hardware & Soft- Drives (Top quality Cumana & Mitsubi- Printers, Printer Paper, Interface Cable, assette Recorder & Cassettes, Monitors, ady made Cables, Plugs & Sockets), Plot- blet) EPROM Programmer, Lightpen Kit,
 SEIKOSHA GP100A – Unihammer Printer, normal & double width characters, dot resolution graphics 10" Tractor feed, parallel interface standard. FREE 500 Sheets £155 SEIKOSHA GP 250X Printer £199 EPSON FX80 PRINTER 160 CPS, 11×9 matrix, proportional spacing, superscript, subscript, dot addressable graphics, Normal, Italic & Elite characters. Up to 256 user definable characters. Down 	DAISEY-WHEEL PRINTER/ An exceptionally high quali Daisy Wheel printer at the priv of a Dot matrix printer. 18CPS Bi-directional, has 3K of Buffe has clear buffer facility, Carriag skip movement, Proportion, spacing; underlining; Bold priv and Shadow print, Prints in tw	32-768KHz 10 100KHz 23 200KHz 27 455KHz 37 200KHz 37 455KHz 37 200KHz 37 27 1008M 27 5, 128MHz 39 7, 15MHz 42 207 1 15MHz 39 6 1.8M32M 20 20MHz 22 200Hz 20 200Hz 20 20 200Hz 20 20 200Hz 20 200Hz 20 20 200Hz 20 20 200Hz 20 20 200Hz 20 20 200Hz 20 20 200Hz 20 20 200Hz 20 20 200Hz 20 20 200Hz 20 20 20 20 20 20 20 20 20 20 20 20 20 2	Model A £299, full range of Bi ware like, Disc shi), Diskettes, Dust Covers, C Connectors (Re, ter (Graphic Ta Joysticks, Sid Machinecode R	Model B £399 (incl. VAT). We stock the C Micro peripherals, Hardware & Soft- Drives (Top quality Cumana & Mitsubi- Printers, Printer Paper, Interface Cable, assette Recorder & Cassettes, Monitors, ady made Cables, Plugs & Sockets), Plot- blet) EPROM Programmer, Lightpen Kit, eways ROM Board, EPROM Eraşer, OM, The highly sophisticated Watford's
 SEIKOSHA GP100A – Unihammer Printer, normal & double width characters, dot resolution graphics 10' Tractor feed, parallel interface standard. FREE 500 Sheets £155 SEIKOSHA GP 250X Printer £199 EPSON FX80 PRINTER 160 CPS, 11×9 matrix, proportional spacing, superscript, subscript, dot addressable graphics, Normal, Italic & Elite characters. Up to 256 user definable characters. Down loadable character set. Condensed and double width printing. 4 user define margin positions. 	DAISEY-WHEEL PRINTER/ An exceptionally high quali Daisy Wheel printer at the price of a Dot matrix printer. 18CPS Bi-directional, has 3K of Buffe has clear buffer facility, Carriag skip movement, Proportion spacing; underlining; Bold pri- and Shadow print. Prints in two colours; Super and subscript fi cility. Impact control facility to	32 758KHz 10 100KHz 23 200KHz 23 200KHz 37 455KHz 37 114Hz 27 200KHz 26 100Hz 27 15MHz 42 15MHz 42 15MHz 42 16MHz 39 41 1432MHz 29 20MHz 20 20MHz 22 255250M 22 32768M 15 0 357954M 30 0	Model A £299 full range of Bi ware like, Disc shi), Diskettes, Dust Covers, C Connectors (Re- ter (Graphic Ta Joysticks, Sid Machinecode R 16K BEEB DFS, cational Applica	Model B £399 (incl. VAT). We stock the BC Micro peripherals, Hardware & Soft- Drives (Top quality Cumana & Mitsubi- Printers, Printer Paper, Interface Cable, assette Recorder & Cassettes, Monitors, ady made Cables, Plugs & Sockets), Plot- blet) EPROM Programmer, Lightpen Kit, eways ROM Board, EPROM Eraser, IOM, The highly sophisticated Watford's WORDWISE, BEEBCALC, Software (Edu- tion & Games), BOOKS, etc. etc. Please
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and no tone controls are common



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and all this is really quite sad, as the £26.50 + £2.00 | TV companies do their best to transmit the highest quality sound. Given this background a compact and Independent TV tuner that connects direct to your Hi-Fi is a must for quality reproduction. The unit is mains-operated

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BRITAIN'S FUTURE

DOES Britain have an independent future in high technology? Has £50m of public money assured the UK of its own chip maker? Will the Transputer put the UK ahead of the world in electronics?

There are no single word answers to these questions but the answers could be vital to the future UK economy. Just recently the name of Inmos has been hitting the headlines again for a number of reasons not the least being their need to find more finance and the resulting talks with GEC and other companies----names like Philips, SGS, Fujitsu and Western Electric have also been reported. Inmos was the subject of much press comment back in '79 and '80 when the 'new' Government hesitated about providing its second £25m.

In the October 1980 issue of PE Nexus wrote the following words "As I write there is still no decision on Inmos an ominous sign reflecting lack of enthusiasm for, if not imminent abandonment of, Government (i.e. taxpayers) support". Within a week or two of that being written the Government (i.e. taxpayers) did cough up and Inmos was away, albeit after losing a valuable six months waiting for a decision. Over the last three years Inmos has quietly built a reputation in the industry for technical excellence and has proved its ability to process high volume chips at Newport; surely it would be madness to let it slip into foreigh ownership now.

Sir Clive Sinclair recently predicted that a "wall of secrecy" will soon be built around high tech. research and he went on to add "Either we get ourselves back into the hardware business or we're out of the game".

Sir Clive suggested that hardware and software would be so closely related that to ensure our ability to stay in the field, and not be reliant on foreign manufacturers, we must develop both. He stressed the "very serious implications" if Inmos was allowed to be bought by a non-UK company.

With this background PE has commissioned Tom Ivall to look at Inmos and its first five years. The article does not provide straightforward answers to the above questions but it gives clear indications of where the UK chip maker is now, how it got there and where it might go in the near future.

TRANSPUTER

The future of Inmos is closely tied up with the Transputer so in order to round off the scene we also commissioned Ray Coles (who writes Micro-File) to take an in depth look at this exciting device. The Transputer article will be published next month in place of Micro-File.

These two articles should interest anyone involved in electronics at any level, because of the implications outlined above, make sure you read them.

Incidentally Sir Clive is not slow in developing new products—see *News* and *Market Place* for details of his new computer.

Nike Kenoche

Technical and Editorial queries and letters

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Copies of most of our recent issues are available from: Post Sales Department (Practical Electronics), IPC Magazines Ltd., Lavington House, 25 Lavington Street, London SE1 OPF, at £1 each including Inland/Overseas p&p. Please state month and year of issue required.

Binders for PE are available from the same address as back numbers at £5-50 each to UK or overseas addresses, including postage, packing and VAT where appropriate. State year and volume required. Items mentioned are available through normal retail outlets, unless otherwise specified. Prices correct at time of going to press.

SINCLAIR'S QUANTUM LEAP

You are probably going to see the computer shown here a great deal over the next few years. It's Sinclair's new QL (Quantum Leap, would you believe) the name is perhaps OTT but then so is the computer. Based on the Motorola 68 008 32 bit chip the QL has 128K of usable RAM (up to 32K can be required from a screen bit map) extendable up to 640K, and 32K of ROM extendable up to 64K containing a new "Sinclair Super BASIC" and Sinclair QDOS operating system.

The unit has a full size "proper" keyboard, two 100K microdrives built-in and sockets for microdrive extension (up to six extra drives), local area network, RGB monitor port, u.h.f. tv port, two standard RS-232-C sockets, two joysticks sockets, ROM cartridges slot and expansion slot for extra memory or peripherals.



Planned enhancements under development are: PASCAL compiler, 68000 assembler, terminal emulator, 0.5mb memory expansion, A to D converter, Winchester interface, modem, parallel printer interface and IEEE-488 interface.

Super BASIC is said to be a radical enhancement of Spectrum BASIC, and QDOS is a new Sinclair development which allows single-user multiple tasking, time sliced priority job scheduler, display handling for multiple screen windows and device-independent I/O.

The QL comes complete with an extensive manual in an A4 ring binder, a 1.8A

RT-VC CHANGE

One of PE's oldest advertisers have just reopened their original Acton premises as an Electronics Discount Centre. RT-VC have used the premises as a mail order operation for many years with shop sales from their Edgware Road address.

The Edgware Road shop remains unaltered while 21 High Street, Acton, is now open for trading and carries a wide range of consumer electronics including telephones, watches, calculators, speakers and record decks plus the well known RT-VC kits and modules. The latter include the PE Stereo Cassette Recorder and a VHF Stereo Tuner that were published in PE in conjunction with RT-VC.

RT-VC have always been known for their low price products and these are now readily available in Acton High St. They are of course continuing their mail order operation from the same address. power supply, a suite of four software programs on microdrive cartridges and four blank cartridges. The software supplied has been developed by Psion and is claimed to "completely out perform existing software for micros" it comprises QL Abacus for spreadsheet analysis, Archive or database management, Easel for graphics and Quill for word processing. All are said to be immediately usable and very advanced, so much so that it is claimed "you probabfy won't refer to the manual"!

All this is provided for £399 including VAT; by mail order only at present. Other things that may be of interest are: The 68008 runs at 7.5MHz and a second processor (Intel 8049) controls keyboard, sound, RS-232-C receive and real time clock functions.

FOOD FOR THOUGHT

B REVES

It is unlikely that Ocean Software have bitten off more than they can chew with 'Mr Wimpey', a new game for the 48K Spectrum, indeed it looks like a recipe for success.

The game involves a culinary concoction of ingredient pinching nasties who constantly hamper the player's attempts to assemble hamburgers. The program also incorporates the company logo and jingle.

Even if this first UK company commissioned program does not go down well the business principle behind it certainly will. In the USA company sponsored programs are already big business, the advantages are obvious if the games climb high in the popularity charts. This will certainly be the first of many such attempts by companies to cash in on the infinite commercial possibilities within the home computer market. Interesting variations spring to mind, who knows what Andrex could come up with.

'Mr Wimpey' is written in 100% machine code and has hi-res graphics and sound. It can be snapped up from leading stores for around £5.90 and will shortly be available for the Commodore 64K.

MULTI-FUNCTION KEYBOARD

The Concept keyboard is a new approach to educational computing, allowing easier pupil-computer integration.

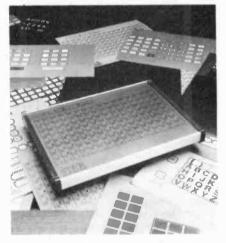
The Concept keyboard takes interchangeable A4-size overlays which define the number, shape, size, colour, position and legending of the keys. Each program can use a separate overlay, with keys appropriate to the application. The ability to respond directly to programmed questions, via keys labelled 'Yes', 'No', 'True', 'False' for example, greatly improves pupils' interaction with the computer.

The keys can be made large enough to allow operation by visually or physically handicapped pupils.

The flat pressure-sensitive keyboard also gives great flexibility in designing teaching programs. A program to teach shopping skills, for example, could use a model trolley and an overlay showing the floor-plan of a supermarket with the various aisles and counters.

The Concept keyboard can be used with any microcomputer. It is of value in any educational application and special education where the normal QWERTY keyboard presents operating difficulties.

The keyboard has an 8×16 matrix of touch-sensitive areas, each producing a unique 7-bit ASCII code which the programmer defines as required. A bleeper with on/off con-



trol, and two additional user-dedicated touch pads, are also provided.

The price of the Concept keyboard (£91.00 ex VAT) includes full documentation and, for educational applications, a connecting lead for the majority of micros and a set of demonstration software.

Star Microterminals Limitd, 22 Hyde Street, Winchester, Hampshire, SO23 7DR. (0962) 51422.

MARGE BLACE **Silicon News Corner** PICO-POWER

Probably the smallest power supply of its type available is the Picopac range from Rastra Electronics; these 1W mains packages would certainly fit into the proverbial matchbox.

The supplies feature small physical size (43.2 × 25.4 × 21.5mm) coupled with high reliability. Modules are available with inputs at 115/220V a.c. 50/60/400Hz and with single or dual outputs. Single outputs range from 5V to 24V d.c. the dual output type being ±15V d.c. Since the units feature series regulation, the residual ripple is well under 1mV.

Despite the tiny size of these units the manufacturers claim an impressive 2kV a.c. isolation for 1 minute between primary and secondary. The Picopac is encapsulated and is intended for p.c.b. mounting. Prices however are not quite so small at £26 for the single and £42 for the dual output version, exc VAT. Details from Rastra Electronics Ltd, 275-281 King Street, Hammersmith, London W6 9NF (01-748 3143/2960).



Zilog (Exxon) introduces 12MHz version of entire Z8 micro family. Zilog (UK) Ltd., Zilog House, Moorbridge Rd., Maidenhead, Berks SL6 8PL

Omron - Flat mini-sized relay uses "seesaw" system which is free from contact bounce and highly shock resistant. IMO Precision Controls, 1000 North Circular Rd., Staples Corner, London NW2.

IMS1400M high performance 16K static RAM. 70ns CE access, 165mW standby power (660mW active). Single supply (5V). I/O is TTL compatible. Inmos, Whitefriars, Lewins Meads, Bristol BS1 2NP.

An electronic potato has been developed by the Scottish Institute of Agricultural Engineering in an attempt to reduce damage during mechanical processing.

The potato-a direct descendant of a similarly pseudo raspberry from the same stable uses an Entran accelerometer to gather information about the forces acting upon it during its automated journey. A v.h.f. transmitter sends out data from the foam potato to remote recording equipment.

It is hoped that the present day loss of over 10 per cent of the nation's maincrop will be reduced using data gleaned from this unlikely 'spudnik'.

CTS101AGB is a high performance, general purpose op. amp. High gain, s/c protected, excellent temp. stability and simplified compensation.

CTS0002GB buffer amp., high speed, high impedance follower.

CTS00081B hybrid, high voltage, high current driver, TTL/DTL to 3A (pulsed) drive.

Inmos MIMS2600 high performance 64K ×1 dynamic RAM. 100ns access, 22mW standby power (303W active). Single supply (5V) with on-chip refresh. I/O is TTL compatible. Bit & nibble mode capability.

Got any bright ideas? Unemployed? Live in London? The GLC are spending £40 million on a scheme to make University and Polytechnic equipment and know-how available to the public. Ideas can be brought to the prototype stage using the scheme which already has a list of new ideas including medical systems and a robot arm. It is hoped that jobs may ultimately be created to fill up some of the 33 million square feet of idle factory space in the capital.

Sixty of the world's top CMOS experts agree that Ultra Large Scale Integration will, within five years, allow chips with one billion transistors on them, to go into production. How this will be achieved is shrouded in some mystery, but Alan Aitken, of Mitel, has stated that ULSI is already possible, the only thing holding up production he said is the investment required to adapt existing aquipment.



Please check dates before setting out, as we cannot guarantee the accuracy of the information presented below. Note: some exhibitions may be trade only. If you are organising any electrical/electronics, radio or scientific event, big or small, we shall be glad to include it here. Address details to Mike Abbott.

Barclays Techmart Feb. 21-25. NEC, B/ham. J4 Electrex Feb. 27-March 2. NEC, B/ham. L3 Hybrid Microtech Feb. 28. Cunard Int. Hotel, London. R2

Scotest March 6-8. Anderson Exhibition Cntr., Glasgow. T Scottish Sensors March 6-8. Anderson Ex. Cntr., Glasgow. T Home Appliances International March 12-15. NEC, B/ham, M Computer Trade Show March 13-15. Wemb. Conf. Cntr. Z1 Business Telecom March 13-15. Barbican Cntr., London. O Visit to Firefly Electric Vehicles (Milton Keynes). March 17. R1 Electro-Optics/Laser Int. March 20-22. Metropole, Brighton. T1 Information Technology (Conf. & Ex.) March 20-22. London. \$ 01-828 2333

Scottish Computer Show March '84. Holiday Inn, Glasgow. T1 Fibre Optics May 1-3. Porter Tun Room, Whitbread Brewery. E All Electronics /ECIF May 1-3. Barbican, London. E Biotech Europe May 15-17. Wembley Conf. Cntr., London. O Micro City May 15-17. Exhibition Complex, Bristol. F3 Scotelex June 5-7. Royal Highland Exhibition Halls, Ingliston, Edinburgh. 05 IBM System User Show June 12-14. Wembley Conf. Cntr., London. O Qualex June 19-21. Corn Exchange, Brighton. D4 Surface Treatment & Finishing Show June 25-29. Birmingham. M Networks July 3-5. Wembley Conf. Cntr., London. O Cable July 10-12. Wembley Conf. Cntr., London. O Testmex Sept. 11-13. Grosvenor Ho. Pk. Lane, London. E Building & Home Improvement Sept. 25-30. Earls Court, London. M

- Network & 0280 815226 D4
- Evan Steadman & 0799 26699 E
- F3 Tomorrow's World & 0272 292156
- NEC & 021 780 4141 14
- L3 Electrex Ltd. C 0483 222888
- Montbuild @ 01-486 1951 Μ
- Institute of Electronics & 0706 43661 05
- **R1** Battery Vehicle Association. & Brian Hampton, 0908 316991
- **R2** \$ 08956 32476 Т
 - Trident & 0822 4671
- T1 Cahners @ 0483 38085
- **Z**1 IPC C 01-643 8040

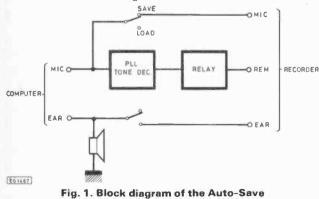
Spectrum MITO-SAVE R.A.Penfold

HE popular Sinclair ZX Spectrum computer has a quite fast and efficient cassette interface, but it can be a little awkward to use. One reason for this is that problems can arise if the "Ear" and "Mic" sockets of the computer are both connected to their respective sockets on the cassette recorder, and for satisfactory results it is usually necessary to only connect the lead that is actually being used. Another problem is the lack of any automatic control of the cassette motor when loading and saving. This is not really too important when loading since the computer will continue to search until the program is found, giving the user unlimited time to load the cassette into the recorder and run it through to the beginning of the appropriate program. On the other hand, when saving a program it is very much easier if the cassette and recorder can be set up ready to record, and the computer will then automatically start the recorder, record the program, and switch the recorder off again.

SIMPLE AUTO SWITCH

The problem of having to unplug one lead and plug in the other, every time a change is made from loading to saving (or vice versa), is easily overcome by using a switch to disconnect whichever of the leads is not required. A simple way of providing an auto-save facility would be to have a switch which would activate the cassette motor when an output from the "Mic" socket of the recorder was detected. There would obviously be some slight delay between the start of an output from the computer and the recorder beginning to record properly, but the Spectrum precedes all data with a tone leader (to operate the auto recording level of the recorder), and in practice this system gives no loss of data.

This auto-save unit uses what is basically the system outlined above, as can be seen from the block diagram of the unit which is shown in Fig. 1.



A two pole switch is used to connect either the "Mic" lead or the "Ear" lead, depending on the mode of operation selected. A set of relay contacts control the cassette motor via the "Rem" (remote) socket of the recorder, and a third pole on the save/load switch is used to place a short circuit on the "Rem" output when the unit is in the "load" mode and the auto switching is inoperative. This also enables the recorder to be used in the fast forward and rewind modes without having to unplug the remote lead.

Although it might, on the face of it, appear that using a simple amplifier, rectifier, smoothing circuit, and relay driver would give satisfactory results and activate the relay in the presence of an output signal, in practice things are slightly less straightforward. The problem stems from the fact that signals other than the "save" signal are fed to the "Mic" socket. These come from the computer's sound generator, and apart from the signal produced by BEEP commands there is also the signal generated each time a key is operated.

The problem is largely overcome by using a phase locked loop tone decoder to drive the relay. This does not respond to the short bursts of keyboard tone even if a number of them follow in rapid succession. It will respond to any signals within its narrow lock range that are caused by BEEP



instructions, but this can be overcome by avoiding this small range of frequencies, and in practice the tape recorder would normally be switched off anyway when a program is running. It would therefore be irrelevant even if a spurious operation of the unit did occur.

It can be very helpful to monitor the output of the recorder when loading programs as it is then immediately obvious if a program is being fed into the computer but is failing to load, or if some other loading problem occurs. A loudspeaker is therefore used to monitor the signal being fed into the computer.

THE CIRCUIT

It will be apparent from the circuit diagram of Fig. 2 that the unit uses few components and has a very simple circuit.

IC1 is an NE567 PLL tone decoder, and as this requires an input signal of only about 20 millivolts r.m.s. no preamplification is required. However, as there is normally a very low input impedance at the microphone input of a cassette recorder, R1 is added in series with the output to the recorder to prevent loading from reducing the signal to an inadequate level. Of course, losses through R1 substantially reduce the signal level reaching the "Mic" input of the recorder, but in practice the signal level still seems to be far higher than the minimum acceptable level.

The timing components for the oscillator in the PLL are VR1, R2 and C2. The Spectrum has a nominal tone leader frequency of 800 hertz, and VR1 is adjusted for an 800 hertz centre frequency.

A switching action is used to detect whether or not the oscillator has locked on to the same frequency as that of the incoming signal. Basically, all that happens is the oscillator operates an electronic switch and the input signal is fed through this switch. If the two signals are at the same frequency the switch cuts off negative half cycles but allows positive ones to pass. This rectified signal is smoothed and used to drive an internal non switching transistor. C4 is the smoothing capacitor and the collector of the switching transistor connects to pin 8 of the NE567. C3 is the capacitor in the lowpass filter of the PLL, incidentally.

If the input signal and the oscillator are at different fre-

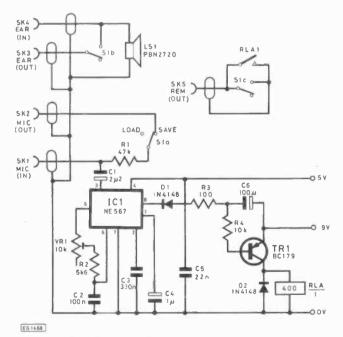


Fig. 2. Circuit diagram of the Auto-Save

quencies the two signals will have a constantly changing phase relationship so that the electronic switch passes a mixture of positive and negative signals. This gives zero average voltage across C4 and the output transistor is not switched on.

The output transistor is activated continuously when the 800 hertz tone leader is present, but when data is being saved the output tone is modulated and the output transistor is pulsed on intermittently. The output of IC1 is therefore used to drive a smoothing circuit which has a fast attack and a long decay of about 4 seconds, and this drives discrete switching transistor TR1 which in turn drives the relay. This system prevents the relay from cutting out while a program is being saved and gives good reliability. A relay is better than some form of electronic switching in this application since the relay contacts are totally isolated from the rest of the circuit. With some tape recorders neither side of the REM socket is at earth potential. Also, using a relay there is no significant voltage drop through the switch.

LS1 is the loudspeaker which monitors the signal entering the computer during load operations. This is actually a ceramic resonator rather than a normal loudspeaker, and although it only provides limited volume, it is adequate in this respect. In fact, higher volume would be unnecessary and undesirable in this application.

S1 is the switch which connects the "Ear" or "Mic" lead, as appropriate, and places a short circuit across the "Rem" socket when the unit is set in the "load" mode. Power for the circuit is obtained from the OV, 5V and 9V rails of the Spectrum edge connector.

LUIVIPUIN	IENTS
Resistors	
R1	47k
R2	5k6
R3	100
R 4	10k
All resistors	W 5% carbon film
Potentiomet	er
VR1	10k 0.1W horizontal preset
Capacitors	
C1	2µ2 63V radial electrolytic
C2	100n polyester
C3	330n polyester
C4	1µ 63V radial electrolytic
C5	22n ceramic plate
C6	100µ 10V radial electrolytic
Semiconduc	
D1, D2	1N4148 (2 off)
TR1	BC179
101	NE567
Miscellaneou	
51	4 way 3 pole rotary (with end stop)
LS1	PBN2720 ceramic resonator
SK1, 2, 3, 4	
SK5	2.5mm jack socket
RLA	12 volt 400 coil, s.p.s.t. contacts, min PCM
	(Maplin) Printed circuit board 3-1 x 1-6in.
	Metal box 133 x 70 x 38mm
	28 way Spectrum edge connector
	(Watford or Technomatic)
	Wire, fixings, etc.

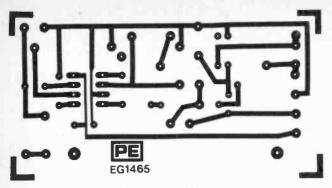


Fig. 3. P.c.b. design

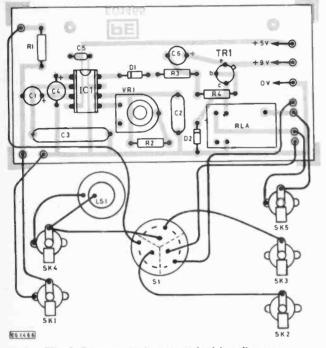


Fig. 4. Component layout and wiring diagram

CONSTRUCTION

The printed circuit board design is shown in Fig. 3, with the component layout and wiring diagram shown in Fig. 4. If a different form of construction is used, note that supply



PET 2001 8K RAM (expandable) with integral monitor and cassette deck £200 o.n.o. Tel: Lytham (0253) 737397. D. R. Worley, 14 Mythop Ave., Lytham, Lancs.

CASIO FX31 scientific cal. Book-wallet-price £6-00. Holdway, Flat 20, Studland Close, Millbrook, Southampton.

OLIVETTI PR 1350 DOT Matrix printer with reference and service manuals. £130 o.n.o. Swop twin beam — scope. D. Bevan, 17 Beaufort Rd, Kingswood, Bristol. Tel: (0272) 616936.

WANTED any service information on G.E.C. TERMINET 300 Printer. Will pay. Tel: 01-651 4885. A. G. Seagrave, 175 Sorrel Bank, Linton Glade, Forestdale, Croydon CR0 9LZ.

CCTV Camera B/W early Crofton kit model complete and working full manuals v.g.c. £70 with lens. D. Russell, 9 South Beach Road, Ardrossan, Ayrshire, KA22 8AX. Tel: (0294) 64144. WANTED Smart 2-update Nov. 1980 assembly instructions, especially page 7 system layout—one sheet copy only. Claessens Guido, Oversneslaan 51-2610 Wilryk, Belgium. Tel: 03-828 2314.

VOCODER, best of ETIs—Elektors, sensible offers, or exchange for colour computer plus accessories (value £200). J. Logsdon, Top Flat, 13 Bowmans Road, Dartford, Kent DA1 3QP.

PE 'Orion' amp, new Sanyo speakers, McDonald 610 turntable, small tuner, v.g. stereo sound £15 o.n.o. Mr. A. L. G. Senior, 22 Robinia Walk, Whitchurch, Bristol BS14 OSH. Tel: (0272) 830213.

WANTED manual for Tektronix scope type 545B. Will buy or borrow to copy, willing to pay. T. Measor, 5 Midlothian Road, Hartlepool, Cleveland TS25 3RH.

TELEQUIPMENT D61a dual trace oscilloscope with X10 probe and manual wanted. E. M. Jackson, Coombe Farm, Gidleigh, Chagford, Newton Abbot, Devon TQ13 8HP.

CLEF Microsynth. Fully built and housed. £125 o.n.o. Tel: (0272) 516304. B. Wiltshire, 7 South Hayes, Eastville, Bristol.



decoupling capacitor C5 should be fitted close to IC1 or instability is almost certain to occur. S1 is a 4 way 3 pole rotary type having an adjustable end-stop which is set for 2 way operation.

Provided the specified relay is used it can be mounted on the printed circuit board, but if an alternative is used it will be necessary to modify the p.c.b. or mount the relay offboard. Any relay having at least one set of make contacts (or a set of changeover contacts), a coil resistance of about 300 ohms or more, and capable of operating from a 9 volt supply can be used in the unit.

The plain side of ceramic resonator LS1 is glued to the inside of the case at any convenient place using a good quality general purpose adhesive. This component does not have any tags or ready-connected leads, and soldered connections are made direct to the inner disc and outer ring. The connection to the inner disc should be completed fairly rapidly, to avoid damaging the component due to overheating.

As mentioned earlier, the "Rem" socket of the recorder may have neither terminal at earth potential, and if a metal case is used SK5 should be an insulated socket, or it should be insulated from the case. Alternatively, a plastic case could be used, but a wire to connect the earth tags of the other four sockets would then be needed.

The connection to the Spectrum edge connector is made via a 3 way cable, and an exit hole is drilled for this in oneside of the case. The edge connector is a 2 x 28 way type, and should preferably be a type having the Spectrum polarising "key". Refer to page 160 of the Spectrum manual for connection details of the edge connector.

VR1 must be given the correct setting before the finished unit will function properly, and a suitable setting is found by empirical means.

BREAKING, UK101. Cegmon Word Processor new basics 1, 3 & 4 assembler editor chips available. Tel: (0642) 484122. D. Doyle, 21 Skelton Drive, Marske-by-the-Sea, Redcar, Cleveland TS11 THN.

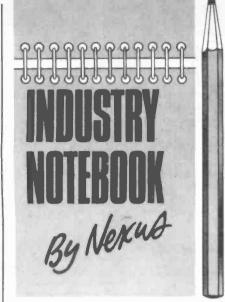
VALVES wanted, must be new and boxed. Also valve sockets and plugs, transformers, capacitors, tuners, amplifiers. N. Covington, 25 Ridge Road, Letchworth, Herts SG6 1PT. Tel: (04626) 79681.

MENTA, Z80 Microcomputer for control applications, including manual £75, five interface modules designed for Menta, s.a.e. Mr. D. H. Slater, rear of 25 New Market Street, Colne, Lancs B88 9BJ.

WANTED circuit diagram or service manual for ferograph series Seven Model 71SH. Bob Allen, 69 Callcott Road, Kilburn, London NW6

RS232 interface module with instruction booklet for Microline 80 printer. Unused. £25. Tel: Oxford (0865) 779855.

HELP1 Tandy 603043 Radio controlled Lamborghini—TX/RX Circuit and service info required. Chris Finn, 11 Alexandra Drive, Beverley, E. Yorks. Tel: (0482) 868899.



One World

We learn something new every day. For example that the greatest civil engineer of his time, Isambard Kingdom Brunel, was not as British as I had believed, his father having been French and the young Brunel educated in Paris. I learnt this from an IBM advertisement designed to convince us all that this huge multinational corporation, though not British in parentage, is at least as British as Brunel ever was because it practises its skills in Britain just as Brunel did in his time.

So what? The electrical and electronic sciences have always been international in character and, in fact, origin. Our own fundamental units of measurement, the Volt, Amp and Ohm are derived from the names of early Italian, French and German pioneers, the Farad from an Englishman.

The developments that led to radio are attributed to Maxwell, Hertz, Popoff and Marconi, respectively British, German, Russian and Italian. In television the inventor of the first camera tube, the iconoscope, was Zworykin who emigrated to the United States after the Russian revolution. Zworykin was building on earlier work such as the discovery of cathode rays by Crookes (British) and the invention of the cathode ray oscilloscope by Braun (German).

The scientific community has always believed in open publication of findings for the benefit of all. Not so the business community who guard their secrets, prudently patenting their products before disclosure.

But while protecting their products individually the electronics industry has always been a big sharer of ideas and even designs through cross licensing both within and across national boundaries whenever it is to mutual advantage. This sharing has accelerated in the age of solid state when it soon became apparent that secondsourcing was not giving a product away to a competitor but greatly expanding a market. Joint ventures are also common, a recent example being CMOS gate arrays designed in Britain by Smiths Industries' subsidiary Micro Circuit Engineering to be processed by ITT in establishments in the United States and Belgium.

One American company, Advanced Micro Devices, is trying to go beyond crosslicensing into co-operative R & D. AMD's president, Jerry Sanders, is clearly worried over his own company's 100 million dollar spend on R & D in a single year. He recently stated that he and other like-minded semiconductor manufacturers together with equipment manufacturers were contemplating joint formation of R & D organisations and then sharing the research results.

This idea has its parallel in governmentsponsored schemes for advancing technology. Whether a private enterprise R & D co-operative would be more effective or even workable is an open question. The most likely cash benefit is in the potential for reducing duplication in R & D activities among participating companies. On the other hand it can be argued that the intense competition in private enterprise to introduce exciting new products is the prime mover of technological advance.

The proof is clearly visible in a comparison of the competitive system of the West with the non-competitive Soviet Union. There is no reason to suppose Russian engineers to be dimmer or less numerous than those in the West and yet they continue to lag behind in almost every field with the possible exceptions of space exploration and armaments.

Let's get back to IBM and Brunel! I may be wrong but I have it as a dim memory that the founder of IBM was himself British, or of British parentage. But who cares in any serious way? My colour TV bears the label of a famous British company whose parent organisation is in the Netherlands where it was most probably designed. The receiver was assembled in Singapore from components manufactured in several other countries.

IBM's long awaited personal computer will proudly bear the IBM label. But its 'works', the p.c.bs, will be made by a British company unheard of by those not in the trade. I refer to AB Electronics whose shares gained over £1 on announcement of the IBM contract which, through IBM Greenock, will serve the computer markets in Europe, the Middle East and Africa. Electronics is truly international, one world, and I'm glad it's so. But I suspect that all of us still enjoy a patriotic glow on achievements by and in our own country.

Piracy

Joint ventures, cross-licensing and other mutually advantageous deals have proved their worth over many years through legal or even gentlemen's agreements arranged in a civilised way. In October 1983 I drew attention to look-alike personal computers flooding the market from the Far East and, in particular, the possibility of pirated software becoming an even greater menace.

My fears seem to have been fully justified with software houses claiming collective losses of tens of millions of pounds. Pirating goes right across the board from schoolboy amateurs to skilled computer crooks who can make a good living by selling pirated programs of the more expensive business types at about one tenth of the list price. Protective devices have so far proved ineffective and the copyright laws, as far as the UK is concerned, cover only literature, music and artistic content. New legislation is contemplated.

Lady Harrison

One of the least publicised activities of the Racal Group is services for oil exploration. These were inherited through Decca's earlier involvement in navigation and precise positioning systems and, since the acquisition of Decca by Racal, have been greatly expanded through the formation of Racal Energy Resources Ltd.

Last November Lady Harrison, wife of Racal chairman Sir Ernest Harrison, launched a new geophysical survey ship, the m.v. 'Lady Harrison'. The vessel was launched from the Bergen, Norway, shipyard where she was built. She entered service in January and will operate wherever required in the world and almost certainly in offshore China where Racal already operates joint venture companies with the China National Offshore Oil Corporation for positioning and survey work.

Needless to say the ship is stuffed full of electronics and her complement of 34 crew and scientists are all accommodated in single-berth air-conditioned cabins.

Cablesat

Whatever the merits of privatisation (the controversy is still very much alive) the mere prospect continues to galvanise British Telecom. On March 1st BT starts routeing, via Intelsat V, entertainment TV programmes to local cable networks.

The programmes come from United Cable Programmes, a consortium of British companies. They will be transmitted to London Telecom Tower and then on to the London Earth Station at North Woolwich where they will be transmitted to Intelsat V. The participating cable operators will each have their own small satellite dish aerials at their cable head-ends for reception and feed-in to their cable systems. The signals will travel 44,600 miles in space before arriving at their destination. It may sound a long way round but is clearly a more economical method than relaying the signals individually to cable companies whose networks are geographically widely spaced.

Another advanced project for BT is the first transatlantic fibre-optic cable. This has been talked about for a year or two but has now been firmed up as TAT-8 costing in all £225 million shared between British Telecom, AT & T Communications (US) and Submarcom (France).

A new innovation apart from the fibreoptic cable itself is the world's first underwater junction box where the main link divides with one branch to the UK landing point at Widemouth Bay, Cornwall, the other to Penmarche on the coast of Brittany.

SERICONDUCTOR CIRCUITS TOM GASKELL B.A. (Hons)

TACHOMETERS (LM 2917N–8 AND LM 2917N)

LTHOUGH the measurement of frequen-A cies and speeds often involves digital techniques, it is preferable in some cases to obtain a purely analogue representation of these parameters. Analogue displays can have advantages in resolution, readability under rapidly changing conditions, and simplicity. The LM 2917N-8 is an 8 pin 'tachometer', or frequency-to-voltage converter i.c. which is specifically designed for this type of application. The i.c. incorporates not only tachometer circuitry, but also extra general purpose facilities such as internal voltage regulation, a driver transistor for external loads, and an opamp with an uncommitted inverting input. This allows for considerable flexibility in use, and makes the device ideal for incorporation into many frequency or speed sensing and measuring systems. The LM 2917N is also available; this is a 14 pin version, with extra connections available to parts of the internal circuitry. It does not have input protection for negative voltages, unlike the LM 2917N-8, so be careful not to confuse the two! All diagrams will refer to the '-8' version, unless otherwise stated, although '-8' circuits are generally able to use the 14 pin i.c., with the necessary extra connections, bearing in mind that all-important input protection.

The pinout and specifications are given in Fig. 1, with block diagrams given in Fig. 2 and Fig. 3. A current limiting resistor must be provided for the internal 7.5V Zener diode, to limit the current to a maximum of 25mA. The minimum current should be 6mA (the maximum internal quiescent current). If this Zener diode is unacceptable, the LM 2907N-8 and LM 2907N are equivalent devices without it.

METHOD OF OPERATION

The input to the i.c. is a differential amplifier with hysteresis. (Hysteresis is the effect whereby the input passes through a threshold voltage in the positive going direction, then has to drop to a somewhat lower, or more negative, voltage in the negative going direction before the output will turn off. It helps to prevent spurious oscillations at the exact point of changeover). In the '-8' device, the input is protected to ±28V, since the input must swing about OV, inferring an a.c. coupled input in most cases. Since it is possible to bias both inputs to the 14 pin i.c., this has no such protection, hence the earlier warning. Because of the very high gain of the input amplifier, and the absence of any negative feedback, the output is a square wave, the frequency of which is identical to the input signal.

The square wave signal causes the 'charge pump' circuit to charge, or discharge (as appropriate) the timing capacitor C_T between two internal voltage references which are half the Zener supply voltage apart. As a result, the average of the current pulses pumping into INPUT 1 0 0V INPUT 2 0 0V CARACITOR 2 INTEGRATOR 3 6 4-VE SUPPLY METHODR 3 6 0/P TRANSISTOR CO/P TRANSISTOR 5 0/P TRANSISTOR

Fig. 1. Pin out and specification (MIR) LM2917N-8

Characteristic	Notes	Min.	Typically	Max.	Units
Supply voltage	All spec's measured at +12V		+12	+28	V
Quiescent current			3.8	6	mA
Temperature range		-40		+85	°C
ZENER VOLTAGE					
REGULATOR					
Zener voltage	Measured at pin 6		7.56		V
Effective internal					
series resistance			10.5	15	Ω
Max. supply current	Fed into pin 6			25	mA
OP-AMP AND O/P					
TRANSISTOR				10	
Input offset voltage	Input voltage = $6V$		3	10	mV
Input bias current	Input voltage $= 6V$		50 200	500	nA V/mV
Voltage gain			200	(Zener	v/mv
Input common-mode voltage range		0		voltage	v
voltage range		0		-1.5	v
Output sink current	V_{ce} (sat) = 1.0V	40	50	-1.5)	mA
Output source current	$V_{ce}(sat) = 1.0V$ $V_{ce}(sat) = 2.0V$	40	10		mA
Saturation voltage	5mA collector current		0.1	0.5	v
Op-amp i/p voltage	(Also, collector voltage)	0		+28	v
I/P AMPLIFIER AND	(The concercit to hage)			120	
CHARGE PUMP					
I/p voltage				+28*	V V
I/p thresholds)	±10	±15	+40	mV
Hysteresis	l/p = 1kHz, 250mV p/p		+30		mV
Input offset voltage			5	15	mV
Input bias current	$I/p \text{ voltage} = \pm 50 \text{mV d.c.}$		0.1	1	μA
Linearity	I/p = 1 kHz to $10 kHz$	-1.0	0.3	+1.0	%
(Variation in correct o/p					
voltage, with respect to					
5kHz voltage)					

* 0-28V for the LM 2917N

C_T is given by:

average current = $V_z \times f_I \times C_T$

where $V_z = Zener$ voltage and $f_I = input$ frequency.

The output of the charge pump 'mirrors' an exactly equivalent current into the integration network C_1 and R_1 . The resistor acts as a load for the current mirror, and the capacitor smooths the pulsed waveform to provide a d.c. voltage at pin 3 (for LM 2917N-8) given by: voltage at pin 3 = $V_z \times f_1 \times C_T \times R_1$ In practice, due to i.c. tolerances, the d.c. voltage can vary from 0.9 to 1.1 times this value. This 'gain constant' error varies from one i.c. to the next, but stays constant within each i.c.

PRACTICAL CONSIDERATIONS

The larger the value of C_I, the less ripple

will be produced, but the slower the circuit will be to respond to changes in frequency. The values of C_T and R_I will also affect response speed; C_I should be kept larger than 100p to avoid voltage errors. The value of ripple on the output is given by:

ripple voltage p/p =
$$\frac{V_z \times C_T}{(2 \times C_l)}$$

× $\left(l - \frac{V_z \times f_l \times C_T}{I_o} \right)$

 I_0 is the available output current from pin 2 or pin 3. This can vary from 140–240µA; typically it is 180µA. Finally, the maximum input frequency for the system is:

$$f_{max} = \frac{I_0}{V_z \times C_T}$$

BASIC CIRCUITS

The most effective way to illustrate the use

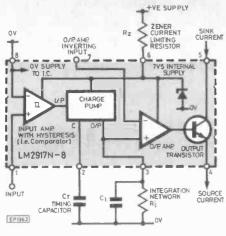


Fig. 2. Block diagram of LM 2917-8

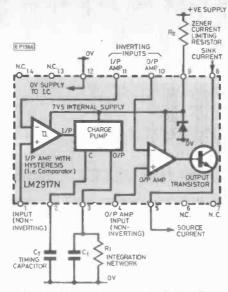
of the output op-amp and transistor is to consider two typical examples of basic circuits. Fig. 4 shows a simple tachometer, with the transistor connected as an emitter follower. The connection to pin 7 therefore provides negative feedback to the op-amp, which acts as a unity gain voltage follower. R_L is a load resistor, which can be replaced with a 5V (full scale) meter movement, or can feed into a l.e.d. bargraph circuit if required. Remember to a.c. couple the input (and tie down pin 1 to 0V with a high value resistor) for most applications, or in the case of the LM 2917N, bias the inputs up to around half rail voltage.

Fig. 5 shows a speed activated switch, with the op-amp acting as a comparator. When the voltage at pin 3 exceeds the voltage at pin 7 (set up by the two 4k7 resistors), the output transistor turns on, sinking up to 40mA from the load. This occurs at the frequency given by:

 $f_{switch} = \overline{(2 \times R_I \times C_T)}$

APPLICATION

Fig. 6 shows the circuit diagram of a more sophisticated 'speed switch', with Fig. 7 showing the Veroboard layout required for this. R2, R3, and R4 set the threshold at which the output amplifier switches. When this happens, the





i.c.'s output transistor turns on, causing D2 to light up and TR1 to turn on, effectively connecting R14 in parallel with C6, which results in the voltage on C6 gradually dropping. This dropping occurs until the output op-amp turns off again, turning off the output transistor and TR1 in turn; the voltage across C6 starts to rise again when this happens, which in turn causes the output op-amp to turn on, etc. The connection from the resistor chain R2, R3, and R4 to pin 7 of IC1 provides extra

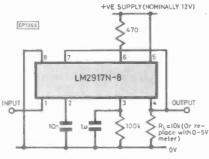


Fig. 4. Simple tachometer

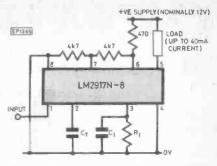


Fig. 5. Simple speed activated switch

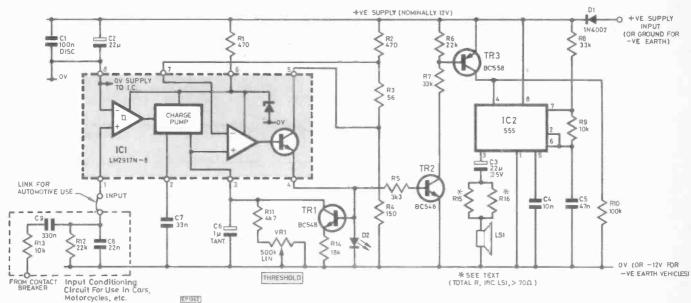
hysteresis in the system, ensuring that the system does not oscillate at high frequencies around the turn on/turn off point of the output op-amp. There will, of course, be the low frequency oscillation as described above, the frequency of which will be determined by the rate at which IC1 pin 3 can charge up C6, which in turn is determined by the input frequency.

The circuit will have no effect until a certain frequency is exceeded, at which point D2 will start to flash on and off slowly. If the input frequency increases, the l.e.d. will flash at a faster and faster rate, until it remains illuminated continuously. The threshold frequency at which the l.e.d. first lights up can be set via VR 1.

AUDIBLE WARNING

IC2 is a 555 timer i.e. connected as an audio frequency oscillator. TR2 and TR3 turn the enable pin (pin 4) of the i.e. on whenever D2 is illuminated, providing an audible warning. The transducer used for this can be a piezo-sounder, in which case no series resistor is likely to be needed, or a loudspeaker, in which case the impedance of the loudspeaker, in series with dropper resistors, should ideally be approximately 70 ohms or more. The series dropper resistors shown asterisked in Fig. 6 should total 1W for low impedance loudspeakers. Use a pair of 0.5W 150 ohm resistors in parallel for a 4 to 16 ohm loudspeaker.

Fig. 6 (Below). Circuit diagram of overspeed alarm or 'speed switch'



D1 protects against incorrect connection to the supply, and, together with decoupling capacitors C1 and C2, provides a measure of isolation if used in 'noisy' automotive electrical systems. The circuit can be used to monitor car or motorbike engine revs if the input conditioning circuit shown in Fig. 6 is used. This circuit provides decoupling, filtering, and attenuation of the contact breaker voltage spikes, and is suitable for both positive and negative earth systems. Don't forget to include a fuse in the positive supply feed to the circuit, though, for safety (or negative supply for positive earth vehicles). If the LM 2917N is being used, a Zener diode should be fitted between pin 1 and OV (with its anode connected to 0V) to protect against reverse voltages. The value is not critical, but 12V should be adequate in most cases (other changes to the circuit of Fig. 6 are also necessary, of course).

1S UNKS RETAIN Fig. 7. Veroboard C2 layout for overspeed alarm LINK FOR AUTOMOTIVE USE VRI VR1 WIPER

SOME ADVICE

Although this circuit works well, it would not be advisable to rely on it for keeping to speed limits, since it monitors engine revs, not road speed!

The LM 2917N-8, and LM 2917N, are useful devices for many frequency-to-voltage conversion applications. They are readily available from Cricklewood Electronics Ltd., 40 Cricklewood Broadway, London NW2 3ET.

EP 1361 A

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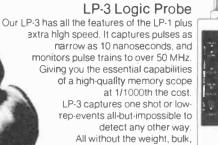


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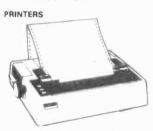
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V.T.'s views and opinions are entirely his own and not necessarily those of PE

could tell immediately that he was an engineer of the old school. A dead giveaway was the slide rule poking out of his top pocket. Remember the slide rule? I rated him classical junction transistor vintage. He sighed and shook his head sadly.

"You know," he said. "I sometimes think this high-technology electronics business is getting a bit too clever for comfort. Sophistication, as they call it, is becoming an end in itself. Complexity is chic and it's jolly hard on the old hands like myself. Most mindboggling of all is this computer-age language. I just can't get the hang of it.

"Words and phrases we learned at mother's knee have been deprived of their original meanings by the chip brigade. For instance, before the microprocessor processed itself into our lives, a bus driver was a chap who swore at cabbies and didn't always stop at one's request. A byte (see, they can't even spell anymore) was a munch on a cheese and pickle sandwich or something you got from a playful wasp while rolling in the long grass. And a RAM was a character much sought after by broody ewes."

I could have gone on with the usual gaff about the forward march of science and the need to keep up with the rest of the world. But he didn't seem in the right frame of mind to take it. So the best comfort I could offer was an invitation to join me on a visit to the HQ of the Sutton (Surrey) Talking Newspaper for the Blind. For him it would be a trip down the memory lane of basic electronics-which, when all is said and done, continues to serve humanity without benefit of the sophistication he finds so difficult to cope with. There's nothing particularly new about talking newspapers. They had their origin in Sweden and first reached our shores in the early 1960s. The STN was mooted in neighbouring Carshalton in 1974 and came out with its first issue three months later.

Lesley Page, a one-time employee of the Bank of England and a socially-active lady with a rare gift for organisation, is the STN's secretary. She told me: "In the initial stages we were financed by interest-free loans from the local Rotary Club. But thanks to our own fund-raising activities we were able to redeem them within a year. The local library lent us their recording equipment and we worked from the flat of the late John Bradley, the much-missed president of the British Amateur Tape Recording Society.

"Then came a splendid stroke of luck. The Wallington & Carshalton Round Table offered to buy us our own equipment if we could find ourselves permanent premises. Sutton Council helped generously here by giving us a suite of rooms in the building which we share with the Registrar of Births, Deaths & Marriages and the Rent Officer. Distinguished company indeed."

It was Thursday-'Press day'-when my morose friend and I called on STN. In one room a trio of ladies were busy unpacking and sorting the returned C60 cassettes carrying the previous week's issue (five mailbags of them in all). In another room a team of editors were scanning the local newspapers, supplied free by the publishers, for the 'hard news' side of the tape. Contary to what you might expect, there is no bias in selection towards only pleasant or neutral news. "The blind dislike the idea of being protected from unpleasant things," said Lesley. "They want to hear about both the good and the bad so that they can discuss current events with their sighted friends. Anything goes, from muggings to garden fetes." The second side of the tape accommodates the 'magazine' section. In this the blind themselves have a large slice of the action. They provide articles, seek out interviews with local officials and prominent personalities. There are items about holidays and leisure pursuits. One blind man has even contributed an account of his experiences as a mountaineer!

"You're out of date, dad. Your mind is pre-microchip"

In the control room I spoke with Doug Cook, formerly an engineer with the Post Office. He was in the process of making the master tape of the magazine section. "With our duplicating machines," he said, "we can turn out 13 copies in three minutes. We edit them so that halfway through there's a break for music which gives our 'readers', as we call the listeners, a chance to put the kettle on." By now all was ready for recording the news. The team consisted of one presenter and four readers, all of whom identified themselves by name. Their professionalism was remarkable, though, says Lesley: "We don't really need professionals-just people with enthusiasm and clarity."

The clock stood at 8.30 p.m. All the tapes were completed and checked. A standard procedure, by the way, is to include a reminder to turn off the recorder and to turn over the reversible label on the postal pouch for return of the tape to STN headquarters. And in case you're wondering how blind persons differentiate between the two sides of the tape, there's a tactile strip on the face of the cassette.

The rest was sheer humping. First, the registration of each pouch before it went into the mailbag. Then a trip to the back door of the main Post Office. The mailings—handled free of charge in both directions—would be dealt with overnight and the majority of tapes would reach their destinations by first post Friday. As Lesley said: "Sometimes we even beat the newspapers."

Some 300 blind people (out of a registered total of about 500) in the Sutton area regularly receive the STN. Applications come mostly through social workers. Most of the 'readers' are elderly, but there is a fair sprinkling of younger ones too. Many people have their own tape recorders, but those who do not borrow them from the STN free of charge. Between 200 and 300 public-spirited citizens, all unpaid and totally dedicated, working on a well-organised rota system, help to produce the newspaper every week. They come from all walks of life and many of them have blind relatives. "At the moment we have no shortage of volunteers," says Lesley.

The STN, which is a registered charity, costs between $\pounds1500$ and $\pounds2000$ a year to run. But rather than simply exist from year-to-year, a move has been made to set up an investment fund of around $\pounds20,000$ to provide an assured income. This is being achieved by gala concerts, street collections, the sale of ballpoint pens and other novelties. Some schools have adopted STN as their pet charity for a specified period. There are regular carol-singing forays at Christmas. Even the local police force has contributed by making over some of the proceeds from the sale of unclaimed stolen property.

Backing the STN and similar organisations throughout Britain, is the Talking Newspaper Association of the UK. It deals with such matters as copyright, is the principal contact with official bodies and provides many other kinds of ideas and help. Here again, all concerned are unpaid volunteers.

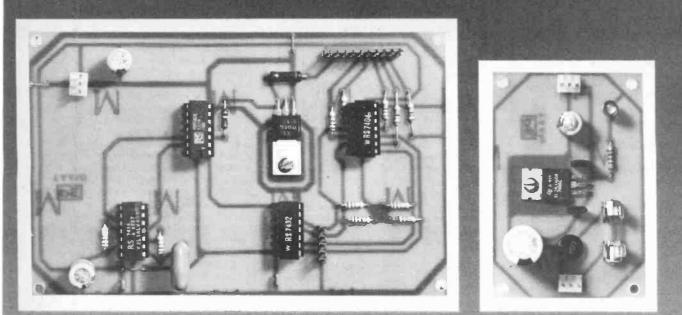
For those who have been reared on modern technology and all its wonders, the STN and others like it may seem an age away from the sophistication of the present. OK, so basic electronics may be old hat for the whiz-kids of the 1980s. But those same basics are helping to bring a fuller life and a broader involvement with society to a lot of people who wouldn't know, and couldn't care less about, the difference between a random access memory and a plate of fish and chips. My old engineer liked that sentiment.

I see that Football League clubs are likely to be offered some sort of microprocessor gubbins that will bring knife-toting, chaincarrying and otherwise mayhem-oriented louts to a standstill at the turnstiles. Anyone purporting to be a genuine supporter would be issued with a plastic card to establish his identity. This would then be screened for authenticity before he was allowed on to the ground. But would this really completely deter those who seem hell-bent on bovver and



have little or no interest in the game?

I loved that piece by Ray Connolly in the London evening newspaper, The Standard. Failing to follow the interpretation by an 11year-old of a War Games movie, he was told: "You're out of date, Dad. Your mind is premicrochip. You need re-programming." Hard cheese, Ray. Maybe you'd better link up with my old mate with the slide rule. You seem to have a lot in common.



MICHAELTOOLEY BA DAVID WHITFIELD MA MSc C Eng MIEE

N this month's issue we begin a new series which provides some practical examples of digital techniques. These projects, which have been carefully selected to complement the series entitled 'Introduction to Digital Electronics', also make excellent constructional projects in their own right, finding numerous applications in the home, school and workplace. Each project uses low-cost, readily available components and single-sided p.c.b.s are used throughout.

We start, this month, with a simple Anti-Theft Alarm which is designed to provide an audible and visual warning that property or goods are being tampered with. This project illustrates the use of some of the basic logic gates, demonstrates techniques for driving l.e.d.s, and shows how simple square wave oscillators can be constructed using Schmitt logic gates. A separate power supply module is also described. This module provides a regulated 5V supply of up to 500mA and is suitable for use with both the Anti-Theft Alarm and any of the subsequent projects.

CIRCUIT DESCRIPTION

The complete circuit of the Anti-Theft Alarm is shown in Fig. 1. The alarm is provided with four input loops which link points A, B, C, and D respectively to the common OV rail. Whenever one, or more, of the loops is broken the respective pull-up resistor, R1 to R4, will generate a logic 1 input at IC1 which is arranged to form a four-input OR gate. The normal state of the output of IC1c, when all of the loops are closed, will be a logic 0. If, however, any of the loops is broken, the output from IC1c will become logic 1.

In order to provide a visual indication of which one of the loops is broken, IC4 is arranged as an I.e.d. driver, inverting the logical input to IC1 so that the respective I.e.d. becomes illuminated whenever an output goes low. A fifth I.e.d. is included merely to indicate that the supply is connected and that the alarm is active.

IC2a uses a Schmitt inverter to form a simple oscillator which produces a square wave output at approximately 3kHz. A similar stage, IC2f, operates at the much lower frequency of 3Hz. An inverting buffer follows each oscillator and then both square wave signals are applied to a twoinput AND gate, IC3d. The resulting output from IC3d consists of 200ms bursts of 3kHz signal which is then fed to a further two-input AND gate, IC3a.

The gated square wave signal from IC3d only appears at the output of IC3a when a logic 1 appears at the output of IC1c (i.e. when any one, or more, of the loops is broken). In order to provide an audible output at ample volume, a VMOS f.e.t., TR1, follows IC3a. This device has a near infinite input impedance and is capable of driving the low impedance load presented by the loudspeaker. A series resistor, R13, is included in order to both reduce the volume of the output signal and reduce the peak drain current flowing in TR1 to an acceptable value.

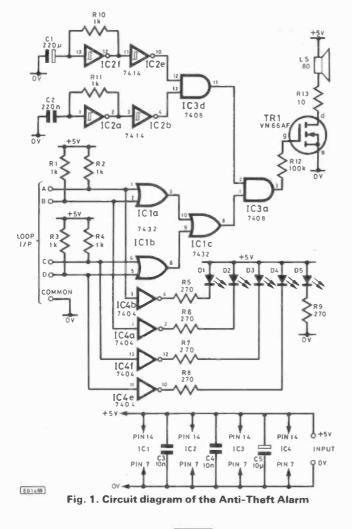
The circuit diagram of the Power Supply Module is shown in Fig. 2. This uses a conventional i.c. regulator and an l.e.d. is incorporated in order to provide a visual indication of the d.c. output. Little further comment is necessary other than that the nominal 6V a.c. input is derived from a fully encapsulated mains transformer of similar type to that used with the Logic Tutor.

CONSTRUCTION

The Anti-Theft Alarm is built on a single sided p.c.b. measuring approximately 140×90 mm, the copper foil layout of which is shown in Fig. 3. The corresponding component layout on the top surface of the p.c.b. is given in Fig. 4. Interconnections from the p.c.b. to the four input loops, l.e.d. indicators, loudspeaker and power supply are all made via 0.1'' matrix p.c.b. connectors, the wiring for which is shown in Fig. 5.

Components should be assembled on the p.c.b. in the following sequence: d.i.l. sockets, p.c.b. connectors, resistors, capacitors, f.e.t. Once assembly has been completed the underside of the p.c.b. should be carefully

SECURITY PROJECT



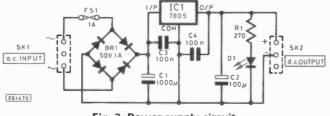


Fig. 2. Power supply circuit

checked for solder splashes, bridges between adjacent tracks, and dry joints. Finally, the i.c.s may be inserted in their respective holders, taking care to ensure the correct orientation of each device. Constructional details of the enclosure and off-board wiring have not been given since this will undoubtedly be a matter of preference for the individual constructor.

The p.c.b. layout for the Power Supply Module and corresponding component layout are shown in Figs. 6 and 7. Assembly is very straightforward; however, care should be taken to ensure that the bridge rectifier is correctly orientated. The i.c. regulator should not require a heatsink for this project; however, if one is available rated at around 17.5° C/W, it may be fitted to meet the supply current demands of more ambitious projects. Once complete, and before the a.c. input is applied, the Power Supply Module should be

COMPONENTS

ANTI-THEFT ALARM

Resistors

R1, R2, R3, R4, R10, R
R5, R6, R7, R8, R9
R12
R13

111 1k (6 off) 270 (5 off) 100k 10

Capacitors

C1	
C2	
C3, C4	
C5	

220μ 16V p.c. elect. 220n polystyrene 10n ceramic disc (2 off) 10μ 16V p.c. elect.

Semiconductors

D1, D2, D3, D4	Red I.e.d. (4 off)
D5	Green I.e.d.
TR1	VN66AF
IC1	7432
IC2	7414
IC3	7408
IC4	7404

Miscellaneous

P.c.b. 14-pin d.i.l. sockets (4 off) 3-way 0-1" p.c.b. plug and socket 5-way 0-1" p.c.b. plug and socket 10-way 0-1" p.c.b. plug and socket 80 ohm loudspeaker

POWER SUPPLY MODULE

Resistors

R1

Capacitors C1 C2 C3, C4

1000μ 16V p.c. elect. 100μ 16V p.c. elect. 100n polyester (2 off)

270

Semiconductors

D1 BR1

IC1

Red I.e.d. 50V 1A bridge rectifier 7805

Miscellaneous

P.c.b. 3-way 0·1" p.c.b. plug and socket (2 off) 1A 20mm fuse and p.c. fuse clips

carefully checked for soldering faults. The mains transformer is rated at 6V 3VA and should be housed in a fully insulated plastic encapsulation integral with the mains lead and plug.

TESTING

Testing the Anti-Theft Alarm is simply a matter of checking that the 5V supply is present and, if this is the case, D5 should be illuminated. Each of the input loops should then be open-circuited in turn. The alarm should be activated whenever any one of the loops is broken and the corresponding l.e.d., D1 to D4, should become illuminated. The input loops will normally consist of lengths of stranded insulated wire running through the goods to be protected.

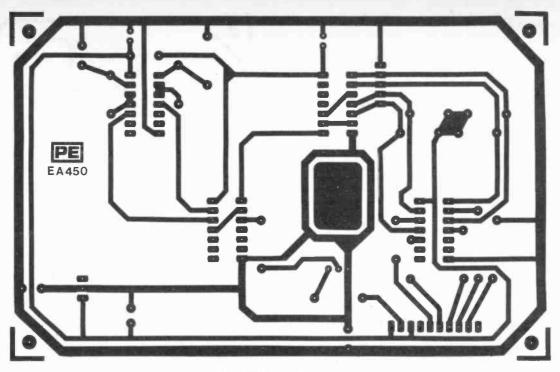


Fig. 3. Main p.c.b. design

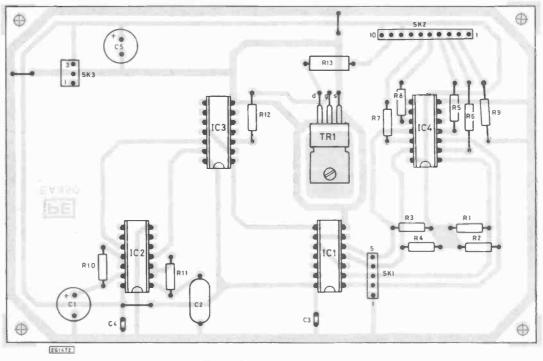


Fig. 4. Component layout

They may also consist of thin strips of foil fastened to windows and glass doors by means of a suitable adhesive. Indiscriminate breaking of the glass will cause the foil strip to break and the alarm to be set off.

MODIFICATIONS

The sound level of the output may be adjusted by varying R13 which should be reduced in value if more output is re-

quired or increased in value if less output is required. If R13 is reduced to less than $5\cdot 6$ ohms a small heatsink will be required for TR1.

The frequency (pitch) of the audible warning signal may be changed by altering the value of C2. A larger value (say 470nF) will decrease the frequency, whilst a smaller value (say 100nF) will increase the frequency. If it is necessary to alter the rate at which the audible output is pulsed on and

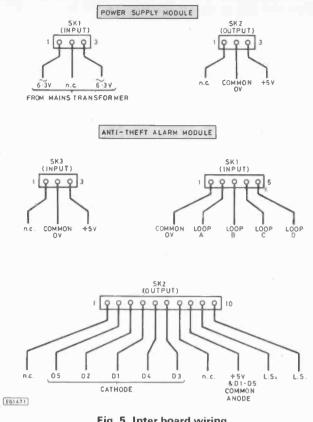


Fig. 5. Inter board wiring

off, C1 may be similarly varied. Appropriate values lie in the range 100µF to 680µF.

To drive several loudspeakers, the circuit around R12, TR1, and R13 should be duplicated. Each loudspeaker then has its own driver circuit. The signal input for all of the driver circuits is derived from pin 3 of IC3a. The loudspeakers

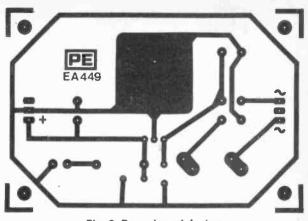


Fig. 6. P.s.u. board design

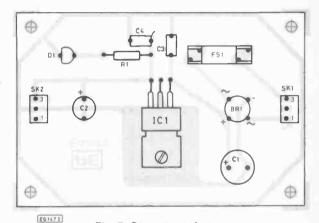


Fig. 7. Component layout

should be placed at various strategic points. These may, for example, include passageways, doorways, counter and checkout areas. *

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S PL	l enclose cheque/PO for £
TAL	Name
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l ž	
2	0
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*** LOW-POWER STEREO AMPLIFIER *** Modest budget project, ideal for the beginner. Output 2.5 watts per channel. Three inputs: for ceramic cartridge pickup, tape recorder and auxiliary. Bass and treble tone controls. 8 ohm outputs.

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Connects to the User and Analogue Ports to produce an accurate digital multimeter with screen readout. Voltage, Resistance, Capacitance measurements, in ranges up to 100V, 10MΩ and 10µF respectively.

> MARCH ISSUE **ON SALE FEBRUARY 17**



N THIS, the concluding part, details of the p.c.b. assembly and case construction are given. The project is a remote VDU/Keyboard terminal capable of RS232 serial communication with any home computer with an RS232 port.

P.C.B. ASSEMBLY

The p.c.b. foil pattern and component layout are shown in Figs. 2.1 and 2.2.

The components should be installed on the p.c.b. in the following order:

- a) Links, terminal pins and regulator leads.
- b) I.c. sockets.
- c) Capacitors and resistors.
- d) Modulator, buzzer and crystals.
- e) Connectors.

It is strongly recommended that i.c. sockets are used, as it is difficult to change faulty or incorrectly installed devices if they are soldered to the p.c.b. Before proceeding any further it is wise to check for incorrect component locations and solder bridges. These are most likely to be found in the RAM area of the p.c.b.

CASE

There is a wide range of commercially available cases that the reader may choose from to house the system. However, the author found none suitable for his requirements and so constructed the case shown in the photographs. The side plates are made of solid mahogany, with the chassis, back and cover plates made from aluminium sheet, spray painted. The wooden side plates are cut to size and the support battens screwed to them as shown in Fig. 2.3, and the aluminium panels cut and drilled to the dimensions shown in that Fig. The back panel carries the UHF and monitor output sockets, mains input socket, the full/half duplex switch, the 25-way D-series connector for the RS232 link, and is also used as a heat sink by the three voltage regulators which should be fitted using insulating mica washers. The back plate is connected to the chassis by a length of 13mm aluminium angle as shown. Two identical covers should be constructed, one of these being cut to accept the chosen keyboard. All the aluminium panels should be rubbed down with wire wool before being sprayed. The keyboard is then secured to its cover, the various components fitted to the back plate which can be bolted to the chassis. The p.c.b.,

mounted on insulating spacers, and the transformer are then fitted to the chassis. The various parts should next be wired together as shown in Fig. 2.4. Finally, No. 5 x $\frac{1}{2}$ inch countersunk screws are used to mount the aluminium panels to the side plate battens, with the exception of the top cover plate which should be fitted after the Computer Terminal has been tested.

TESTING

Before inserting any i.c.s the power supplies should be checked to establish that the correct voltages are being produced. Check that the correct voltages are present on the various i.c. power pins. If all is well the unit should be switched off and the i.c.s inserted, taking care to insert IC12 and IC15 the correct way round. The normal precautions should be employed when handling the i.c.s, *especially the RAMs.* The full/half duplex switch should be set to the half duplex position, the monitor or television connected and switched on.

The terminal can now be switched on. If a television is being used, it should be tuned to channel 36 (that used by video recorders). The screen will be filled with random characters. It may be necessary to adjust VR1 and VR2 for best results. The reader will notice a flashing cursor somewhere on the screen: characters entered on the keyboard will be displayed at the cursor position. The cursor itself may be moved around the screen, or the screen cleared by entering the ASCII control characters listed in Part 1.



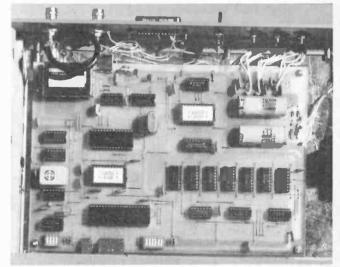
COMPUTING

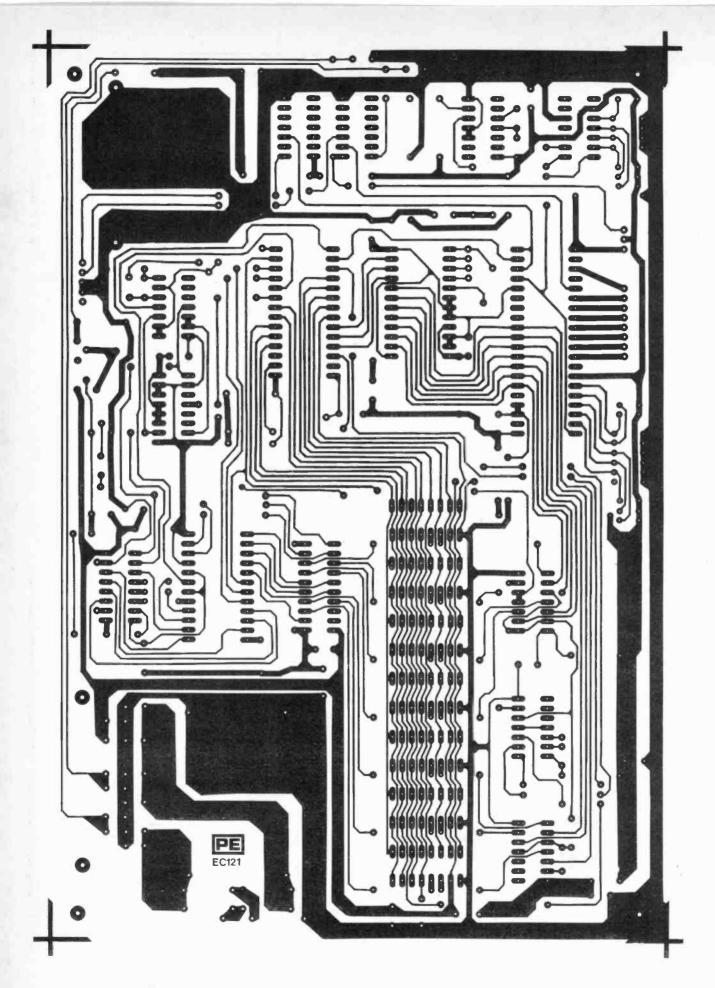
COMPONEN	TS	IC20 IC21	74LS132 1488	
		IC21	1489	
Resistors		1022	7805	
R1-9, R11, R17	10k (11 off)	IC24	7812	
R10		IC25	7912	
R12	10M	TR1.2		
R12	100R	D1-4	BC109, BC547 etc (2 off) 1N4001 (4 off)	
	2k	D1-4	1N4001 (4 off)	
R14, R18	1k (2 off)			
R15	4k7	and the second		
R16	82R (12W)	Miscellaneous		
All resistors W 5	% unless otherwise stated	X1	1 MHz crystal	
Potentiometers		×2	5.0688MHz crystal	
	And the second sec	UHF modulator	Astec 1233 (8MHz)	
VR1	470R	S1-4	4-way p.c.b.	
VR2	100R	S5-10	6-way p.c.b.	
		S11	S.p.d.t.	
		SK1	25-way D-Series	
Capacitors		SK2,3	BNC Chassis Mounting	
C1	100p	SK4	IEC Mains Connector	
C2	22µ/10V	SK5	5-way p.c.b. Connector	
C3,4	2200µ/25V (2 off)	SK6	3-way p.c.b. Connector	
C5-30	100n (26 off)	SK7	8-way p.c.b. Connector	
		Buzzer	Verospeed 41-22515K	
		T1	12-0-12 25VA transformer	
Semiconductors		Keyboard		
IC1-7	2102/7-4	Case (see text)		
101-7	2102 (7 off) 74LS374	Double Eurocard single-sided p.c.b.		
109	SFF96364	I.c. sockets	3	
IC10				
	2716 EPROM			
IC11	6402 or AY-5-1013 (see text)	C	onstructors' Note	
IC12	2716 EPROM	A Hex dump of the EPROM contents is available fro		
IC13	74LS163			
IC14	74121	P.E. (Poole office); please send 230 x 150mm SAE. Pre		
IC15	74LS165	programmed EPROMs and COM8126s are available from:		
IC16	COM8126		," 25 Braycourt Avenue, Walton-c	
IC17	74LS08		12 2AZ. Printed circuit boards, if r	
IC18	74LS00		P.E.'s usual suppliers (see advertiser	
IC19	74LS08	will in any case be av	ailable from this supplier.	

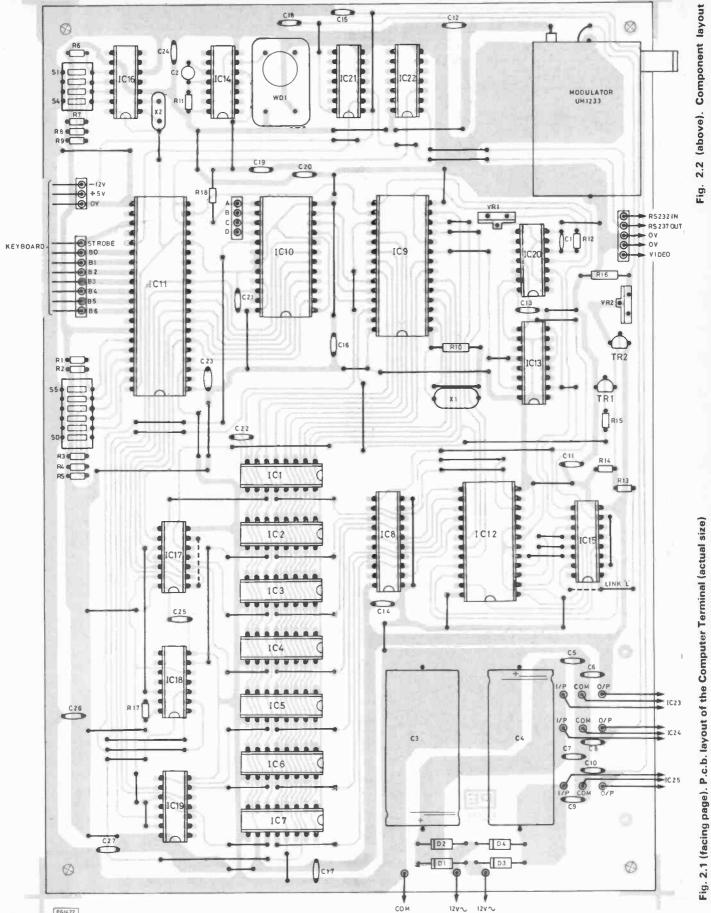


Internal views of the Computer Terminal



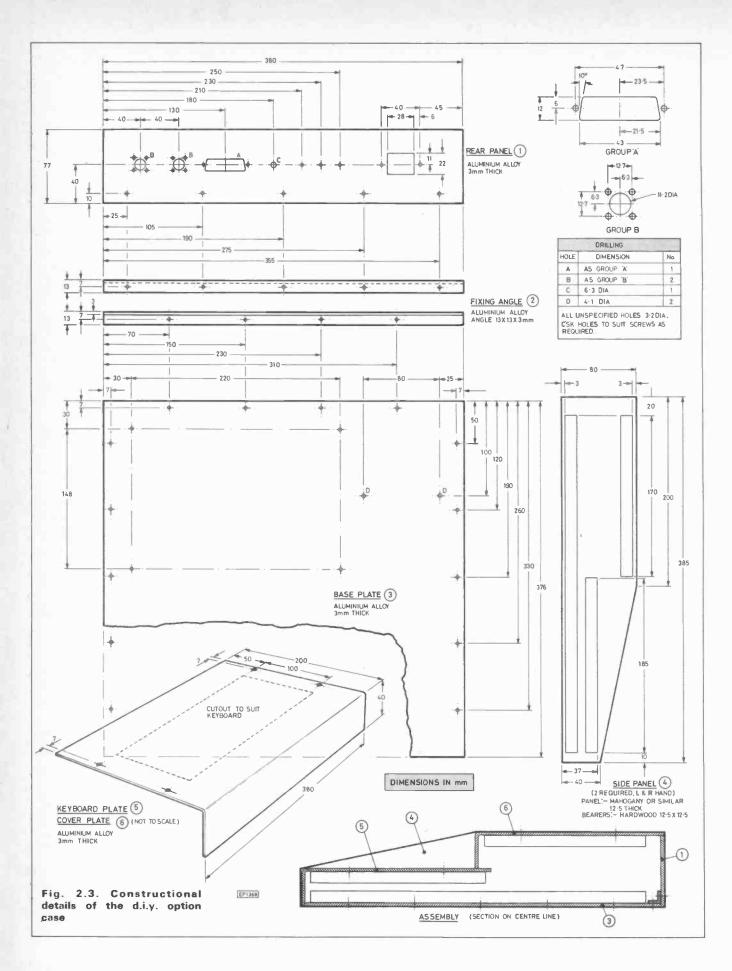






EG1422

31



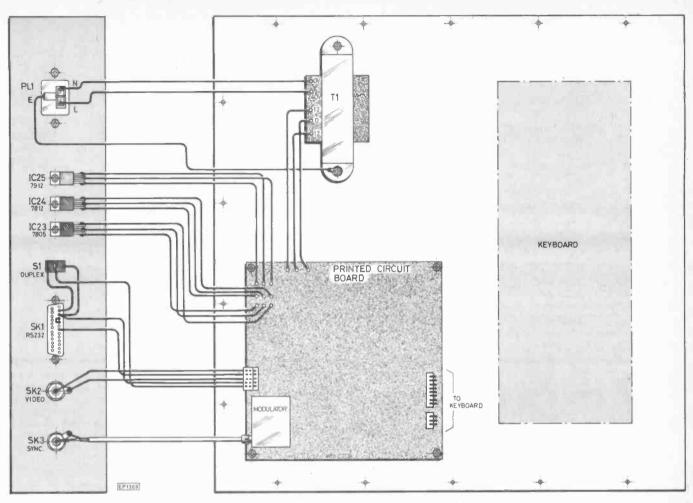


Fig. 2.4. Wiring diagram of the Computer Terminal

The BEL function can be checked by pushing the CTL and G keys 'together, whereupon a buzzing sound should be heard. Note that the UART latches its receiver outputs to the last character detected. As the buzzer's monostable is edge triggered it will only respond to the *first* CTL/G when several are sent consecutively. Normally CTL/G would be followed by a different character.

Switch to full duplex, the screen will remain unchanged, but characters entered on the keyboard will not appear on the screen. Connect the terminal to the host system via an RS232 cable. The host system's output should now be displayed on the screen. Similarly the host system should respond to characters entered on the keyboard.

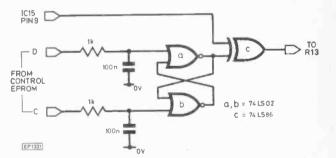
ADDITIONAL FEATURES

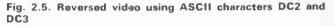
As previously described, the control EPROM is programmed so that four of its outputs respond to the ASCII control characters as shown below:

03 — CTL/G (BEL) — p.c.b. pin A 04 — CTL/Q (DC1) — p.c.b. pin B 05 — CTL/R (DC2) — p.c.b. pin C 06 — CTL/S (DC3) — p.c.b. pin D

A p.c.b. plug is provided so that these signals may be used to drive additional circuitry.

The circuit in Fig. 2.5 shows how normal or reversed video could be selected using the ASCII control characters DC2 and DC3. Gates 1A and 1B form a bistable flip-flop, set





by DC2 and reset by DC3. The flip-flop's output is exclusive ORed with the normal video signal to produce normal or reversed video which is fed to the transistor mixer TR1. Issuing a DC2 character will cause all following characters to be reversed until a DC3 character is issued to revert back to normal video. The reader can therefore select various parts of the screen to display reversed video at will. If this circuit is used link "L" must be removed from the p.c.b.

A similar circuit (see Fig. 2.6) could be used to control a relay which could drive, for example, a cassette recorder's motor. DC3 would turn it on and DC2 turn it off. These two examples serve to indicate the types of additional facilities that may be included in the system and is by no means an exhaustive list.

INTERFACING WITH THE BBC COMPUTER

As stated at the beginning of this article, the Computer Terminal can be used as a second terminal for a BBC computer. The following notes describe how this can be achieved. With this terminal, or "glass teletype", connected to the BBC's RS432 socket, the command *FX2,1 allows the BBC computer to get characters from the "glass teletype", whilst *FX3,7 allows data to be sent from the BBC computer to the "glass teletype". Note that in this mode the BBC computer's keyboard and screen are disabled. The BBC computer's Baud rate is set to the same value as that of the PE terminal (say 2400 Baud) by using the commands *FX7,5 and *FX8,5 for receive and transmit rates respectively. Reference should be made to the BBC computer's "user guide" for further information on the use of the RS423 port.

CONCLUSION

Although reference has been made to the BBC computer, it is by no means the only system to which the terminal may be interfaced. The Computer Terminal can be used with any system fitted with a RS232 or RS423 interface. Examples of such systems are: Microprocessor development systems. Modems, EPROM programmers, Printers, as a terminal for a RTTY radio receiver, or on its own in half duplex as a practice typewriter.



Gas Saver

Sir—The boiler referred to in this article is obsolete, production finishing in 1970; although later series continued the basic design through to 1980.

The heating interests of Ideal-Standard Ltd. were incorporated into the Stelrad Group Ltd. in 1976 and it is with Stelrad that I am employed as Senior Controls Engineer within Group R&D department. In this capacity I must point out the problems associated with "add-on" modifications to approved gas appliances.

Interference with the working parts (in particular the electrical controls) of an approved gas boiler could invalidate the approval and warranty/service agreements as well as infringing the Gas Safety Regulations and, more to the point, could seriously impair the safe working of the appliance.

Any modification must give due regard as to the consequences—in particular taking full responsibility for the modifications carried out.

Obviously appreciable running cost savings can be made and manufacturers are currently investigating many possibilities for future incorporation into manufactured appliances.

The article also seems to suggest that only electronics can give the savings indicated. However, with the inclusion of a clamp-on cylinder thermostat and some simple wiring modifications the indicated savings could be achieved for less initial outlay, without invalidating the above comments.

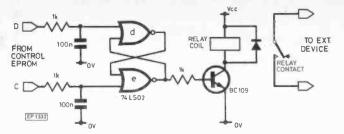
It would appear that there is little appreciation for heating, as the article seems to concentrate on controlled hot water and controlled boiler temperature rather than total comfort and cost effectiveness. As regards to controlling the gas valves via triacs and the associated gates and comparators, this is at present not accepted by the Industry for primary output because of its possible failure mode resulting in an unsafe condition, among other factors. It is true though that the article does suggest the thermostats provided with the boiler should be connected in series with the "Gas Saver" but this is not shown on the diagram and is not highlighted sufficiently within the article.

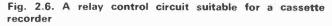
As you state in the article "... Safety is all important in any equipment ... using gas and electricity simultaneously, particularly, when running continuously without supervision." Hence we would suggest this should be left to experts as a little knowledge can be, so often, dangerous.

The subject is too large to handle in a few lines but it is hoped that the foregoing will be seen as constructive and helpful as we all endeavour to further the interest of electronics to the benefit of the Industry and our customers. M. J. Blissett,

Senior Controls Engineer, Stelrad Group Ltd.

We have received a couple of similar letters, and it seems I must first plead guilty to perpetuating the misconception that the copper tube in the typical boiler thermostal conducts heat directly. In fact, it contains a fluid which expands when heated, and the capillary action is used to operate electrical contacts via a "bellows" mechanism. Although not as rapid as electronics, the action is not as slow as the article suggested.





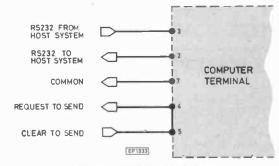


Fig. 2.7. RS232 connections

To respond to the particular points raised by Mr. Blissett: First, I believe most consumers cannot afford to replace their C.H. system (or any other appliance) each time it is declared obsolete. Gas Saver was intended to allow the older, or cheaper, system to become more economical, given its inherent limitations.

An older system will not be covered by a manufacturer's warranty, but of course, Mr. Blissett is right to point out that a consumer should not carry out d.i.y. modifications that will invalidate a service agreement, and is indeed personally responsible for any such alterations. Beyond this, it is difficult to see how Gas Saver could impair reliability when connected, as suggested, in series with the existing thermostat. However, if I did not "highlight" this precaution sufficiently in the article, let me stress it now. A number of hobbyists experiment with electronics C.H. control, and look upon published material as further input, which is why I emphasised safety in general.

We accept the fact that "mechanical" equivalents to circuits published in Practical Electronics often do exist; as in "timers" for example. The clamp-on cylinder thermostat will not be as cheap if a professional is called in to install it—which I presume is advocated. The electronics enthusiast will argue that his approach paves the way to more flexible programming, making it possible to consider a timer that not only turns the C.H. system on and off, but which permits a programme of differing temperatures etc.

Failure modes should obviously be taken into account, and the article did underline this, hopefully to benefit also the hobbyist with his own ideas. But whether or not magazines should publish projects with which someone could have an accident, is a broader issue. I am sure the d.i.y. brand of hobbyist generally knows his own limitations and has the sense to avoid activities about which he has doubts.

M.A.

FILESHEET 14 8073

T would appear that about the only thing the various single-chip microprocessor families have in common is that they are all different! This month we are going to take a look at the gospel according to National Semiconductor as expounded by their 8070 family, and as usual there are a few surprises in the approach they have taken.

At first sight National appear to have been an also-ran in the great microprocessor race, because although they have produced a number of original chip designs, they have never become a serious challenge to the Intel-Motorola-Zilog "Big three", and have probably made more money from second-sourcing Intel designs such as the 4040, 8080, and 8048 than they have from the chips from their own stable. Whether this somewhat mediocre performance is a reflection on the quality of their designs or whether it is due to shortcomings in their marketing policy I cannot say, but it will be interesting to see how their latest offering, the very powerful 16 bit NS16032 fares in the coming months.

The first National microprocessor to achieve popular prominence was the 8 bit SC/MP, which pioneers in the microprocessor hobby field may remember as one of the first devices to become available in hobby kit form. I certainly remember reviewing for P.E. one of the first evaluation kits in the country, and I remember being impressed by its "generous" provision of 512 bytes of ROM based monitor software and its 256 byte RAM area for user programs. All of that squeezed onto just *one* single Eurocard! Of course, that was in the antediluvian days of 1976 or 1977 and things have changed a lot since then. The PMOS SC/MP caught on quite well, especially in Europe, and was soon followed by a 5 volt NMOS version, the SC/MP 8060, but in the end its limited processor performance and restrictive 12 bit direct addressing range caused it to lose ground to the competing Intel and Motorola processors.

National did not abandon the basic architecture of the 8060 however, and in 1980 they introduced the 8070 family which features extended performance and the capability to use an on-chip ROM and RAM array, a logical move since the original 8060 had proved most successful in the low cost controller applications most suited to single chip processors.

One of the most successful features of the 8060 family was its suitability for use in multi-processor systems thanks to an extensive set of control inputs and outputs, and it was decided to retain this feature on the 8070. A decision was also made to have separate non-multiplexed data and address busses, using 24 pins in all, and this, combined with the extensive control facilities, left only five pins available for I/O use.

This lack of the usual complement of parallel I/O ports puts the 8070 family on the fringes of the single chip processor scene, and makes the use of external I/O chips a necessity in most applications, but despite this apparent disadvantage there are certainly plenty of jobs in which the particular characteristics of the 8070 family make it the most suitable choice.

There are currently three devices in the family, the 8070 itself which has 64 bytes of on-chip RAM but no ROM, the 8072 which has 2.5K bytes of masked ROM for high volume applications, and the 8073 which is an 8072 with the ROM preprogrammed with a monitor and a Tiny BASIC interpreter, in the style of the Zilog Z8671 discussed last month. All three chips have the same basic internal architecture, instruction set, and pin connections, and all feature an 8 bit data bus, a 16 bit address bus and a 16 x 16 bit hardware multiplier/divider.

The 8070 and 8073 are both usable for hobby applications, but there seems to be little to recommend the multichip 8070 solution

over competitive devices unless a potential user suffers from 8060 nostalgia! Since there is no EPROM version I have chosen to feature the 8073 which is one of the two devices available which feature on-chip BASIC (the other being the Z8671).

Even when programming in BASIC, it is desirable to know something about the internal architecture of the chip itself, and so these details, common to the whole family are given as usual. Details of the BASIC interpreter which is of course specific to the 8073, are given in the Software section.

As you may have expected, the launch of the on-chip BASIC 8073 caused quite a surge of interest and more requests for data sheets than had ever been received for any previous National product. This must have generated mixed feelings at National, because data mailings are expensive and they must have realised that most recipients were either just plain curious, or were serious potential customers who would ultimately buy only one or two devices, since a device programmed in BASIC is not a cost effective solution for high volume applications.

Still, their loss is our gain, since a single-chip processor programmable in BASIC is an excellent choice for many one-off hobby applications!

REGISTERS

The original 8060 register set is carried through into the 8070 family with little change, although some names have been changed to reflect improvements in register usage and flexibility. The new family uses a single 8 bit accumulator register which acts as the implied source or destination for many instructions in typical first generation style, but this has been extended by means of an additional 8 bit register called the Extension register (E) which can be used either by itself as a temporary data store, or together with the accumulator to form the 16 bit EA accumulator for 16 bit operations.

There are five 16 bit registers, two of which are the Program Counter (PC) and the Stack Pointer which are quite conventional. There are two pointer registers (P2 and P3), which would be called index registers in most other processors, and finally something a little different, the Temporary (T) register which is needed for the 16 bit multiplier or divisor in multiplication or division operations, and can also be used as a general purpose 16 bit data store.

The only other user accessible register is the Status register (S), and this contains the eight flag bits as shown on the file sheet. Five of the flag bits are used for the two input lines, SA and SB, and the three output lines F1, F2 and F3, which are the closest the 8070 family comes to having any parallel I/O capability on-chip.

The only other flags available are the conventional Carry (CY), Overflow (OU), and Interrupt Enabled (IE), which means that there are no zero, sign, or auxiliary carry flags. No doubt the zero and sign functions can be simulated easily enough, but the lack of an auxiliary carry flag has the potentially serious implication that no direct BCD arithmetic is possible. Fortunately however, there is no requirement for BCD arithmetic when using the 8073's Tiny BASIC, and so there is no need to worry too much about this feature unless the use of an 8070 is being considered.

Apart from the above mentioned flag limitations, the 8070 family has quite a useful complement of registers.

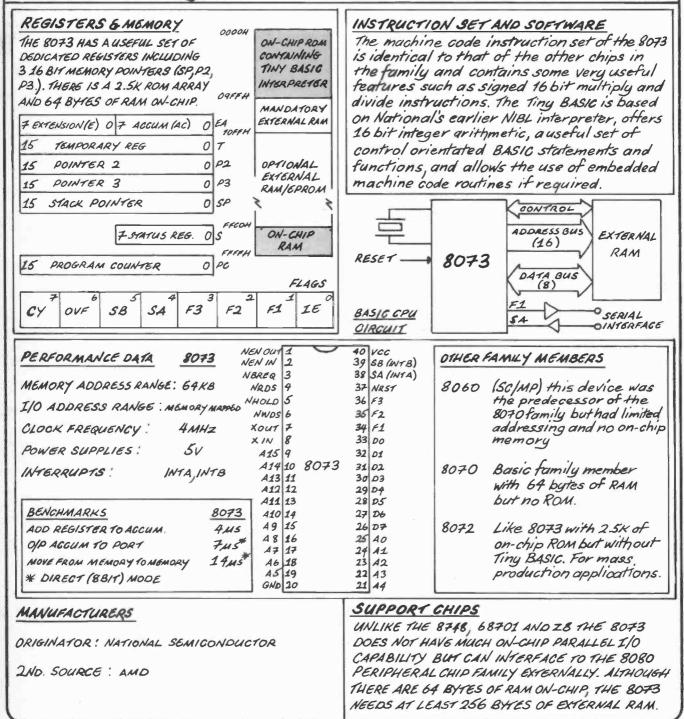
INSTRUCTION SET

Although the 8070 family instruction set has obvious links with the earlier SC/MP 8060 set, there are some deletions and several useful additions.

8073 REFERENCE FILE SHEET

GENERAL

The 8073 is a member of the National Semiconductor range of 8 bit NMOS processors which has been developed from the earlier SC/MP 8060 family. The 8073 has the outstanding feature of an on-chip Tiny BASIC interpreter stored in 2.5K bytes of ROM and is designed for low cost controller applications which do not require the high speed of machine code. Unlike most other single chip microprocessors the 8073 has very few on-chip I/O lines, but it does have extensive control features to allow multiprocessing.



- INSTRUCTION SET SUMMARY --

MNE- FIRST SECOND MONIC OPERAND OPERAND OPERATION PERFORMED	A E (A)(E)	EA SP (EA)(SP)	ACH EA P2 (EA)- →(P2)	EA P3 (EA)(P3)	A (A1)(A1-1), b = 7, 1, 0A7	SR EA (EAI)→(EAI-1) I = 15. 1; 0→EA15	SRL A (Ai)→(A··1), i = 7, 1, CY→A7	RR A (AJ)(A-1); i = 7, 1, A0A7	RRL A (A1)-(A1), 1 = 7, 1, A0CYA7	A (A+1)(A), 1 = 6.0.0-A0	SL EA (EA+1)(EA), i = 14.0.0-EA0	SSM See Text	BND If ASCII (PC) addr If nol digit 7 or 9, If digit 7	A ((SP)→(SP) · 1 ((SP))→(A)	EA ((SP)) · 1 (E). ((SP)) · 2 (SP) (SP) 2	PUSH PC ((SPI) - 1-(PCH); ((SP)) - 2(PCL); (SP)(SP) -2	P2 ((SP)) - 1 (P2H). ((SP)) - 2 (P2L). (SP) (SP) 2	P3 ((SP)) · 1 ↔ (P3H). ((SP)) · 2 ↔ (P3L). (SP) ↔ (SP) · 2	P2 ((SP)) · 1-(P2H). ((SP)) · 2-(P2L). (SP)-(SP) · 2.	PLI P3 ((5°C) - UVC - UVC) - UVC - (7°C) - UVC - (7°C)	(+ (ds)(ds)) ((ds))(v)	EA (A)((SP)). (E) ((SP) (SP)	POP P2 (SP)→ (SP)) - 1. (SP)→ -(SP) - 2	b3 (P31) (- ((SP)) (P24) ((SP)) · · 1 (SP) (SP) · 2	L BRA (PC) (PC) - disp	BP H (A) > 0 (PC)(PC) · disp	B2 II (A) = 0 (PC) + disp	BNZ II (A) # 0. (PC)(PC) · disp	JMP (PCH) byte 3. (PCL) byte 2	JSR ((SP)) - 1 - (PCH) - DVIE 3 ((SP)) - 2 - (PCL) - DVIE 2 (SP) - (SP) - 2	CALL 0 · 15 ((SP)) · 1 · (OZ) · 2'N), ((SP) · 2 · 2 · (PCL) · (02) · 2'N), ((SP) · 2	RET (PCL)((SP)), (PCH)((SP)) - 1, (SP)(SP) + 2	LD PC EA (PC)-(EA)	XCH PC EA (PC)-→(EA)	ILD A (A), (addr) ← (addr) + 1	DLD A (A), (addr)(addr) - 1
INSTRUCTION			EXCHANGE REGISTERS			SHIFT RIGHT	SHIFT RIGHT WITH LINK	ROTATE RIGHT	ROTATE RIGHT WITH LINK		SHIFT LEFT	SEARCH AND SKIP IF CHARACTER MATCHED	BRANCH IF NOT DIGIT			PUSM				INMEDIATE			404		BRANCH UNCONDITIONAL	BRANCH POSITIVE	BRANCH ZERO	BRANCH NOT ZERO	JUMP UNCONDITIONAL	JUMP TO SUBROUTINE	CALL	RETURN	LOAD PC	EXCHANGE PC	INCREMENT AND LOAD	DECREMENT AND LOAD
OPERATION PERFORMED	(A)+(addr)	(EA)+-(addr + 1, addr)	(T) (addr + 1, addr)	(SP)(PC + 2, PC + 1)	(P2)+- (PC + 2, PC + 1)	(P3) (PC + 2, PC + 1)	(A)(E)	(E)(A)	(A) ↔ (S)	(S) (A)	(EA){PC)	(EA) ↔ (SP)	(EA)(P2)	(EA)→-(P3)	(SP)(EA)	(P2) (EA)	(P3)(EA)	(T)(EA)	(EA)(T)	(A)(sddr)	(AE) → (addr + 1, addr)	(A) +- (A) + (ador)	(A)(A) + (E)	(EA)(EA) • (addr + 1, addr)	{A}(A) - {addr}	(A)(A) · (E)	(EA)(EA) - (addr + 1, addr)	[EA)→[[EA] '[1]] 31-16. [T]→[[EA] ' [T]] 15.0	Ouotient' (EA)[(EA / (T)] 15.0 Remainder' (T){(EA / (T)]	(A)(A) // (addr)	(A)→-(A) ∧ (E)	(S)(S) /> data	(A)+(A) √/ (addr)	(A) ← (A) √/ (E)	(S) ← (S) √/ data	(A)(A) -+ (addr)
SECOND							w	4	v	<	PC 2	SP SP	54	P3	EA	EA	ĒA	EA	F				w			ω		F	÷.		ω			u		
FIRST	«	EA	-	es.	2	8	*	w	<	v	EA	EA	EA	EA	SP	P2	P3	T	EA	4	EA	۲	v	EA	×	×	EA	EA	EA	×	<	s	V	×	IJ	<
INSTRUCTION MINE- C								L		LOAD LD										STORE CT			ADD			SUBTRACT SUB		MULTIPLY MPY	DIVIDE		AND			۴Ö		

Gone are the flag manipulations (Carry Set and Clear, Interrupt Enable and Disable) and these functions now have to be performed by means of logic instructions operating on the status register. Also missing are the unique SC/MP Delay instruction, which now has to be simulated with a counter loop, and the decimal arithmetic operators which represent a more serious loss.

Improvements include the inclusion of a true Jump to Subroutine Instruction, Push and Pop stack instruction, and a new one byte Call instruction which operates like JSR but uses up to 16 fixed vectors as indirect jump addresses, just like the 8080 style Restart. The new signed 16 bit Multiply and Divide instructions are particularly useful for high level language operation of course, and the unique "Search and Skip if character Matched" (SSM) and "Branch if Not Dlgit" (BND) appear to have been included with the needs of the 8073 BASIC interpreter very much in mind.

The SSM instruction searches through a 256 byte memory block for a character that matches the accumulator contents using the P2 or P3 register as a pointer. When a match is found the following two program bytes are skipped and the chosen pointer register indicates the address of the matching byte, very useful for interpretive programming.

The BND instruction tests the ASCII character in the accumulator to see if it corresponds to one of the ASCII decimal digit codes (30H to 39H). If it does not then a PC relative branch is executed, but if it does the ASCII character is converted into its binary equivalent (00H to 09H) thus saving several program steps. A useful feature for keyboard orientated applications.

There are 192 instruction types in the 8070 set, supplemented by a useful set of 9 addressing modes including Implied, Immediate, Direct Absolute, Indirect, Indexed, Auto Indexed, Program Counter Relative, and Pointer Relative. All in all, quite a useful instruction set with some nice features.

SOFTWARE

The 8070 family is intended mainly for controller applications and does not aspire to the dizzy heights of a common user software base or a disc operating system, so this section will be devoted to a description of the 8073 Tiny BASIC interpreter.

Tiny BASIC is not intended for general purpose data processing applications of course, because it has only integer arithmetic, no array capability and only limited string handling. It is mainly useful for the rapid creation and testing of controller type programs as an alternative to assembly language, and is a boon wherever the fatal flaw of slow operation can be tolerated (tens of milliseconds rather than the hundreds of microseconds possible with an assembly language version).

The 8073 contains the complete Tiny BASIC interpreter and system monitor code within its 2.5K bytes of on-chip ROM, and needs only some external RAM and an RS232 interface to a terminal to function as a complete system. The external RAM must total at least 256 bytes, plus any additional amount required to hold the user program (a bytewide 2K x 8 RAM such as the Mostek 4802 would be ideal). No external UART is required because the system monitor contains routines which emulate a UART, making F1 the serial output, F2 a "ready" flag, and SA the serial input. Baud rates of between 110 and 4800 are handled by the monitor and can be selected by programming the D1 and D2 bits of memory or I/O location FDOOH appropriately. If bit D7 of the same location is set to zero, the monitor I/O routines are not used, but instead a branch is made to user supplied routines located at addresses stored in FDO1H/FDO2H for character output, and FDO3H/FDO4H for character input. This useful facility allows the connection of other types of character I/O device (such as a parallel ASCII keyboard and LED display) if required. Note however, that the user subroutines have to be in machine code, not BASICI

When the 8073 is powered up or reset the Tiny BASIC automatically performs a memory search to find the address range of any external RAM which is connected as a contiguous block above 1000H. After locating the RAM area and extent, Tiny BASIC then tests location 8000H to see if it is RAM. If it is, COMMAND mode is entered and user inputs via the terminal are awaited. If it is not, the interpreter will assume that an EPROM based BASIC program resides there and execution will be attempted. If there is not an EPROM program resident, the execution attempt will be aborted and COMMAND mode will be entered.

This feature makes possible the creation of stand-alone, BASIC programmed control systems, which need not use a terminal (for example a central heating controller). Programs can be developed using RAM and a terminal, then blown into EPROM for continued automatic use.

In program development (or RAM) mode, the user is required to initialise the system by entering two commands as follows:----

NEW (ADDRESS)

NEW Carriage Return.

These commands establish the start and end addresses for the new program which can then be entered, with line numbers, in the normal way.

In addition to NEW, the RUN, CONT (Continue), and LIST commands are available.

A useful range of BASIC statements is catered for, as follows:

REM anything: Remark (no operation).

CLEAR: Initializes all variables to O, disables interrupts, and resets all stacks (GOSUB FOR-NEXT DO-UNTIL).

(LET) var = expr: Assigns expression value to variable.

(LET) STAT = expr: Sets the STATUS word equal to the least significant byte of "expr." When the STATUS word is used to enable interrupts at the hardware level, interrupt processing will be deferred for one statement.

(LET) @ factor = expr: Sets the memory location pointed to by 'factor' equal to the least significant byte of 'expr.'

(LET) \$ factor = "string": Assigns a string in RAM starting at the address 'factor.' Strings are terminated by a carriage return.

(LET) \$ factor = \$ factor: Memory to memory assignment (copy).

PRINT expr: Prints the value of 'expr.'

PRINT "string": Prints the string.

PRINT \$ factor: Prints the string starting at the memory address 'factor.'

IF expr (THEN) statements: Remainder of the program line is executed if 'expr' is true (non-zero).

FOR var = expr TO expr (STEP expr): FOR loop initiation. Loops may be nested to four levels.

NEXT var: For loop termination.

DO: DO loop initiation. DO loops may be nested to eight levels.

UNTIL expr: DO loop termination.

GO TO expr: Transfer control to statement number 'expr.

GO SUB expr: Call subroutine at satement number 'expr'. Subroutines may be nested to eight levels.

RETURN: Return from subroutine.

INPUT var: Read value from console into variable.

INPUT \$ factor: Read string from console into memory beginning at address 'factor.'

LINK expr: Links to an assembly language subroutine which begins at address 'expr.' A "RET" instruction in this routine will cause continuation of the NSC Tiny BASIC program. hprogram.

³/₄expr: Interrupt processing definition. When interrupt number 1 or 2 occurs, NSC Tiny BASIC will execute a GOSUB beginning at line number 'expr.' If 'expr' is zero, the corresponding interrupt is disabled at the software level.

DELAY expr: Delay for 'expr' time units (nominally milliseconds. 1–1040). DELAY O gives the maximum delay of 1040 milliseconds.

STOP: Terminate program execution. A message is printed and the Microinterpreter returns to COMMAND mode.

Note the useful machine code LINK statement, ON 1 or 2 interrupt handler, and the DELAY capability, each of which make the 8073 BASIC ideal for control applications.

All arithmetic is performed in 16 bit signed integer format (-32768 to +32767) and the following operators and functions are provided:----

Arithmetic operators: addition, subtraction, multiplication, division

Relational operators: less than, greater than, equal to, not equal to, less than or equal to, greater than or equal to Logical operators: logical AND, logical OR, logical NOT

FUNCTION SUMMARY

(e) factor: The memory/peripheral address for memory-I/O read/write operations.

STAT: STATUS register.

TOP: Top-Of-Program address (first available memory address after end-of-program byte).

INC (x), DEC (x): Increment or Decrement a memory location (non-interruptable for multiprocessing).

MOD(x,y): Modulus function (remainder of x/y).

RND(x,y): Random number generator (in interval x,y).

There can be little doubt that the 8073 represents an excellent way into do-it-yourself microprocessor applications.

INTERFACING

The 8070 family all run from a single 5 volt supply and have onchip clock oscillators to keep external components to a minimum.

A full set of control lines are provided to allow the design of multi-processor systems sharing a common memory and I/O bus, as follows:—

NWDS	tri-state	output	similar	to	the	WR	line	of	8080	
	style pro	cessors								

NRDS tri-state output similar to the RD line of 8080 style processors.

NENIN when this input is low, the 8070 is allowed access to the bus. When set high by another device such as a second 8070 or a DMA chip the 8070 is denied bus access.

NENOUT This active low bus enable output provides a "busgrant" to other devices which require bus access.

NBREQ A bi-directional input/output which accepts bus requests from other devices as an input when set high, and generates an own-request when set low.

When required, for example in DMA or multiprocessor systems, the extensive set of internal 8070 bus control logic can save a considerable number of external gate packages.

Two interrupt inputs are available on the 8070 family of processors by utilising the two sense lines SA and SB, called INTA and INTB when used for this purpose. Both interrupt lines are dis-

abled when the IE flag in the status register is set to zero, and the SA SB flag bits can be used as program readable inputs.

When used as interrupts (IE = 1) INTA has higher priority than INTB, but both inputs are edge triggered to remove the need for external interrupt acknowledge logic. A high to low transition on either input causes the program counter contents to be pushed onto the stack, the program counter to be set to 0004H (INTA) or 0007H (INTB), and the IE bit set to zero. The programmer is responsible for storing appropriate BRANCH or JUMP instructions in locations 0004H and 0007H, so that access to interrupt routines stored anywhere in memory can be achieved. (In the case of the 8073, this is handled automatically by the Tiny BASIC interpreter of course.)

There are no special peripheral chips designed especially for the 8070 (or even the earlier 8060) family, but this is not a major drawback because most Intel 8080 peripherals can easily be used. Unlike the 8080 however, the 8070 family has no separate I/O address space and so the peripherals must be memory-mapped.

For serial I/O an external UART could be used, but a cheaper way is to implement a software UART using the sense and flag lines like that provided in the 8073 interpreter.

APPLICATIONS

The 8070 provides a useful compromise between the 8048/Z8 style "everything-on-board" single chip processors and the 6800/8080 style multi-chip solutions. It is probably not as good as the 68701 which can also provide this compromise, but it is, after all, a good deal less expensive!

I personally would not use the basic no-ROM 8070, because it has few advantages over other multi-chip processors like the 6802, but the 8073 with its on-chip BASIC interpreter is an excellent choice for hobby projects and can be recommended to everyone who wants to get into system design with the minimum financial outlay and risk. The design of a homebrew 8073 development system is quite straightforward, but for those who want to get started quickly there are a number of 8073 single board systems now available, such as the one designed by Essex University.

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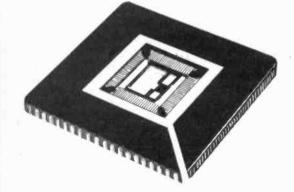
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Π.

MICROSTEPPER

"Freeze frame" your micro, instruction by instruction, to see what's going on during educational and debugging exercises.

PR



TRANSPUTER

Inmos claim the Transputer array processor will set new standards in ease of programming, provide maximum performance to the user, exploit future developments in VLSI within a compatible family and be able to form fifth generation systems with large numbers of concurrent computing elements. Next month we take a close look at the device.



Space Watch...

EUROPEAN SPACE AGENCY PROJECT

It is proposed that the ESA should submit designs for a space station for a joint enterprise with the United States. It is expected that it will require funding of some ten million pounds. ESA would retain the option of going it alone if the United States decided not to participate. It is, however, apparent that the radical re-designing necessary for use with a single shot launcher suggests that it is better to spend the money on launching by shuttle and concentrate on space stations. The experience with Ariane may also have influenced the decision. Greater-attention is now being paid to finance when dealing with these very large projects. Of course, it is also true that new techniques are more reliable and that hardware can be built to a high standard. The source of money has realised that risks are reduced by the methods in use, it must also be remembered that failures are less likely now so that insurance rates have fallen. It is true that precise anticipation of costs is dealt with in a more efficient way, since the guesswork of the past is almost gone. There is everything to gain as far as the ESA is concerned, since cooperation has proved successful in the past and the rapid advances in know-how are available for every country.

This new venture could well be the beginning of a successful co-operative. A significant part of this study is the long, hard look approach. In principle there are three parts, the modules, the platform units and the orbital manoeuvring units.

- Modules—These are pressurised segments and would be used for experiments and logistics. They could be adapted for crew living quarters, though it is possible that the USA might keep this within their own confines.
- **Platform units**—This study will look at unpressurised components and in the main this will refer to free-flying unmanned units that could be used for materials processing and the like.
- Orbital manoeuvring units—Studies of unmanned orbit transfer and space station service vehicles will be included. This valuation will be set at about £250,000 and will be carried out by the Messerschmitt-

Boelkow-Blohm consortium and Erno, with the help of AEG, Aeritalia, British Aerospace, Dornier, Fokker, Matra, Sebra, Sener and Aerospatiale. West Germany and Italy have already done work to this end (Columbia programme).

COLUMBIA PROGRAMME

The study carried out by Germany and Italy was called Columbus. This was undertaken as a special study and centres on a pressurised module, capable of being docked with a station, for long duration missions. Thus if could be used as a building brick for space stations. The module could contain a docking facility, complete with pressurised docking-berthing port, and one experimental air-lock. This module would be compatible with the shuttle space orbiter's payload bay, since it will be of the standard size. A service module using a portion of the Columbus module could be developed as a support/link vehicle to the space station. It would be equipped with a Solar array that could provide power when going to and from the station. There would be a small manoeuvring system. Crew transfer would be by a manned space vehicle.

Unmanned platforms would be derived from Eureka or the German SPAS to operate from the station as free-flying carriers of scientific experiments. It is evident that commercially viable processes may be achieved effectively, as the shuttle has proved, it is already attracting finance. This is clear with the fall in insurance rates and movement to get places in the launch queue. It would be wise, for the sake of the vital experiments that science needs to continuously carry out, that the two sides get together. One way of doing itself a commercial service would be for commerce to finance science in a more extensive manner. It is true that some of the large organisations do this, but what of the smaller commercial concerns whose work is essential in the new world to come? It is essential in the long run that cooperation is the operative word, and by cooperation that it means all the nations of the world would participate.

FUEL CELLS

In the Orbiter Columbia, each fuel cell has been tested to a peak power of 16kW. Hitherto this has been at the lower level of 14/15kW, the reason for this being that the power was much more in demand for the 54 workdays of the mission of Columbia 9.

The fuel cell power and water generation system contained one-third more than previously allotted. There are three stacks of 32 cells each in the vehicle. Earlier units flew with two stacks of 32 cells each. Each cell contains hydrogen and oxygen electrodes and an electrolyte of potassium hydroxide and water. The fuel cell normally will supply 2.12kW. At 2kW per cell, each stack can supply 32.5V and 61.5A of direct current. At 12kW it can supply 27.5V at a current of 43.6A. Water is recovered from the system which is used for drinking and cooling. The designers, United Technologies Power Systems, claim that the system can be developed to supply a 24kW output and a 5,000 hour operating lifetime.

HEARING AND SPACE

Spacelab has proved an old theory of hearing originally proposed in 1914. This was related to the semi-circular canals of the inner ear. It was found that if air at different temperatures was blown into the ear, then the sensation of turning was induced, even if the person was not moving. It was believed that the cause was the different density of the air and the fluid in the semi-circular canal. Spacelab have now confirmed this theory. The investigators used the eye movements of the astronauts to assess the temperatures. Another test, which was designed to determine the adaptation of the body to weightlessness, caused motion sickness for specialist crew member Byron K. Lichtenberg, requiring the termination of a life-sciences experiment.

A further test designed by an English psychology scientist, and mentioned in a recent *Spacewatch*, was designed for estimating different densities of pairs of balls which were visually of the same size.

A partially completed experiment was undertaken by Owen Garriott and Byron Lichtenberg; it was completed by Owen Garriott only because it caused Lichtenberg pain. The object was to discover the effect of weightlessness on reflexes and posture. The method was to drag the astronaut towards the floor and slightly shock him behind the knees during his descent. In order to minimise motion sickness the crew slowed all their movements during the mission. It is believed by Garriott that the movement of the head plays an important part in solving the problem. It certainly seems that some re-thinking needs to be done on these matters. Another experiment consisted of observing a field of dots which is rotating, followed by 35mm photographs of eye movements of the reaction of the subjects. This could not be completed owing to the failure of the photoflash. There will be a report published later and this will appear in a future issue of Spacewatch.

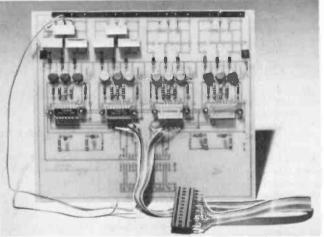
VENUS OBSERVED

There have been some reports of the Russian Space Explorer which are quite informative in that they confirm the finding of earlier space and ground-based instruments. The information is interesting for the planet has been the subject of two probes, Venera 15 and 16, which have been orbiting Venus since October. They have radar for investigating in close-up mode. It is claimed that resolution of one to two kilometres has been achieved. It needs a resolution of as good as at least one kilometre to assess the mountain elevations. If the resolution on these vehicles is less than one kilometre then we will have to wait for the publication of the results. The USA will not be ready to map at this level before 1988 or thereabouts. There are some pictures of the Soviet work around Venus. These are clear and show the general terrain, both craters and elevated land. There are large craters and considerable signs of volcanic activity. Near the pole it was noticeable that there is a large volcanic dome rising from an undulating terrain. One picture shows distinct lava flows, another shows a crater some 32×43 miles in size Such pictures are only available after penetration of the cloud cover. The Soviet orbiters are able to overcome this.

EXPANDING THE

PART FIVE SAM

STEPPER MOTOR CONTROL



FOR AROUND £29

HIS month, we first catch up on the input and output routines held over from Part 4, and then go on to look at two stepper motor control boards ideal for the robotics experimenter

Fig. 5.1. OUTPUT ROUTINE for displaying the state of ports in **Binary**

The following programs are not the most sophisticated, but it is hoped that they will help realise the potential of this series of interfaces.

- 05 PRINT"Shift/ClrHome":REM Clear screen
- 10 POKE 37138,255:REM Set DDR to required state
- **15 PRINT"DDR SETTING"**
- 18 PRINT PEEK(37138):REM Display DDR setting
- **19 PRINT:PRINT:REM Spaces**
- **20 PRINT"SET I/O REGISTER"**
- 30 INPUT X:REM To put a decimal value in I/O Register
- 35 IF X<0 OR X>255 GOTO 20:REM Must be 0 to 255 inclusive
- 40 POKE 37136,X:REM Enter value
- **50 PRINT"I/O REGISTER"**
- 55 PRINT PEEK(37136):REM Display it:PRINT:PRINT
- **60 PRINT"STATE OF PORTS"**
- 70 PRINT"P7 P6 P5 P4 P3 P2 P1 P0"
- 80 GOSUB 100:REM Go to Decimal to Binary conversion routine

90 GOTO 20:REM To reset I/O Registers 100 P0=X-INT(X/2)*2:REM Decimal to Binary conversion 105 X=INT(X/2) 110 P1=X-INT(X/2)*2 115 X=INT(X/2) 120 P2=X-INT(X/2)*2 125 X = INT(X/2)130 P3=X-INT(X/2)*2 135 X=INT(X/2) 140 P4=X-INT(X/2)*2 145 X = INT(X/2)150 P5=X-INT(X/2)*2 155 X = INT(X/2)160 P6=X-INT(X/2)*2 165 X=INT(X/2) 170 P7=X-INT(X/2)*2 175 X=INT(X/2) 200 PRINT P7:P6:P5:P4:P3:P2:P1:P0 **205 PRINT:PRINT** 210 RETURN:Return to line 80 in program

The conversion program is an integer arithmetic process and should therefore be possible on even the simplest machines. The principle is to divide the decimal figure by 2 and place the remainder in the least significant bit.

e.g. 255 Decimal becomes 1 1 1 1 1 1 1 Binary

-									
		P7	P6	P 5	P4	P3	P2	P1	P 0
255/2	Rem	0	0	0	0	0	0	0	1
127/2		0	0	0	0	0	0	1	0
63/2		0	0	0	0	0	1	0	0
31/2	**	0	0	0	0	1	0	0	0
15/2	99	0	0	0	1	0	0	0	0
7/2		0	0	1	0	0	0	0	0
3/2	99	0	1	0	0	0	0	0	0
1/2		1	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	1

Similarly, 131 Decimal becomes 10000011

		P7	P6	P5	P4	P3	P2	P1	P0
131/2	Rem	0	0	0	0	0	0	0	1
65/2	**	0	0	0	0	0	0	1	0
32/2	99	0	0	0	0	0	0	0	0
16/2	**	0	0	0	0	0	0	0	0
8/2	**	0	0	0	0	0	0	0	0
2/2	**	0	0	0	0	0	0	0	0
1/2	**	1	0	0	0	0	0	0	0
		1	0	0	0	0	0	1	1

Fig. 5.2. This program makes further use of changing outputs during the running of a program

05 PRINT"Shift/ClrHome":REM Clear screen 10 POKE 37138,255:REM Set DDR to required state **15 PRINT"DDR SETTING"** 18 PRINT PEEK(37138):REM Display DDR setting **19 PRINT:PRINT:REM Spaces 20 PRINT"SET I/O REGISTER"** 30 INPUT X:REM To put a decimal value in I/O Register 35 IF X<0 OR X>255 GOTO 20:REM (0 to 255) 40 POKE 37136.X:REM Enter decimal value 42 PRINT:PRINT **45 PRINT"INITIAL STATE OF PORT"** 50 Z=X:REM Put value of X into Z 55 GOSUB 200:REM To dec/bin conversion routine **60 PRINT"CHANGE OUTPUT?"** 65 INPUT Y:REM Enter decimal value 70 IF Y <0 OR Y>255 GOTO 60 72 Z=Y:REM Put value of Y into Z 75 GOSUB 200 80 INPUT"YES OR NO";AS:REM Examine output 82 IF AS="YES" GOTO 90:REM pattern before accepting 85 IF A\$="NO" GOTO 60 90 POKE 37136,Y:REM Satisfactory, so enter 95 PRINT:PRINT:PRINT:PRINT **100 PRINT^{*}I/O REGISTER**" 105 PRINT PEEK(37136):REM Display it:PRINT:PRINT **110 PRINT"STATE OF PORTS"** 120 PRINT"P7 P6 P5 P4 P3 P2 P1 P0" 130 GOSUB 200:REM To dec/bin conversion routine 140 GOTO 60:REM To reset I/O Registers 200 P0=Z-INT(Z/2)*2:REM Decimal to Binary conversion 205 Z=INT(Z/2) 210 P1=Z-INT(Z/2)*2 215 Z = INT(Z/2)220 P2=Z-INT(Z/2)*2 225 Z=INT(Z/2) 230 P3=Z-INT(Z/2)*2 235 Z=INT(Z/2) 240 P4=Z-INT(Z/2)*2 245 Z=INT(Z/2) 250 P5=Z-INT(Z/2)*2 255 Z=INT(Z/2) 260 P6=Z-INT(Z/2)*2 $265 \ Z = INT(Z/2)$ 270 P7=Z-INT(Z/2)*2 275 Z=INT(Z/2) 200 PRINT P7;P6;P5;P4;P3;P2;P1;P0:REM Display ports **205 PRINT:PRINT** 210 RETURN: REM Return to line 140 in program

Fig. 5.3. INPUT ROUTINE for changing the DDR register and displaying the state of ports in Binary

- 05 PRINT"Shift/Clr Home":REM Clear screen
- 10 PRINT"INITIAL DDR SETTING"
- 15 PRINT PEEK(37138):REM Display it
- **20 PRINT:PRINT**
- **30 PRINT"KEY THIS IN"**
- 35 INPUT D
- 40 Z=D:REM Put value of D into Z
- 45 GOSUB 200:REM Go to Decimal to Binary converter routine
- 50 PRINT:PRINT
- 60 PRINT"CHANGE DDR SETTING?"
- 70 INPUT"Y OR N";A\$
- 80 PRINT:PRINT
- 90 IF A\$="Y" GOTO 300:REM To bin/dec

- 95 IF AS="N" GOTO 100:REM Carry on
- 100 PRINT"I/O REGISTER"
- 105 PRINT PEEK(37136): REM Display it:PRINT:PRINT
- **110 PRINT"KEY THIS IN":PRINT:PRINT**
- 115 INPUT Y
- **120 PRINT"STATE OF PORTS"**
- 125 PRINT"P7 P6 P5 P4 P3 P2 P1 P0"
- 130 Z=Y:REM Put value of Y into Z
- 132 REM Note here that Vic 20 requires logic '0' for Input and
- 133 REM holds lines without inputs at logic '1' on simulator
- 135 GOSUB 200:REM To dec/bin conversion routine
- 140 GOTO 100:REM To reset display of I/O Registers
- 200 P0=Z-INT(Z/2)*2:REM Decimal to Binary conversion 205 Z=INT(Z/2)
- 210 P1=Z-INT(Z/2)*2
- 215 Z=INT(Z/2)
- 220 P2=Z-INT(Z/2)*2
- 225 Z=INT(Z/2)
- 230 P3=Z-INT(Z/2)*2
- 235 Z=INT(Z/2)
- 240 P4=Z-INT(Z/2)*2
- 245 Z=INT(Z/2)
- 250 P5=Z-INT(Z/2)*2
- 255 Z=INT(Z/2)
- 260 $P6=Z-INT(Z/2)^{*2}$
- 265 Z=INT(Z/2)
- 270 P7=Z-INT(Z/2)*2
- 275 Z = INT(Z/2)
- 200 PRINT P7;P6;P5;P4;P3;P2;P1;P0:REM Display ports
- 205 PRINT:PRINT
- 210 RETURN:REM Return to line 140 in program
- 300 INPUT"ENTER BIT PATTERN :";B\$:REM Binary to Decimal converter
- 310 IF LEN(B\$) <> 8 THEN PRINT"8 BITS PLEASE"
- 315 GOTO 300:REM Do again if wrong
- 320 M=0:N=0
- 330 FOR P=8 TO 1 STEP-1:N=N+1
- 340 M=M+VAL(MID\$(B\$,N,1))*2 (P-1)
- 350 NEXT P
- 360 PRINT B\$;"=";M
- 365 PRINT"KEY THIS IN"
- 370 INPUT M:POKE 37138,M
- **380 PRINT"STATE OF DDR"**
- 390 Z=M:GOTO 45:REM Return to program

STEPPER MOTOR INTERFACES

The next stage in this series concerns interfacing the computer with stepper motors, and their application in practical experiments. Two stepper motor controllers are described, with designs for two p.c.b.s which will each accommodate four controllers. This enables experimentation with XY movement involving two axes, or simple robotics having four axes, as opposed to the usual five or six axes normally found on commercial controllers, but of course, at a fraction of the cost of the latter.

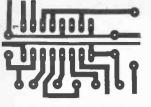
The SDB520 i.c. is chosen for its versatility and power handling capabilities, whilst the SAA1027, though more limited in its application, has been a popular device in schools and colleges for several years.

The prime consideration in interfacing is always the safety of the host computer. The SDB520 and SAA1027, because of their different inherent characteristics, are treated differently where the method of electrical isolation from the computer is concerned. This is explained within the text covering the individual devices.

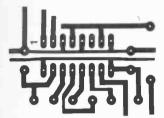
Stepper motors are available, suitable for such a wide variety of applications that it is impossible to report on them to any great extent in the space available here. A useful

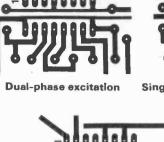
Fig. 5.7. P.c.b. configurations (IC1-4) for stepper motor control 1

4-PHASE MOTOR LINKS



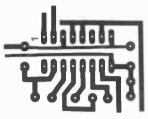
Single-phase excitation







Single/dual-phase excitation



3. DHASE **MOTOR LINKS**

Single-phase excitation

Dual-phase excitation

source of very cheap, yet top quality low and medium power motors is ex-equipment. This source often provides much of the hardwear required for constructing a functional machine. A visit to an Amateur Radio rally is well worth the entrance fee, as many of the advertisers in Practical Electronics and Practical Wireless attend with such bargain packages. More important, in general, these people are not just salesmen, but practical constructors who have tried the equipment out for themselves, and are free with advice on wiring and serviceability. Some general comments are therefore included which are applicable to the article.

Some programming hints are included, suggesting methods of "stepping" the motors clockwise, counterclockwise, and for angular movement where more than one motor is being operated.

Those who have constructed the l.e.d.s and switches board can use it for development of their programs as with any other output program.

THE SDB520 DRIVER BOARD

The first p.c.b. described uses the versatile SDB520 Stepper Motor Driver i.c., which can be used with 3-phase or 4phase motors. In addition to this, the chip enables the use of either type of motor in single, dual, or single/dual phase excitation.

In order to accommodate all these functions, connections from pins 3, 4 and 5 have been left open. In all modes, pins 7 and 10 are connected via a 2k2 resistor to the +5V d.c. supply, whilst pins 3, 4 and 5 are either individually coupled with these, or taken to ground. Provision has also been made to mount capacitors between motor coils 1 and 2, 2 and 3, 1 and 3 for 3-phase motors and 1 and 3, 2 and 4 for 4-phase motors.

Opto isolated output from the computer is provided, a feature that the author normally recommends. However, in the case of the SDB520, it is well protected internally against short circuit, making opto isolation at low motor voltages and current, less necessary. It is provided for the less experienced constructor, and those who may have larger motors available.

The SDB520 uses the +5V d.c. supply from the computer, provision for external supply being made for use with computers other than the Vic 20. The outputs from the driver turn on their associated transistors sequentially, allowing current to flow through the relevant motor coil. The transistors used on the board are BFY51, 2N3053 or similar 0.7W NPN transistors that can handle up to 1A of current.

Single/dual-phase excitation

COMPONENTS

STEPPER MOTOR CONTROL 1

Resistors

R1,2,6,7,11,12,17,18 2k2 (8 off) R3,4,5,8,9,10,13-16, 100 (14 off) 19-22 R23 See note All resistors 1W 5%. R23 (if necessary) depends upon motors/supply voltage, and is not mounted on the board.

Capacitors

2µ2 (4 off) C1,6,11,15 10µ (4 off) C2,7,12,16 C3,4,5,8,9,10,13,14,17,181µF poly (10 off)

Transistors & Diodes

D1-14 TR1-14

IC1-4

1N4001 (14 off) 2N3053 or similar (14 off)

Integrated Circuits

SDB520 (4 off)

COMPONENTS . . .

STEPPER MOTOR CONTROL 1 Opto-coupling option (shown in comp. layout)

Resistors	
R23-26,31-34	
R27-30,35-37	

Diodes

D15

470 (8 off) 12k (8 off)

1N4001

ILQ74

Integrated Circuits 105.6

Should there be a need for greater current handling, 2N3055 transistors can be mounted externally on heatsinks. Motor voltages are typically 12 to 24V d.c. and might require a small value 50W wirewound resistor at the common positive motor supply to correct L/R ratio. This information should be available with the motor.

The p.c.b. is single-sided fibre-glass, approximately 165×148 mm, and requires short links on the upper surface. As mentioned earlier, in order to increase the versatility of the board, connections have to be made between pins 3, 4 and 5 and ground, or commoned with pins 7 and 10. A solder blob is all that is required, and this can be carried out neatly by using a single strand from multi-strand cable to bridge the gap and allowing solder to flow over it from side to side.

Pulses are supplied to two inputs, CD Counter clockwise, at pin 1 and CU Clockwise, at pin 2. A change from Low to High and back to Low will trigger the i.c. The inputs are designed with high noise margin, and comprise a Schmitt trigger circuit.

OC at pin 3 selects 3 phase, Low, or 4 phase, High, operation. EA and EB on pins 4 and 5, comprise the mode switching terminal.

- EB EA Mode
- 0 0 Line drive facility
- 0 1 Single phase excitation
- 1 0 Dual phase excitation
- 1 1 Single/dual phase excitation

Mo at pin 6, provides a sequence monitor, low, when counter content is 000.

OFF 01.3 on pin 7 and OFF 02.4 on pin 10 provide excitation OFF or line drive input terminal, when terminals become Low without relation of sequence content, when output terminals are = 0. At pin 8 is the 0V supply terminal. Vcc2 at pin 9, the output driver power supply.

Output driver terminals are at pin 11, 4, pin 12, 2, pin 13, 3, and pin 14, 1. A clamping diode is inserted in the output.

R at pin 15 is the Reset input terminal, tied to Vcc via a $2k^2$ resistor. Vcc1 at pin 16 is the power supply for the logic circuit.

COMPONENTS	
STEPPER MOTOR CONTR	OL 2
Resistors	
R1-4	470 (4 off)
R5,6,11,12,21,22,27,28	12k (8 off)
R7,8,13,14,23,24,29,30	4k7 (8 off)
R9,15,25,31	100 (4 off)
R10,16,26,32	150 ½W (4 off)
All resistors $\frac{1}{4}$ W 5% unless other	erwise stated.
Capacitors	
C1-4	100n (4 off)
Diodes	
D1	1N4001
Integrated Circuits	
IC1.4	ILQ74 (2 off)
IC2,3,5,6	SAA1027 (4 off

USE OF OPTO ISOLATORS

Those who have followed this series will note that the l.e.d.s in the opto isolators are turned on by making the cathode low relative to the power supply. This means, without the inclusion of inverters, that the logic is incorrect for an output on the Vic 20. For the purists this is overcome by complementing the binary pattern required at the output port and placing this value in the I/O Register.

Output required		10101010	Decimal 170
Complement		01010101	Decimal 85
	Total	11111111	255

The easiest way, of course, is to treat the outputs required as inputs.

SDB520 DRIVER EXCITATION SEQUENCE

3-Phase motor excitation

	Single phase					Dual phase							Single/dual phase						
0 1 2	01 0 0	02 0 1 0	0 0 1	04 0 0	CCW ↓ CW	0 1 2	1 0 1	02 1 1 0	03 0 1	0 0 0	ccw ¢₩	0 1 2 3 4 5	01 1 0 0 0	02 0 1 1 1 0 0	03 0 0 1 1 1	0 0 0 0 0 0 0	CCW CW		

4-Phase motor excitation

	Single phase					Dual phase							Single/dual phase					
0	01	0	0	04	CCW	0	01	02	03	Q4 0	CCW	n	01	02	-	04	CCW	
1	0	1	0	0	Î	1	0	1	1	0	Î	1	1	1	0	0	Î	
2 3	0	0 0	1 0	0 1	cw	2 3	0	0 0	0	1	cw	2 3	0	1	0 1	0 0		
												4 5	0	0 0	1	0		
												6 7	0	0 0	0 0	1 1	cw	

Sequence monitor (pin 6) is logic 0 at sequence stage 0 and logic 1 at other stages of sequence.

Pads are provided on the p.c.b. should it be wished to monitor the outputs whilst developing programs and setting up motors.

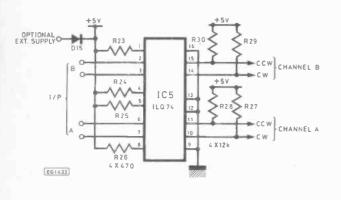
The monitor is active low, therefore when it becomes active at the beginning of each sequence, the cathode of the monitor l.e.d. is pulled down relative to the 5Vd.c. supply and comes on.

THE SAA1027 DRIVER BOARD

The SAA1027 is intended for pulse to step control of fourphase two stator motors. It is capable of driving a motor winding load of 350mA per phase and is encased in a 16 pin dual in line plastic package.

Pulses are supplied to a single input, whilst the direction of rotation is controlled by a voltage level applied to a gate input. A further input sets the four output stages. Supply voltages can be between 9.5 and 18Vd.c., but a single 12Vd.c. power supply is normally used to operate the driver

Fig. 5.4(a). Circuit diagram of SDB520 driver (3-coil motor type) annotated as in the p.c.b. layout shown below (channels A and B)



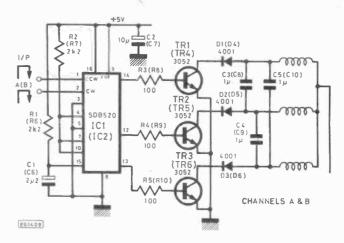


Fig. 5.5. P.c.b. layout of stepper motor control board 1. SDB520 type (actual size). This is a versatile board, designed to accommodate-various component configurations. For example, the ILQ74s (IC5 & IC6) opto-isolators are optional

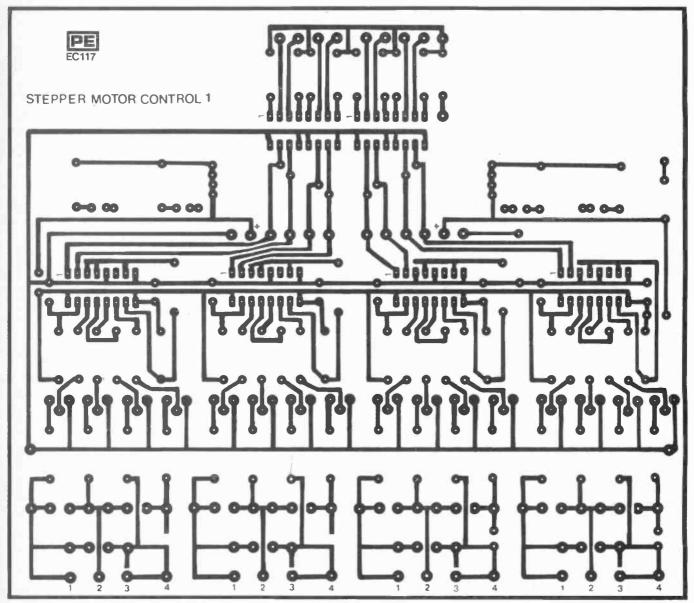
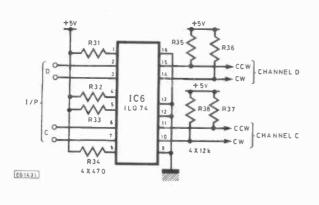


Fig. 5.4(b). Circult diagram of SDB520 driver (4-coil motor type) annotated as in the p.c.b. layout shown below (channels C and D)



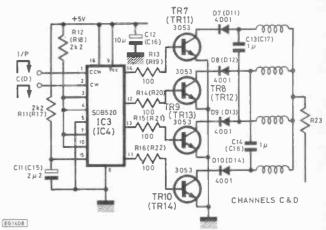
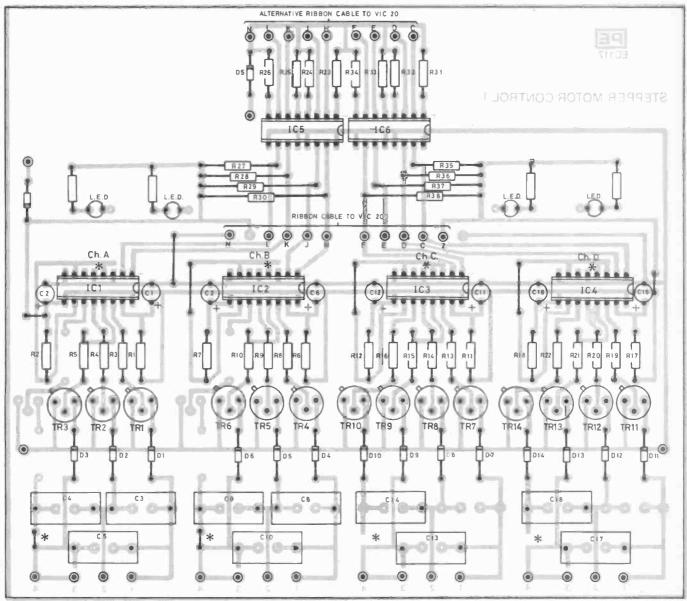


Fig. 5.6. Stepper motor control board 1 component layout, shown with channels A & B dedicated to the 3-coil configuration, and channels C & D dedicated to the 4-coil configuration. Asterisks draw attention to the link areas that allow reconfiguration. The I.e.d.s allow optional data signal monitoring



EG1427

i.c. and the motor. The output drivers (pins 6,8,9,11) are open collector. The breakdown voltage is 18Vd.c. and this must not be exceeded.

- **Pin connections**
- (1) no connection
- (2) Set input S
- (3) Direction input (CW/CCW) R
- (4) Bias resistor B (positive supply)
- (5) Ground (negative supply)
- (6) Q1 (output)
- (7) no connection
- (8) Q2 (output)
- (9) Q3 (output)
- (10) no connection
- (11) Q4 (output)
- (12) Ground (negative supply)
- (13) VD (positive supply)
- (14) VP (positive supply)
- (15) Trigger input T
- (16) no connection

INPUTS

The three inputs are controlled by applying high or low voltage levels to the terminals. The high level voltage can be between 7.5 and 18Vd.c. (12Vd.c. typical) and is normally equal to, but not greater than, the voltage on pin 14. Input current is high, typically 1µA. The low level voltage can be between 0 and 4.5Vd.c. maximum. Low level current is typically -30µA per input.

TRIGGER INPUT

The voltage on T, pin 15 is normally high when not being pulsed and is held at Vs via a 4k7 resistor. A change from high to low and back to high will trigger the i.c. The motor is connected to the output stages on the positive edge, low to high of the pulse.

SET INPUT

Pin 2, S is tied to Vs, enabling all outputs.

DIRECTION INPUT

Applying a high level to pin 3 causes the motor to be stepped CCW, whilst a low level to pin 3 causes the motor to step CW. The input is tied high via 4k7 resistor for maximum noise immunity.

BIAS RESISTOR

RB can be calculated, first from supply voltage and motor coil resistance to arrive at IQ. Then, by reference to graph, IB and VS permits calculation of RB.

When motors with current of 350mA (max) per winding are used, the bias current to pin 4 should be 80mA (max).

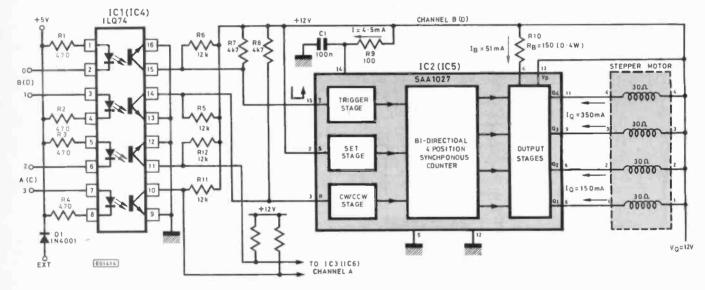
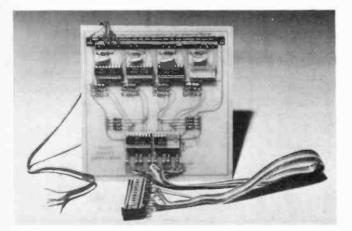


Fig. 5.8. Circuit diagram of the SAA1027 type driver board. There are four identical channels. Channel B is shown here



CHANNEL

A	B	C	D
	R1		R17
- 1	R2	-	R18
R3 4	-	R19	
R4	-	R20	_
R11	R5	R27	R21
R12	R6	R28	R22
R13	R7	R29	R23
R14	R 8	R30	R24
R15	R 9	R31	R25
R16	R10	R32	R26
C1	C2	C3	C4
IC3	IC2	IC5	1C6
IC	1	IC	4

There are four channels. The

circuit diagram shows a single channel, and this table indicates the equivalent components for the other channels.

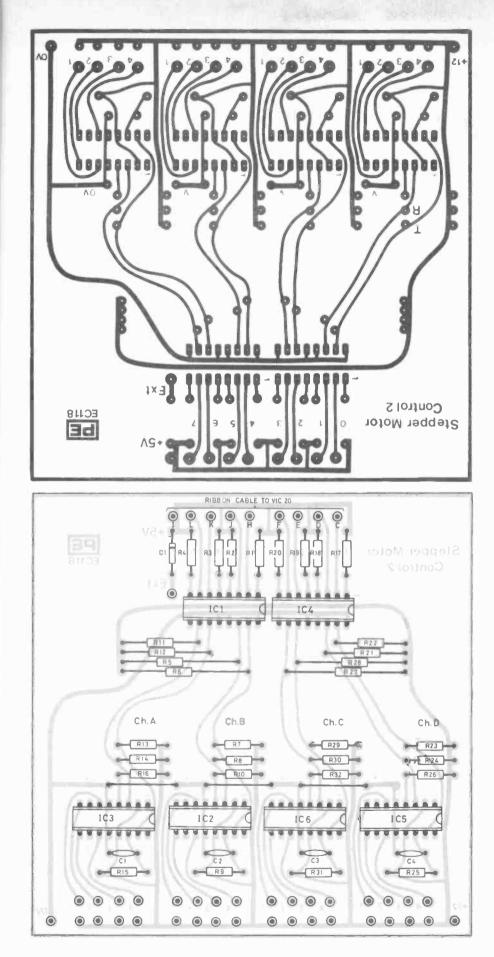
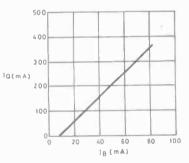


Fig. 5.9. P.c.b. layout of stepper motor comtrol 2. SAA1027 type (actual size)

A typical surplus/ex-equipment stepper motor





Bias current and output current relationship of SAA1027 output stage

Fig. 5.10. Component layout of stepper motor control 2



Likewise, when the output current is 50mA, bias current should be 20mA. A linear graph plotted between these values is shown on page 43.

The R/C network at pin 14 stretches the pulse from trigger input, pin 15, to a length detectable by the trigger stage.

OUTPUTS

The switching sequence of the four phases is controlled by the logic part of the circuit and the four output stages, Q1 at pin 6, Q2 at pin 8, Q3 at pin 9 and Q4 at pin 11 are protected against transient spikes by integrated diodes.

OPTO ISOLATION

It is usual to use TTL Buffers between the computer and the SAA1027, but due to the danger of the maximum 18Vd.c. being exceeded, and added susceptibility of the i.c. to overheating and breakdown, it was decided to use opto isolation.

The collector of the transistor in the opto isolator is held high, at logic "1" via the 270k resistor connecting it to the power supply. When a logic "0" at the output port sinks the l.e.d. and turns it "on", the transistor is turned on also, causing the collector to go low. When the output changes back to logic "0" the l.e.d. turns off. The transistor also turns off, bringing the collector once again to high, causing excitation and creating a pulse.

Should overheating be experienced, clip-on d.i.l. heatsinks are available from most advertisers.

This board is much smaller than the SDB520 board because the driver is complete in itself and requires no external components beyond the capacitor and resistors mentioned. It is made on a 120mm square of single sided fibre-glass p.c.b. Short links are required on the component side to connect the ground rails. Provision is made for an external 5Vd.c. power supply if used on a computer other than the Vic 20.

STEPPER MOTORS

A summary of various descriptions of a stepper motor would be "a direct digital motion control device that converts electrical pulses into discrete mechanical rotational movements. It possesses the ability to rotate in either direction, as well as start and stop at various mechanical, rotational positions. Its shaft moves in precise angular increments for each input excitation or step. The stepper motor allows control of position, velocity, distance and direction".

STEPPING

Due to the nature of its construction, unlike a normal free running motor, a stepper motor moves through a precisely defined arc of a complete revolution for each pulse and is

BAZAAR

PYE AM25B Crystal, 4 Metres, 70.26MHz, Tx, Rx, v.g.c., £12. DX200L receiver covers all bauds to 30MHz, £75. Mr R. A. Pearson, Tel: Swansea 582941.

WANTED ZX Spectrum any condition, 1-6K or 48K. Tel: Aberdeen (0224) 742358, after 6.30p.m. Alan Stewart, 11 Straik Place, Elrick, Skene, Aberdeenshire, AB3 6TN, Scotland.

MAPLIN, 3800 synth parts from unfinished synth, PCB's, components, keyboard, pots, etc. £95. Tel: 01-393 1577 (evenings). V. Carter, Fitznells, 2 Chessington Road, Ewell, Epsom, Surrey, KT17 1TF.

HAVE Chinon, Super 8 sound cine camera, many extras. Swop multi band scanner or sell £120. Tel: (0734) 340052. Mr E. Chopin, 34 Paddock Heights, Twyford, Berks, RG10 0AR. **MZ80K**, I/O Box, unused £70. Serial Board £50. Bidirect 80 Column Printer £220. Wanted Twin Fdos for Sharp NIZ 80K. Phone R. H. Pearce, 8 Holly Oak Road, Southampton, S01 6GD (0703) 788278.

ZX81 + keyboard and 32K RAM pack £45 o.n.o., includes manual, all leads, etc. D. Snowdon, 124 Walpole Road, S. Woodford, London, E18 2LL. Tel: 01-504 0565.

STEREO Amp and preamp transistor. Three inputs. 25 watts each channel output, working, but no case. £20, p.p. £5. L. T. Hill, 14 Rothesay Terrace, Bedlington, Northumberland.

RELAYS new 24V d.p.d.t., open type boxed (20). Labgear television distribution amplifiers, new boxed (2). Offers. Tel: R, Yates (0342) 832078 Lingfield, Surrey.

WANTED ZX81 in good working condition. Will

held in that position until the next pulse, which moves the rotor through the same angle of rotation. Small motors usually come in 3 or 4 phase types and the number of steps to a complete revolution varies greatly, typically from 4 to 90, or angular movements varying from 90 degrees to 4 degrees.

SEQUENCE

Each phase is excited sequentially, the rotor moving in precise steps, in the same direction, for each excitation. Reversing the stepping sequence of the phases reverses the direction of movement of the rotor by the same precise angle. These processes are controlled by the internal logic of the stepper motor driver i.c.

ACCURACY

Unlike a normal motor, which keeps running after removal of power until stopped by friction, the stepper motor stops at a predictable position. Any errors of angular position are restricted to each single movement and are nonaccumulative. An error of 1 degree in each and every step, no matter how many steps are performed, will be an error of just 1 degree at the end of a cycle. Accuracy varies from 0.01 degree for small steps to 5 degrees for large steps. Obviously, for precise positioning, the greater the number of steps the greater the accuracy.

In dual-excitation mode, two coils are excited simultaneously. This stops the motor in a position half-way between normal stopping positions, but because of increased holding torque gives consistent accuracy.

HOLDING TORQUE

At standstill, the torque required to deflect the motor a full step is called the Holding Torque. This is normally higher than the running torque and acts as a strong brake in holding the load. The higher the holding torque the more accurate the position of the rotor. Most stepper motors will operate at much lower voltages than that recommended by the manufacturer, but with decreased holding torque and therefore decreased accuracy. A similar situation can arise with increased step frequency due to the fact that the rise time of the coil limits the percentage of power actually delivered to the motor. The result can be incorrect starting or loss of steps. This effect is sometimes compensated for by increasing the supply voltage and including a series resistor to correct the L/R ratio of the circuit as depicted in the SDB520 4-phase schematic.

Next Month: Applications and control of stepper motor boards. Also, DAC and ADC boards.

pay up to $\pounds 30$ delivered in Sweden. Mr. L. E. Abrahamsson, Kovra 3184, S-84044 Oviken, Sweden,

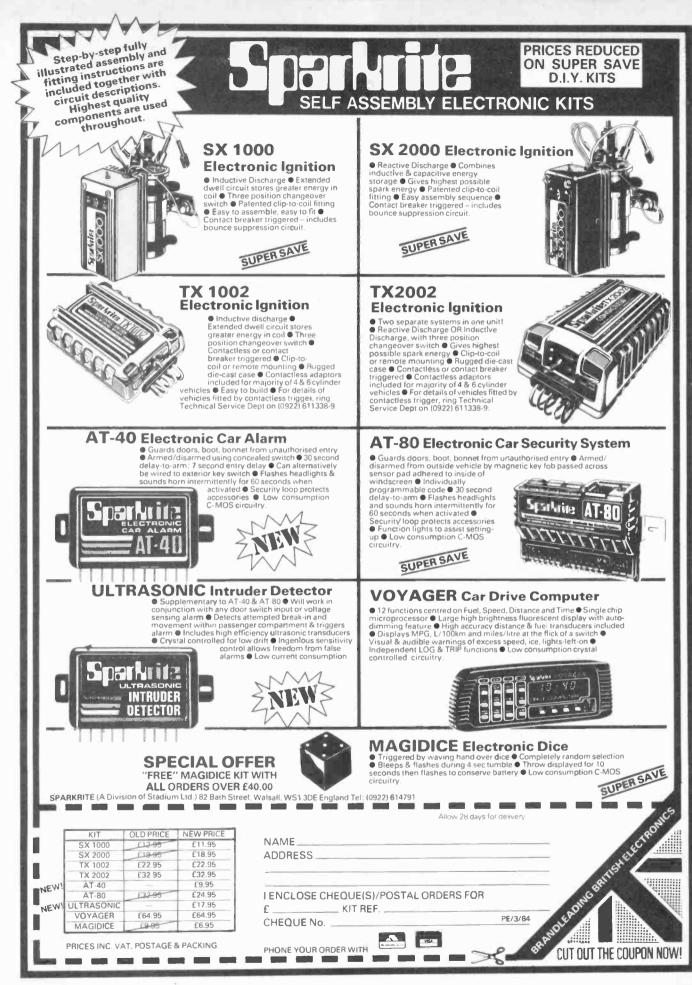
WANTED UK101 p.c.b. or any discarded 101's, working or not. Fair price for suitable boards. C. Hellen, Tel: Wivenhoe (020622) 5671.

FORGESTONE 400 TV 22" with spare decoder and manual. Offers Tel: 0634 812629. P. Topping, 10 Applery Close, Rochester, Kent.

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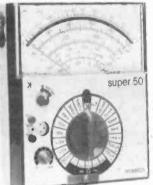
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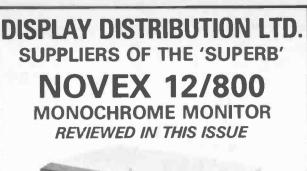
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MONITORS... for Home Computers

MICHAEL TOOLEY BA DAVID WHITFIELD MA MSc CEng MIEE

PART TWO

THIS month we complete our brief look at monitors for home computers by reviewing two current models. The two units tested are representative of the most popular types of monitor for home computing: a high resolution monochrome monitor, and a medium resolution RGB monitor. The monitors have been reviewed primarily from a user's viewpoint, and the usual technical tests have been largely replaced by an extended practical evaluation with a BBC Micro.

NOVEX MONOCHROME MONITOR

First Impressions The Novex 12/800 is a transistorised custom-designed monochrome monitor from Taiwan. It comes well packed, and is supplied complete with a manual and a phono-to-phono lead. The manual, although rather quaintly worded in places, is well illustrated and provides all of the necessary information.

The unit has a 12-inch green (P31) phosphor display tube, and is attractively packaged in a two-tone beige and brown steel case measuring approximately 30×29×30cm. The colour scheme and styling are pleasing to the eye, and are a good match for Apple or BBC computers. The tube has a moulded surround which includes an illuminated mains switch and a door concealing a number of controls. The monitor weighs approximately 8kg, and is mounted on rubber feet. The video connectors, mains lead and two slide switches are located on the rear panel.

Front Panel The screen surround includes the illuminated mains switch, and a button to release the door concealing the preset adjustments and controls. The two screwdriver preset adjustments are for picture height and width. These are factory adjusted for optimum setting, and should therefore need little or no attention. The remaining controls are intended for user adjustment and allow setting of brightness, contrast, horizontal hold, and vertical hold. All of the presets and controls are clearly labelled.

The four controls all have a useful range of adjustment. Correct setting of the two hold controls is well described in the manual. The adjustment of contrast and brightness is not quite so well covered in the manual. The best way to perform the adjustment was easily found to be as follows. Both controls should be turned fully clockwise for the brightest possible picture; the raster should then be clearly visible. Next the brightness is reduced until the raster just disappears. Finally the contrast should be adjusted to produce an acceptable picture; the actual setting here is a matter of personal preference. Once set, little adjustment to any of the controls is necessary, and then usually only to take account of different ambient lighting conditions.

Rear Panel The mains power lead enters through a securing grommet on the monitor's rear panel. The length of this lead is a rather miserly 1.5 metres (in common, it must be said, with much other equipment); no plug is provided.

Also on the rear panel are two miniature slide switches and two phono **so**ckets, all clearly labelled. The reviewers' first reaction to the use of phono sockets was to look around for a spare pair of BNC sockets to fit in their place, but this again is a matter of personal preference.

The video input signal is connected to one of the phono sockets, and the second socket is internally connected to the input socket. This provides a video output signal which is useful for loop-through connection to more than one monitor. In order to be able to obtain the maximum video bandwidth, the video signal should be terminated (by 75 ohms) at the last monitor in the chain. A switch is provided to allow the signal to be left unterminated (high impedance for an intermediate unit), or terminated in 75 ohms (for the last or only monitor). In practice, the two phono sockets are interchangeable, and are labelled merely for convenience.

The second slide switch on the rear panel is labelled 'GRAPHICS' and 'DATA'. This allows the monitor's performance to be separately optimised for high resolution graphics and 80-column text.

Inside The Case On the rear of the case is a removable panel bearing warnings of electrical shock risk, and advising of no user servicable components. The internal construction is based on a large single-sided p.c.b. which is securely mounted on the base plate. This contains the majority of the components, and is screen printed for ease of component identification. Mounted on the base of the tube is a much smaller p.c.b. which carries the video amplifier. This is a common practice to minimise stray capacitance, and hence allow the the maximum video bandwidth to be retained.

The internal construction is very compact, and represents a utilitarian appearance in interesting contrast to the external styling. The unit is clearly a custom designed monitor, rather than a modified television chassis. The power supply incorporates a mains transformer, and has no provision for operation from an external 12 volt d.c. supply.

Looking inside the case from the rear, there are three



COMPUTING

preset controls mounted on the edge of the main circuit board. These turn out to be (left to right): picture height, focus and black level adjustments. These are factory presets which are not intended for user adjustment.

Picture Quality In order to evaluate the picture quality, the monitor was connected to the video output of a BBC Micro. Tests were conducted using 20, 40 and 80-column text, and high resolution coloured graphics displays. The video signal was terminated by 75 ohms.

After using a black and white television, the first thing that strikes the user is the clarity of the display. The difference between the display on a monochrome television, and the display on the monitor, has to be seen to be believed. In fact going back to the television display after a number of hours of use with the monitor can cause acute frustration. The temptation is to keep trying to adjust the televison tuning to regain the 'lost' definition; a substantially fruitless exercise. It is on 80-column displays, however, that the difference is most apparent. The test is easily readable on the monitor, whereas on a television display, prolonged viewing is tiring.

The other factor which is quite noticeable is that the green phosphor has a significantly longer persistence than the white phosphor. This is quite typical of the P31 phosphor, and probably contributes to the strain-free display which can happily be viewed for many hours.

In 80-column mode the use of the 'graphics/data' switch eventually becomes clear. When switching from 'graphics' to 'data', very close observation of the screen shows that the leading edges of all characters become very slightly emphasised. This does not have any noticeable effect except on a very narrow vertical line (e.g. the centre upright of 'W'), which then becomes more clearly visible. Such lines represent very high video frequencies, and often result in a slightly fainter display, although remaining quite visible. The 'data' position appears to compensate for this effect by altering the time constant of the video amplifier to induce slight ringing. The end result is to allow the display of 80-column text to be outstandingly clear, but without compromising very high resolution graphics displays.

The overall display shows good linearity in both horizontal and vertical directions. There is no evidence of power supply problems with the display brightness, and the unit runs cool even after many hours of use. The picture focus is generally excellent, with only slight defocussing evident in the top right corner of the display. This would normally go unnoticed in everyday use. The display resolution is quoted at 1000 lines in the screen centre, and 800 lines in the corner. This is more than adequate for 80-column text, and in practice individual pixels can be distinguished (the BBC Micro uses 640 pixels per line in 80-column text mode).

The BBC Micro produces displays in up to eight colours, although black is not really a colour as such. When displayed on the Novex monitor, these colours appear as shades of green, but they are still distinguishable by virtue of their different brightness levels. In order of decreasing brightness, the colours appear as:—

WHITE	(Brightest)
YELLOW	
CYAN	
GREEN	
MAGENTA	
RED	
BLUE	
(BLACK)	(Darkest)

As delivered, the review unit was unable to display blue at all, and had some difficulty with red. However, after adjustment of the black level internal preset (not a user adjustment), all of the colours were visible and distinguishable.

VERDICT The overall impression after prolonged use (including preparing this review!) is excellent. The monitor is neat, compact, pleasant to use and fuss-free. It is ideal for word processing and any high resolution applications, and would make a very welcome addition to any home computer system.

CABEL RGB MONITOR

First Impressions The Cabel 370A is an RGB colour monitor which is supplied complete with a BBC Micro compatible RGB video lead. The unit as delivered has its colour settings optimised for the BBC Micro, and is extremely well packed in a double box. A single A4 instruction sheet is supplied which gives basic operating information, but this appears to have been rather hastily prepared, and contains a number of typographical errors. Hopefully this is an interim measure, pending production of a more substantial manual.

The monitor has a 14-inch Mullard colour tube with a dot pitch of 0.65mm, and is packaged in a strong moulded case with an integral combined carrying handle and ventilation slot. The colour scheme is beige (case body) and black (front panel). It must be said, however, that the overall styling is spoilt by poor design of the front panel. This is a great shame because the effect could have been so much better with only a little more effort and attention to matters of styling and ergonomics. As it is the two front panel controls (round knobs) are too close together, and in sharp contrast to the (square) mains switch. The mains indicator is a small (round) l.e.d. in the middle of a large blanking plug filling the hole occupied on previous models by the video connector. This said, we should remember that the prime function of the unit is to produce colour displays.

The overall dimensions of the monitor are probably the smallest possible for a unit using a 14-inch tube, and are approximately 39×36×41cm. The case itself tapers from front to back, and also inclines the screen usefully backwards to assist viewing. The height of the screen above the bench would allow it to stand behind many micros, in the (unlikely) event that sufficient bench space is available. The best alternative viewing position involves placing the monitor beside the computer. The unit weighs approximately 13kg, and is mounted on four rubber feet. All controls are on the front panel, and all leads connect at the rear.

Front Panel The front panel contains the mains switch and power indicator. The indicator provides a useful indication of whether the automatic power supply shut-down



circuitry has operated. Two controls allow adjustment of brightness and 'interlaceing'. The latter control seems wrongly labelled (and spelt!), and behaves as a contrast control; it certainly has no effect on picture scan interlacing. Both controls work well and have a useful range of adjustment.

Rear Panel The mains power lead enters the unit through a grommet on the rear panel. This lead is approximately 2 metres long (still a little on the short side, but a useful length), and has a fitted 13A plug. The video input is via a 6pin DIN socket, wired to be compatible with the BBC Micro. The RGB input is terminated in 75 ohms, and automatically switches to accept inputs with positive or negative sync. The rear of the case contains ventilation slots, which are numerous enough to provide a good flow of air, yet narrow enough to prevent the intrusion of foreign objects.

Inside The Case At the rear of the case is a label which warns of electrical shock hazard if the cover is removed, and indicates that there are no user serviceable parts inside. Access is provided to ten preset adjustments through small holes in the base and rear of the case, obviating the need to remove the cover. The adjustments provided are for: red/green/blue input sensitivity, horizontal/vertical shift, field sync/linearity/amplitude, line width and linearity, and focus. The unit is provided fully aligned, and no adjustments were found to be necessary to the review sample.

The case itself is of substantial construction, and is removed by unscrewing the four feet. The internal construction of the monitor is extremely impressive, and is based around a standard Mullard colour monitor chassis, to which the case is attached. The chassis is built around the cradle which supports the colour tube. The tube itself is a standard television style 90-degree tube. The main circuit board is mounted in the base of the cradle, and is neatly laid out for automatic component insertion. The three (red, green, blue) video amplifiers, and the focus control, are mounted on a smaller second board mounted on the tube base. Signal connections between the sub-assemblies are by means of multiway cables/connectors. All in all, a very well constructed unit incorporating the very latest technology.

Picture Quality The picture quality of the Cabel monitor was evaluated by driving it from the RGB output of a BBC Micro. The tests involved 20,40 and 80-column text, and high resolution coloured graphics.

When set against a standard, well-adjusted domestic colour television, the picture quality from the monitor can only be described as excellent. The difference has to be seen to be believed. The saturated, stable colours which are obtained are a delight to observe, and it is possible (using only the front panel controls) to obtain a colour display to suit all tastes. The usual problem is that no two people can ever agree on the subjectively 'correct' settings for any colour display; the reviewers certainly disagreed! The important point, however, is that the range of adjustment available on the monitor is more than enough to cater for all tastes. Whatever your preference, the final picture quality is excellent.

When used for text displays, the CE370A produces perfectly acceptable and stable displays for 20 and 40-column text. However, the 10MHz bandwidth causes a few problems with 80-column text. The actual horizontal resolution quoted for the display is 430 pixels per line, and the BBC Micro uses 640 pixels per line for 80-column text. The resulting text is still quite readable, but not pleasantly so for prolonged periods. A viewing distance of approximately 1.2 metres (eye-to-screen) was found to be the optimum for 80column text. If contemplating frequent and prolonged use with 80-column text, the higher resolution CAT370 (22MHz, 0.65mm dot pitch, 430 pixel) or HR370 (22MHz, 0.3mm dot pitch, 640 pixel) models should be considered as possible alternatives.

The ideal, and the recommended, position for the monitor is behind the computer console. This has the advantage of increasing the separation between the eye of the user and the screen. The bottom of the screen is then 9cm above the bench level, and this means that it is not obscured by most micros. The screen size should be considered when deciding where to position any monitor; a large screen too close can be as bad as a small screen too far away. Both situations can lead to fatigue with prolonged use. In use the monitor normally runs warm, but the ventilation is quite adequate, and no hot spots are evident.

VERDICT The overall impression gained from prolonged use (including preparing last month's article) is of a unit which offers good performance for price. The styling is a matter of personal taste, but the colour quality of the display is unreservedly excellent. It would be unreasonable to expect too much from a medium resolution RGB monitor when it comes to displaying 80-column text. The performance achieved is as good as could be expected, and in general it is necessary to spend around twice as much to obtain a monitor to match (say) the Novex in this respect.

FINAL THOUGHTS

The selection of a monitor for your particular application, and to suit your budget, will always be a matter of personal choice. The two units reviewed are both worthy of serious consideration. The reviews also indicate some points which might be considered when making a selection. Wherever possible, try and see your final choice of monitor in action before you take delivery; both review samples arrived damaged after carriage by road and rail, despite having been very well packed. Prices for monitors appear to have substantially stabilised, so there is unlikely to be any significant price reductions in the near future.

The Novex 12/800 is priced at £75.62 excluding VAT and p&p and is available from Display Distribution Limited, 35 Grosvenor Road, Twickenham, Middlesex (01-891 1923).

The Cabel 370A is priced as £199:50 excluding VAT and p&p and is available from Cabel Electronics, 19 High Street, Tewkesbury, Glos. (0684 298840).



SOON after Britain's state-owned microelectronics company passed its fifth anniversary it sent out advance information on its latest development, a single-chip microcomputer called a Transputer. The fact that the device did not at that moment exist as a real component illustrates both the confidence of Inmos and the commercial conditions in which the company has to operate.

With fierce competition from the mighty American and Japanese semiconductor industries and prices of integrated circuits falling all the time, the only way to survive commercially is to keep on developing new products that will leapfrog their rivals in facilities, performance or price. In such conditions you have to announce and describe your latest development well ahead of its actual existence as a component on the market.

The idea, of course, is to stake a claim as soon as possible with the potential customers—the electronic equipment manufacturers—who are always waiting to pounce on devices using the latest and most advantageous technology to give their own products a competitive edge. To make such claims ahead of actuality you have to be very confident.

GENESIS

So what has Inmos actually achieved in its first five years in this dangerously competitive world? Inmos International PLC, as it is now known, was founded in August 1978 specifically to develop, manufacture and sell very large scale integrated circuits (VLSI) as standard devices in volume production. This means ICs with 100,000 or more transistors on a single chip. The Labour government of that time had become convinced that the UK should have a stake in this high-technology business. Apart from the international trading advantages of being in such a field of manufacture, they felt it would create more jobs and would also help the UK electronics industry to be less dependent on imported devices, or the products of foreign-owned companies, and therefore less vulnerable to technical/commercial decisions made in other parts of the world.

As British private capital had not produced any such VLSI company it was decided to invest \pounds 50M of public money in the venture, \pounds 25M immediately (1978) and a further \pounds 25M at a later date. This was arranged through the National Enterprise Board (NEB), a state run agency already existing to launch or support industrial companies felt to be important to the economy.

The NEB is now part of the British Technology Group. Recently it has been given the new role of assisting technology transfer and will be divesting itself of its holdings in the share capital of various companies.

It so happened that the government's aim had coincided with the ambitions of two very able technologists, who were then looking for an opportunity to exploit their ideas of producing large information processing systems on small silicon chips. Iann Barron, an English systems research specialist, then aged 42, had formed the first UK minicomputer company, Computer Technology Ltd, in 1965 and later had been a consultant in computers and information technology. The second party was Dr Richard Petritz, an American physicist, then 55, who had directed Texas Instruments' semiconductor research for ten years from 1958 and later had formed a company in Dallas for launching new electronics firms—one of which was Mostek.

Legend has it that these two discussed and formulated their common aims at Chicago Airport after a technical conference in 1977. Iann Barron was already aware of UK government intentions through his consulting work for the Department of Industry (now DTI), and it was only a matter of months before an agreement was signed to set up the new British VLSI company with these two individuals as founders.

A third founder was another American physicist, Dr Paul Schroeder, then 38, who had worked for Bell Telephone Laboratories on memory design and in 1967 had become director of memory design engineering at Mostek. (Dr Schroeder, an expert on MOS dynamic memory devices, resigned from Inmos in 1982.)

The British Chip Manufacturer

The essence of the setting-up agreement was that Inmos would be a subsidiary of the NEB. In return for the £50M of public funds, the NEB was to hold $72\frac{1}{2}$ per cent of the equity in the company. A further 15 per cent of the shareholding was to be divided among the three founders and the remaining $12\frac{1}{2}$ per cent between key employees of the company. Richard Petritz was appointed managing director.

The overall plan was to start by developing, manufacturing and selling random access memories (RAMs) because there was already a large and growing market for these devices. This activity would provide a manufacturing and commercial base from which other VLSI devices would be launched. Process technology and initial manufacturing would be based in the USA because that country had a large pool of people already skilled in VLSI technology. Then, after the products had been launched there, they would be transferred to the UK for volume production. Memories would be marketed and sold from the USA because North America provided a very big demand for these products.

THE EARLY YEARS

Less than a year after the founding of Inmos, and before the NEB had produced the second £25M of the investment capital, the 1979 General Election brought in a Conservative government—a government opposed to the principle of stateowned industries, committed to keeping down public expenditure and unwilling to use public funds to support loss-making private sector companies. The affairs of Inmos then moved into the political arena.

The new government hesitated for about a year and clearly would have liked the second £25M to be found from private sources of capital. There was dissension within the Department of Industry and lengthy deliberations on where the UK factory was to be sited. But Sir Keith Joseph, the then industry minister, was in favour of the original method of funding and in the end the remaining £25M of public money was provided, by a new NEB, in August 1980.

Meanwhile the Inmos plans for an American plant had gone ahead on schedule. Colorado Springs had been chosen as a good area for potential employees and by September 1979 the company had started building a plant there. By March 1980 an experimental establishment at Harrison Park had developed an NMOS process for making RAMs with 2–3 μ m active area widths in the silicon. And by May 1980 the first samples of 16K static RAMs made by this process were available. The Colorado Springs plant started operations in March 1981 and by December of that year had produced the first samples of dynamic RAMS. The abbreviation MOS stands for the three kinds of material, metal—oxide—semiconductor, used to construct the integrated field-effect transistors in these devices. The N in NMOS indicates that the conducting channel of these integrated f.e.t.s is silicon containing inpurity atoms giving it a greater density of conduction electrons, making them the majority carriers, than of mobile holes—in other words the silicon is an n-type semiconductor. In the RAMs referred to the f.e.t. structures within the silicon are $2-3\mu m$ wide.

Static RAMs are constructed on the principle of using an integrated flip-flop or bistable circuit to store each binary digit, 1 or 0. They are faster than dynamic RAMs but dissipate power continuously to hold the information, have a lower packing density and are usually more expensive.

Dynamic RAMs are constructed on the principle of using a MOS capacitor, in conjunction with a MOS field-effect transistor, to store each 1 or 0 binary digit as an electric charge. Consequently, to hold information the charge in the capacitor has to be constantly maintained, or 'refreshed', by other circuitry. Dynamic RAMs use power only when reading and writing is taking place and their standby power dissipation is very low.

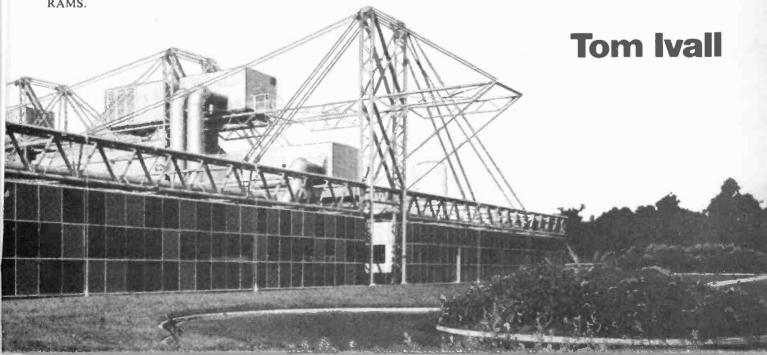
UK FACTORY SITE

Back in the UK the government eventually decided that the factory for volume production should be built in South Wales, and in January 1981 the construction of a plant of spectacularly advanced architectural design was initiated at Cardiff Road, Duffryn, Newport, Gwent. This was conveniently just a few miles over the Severn Bridge from the Inmos administration and R&D centre in Bristol, at Whitefriars, Lewins Mead. The Newport factory started operations in June 1982 and by November of that year was producing in volume the first 16K static RAMs, initially manufactured at Colorado Springs. And in February 1983 the Newport factory started volume production of the dynamic RAMs.

Altogether these three Inmos establishments now employ an average of 1350 people. There are 750 at Inmos Corporation, Colorado Springs; 500 at Inmos Limited, Newport; and 100 at Bristol. The R&D people at Bristol work on microcomputers and computer aided design, while those at Colorado Springs are concerned with memory products and process technology.

INMOS TODAY

What, then, is the position of Inmos now, in terms of its products, markets, technical developments, commercial viability and plans for the future?



First, the products. At the time of writing the i.c.s in production and on the market are all semiconductor memories. Categorized purely in terms of storage capacity and/or chip organization there are seven basic products, but these have variants with different specifications, packaging etc. that make a total of 32 type numbers.

The range of 16K static RAMs contains the $16K \times 1$ type IMS1400 in versions with access times down to 35ns; the 4K \times 4 type IMS1420; and the slightly different 4K \times 4 IMS1421, both in versions with access times down to 45ns.

All these are available in plastic or ceramic d.i.p. or in chip carrier packaging. In addition there are military specification versions, the IMS1400M and 1420M, both available in d.i.p. or chip carrier form. Inmos claim that the 16K IMS1400 and 1420 are "the fastest static RAMs available for use in military and computer applications."

The company also make a range of 64K dynamic RAMs. The 64K \times 1 type IMS2600 comes in versions with access times down to 100ns and is available in either d.i.p. or chip carrier packaging. IMS2620 has a 16K \times 4 organization and is also in versions with access times down to 100ns, while the IMS2630 is an 8K \times 8 memory in versions with access times down to 120ns—these two devices both being packaged in d.i.p. form. Recently Inmos and the Intel Corporation have agreed a common specification for future dynamic RAMs made by a new high speed CMOS process, so that users will have two sources of functionally identical products.

Finally, to complete the seven basic products, the latest to be marketed is a 64K electrically erasable programmable read-only memory (EEPROM) in a d.i.p. package, the IMS3430. Made by a process called Nitrox which produces memory cells of very small area, this device has an $8K \times 8$ organization and requires only a single 5V supply. The whole ROM can be programmed in 1.3s.

In the dynamic RAMs, two particular features contributing to good performance and convenience in use are what are called the 'nibble' mode of operation and the 'CAS before RAS' method of refresh assistance. The term 'nibble' means simply half a byte (a metaphor built on a pun!), or four bits. It describes a facility in the 64K dynamic RAM which allows four data bits to be read or written sequentially for a single address access. It is a design response to the electronic industry's demand for faster and faster memory operation and is provided by other manufacturers under the name 'serial access'. In the IMS2600₁₀ for instance, the nibble mode allows serial access to two, three or four bits at a bit rate of 25MHz.

All dynamic RAMs need refresh assistance, but the tech-





niques used by some manufacturers have the effect of restricting memory expansion and increasing the standby power dissipation. The Inmos method of refresh assistance avoids these problems. To determine whether a normal access or a refresh cycle should be performed the chip samples the high/low state of the column address strobe (\overline{CAS}) as the row address strobe (\overline{RAS}) falls to the low state. If \overline{CAS} is low as \overline{RAS} goes low, the memory ignores any address inputs and substitutes the contents of an on-chip 8-bit counter to determine the row to be refreshed.

MANUFACTURING PROCESSES

All these memory devices are manufactured by advanced VLSI processes, in which Inmos invested very heavily in order to remain competitive. This technology has three main characteristics. First, the etching of the different layers of material on a chip is done by the plasma, or dry, method, to achieve greater dimensional stability than is possible by the use of acids.

Secondly, ion implantation is used to give a more controllable depth of impurity atoms in the crystal lattice below the semiconductor surface than is possible with the conventional diffusion method. Depth of penetration is controlled by the energy imparted by acceleration to the ions bombarding the silicon surface. Thirdly, the Inmos process technology uses wafer stepping photolithography, in which the circuit patterns are projected onto the semiconductor wafer one chip at a time. This gives better line definition and alignment accuracy, and hence higher yields, than when a pattern is projected onto the whole wafer in one operation.

Another technique which improves the yield of memory chips is to introduce redundancy, in the form of spare rows and columns of cells in the memory matrix. At the wafer testing stage any failed cells are identified and this information is programmed into the chips in such a way that when these cells are addressed the device brings in the spare good cells to replace them.

MARKETS

The principal markets of Inmos memories are in the USA and these take over 70% of the company's output. The remainder are distributed throughout the rest of the world. Inmos claims to have secured "a major share" of the world market for 16K fast static RAMs, which are going mainly to the USA, Europe and Japan. In general the firm's memory products are used in mainframe and mini computers, peripheral buffers, radar systems, aircraft flight computers, video displays and telecommunications digital switching equipment.



RECENT TECHNICAL DEVELOPMENTS

In the past few years technical developments from Inmos have included the OCCAM programming language for single and multiple microcomputer applications and a set of computer based aids for designing VLSI devices. In semiconductor products probably the most advanced development is the Transputer (see January issue editorial, p.13). This name, derived from 'transistor' and 'computer', actually refers to a family of products. The first of these, due on the market soon as the IMS T424, is a 32-bit microcomputer on a single chip capable of handling 10 million instructions per second. An article by Ray Coles will explain the device in more detail next month.

The most significant thing about this device is that, as well as being suitable for conventional applications, it is designed to allow operation in arrays of similar microcomputers all working in co-ordination with each other—'concurrent processing' as Inmos calls it. For this purpose the single VLSI chip includes circuits allowing it to communicate with other such microcomputers—four 15Mbyte/s two-way serial data links. This principle of array processing is very much aimed at the future 'fifth generation' computer systems, which will probably work at about a thousand times the performance level of present computers to provide intelligent interaction between people and machines. The CMOS silicon chip of the IMS T424 containe 250,000 active devices, includes 4Kbyte of RAM and is packaged in an 84-contact ceramic chip carrier.

HOW THE MONEY WAS USED

From the beginning the Inmos management realized that the original funding of \pounds 50M would not be enough to sustain the corporate plan aimed at profitability. In the intervening years the effects of inflation and the falling value of the pound sterling relative to the US dollar have made the deficiency even worse. A market and technical assessment by independent consultants later confirmed this situation. The directors wanted to raise a further £50M in the form of loans, but the government had already set a borrowing limit of £35.5M. The upshot was that in 1983 the NEB agreed to provide a further £15M as an additional equity investment. This increased the NEB's holding in the share capital to 75 per cent and correspondingly reduced the proportion held by individual directors and employees.

Thus the capitalization was increased to $\pounds 65M$. On top of this, the leasing, loans and investment grants arranged with banks and other sources (including the EEC) have brought the

total funding to about £100M to date.

How has all this money been used? The ultimate purpose of the investment, of course, is to create a profitable company financing itself out of its own trading activity. The NEB, having performed its function of launching the enterprise, would then be able to sell off its shareholding in a going concern to good advantage, at the least recovering the investment of public money and at the best obtaining some return for it.

The 1982 annual report is the latest account showing how far Inmos has progressed along this road. First of all, its use of the capital investment. The company now has tangible fixed assets of $\pounds 44 \cdot 1M$, in the form of various buildings and their equipment. This sum is made up of $\pounds 20 \cdot 2M$ in freehold land and buildings, $\pounds 168,000$ in short-leasehold land and buildings and $\pounds 23 \cdot 7M$ in plant and equipment. There are also current assets, in the form of stocks, cash and debts, and after the current liabilities have been deducted this leaves the company with total assets of $\pounds 47 \cdot 2M$.

Now to the current trading position. In 1982 sales of MOS memory products amounted to £13.7M. This was a very big increase from the corresponding 1981 sales figure of £2.1M. However, the operating costs relating to these 1982 sales—manufacturing, engineering, product support, distribution and administration—totalled £22.3M, resulting in an operating loss of £8.6M. Apart from this, starting up the Newport factory cost £3.6M, the continuing research and development work required £4.5M, the interest charges on loans were £1.2M, while losses on the dollar-pound exchange rate came to £2.3M.

Altogether the profit and loss account for 1982 showed a loss of $\pounds 20.3M$. Losses brought forward from previous years amounted to $\pounds 21.6M$, so the accumulated loss carried forward from 1982 was $\pounds 42M$.

PROFIT IN 84?

Obviously Inmos still has a long way to go. In the 1982 report the directors said that they expected the 1983 results to show "a move towards profitability", while the chairman, Malcolm Wilcox, said that if all went well "the scene will be set for a move into profit in 1984." The 1983 annual report, soon to be published, will show to what extent these optimistic comments are justified. They seem to suggest that by the end of 1983 Inmos would at least have broken even on its monthly revenues. At the turn of the year company officials were saying no more, but seemed to be quietly confident that the 1983 results would show a more than doubled turnover.

So whet does the future hold for Inmos? To begin with, a company spokesman told PE that there is "no immediate danger of going bust." The firm now has enough money to keep going. But it still has to keep up with the relentless march of technical innovation to remain among the leaders in the field of manufacture, and also has to contend with equally relentless commercial competition in world markets. This means, for example, that "significant sums" will be needed to build new wafer processing facilities.

For such future investment Inmos is now looking towards private sources of finance, and the 1982 annual report stated that "discussions in this regard are now on course." One result could be that other companies or financial institutions will be buying significant minority shareholdings in the firm.

If this does indeed happen and the process continues, with the NEB gradually divesting itself of its majority shareholding as intended, Inmos will eventually end up as a public company with share prices quoted on the Stock Exchange. This transformation, from ownership by the state to a variegated ownership by pension funds, insurance companies, institutions, trade unions and even private individuals, is a process that could well be starting some time this year.

INTRODUCTION TO DIGITAL ELECTRONICS

MICHAEL TOOLEY BA DAVID WHITFIELD MA MSc CEng MIEE O&A Level Part Six

So FAR in the series we have only dealt with logic gates having two inputs. The time has now come to extend our knowledge to include gates having three, or more, inputs. The twoinput gates which we have previously considered are: AND, OR, NAND and NOR. We shall now consider their three-input counterparts.

A three-input logic gate has inputs which we shall, for convenience, label A, B and C. Again there is no particular significance in the choice of letters other than that they are simply the first three letters of the alphabet. To be consistent with the two-input gates previously considered, we shall again refer to the outputs as X. The Boolean expression for each of the three-input gates will, of course, involve the three variables A, B and C. Taking the threeinput AND gate first, we find that its output is A AND B AND C. Putting this in correct Boolean form gives:

$X = A \cdot B \cdot C$

In terms of the logical state of the inputs, the output X will be a 1 whenever A, B and C are all 1. Any other combination of inputs (e.g. A = 0, B = 0, C = 1) will produce a 0 output. Since we are dealing with a three-input gate, there are 2^3 (= 8) possible combinations of the logical input states. The truth table will, therefore, consist of eight lines covering the input states arranged in four columns, three for the inputs and one for the output, as shown in Table 6.1.

The output of a three-input OR gate is A OR B OR C. In correct Boolean form this is:

X = A + B + C

The output X will be a 1 whenever any one, or more, of the inputs is a 1. The truth table will take the same form

INPUTS		OUTPUT	
A	в	С	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

EG 1269

Table 6.1. Truth table for a threeinput AND gate

as that used for the three-input AND except that the output column will contain 1's in each line except for that which corresponds to the input state: A = 0, B = 0, C = 0. This, incidentally, yields the important result that the output of a three-input OR gate is the logical opposite (complement) of the output of a gate for which the Boolean expression is (NOT A) AND (NOT B) AND (NOT C). Thus we conclude that:

$\overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$

This is an important result which we shall be returning to in Part Seven when we introduce De Morgan's Theorem.

The truth table for a three-input OR gate is shown in Table 6.2. As in the case of their counterparts, three-input inverting gates, NAND and NOR, produce the complement of their respective AND and OR counterparts. The output of a three-input NAND is NOT (A AND B AND C), or:

$$X = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

The output of a three-input NOR gate is NOT (A OR B OR C), or: $X = \overline{A + B + C}$

INPUT		OUTPUT	
A	в	С	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

EG1270

Table 6.2. Truth table for a threeinput OR gate

The truth tables for the three-input NAND and NOR gates are respectively shown in Tables 6.3 and 6.4. Unfortunately, these two are easily confused and the recommended method for distinguishing between them is to FIRST consider the output of the corresponding non-inverting gate (i.e.

INPUTS			OUTPUT
A	В	С	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table 6.3. Truth table for a threeinput NAND gate

AND or OR) and simply complement its output state (i.e. whenever a 1 appears in the output column change it for 0, and vice-versa).

	INPUT	OUTPUT	
A	B	С	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

EG1272

Table 6.4. Truth table for a threeinput NOR gate

FOUR (AND MORE!) INPUT GATES

Having dealt with three-input gates it is worth considering what happens when we are presented with gates with four, and more, inputs. The procedure for deriving the Boolean expressions and truth tables naturally follows that adopted for the three-input gates. The Boolean expression for a gate with n different inputs will have 2ⁿ lines. The truth table will have n columns for the inputs and just one column for the output. Hence the Boolean expression for the output of a four-input gate (n = 4)will involve four variables (A, B, C and D) and its truth table will have 24 (= 16) lines.

The Boolean expressions of the outputs of four-input gates are shown below. The symbols for these gates are, together with those for their threeinput counterparts, shown in Fig. 6.1.

AND	$X = A \cdot B \cdot C \cdot D$
OR	$\mathbf{X} = \mathbf{A} + \mathbf{B} + \mathbf{C} + \mathbf{D}$
NAND	$X = \overline{A \cdot B \cdot C \cdot D}$
NOR	$X = \overline{A + B + C + D}$

By now, readers should be familiar with Boolean expressions and truth tables for gates with up to four inputs. We shall, however, be returning to this topic in Part Seven when the important applications of De Morgan's Theorem will be discussed.

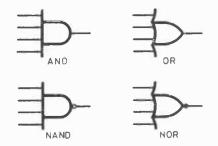
J-K BISTABLES

Unlike the two types of bistable which we have met previously in Part Five, the J-K bistable provides direct as well as clocked inputs. The direct inputs, usually labelled 'preset' and 'preclear', are normally used to initialise the state of the bistable before data is clocked into it by means of the J and K inputs. There is, incidentally, no particular significance in the letters J and K other than that they are consecutive letters in the alphabet and are





THREE-INPUT GATES



FOUR-INPUT GATES

EG1279

Fig. 6.1. Symbols used for three and four-input logic gates. Note: BS symbols follow the style of the two-input gates previously described in Part Two

unlikely to be confused with other letters used thus far to identify inputs and outputs.

The symbol for a J-K bistable is shown in Fig. 6.2. Note that there are five inputs: preset and preclear (the two direct inputs), J and K (the two clocked inputs), clock, and two outputs: Q and \overline{Q} . As with the previous forms of bistable, the two outputs are complementary (i.e. when Q = 1, $\overline{Q} =$ O, and vice versa). It should also be noted that, in the case of practical J-K bistables like the 7473 that we shall be describing later, the preset and preclear inputs are often 'active low'. This means that they are normally connected to logic 1 and must be taken 'low' (to logic 0) in order to preset or preclear the Q output.

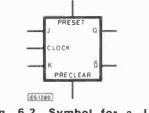


Fig. 6.2. Symbol for a J-K bistable

In all circumstances the direct inputs dominate and clocked operation is

enabled when both of these inputs are taken to logic 1. It is, therefore, necessary to consider TWO truth tables: one for the operation of the direct inputs and one for the clocked inputs. These two truth tables are

PRESET	PRECLEAR	Q
0	0	INDETERMINATE
0	1	1
1	0	0
1	1	ENABLES CLOCKED

Table 6.5. Truth table for the direct inputs of a J-K bistable

J	K	Q n+1	COMMENT
0	0	Qn	NO CHANGE
0	1	0	OUTPUT PRECLEARED
1	0	1	OUTPUT PRESET
1	1	Qn	0/P CHANGES STATE

Table 6.6. Truth table for the clocked inputs of a J-K bistable

respectively shown in Tables 6.5 and 6.6. The truth table for the clocked inputs is relatively complex: however, for three of the input conditions it is similar to that of an R-S bistable. The output column of the clocked input truth table (Table 6.6) shows the state of the Q output after a falling edge clock transition (i.e. after a change of clock state from 1 to 0). This is denoted by Qn+1 whereas the previous clock state is Qn. We shall now consider separately the four possible conditions which can arise for both the direct and clocked inputs, referring initially to Table 6.5:

1. If both preset and preclear inputs are taken to logic 0 an indeterminate state exists and the outputs, Q and \overline{Q} , may no longer be complementary. This condition must be avoided.

2. If the preset input is taken to logic 1 and the preclear input is taken to logic 0, the state of the Q output immediately becomes logic 0 whilst the Q output becomes logic 1; i.e. the bistable is precleared.

3. If the preset input is taken to logic 0 and the preclear input is taken to logic 1, the Q output immediately becomes logic 1 whilst the Q output immediately becomes logic 0; i.e. the bistable is preset.

4. If both preset and preclear inputs are taken to logic 1 the bistable is ready for clocked operation and the following rules are obeyed (as in Table 6.6):

(a) If both J and K inputs are taken to logic 0 the Q and \overline{Q} outputs do not change state on a falling clock transition. Thus Q_{n+1} is the same as Q_n and $\overline{Q_{n+1}}$ is the same as $\overline{Q_n}$.

(b) If the J input is at logic \overline{O} and the K input is at logic 1, the Q output stays, or becomes, O when the next falling clock transition occurs. The \overline{Q} output takes the opposite logical state.

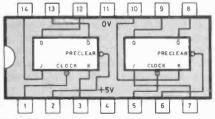
(c) If the J input is at logic 1 and the K input is at logic 0, the Q output stays, or becomes, 1 when the next falling clock transition occurs. The \overline{Q} output takes the opposite logical state.

(d) If both the J and K inputs are taken to logic 1, the Q and \overline{Q} outputs change state when the next falling , clock transition occurs. Thus Q_{n+1} is the same as $\overline{Q_n}$ and conversely $\overline{Q_{n+1}}$ is the same as Q_n .

In case (a) the bistable ignores the clock transition whilst in cases (b) and (c) the complementary states of the J and K inputs are effectively passed, on the falling clock edge, to the Q and \overline{Q} outputs respectively. In case (d) the bistable is configured for operation as a binary divider. If this still appears to be a little difficult to understand the following practical investigation should help to make things clear!

THE 7473 J-K BISTABLE

The 7473 contains two independent J–K bistables, as shown in Fig. 6.3. The 74107 is electrically identical to the 7473 but has more conventional supply connections (TTL devices usually have pins 14 and 7 as the +5V and OV connections respectively). The two internal bistable stages are themselves identical and each has the usual J, K and clock inputs. A preset input is,



EG1281

Fig. 6.3. Internal arrangement of the 7473 J–K bistable. Note: The circle on the clock and preclear inputs indicate an 'active low'

however, not provided and only a preclear input is available for the direct control of the bistable. The preclear is, incidentally, an 'active low' input as mentioned previously. To all intents and purposes, the bistable operates as if the missing preset input were internally connected to logic 1. Thus, for normal clocked operation, it is only necessary to connect the preclear input to logic 1. In actual fact the preclear input 'floats' to logic 1 if left unconnected. However, since leaving inputs unconnected is not generally considered good practice, it is recommended that a physical link to logic 1 be made external to the i.c. There can then be absolutely no doubt about the logical condition present on the preclear input! It should also be noted that the state of the J and K inputs should be changed once only during each clock cycle. Ideally this change should be made immediately after the clock transition. Any subsequent changes in the logical state of the J and K inputs can cause invalid states within the bistable.

Insert the 7473 into the dual-in-line socket marked 'A' on the Logic Tutor. The chip should be orientated so that pin 1 is in position A1, pin 7 in position A7, pin 8 in position A10 and pin 14 in position A16. During this investigation we shall be using only one of the two available J-K bistables contained within the i.c. The following connections should be made in order to facilitate clocked operation of the bistable:

A1	to	S1	(S1 will act as the clock)
A2	to	logic 1	(preclear to 1)
A3	to	S4	(S4 will act as the K input)
A4	to	+5V	(positive supply)
A13	to	0V	(0V)
A14	to	53	(S3 will act as the J input)
A15	to	D2	(D2 indicates the Q output)
A16	to	D1	(D1 indicates the Q output)

Set S3 and S4 initially to produce logic 0 outputs and note the state of the Q and \overline{Q} outputs by observing the indication produced by D1 and D2 respectively. The outputs should, of course, be complementary! Now depress and release S1. This causes a $0 \rightarrow 1 \rightarrow 0$ pulse on the clock input. There should be no change in the Q and \overline{Q} outputs. Set S4 to produce a logic 1 K input whilst S3 should remain at logic 0. Now depress and release S1 for a second time. This time the Q output should go to logic 0 and \overline{Q} should go to 1 regardless of their previous state. Set S3 to produce a logic 1 on the J input and S4 to produce a logic 0 on the K input. Depress and release S1 again and check that the Q output becomes 1 whilst the \overline{Q} output becomes 0. Finally, set both S3 and S4 to logic 1. Repeatedly depress and release S1 to produce a train of successive clock pulses. This should cause the Q and \overline{Q} outputs to alternate between logic 1 and logic 0, a change being made each time S1 is operated.

MASTER-SLAVE BISTABLES

At this point readers may be wondering what the internal logic of a J-Kbistable looks like. It is, in fact, an elegant and ingenious arrangement known as a 'master-slave'. Both the master and the slave are simply conventional R-S bistables, the trick comes in the arrangement of the logic gates which interconnect them.

The basic arrangement of a J-K master-slave bistable is shown in Fig. 6.4. Let us assume that, initially, J, K and clock are all at logic 0. If preset is taken to logic 1 whilst preclear remains at logic 0 then the master bistable is set and its Q output becomes logic 1. Since the clock is at logic 0, the inverted clock will be a 1. This, together with the Q output from the master bistable, is fed to a two-input AND gate which generates a logic 1 to set the slave bistable. The final Q output of the complete arrangement is thus logic 1. The operation of the preclear input is similar. In this case, however, the resulting final Q output is a Q. When both preset and preclear are taken to logic 1 an attempt is made to set and reset both bistables at the same time. It is thus impossible to predict what will happen and the final output is indeterminate. When both preset and preclear are taken to logic 1 the two OR gates are ready to pass data from the three-input AND gates to the set and reset inputs of the master bistable. Note that the final Q and \overline{Q} outputs are fed back to the three-input AND gates and thus they must generate complementary logic states by virtue of the opposite state of the Q and \overline{Q} outputs. The master is thus set or reset depending upon the state of the J and K inputs whenever the clock is at logic 1. When the clock changes to logic 0, data is transferred from the master to the slave by means of the two-input AND gates.

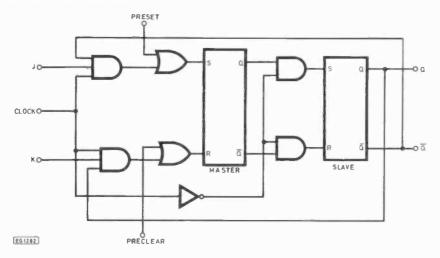


Fig. 6.4. Basic arrangement of a master slave bistable

In practice J-K bistables may also be of the edge-triggered variety. Unlike the master-slave type, where data is fed into the bistable during the logic 1 part of the clock cycle and appears at the output when the clock goes to logic O, the edge-triggered bistable transfers data from input to output on the same edge of the clock cycle. This is achieved by means of an internal pulse narrowing circuit which converts the clock to a narrow 'spike' shorter in duration than the delay which occurs in the bistable changing its state. The truth table is, however, identical for both types.

CLOCKS AND OSCILLATORS

Clocks are vital to the correct timing of operations in digital logic circuits. The basic requirement of a clock is that it provides a repetitive pulse waveform of accurate period. The most basic form of clock is merely a TTL compatible oscillator which produces a square wave output of 5V pk-pk at a known frequency. More complex clocks, such as those which are used for 'real time' applications, may be required to operate with a frequency stability and accuracy of better than ten parts per million. Oscillators may also be reguired for purposes other than purely timing. These applications include the testing of logic systems, the generation of alarm and warning signals, and the transmission of data in serial form. Before examining the subject in greater detail it is worth defining some of the relevant terms in popular use.

FREQUENCY: The frequency of an oscillator is the number of cycles of its output which occur in a second. An oscillator which, for example, generates

50 pulses per second has a frequency of 50Hz. Similarly, an oscillator which provides an output of 1kHz is producing 1000 pulses per second.

PERIOD: The period of an oscillator is the time for one complete cycle of its output. Naturally, the higher the frequency the smaller the period will be. In the previous examples the periods are 1/50 second (or 20ms) and 1/1000 second (or 1ms), respectively. The period of a waveform (in seconds) is thus simply the reciprocal of its frequency (in Hz).

MARK TO SPACE RATIO: The mark to space ratio of a pulse waveform is the ratio of 'on' (logic 1) to 'off' (logic 0) time. For a perfect square wave the 'on' and 'off' times will be the same, hence it is said to exhibit a 1:1 mark to space ratio.

DUTY CYCLE: The duty cycle of a pulse waveform is the ratio of the 'on' to ('on' plus 'off') times, normally expressed as a percentage. A perfect square wave would thus exhibit a 50% duty cycle.

OSCILLATOR USING SCHMITT INVERTERS

A very simple TTL oscillator configured around two gates of a hex inverter is shown in Fig. 6.5. This arrangement uses a 7414 device rather than the more familiar pincompatible 7404. The 7414 is much to be preferred for this particular application by virtue of its internal Schmitt action which offers an amount of hysteresis in the voltage levels for the logic 0 and 1 thresholds. The 7404 will not operate reliably in this circuit.

The first of the two gates has two external components: a resistor which

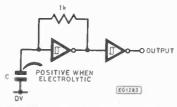


Fig. 6.5. Simple TTL oscillator using Schmitt inverters

С	fout
u 470	1·5Hz
47 y	15Hz
4 y 7	150Hz
470n	1·5kHz
47 n	15kHz
4n7	150 k Hz
470p	1.3MHz
47p	8MHz
[EG1275]	

Table 6.7. Values of C and corresponding output frequency for the circuit in Fig. 6.5

provides positive feedback from the output to the input, and a timing capacitor connected from the input to OV. The second gate merely acts as an inverting buffer to provide a measure of isolation of the first gate from the load connected to the output.

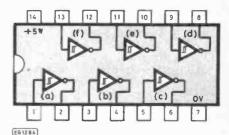
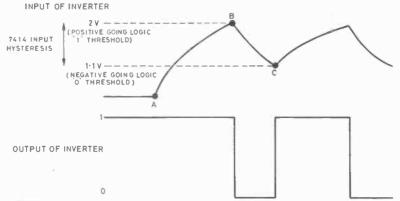


Fig. 6.6. Pin connections for the 7414 hex Schmitt inverter

In order to explain the operation of the ascillator we must consider what happens when power is first applied to the circuit (A in the waveform diagram of Fig. 6.7). Furthermore, we shall only be concerned with the first of the two logic gates since the second stage merely acts as an inverter and takes no part in the oscillatory action. The capacitor C will be initially uncharged and thus the voltage across it will be zero. The input to the first logic gate will then be logic 0 whilst its output must be logic 1 by virtue of the inverting action of the gate. The logic 1 state of the output will be represented by a voltage of somewhat less than the 5V supply. Current will thus flow through resistor R (from right to left in



EG1285

Fig. 6.7. Waveforms for the Schmitt oscillator

CHRYSTAL FREQUENCY RANGE	C1
2 - 4 MH z	220p
4 — 9 M Hz	68p
9-15MHz	47p

EG1276

Table 6.8. Typical values of C andfrequency for the circuit of Fig.6.7

the circuit diagram) to charge the capacitor. This causes the voltage across the capacitor to rise in an exponential fashion until it reaches the point at which the gate recognises a logic 1 at its input (B on the waveform diagram). For the 7414 this condition occurs at an input voltage of approximately 2V. The time taken to achieve this value of input voltage depends upon the CR time constant (i.e. the product of capacitance, C, and resistance, R). The output of the logic gate rapidly falls to OV as the gate changes state to produce a logic O output. The capacitor now discharges through R (current flowing left to right in the circuit diagram) until the voltage at the input of the gate falls exponentially to the level at which a logic O is recognised (C on the waveform diagram). This condition is reached at approximately 1.1V and, at this point, the gate returns to its earlier state with a logic 1 output. The cycle thus repeats itself indefinitely or until the power is removed from the circuit. The output waveform of the oscillator is square and TTL compatible but has a mark to space ratio of approximately 3:1. This is not, however, a very severe drawback since we can achieve a precise 50% duty cycle by simply adding an extra bistable stage as we shall later show.

CRYSTAL OSCILLATORS

Many applications for clocks require

the oscillator to be exceptionally stable in output frequency and, where precise timing is important, accurately maintained at a particular frequency. Furthermore, in many applications the clock is required to operate at a high frequency, often in excess of 1 or 2MHz. In such applications a quartz crystal may be employed to act as the frequency determining element, as shown in Fig. 6.8. This circuit is somewhat similar to that shown previously with the addition of a crystal and extra capacitor. The circuit can be considered as a free-running oscillator, like those previously described, which is locked to the crystal frequency. The value of C1 in particular has to be chosen so that the stage will operate at, or near, the desired output frequency with the crystal disconnected. Values for C1 of 47pF and 220pF are appropriate to the frequency ranges 8 to 15MHz and 2 to 8MHz respectively. A clock frequency of greater than 2MHz may appear to be somewhat high at first sight. It is, however, a relatively simple matter to divide the oscillator output frequency by a fixed amount (e.g. 10, 100, 16, 64 etc.) as we shall see in Part Seven.

Even when the circuit is correctly operating in the crystal locked condition there may still be a very slight error between the actual frequency produced and that desired (or that marked on the crystal). In such a case a small amount of capacitance may be connected in parallel with the crystal to trim the frequency precisely. This capacitance should not normally exceed a value of 68pF. A practical solution would be to connect a 50pF trimmer directly across the crystal terminals and adjusting this component using a digital frequency meter connected to the clock output.

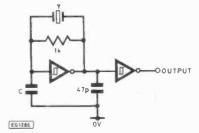


Fig. 6.8. Typical TTL crystal oscillator

С	fmin	fmax
470y	0.25 Hz	1Hz
47 µ	2·5Hz	10 H z
4 y 7	25Hz	100Hz
470n	250 Hz	1kHz
47n	2·5kHz	10 kHz
4n7	25kHz	100kHz
470p	250kHz	1MHz
47p	2.3MHz	9MHz

EG1277

 Table
 6.9.
 Values
 of
 C
 and

 corresponding
 frequency
 range
 for
 the circuit of
 Fig. 6.8
 for
 for

VARIABLE FREQUENCY OSCILLATORS

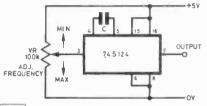
Occasionally one requires a variable frequency oscillator capable of adjustment over a wide range. Whilst such a signal can, of course, be readily derived from a conventional laboratory signal generator, there is a very simple and effective circuit arrangement based on the 74S124 which provides this function using only two external components.

The circuit of a variable frequency clock using a 74S124 is shown in Fig. 6.9. This produces a reasonable 50% duty cycle square wave output and is capable of reliable operation extending from below 1Hz to beyond 20MHz. The frequency is continuously variable by means of the control potentiometer which provides an adjustment range of approximately 4:1. Typical values of capacitor together with maximum and minimum operating frequencies are shown in Table 6.9.

TWO-PHASE CLOCKS

In microprocessor systems, and sophisticated logic systems generally, there is often a need for a clock which produces complementary outputs. Such a clock is known as a two-phase (or bi-phase) clock, the typical output waveform of which is shown in Fig. 6.10. Fortunately, complementary outputs are easy to obtain from a bistable

element and thus a two-phase clock may simply consist of an oscillator followed by a bistable. There is, however, one minor complication: the bistable effectively operates as a binary divider and hence the oscillator must



EG1287

Fig. 6.9. Variable frequency clock using the 74S124

RESISTANCE, R	CAPACITANCE, C	APPX. MONOSTA BLE PERIOD, t
10 k	10p	70 n s
2 k 2	100p	150 ns
10k	100p	700 ns
2 k 2	1n	1-5µs
10 k	1n	z بر 7
2 k 2	10n	15 µs
10 k	10 n	70 y s
2 k 2	100 n	150 y s
10k	100 n	700 µs
2 k 2	1μ	1.5 ms
10 k	1,0	7 m s
2 k 2	10 µ	15 ms
10k	10 µ	70 m s
2 k 2	100 y	150 m s
10k	100 y	700 m s

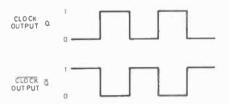
EG 1278

Table 6.10. Typical values of CR and monostable period for the circuit of Fig. 6.9

operate at twice the desired clock frequency.

TWO-PHASE CLOCK USING THE 7414 and 7473

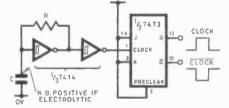
A two-phase clock which illustrates some of the principles discussed earlier, is shown in Fig. 6.11. Here the oscillator uses a 7414 hex Schmitt inverter which produces an output at about 2Hz with a mark:space ratio of approximately 3:1. The oscillator output is fed to the clock input of a 7473 J-K bistable. The timing diagram for the circuit is shown in Fig. 6.12. It should be noted that the output frequency is a symmetrical square wave having a frequency which is exactly half that of the oscillator. This arrangement can be tested by inserting 7414 and 7473 devices in sockets A and B respectively of the Logic Tutor and then making the following connections:



EG1288

Fig. 6.10. Output waveforms for a two-phase clock

A1	to	OV via	(+ve to A1)
		220µF	(timing capacitor)
		capacitor	(
A2	to	A1 via	(timing resistor)
		1kΩ	
		resistor	
A3	to	A2	(linking inverter
			stages)
A4	to	D1	(D1 indicates
			oscillator
			output)
A7	to	OV	(0∨)
A16	to	+5V	(positive supply)
B 1	to	A 4	(bistable clock
			input)
B2	to	logic 1	(preclear to
			logic 1)
В3	to	logic 1	(K to logic 1)
B4	to	+5V	(positive supply)
B13	to	OV	(OV)
B14	to	D2	(D2 indicates the
			clock output)
B15	to	D3	(D3 indicates the
			clock output)
B16	to	logic 1	(J to logic 1)
		LO	GIC 1



EG1289

Fig. 6.11. Two-phase clock using 7414 and 7473 devices

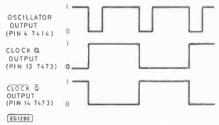


Fig. 6.12. Timing diagram for the circuit in Fig. 6.11

The state of D1, D2 and D3 are used to indicate the oscillator, clock, and clock outputs respectively. D1 should be seen to flash at approximately 2Hz whilst D2 and D3 flash at exactly half this rate and will always have opposite states. The speed of operation may be varied by making suitable changes to the value of C. The value of R should, however, not be changed since $1k\Omega$ is optimum for this circuit. Increasing the value much above $1k\Omega$ will render the circuit inoperative (the logic 0 input state is no longer properly maintained) whilst reducing it much below $1k\Omega$ means that an impractically large value of capacitor has to be used in order to obtain a particular clock rate. Values of C, together with approximate output frequencies produced, with $R = 1k\Omega$ are shown in Table 6.9.

MONOSTABLES

The R–S, D, and J–K bistables which we have met so far all possess two stable states. Once put in one or other of the states they will remain in that state until something happens to produce a change of state. There are, however, a number of applications in which a momentary pulse of fixed duration is required. A device which fulfils this function has only one stable state and is known as a monostable.

The action of a monostable is quite simple: its output is initially logic 0 until a level change or edge arrives at its trigger input. This level change can be from 0 to 1 (positive edge trigger) or 1 to 0 (negative edge trigger). Immediately the trigger is received, the output of the monostable changes state to logic 1. Then, after a time interval determined by external components, the output reverts to logic 0. The monostable then awaits the arrival of the next trigger.

Monostables are available in a variety of forms and, whereas it is possible to make a simple form of monostable from individual logic gates, the use of a purpose designed integrated circuit monostable is much to be preferred. To understand the basic principles of monostable pulse generators we will, however, first consider some simple yet effective monostables which employ familiar logic gates.

SIMPLE MONOSTABLES USING INVERTERS

The simplest method of generating a monostable pulse involves the use of an inverting gate together with an external capacitance-resistance (C-R) network. The arrangement of Fig. 6.13 shows how a negative output pulse $(1 \rightarrow 0 \rightarrow 1)$ can be generated by a positive edge trigger. If we need to

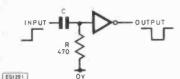


Fig. 6.13. Simple negative-going output positive edge triggered monostable using an inverter

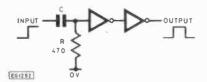


Fig. 6.14. Simple positive-going output positive edge triggered monostable using inverters

produce a positive output pulse (0 \rightarrow $1 \rightarrow 0$) then we only need to add a second inverting stage, as shown in Fig. 6.14. In order to explain how the circuit operates we need to consider what happens when the trigger arrives. Initially, capacitor C is uncharged since the voltage level at the input is zero before the trigger pulse arrives. When the trigger does arrive, the input voltage rapidly rises from OV to approximately 5V. This is conveyed, via the capacitor, to the input of the inverting gate. The inverter recognises a logic 1 input whenever the voltage at its input exceeds approximately 1.5V thus its output changes state, from 1 to 0 when the input voltage passes through 1.5V. The capacitor then charges through the resistor, R, and the voltage at the input of the gate then falls exponentially back towards OV. When the input voltage falls below approximately 1.5V, the gate recognises a logic 0 input and its output state reverts to logic 1. Waveforms for this circuit arrangement are shown in Fig. 6.15. The time taken for the capacitor to charge depends upon the time constant of the circuit (C x R). Thus the duration of the monostable output pulse can be varied simply by changing the values present.

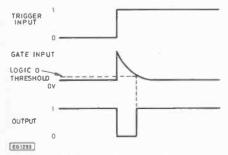


Fig. 6.15. Waveforms for the circuit shown in Fig. 6.13 Note, however, that a value of 470Ω for R is optimum for this circuit. It should not be increased much above, or below, this value and hence the value of capacitance should be varied in order to achieve different pulse durations. Long duration pulses may require the use of large value capacitors and hence electrolytic types may have to be used. In such cases, it is essential that capacitors are low leakage types and, furthermore, close tolerance varieties are necessary if an accurately defined output pulse duration is required.

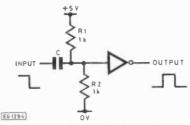


Fig. 6.16. Simple positive-going output negative edge triggered monostable using an inverter

Figs. 6.16 and 6.17 respectively show how positive and negative output pulses may be derived from a negative edge trigger. These circuits are somewhat similar in operation to those which operate from a positive edge trigger. In this case, however, the input

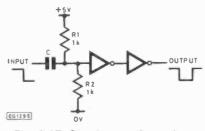


Fig. 6.17. Simple negative-going output negative edge triggered monostable using inverters

of the inverting gate is biased into the logic 1 condition by means of an additional resistor connected to the positive supply rail. This places a quiescent voltage of approximately 2.5V at the input of the logic gate.

PULSE GENERATOR USING THE 7404

The two short exercises which follow are designed to confirm the operation of the 7404 hex-inverter as a monostable pulse generator. Both exercises involve the generation of a positive pulse, the first being triggered by a positive edge whilst the second is triggered by a negative edge. The positive edge triggered monostable follows the arrangement shown in Fig. 6.14 and is constructed using the following links on the Logic Tutor:

A1	to	S1	via 100µF capacitor (+ve to S1)
A1	to	0V	via 470 Ω resistor
A2	to	A3	
A4	to	D1	(D1 indicates the
			output)
A7	to	0V	(0∨)
A16	to	+5V	(positive supply)

The 7404 should be inserted into socket A, taking care to orientate the package so that pin 1 aligns with A1. In the absence of any input from S1, D1 should remain extinguished. Immediately S1 is depressed, however, a positive edge is generated and D1 should flash momentarily (i.e. approx. 0.2 second) and then become extinguished again. If S1 is pressed, and held down, only one flash will be generated. If S1 is pressed and then released repeatedly D1 will flash once for each positive edge generated.

The negative edge triggered monostable follows the arrangement shown in Fig. 6.16 and uses the following links on the Logic Tutor;

A1	to	S1	via 100µF capacitor
			(-ve to S1)
A1	to	0V	via $1k\Omega$ resistor
A1	to	+5V	via 1kΩ resistor
A2	to	D1	(D1 indicates the
			output)
A7	to	0V	(0∨)
A16	to	+5V	(positive supply)

The 7404 should again be inserted into socket A. In the absence of any input from S1, D1 should again remain extinguished. When S1 is depressed nothing should happen and D1 should remain extinguished since the circuit is designed to ignore a positive edge transition. Releasing S1, which produces a negative edge, should cause D1 to flash momentarily and then become extinguished again. If S1 is pressed and released repeatedly D1 should flash once for each negative edge generated.

NEXT MONTH: We continue by looking at the 74121 monostable, pulse stretching techniques, a variable width pulse generator, De Morgan's Theorem, Karnaugh Maps and an intruder alarm for our electronic shop. Appearing every month, Micro-Bus now presents ideas, applications and programs for the most popular microcomputers and all micro-related projects so far published in PE. Ideas must be original, and payment will be made for any contribution featured.

MICRO-BUS

COPYING M/C

Sir-when copying machine code tapes for the UK101 to make back-up copies or for a high speed cassette interface, there can be problems due to some programs overwriting e.g. page zero memory. Also in order to exit machine code games etc. it is very often necessary to press reset, and this may foul up the program making it pointless to attempt to save it.

A way round this problem is to use the NMI (non-maskable interrupt). By connecting a push-to-make switch from ground to either pin 6 of the 6502 or pin 2 of J1 you can jump to any memory location via the NMI vector at HEX 0130. With Ceamon the ideal place to jump to is FEOC, the machine code monitor warm start. To do this enter the monitor by reset M and enter 0130 4C,OC,FE. (0130 JMP FEOC.)

Before the program can be SAVED you need to know the start, end and entry points (RAM addresses) of the code. To make it easy to find the end address it is advisable to fill all RAM with the same number so that when loading the program it will only overwrite the RAM it occupies. For example the original BASIC 4 chip will, when cold-starting, fill all user RAM with HEX 24, and by finding the last "24" overwritten you can find the end address of the code to be saved.

The start and entry (or "Go") addresses can usually be found by watching the screen when loading. When loading with Cegmon the start address appears first, followed by Hex pairs of digits and then the "Go" address. It is possible that the first address may be that of a checksum or other loader so this method may not work in every case. A better way is to use Exmon but you may need a relocated version that doesn't clash with the program for memory space.

To summarise, cold start (if RAM test doesn't fill RAM then fill all RAM with a FOR-NEXT loop e.g. FOR J = 768 TO 16348 : POKE J,36 : NEXT), then enter the machine code monitor and enter 0130 4C,OC,FE. Now LOAD the program to be SAVED and note down the start address and entry address when they appear on the screen—but you'll have to be ready as they will disappear almost immediately. The

program or game will start but press the NMI switch and the computer will jump to the monitor warm start. Cegmon's tabulate command will assist in finding the last RAM location before all the "24s"-vou can now tell the end address. Finally SAVE by typing S START, END ENTRY e.g. S 0240,0FFF 0800.

Here are some useful routines: To jump out of BASIC and load M.C.:

POKE 251,1 : & GO£ F988 or

POKE 251.1 : CALL -1655 To jump out of M.C. and run BASIC :

JSR £ A477 JMP £A5C2

If saving non-continuous blocks of RAM then the "Go" address is £ FA2E e.g. S 0235,02FF FA2E then S 1C00,1CFF 0000

To double space text on screen : POKE 15.0

To prevent carriage returns half way along lines when for example printing 'TEST' within a loop : POKE 14,0 (within the loop). To LIST within a program without returning to command mode

POKE 4,194 : POKE 5,165 : LIST : POKE 4,195 : POKE 5,168

(for BASIC 5 after LIST put POKE 4,136 : POKE 5.146 J

If you have BASIC 5 from Premier then try POKEing 316 with 63 or 65 when doing blocks, vertical lines etc.

> Dave Henniker, Edinburgh.

UK101 REM REMOVER

Sir-I have a UK101 with 48K of RAM and the original monitor.

The following program may be of interest to your readers. It is a "REM remover" for UK101. As the program is fairly long (303 bytes) it is shown as a memory dump. The program occupies locations 1E80 to 1FAF. Memory will need restricting if the program is to be resident while BASIC programs are runnina.

To use the program, have the code resident and load a BASIC program with lots of REMs. It is worthwhile doing a ?FRE(I) at this point. Press reset, M, 1E80 and G. The program returns to BASIC when it has finished. All REMs should have been

removed. Do a ?FRE(I) to see how much space has been recovered.

and MICROPROMPT

S. Jaworski, Walsall

1E8Ø A9 Ø1 85 30 A9 85 31 03 1E88 AQ. 60 85 38 AØ nn FA BI 1E90 30 DØ 2E **C8** B1 30 DØ 29 1E98 A5 FØ 22 A9 00 Q1 38 **A8** 1EAØ 36 **C**8 91 36 38 A5 30 E5 IEA: 36 85 36 A5 31 E5 37 85 IEBØ 37 38 A 5 7B E5 36 85 7**B** 1EB8 A.5 7C E5 37 85 7C 4C 74 1FCØ A 2 AØ 00 FA BI 30 85 32 1EC8 **C**8 **B**1 30 85 33 AØ 04 EA 1EDØ 30 **C**9 8E DØ B1 1 B A5 38 A5 1ED8 DØ ØC 30 85 36 A5 31 1EEC 85 37 A9 ØL 85 38 A5 32 1EE8 85 30 A 5 33 85 31 4C 8C 1EFØ 1E A5 38 DØ 2D AØ 05 EA **TEER** FØ R1 30 EØ FA CQ 8F 04 1F00 **C**8 4**C F8** 1E 18 98 65 30 1F08 A9 00 85 85 36 65 31 37 91 1F10 A9 00 88 30 **A8** A5 36 1F18 91 30 **C**8 A S 37 91 30 40 1F20 E5 85 E2 1E 38 A 5 30 36 1F28 2CE5 A5 31 37 85 2D38 1F30 A5 **7B** E5 2C85 7B A5 7C 1F38 E5 2D85 7C A5 36 85 2E1F40 **A**5 37 85 2F A 5 30 85 34 1F48 A5 31 85 35 AØ 00 EA 38 1F50-B1 30 85 32 E5 2C91 30 1F58 **C**8 30 E5 2D 91 **B1** 85 33 1F6Ø 3Ø A5 33 FØ ØB A5 32 88 1F68 85 3Ø A5 33 85 31 4C 4C 1F70 1F DØ **F1** 00 91 A 5 32 A9 1F78 ØØ EA 30 **C**8 91 30 88 AØ **B**1 91 **E6** 1F80 34 36 **E6** 36 34 1F88 A.5 34 DØ 02 E6 35 A.5 36 1F90 DØ Ø2 **E6** 37 A5 37 C5 7C 1F98 C5 DØ EØ DØ E6 A5 36 7B 85 1FAØ A5 2E 30 A5 2F 85 31 85 4C 8C 1FA8 A9 ØØ 38 1**E**

HELP!

Sir—I would very much like to hear from any reader who might be in a position to supply me with either a R.O.M., tape or just a listing of the full advertised plot routines for the Computer User Aids UK101 High Resolution Board

> Harry Odes, London.

ZX81 SCREEN SAVE

Sir—This should interest owners of the ZX81 (16K), and provide a means whereby the contents of the screen can be recorded on tape and then retrieved at a later date.

The program puts the contents of the display file into a numeric string, which is recorded on tape following the command Save. After a Load instruction this same string is loaded into memory and on the command GOTO 50 the string is POKED into the new display file. There is just one important proviso: Do not use the instruction Run, as its use will wipe out the string and cause the program to crash. Lines 18, 40, 42, 52, 54, 56, 76 and 78 check for just such a crash and advise the user should it happen.

The Screen Save program is meant to run with any other user program (space permitting) and has been specially condensed into less than 100 lines such that it can be sandwiched into existing programs. To illustrate the point, Screen Save (lines 10-80) has been written in conjunction with "Cheese Nibbler" (lines 95–130).

To operate the program/programs run "Cheese Nibbler" at 100. When an interesting pattern presents itself, press any key which will cause the display to be memorised in "A" string. At this stage the program and the display can be taped by "SAVE Screen Save". At a later date the tape can be loaded back with "LOAD Screen Save". The original display is available on the command "GOTO 50" or the "Cheese Nibbler" program is entered on the instruction "RUN 100". The illegal command "RUN" or "RUN 50" will cause a crash into the user advice in line 78.

Incidentally I do not claim any originality for "Cheese Nibbler"; it is straight out of the ZX81 BASIC programming book chapter 18.

- J. Vella, Carlisle,
- 10 REM "SCREEN SAVE"
- 12 REM "TO RETRIEVE DISPLAY, ASK ZX81 TO GOTO 56"
- 14 REM "A,C,D,E,L,P,Q,V USED AS SUBSCRIPTS IN PRG 1-90"
- 16 REM "MAIN PRG AT 100"
- 18 GOTO 76
- 20 FAST
- 22 LET D=PEEK 16396+256* PEEK 16397
- 24 LET V=PEEK 164ØØ+256* PEEK 164Ø1
- 26 LET L=V-D
- 28 DIM A (L)
- 30 LET Q=0
- 32 FOR P=D TO (V-I)
- 34 LET Q=Q+1
- 36 LET A (Q)=PEEK P
- 38 NEXT P
- 40 LET E=PEEK 16405

- 42 POKE 16507, E
- 44 PRINT AT 21, Ø;" DISPLAY SAVED IN MEMORY "
- 46 SLOW
- 48 GOTO 100
- 50 FAST
- 52 LET C=PEEK 16507
- 54 LET E=PEEK 164Ø5 56 IF E>C+1 OR E<C-1 THEN
- GOTO 76 ' 58 LET D=PEEK 16396+256*
- PEEK 16397
- 60 LET V=PEEK 16400+256* PEEK 16401
- 62 LET Q=Ø
- 64 FOR P=D TO (V-2)
- 68 POKE P, A (Q)
- 70 NEXT P
- 72 SLOW
- 74 GOTO 140
- 76 SLOW
- 78 PRINT" YOU HAVE WIPED OUT THE DATA RELOAD TAPE AND GOTO 50 MAIN PROG AT 100"
- 80 STOP
- 95 REM "CHEESE NIBBLER"
- 100 PLOT INT (RND*64), INT (RND*44)
- 110 UNPLOT INT (RND*64), INT (RND*44)
- 120 IF CODE INKEY\$=0 THEN GOTO 100
- 130 GOTO 20
- 140 STOP
- NOTE: Bold characters represent inverse videc



Temperature Sense

Sir—As a regular reader of PE, I was interested in the article *Gas Saver* in the December issue. The point of my letter concerns additional experiments (using diode sensors on a solid fuel system), and these included monitoring the hot water tank temperature to obtain a differential control of the system in a similar manner to the author's; and there may be a simpler method of assessing the hot water tank temperature indirectly. This entails siting the "remote" sensor at the boiler end of the hot water return pipe rather than on the storage tank itself.

Due to the exchange losses in the boiler the temperature in the return pipe will initially be lower than the outflow pipe, but will increase as less heat is absorbed in the heat exchanger, and it is possible to obtain a correlation between the pipes' differential and tank temperature.

The reason for my suggestion is two-fold it removes the possible requirements of any structural work for the feed wire and access to the tank, and therefore reduces the feed wire to a foot or two. The length of this lead caused me problems, not structural as I only had a free lead, but I found that due to the length of the lead my central heating was being operated by my son's CB, even after I used screened lead and attempted several filtering methods.

This suggestion is offered to anyone suffering from a similar problem, as it would not appear to entail any circuit changes, and the original calibration could accommodate it.

N. L. Smith, Stoke-on Trent.

Chip Query

Sir—In your current issue is a letter by E. J. Hatch about the series "Introduction to Digital Electronics". I endorse what he says but I would like to query your reply, giving a list of necessary i.c.'s; the last of these is given as 745124, which doesn't exist.

Could you please tell me what was intended? Also do we need more than one of any of these i.c.'s?

> J. A. J. Jarvis Chester.

We are sorry but an error did in fact creep into our reply. The 745124 should have been a 745124 which is available from Watford Electronics.

Only one of each of the i.c.s is necessary.

BAZAAR

NEEDED to complete collection: 'Practical Electronics' volume One issue Three (January 1965) any price considered. Pete Wilcox, Cottage No. 2, Kilduncan Farm, Kingsbarns, Nr. St. Andrews, Fife, Scotland KY16 8QF. Tel: St. Andrews 76161, Ext. 7269, 9a.m.–5.30p.m.

UK101, cased, Cegmon-screen and keyboard expansions. 20K RAM, five extended ROMS, sound, software, manuals. £100. D. Fellows, 26 Westbourne Avenue, Emsworth, Hants, P010 7QU.

ACORN Atom 12K RAM 12K ROM, software including asteroids invaders power supply leads and manuals included £120 o.n.o. lan Wood, 118 Burford, Brookside, Telford, Shropshire, TF3 1LL. Tel: Telford 592973.

FREE! Diodes small types. Send s.a.e. by return. Also clearing bags of components. Wanted C.B. sets. Dave, 29 St. Johns Close, Leatherhead, Surrey.

TEKTRONIX oscilloscopes, dual trace, dual timebase. Good condition. 545A £130. 545B £160. Airmec type 399 oscillator £35. T. J. L. Haley, 8 Woodhall Gate, Pinner, Middlesex. Tel: 01-868 4221.

2716–1/2 Intel. Eproms. £1 each or £30 the lot (35 Eproms). An exchange would be considered (EG 6116 RAMS), L. Faragher, 17 Lyndene Close, Earlshilton, Leics. Tel: Hinckley (0455) 46354.

ELECTRIC piano with pedals (soft and sustaln). Has 3 voices: piano, honky-tonk and harpsichord, £130. Mr. A. R. Andrews, 6 Lower Bevendean Ave, Brighton, E. Sussex BN2 4FE. Tel: (0273) 606755 Ex. 608 (office hours).



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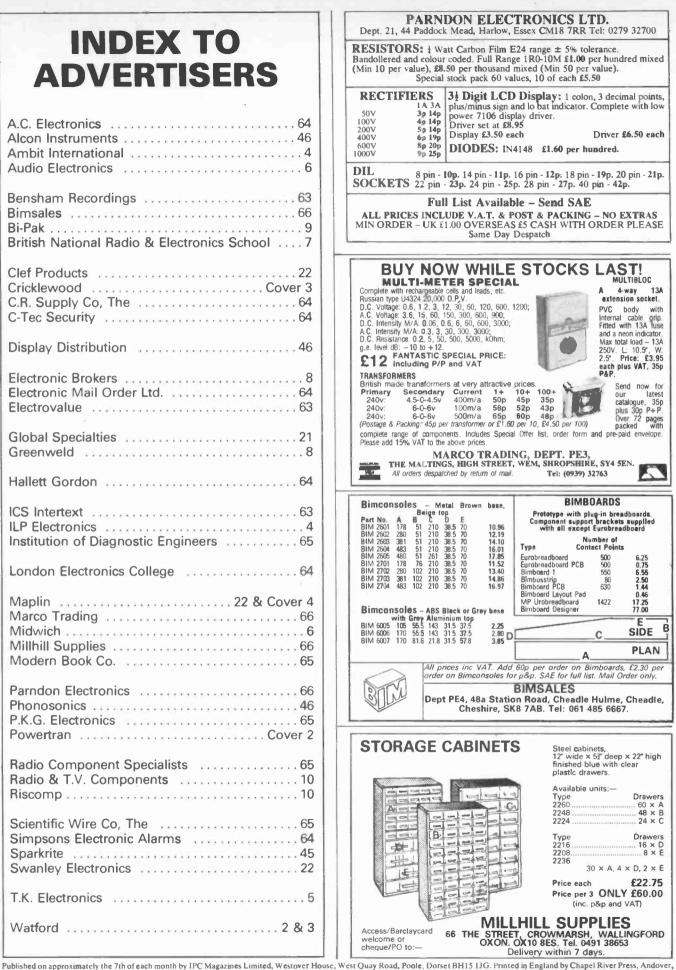






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Computing Shop



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27p 37p 25p	H 549 H 5493 B 549C	13p 14p 15p	BU226 BU3265 BU406	3 95 2 35 1.45	1N4001 1N4002 1N4003	4р 4%р 5р	OPT many in	ήC	TBA530 TBA5300 TBA540 TBA5400	2.55 2.76 2.72 2.74	PRICES P METRE	PE R E
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55p 1 00 10p 12p	BC 558 BC 558 BC 558A	16p 16p 14p 15p	E430 J300 J310	5.95 70p	1N4007 1N4009 1N4148	7р 20р 3р	R Red G = Green Y + Yellow		TBA570 TBA5700 TDA1002	2 87 2.37 2.48 3 39	Twin 2 % An	np 16p
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37p 29p 30p	BCY70 BCY71 BCY72	16p 16p 19p	MJ3000 MJ3001 MJ4502	2 19 2 25 3 99	1544 BA102 BA115	10p 25p 25p	R1M G1M V1M	25p 27p 27p	TDA2611A TDA7000 TL061	2 50 3 45 40p	4 Core 4 Sc	44p
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20p 10p 12p 13p	BD 136 BD 137 BD 138 BD 139	35p 37p 37p 38p	MJ15016 MJE340 MJE350 MJE2955	3 34 53p 1 50	BA155 BA156 BA157	15p 38p 25p	Y 5C Super bri high effici	17p ght	TL072 TL074 TL081 TL082	45p 1 35 34p 45p	12 Core Heavy Duty MikelGuitar Lead	80p
13p 10p 12p	BD140 BD237 3D238	38p 98p 98p	MJE 2955 MJE 3055 MJE 2955T MJE 3055T	1 95 1 95 99p	BA158 BA150 BA182	30p 32p 40p	Large (100 brighte R5U	times r) 38p	TL084 UAA170 UAA180	1 20 2 49 2 49	AERIAL 50Ω RG 58A 75Ω UHF	ιI
13p 35p 23p	80239A 80239C 80240A	57p 64p 59p	MPSA05 MPSA06 MPSA10	69p 23p 25p 28p	BA201 BA202 BA316 BA317	18p 26p 25p	G5U Y5U Rectange	42p 42p Jar	ULN2003 UPC 575C2 UPC 1156	75p 2.00 2 75	75Ω VHF 300Ω Flat RAINBO	28p 14p
27p 11p 12p	8D 240C 8D 241A 8D 241C	73p 61p 67p	MPSA12 MPSA13 MPSA14	29p 48p 46p	BA318 BAV10 BAV19	25p 30p 16p 15p	Stackable R5R G5R Y5R	17p 18p	UPC1156H UPC1182 UPC1185	2 75 3 75 1 95	Prices per 8 way	1001 25p
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13p 18p 42p	BD245A BD245C BD246A	1 14 1 30 1 20	MPSA56 MPSA65 MPSA66	30p 40p 47p	SCF 's		CA3048 CA3059 CA3090A0	2 15 2 80 3 70	FORMEI A 240V Po	RS mary	40 way 64 way	88p 1.49
48p 10p 10p 13p	BD246C BC249A BD249C BD250A	1 50 2 00 2 31 2 11	MPSA70 MPSA92 MPSA93 MPSL01	45p 39p 39p 46p	TRIACS DIACS		CA3130E CA3130T CA3140E CA3140T	87p 235 39p 140	6 0 6V 9 0 9 12 0 12V 15 0 15V	IV	BATTER Top qualit	IES
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16p 25p 26p	BD440 BD441 8D442	91p 91p 93p	MPSU51 MPSU55 MPSU56	88p 58p 59p	M 600V TIC 105A TIC 1053	46p 47p	ICM7555 ICM7556 LC7120	80p 1 50 3 20	0 - 6 - 6 - 9 -	9.50 9 4.25	HP2(4AH) HP7(5AH) HP11(12AH) PP3(110mAH	4 75 99p 2 29
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20p 25p 25p 27p	BD 538 BD 538 BD 539	75p 80p 80p 80p	TIP 30A TIP 30C TIP 31A	38p 35p 36p 33p	TIC116A TIC116A	66p 68p	LF351 LF353 LF355 LF356	47p 92p 83p 92p	credit any difference			6 of 15.59
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10p 11p 12p	BD 678 BD 711 BD 712	83p 132 132	11P34C 11P35A 11P35C	88p 1 09 1 28	12A TIC 1260 TIC 1250 TIC 1250 TIC 125M	73p 77p 96p	LM379S LM380N14 LM380NB	5.50 75p 1.50	25 - 17 375 - 17	2 99 3 85 4 93	HP7 (Up to 4 time) £	5 85
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24p	BF 196 BF 197 BF 198	12p 12p 15p	TIP110 TIP112 TIP115	74p 90p 81p	TIC 236D(12	2A) 1.16	LM 23CH LM 23CN LM 25CH LM 725CN	35p 3.40 3.19	PCB MAT	6p	No 2 (Small) No 3 (Med) No 6 (Micro)	85p
12 p 13 p	BF 199 BF 200 BF 224J	15p 75p 32p	TIP115 TIP117 TIP120 TIP122	96p 69p 73p	TiC 2530(20	1 22 0A) 1 90	LM741CH LM741CN LM741CN1	96p 18p 480p	FERRIC CHLORID Quick dissol	vina i	XS 240 X 25 No 50 ISmal	845 11 85p
14p	BF225J BF244A BF244B BF245A	55p)	TIP125 TIP127 TIP130 TIP132	84p 84p 93p 93p	TIC 263D(25	5A) 2 11	LM747CN LM748CH LM748CN LM1871	69p 1.00 35p	Enough to m over 1 litre ETCH RESI TRANSFEI	1.69 ST	No 51 (Med No 52 (Lge) SOLDER 125	185p 85p
11p 12p 13p	8F2458 8F246 8F246A	65p	TIP135	99p 99p	BR 100 ST 2	29p 29p	LM1872 LM1877	3.25 4.39 5.95 7.44	1 Thin lines 2 Thick line	s	18swg 22swg PLUGS	2.95 3.10
10p 13p 13p	BF 24 6B 8F 24 7A BF 24 7B	75p 75p	TIP 140 TIP 142 TIP 145 TIP 147	1 04	ZENER		LM1889 LM2907N LM2907NB	3 77	3 Thin bend 4 Thick ber 5 DIL pade 6 Transisto	ds	D' Connec	TS tors
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13p 10p 13p	BF256B BF256C BF257	58p 65p 30p	TIS43 TIS88A VN10KM	50p 80p 60p	2 4 4 7	7p	LM3911 LM3914 LM3915	1 20 3 25 3 25	9 Mixture. Any shee	1 of	Male	1.60 2.09 1.00
14p 14p 16p	BF258 BF259 BF457 BF458 BF458 BF459	32p 35p 46p	VN46AF VN66AF ZTX107 ZTX108	95p 99p 10p	E 24 Series 3 3 82V	14p	LM13600 MF10 NE531N	1 15 3 50 1 36	above GRADE OF GLASS PCB	35p VE	Phono Plu Bik Red, Grn Wt or Yell	as
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16p 17p 15p	BFR 39 BFR 40 BFR 41	25p 25p 25p	ZTX 301 ZTX 302 ZTX 303 ZTX 304	15p 15p 23p 15p	1 amp ty W01 100* W02 (200)	28p	NE 556 NE 558 NE 560 NE 565	65p 1.89 3.25 1.18	420 · 245m	195	Quad ZIF SOCK	40p
16p 17p 18p	8FR 79 8FR 80 8FR 81	25p 25p 25p	2TX310 2TX311 2TX312	35p 32p 35p	W04 200 A 08 800 amp type	34p 38p 50p	NE 566 NE 567 NE 570	1.49	DALO ETC RESIST PE	H N	28pm 40pm	4 35 5 00 5 35
45p 44p 43p	8FR90 8FS28 8FS61	2 11 2.95 1 00	2TX313 2TX314 2TX320 2TX330	36p 24p 35p	Stuare with 501 (100) 52 (200)	46p 50p	NE571 NE5534A RC4194	3.99 1.45 3.95	PHOTO SENSITIVE 1st Class Epr	РСВ	TOGGLE IM	49p
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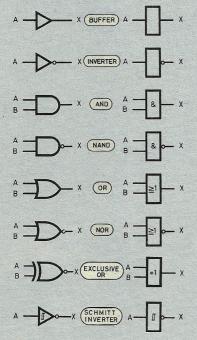


DIGITAL LOGIC

Digital logic is based on the idea of only two (binary) states. These two states are known variously as true & false, on & off, logic 1 & logic 0, or more frequently just 1 & 0. A digital signal is always in one of these two states (or moving between them). Digital logic gates allow these signals to be manipulated. Suitable combinations of digital signals and logic gates allow circuits to be built to perform a wide range of useful functions.

LOGIC SYMBOLS

Digital circuit diagrams use standard symbols to represent logic gates. The most frequently used symbols are from the BS or the MIL series. The common symbols from these two series are shown below.



PIN NUMBERING

TTL i.c.s are usually in dual-in-line (d.i.l.) packages. These have oblong plastic or ceramic bodies which protect the silicon chip. Parallel rows of pins 0.1'' apart protrude from the two long sides of the i.c., with a total of usually 14, 16 or 24 pins. The pins are numbered anti-clockwise from 1 when look-

ing from the top (i.e. pins pointing downwards). The end of the package containing pin 1 is identified by an indentation, and/or there is a smaller hole next to pin 1.

GATE FUNCTIONS

A two-input gate can have 16 possible functions. Not all of these are actually available as logic gates. The table below identifies the possible inputs, with their corresponding outputs, for all 16 functions.

LOGICAL	INPUTS				\land
FUNCTION	A=0 B=0	A=0 B=1	A=1 B=0	A=1 B=1	
LOGIC O	0	0	0	0	325
A.8	0	0	0	1	
n/a	0	0	1	0	
А	0	0	1	1	
n/a	0	1	0	0	
В	0	1	0	1	ruc
A⊙B	0	1	1	0	OUTPUTS
A + B	0	1	1	1	SLI
A+B	1	0	0	0	
Ā⊙B	1	0	0	1	
B	1	0	1	0	
n/a	1	0	1	1	
Ā	1	1	0	0	
n/a	• 1	1	0	1	
A.B	1	1	1	0	
LOGIC 1	1	1	1	1	

7400 TTL FAMILY

Logic families are collections of logic gates based on the same basic gate, and they greatly simplify the construction of logic circuits. Gates from a family all use a common power supply, and they may be connected together using a simple set of rules, safe in the knowledge that they are all compatible. The most common family is the 7400 series of TTL gates. Within this family there are a number of sub-families, and the numbering of TTL i.c.s is according to the following general rules.

SN74LS86N

- SN Manufacturer's prefix (may be any letters)
- 74 Indicates 7400 series TTL
- LS Indicates which TTL subfamily:

null =	= standard	LS = low-power
H = H	high speed	Schottky
L = Ic	ow power	S = Schottky
86	Indicates	gate function
	e.g. 00 =	quad 2-i/p NAND
	86 = 0	quad 2-i/p Ex-OR

N Manufacturer's package code e.g. N = plastic d.i.l. pack

Typically, TTL i.c.s are referred to in circuits without any reference to the manufacturer's prefix or suffix, e.g. the device above would be described as a 74LS86.

LOGIC LEVELS

The voltage levels used to represent logic 0 and logic 1 are defined for TTL signals as below. Voltages between these levels are not permitted TTL levels.

Gate outputs	OV to +0.8V	
	Logic 1	Above +2.4V
Gate inputs:	Logic O	OV to +0.8V
	Logic 1	Above +2.0V

An unloaded standard TTL gate has output levels of around +0.2V for logic 0 and +3.5V for logic 1. These levels tend to move up and down, respectively, as more gates are connected to the output.

BOOLEAN SYMBOLS

Boolean Algebra is a shorthand way of representing the behaviour of gates. It uses true and false to represent logic 1 and logic 0. For inputs of A and B, and an output of X, the Boolean shorthand for the common gates is as follows.

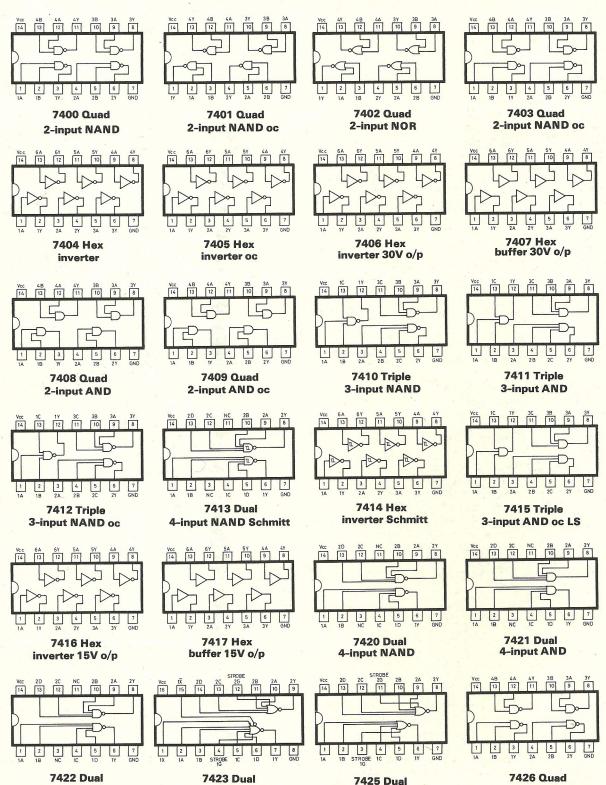
Buffer	X = A
Inverter	$X = \overline{A}$
AND	$X = A \cdot B$
OR	X = A + B
NAND	$X = \overline{A \cdot B}$
NOR	$X = \overline{A + B}$
Exclusive-OR	$X = A \oplus B$

USEFUL IDENTITIES

The following are useful Boolean Identities which allow simplification of logic circuits, or the use of a smaller number of different gates, to perform the same function.

A + 0 = A	A.0=0	$A \oplus 0 = A$
A + 1 = 1	A.1=A	$A \oplus 1 = \overline{A}$
A + A = A	$A \cdot A = A$	$A \oplus A = 0$
$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$	$A \oplus \overline{A} = 1$
	$\overline{\overline{A}} = A$	

When looking at inverting gates, each logical inversion introduces an over-rule on the signal (to represent the inversion). Over-rules of *identical* length cancel out in pairs, as indicated in the last identity.



4-input NAND oc

7423 Dual 4-input NOR expand 7426 Quad 2-input NAND high volts

4-input NOR strobe