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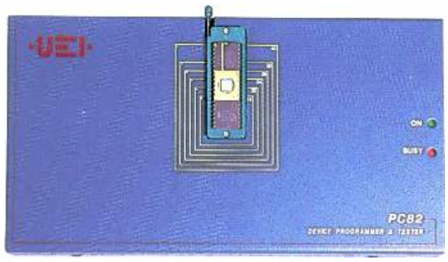

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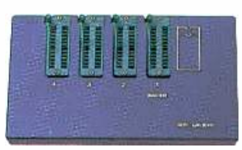

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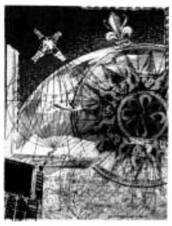

Cover: Kevin Clarkson

REGULARS

In next month's issue: Compressing the waves. Speech compression, with the aim of increasing perceived loudness, forms part of nearly every audio communications system. A new system, which works by compressing the waveform on a cycle-by-cycle basis represents a genuine advance on speech processing technology.
JANUARY ISSUE IS ON SALE DECEMBER 31

EDITOR
Frank Ogden
081-652 3128

DEPUTY EDITOR
Jonathan Campbell
081-652 8638

CONSULTANT
Derek Rowe

DESIGN & PRODUCTION
Alan Kerr

EDITORIAL ADMINISTRATION
Lorraine Spindler
081-652 3614

SALES MANAGER
Patrick Irwin
081-652 3732

SALES EXECUTIVES
Pat Bunce
081-652 8339

ADVERTISING PRODUCTION
Shirley Lawrence
081-652 8659

PUBLISHER
Robert Marcus

EDITORIAL FACSIMILE
081-652 8956

CLASSIFIED FACSIMILE
081-652 8931

Focusing on power lines

Last month's issue carried an article "Natural radiation focused by power lines" written by consultant and amateur scientist Tony Hopwood. Mr Hopwood postulated that most rare of things, an original idea and, like the best ones, it was simple.

The principal components of natural background radiation are low velocity charged particles. They arise from natural radioactive decay products, solar eruptions and molecular ionisation by high energy cosmic ray photons. There is general agreement that charged particle radiation is particularly active, biologically speaking. For instance, radioactive radon gas derived from decaying uranic elements in granite induces lung cancer through alpha particle emission. There is no dispute about this.

Mr Hopwood, a man long interested in solar geomagnetic activity, predicted that interaction between the magnetic field surrounding power lines might deflect charged particle radiation (of all origins) into radiation belts focused either side of the cable run. Armed with a portable thin walled G-M counter he looked for confirmation of his hypothesis.

He claims in his article that he has found it. Having made "hundreds of readings" of background radiation in an orthogonal traverse below power lines, he reports an averaged increase of 100 per cent in background radiation at a critical distance from the power line centre, a distance which seems to relate both trigonometrically to the height of the line and electrically to the intensity of the magnetic field.

What makes Mr Hopwood's idea so interesting is that it does not conflict with known physics and neither does it require a new explanation for disease pathology.

I have always taken the view that statistical, and its near relation hearsay, evidence connecting powerlines and other sustained non-ionising field exposure to disease has occurred too frequently to be ignored. After all, it should be remembered that the whole business arose out of medical epidemiologists researching childhood leukaemia clusters. But I have never been terribly happy with some of the explanations put forward for the apparent effects: low energy cyclotron resonance in calcium ions for example. This might be a factor but it is not half as compelling as, say, a simple increase in whole body radiation exposure.

Occam's razor works in favour of Tony Hopwood.

When we published the article last month, National Power referred journalists to the findings of an enquiry into the effects of non-ionising radiation carried out by Sir Richard Doll. His report said that there was no proven link. I am inclined to Sir Richard's view but this would be to miss the point. The Doll Report considered scientific work on the direct effects of low frequency exposure which would of course not show the effects contained in Mr Hopwood's hypothesis.

Proving or debunking Mr Hopwood's ideas would be about as cheap as environmental health research could be. Sir Richard Doll may not have the last word on power line related disease until this is undertaken.

Frank Ogden

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68060 the last instruction to 68k processor family?

America's biggest semiconductor maker Motorola has released details of the next addition to its long-established *68000* cisc line, possibly the last in this family.

The company recently announced it had produced silicon for the first *PowerPC* risc microprocessor. Developed along with IBM, this is a single chip implementation of IBM's *RS/6000* risc chipsets and will be used in future desktop and portable machines from IBM and Apple.

Motorola teamed up with the two computer makers because it had manifestly failed to gain acceptance for its earlier risc microprocessor, the *88000* family, as a standard engine to power high-performance computers.

Now in its second generation, the 88K has had some success in high-end servers and niche graphics processing applications and Motorola spokesmen react defensively to any suggestions that it may be "de-emphasised": "I bet some of the smaller sparc makers would be very happy with the revenues we get from the *88000*" said the company's Clive Gay.

The advent of the *PowerPC* has led to doubts about the future of the *68000* cisc processor, currently the brains in Apple's computers. The same family was also found in Unix workstations a few years ago, but most computer makers in that line have moved towards risc microprocessors such as the sparc (Sun Microsystems), or PA-risc (Hewlett Packard/Apollo). However, Motorola insists that at least three future generations of *68000* will be built, the first of which will be the *68060* due to sample in the latter part of next year.

It been set the target of tripling the performance of its predecessor the *68040* and has incorporated many risc-like features to do so.

These include a superscalar implementation allowing instructions to be executed in a single cycle, multiple pipelines, independent execution units and a dedicated unit to predict and prefetch instructions that are required following a branch.

The *68060* has a Harvard architecture, where separate paths are provided to the execution units for data and instructions. Each path has a separate 8KByte cache memory, allowing instructions and data to be accessed simultaneously by the instruction units.

The 060, which will contain two million 0.5μm transistors, has independent instruction and data memory management units. The full addressing range is 4GBytes, and each MMU can support demand-paged virtual memory operating systems with either 4 or 8KByte page sizes. They also provide write protection on a page by page basis.

Electronics in the driving seat

Stricter emission controls continue to be the driving force behind vehicle electronics, but the emphasis – as seen at last October's Motor Show – is changing to communications between subsystems.

Safety is being linked to engine management, and most of the components for the era of drive-by-wire are in place or in development.

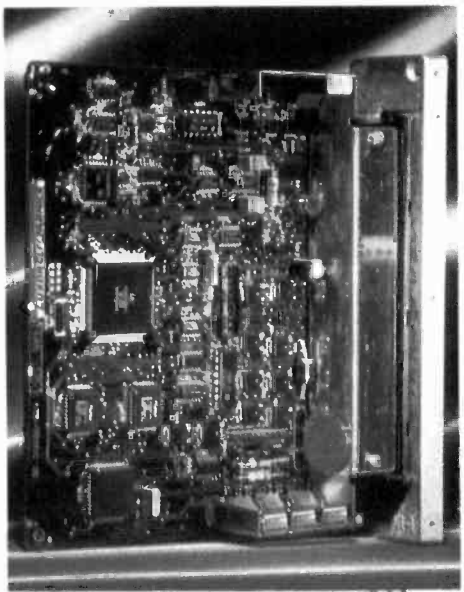
Although electronic fuel injection for petrol engines is celebrating its 25th anniversary (the Bosch Jetronic system was introduced in 1962 to help Volkswagen meet the first Californian emission limits), diesel engines are only now beginning to catch up. One example is the new BMW diesel, due in the showrooms in January. Electronic injection/ignition is also a key factor in the use of compressed natural gas (CNG) to fuel vehicles.

Even small cars now incorporate engine management units. The new Nissan Micra, launched at the show, has a 16-bit microcomputer control unit, as well as an anti-lock braking system linked to the computer-controlled continuously-variable automatic transmission.

Elsewhere, ABS is being linked to engine management systems to improve traction control. Bosch's new electronically-managed suspension and four-wheel steering systems also interact with ABS. In future, the ABS wheel-speed sensor may also provide information for map-matching in car navigation systems.

Leaving horsepower aside, prizes for sheer computing power in engine management go to Saab with its new 32-bit Trionic system. It carries out two million calculations per second and, for every 500cm travelled at 50mph, produces enough information to fill an office binder.

The need for this awesome number-crunching capacity, says Saab, is because smaller engine management systems – 8 or 16-bit – can only cope when the engine is in a steady state at more or less constant speed and load. Control of fuel injection and ignition timing goes somewhat to pieces in transient conditions – acceleration or



Saab's 32-bit Trionic engine management computer meets 1999 Californian emission levels and even cleans up exhaust from other cars; it is fitted to new 9000 2.3 litre turbo models

Cache coherency is maintained between main memory caches by snooping the external bus. The bus snooper has priority over the execution units.

A new feature is an instruction fetch controller that operates in front of the main instruction pipeline. It has its own fetch pipeline that calls up instructions before they are needed by the instruction controller and its object is to keep the instruction execution pipeline loaded.

According to Jack Browne, Motorola's director of 68K operations: "Branches occur 80 per cent of the time, so if we can improve our branch prediction, we can improve the overall performance."

A branch target cache allows the instruction fetch pipeline to detect and change the instruction stream before the change of flow affects the instruction execution controller. It is examined for a valid branch entry after each instruction fetch address is generated in the fetch pipeline.

If a cache hit does not occur, the fetch

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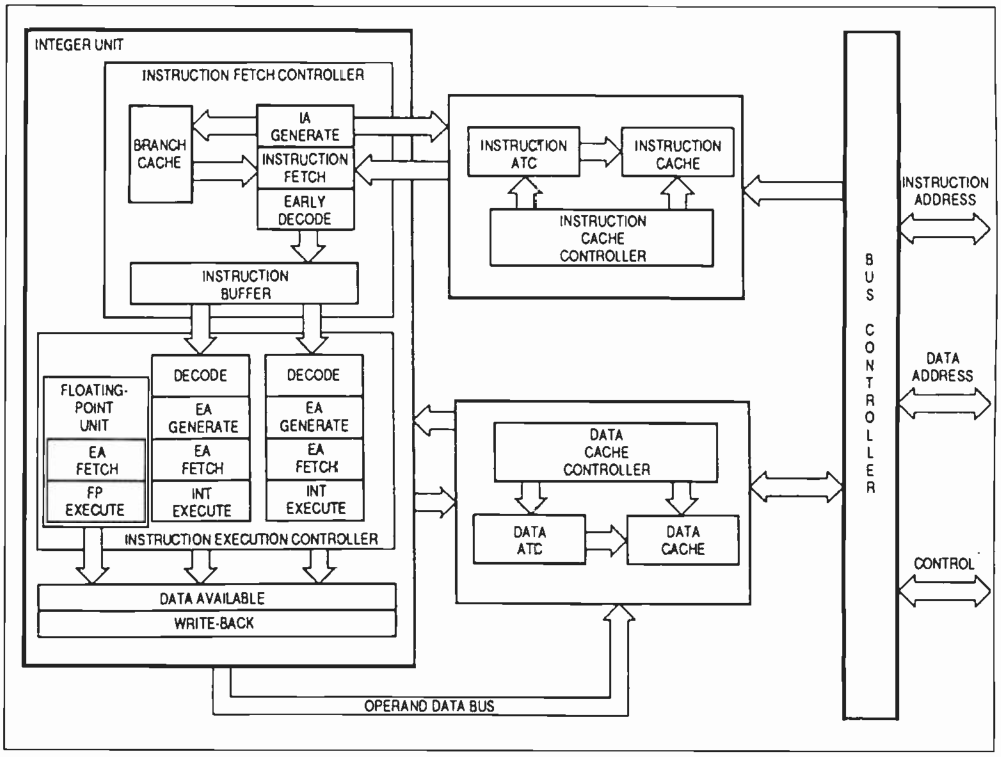


deceleration – and calculations become approximate until the speed settles down again. Too much fuel is used and emission levels rise.

The Saab Trionic system fitted to the 9000 2.3 Turbo is designed to exercise precise control in all conditions; it even checks for accelerator movement during each individual fuel injection pulse and adjusts the timing accordingly. The result is an integrated system capable not only of meeting proposed 1999 California emission control levels but also of cleaning up other cars' exhausts, as a video demonstration showed.

A new Trionic-equipped car, emitting hydrocarbons at 10ppm and nitrogen oxides at 0.01%, had the exhaust from a 1950s Saab 2-stroke, belching out 2000ppm of hydrocarbons and 1.5% nitrogen oxide, fed into its air intake. Levels from the new car's exhaust immediately shot up but within a few seconds settled back to their original figures.

By 1995, it has been predicted that electronics will comprise 15% of a new car's cost. A good proportion of that will be elsewhere than under the bonnet.

One of the most imaginative recent developments has been Lotus Engineering's work on noise cancellation, using inverted noise feedback played through the standard car stereo speakers following processing by a DSP system. This has now reached production stage, with a system manufactured by Hitachi being fitted as an option in the Nissan Bluebird in Japan. Lotus is now working on road noise and exhaust noise cancellation.

Driver aids, or what the industry calls MMI (man/machine interface) mostly rely on electronics. Bosch demonstrated a new reversing aid called Parkpilot, a set of ultrasonic sensors mounted on the rear bumper and connected to a dashboard display which let you know when you are getting too close to the car behind, or a bollard or a wall.

A more ambitious project – said by Lucas to be close to the market – is intelligent cruise control, an adaptation of microwave technology designed for missile seeker heads. A front-mounted sensor locks on to the vehicle in front and then regulates speed to maintain a safe distance from it. Such developments currently raise more questions than answers. (What do you do if a juggernaut is too close behind you?) The next task agreed by all is to address the integration of all these devices, and develop hierarchies of control.

Fight to drive

There is much jockeying for the right to do the integrating. Lucas and Bosch are established motor industry developer/suppliers but Philips claims to be slowly evolving into a car components company. Through a joint venture with Acustar of America it is developing car information systems, integrated instrument panels on which to display them and multiplex systems to replace the ever-increasing quantities of wiring which would otherwise be required. Progress so far can be seen in the new Renault Safrane – a double-DIN CD/radio/cellular-phone panel, linked to a control stalk on the steering column and an information display below the windscreen. In its more recognised role, Philips was showing a prototype of the first in-car DCC unit, due next spring.

Car navigation progresses slowly. Blaupunkt has at last brought to market – on its Stockholm model – the long-awaited TIM traffic memo function, which stores on a speech chip any RDS traffic messages broadcast while the driver is out of the car. Four minutes-worth, constantly renewed, can be held, covering a user-selectable period of three hours.

Carin, the Philips route guide, has stalled in the UK for want of suitable digital maps. Those which do exist cannot distinguish between, for instance, a railway bridge and a level crossing. On the continent, however, parts of Germany and France have been mapped and Carin is promised by Philips as standard equipment on a continental luxury car (my guess would be a Renault) in the autumn of next year.

A Ford approach to vehicle location uses satellite global positioning system (GPS) which would enable the driver to summon breakdown assistance without leaving the vehicle, and would also help police to track stolen vehicles.

Peter Willis.

pipeline continues fetching instructions sequentially. If a hit does occur, the current instruction stream is discarded and a new stream is fetched starting at the location indicated by the branch target cache.

A feature of the instruction execution controller is two integer execution pipelines. A floating-point execution unit is also included.

The on-chip floating point unit performs in hardware all the floating point instructions of earlier *68000* devices. Furthermore, it emulates in software IEEE-compliant exception handlers, and unimplemented data type and data format handlers.

As far as users of the new device go, Motorola claims that it will continue to dominate the embedded control market. This includes games machines such as Sega and Atari, telecommunications and automotive applications. Furthermore, there is still some mileage in the CPU stakes as Apple's Blueprint for the Nineties manifesto promises to adopt the 060 as an upgrade to its existing 040-based machines.

David D'Arcy, *Electronics Weekly*

Boom time for CD-ROM

Germany is also expected to set the pace for growth in the CD-rom market for PC systems.

German sales of CD-rom drives, which currently account for around 24% of the total $68.2 million European market, will increase rapidly to around $47 million by the year 1996, according to a report from international market research publisher, Frost and Sullivan. .

The UK, currently the second largest market, worth $15.2 million, will grow at a slower rate but will maintain its overall position by 1996 when it will be worth $35.6 million.

Cad asic start-up

Oxford Semiconductor has been formed to design and supply asics. Based in Abingdon, Oxfordshire, the new firm will also develop computer aided design (cad) tools to work in existing cad vendors' frameworks for asic design, and offer system level design services, including project management. The firm will buy silicon from a variety of asic foundries.

Oxford Semiconductor's managing director, Tim Cook, was formerly with venture capitalist Wardsend Associates, which has provided most of the finance for the company. Jalil Orace, previously with Harwell Instruments, is technical director and James Lewis, from Logical Integration, is marketing director.

HDTV in standard tv channel

BBC Engineering and Thomson-CSF Laboratories have co-operated and succeeded in transmitting digitally in a standard television channel, using a high spectral efficiency modulation technique.

The technique, in which a digital TV signal was broadcast in a standard 8MHz TV channel from a low power transmitter at Crystal Palace to a number of test sites in South London and Surrey, is part of a programme intended to bring digital HDTV to the public via terrestrial transmission networks.

The modulation technique which was developed in France by Thomson conveys about 60Mbit/s in a single 8MHz UHF TV channel. The system transmits two separate 30Mbit/s signals, one broadcast with horizontal polarisation, the other with vertical polarisation. Each signal consists of an OFDM (Orthogonal Frequency Division Modulation) ensemble of about 500 closely spaced carriers, all digitally modulated using 64QAM. In principle, with the addition of other work being carried out on digital compression, this would allow two HDTV programmes to be transmitted in one 8MHz TV channel.

Digital laser disc development

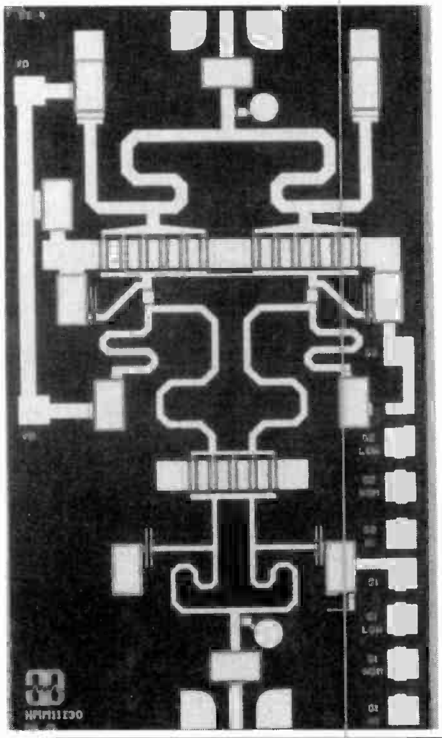
Pioneer, the Japanese consumer and industrial electronics firm, is developing digital versions of its recordable 12in. Laser disc system,aimed at professional users such as TV companies.

Yuichiro Yokoyama, head of business planning for Pioneer's industrial systems division, said the company intended to produce two different versions of the system: a high-end studio quality version for TV material, using JPEG image compression technology to condense individual frames, will be ready in 1995. A slightly lower-quality version, using MPEG-2 compression, is scheduled for 1994.

Applying synthetic diamonds

AT&T is claiming to have won the race to offer the first commercial application of synthetic diamond films in electronic heatsinks. The company has developed a synthetic diamond film that can be bonded electrically and has a thermal conductivity of more than 10W per degree Kelvin.cm. In some applications, it can better the 22W per degree Kelvin.cm conductivity that natural diamond offers.

The new synthetic diamond sub-mounts will be in production before the end of the year under licence from AT&T. Companies offering it will include chemical vapour deposit diamond specialists such as GE, Sumitomo Electric and Drukker, of the US, Japan and Holland respectively.



X-band mmics: Harris Microwave Semiconductor integrated X-band GaAs mmic is 100% tested on wafer for dc and rf performance.
Applications for X-band, which range from 8 to 12GHz, include the growing markets for airborne radar and commercial telecommunications.
With a rated minimum output power of 29.0dBm for driver and power applications, the directly cascadable HMM-11130 offers a complete mmic-based solution for mic hybrid replacement. Features that aid the design process include direct cascadability without interstage matching and an on-chip gate resistor network for simple bias point selection.

RESEARCH NOTES

Taking the uncertainty out of explosives

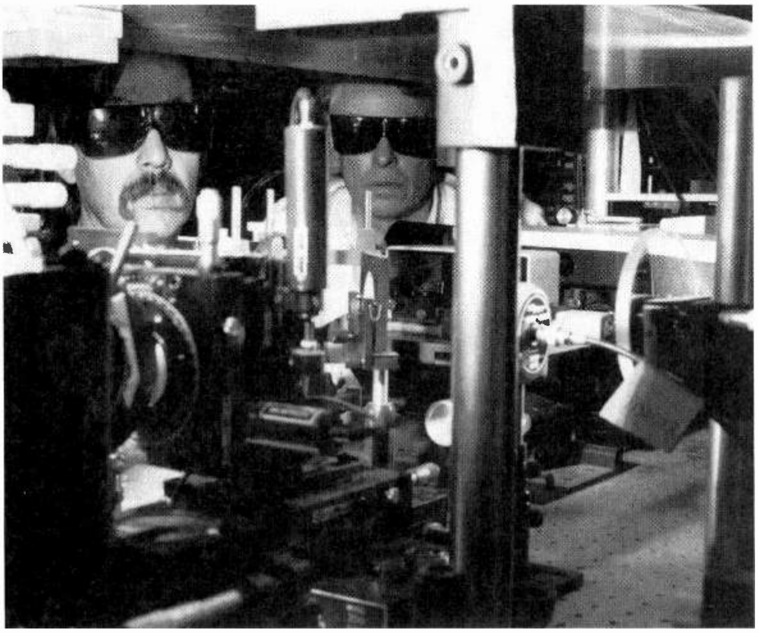
An optical detonator system for rockets and explosives that requires no electrical circuitry is the latest advance to come out of Los Alamos National Laboratories in New Mexico. The advantage – a fairly obvious one – is the virtual elimination of accidents.

Electrical detonators are universally employed for everything from quarry blasting to firing explosive bolts on satellites, but they are not without their risks. As Dr Dennis Paisley of the Los Alamos Detonation Systems Group puts it: "Once you put electrical wires against an explosive charge, you can easily induce electric current into the wires from stray electromagnetic fields and accidentally either fire the detonator or disable it".

Electrical detonation systems are usually extremely well designed, employing complex safety interlocks and well-screened circuitry. Even so there have been cases of rockets going off unbidden or of launches having to be cancelled because of the risk of malfunction during a thunderstorm.

The answer, says Paisley, is to use optical fibres which are effectively immune from natural or other interference. No naturally-occurring events (and few human generated ones) can deliver enough optical power to fire an explosive inadvertently.

Paisley's team, consisting of David Stahl, Nelson Montoya and Mel Garcia, is now going one stage further: putting explosives inside a Faraday cage with no metal intrusions. This excludes all electromagnetic fields and eliminates the risk of induced currents in metal parts. The only connection is a quartz fibre terminated in an aluminium cap (which if necessary can be part of the Faraday cage).



Optical explosion: Aluminium cap propelled to the speed of a micrometeorite by laser.

To fire the explosive the group sends a high-power laser pulse along the fibre. At its other end the pulse generates a plasma which propels the aluminium cap (400-600μm in diameter) at a speed of 4000 m/s into the explosive. The energy is enough to cause detonation, even of the most modern shock-proof explosives.

The optical detonator was originally developed for military applications. But it could well find uses in the mining industry and in oil exploration. The Los Alamos team identifies several benefits in addition to reducing the risk to those workers directly handling explosives. The fact that the system is completely immune to electromagnetic interference means other activities need not be prohibited during blasting. Workers nearby can continue to use welding gear, operate mobile radios and operate electrical switchgear.

When questioned about the high cost of using an expensive laser system, Dennis Paisley points out that many explosives systems cost hundreds of millions of dollars and often involve risks to dozens of lives (just think of the Space Shuttle). Also, the laser end of the detonator is infinitely re-usable: all that goes up in a puff of smoke is a few metres of quartz optic fibre.

As well as improving safety in the explosives industry, the Los Alamos optical detonator has a secondary use in space research. The fact that the fibre can propel a tiny metal disc at extraordinary speeds means that it can simulate the micro-meteorites that are such a hazard to spacecraft. Understanding how structures behave when shot at by microscopic projectiles flying at 4000m/s will provide valuable data for designing tomorrow's space vehicles

Crystal thinks it's a liquid (or is it the other way round)?

Using an ultra-fast laser system, scientists at the University of Rochester NY have heated a lead crystal above its melting point so quickly it does not have time to melt! Even though the crystal reaches 700K, 100° above its normal melting point, the crystals remain solid for a few critical picoseconds. The delay may not sound long, but it is enough time for the researchers to take a "snap-shot" of the material's superheated crystal structure – something rarely seen before in a metal.

Superheated solids, though less familiar than superheated liquids, have been studied for many years now. Some materials, like quartz, are relatively easy to superheat up to several hundreds of degrees above their normal bulk melting points: their high viscosity slows down the propagation of the solid/liquid interface.

Metals are much more difficult to superheat because they are far less viscous in the liquid form – though in the past some have been superheated, remaining solid a few degrees above their normal melting points. As long ago as 1939, Russian scientists superheated a crystal of tin by 2°

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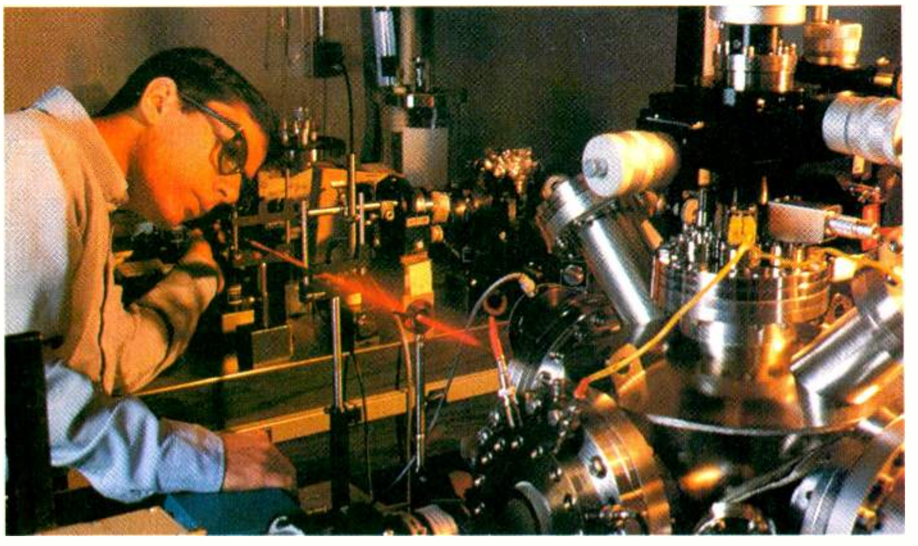

An ultra-fast laser is used to heat the sample and also to trigger the electronic camera.

by heating one part of the crystal while simultaneously cooling another. Superheating metals by more than a few tens of degrees above their melting points is nevertheless difficult.

But by using an ultra-fast Nd:yag laser, the Rochester team (*Phys Rev Lett Vol 69 No 8*) managed to catch a lead crystal in the midst of this transition from the ordered crystal state of a solid to the disordered state of a liquid. The temperature indicated that the crystal lattice should long since have broken down, but the atoms had not yet adapted to the temperature change. During the 180ps laser pulse a few atoms had begun to vibrate out of position, but not enough to have destroyed the lattice and transformed the solid into a liquid.

One key to the success of the experiment was the type of material used. The team used a lead crystal cut in such a way that the exposed surface had atoms packed more closely than usual. Because of the tight packing in this Pb{III} structure the atoms could not move out of place so quickly when heated.

To detect this picosecond superheated state, the researchers split their laser source into two beams: one to heat the sample and the other to activate the electron gun used to take the picture.

Electrons bombarded the sample just a few picoseconds after the sample was heated by the first part of the laser beam. They then bounced off the surface atoms to form a "reflection high-energy electron diffraction" pattern (rheed), an image of the crystal lattice. All before the crystal had time to realise that it shouldn't be a lattice any more!

Lights that make the radio fade

Back in the (good) old days when we all listened to LF and MF radios, the most common sources of interference seemed to be power tools and fluorescent lights. That of course has all changed with the advent of FM and digital signal technology... or has it? According to P Melançon and J Lebel of the Communications Research Centre in Ottawa (*Electronics Letters*, Vol 28, No 18), the fluorescent light has once more become the enemy of radio communicators, though not in a way that anyone could expect.

The problem came to light when researchers were investigating multipath propagation over indoor paths at 910MHz. Multipath is generally acknowledged to be the main source of indoor fading, though usually at a slow rate (less than 5Hz) and often the result of people moving around within the building. What puzzled the Canadian researchers was their discovery of rapid fading at a frequency of 120Hz, twice that of the Canadian power line frequency.

By a process of elimination – involving setting up a CW signal generator and monitoring its signal over a variety of direct and indirect paths inside a building – the researchers were eventually able to implicate the arrays of lights that covered the ceilings.

Their first experiment involved placing a directional horn antenna 30cm from a fluorescent tube and using the horn to generate a signal varying between 0.5 and 10.0GHz. A receiver horn pointed at the light and used to detect reflected signals showed a very marked 120Hz modulation of the signal amplitude that peaked in intensity at a signal frequency of 2GHz. Just to prove that the effect had nothing to do with signals generated directly by the lamp itself, the Canadians checked it out with a passive receiver and also by the use of aluminium screens.

After further experiments simulating the sort of signal paths that might be employed by users of indoor communication equipment, the team concluded that the problem had nothing at all to do with faulty fluorescent fittings; these particular ones proved to have a very quiet RFI profile. The true source of the varying reflections turned out to be the excited gas inside the tubes.

In effect the gas acts as an electrical conductor and reflects radio signals in much the same way as the excited gas that comprises the aurora. But because the gas in a mains-driven fluorescent tube conducts in bursts at twice the frequency of the mains, it also reflects radio signals in bursts. Reflections from a fluorescent tube are thus strongly modulated at twice the mains frequency, ie 120Hz in Canada.

The researchers say that this effect is dependent on the size of the tube and the geometry of the fitting. They also say that, while the fading that results from the resulting multipath is not like normal slow fading, it does degrade the average signal-to-noise ratio and also superimposes a strong 120Hz modulation on any signal – especially around 2GHz – being transmitted within a building containing fluorescent lights.

In their latest paper, Melançon and Lebel suggest that if received signal amplitudes need to be kept within specified limits, AGC systems must be designed to compensate for fading at 120Hz. Better still might be to install fluorescent lights with RF ballasts... unless someone knows of any problems that occur when a radio signal acquires a spurious modulation at tens of kHz.

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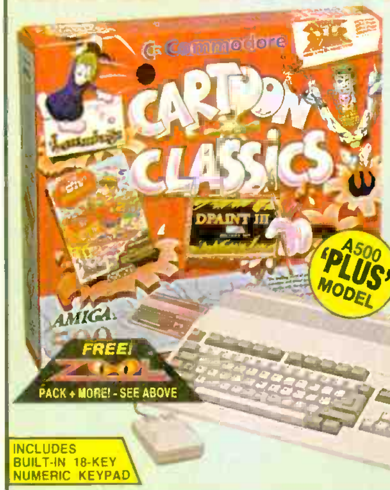

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SEE PANEL ABOVE

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CIRCLE NO. 109 ON REPLY CARD

Place in the sun for new battery materials?

A whole new technology for harvesting sunlight has been opened up by discovery of composite materials with valuable light properties. Mark Thompson and graduate student Lori Vermeulen of Princeton University have identified a series of materials that look to be much more efficient than photovoltaic cells at converting light into energy. They can also store energy until required and in that way imitate the way green plants intercept and store sunlight.

The materials are layers of zirconium phosphonate and viologen compounds, which react to light by acquiring electrical charges. Sunlight causes electrons to leave the "donor" and become part of the "acceptor" compound. The resulting charged compounds are then ready to react with a second set of substances to convert the energy into a usable form.

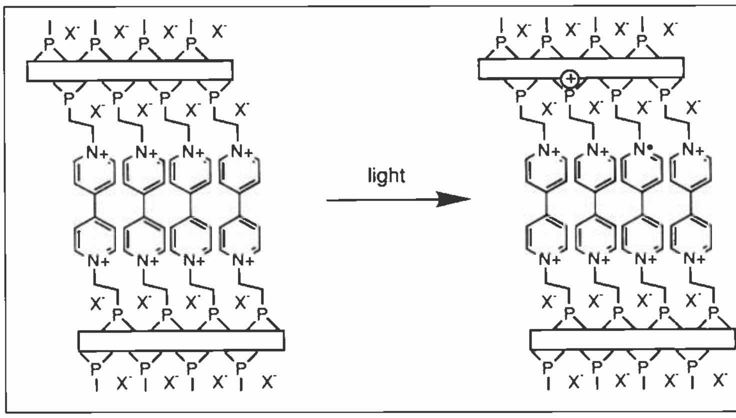
The critical part of the process is keeping the newly acquired charges separate for long enough to allow conversion into some form of extractable energy. Previously researchers have faced considerable difficulties in trying to maintain this "charge-separated" state because it normally reverses in the presence of air. Thompson and Vermeulen prevent the reversion with the tight meshwork structure of the zirconium and viologen compounds.

In classic style, the discovery was accidental.

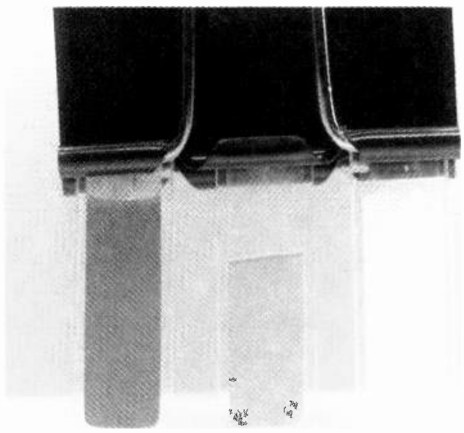
In July last year, Lori Vermeulen took a sample of the material on a slide from Thompson's lab and walked down the road to use the X-ray diffraction equipment in another building at Princeton. As she walked, the material, looking like a smear of wet white chalk-dust turned blue. She returned and repeated the walk with two new slides, one covered up and the other exposed to sunlight. The exposed material again turned blue.

The colour was immediately recognized as significant by Thompson: "Blue is not the normal run-of-the-mill colour of these compounds. When they decompose, they turn yellow, brown or red, but they don't turn blue". The colour indicated that some of the charge-separated electrons were not going back to their original state. In other words, energy was being stored.

Some electrons do eventually return, since the bright blue colour fades to pale blue after about five hours. But since publication of their *Nature* paper, the two scientists have made another version of the material which seems more able to capture and store sunlight. What is more, it can be made from cheap and readily-available starting materials.



Thompson and Vermeulen's layered viologen compound (left) and the result after reaction with UV light.



Before, between and after (right to left) exposure to UV. The layered viologen compound left in the dark, exposed to sunlight for 2h, and irradiated with a UV lamp for 2h.

Vermeulen has also made a version of the material that looks as if it is porous – meaning it should be possible to pump energy-harvesting molecules through the pores. She plans soon to test this strategy for extracting the stored energy. If the porous compounds are successful, they will certainly be much less expensive than semiconductor-based solar power systems.

Other plans are to use the materials in memory applications. If they can be made transparent to laser light (for write and read operations), the potential in high density non-volatile memories is considerable.

Diode turns blue at room temperature

A team at Sony Corporation Research Centre in Yokohama has developed a CW laser diode that produces a deep blue output (*Electronics Letters Vol 28 No 19*). So far, the prototype works at liquid nitrogen temperatures (-196°C). But there is no theoretical obstacle to producing a room-temperature version with wide application in data storage and retrieval systems – operating at the blue (short wavelength) end of the visible spectrum allows the laser to handle higher data rates.

The new Sony laser is the result of research into II-VI semiconductors, materials based on elements in groups II and VI of the periodic table. Doped II-VI semiconductors, because they have a wide band-gap, are capable of generating shorter wavelength radiation than the more usual III-V semiconductors such as gallium arsenide or its derivatives.

Research on wide gap II-VI semiconductor lasers is of quite recent origin. The first ZnCdSe/ZnSe pulsed laser reported last year (*Appl Phys Lett 1991, 59, 1272*) operated at room temperature and produced light in the blue/green part of the spectrum. Its success was largely the result of improved p-type doping techniques.

The latest blue laser, generating light at a wavelength of 447nm, also employs advanced doping techniques. But it makes use of different II-VI compounds created by molecular beam epitaxy. The chemistry in this case is ZnSe/ZnMgSSe, and when immersed in liquid nitrogen, the device begins to lase at a threshold current density of 225A/cm^2. The Sony team says that this result was achieved in spite of not having a good ohmic contact between the gold/palladium electrode and the p-type cap layer. If this problem can be overcome, then it should be possible to make a practical true-blue room-temperature CW laser diode.

Research Notes is written by John Wilson of the BBC World Service.

GPS

The global positioning satellite system will form the basis of the next public utility. Pin-pointing any location on earth to within a few centimetres, its applications will spread beyond simple navigation. For instance, low cost GPS equipment may be used to locate vehicles in a delivery fleet or a mass transit system. Philip Mattos, transputer expert and a pioneer in harnessing low cost microelectronics to GPS reception and processing, begins a series on the design aspects of GPS electronics.

A complete GPS receiver with map display position output. Everything apart from the front-end converter is engineered in software running on an Inmos transputer. The system, which provides both PAL and NTSC composite video, will provide the main design example used in this series on GPS.

The Navstar Global Positioning System, now known as GPS, dates back to 1973, following the US Navy Transit satellite system, operational since 1964, the *Timation* high tech research programme, and the US Air Force 621B programme. The first GPS signals from space came from the Navigation Test Satellite, in June 1977.

The initial constellation of GPS satellites, intended to prove the GPS concept, were launched from 1978 to 1985, with 2-D navigation first possible in October 78, and 3-D in December 78, both only for a few hours a day. These were launched by rocket from Vandenberg Air Force Base, California.

The Block II operational GPS satellites were launched from 1988 onwards, initially on the space shuttle, but following the Challenger disaster there was a considerable delay, and the launches were rescheduled on McDonnell-Douglas Delta Rockets. As of July 1992, there are four Block I satellites still functioning, numbers 3, 11, 12 and 13, following the death of number 9 in early 1991 due to a motion wheel bearing failure, and number 6 in spring 1992 due to a power system failure. There are 14 Block II satellites available (2, 14, 15, 16, 17, 18, 19, 20, 21, 23, 24, 25, 26, 28).

Current satellites in service provide 2-D coverage 24 hours a day , and about 21 hours of 3-D coverage, depending on latitude and antenna used for marine/air use. Land use, in town or in rough terrain, is much less available, as the visible horizon, assumed as 5° at sea, is more like 25°, but 2-D coverage is still available almost 24 hours a day.

There have been two other major delays since the Challenger disaster. The first was caused by a breakdown in the automatic solar-panel controls on number 24, the second by lubrication failures on the momentum wheels both in space and on ground tests. On both occasions delays were inserted to ensure the future reliability of the system... but the lubrication failures were actually caused by earlier delays: the time the satellites had been waiting on the ground to be launched. The system is expected to be declared operational in 1995, and the US government has guaranteed its availability without direct user fees for ten years from that point.

Why GPS?

A new navigation system was needed for many reasons. GPS has many features that make it desirable over older systems. It is global including space in orbits much below the GPS satellites themselves; it offers continuous coverage, in contrast to the earlier *transit* system which gave a fix every few hours; it is unjammable by an enemy in time of war, and finally, it offers height as well as latitude and longitude.

Both Loran and Decca suffer from limited coverage, especially in developing countries and the Southern Hemisphere. In fact Decca coverage is largely limited to North West Europe, South Africa, the Gulf and Australia. Neither can give a user's height, and their accuracy can be as bad as 500 metres, although repeatability is much better than that.

They are also not suitable for high dynamics vehicles such as fighter aircraft, nor are they effective in towns, due to excessive interference from mains-powered equipment generating low frequency interference.

Explaining the GPS requires a background knowledge of simpler terrestrial systems and the *Transit* satellite system. The features detailed are those where parallels can be made from the GPS system.

Loran and Decca systems work by transmitting signals from several ground stations, the hyperbolic systems, so called because the position lines on a chart take the form of hyperbola. Until the advent of the microprocessor, the position was found by looking up overprinted position lines on a chart.

Loran

The mobile calculates the propagation delay from each of the transmitters, and thus the distance, and from this calculates its position. This may be done from just two transmitters.

It sounds simple, but is not the whole story. Firstly, as the exact moment transmission is not known on the mobile, an absolute propagation time cannot be found directly. This is solved by locking the transmitters together, so that their relative relationship is known. The time differences (TDs) can then be measured at the mobile (**Fig.1**). Calculating a position from the TDs requires three signals (**Fig. 2**). However if the user crosses the line joining two transmitters, outside the transmitters, known as the baseline extension, the accuracy deteriorates very badly, being insoluble on the line. To cover for this problem, the minimum effective chain of transmitters is four.

The next problem is how to prevent multiple transmitters from interfering with each other, an aspect handled differently in the two systems. Loran uses a single frequency, and each transmitter sends a group of pulses. (**Fig. 3**). As a pulse group takes less than 10ms and is repeated never faster than about 50ms, several transmitters can operate in the same area with carefully allocated time separations.

Different chains of transmitters can be identified by the repetition rate of the groups (Group Repetition Interval, GRI). If collisions occur in the time domain, because of the different GRIs, the next cycle will not collide. The eight pulses of a group have a pattern of

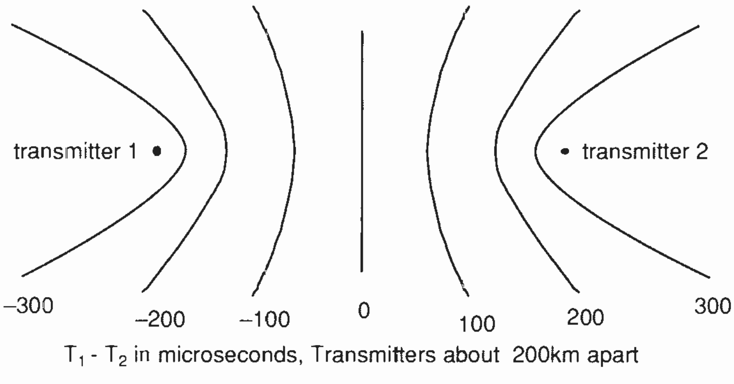


Fig .1. Hyperbolic systems before the microprocessor used an overprinted chart to lookup the lines of position, having read the relative delay from the receiver. The drawing shows the overlay for a pair of transmitters, after subtracting the delays in transmitter start time that are inserted to ensure the signals due not overlap each other.

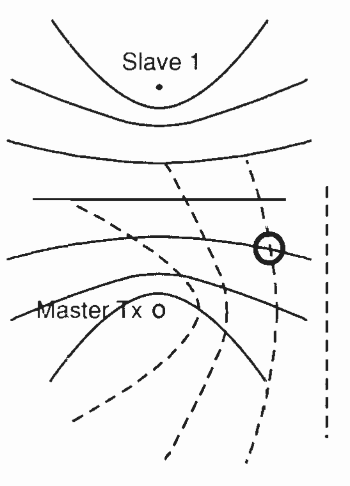


Fig. 2 Hyperbolic 2-D positioning with two sets of overlays. The receiver is positioned where the appropriate delay contours intersect.

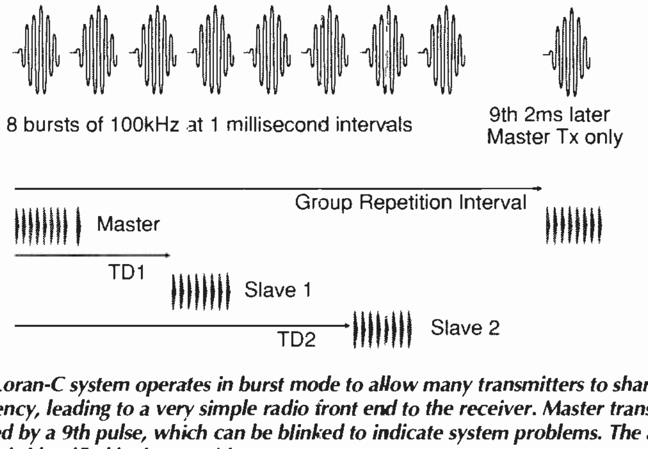


Fig. 3. The Loran-C system operates in burst mode to allow many transmitters to share the same frequency, leading to a very simple radio front end to the receiver. Master transmitters are identified by a 9th pulse, which can be blinked to indicate system problems. The actual chain in use is identified by its repetition rate.

phase inversions to minimise the effect of other (CW) interfering signals that may distort the phase.

As Loran means Long Range Navigation, the signal can be very weak at the extremities of range, and then problems arise with interference between ground wave and sky wave signals.

This problem is handled by specifying a particular carrier wave zero crossing as the timing point, and making it early in the pulse so that the sky wave has not yet arrived. The particular carrier wave is identified by shaping the amplitude envelope of the transmitted waveform. The receiver then ratios the peak-amplitudes on receive to identify a particular cycle.

Decca

Decca, on the other hand, operates an almost continuous transmission from each transmitter, and separates/identifies them by carrier frequency. In each chain there is a transmitter at multiples of 5, 6, 8 and 9 of a reference frequency around 14 kHz. Thus carriers are at 70, 84, 112, 126kHz.

Decca is a short range system, so normally adjacent chains do not interfere greatly, but in order to cover abnormal propagation, the 14kHz reference is marginally different on each chain, and common or almost common frequencies are given large geographical separations.

Originally Decca was a continuous wave system, but the reason now for the word "almost" is that interruptions were introduced to allow the user to identify a particular cycle of the carrier wave. Before this, Decca had an ambiguity of a multiple of four miles, the lane problem. In addition to the interruptions, the

SPREADING THE SPECTRUM

Spread spectrum is as the name implies. Rather than simply applying data to a carrier as in AM, SSB, or FM, where the modulation sidebands are scarcely wider than the data they contain and concentrated in a small group near the carrier frequency, the energy of the carrier is deliberately spread out over a wide band, so much so that it disappears below the thermal and atmospheric noise. Essentially, there is now no detectable signal.

This could be achieved by band-limiting, modulating with low bit rate data, and up-mixing the signal from a noise diode. However, this would be irrecoverable as the receiver would not have access to the same noise source to reverse the operation. A truly random noise source would result in a flat spectrum.

In a practical system the spreading operation is done using a pseudo-random noise source, a pair of fed-back shift registers that each generate a maximal length sequence. This operation can be repeated at the receiver. The use of two sequences, a Gold code, results in low cross-correlation between the satellites, and low auto-correlation at erroneous offsets with itself, and thus is almost as good as the truly random noise diode.

This pseudo-random sequence results in the well known Sync function, Sin(x/x where the spectrum is as shown in Fig. 5 of the main text; the first nulls are spaced away from the carrier by the clock rate of the generating shift-registers.

A more detailed look at the spectrum would show that it is a comb of frequencies, each spaced 1kHz apart. The 1kHz spacing arises through the repetition time of the entire sequence, which is one millisecond. In order to recover the signal, this comb must be gathered together into a single carrier again, which is done in the receiver by re-applying the noise sequence in a digital mixer.

A simple way to understand spread spectrum modulation in the context of GPS is to use a worked example.

Consider a code 11010010. It has eight "chips", and appears random. If we wish to transmit some data, we could transmit the whole code for a 1, and then the same code inverted for a zero. Thus:

11010010 00101101

Note that if we exclusive-OR this pattern with a locally generated copy of the code, we get:

00000000 11111111

Thus if, for maximum noise performance, we pass the output through a filter with the same bandwidth as the data rate, we recover our 1,0, despite the inversion. In this case, such a filter would give amplitudes of 0 and 8 respectively for the two data bits. Note that 8 is the power gain due to correlation; the transmitted signal had peak amplitude of 1. The amplitude of our recovered signal here is as transmitted, as there is no loss.

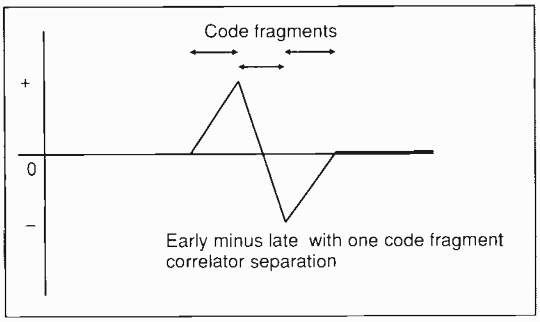
In real life, there is a loss due to limited bandwidth, limited sampling rates, thermal noise, and imperfect synchronisation between received and locally-generated codes.

Note that if the code is mis-aligned by more than one chip, no signal is recovered. Using 0,1 as the input levels, the result averages to 4,4, as would random noise. The shape of the amplitude/synchronisation response is critical to accurate tracking. It is the accuracy of the tracking in the time domain that controls the positional accuracy of the receiver.

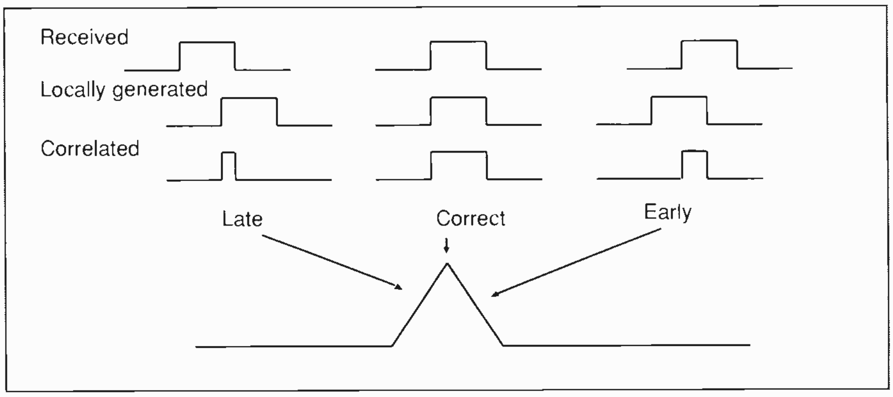
Correlating a square wave against a square wave yields a triangular wave:

The best results are given by an early/late tracker, using the late signal subtracted from the early to give an error signal to control the tracker. The response is then dependent on the sampling rate, and the radio receiver bandwidth.

A receiver exists using this technology that can track the satellite signal to a resolution of 6cm . This means it can immediately resolve carrier ambiguities which crop up every 20cm



Error signal that advances or retards tracker. Differencing the signals from two correlators that have a small time offset yields a error signal that can control a tracker to keep the receiver in lock with the transmitter.



Correlation response of a squared pulse. Recovering a spread-spectrum signal relies on the fact that it can be de-spread when multiplied by the same spreading code again. More than one chip of the code in timing error means no signal, and a single correlator does not know which way to adjust to find the peak.

without post processing or p-code.

Note that this simplified example has ignored the carrier frequency itself. Thus the receiver must have two tracking loops. One as in the example, achieves timing measurement and correlation gain by removing the spread-spectrum code, leaving a narrow-band carrier transmitters each transmit all the 4 frequencies together for a short time. By mixing these in the receiver, the 14kHz reference can be generated, giving a super-lane width measured in tens-of-miles. Thus the three resolutions, interruptions, 14kHz phase, and carrier phase interlock to resolve all the ambiguities.

The Omega system is another quasi-continuous wave system, using frequencies around 10kHz that propagate around the earth. This gives global coverage, but accuracy only to the miles level.

Transit

The Transit system uses only a single transmitter, based in space. Using it twice, moving on a known orbit, is equivalent to two transmitters. This means fixes are not immediate, and the user's motion between observations must be accurately known.

Transit does not use ranging, but rather Doppler shift caused by the satellite's motion. Measuring the frequency of a single received signal gives a result distorted by satellite doppler and user reference error. By using two transmission frequencies, the reference error can be removed and a true doppler shift found. Knowing the velocity of the satellite, this doppler frequency gives a cone of position around the line of motion of the satellite, and the intersection of the cone with the earths surface gives a line of position. Repeating the operation a few hours later, when the satellite's line of motion has changed significantly due to the curvature of its orbit, gives a second intersecting line of position. This produces an actual position for a stationary user, or for a mobile user after compensation for his own motion in that time.(**Fig. 4**)

carrying BPSK data. The second removes the carrier using a phase-locked loop, with the data as its output.

Who uses it, and why

Until recently spread spectrum was the unique preserve of the military, who liked its covert nature, as the signal cannot be detected by conventional means. Radio amateurs were prevented from researching it by the terms of their licence. In the last few years, with the de-licensing of low-power transmitters in the USA, and proposals for new cellular phone and satellite-phone applications, it has become much more popular. I have even worked on a remote signalling application using spread-spectrum down power cables. Spread spectrum allows two new dimensions in the fight for spectrum efficiency. While it uses a wide band in the frequency domain, many users can occupy the same band. Within that band, their signals can be separated by the code they use, by the centre frequency, and even on the same code, can be separated in the time domain. This latter feature is made possible by the fact that the spread spectrum signal has within it accurate time signals, the code epochs.

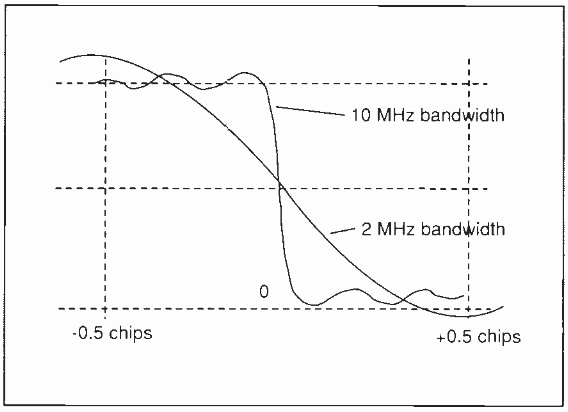
In the cellular-phone area, the signal reaches the vehicle after bouncing off several buildings. Thus several copies of the signal reach the receiver. A conventional receiver must use the strongest, and the others count as interference, ie are detrimental. A spread-spectrum receiver can track several of the signals, re-time them and add the energy in each.

As the power needed for spread-spectrum is so much lower than traditional modulation methods, it is very suitable for portable transmitters. This is a trade-off between the number of users and their power output.

An additional set of channels can even be gained under existing narrowband signals. The spread-spectrum signal is too low in energy density to affect the narrow band receiver, and the act of de-spreading the signal in the receiver actually spreads the energy of the narrow band transmission out, so that both systems can co-exist on the same frequencies, subject to the near-far problem described below.

As receiver frequencies get higher, narrowband systems either need filters with tighter percentage bandwidths, or more stages of down conversion. Spread-spectrum allows very simple analogue receiver design followed by a simple A/D converter. All the narrow band work can then be done in the digital section, be it asic circuitry or as a software engine in a fast processor.

Error signal vs. receiver bandwidth. The shape of the error signal is dependent on the separation of the two correlators and the bandwidth of the receiver. Initial acquisition and tracking have different requirements, and there is no benefit in using a wide bandwidth receiver if the correlator spacing is wide. Acquisition uses a wide separation for a good pull-in range, while tracking uses a narrow separation for maximum gain inside the loop, and hence minimum tracking noise.

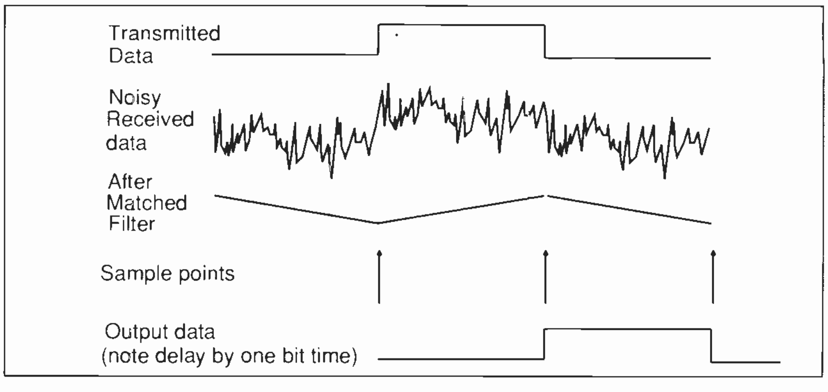


Spreading problems

There is one drawback with general use of spread-spectrum, and that is known as the near-far problem. It doesn't affect GPS, as all the transmitters are in space, and thus "far", except when local pseudo-satellites, or pseudolites, are used, as has been proposed for precision landing at airports. For general use however, when a receiver is near to an alien transmitter, that transmitter's signal will not be buried below the thermal noise, but may saturate the receiver and prevent its reception of the desired signal. This is easily handled in satellite communications by allocating widely separate bands to the up and down links as is done for narrowband links.

In terrestrial systems this is less achievable as, near the base station, the mobile receiver would be drowned, and would also drown the base station. Current systems such as GSM already have dynamic control of transmitter power. A more sophisticated version of this would solve the problem where frequency bands can be allocated to a single network, as far as the base station is concerned. However the car parked alongside may still be drowned, as the base station must transmit high power to reach a remote mobile operating simultaneously, in the same band, on a different code.

Data extraction. Two stages of bandwidth reduction give considerable signal to noise ratio improvement. The one millisecond filter in the correlator collects 1000 code chips together, a 30dB gain for a 1kHz data bandwidth. The data extractor then filters over a matched 20ms, synchronised to the data edges, reducing the bandwidth to 50Hz, a further 13dB of gain.



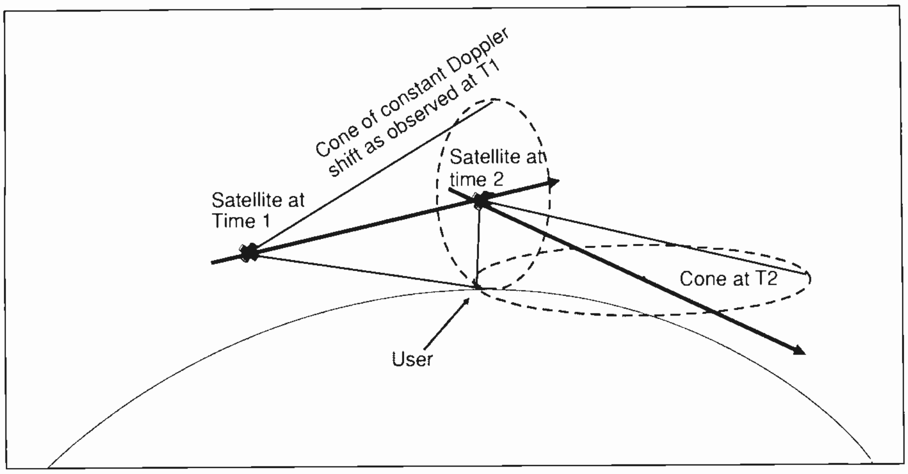


Fig. 4. The Transit satellite system operates by measuring the Doppler shift caused by the satellite's motion. As multiple satellites are not usually available, the same one can be used twice with a time separation, but the vessel's course and speed meanwhile must be accurately known. Fixes are infrequent, as there are one to two hours between each low-orbit satellite pass

GPS uses the time-delay ranging of the hyperbolic systems for positioning, plus the doppler (or integrated doppler) measurements to smooth the tracking of the time delay, and also to derive user velocity. Its time delay is measured from the code tracker of the spread spectrum demodulator (see box). The spectrum and modulation are shown in **Fig. 5**.

The GPS system, structure and signals.

The GPS system has a network of transmitters just like the terrestrial systems, but on satellites in space. Just as the terrestrial systems overcame their problems like baseline extension and transmitter separation and identification by careful design, so too does GPS.

The GPS equivalent of the baseline extension problem is the GDOP, geometric dilution of precision. When the currently visible satellites are badly positioned, the accuracy deteriorates. When insufficient satellites are visible, there is no service. To best cover the earth with best accuracy for the longest period of each day, considerable effort was put in to the orbit configuration, or constellation.

The satellites orbit at a height of 20,200km, twice per sidereal day (23 hours and 56 minutes). This means that they cover the same ground track each day, four minutes earlier each day. The early plans called for three orbit planes of six satellites plus three spares, 60° inclination to the horizon. However when all the satellites in use are in a single plane, and the user passes through that plane, the accuracy is badly degraded. This happens far less if the satellites orbit in more separate planes, so the current plan is six planes of three satellites, with a spare in alternate planes. At the same time, the inclination was reduced from 60 to 55°.

The satellites all transmit continuously on the same frequency so, like the Decca system, a method of separation and identification is required. As the carrier frequency is 1575 MHz, the ambiguity would occur every 20cm, so a solution is required here too.

A single method fixes all three problems. The transmission uses spread spectrum modulation. This means that the carrier wave is phase inverted by a pseudo-random code. This code runs at a 1.023 MHz rate, and spreads the carrier energy over a 2MHz bandwidth, thus reducing the power density below the front end noise of the receiver. To recover the signal, it is multiplied by a replica of the code used in the satellite.

The code has a length of 1023 bits and thus repeats every millisecond. This results in a range ambiguity of 300km, acceptable in most circumstances, and may be resolved further from the transmitted data bits (6000 km/bit), with total resolution from the data-content.

By giving each satellite its own code, only the signal from the selected satellite is gathered into a narrow bandwidth and detected. Thus many satellites can coexist without interference, and may be individually identified.

The actual power level available to the receiver is a minimum of −160dBW, or −130dBm, to the civilian user with a 0dBi gain antenna. For comparison, the thermal noise in a receiver of 1MHz bandwidth is kTB, where k is Boltzmans constant, T the absolute temperature, B the bandwidth. This yields −114dBm for the thermal noise plus say 1dB for receiver noise factor. Thus the signal is some 17dB below the noise.

The correlation process (see box) allows a gain of 30dB, bringing the signal to noise ratio up to +13dB, in a bandwidth of 1kHz. It is at about this level that the receiver must first lock onto the signal. It can then narrow the bandwidth further in a carrier loop to 50Hz to extract the data, representing another 13dB. At 26dB signal-to-noise ratio, error free reception of the system data can be achieved without difficulty. The limiting feature is not in tracking the signal, but in acquiring initial lock, both in the time and frequency domain.

Added sophistication

The single satellite signal is extended in three ways in order to add facilities to the system or improve its accuracy. Firstly, data is added to the system by a second level of binary phase shift keying (BPSK) modulation at a 50 baud rate. If not provided over the satellite itself, a separate terrestrial transmission would be needed in order to inform the user of the satellites' own position, and transmission times. This is feasible, and is used for surveying work with post processing, but would not be feasible mid-ocean in real time.

Secondly, each satellite also transmits a second, much faster code and, thirdly, it also transmits on a second frequency.

The second code, known as the P, or precise code, is reserved for the military. Its original purpose was to give a much better accuracy than the commercial system since its 100ns code chips should produce better receiver tracking accuracy than the commercial 1μs code bits.

This design feature has been overtaken by receiver technology in the intervening 15 years. Receivers can now track the carrier wave, which has a 600ps period. In any case, it is not the receiver tracking error that dominates system error, but ionospheric distortion and deliberate degradation by the US DoD known as Selective Availability (SA).

However the p-code signal has a further function. It can be switched to another code in times of war. This is known as anti-spoofing mode, and it prevents the enemy from generating spoof signals that would deceive GPS receivers into giving erroneous positions.

Because the p-code is chipping ten times faster, it also has ten times wider bandwidth. This makes it even harder to jam, and, if receivers could sample fast enough, would allow greater correlation gain over the same integration period.

The reason for a second frequency, L2, is that the inevitable ionospheric delay to the signals is mathematically related to the frequency. Thus by timing two signals known to have been transmitted from the same satellite at the same time, the receiver can calculate the delay incurred in the ionosphere, and compensate.

The second frequency does not carry the clear access (C/A) code, only the p-code, so is not in principle available to commercial users. Only survey sets need this accuracy, so the current trend is to provide two modes: one that uses the p-code, and another that uses a squaring technique rather than correlating with a locally generated satellite code. The squaring method is only used when the anti-spoofing mode on the satellite is enabled, as it incurs considerable (about 6dB) signal-to-noise ratio loss.

Extra-terrestrial concerns

There are many receiver tasks which do not arise with the hyperbolic systems. Some are new, caused by the motion of the satellites versus the "fixed" terrestrial transmitters. Others always existed but, because of the improved accuracy of GPS, are now relevant. Previously they could be ignored.

On the benefits side, Loran and Decca were designed before microcomputers existed. All GPS receivers have a powerful microprocessor, often more than one.

The motion of the satellites is handled by transmitting from the satellites themselves the coefficients of equations describing their orbits. The receiver can then calculate the satellite position precisely at any given time. Here hangs a problem: what time? We do not want the position of the satellite when we received the signal; rather when it was transmitted. Without knowing the satellite's position, we cannot work out the propagation time.

This circular argument is difficult for man, simple for computer, as the computer sees this not as a circular argument but a recursive one: it simply repeats the calculation, getting more and more accurate, until the error is insignificant. With the satellite travelling around 5km/s, the initial estimate may be 350m out.

Having calculated the satellite's position, we ask "relative to what?" GPS uses earth-centred earth-fixed (ECEF) coordinates, in order to tie in cleanly to latitude-longitude-altitude. But if the calculations were all done in this mode, the signals would not be travelling in straight line, as during the 70ms or so that the signal is travelling from the satellite to the user, the ECEF coordinate frame has rotated. This must be accommodated in calculating the satellite position. The error is not insignificant: in 70ms the user on the surface of the earth moves some forty metres in an easterly direction simply due to earth rotation. The apparent satellite position has moved about four times that in a westerly direction, due to the greater radius at the satellite.

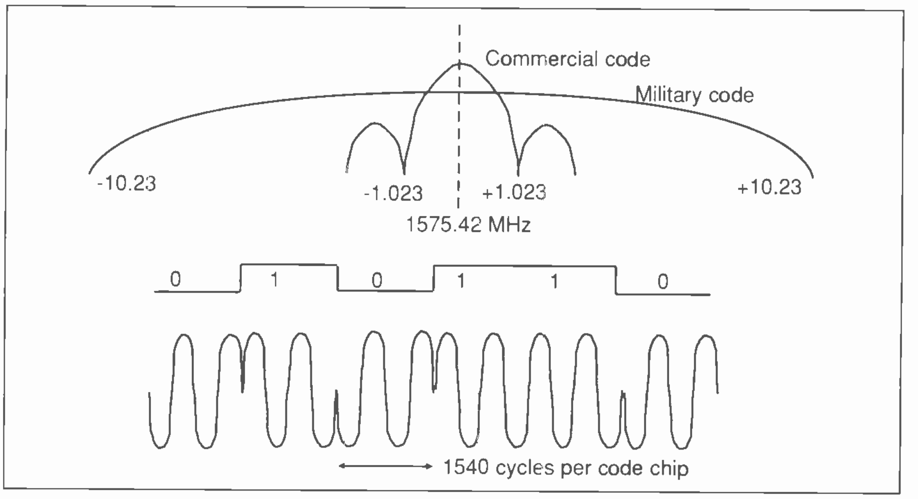


Fig. 5. GPS combines the benefits of terrestrial systems with continuous availability, satellite systems for global coverage, at the cost of many satellites and a complicated receiver to decode a complex modulation scheme. Spread spectrum allows all 24 satellites to transmit continuously on the same frequency.

The biggest correction made by the user is for ionospheric distortion. This did occur on advanced Loran sets, where the sky wave was used with correction tables (Additional secondary factors, ASF), but with GPS it accounts for around 30m of the error budget, so is very important.

Even relativity is considered in the system design. The satellite system clocks are run a little slow in order to allow for the apparent increase in frequency as the signal approaches the earth caused by the interaction of the signal and the gravity gradient. The receiver also performs a mathematical calculation provided in the GPS spec to correct for the varying speed of light due to gravity. ■

Next month: *Radio architecture and data extraction*

Applying the heavy boot to eprom bugs

Trace and emulation, optional eprom programmer and wide device range: if you need it all, Martin Cummings shows how Seeker could be what you are missing.

Trace Technology describes *Seeker* as a universal emulation system for 8-bit microprocessors. In fact it is a curious combination of eprom emulator and logic analyser, currently supporting over 20 processors.

Eprom emulation allows replacement of the target board's eprom with *Seeker*'s memory containing the program. Once in, modification is much easier than re-burning an eprom. In addition, when the program is running, *Seeker* monitors 40 bits of information – including data and address buses – and will produce a trace of this information leading up to or surrounding an event.

Full control over the program and processor control signals means it is also possible to dump or modify memory, i/o locations or to go inside the processor and have access to the contents of all internal registers. The result is full emulation, even where the target has a soldered in processor chip. All that is needed is a socketed eprom and access to a few other signals somewhere on the board.

Help and manuals

On-screen help is provided. Often a message explains what to do next and the pull down help menu is always available – giving brief details about most commands and functions and almost as helpful as the manual.

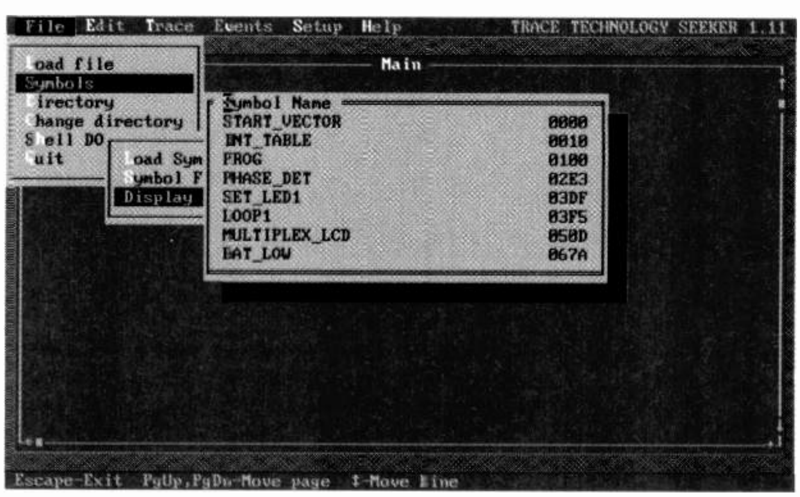
The manual itself is about 40 double-sided A5 ring bound pages, combin ng text with p enty ot screen dumps and associated explanations. Although a little -erse in places it covers all the commands and, in general, gives sufficient information for an engineer to ncrease speed quickly.

Intelligent hardware

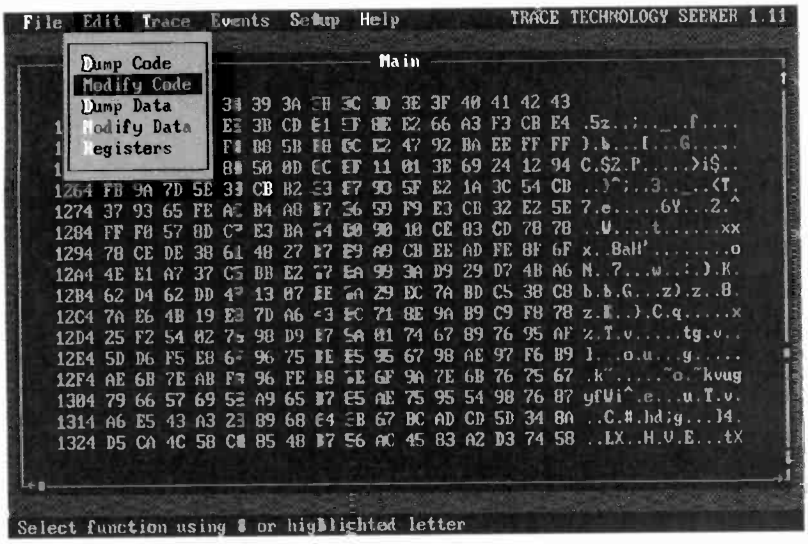
Seeker is a box of circuitry – mainly memory and logic although its *Z8* processor makes it intelligent in its own right. Main connection to the target board is a 28-pin header on the end of about 450mm of flat cable that replaces the eprom. The header is supplied plugged into a sacrificial socket so that when the inevitable happens and pins break off, only the socket needs to be replaced. Of a further 26 connections on another flat cable, some interface to the processor control signals, others to any address bits that do not exist at the eprom socket and up to eight external bits can monitor, for example, i/o signals.

The package comes well equipped with miniature probes for each individual signal, so connecting them, though laborious, is made as painless as possible. Trace will also supply adaptors configured for particular microprocessors with all the connections taken to a header that plugs into the processor socket if one is fitted. The adaptors are only small PCBs to assist connection, and have no active circuitry and so are relatively cheap.

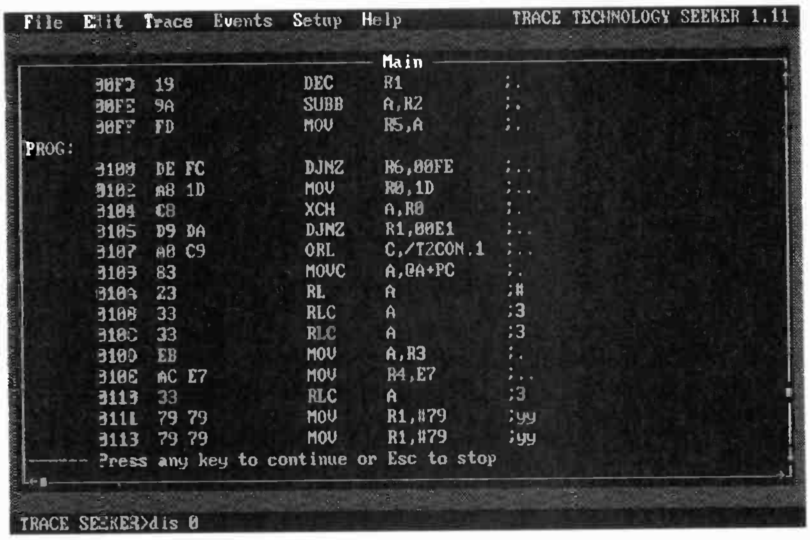
An IBM-compatible acts as a file server and user interface, and connects to it via a serial port – almost any PC with a serial port will suffice. A mains adaptor is supplied to provide the 9V needed by the unit. Unfortunately a serial cable to the computer is not supplied, though the manual gives clear instructions for the connections to be made for either 25 or 9 pin ports and only a three wire connection is needed. In general, connections are straightforward and the manual



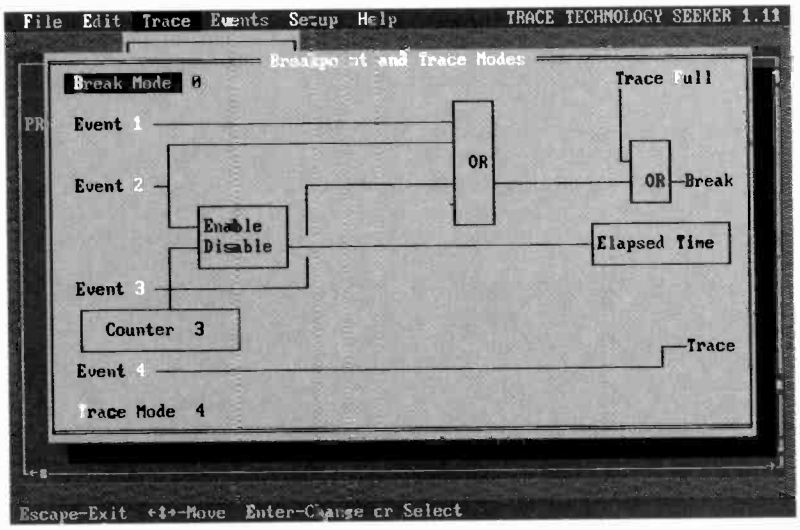
Taking a look at the address symbols loaded into Seeker.



Viewing and modifying code.



Code disassembled together with symbols associated with addresses.



A main strength of Seeker is its ability to configure the program break point and what to trace during the run.

gives plenty of information so it should be possible to have the unit running first time.

The unit itself is slightly smaller than a shoe box, with power and serial inputs on one end and flat cables coming out the other; internal circuitry and packaging are manufactured to a high standard. Up to three internal expansion cards can be fitted, expanding memory and allowing several eproms to be emulated. In place of one of the expansion boards, in addition to the emulation and trace circuitry, an eprom programmer option can be fitted inside the box with a zero insertion force socket on the top. A low profile box is also available with one spare slot for memory or programmer, although it has the same footprint as the standard unit.

Software options

Software, supplied on both formats of disk, must be loaded onto the host machine's hard disk, though installation is simple and *Seeker* takes a modest 650kbytes of disk space. The READ.ME file provides the usual list of enhancements and lists numerous software revisions, and while clearly there have been bugs, it is also evident that these have quickly been resolved and features have been added along the way.

Several software options can be selected on start up, including the ability to select COM1 or 2 as the interface to *Seeker* and the choice of not shadowing the pull down windows – sometimes a distracting feature on LCD screens.

Once running, the screen presents a large window ready for text display, together with six menu items along the top line that can be selected either by mouse or keyboard. In fact more commands are available than are presented on the pull down menus, causing confusion to those of us that only read the manual as a last resort. Some commands are typed in at a command line that appears at the bottom of the screen when the first letter is typed. Once learned, the commands can be abbreviated to a minimum of three letters.

Running *Seeker*

Before starting, a few basics must be configured – such as which microprocessor is in the target board and what sort of eprom is to be emulated. But with no more than this the program file can be loaded into Seeker and the target board started running. Most standard file formats are accepted and the transfer of data down the serial link into the unit is almost instantaneous – the software configures the serial link to operate at 57.6Kbaud.

Target program execution can be halted, continued, single stepped or instructed to run for up to 20 instructions. At each step the processor register contents are displayed and there is access to view and modify memory, i/o space or registers.

Unfortunately the user interface, while adequate for the job, is not the smoothest and easiest to drive – a fact that becomes apparent after a little time has been spent keying in commands. Everything can be done if you know exactly what to type and are clear on the syntax. But stray beyond this and both the user and *Seeker* can easily become confused.

For example when dumping memory to the screen, a scroll bar on the right hand side of the screen could reasonably be expected to scroll through memory, but in fact it scrolls back through previous commands and screens that have been displayed. OK if you are expecting it: confusing if you are not.

Like most programs now, macros can be created to store and replay favourite commands at the press of a function key. The facility is easy to take for granted, but bug hunting is often mechanical and laborious and any aid to automation is to be applauded.

Configurable breaks and trace

Probably the main strength of *Seeker* is its ability to configure the program break point and what to trace during the run.

The basis of this is four configurable events, three 16-bit counters and some logic that connects them to the break point and trace memory enable. The configuration and logic is presented graphically on screen (see picture) and as such is very easy to understand and use.

Events are defined by the pattern presented on the 40-bit trace inputs – that means any combination of address, data, control and external bits. Unique values can be defined or wildcards used for bits or nibbles. In addition, And/Or logical operators can be used and ranges of numbers included to create a complex definition of the event or events to be detected. For example an event could be as simple as "event 1 if address=10CD" or more complex such as "event 1 if address=10CD & data=00-0A & control=mw".

Several arrangements of the logic connecting the four events to the break point and trace buffer are possible. The logic is not fully configurable by the user who can merely select one of the four configurations for events to cause a break and one of the six definitions of trace enable. But the predefined combinations are fairly complex in their own right, providing all sorts of possibilities and it is only the most extreme of circumstances that will not be satisfied by one of them. An elapsed time counter can be gated on and off by two of the events.

One example of a configuration would be a break being forced if either event one or four occurs after event two but before event three. The elapsed time counter would accumulate time between event two and three, and the trace buffers would store all cycles. At any time, on demand, a status window can be displayed giving the current counter values, elapsed time and whether the target is running or not.

The trace buffer is 2048 by 40 bits. Each cycle gives values for data, address, the external signals and the type of cycle (read/write/instruction fetch etc.) together with an identity number for the cycle within the trace buffer. Numbers, except the cycle number, are given in hex and although the display is slightly configurable it seems a shame that values in binary cannot be displayed.

Ploughing through the trace buffer can be mind numbing. Encouragingly, the buffer can be searched for an event (defined as above). Supplied as part of the software is a disassembler for each supported processor, so the trace buffer can be converted from hex numbers back into assembler. Where an assembler or compiler provides a symbol table, it can be loaded, and symbols automatically appear in the disassembled code as labels against the appropriate addresses. Several symbol file formats are supported – desperate users can even type in their own. Symbols come in useful elsewhere because they can be used in place of address values when constructing event definitions.

Printing

Tucked away in the latter pages of the manual is a rather curious command that captures the screen to a text file. It actually deals with a little more than the screen, so that if for example you have just scrolled through the trace buffer, then the file will capture everything viewed, not just the current screen. The file is given a title header with a date and time stamp which helps to identify the most recent if several dumps have been made as the debugging progresses.

The manual never explains quite what should be done with this file so I used my initiative and copied it to the printer: it would seem that this is the only way to get a print.

But it does mean that the trace file can be viewed and edited before printing although I am not convinced of the need for this. Unusually, there is no direct print facility.

Weighing up the benefits

The overall impression of *Seeker* is of a device with some powerful features that could be invaluable in tracking down

SYSTEM DETAILS

Processors supported:

Z80	8031	6800	68HC11	63C3	Z8671
Z8400	80C31	6802	68HC811	63C9	Z8681
Z84C00	8051	6803		63C9E	Z8681
Z84C01	80C51	6805E		63C3R	Z86C91
Z84C02	8032	6809		63C3X	Z8800
Z84C50	80C32	6809E		63C3Y	Z8801
Z84C011	8052				Z8802
Z84C013	80C52				
Z84C015	80C154				
	80C51FA				
	80C552				
	85C154				

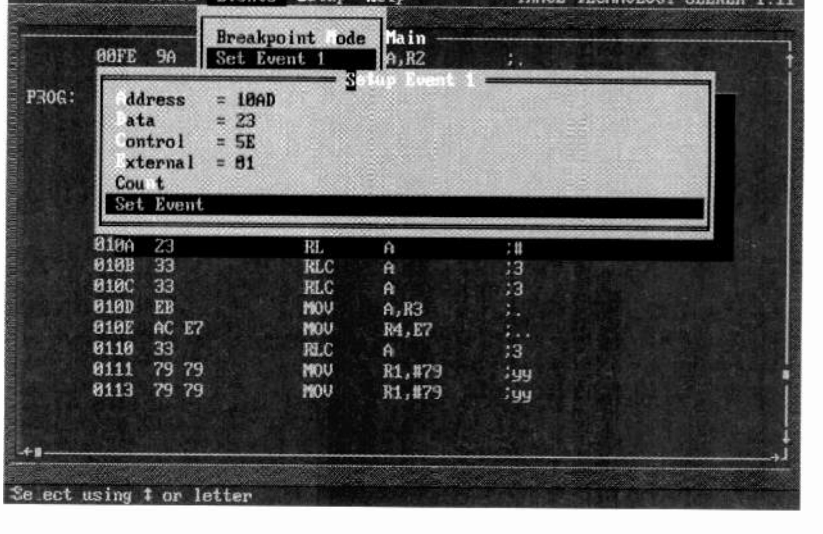
Target board requirements:
Target processor must be supported
One or more eprom sockets
Access to control signals
Minimum bus cycle not less than 280ns

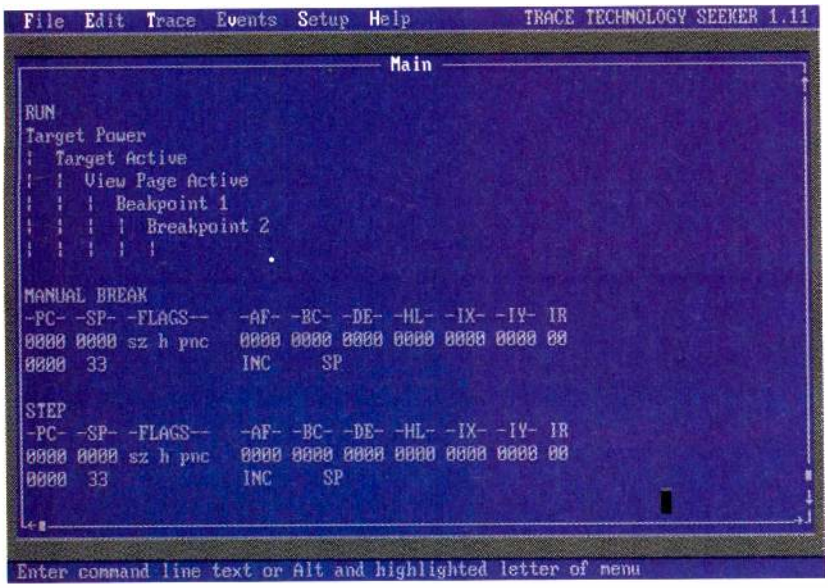
Target code formats supported:
Binary
Intel hexExtended Intel hex
Motorola S19
Motorola S28
Motorola S37
Tektronix hex
Extended Tektronix hex

Eproms supported:
2516 2716 2532 2564
2764 27128 27256 27512

Symbol file formats supported:
IAR SYMBOLIC
AVOCET SYM
TRACE
HITECH MAP
HITECH SYM
2500AD MAP
ADDRESS SYMBOL
SYMBOL ADDRESS
INTEL M51

Configuring an event.





Seeker can single-step, showing the processor status at each step.

the more elusive bugs infesting real-time microcontrollers. The product is wrapped up in a competent but unglamorous package together with software and a user interface that has clearly been written by engineers, for engineers – without the scrutiny of a marketing man. Perhaps we have all been spoilt by seductive windows, icons and user-machine interfaces that have taken many man years to develop.

What marks the package out from the crowd is the number of different microprocessor families it can handle at its price. While this is undoubtedly an advantage I wonder in practice how many companies and engineers need to chop and change devices that much. Most organisations stick with one device, the investment in learning and software a significant disincentive to quick change. Maybe *Seeker* goes a little way to reducing that disincentive.

If the trace facilities appeal, then you will probably be comparing *Seeker* with a logic analyser. If it is eprom emulation that is needed then this can be achieved at much lower cost, and to be fair there are other Trace Technology products that fill that niche.

However for users who need both, together with the option of an eprom programmer and the ability to deal with a wide variety of eight bit devices, then *Seeker* is worth a second look. ■

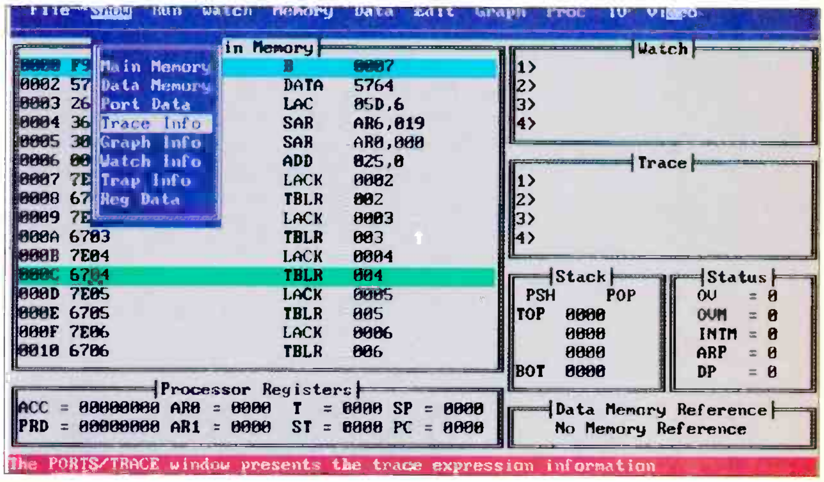
SUPPLIER DETAILS
Trace Technology, Unit 4, Shuttleworth Road, Elms Industrial Estate, Bedford MK41 0EP, UK.Tel: 0234 266455
£1950 + VAT

Developing the TMS320C10 for £50?

Signal Research's low cost and easy-to-use DSP development package is a must for any designer working with the first generation of TI DSP devices says Alan Brown.

Cheapness and simple architecture have turned the *TMS320C10*, and its eprom version from Texas Instruments, into a hugely popular digital signal processor. It was one of the first DSPs and is now used in products ranging from small scale control systems to adaptive filters for telecoms systems. Unfortunately up to now suitable dos software development tools have been rather expensive. But a complete software development package from Signals Research of Edinburgh, weighing in at around £50, could change that.

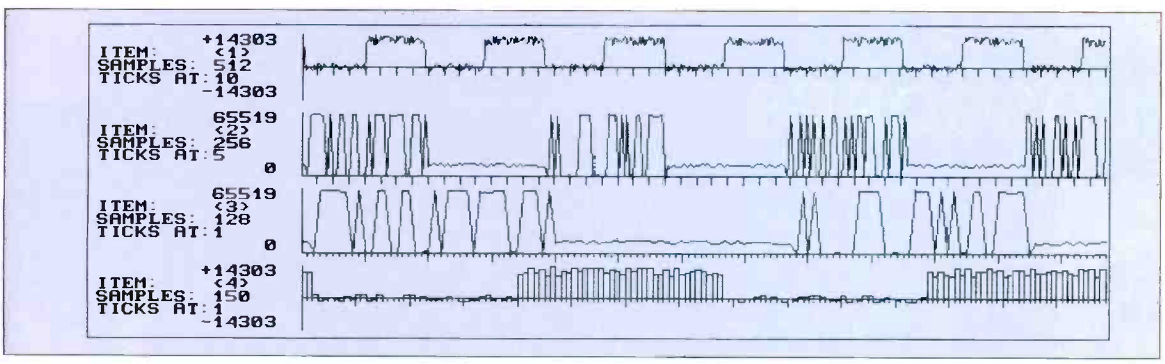
SR's package consists of a cross assembler, a linker and a software simulator for either the *C10* or the *E15*. Run it on a PC and it represents a complete software development facility, remarkably straightforward to use.



Simulator display has a major part given over to the code being executed. The current line of execution is highlighted.

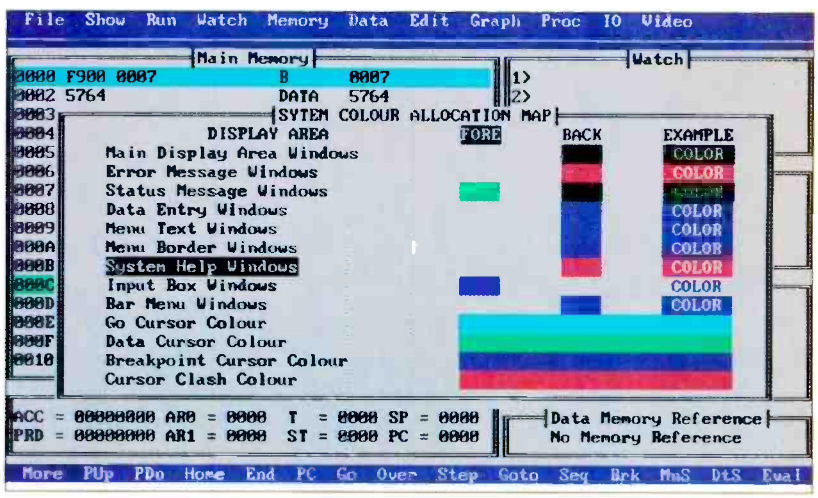
Assembling and linking

The cross assembler is a normal two pass utility which recognises the assembler directives found in TI's own product – differences are minor. The cross assembler is also able to produce the relocatable code useful in large program creation based on modular design. As expected, two output files are produced, the assembly listings (.LST) and an object module (.OBJ).



Plotting input and output data files on the simulator. Up to four graphical outputs or inputs can be plotted – useful when checking if the program is operating as expected.

The linker on the other hand operates differently to the TI product. No command file is required as the object modules for linking are entered into the command line in the order of linking. The three output files are a map file (.MAP) containing the address allocations for each object module; code file



Colours can be configured.

SYSTEM REQUIREMENTS
PC with hard disc
MS-dos 3.x
VGA/EGA or Hercules graphics
Mouse (optional)
Suitable text editor

(.COD) which is the executable code, and a symbol file (.SYM) for use by the simulator. The linker needs the normal information relating to data and program offset values.

The only facility missing from the package is a dedicated text editor – which would be especially useful if it had an attached help file specific to the product. In essence the help file would consist of the user manual on disc. The manual itself is reasonably informative, gives information relating to the assembly language instructions for the *TMS320C10* and also provides detailed information on the operation of the simulator. But it would be more accessible as a help file where a search could be performed on a highlighted word.

Simulated treats

The package includes a well designed software simulator – a treat to use – that works with either VGA/EGA or on a Hercules monitor using the supplied *Herc* utility.

After loading an output file from the linker into the simulator, the SYMDEF option will carry the symbols from the source file which appear in the simulator's main memory window. A major part of the display is given over to the code being executed and the current line of execution is highlighted. When examining memory this area is given over to the memory display.

The simulator can be mouse driven, with an attractive feature being the array of drop-down menus at the top of the screen – extra commands are available at the base of the screen. The two regions on the screen used for error emending purposes are a parameter watch facility and a trace option.

Simulating input data through any of the ports is achieved by attaching disc files directly to the ports – remarkably easy to set up from an option in the IO menu. Input and output data files can be in any format (hex, decimal etc), or the graphics facility allows data to be plotted as it comes out of a port(s).

Up to four graphical outputs or inputs can be plotted in an appealing facility that proves useful when checking if the program is operating as expected. Contents of all the processor registers are shown by the simulator which comes with a variety of operating options: single stepping, break points, background processing to name just a few.

For the colour conscious the display can be changed and the configuration of the simulator can also be saved.

My only reservation about the simulator is its apparent inability to simulate the effect of either the BIO or INT pins going low. These pins are used for polling and interrupt purposes respectively and their usage is quite important in the design of a *TMS320C10* system.

Must have one

Any designer working with the first generation of TI DSP devices should have the *TMS3201X* DSP development package. Ease of use, low cost and completeness as a software development package make it a beguiling product. The processor, with its uncluttered architecture, is a good teaching tool and the package will interest educational institutions making the most of a limited budget.

TMS320C10 still has a lot of mileage left in it and this package will further its appeal especially for the user taking a first tentative step into the world of DSP. ■

SUPPLIER DETAILS
£50. Signals Research Ltd, 113/9 Bellevue Road, Edinburgh, EH7 4DG.

IT'S A DIRTY JOB but now a PC can do it

Take the PC_e bus and a handful of plug-in cards and what have you got? A powerful machine running PC software but not frightened of getting its digits dirty, says Chris Nabavi*.

Walk round almost any industrial plant and you will see PCs being used for plant monitoring, data gathering and process control. In effect, the ubiquitous PC is taking over more and more tasks for which it was not originally intended.

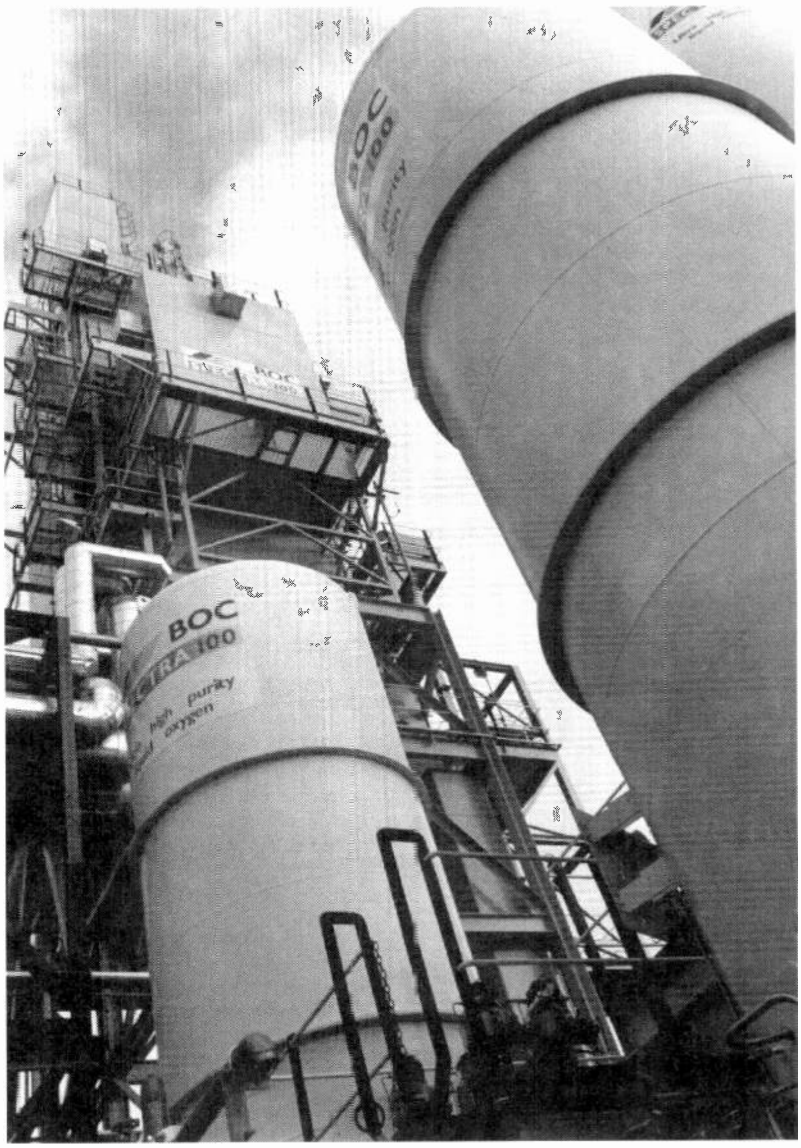
The attraction of the PC is its widespread acceptance. If a system can be made "PC compatible", its design becomes easier to implement and maintain. Good quality compilers and other software development tools can also be obtained at modest prices and the system can be upgraded and modified much more easily.

But a disadvantage of using a PC in an industrial environment is that it has been designed as a desktop unit. In particular, the card format is unsuitable for three reasons:

- The mother board is often difficult to access and ISA expansion cards come in different lengths, relying on the connector as the main means of mechanical support. This makes them unable to withstand vibration.
- Long thin shape of the standard ISA expansion cards with the bus connectors on the long edge makes them awkward to fit in an industrial housing such as a rack.
- Direct connector (ie one that uses gold plated PCB fingers) is not as reliable as a two part connector of the type normally specified for industrial environments.

Over the last few years, some manufacturers have attempted to follow a middle road, offering a measure of PC compatibility, but remaining suitable for industrial applications. Several companies offer STE cards which claim to be "PC

*Sherwood Data Systems, High Wycombe.



The PC_e bus allows all the software options and convenience that make PCs such a popular choice , while forming the basis for machines much more suited to the industrial environment.

Bus definition

PC_e bus signals are electrically and functionally identical to those of the ISA standard. The 62 pin connector corresponds to the 8-bit connector in the older XT style PCs, and a 36 pin auxiliary connector corresponds with the upper data byte and other additions used in 16-bit PC-ATs. To map the 98 pin ISA bus onto the 96 pin DIN41612 connector of the PC_e bus, two signals have to be sacrificed; these are one of the triplicated +5V supply pins and the –5V supply.

Since modern chips tend to use less power than when the PC-XT bus was first defined, the loss of one of the three +5V supply rails imposes no real penalty. The cards are also smaller, and the connector is better, so the remaining two +5V lines are quite adequate. Loss of the –5V rail is also not important as it is rarely used on modern cards and can be easily generated from –12V on any card that needs it. For example, Sherwood Data Systems has designed a PC_e-to-ISA card adapter to allow ISA cards to be used in a PC_e system (mainly for development purposes). This adapter card has a -5V regulator on it so that the full ISA bus specification can be met.

Mapping of the ISA signals onto the 96 pin DIN connector was quite cleverly thought out by the bus originators. Pin out of most PC chip sets has been designed to allow routing to the ISA bus without the need for numerous cross-overs, simplifying board layout and conserving space. So the PC_e bus follows the same pin sequence as far as practical. The main 62 pin XT connector is mapped on to the outer two rows of the PC_e 96 pin connector, and the remaining signals are mainly on the inner row. This scheme allows many cards to be designed with the two row 64 pin version of the DIN41612 connector and a simple XT style system can be built using 64 pin connectors with a consequent saving in cost and complexity. Since the 64 pin and the 96 pin connectors are compatible, XT and AT versions of PC_e cards can be mixed in a system, just as in a conventional PC.

The PC_e bus signals are shown in Table 1. Note that a few of the signals are sometimes known by different names. For example on XT systems IRQ9 is IRQ2 and the signal -REFRESH is provided by -DACK0. The AT signal 0WS is also known as -SRDY or ENDXFR, and CLK is sometimes called BCLK. The signal timing and electrical drive specifications are all identical to those on the standard ISA bus.

Anyone wishing to design PC_e cards should refer to one of the many ISA reference books or to the IEEE P996 standard itself for complete descriptions of the signals (see bibliography).

Table 1. PC_e Bus signal pin out

Pin	Row a	Row b	Row c
1	0VL	-MASTER	-IOCHCHK
2	RSTDRV	SD15	SD7
3	+5V	SD14	SD6
4	IRQ9	SD13	SD5
5	-MEMR	SD12	SD4
6	DRQ2	SD11	SD3
7	-12V	SD10	SD2
8	0WS	SD9	SD1
9	+12V	SD8	SD0
10	0VL	-SBHE	IOCHRDY
11	-SMEMW	LA23	AEN
12	-SMEMR	LA22	SA19
13	-IOW	LA21	SA18
14	-IOR	LA20	SA17
15	-DACK3	LA19	SA16
16	DRQ3	LA18	SA15
17	-DACK1	LA17	SA14
18	DRQ1	-DACK7	SA13
19	-REFRESH	DRQ7	SA12
20	CLK	-DACK6	SA11
21	IRQ7	DRQ6	SA10
22	IRQ6	-DACK5	SA9
23	IRQ5	DRQ5	SA8
24	IRQ4	-DACK0	SA7
25	IRQ3	DRQ0	SA6
26	-DACK2	-MEMCS16	SA5
27	T/C	-IOCS16	SA4
28	BALE	IRQ15	SA3
29	+5V	IRQ14	SA2
30	OSC	IRQ12	SA1
31	-MEMW	IRQ11	SA0
32	0VL	IRQ10	0VL

compatible". But the problem with such compromises is that it is difficult, if not impossible, to obtain a sufficient level of compatibility to run a wide range of standard PC software.

Modern PC programs tend to make heavy use of interrupts and often assume that certain hardware resources are available in precisely defined ways – particularly in graphics and communications software. Older, more general buses such as STE and VME were not developed with this in mind and impose restrictions on system design making it impossible to obtain proper PC compatibility.

One other approach is still to use standard PC cards, but provide a better mechanical framework so that compatibility is assured within an industrial housing. Unfortunately such "industrial" PCs tend to be both expensive and unwieldy.

Enter the PC_e bus

But a simple solution now available – already being adopted in the UK and Germany – is to use the standard ISA signals as found on all standard PC cards, and map them onto a high quality 96 pin DIN41612 male connector. The card itself is the popular single Eurocard which measures 100 x 160mm. In the UK, the bus is known as the PC_e bus (in Germany it is also called the VG96 bus, though strictly speaking, this is simply a name for the 96 pin connector). Unlike the standard PC based on a mother-board with plug-in expansion cards, the PC_e system uses separate cards for all the electronics and a back-plane without any active components.

The bus definition is an informal one, but since the signals are the same as those of the ISA standard, adopted as the IEEE P996 bus, all the signal meanings, timings and other characteristics are fully and formally defined. Ensuring a design conforms to the standard is also straightforward since the semiconductor industry now offers a large range of PC chip sets, designed for use in conventional PCs, but ideal for PC_e bus systems. Such chip sets handle bus interfacing and result in a compact, low chip-count design. Without them, obtaining the required level of integration on a single Eurocard would be impossible.

The fact that VLSI PC chip sets developed for the high volume desktop PC market can be used, allows PC_e systems to achieve a high level of performance and functionality but at a price normally associated with consumer products.

Available PC_e products

PC_e cards available include *8086*, *286*, *386SX* and *486SLC* based CPUs, multifunction i/o cards, flat panel and CRT based VGA display boards, opto-isolated industrial interfaces, prototyping cards, GPS (satellite positioning) cards and touch screen interfaces.

To build the equivalent of a standard PC-AT, first designs on the market needed three cards: a processor card; a display card and an i/o card. Processor cards contain the microprocessor, bios rom, ram, keyboard controller and system- and bus-controller chips.

But a more recent design, based on the *pcChip,* has a complete PC-XT on a single Eurocard. The level of integration is now so high that an LCD/CRT display driver, three serial ports, a parallel port, rom and ram discs, real time and time of day clocks, keyboard interface and loudspeaker can all be included on one Eurocard along with the CPU, main memory and bios eprom. The card has a PC_e bus interface on it, though it is often used by itself. By adding small riser cards, other options such as conventional disks or a PCMCIA interface can be added.

Industrial applications may benefit from one of the special cards designed for real world interfacing. These include high- and low-voltage opto-isolated sensing and switching for industrial plant control. A variety of back-planes and different types of card-frames and racking systems are also available.

How compatible?

PC compatibility means different things to different people. Obviously, PC_e cards are not compatible in the sense that they cannot be plugged into a conventional PC. But for most users the important question is whether software developed for a standard desktop PC will run without change.

On this aspect, experience has been built up on PC_e bus based systems with a wide selection of common PC software, including compilers, word processors, cad software. Even more importantly, the bus handles the highly critical packages Deskview and Windows which run the processors in virtual mode and involve memory management.

Software performs as expected. But then it should, as the cards use standard PC circuits, and the card shape and connector type cannot affect operation of the software. PC_e systems have been run with both Microsoft MS-dos and Digital Research DR-dos.

Look – no disks

Conventional PCs use hard and floppy disks. But for industrial applications, rom-based systems with no moving parts are often more attractive, and so processor cards able to incorporate applications software in an extra large bios rom in the form of a rom disc have been designed. The rom acts just like an ordinary disk (except that it is read-only), and a suitable autoexec file will prompt the system to load and run applications automatically on power up, allowing the system to be dedicated to a particular task or set of tasks. Unless required by applications software, there is no need for a keyboard or display since the bios can be set to ignore errors generated during the power on system test (post) which would otherwise occur. Battery-backed ram disks can be used when a solid state writable medium is required.

Standard future

Reaction of users to the PC_e bus and the cards developed so far has been favourable. Eurocards have always been popular and are well supported by rack and case manufacturers and suppliers of ancillary equipment such as power supplies.

Systems can be made very small, with just a single card, or can be designed for expansion up to 21 cards in a full 19in rack.

In Germany the bus standard has been adopted by several large manufacturing companies and is now spreading to other countries. As yet, there does not seem to be a move to have the PC_e bus adopted formally. But many of the existing standards were used in industry for some time before being formalised. In the case of the PC_e bus, the fact that it is simply an existing formal standard on a different connector and card format should mean that there will be none of the usual misunderstandings and inconsistencies normally experienced with informal bus standards.

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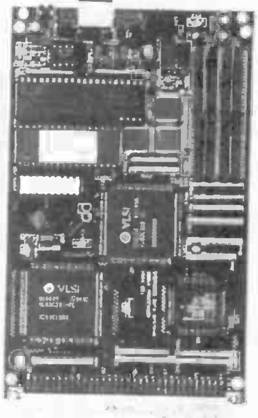
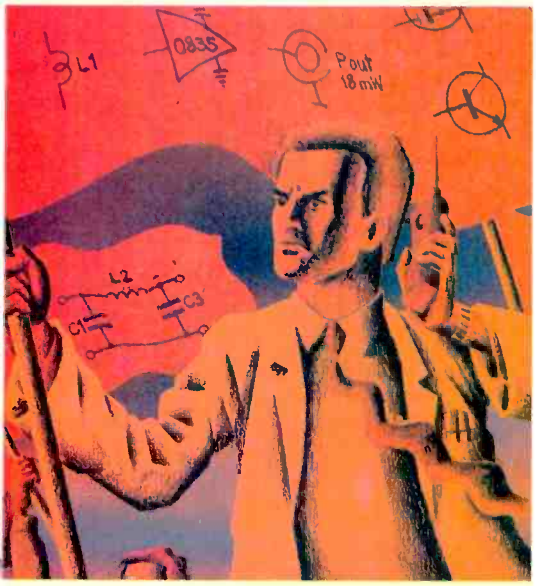


A 386SX based PC_e processor card from Sherwood Data Systems.

THE RF DESIGN REVOLUTION

3: Devices for frequency synthesis



DAVE BELL

Frequency generation is at the heart of RF design. Virtually all radiocomms systems operate on channelised frequency allocations. Demands on the spectrum require that frequency slots must be re-used; frequency agility is a must for user equipment. Only frequency synthesis can provide this. By Tim Stanley.

Direct digital synthesis provides advantages over its phase-locked equivalent – phase continuity while fast-frequency-hopping for instance. DDS systems exhibit phase noise performance determined mainly by the reference oscillator, a vast improvement on phase locked loops.

The most significant problem with DDS is the presence of unwanted spurious frequencies (spurs) in the output spectrum. These arise through non-linearity and quantisation error in the dac.

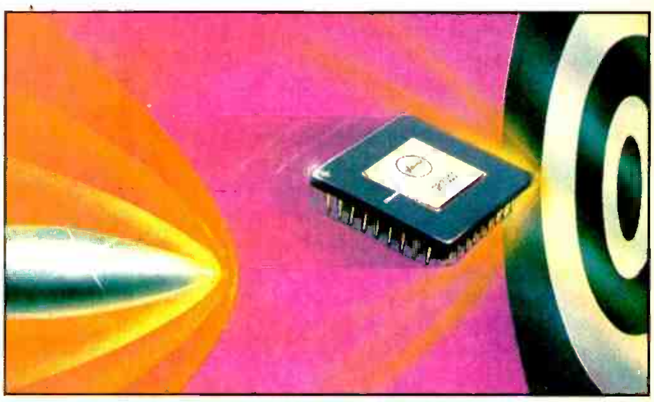
At some frequencies, these spurs may appear close to the required carrier and are therefore difficult to filter out. With the Plessey *SP2002* DDS system chip and most others, only the eight most significant bits of the accumulator are processed so that, regardless of the accuracy of the dac, the output voltage generated for any sampled point can only be approximate. This truncation error and any additional inaccuracy introduced in the dac lead to the generation of spurs in the output spectrum of the DDS. The spur amplitude can be reduced by increasing the number of accumulator bits used to determine the output, and by improving the dac accuracy.

The frequency of the spurs can be predicted, and in systems with reasonably wide-spaced channels it is possible, by careful choice of clock frequency, to ensure a minimum frequency separation of the closest spur at all the required tuning points.

Assume that an *SP2002* system is required to tune over the frequency range 100 to 120MHz in 50kHz steps. Using a clock frequency of 1638.4MHz will give a minimum frequency increment using the LSB input of the tuning bus of 0.762939453Hz. Bit16 of the tuning bus produces a tuning increment of exactly 50kHz. Tuning any frequency between 100 and 120MHz doesn't require any bits less significant than bit 16. Since no spurs will be produced closer to carrier than the incremental frequency of the least significant input bit used, this scheme will guarantee that no spurs occur at less than 50kHz from carrier. This topic is covered in the excellent series of articles on DDS by Ian Hickman (*EW+WW*, Aug-Nov 92).

By using a DDS in conjunction with a phase-locked loop synthesiser, as shown in **Fig. 1**, it is possible to design the PLL so that the loop bandwidth is less than 50kHz, thus removing any spurs from the final output. The PLL can also be used to increase the output frequency of the system to any desired value.

For a system requiring very close channel spacing, the hybrid DDS/PLL approach may not be appropriate since very narrow loop bandwidth may be required to suppress the close-in spurs generated by use of the low significance input bits, thus slowing down the loop response time. In these circumstances the use of frequency division, using widely available prescalers, can provide a better solution. The frequency divide reduces the spur level but has the possible disadvantage also of reducing the output frequency and channel step size. By combining the frequency division with mixing, the output frequency can be



Plessey's SP2002 direct waveform synthesiser processes only the eight most significant bits of the accumulator.

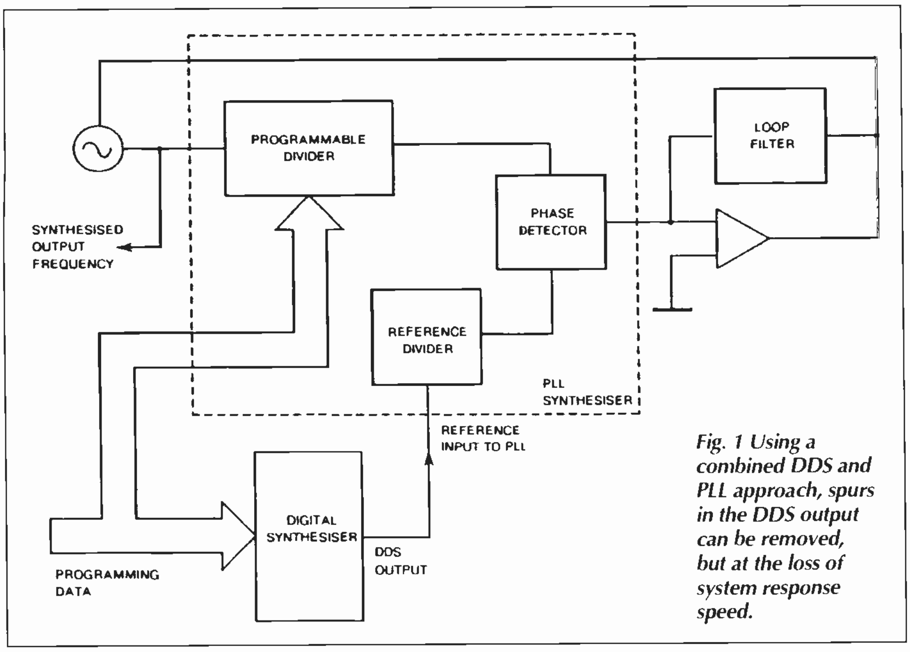


Fig. 1 Using a combined DDS and PLL approach, spurs in the DDS output can be removed, but at the loss of system response speed.

shifted to any desired point in the spectrum but the reduction in step size will remain.

The combination of mixing and dividing is very flexible and an almost infinite range of possibilities exists, but the method may require considerable additional hardware in the form of amplifiers and filters to produce a workable system.

Fully-Integrated DDS

The *SP2002* perhaps leads the field in DDS devices, being claimed by Plessey-GEC as the only fully integrated DDS IC to operate into the UHF output frequency range. This device comprises dual 8-bit dacs on-chip for sine wave outputs. Sine and cosine look-up tables are also integrated to provide quadrature outputs.

Operating at its highest speed, the device is clocking some 2000 to 3000 gates at nearly 2GHz; consumption is 5W using a 4.5V supply. The block diagram is shown in **Fig 2**; a typical application circuit in **Fig 3**.

The Stanford *STEL 2173* is another DDS device (termed a "numerically controlled oscillator" by the manufacturer) in the same league as the *SP2002*. Although it requires an external dac, it provides 0 to 400MHz output frequency range with 32-bit frequency resolution – equivalent to 0.23Hz at 1GHz clock frequency. The maximum clock frequency is quoted as 1GHz. Stanford states that spectral purity in a complete system is mainly determined by the characteristics of the chosen dac. Frequency hopping can be achieved in 16ns, although this will be lengthened by the dac delay. A 2-bit phase modulator is incorporated on-chip.

For quadrature outputs, two devices would have to be used, phase modulated to 0° and 90°. Lower cost 600MHz and 800MHz clock frequency versions are available. A block diagram is shown in **Fig. 4** and a typical application circuit in **Fig. 5**.

To maximise spectral purity, connections between dac and DDS chip should use transmission line elements of equal length. The analogue output of the dac should be isolated from the clock and other signals by close control of ground loops. Grounding and decoupling should be done with the objective of optimising the step response of the dac.

Table 1. Direct Digital Synthesisers

Manufacturer / Type No. / Technology / O/P Freq.range / Step / Clock Freq. / Hop speed / Noise / Spurious / Harmonics / Supply / Package / Price / Comments

GEC-Plessey / SP2002 / Si Bipolar / 0 - 400MHz / 0.5Hz @1GHz clock / up to 1.6GHz / 25ns (1.6GHz clock) / –135dBc/Hz at 10kHz from carrier / –45dBc typ. worst product / –43dBc typ. worst (3rd) / 4.5V 1.1 A typ. / PGA 68 pin grid / 1 - 24: £629.13, 100 - 999: £420.98. Prelim data.

Stanford / STEL 2173 / GaAs / 400MHz max / 0.23Hz @1GHz clock / 1GHz max / 16ns +dac delay / - / –55dBc typ / –5V 1.2A @1.2GHz clock / Die or 132 pin CQFP / 1 - 9: £1159, 25 - 99: £1004 / Prelim data.

Stanford / STEL 1180 / cmos / 25MHz max / 0.014Hz @60MHz clock / 60MHz max / ?(Auto. chirp facility) / 5V 4mA/MHz clock / 68 pin PLCC / 1 - 9: £128, 25 - 99: £111

Stanford / STEL 1177 / cmos / 15MHz max / 0.014Hz @60MHz clock / 60MHz max / 67ns +dac delay / - / –75dBc typ / 5V 4mA/MHz clock / / 1 - 9: £223, 25 - 99 £193

Harris / HSP 45106 / cmos / 20MHz max / 0.010Hz @40MHz clock / 40MHz max / 25ns @ 40MHz clock / –90dBc / 5V 256mA @25.6MHz clock / / 1 off: £68.30, 100 off: £35.94

Harris / HSP 45102 / cmos / 20MHz max / 0.009Hz @40MHz clock / 40MHz max / 25ns @ 40MHz clock / –60dBc / 5V 99mA @ 33MHz clock / 28 pin SOIC / 1 off: £34.00, 100 off:£17.90 / Low cost.

Sciteq / DDS-1 / ? / 11MHz max / 0.005Hz @ 25MHz clock / 25MHz max / <1µs / / –60dBc / +5V 150mA and –5.2V 100mA / 1X1" ceramic / 1 off: $350, 100 off: $150 / "The only DDS with 11-bit AM facility"

A spectral plot of the NCO output after conversion by a Tri-Quint *TQ6114* dac is shown in **Fig. 6**. In this case the clock frequency is programmed to 234.567MHz. The maximum non-harmonic spur level observed over the entire useful output frequency range in this case is –44 dBc. The spur levels are limited by the dynamic range of the dac. One should note that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the nyquist frequency (50% of the clock frequency). The image of the harmonic at the frequency $F_c - 2F_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $F_c/3$. It would be necessary to obtain a dac with better dynamic linearity to improve the spur levels.

The dynamic linearity of a dac is a function

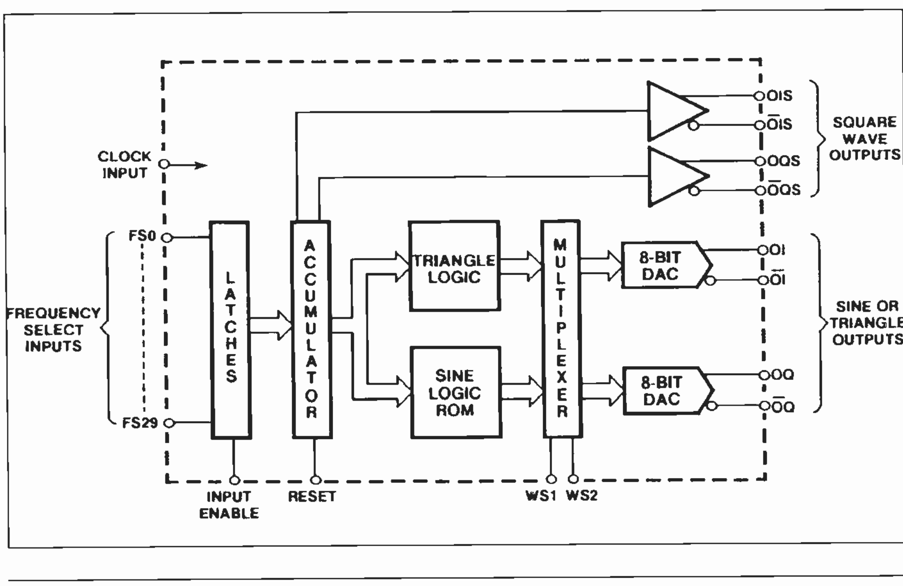


Fig. 2. Nearly 3000 gates are clocked at 1.6GHz to make the SP 2002 from GEC-Plessey Semiconductors the fastest fully integrated Direct Digital Synthesiser, providing sine wave outputs into the UHF range. High resolution, low phase noise and fast frequency hopping are some of the advantages of DDS over conventional Phase-Locked Loop synthesis.

Table 2. Phase locked loop synthesiser chips

Manufacturer / Type no. / Technology / Input freq. / Step size / Ref. Freq. / Supply / Input sens. / Package / Price / Comments

GEC-PLessey / NJ88C33 / cmos / 150MHz max. / 37kHz @150 MHz? / 52MHz max / 5V 2mA / DP14, MP14 / 1 – 24: £5.19, 100 – 999: £3.58 / Prelim. data

Swindon Silicon Systems / SSSB 139 / Si / 4GHz max. / Fin/67 / 200MHz max / 5V 155mA typ. / ECL / 28 pin LCC / 1 – 24: £86, 100 – 499: £60

Phillips / TSA 5511 / PLL / Si Bipolar / 64MHz to 1.3GHz / 50kHz at 1GHz o/p / 4MHz max. / 5V 35mA typ / 40 mV at 1.3GHz / SOT 102, 109 or 163 / 1 – 29: £2.28, 100 – 999: £1.45 / IsquaredC bus. For TV tuners. Prelim. spec.

Phillips / UMA 1014T / Bipolar / 50MHz to 1.1GHz / 5kHz to 100kHz throughout range. / 3 to 16MHz / 5V 115mA typ. / 50 mV @1.1GHz / Plastic; SO16 SSOP20 / 1 – 29: £6.783, 100 – 999: £4.76 / IsquaredC bus. Low power. For cellular radio. "Objective" spec.

Phillips / UMF 1009T / cmos / 18MHz max / ? / 16.8MHz max / / 5V 2.5 Ma max / 0.5 v p-p / SO16 Plastic / ? / IsquaredC bus. / Low power. Integrated ref. osc. / Prelim. spec.

Fujitsu / MB87006A / cmos / 17MHz max / ? / ?5V 3.5mA typ. / ? / 16 pin DIP, SOP / £1.55 /

Siemens / PMB 2306 / cmos / 220MHz max / 13kHz @220MHz? / 50MHz max. / 5V 3.5mA typ. / 180 mV / P-DSO-14 / 1 – 25: £5.00, 100 – 249: £4.50 / "Extremely fast phase detector". High i/p sens. Prelim. spec.

Siemens / TBB 206 / cmos / 90MHz max / 22kHz @90MHz? / 30MHz max / 5V 2.5mA typ. / 50 mV / P-DIP-14, P-DSO-14 / 1 – 99: £3.60, 100 – 249: £3.32 / High i/p sens. / Low power. "Extremely fast phase detector". Preliminary data.

Siemens Semiconductors, Siemens House, Windmill Road, Sunbury-on-Thames, Middx, TW16 7HS, Tel 0932 752615, Fax 0932 752632

GEC Plessey Semiconductors, Cheney Manor, Swindon, Wilts, SN2 2QW, Tel 0793 518000, Fax 0793 518411

Fujitsu Microelctronics Ltd, Electronic Components Div, Hargrave House, Belmont Road, Maidenhead, Berks, SL6 6NE, Tel 0628 76100, Fax 0628 781484

Stanford Telecom, UK Agents: BFI Ibexsa Electronics Ltd., BFI Ibexsa House, Burnt Ash Road, Quarry Wood Estate, Aylesford South, Kent, ME20 7NA, Tel 0622 882467, Fax 0622 882469

Harris Semiconductor Ltd, Riverside Way, Wattchmoor Park, Camberley, Surrey, GU15 3YQ, Tel 0276 686886, Fax 0276 682323

Sciteq Electronics Inc, UK Agents: Lyons Instruments Ltd., Ware Road, Hoddesdon, Herts, EN11 9DX, Tel 0992 467161, Fax 0992 444513

Swindon Silicon Systems Ltd, Radnor Street, Swindon, Wilts, SN1 3PR, Tel 0793614039, Fax 0793 616215

Phillips Semiconductors, Distributor: Macro, Burnham Lane, Slough, SL1 6LN, Tel 0628 604383, Fax 0628 666873/66807

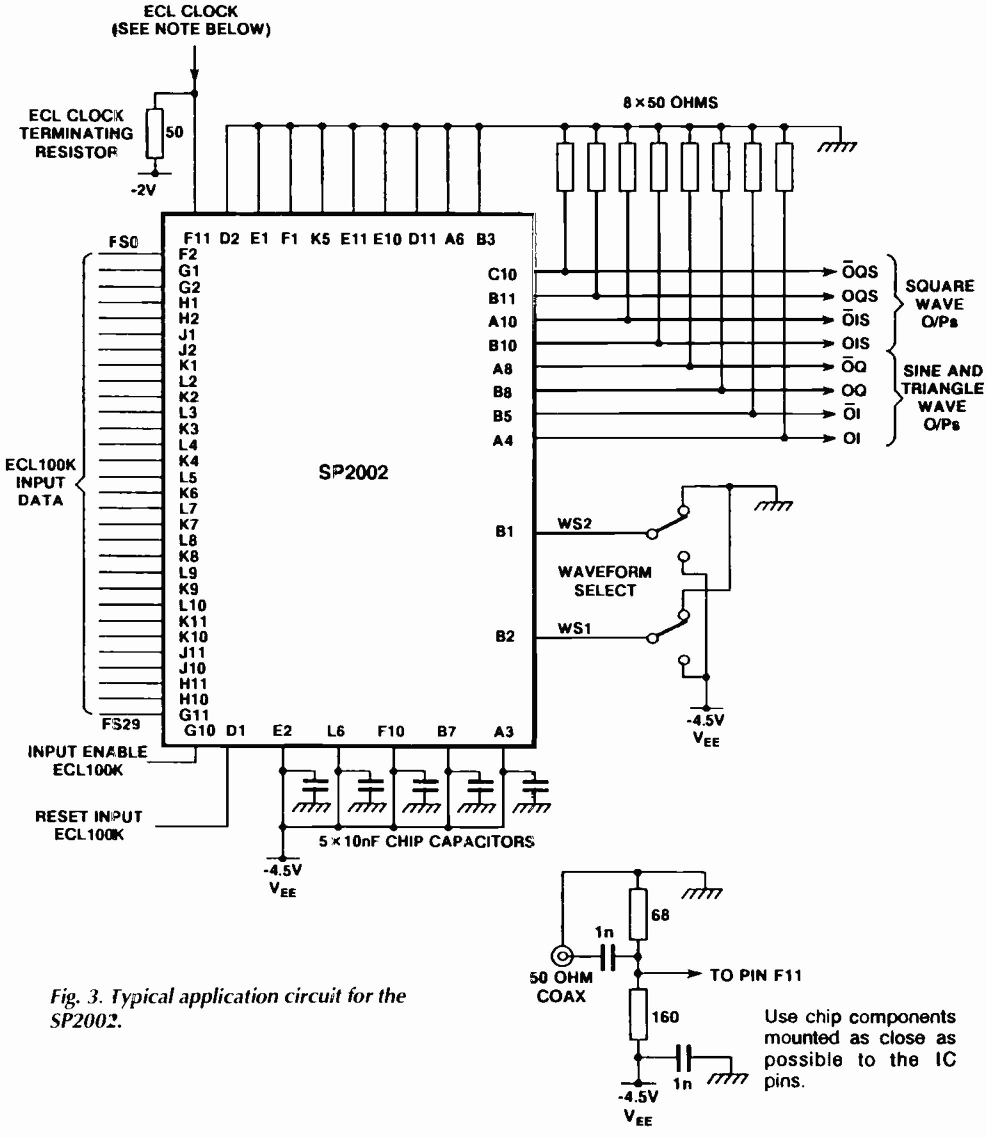
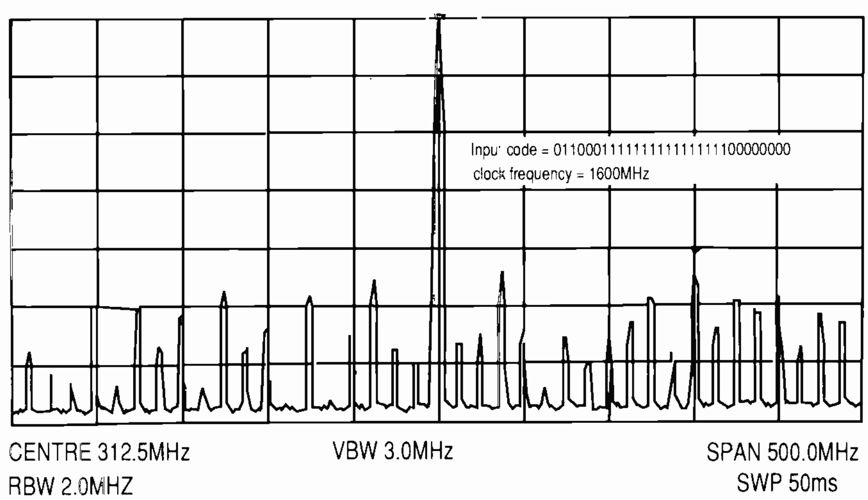


Fig. 3. Typical application circuit for the SP2002.



Typical SP2002 DDS output spectrum. The spur amplitudes produced tend to be affected by the output frequency rather than the clock frequency. The trace shows the worst case spur levels at an output frequency of 100MHz with a clock frequency of 400MHz and 1600MHz and, as can be seen, in both cases the worst case spur level is very close to the theoretical limit of –48dBc. This remains close to –48dBc at all output frequencies up to about 125MHz but degrades above this frequency to about –45dBc at 200MHz, –40dBc at 300MHz and –31dBc at the maximum output of 400MHz. A difficulty in determining the worst case spur for any output frequency is that there is often a "close-in series" and another further out which must both be examined separately to find the spur of the greatest magnitude.

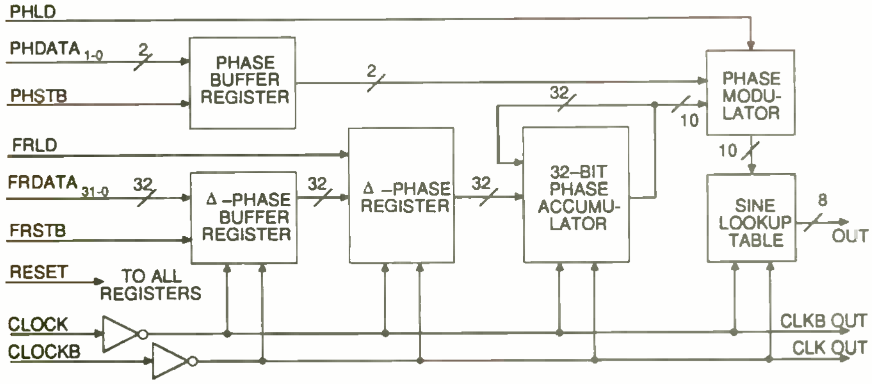


Fig. 4 The STEL2173 Numerically Controlled Oscillator from Stanford, usable for synthesis of up to 400MHz, provides 32-bit frequency resolution (i.e. 0.23Hz at 1GHz clock) and very fast frequency hopping – although the external digital to analogue converter required will add to the settling time.

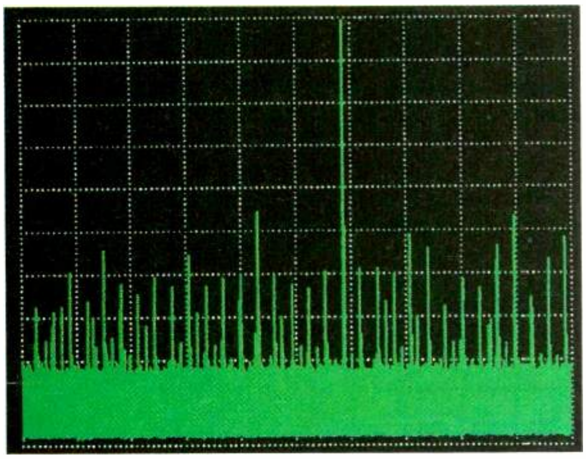


Fig .6. STEL2173 typical output spectrum using the application circuit of Fig. 5. Particular attention must be paid to the wiring between the DDS controller chip and the outboard dac. Any variation in phase delay between the bits presented to the converter will manifest itself as increased spur levels in the output spectrum.. Frequency span 0-400MHz Reference level +0dBm Resolution bandwidth 10kHz Scale log 10dB/div Output frequency 234.567MHz Clock frequency 1GHz.

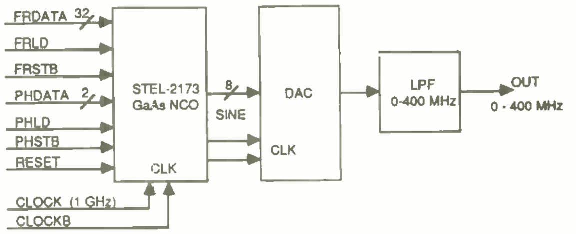
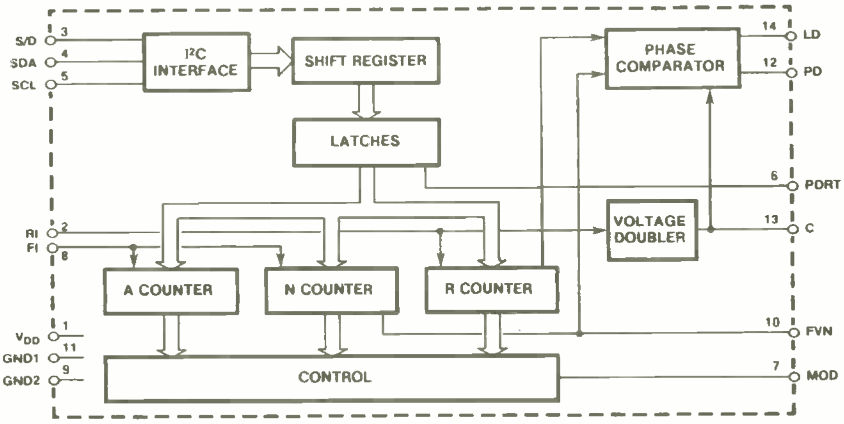
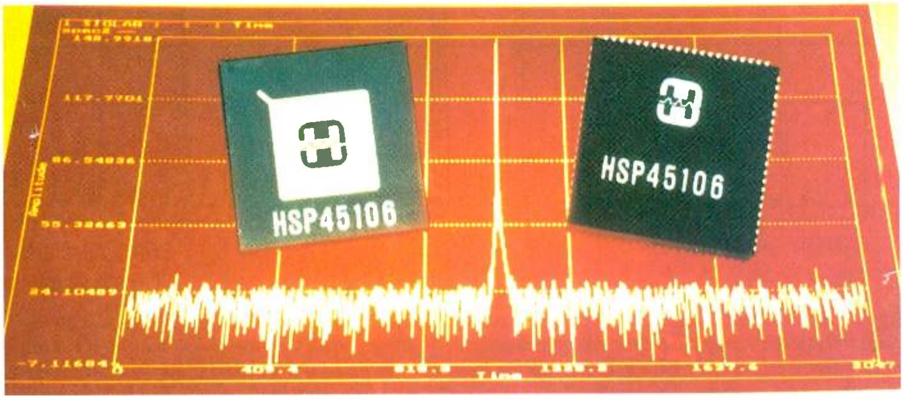


Fig. 5 The STEL2173 is used with a high-speed D to A converter, such as the TriQuint TQ6112, for a phase-coherent, fast switching frequency synthesiser. The spurious components at the output of the low-pass filter are about 55dB below the primary output component. With a clock frequency of 858.9935MHz (ie 0.2 X 232Hz), the frequency steps obtainable are exactly 0.2Hz. The output frequency may be programmed from DC to over 400MHz – depending on the low-pass filter. In order to keep the sampling components above the Nyquist frequency at a level compatible with the other spurious components, the low-pass filter needs to have at least 55dB attenuation above Fc – Fo, where Fc is the clock frequency and Fo is the highest output frequency desired.

Fig. 7. Simplified block diagram, and (Fig. 8.) typical application circuit for 60 to 80MHz, of the new NJ88C33 Phase-locked Loop IC from GEC-Plessey. The device can be used for synthesis up to 150MHz without pre-scaling, requiring only 2mA typical supply current at 5V.





Harris has recently added to its range of NCOs for use up to about 40MHz output, with the HSP 45106. Frequency resolution is 32 bits (0.01Hz at 40MHz) and programmable phase control register allows control to better than 0.006 degrees. For applications at these frequencies, the range provides a cost-effective solution – the HSP 45102 is offered as a low-cost device at £17.90 (100-off price). 69dB of spurious-free dynamic range is claimed to be attainable.

both of its static linearity and its dynamic characteristics, such as settling tine and slew rates. At higher output frequencies the waveform produced by the dac will have large output changes from sample to sample. For this reason, the settling time of the dac should be short in comparison with the clock period. As a general rule, the dac used should have the lowest possible glitch energy as well as the shortest possible settling time.

Phase-Locked Loops

For many applications, and particularly those in battery operated/portable equipment, conventional PLLs are still the obvious choice for programmable frequency generation. Development of new devices with ever reducing power requirements continues.

GEC-Plessey's *NJ88C33* offers I²C bus pro-

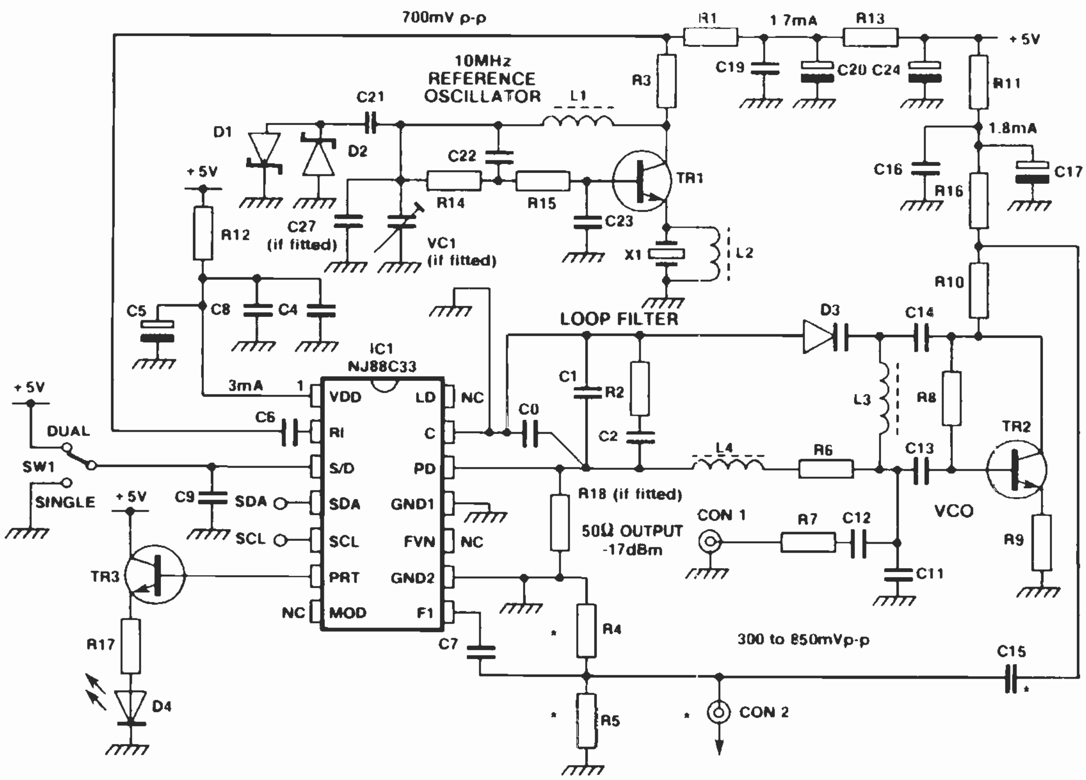


Fig. 8. The GEC-Plessey NJ88C33 evaluation board provides a reference oscillator, a 60 to 80MHz VCO and a simple loop filter to complete a minimal frequency synthesiser loop. The two units allow analysis of different loop variables as well as the selection of comparison frequencies for fast frequency-lopping loops.

grammability and is usable up to 150MHz input without external pre-scalers. It needs just 15mW to power the device which uses a digital phase comparator. Envisaged applications include cordless telephones (CT2, DECT), cellular phones (GSM, PCN, ETACS) and sonar buoys. Block and application diagrams are shown in **Figs. 7** and **8**.

Another device exploiting the low-power advantages of cmos is the Siemens' *PMB2306*. Special PLL features include an input sensitivity of 180mV up to 220MHz and extremely fast phase detector for frequency hopping applications. Phillips *TSA5511* is a low-cost bipolar single-chip synthesiser for use from 64MHz to 1.3GHz offered at £1.45 in 100-off quantities, intended primarily for terrestrial and satellite TV tuners. Features include I²C bus transceiver and device address selection for picture-in-picture capability using duplicate circuits. **Fig. 9** shows the device architecture. ■

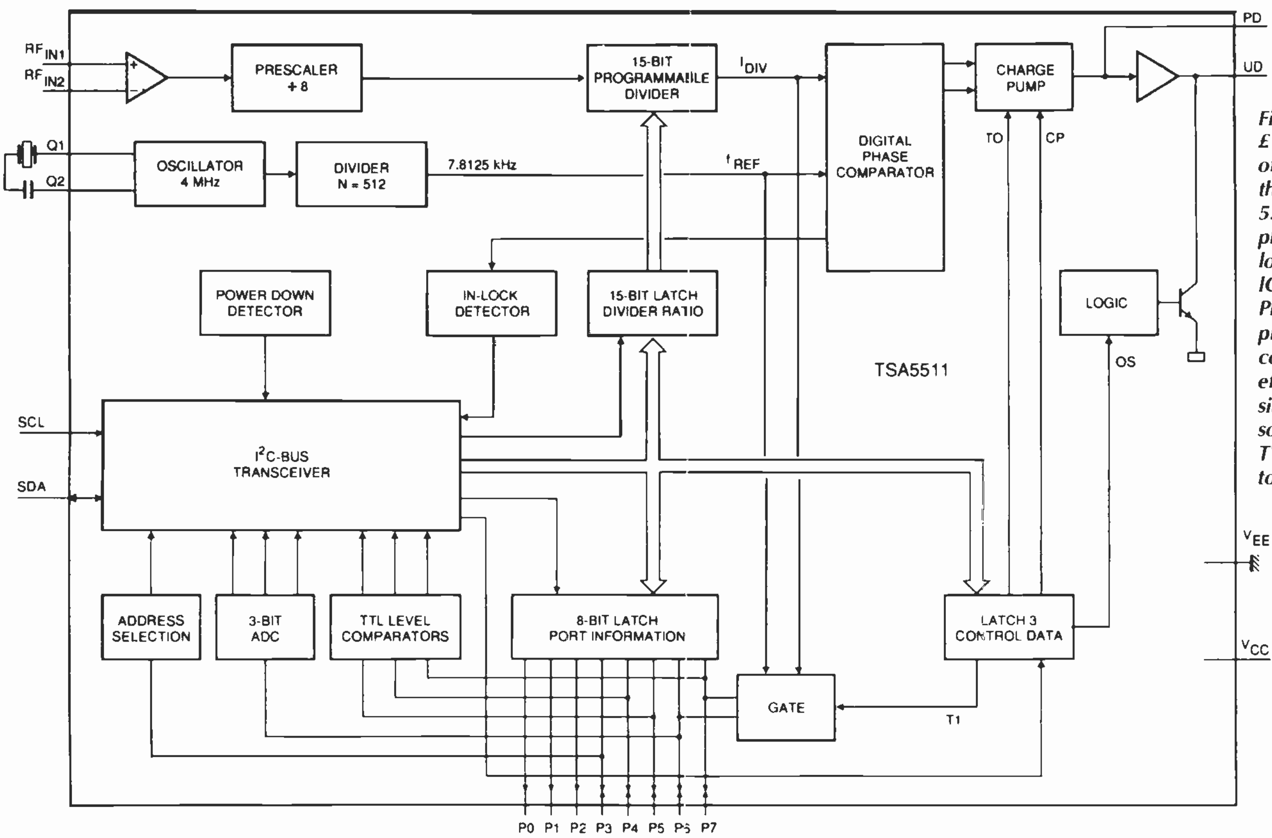


Fig. 9 At £1.45 (100-off price) the TSA 5511 phase-locked loop IC from Phillips provides a cost-effective single-chip solution for TV tuners to 1.3GHz

Crossed eyes

I have read Pat Hawker's articles "The handheld that endangers eyes" and "RF exposure puzzle remains", (*EW + WW*, RF Connections, October 1992), several times. They present viewpoints which appear to share a common theme: uncertainty and lack of firm evidence. What was the intention? If it was to connect eye damage risk to hand-portable radios, that was certainly not achieved by data in the text.

The Kuster and Balzano study referred to is not definite, stating a need to revise health safety regulations for handheld equipment but without giving any indication of what a realistic limit would need to be in practice. Using the worst Kuster and Balzano figures quoted – an SAR of 40mW/g – a sample of tissue (assumed mainly water) in such a field would need to be exposed continuously for over eight minutes in vacuo for the rise in temperature of 5K mentioned as an established cause of eye damage. Even a bloodless eye lens, immersed in fluid, must lose heat at a sufficient rate for the 40mJ/s of heat involved to reach equilibrium with a far smaller temperature differential.

Presumably the furnace workers' eye damage accumulated over a period of time, a factor not addressed in the case of RF. It is worth remembering that, in bright sunlight, the radiant energy incident on a 5mm pupil is not far short of 20mW and you do not have to be looking straight at the sun for this to be the case. Lens mass must surely not exceed 200mg (my own guess), resulting in a quite natural radiation incidence, and presumably SAR, of around 100mW/g.

Lack of epidemiological data is notable with personal radios in use by military, police and commercial interests for many years in large numbers. Risks of a serious nature would surely have been noticed by now. I am not claiming there is no risk but if there is, it is by no means established in your article which does not display the kind of logical consistency needed to form a clear objective view of important matters such as these.

You are quite right to bring these varied viewpoints to our attention but your big mistake is to come to a sweeping conclusion not supported by the article. The title "The handhelds that endanger eyes" screams such a conclusion at the reader. It is a sensational headline and will alarm many people unnecessarily.

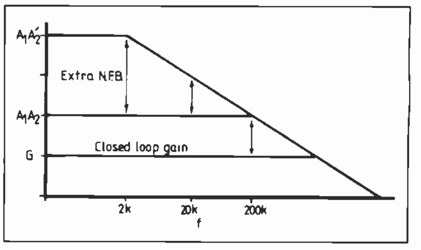
A J Honk
Epsom

200 what amplifier?

Andrew Hefley's design article "High Fidelity, Low Feedback, 200 Watts", (*EW + WW*, June 1992), raises a number of issues fundamental to the design of practical high performance amplifiers.

The concept that TID occurs in amplifiers with open loop bandwidths less than 20kHz has long been discredited and replaced with the requirements of adequate slewing rate for low 20kHz THD. Within this single constraint, a design with increased available loop gain, for feedback, below 20kHz is effective in reducing THD and IMD in most audible mid-range frequencies. The importance is apparent when we acknowledge that modern ribbon loudspeakers are capable of THD of 0.01% and that the power amplifier should not be a weak link by adding significantly to this. Hefley's design ignores the fact and deliberately wide-bands open loop response to well beyond even 20kHz, effectively wasting gain which could otherwise be used for mid-range distortion reduction. Indeed, a performance metric of 20kHz THD is better served by exchanging bandwidth for open loop gain to below 20kHz by increasing R_{25}, R_{26} to 27K or greater. The effect is not only to reduce output stage transconductance errors, at which global feedback is very effective but also reduce modulation of 2nd stage current and input differential signal by an order of magnitude, resulting in lower open loop THD.

A further distortion mechanism not well addressed in Hefley's design is common mode distortion due to finite tail resistance of the input differential stage. Common mode voltage, set by the closed loop gain requirement or sensitivity to the amplifier is greater than differential input voltage by the amount of loop negative feedback. Any distortion it



generates will be more significant the higher the feedback, as current variation in the tail due to common mode voltage modulates transconductance of the stage. Predominantly even order distortion, it is partially balanced out in Hefley's design in the following complementary common emitter stage. But the simple expedient of replacing R_7 and R_8 with quality current sources is far preferable to an imperfect cancellation technique. Of further benefit here would be to take both outputs from the input stage to a fully complementary differential of folded cascode second stage, as it would with improving PSRR.

A third area of concern with Hefley's design becomes apparent by considering its use with an appropriate size of power transformer for the application. A 100W/ch amplifier should function effectively with a power transformer of no more than 300VA in combination with the 10,000µF filter capacitors. The typically poor transformer regulation permits substantial extra amplifier power output under low duty transient conditions – in line with the demands of modern musical programming. While Hefley's design provides RC filtering of power supply impedance interactions, this filtering is ineffective at very low frequencies where power envelope demands substantially modulate supply voltage. Increased gain before the intrusion point, in this case the input stage collector(s), is not an option here as it would compromise input signal handling and distortion. A more elegant solution is to reduce the intrusion using a fully differential or folded cascode second stage, effecting a typical 46dB improvement using standard components.

Finally, Hefley makes two, fundamentally flawed, statements - "A side effect of a high open loop

Alternative route to dat

I would like to propose a simple alternative to the design mentioned in the article "Improved pre-amps put dat back on the road", (*EW + WW*, October 1992), where a basic differential amplifier is complimented by an inverter. The input common mode signal is nearly zero. A simple way of maintaining the DC output around $1/2V_{cc}$ is obtained.

The gain is halved, so resistor values of R_3 need to be doubled, while noise behaviour is nearly the same compared to the published circuit. Noise contribution of IC_1 is negligible.

Nanno Herder
Netherlands

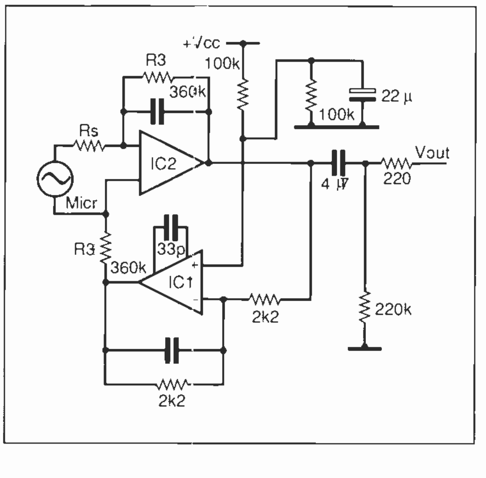
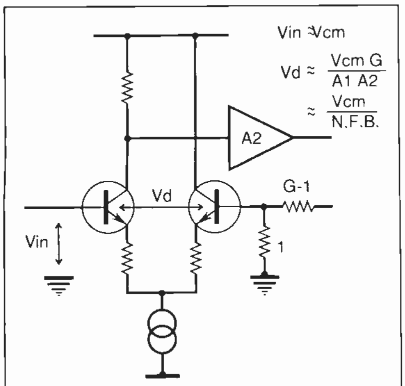


Fig. 1. Alternative mic preamp design



gain is that wide bandwidth is very difficult to achieve with two gain changes". But examples exist of well designed, albeit elaborate, single gain stage op-amps with folded cascode and current mirror loading achieving 110MHz GBW which translates to 20kHz bandwidth and 74dB gain – wide bandwidth *and* high gain.

Also: "Install multiple output devices to keep the current excursion low for each device so as to stay within a linear range of gain". In a typical class AB output stage, the greatest transconductance error occurs near zero (output current) crossing, the high current output being linearised by the emitter resistors. No matter how many output transistors are used, they must, in a conventional output stage, all traverse zero crossing at which r_e is of little value. Apart from elaborate correction circuits, global and nested feedback is very effective here as long as the excess gain does not drop substantially as with an unbiased output stage.

Greg Ball
Australia

Attraction of electricity without magnetism

I am pleased to be able to say, thanks to the article "Electricity without Magnetism", (*EW + WW*, July 1992) being published such interest has now been aroused that a small stock of defunct material has come into Strachan's possession, enough to build a new demonstration prototype comprising 1300 junction pairs connected in a 100x13 configured series-parallel array. Without any additional input other than ice this demonstrably delivers 0.60V continuously to drive an electric motor when small pieces of ice are melting on its non-ambient heat sink surface. This corresponds to 6mV per junction for a 20°C temperature differential, or 300μV/°C as a thermoelectric EMF temperature differential obtained from an aluminium-nickel bimetallic combination. Warm water flowing over the same surface drives the electric motor, and a pool of water left on the surface freezes extremely rapidly if the motor is replaced with a small battery to feed input power.

Research interest attracted by the article has reactivated the R & D and should allow us to confirm the physical nature of the action involved.

I have also been questioned by several readers about the heading given to my article . It was in fact an *EW + WW* initiative to alter the original title "Electronic Heat Engine", presumably resulting from an editorial deletion of introductory text. The latter had introduced Strachan-Aspen's invention as a way of generating electricity from heat without using a traditional steam turbine and electromagnetic generator.

While the Editor's opinion, expressed in conjunction with the article, stresses the view that the piezo-electric substrate material used may be the seat of the action, no doubt having regard to its pyroelectric properties, I do believe enhancement of the Peltier effect by dynamic excitation will prove to be the correct interpretation. In this regard, the hypothesis of cold spots choking the performance of conventional bimetallic thermocouples is supported, not only by our avoidance of the effect by rapid interruption of current flow, but by diagnostic tests probing effects of magnetic fields on junction current. Note that stray junction fields from residual magnetism of nickel are presented in the device described.

H Aspden
Southampton

Keeping an ear to the ground

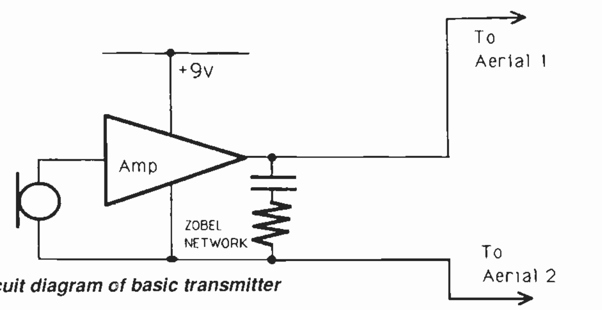
I have discovered a completely new communications medium, where there is no interference, no broadcast stations and in fact no transmissions of any sort. I have listened and called CQ for weeks at a time, all to no avail. I have tentatively transmitted at very low power levels, 2mW, walked 200m away and have received my own test signals.

Experimental apparatus needed is extremely simple – even my children use it – and I cannot understand why something so simple does not seem to be used by anyone else.

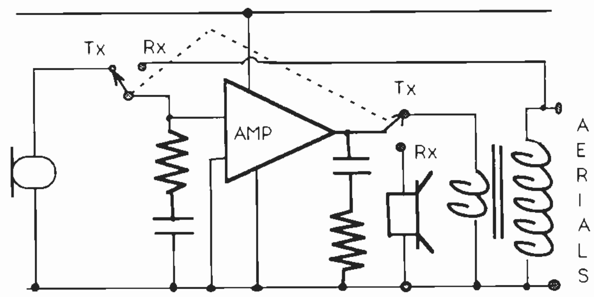
Main tests were carried out in the village of Harpenden, near Luton airport (IARU locator, I091TU, ordnance survey grid TL11) and initially were simplex, one-way communication.

My transmitter is constructed from an old radio, adding a few bits from my junk box, and aerials (two needed for each transmitter) are made from copper pipe, both approximately 4ft long. These I trimmed and placed strategically 168ft apart in my garden. Unfortunately power levels generated were low. 2W into a few ohms and I found impedance of the "new ether", due to local conditions, to be approximately 1000Ω. I could not fit the transmitter and antennas satisfactorily so I found that actual power transmitted was approximately 2mW. But, even with these minimal power levels, because there were no other transmissions at all, I was able to transmit approximately 200m! After such success from so basic equipment my initial calculations show almost all the UK could be covered by one 50W transmitter placed in the Midlands. Antennas could run both East and West, placed in the North and Irish Seas, giving complete UK coverage. Calculations show significant signal levels would appear throughout the World with a focus point in New Zealand. To demonstrate the theory take 9ft of resistance wire (900Ω), and place across a 9V DC battery. A current of approximately 10mA would be expected to flow. If voltmeter probes are placed across the central 3ft of resistance wire, a 3V reading would be expected (using Ohms law). To extend, use a 9V AC signal generator and expect to see similar volt meter AC signals.

If a signal generator is replaced with an audio amplifier, (where 900Ω resistance acts as a loud speaker), we would expect to hear, with the voltmeter turned into headphones, reduced volume signals (approximately one-third). Mismatch of audio amplifier to resistance wire is high and ideally a matching transformer should be employed.



Circuit diagram of basic transmitter



Full circuit diagram of transceiver

Consider an ohmmeter switched to a kΩ setting with probes 4ft long on wires 10ft long. If these probes are inserted into the ground, depending on distances between probes, the ohmmeter would be expected to show a resistance. Precise values of resistance depend on soil conductivity, length and distance of probes, amount of dissolved salts and absorbed water in soil. Take a poor sample of soil, with shorter probes and greater distance apart and assume the measured resistance between these two probes is 900Ω. Take the experimental equipment, (ie audio amplifier) and replace 900Ω of resistance wire with two ohmmeter probes – not forgetting to disconnect the ohm meter – and we will have a circuit consisting of an amplifier with its loud speaker replaced by two probes going into the ground. The probes represent, together with the ground loading, a resistance of 900Ω.

Examine between these two probes to find similar signal conditions, as experienced with the 900Ω resistance wire. By putting headphone terminals a few feet apart in the soil, audio signals transmitted will be received from the audio amplifier.

Signals are proportional to distance (ie resistance) between transmitting probes and receiving probes. We are in fact using the earth as a simple single sheet resistor.

No carrier wave is needed, tuned resonant circuits or high gain antennas are required, only audio amplifier and speaker leads buried a significant distance apart in the soil are required. A receiver can be – provided signal strengths are high enough – an ordinary pair of earphones, but greater distances have been achieved by using an audio amplifier where amplifier input is also just two probes taken from the ground.

Using extremely simple transceivers (audio amplifiers) it is possible to communicate through the Earth itself. Could it not be used for transmission and broadcast even of signals and communications data? Simple experimental tests have proved the viability, but mathematics of spherical sheet conductors, combined with skin effect is beyond me. I will leave it to others while listening and transmitting most weekends.

Andrew Ainger
Hertfordshire

Sorry Mr Ainger, your idea is not new. It first emerged in the early 50s but this doesn't mean that it shouldn't be reassessed using carrier techniques.
Editor

CFA – no tricks

In case Mr Donaldson (*EW + WW*, Letters, October 1992) should think we are members of the "sleight-of-hand" brigade, may I correct a slip in our "CFA working assumptions" article (*EW + WW*, December 1990) explaining how we believe a half-wave dipole radiates.

Figure 11, in the article, is correct but accompanying text should have read "entered from the feeder a *quarter* of a cycle earlier...". The calculation then becomes:

$$0 = \frac{r}{c} - \frac{\pi r}{2c} - \frac{\lambda}{4c} - \frac{r}{c}$$

$$0 = -\frac{\pi r}{2c} + \frac{\lambda}{4c}$$

So

$$r = \frac{\lambda}{2\pi}$$

the distance from conductors at which the radio wave is Poynting-Vector synthesised.

I wonder how many careful readers spotted that with the (correctly drawn) diagram the explanation made nonsense because, at the distance erroneously calculated, the position for charges at the moment shown would not even have been located on the wires.

Yes, we are trying to dispel any sleight-of-hand we see in textbooks. With our CFA, the current to top plate of the D-field system indeed creates magnetism of an opposite direction but it is located close-in near the wire since there flux paths are of low reluctance.

Magnetic flux used in the interaction zone is the widely spread field caused by widely spread displacement current of the D-plate system. If it were not widespread, it would be much more difficult to adjust the phase relationship. An interaction zone of 1/100 of a wavelength requires phase accuracy in adjustment of better than 1/100 of a cycle, such as 3.6°.

M C Hately
Hately Antenna Technology
Aberdeen

Unreal mic pre-amp

I seriously doubt claims of superior microphone preamplifier performance (in terms of high-fidelity) made by Adrian Pickering and Max Hadley, (*EW + WW*, October 1992). The design is fundamentally flawed because it makes no allowances for real-life behaviour of moving-coil microphones. Preamplifier gain is set by the impedance of the microphone, assumed by Pickering and Hadley to be a constant 200Ω at all audio frequencies – clearly unrealistic. Performance of their preamplifier must be much more sensitive and unforgiving of microphone characteristics than most (if not all) other designs. They fail to address this, apart from an unsupported statement qualifying established practice as a "myth". While their preamplifier may attain a low noise figure and be adequate for voice recording, frequency response with a real life microphone must be far from high-fidelity.

The basis of their extreme design seems to be a need to avoid the thermal noise of resistors: "Any resistances in the input generate their own thermal noise and", for this reason, "should be avoided". A fallacy, because thermal noise must be calculated for the equivalent impedance of the circuit; adding a 1kΩ resistor in parallel with the microphone actually lowers thermal noise (although it also lowers the signal). In addition, the 1kΩ load provides a reasonable (possibly not optimal) degree of damping for the movement of the microphone membrane. In contrast, self-induced Foucault's currents in the short-circuited microphone will definitely over-damp the microphone's response, and should result in a muffled sound. Plus, the very stiff membrane of the short-circuited microphone will result in a very poor coupling of sound wave energy and in a low microphone sensitivity.

P C Meunier
Cambridge ■

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FG 506 FG513

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THE 180 SERIES

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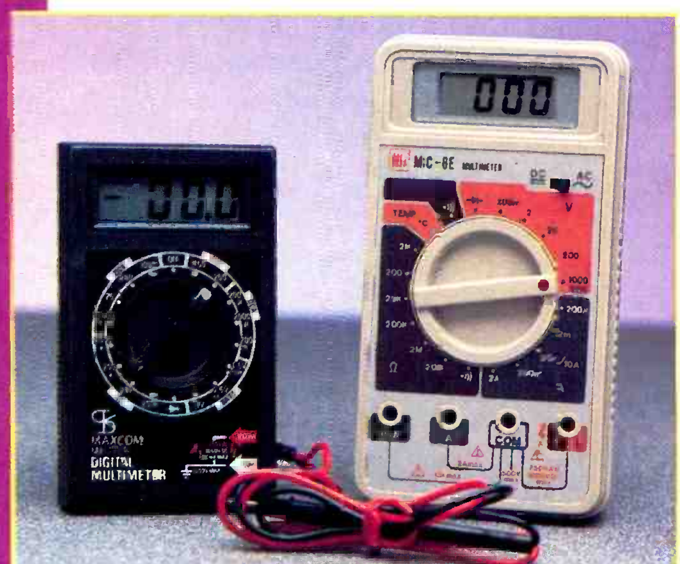

MX170B MIC-6E

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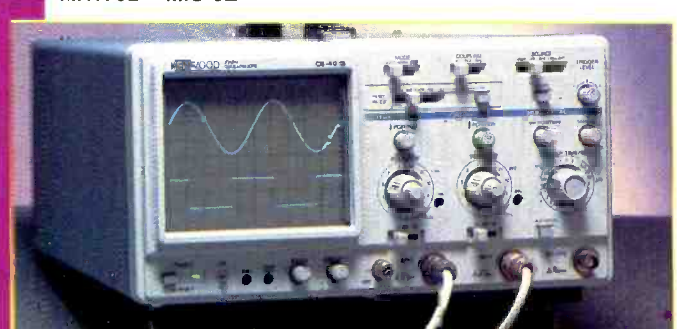
The CS4025 20MHz dual trace oscilloscope offers a comprehensive range of facilities including a high sensitivity vertical amplifier providing from 1mV to 5V/div in CH1, ALT, CHOP, ADD, CH2 modes with inverse polarity on CH2. The horizontal timebase offers a sweep range of 0.5s/div to 0.5µs/div plus x10 sweep expansion and X-Y mode. Triggering can be auto or normal from vert, CH1, CH2, line or external sources with coupling provided for AC, TV-F and TV-L. The CS4025 is supplied complete with matching probes for £295.00 plus VAT (£346.62).



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3. A 0.02Hz to 2MHz full featured sweep/function generator producing sine, square, triangle, skewed sine, pulse and a TTL output and linear or logarithmic sweep. Outputs of 50Ω and 600Ω impedance are standard features;

4. An auto/manual $3^1/_2$ digit LCD multimeter reading DCV, DCA, ACV, ACA, resistance, and relative measurement with data hold functions.

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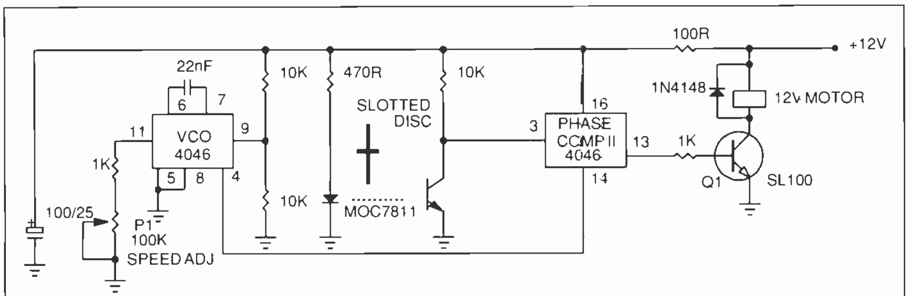
PLL motor-speed controller

This is a simple closed-loop controller for fractional-horsepower DC motors, although it is suggested that larger transistors will supply larger motors.

In essence, a slotted disc on the motor shaft, moving in the gap of an optical sensor, produces pulses at a frequency f_m dependent on the motor speed and the number of slots in the disc. Pulse rate and the reference frequency generated by the PLL's VCO are compared in the phase comparator and, when f_m is less than f_{ref}, the phase-comparator output goes high and Q_1 conducts, driving the motor, the reverse being the case when f_m exceeeds the reference frequency. The outcome is that motor speed is that which causes f_m to equal f_{ref}, which is variable by means of the potentiometer and by altering the value of C_1.

The circuit will control motor speed smoothly at speeds down to 300rpm, assuming the disc has at least ten slots in it.

M.S. Nagaraj,
ISRO Satellite Centre,
Bangalore, India



Phase-locked loop smoothly controls DC motor speed down to about 300rpm

Audible compass

Instead of graduations in degrees, this compass emits a tone which varies in frequency depending on where it is pointing – high pitch for north, low for south, the difference being about an octave. It is much more stable than some other published designs.

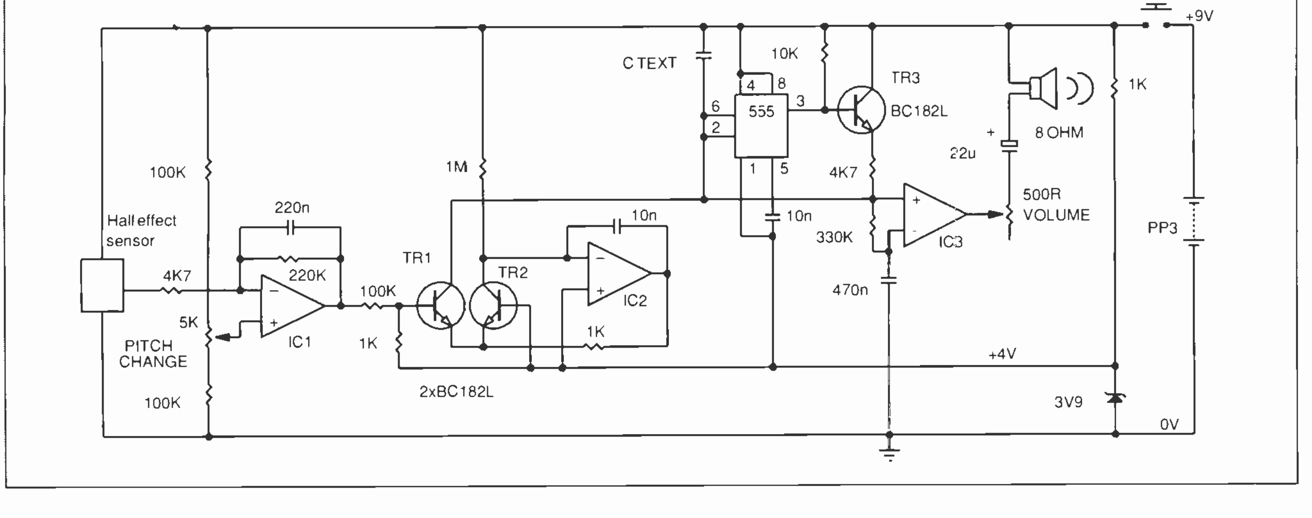
The sensor is an RS Components *Lohet II* Hall-effect chip, whose sensitivity is increased by the addition of 60mm x 9mm ferrite rods glued to its faces. Its output is amplified by IC_1 and taken to a voltage-to-current converter having an antilog characteristic, so that equal changes in input voltage give rise to equal changes in pitch, rather than in frequency. Transistors Tr_1, Tr_2 and IC_2 form the converter, Tr_1 being the current sink for the *555* current-to-frequency converter circuitry, whose output saturates IC_3 to drive the 40mm speaker.

To set up, adjust the pitch control and/or board orientation to obtain 4V at the output of IC_1. Then select C to give an output frequency of about 1kHz, which is two octaves above middle C.

The three op-amps are contained in one *LM324*.

W Gough
Department of Physics and Astronomy
University of Wales
Cardiff

Compass gives a tone output, its pitch indicating direction. Sensor is obtainable from RS Components.



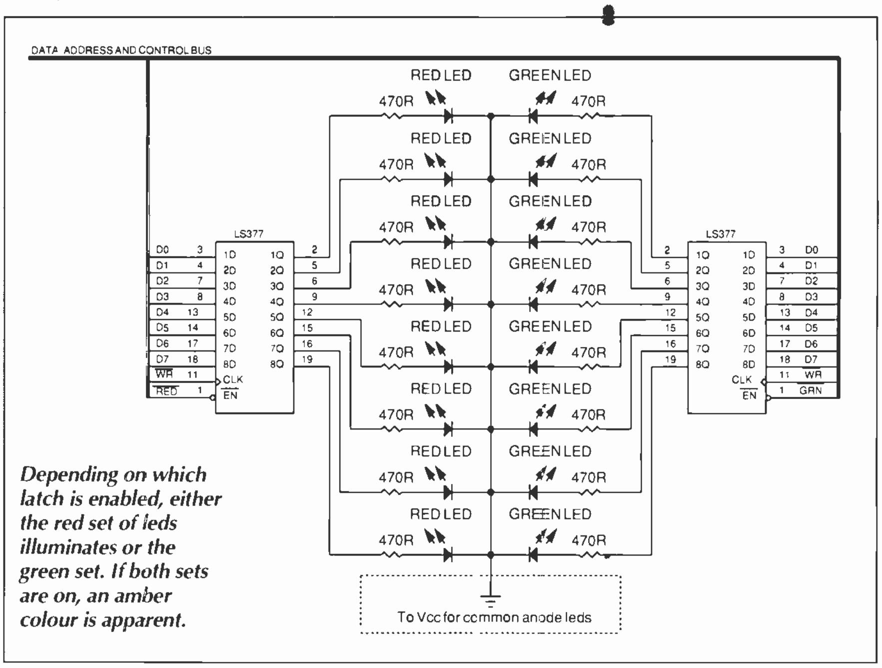
Three-colour bar graph

Using one package of green and red leds, you can get three colours — green, red and amber, the latter being a mixture of red and green used to display two sets of overlapping data.

Address lines A_0 and A_1 determine which of the sets of data from the bus is stored in the latches and whether red or green leds are on by activating port write pulses /PWR. If both A_0 and A_1 are low, both latches store the same data, all leds will be on and the colour will be amber.

Small mods to the address decoding circuit allows expansion of this idea to any number of led groups to make a bar-graph display.

J Vandana
World Friends Design Group
Tamilnadu India



Depending on which latch is enabled, either the red set of leds illuminates or the green set. If both sets are on, an amber colour is apparent.

Phase-linear crossover

This circuit, in which a low-pass, switched-capacitor filter is cascaded with an all-pass type, gives a tunable filter with a flat characteristic – a development originally due to Lipshitz and Vanderkooy. **Figure 1** shows the basics: a low-pass section and a high-pass characteristic obtained by a time delay and subtraction circuit. In practical designs, cascading a fourth-order Butterworth low-pass with a second-order all-pass equalises the attenuation and produces a phase-shift-free network, since an all-pass gives twice the phase shift of a low-pass of the same order.

This design uses the *ML2111* filter block; a universal, high-frequency (150kHz) dual filter consisting of two independent bi-quad switched-capacitor filters, used here in the configuration of **Fig. 2**. Two integrators are used, in which the resistance is simulated by switching a small capacitance to give

$$V_{out} = \frac{\omega_{CLK} C_u}{sC} V_{in} = \frac{\omega_{CLK}}{s} V_{in}$$

where C_u is the switched capacitor.

For the circuit of Fig.2,

$$V_1 = -\frac{R_2}{R_1} V_{in} - \frac{R_2}{R_3} V_4$$

$$V_5 = \frac{\omega_{CLK}}{s} V_4 = \frac{\omega_{CLK}^2}{s^2} V_3$$

$$V_3 = V_1 - V_2 = V_1 - V_5$$

Transfer functions of the universal filter are:

high-pass

$$\frac{V_3}{V_{in}} = -A\frac{s_o^2}{K_o}$$

low-pass

$$\frac{V_5}{V_{in}} = -A\frac{1}{K_o}$$

band-pass

$$\frac{V_4}{V_{in}} = -A\frac{s_o}{K_o}$$

where $s_0 = s/\ \ = j/\ _{CLK}$
$A = R_2/R_1$
and

$$K_0 = 1 + \frac{R_2}{R_3} s_0 + s_0^2$$

Advantages are clear: cut-off is easily set by varying clock frequency; Q can be chosen by selecting the value of R_3; gain depends on the values of R_2 and R_1 and can be set by varying R_1.

Figure 3 is the practical circuit, in which half the *ML2111* is a low-pass filter feeding the other half, the equaliser.

Kamil Kraus
Rokycany
Czechoslovakia

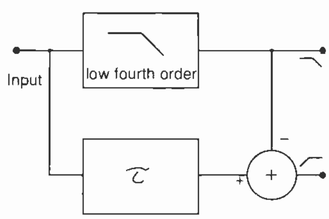


Fig.1. A phase-linear network with a low-pass section and a high-pass using time delay and subtraction.

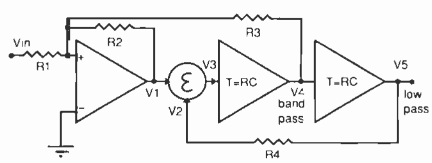


Fig.2. Configuration of ML2111 filter block, in which a resistor is simulated by a switched capacitor.

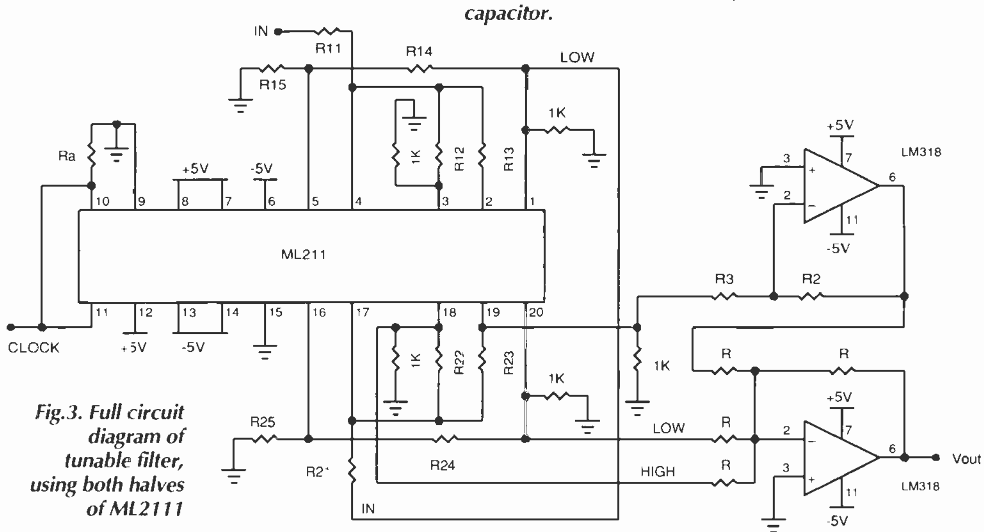


Fig.3. Full circuit diagram of tunable filter, using both halves of ML2111

DIY LSI

2: nuts and bolts

Continuing their series on using the new programmable logic families, Dave Nicklin* and Nick Sawyer* describe the main differences between FPGAs and EPLDs, both in terms of their respective architectures and design methodologies.

FPGA has a structure that can best be described as an "array-of-blocks" connected together via programmable interconnect. The amount of logic that each logic block can synthesise depends on which family of FPGAs is being used. Xilinx refers to its logic blocks as configurable logic blocks (CLBs) and the FPGA devices themselves are called Logic Cell Arrays (LCAs).

Structure of a CLB

The diagram, **Fig. 5**, shows the structure of the *XC4000* CLB. Each function generator (F and G) is a look up table that can implement any function of four variables. These may be optionally combined together via the smaller function generator (H) to provide various permutations of up to nine separate logic variables. For example, the logic in **Fig. 6** can all be mapped into one CLB. The worst case delay through a single CLB is between 4.5 and 7ns depending on the speed grade of the device. Compare this with the delay of the same logic when implemented in fast-TTL. The performance increase is obvious, and as all FPGAs use a cmos process they also have the advantage of drawing much less power.

A function generator is a circuit which can take a number of input variables and generate an output which is any Boolean function of its inputs. There are various ways in which a programmable function generator can be implemented. Xilinx LCAs use a series of lookup tables, whereas other manufacturers use multiplexers or modified AND-OR logic to achieve the same function.

CLBs also contain D-type flip-flops which allow the engineer to produce efficient synchronous designs. Many FPGA manufacturers do not have these dedicated flip-flops and have to construct them out of logic blocks, thereby reducing the resource available for the rest of the logic in the design.

Interconnect

The logic blocks within an FPGA are connected together via programmable interconnect much as discrete packages on a PCB would be connected together. The interconnect structure of LCA devices is composed of metal segments with programmable switching points to implement the desired connections.

An FPGA normally has either three or four types of interconnect mechanism. Adjacent logic blocks are connected via local interconnect, which is very fast. General purpose interconnect covers the rest of the device and is usually slightly slower due to the number of interconnect points in each section. The third

*Xilinx UK

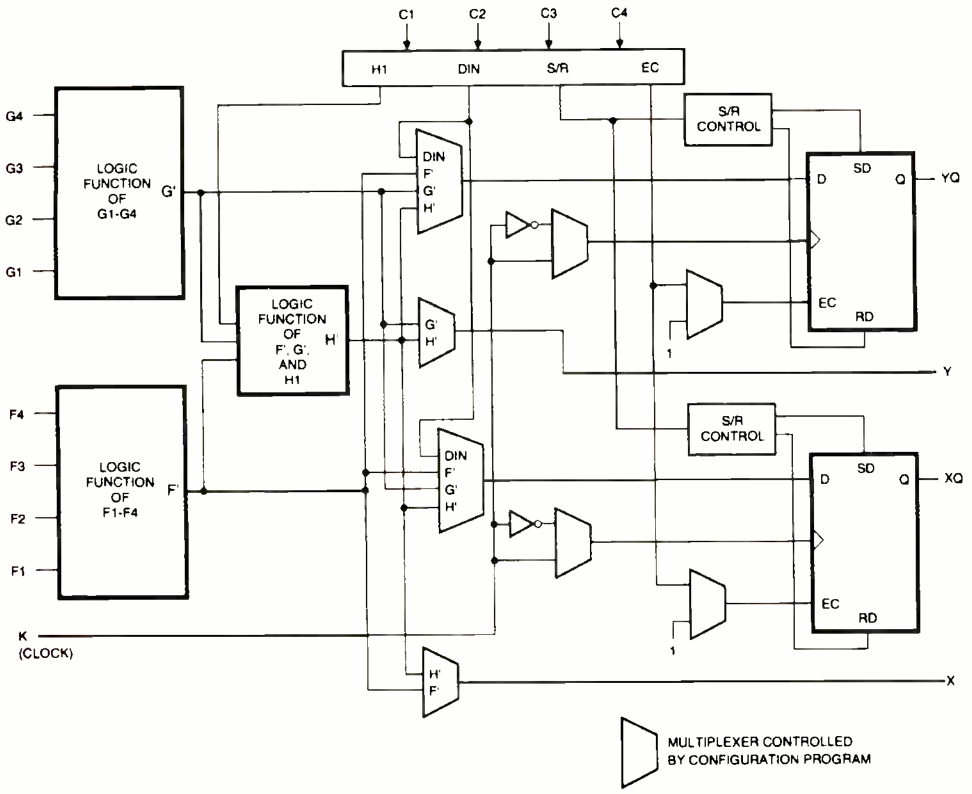


Fig. 5. Structure of an XC4000 configurable logic block. Each function generator (F and G) is a look up table that can implement any function of four variables. These may be optionally combined together via the smaller function generator (H) to provide various permutations of up to nine separate logic variables.

type of interconnect is formed by paths which allow signals to traverse the entire chip easily and rapidly. These are called Longlines and Global Interconnect. The diagram in **Fig. 7** shows some of the routing resources available in the *XC4000* family.

One analogy relates the FPGA interconnect scheme to the American road system. The direct interconnections are like the back streets round the block. They are fast but only connect over short distances before joining a main street. The main street is slower because of all the junctions onto it and crossing it, and for travelling longer distances it is often better to hop on the freeway i.e the longlines. These different types of available interconnect resource help make the routing of FPGAs to be both flexible and efficient. In fact, the interconnect scheme is one of the major differences between FPGAs and EPLDs.

► 1019

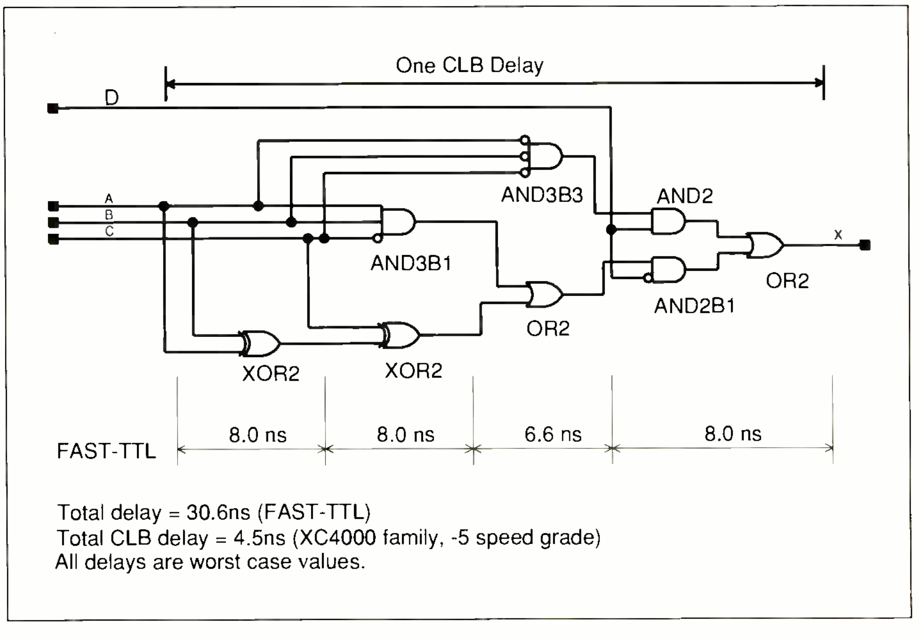


Fig. 6. Comparison of FAST-TTL and CLB delay. The worst case delay through a single CLB is between 4.5 and 7ns depending on the speed grade of the device. Compare this with the delay of the same logic when implemented in fast-TTL. The performance increase is obvious, and as all FPGAs use a cmos process they also have the advantage of drawing much less power.

COMPETITION

Win a programmable logic development system

In conjunction with this series, Xilinx is offering a complete development system worth around £5000 to the winner of a simple competition to challenge readers' ingenuity.

The prize includes the *DS502 LCA* development system, which caters for all of Xilinx FPGA families and the *DS550* development system, which caters for Xilinx *XC7200* family of EPLD devices. These will be bundled together with a *Viewdraw-LCA* schematic entry package, and the Xilinx *X-BLOX* logic synthesis package (which is to be described next month). The package will enable the winner to go from concept circuit to completed design using the bundled *XC4000* based evaluation board.

To enter, simply suggest the best use that can be made of the unique reprogrammability features that characterise the Xilinx sram based FPGAs. This should include suggestions for hardware that can be reconfigured either before or during operation. We look forward to receiving your suggestions, and please note that we are not looking for the best slogan to decide the winner in the event of a tie! However preference will be given to entries that perform a generally 'useful' function. It has been left to individual contestants to decide the degree of design detail presented in the competition entry.

All entries should be sent to Nick Sawyer or Dave Nicklin at Xilinx UK Ltd , Suite 1B, Cobb House, Oyster Lane, Byfleet, Surrey KT 14 7DU BY MARCH 17. We will choose the winner on the March 31 1993, and notify him/her soon after that date. The winning design will be published in the June 1993 issue of *EW + WW*.

Simple FPGA design

Following the examination of a typical pal based circuit last month, we offer a comparison built with FPGA of the sort that first emerged in the mid-eighties.

The circuit shown below is not dissimilar to the earlier example, but now uses the Xilinx *XC2018* to perform the logic functions. Other technologies have moved on as well. The system clock is now up to 8MHz, and the system memory is provided by 256K bit dynamic rams for data, and a 32K x 8 eprom for program storage. Once again the circuit is an imaginary protocol converter/buffer, but running at a much higher data rate, and therefore needing larger amounts of ram for storage. Because of the much higher data rates, the circuit requires data to be transferred out of the serial controller by DMA, and a very low CPU interrupt latency is required, ie the CPU needs to respond to, and act upon, an interrupt as soon as possible.

None of these concepts was new, but the idea of integrating all the required functions onto a single user programmable device was. As discussed last month, the only other course open to the designer requiring high circuit density was to produce a gate-array or other asic.

The circuit function consists of several distinct blocks of logic, which we will look at in turn to show the role of FPGA in the design process.

Address decoding. This function would normally be performed by either MSI logic or a pal as described last month, and is simply combinatorial logic. The FPGA provides the function by decoding the top four address lines, at a 'cost' of one logic block, i.e. CLB per address decode.

Memory Management. With the advent of high density memories the memory limit of 64K in 8-bit machines began to look a bit feeble. However most applications only had a requirement for larger areas of data rather than program storage. Some simple memory management techniques can therefore be used to get around the problem. In this design the 256K dram is considered as 16 pages of 16Kbyte each. Since we need one of these pages permanently enabled for things like stack storage, this takes up 16Kbyte of the memory map. The eprom requires 32K, so the remaining 16K of the logical map can be mapped 13 times into the dram. The technique to do this is very simple. A register in the FPGA is written with a four bit value indicating which of the pages is to be used. When an address in the logical page range that requires translation (e.g. 8000 to BFFF hex) is detected, then the value in the register is used to form the extra two bits of physical address which are required by the dram. Obviously the control code in the *Z80* will keep track of which page is used at all times. The circuit is easy to implement in the FPGA, which is rich in registers. A four-bit register is made from flip-flops to give read and write capability at a unique address in the i/o map; this also needs address decoding as described above (requirement five logic blocks). A comparator works on the top two bits of the address bus to see when translation is required (one logic block), and this controls four two-to-one multiplexers which generate the physical address for the dram (four logic blocks).

Dram control and refresh. Control of a dram consists of presenting the first half of the address on the address bus (in this case nine bits), and then activating an active low signal called RAS (Row Address Strobe). On the next clock the remaining nine bits of address are placed on the bus, and the CAS (column address strobe) is activated. The cycle is ended by pulling both RAS and CAS back high again. If the write line is low during this cycle, then data is written, if not then data is read.

The refresh timing is provided by the *Z80*, which has a special refresh cycle after each opcode fetch. However the *Z80* generates only seven bits of refresh address, and so two more bits have to be provided by a two bit counter within the FPGA (two logic blocks).

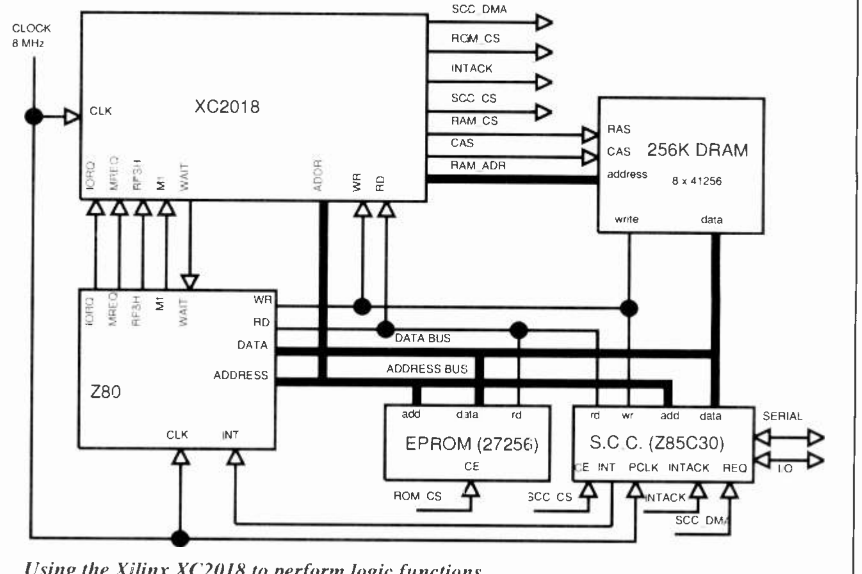
The RAS address, the CAS address and the refresh address are enabled onto the address bus for the dram at the appropriate points in time by nine four-to-one multiplexers. The spare input is for the DMA address described later. This function requires eighteen logic blocks for the multiplexers, and four logic blocks for the control circuitry.

Interrupt Acknowledge. The Interrupt Acknowledge function is very important to the response time of the CPU to an interrupt from the serial controller. The CPU can always go and read the SCC registers to see which potential source caused the interrupt, but it is much more efficient for the SCC to put a vector on the bus, and thus force the processor directly to the correct routine.

The logic necessary is not complicated, being a shift register that generates four wait states for the *Z80*, and a delayed read signal for the SCC, and is ideal to implement in the FPGA architecture taking four logic blocks.

Direct Memory Access. DMA is a way of transferring data from a peripheral to memory (or vice versa) in any computer system. The *Z80* family includes a DMA, but one of the advantages of the FPGA is that spare resource can be used to perform such functions. In this case the DMA is an eighteen bit up counter whose initial value is written by the *Z80*. When a DMA request occurs, data is taken from the SCC and written directly into memory on a flyby basis, ie the microprocessor is bypassed, and the transfer lasts only a single execution cycle. In order to "grab" the bus, the FPGA needs to persuade the micro to let go via a bus request signal (two logic blocks), and then enable the DMA acknowledge line to the SCC (one logic block) while generating a write address for the dynamic rams, using the multiplexers described above.

The required circuitry will easily fit into the chosen device, and leave some room over for expansion for any other logic functions that may be required. The example is simple, but hopefully illustrates the concepts and flexibility of the FPGA architecture. Next month's article will consider the same design based on EPLD.



Using the Xilinx XC2018 to perform logic functions

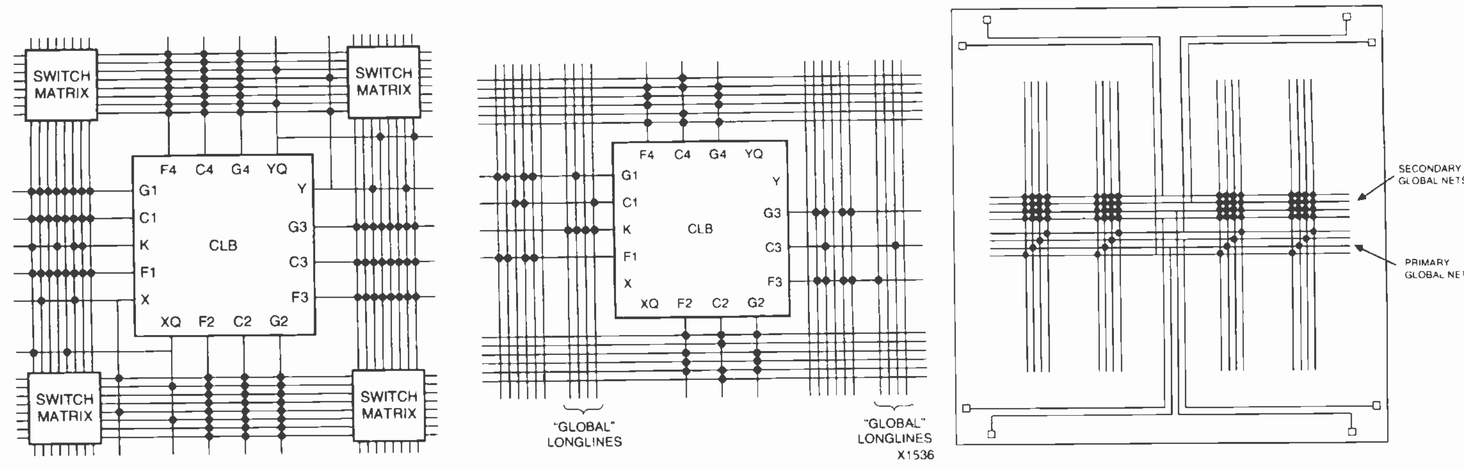


Fig. 7. Some of the routing resource available in the XC4000 family.

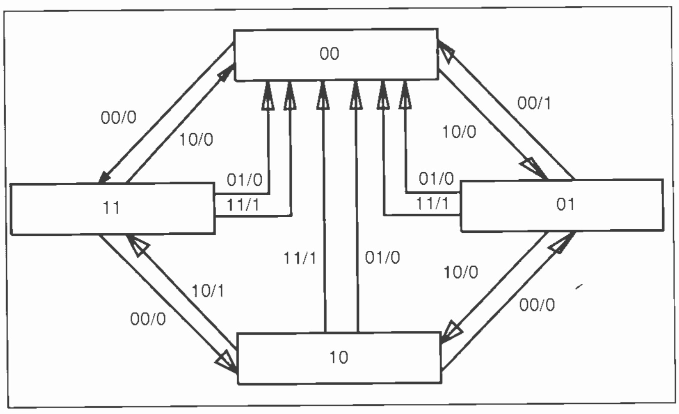
State machines - what are they?

State machines are systems that change from one (stable) state (the current state) to another state (the next state) after the application of a clock pulse. A state in this case is usually defined as being a certain set of registers holding a unique binary value. The next state is determined both by the current state, and the value of any inputs to the state machine.

Thus virtually any digital system with a clock (or clocks) can be considered a state machine, but there are normally too many variables for the designer to hold in his mind and design with. The design of a microprocessor is a very typical example of this: it may be defined mathematically in terms of its next state, but it is extremely cumbersome to do so. For this reason the day to day usage of 'state machine' is reserved for (usually) small, (usually) fast pieces of logic performing a clearly defined function.

One familiar state machine is the traffic light, though they often seem to use a very slow clock! The basic sequence of red to red and amber to green to amber and back to red is a very simple state machine, and can of course be modified by the lights on another junction, pedestrian push-buttons and various other options. (We hope that North American and European readers are not too confused by the concept of a red and amber state!)

In the world of digital electronics the classic example of the state machine is the binary counter. After a reset (state 0, say), the next required state is 1, then 2 etc. The last state in the sequence will then feed back to the first state, thus closing the loop and giving an infinite sequence. A counter state machine actually 'counts' by feeding back and logically combining the present outputs in a way that will generate the next desired value after the clock has occurred. The simplest form of counter is a divide-by-2 circuit using just one register or flip-flop (flip = state 0, flop = state 1) with its output fed back through an inverter to its input, thus causing a change to the other state every clock pulse.



In longer counters, the count length (i.e., number of possible states) will be determined by how many registers are present, and is given by 2^n. For example a four bit binary counter has up to sixteen states, five gives 32 states, etc. Now the counter example is all very well, but so far we have defined no real inputs; we are assuming that the counter will just move happily from one state to the next *ad nauseam*, and start again when it has finished. This is a useful circuit, but not very clever or efficient.

A typical counter will also have various other inputs to the state machine, such as a synchronous reset line, and a line to tell the counter whether to count up in binary, or to count down. It may also need other outputs such as a carry out for enabling another state machine. Outputs are generated by decoding the encoded output values. Referring now to the figure we can see the state drawing for the useful 2-bit binary counter (two bits was just chosen for clarity and brevity; longer counters are no more complicated). There are four states, represented by the four boxes which contain the encoded form of the current state, i.e. the current count. Movement between states is shown by the arrows, and the values next to the arrows are the values of the two inputs to our state machine, reset (RST) and up/down (UD), followed by the required output from the state machine, i.e. the carry (CARRY).

Thus if RST is ever one, the machine will move to state 0 with the output value of 0 or 1 depending on the value of the UD input, if UD is one, the machine will cycle clockwise, and if UD is low, it will cycle anti-clockwise. If we are counting up and reach state 3, then the CARRY line goes high indicating a carry is present, whereas if we are counting down, the CARRY line is required to go high at state 0 indicating that a borrow is required.

Shown below are the equations generated to satisfy the state diagram. These are written

Other features

The latest *LCA* devices incorporate more system level features, which are intended to assist system integration. For example, the *XC4000* has additional logic called "fast carry logic" which allows the designer to produce optimised arithmetic functions such as adders, subtracters, counters and accumulators. The additional logic is incorporated into each CLB on the device, and every CLB can be cascaded with its neighbour using dedicated high-speed interconnect. These are resource efficient because they remove the need to use the 'conventional' logic blocks to generate a carry signal, and they are fast because of the dedicated routing path.

The device CLBs also allow designers to access the function generator look-up tables directly and use them as fast ram. This means that fast fifos, parallel shift registers and small blocks of ram can also be incorporated efficiently into an FPGA based design. In fact, if rams are used in a design the effective capacity of the FPGA, measured in gate-array equivalent gates can easily exceed the usable gate figure which characterises the part. As an example, a long shift register can be implemented using a ram (eg 256 x 1), and a pair of counters. This is much more efficient than using the 256 flip-flops of a normal shift register, and will increase circuit density several-fold.

The EPLD Architecture

EPLD architectures differ markedly from FPGA. The devices themselves are mostly manufactured using a cmos eprom process and therefore dissipate more power than either sram or anti-fuse FPGAs. Their structure usually consists of a relatively small number (4 to 16) of large function blocks, each of which is effectively a high-end pal. The blocks are connected together via interconnect which provides 100% interconnectivity between each and every block and sub-block. The Xilinx EPLD architecture consists of four or eight function blocks, each of which contains nine sub-blocks called macrocells. It is the macrocells that contain the AND-OR logic typical of an EPLD. The function blocks are connected together by the universal interconnect matrix. **Figure 8** shows the EPLD structure of a Xilinx *XC7272* EPLD device which has eight function blocks.

The Function Block

Each function block in a Xilinx EPLD contains nine macrocells. There are 21 inputs to each block from the universal interconnect matrix (UIM), and these feed a programmable AND array. **Figure 9** shows the plan of a single function block. Each macrocell has five exclusive or private product terms which allow a degree of flexibility within each function block. There are also twelve product terms which are shared between all 9 macrocells in the function block. The product terms feed into a set of OR gates to produce the familiar "sum-of-products" expression which was detailed in last month's issue.

Most EPLDs have this basic structure in common, although the number of blocks available and the structure of the AND/OR array varies considerably between manufacturers.

The Xilinx EPLD incorporates an ALU in its macrocell. The ALU block can implement any function of two variables, as well as an ADD function with fast-carry. This enables the macrocell to implement fast adders and other arithmetic functions efficiently.

EPLD interconnect

Almost all EPLD devices provide 100% connection between each and every module, and i/o blocks. This allows EPLD manufacturers to characterise the maximum interconnect delay and combine it with the delay through the macrocell. Therefore the interconnect delay is effectively zero, but the logic block delays are longer than those for an FPGA. This characterisation allows the designer to know precisely the delay through each section of their logic design before committing to silicon. Timing simulation is therefore less of a necessity, and many engineers prefer to sacrifice some degree of flexibility, in order to have this level of control over their design's performance.

Every EPLD manufacturer provides a different style of interconnect architecture. Each interconnect scheme aims to improve the flexibility of routing, without losing the advantage of predictability. For example, the Xilinx UIM has a feature of being able to wire-AND signals which are commoned together on the same interconnect line. This means that very large product term functions can be made with zero effective delay. This is an especially useful feature for decode functions and for complex state-machine designs.

EPLDs are starting to appear in technologies other than eprom. There are a number of companies who have eeprom, and others are planning to develop flash components as well.

in a form of hardware description language called *ABEL* which is available from the CAE company Data I/O. We will discuss this method of data entry much more in the software section next month. Note the statement showing how the states are to be encoded in the registers.

```
module counter
title 'counter - encoded form'

"define the inputs
        clock,ud,rst            pin;

"define the outputs
        carry       pin istype 'com';

"define the internal nodes
        qa,qb       node istype 'reg';

"set up the state assignments
        count       =       [qb,qa];
        s0          =       [0,0];
        s1          =       [0,1];
        s2          =       [1,0];
        s3          =       [1,1];

"define some variables for the
carry output equation
        zero        = count     == s0;
        three       = count     == s3;

xilinx property 'initialstate zero';
equations

"define a clock
        count.clk =             clock;

"define the carry output
carry   = (zero & !ud) # (three & ud);

"define the state machine
state_diagram count

        state s0:  if (rst) then s0
        else if (ud) then s1
        else s3;

        state s1:  if (rst) then s0
        else if (ud) then s2
        else s0;

        state s2:  if (rst) then s0
        else if (ud) then s3
        else s1;

        state s3:  if (rst) then s0
        else if (ud) then s0
        else s2;

end
```

The example shown uses a small number of registers to encode the state value and is therefore known as the encoded state machine format. It is well suited to the pal and EPLD types of architecture which contain relatively few registers, and wide enough gates (high fan-in) to decode the feedback signals (remember that a single state in a 16-state machine, for instance, is encoded in four registers, and will always require a 4-input gate to decode it). The FPGA with a much higher number of registers and lower fan-in is far better suited to the symbolic or one-hot form of state machine. In this format, one register is used per state, and only one register can have a high output at any time, thus cutting down on the possible feedback combinations, i.e. to feedback a single state requires only one line.

Both data entry methods are equally valid. The counter can be implemented in either encoded or symbolic form according to the target architecture, and (to a certain extent) the efficacy of the logic optimisation software.

More about this subject next month.

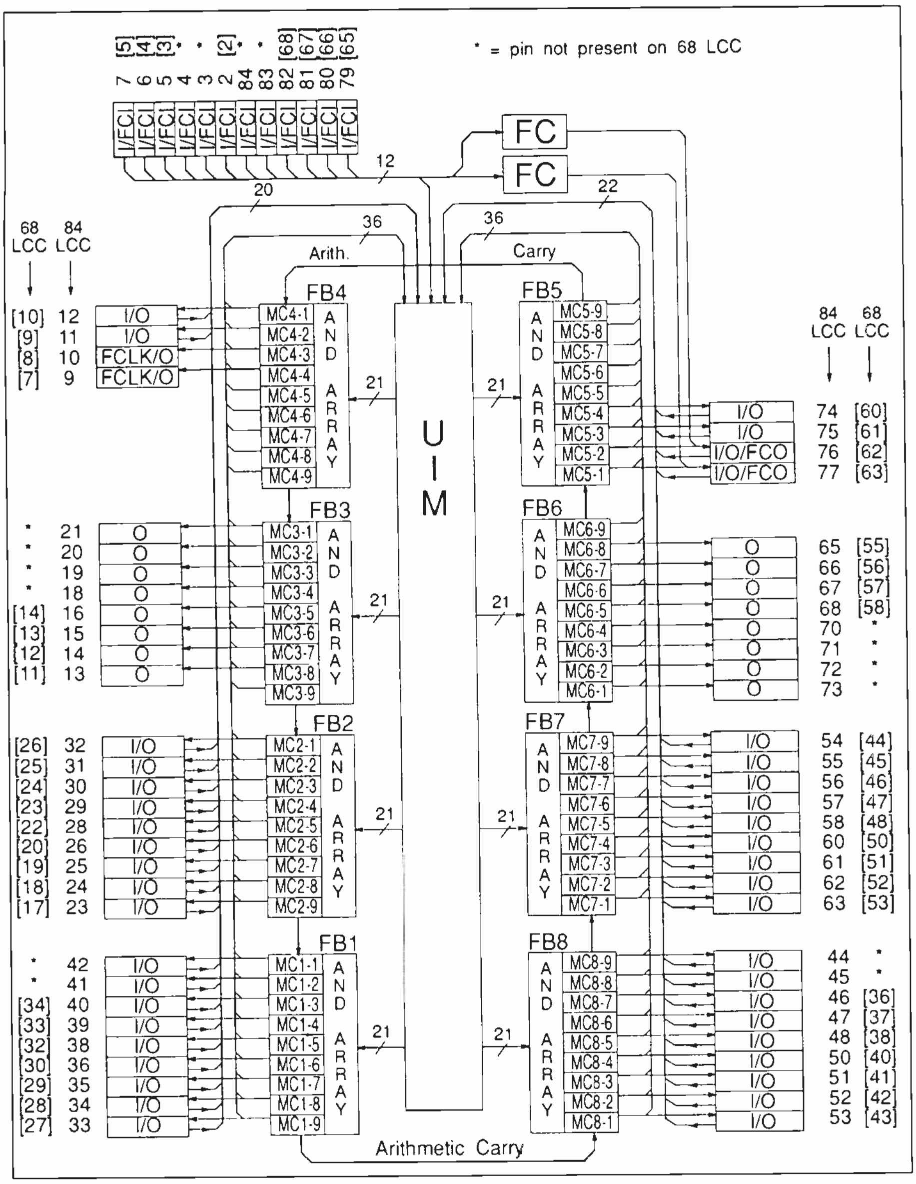


Fig. 8. A typical ELPD structure. This is the Xilinx XC7272 device.

These products consume less power than eproms, and may be programmed on-the-board, a major system feature.

Architectural comparisons

EPLDs pay for their predictability with a lack of flexibility. For example, if a designer has to use two macrocells in series to provide a particular function, then the configuration incurs a large delay. Also, if not all the terms in a macrocell are used, then much potential functionality has been wasted.

The logic blocks in the FPGA are smaller and quicker than those of the EPLD. But it is only after the blocks have been placed and the interconnect routed that all the path delays can be calculated and the design evaluated to see if the system performance requirements have been met. For these reasons, EPLDs lend themselves to regular, synchronous designs such as state machines, address decoders and large binary counters. FPGAs are ideal for register rich circuits, multi-level logic applications and fast pipelined designs.

The two market segments overlap in many areas, and work is being carried out to make each methodology more competitive with the other. These developments are being made both in hardware and software design. Some EPLD manufacturers are designing new families of devices which will have a variable level of predictability, depending on which type of interconnect is being used. For example, blocks connected vertically deliver a known propagation time, but connected horizontally will result in a different, unspecified delay. This approach is making the EPLD more like the FPGA.

Another approach uses software engineering to remove unpredictability over critical paths. The designer tells the software about the timing requirements of his design, such as clock-to-setup and pad-to-pad for the critical paths, and the logic is subsequently partitioned and routed to try and meet these requirements.

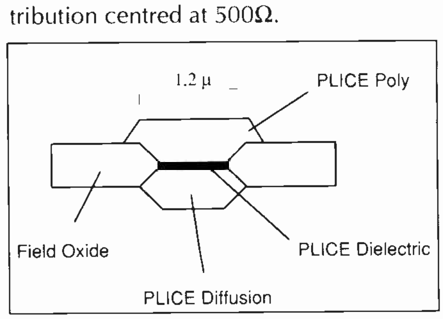
This example illustrates the extremely important role that the software plays in the design of FPGAs and EPLDs. In the next issue we shall explore the developments that are being made in software to exploit both products to their full potential. ■

Actel field programmable gate arrays

Actel has taken a different approach to building configurable logic with antifuse technology, a system which builds permanent circuit links in silicon. Although this may provide speed and density advantages, once programmed, a device cannot be erased and reprogrammed. Contrast this with an FPGA based on a static ram or eprom overlay technology.

The PLICE (programmable low impedance circuit element) antifuse is a dielectric-based element consisting of an oxide-nitride-oxide structure. The ONO antifuse, sandwiched between N+ diffusion and N+ polysilicon, is placed in a dense array limited only by metal pitches.

When a programming voltage is impressed across the normally open antifuse structure, the insulating layer breaks down and a bi-directional low-impedance connection is established by the formation of a polycrystalline structure between diffusion and polysilicon. By choosing a programming voltage, the antifuse can be programmed within one millisecond, and exhibits resistance distribution centred at 500Ω.



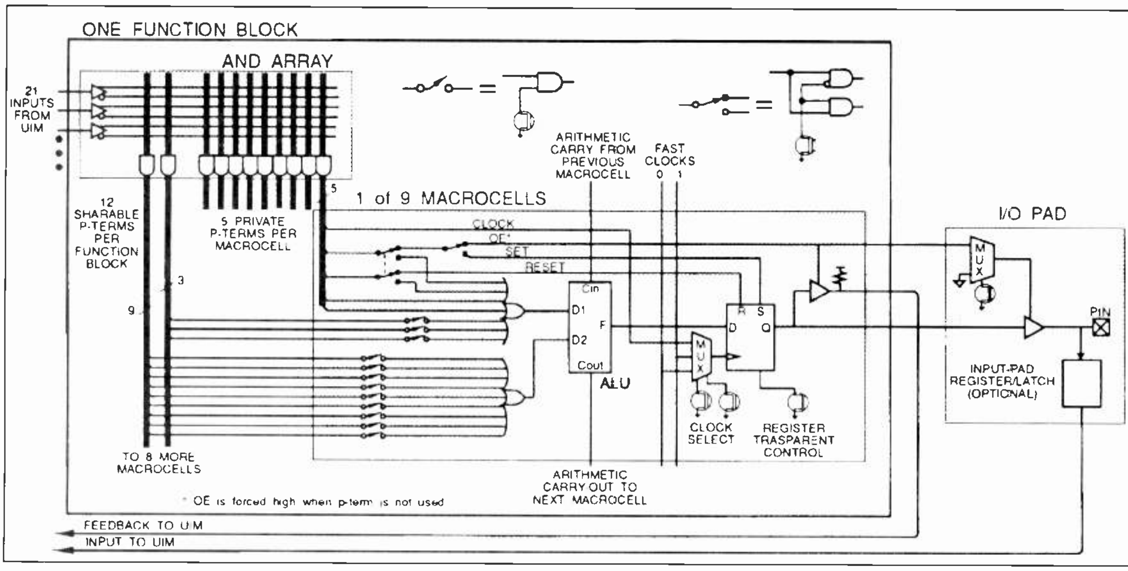


Fig. 9. An EPLD basic function block. Each macrocell has five exclusive or private product terms which allow a degree of flexibility within each function block. There are also twelve product terms which are shared between all 9 macrocells in the function block. The product terms feed into a set of OR gates to produce the familiar "sum-of-products" expression which was detailed in last month's issue.

Fabrication of the PLICE antifuse takes three additional mask steps on a conventional 12-mask, double layer metal, twin tub cmos technology. The antifuse element (see figure, left) has the area of a typical semiconductor contact or via and occupies 1.5μm² using a 1.2μm process.

Architecture

Actel FPGA architecture uses antifuse elements for electrically programmable interconnections. The architecture exhibits the familiar channelled gate array organisation – rows of fine granularity logic cells interspersed with routing channels. Where it differs from a traditional gate array is that instead of including an area for custom metalisation, the channels contain wiring segments of various lengths that can be connected to the required logic by the programmable low impedance antifuses.

This architecture consists of a logic module matrix arranged in rows separated by wiring channels. Within these wiring channels are segmented horizontal tracks. Vertical interconnect tracks span the rows of logic modules and horizontal wiring channels. PLICE antifuses located between track segments and at the intersections of the horizontal and vertical tracks, connect nets together and logic module inputs to outputs. During programming, antifuses are selectively programmed to complete the connections required by the circuit applications. The figure, right, details a section of Actel's field programmable channelled gate arrays showing a subset of the tracks, antifuse elements and interconnect architecture. Inputs to logic modules span the adjacent routing channels whereas outputs span two channels in either direction. In addition uncommitted vertical tracks span several rows of modules.

ACT1 Family

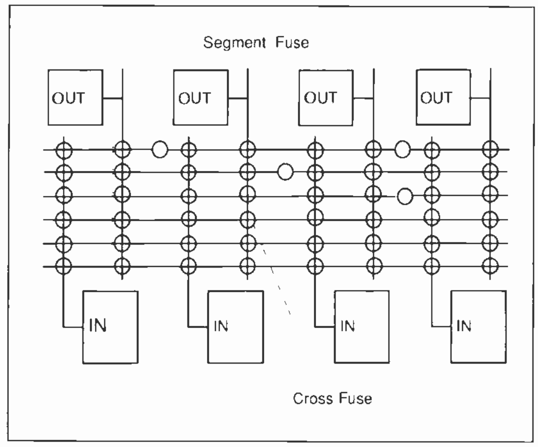
The first family of Actel FPGAs consists of two members, the *1010* and *1020* offering 1200 and 2000 gates respectively. The logic modules are all identical with eight inputs and one output. The basic functionality of the module is a 4 to1 multiplexer with a gate on one of the select inputs. This function allows implementation of basic logic functions by simply connecting relevant inputs to V_{CC} or Ground. Level sensitive latches are implemented in one module by applying feedback to the element. Edge triggered flip-flops are produced by combining two modules in a master-slave configuration.

ACT2 Family

The *ACT2* family provides devices up to 8000 gates, with 16-bit counter performance in excess of 80MHz, 16 bit accumulators over 30MHz and system level performance to over 50MHz.

The logic modules are again arranged in rows separated by fixed segmented routing channels. The logic modules have been enhanced slightly and consist of two types, Combinatorial (C Module) and Sequential (S Module). The C Module has been enhanced over the *ACT1* module to implement higher fan-in combinatorial functions such as 5-input AND, OR, NAND and NOR gates. In addition a wider range of AND-OR and AND-XOR gates are available in a single module. The S Module is optimised to implement high speed flip-flops and latches within a single module and includes combinatorial logic that allows an additional level of logic to be implemented without additional propagation delay. Table 2 indicates the main features of this family.

For highly combinatorial designs, the S module can function identically to the C module. For register intensive applica-



tions, two C modules can be combined to form an edge triggered macro like *ACT1* devices.

ACT3 Family

The *ACT3* family, with devices spanning capacities less than 1000 gates to more than 10,000, represents the third generation of Actel FPGAs. The devices offer an abundance of Inputs/Outputs ranging from less than 100 pins to over 200 pins. They are implemented in a silicon gate scalable 0.8μm double-metal cmos process and again employ antifuse technology.

The *ACT3* enhancements include four high speed clock distribution networks. The i/o module is enhanced significantly, allowing more complex logic functions to be implemented in the module. This significantly increases performance of key parameters like clock to output. Clocking flexibility is also enhanced over earlier families with the inclusion of two high speed dedicated clocks in addition to the two routed clocks found in *ACT2*.

Andrew Biddle, *Actel Europe Ltd*

Design it yourself linear asic

UK semiconductor company Zetex has used its new linear semicustom bipolar process to produce the first members of a standard product linear family. You too could be designing low cost, low volume linear asics. By Hans Camenzind and Dave Brotton*.

Fitting a bandgap voltage reference into an SOT23 package – which measures 0.84 x 0.84mm – requires a small chip. A knee current of 60µA requires large resistor values which consume chip area. Totally incompatible? A new Zetex linear asic array uses geometries small enough to fit into an SOT23 package. It has used its own *700 series* asic system to produce the *ZRA* family standard product voltage references using 19 transistors and 90kΩ of resistance.

The heart of any low-voltage reference is the bandgap circuit. This basically consists of an unbalanced transistor pair. Transistors Tr_1, Tr_2 and Tr_3 are connected in parallel and, together, they have six emitters. The right-hand side of the pair consists of only Tr_4, with a single emitter. The transistors being unequal, the pair has an offset voltage. Fortunately, this voltage is one of the rare parameters that is not dependent on the process: it depends only on the ratio of the emitter areas:

$$V_{BE1} - V_{BE2} = \frac{kT}{q}\log_n(A_1 / A_2)$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, q is the electron charge, and A_1/A_2 is the ratio of the two emitter areas. For 6:1 emitter ratio we get at room temperature:

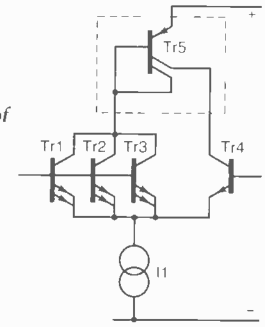
$$V_{BE1} - V_{BE2} = \frac{kT}{q}\log_n 6 \qquad = 46mV$$

This is a small voltage, but a useful one nevertheless. Note that, with T present in the equation, this voltage has a strong positive temperature coefficient.

The offset voltage is only exact if the collector currents in $Tr_{1\text{-}3}$ and Tr_4 are equal. This is the job of Tr_5, a dual collector PNP transistor (one of the many configurations made from the basic convertible transistor cell on the *700 Series* chips). It is connected as a current mirror: the collector current of $Tr_{1\text{-}3}$ is returned to the collector of Tr_4 without changing its magnitude.

We now take this small, temperature dependent offset voltage, put it across a resistor (R_1) and add more resistance at both ends (R_2 and R_3). If this resistor string is in a feedback loop, the voltage will adjust itself so that there is exactly 46mV across R_1 (only then are the currents of the transistor pair balanced). This means that all resistors together drop 46mV x 27 = 1.242V, still with the same positive temperature coefficient.

The *700* linear array includes only one value of (diffused) resistor: 750Ω. A single resistor gives consistent ratios. Different resistor values are created by parallel or series connection. In the diagram the resistor values are given as multiples of basic resistors, eg 13 is 13 x 0.75k = 9.75kΩ. Note, however, that the multiplied voltage does not depend on absolute resistance, only on ratios. (The reason we placed the additional resistance at both ends of R_1 is to give the transistors maximum operating headroom).



Bandgap circuit at the heart of any low-voltage reference.

Going for cancellation

Diodes have a negative temperature co-efficient and this parameter, too, is independent of the process, at least to the first order. In ICs, diodes are made from transistors, which also makes them more accurate. If we add two such diode-connected transistors and connect them in series with the resistor string, we get a cancellation of temperature coefficients. Exact cancellation only happens in integers of 1.25V – the bandgap voltage of silicon. Here we dimensioned the resistor ratio so that the delta V_{BE1}–V_{BE2} temperature coefficient cancels that of two diodes: thus the total voltage amounts to 2.5V.

A second PNP stage, Tr_8, and an NPN darlington output stage, Tr_9 and Tr_{10} close the feedback loop. Tr_{10} is a large transistor capable of handling up to 200mA, thus extending the current range by an order of magnitude over competitive devices.

Closing the feedback loop creates a potential stability problem. Though the feedback is neg-

DESIGN YOUR OWN LINEAR CHIP

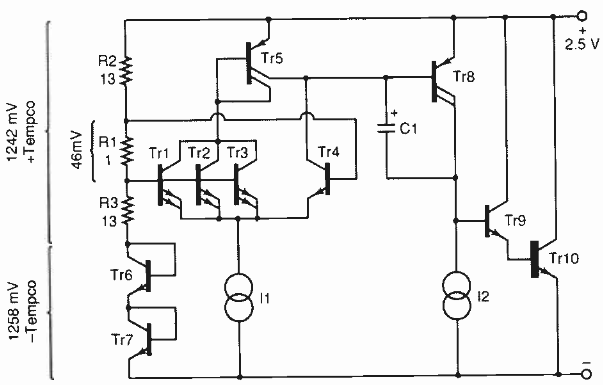
There are eight arrays in the *700* series. The smallest one fits into any SMD package from SOT23 upwards. The remaining seven chips form a smooth progression in size: each chip is approximately 30% larger in area than the previous one.

Each array contains the same basic components and is based on an identical architecture. In the centre portion of the arrrays are islands of 12 transistors each, 10 of which are covertible from NPN to PNP and two are Schottky NPN. These islands are surrounded by a field of resistors. The number of resistors and the total resistance is extra large which makes the IC easier to design. All devices are made with a relatively small geometry process returning a typical f_t of 800MHz and 20V operation.

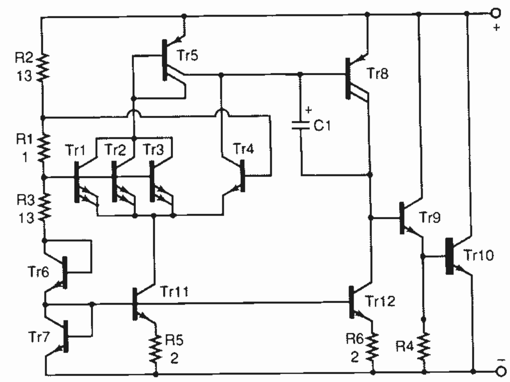
Between the bonding pads along the periphery are all other devices: large (200mA) npn transistors, 6mA PNP devices, high value resistors and junction capacitors. Sprinkled throughout each array are low value cross-under resistors.

Array design software runs on a standard *386* PC. Each semicustom chip made by the Zetex process has an associated non-recurring engineering charge of about £3000. Time to sampling is typically around four weeks. There is no low-volume limitation. A device can move to volume production in eight to ten weeks from initial design.

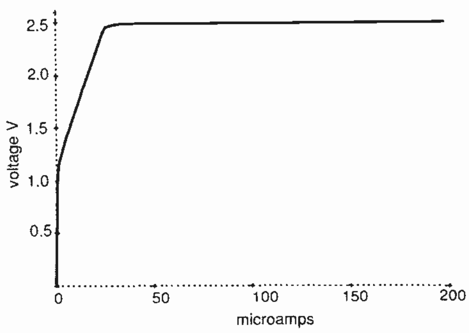
*Zetex



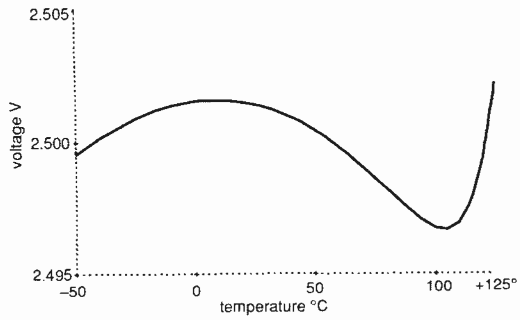
Closing the feedback loop with a bias string. The resistor values refer to multiples of 750Ω.



Adding the bias currents through current mirrors. The 200mA output transistor allows exceptional dynamic range for a bandgap reference.



Knee current of the reference – less than 40µA



Temperature performance as obtained by Spice analysis.

ative, each stage adds some delay and, at some frequency, the phase lag is large enough to cause the feedback to become positive. At this point the entire circuit oscillates provided that the loop gain is greater than unity. To prevent this from happening, C_1 is added, a 20pF junction capacitor, which rolls off the frequency response of the loop so that gain is less than one at an added phase shift of 180°.

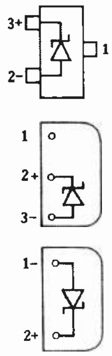
There is one further factor for consideration. There is a small error in the current mirror, Tr_5. The current delivered by Tr_{1-3} must supply the base current of Tr_5 and this portion of the current is not returned by Tr_5. For a lateral PNP transistor, h_{FE} can be as low as 40, giving an error of up to 5% in current, or 1.3mV in offset voltage. We can remedy this by having Tr_8 operate at exactly the same current as Tr_5 (I_1=I_2), in which case Tr_8 takes as much current from the right side as Tr_5 takes from the left.

The circuit shows how this is accomplished. Transistors Tr_{11} and Tr_{12} derive their currents from Tr_7 and their currents are lowered by emitter resistors. As long as resistors and transistors are identical, the two currents match. In this diagram we also added a "pinch" resistor (R_4, a less accurate, but higher value resistor) to divert leakage current from the base of Tr_{10} at high temperature.

The final circuit diagram shows something else: there is only one resistor string, ie the multiplication of the offset voltage and the generation of the bias currents are performed by the same resistors. In addition their values need not be exceptionally high because they are only connected across approximately half the total voltage. Thus, with less than 90kΩ of resistance, we were able to achieve a knee current which is significantly below that of competitive devices.

Model design

Good models help considerably in the design of this type of circuit. Circuit analysis programs such as PSpice allow the voltage to be plotted directly against temperature. You run the analysis several times, varying R_2 (or R_3) until the curve no longer has a tilt to it. You will notice the characteristic bow in the curve plus an increase at the high-temperature end. The latter is noticeable primarily with low-current circuits, when leakage currents start introducing small errors. We find that, with our refined models, we can predict a bandgap voltage within 50mV and the temperature coefficient within 50ppm/°C. With what many people consider to be a limitation of a semi-custom chip, we were able to design a voltage reference device – the ZRA250 – which exceeded the performance of full-custom alternatives for every parameter. ■

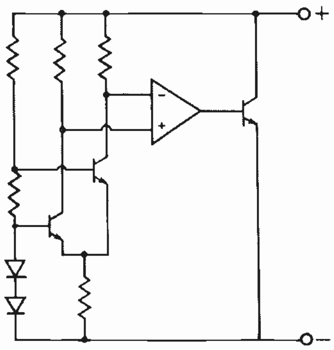


Pinout diagrams

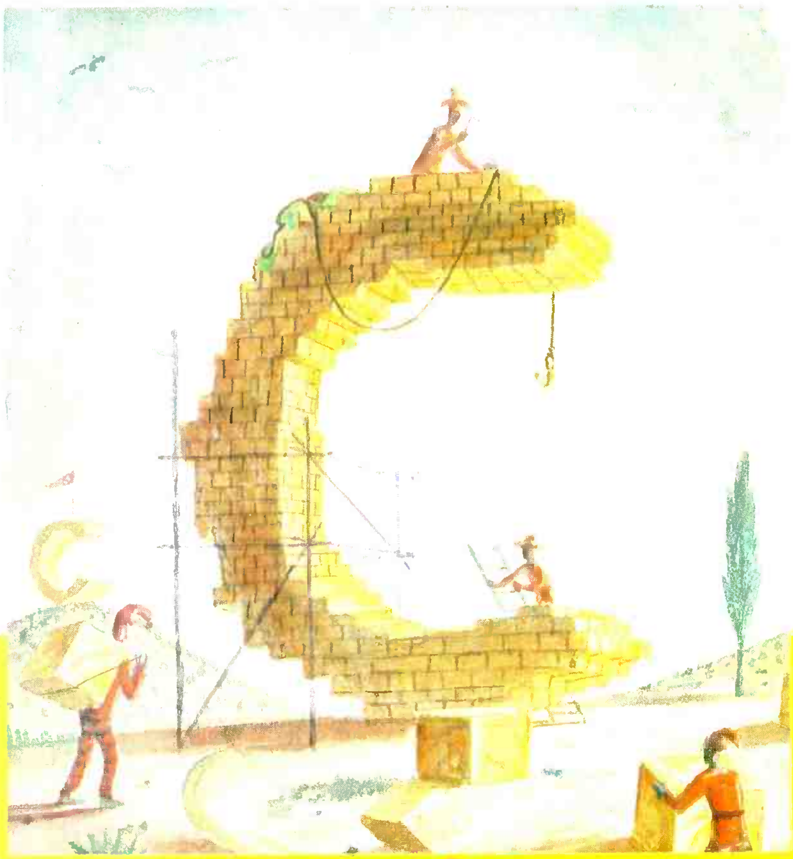
SO23

E-line 3 pin

E-line 2 pin



Functional circuit diagram of ZRA series bandgap voltage references.



The series of articles "Interfacing with C" by Howard Hutchings presented the basics of interfacing C with real world signals. ***John Edwards*** *examines some of the technical points raised in the original series and extends them further.*

EXTENDED C INTERFACING

Revised software listings featured in this article are now included on the *"Interfacing with C"* disc.

See page 1031 for details.

This article follows on from practical application of the programs and theories presented in the original series of articles. Dr Hutchings excellent series dealt with many difficult but crucial topics, some of which deserve further explanation. In addition to presenting the modified and extended versions of the originals, this article also presents another aspect of digital signal processing not covered in the original article: adaptive filtering.

Referring to the original series, the first chapter deals with memory and i/o space. *Listing 1* specifically says *reading i/o space, using pointers*. The *80X86* architecture has two external, though somewhat intertwined systems: the memory bus, in which all program and data resides, and the i/o bus which is used for peripherals in the case of the PC. Each bus is designed to meet a particular requirement. The memory map can be accessed via pointers and segment/offset registers, while the i/o map is accessed via specific input and output machine code instructions (in and out).

C pointers do not call the input and output functions and neither can the input and output functions access memory. For these reasons *listing 1.1* does not read peripherals' i/o bus and though it may be safe when reading data, could potentially be disastrous when writing to memory.

As an explanation, the PC, when it loads a program, will relocate it to the most appropriate memory area and indeed a single program, when run twice, can be loaded to two different memory areas. Therefore if a program were to write to a fixed location in memory without first checking as the example does, it could overwrite any part of the program or operating system. Anyone who has written programs to write directly to the memory map like this will appreciate that a lack of care could end with disastrous consequences.

A further situation that could potentially cause bugs concerned buffer allocation on the stack. Several of the examples in the series declared arrays locally to a function. This action places them on the stack, not always a good idea, because Microsoft C uses a default stack size of 2048 bytes. Several of the examples use multiple local buffers of 1024 floating point words (4096 bytes), plus several other variables and structures. Although the stack easily overflowed, all the examples can and do run. The reason they appear to run correctly is that heap and program space is generally allocated from the opposite end of a memory segment to the stack. When you want to use the examples in a real application, the code and heap space will grow and very soon meet the stack in the middle. Although the system may run several times before crashing, the program will be impossible to debug because the compiler or linker will not be able to warn of potential problems.

In most C compilers there is a command line switch to increase the stack size but a fairly major point about using the stack is that it takes time during the function call to initialise it, the stack being accessed via indirect memory references. Program execution is much more efficient if the array is declared global and pointers are used. Many sources will indicate that this is not necessarily good programming style; real signal processing systems with compact code demand performance as a higher priority.

The Discrete Fourier Transform example, *program 6.1*, showed the application of the principle in analysing real world signals via synthesized data. Following the DFT was a description of the theory behind the FFT, which leads into the code for the FFT itself. The first thing that struck me about the output of the FFT was that it was totally out of scale for the input. In order to discover the cause it was necessary to take a step back and feed in the known source data into the DFT examples and compare the FFT results with the known output of the DFT. The FFT result appeared wrong and the program frequently crashed out into dos.

Code debugging used some simple techniques to print out successive results; the appropriate lines of code still remain in the modified version to show how they were used. The debug statements were surrounded by an IFDEF(), ENDIF() pair and if DEBUG is defined at the top of the program or on the compile command line, the PRINTF() statement outputs successive results to the screen, bin by bin, so that errors can be spotted and bugs removed.

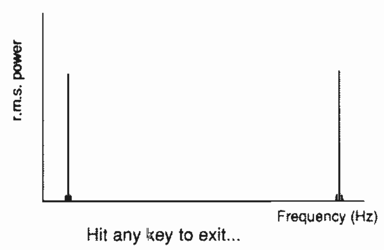
The largest source of the error derived from the most fundamental of C programming mistakes: *C array offsets start at 0 not 1*. This error is typical when the original source of a program is *Basic* or, more often in DSP, *Fortran*. The array indexing, for loops and conditional branches were modified to remove the bug, and code worked with the test data. The importance of this is that if a 128 point array for example is indexed from 1 instead of 0, the last sample will in fact be the next variable or array, which will get overwritten after 128 points.

Another potential source of error concerned the basic programming rule: *use meaningful names for variables*. The names chosen had no relation to the actual use of the variable.

Example 1

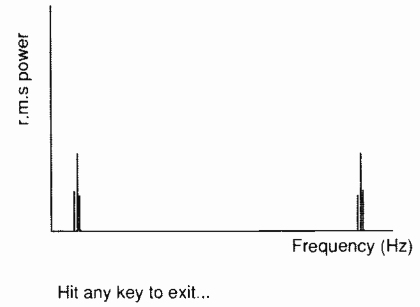
```
/* 128 point FFT program */
#include <stdio.h>
#include <math.h>
#include <graph.h>
#include <conio.h>
#include <stdlib.h>

#define     PI                          3.14159
#define     FFT_SIZE    128
double      ar[FFT_SIZE], ai[FFT_SIZE];   /* Real & Imag data
                                          arrays */
double      sine[FFT_SIZE], cosine[FFT_SIZE];   /* Sin &
Cos                                             table
arrays */
struct      videoconfig   screen_size;

void main(void)
{
int         a, d, f, g, h, graph_y;
int         u, i, j;
int         m, r, s;                      /* Bit twiddling
                                          registers */
int         transform_size;
double      theta_inc, theta, k, l, log2size, co, si,
            mean_sq_power, rms;
double      real_sum, imag_sum;

transform_size = FFT_SIZE;   /* Set FFT size */
log2size = log10(FFT_SIZE)/log10(2);          /* Log2 FFT_SIZE */
/* Config video mode and draw axis */
_setvideomode(_DEFAULTMODE);
_setvideomode(_HRES16COLOR);
_clearscreen(_GCLEARSCREEN);
_setbkcolor(_GRAY);
_getvideoconfig(&screen_size);
_setlogorg(screen_size.numxpixels/4, screen_size.numypixels/2);
_moveto       (0, 0);
_lineto (320, 0);
_moveto       (0, 0);
_lineto (0, -90);
_settextcolor (3);
_settextposition (4, 8);
_outtext ("r.m.s. power");
_settextposition (14, 50);
_outtext ("Frequency (Hz)");

for (i = 0; i < FFT_SIZE; i++) {  /* Synthetic signal */
            ar[i] = sin(19.9*PI*i/FFT_SIZE);
            ai[i] = 0.0;
            }
theta_inc = 2.0 * PI / FFT_SIZE;
a = FFT_SIZE;
for (i = 0; i < (int)log2size; i++) {
            d = a;
            a = a/2;
            theta = 0;
            for (f = 0; f < a; f++) {
            co = cos(theta);
            si = sin(theta);
            theta += theta_inc;
            for (u = 1, g = d; g <= transform_size; g = u*d) {
                        u++;
                        h = g-d+f;
                        j = h + a;
                        k = ar[h] - ar[j];
                        l = ai[h] - ai[j];
                        ar[h] = ar[h] + ar[j];
                        ai[h] = ai[h] + ai[j];
                        ar[j] = co*k + si*l;
                        ai[j] = co*l - si*k;
                        }
            }
            theta_inc *= 2.0;
            }
                        /* Reorder scrambled data */
for (r = 0, m = 0; r < transform_size; r++) {
            if (r < m) {
            k = ar[m];
            l = ai[m];
            ar[m] = ar[r];
            ai[m] = ai[r];
            ar[r] = k;          ai[r] = l;
            }
            s = transform_size/2;
            while ((s <= m) && (s >= 1)) {
            m -= s;
            s /= 2;
            }
            m += s;
            }
_setcolor (14);
for (i = 0; i < transform_size; i++) {
                        /* Draw results */
            real_sum = ar[i]/FFT_SIZE;
            imag_sum = ai[i]/FFT_SIZE;
            mean_sq_power = real_sum*real_sum +
                        imag_sum*imag_sum;
            rms = sqrt(mean_sq_power);
                        /* Square root improves graphic
                        display */
            graph_y = (int)(320.0 * ((double)i)/FFT_SIZE);
            _moveto       (graph_y, 0);   /* Scale and plot o/p */
            _lineto (graph_y, ((int)(-100.0 * rms)));
#ifdef DEBUG
            _settextposition (22, 20);
            printf ("real = %f, imag = %f", ar[i], ai[i]);
            while (!kbhit())
            ;
            getch();
#endif
            }
_settextposition (20, 20);
_outtext ("Hit any key to exit...");
while (!kbhit())
            ;
getch();
_setvideomode(_DEFAULTMODE);
exit (0);
}
```

Output results from listing 1.



Example 2

```
/* 128 Point Real FFT */
#include <stdio.h>
#include <math.h>
#include <graph.h>
#include <conio.h>
#include <stdlib.h>

#define     FFT_SIZE      128
#define     HALF_FFT_SIZE           64
#define     FLOAT_FFT_SIZE          128.0
#define     LOG2SIZE      7
#define     PI            3.14159
#define     SINE_TABLE_SIZE         HALF_FFT_SIZE
struct      videoconfig   screen_size;

double      window_table[FFT_SIZE];
double      sine[SINE_TABLE_SIZE],
cosine[SINE_TABLE_SIZE];  /* Sin & Cos table arrays */
double      ar[FFT_SIZE], ai[FFT_SIZE];  /* Real & Imag data
                                            arrays */
void main(void)
{
int         i, j, k, num_bflys, bfly_cntr, g, h, u;
int         angle, angle_inc;          /* Angle to step thro
                                          sin & cos tables */
double      real_tmp, imag_tmp;
int         graph_y;
double      real_sum, imag_sum;
double      theta_inc, theta, co, si, mean_sq_power, rms;
double      *rp, *wp;

/* Config video mode and draw axis */
_setvideomode(_DEFAULTMODE);
_setvideomode(_HRES16COLOR);
_clearscreen(_GCLEARSCREEN);
_setbkcolor(_GRAY);
_getvideoconfig(&screen_size);
_setlogorg(screen_size.numxpixels/4, screen_size.numypixels/2);
_moveto     (0, 0);
_lineto (320, 0);
_moveto     (0, 0);
_lineto (0, -90);
_settextcolor (3);
_settextposition (4, 8);
_outtext ("r.m.s. power");
_settextposition (14, 50);
_outtext ("Frequency (Hz)");

for (i = 0; i < FFT_SIZE; i++) {  /* Synthetic real signal */
            ar[i] = sin(19.9*PI*((double)i)/FLOAT_FFT_SIZE);
            ai[i] = 0.0;
            }

theta_inc = 2.0 * PI / FLOAT_FFT_SIZE;
angle_inc = 1;

                              /* Generate Sine and Cos tables */
for (i = 0, theta = 0.0; i < SINE_TABLE_SIZE; i++, theta +=
theta_inc) {
            cosine[i] = cos(theta);
            sine[i] = sin(theta);
            }
                              /* Generate window table */
for (i = 0, theta = 0.0; i < FFT_SIZE; i++, theta += theta_inc)
            window_table[i] = 0.5*(1-cos(theta));         /*
Hanning window */

                              /* Apply window to real data */
rp = ar;
wp = window_table;
for (i = 0; i < FFT_SIZE; i++)
            *rp++ *= *wp++;

num_bflys = HALF_FFT_SIZE;
angle = 0;
h = 0;
j = HALF_FFT_SIZE;
                                        /* First stage */
for (bfly_cntr = 0; bfly_cntr < num_bflys; bfly_cntr++) {
            co = cosine[angle];
            si = sine[angle];
            angle++;
            real_tmp = ar[h] - ar[j];
            ar[h] = ar[h] + ar[j];
            ar[j] = co*real_tmp;
            ai[j] = si*real_tmp;
            h++;
            j++;
            }

angle_inc = 2;
for (i = 1; i < (LOG2SIZE - 1); i++) {            /* Middle stages */
            k = num_bflys;
            num_bflys >>= 1;
            angle = 0;
            for (bfly_cntr = 0; bfly_cntr < num_bflys; bfly_cntr++) {
            co = cosine[angle];
            si = sine[angle];
            angle += angle_inc;
            for (g = k, u = 1; g <= FFT_SIZE; g = u*k) {
                        u++;
                        h = g-k+bfly_cntr;
                        j = h + num_bflys;
                        real_tmp = ar[h] - ar[j];
                        imag_tmp = ai[h] - ai[j];
                        ar[h] = ar[h] + ar[j];
                        ai[h] = ai[h] + ai[j];
                        ar[j] = co*real_tmp - si*imag_tmp;
                        ai[j] = co*imag_tmp + si*real_tmp;
                        }
            }
            angle_inc <<= 1;
            }

                                        /* Last stage */
for (h = 0, j = 1; h < FFT_SIZE; h += 2, j += 2) {
            real_tmp = ar[h] - ar[j];
            imag_tmp = ai[h] - ai[j];
            ar[h] = ar[h] + ar[j];
            ai[h] = ai[h] + ai[j];
            ar[j] = real_tmp;             /* Cos = 1, sin = 0 */
            ai[j] = imag_tmp;
            }

                                        /* Reorder
                                        scrambled data */
for (j = 0, i = 0; j < FFT_SIZE; j++) {
            if (j < i) {
            real_tmp = ar[i];
            imag_tmp = ai[i];
            ar[i] = ar[j];
            ai[i] = ai[j];
            ar[j] = real_tmp;
            ai[j] = imag_tmp;
            }
            k = HALF_FFT_SIZE;
            while ((k <= i) && (k >= 1)) {
            i -= k;
            k >>= 1;
            }
            i += k;
            }
_setcolor (14);
for (i = 0; i < FFT_SIZE; i++) {
                        /* Draw results */
            real_sum = ar[i]/FFT_SIZE;
            imag_sum = ai[i]/FFT_SIZE;
            mean_sq_power = real_sum*real_sum +
                        imag_sum*imag_sum;
            rms = sqrt(mean_sq_power);
                        /* Square root improves graphic
                        display */
            graph_y = (int)(320.0 *
                        ((double)i)/FLOAT_FFT_SIZE);
            _moveto     (graph_y, 0);    /* Scale and plot o/p */
            _lineto (graph_y, ((int)(-100.0 * rms)));
#ifdef DEBUG
            _settextposition (22, 20);
            printf ("real = %f, imag = %f", ar[i], ai[i]);
                        while (!kbhit())
            ;
            getch();
#endif
            }
_settextposition (20, 20);
_outtext ("Hit any key to exit...");
while (!kbhit())
            ;
getch();
_setvideomode(_DEFAULTMODE);
exit(0);
}
```



Output from listing 2.

Example 1 shows the modified program which was verified against the data for the DFT. This is by no means optimal, but is functional. A typical example of the easy optimisation possible was to generate a sine and cosine table at the start of the program and use this rather than the sin() or cos() functions to generate the twiddle factors when performing the FFT.

Example 2 has been optimised to produce practical code. It executes a real FFT algorithm[1]. To give some idea of efficiency, it has been used in a real application using a *TMS320C30* floating point DSP, processing data at up to 35kHz. This is about one fifth the speed of an optimised assembler version.

The theory of processing real data is similar to processing complex (real+imaginary) numbers: because the input data has no complex part there are computational savings since not all the points need to be computed. The non-computed points do not need to be saved so there are storage savings as well.

The real data, unlike the imaginary data, of the FFT is symmetrical about zero frequency and therefore any point (k) of an N point FFT can be computed using samples $0 <= k <= N/2$, ie only using half the data. Example 2 has been adapted from an IEEE paper on the subject of real FFTs[1], but the maths is not for the faint hearted. As a matter of personal interest the reader may care to compare the processing efficiencies of the examples in this article with the originals although these examples are not fully optimised by any means.

In addition to the FFT, the real FFT example also performs a Hanning window on the data. The effect can be compared to other window functions by simply changing the equation that initialises the window.

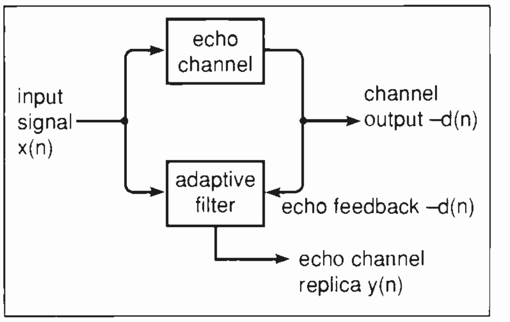


Fig. 1 Block diagram of the adaptive filter demonstration program.

Example 3

```
/* 128 Point LMS Adaptive filter test program */
#include <stdio.h>
#include <math.h>
#include <graph.h>
#include <conio.h>
#include <stdlib.h>
#include <time.h>

/* Declare constants */

#define     LMSSTEPSIZE         0.02
#define     LMSLENGTH   128
#define     ECHOLENGTH          128
                        /* Initialise echo path filter coefficients */
double      echopathtaps[ECHOLENGTH] = {
    -5.34266824816E-0004, 1.24568792546E-0003, 8.73278953630E-0004,
    4.37786545396E-0004, 1.57576481250E-0003, -1.38557006660E-0003,
    1.90710297624E-0004, -1.85794214656E-0003, -2.00704829381E-0003,
    2.40455797115E-0004, -2.04022181601E-0003, 2.71242012844E-0003,
    8.82181294290E-0004, 2.06390803758E-0003, 3.46115122350E-0003,
    -1.75033817834E-0003, 1.86645226647E-0003, -4.19706616768E-0003,
    -2.84686649762E-0003, -1.38480747151E-0003, -4.84877083488E-0003,
    4.15691399504E-0003, -5.59004695862E-0004, 5.33078655121E-0003,
    5.64663098926E-0003, -6.64415849217E-0004, 5.54512386900E-0003,
    -7.26170537971E-0003, -2.32956984257E-0003, -5.38280517195E-0003,
    -8.92656985171E-0003, 4.46954409718E-0003, -4.72452163230E-0003,
    1.05439735389E-0002, 7.10658444744E-0003, 3.43906801399E-0003,
    1.19942117579E-0002, -1.02552167173E-0002, 1.37716894902E-0003,
    -1.31325730564E-0002, -1.39301212180E-0002, 1.64388322268E-0003,
    -1.37820329052E-0002, 1.81624192809E-0002, 5.87454453127E-0003,
    1.37146029376E-0002, 2.30328314183E-0002, -1.17097244170E-0002,
    1.26049642763E-0002, -2.87440911303E-0002, -1.98723865258E-0002,
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    -2.04022181601E-0003, 2.40455797115E-0004, -2.00704829381E-0003,
    -1.85794214656E-0003, 1.90710297624E-0004, -1.38557006660E-0003,
    1.57576481250E-0003, 4.37786545396E-0004, 8.73278953630E-0004,
    1.24568792546E-0003, -5.34266824816E-0004
            };
double      oldlmstaps[LMSLENGTH];
double      lmstaps[LMSLENGTH];
double      echopath[ECHOLENGTH], lmsfilter[LMSLENGTH];
int         echostart_index, lmsstart_index, lmsfiltstart_index;

void        main(void);
double      fir_filter (double);
double      lms_filter (double);
void        lms (double);
struct      videoconfig    screen_size;

double      *lmstaps_ptr, *lmsstate_ptr;double        *echopathtaps_ptr, *echopathstate_ptr;
int         i;
double      data, replica, echo, error, lmsstep;
int         graph_y;

            .
void main(void)
{
            /* Initialise the LMS filter array to 0 */
for (i = 0; i < FILTER_SIZE; i++) {
            lmstaps[i] = 0.0;
            }

srand ((unsigned int) time);    /* Randomise the seed */
/* Config video mode and draw axis */
_setvideomode(_DEFAULTMODE);
_setvideomode(_HRES16COLOR);
_clearscreen(_GCLEARSCREEN);
_setbkcolor(_GRAY);
_getvideoconfig(&screen_size);
_setlogorg(screen_size.numxpixels/4, screen_size.numypixels/2);
_moveto     (0, 0);
_lineto (320, 0);
_moveto     (0, 0);
_lineto (0, -90);
_settextcolor (3);
_settextposition (4, 8);
_outtext ("Tap value");
_settextposition (16, 60);
_outtext ("Filter Tap");
                        /* Init pointers to cata */
echopathstate_ptr = echopath;
echopathtaps_ptr = echopathtaps;
lmstaps_ptr = lmstaps;
lmsstate_ptr = lmsfilter;
lmsstart_index = 0;
lmsfiltstart_index = 0;
echostart_index = 0;
_setcolor (14);
_settextposition (20, 2);
_outtext ("Hit any key to exit...");
while (!kbhit()) {
            cata = (((double)rand()) - 16383.0) / 16383.0;
            echo = fir_filter (data);       /* Apply echo path
            filter */
```

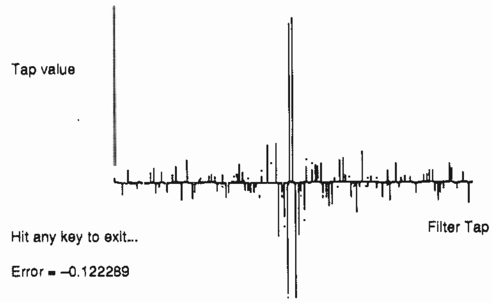
```
            replica = lms_filter(data);         /* Generate replica */
            error = echo - replica;
            lmsstep = 2.0 * LMSSTEPSIZE * error;
                                                /* Lms step size */
            lms(lmsstep);                       /* Update LMS filter */
            /* Display LMS taps after being updated */
            /* Also displays error and target tap value */
            for (i = 0; i < LMSLENGTH; i++) {
            graph_y = (int)(320.0 * ((double)i) / LMSLENGTH);
            _setcolor (0);
            _moveto     (graph_y, 0);   /* Clear old o/p */
            _lineto (graph_y, ((int)(-100.0 * 2.0 *
                        oldlmstaps[i])));
            _setcolor (14);
            _moveto     (graph_y, 0);   /* Scale and plot o/p */
            _lineto (graph_y, ((int)(-100.0 * 2.0 * lmstaps[i])));
            _setpixel (graph_y, ((int)(-100.0 * 2.0 *
                        echopathtaps[i])));
            }
            for (i = 0; i < LMSLENGTH; i++)
                        /* Store to clear old graph */
            oldlmstaps[i] = lmstaps[i];
            _settextposition (22, 2);
            printf ("Error = %lf", error);
#ifdef DEBUG
            while (!kbhit())
            ;
            getch();
#endif
            }
getch();
_setvideomode(_DEFAULTMODE);
exit (0);
}

double      fir_filter (stage_input)
double      stage_input;{
double      acc;
int         i, j;
echopath[echostart_index] = stage_input;
j = --echostart_index;
acc = 0.0;
for (i = 0; i < ECHOLENGTH; i++) {
            j = ++j % ECHOLENGTH;       /* Circular buf
                                        requires modulo inc */
            acc += echopathtaps[i] * echopath[j];
            }
echostart_index = j;
return acc;
}

double      lms_filter (stage_input)
double      stage_input;
{
double      acc;
int         i, j;
lmsfilter[lmsfiltstart_index] = stage_input;
j = --lmsfiltstart_index;
acc = 0.0;
for (i = 0; i < LMSLENGTH; i++) {
            j = ++j % LMSLENGTH;        /* Circular buf
                                        requires modulo inc */
            acc += lmstaps[i] * lmsfilter[j];
            }
lmsfiltstart_index = j;
return acc;
}

void        lms (lmsstep)   /* Update LMS filter */
double      lmsstep;
{
int         i, j;
                        /* Update weights w(n) */
j = --lmsstart_index;
for (i = 0; i < LMSLENGTH; i++) {
            j = ++j % LMSLENGTH;   /* Circular buf requires
                                        modulo inc */
            lmstaps[i] += lmsfilter[j] * lmsstep;
            }
lmsstart_index = j;
}
```

Output from listing 3



Adaptive filtering

The principles of adaptive digital filtering are simple. For instance, given an arbitrary signal that has passed down an unknown communications channel, how do we recreate the original signal? A classic requirement for this is telephony: every telephone line is different and the characteristics of a line are prone to variation during the call. To equalise the effects of the line, we could for example set up a filter with fixed coefficients at the start of the call. But as soon as the channel characteristics change, the transmission performance will drop because the filter coefficients are no longer optimal. The communications channel may even fall over. The solution is to use a filter that continuously adapts itself to the channel.

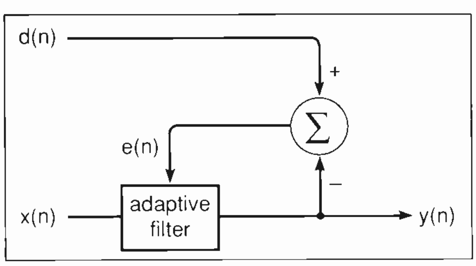


Fig. 2 Block diagram of an adaptive LMS filter

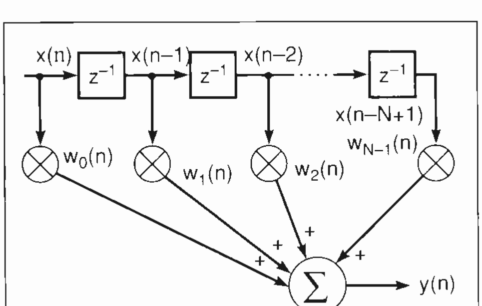


Fig. 3 Linear finite impulse response filter structure

The block diagram for the adaptive filter test program (**Example 3**) is shown in **Fig. 1** while **Fig. 2** depicts the block diagram for the adaptive filter update routine. The algorithm chosen is the Least Mean Square error solution based around the linear transversal finite impulse response filter (**Fig. 3**). The feedback path allows the mean squared error between the output signal and the expected signal to be calculated and this is used to update the taps according to these equations:

$$y(n)=\sum_{k=0}^{N-1} w(k)\times x(n-k) \qquad 1$$

$$e(n)=d(n)-y(n) \qquad 2$$

$$w(k)=w(k)+\mu\times e(n)\times x(n-k)$$

$$\text{for } k=0,1,2,\ldots,N-1 \qquad 3$$

$e(n)$ is the error signal, $d(n)$ is the actual output and $y(n)$ is the required output. The variable μ represents a gain factor controlling convergence of the filter.

The example is most like an adaptive echo canceller. The echo filter simulates a transmission line with a far end echo. The adaptive filter replicates the echo by adapting itself to match the transmission line characteristics. The echo estimation can then be removed from the received signal to leave just the signal transmitted from the far end.

The echo path filter is a practical working bandpass filter. It has a centre frequency of the sample rate divided by four and a bandwidth equal to its centre frequency. The echo path filter coefficients show as dots on the output graph and these are the targets for the adaptive filter coefficients.

The step size for the filter may be modified to see the effect this has on the adaptation of the filter: too large and the filter is unstable or it fails to converge and too small and convergence is too slow to be of practical benefit. ■

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2. A. V. Oppenheim and R. W. Schafer, Digital Signal Processing, Englewood Cliffs, NJ: Prentice Hall, 1975.
3. L. R. Rabiner and B. Gold, Theory and Application of Digital Signal Processing, Englewood Cliffs, NJ: Prentice Hall, 1975.

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Battery charging

NiCd cells are usually fairly abused devices; according to Telefunken, they only reach about 30% of their possible service life because charging is improperly done.

In theory, cells should be charged for 14 hours, after which they should be turned over to trickle charge or at least have the charge interrupted. In practice, people forget to switch over, particularly since manufacturers do not make a point of it in their operating instructions. Even worse, but in widespread use, is the boost charge method, where the cell is charged until its temperature starts to rise: in other words, when it has been damaged by overcharging and its life has been reduced.

Telefunken has the *U2400B*, an IC incorporating all the facilities needed for gentle charging and all monitoring functions, **Fig.1** being its internal block diagram, with a few extra bits.

At power-up, with no battery connected, the red led comes on. Connecting a battery with a minimum terminal voltage of 200mV to pin 4 starts the discharge phase at pin 10 after 2s, this being indicated by the red led flashing. When the battery voltage shows less than 500mV at pin 6, the green led flashes to indi-

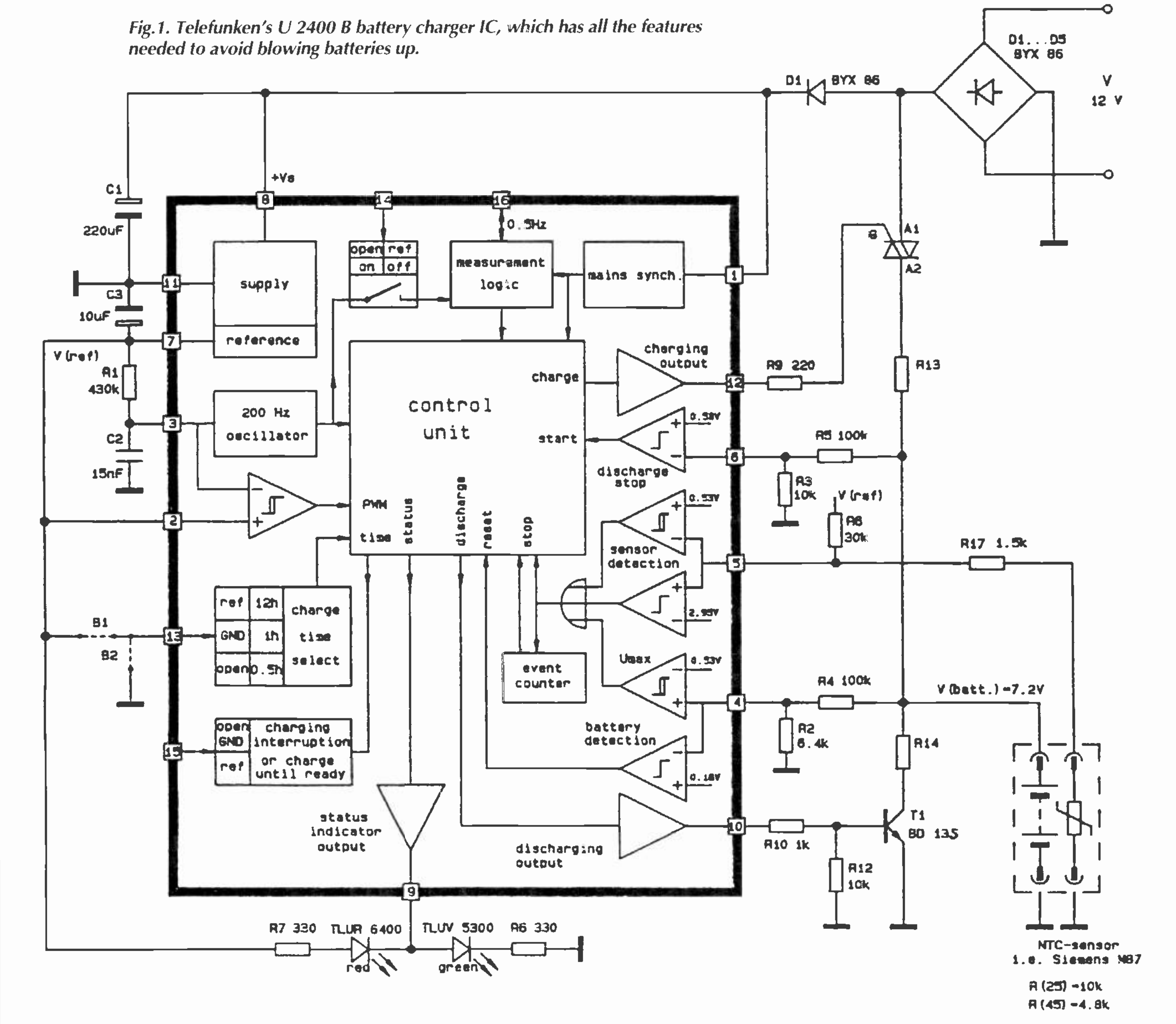


Fig.1. Telefunken's U 2400 B battery charger IC, which has all the features needed to avoid blowing batteries up.

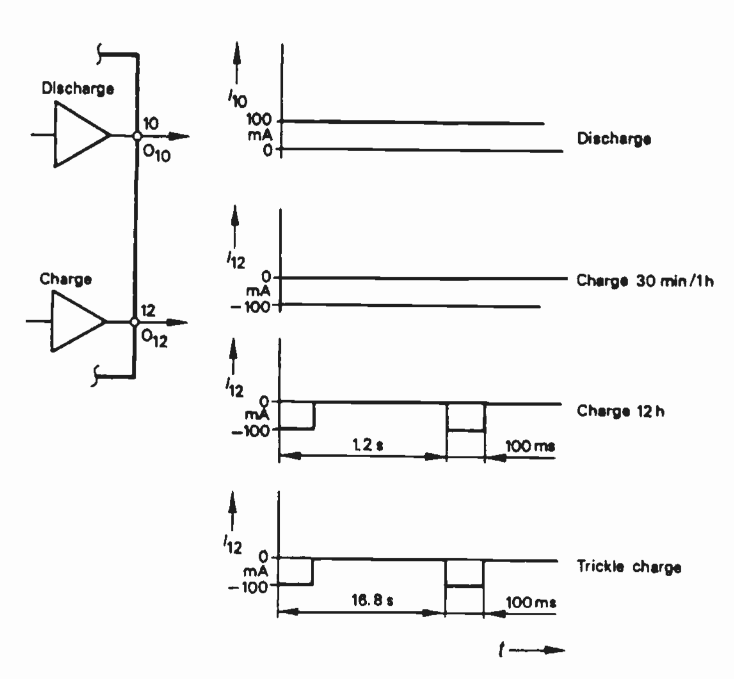


Fig.2. Timing of the discharge, charge and trickle charge operations. Pulse operation comes into action for a 12h charge and trickle charge.

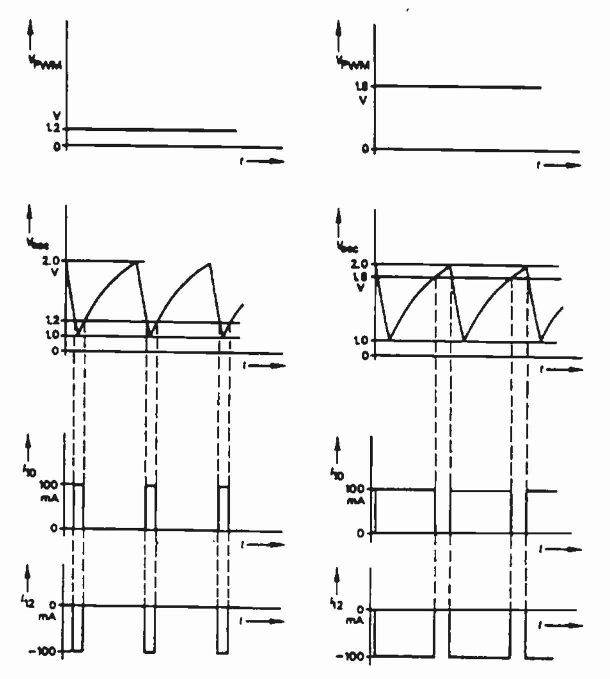


Fig.4. Timing of charge and discharge currents in the PWM circuit.

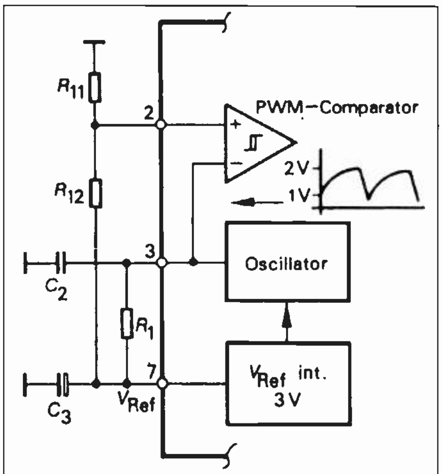


Fig.3. PWM comparator circuit; a variable pin 2 voltage allows matching to different battery capacities.

cate that discharge has stopped and that the charge output at pin 12 is active. After the charge period finishes (after 0.5h. 1h or 12h pulsed charge), trickle charging starts, indicated by the green led being on constantly; at this point, the battery has taken all it can. **Figure 2** is the timing diagram.

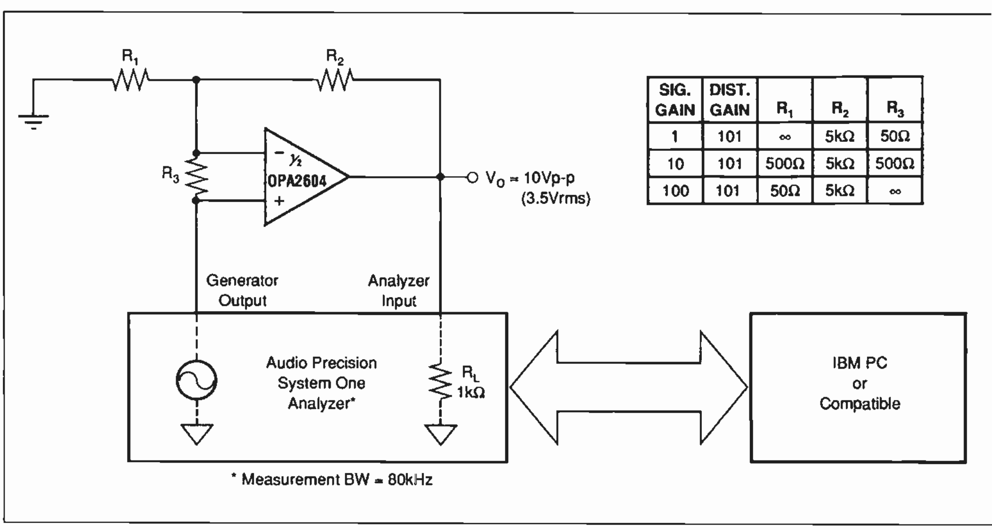
All outputs are made inactive by anything at all unfortunate in the way of temperature, overvoltage or pressure and the timer is interrupted in all three phases and in each mode if one of these limits is exceeded. A two-stage counter notches up one at every such excess, two counts being enough to bring pin 15 into action. Depending on whether pin 15 is open-circuit or connected to V_{ref}, either everything stops (flashing red) or the IC tries to make the best of a bad job (flashing red and green) to give the best charge possible even if the battery is already damaged. Pulse-width modulation of charge, discharge and trickle charge is brought about by the internal 200Hz sawtooth oscillator. Discharge and charge outputs are switched off when the sawtooth exceeds Vref on pin 2; the resulting PWM is effective in all three modes and if pin 2 voltage is varied by means of a switched network, output current to the battery can be made to match various battery capacities. **Figure 3** is the PWM circuit and its timing diagram is seen in **Fig. 4**.

Telefunken Electronic GmbH, *Postfach 700263, Stresemannellee 28, D-6000, Frankfurt/Main 70, Germany.*

Low-distortion amplification

Burr-Brown's OPA2604 offers very low distortion (THD+noise at 1kHz 0.0003%), low noise (noise density down to 10nV/ Hz at 10kHz) and a gain*bandwidth product of 20MHz. It will drive 35mA at ±12V into 600Ω and is unity-gain stable.

An interesting section of the application note is the explanation of the need for the circuit in Fig.1. It seems that distortion produced by the OPA2604 is beyond the capabilities of any commercially available test gear, so this circuit had to be dreamed up to increase the dis-



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	5kΩ	50Ω
10	101	500Ω	5kΩ	500Ω
100	101	50Ω	5kΩ	∞

Fig.1. Burr-Brown's OPA2604 dual op-amp generates an amount of distortion below the measurement range of commercial instruments. This circuit increases the distortion by a precise 101 times, while leaving the signal intact so that it can be measured.

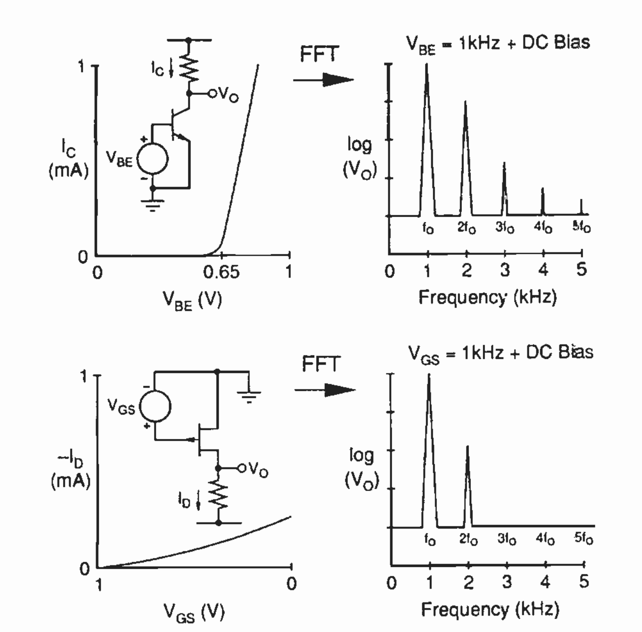


Fig.2. Odd harmonics sound worse than even ones. Fet devices exhibit a square-law transfer characteristic, as against the bipolar exponential curve and therefore generate mostly even-order harmonics.

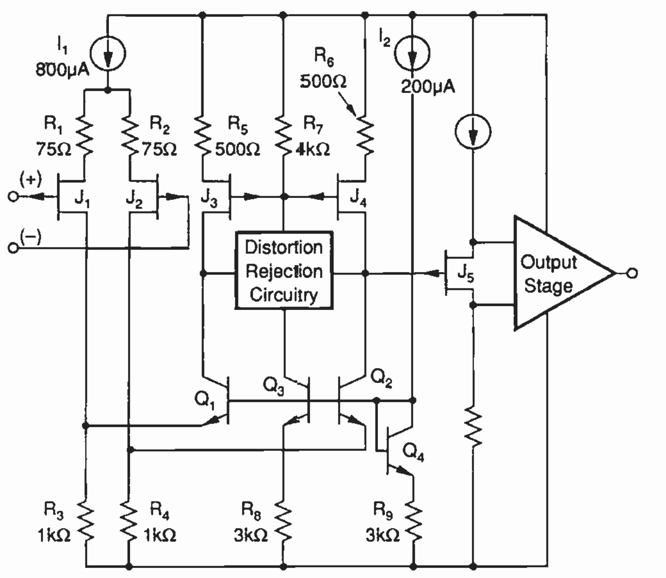


Fig.3. Layout of one section of an OPA2604. The comparatively high input-stage current of 800μA gives higher transconductance and reduces voltage noise.

tortion by a factor of 101 to make it possible to measure it. Resistor R_3, added to what is a standard inverting op-amp, leaves the closed-loop gain alone but rduces the feedback for error correction by 101 times. Input signal and load arrangements are normal.

This op-amp uses fets in the input and as phase-splitters in the output stage. Burr-Brown includes in the note a piece on sound quality, in which it is remarked that the reason many people believe that fet audio amplifiers sound better than bipolar types is that the fet's square-law drain characteristic generates fewer odd harmonics than the bipolar transistor's exponential transfer curve. Figure 2 is a comparison of the two types, with their FFTs. It has to be said, though, that at this level of distortion it would be difficult to discern the difference, unless one's ears were genuine 18ct. Bipolar transistors are only used here where their graceless transfer characteristic has least leverage.

Circuit arrangement of half an *OPA2604*, shown in Fig.3, is a folded-cascode input stage with a unity-gain output stage. Input current to the input junction fets is 100pA, or about 3000 times less than that of a bipolar-input op-amp, greatly reducing current noise at higher source impedances. Output is a junction fet phase-splitter driving high-speed n-p-n output drivers. The two channels are entirely independent of each other, even including bias circuitry, so that cross-talk is eliminated.

No particular audio circuits are given in the note, but Fig.4 is a current-output D-to-A converter, the current being converted to voltage drive by two *OPA2604*s, the second a low-pass filter with a 20kHz cut-off.

Burr-Brown International Ltd, *1 Millfield House, Woodshots Meadow, Watford, Hertfordshire WD1 8YX. Telephone 923 33837.*

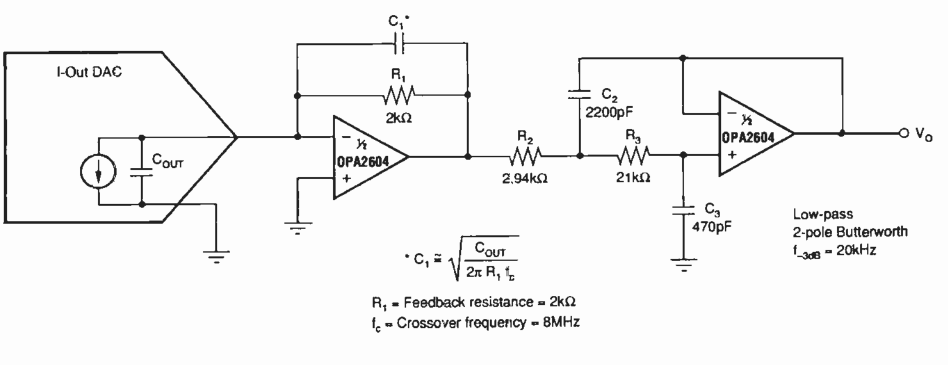


Fig.4. Current-output digital-to-analogue converter, with an OPA2604 converting the current to a voltage and another acting as a low-pass filter.

Clock distribution by ECL

Motorola's application note AN1405 is meant for designers of cmos and TTL logic systems who feel ill when anyone mentions ECL. It is possible that such designers are not aware that their problems with keeping clock skew within reasonable limits in high-speed, high-efficiency systems can be reduced or even eliminated by the use of ECL. Motorola, in the person of Todd Pearson, has set out to put them straight.

This is not the place to retail the note verbatim, since it is a well written explanation of the benefits to be obtained and is freely obtainable. It first of all explains the three mechanisms causing clock skew: duty-cycle skew, output-to-output skew and part-to-part skew; going on to detail the manner in which ECL, and in particular differential clock interconnection, will reduce the problem.

In passing, anyone who automatically thinks of ECL in terms of power-hungry devices had better think again; at about 20MHz, dynamic power of ECL is roughly the same as cmos and at 100MHz it is something like one-seventh. In this case, static power is irrelevant, since clock devices are never static.

Pearson also points out that, with reduced skew, you can use more of the clock cycle in which to carry out "value-added" operations.

Motorola Ltd, *European Literature Centre, 88 Tannners Drive, Blakelands, Milton Keynes, MK14 5BP. Telephone 0908 614614.*

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Fast, 16-bit A-to-D. Track-and-hold amplifier, sub-ranging A-to-D converter, voltage reference, and linearity and autozero calibration are all on-chip in the *AD1385* 500ksample/s, 16-bit sampling analogue-to-digital converter. Minimum THD and signal-to-noise ratio are both 90dB at 5kHz; S:N at 200kHz is 88dB. Differential and integral non-linearity are ±0.0006% and ±0.0015% FSD and maximum gain error is ±0.15%. Analog Devices, 0932 232222.

D-to-A converter. Video digital-to-analogue converters from Fujitsu, *MB40730* and *MB40760,* have 10-bit resolution, a minimum sampling rate of 60Msamples/s and linearity error of less than 0.1%. Power dissipation is 180mW and output is 2V pk-pk. The *'30* has ECL10KH i/o, while the *'60* is TTL-compatible. Three voltage references are selectable for output voltage, or an external reference can be used. Fujitsu Microlectronics, 0628 76100.

Discrete active devices

Wide-band transistors. *BFG 505/20/40* are 9GHz silicon planar epitaxial transistors from Philips with collector/emitter and collector/base voltages of 15V and 20V, 18-120mA collector current, power dissipation 1W, RF gain 13dB and noise figure 1.9dB at 2GHz. Gothic Crellon Ltd, 0734 788878.

High-voltage mosfet. Supertex *LND150* is a high-voltage depletion-mode mosfet with a drain-to-source breakdown of 500V and an on-state resistance of 1kΩ. Minimum on-state current is 1mA and typical input capacitance is 8pF. Its gate is internally protected against electrostatic discharge up to 1kV. Kudos Thame Ltd, 0734 351010.

Low-noise microwave transistor. *B12V105* from Bipolarics is a silicon low-noise type meant for use in low-power applications from VHF to microwave frequencies. Transition frequency is over 10GHz at 10-25mA and power gain 19dB at 1GHz and 12.5dB at 2GHz. Noise figure is 1.6dB or less at 900MHz. Tekelec UK, 0753 548585.

SM pin diodes. A family of pin diodes for surface-mounting and meant for frequency-hopping radio and filters is announced by Tekelec. Two kinds of SM package are made: a rectangular ceramic type with low inductance and a cylindrical one with low capacitance. Maximum breakdown voltage is 550V and lowest junction C is 0.15pF. Tekelec UK, 0753 548585.

Microwave power transistor. Tekelec UK has a new power transistor, the *BPT23E01,* meant for 1W linear common-emitter use in the range 1.8-2.4GHz. At 900MHz, power gain is 12dB and at 2GHz, 9dB. Collector efficiency in Class A is 30%. Tekelec UK, 0753 548585.

Linear integrated circuits

Low-drift instrumentation amp. With a maximum gain drift of 5ppm/°C and 0.6μV/°C voltage offset drift, Analog's *AD621* is claimed to be the industry's lowest-drift amplifier. Non-linearity is 10ppm FSD, initial voltage offset 50μV and gain error 0.05%. Pin-strappable gains of 10 and 100 are available and input voltage noise is 13nV/√Hz; input current noise is 0.1pA/√Hz. Maximum current supply needed is 1.3mA from ±2.3V to ±18V. Analog Devices, 0932 232222.

Instrumentation amplifier. Combining high accuracy with small size, Burr-Brown's *INA 114* amplifier offers a 50μV maximum offset, 0.25μV/°C offset drift and 115dB minimum CMRR. Gain is programmable from 1 to 10,000 by a single resistor. Supply range is ±2.25V to ±18V and the amplifier has input protection to ±40V. Burr-Brown International Ltd, 0923 33837.

Wide-band buffer amp. Harris's *HFA1110* is a closed-loop buffer amplifier with a bandwidth of 700MHz, a slew rate of 2,500V/μs and a 7ns settling time to 0.02%. Selectable gains of +1, –1 or +2 without external components and 60mA of output current make it well suited to cable driving, and its closed-loop design renders it useful as a current-to-voltage converter in D-to-As working at frequencies up to 100MHz. Gain flatness is 0.04dB to 50MHz. Thame Components Ltd, 0844 261188.

16Mbit drams. Toshiba is now in full production of 16Mbit drams, which are organised as 16M x 1bit and 4M x 4bit with high-density memory applications in workstations in mind. Single 5V operation is kept, but the supply is internally converted to 3.3V for reliability. Access times available are 60ns, 70ns and 80ns. Toshiba Electronics (UK) Ltd, 0276 694600.

Logic building blocks

Clock recovery. AD's *AD802-155* is used in the reciver circuit of a datacomms link to recover clocking from the data stream, regenerating retimed data and clock with no external crystal. It is the first in a family designed for different bit rates. Output jitter is insensitive to input data pattern and is typically 2.2° RMS with maximum data transition density and 3.3°RMS with a 2^{23}-1 pseudorandom input. It keeps lock on a featureless expanse of up to 240bit. Analog Devices, 0932 232222.

Zero delay buffer. To regenerate clocks in high-speed systems where skewing can be a problem, the *Avasem 9170* uses a cmos phase-locking technique. Multiples or divisions of the original clock are also generated. Even when the original duty cycle has degenerated to 20%:80%, the output is a respectable 48%:52%. Microelectronics Technology, 0844 278781.

24-bit colour palettes. 24-bit versions of Sierra's HiCOLOR family of colour palettes, the *SC15025/6,* offer up to 16.8 million colours and work with VGA and super VGA controllers. The devices are pin and function-compatible with earlier Sierra HiCOLOR units. Operating speed is up to 125MHz and the *15026* has 15 overlay registers as well as the triple 6-bit or 8-bit D-to-As in the *15025.* Sierra Semiconductor, 0793 618492.

Memory chips

Microprocessors and controllers

SCSI controllers. *Am53C94/6* are the first of a new family of Small Computer System Interface controllers from AMD, being plug-in replacements for the standard *53C94/6* but with the company's Glitch Eater circuitry to reduce the incidence of false-clocking due to system noise. A set of development software is available. Advanced Micro Devices UK Ltd, 0483 740440.

Ethernet IC. Alice is Artisoft's

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response to the requirement to make new PCs ready for network use from the start. It is a lan interface chip to be used in conjunction with Artisoft's LANtastic software and is software-compatible with the company's own *AE-2*, with Novell's *NE1000* and *NE2000*, supporting a wide variety of network operating systems. ISA and Microchannel buses are on the same chip. Engineering samples are now available. Artisoft, 0753 554999.

Mixed-signal ICs.
LD/DTMF dialler. For use with most common microprocessors, GEC Plessey's *MA525* dialler provides blocks of up to 21 digits at a time from the bus interface, which can be dialled in order with correct format and timing. Access pause and timed flash are stored and redial is included. All dialling conditions and timings are programmable in both LD and DTMF modes. Either MF tone or pulse dialling are selectable for each dial sequence to allow dialling followed by MF data transfer. Gothic Crellon Ltd, 0734 788878.

PC sound. Sierra introduces three new chipsets for PC sound synthesis. *ST8000* provides *Sound Blaster* emulation, ADPCM, a joystick port, MIDI interface and digital audio recording and playback. ST8001 does all that and also offers the Aria synthesiser and a 512Kbyte sound library, while the *ST8002* has all these features and a 1Mbye sound library. All are compatible with Microsoft's Multimedia Level 1. Sierra Semiconductor Ltd, 0793 618492.

Oscillators

Crystal oscillator. HCD's new *HCD364* oven-controlled crystal oscillator offers 5^{10}-8 frequency shift over the -20°C to 70°C temperature range. Phase noise is better than −130dBc/Hz at 100Hz offset and −150dBc/Hz at 1kHz offset. Frequency range is 4-16MHz and output is sinusoidal, a TTL/HCMOS version to come soon. HCD Research Ltd, 0444 415008.

Programmable logic arrays

High-speed FPGAs.
QuickLogic/Cypress field-programmable gate arrays, which are of 2000 to 20,000-gate level, are claimed to exhibit the lowest resistance and capacitance of any available, that and the Quicklogic ViaLink architecture resulting in system speeds for the *QL8X12* and *QL12X16* of 50MHz and internal logic speeds of up to 100MHz. Ambar Components Ltd, 0844 261144.

Field-programmable arrays. *TPC 12* FPGAs by TI are now fully released, together with a suite of development systems for PCs and workstations. Users are able to achieve a higher gate density on one chip than in the earlier *10* series, due to the fact that there are many more logic modules available, including the sequential type as well as combinational modules. System frequencies up to 60MHz are obtainable. Texas Instruments, 0234 223252.

Network measurement. For measurements in digital mobile communications networks, R. & S. offers the PCS Inpulse Response Analyser, this parameter being the best way to evaluate channel quality by sampling signals from the channel in conjunction with the ESVD test receiver. The instrument display channel impulse response in real time, with measurement of propagation delay down to 80µs and a dynamic range of 18dB. Rohde & Schwarz UK Ltd, 0252 811377.

Power semiconductors

Fast rectifiers. Intended for use in switched-mode PSUs, UPSs and automotive systems, Harris's *RUR 3010/15/20* ultra-fast rectifiers feature current ratings of 8-80A, peak repetitive reverse voltages of 100-1000V and recovery times of less than 45ns. The 15A *MUR/RUR 1510* series are faster, with a 30ns recovery, reverse voltage of 200V and forward current of 30A (200A surge). Harris Semiconductor (UK), 0276 686886.

Radar TX transistors. Developing 750W typical output power, the Philips *MX1011BY700Y* transistor is meant for radar transmitter use in the 1030-1090MHz range. In medium-pulse, heavy-duty use, the upper limit is 1150MHz. In short-pulse use (10µs, 4% duty cycle), output power is 650W at 1090MHz, with a power gain of 6dB and 54% efficiency. Philips Semiconductors Ltd 071 436 4144.

PASSIVE

HV transformer. Coiltronics's *CTX110459* is a miniature, surface-mounted 6W transformer, which provides 550V peak running at 11mA; peak firing voltage is 1.7kV. Input voltage is 3-20V at 40kHz and operating range is −40 to 85° Celsius. Microelectronics Technology, 0844 278781.

Displays

EL flat panels. Half the thickness and two-thirds the weight of earlier types, electroluminescent flat-panel displays from Planar Systems also take less than half the power normally needed. Resolutions of from 320 by 256 to 640 by 400 are accompanied by variable contrast and brightness, integral power supply and high brightness. MTBF is over 30,000 hours. Review Display Systems Ltd, 0959 563345.

Filters

Din rail-mounted filters. DRF Din rail mounted filters and suppressors from Roxburgh come in 1A, 3A and 6A versions and are suitable for both top-hat and G-type rails. Operating frequency is 150kHz-30kHz at line voltage, with spike protection. DVS surge suppressors are supplied in 24V, 49V, 110V and 240V versions in top-hat mountings. Roxburgh Electronics Ltd, 0724 281770.

Miniature filters. RF filter designs that previously needed large tubular components are now realised in ultra-miniature PCB-mounted components in a new range by Trilithic. Band-pass, low-pass and high-pass types are available in the range 30-2500MHz in TO-5, TO-8 and SM cans and in Tchebyshev, Butterworth, Bessel, Gaussian, elliptic and linear-phase forms. Trilithic Ltd, 0442 891130.

Hardware

Chip emulator. Correct-A Chip sockets from Aries incorporate a user's own circuitry within the socket (of various types) to create a "semi-hybrid daughter board" and save up to 32 square centimetres of board space. Mother boards can be given "function sites", various plug-in functions then being applied to the sites. By using the small PCB in the socket, any IC pin can be connected to any board hole. Aries Electronics (Europe), 0908 260007.

Instrumentation

VXIbus chassis. B&K's *2817* chassis is a general-purpose mainframe for VXIbus and VMEbus modules, providing 13 slots for C-size VXIbus modules or direct insertion of B-size or VMEbus modules without adaptors or any modification. Auto-jumper connection to the back-plane gives flexibility of positioning and automatically shorts unused slots. The chassis has a back-plane designed for high-speed use and a 600W power supply with overcurrent, overvoltage, DC and AC fail and overheat detection. Bruel & Kjaer, 081-954 2366.

250MHz oscilloscope. Model *2250* from Leader is a 250MHz instrument with PAL, NTSC and HDTV line selectors, a frequency counter, an event trigger and digital voltmeter. Four cursors and sub-cursors are provided. Features include auto setup, automatic ranging in X and Y directions, self calibration, automatic probe compensation, on-screen calendar and comments. Leader Instruments (Europe), 0753 538022.

Video output from DSO.
Yokogawa's *DL1000* series of digital storage oscilloscopes are now able to provide a PAL television signal of the screen image, a facility that allows the display of an oscilloscope trace on a large TV screen or recording on video tape. One advantage of the recording option is the increase in long-term monitoring provided. It is also possible to make a printout of the recording without interrupting recording. Martron Instruments Ltd, 0494 459200.

40MHz oscilloscope. *CS-5130* by Kenwood is a 40MHz dual-trace instrument with on-screen readout and delayed timebase, the cursor reading voltage difference, time difference, frequency, ratio and phase, all shown on the screen. The tube is a 150mm, dome-mesh type with a 12kV PDA potential. Trio-Kenwood UK Ltd, 0923 816444.

Arbitrary-waveform generator. In addition to to the usual sine, square and triangular waveforms and some not so usual, the Model *295* from Wavetek allows its user to draw any waveform on a screen, using a mouse or mathematical expressions, whereupon the instrument will output that waveform at up to 10MHz. As well as the internal standard waveforms provided, another 30 are on a dos-compatible disk. Frequency accuracy is within two parts per million. Wavetek Ltd, 0603 404824.

Literature

Consumer ICs. GEC Plessey Semiconductors's consumer IC handbook, now available free, describes more than 100 ICs for satellite and cable TV, teletext, TV decoders and PWM waveform generators. Gothic Crellon Ltd, 0734 788878.

Microcomputer guide. Features available in Hitachi's H8/300 series of 8-bit single-chip microcomputers are described in a new guide, which gives details of the new *H8/329* and *H8/338* families, which offer 48K rom and 2K ram, two full uart ports and eight channels of A-to-D conversion. Hitachi Europe Ltd, 0628 585000.

8051 C programming. A primer on the use of *C* for programming embedded microcontrollers is produced by Hitex, taking into account the difficulties of accessing pripherals at specific addresses. The *C51* primer is based on several years experience of a technical support line and therefore has most of the answers ready. Hitex (UK) Ltd, 0203 692066.

RF seals. James Walker's *Shieldseal* conductive elastomers provide good contact with metal flanges to allow low-resistance current flow across enclosure joints, also sealing against moisture and other contaminants. All but the commercial grades give over 100dB of RF attenuation, the commercial types giving 78dB. Shieldseal is supplied in extrusions and flat sheets, or can be supplied ready-moulded to shape. Conductive adhesives are available. James Walker & Co. Ltd, 0483 757575.

Power supplies

Power-factor correction. Using Coutant-Lambda's *PF 450* power supply with the company's *CN 280 PF* and harmonic correction module produces a 260 by 150 by 50mm unit with a power factor of 0.99 at 640W and a universal input of 85 265V AC. The module provides alarms for abnormal PF operation and for overvoltage and thermal conditions and current limit. Coutant-Lambda Ltd, 0271 865656.

Variable power. DSL's *PR* series of linear power supplies provide variable voltage outputs from 2-7V, 10-15V or 20-30V at up to 3840W and 160A continuous. They are fully protected against shorts, RF power and back-EMF and there is an overvoltage crowbar. DSL, 0279 416841.

Modular DC power supply. California Instruments model *1200 DCS* programmable DC supply for the ATE sector provides up to eight separate isolated outputs per chassis in 5.25in height, front chassis module loading form. Each output has self test and is fully protected. Wessex Electronics Ltd, 0272 571404.

Radio communications products

Small 418MHz Rx. Short range telemetry links needing small size and low power consumption will benefit from the hybrid super-regen. receiver module from Quantelec, which is 41 by 14 by 6mm and takes 1mA from 5V. It works with any 418MHz keyed-carrier transmitter, sensitivity being -90dBm or 25μV. Digital data is output at 5V logic level. Quantelec Ltd, 0993 776488.

Switches and relays

Rotary switches. Miniature switches made by Cole Instrument Corp., the *3900* series of half-inch multi-deck rotary switches are to MIL standard, being proof against flux and contamination, moisture and corrosion, and possess self-cleaning contacts to give a 0.02Ω contact resistance over a 25,000-cycle minimum life. They come in various index steps from 30° to 90° with up to six poles per deck; contact rating is 1A at 115v AC and 28V DC. Acal Electronics Ltd, 0344 727272.

Transducers and sensors

Flame detector. Centronic's range of UV detectors now includes the *OSI-310*, which uses a photodiode, filter and built-in amplifier optimised for the 310nm light emission from flames such as those from oil and gas burners, while remaining relatively insensitive to the radiation from incandescent bodies. Responsivity is 100V/μW into 50Ω and typical current consumption is 0.1mA. Centronic Ltd, 0689 842121.

Audio transducer. Star Micronics has produced the *HGP-12A* audio output transducer for the car and similar industries. It produces an 85dBA minimum tone of 1700-2200Hz from 12V and operates at temperatures between −40° and 90°C; height is 12mm and diameter 16mm. Roxburgh Electronics Ltd, 0724 281770.

COMPUTER

Computer board level products

Neural networking. Amplicon Liveline's *NT5000* is a data capture, learning and simulation package for PC ATs, the system being trained to carry out complicated tasks without the need for programming. A combination of hardware and software, the package includes a portable processing unit with a number of analogue and digital inputs and outputs and an LCD, to be connected to the host by RS232. Software provides a graphical network editor, colour interface using a mouse and automatic neural network generation. Amplicon Liveline Ltd, 0273 608331.

GPS for PCs. Global Positioning System information is received and processed by Amplicon Liveline's *XR4-PC* board. The board has its own antenna, which receives pulses from up to eight GPS satellites to give position within 100m anywhere in the world, even when travelling at up to 200mile/h. Several programs give various types of display and raw satellite information is available. No system memory is taken up and the board is programmable in most high level languages: a *C* library of functions is supplied. Amplicon Liveline Ltd. 0273 608331

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A/D I/O for the PC. Amplicon's *PC 30PG* is a high-speed (up to 200kHz) analogue and digital input/output board for the PC AT, consisting of a 12-bit A-to-D converter with 16 single-ended or 8 differential inputs and programmable gain; two 12-bit and two 8-bit D-to-A converters for either bipolar or unipolar working; 24 lines of digital i/o; and a user-configured counter/timer. Software is provided in most of the compiled languages, and Windows 3 data acquisition software is available. Amplicon Liveline Ltd, 0273 608331.

Comprehensive systems card. PSI's *Mini-Module+Plus* is a single-board system with a large array of inputs and outputs. There are 20 digital i/os, two 16-bit counters, two RS232 serial ports with an RS485 option, an IIC port, eight 12-bit A-to-D channels at 10µs, four 12-bit D-to-A channels, a calendar clock alarm, up to 1Mbyte of sram, up to 1Mbyte of rom and an LCD drive. A full PC package supports development, programming being in *C, C++, Modula-2* or assembler. Its *68000* runs at 16MHz. PSI Systems Ltd, 0371 876088.

Development and evaluation

8051 development. With its graphical user interface, the *C-SPY/S* high-level debugger and a real-time kernel, IAR's *ITS8051* is described as a "total-solutions" toolkit for *8051* development. It offers memory-specific pointers and a register optimiser that uses all registers and gives appropriate priority to each variable. The compiler is claimed to give the most compact *C* code on the market. IAR Systems Ltd, 071-924 3334.

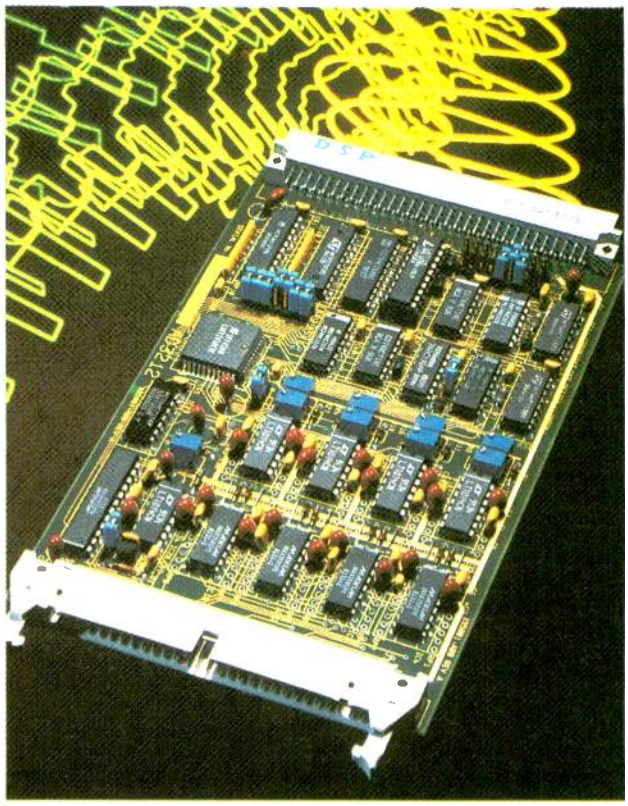
Transputer data acquisition. Claimed to be the highest speed analogue interface for transputer systems, the *adt164* data acquisition module provides up to four channels of simultaneously sampled data at 1MHz per channel, with a resolution of 12bit in a size 4 transputer module. Data is processed on board by a *T400* or *T805* transputer and stored in a 4Mbyte memory. *adt164* is compatible with TRAMs from other makers and is therefore usable with number-crunching TRAMs containing *i860, DSP56001* and others for real-time signal processing. Sunnyside Systems Ltd, 0506 460345.

Another GPS for PCs. The Twenty First Century *GPS-PC1* is a Global Positioning System receiver card for half-card PC slots, based on the Rockwell-Collins *Navcore 5* module and using a passive antenna. Tracking five satellites simultaneously, the unit gives position, velocity and acceleration information in three dimensions, all displayed on screen in choice of units. The information can be linked to other packages, such as the popular *Autoroute* and many navigational applications. Twenty First Century Ltd, 0794 884713.

Computer systems

Windows data and control. *Windata/L* is a low-speed data acquisition and control system, consisting of a PC XT/AT card, cabling, connection panel and Windows-based software. It will handle 8-32 thermocouple inputs, 16-64 voltage loop or 4-20mA current loop inputs. The card also has two 12-bit ±5V analogue inputs and 16 i/o channels. Data Translation Ltd, 0734 793838.

FPGA programmer. *Activator 2* from TI is a programmer for 10 and 12 series field-programmable gate arrays, using a SCSI interface to communicate with the ALS. Versions for *386/486* PCs, HP *Apollo* workstations and *Sun 4* workstations are available. Texas Instruments, 0234 223252.



Computer peripherals

Rewritable optical disks. Half-height 3.5in optical drives from Sony in the *SMO-301* range use 3.5in ISO/ANSI-standard continuous composite magneto-optical disks with a formatted capacity of 128Mbyte. Rotational speed is 3000rpm, giving a data transfer rate of 625kbyte/s and a seek time of 40ms. A buffer allows burst transfers at up to 4Mbyte/s. Sony Components Ltd 0784 467864.

STEbus analogue i/o. *AD3212* analogue interface board for the IEEE-1000 standard STEbus provides 32 high-speed analogue inputs and four analogue outputs to 12-bit accuracy; inputs can be configured as 16 double-ended channels. A 32-word FIFO buffers incoming data to reduce interrupt requirements and a timer allows conversion delays between samples to be set independently. Dean Microsystems, 0344 727269.

Software

PCB temperature analysis. Flogate is an interface used with Racal-Redac's *Visula Cad Expert* PCB layout package and Flomerics's Flotherm thermal analysis package to identify hot spots on PCBs, modifications being quickly re-evaluated. The combined system takes into account geometry and thermal power of a PCB and identifies air flow and heat transfer data, down loading it into Cad Expert. Flomerics Ltd, 081-547 3373.

Neural nets for Windows. *NeuDesk* is a Windows-based neural network package for PCs, intended to allow new users to evaluate the technique. One master drop-down menu takes the user through an entire network development process, ending with a trained system. The package includes a validation process which terminates training when the network is optimally trained. Neural Computer Sciences, 0703 667775.

■

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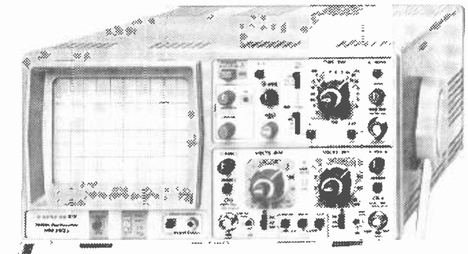
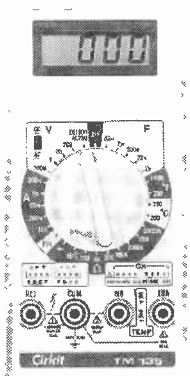


Offer must end 31st Jan 93

PART NO.	DESCRIPTION	USUAL PRICE	OFFER PRICE
HM203-7	20MHz, dual channel, 1mV/cm, component tester	£338.00	**£312.54**
HM205-3	20MHz, digital storage/analogue 'scope	£610.00	**£583.83**
HM604	60MHz, dual channel, 1mV/cm, delay time base	£610.00	**£583.83**
HM1005	100MHz, 3 channel, 6 trace, delay time base	£792.00	**£765.11**



MULTIMETERS

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The TM series of low cost meters, with 3½ digit LCDs, full overload protection, strong ABS cases and packed with features. Supplied with test leads, battery and manual

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PART NO.	DESCRIPTION	USUAL PRICE	OFFER PRICE
TM 5315	DC current (10A) continuity and diode test	£17.01	**£16.38**
TM 5365	Capacitance and frequency (200kHz) ranges	£31.06	**£25.52**
TM 5375	Frequency range (20MHz) and HFE test	£31.45	**£26.80**
TM 115	AC & DC current (10A), HFE and continuity test	£27.66	**£26.37**
TM 135	Capacitance ranges, temp. (inc probes), HF, diode and continuity test	£39.11	**£35.32**
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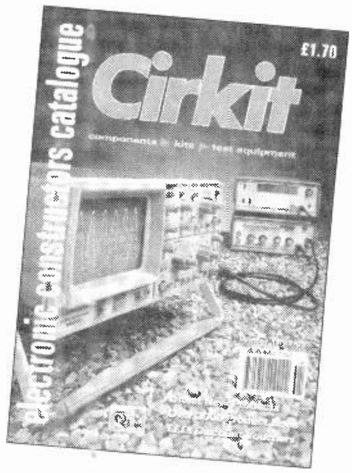

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Circuits, Systems & Standards

First published in the US magazine EDN and edited here by Ian Hickman

Thermal tester verifies transistors

Is your device well and truly heat-sunk?
An in-situ tester for the adequacy of heat sink arrangements. Ideal for the development lab and for sample testing of production units to ensure quality is maintained.

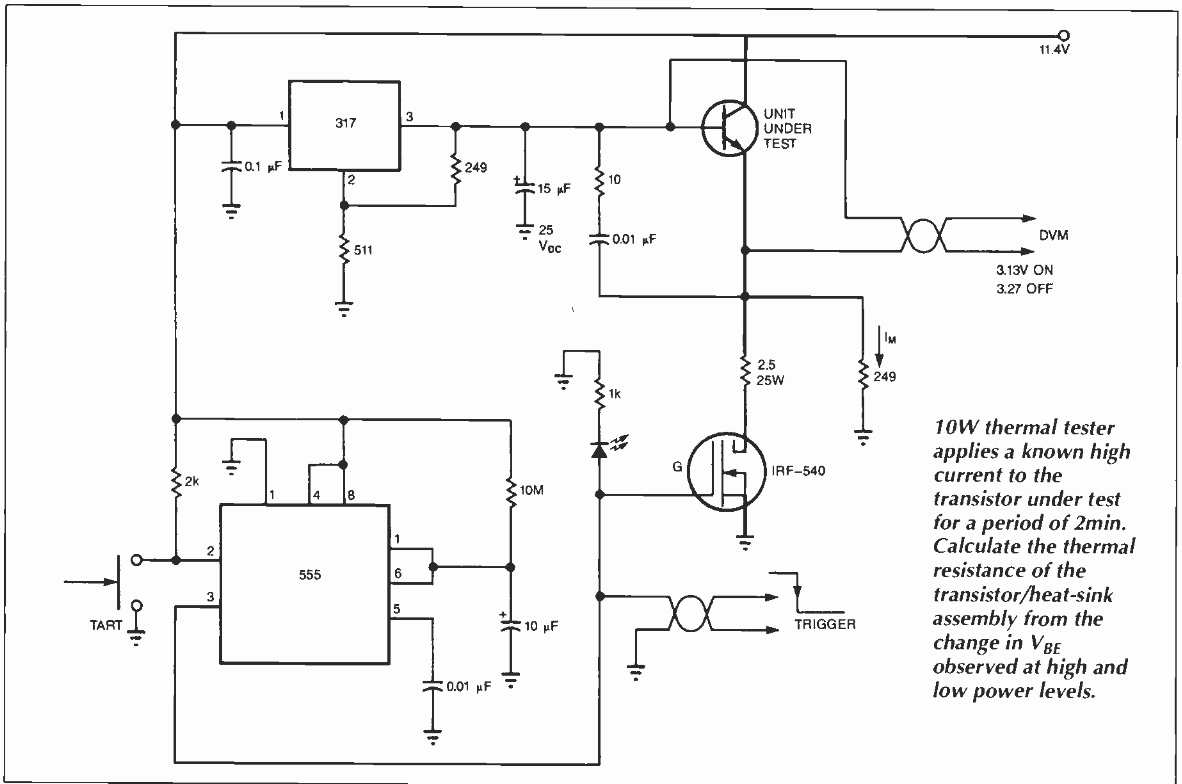
This tester verifies the thermal interface between a power transistor and its heat sink by measuring the temperature-sensitive V_{BE} of the transistor under test.

The unit first calibrates dissipation of the transistor under test with a fixed, low-level current then switches on a high current for a certain time and finally returns to the original low level. Record the V_{BE} at the various stages in this test to calculate the thermal resistance of the transistor/heat-sink interface.

To find T_J max, first find the decrease in V_{BE} between the reading at the end of the high-power stage and the steady-state value during the low-power stage. Then, T_J°C = ambient temperature°C + decrease/2.2mV/°C. Similarly, the effective total thermal resistance for the transistor/heat-sink assembly is (decrease/2.2mV/°C)/10.

An 11.4V input yields 10W dissipation in the transistor under test. The tester comes up in the low-power mode and after warm-up the low-level V_{BE} can be measured. Press the test switch and the *555* timer turns on the dmos switch, and the current in the transistor under test jumps to 1.1A. The timer times out in 2min. A variety of common lab instruments can be used to record data.

***Carlo Venditti,** C S Draper Lab, Cambridge, MA.*



10W thermal tester applies a known high current to the transistor under test for a period of 2min. Calculate the thermal resistance of the transistor/heat-sink assembly from the change in V_{BE} observed at high and low power levels.

Divider displays uncanny accuracy

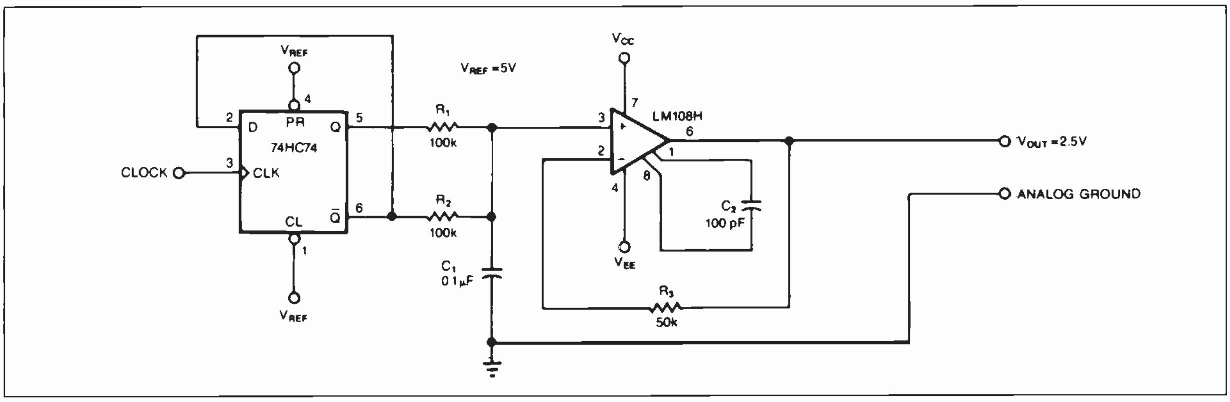
The voltage divider divides V_{REF} in half with uncanny accuracy yet uses no precision components: note that unlike dividers based on precision resistors, which can divide a voltage in virtually any proportion, this circuit will only divide V_{REF} in half.

The circuit uses a cmos flip-flop to toggle the divider resistors, R_1 and R_2, between V_{REF} and ground. R_1 and R_2 need not be precision resistors because the toggling action, along with C_1, averages any error toward zero.

Because the effects of the flip-flop's output transistors' on-resistances and any mismatch between R_1 and R_2 tends to average out, the major source of inaccuracy in this circuit is asymmetry in the flip-flop's time division. Accuracy of the circuit can be further improved by buffering the Q and $\overline{Q}$ outputs with an HC-type line driver with paralleled outputs. The device would further reduce the effects of the flip-flop's output transistors' on-resistances.

Exact voltage divider
Here is a solution just waiting for a problem to solve. If you need to derive a half reference-voltage point and just happen to have a clock waveform handy, but cannot afford precision resistors, here is your answer. Or you could use the flip-flop to control cmos switches likewise, to produce a midpoint voltage between any two voltages V_{REF1} and V_{REF2}.
IH

Michael A Wyatt, *SSAvD Honywell Inc, Clearwater, FL.*



Dividing V_{REF} in half using no precision components.

Decode overlapped eprom, ram and i/o

Today's large ram and eprom chips (32k/64k bytes and up) allow the size, complexity, and even the cost of eprom-based microcontroller systems to be reduced. Using a physical memory composed of two 32kbyte ram chips and two 32kbyte eprom chips (**Fig. 1**), a 64kbyte memory can be implemented in which the ram and eprom sections overlap almost completely.

The arrangement allows nearly full use of the addressable space because the system's ram/eprom boundary can be set where it belongs – near the application's highest eprom location. A conventional system's boundary, on the other hand, must lie on an address location determined by the physical chip size (in bytes).

For example, for a system based on three eprom chips of 8kbyte each, the ram must begin at the 24kbyte level. Therefore, if an application requires only 17kbyte of eprom, 7kbyte of memory must be foregone.

The system in Fig. 1 also includes space for eight memory-mapped i/o devices, located at the top of the ram for the convenience of microcontrollers such as the *8051*, which lack an IO/$\overline{M}$ signal. The eight base addresses shown reserve 16 ram locations for each device, leaving the top 128 ram addresses inaccessible. Ram and eprom boundaries are established by using a dip switch or jumpers manually to set the fence address B_{15}-B_8, shown in the memory's logical-organisation diagram (**Fig. 2**).

In **Fig. 3**, the magnitude comparator IC_1, compares the

Flexible addressing for microcontrollers
A useful memory mapping arrangement to enable as much or as little memory as needed to be dedicated to eprom (to the nearest 256 bit boundary) with the rest available for ram, except for a few locations at the top of memory which it reserves for i/o.
IH

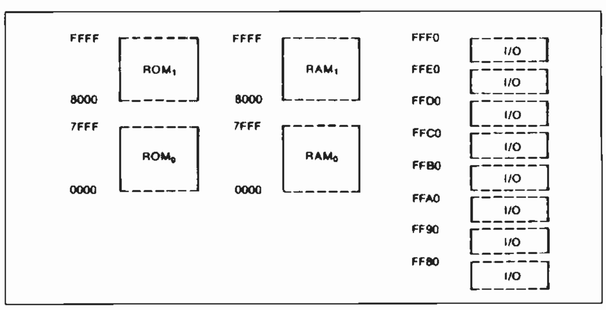


Fig. 1. 64kbyte memory system provides 64kbytes of physical ram virtually overlapped by 64kbytes of physical eprom.

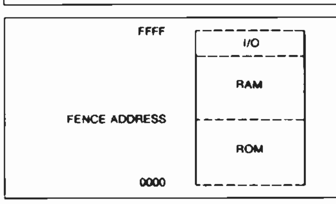


Fig. 2. Logical organisation of the memory in Fig. 1 locates memory-mapped i/o space at the top of the ram and allows the boundary to be set between the ram and eprom by manually setting a fence address.

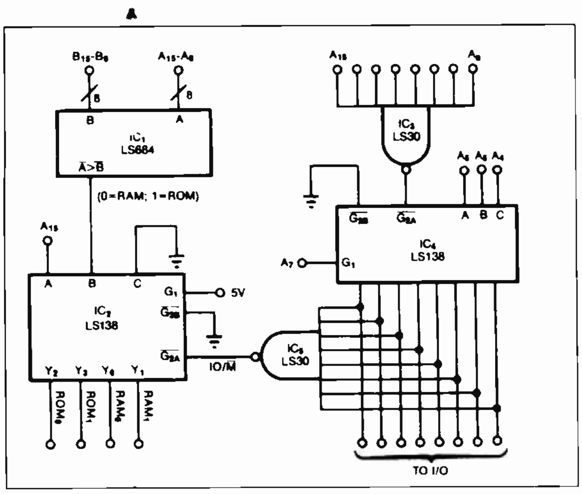


Fig. 3. These ICs control the memory in Fig. 1. IC_1 and IC_2 select the ram and eprom chips according to fence-address position, and IC_3 and IC_4 decode i/o addresses. IC_5 generates an IO/$\overline{M}$ signal

high byte of the fence address with the high-byte address lines and issues a signal – 0 for ram, 1 for rom. (Comparing only the high bytes simplifies the decoding circuit but leaves as much as 256bytes of ram unaddressable.) Next, the two- to four-line decoder IC_2 uses the decoder signal and the A_{15} address line to activate the appropriate memory chip. The eight-input Nand gate IC_3 and the three- to eight-line decoder IC_4 generate chip-select signals for the eight i/o devices. For active i/o devices, another eight-input Nand gate (IC_6) generates an IO/$\overline{M}$ signal that disables the selection of ram.

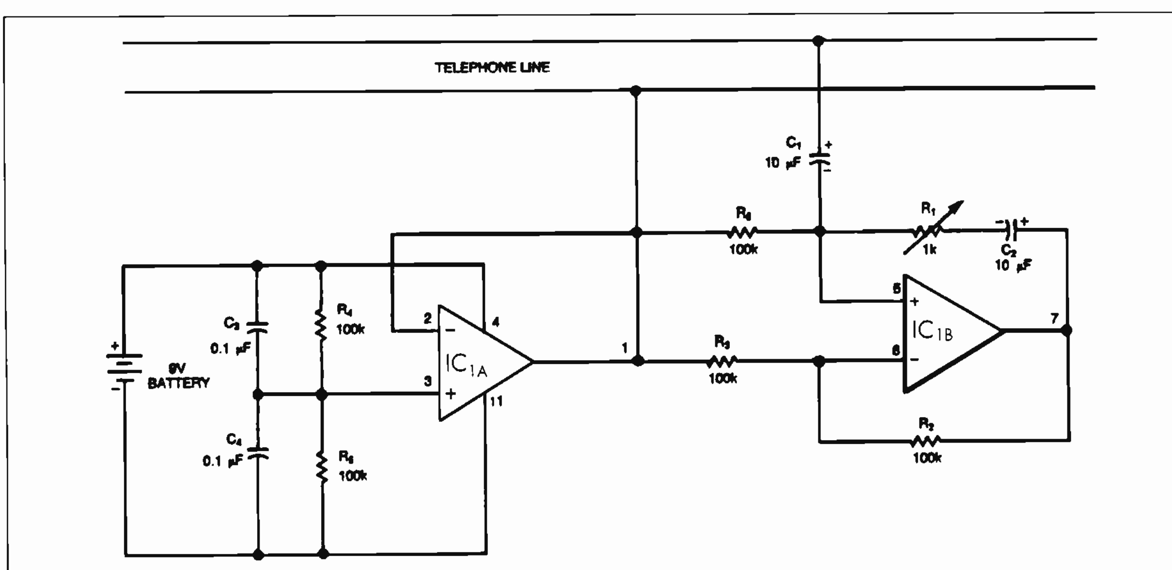
W H Payne, *Sandia Labs, Albuquerque,*

Amplifier handles duplex line

Another amplifier for a two-wire line
Another approach to amplification in a two-wire line is simply to bridge a negative resistance across the line. If the return loss of the terminations is too low at some frequency, the circuit will sing around at that frequency.
IH

This bidirectional amplifier, able to amplify both signals of a duplex telephone conversation, uses the principle of negative resistance. Obviously, such an amplifier could easily be unstable; but R_1 can be adjusted for maximum amplification and the circuit will remain stable. You might also consider replacing the *LM324* op amps with op amps that would distort less, such as the *LM1558*, *LF412*, *LF353* or *LF442*.

***Mansour Ahmadian,** Technical and Engineeng University, Tehran, Iran.*



Amplifier uses negative-resistance principle to amplify full-duplex telephone signals.

A digital-to-analogue converter is hardly a cheap alternative to a potentiometer. However, some readily pay the price, only to get rid of the "dirty" mechanical contact, while others are prepared to pay for remote control and repeatable settings. Erik Margan describes an ingenious design using a single D-to-A back to front.

Single D-to-A equalisation

In contrast with other digitally controlled equalisation circuits, which use either a D-to-A to set the analogue voltage for driving two VCAs, or use two D-to-As to provide the required boost-cut function, the circuit described below exploits the available complementary outputs of some cmos D-to-As, like *AD7524*, to achieve the same result with only one D-to-A.

Actually, the D-to-A is connected backwards; the complementary outputs function as inputs and the voltage reference input is used as output. This is possible due to bidirectional cmos switches in the D-to-A and the symmetrical ±7.5Vdc power supply for the D-to-A and control logic. Since the voltage swing capability of D-to-A outputs is limited, two resistive dividers level the signal down and an op-amp is used to restore gain and compensate for filter losses.

This op-amp also serves as a low-impedance driver for the filter section, thus preventing filter transfer function variations with boost/cut setting (a weak point of many equalisers using gyrators).

The second op-amp boosts or cuts the filter output by

$$G = 2 + \frac{R_m}{R_n} = 4$$

multiplied by the 4-bit digital code in symmetrical offset-binary format (0111 = 1000 = 0dB).

For the band-pass filter I have used a series-shunt R C network. Its transfer function is:

$$F(j_\omega) = \frac{\dfrac{R_b}{j_\omega C_b R_b + 1}}{R_a + \dfrac{1}{j\omega C_a} + \dfrac{R_b}{j\omega C_b R_b + 1}}$$

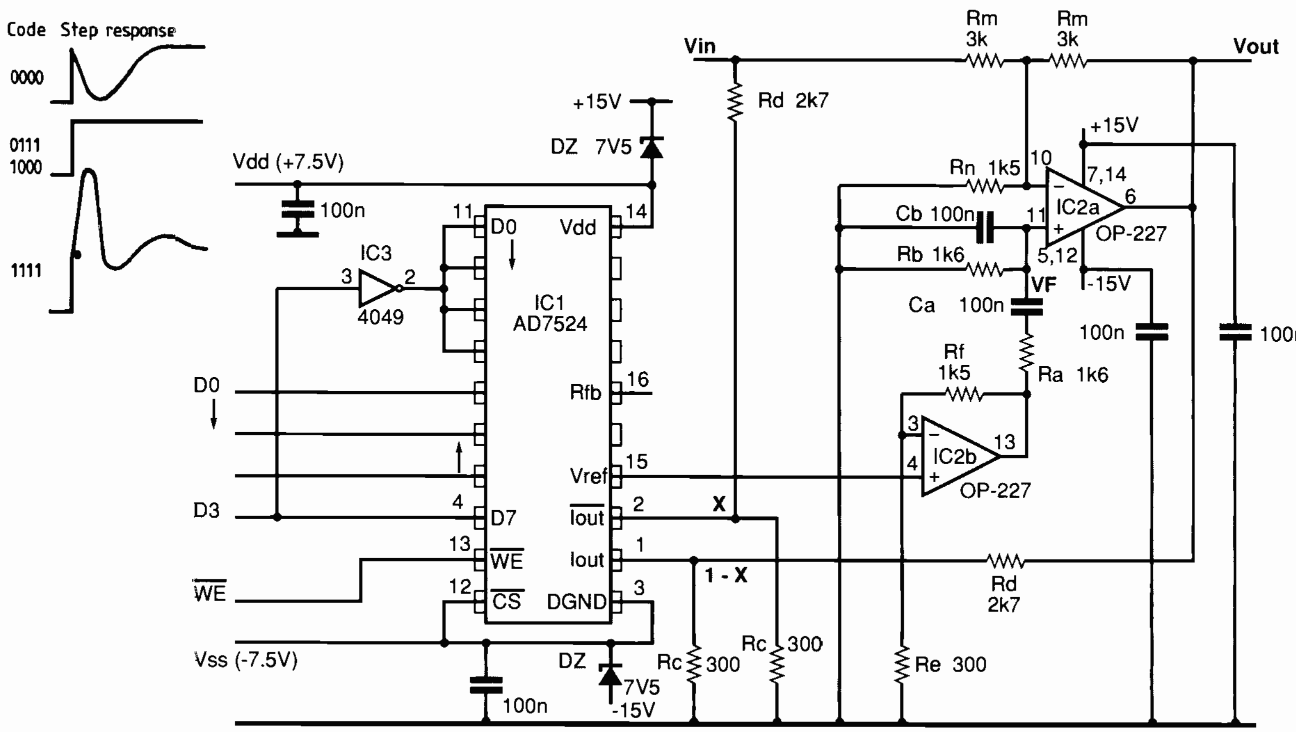


Fig.1. Circuit diagram. Note the ±7.5V DC power supply for the D-to-Aand the data control logic.

With little rearrangement, it may be rewritten as:

$$F(j\omega)=\frac{\frac{1}{R_aC_b}j\omega}{(j\omega)^2+j\omega\left(\frac{1}{R_aC_a}+\frac{1}{R_bC_b}+\frac{1}{R_aC_b}\right)+\frac{1}{R_aC_aR_bC_b}}$$

If we compare this to the normalized biquadratic form:

$$H(s)=A_0\frac{\frac{\omega_0}{Q}s}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}$$

we find the filter centre frequency at:

$$\omega_0=\sqrt{\frac{1}{R_aC_aR_bC_b}}$$

From the last three equations we may calculate the filter Q-factor:

$$Q=\frac{\sqrt{\frac{1}{R_aC_aR_bC_b}}}{\frac{1}{R_aC_a}+\frac{1}{R_bC_b}+\frac{1}{R_aC_b}}=\frac{1}{\sqrt{\frac{R_bC_b}{R_aC_a}}+\sqrt{\frac{R_aC_a}{R_bC_b}}+\sqrt{\frac{R_bC_a}{R_aC_b}}}$$

and the attenuation at the centre frequency:

$$=\frac{1}{R_aC_b}\cdot\frac{1}{\frac{1}{R_aC_a}+\frac{1}{R_bC_b}+\frac{1}{R_aC_b}}=\frac{1}{\frac{C_b}{C_a}+\frac{R_a}{R_b}+1}$$

If $R_a=R_b=R$ and $C_a=C_b=C$ then

$$\omega_0=\frac{1}{RC}\qquad Q=\frac{1}{3}\qquad A_0=\frac{1}{3}$$

and this results in one-octave band-width. The filter output voltage is:

$$V_F=(xV_{in}+(1-x)V_{out})a_1A_1F(j\omega)$$

where:

$$0\geq x\geq 1\quad a_1=\frac{R_d}{R_c+R_d}=\frac{1}{10}\quad A_1=1+\frac{R_e}{R_f}=6$$

The system output voltage is then:

$$V_{out}=-V_{in}+a_1A_1GV_F$$

So the system transfer function will be:

$$\frac{V_{out}}{V_{in}}=-\frac{1-xa_1A_1GF(j\omega)}{1-(1-x)a_1A_1GF(j\omega)}$$

Of course, x is digital code dependent:

$$=\frac{D_32^7+D_22^6+D_12^5+D_02^4+\overline{D_3}(2^3+2^2+2^1+2^0)}{2^8-1}$$

Figure.1 shows the circuit schematic diagram and **Fig.2** shows the frequency responses for various settings. To make the settings symmetrical, I used a 4-bit code with the MSB inverted and tied to the lower four bits. Due to the $x/(1-x)$ law, the increment at the filter centre frequency is 1.5dB around code 1000, rising up to 2.2dB at extremes. Of course, up to 8-bit control is possible.

Other equalizing sections are connected serially. It is possible to use two separate virtual-earth summing junctions for a parallel connection of sections and the D-to-A is then connected in the usual way, but the result is much more noisy. The serial system single-stage noise gain is low (G = 4, with no boost or cut), the noise of other stages is passed unaffected and the D-to-A noise (the dominant noise source) is filtered in one-octave bands, so a 10-band system will be as noisy as a single wideband stage. Use low impedances wherever possible and low-noise op-amps like the dual *OP227*.

The maximum input signal level is $2V_{pp}$, which should allow for boost on all stages without severe distortion and a good signal-to-noise ratio. With filters one-octave wide, some mutual influence of adjacent bands is inevitable (see **Fig. 3**). If this is undesirable, use more elaborate filters ■

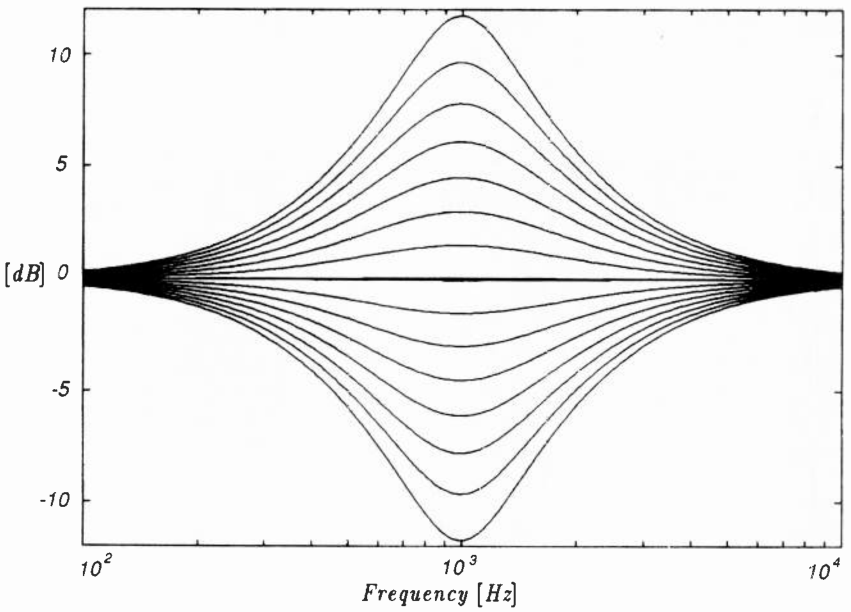


Fig.2. Frequency responses of a single 1kHz equalising section at various code values (0F, 1F, 2F, ..., 7F, 89, 90, A0, ..., F0). Maximum boost and cut is 12dB. Because of the x/(1-x) law, the steps are not equidistant; the lowest is around 1.5dB and the highest is around 2.2dB.

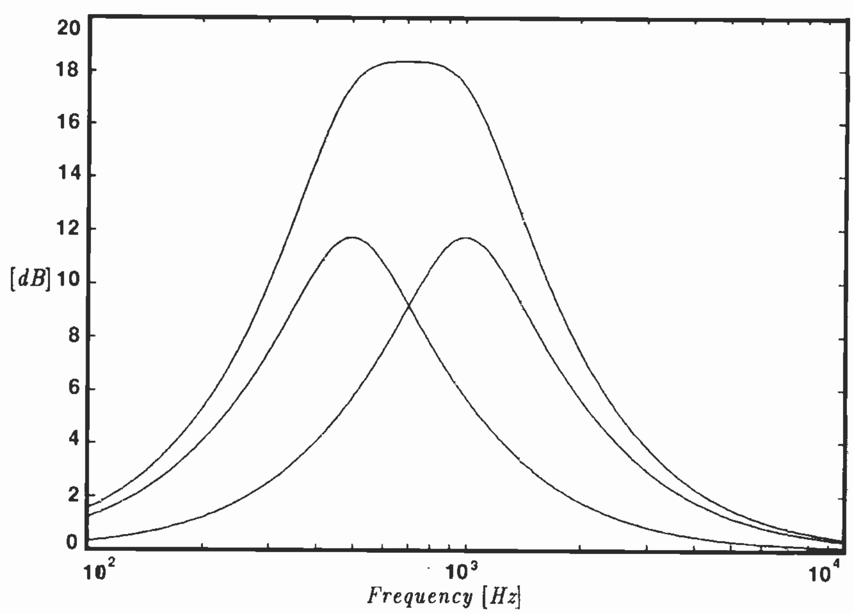


Fig.3. Interaction of two adjacent (one octave apart) sections at maximum boost. The resulting boost is 18dB. If this is undesired, more selective and more complex filter types must be used.

DESIGN BRIEF

Bringing the optoisolator into line

Ian Hickman looks at use of the Siemens IL300 optocoupler in a low-drift high-linearity isolator.

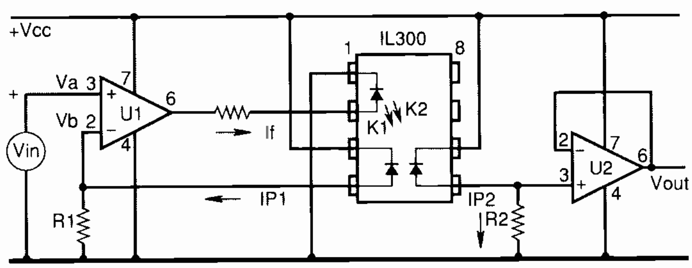


Fig. 1. Typical application circuit for the IL300 linear optocoupler, in positive-going unipolar photoconductive mode. Although K_1 and K_2 vary with temperature, their ratio K_3 is virtually temperature independent. Devices are coded into bands according to the spreads of K_1 and K_3.

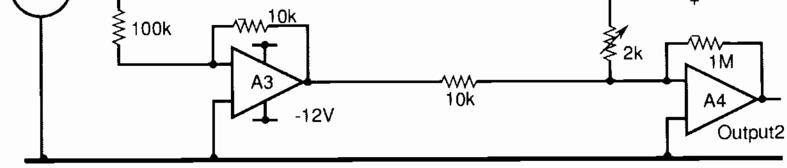


Fig. 2. Test circuit used for evaluating the IL300 operating in positive unipolar photovoltaic mode. Ideally, there should be zero resultant signal at output 2.

Carrying signals across a voltage barrier so that the signal on the output side is isolated and floating relative to the signal on the input side is a common requirement in industrial, instrumentation, medical and communications systems. Simple capacitive isolation may suffice where only AC signal components are of interest. But often DC coupling is needed, for example in the control loop of a direct-off-mains switching power supply.

Various solutions are possible. Isolation amplifiers are available as standard products in IC form from manufacturers such as Analog Devices and Burr Brown. Another method involves a V-to-F (voltage to frequency converter) to carry the signal across via a high voltage working capacitor, or using a led-photodiode link, followed by an F-to-V. But the V-to-F and F-to-V settling times introduces delays which can introduce an embarrassing phase shift into a control loop. The F-to-V and the V-to-F could be dropped, and the input signal applied using a voltage to current converter to the led, taking the output voltage from the coupled phot-diode or transistor – though ut drift and poor linearity are problems.

Low-drift high-linearity isolator

But a low-drift high-linearity isolator is available in the form of the Siemens *IL300* linear optocoupler. The coupler contains a led and a highly insulated output photodiode, and a second photodiode which is also illuminated by the led and so can be used in a feedback loop to control the led current. Ratio K_1 of the feedback (servo) photodiode current to led current is specified at a led forward current I_f of 10mA, as is K_2, the ratio of output photodiode current to led current (see the typical application circuit **Fig. 1**). The two photodiodes are pin devices whose photocurrent is linearly related to the incident luminous flux. High loop gain of the NFB loop enclosing the led and the input photodiode means Ip_1 in Fig. 1 will be linearly related to V_{in}, even though the light output of the led is not linearly related to its forward current.

The constant of linearity is slightly temperature dependent, but this affects the output photodiode equally, so K_3 (ratio of K_1 and K_2) is virtually temperature independent. Thus $V_o/V_{in} = (K_2.R_2)/(K_1.R_1) = K_3(R_2/R_1)$.

Production spreads on both K_1 and K_2 – and hence also on K_3 – mean the devices are binned into two selections for K_1 and ten for K_2. (see box, Bin sorting and categories) and coded accordingly.

Any semiconductor photodiode can be used in either of two modes, photovoltaic or photoconductive. Photoconductive mode provides the higher signal transfer bandwidth in the *IL300* and so the device's performance is specified in this mode. But photovoltaic mode provides lower offset drift and greater linearity (better than 12 bit).

Device testing

In a circuit used to test a sample device (coded *WI*) the plan was to subtract the output from a sample of the input, leaving only the distortion produced in the device under test (**Fig. 2**). This "take away the number you first thought of" technique is powerful and useful - within limits. In principle, any test signal will do, but a sine-wave is the most useful as it provides information on the order of the distortion mechanism.

A 5V pk-pk sine-wave input at 50Hz was applied to the circuit, as shown in the Channel 1 trace in **Fig. 3**. The circuit is non-inverting, so an inverting amplifier A_3 was included in the input signal sample path, to permit outphasing. After carefully adjusting the 2K potentiometer to cancel the component in the output which represented the input, the resultant distortion (measured at output *2*) is seen to be about 300µV pk-pk, allowing for the 40dB gain in A_4. This compares with a wanted signal at output *1* of about 500mV pk-pk, allowing for the "gain" of one tenth from input to output *1*. Thus the distortion – assuming it all occurs in the optocoupler with no contribution from the op-amps – is well over 60dB down and is visibly almost pure second harmonic, as would be expected from a device operated in single-ended mode. Note that to use this outphasing test method, the ground rails of the input and output circuits have been commoned. In practice, they would be totally separate, this being the purpose of an opto coupler.

Repeating the test with a 200Hz input (**Fig. 4**) produced a large fundamental component at output *2* which could not be outphased. The effect is caused by phase-shift on the optocoupler path exceeding that through the outphasing side path, which contained only one op-amp as against two and the optocoupler for the signal path. A twentieth of a degree more phase shift through one path than the other will cause a quadrature component 60dB down. It cannot be outphased by the potentiometer and is one of the limits to this technique. (Adding a balancing delay in the side path – a sniff of CR – would permit complete outphasing of the test signal, provided all frequency components of the test signal were delayed equally. This is clearly easier to arrange with a sine-wave test signal consisting of just the one frequency component.)

Applying a 20kHz 3.5V pk-pk square-wave gives some idea of the bandwidth available in the photovoltaic mode, the input and output *1* waveforms being as shown in **Fig. 5**. To control ringing, add the 10pF capacitor between output A_1 in Fig. 2 and the inverting input of A_1. Without this capacitor, each edge of the square wave shows two complete cycles of ringing at about 100kHz. The result agrees well with the 50 or 60kHz bandwidth quoted by the manufacturer and shown in **Fig. 6a**. If the two photodiodes and the led are reversed, the latter being returned to ground rather than $+V_{cc}$, the result is a negative-going unipolar photovoltaic isolation amplifier.

Bipolar operation

A bipolar photovoltaic amplifier can be constructed using two *IL300*s, with each detector and led connected in antiparallel, **Fig. 7**. The arrangement gives very low offset drift and exceedingly good linearity. But the bad news is that crossover distortion due to charge storage in the photodiodes severely limits bandwidth. Using matched K_3s, with a bipolar input signal centred on ground and taking a hefty 5% as the acceptable distortion limit, the bandwidth is typically less than 1kHz.

Bipolar operation with around 50kHz bandwidth can be achieved, with the circuit of Fig. 1, by using constant current sources to pre-bias the amplifier to the middle of its range. Internal warming of the op-amp driving current through the led is a source of zero drift in all the optocoupler circuits discussed here. It can be reduced by using an emitter follower at the op-amp's output to drive the led, shifting most of the dissipation out of the op-amp.

But in circuits using pre-bias, zero drift is also critically dependent on the quality and stability of the current sources. So photoconductive mode might be preferable with its

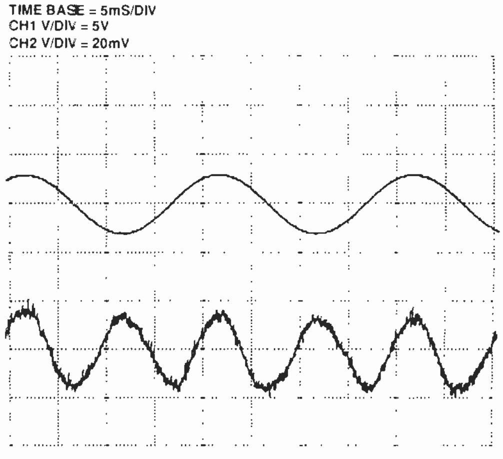


Fig. 3. 5V pk-pk 50Hz input test signal to circuit of Fig. 2 (upper trace) and outphased distortion products (lower trace).

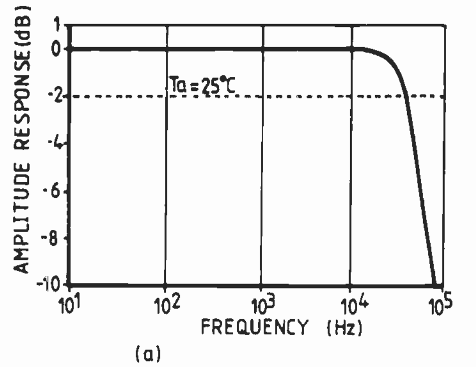


Fig. 4. As Fig. 3 but test frequency increased to 200Hz. The residual at output 2 now contains a large component at the 200Hz fundament il.

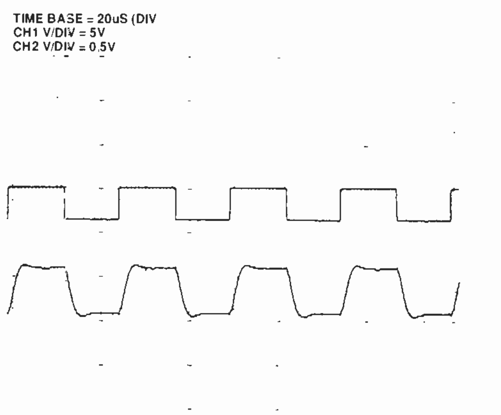


Fig. 5. Input and output 1 (Fig. 2) with a 3.5V pk-pk 20kHz square-wave input.

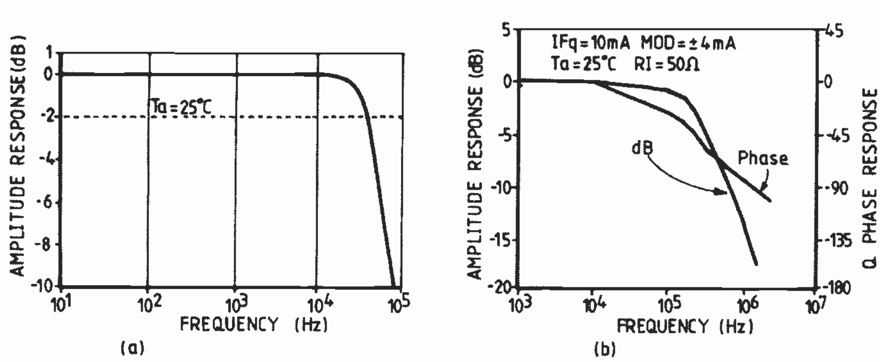


Fig. 6. (left) Bandwidth of the IL300 optocoupler: a) in photovoltaic mode b) in photoconductive mode.

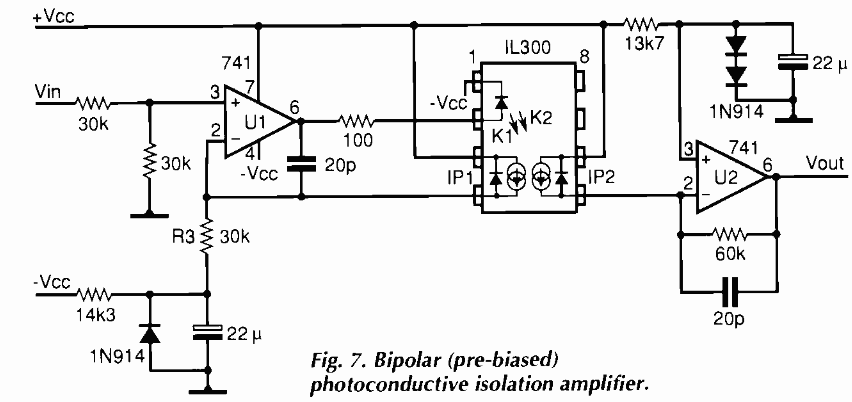


Fig. 7. Bipolar (pre-biased) photoconductive isolation amplifier.

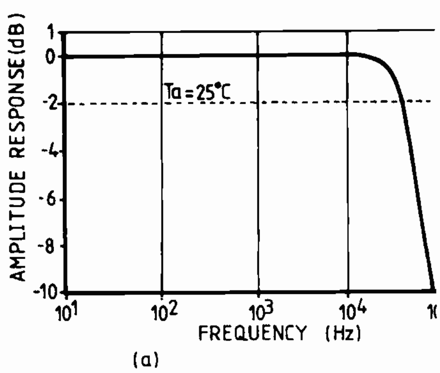


Fig. 8. Input a) and residual b) waveforms using the IL300 in the pre-biased bipolar photoconductive amplifier circuit of Fig. 7.

bandwidth in the range 100-150kHz, **Fig. 6b**.

Figure 7 shows a bipolar photoconductive isolation amplifier, using rudimentary constant voltage sources for pre-bias. Note that IP_2 flows through a 60K resistor, against 30K for IP_1, to restore the gain to unity, allowing for the 2:1 attenuation pad at the input – twice the pre-bias voltage is needed in the output circuit. This circuit was substituted for the A_1 and A_2 circuit in Fig. 2 and the 50Hz distortion test repeated. (Because the Fig. 7 circuit is inverting, amplifier A_3 in Fig. 2 is not needed and so is bypassed.) This time, the amplitude of the 50Hz input is only 4V pk-pk, **Fig. 8a**, yet the amplitude of the residual (**Fig. 8b**) is as large if not larger than in Fig. 3.

Further, its distinct triangularity indicates significant higher order distortion terms – illustrating the slightly poorer linearity of the optocoupler in the photoconductive mode.

Clearly, zero drift will also be dependent on the quality of the bias sources, which in Fig. 7 is not very good. Better performance can be expected from a circuit using devices such as the *LM313*. An even more ingenious approach is to use a second *IL300* to provide the input circuit with an offset voltage tracking that in the output circuit, **Fig. 9**.

Improving CMRR

Whether unipolar or bipolar, all the circuits discussed so far have been single ended: ie accepting an input which is unbalanced with respect to the input circuit ground. The CMRR (common mode rejection versus frequency) achieved is simply that provided by the optocoupler itself. In the case of the *IL300*, the figure is typically 130dB at 50Hz falling linearly (in terms of dB versus log frequency) to about 60dB at 100kHz.

Where the signal source is balanced with respect to the input circuit ground, a much greater CMRR can be achieved using a differential isolation amplifier. Additional isolation comes from the bridge connection of the amplifier on the output side, which combines the inverting and non-inverting inputs to provide a single ended output. Siemens[1] has published differential input circuits operating in both the photovoltaic and photoconductive modes, the former offering a bandwidth of 50kHz combined with a CMRR at 10kHz of 140dB.

Bin sorting and categories

K_1 (servo gain) is sorted into two bins, each in 2:1 ratios:
Bin *W* = 0.0036-0.0072
Bin *X* = 0.0055-0.0110
K_1 is tested at I_f = 10mA, V_{det} = 0.15V.
K_3 (transfer gain) is sorted into bins that are ±5%, as follows:

Bin *A* = 0.560-0.623
Bin *B* = 0.623-0.693
Bin *C* = 0.693- 0.769
Bin *D* = 0.769-0.855
Bin *E* = 0.855-0.950
Bin *F* = 0.950-1.056
Bin *G* = 1.056-1.175
Bin *H* = 1.175-1.304
Bin *I* = 1.304-1.449
Bin *J* = 1.449-1.610

$K_3 = K_2/K_1$. K_3 is tested at I_f = 10mA. V_{def} = 0.15V.

Bin categories
The twenty bin categories are a combination of bin sortings and indicated as a two alpha character code. The first character specifies K_1 bins, the second K_3 bins. For example, a code *WF* specifies a K_1 range of 0.0036-0.0072 and a K_3 range of 0.950-1.056.

K_1, K_3	K_1, K_3
WA	XA
WB	XB
WC	XC
WD	XD
WE	XE
WF	XF
WG	XG
WH	XH
WI	XI
WJ	XJ

The *IL300* is shipped in tubes of 50 each. Each tube contains one category of K_1 and K_3. The category of the parts in the tube is marked both on the tube and on each part.

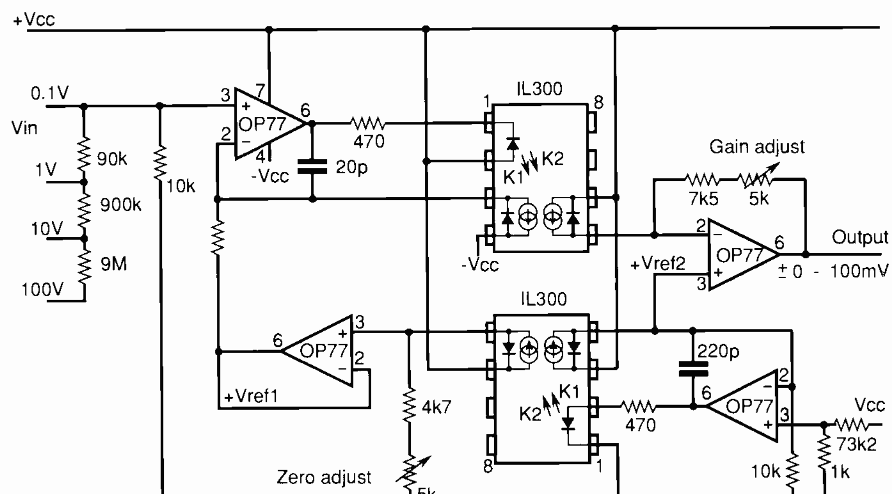
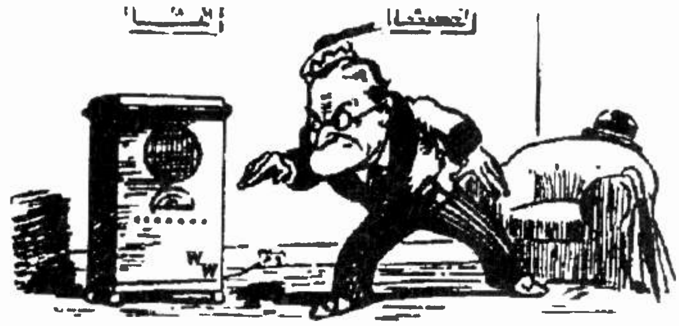


Fig. 9. Bipolar photoconductive isolation amplifier using an additional optocoupler to convey to the input amplifier the same pre-bias voltage used in the output amplifier. (

Reference
1. Designing Linear Amplifiers Using the IL300 Optocoupler Siemens Appnote 50, March 1991.



WHITE NOISE *by Hot Carrier*

Fibres, phones and fair competition

Hot Carrier HQ is now wired for cable TV. The attraction is not so much old movies and "art" films; more that the signals are free from interference from French stations during periods of high pressure – a not unfamiliar story for those on the south coast.

But one of the most important considerations was the promise of a non-BT phone service. Before cable, the only competition for BT was Mercury – a service not widely available to private households. But with a fibre optic network in place, the extra bandwidth needed to support a phone service, on top of forty TV channels, is negligible.

As a result, the number of residential customers served by the telephone networks operated by cable companies more than doubled in the first half of 1992.

Now this is all in accordance with the government's policy of competition. But while the cable TV companies are permitted to compete with BT in offering a telephone service, BT is debarred for the present – indeed for at least seven years – from the tit-for-tat offering of cable TV to its phone customers.

The government aim is to stimulate a meaningful degree of competition to BT in the domestic phone business, as fast as possible. In this context, giving the cable companies a head start is clearly no bad thing. But seven years – that's not really a

Putting the accent on electricity tariffs

Load management techniques such as off-peak tariffs, white meters, tariff 7 and even control of off-peak loads by means of inaudible signals impressed on the BBC's long wave 198kHz transmitter are as nothing compared to the radical steps taken by *Electricité de France*. There, even for domestic premises, the standing charge depends on the maximum demand. But some tariffs are much stranger, though shot through with Gallic logic. One is the *tarif effacement jours de pointe* or EJP. Here, in exchange for a low standing charge and half price electricity 24 hours a day, a consumer agrees to be *effaced* from the load on EDF's network for up to 22 days a year, between November and March. The *jours de pointe* are not known in advance, can come singly or consecutively and are signalled to the consumer by a red light, installed by EDF, glowing brightly. Consumers can still use electricity if necessary. But it will be charged at ten times the non-EJP unit charge, ie twenty times the special rate. The Hot Carrier abode has gas central heating and two standby means of powering the circulation pump – a 12 to 240V 150W inverter and a 1kW Kawasaki petrol generator. So an EJP tariff available in the UK would be just fine by Hot Carrier.

Taking the lead for greener PCBs

Many manufacturers are still happily using ozone-layer-damaging fluorocarbon-based PCB cleaning compounds while others are "thinking about doing something about it". But some have already made the break, using a no-clean approach based on new solder formulations containing special low residue fluxes. Or turning to terpenes, such as Siemens' Munich hybrid plant, in a development being supported by the German Federal Office of the Environment. Terpenes are naturally occurring extracts of various sources, including lemon peel. They exhibit extremely low evaporation losses due to their low volatility, are exceedingly effective at absorbing flux remnants and remain reusable over long periods. Furthermore, they can be extracted as a by-product from the otherwise wasted peel of lemons grown for lemon juice in the country of origin. So not only is this material biodegradable, it would still be produced anyway, whether for PCB cleaning or not. The point is that Hot Carrier culled this encouraging piece of information from Siemens' house magazine. A number of UK companies are avoiding the use of CFCs one way or another, but we don't seem to hear too much about it. In my experience, if you blow your trumpet, others will take up your tune. But if you don't, no one else will blow it for you.

Working redundant?

Until he took voluntary redundancy Greg was a components engineer. He was only a few years from normal retirement age and had been thinking about retiring early anyway. So when the call went round for volunteers following a company "merger" he duly offered to bite the bullet. As the company's only components engineer he was a little surprised to be able walk away with a pension and a handshake. Perhaps less surprisingly the company have had to take him back two or three days a week as a consultant. So did the firm immediately start training a young engineer as eventual replacement? Not a bit of it.

Unfortunately this is just the normal approach of management in the UK. Keep the ship off the rocks and don't worry about steering the best course to the destination. British managers are becoming so used to management-by-crisis that whenever the panic lifts even slightly, in their relief their thoughts turn to not to forward planning but to golf. Happy "retirement", Greg!

Best of British?

When Siemens took over parts of the old Plessey empire, the German company agreed that all employees would be no worse off, when they came to retire, than under the terms of the various Plessey pension funds. But what about good old British GEC? No such pledge has been forthcoming from this quarter concerning the ex-Plessey employees inherited by the company following the takeover. Representatives of employees and of MSF have been fighting for such a pledge – apparently with not too much success. Now Siemens has stepped in with an offer to guarantee to top-up any ex-Plessey GEC employees' pensions to a no-worse-off level. The company fears that the wrangling could go on for years, preventing formal winding up of the Plessey fund and affecting its own ex-Plessey prospective pensioners. In this extraodinary scenario, at the time of writing, GEC had not even undertaken to notify ex-Plessey staff, when they retire, of their entitlement to this Siemens top-up money. So much for British fair play.

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