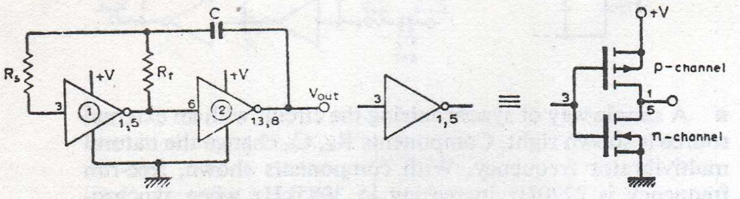
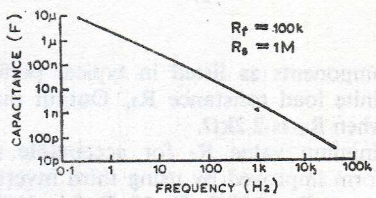
Complementary m.o.s. astable circuit



Typical performance
IC: CD 4007AE
Supply: +10V
R_f: 100kΩ; R_s: 1MΩ
C: 10μF; f: 424Hz
Load resistance: ∞
Supply current: 280μA
Square wave available at V_{out}
Output excursion: 0.03 to 9.9V
Mark-to-space ratio: 0.93
Rise time: 200ns



Circuit description

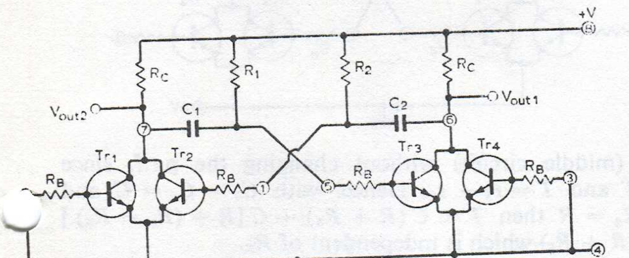
This integrated circuit package comprises three n-channel and three p-channel enhancement-type m.o.s. transistors which may be arranged to form three separate inverters. The above circuit uses two inverters, the first inverter being biased to its amplifying region by resistor R_s, and in this region the loop gain is sufficient to initiate multivibrator action. When the output of inverter 2 goes high, the input is low and the input of inverter 1 is high. As the capacitor charges up via resistor R_f, the voltage across R_f, and hence the voltage applied to the gate of the first inverter, falls. When this voltage at the junction of C and R_f passes through the threshold value of the first inverter, the output becomes high, switching the output of inverter 2 to a low state. Capacitor C will now charge in the opposite direction via resistor R_f and when the voltage at the junction of C, R_f and R_s rises towards and crosses over the threshold level, the output of inverter 1 again goes low, the output of inverter 2 is switched to the high state and the cycle repeats.

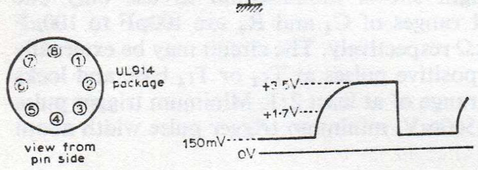
The waveform achieved is fairly symmetrical because the threshold point is close to half the supply voltage value. However, this means that the mark-to-space ratio is not unity, but this may be arranged by circuit modification. Resistor R_s also improves the frequency stability of the circuit with respect to supply voltage changes, and should be at least twice the value of R_f.

Component changes

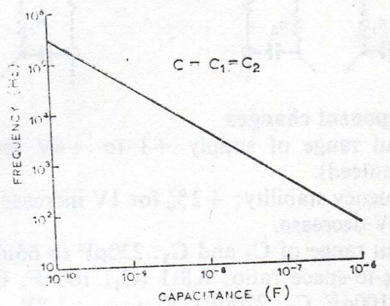
- With supply of +10V, R_f of 100kΩ, and C of 2.2nF, mark-to-space ratio varies from 0.76 to 0.92:1 for R_s from 0 to 1MΩ.

R.t.l. astable circuit





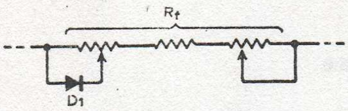
Typical performance
L914 package contains
—four 2N708-type
—R_B of 450Ω; R_C of 640Ω
External components:
R_1, R_2: 10kΩ ±5%
C_1, C_2: 100nF ±10%
Supply: 3.6V, 6.5mA
P.r.f. 699Hz (see graph)
Mark to space ratio: 1.06
V_{out1} waveform as shown

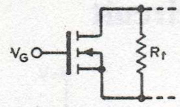


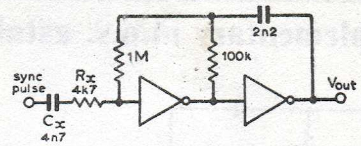
Circuit description

The L914 contains two identical resistor-transistor logic (r.t.l.) gates. In the above arrangement one input to each gate is not used, pins 2 and 3 being grounded to effectively remove Tr_1 and Tr_4 from the circuit. Transistors Tr_2 and Tr_3 are interconnected to form a cross-coupled astable which may be considered to be a two-stage amplifier with its output fed back to its input and having very high loop gain. The circuit is inherently self-starting; any dissimilarity however small between the two halves of the circuit causes one transistor to be off and the other saturated.

Consider Tr_2 on and Tr_3 off. In this state the circuit levels are: Tr_2 collector: $V_{CE(sat)}$, Tr_2 base: $V_{BE(on)}$, Tr_3 collector: +V and Tr_3 base: approx. −V due to the negative-going transition at Tr_2 collector. When switched from off to on the charge on C_1 cannot change instantaneously. C_1's charge will then change with a time constant C_1R_1, as its right-hand plate attempts to change to +V from −V. However, when this potential slightly exceeds 0V, Tr_3's base-emitter junction becomes forward-biased and it rapidly turns on, its collector voltage falling to $V_{CE(sat)}$. The negative step passes to Tr_2 base through C_2 switching Tr_2 off. The circuit is now in its other quasi-stable state. This action repeats continuously, producing antiphase square waves at Tr_2 and Tr_3 collectors. The off-times of Tr_3 and Tr_2 are given by $t_1 = 0.6931C_1R_1$ and $t_2 = 0.6931C_2R_2$ sec. The p.r.f. of the square waves is thus: $f = 1/T$, where $T = t_1 + t_2$. The mark-to-space ratio is adjustable by altering the ratio C_1/C_2 and/or R_1/R_2.







● Components as listed in typical performance data but with finite load resistance R_L. Output pulse level down by 10% when R_L is 2.2kΩ.

● Minimum value R_f for acceptable waveform: 6.8kΩ. Waveform improved by using third inverter as buffer. With R_s of zero, R_f: 6.8kΩ, C: 39pF, f is 610kHz (supply 10V). With R_s of zero, R_f: 10kΩ, C: 10pF, f is 650kHz (supply 10V). If supply is increased to 15V, f is 900kHz.

Circuit modifications

● Output waveform duty cycle may be controlled by replacing R_f with the arrangement shown left. The adjustment of this diode shunt causes the frequency of the circuit to vary, and another variable resistance can be added to compensate the change. If a 50% duty cycle is not obtained, reverse the diode D_1.

● A voltage-controlled oscillator is obtained when R_f is replaced by the arrangement shown centre. With V_G in the range 0 to +10V using an n-channel device, frequency is variable from approximately 20 to 30kHz for a supply of +10V and R_f: 10kΩ, R_s: 100kΩ and C: 2.2nF.

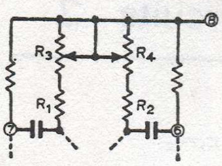
● A simple way of synchronizing the circuit with an external source is shown right. Components R_x, C_x change the natural multivibrator frequency. With components shown, free-run frequency is 2220Hz increasing to 3985kHz when synchronizing components are connected but with zero source signal. Locking frequency range approximately 22/1 but can depend on level of synchronizing pulse. Suitable pulse level 0.5 to 1.0V.

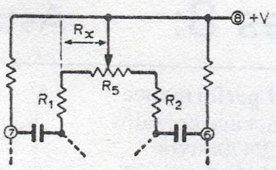
Further reading

RCA COS/MOS Digital Integrated Circuits, SSD-203A, 1973, pp. 353-9.
Low-speed astable uses c.m.o.s., *Electronic Components*, 6 April, 1973, p. 294.
Clock oscillator for telemetry systems uses c.m.o.s. chip to minimize power drain, *Electronic Design*, vol. 20, 1972, p. 84.

Cross references

Series 8, card 3.
Series 3, card 11





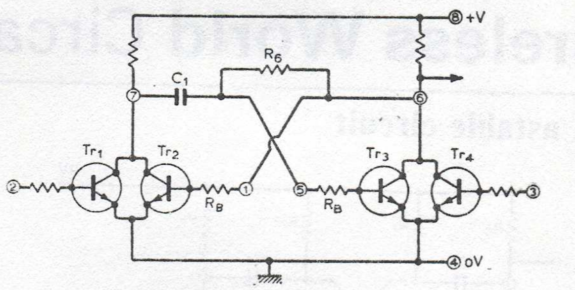
Component changes

Useful range of supply +1 to +6V (exceeds rating, not guaranteed).
Frequency stability: +2% for 1V increase in supply, −3.5% for 1V decrease.
Useful range of C_1 and C_2: 220pF to 66μF (p.r.f. ≈ 1.4Hz).
Mark-to-space ratio: 6.8:1 (C_1: 100nF, C_2: 22μF) to 1.8:5 (C_1: 100nF, C_2: 220pF), $V_{out(max)}$: 1.8V.
Useful range of R_1 and R_2: 2.2kΩ $V_{out\,(max)}$: 2.8V to 33kΩ (V_{out} distorted in "0V" region).
Complementary square wave is available at V_{out2}.
At either output $V_{out(max)}$ falls by 10% when loaded with 4.7kΩ.

Circuit modifications

● As p.r.f. and mark-to-space ratio depend on the C_1R_1 and C_2R_2 time constants, a variable-frequency square wave is obtained by switching in different, but equal, values of capacitance and varying the p.r.f. continuously with R_1 and R_2 in the form of ganged potentiometers. See circuit left, where R_1, R_2 are 2.2kΩ and R_3, R_4 are 22kΩ. If only one resistor is variable, the mark-to-space ratio is variable but so also is the p.r.f.

● A modification allows the mark-to-space ratio to be made greater or less than unity by adjusting the position of the slider of R_5 (middle circuit) without changing the p.r.f. since $f = 1/T$ and $T = t_1 + t_2$. Hence, with $C_1 = C_2 = C$ and $R_1 = R_2 = R$ then $T \propto C\,(R + R_x) + C\,[R + (R_5 - R_x)]$ $\propto C\,(2R + R_5)$ which is independent of R_x.



● Circuit on right shows modification to use only one capacitor. Useful ranges of C_1 and R_6 are 100pF to 100μF and 470Ω to 100kΩ respectively. The circuit may be externally synchronized by positive pulses at Tr_1 or Tr_4 base and locks over a frequency range of at least 2:1. Minimum trigger pulse amplitude about 500mV, minimum trigger pulse width about 200ns.

Further reading

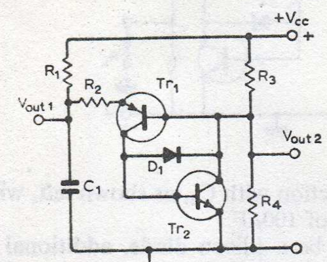
Fenwick, P. M., Pulse generator using r.t.l. integrated circuits, *Radio and Electronic Engineer*, 1969, pp. 374-6.
Bowes, R. C., Improved crosscoupled multivibrator controllable in frequency over a wide range, *Electronics Letters*, vol. 7, 1971. pp. 181/2.

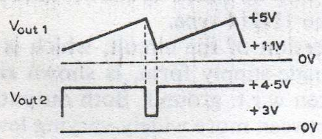
Cross references

Series 8, cards 8, 12.

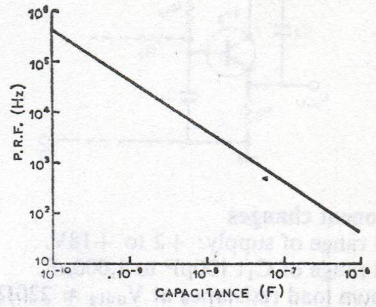
Wireless World Circard Series 8: Astable Circuits 3

Complementary astable circuit





Typical performance
Supply: +9V, 4.5mA
Tr_1: BC126; Tr_2 BC125
Diode: HP5082-2800
R_1: 27kΩ; R_2: 47Ω
R_3, R_4: 1kΩ, C_1: 10nF
P.r.f. 6.1kHz
Mark-to-space ratio: 49:1
Rise time of V_{out2}: 1.2μs



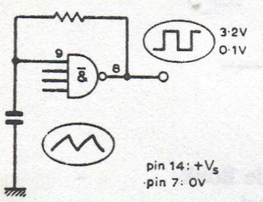
Circuit description
When the supply is connected, Tr_1 base and Tr_2 collector are at a potential determined by the ratio R_4/R_3, which could be in the form of a potentiometer to set the upper level of V_{out1} and V_{out2}. The p.d. across C_1 is zero, so the base-emitter junction of Tr_1 is reverse-biased and both transistors are cut off. Capacitor C_1 begins to charge exponentially with time constant C_1R_1 causing the p.d. across it to rise towards $+V_{cc}$. When the capacitor voltage slightly exceeds the base potential of Tr_1 the base-emitter junction begins to be forward-biased, significant conduction occurring when the capacitor voltage is approximately 0.5V more positive than Tr_1 base.

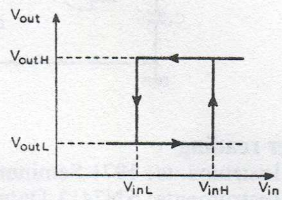
Positive feedback, due to the interconnection of the bases and collectors of the complementary pair of transistors, ensures that this transition to the on-state is very rapid. Thus C_1 discharges through Tr_1 and Tr_2 with R_2 providing a discharge current-limiting action. Diode D_1 prevents the transistors saturating and ensures that the circuit can re-cycle.

The capacitor does not completely discharge, but as the current in the transistors falls the loop gain around Tr_1 and Tr_2 reduces to a value that cannot maintain conduction, which ceases when Tr_1's emitter voltage falls to about 1V. Both Tr_1 and Tr_2 rapidly switch off allowing C_1 to recharge through R_1 and V_{out2} returns to its initial value determined by R_4/R_3. During the discharge of the capacitor, a narrow negative-going pulse is obtained at the junction of R_3 and R_4 due to the conduction of Tr_2.

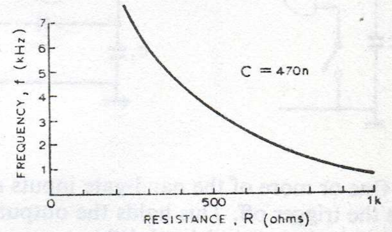
Wireless World Circard Series 8: Astable Circuits 4

T.t.l. Schmitt astable circuit





Typical performance
IC: ½ SN7413
Supply: 5V
R: 330 ±5%
C: 220nF ±5%
f: 10.8kHz
Mark-to-space ratio: 0.5:1

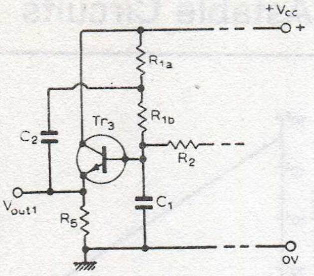


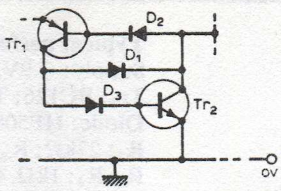
Circuit description
This circuit is internally constructed to behave as a Schmitt trigger, i.e. having two distinct output states, switching between them according to the voltage at the input, with a constant hysteresis between the input levels for switching. The relationship between the input and output states is shown above. The output remains low for $V_{inH} > V_{in} > V_{inL}$. When the input level exceeds V_{inH}, the circuit enters its active region, the action is regenerative, and the output becomes V_{outH} and would remain at this level until the input voltage was reduced to less than V_{inL}.

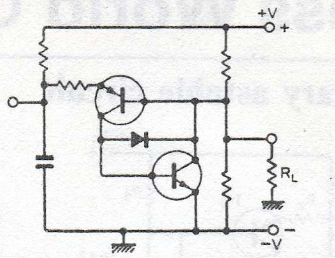
In the circuit, a convenient starting point of the output high and the input low may be assumed. The capacitor will tend to charge up towards the output voltage, but when the capacitor voltage reaches the transition level for the i.c., the output falls to near zero voltage. The capacitor then discharges through R until its potential reaches that at which the reverse of the output states occurs, where the output again goes high.

Component changes
Useful range of R: 220 to 1000Ω. Astable will not function for R ⩾ 1.5kΩ.
Useful range of C: 2.2nF to 22μF.
Useful range of supply: 4.5 to 5.5V. Operation outside this rated range is possible, but performance not guaranteed. Typically with R: 680Ω and C: 470nF, frequency range is 1.9 to 2.4kHz for supply ranging from 3.5 to 7V.
For supply of 4.5 to 5.5V, frequency stability is approximately ±3%/V.
Circuit will supply loads from infinity down to 1kΩ, with a reduction of frequency of less than 2.5%.

Circuit modifications
- Normally the four inputs of the input nand gate may be used in parallel or taken to the supply rail.







Component changes
Useful range of supply: +2 to +18V.
Useful range of C_1: 100pF to 1,000μF.
Minimum load resistance at $V_{out2} \approx 220\Omega$.
Frequency stability: +0.3%/V increase in supply.
Tr_1: ME0413, 2N3906, BCY71
Tr_2: ME4103, 2N3904, BC107.

Circuit modifications

- Replacing R_3 and R_4 by a potentiometer across the supply changes the value of the capacitor voltage required to trigger the transistors into conduction and hence controls the period and amplitude of the output waveforms for given values of C_1 and R_1.
- Narrow positive-going pulses in antiphase with those at V_{out2} can be obtained by including a small resistor in series with Tr_2 emitter to the 0-V rail.
- The 'exponential' waveform, V_{out1}, can be made into a more linear sweep by replacing R_1 with a constant-current source. This sweep output can be extracted without significant loading by using an emitter follower. Linearity of the sweep output may be improved by splitting R_1 into R_{1a} and R_{1b} and bootstrapping their junction with C_2, as shown left, where C_2 should be of the order of 100μF.

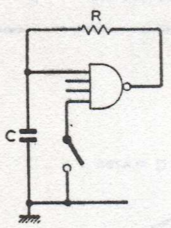
If D_1 is required to be a silicon diode, additional silicon diodes D_2 and D_3 should be added as shown centre where all diodes could be of the 1N914-type.

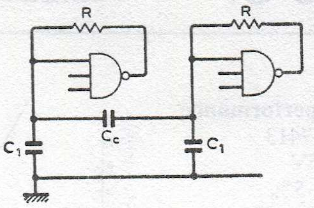
- A dual-supply version of the circuit, which is otherwise identical with the single-supply form, is shown right where both outputs are taken w.r.t. ground. Both outputs can then be made to switch between more widely-varying levels and by adjusting the ratio R_4/R_3 to set Tr_1 base to zero volt in the off-state, negative pulses may be obtained at V_{out2}.

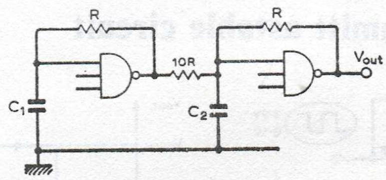
Further reading

Hemingway, T. K., Electronic Designer's Handbook, section 15, Business Publications, 1967.
Thomas, H. E., Handbook of Electronic Circuit Design Analysis, Reston Publishing Co. Inc., 1972, pp. 41-7.
Coers, G., Astable multivibrator needs only one capacitor, *Electronics*, vol. 46, 18 Jan. 1973, p. 171.

Cross references
Series 2, cards 5, 12. Series 3, card 6.
Series 6, card 8. Series 8, card 1.







- One or more of the nand-gate inputs may be grounded to gate the trigger off. This holds the output permanently in the high or logic 1 state (circuit left).
- Two such circuits operating at different frequencies may be locked by capacitive coupling between junctions of C, R elements. The coupling capacitor might be typically $C_1/10$, where C_1 is the smaller of the two multivibrator capacitors (circuit middle).
- A further interconnection is shown right. Assume that the first oscillator frequency is lower than the second. When the first output is high, C_2 charges at a faster rate when the second oscillator output is high, and also then discharges more slowly when V_{out} goes down, thus giving alternate signal outputs of low mark-to-space ratio, followed by high mark-to-space ratio.

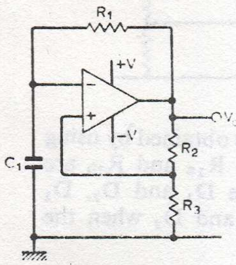
Further reading

Texas Instruments: 1971 Seminar Slide Book.
Texas Instruments: SN7413 Data Sheet.

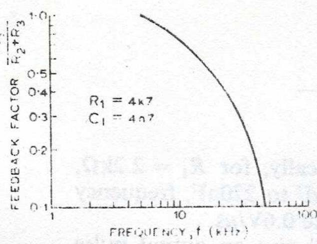
Cross references
Series 2, cards 3, 8.
Series 8, card 10.

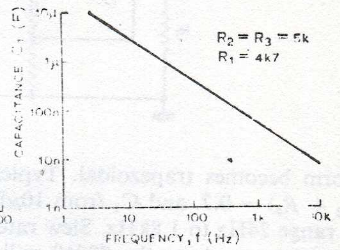
Wireless World Circard Series 8: Astable Circuits 5

Operational amplifier astable circuit



Typical performance
IC: 301
Supply: ±15V
C_1: 4.7nF ±5%
R_1: 4.7kΩ ±5%
R_2, R_3: 5kΩ ±5%
Output square wave: 28V pk-pk
Slew rate: 8V/μs
Variation of frequency with feedback factor and capacitance C_1 shown on graphs.



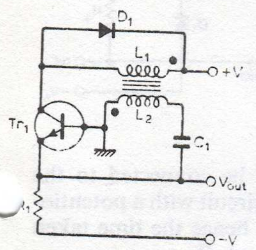


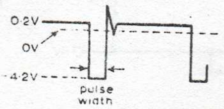
Circuit description
The circuit shown uses an operational amplifier where the output switches between the positive and negative saturation levels of the amplifier, giving a square wave output. The period of the waveform depends on the time constant C_1R_1 and the feedback factor, determined by the ratio of $R_3/(R_2 + R_3)$. Assume the output has switched to the positive saturation level; the voltage at the non-inverting input is $+V_{sat}R_3/(R_2 + R_3)$ and the voltage at the inverting input is negative with respect to this value. However capacitor C_1 now begins to charge towards $+V_{sat}$, but when the capacitance voltage is almost equal to the feedback voltage, the amplifier comes out of saturation, and the regenerative action due to the positive feedback drives the amplifier quickly into negative saturation before the capacitance voltage can alter. C_1 will now charge towards $-V_{sat}$, but again a rapid transition to the positive saturation state will occur when the voltage across C_1 reaches $-V_{sat}R_3/(R_2 + R_3)$, and the cycle repeats. The duty cycle of this astable circuit is almost independent of the pulse repetition frequency, because the threshold levels are fairly well specified to each op-amp.

Component changes
Useful range of R_1: 6.8k to 2.2kΩ.
Useful range of C_1: 10μF to 4.7nF for R_1 = 4.7kΩ.
Frequency stability: For C_1: 22nF, R_2, R_3: 5kΩ, R_1: 4.7kΩ, supply of ±15V and f = 4470Hz, decreasing supply to ±10V reduces frequency by <1%.
Operation possible down to ±3V; frequency down by 8%.
Any other operational amplifier may be used, e.g. 741, but frequency range restricted because at higher frequencies

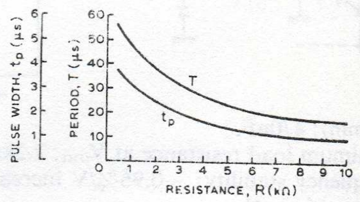
Wireless World Circard Series 8: Astable Circuits 6

Astable blocking oscillator





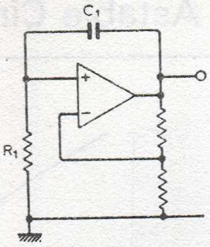
Typical performance
Supply: +10V, 860μA, −3V 1.1mA
Tr_1: BC125, D_1: SP2
R_1: 6.8kΩ; C_1: 4.7μF
L_1: 30 turns of 36 s.w.g. en. Cu
L_2: 15 turns of 36 s.w.g. en. Cu; both on FX2049 ferrite core.
P.r.f.: 46.6kHz
Pulse width: 1.15μs



Circuit description
Many multivibrators have their timing determined by the interval for which an energy storage element holds an active device in the off state. The output pulse is then available at a high output resistance point, at a low power level, and its rise and fall times are significantly influenced by stray capacitance. The blocking oscillator is an example of circuits which overcome these problems by timing the output pulse within the low output resistance, high-current, saturation region by use of a transformer to provide positive feedback with a loop gain greater than unity. Successful design depends on correct choice of the transformer, which should have small stray capacitances and a magnetizing inductance much larger than its leakage inductance. These requirements can be met by making the transformer physically small, interleaving the windings and using a high-permeability core.

At switch-on the base-emitter junction is forward-biased and the collector current rapidly rises to almost equal the emitter current which depends on R_1 and −V. The transformer ensures that a much larger emitter current flows to saturate Tr_1 and C_1 charges in a direction that reverse-biases the base-emitter junction causing Tr_1 to cut-off. A very narrow pulse is generated and the circuit will not regenerate until C_1 has discharged through R_1. When Tr_1 cuts off D_1 protects the base-collector junction from the large induced e.m.f. in L_1 and restricts V_{CB} to +V. Capacitor C_1 should be large enough to ensure that the magnetizing inductance of L_1 controls the pulse width and C_1 controls the off-time. The pulse width depends on C_1 rather than L_1 if C_1 is too small.

Component changes
Useful range of +V: +4 to +14V; $-V_{min}$: −1V.
Useful range of R_1: 470Ω to 10kΩ.

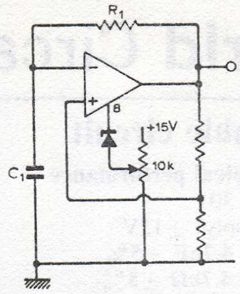


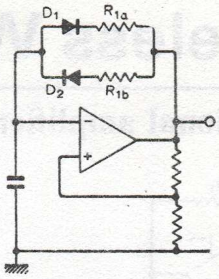
waveform becomes trapezoidal. Typically, for $R_1 = 2.2k\Omega$, $R_3/(R_2 + R_3) = 0.7$ and C_1 from $10\mu F$ to 220nF, frequency in the range 24Hz to 1.8kHz. Slew rate $0.6V/\mu s$.

A comparator such as the 72710 will give an output pulse excursion of −0.5 to +2.8V for supplies of +12V and −6V. For R_2, R_3: $5k\Omega$, useful range of R_1 is 1.5k to $6.8k\Omega$ and C_1 47pF to $22\mu F$ giving frequencies in the range 630kHz to 3Hz.

Circuit modifications

- Interchange C_1, R_1 and the input connections as shown left. For similar component values as in main diagram, frequency is reduced to approximately one third. Note that the derivative of square-wave output is obtained at the non-inverting input.
- Output levels may be clamped for driving t.t.l. loads by connecting a zener diode/resistance network across the output. Clipping at much lower current levels is possible with some amplifiers (e.g. 301), where access is available to the drive point of the output stage. An adjustable arrangement is shown in the middle circuit.





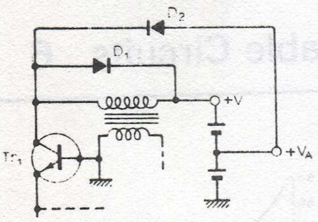
- An unequal mark-to-space ratio may be obtained by using the circuit shown right. The two resistors R_{1a} and R_{1b} are selected by the switching action of diodes D_1 and D_2, D_1 conducting when the output is negative, and D_2 when the output is positive.

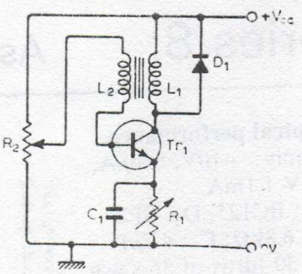
Further reading

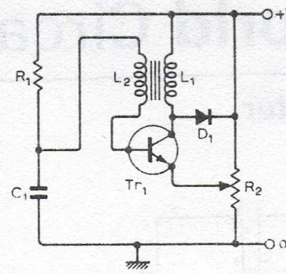
Clayton, G. B., Operational Amplifiers, *Wireless World*, vol. 75, 1969.

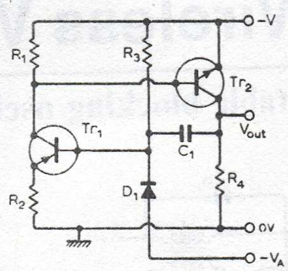
Shah, M. J., Feedback pot extends multivibrator duty cycle, *Electronics*, September, 1971, p. 62.

National Semiconductor application note AN4-1.









C_1(min): 470nF.

Minimum load resistance at V_{out}: $2.2k\Omega$.

Frequency stability: −0.96%/V increase in +V, −0.77%/V increase in −V.

Circuit modifications

- It is often convenient to obtain the output pulse from a third winding L_3 to provide d.c. isolation, a suitable transformer turns ratio for L_1, L_2 and L_3 being n:1:1.
- A diode D_2 can be connected as shown left to prevent saturation of the transistor. As the collector current increases during switch-on, the collector voltage falls until it reaches $+V_A$ causing D_2 to conduct clamping the collector at approximately $+V_A$. The current shunted from the collector by D_2 decreases as that in the magnetizing inductance of L_1 increases, the on period of Tr_1 ending when the diode current falls to zero.
- Middle left circuit shows a single-supply version of the circuit with R_1 and C_1 in the emitter. The R_1C_1 time constant determines the time for which Tr_1 is off and hence the mark-to-space ratio can be varied by means of R_1. Alternatively, the p.r.f. may be adjusted by means of R_2 which controls the base potential and hence the timing of the off/on transition.
- The R_1C_1 timing components may be connected to the base of Tr_1 as shown in the middle right circuit with a potentiometer R_2 fixing the emitter voltage and hence the time taken for Tr_1 to switch on as C_1 charges through R_1.
- An R-C circuit capable of producing very narrow pulses and very small mark-to-space ratio is shown right. Pulse widths of around 250ns with a mark-to-space ratio of at least 1/100,000 are obtainable with −V of −6V, $-V_A$ of −0.5V, Tr_1: BSX29; Tr_2: BSY17; D_1: EA828; R_1: $100k\Omega$, R_2, R_4: 50Ω, R_3: $2M\Omega$ and C_1: 50nF.

Further reading

Linwill, J. G. & Mattson, R. H., Junction transistor blocking oscillators, *Proc.I.R.E.*, 1955, pp. 1632-9.

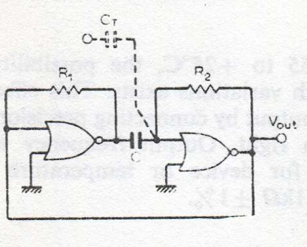
Strauss, L., Wave Generation and Shaping, Chap. 12, McGraw-Hill, 1960.

Fontaine, G., Transistors in Pulse Circuits, Chap. 10, Philips, 1971.

Tesic, S., Multivibrator with very small mark-to-space ratio, *Electronic Engineering*, 1967, pp. 671-3.

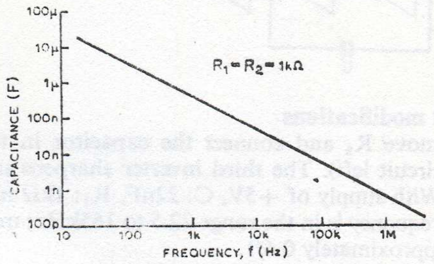
Wireless World Circard Series 8: Astable Circuits 7

T.t.l. dual inverter astable circuit



Circuit description
Capacitor C_1 alternately charges and discharges through R_2 because loop gain of the system ensures that the output of the second inverter switches between logic 0 and logic 1 states. When the potential difference with respect to ground at the input of I_2 crosses the critical level. Resistor R_1 is necessary to bias the first inverter I_1, and thus prevent the possible stable state of inverter I_1 output at almost 0V in the logic zero state, and the output of I_2 in the logic 1 state. Charge and discharge cycles have different durations because the input switching level is not symmetrical with respect to the output 0 and 1 states, and also there is an additional charging path for the input of the second inverter at 0 state. Note that when using nor gates as inverters, the unused input should be tied to logic 0 voltage level.

Typical performance
Supply: +5V
IC: ½ 7402
R_1, R_2: 1kΩ ±5%
C: 100pF ±5%
Frequency: 2.78MHz
Stability > ±1% for supply in the range 4.75 to 5.25V for a span of 3kHz to 3MHz



Component changes
Useful range of C: 100pF to 22µF.
Useful range of R_1: 220Ω to 1kΩ.
Useful range of R_2: 150Ω to 1kΩ.
Alternative IC: SN7404 hex inverter.
Circuit operates within the supply range 4.5 to 6V, but not guaranteed outside t.t.l. voltage limits.
In an attempt made to achieve high frequencies, the range of resistance values is critical. Typical values R_1: 1kΩ, R_2: 330Ω, C: 120pF, f: 6.7MHz. With nor or nand gates, a spare input is available for external synchronization. Frequency will lock over the range of 4:1 with input pulse widths down to 100ns (positive-going pulse for nor, and negative-going for nand). Capacitive coupling of the trigger source may be used with the inverters of SN7404. Typically $C_T = C/100$. Three separate, harmonically-locked astables can then be produced.

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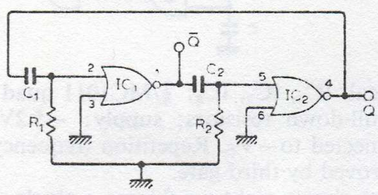
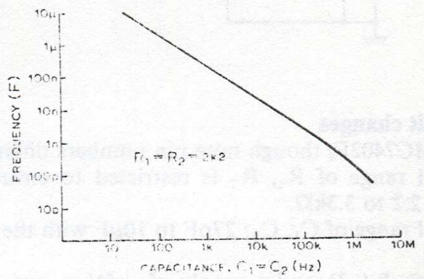
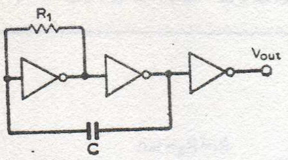
Coupled logic gates astable circuit

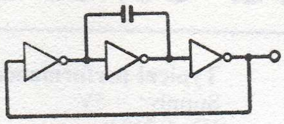


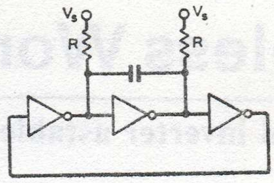
Circuit description
The values of the current sinking resistors R_1 and R_2 are critical in this type of circuit, which uses nor logic gates in a cross-coupled mode. It is possible for both gate inputs to sink logic 0 level input currents simultaneously, and this produces a stable state in which both outputs are at logic 1. To avoid this choose values of R_1 and R_2 so that the gate input levels are near the logic threshold level; as the capacitors go through their charging cycles, one gate will be above and one below the threshold level. Assume the Q output has changed from the 0 to 1 logic level of approximately +3V due to the input having reached the threshold value. This output transisition is coupled through the capacitor C_2 to make the input of the first gate high, and hence the output Q is low or logic 0. As C_2 charges up towards the positive supply via R_2, the voltage across R_2 and hence the input level at the first gate decreases. At the same time C_1 charges via the base resistor of the input transistor of the gate. The output will change state at a time dependent on whichever gate input first crosses the threshold level. Output Q will then be high (approximately +3.0V) and Q low. Capacitor C_1 will now tend to charge in the opposite direction towards d.c. supply via R_1, and C_2 also charges in the opposite direction via the input transistor of the first gate until the outputs change state, then the cycle repeats.
Frequency of oscillation is determined by C_1, C_2, R_1 and R_2. If $C_1 = C_2 = C$, $R_1 = R_2 = R$, the frequency is approximately $1/2CR$ (Hz) C is in farads and R in ohms. Provided resistors are carefully chosen to ensure self-starting, a wide range of frequencies are available by carrying C_1 and C_2. This type of circuit using standard gates or inverters does not provide stable frequencies as the threshold voltages depend on temperature and supply voltage.

Typical data
Supply: +5V
ICs: ½ SN7402N
R_1, R_2: 2.2kΩ ±5%
C_1, C_2: 0.1µF ±5%
Frequency: 2015Hz
Mark-to-space ratio: 1.27:1
Pulse excursion: 0.3 to 3.2V
Connect unused inputs to ground for inverter operation.









Circuit modifications

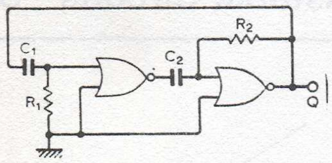
- Remove R_2 and connect the capacitor in the feedback loop (circuit left). The third inverter sharpens up the waveform. With supply of +5V, C: 22nF, R_1: 1kΩ max. to 100Ω min., frequency is in the range 22.5 to 165kHz; mark-to-space ratio approximately 0.6/1.
- Middle circuit uses the SN7404 again, where frequency of oscillation is determined by the propagation delays through the gates. The external capacitance changes the delay associated with two gates and thus alters the frequency. Useful range of C: 1 to 10nF. Frequency 4 to 0.5MHz. Waveform essentially square, but deterioration evident above about 3MHz. Frequency stability fairly poor. Approximately ±10%/V.
- Tuning resistors in the middle network comprise the integrated circuit resistors. With perhaps resistance variations of ±20% from device to device, and a like tolerance over the temperature range −55 to +25°C, the possibility of frequency and pulse width variations exists. This effect can be minimized for a given output by connecting precision external components as shown right. Output frequency may then remain within ±5% for device or temperature changes. Typically R should be 1kΩ ±1%.

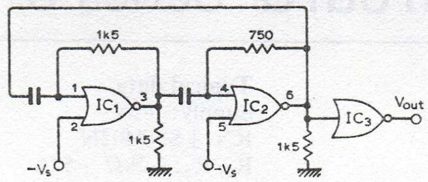
Further reading

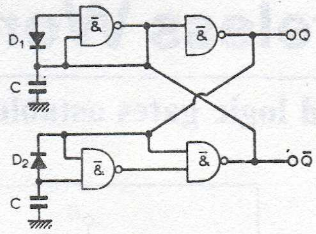
Malmstaat and Enke, Digital Electronics for Scientists, Benjamin, 1969.
Wide range multivibrator costs just 25c to build, *Electronics*, 1971, p. 59.
MDTL Multivibrator Circuits, Motorola application note AN-409.

Cross reference

Series 8, card 8.







Circuit changes

Use MC7402F, though note pin numbers different.
Useful range of R_1, R_2 is restricted to ensure that circuit starts 2.2 to 3.3kΩ.
Useful range of C_1, C_2: 27pF to 10μF with the above resistor values.
With C: 0.1μF, and a supply of +5V, a variation of supply voltage of ±5% produces a percentage frequency change of +5% or −9% respectively.
Nand gates may be used in place of nor gates. In this case, unused pins should be connected to the positive supply line.
Waveform of basic astable circuit is improved when the output is applied through an additional gate.
Mark-to-space ratio adjustable by having different values of C_1 and C_2.

Circuit modifications

- Range of resistance values for R_1 and R_2 ensuring self-starting increased slightly, if R_2 is taken to output (left). Range then 1.5 to 3.3kΩ.
- Emitter-coupled logic gates in the middle configuration can provide a high frequency signal, but the component values tend to be critical. IC_1, IC_2, IC_3: ¼/MC1011 quad-nor gates using 1.5kΩ pull-down resistors; supply: −5.2V. Unused input pins connected to $-V_S$. Repetition frequency 25MHz. Waveform improved by third gate.
- Arrangement shown right would use a single quad two-input nand gate, useful C range being 10pF to 1μF. Self-starting problem may be overcome with an extra gate, but a 3-input nand gate then required (cf. Mullard).

Further reading

Integrated Logic Circuit Applications Mullard FJ Range, Mullard Ltd., 1968.
Malmstadt & Enke, Digital Electronics for Scientists, Benjamin., 1969.
2MHz Square Wave Generator uses two TTL gates, p. 110, 400 ideas for design, vol. 2, Hayden.
Simple clock generator has guaranteed start-up. *Electronic Design*, vol. 13, 1971, p. 86.

Cross reference

Series 8, card 7.

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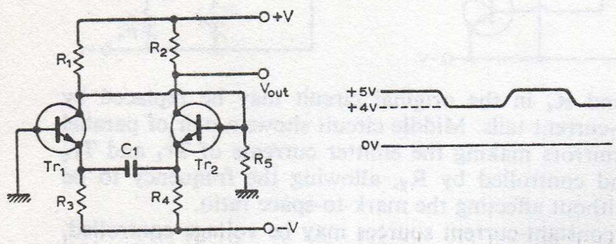
Emitter-coupled astable circuit



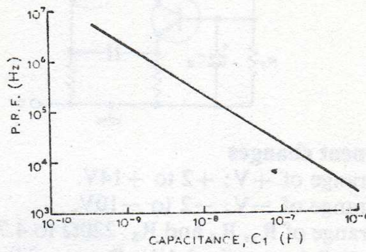
Circuit description
Compared with a conventional saturating, cross-coupled astable circuit, this emitter-coupled circuit uses a single timing capacitor, is capable of producing an improved output waveform, can operate at higher frequencies and can be designed to provide a much better frequency stability. The higher switching speeds are obtained because neither transistor is allowed to saturate and the output waveform does not switch between wide limits.
Consider the circuit to be in the state of Tr_2 off and Tr_1 on. The emitter current of Tr_1 divides into a component in R_3 and a charging current in C_1 and R_4. At the instant that Tr_1 switches on this charging current produces negligible p.d. across C_1 and a p.d. across R_4 sufficiently large to ensure that Tr_2 is off. As C_1 charges, its p.d. increases and that across R_4 falls until the base-emitter junction of Tr_2 becomes forward-biased. Transistor Tr_2 begins to conduct and the emitter current of Tr_1 falls causing the collector potential of Tr_1 and the base potential of Tr_2 to rise. This action causes Tr_2 to conduct more heavily and Tr_1 to switch off. This sequence is then repeated with Tr_2 emitter providing the current to charge C_1 through R_3 until the switching action restores the circuit to its original state of Tr_2 off and Tr_1 on.
Tr_1 will be on for a time:

$$t_1 = C_1R_1R_5\,(R_3 + R_4)/R_3(R_1 + R_5) + R_1R_5$$

and Tr_2 will be on for a time:

$$t_2 = \frac{C_1(R_3 + R_4)}{\left[\frac{+V}{1 - V\,1 - V_{\mathrm{BE\,on}}}\right]\left[\frac{R_4}{R_1} - \frac{R_5}{R_1 + R_5}\right] + \frac{R_4(R_1 + R_5)}{R_1R_5} - \frac{R_4}{R_3} - 2}$$

Typical performance
Supplies: +5V, 6.4mA; −5V, 2.5mA
Tr_1, Tr_2: 2N706
R_1, R_2, R_5: 470Ω
R_3: 3.3kΩ; R_4: 4.7kΩ
C_1: 1.5nF
P.r.f.: 1MHz
Mark-to-space ratio: 1.04:1
Rise and fall time: ≈30ns



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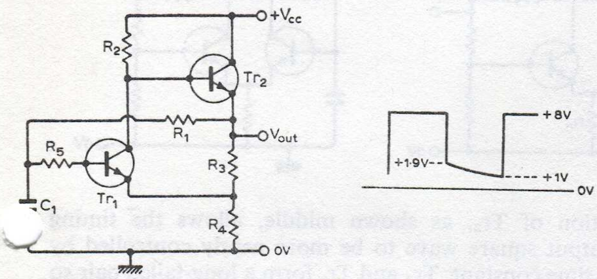
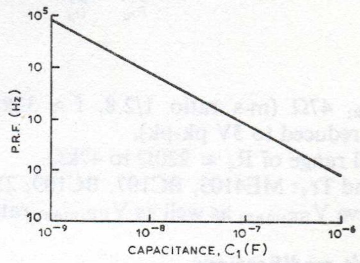
Discrete-component Schmitt astable

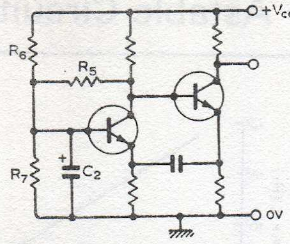


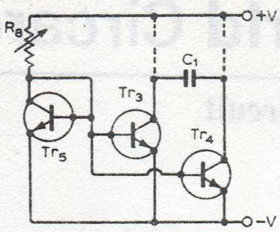
Circuit description
This circuit is a Schmitt trigger with overall feedback provided via R_1 and C_1. Consider C_1 to be uncharged, then when the supply is connected Tr_2 emitter is initially at 0V but Tr_2 immediately conducts due to the base drive through R_2. Thus Tr_2 emitter rapidly switches to a level close to $+V_{cc}$ and, with $R_3 = R_4$, Tr_1 emitter rises to half this value. However, Tr_1 remains cut off due to the lack of base drive. Capacitor C_1 begins to charge "exponentially" through R_1 aiming to reach the emitter potential of Tr_2, but when the capacitor voltage exceeds that at Tr_1 emitter the capacitor begins to discharge mainly through R_1, R_3 and R_4 and partially through R_5, Tr_1 base-emitter junction and R_4 driving Tr_1 on and into saturation.
The collector potential of Tr_1 falls to a low value as also does Tr_2 emitter, their being insufficient p.d. available to keep Tr_2 in conduction so that it switches off. C_1 continues to discharge until Tr_1 comes out of saturation, when its collector potential rises sharply. This rise is transferred to Tr_2 emitter, which begins to conduct, and hence to the emitter of Tr_1. This positive feedback rapidly cuts off Tr_1 leaving Tr_2 in full conduction until, as C_1 charges again through R_1, the higher potential needed at Tr_1 base to restart the cycle is attained.

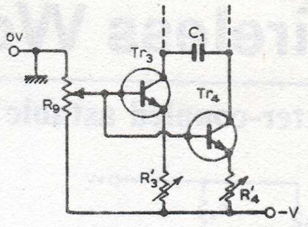
Typical performance
Supply: +9V, 5.6mA
Tr_1, Tr_2: 2N706
R_1: 10kΩ; R_2: 4.7kΩ
R_3, R_4: 470Ω
R_5: 2.2kΩ; C_1: 10nF
P.r.f.: 9.83kHz
Mark-to-space ratio: 1.13/1
Rise time: 400ms
Fall time: 300ns



Component changes
Useful range of $+V_{cc}$: +4 to +15V.
Useful range of C_1: 100pF to 1000μF.
Frequency stability: −0.46%/V increase in $+V_{cc}$.
$R_{1(min)}$ 470Ω (m-s ratio 1/5), $R_{1(max)}$ 1MΩ (m-s ratio 48/1).
$R_{2(min)}$ 680Ω (p.r.f.: 77kHz), $R_{2(max)}$ 100kΩ (V_{out} reduced to +5.2V).
$R_{3(min)}$ 47Ω (m-s ratio 5/1), $R_{3(max)}$ 2.2kΩ (m-s ratio 1/3, f ≈ 31kHz).







Component changes
Useful range of +V: +2 to +14V.
Useful range of −V: −2 to −10V.
Useful range of R_1, R_2 and R_5: 220Ω to 4.7kΩ.
$R_{3(min)}$ 1kΩ (m-s ratio 3.4/1), $R_{3(max)}$ 27kΩ (m-s ratio 1/10).
$R_{4(min)}$ 1kΩ (m-s ratio 1/4), $R_{4(max)}$ 33kΩ (m-s ratio 8/1).
Useful range of C_1: 180pF to 1000μF.
Frequency stability: −1.2%/V increase in +V, −6%/V increase in −V.
Tr_1 and Tr_2: ME4103, 2N708, HE301, BSY95A.

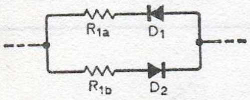
Circuit modifications

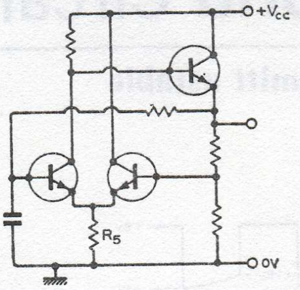
- If R_3 and R_4 are replaced by a potentiometer connected across C_1 with its sliding contact taken to the −V rail, the mark-to-space ratio of the output waveform may be varied without changing its frequency.
- The on-time of Tr_1 is independent of the supply voltages and the on-time of Tr_2 depends on the ratio $+V/[1 - V/-V_{BE(on)}]$. Hence, high frequency stability is obtained if the ratio of the supply voltages is constant. This condition is assured if only a single supply is used as shown left which can provide a frequency stability of 1% for a ±50% change in $+V_{cc}$.
- R_3 and R_4 in the original circuit may be replaced by constant-current tails. Middle circuit shows a pair of parallel current mirrors making the emitter currents of Tr_1 and Tr_2 equal and controlled by R_8, allowing the frequency to be varied without affecting the mark-to-space ratio.
- The constant-current sources may be voltage controlled, by R_9 in the circuit shown right and the currents in Tr_1 and Tr_2 controlled independently by R_3' and R_4' respectively.

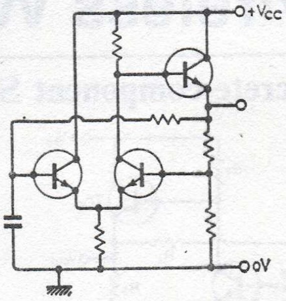
A larger amplitude output, at slower speed, may be obtained by connecting the original output point to the base of a p-n-p transistor with its emitter connected to the +V rail and its collector returned the −V rail through say a 1-kΩ resistor. If this resistor is connected instead to the 0-V line a t.t.l.-compatible output is obtainable using +V = +5V.

Further reading
Beneteau, P. J. and Evangelisti, A., An Improved Emitter-Coupled Multivibrator—SGS-Fairchild application report APP-59, 1963.
Electronic Circuit Design Handbook, TAB Books, 1971, pp. 86/7.

Cross reference
Series 3, card 2.







$R_{4(min)}$ 47Ω (m-s ratio 1/2.8, f ≈ 33kHz), $R_{4(max)}$ 2.2kΩ (V_{out} reduced to 5V pk-pk).
Useful range of R_5 ≈ 220Ω to 47kΩ.
Tr_1 and Tr_2: ME4103, BC107, BC109, 2N3904.
Observe $V_{BE(max)}$ as well as $V_{CE(max)}$ rating.

Circuit modifications

- If R_1 is not too large the p.r.f. only is affected by adjusting the R_1C_1 time constant; this will not be the case when R_1 reaches a value that is comparable with the relatively high resistance discharge path through R_5, Tr_1 base-emitter junction and R_4. Both the p.r.f. and mark-to-space ratio can be made variable by varying the R_3/R_4 potential divider ratio. Resistors R_3 and R_4 can conveniently be made into a continuously-variable potentiometer or R_4 can be made a voltage-variable resistor, e.g. by use of a f.e.t.
- When a small, but controlled, mark-to-space ratio is required R_1 may be replaced by the resistor-diode combination shown left. Both diodes could be of the 1N914 type. The circuit may be synchronized from an external oscillator by resistive coupling to the emitter of Tr_1 or by capacitive coupling to its base.
- Addition of Tr_3, as shown middle, allows the timing of the output square wave to be more nearly controlled by the R_1C_1 time constant. Tr_1 and Tr_3 form a long-tailed pair so that the junction of C_1 and R_1 are effectively connected to one intput of a differential operational amplifier.
- Circuit right shows a similar form of modification which has the merit of allowing V_{out} to swing almost between the levels of the supply rail potentials.

Further reading
SGS-Fairchild: Industrial Circuit Handbook, pp. 48/9, 1967.
Sylvan, T. P., The Unijunction Transistor, Characteristics and Applications, General Electric Co., N.Y., 1965, pp. 52/3.

Cross references
Series 2, cards 2, 7.
Series 8, cards 4, 5 & 12.

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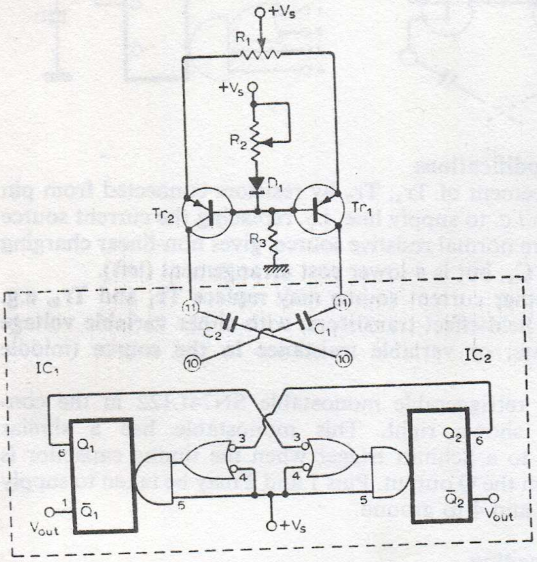
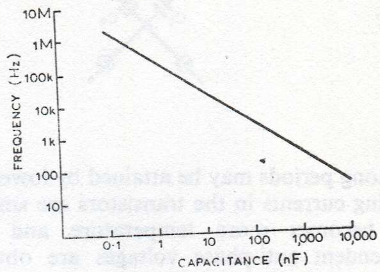
Dual-monostable astable circuit



Typical performance
Supply: +5V, 46.5mA
ICs: SN74121N (monostable)
Tr_1, Tr_2: ME0413;
D: PS101
C_1, C_2: 10nF
R_1: 2kΩ
R_2, R_3: 1kΩ
Frequency: 28.6kHz
Pulse excursion: 0.2 to 3.6V
Rise time: 100ns
Fall time: 50ns



Circuit description
Astable circuits can be constructed out of cross-coupled monostable circuits provided that the output of one monostable can be used to initiate the timing cycle of the other. The circuit shows the interconnection between two t.t.l. monostable i.cs. The timing capacitors for the two parts of the period are C_1 and C_2, and these might be equal or different, depending on the need for unity or other mark-to-space ratios. In place of the resistive part of the timing circuit, Tr_1 and Tr_2 provide constant currents, so that the capacitors charge linearly. This allows a ramp waveform to be extracted at pin 11 on either i.c. It has the further advantage that varying the common potential at the bases of Tr_1 and Tr_2 with R_2 allows both charging currents to be varied simultaneously, i.e. a change in frequency without change in mark-to-space ratio. By varying the tapping point on R_1, the balance between the currents in Tr_1, Tr_2 collectors are changed and the mark-to-space ratio is varied with a relatively small change in total period, i.e. in frequency. Diode D_1 gives temperature compensation for the base-emitter potential changes of Tr_1 and

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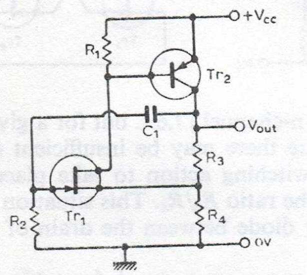
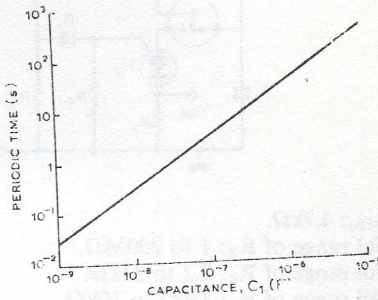
Astable circuit with f.e.t.

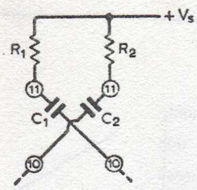


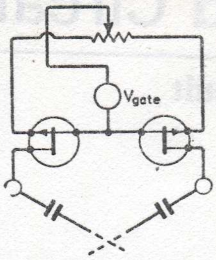
Typical data
Supply: +9V, 760μA
Tr_1: 2N5457;
Tr_2: BC126
R_1: 100kΩ; R_2: 10MΩ
R_3: 3.3kΩ; R_4: 6.8kΩ
C_1: 1nF
P.r.f. 31.2Hz
Mark-to-space ratio: 1.71:1

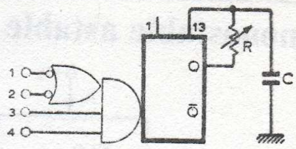


Circuit description
When the supply is connected both active devices conduct with currents determined by the negative feedback due to R_3 and R_4. The collector potential of Tr_2 jumps sharply to a level approaching $+V_{CC}$ and the source of Tr_1 jumps towards the full $V_{CC}\ R_4/(R_3+R_4)$. With C_1 initially uncharged, the full positive step at Tr_2 collector is passed to the gate of Tr_1 so that the gate-source junction becomes forward biased by about 500mV and the charging current flows through it to ground via R_4. The initial charging current in C_1 is thus larger than it would have been if C_1 charged simply through R_2. The p.d. across R_2 falls rapidly as C_1 charges through R_4 causing the f.e.t. junction to be reverse biased and the charging time constant of C_1 to charge to the much larger value of C_1R_2. Capacitor C_1 continues to charge until the gate potential of Tr_1 falls below its source potential by an amount that approaches the pinch-off value causing Tr_2 to switch off due to the reduction of base current.
The output switches back to virtually 0V as C_1 discharges through R_2, R_3 and R_4, where $R_2 \gg R_3 + R_4$, until the gate source p.d. allows sufficient drain current in Tr_1 to switch Tr_2 on and the circuit re-cycles. Due to the low reverse-bias gate current of the f.e.t., long time intervals can be obtained between the changes of state using reasonable component values, provided that C_1 is a low-leakage type. The accuracy of these long time intervals however depends on ill-defined value of the pinch-off voltage of the f.e.t.

Component changes
Useful range of supply: +6 to +30V.
Useful range of C_1: 10pF to 100μF, low-leakage type.







Tr_2. Long periods may be attained by lowering R_2 so that the charging currents in the transistors are small, but the period then becomes more temperature and supply sensitive. Independent anti-phase voltages are obtainable at the Q outputs of the two i.cs without any loading effects on the interconnection circuitry.

Component changes

With C_1, C_2: 10μF and minimum setting of R_1, frequency is 1.6Hz. With C_1, C_2: 10nF, and maximum setting of R_1, mark-to-space ratio is variable from 0.03 to 0.98.

Frequency stability within $\pm 3\%$ for a supply change of ± 0.5 on 5V.

Resistive loading may be reduced to 2.2kΩ to maintain pulse height within 90% of maximum level. Absolute minimum load 150Ω where pulse level is then down to 1.9V.

For fixed capacitance, frequency range roughly 10/1 by varying R_1.

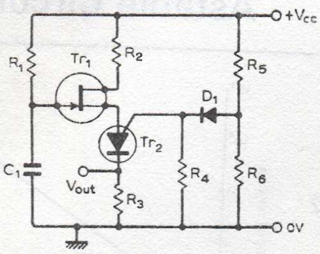
Circuit modifications

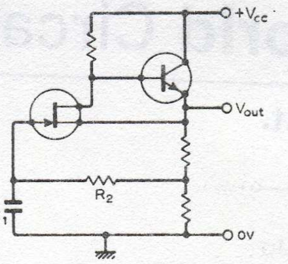
- Replacement of Tr_1, Tr_2 by resistors connected from pin 11 on each i.c. to supply line, i.e. replacing the current source by the more normal resistive source, gives non-linear charging of C_1 and C_2, but is a lower cost arrangement (left).
- Any other current source may replace Tr_1 and Tr_2, e.g. p-channel field-effect transistors, with either variable voltage on the gate, or variable resistance in the source (middle circuit).
- Use a retriggerable monostable SN74L122 in the configuration shown right. This monostable has a similar behaviour to a Schmitt trigger when the timing capacitor is driven from the Q output. Pins 1 and 2 may be taken to supply line and 3 and 4 to ground.

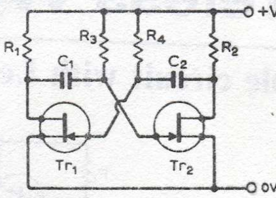
Further reading

Photo-f.e.ts make multivibrator respond to incident light, in 400 Ideas for Design, vol. 2, Hayden, 1971, p.107.

Smith, D. T., Multivibrators with seven-decade range in period, *Wireless World*, Feb. 1972, pp. 85/6.







$R_{1(min)}$: 4.7kΩ.
Useful range of R_2: 1 to 200MΩ.
Useful range of R_3: 2.2 to 33kΩ.
Useful range of R_4: 330Ω to 10kΩ.
Minimum load resistance: 220Ω.
Frequency stability: $+1\%$/V increase in V_{CC}.

Circuit modifications

- Another circuit that can produce output pulses separated by a long time interval is shown left. When the supply is connected, the low-leakage capacitor C_1 charges through R_1 until the gate potential of the n-channel j.f.e.t. reaches the threshold voltage of the programmable unijunction transistor Tr_2 minus $V_{GS(off)}$ of Tr_1. On reaching this gate voltage of $+V_{CC}R_6(R_5+R_6-V_{GS(off)})$, the gate-source junction of Tr_1 becomes forward biased and C_1 discharges through it to ground via Tr_2 and R_3 providing an output pulse across R_3. Transistor Tr_1 then cuts off and the charge-discharge cycle of C_1 is repeated.
- Caution is necessary in replacing bipolar junction transistors, in circuits that are known to work by field-effect transistors. In the middle circuit Tr_1 of a Schmitt astable has been changed to an n-channel j.f.e.t. but for a given pinch-off voltage and R_1-value there may be insufficient drain-source p.d. to allow the switching action to take place, except by critically adjusting the ratio R_3/R_4. This situation is improved by inserting a zener diode between the drain of Tr_1 and the base of Tr_2.
- Circuit right shows a cross-coupled astable where n-p-n transistors have been replaced with n-channel j.f.e.ts. This circuit will not switch unless R_3 and R_4 are returned to ground instead of $+V_{CC}$ and should be returned to a slightly negative rail to ensure self-starting.

Further reading

FET and UJT provide timing over a wide temperature range, in 400 Ideas for Design, Hayden, 1971, pp. 192/3.

Watson, J., Introduction to Field Effect Transistors, Siliconix, 1970.

Cobbold, R. S. C., Theory and Applications of Field Effect Transistors, Wiley, 1970.

Cross references

Series 8, cards 2, 5 & 10.